A CMOS 15-bit 125-MS/s Time-Interleaved ADC With Digital Background Calibration

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***Abstract*—A 15-bit 125-MS/s two-channel time-interleaved pipelined ADC is fabricated in a 0.18 μm CMOS technology, and achieves 91.9 dB SFDR, 69.9 dB SNDR for a 9.99 MHz input. This ADC incorporates a single sample-and-hold amplifier which employs a precharged circuit configuration to mitigate performance requirements for its opamp. Digital background calibration is applied to maintain the conversion linearity of each A/D channel and also correct both gain and offset mismatches between the two channels. Excluding I/O buffers, the chip occupies an area of 4.3×4.3 mm^2 and dissipates 909 mW from a 1.8 V supply.**

***Index Terms*—Analog–digital conversion, calibration, sample and hold circuits.**

I. Introduction

NYQUIST-RATE analog-to-digital converters (ADCs) of more than 12-bit resolution have been predominantly realized using the pipelined analog-to-digital conversion (A/D) architecture. In switched-capacitor pipelined ADCs, the linearities of sample-and-hold amplifiers and pipeline stages are ensured by using high-gain opamps with capacitor feedback. Pipelined ADCs of more than 14-bit resolution can be achieved by incorporating digital calibration (either foreground or background) to mitigate the requirements for device matching and opamps' DC gain [1]–[3]. The maximum sampling rate of a pipelined ADC is mainly determined by the achievable operating speed of its internal high-gain opamps.

The time-interleaved (TI) architecture which contains more than one A/D channels to share the conversion operations can overcome the speed limitation imposed by their internal circuit blocks [4]. However, the overall accuracy of a TI ADC can be degraded by the gain, offset, and sampling phase mismatches among its A/D channels. Many calibration techniques have been developed to correct the A/D errors caused by these mismatches. To take advantage of low-cost digital circuits in scaled CMOS technologies, there are calibration schemes that can execute the calibration procedures continuously in the background, while requiring no external reference signals or extra A/D channels [5], [6]. These schemes are able to extract mismatch information directly from the ADC's digital outputs. These techniques usually involve complicated signal processing in the digital domain. They also impose certain requirements on the ADC's input signal, e.g., it must be band-limited and asynchronous with the ADC's sampling clock.

In this paper, we present a 15-bit 125-MS/s CMOS TI ADC which consists of two pipelined A/D channels. This ADC incorporates a single sample-and-hold amplifier (SHA) to avoid sampling phase mismatch. The SHA uses a precharged circuit configuration to mitigate the performance requirements for its opamp which has to operate at a maximum clock rate of 125 MHz. Digital background calibration is employed to maintain the conversion linearity of each A/D channel and also correct both gain and offset mismatches between the two channels. The calibration is proceeded continuously in the background without interrupting the normal A/D operations. The calibration schemes incorporated in this ADC are robust since they do not rely on input signal condition. The ADC chip was fabricated in a 0.18 μm 1P6M CMOS technology with MIM capacitors, and operates under a single 1.8 V supply.

The rest of this paper is organized as follows. Section II describes the overall architecture of this ADC. Section III details the design of the SHA. Section IV briefs the design of the pipeline stage under calibration and its operation principles. Section V describes the ADC's digital functional blocks for output encoding and correction. Section VI presents the experimental results of this ADC prototype. Section VII draws conclusions. Finally, an appendix provides theoretical study of opamp requirements for the SHA.

II. ADC Architecture

Fig. 1 shows the block diagram of the TI ADC. It consists of a single sample-and-hold amplifier (SHA) and two identical pipelined A/D channels. The use of a single SHA can avoid any sampling skew error. The offset and gain mismatch between the two A/D channels are corrected in the back-end digital domain. The final digital output is obtained by multiplexing the outputs from the two A/D channels.

Two random choppers, CHP1 and CHP2, are placed in front of the two A/D channels respectively to time interleave the SHA's outputs and also enable offset calibration [5]. The choppers are controlled by a binary-valued random sequence, q_c.

Each A/D channel consists of 17 radix-2 1.5-bit switched-capacitor (SC) pipeline stages and a final 2-bit flash stage. The pipeline employs a correlation-based digital background calibration scheme to achieve high linearity [2]. A q random sequence is injected into the pipeline to facilitate the pipeline calibration. Normally, 15 stages are sufficient to generate an effective 15-bit resolution in this design. Three extra stages are added to obtain more resolution when perform calibration

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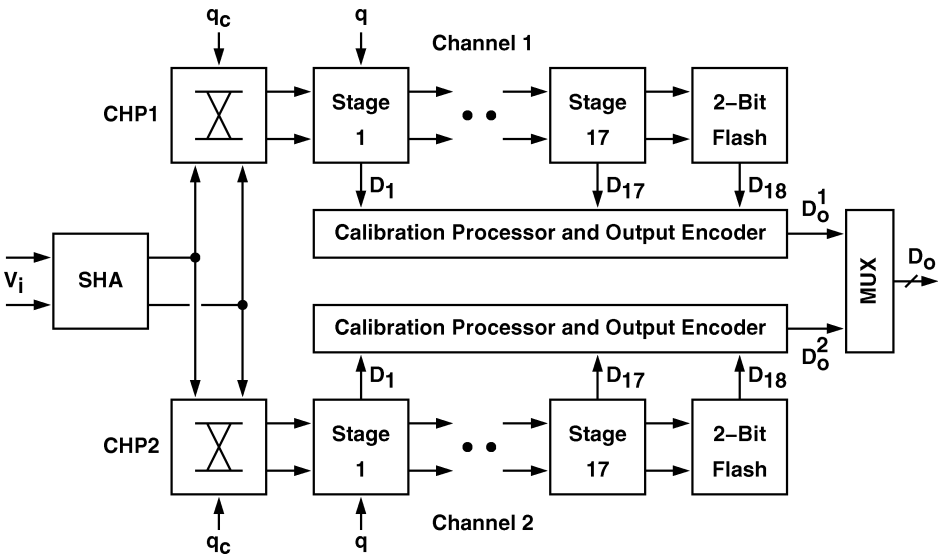

Fig. 1. Time-interleaved pipelined ADC with single SHA.

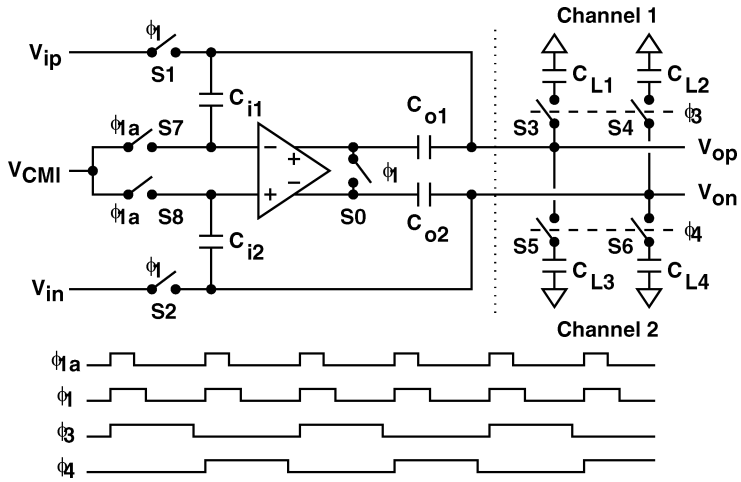

Fig. 2. Precharged sample-and-hold amplifier (PC-SHA).

measurement, and to reduce truncation errors in the digital calibration logic.

III. Sample-and-Hold Amplifier (SHA)

A single SHA is used in this TI ADC. Unlike the following A/D channels, the SHA is required to operate at the ADC's full sampling rate. To mitigate opamp's performance requirements, the SHA in this design is based on a precharge scheme [7], which is briefed in Section III-A. The original design is sensitive to output network mismatch. Thus, a modified design was adopted and described in Section III-B. The SHA's circuit design is covered in Section III-C.

A. Precharged SHA (PC-SHA)

Fig. 2 shows the schematic of a precharged SHA (PC-SHA) [7]. In this SHA, the ϕ_1 and ϕ_{1a} clocks control the operation of the SHA, while the ϕ_3 and ϕ_4 clocks demultiplex the SHA's outputs to one of the A/D channels. During the ϕ_3 sample mode ($\phi_3 = 1$ and $\phi_1 = 1$), the input not only drives the C_{i1} and C_{i2} sampling capacitors but also precharges the SHA's output nodes, including the input capacitive loadings of A/D channel 1, C_{L1} and C_{L2}. During the ϕ_4 sample mode ($\phi_4 = 1$ and $\phi_1 = 1$), the input capacitive loadings of A/D channel 2, C_{L3} and C_{L4}, are precharged instead. During the sample-mode period, the opamp's outputs are equalized by the S0 switch, thus, the two output coupling capacitors, C_{o1} and C_{o2}, are added.

The PC-SHA's steady-state output in the hold mode ($\phi_1 = 0$) can be expressed as

$$V_o \approx V_i \left[1 + \frac{1}{A_0}\left(\frac{V_{co}}{V_i} - 1\right) + \frac{1}{A_0}\frac{C_L}{C_o}\left(\frac{V_{cl}}{V_i} - 1\right)\right] \quad (1)$$

where A_0 is the opamp's DC voltage gain, V_i, V_{co} and V_{cl} are the sampled voltages stored on C_i, C_o and C_L respectively during the preceding sample mode. Equation (1) shows that the combination of precharging and output capacitor coupling reduces the opamp's DC gain requirement. The voltage difference between V_i and V_{co} and the difference between V_i and V_{cl} are mainly due to the time difference between the falling edges of ϕ_1 and ϕ_{1a}. For bottom-plate sampling, the ϕ_{1a} clock turns off the switches

under its control before the ϕ_1 clock does. In this case, it is desirable to make the time difference between ϕ_1 and ϕ_{1a} small so that $V_{co}/V_i \approx 1$ and $V_{cl}/V_i \approx 1$. When the SHA is switched from the sample mode to the hold mode, the voltage changes at the opamp's output can be expressed as

$$\Delta V_{o,op} = V_i \left[\left(1 - \frac{V_{co}}{V_i} \right) + \frac{C_L}{C_o} \left(1 - \frac{V_{cl}}{V_i} \right) \right]. \quad (2)$$

Thus, the combination of output capacitor coupling and precharging also reduces the opamp's output voltage swing requirement, which leads to lower distortion.

The time constant for a PC-SHA to settle during the hold mode is larger than that for a traditional flip-around SHA. However, the overall settling time for a PC-SHA is shorter, since it takes less number of time constant for the opamp to reach the voltage change of (2) if $V_{co}/V_i \approx 1$ and $V_{cl}/V_i \approx 1$ [7]. If a maximum slew rate for the opamp's outputs is imposed, the PC-SHA's settling time advantage is even greater, since its reduced output swing also mitigates the slew-rate effect.

The precharge operation is to preset the SHA's outputs, V_{op} and $V_{\rm on}$, close to their respective final values in the succeeding hold-mode period, thus relaxing the performance specifications for the opamp. For a single-channel pipelined ADC, extra time period has to be allocated for the precharging operation. However, in a two-channel TI ADC system, the SHA's precharge phase and the succeeding hold phase constitute only the sample phase for either one A/D channel, thus no extra time slot is needed.

B. Buffered-Precharged SHA (BP-SHA)

However, the PC-SHA's linearity can be degraded by the mismatches between the S3-S4 output network and the S5-S6 output network. Fig. 3 shows the PC-SHA's single-ended circuit configuration during the sample mode and the hold mode. The S3 and S5 switches are modeled as two voltage-controlled resistors, R_{S3} and R_{S5}. During the ϕ_3 sample phase, the R_{S3}-C_{L1} network is connected to the V_o node. During the ϕ_4 sample phase, the R_{S5}-C_{L3} network is connected to the V_o node. If there are mismatches between the R_{S3}-C_{L1} and R_{S5}-C_{L3} networks, the V_i-to-V_o frequency response is varied due to different output loading, as the SHA alternating between the ϕ_3 and ϕ_4 phases. Furthermore, when the SHA is being switched from the sample mode to the hold mode, charges are injected into the V_o node with the S1 switch being turned off. If there are mismatches between the R_{S3}-C_{L1} and R_{S5}-C_{L3} networks, the V_o changes due to charge injection in the ϕ_3 phase is different from that in the ϕ_4 phase.

A single-ended PC-SHA similar to the circuits of Fig. 3 is simulated, in which the input is a single-tone signal at $f_{\rm in}$ frequency. The effect of output network variation in the ϕ_3 and ϕ_4 phases is manifested as a spurious tone at $f_s/2 - f_{\rm in}$ frequency in the output, where f_s is the sampling frequency. Fig. 4 shows the magnitude of this spurious tone relative to the $f_{\rm in}$ signal in the output. It is assumed that the opamp is ideal, $f_s = 125$ MHz, $f_{\rm in} = 60.9$ MHz, $C_i = 4$ pF, $C_o = 6$ pF, $R_{S3} = (1+\varepsilon_R/2)R$, $R_{S5} = (1-\varepsilon_R/2)R$, $C_{L1} = (1+\varepsilon_C/2)C$ and $C_{L3} = (1-\varepsilon_C/2)C$, where $R = 60\,\Omega$ and $C = 4$ pF. The S1 switch is realized with a 0.18 μm n-channel MOSFET with $W = 64$ μm and $L = 0.18$ μm. A constant-V_{gs} bootstrapping circuit is used for S1 gate control [8]. The mismatches between the R_{S3}-C_{L1} and R_{S5}-C_{L3} networks are represented by ε_R and ε_C. It is required that $\varepsilon_R < 0.001$ and $\varepsilon_C < 0.001$ in order to reduce this spurious tone to less than -85 dB.

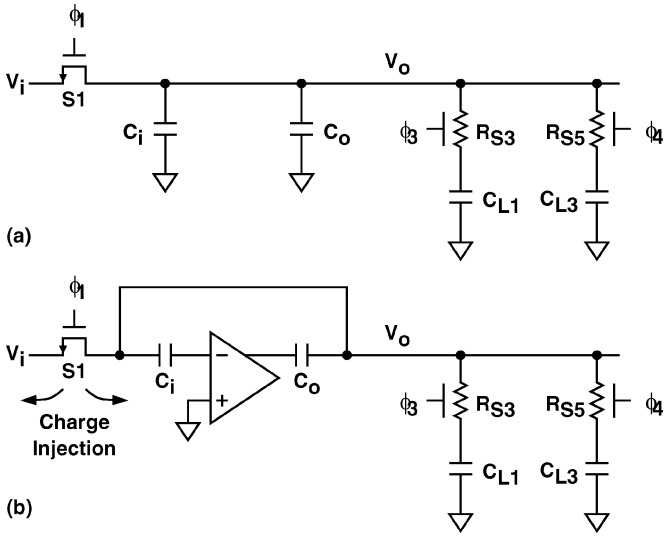

Fig. 3. Simplified PC-SHA circuit models. (a) Sample-mode circuit model. (b) Hold-mode circuit model.

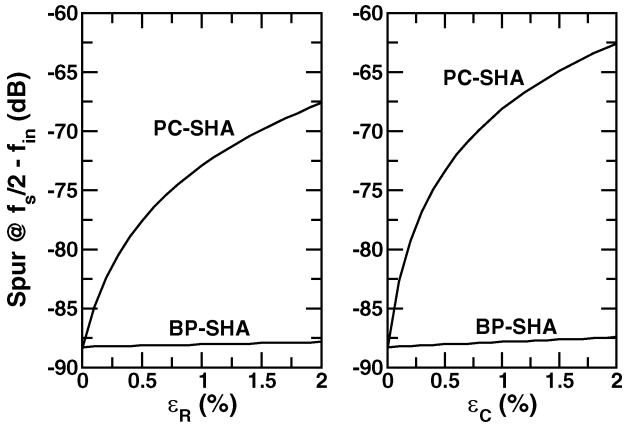

Fig. 4. Spurious-tone simulation results for PC-SHA and BP-SHA at various mismatches.

To mitigate the above mismatch effects, the buffered-precharged SHA (BP-SHA) shown in Fig. 5 is proposed for this ADC design. Two unity-gain buffers, B1 and B2, are added so that the V_i-to-V_o frequency response can remain the same during either the ϕ_3 sample phase or the ϕ_4 sample phase. By inserting the S5 and S6 switches, the charge injection from the S1 and S2 switches can no longer affect the final V_o output in the hold mode. The charge injections from the additional S5 and S6 switches as well as mismatches between the output multiplexer networks have little effect on the final V_o value during the hold mode. Also shown in Fig. 5 are the CHP1 and CHP2 choppers previously shown in Fig. 1. This SHA samples the input using the ϕ_1 clock at sampling frequency $f_s = 125$ MS/s. Each chopper consists of 4 analog switches controlled by either the ϕ_3 or ϕ_4 clocks with a frequency at $f_s/2$. The polarity of the choppers' outputs is controlled by a

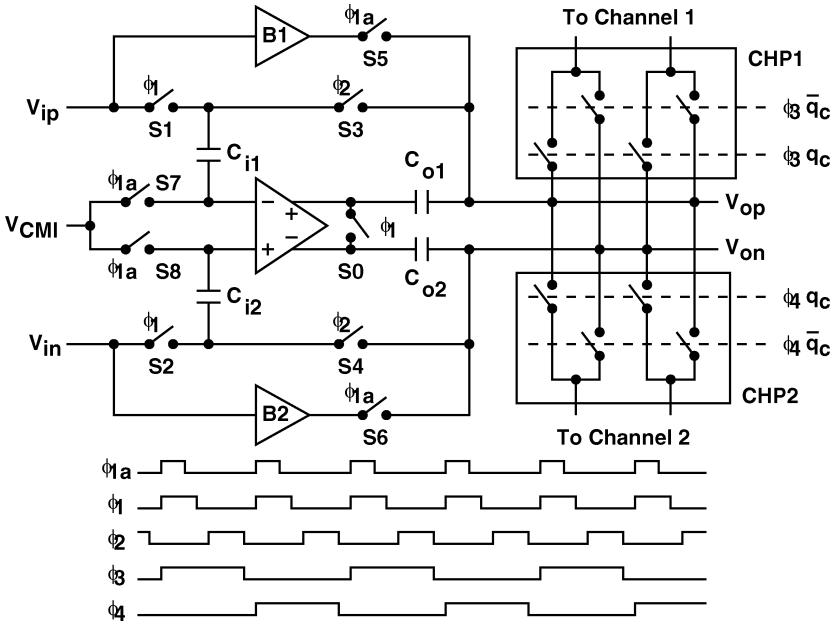

Fig. 5. Buffered-precharged SHA (BP-SHA) with CHP1 and CHP2 choppers.

q_c binary random sequence alternating between 1 and 0. Both S1 and S2 switches are constant-V_{gs} bootstrapped switches [8], which can reduce the distortion of the input sampling network.

C. SHA Circuit Design

Fig. 6 shows the schematic of the SHA's core opamp. The fully differential two-stage configuration consists of a telescopic first stage followed by a common-source second stage. The C_{c1} and C_{c2} capacitors provide conventional current-buffering Miller compensation [9]. The C_{c3} and C_{c4} capacitors are added to improve gain margin [10]. Two separate switched-capacitor common-mode feedback circuits are used to generate control voltages V_{cf1} and V_{cf2} for the first and second stages of the opamp. The input common-mode voltage is set to 0.95 V, and the output common-mode voltage is set to 1.15 V. The opamp can provide a differential output voltage range of 1.9 V. The overall DC voltage gain of the opamp is more than 90 dB. The opamp dissipates 100 mW of power and achieves a unity-gain frequency of 1.66 GHz when capacitors are $C_i = 4$ pF, $C_o = 6$ pF, and $C_L = 4$ pF.

Fig. 7 shows the schematic of the B1 and B2 unity-gain buffers. It is a simple single-stage amplifier with an open-loop DC voltage gain of 32 dB. Each buffer dissipates 13 mW of power while driving a total output capacitive load of 7 pF, while delivering a unity-gain frequency of 2.3 GHz and a slew rate of 1 V/nsec. The behavior of this buffer may deviate from an ideal one due to offset and low open-loop voltage gain of the amplifier. This non-ideal buffer behavior is not crucial in determining the final SHA's output in the hold mode, but the deviation results in a less accurate precharge operation. As manifested in (1), poor precharge operation increases the values of $|V_{co} - V_i|$ and $|V_{cl} - V_i|$, and demands an increase in the opamp's voltage gain, A_0, to maintain the SHA's linearity. A poor precharge operation also dictates a larger opamp's output change in the hold mode than the $\Delta V_{o,op}$ of (2), which may lead to a longer hold-mode settling time.

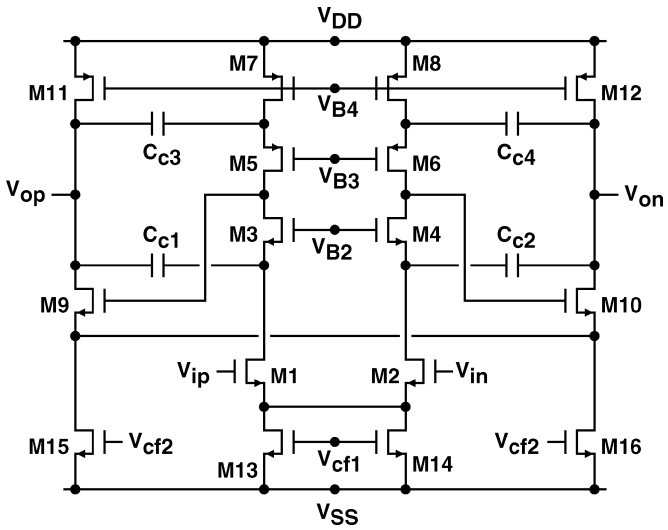

Fig. 6. Operational amplifier of the SHA.

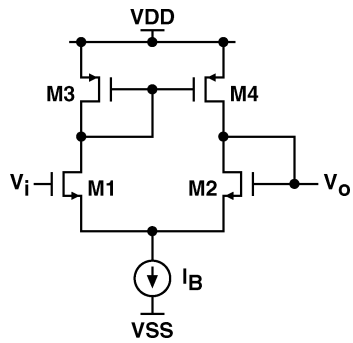

Fig. 7. Unity-gain buffer of the SHA.

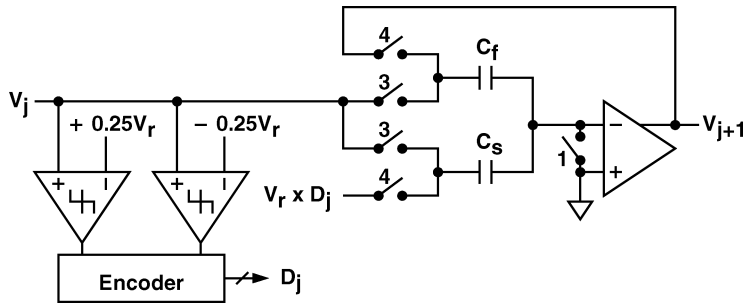

Fig. 8. Radix-2 1.5-bit switched-capacitor pipeline stage.

Fig. 4 also shows the spurious-tone simulation results for a BP-SHA. Simulation condition is similar to the PC-SHA simulation case. The circuit of Fig. 7 is directly used as an unity-gain buffer. As clearly shown in Fig. 4, the BP-SHA is almost immune to both ε_R and ε_C mismatches.

The overall transconductance (G_m) and DC gain (A_0) requirements for BP-SHA's core opamp and buffers can be found in the Appendix. This theoretical study shows that there are G_m and A_0 trade-offs between the core opamp and buffers. By choosing a proper precharge error, α, defined in the Appendix, it is possible to find a optimal design with minimal power consumption. However, optimal design was not pursued in this design due to design time constrain. The core opamp was modified from a flip-around SHA (FA-SHA) design. Speed was enhanced by pushing non-dominant poles to higher frequencies. This was made possible by the relaxing specifications for slew rate and output voltage range.

It is difficult and beyond the scope of this paper to theoretically compare the performance between a BP-SHA and a FA-SHA. The G_m and A_0 requirements for FA-SHA's opamp can also be found in the Appendix. From our own experience, the FA-SHA's speed is greatly limited by the demand of both high A_0 and large output voltage range. The speed cannot be further increased by simple device scaling due to phase margin consideration. Using similar opamp, we were able to design a BP-SHA with better speed performance.

IV. Pipeline Stage

Fig. 8 shows the single-ended version of a radix-2 1.5-bit switched-capacitor (SC) pipeline stage as the jth stage of a pipelined ADC. When $\phi_3 = 1$, V_j is sampled onto capacitor C_f and C_s. The digital code, $D_j \in \{-1, 0, +1\}$, is obtained by comparing V_j with $+0.25V_r$ and $-0.25V_r$. When $\phi_4 = 1$, the output V_{j+1} can be written as

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j) - V_j^{\mathrm{os}}\right] \tag{3}$$

with

$$\hat{G}_j = \frac{C_s + C_f}{C_f} \times \frac{1}{1 + \frac{1}{A_0} \cdot \frac{C_s + C_f + C_p}{C_f}} \tag{4}$$

and

$$\hat{V}_j^{\mathrm{da}}(D_j) = V_r \cdot \frac{C_s}{C_s + C_f} \times D_j \tag{5}$$

where C_p denotes the parasitic capacitance associated with the opamp's negative input, and A_0 is the opamp's DC voltage gain. The V_j^{os} term accounts for the offset effect of the jth stage, including opamp's input-referred offset voltage and charge injection from analog switches. For the ideal case, we have $C_s = C_f$ and $A_0 = \infty$, thus the ideal stage gain is $G_j = 2$, and the nominal voltage range for both stage's input and output is $\pm 0.5V_r$.

Calibration of the jth stage is to measure

$$R_j(D_c) = \hat{G}_j \times \hat{V}_j^{\mathrm{da}}(D_c) \tag{6}$$

where $D_c \in \{-1, 0, +1\}$. Fig. 9 shows a modified pipeline stage that facilitates background calibration [2]. The schematic is identical to that of Fig. 8, except that the C_s capacitor is split into N equal fragments. Thus, we have $C_s = \sum_{i=1}^{N} C_{s,i}$. When $\phi_4 = 1$, all the C_s capacitors are connected to $D_j \cdot V_r$, except the $C_{s,i}$ capacitor which is connected to $q \cdot V_r$. The q signal is a digital binary-valued sequence generated from a pseudo random generator. To measure $R_j(+1)$, the value of q alternates between $+1$ and 0. To measure $R_j(-1)$, q alternates between -1 and 0.

Fig. 10 shows the scheme of digital background calibration. The V_{j+1} output of the jth pipeline stage is digitized by a backend z-ADC with a corresponding D_z digital output. The z-ADC comprises of the $(j+1)$th, $(j+2) - \mathrm{th}, \ldots$, pipeline stages. With injection of the q signal, V_{j+1} becomes

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j) - V_j^{\mathrm{os}}\right] + R_{j,i}(D_j) \times D_j - R_{j,i}(q) \times q \tag{7}$$

where

$$R_{j,i}(D_c) = R_j(D_c) \times \frac{C_{s,i}}{C_s}. \tag{8}$$

The last two terms in (7) are due to q injection. Assume the z-ADC has a linear transfer characteristic, then V_{j+1} can be denoted as

$$V_{j+1} = \frac{G_z}{\hat{G}_z} \times D_z + O_z + Q_z. \tag{9}$$

The z-ADC has a gain error of $G_z/\hat{G}_z$, an offset of O_z and a quantization error of Q_z. Here, G_z represents the specified stage gain and $\hat{G}_z$ is the realized stage gain. The z-ADC's output, D_z, is correlated with a q' random sequence and then integrated on an accumulator. The q' signal has the same waveform pattern

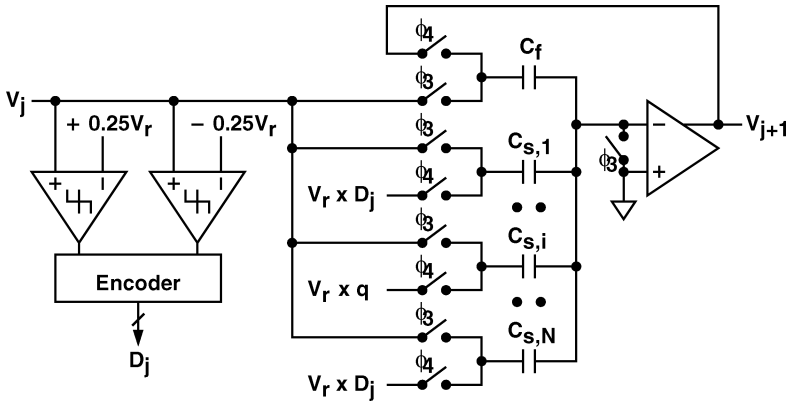

Fig. 9. Modified pipeline stage for background calibration.

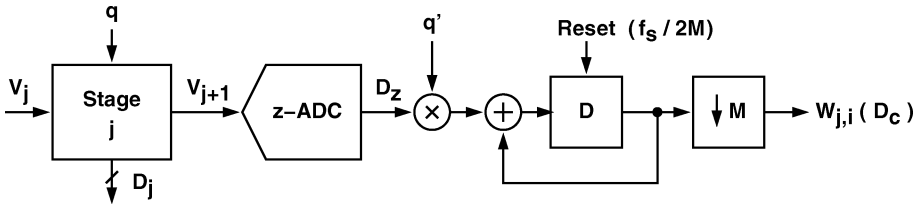

Fig. 10. Background calibration of pipeline stage.

as the q sequence but alternates between $+1$ and -1. The accumulator's output, $W_{j,i}(D_c)$, is taken only after M cycles of integration, where M is the period of the q pseudo-random sequence. In one M period, the q' sequence needs to have equal number of $+1$ and -1. The down-sampled $W_{j,i}(D_c)$ output can be expressed as

$$W_{j,i}(D_c) = \frac{\hat{G}_z}{G_z} \times R_{j,i}(D_c). \tag{10}$$

In summary, $W_{j,i}(+1)$ is extracted by letting $q \in \{0, +1\}$ and connecting q to the $C_{s,i}$ capacitor of the jth pipeline stage, $W_{j,i}(-1)$ is extracted by letting $q \in \{0, -1\}$. The value of $W_{j,i}(0)$ can be preset to 0. Additional calibration data, $W_j(D_c)$, are calculated by using

$$W_j(D_c) = \sum_{i=1}^{N} W_{j,i}(D_c). \tag{11}$$

Note that $W_j(D_c)$ represents the magnitude of $R_j(D_c)$ measured by the z-ADC, and $W_{j,i}(D_c)$ represents the magnitude of $R_{j,i}(D_c)$ measured by the z-ADC, To calibrate one pipeline stage, a total of $2 \times N \times M$ samples are required since $i = 1, 2, \ldots, N$ and $D_c = -1, +1$.

Fig. 11 shows a pipelined ADC model. In this model, the V_{j+1} analog output of the jth stage is digitalized by the following back-end stages (z-ADC) which return the $D_{o,j+1}$ (D_z) digital code. Once the jth stage is calibrated and all calibration data are collected, including $W_{j,i}(D_c)$ and $W_j(D_c)$ for all i and D_c, the $D_{o,j}$ is encoded as

$$D_{o,j} = \frac{1}{G_j}\left[W_j(D_j) + D_{o,j+1} - W_{j,i}(D_j) \times D_j + W_{j,i}(q) \times q\right]. \tag{12}$$

The last two terms on the right-hand side of (12) are required to remove the calibration signals introduced by q, which manifest as the last two terms in (7). To reconfigure the jth stage into a normal pipeline stage without q injection, one can simply let $q = D_j$ and encodes $D_{o,j}$ as

$$D_{o,j} = \frac{1}{G_j}\left[W_j(D_j) + D_{o,j+1}\right]. \tag{13}$$

With either (12) or (13) the relationship between $D_{o,j}$ and V_j can be expressed as

$$V_j = \frac{G_j G_z}{\hat{G}_j \hat{G}_z} \times D_{o,j} + \frac{Q_z}{\hat{G}_j} \tag{14}$$

where G_j is the nominal gain of the jth pipeline stage. Equation (14) shows that $D_{o,j}$ is indeed a digital representation of V_j. The overall quantization error is reduced by the G_j stage gain. Offset is neglected since it does not affect nonlinearity.

In this ADC design, only the first six stages in each A/D channel are subjected to background calibration, and adopt the circuit configuration of Fig. 9. The number of C_s fragments is four, i.e., $N = 4$. The remaining pipeline stages have the circuit configuration of Fig. 8. In each A/D channel, the first six stages are implemented with identical capacitors and opamps. The nominal values of the capacitors are $C_f = 2$ pF and $C_s = 2$ pF. The opamps are similar to the one shown in Fig. 6, and each consumes 47 mW of power. The opamps and capacitors are scaled by half in the next five stages. Another scaling by half is applied to the remaining stages. This ADC prototype was not optimized for minimum power consumption.

V. ADC Output Encoding and Correction

Fig. 12 shows the digital output encoding and correction block diagram for each A/D channel. The calibration pro-

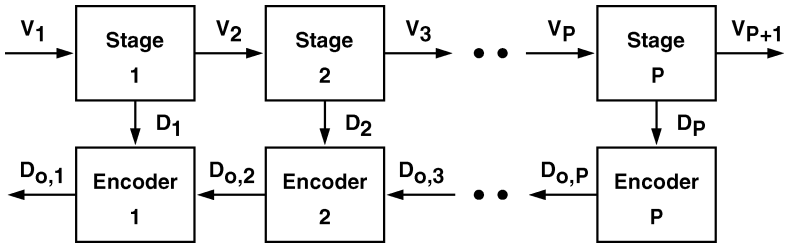

Fig. 11. Pipelined ADC model.

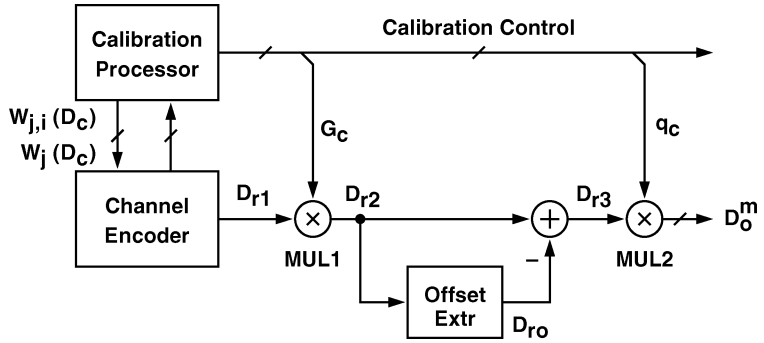

Fig. 12. Digital output encoding and correction.

cessor (CP) executes the calibration procedures described in Section IV, updating $W_{j,i}(D_c)$ and $W_j(D_c)$ calibration data constantly. To achieve 15-bit accuracy, the period of the q pseudo-random sequence is chosen to be $M = 2^{28}$ [2]. Assume there are P pipeline stages in each A/D channel, and only the first K stages are subjected to calibration. For pipeline stages with $j > K$, we can simply choose $W_j(D_c) = D_c$ where $D_c \in \{-1, 0, +1\}$. Calibration is preceded backward and sequentially while the ADC performing its normal A/D conversion. Referring to Fig. 11, we calibrate the Kth stage first using q injection. Both $W_{K,i}(D_c)$ and $W_K(D_c)$ calibration data are extracted from $D_{o,K+1}$. Then, we calibrate the $(K-1)$th stage and extract both $W_{K-1,i}(D_c)$ and $W_{K-1}(D_c)$ data from $D_{o,K}$. The procedure continues toward the first stage to complete one calibration cycle. The encoder in each pipeline stage uses either (12) or (13) to generate $D_{o,j}$.

The D_{r1} channel encoder output in Fig. 12, represents the $D_{o,1}$ digital code in Fig. 11. By applying (14) recursively and neglecting q and offset, D_{r1} can be expressed as

$$V_1 = \frac{G_1 G_2 \cdots G_P}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_P} \times D_{r1} + \frac{V_{P+1}}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_P} \tag{15}$$

with

$$D_{r1} = D_{o,1} = \sum_{j=1}^{P} \frac{W_j(D_j)}{G_1 G_2 \cdots G_j}. \tag{16}$$

The last term in (15) is the quantization error of the overall A/D conversion.

Fig. 12 also contains operations to equalize both conversion gains and offsets of the two A/D channels. The CP generates a gain correction factor, G_c. using the $W_j(D_c)$ calibration data. The normalized D_{r2} signal is obtained by multiplying D_{r1} with G_c. The V_1-to-D_{r2} conversion gains for both A/D channels are then equalized. The overall DC offset of the A/D channel, D_{ro}, is extracted from D_{r2}. The D_{r3} signal is the D_{r2} signal with its DC offset removed. Finally, the single channel output, D_o^m where $m \in \{1, 2\}$, is obtained by unscrambling D_{r3} with the q_c sequence.

The following subsections provide more details on gain correction and offset extraction.

A. Gain Correction

The gain correction assumes the fact that all pipeline stages have the same basic configuration of Fig. 8, and share identical V_r reference voltage. From (4), (5), and (6), $R_j(D_c)$ can be rewritten as

$$\begin{aligned} R_j(D_c) &= V_r \times D_c \times \left(\hat{G}_j - \frac{1}{1+\mu_j}\right) \\ &\approx V_r \times D_c \times \left(\hat{G}_j - 1 + \mu_j\right) \end{aligned} \tag{17}$$

where $\mu_j = (1/A_0)[(C_s + C_f + C_p)/C_f]$. From (15), (16), and (17), neglecting quantization error, and letting D_j for all j have the same value, i.e., $D_j = D_s$, we have

$$V_1 = \frac{G_1 G_2 \cdots G_P}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_P} \times \sum_{j=1}^{P} \frac{W_j(D_s)}{G_1 G_2 \cdots G_j} \tag{18}$$

$$= \sum_{j=1}^{P} \frac{R_j(D_s)}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_j} \tag{19}$$

$$= D_s V_r \left(1 - \frac{1}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_P} + \sum_{j=1}^{P} \frac{\mu_j}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_j}\right). \tag{20}$$

The above equation shows that a D_{r1} digital code with $D_j = +1$ for all j is to represent a V_1 analog input close to $+V_r$. On the other hand, a D_{r1} digital code with $D_j = -1$ for all j is to

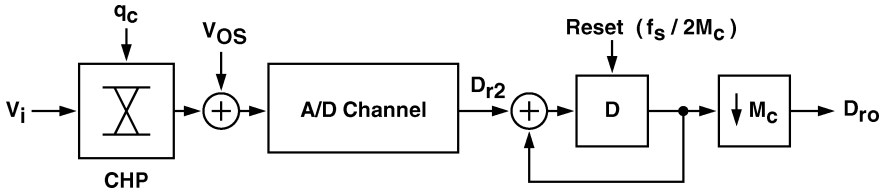

Fig. 14. Offset extraction signal-flow diagram.

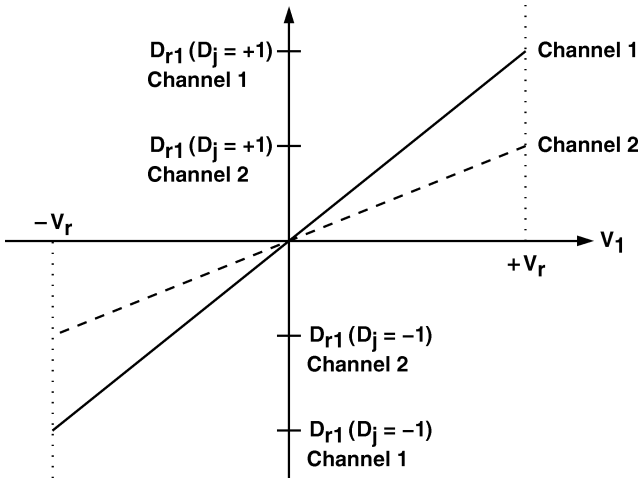

Fig. 13. V_1 to D_{r1} transfer functions.

represent a V_1 analog input close to $-V_r$. This statement is true regardless of the value of $R_j(D_c)$.

Fig. 13 illustrates the V_1 to D_{r1} transfer functions for two A/D channels with different conversion gains. To equalize the conversion gains, the G_c gain correction factor can be chosen as

$$G_c = \frac{\Delta V_1}{\Delta D_{r1}}. \tag{21}$$

Then, the same D_r code range covers the same V_1 voltage range. From (20) with $D_s = +1$ and $D_s = -1$, the required G_c can be expressed as

$$G_c = \frac{2}{\sum_{j=1}^{P} \frac{W_j(+1)}{G_1 G_2 \cdots G_j} - \sum_{j=1}^{P} \frac{W_j(-1)}{G_1 G_2 \cdots G_j}} \times (1+\varepsilon_g) \tag{22}$$

where ε_g is

$$\varepsilon_g = -\frac{1}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_P} + \sum_{j=1}^{P} \frac{\mu_j}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_j}. \tag{23}$$

Since, $G_j = 2$ for all j in this design, the CP in Fig. 12 calculates the G_c gain correction factor using

$$G_c = \frac{2}{\sum_{j=1}^{P} \frac{W_j(+1)}{2^j} - \sum_{j=1}^{P} \frac{W_j(-1)}{2^j}}. \tag{24}$$

To achieve 15-bit accuracy, it requires that $\varepsilon_g < 2^{-15}$. Since $P = 17$ in this ADC design, ε_g is dominated by the last term in (23). Furthermore, assume all pipeline stages are identical and $C_s = C_f$, $C_p = 0$, then $\hat{G}_j = 2/(1+\mu)$ where $\mu = 2/A_0$ and ε_g can be simply approximated by $\varepsilon_g \approx \mu$. Thus, to achieve 15-bit accuracy, we want $\mu < 2^{-15}$, i.e., the DC gain of the opamps must be larger than 2^{16} or 96 dB. For this TI-ADC design, only the ε_g mismatch between the two channel can become A/D error, the DC gain requirement for the opamps is lessened.

B. Offset Extraction

Fig. 14 shows the signal-flow diagram for offset extraction, which is similar to the scheme employed in [11] and [5]. Since the V_i input is scrambled by the CHP chopper, the only DC component in the D_{r2} digital stream is the DC offset of the A/D channel, V_{OS}. The integration-and-dump scheme is used to extract the DC offset from the D_{r2} stream. The resulting output D_{ro} is taken only after every M_c samples of integration of D_{r2}, where M_c is the period of the q_c binary pseudo-random sequence which controls the CHP chopper. The value of D_{ro} includes an estimation of the V_{OS} offset and a perturbation caused by the scrambled V_i signal. Assuming that the magnitude of V_i is uniformly distributed between $+0.5V_r$ and $-0.5V_r$, its averaged power can be approximated by $V_r^2/12$. The integration and dump function of the extractor can reduce the effect of this perturbation power by a factor of M_c. Then, the variance of D_{ro} can be expressed as

$$\sigma^2(D_{ro}) = \frac{1}{M_c} \times \frac{V_r^2}{12}. \tag{25}$$

To achieve B-bit accuracy for the TI ADC, we want $\sigma(D_{ro}) < V_r/2^B$. Thus, the required value of M_c can be expressed as

$$M_c > \frac{1}{3} \times 2^{2(B-1)}. \tag{26}$$

To achieve a resolution of $B = 15$, it is required that $M_c > (1/3)2^{28}$. In this design, $M_c = 2^{28}$ is chosen, so that both the q_c and q sequences have the same period, and can be generated from the same random generator.

VI. Experimental Results

This ADC prototype was fabricated in a $0.18\,\mu$m 1P6M 1.8-V CMOS logic technology with MIM capacitors. All voltage references are externally applied. Fig. 15 shows the ADC's die micrograph. The core area is 4.3×4.3 mm^2. Digital circuits occupy about 11% of the total area. Digital block and analog block use separate power lines. Operating at 125 MS/s sampling rate under a single 1.8 V supply, the analog part consumes 891 mW of power, while the digital part consumes only 18 mW.

Fig. 16 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the calibrated ADC operating at 125 MS/s sample rate with an 1.99 MHz sinusoidal input.

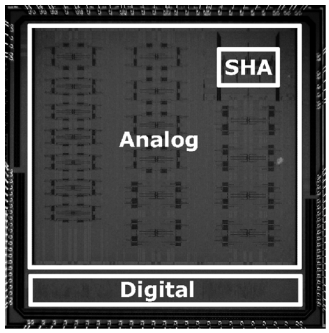

Fig. 15. Micrograph of the ADC prototype.

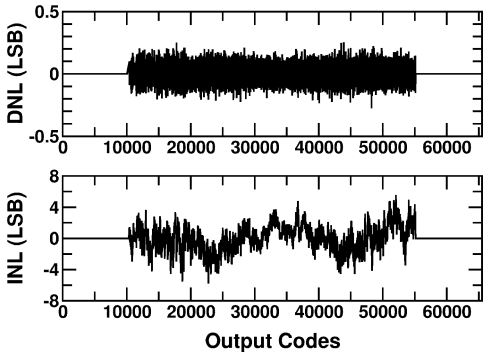

Fig. 16. Measured DNL and INL.

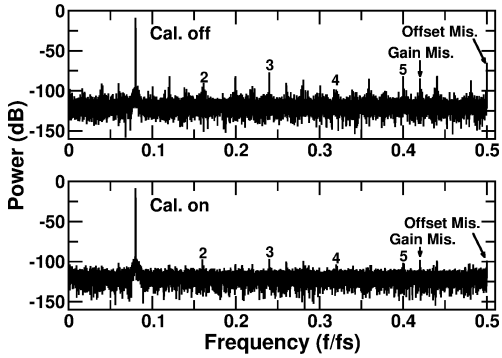

Fig. 17. Measured FFT spectrum.

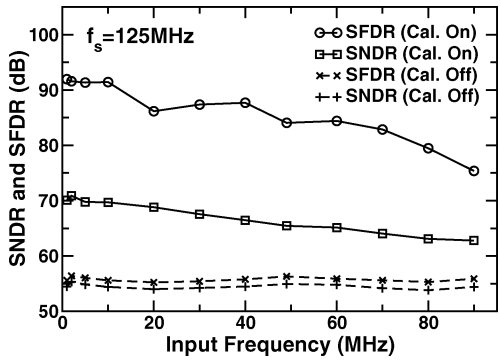

Fig. 18. Measured SNDR and SFDR versus input frequencies.

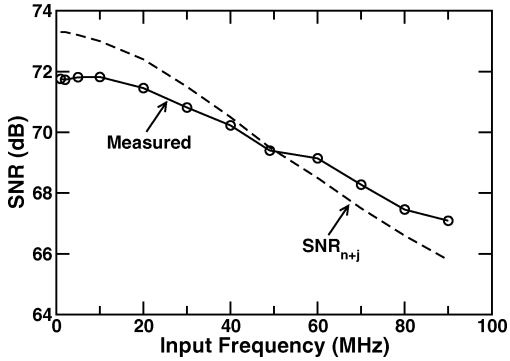

Fig. 19. Measured SNR versus input frequencies.

Digital output codes from a single channel are collected to calculate the DNL and INL. Note that the LSB in Fig. 16 is normalized to 16-bit resolution. The number of registered output codes is approximately (3/4) $\times 2^{16}$. Before activating the calibration processor, the native DNL is $+1.16/-0.61$ LSB and the INL is $+29.8/-29.7$ LSB. After the background calibration is activated. The DNL is reduced to $+0.25/-0.27$ LSB and the INL is reduced to $+5.5/-5.7$ LSB.

Fig. 17 shows the ADC's output FFT spectrum at 125 MS/s sampling rate. The input is a differential 1.4 $V_{\rm pp}$ 9.99 MHz sinusoidal signal. Before calibration, the dominant spurious tone is caused by the offset error. The signal-to-distortion-plus-noise ratio (SNDR) is 54.4 dB and the spurious-free dynamic range (SFDR) is 55.6 dB. After the calibration is activated, the SNDR is improved by 15.5 dB to 69.9 dB and the SFDR is improved by 36.3 dB to 91.9 dB. Calibration reduces the gain-mismatch tone from -85 dB to -98 dB, and reduces the offset-mismatch tone from -65 dB to -99 dB. Fig. 18 shows the ADC's measured SNDR and SFDR versus input frequencies at 125 MS/s sampling rate. The calibration can improve the SNDR by more than 10 dB and the SFDR by about 30 dB for input frequencies up to the Nyquist frequency.

Fig. 19 shows the ADC's measured signal-to-noise ratio (SNR) versus input frequencies at 125 MS/s sampling rate. The input is a differential 1.4 $V_{\rm pp}$ 9.99 MHz sinusoidal signal. The SNR is calculated from the ADC's output FFT spectrum while ignoring the harmonic tones caused by A/D nonlinearity and the spurious tones caused by inter-channel offset and gain mismatches. Also shown in Fig. 19 is the calculated SNR of an ADC model which includes the effect of sampling clock jitter Δt. Its input is $A\sin(2\pi f_{\rm in}t) + n_{ex}$ where n_{ex} is an external noise source. Its SNR can be expressed as [12]

$$\text{SNR}_{n+j} = \frac{\frac{A^2}{2}}{2\pi^2 f_{\rm in}^2 A^2 \overline{\Delta t^2} + \overline{n_{ex}^2}}. \tag{27}$$

By curve-fitting (27) against measured data, the root-mean-square (rms) value of n_{ex} is estimated to be $n_{ex,rms} = 137\,\mu$V, and the rms value of Δt is estimated to be $\Delta t_{rms} = 0.82$ psec.

Table I summarizes the measured specifications of this ADC chip and compare it with published works that claim to have a

TABLE I
PERFORMANCE COMPARISON

	This Work	[1]	[13]	[14]
Technology	0.18 μm CMOS	0.13 μm CMOS	0.35 μm BiCMOS	0.35 μm BiCMOS
Architecture	TI Pipelined	Pipelined	Pipelined	TI Pipelined
Calibration	Digital Background	Digital Background	None	Digital Foreground
Supplies	1.8 V	1.5 V	3.3 V/5 V	3.0 V
Input Range (V_{pp})	1.4 V	1.5 V	2 V	4 V
Power Consumption	0.909 W	0.224 W	1.95 W	1.4 W
Resolution	15 Bits	14 Bits	14 Bits	14 Bits
Max. Sampling Rate	125 MS/s	100MS/s	125 MS/s	100 MS/s
DNL (LSB)	$-0.27/+0.25$	$-1.1/+1.1$	$-0.2/+0.2$	0.97
INL (LSB)	$-5.7/+5.5$	$-2.0/+2.0$	$-0.5/+0.5$	6.9
SNR (@f_{in} = 5 MHz)	70.4 dB	70 dB	75 dB	
SNR (@f_{in} = 49 MHz)	67.3 dB	65 dB	75 dB	
THD (@f_{in} = 5 MHz)	-81.7 dB	-71.1 dB		
THD (@f_{in} = 49 MHz)	-76.9 dB	-68 dB		
THD (@f_{in} = 210 MHz)				-76.3 dB
SFDR (@f_{in} = 5 MHz)	91.6 dB		100 dB	
SFDR (@f_{in} = 70 MHz)	82.9 dB		95 dB	
SFDR (@f_{in} = 210 MHz)				79.9 dB
Active Area	18.5 mm^2	1.02 mm^2	70 mm^2	10.2 mm^2

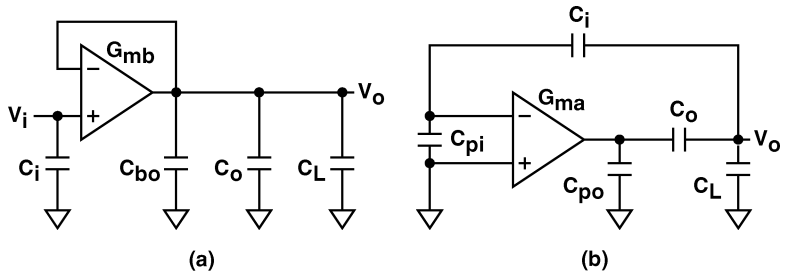

Fig. 20. BP-SHA simplified circuit models. (a) Precharge-mode circuit model. (b) Hold-mode circuit model.

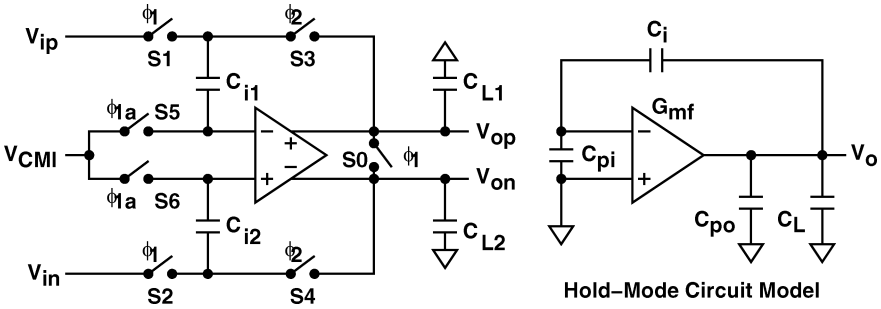

Fig. 21. Flip-around sample-and-hold amplifier (FA-SHA).

maximum sample rate of more than 100 MS/s and a resolution of more than 14 bits.

VII. CONCLUSION

A CMOS high-resolution high-speed TI ADC has been demonstrated. The TI A/D architecture can overcome the speed limitation imposed by the opamps and increase the ADC's overall sampling rate. However, the TI architecture also introduces A/D errors caused by the gain, offset, and sampling phase mismatches. To correct those errors requires extra hardware resources and consumes extra power. This design tried to minimize these overheads without sacrificing ADC's performance.

The TI ADC uses a single front-end SHA to avoid sampling phase mismatch. However, this SHA has to operate at full sampling speed. The precharging operation can mitigate the DC gain and unity-gain frequency requirements for the opamp. The precharging operation is to estimate the final SHA's output in advance, thus relaxing the opamp's duty in forcing the SHA to reach its final output value. This precharging procedure can be easily deployed in a TI ADC, requiring no extra time period.

This ADC uses simple digital signal processing to correct errors caused by gain and offset mismatches. For offset calibration, two additional analog random choppers are inserted at the inputs of the two A/D channels. No additional calibration procedure is required for gain correction. The information of gain mismatch is calculated directly from the calibration data obtained during the calibration of the two pipelined A/D channels. All calibration techniques incorporated in this ADC do not rely on input signal condition.

APPENDIX
BP-SHA'S OPAMP REQUIREMENTS

Consider the BP-SHA of Fig. 5. Both the core opamp and buffers are modeled as ideal transconductors, with G_{ma} for the

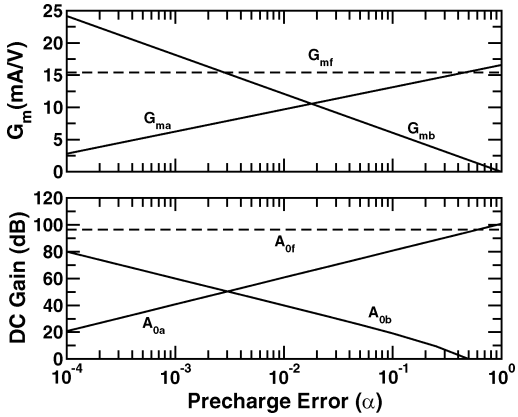

Fig. 22. G_m and A_0 requirements versus precharge error α.

opamp and G_{mb} for the buffers. Fig. 20 shows the resulting simplified circuit models for in precharge mode and hold mode. Capacitors C_{pi} and C_{po} are parasitic capacitors at the opamp's input and output nodes respectively. Capacitor C_{bo} is the parasitic capacitor at the buffer's output node.

Both circuits in Fig. 20 are single-pole systems. In the precharge mode, the G_{mb} buffer drives C_L, C_o, and C_{bo}, forcing V_o approximate V_i. Assume the precharge time is $T_{\rm on}$. At the end of precharge mode, V_o is settled to $(1-\alpha)V_i$, where $\alpha < 1$ is a precharge error. The relationship between G_{mb} and α can be expressed as

$$G_{mb} = \frac{C_{bo}+C_o+C_L}{T_{\rm on}} \times \ln\frac{1}{\alpha}. \tag{28}$$

When entering the hold mode, the G_{ma} opamp drives V_o from $(1-\alpha)V_i$ toward V_i. Assume the hold time is also $T_{\rm on}$. At the end of hold mode, V_o must be settled within $(1-2^{-N_B})V_i$, where N_B represents the SHA's resolution. The required G_{ma} can be written as

$$G_{ma} = \frac{[C_L+C_i||C_{pi}]\left[1+\frac{C_{po}}{C_o}\right]+C_{po}}{T_{\rm on}} \times \frac{C_i+C_{pi}}{C_i} \times [(N_B+1)\ln 2 + \ln\alpha]. \tag{29}$$

Consider a conventional flip-around SHA (FA-SHA) shown in Fig. 21. The opamp is modeled as an ideal G_{mf} transconductor. During hold mode, the opamp drives V_o from 0 toward V_i. Assuming the same $T_{\rm on}$ and N_B conditions as the above, then the required G_{mf} can be written as

$$G_{mf} = \frac{C_L+C_i||C_{pi}+C_{po}}{T_{\rm on}} \times \frac{C_i+C_{pi}}{C_i} \times [(N_B+1)\ln 2]. \tag{30}$$

The top plot in Fig. 22 shows the G_m requirements for both BP-SHA and FA-SHA at different precharge error, α. It is assumed that $C_i = C_L = 4$ pF, $C_o = 6$ pF, $C_{pi} = C_{po} = C_{bo} = 0.5$ pF, and $T_{\rm on} = 4$ nsec for a sampling rate of 125 MS/s.

Following similar analysis procedures, we can find DC gain requirements for the opamps. For a BP-SHA in the precharge mode, the relationship between the buffer's open-loop DC gain, A_{ob}, and precharge error, α, can be approximated as

$$A_{0b} \approx \alpha^{-1}. \tag{31}$$

In the following hold mode, the opamp needs to further drive V_o to within $(1-2^{-N_B})V_i$. Applying (1), the required DC gain, A_{0a}, can be found as

$$A_{0a} \approx \alpha \times 2^{N_B+1} \times \left(1+\frac{C_L}{C_o}\right). \tag{32}$$

For a FA-SHA in the hold mode, the opamp's output needs to vary from 0 and reach $(1-2^{-N_B})V_i$, the required DC gain, A_{0f}, is

$$A_{0f} \approx 2^{N_B+1} \times \left(1+\frac{C_{pi}}{C_i}\right). \tag{33}$$

The bottom plot in Fig. 22 shows the A_0 requirements for both BP-SHA and FA-SHA.

In practical BP-SHA designs, the minimal value of α is bounded by the buffers' offsets and charge injections from switches S5 and S6 located at the buffer's outputs.

Consider only the $\mathrm{kT/C}$ noises of the switches. Since the final hold-mode outputs of both BP-SHA and FA-SHA are determined by the charges on the C_i capacitors. We can expect similar noise performance for BP-SHA and FA-SHA.

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REFERENCES

[1] P. Bogner, F. Kuttner, C. Kropf, T. Hartig, M. Burian, and H. Eul, "A 14b 100 MS/s digitally self-calibrated pipelined ADC in 0.13 μm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2006, vol. 650, pp. 224–225.

[2] H.-C. Liu, Z.-M. Lee, and J. Wu, "A 15-b 40-MS/s CMOS pipelined analog-to-digital converter with digital background calibration," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1047–1056, May 2005.

[3] E. Siragusa and I. Galton, "A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2126–2138, Dec. 2004.

[4] J. William, C. Black, and D. A. Hodges, "Time interleaved converter arrays," *IEEE J. Solid-State Circuits*, vol. SC-15, no. 12, pp. 1022–1028, Dec. 1980.

[5] S. M. Jamal, D. Fu, N. C.-J. Chang, P. J. Hurst, and S. H. Lewis, "A 10-bit 120 MSample/s time-interleaved analog-to-digital converter with digital background calibration," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1618–1627, Dec. 2002.

[6] J. Elbornsson, F. Gustafsson, and J.-E. Eklund, "Blind adaptive equalization of mismatch errors in a time-interleaved A/D converter system," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 151–158, Jan. 2004.

[7] C.-C. Hsu and J.-T. Wu, "A CMOS 33-mW 100-MHz 80-dB SFDR sample-and-hold amplifier," *IEICE Trans. Electron.*, vol. E86-C, pp. 2122–2128, Oct. 2003.

[8] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[9] P. J. Hurst, S. H. Lewis, J. P. Keane, F. Aram, and K. C. Dyer, "Miller compensation using current buffers in fully differential CMOS two-stage operational amplifiers," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 51, no. 2, pp. 275–285, Feb. 2004.

[10] G. S. Ostrem, O. Moldsvor, and A. O. Aaserud, "A compact 3 V, 70 mW, 12-bit video-speed CMOS ADC," *Analog Integr. Circuits Signal Process.*, vol. 15, pp. 27–36, Jan. 1998.

[11] K. Gulati and H.-S. Lee, "A low-power reconfigurable analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1900–1911, Dec. 2001.

[12] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter analysis of high-speed sampling systems," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 220–224, Feb. 1990.
[13] A. M. Ali, C. D. Sneed, R. Sneed, A. Morgan, J. Kornblum, L. Wu, and S. Bardsley, "A 14-bit 125 MS/s IF/RF sampling pipelined A/D converter," in *Proc. IEEE Custom Integrated Circuits Conf.*, San Jose, CA, Sep. 2005, pp. 10-4-1–10-4-4.
[14] V. Hakkarainen, M. Aho, L. Sumanen, M. Waltari, and K. Halonen, "A 14b 200 MHz IF-sampling A/D converter with 79.9 dB SFDR," in *Proc. IEEE Norchip Conf.*, Oslo, Norway, Nov. 2004, pp. 171–174.

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