A 65-fJ/Conversion-Step 0.9-V 200-kS/s Rail-to-Rail 8-bit Successive Approximation ADC

Hao-Chiao Hong, *Member, IEEE*, and Guo-Ming Lee

***Abstract*—An 8-bit successive approximation (SA) analog-to-digital converter (ADC) in 0.18 μm CMOS dedicated for energy-limited applications is presented. The SA ADC achieves a wide effective resolution bandwidth (ERBW) by applying only one bootstrapped switch, thereby preserving the desired low power characteristic. Measurement results show that at a supply voltage of 0.9 V and an output rate of 200 kS/s, the SA ADC performs a peak signal-to-noise-and-distortion ratio of 47.4 dB and an ERBW up to its Nyquist bandwidth (100 kHz). It consumes 2.47 μW in the test, corresponding to a figure of merit of 65 fJ/conversion-step.**

***Index Terms*—ADC, energy efficient, low power, low supply voltage, μW design, successive approximation.**

I. Introduction

MANY energy-limited applications such as wireless sensor networks, biometrics, and portable amusement demand the energy-efficient analog-to-digital converter (ADC) to extend the duration of the system powered by the battery. The energy-efficient feature requests the ADC design to be not only low power but also bandwidth effective.

Power saving can be achieved in many aspects. At architecture level, different ADC architectures consume different power for the same specification. The successive approximation (SA) ADC exhibits the lowest power reported in literature due to its minimal active analog circuit requirement [1]–[9].

At circuit level, decreasing the supply voltage is an effective way to realize a low power design. The power of digital circuits directly benefits from supply voltage reduction. However, the low supply voltage makes the analog circuit design more difficult. For instance, when the sum of the absolute value of the pMOS's threshold voltage and that of the nMOS is larger than the supply voltage, conventional analog switches made of transmission gates may not be fully turned on as they are under a higher supply voltage. The MOSFETs expected to be turned on may now have extremely poor conductances [10] and would limit the bandwidth of the circuits. In addition, some useful design techniques such as cascoding and gain-boosting may not be applicable because of the limited signal swing. The low power requirement further sets the restriction that the circuit design should be as simple as possible.

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For example, the conventional 8-bit charge redistribution based SA ADC in [11] is not suitable for low voltage operation. Its input signal connects to all the capacitors of the digital-to-analog converter (DAC) through ten analog switches. When the input signal level is around half the supply voltage, these switches may have very poor on-resistances at a low supply voltage and thus limits the input bandwidth of the ADC. The switch connecting to the common-mode reference $V_{\rm CM}$ will suffer from the same issue as well since $V_{\rm CM}$ is usually designated to be a half of the supply voltage.

The poor on-resistances of the switches can be improved by using the process providing low threshold voltage (low-$V_{\rm th}$) devices, but such a process is more complex and leads to a higher fabrication cost. The low-$V_{\rm th}$ MOSFETs also have higher leakage currents that will distort the analog samples. Limiting the input signal swing is another solution [7]. Circuit design techniques can also be used to address the issue. Switched-opamp [10], [12], [13] and clock boosting [14]–[16] have been shown to be suitable for low supply voltage design. Yet a bootstrapped switch costs more power than a conventional one. To save the power, the number of the bootstrapped switches should be minimized.

In this paper, an energy-efficient 8-bit SA ADC is demonstrated. This ADC achieves a wide effective resolution bandwidth (ERBW) by applying only one bootstrapped switch. Consequently, the desired low power characteristic is preserved without compromise of its bandwidth. Section II explains the design of the SA ADC and analyzes its power consumption. Measurement results are presented in Section III. Some application dependent approaches to further save the energy are also discussed. Finally, Section IV draws our conclusions.

II. Design of the Successive Approximation ADC

Although a fully-differential circuit structure achieves better common-mode noise rejection and less distortion, it consumes more power. Since our SA ADC design targets on a moderate resolution, all the circuit components except for the comparator possess single-ended structures in order to reduce the power.

Fig. 1 shows the schematic of the proposed SA ADC, which is similar to that of [7]. The fundamental building blocks of the SA ADC consist of a track-and-hold (T/H) circuit, a charge-redistribution DAC, a comparator, and a successive approximation register (SAR).

The ADC has three power supplies: $AV_{\rm DD}$, $DV_{\rm DD}$, and $V_{\rm REF}$. They are designed to be the same voltage $V_{\rm DD}$. $DV_{\rm DD}$ supplies the digital circuits while $V_{\rm REF}$ is the full-scale reference voltage of the ADC. The rest of the circuits are powered by $AV_{\rm DD}$. The SA ADC eliminates the need for any reference

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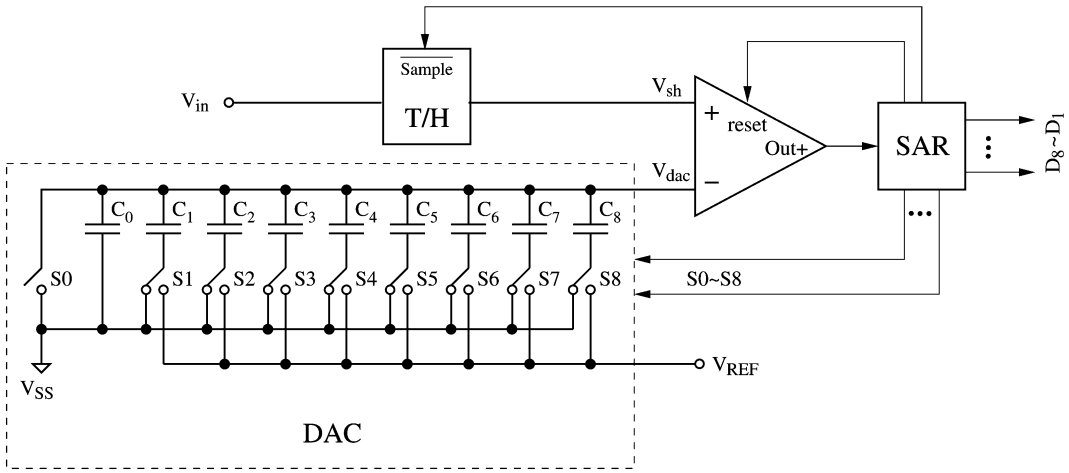

Fig. 1. Schematic of the proposed 8-bit SA ADC.

voltage different from $V_{\rm DD}$, such as the $V_{\rm CM}$ in [11], thus saving the power of the extra voltage generator.

All switches in the DAC part connect to either $V_{\rm REF}$ or the ground $V_{\rm SS}$. Consequently, these switches do not suffer from a poor on-resistance. In fact, there is only one analog switch in this architecture that may be non-fully turned on. This particular switch is located in the T/H block and directly connected to the input signal. The control signal of the switch is boosted to achieve an appropriate on-resistance at a supply voltage of 0.9 V. Compared with the conventional SA ADC in [11], the number of the required bootstrapped switches is reduced from eleven to one. As a result, the proposed ADC has lower circuit complexity as well as lower power dissipation.

A. Track-and-Hold Circuit

The T/H circuit is shown in Fig. 2. It is made of a sampling capacitor C_S and a simple nMOS NB driven by the boosted driver to achieve both low power and a wide bandwidth. The boosted driver produces a periodical output $\rm Sample_{boosted}$ switching between $2 \times V_{\rm DD} - \Delta V$ and the ground $V_{\rm SS}$. ΔV is due to the charge sharing between the boosting capacitor C_{B2} and the parasitic capacitance at the $\rm Sample_{boosted}$ node. An additional pMOS PB is added to alleviate the errors induced by the charge injection and clock feed-through impairments of NB. PB also helps enhance the on-conductance between $V_{\rm in}$ and V_{sh} when $V_{\rm in}$ is close to $V_{\rm DD}$. Both NB and PB have small sizes in order to achieve the following advantages. First, the impairments induced by them are mitigated. Second, their leakage currents, which will distort the sampled input, become less. Finally, the power overhead is reduced. In fact, the power of the boosted switch is negligible since the boosted driver operates at one ninth the clock frequency, as will be explained later. Even though both MOSFETs have small aspect ratios, the boosting technique keeps the on-resistance of the sampling switch small. Fig. 3 shows the simulated on-resistance of the boosted switch.

The T/H circuit has a bandwidth of $1/(2\pi R_{\rm on} C_S)$, where $R_{\rm on}$ is the on-resistance of the boosted switch. Since C_S is set to only 1.28 pF to mitigate the driving issue of the preceding signal source, the bandwidth of the T/H stage is estimated to be larger than 62 MHz.

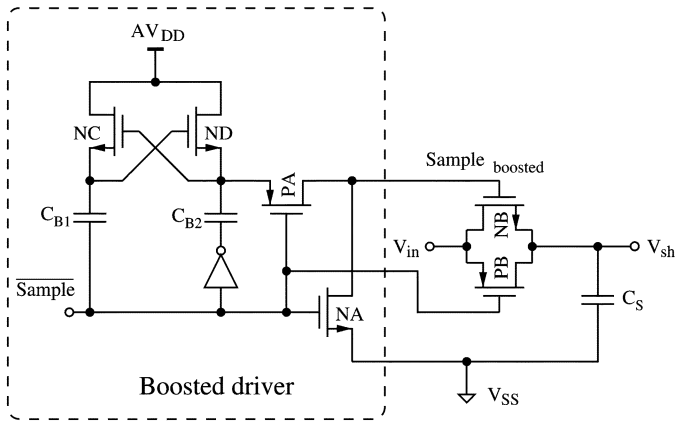

Fig. 2. Schematic of the T/H stage.

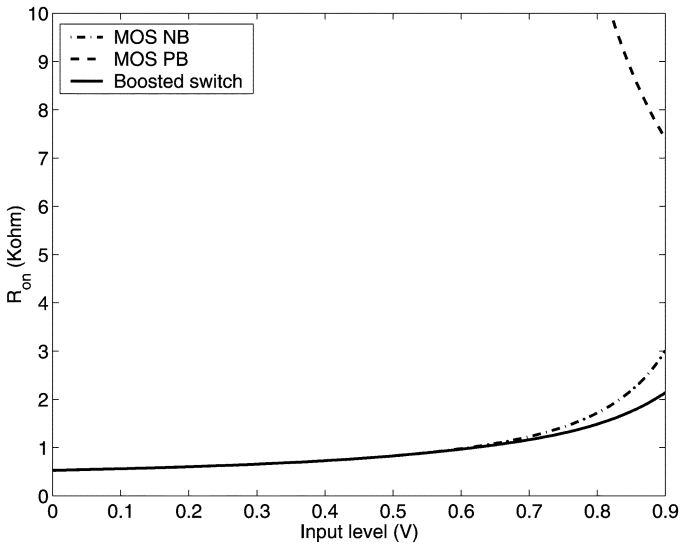

Fig. 3. On-resistance of the boosted switch.

B. Comparator With a Rail-to-Rail Input Range

The low supply voltage inherently limits the maximum input signal swing of an ADC, and thus may lead to a poor peak signal-to-noise ratio (SNR). To overcome the signal swing

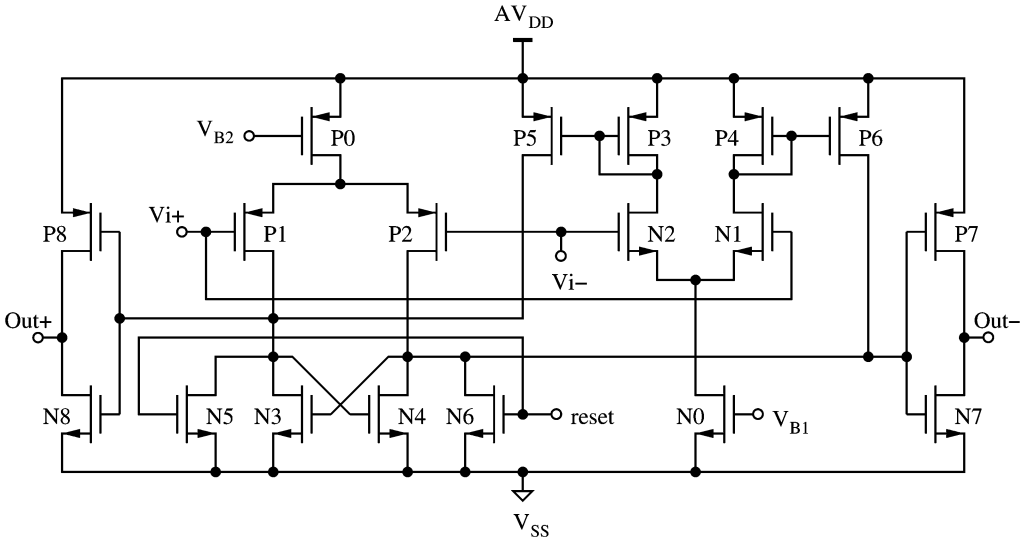

Fig. 4. Schematic of the comparator with a rail-to-rail common-mode input range.

reduction at a low supply voltage, a rail-to-rail input range is required in the SA ADC design. A comparator with a rail-to-rail common-mode input range is substantial for this design in order to achieve the required rail-to-rail input swing.

The proposed comparator is shown in Fig. 4. The p- and n-type differential pairs connected in a parallel manner are used to extend the common-mode input range to the power rails. It is the only block with a fully-differential structure in order to reject the common-mode disturbances induced by the T/H and DAC. Both differential pairs convert the differential input voltages into differential output currents. These currents are summed together respectively to drive the regenerative load formed by $N3$ and $N4$. The two successive inverters with a designated threshold voltage amplify the complementary outputs to their full rail-to-rail logic levels. Additional resetting nMOS $N5$ and $N6$ are added to reduce the hysteresis effect in order to speed up the comparator.

The tail currents of the differential pairs are designed to ensure that both differential pairs still produce sufficiently large differential output currents to drive the regenerative loads in the worst condition. The whole comparator including the bias circuits consumes only 0.6 μW at 0.9 V.

The major issue of using such a rail-to-rail comparator is that the offset of the comparator may depend on the common-mode input. Let V_P be defined as the upper-limit voltage such that the pMOS differential pair will not generate sufficiently large currents to trigger the regenerative load within a clock period once the common-mode input is higher than it. Similarly, let the lower-limit voltage V_N be defined such that the nMOS differential pair will not affect the outputs of the comparator if the common-mode input is below V_N. Then, the offset of the comparator will be dominated by the mismatch of the pMOS differential pair when the common-mode input is between $V_{\rm SS}$ and V_P. Meanwhile, the nMOS differential pair and the following current mirrors determine the offset if the common-mode input is within the range from V_N to $V_{\rm DD}$. Between the the two ranges discussed above, the mismatches of both differential circuits contribute to the offset of the comparator. This common-mode input dependency of the offset may result in distortion.

The threshold voltage mismatch and the peripheral mismatch of the MOSFETs were shown to be two dominant factors that induce the input-referred offset voltage of a differential pair [17]. The square standard deviation of the threshold voltage is known to be

$$\sigma^2(\Delta V_{\rm th}) = \frac{A_{VT0}}{WL} \tag{1}$$

where W and L represent the effective channel width and length of the MOSFETs and A_{VT0} is a process dependent constant. On the other hand, the randomness of the peripherals of the MOSFETs is a less concern if both W and L are large enough. Hence, the areas of the MOSFETs, $N1$, $N2$, and $P1$ to $P6$, were designed to be large so as to address the common-mode input dependent offset. In addition, their layouts were carefully done by using a common-centroid style and adding dummy devices.

C. Successive Approximation Register

The SAR generates the necessary control commands based on the successive approximation algorithm to control the T/H, comparator, and DAC [18]. Nine clock cycles are required to complete a single conversion. Cycle one is the reset cycle. It is needed for avoiding the possible residual charge of the DAC induced by the clock feed-through and charge injection of the switches during the conversion of the preceding sample. The input is also sampled in this cycle. This arrangement provides the T/H stage with a full clock cycle to track the input signal. The ADC conducts bit-cycling in the rest of the cycles to produce the final digital outputs D_8 to D_1.

The SAR is built with standard CMOS logic gates. It is well known that the power consumption of such a CMOS logic circuit is approximately

$$PD V_{\rm DD}(V_{\rm in}) = f_{\rm clk} V_{\rm DD}^2 C_{\rm ckt} \alpha(V_{\rm in}) \tag{2}$$

where $f_{\rm clk}$ represents the clock frequency, $C_{\rm ckt}$ denotes the total capacitance of the circuit nodes, and $\alpha(V_{\rm in})$ is the switching activity factor depending on the analog input $V_{\rm in}$. In order to

save the digital power, all MOSFETs of the digital gates were designed to be as small as possible to minimize $C_{\rm ckt}$.

D. Digital-to-Analog Converter

The DAC is implemented by using a binary-weighted switched-capacitor array as shown in Fig. 1. $S8$ to $S0$ are the control signals generated by the SAR to control the switches of the DAC, and

$$C_i = 2^{i-1}C_0, \quad i \in \{1, \ldots, 8\}. \tag{3}$$

In the above equation, C_0 is the capacitance of the unit capacitor in the switched-capacitor array. Each of the switches connecting to $V_{\rm REF}$ is implemented by a simple PMOS, and a single nMOS is used for the switches connecting to $V_{\rm SS}$.

The major power of the DAC comes from the reference voltage supply. The power consumption of the reference voltage supply when an input $V_{\rm in}$ is applied can be calculated according to

$$PV_{\rm REF}(V_{\rm in}) = \frac{V_{\rm REF}}{T}\sum_{i=1}^{9} Q_i \tag{4}$$

where T denotes the period to convert a sample and Q_i represents the total charge that $V_{\rm REF}$ supplies to the DAC during the ith cycle.

Let $C_{\rm DAC}$ represent the total capacitance of the DAC. In the first cycle, all capacitors of the DAC are reset. There is no charge transferred from $V_{\rm REF}$ to the DAC, thus $Q_1 = 0$. During the second cycle, C_8 connects to $V_{\rm REF}$ while the connections of the rest of the capacitors are not changed. As a result,

$$\begin{aligned} V_{\rm dac8} &= V_{\rm REF}\frac{C_8}{C_{\rm DAC}}, \\ Q_2 &= C_8[(V_{\rm REF} - V_{\rm dac8}) - (0 - 0)]. \end{aligned} \tag{5}$$

In the third cycle, C_7 connects to $V_{\rm REF}$ and C_8 connects to $D_8V_{\rm REF}$. The output of the DAC at the end of this cycle is

$$V_{\rm dac7} = V_{\rm REF}\frac{C_7 + D_8C_8}{C_{\rm DAC}} \tag{6}.$$

$V_{\rm REF}$ supplies C_7 and C_8 with the necessary charge. If $D_8 = 0$, $V_{\rm REF}$ transfers no charge to C_8. Otherwise, the charge stored in C_8 in the second cycle will be shared with C_7. Therefore, the total charge supplied by $V_{\rm REF}$ in the third cycle is written as

$$\begin{aligned} Q_3 = {} & C_7[(V_{\rm REF} - V_{\rm dac7}) - (0 - V_{\rm dac8})] \\ & + D_8C_8[(V_{\rm REF} - V_{\rm dac7}) - (V_{\rm REF} - V_{\rm dac8})]. \end{aligned} \tag{7}$$

Similar deductions lead to a more general expression:

$$\begin{aligned} Q_i = {} & C_{10-i}[(V_{\rm REF} - V_{{\rm dac}(10-i)} + V_{{\rm dac}(11-i)})] \\ & + \sum_{j=11-i}^{8} D_jC_j(V_{{\rm dac}(11-i)} - V_{{\rm dac}(10-i)}), \\ & i \in \{3, \ldots, 9\} \end{aligned} \tag{8}$$

and

$$V_{{\rm dac}i} = V_{\rm REF}\frac{C_i + \sum_{j=i+1}^{8} D_jC_j}{C_{\rm DAC}}. \tag{9}$$

Let D_9 be zero. By combining (8), (9), and (5) with (4), and then applying (3) to the result, the power consumption of the reference voltage supply is derived to be

$$\begin{aligned} PV_{\rm REF}(V_{\rm in}) = {} & \frac{f_{\rm clk}}{9}2^8C_0V_{\rm DD}^2 \\ & \times \left\{ \frac{2^8 - 1}{2^8} + \sum_{i=1}^{7}\left[\left(\frac{1}{2^i} + \sum_{j=0}^{i-1}\frac{D_{(9-j)}}{2^j} \right) \right.\right. \\ & \left.\left. \times \left(-\frac{1}{2^{i+1}} + \frac{D_{(9-i)}}{2^i} \right) \right] \right. \\ & \left. - \left(\frac{1}{2^8} + \sum_{k=0}^{6}\frac{D_{8-k}}{2^{k+1}} \right)^2 \right\} \\ \simeq {} & \frac{f_{\rm clk}}{9}2^8C_0\left(\frac{5}{6}V_{\rm DD}^2 - \frac{1}{2}V_{\rm in}^2 \right). \end{aligned} \tag{10}$$

According to (10), the unit capacitor C_0 in the DAC should be kept as small as possible to save the power dissipation. In practice, the smallest capacitance of C_0 is determined by considering the thermal noise, capacitor matching, and the design rules. For our design, the smallest capacitance is not limited by the KT/C thermal noise. Consequently, C_0 is set to the minimum value, which is about 24 fF, according to the design rules. The binary-weighted capacitor array is laid out based on a common-centroid placement. Each of the non-unit capacitors, C_2 to C_8, is made of plural unit capacitors in parallel for a better matching characteristic.

The switches in the passive DAC are designed to achieve a bandwidth larger than 42 MHz, so as not to limit the bandwidth of the ADC.

III. Measurement Results

The SA ADC was fabricated in a 0.18 μm 1P6M CMOS process through the service of National Chip Implementation Center (CIC), Taiwan. Fig. 5 shows the micrograph of the test chip. The test chip occupies 0.70 mm^2 and the active area of the SA ADC is 0.062 mm^2. In the following measurements, the supply voltages $AV_{\rm DD}$, $DV_{\rm DD}$, and $V_{\rm REF}$ were shorted together on the evaluation board and set to 0.9 V. The amplitude and frequency of the test stimulus and the clock frequency were set to -0.056 dBFS, 1.001 kHz, and 1.8 MHz, respectively, unless otherwise noticed.

A. Static Performance

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the SA ADC are shown in Fig. 6. The INL is in the range of $-0.53/+0.5$ LSB whereas the DNL is within $-0.9/+0.26$ LSB.

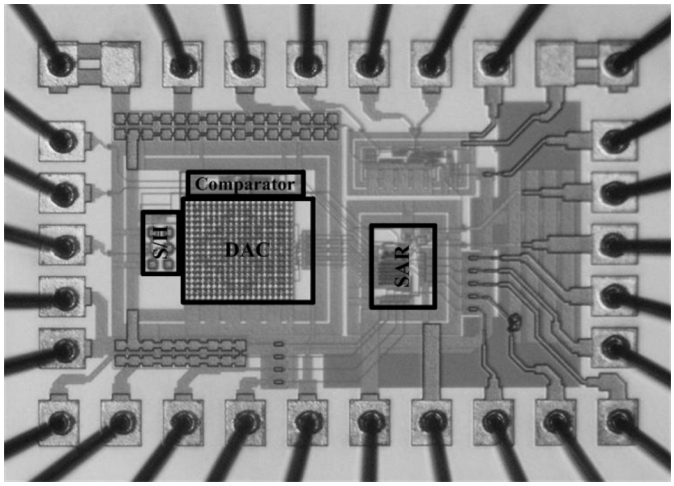

Fig. 5. Micrograph of the test chip.

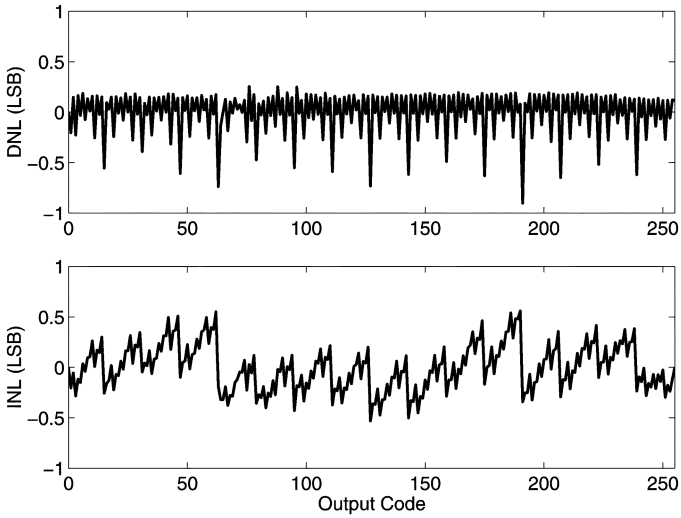

Fig. 6. Measured DNL and INL plots of the SA ADC.

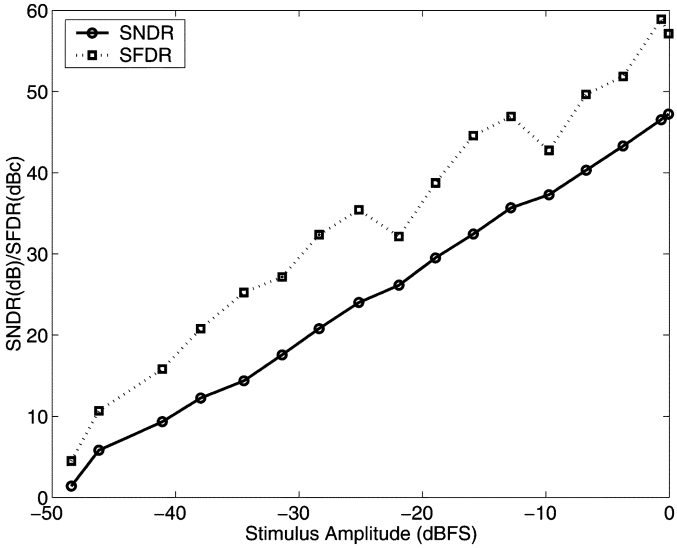

Fig. 7. Measured SNDR and SFDR versus stimulus amplitude.

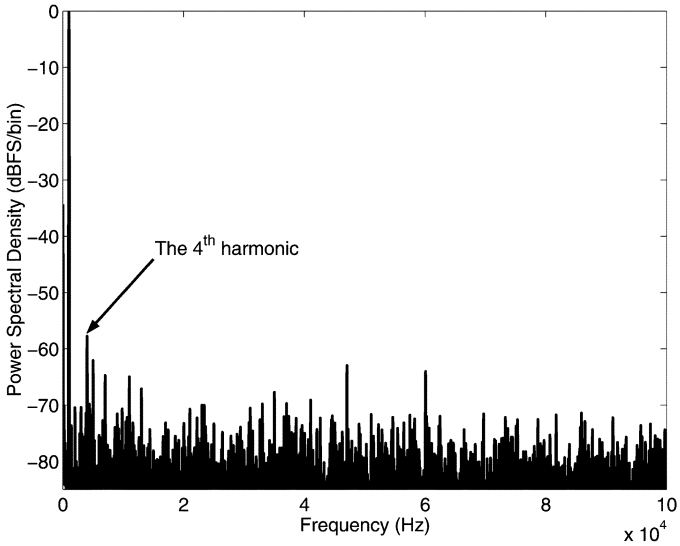

Fig. 8. Measured output spectrum of the SA ADC with the -0.056 dBFS, 1.001 kHz sinusoidal input.

Although it is not possible to directly measure the offset of the comparator versus the common-mode input in our design, the INL plot can provide some information about the impairment. The static test can be regarded as if an input distorted by the common-mode input dependent offset were applied to an offset-free ADC. Hence, the common-mode input dependent offset will lead to a slow bending in the INL plot. According to Fig. 6, no significant INL bending was found. It indicates that the offset variation does not degrade the performance of the ADC under test.

B. Dynamic Performance

Fig. 7 plots the measured signal-to-noise-and-distortion ratio (SNDR) and spurious free dynamic range (SFDR) of the SA ADC with respect to the stimulus amplitude. The results prove that the ADC indeed has a rail-to-rail input range. Besides, the ADC achieves a peak SNDR and a peak SFDR of 47.4 and 58.9 dB, respectively. It corresponds to an effective number of bit (ENOB) of 7.58 bits.

Fig. 8 shows the measured output spectrum of the ADC where the ADC achieves its peak SNDR. 8192 samples were used to derive the spectrum. The main spurious tone is the fourth harmonic of the stimulus, showing that the ADC is somewhat asymmetric at the test setup. Nevertheless, the fourth harmonic is only -58.9 dBFS and thus has no significant impact on the SNDR performance of the ADC. The harmonic distortions of the ADC as functions of the input frequency are shown in Fig. 9.

Fig. 10 illustrates the measurement results of the ADC's SNDR and SFDR versus different stimulus frequencies and amplitudes. The SNDR does not degrade even with the stimulus frequency close to 100 kHz. In other words, this ADC achieves an ERBW no less than its Nyquist bandwidth and the ERBW is independent of the stimulus amplitude.

Fig. 11 depicts the measured SNDR versus the system clock frequency with the 1 kHz sinusoidal stimulus to test the maximum operation speed of the ADC. The ADC is shown to be able to operate at a clock frequency as high as 2 MHz without notable SNDR degradation. Further increasing the clock rate will

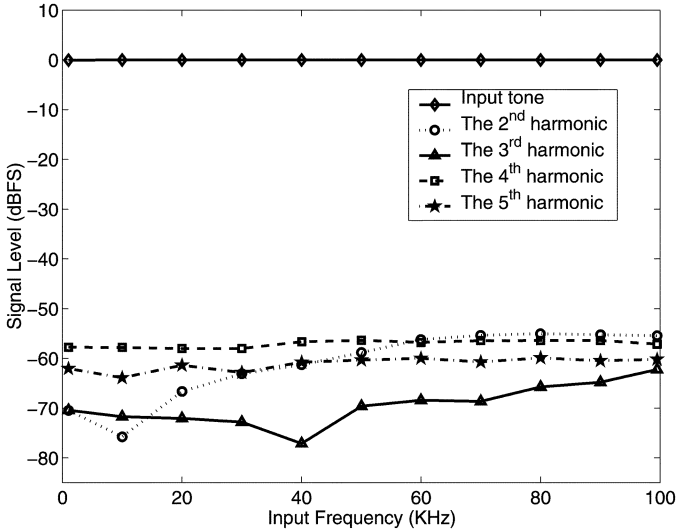

Fig. 9. Measured harmonic distortion versus input frequency.

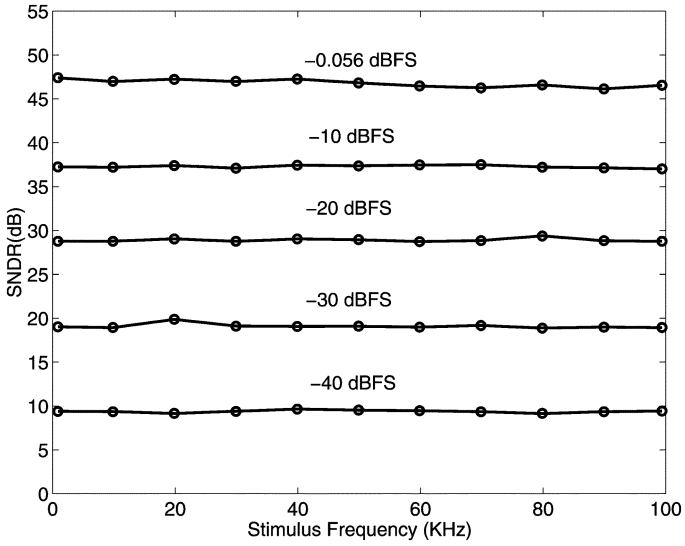

Fig. 10. Measured SNDR versus input frequency at different stimulus amplitudes.

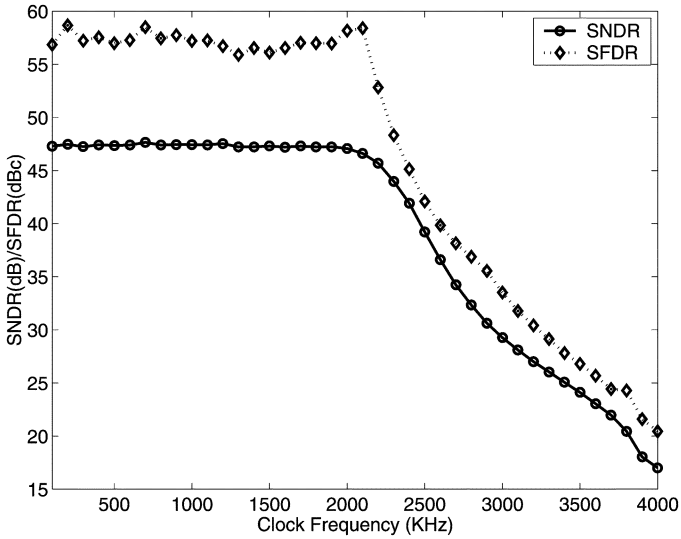

Fig. 11. Measured SNDR and SFDR versus clock frequency with the 1 kHz stimulus.

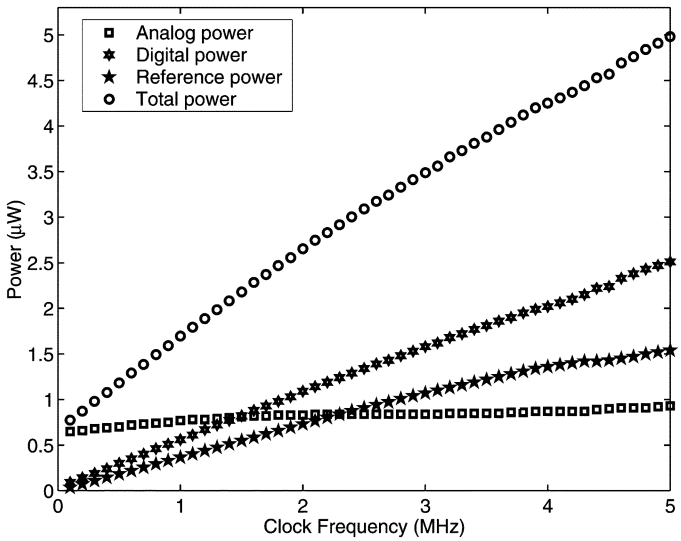

Fig. 12. Measured power versus clock frequency with the 1-kHz stimulus.

degrade the performance of the ADC. Since the bandwidths of the T/H and the DAC are all much higher than 2 MHz, it is the comparator that limits the bandwidth of the ADC design.

C. Power Consumption

The total power dissipation of the SA ADC is 2.47 μW at 0.9 V and a 200 kS/s output rate. The averaged powers of $AV_{\rm DD}$, $DV_{\rm DD}$, and $V_{\rm REF}$ are 0.83, 0.98, and 0.66 μW, respectively. The power may be further reduced depending on applications. Fig. 12 displays the measured power consumption of every power supply versus the clock frequency. The same 1-kHz sinusoidal stimulus was applied to the tests.

Most of the analog power is consumed by the comparator. Due to the constant current sources in the comparator, the analog power of the ADC is almost a constant regardless the clock frequency. For higher output rate applications, the only necessary modification of this design is increasing the bias currents of the comparator.

TABLE I
SUMMARY OF THE SA ADC

Process	0.18μm CMOS		
Active area (mm^2)	0.062		
Supply voltage (V)	1.0	0.9	0.83
Clock frequency (MHz)	3.6	1.8	1.0
Output rate (KHz)	400	200	111
SNDR@f_{in}=1KHz (dB)	45.8	47.4	46.7
ENOB@f_{in}=1KHz (bit)	7.31	7.58	7.46
ERBW (KHz)	200	100	55
Total power dissipation (μW)	6.15	2.47	1.16
Test chip area (mm^2)	0.70		

According to (2) and (10), both powers of $DV_{\rm DD}$ and $V_{\rm REF}$ are dynamic powers. They will automatically scale with the clock frequency. Fig. 12 shows that these two powers are in-

TABLE II
COMPARISON OF THE PROPOSED SA ADC WITH THE STATE-OF-THE-ART RESULTS

Sources	[6]		[7]		[9]	This work		
Technology	0.25μm CMOS		0.18μm CMOS		0.18μm CMOS	0.18μm CMOS		
Supply voltage (V)	1	1.4	0.5	1	1	1	0.9	0.83
Input swing/Supply voltage	1	1	0.25	0.25	N/A	1	1	1
Output rate (Sample/s)	100K	100K	4.1K	150K	100K	400K	200K	111K
ENOB@DC (bit)	7.9	7.9	6.9	8.2	10.55	7.31	7.58	7.46
ENOB@Nyquist bandwidth (bit)	4.5	7.45	4.86	N/A	10.55	7.13	7.44	7.42
ERBW (Hz)	3K	50K	3K	30K	50K	200K	100K	55K
Power dissipation (μW)	3.1	4.6	0.85	30	25	6.15	2.47	1.16
FOM (fJ/conversion-step)	2163	193	1186	1700	167	97	65	60

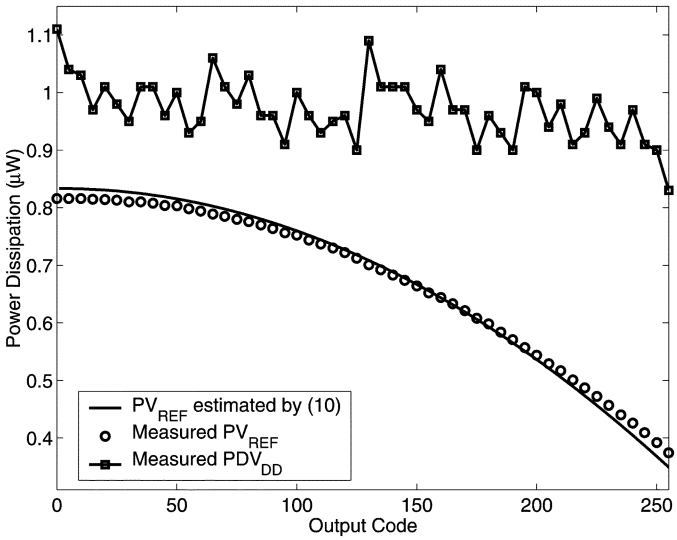

Fig. 13. Dynamic power versus output code.

deed proportional to the clock frequency. At an output rate of 11.1 kS/s, the ADC totally consumes only 0.78 μW.

Reducing the supply voltage is another effective way to further cut down the power for low output rate applications. Our measurement results show that this ADC has a satisfactory performance when operating at a supply voltage as low as 0.83 V and an output rate of 111.1 kS/s. Compared with the dynamic power when the ADC operates at 0.9 V and the same output rate, about 15% of the dynamic power can be saved. Table I lists the summary of the SA ADC design.

Equations (2) and (10) also reveal that the powers of both voltage supplies are input signal dependent. The measured powers of both voltage supplies are plotted in Fig. 13. There is no clear trend for the power of $DV_{\rm DD}$ with respect to the output code because of the randomness of $\alpha(V_{\rm in})$. On the other hand, the measured reference voltage power and the estimated values made by (10) show good agreement. Both results demonstrate that a larger output code consumes less reference voltage power. It leads to a possible power saving scenario: the reference voltage power can be saved by adjusting the common-mode voltage of the input, if the input excursion of the ADC in a certain application is known to be less than the full-scale input range of the ADC. For example, given a sinusoidal input whose amplitude is 0.32 V, $PV_{\rm REF}$ is estimated to be 0.68 μW when the common-mode voltage of the input is set to 0.45 V. By adjusting the common-mode voltage to 0.58 V, the reference voltage power is reduced to 0.58 μW. About 15% of the reference voltage power can be saved, provided that shifting the common-mode voltage of the input costs no additional power.

D. Comparison With Other Approaches

The figure of merit (FOM) used in [19], [20] is referred here to compare the proposed ADC design with other state-of-the-art works. The FOM is defined as

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB@DC}} \cdot 2 \cdot \text{ERBW}}. \tag{11}$$

This FOM is from an energy perspective, instead of a power point of view. It dictates the energy required to accomplish an effective conversion step of an ADC. Table II lists the comparison results. The proposed SA ADC spends the least energy for an effective analog-to-digital conversion step. In addition, it achieves the widest ERBW among these sub-1 V, μW ADC designs.

IV. CONCLUSION

An energy-effective 8-bit SA ADC is presented. At 0.9 V and an output rate of 200 kS/s, the SA ADC achieves an ERBW up to the Nyquist bandwidth, a peak SNDR of 47.4 dB, a peak SFDR of 58.9 dB, and a rail-to-rail input range. From the energy perspective, the proposed ADC achieves an FOM of 65 fJ/conversion-step. The FOM of the ADC is enhanced to be 60 fJ/conversion-step at 0.83 V and a 111.1 kS/s output rate.

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