國 立 交 通 大 學

奈 米 科 技 研 究 所

碩 士 論 文

溶膠-凝膠法應用於非揮發性奈米微晶粒記憶體元件

Novel Sol-Gel Derived Nonvolatile Nanocrystal Memory Devices

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中華民國九十七年六月

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頭陪我一起走過同學們：美榕、宜生、皮、中書，在不同研究方向中各自努力的我們，終於要順利畢業了！也感謝親愛的學弟妹：鄭捷、京彰、柏軒、玟菲、嘉琦、薏卉，及兩位遠道而來的 Sri、Jagan，有你們在實驗室總是充滿笑聲，實驗室的未來要靠你們繼續努力了！當然不能忘記在 NDL 一起努力的夥伴們：秉叡、舜博、貞志、承志、叮噹、煜勝、智超、久富、金木、登偉、伯康，來自四面八方的我們竟可以這麼放得開，跟你們相處的時候總會笑到感覺多了好幾條魚尾紋，這兩年來有你們將我的生活填滿笑聲，真的非常感謝你們。還有奈米所的朋友們：欣霖(皮姐)、奕貞、昶龍、子訓、高超、新堯，即將邁入下一站的我們，給彼此最多的祝福。感謝好友們：淑華、灝儀、秀玲、純如、藍瑛、清泰、益銘、藝蓉、佳芬、閣倫、JOE、詠嘉、總安、惠鈺，很開心我們不因為時空隔絕而斷了聯繫，也因為有你們的鼓勵讓我更有勇氣面對挑戰。

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新穎溶膠-凝膠法應用於非揮發性奈米微晶粒記憶體元件

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摘　要

本論文所探討的內容係以配製的化學溶液經由溶膠-凝膠法，來研究成長奈米微晶粒的機制。我們以四氯化鋯、四氯化鉿及四氯化矽為溶膠-凝膠溶液之前驅物，旋轉塗佈於晶圓上，經高溫退火後形成含有鋯及鉿之金屬矽氧化物。在本實驗中，溫度效應及溶劑效應是影響奈米微晶粒形成的關鍵因素。此外，我們利用溶膠-凝膠法形成之奈米微晶粒材料運用於快閃式記憶體元件中，作為電荷捕捉層(charge trapping layer)，並探討其電性表現。實驗涵概三個主題，我們將其內容摘要說明如後。

第一個主題，我們針對溫度效應做深入探討。實驗中發現溶膠-凝膠法旋轉塗佈在晶圓上形成薄膜，經 600 ^{o}C 高溫退火開始進入不穩定相而造成薄膜表面開始分裂，此時具有較高的表面能(interfacial energy)。當退火溫度高達 900 ^{o}C，

溶膠-凝膠薄膜已經過相變化分裂成完全獨立之奈米微晶粒，此時可以量測得到已達穩定態之低表面能。我們以 900 ^{o}C 退火條件製作完整的記憶體元件，測試資料保存時間為在 125 ^{o}C 的量測環境下經過 10^{6} 秒後只有少於 25%的電荷流失。

第二個主題中，我們針對以溶膠-凝膠法製備快閃記憶體中之電荷捕捉層的相變化機制進行討論。溶膠-凝膠薄膜經 900 ^{o}C 高溫退火後可發現電荷陷捕層產生旋節相分離(spinodal decomposition)而形成奈米微晶粒結晶，而能否形成奈米微晶粒的關鍵在於旋轉塗佈至晶圓上的溶膠-凝膠薄膜厚度。我們選擇兩種不同的溶劑，包括乙醇及異丙醇(IPA)，用以調控薄膜厚度。實驗中發現在乙醇系統中形成之奈米微晶粒呈現完全獨立、分離之形貌，然而，在異丙醇系統中形成之奈米微晶粒卻產生具有內部相連、不完全分離的狀態。根據 Seol 等人利用電腦模擬旋節相分離的狀態，他們推測旋節相分離後的薄膜形貌與薄膜厚度及成分相關，較薄的溶膠-凝膠薄膜經過旋節相分離能夠形成完全獨立之奈米微晶粒。由於以乙醇為溶劑能夠得到較薄之薄膜，經旋節相分離後得到獨立之奈米微晶粒，以此作為記憶體之電荷陷捕層具有良好的記憶體特性，包括資料保存時間久(在 25 ^{o}C 及 85 ^{o}C 量測條件下各只有少於 5%及 10%的電荷流失)，且記憶視窗可高達 10V 之大。

最後，我們利用整合有機與無機材料之溶膠-凝膠法，製造一完整的奈米微晶粒記憶體元件，並進行電性分析。我們成功的製作出特性良好的記憶體，此記憶體具有大的記憶視窗、資料寫入速度快、較長的資料保存時間及元件耐久力佳等等特色。在此主題中，我們針對記憶體的可靠度做一系列的分析探討。由於此奈米微晶粒記憶體元件具有相當大的記憶視窗，期待將來可應用於多位元晶胞之記憶體元件。

Novel Sol-Gel Derived Nonvolatile Nanocrystal Memory Devices

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ABSTRACT

In this thesis, the formation mechanism of nanocrystals (NCs) from the sol-gel spin-coating method had been studied. The $ZrCl_4$, $HfCl_4$, and $SiCl_4$ were used as the sol-gel precursors to form the hafnium and zirconium silicate after high temperature annealing. We evaluated the impact of temperature and preparation solvent type for the formation of sol-gel derived nanocrystals. In addition, the performance of flash memory with the nanocrystal as the charge trapping layer was also demonstrated. The aim of this study is organized in the following.

At first section, we focused on the rapid thermal annealing temperature affected deposited sol-gel transformation. We detected the sol-gel film became unstable and perturbed at 600 °C annealing, and finally transformed into NCs at 900 °C annealing. A mechanism was proposed to explain the transformation of the sol-gel thin film. The

morphology of sol-gel thin film at 600 °C annealing was unstable and had higher interfacial energy. The nano-crystallized process at 900 °C annealing could minimize the energy. As to the memory devices, the property of retention issue (charge preservation ability after program for nanocrystals) for 900 °C annealed sample demonstrated less than 25% charge loss after 10^6 sec duration under 125 °C measurement condition.

Secondly, we investigated the phase separation mechanism for the charge trapping film in sol-gel derived nanocrystal memory. The nano-crystallization from spinodal phase separation was observed for sol-gel thin film at 900 °C annealing, and was strongly related to the thickness of the spin-coated thin film. We chose ethanol and IPA as the solvent in order to control the sol-gel film thickness. We found the morphology of the NCs in ethanol system existed in the isolated form, while interconnected form in IPA system. Seol et al.*[1, 2]* utilized computer simulation to deduce the spinodal decomposition process. They suggested the morphology of decomposed phases on initially homogeneous thin film strongly depends on the film thickness and the composition. Ethanol as preparation solvent deposited a thinner film, and formed isolated NCs after spinodal decomposition. Ethanol system sample as memory device exhibited excellent performance such as the data retention less than 5% and 10% charge loss at 25 °C and 85 °C, respectively. The ethanol system sample also demonstrated a large memory window (~10V) than IPA system (~3V).

Finally, the detailed electrical properties for the sol-gel derived NC memory were measured. The obtained flash memory exhibited excellent characteristics such as large memory window, high program speed, and superior gate/drain disturbance properties. In addition, the reliability of the memory was also evaluated in this section. The sol-gel derived NC memory with large memory window from 900 °C annealed sample shows the effectiveness of device operation for future multibit application.

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Chapter 1

Introduction

1.1 General introduction

Silicon technology based nonvolatile memories (NVM) possess the feature of retaining information without any consumption of power, they can maintain the function of a computer hard drive, storing a few bytes up to a few Gigabytes of code and/or data. Prominent examples of applications enabled by NVM are cellular phones, MP3 players, digital cameras, and microcontrollers.*[3]* (See Figure 1.1) A nonvolatile memory (NVM) device is a MOS transistor that has a source, a drain, an access or a control gate, and a floating gate. The schematic cross-section of a floating gate memory device shows in Figure 1.2. It is structurally different from a standard MOSFET in its floating gate, which is electrically isolated, or "floating".*[4]* Nonvolatile memories are subdivided into two main classes: floating gate and charge-trapping. The different series of nonvolatile memory families can be qualitatively compared in terms of flexibility and cost. Flexibility means the possibility to be programmed and erased many times on the system with minimal granularity (whole chip, page, byte, bit); cost means process complexity and in particular of silicon occupancy, i.e., density or, in simpler words, cell size.

In floating gate memory devices, charge or data is stored in the floating gate and

is retained when the power is removed. All floating gate memories have the same generic cell structure. Floating gate devices are typically used in EPROM (Electrically Programmable Read Only Memory) and EEPROM's (Electrically Erasable and Programmable Read Only Memory). Charge-trapping devices were invented in 1967 *[5]* and were the first electrically alterable semiconductor devices. In charge-trapping memory devices, charge or data is stored in the discrete nitride traps and is also retained when the power is removed. Charge-trapping devices are typically used in MNOS (Metal Nitride Oxide Silicon) *[6]*, SNOS (Silicon Nitride Oxide Semiconductor) *[7]*, and SONOS (Silicon Oxide Nitride Oxide Semiconductor) *[8]*.

The semiconductor industry has experienced many changes since flash memory first appeared in the early 1980s. The growth of consumer electronics market urges the demand of flash memory and helps to make it a prominent segment within the semiconductor industry. These concerns proved the flash memory market began to grow in the early 1990s. Broadly speaking, flash memory ideally suits the consumer electronics market, because it bestows upon electronic devices two qualities that the market demands: mobility and miniaturization. Because of its small, reliable, and nonvolatile properties, numerous applications not practicable with traditional data storage technology are emerging. Flash memory brings mobility and miniaturization to electronics products, two defining features of most consumer electronics products today.*[9]* These concerns proved to be unfounded as the flash memory market began to grow in the early 1990s (Table 1.1).

The flash memory devices are increasing interest for portable electronic productions because of its high data retention, low cost, and low power consumption characteristics.*[10, 11]* The basic concepts and the functionality of a floating gate (FG) device are easily understood if it is possible to determine the FG potential. The FG acts as a potential well. If a charge is forced into the well, it cannot move without

applying an external force: the FG stores charge. However, the conventional FG-NVM suffers from charge loss problem as the feature size of the device continues to shrink.*[12]* A discrete nanocrystal (NC) memory was then proposed as a replacement of the conventional FG memory.*[13]* The NC memory is expected to preserve the trapped charge efficiently due to the discrete charge storage node, while also demonstrate excellent features such as fast program/erase speeds, low programming potentials, and high endurance.*[14]* The chart of non-volatile memory history shows in Figure 1.3. Thanks to this characteristic, the nonvolatile memories offer the system a different opportunity and cover a wide range of applications, from consumer and automotive to computer and communication.

	Cell Phone	Consumer	Automotive	Computer & Communication
EPROM	Analog, Residential	Games, Set Top Box	Engine Mgt	HDD, Copiers, Fax, Switching
FLASH	Digital (GSM)	Set Top Box PDA	All Power Train Car Navigation, ABS, GPS	HDD, PC Bios, CDROM
EEPROM	Digital (GSM)	Audio, Video	All Car Body	PC SPD, Graphic boards, Printers

Figure 1.1 Main nonvolatile memory applications.

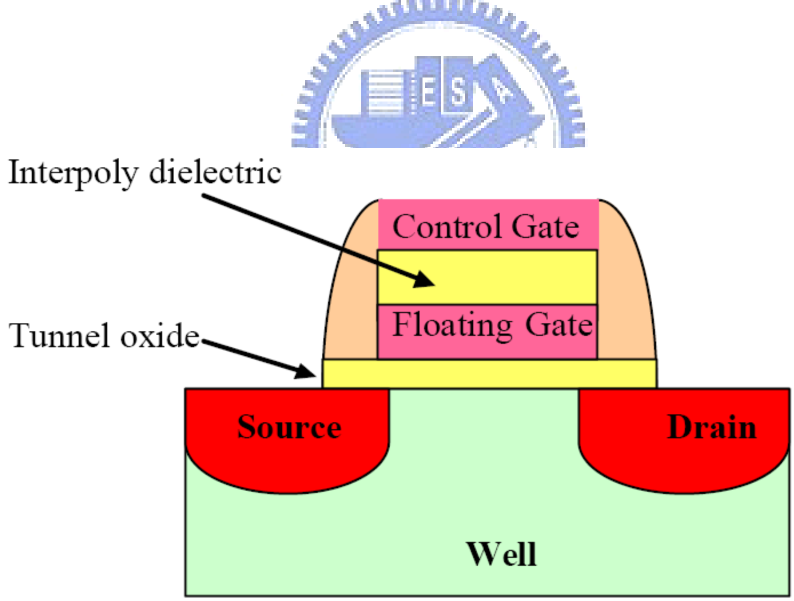

Figure 1.2 Schematic cross-section of a floating gate memory device.

Table 1.1 The rise of the flash memory market

	Flash memory market (USD Million)	Flash memory market annual percentage growth	Flash memory as a percentage of total semiconductor market	Flash memory as percentage of total memory market
1990	35		0.1	0.3
1991	135	286	0.3	1.0
1992	270	130	0.5	1.8
1993	640	106	0.8	3.0
1994	865	35	0.9	2.7
1995	1,860	115	1.3	3.5
1996	2,611	40	2.0	7.2
1997	2,702	3	2.0	9.2
1998	2,493	-8	2.0	10.8
1999	4,561	83	3.1	14.1
2000	10,637	133	5.2	21.6
2001	7,595	-29	5.5	30.5
2002	7,767	2	5.5	28.7
2003	11,739	51	7.1	36.1
2004	15,611	33	7.3	33.1
2005	18,569	19	8.2	38.3
2006	20,275	9	8.1	34.4

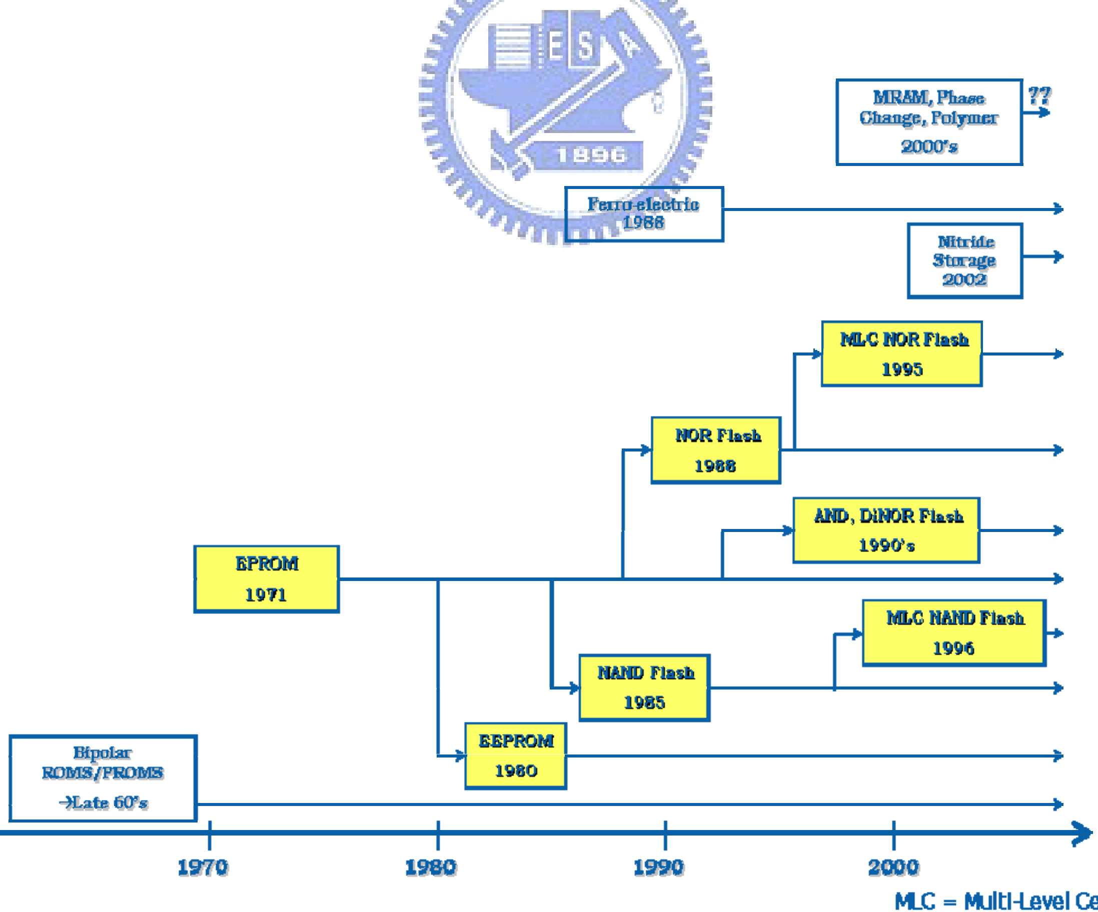

Figure 1.3 Non-volatile memory history.

1.2 Overview of flash memory devices

The Flash memories were commercially introduced in the early 1990s and since that time they have been able to follow the Moore's law, and the scaling rules imposed by the market. The cell size shrinkage of flash memory from 1992 to 2002 was shown in Figure 1.4. It turns out that the cell size decreases 30 times for each decade, closely following the scaling of the DRAM, today still considered as the reference memory technology that sets the pace to the technology node evolution.*[3]*

To address the scaling limitation of the insulators surrounding the floating gate, "thin film storage" (TFS) memories have been developed. Floating gate structure has been widely used for nonvolatile memory application. The schematic cross section of a floating-gate memory device is shown in Figure 1.5. Instead of using floating gates, charges are stored in a thin insulating film which contains storage sites such as traps or small silicon crystals. The charges cannot move easily from site to site, and therefore a single oxide defect does not lead to complete charge loss.*[15]*

The study of flash memory in the recent 30 years was focused on the charge storage layer, as shown in Figure 1.6. The nitride layer is sandwiched between a thin bottom oxide and a blocking oxide.*[16]* SONOS devices trap charge in a nitride layer instead of using a poly-silicon floating gate. Within the nitride layer, electrons and holes can be stored in localized traps, with negligible lateral conduction. However, SONOS-type flash memories have several drawbacks such as shallow trap energy level, erase saturation and vertical stored charge migration.*[17]* The programming speed and operating voltage problem can be solved by reducing the tunnel oxide thickness, while seriously degrades the retention capability of the memory*[18]*.

Due to the drawbacks of the conventional FG device prone to failure of the FG isolate, nanocrystal nonvolatile memory with the FG of the distributed charge storage

structure and long-term nonvolatile was introduced. As shown in Figure 1.7, "nanocrystal" refers to a crystalline structure whose dimensions are small enough to the nanometer scale that its electronic properties begin to resemble those of an atom or molecule rather than those of the bulk crystal. Nanocrystal memories can achieve better reliability and higher bit density than conventional non-volatile memories and thus, have been drawing much attention. In a nanocrystal flash memory device, charge is stored in discrete, mutually isolated, and crystallized nanocrystals or dots. Each dot typically stores only a handful of electrons; collectively the charges stored in these dots control the channel conductivity of the memory transistor. The electrons stored in the nanocrystal directly above the defect will be affected since the nanocrystals are separated from each other by the gate oxide dielectric.*[19]* Given a large number of nanocrystals, the cell is immune to local defects of the tunnel oxide. Many efforts have been made to improve the performance of the NC based nonvolatile memory.*[20, 21]*

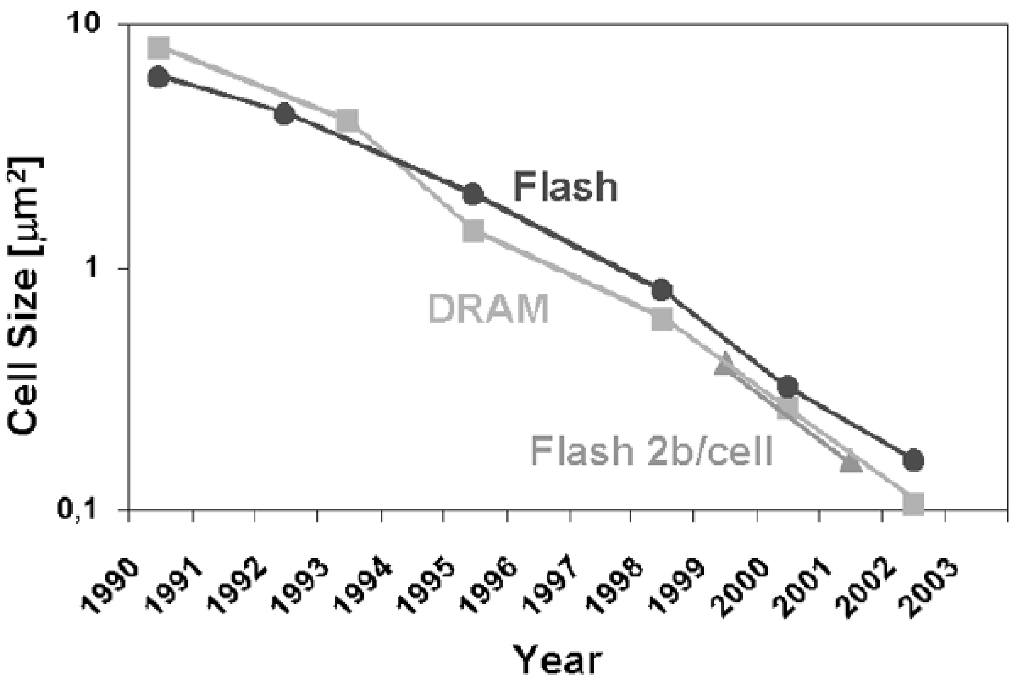

Figure 1.4 DRAM and Flash cell size reduction versus year. The scaling has been of about a factor 30 in ten years.

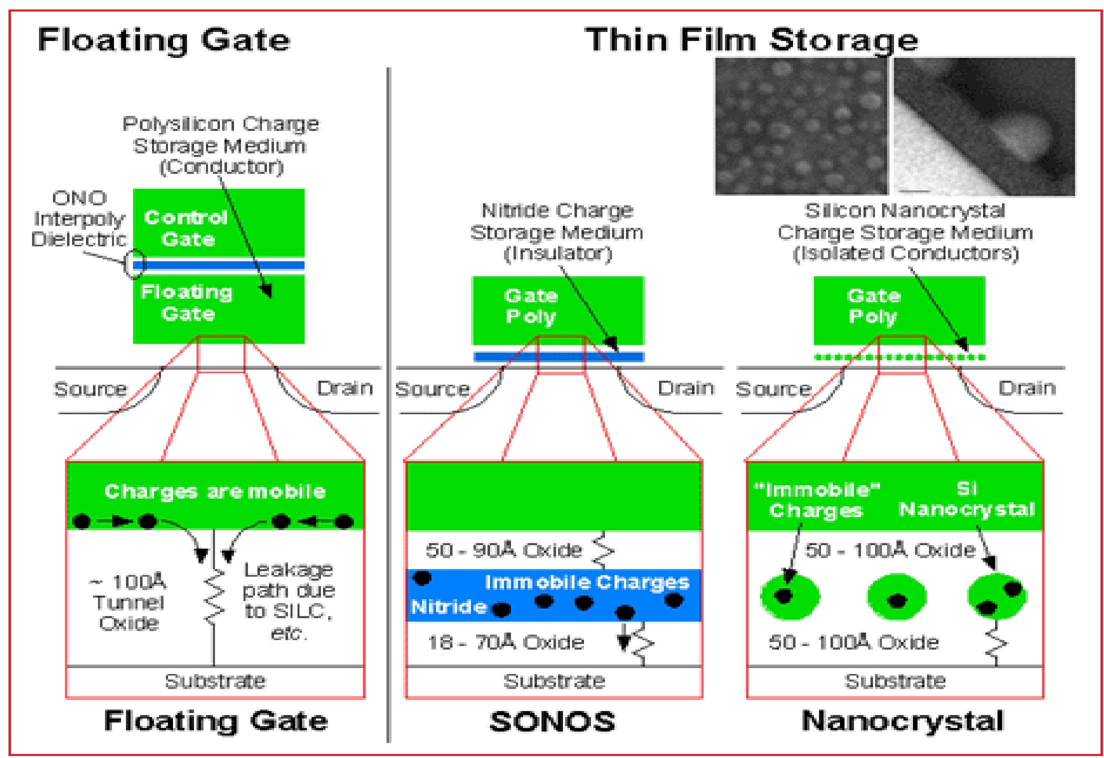

Figure 1.5 Schematics of floating gate and thin-film storage-based embedded nonvolatile memory bit cells. Depending on the charge stored inside the gate dielectric of a MOS field-effect transistor, the threshold voltage can be very high (off state) or so low that a read voltage applied to the poly-silicon gate can turn on the transistor (on state).

Source: Motorola Inc.

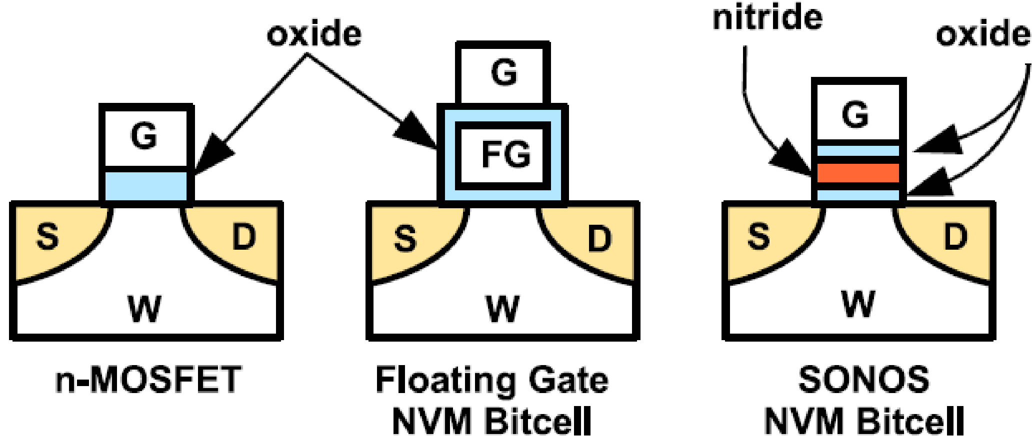

Figure 1.6 Operating principle of traditional NVM based on charge storage on floating gates or in nitride traps (SONOS), embedded into the gate oxide of a MOSFET.

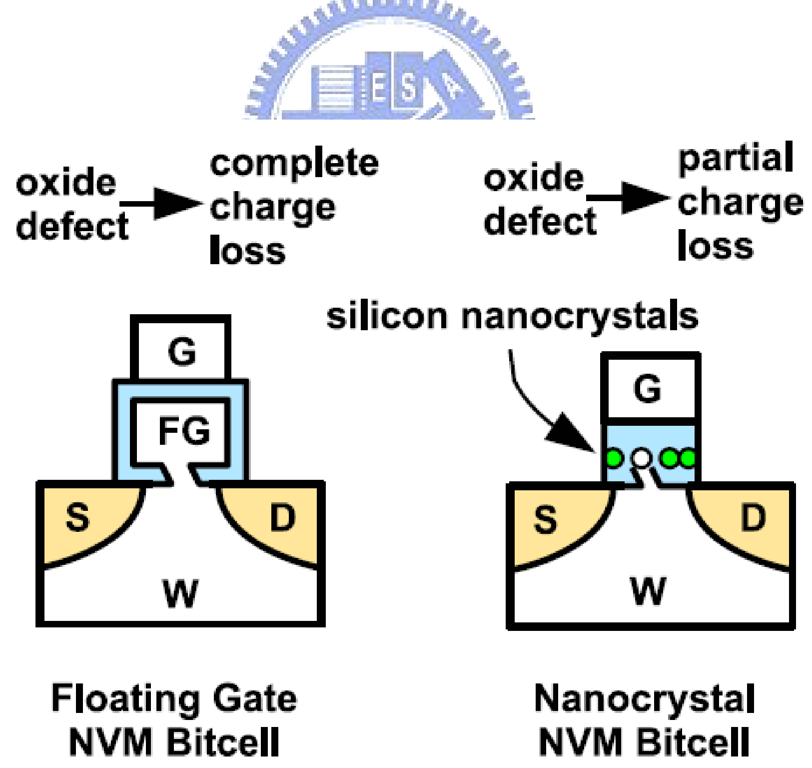

Figure 1.7 Schematic showing that one oxide defect can discharge the entire floating gate, whereas if localized charge is stored, only partial discharge occurs.

1.3 Sol-gel technology derived hybrid materials

The first, although incidental, observation of sol-gel process dates back to 1846. It covered the hydrolysis and poly-condensation of silicic acid under humidity, which progressed to the point of a silicate glass formation. An extension of the chemical principles involved was shown in 1969-1971, pointing out the importance of reactions of several metal alkoxides in solution under formation of metal (I)–oxygen–metal (II) bonds. This made the possibility of production of defined multi-component oxide glasses, glass-ceramics and crystalline layers. This research effort into the involved basic chemistry followed the path used in the study of reactions of metal-organic compounds.*[22]* Sol–gel processing has been widely used because it permits fabrication of oxide materials under mild conditions and with a wide range of adjustable experimental parameters. To give a very brief definition, a sol–gel procedure encompasses any process that involves polymerization of soluble precursor molecules to afford a polymeric material, via the intermediate formation of a colloidal sol phase. *[23]*

Sol-gel process contains fractal geometry and percolation theory in physics, hydrolysis and poly-condensation mechanism in chemistry, sintering and structural relaxation in ceramics, and so on. Figure1.8 illustrates the sol-gel process cycle. The sol-gel process allows synthesizing ceramic materials of high purity and homogeneity by means of preparation techniques different from the traditional process of fusion of oxides. This process occurs in liquid solution of organometallic precursors, by means of hydrolysis and condensation reactions, lead to the formation of a new phase (Sol). This method was derived from the known chemistry of reaction of a metal halide with a metal alkoxide acting as the oxygen donor. In this reaction, the condensation between M–X and M–O–R forms the M–O–M bridge with the elimination of alkyl

halide.*[23, 24]* Film-forming oxides are primarily Group 3 through Group 8 elements of the periodic table, such as Al, In, Si, Zr, Ti, Hf, Sn, Pb, Ta, Fe, Ni and several rare earth elements. They can exist as amorphous or (mostly) crystalline layers.*[22]*

Sol-gel processing can be divided into three main steps, that is, hydrolysis, condensation, and gelation (polymerization), as shown in Figure 1.9. The objective of these reactions is to generate the metal-oxygen-metal (M–O–M) bonds in the reacting solution that make up the oxide material. At hydrolysis step (hydrolysis), metal halides or metal alkoxides react with water to pass into hydroxo metals (≡M–OH) in sol-gel process. Then, two hydroxo metals (≡M–OH) reacts to an oxygen single bridge bond (–O–) between these two metal centers and an byproduct (water), which is called condensation step. Finally, gelation step proceeds continuous to condense numbers of hydroxo metals and link together to form a metal oxide network. The reaction of sol-gel solution and substrate surface are illustrated in Figure 1.10.

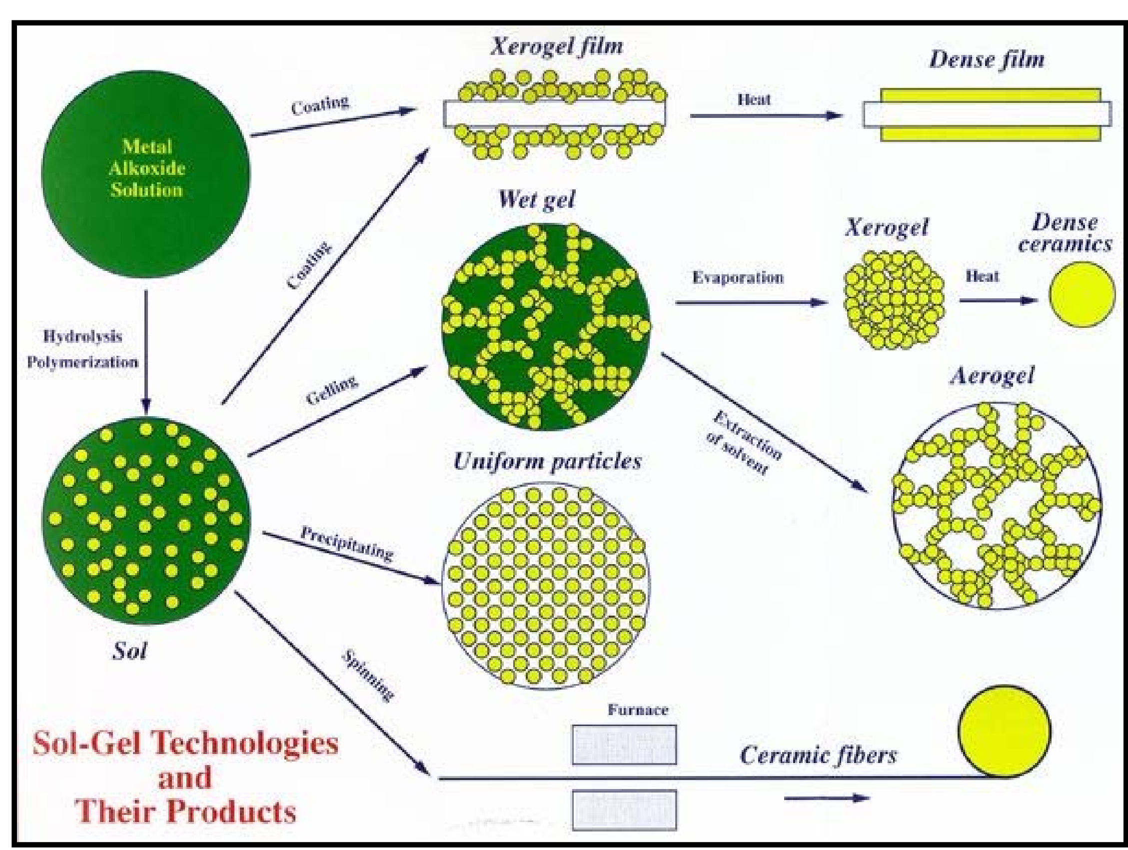

Figure 1.8 The sol-gel process cycle.

Figure 1.9 Basic steps of a typical sol–gel process.

Figure 1.10 The reaction of sol-gel solution and substrate surface.

1.4 Phase separation for spinodal decomposition

1.4.1 Spinodal decomposition

Spinodal decomposition is a method by which a mixture of two or more materials can separate into distinct regions with different material concentrations. This method differs from nucleation in that phase separation due to spinodal decomposition occurs throughout the material. With the advent of techniques capable of producing metastable crystalline phases with a grain size in the range of 10–100 nm (examples of such processes would include rapid solidification, laser processing and mechanical milling), there is considerable interest in phase transformations in such materials.*[25]*

The phenomenon of phase separation in glasses was discovered a long time ago. As early as 1904, Guertler *[26]* observed immiscibility in alkali borate melts. In general, there are two principal mechanisms of phase separation by nucleation and growth or alternatively by spinodal decomposition. The morphology of the resulting phases is different. If we wish to study phase separation in the unstable region, we must choose systems in which it is possible to bring a homogeneous solution through the metastable region without significant phase separation. Thus we should choose a system in which phase is slow compared with the time while it takes to change the temperature of the sample. The speed of phase separation is related to the diffusion coefficient, which is small for solids and viscous liquids, such as glass forming solutions.*[27]*

Fick's first law is used in steady-state diffusion, which is empirical in that it assumes that the diffusion flux is proportional to a concentration gradient. It would be more reasonable to assume that diffusion occurs in order to minimize the free energy so that the flux should be driven by a gradient of free energy:

$$J_A = -C_A M_A \frac{\partial \mu_A}{\partial x} \qquad \text{so that} \qquad D_A = C_A M_A \frac{\partial \mu_A}{\partial C_A}$$

where the (positive) proportionality constant M_A is known as the mobility of A; J is the diffusion flux; D is the diffusion coefficient or diffusivity; C is the concentration. In this equation, the diffusion coefficient is related to the mobility by comparison with Fick's first law. *[28]*

If $\partial \mu_A / \partial C_A > 0$ then the diffusion coefficient is positive and the chemical potential gradient is along the same direction as the concentration gradient. However, if $\partial \mu_A / \partial C_A < 0$ then the diffusion will occur against a concentration gradient. The diffusion coefficient will be zero when $\partial \mu_A / \partial C_A = 0$

Figure 1.11 illustrates the miscibility gap defined by curve ad which is obtained by applying the common–tangent construction. Any homogeneous solution cooled into the miscibility gap will tend to decompose into A–rich and B–rich regions with a net reduction in the free energy. The spinodal decomposition of region III is defined by the locus of the points of $(\partial \mu_A / \partial C_A = 0)$ inflexion on the free energy diagram as a function of temperature. Homogeneous solutions which are cooled within the chemical spinodal can in principle become unstable to infinitesimal perturbations in the chemical composition, leading to the development of A–rich and B–rich regions. Note that if a homogeneous solution is cooled into the region between the chemical spinodal and the miscibility gap, then large composition fluctuations are needed before phase separation can occur; this happens by a process known as nucleation and growth. *[29]*

Kingon and Maria were first to explain the observed microstructures with the presence of a liquid miscibility gap in the ZrO_2–SiO_2 system (Figure 1.12).*[30]* The reliable features in HfO_2–SiO_2 phase diagram coincide with features of the ZrO_2–SiO_2 phase diagram and Hf and Zr show very similar chemical behavior. In a metastable phase equilibrium one or more phases are absent. In the HfO_2–SiO_2 or ZrO_2–SiO_2

system, this is the crystalline silicate. Metastable phase diagrams and phase hierarchies are used widely in rapidly solidified alloys and can be applied to amorphous materials synthesized from precursors.*[31]* As shown in Figure 1.13, the situation is more complicated for the ZrO_2–SiO_2 system (and most likely for HfO_2–SiO_2) due to the presence of the liquid miscibility gap and the thermodynamically required spinodal.

1.4.2 Comparison with nucleation and spinodal decomposition

An initially homogeneous solution develops fluctuations of chemical composition when the condition fell into the spinodal region. During nucleation and growth, there is a sharp interface between the parent and product crystals; furthermore, the precipitate at all stages of its existence has the required equilibrium composition. Spinodal decomposition involves uphill diffusion whereas diffusion is always down a concentration gradient for nucleation. The growth of nucleation type and spinodal decomposition type are illustrated in Table 1.2.*[28]*

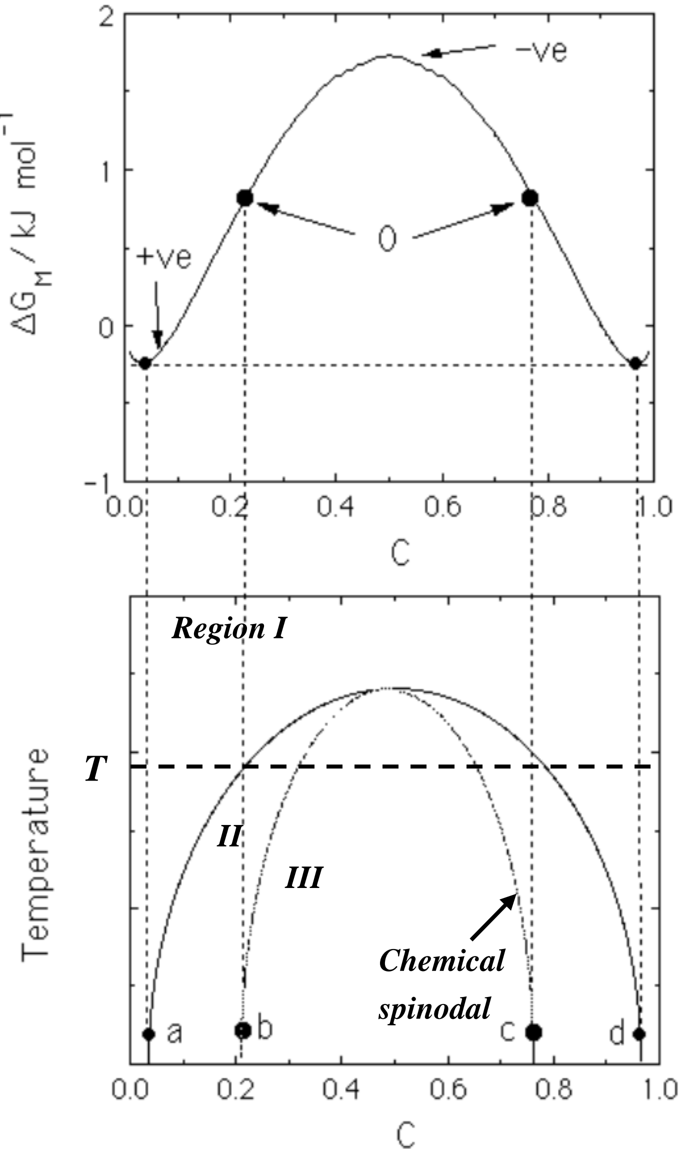

Figure 1.11 The miscibility gap and the chemical spinodal.

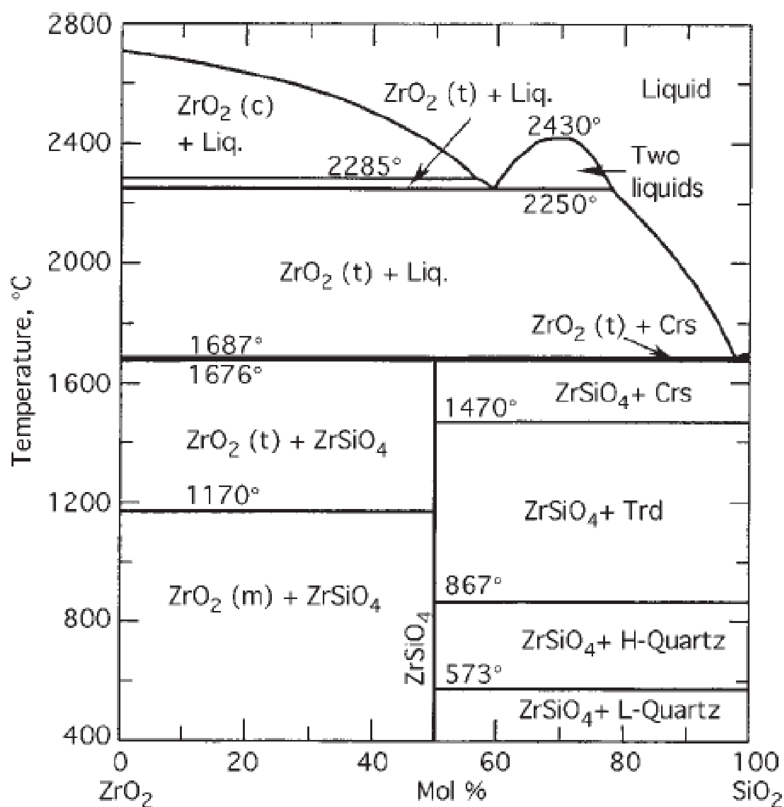

Figure 1.12 The pseudo-binary ZrO_2–SiO_2 phase diagram.*[31]*

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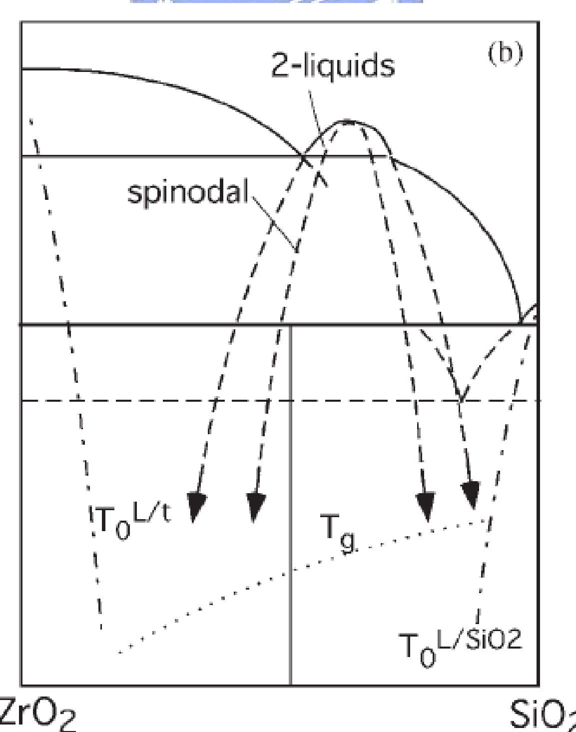


Figure 1.13 Metastable phase diagram with the extensions of the liquid miscibility gap and spinodal (dashed), the glass transition temperature (dotted line), and T_0 curves (dash-dotted line).*[31]*

Table 1.2 Comparison of nucleation and spinodal decomposition

Nucleation	Spinodal decomposition
Invariance of second-phase composition with time	Continuous variation of both extremes in composition with time
Interface between phases is always same degree of sharpness during growth	Interface between phases initially is very diffuse, eventually sharpens
Tendency for random distribution of particle sizes and position in matrix	Regularity of second-phase distribution in size and position characterized by a geometric spacing
Tendency for separation of second-phase spherical particles with low connectivity	Tendency for separation of second phase, non-spherical particles with high connectivity.

1.5 Motivation

The only stored charges at the nanocrystals adjacent to the defect leak through the tunneling dielectric, compared to huge charge loss of conventional Flash memory due to the lateral charge transport. This signifies that the NC memory has the ability to alleviate the scaling limitations of conventional Flash memory as well as extended the retention time.*[32]* Various materials have been used to form NCs, such as silicon *[33, 34]*, germanium (Ge) *[35]* and metal *[36]*, as the charge storage layer for nonvolatile memories.

In this thesis, we proposed a novel sol-gel spin coating method to fabricate high-κ material combined thin film, and annealing for driving the sol-gel film transformed into NCs. The sol-gel solution provided colloidal solvents or precursor compounds when metal halides were hydrolyzed under controlled conditions in a beaker. In the sol-gel reaction, hydrolysis, condensation, and polymerization steps occurred to form metal-oxide networks in the colloid liquid. The most interesting feature of sol-gel processing in the solution was its ability to synthesize new types of materials that were known as "inorganic-organic hybrids."*[24]* The film formation with sol-gel spin coating method was a simpler than ALD, PVD, or CVD technologies due to its cheaper precursors and tools. In addition, the film can be fabricated in the normal pressure environment instead of high vacuum system.

The crystallization of transferring the charge trapping thin film into the NC phase during thermal annealing was dependent on the composition of sol-gel solution, preparation solvent, and annealing temperature. The formation of coexisting hafnium silicate and zirconium silicate NC memory had been previously published.*[37, 38]* However, the effect of annealing temperature that controlled the formation of NC, degree of crystallization, interfacial energy, and charge retention in the sol-gel derived

memory was still unclear. The formation mechanism to explain the growth of nanocrystal was also still unclear. In the thesis, we had clarified the questionable point with physical and electrical characteristics studies.

Finally, we utilized the best NC formation condition to prepare charge trapping layer for a memory device. We expected the sol-gel derived nanocrystal memory devices with superior electrical characteristics in terms of large memory windows, high write/erase speed, long retention time, good disturbs, and excellent endurance performance.

Chapter 2

Nanocrystal Memory Device principles and operations

2.1 Fundamentals of the NC memory

Nonvolatile memory devices based on the charge storage in discrete charge traps such as semiconductor and metal nanocrystals (NCs) have recently attracted much attention in view of their potential application for high-density nonvolatile memory (NVM) devices.*[39]* The use of discrete charge-trap of nanocrystals offers an advantage of preventing lateral charge movement, thereby enhances the data retention characteristic.*[40]* The nonvolatile metal nanocrystal memory devices were extensively investigated over semiconductor nanocrystals because of several advantages, such as stronger coupling with the conduction channel, higher density of states (transport perspectives) than semiconductor (i.e., better charge storage), and a wide range of available work functions (faster programming speed and better data retention).*[6]*

2.2 NC Memory characteristics

2.2.1 Basic program/erase principle

The basic principle of programming the memory is that electrons or holes inject into the charge trapping layer and hence cause the threshold voltage shift. Figure 2.1(a)

shows the cross-section scheme of the nanocrystal memory device. The electrons/holes from channel are injected through tunneling oxide due to the horizontal field of controlling gate to Si-substrate, and therefore trapped into the nanocrystall. Two major mechanisms has been proposed to explain the program of the flash memory, that is, Fowler-Nordheim (FN) tunneling and channel hot-electron injection (CHEI). The energy bands of the nanocrystal memory device at program and erase are illustrated in Figure 2.1(b) and 2.1(c), respectively. During the program process, a positive gate voltage is applied to inject channel inversion-layered electrons into the nanocrystals. During the erase process, a negative gate bias is applied to cause the accumulation layered holes to inject into the nanocrystal and recombine with the trapped electrons..*[8]* The program and erase process result in the shifting of the threshold voltage, which is proportional to the quantities of trapped charges.

Program

The CHEI mechanism is generally used in flash memories, where a lateral electric field (from drain to source) "heats" the electrons and a transversal electric field (from controlling gate to channel) injects the hot carriers through the oxide. The physical mechanism of CHEI is relatively simple depicted in Fig 2.3. An electron traveling from the source to the drain gains energy from the lateral electric field and loses energy to the lattice vibrations (acoustic and optical phonons).*[41]* At large drain bias, the minority carriers that flow in the channel are heated by the large electric fields occurred at the drain side of the channel and their energy distribution is shifted higher. For fields exceeding this value, electrons are no longer in equilibrium with the lattice, and their energy relative to the conduction band edge begins to increase. Electrons are "heated" by the high lateral electric field, and a small fraction of them have enough energy to surmount the barrier between oxide and silicon

conduction band edges. For an electron to overcome this potential barrier, three conditions must hold.*[42]*

(1) Its kinetic energy has to be higher than the potential barrier.

(2) It must be directed toward the barrier.

(3) The field in the oxide should be collecting it.

Erase

Charge-trapping memory is erased by band-to-band tunneling hot hole (BBHH) injection, under which condition the drain is positively biased and the gate negatively biased. Due to the hot hole injection mechanism, BBHH injection has the advantage of a lower voltage bias and a faster erasing speed than the FN tunneling.*[42]*

During the erase operation, holes are injected from the p-type substrate into the charge trapping layer valence band. These holes "trap" at the top oxide interface because of the large barrier height. Electrons may tunnel from an n^+ gate into charge trapping layer and combine with the injected holes. Band-to-band tunneling process that occurs in the deeply depleted n^+ surface region under gate-to-drain overlap area is another method used to erase the SONOS memory device. This mechanism is to simultaneously apply a negative voltage to the gate and a positive voltage to the drain. Then the hot holes are injected through the bottom oxide and recombine with the stored electrons. Figure 2.4 illustrates the hot holes injection generated by band-to-band tunneling process.

2.2.2 Basic reliability principle

2.2.2.1 Retention

As in any nonvolatile memory technology, Flash memories are specified to retain data for over ten years. This means the loss of charge stored in the charge-trapping

layer must be as minimal as possible.*[3]* Possible causes of charge loss are: (1) defects in the tunnel oxide; (2) defects in the interpoly dielectric; (3) mobile ion contamination; and (4) detrapping of charge from insulating layers surrounding the charge-trapping layer. During the retention mode, the electrons inside the nanocrystal can not be stored in the conduction band for several reasons.*[43]* The generation of defects in the tunnel oxide can be divided into an extrinsic and an intrinsic one. The former is due to defects in the device structure; the latter to the physical mechanisms that are used to program and erase the cell. The electrons can subsequently detrap with time, especially at high temperature. The charge variation results in a variation of the charge-trapping layer potential and thus in cell decrease, even if no leakage has actually occurred. This apparent charge loss disappears if the process ends with a thermal treatment able to remove the trapped charge.

The retention capability of flash memories has to be checked by using accelerated tests that usually adopt screening electric fields and hostile environments at high temperature.

2.2.2.2 Endurance

Cycling is known to cause a fairly uniform wear-out of cell performance, which eventually limits Flash memory endurance.*[44]* As the experiment was performed applying constant pulses, the variations of program and erase threshold voltage levels are described as "program/erase threshold voltage window closure" and give a measure of the tunnel oxide aging. In particular, the reduction of the programmed threshold with cycling is due to trap generation in the oxide and to interface state generation at the drain side of the channel, which are mechanisms specific to hot-electron degradation. The evolution of the erase threshold voltage reflects the dynamics of net fixed charge in the tunnel oxide as a function of the injected charge.

The initial lowering of the erase is due to a pile-up of positive charge which enhances tunneling efficiency, while the long-term increase of the erase is due to a generation of negative traps. A typical result of an endurance test on a single cell is illustrated in Figure 2.5.

2.2.2.3 Disturbance

The first failure phenomenon, "program disturbance," often takes place under the electrical stress applied to those neighboring un-programmed cells during programming a specific cell in the array. Two types of program disturbances, gate (word-line, or WL) disturbance and drain (bit-line, or BL) disturbance need be considered.*[3]* In Figure 2.6, shows the schematic circuitry of the memory array. During programming cell A, gate disturbance occurs in the cell B and same for those cells connected with the same word-line because the gate stress is applied to the same word-line. During programming cell A, drain disturbance occurs in the cell C and same for those cells connected with the same bit-line because the drain stress is applied to the same bit-line. For the cell reading, the unwanted electron injection would happen while the word-line voltage and bit-line voltage are under read operation. This phenomenon would result in a significant threshold voltage shift of our selected reading cell. This is call read disturbance.

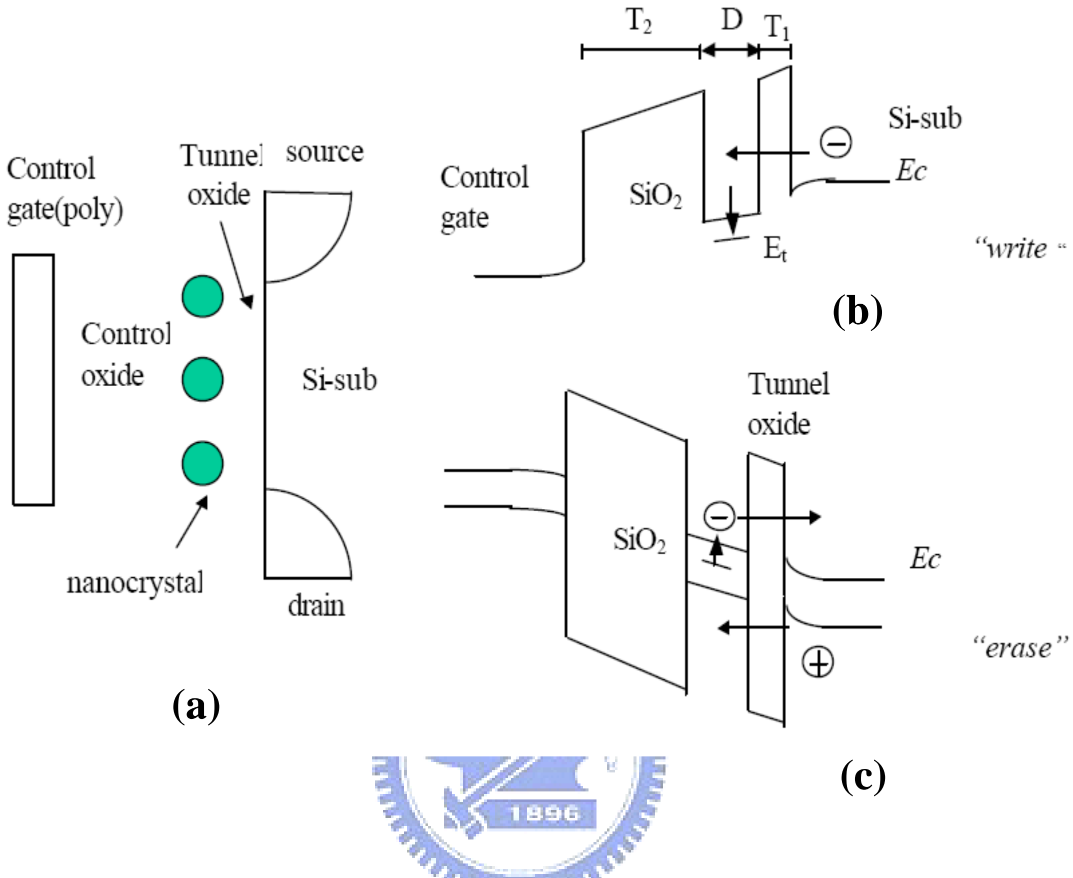


Figure 2.1 (a) Schematic cross-section of nanocrystal memory device structure; (b) illustration of write process: inversion- layer electron tunnels into the nanocrystal; (c) illustration of erase process: accumulation layer hole tunnels into the nanocrystal, electron in nanocrystal can tunnel back to the channel.

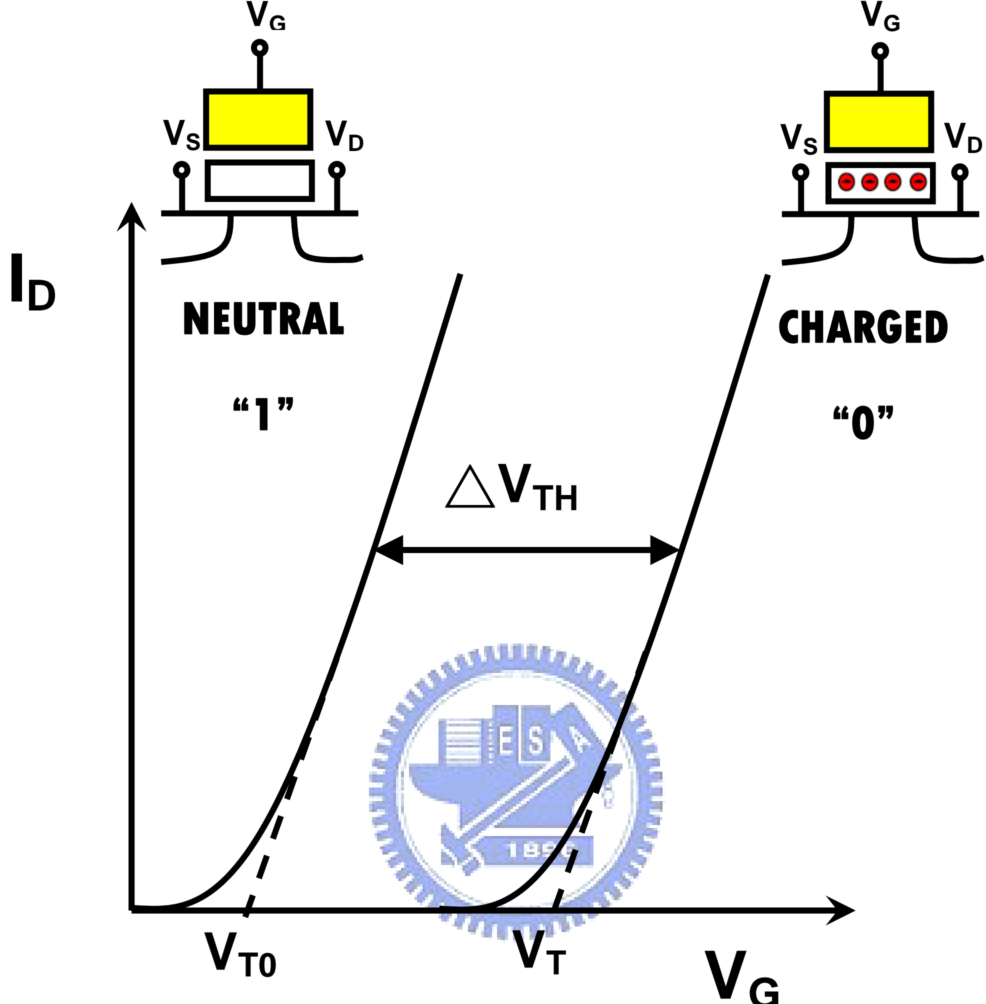


Figure 2.2 Id–Vg curves of an FG device when there is no charge stored in the FG (neutral) and when a negative charge is stored in the FG (charged).

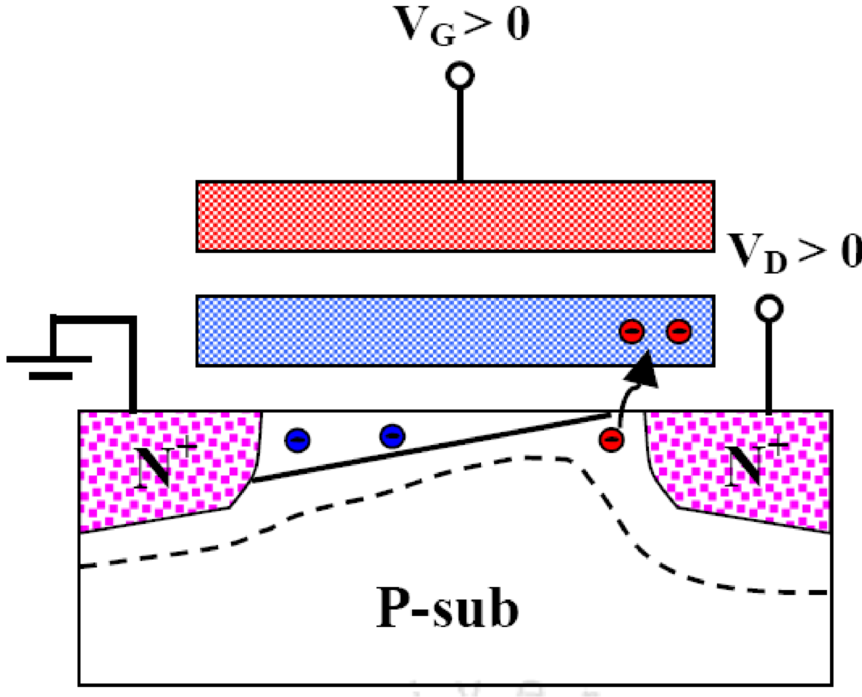


Figure 2.3 The procedure of hot electrons injection.

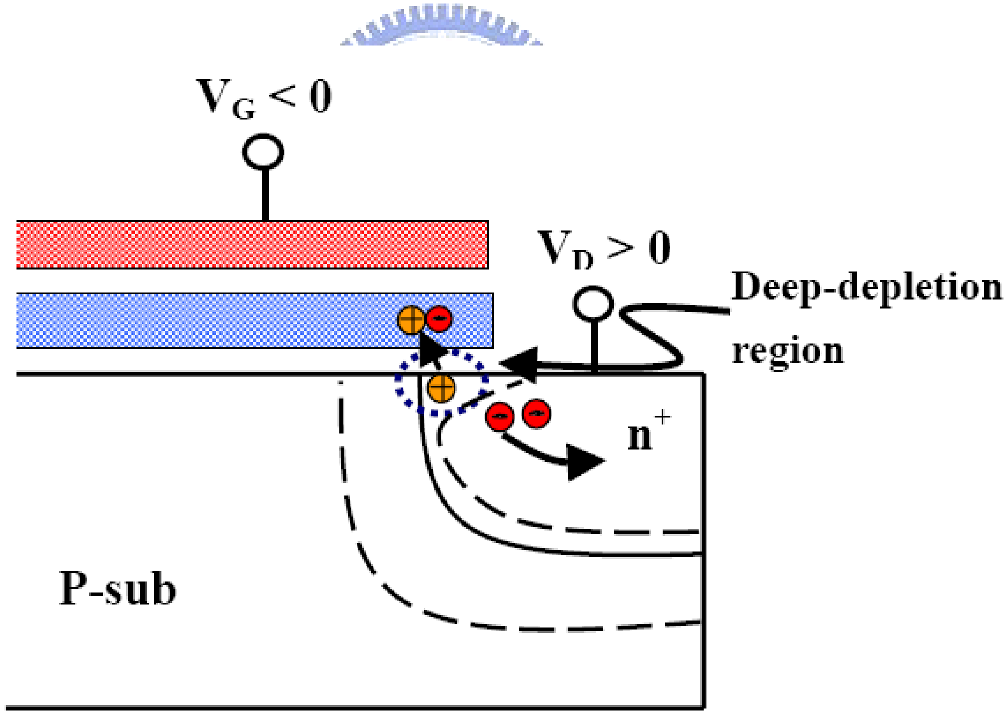


Figure 2.4 The hot holes injection generated by band-to-band tunneling.

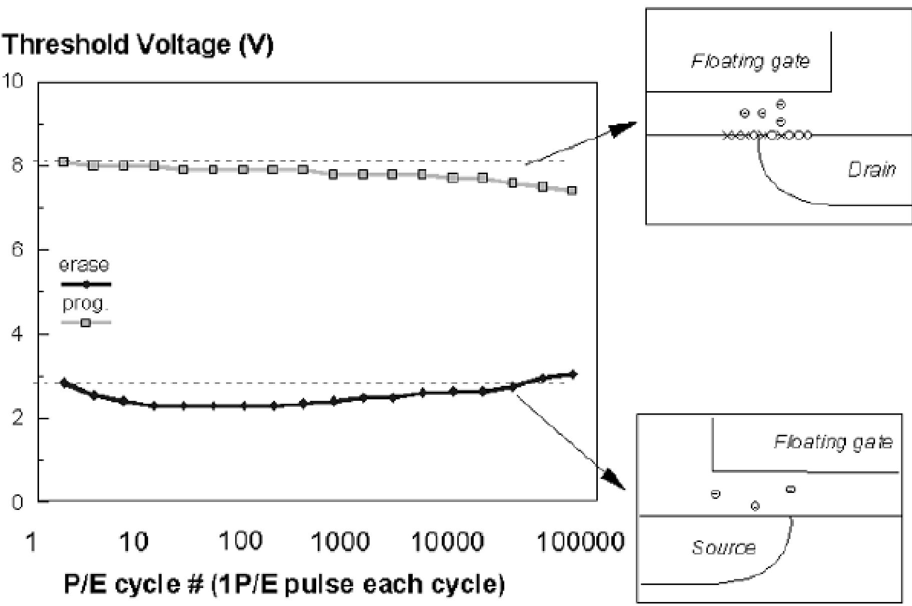


Figure 2.5 Threshold voltage window closure as a function of program/erase cycles on a single cell.

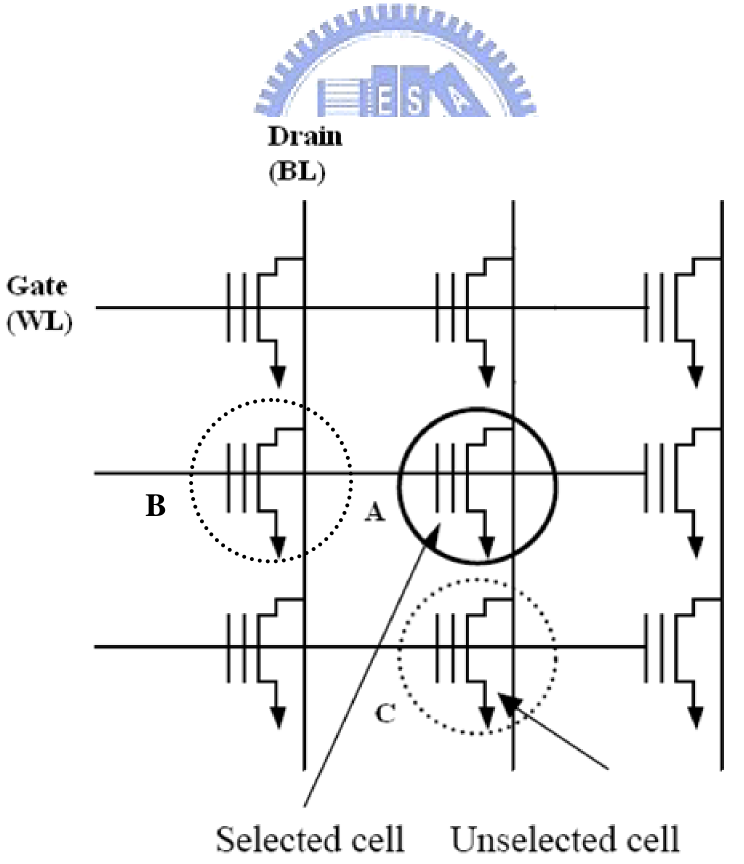


Figure 2.6 The schematic illustrates the disturb condition. Cell A is the programming cell. Cell B and Cell C perform the gate disturb and drain disturb, respectively.

Chapter 3

Nanocrystallization and interfacial tension of charge trapping layer

3.1 Introduction

In the recent years, the emphasis of material design has dramatically changed towards a general understanding and control of the fundamental connections between the chemistry on a molecular level and material properties on the macroscopic scale. Looking towards the 21st century, advances in information processing, communication (microelectronics), medicine etc. require miniaturized materials with superior properties and performance. "Nanotechnology", which is essentially material science on a nanometer scale, is a subject that combines the efforts of scientists in interdisciplinary research (physicists, chemists and material scientists).

According to the International Technology Roadmap for Semiconductors, there are critical limitations for aggressively scaling the conventional nonvolatile floating-gate memories below sub-70-nm node. For conventional SONOS, erase saturation and vertical stored charge migration*[45]* are the major drawbacks; while for nanocrystal memories good enough charge keeping capability of the discrete storage nodes and the formation of nanocrystals with constant size, high density and uniform distribution are the extremely challenging issues.*[46]* Therefore, the poly-silicon–oxide–nitride–oxide–silicon (SONOS)-type memories including nitride

memories and nanocrystal memories have recently attracted much attention for the application in the next-generation nonvolatile memories*[35, 47, 48]* because of their great potential for achieving high program/erase (P/E) speed, low programming voltage and low power performance.

The conventional floating gate (FG) nonvolatile memory (NVM)*[39, 49]* suffers from a charge loss problem as the feature size of the device continues to shrink.*[50]* A discrete nanocrystal (NC) memory was then proposed as a replacement of the conventional FG memory. The NC memory is expected efficiently to preserve the trapped charge due to the discrete charge storage node, while also demonstrate excellent features such as fast program/erase speeds, low programming potentials, and high endurance. We have proposed a sol-gel spin-coating method to fabricate the charge trapping film that can be fabricated in a normal atmospheric pressure instead of high-vacuum system. Many methods to fabricate nanocrystals (NCs) have been widely investigated recently such as physical vapor deposition (PVD), chemical vapor deposition (CVD), and ion beam synthesis. In addition to these deposition methods, a NC formation process by using sol–gel spin-coating method has been reported by our group.*[38]* Compare to others, the benefit of sol–gel spin-coating method is relatively cheap, simple, and can be fabricated in a normal atmospheric pressure instead of high-vacuum system. In addition, the ability to synthesize new type of materials that are known as "inorganic–organic hybrids" will induce various application of the sol–gel processing.

Sol-gel process contains fractal geometry and percolation theory in physics, hydrolysis and poly-condensation mechanism in chemistry, sintering and structural relaxation in ceramics, and so on. When sol is prepared with starting materials of molecular unit, a solid fractal network is obtained through hydrolysis and condensation reaction. Then an improved properties of ceramic could be obtained by

removing inhomogeneity in materials through the control of chemical reaction concerning with inorganic polymerization.*[51]* Transition metal oxides are widely used in many important technological applications such as solar energy conversion, catalysis, magnetic recording, sensors, and ceramics. Yet compared to the intensive study of nanocrystals of semiconductors and metals, relatively little work has been done on the metal oxides.*[24, 52]*

The crystallization of transferring the charge trapping thin film into the NC phase during thermal annealing is dependent on the sol-gel composition, preparation solvent, and annealing temperature. The formation of coexisting hafnium silicate and zirconium silicate NC memory has been previously published.*[37]* In general, the NC formation is related to the solid phase segregation induced seeding effect.*[53]* However, the effect of annealing temperature that controls the formation of NC, degree of crystallization, interfacial energy, and charge retention in the sol-gel derived memory is still unclear.

3.2 Experimental

3.2.1 Formation of sol-gel derived thin film/nanocrystals

Prior to various annealing treatments, the sol-gel thin film was deposited by the spin-coating method from the precursors of zirconium tetrachloride, hafnium tetrachloride, and silicon tetrachloride. The sol-gel solution was prepared as the experiment procedure flow which was shown in Figure 3.1. The solution were synthesized by the sol-gel method using the precursors of the analytical reagent graded zirconium tetrachloride ($ZrCl_4$, 99.5%, Aldrich, USA), hafnium tetrachloride ($HfCl_4$, 99.5%, Aldrich, USA), and silicon tetrachloride ($SiCl_4$, 99.5%, Aldrich, USA). The above precursors were dissolved in ethanol, and a suitable amount of

hydrochloric acid serving as the catalyst was added into the solution for hydrolysis and condensation. Then, we mixed $ZrCl_4$, $HfCl_4$, and $SiCl_4$ solutions together for preparing the sol-gel solution for following experiment. The concentration of molar ratio for $ZrCl_4$, $HfCl_4$, $SiCl_4$, and ethanol in the sol-gel solution was 1:1:1:1000. The mixed solution was stirred for 0.5 hr at room temperature. After well mixed, we spin coated the sol-gel solution on the silicon substrates at rotation speed of 3000 rpm for 60 sec at room temperature by using a Tokyo Electron Limited (TEL) system (Clean Track Model-MK8). Afterwards, these samples were subjected to rapid thermal annealing (RTA) treatment at various temperatures for 60 sec under an O_2 ambient. Finally, the samples were subjected to XPS, TEM, AFM, and interfacial energy analyses.

3.2.2 Memory device fabrication

The fabrication of sol-gel spin-coating NC memory was started with local oxidation of Si process on a p-type (100) silicon substrate. A 10 nm tunneling oxide film was thermally grown at 925 °C in a furnace. The sol-gel film was then formed through sol-gel spin coating and RTA process mentioned above. The 20 nm blocking oxide was deposited by plasma enhanced chemical-vapor deposition (PECVD) tetraethylorthosilicate (TEOS). Followed by a 200-nm-thick amorphous Si gate was deposited. Finally, gate pattering, source/drain (S/D) implanting, and the rest of the subsequent metal-oxide-semiconductor (MOS) processes were used to fabricate the NC-NVM devices.

3.3 Results and discussion

3.3.1 RTA temperature effect of sol-gel film transformation

The high resolution structural characterization of the NCs was carried out by the high-resolution transmission electron microscopy (HRTEM, JEOL2100F) operated at 300 kV. The cross-sectional TEM images of the sol-gel derived thin films samples that annealed at 400, 600, and 900 °C were illustrated in Figure 3.2. The sample in Figure 3.2(a) by 400 °C RTA treatment exhibited a continuous and smooth film. This observation suggested the annealing temperature at 400 °C has no effect on the film's morphology. As to the sample annealing at 600 °C, Figure 3.2(b) revealed the morphology of thin film was discontinuous and uneven. If the annealing temperature was elevated to 900 °C, the film illustrated in Figure 3.2(c) was complete transferred into isolated NCs. Each crystal size of the TEM image was estimated to be 6–10 nm. Literature had proposed the spinodal decomposition effect*[31]* to explain the annealing effect for formation of zirconium silicate. We inferred that the darker NCs in Figure 3.2(c) were formed from the high–molecular–weight hafnium silicate, and the bright NCs were from the low–molecular–weight zirconium silicate.*[37]* Figure 3.3 shows the elemental composition of the binary metal oxides NCs which were estimated by energy dispersive X-ray spectroscopy (EDS).

The nature of the chemical bonding for the transformation of thin film into NC was characterized by using x-ray photoelectron spectroscopy (XPS) analysis. Figure 3.4 provided a comparison of the XPS results for (a) Si 2p, (b) Zr 3d, (c) Hf 4f, and (d) O 1s bonding for samples annealed at different temperatures. Figure 3.4(a) showed the increasing of binding energy of Si 2p from 100.40 eV (400 °C RTA) to 100.95 eV (900 °C RTA) with various annealing temperature. This observation related to the oxidization of the Si atom toward spectrum blue-shift. Both binding energies of Zr 3d

and Hf 4f shown in Figs. 3.4(b) and (c) exhibited the shifting to the higher energies upon increasing the annealing temperature. This observation suggested that the oxygen atoms of Zr–O and Hf–O bonds reacted with their nearby Si atoms, forming hafnium and zirconium silicate.*[54]* As to the O 1s spectra in Figure 3.4(d), each peak can be deconvoluted into two peaks, i.e., the higher and lower energy peaks, which were respectively attributed to the SiO_2 and metal-rich silicate.*[6]* If the annealing temperature was increased, the intensity ratio of lower energy peak to higher energy peak was increased. This result indicated the hafnium and zirconium silicates were toward the bonding of metal-rich silicate. This finding was also consistent with the observation of Hf 4f and Zr 3d spectra.

3.3.2 Interfacial tension analysis

Figure 3.5 showed the interfacial tension (interfacial energy per unit area) of the hafnium and zirconium silicates as a function of annealing temperature. The surface free energy was evaluated using van Oss and Good's three-liquid acid-base method. According to this approach (refer to equation (1)), the surface free energy of a solid, γ_s, can be calculated from a combination of three factors:

$$\gamma_S = \gamma_S^{LW} + \gamma_S^{AB} = \gamma_S^{LW} + 2\sqrt{\gamma_S^{+}\gamma_S^{-}} \qquad (1)$$

Where γ^{LW} is the Liftshitz/van der Waals component, γ_s^{AB} is the acid-base component, γ^{+} is the Lewis acid component, and γ^{-} is the Lewis base component. Values of γ_s^{LW}, γ_s^{+}, and γ_s^{-} can be calculated from equation (2) after measuring the liquid-solid contact angles (θ) of these three characterizing liquids.

In equation (2), γ_L is the surface tension of the liquid, and subscripts S and L refer to solid and liquid, respectively. Diiodomethane was selected as the apolar liquid, and water and ethylene glycol were selected as the polar liquid pair. The surface energy of these three liquids shows in Table 3.1. The calculated surface free energies

of the thin films follow similar trends to those observed for the advancing contact angles.

$$\begin{aligned}
\gamma_{L1}(1+\cos\theta_1) &= 2\left(\sqrt{\gamma_S^{LW}\gamma_{L1}^{LW}}+\sqrt{\gamma_S^{+}\gamma_{L1}^{-}}+\sqrt{\gamma_S^{-}\gamma_{L1}^{+}}\right)\\
\gamma_{L2}(1+\cos\theta_2) &= 2\left(\sqrt{\gamma_S^{LW}\gamma_{L2}^{LW}}+\sqrt{\gamma_S^{+}\gamma_{L2}^{-}}+\sqrt{\gamma_S^{-}\gamma_{L2}^{+}}\right)\\
\gamma_{L3}(1+\cos\theta_3) &= 2\left(\sqrt{\gamma_S^{LW}\gamma_{L3}^{LW}}+\sqrt{\gamma_S^{+}\gamma_{L3}^{-}}+\sqrt{\gamma_S^{-}\gamma_{L3}^{+}}\right)
\end{aligned} \quad (2)$$

As Figure 3.5 depicted, the interfacial energy of sol-gel spin coated film that abruptly increases from 400 °C to 600 °C annealing, and then slightly decreases from 600 °C to 1050 °C. The advancing contact angle of the polymer surface was measured by using Krüss GH-100 goniometer with deionized water, ethylene glycol, and diiodomethane as the standard solution to measure the surface free energy of the sol-gel film. The sol-gel thin film is thermodynamically not stable due to their high surface energy, therefore it nucleate whereby it is stabilized with the surface energy decrease.

As Figure 3.2 (a) mentioned, the surface at 400 °C RTA is still smooth and possesses the lowest energy. The surface morphology of 600 °C RTA sample is rough in Figure 3.2 (b), implying that the surface is unstable and in higher energy state. At 900 °C RTA, the interfacial energy is decreased in comparison with 600 °C RTA due to the formation of NCs. We proposed a model in Figure 3.6 to describe the observed transformation phenomenon on the sol-gel spin-coating film. The sol-gel film is continuous and smooth as deposited and retains the same morphology at 400 °C annealing. It becomes unstable at 600 °C annealing, and phase separation is then observed in order to reduce the surface energy. Upon 900 °C annealing, the sol-gel film reaches a stable state due to the formation of NCs.

Table 3.1 The surface-free-energies (γ) of diiodomethane, water and ethylene glycol.

	σ_L^{LW} (mJ/cm²)	σ_L^{+} (mJ/cm²)	σ_L^{-} (mJ/cm²)	σ_L^{total} (mJ/cm²)
water	21.8	25.5	25.5	72.8
ethylene glycol	29	1.92	47	48
diiodomethane	50.8	0	0	50.8

3.3.3 Comparison of data retention

The sol-gel derived NC was used as the charge trapping that purposed in the nonvolatile nanocrystal memory (NVM) device. Figures 3.7 (a) and (b) illustrated the retention characteristics for the devices annealed at 600 °C and 900 °C, respectively. For both 600 ^{o}C and 900 ^{o}C samples at 25 °C measurement, the retention times can be extrapolated up to 10^6 sec for only about 5% charge loss, while less then 10% charge loss at 85 °C measurement. As the testing temperature increased to 125 °C, a significant charge loss at 10^6 sec was observed for the 600 °C annealed sample, while the 900 °C annealed sample still retained its good characteristic for retention time of 10^5 sec with less then 20% charge loss. The result explained the importance of NC formation for the NVM. The NC discretely dispersed in the charge trapping layer, which alleviated the charge loss problem when defects existed in the thin tunneling oxide and immunized to stress induced leakage current (SILC) effect.

3.4 Summary

In conclusion, we discussed the morphology of sol-gel derived charge tapping layer with different annealing temperatures. The XPS characterization indicated the annealing treatment under oxygen ambient can activate the formation of metal silicates (i.e., hafnium silicate and zirconium silicate). Together with the TEM images

and interfacial energies, we proposed a mechanism to explain the process of sol-gel thin film transformation into NCs. We observed the 400 °C RTA treatment had no effect on the thin film, while 600 °C and 900 °C anneals affected the film's phase separation. The film during phase separation exhibited higher interfacial energy (600 ^{o}C RTA) and after transformation to NCs can minimize the interfacial energy (900 ^{o}C RTA). The sol-gel derived NCs successfully played an important role of charge trapping purposed in NC memory device. The 900 °C annealed sample demonstrated the satisfactory retention characteristic than the 600 °C annealed sample due to the NC formation. The large V_{th} shift of the 900 °C annealed sample was potential for future multi-bit application.

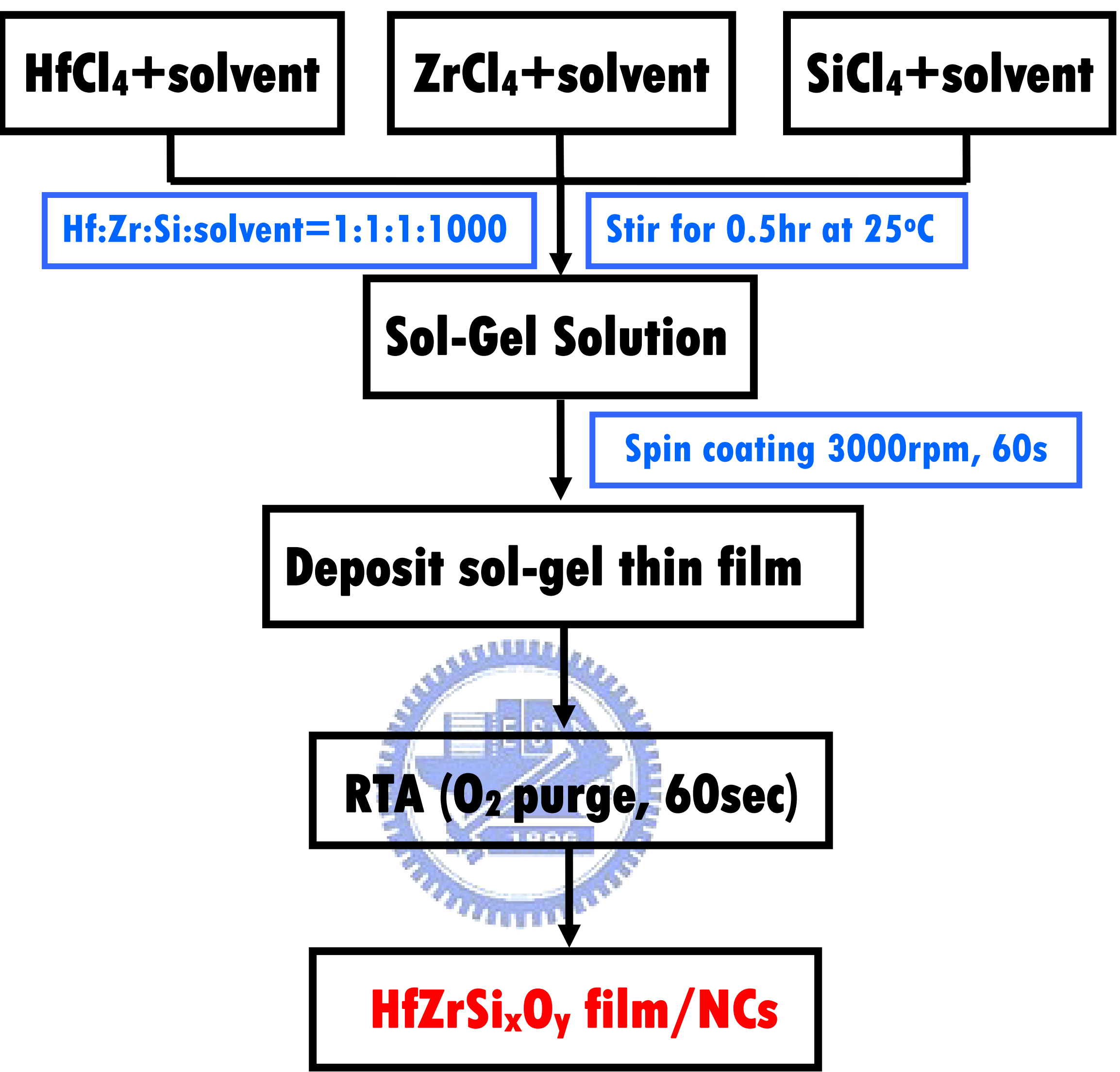


Figure 3.1 The experimental procedure flow of $HfZrSi_xO_y$ film/NCs preparation by sol-gel technique.

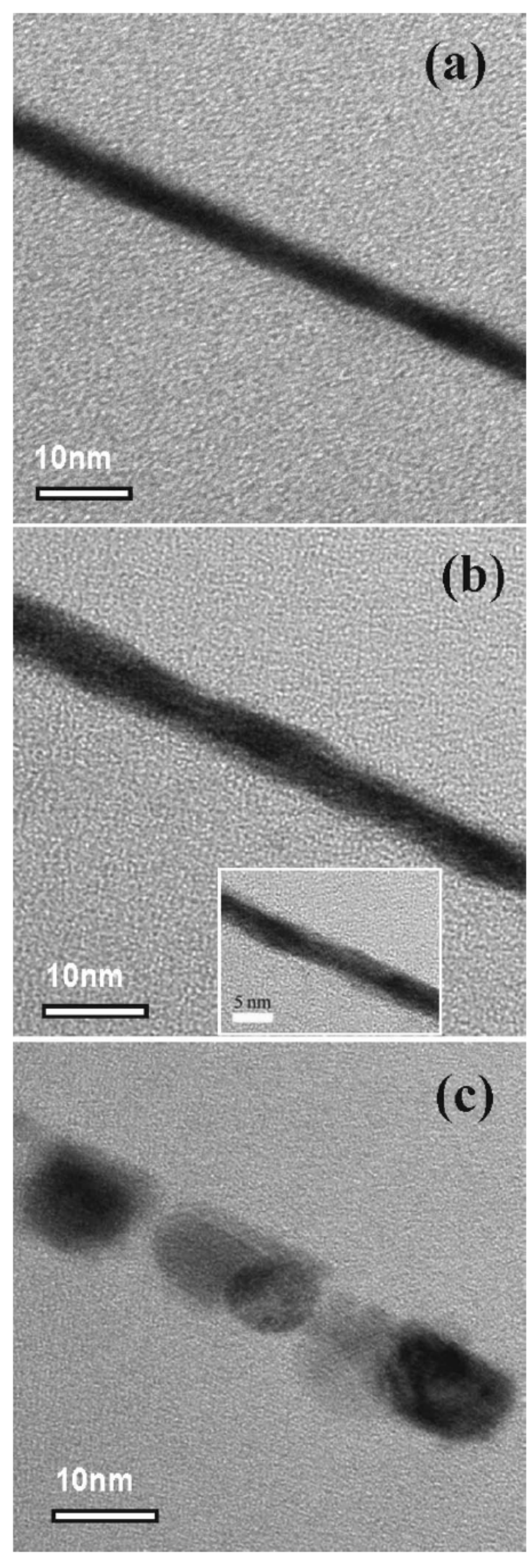


Figure 3.2 Cross-sectional TEM images of the thin film transformation with (a) 400 °C, (b) 600 °C, and (c) 900 °C annealing treatments.

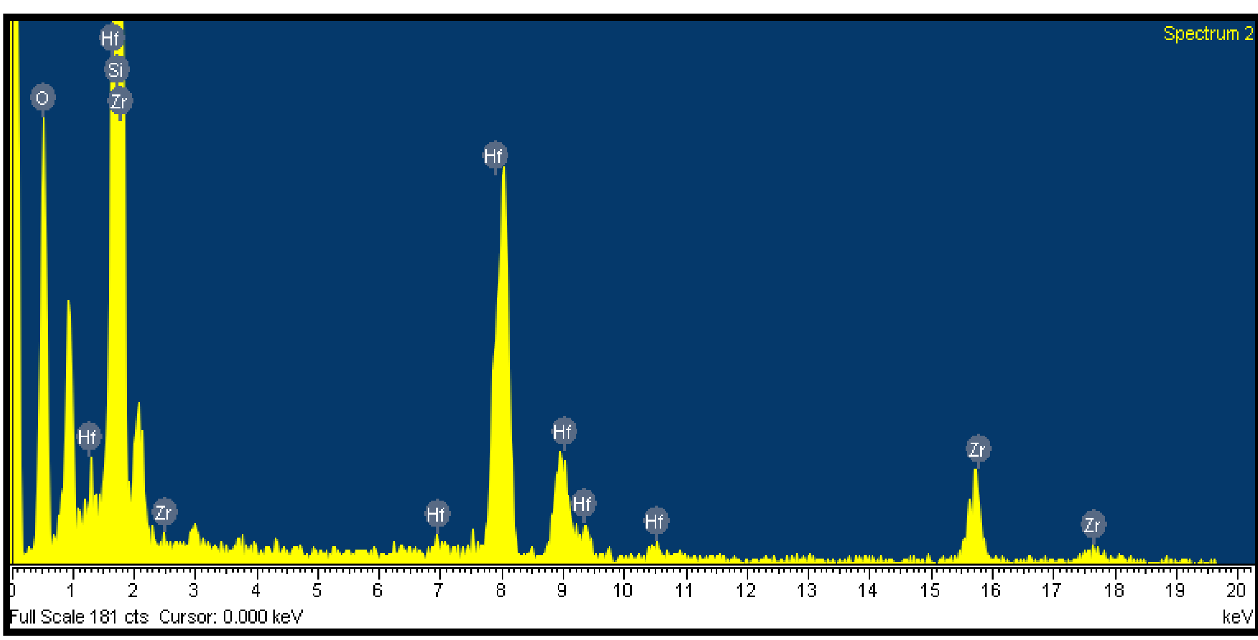


Figure 3.3 EDS spectrum of the sol-gel derived nanocrystal.

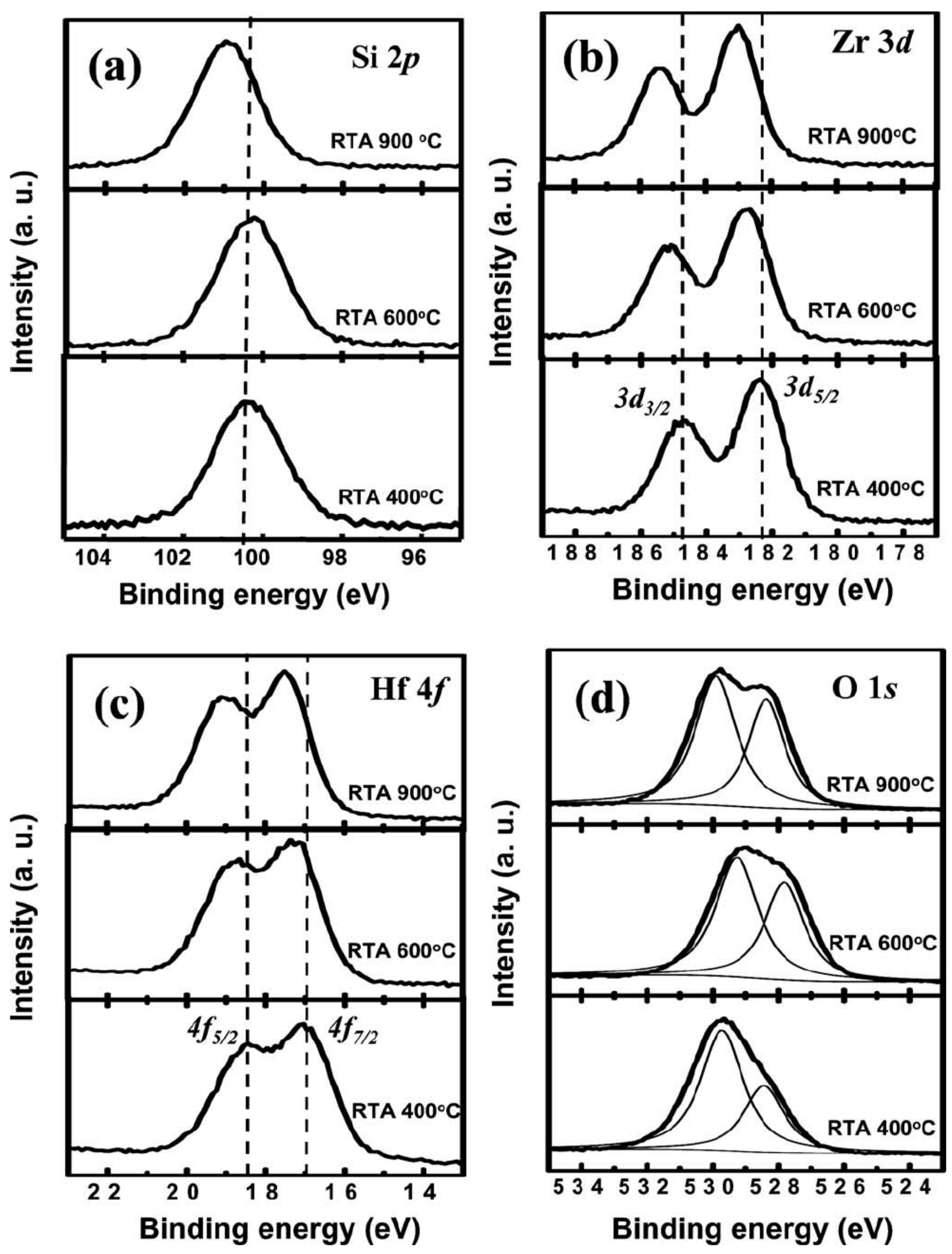


Figure 3.4 (a) Si 2p, (b) Zr 3d, (c) Hf 4f, and (d) O 1s XPS spectra of the sol-gel thin films after different annealing temperatures.

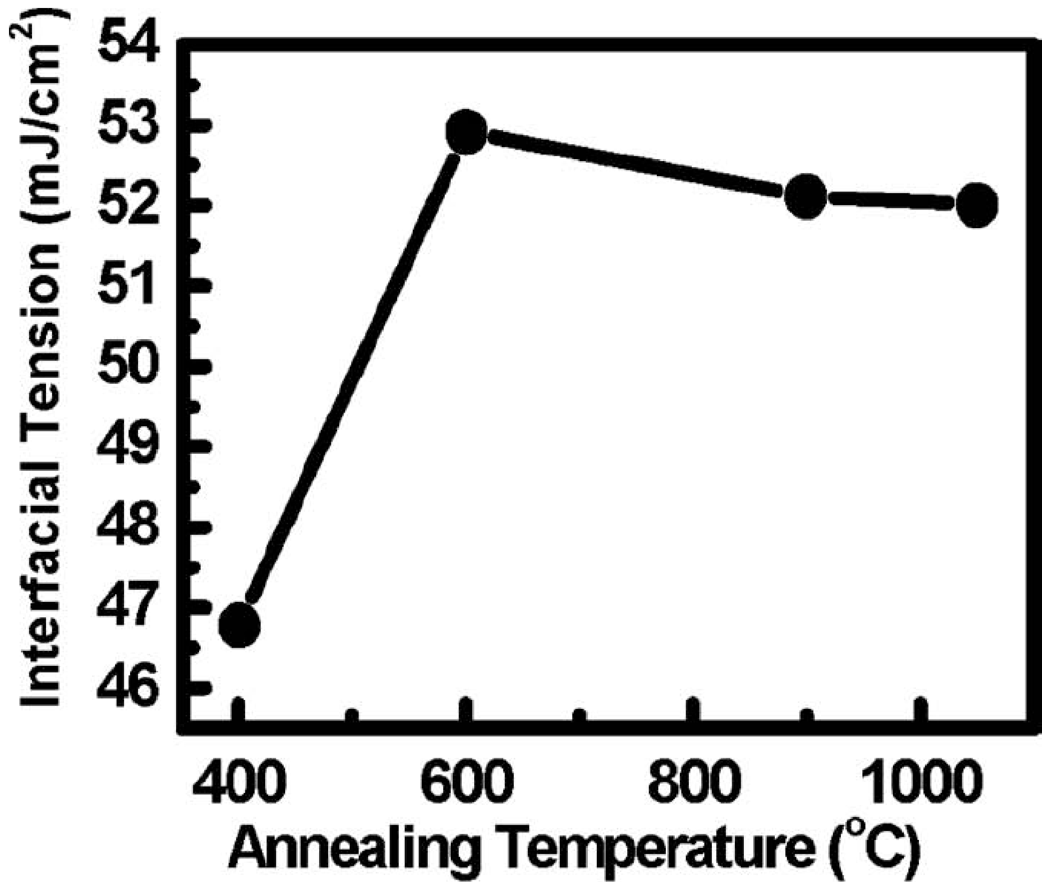


Figure 3.5 Interfacial tension of the sol-gel thin film as a function of annealing temperature.

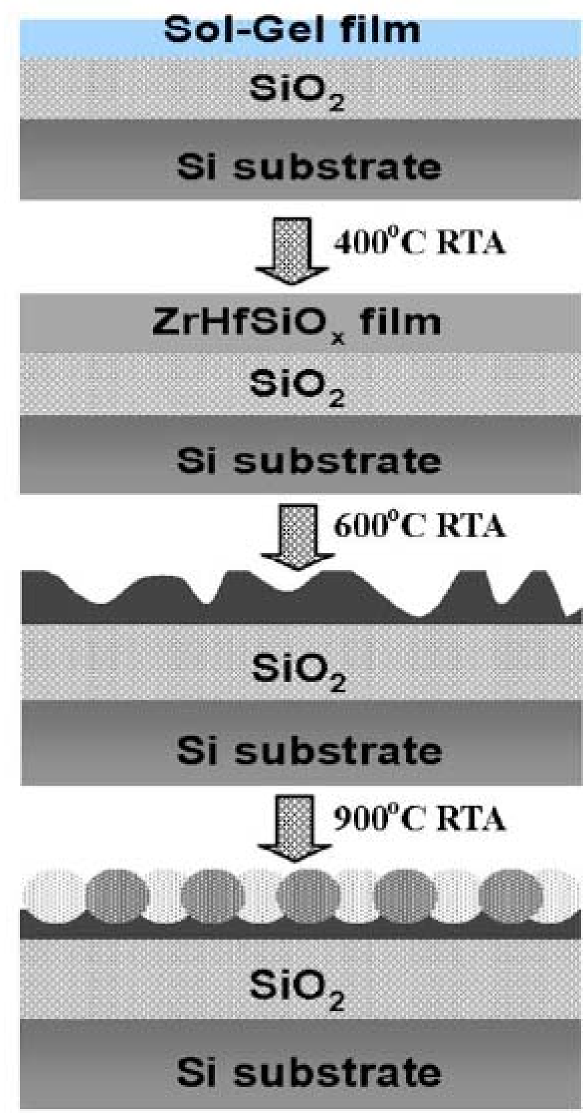


Figure 3.6 Transformation processes of the sol-gel thin film to NC.

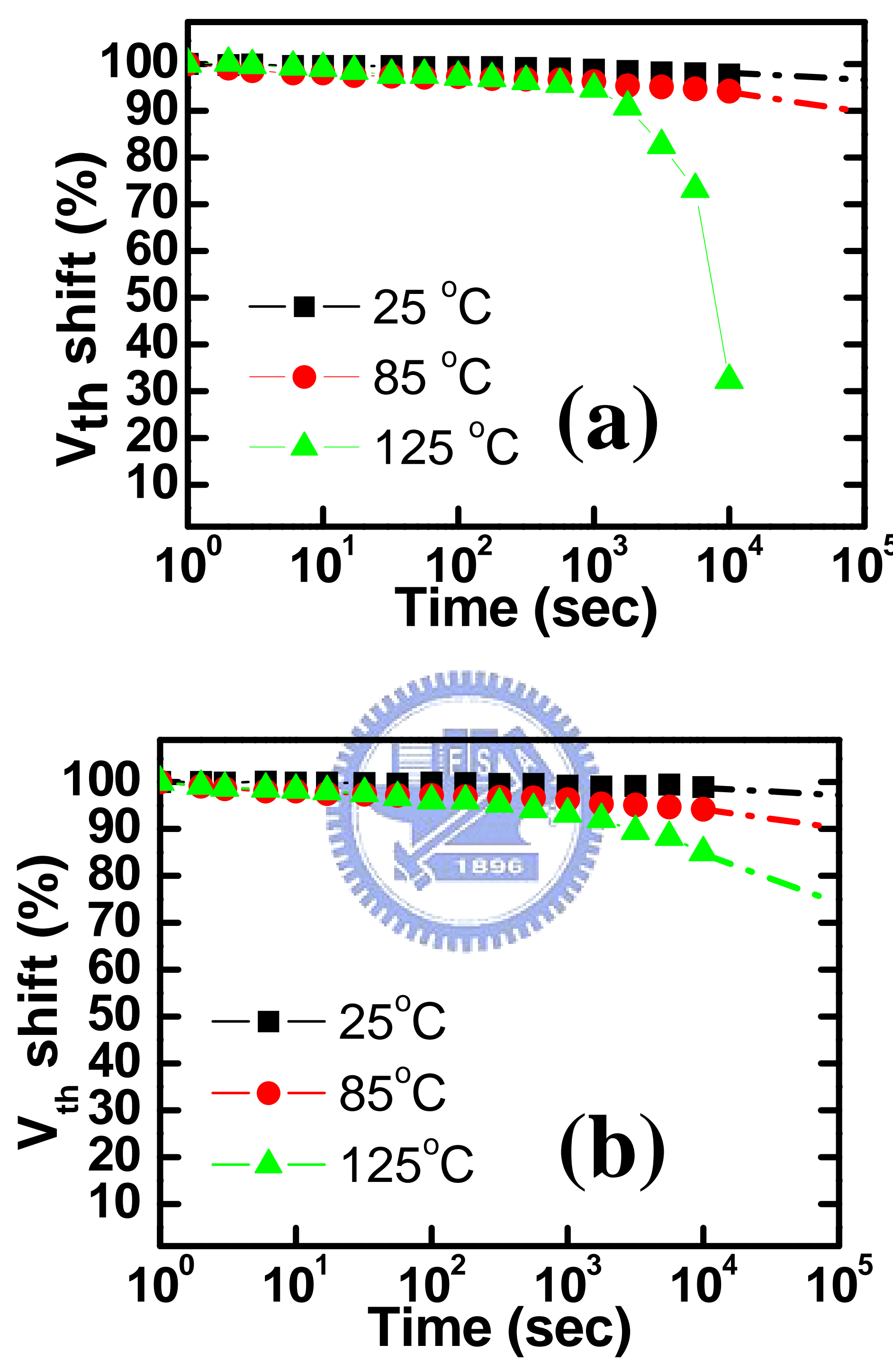


Figure 3.7 Retention characteristics of the NC memories annealed at (a) 600 °C, and (b) 900 °C under respective measurement temperatures of 25 °C, 85 °C, and 125 °C.

Chapter 4

Phase separation of charge trapping layers

4.1 Introduction

Spinodal decomposition takes place through spontaneous reaction of compositional fluctuations when a homogeneous phase becomes unstable under annealing.*[55]* The mechanism of spinodal decomposition induces the film transformation into interconnected or discrete morphology. The morphology of decomposed phases depends on the film thickness and the composition.*[1, 2]* The nanocrystal memory can keep the trapped charge tightly to avoid the charge loss problem in conventional thin film memory.*[56-58]* As to the sol-gel-derived nonvolatile memory devices using nanocrystals (NCs) as charge storage layers,*[38, 59]* the formation mechanism of growing nanocrystals is still unclear.

The spinodal decomposition occurred in the charge trapping thin film into the nanocrystal phase during thermal annealing is related to the sol-gel solution composition, annealing temperature and preparation solvent. The electric performance of coexisting hafnium silicate and zirconium silicate nanocrystal memory has published previously.*[37]* However, the effect of preparation solvent that affect the formation of nanocrystal, nanocrystal morphology, and charge retention in the sol-gel derived NC memory still indistinct. There is no a priori assumption for the effect preparation

solvent constraint on the nanocrystal evolution. We demonstrated the assumption of preparation solvent effect nanocrystal formation, isolation degree, and electric property in this thesis.

The sol-gel solution is prepared by well dispersion of precursors in the solvent. Prior to form the solid thin film, the sol-gel spin-coating film needs a suitable baking condition.*[60]* The solvent property plays an important role on deciding the sol-gel film thickness due to the dispersion condition and the viscosity. The different film thicknesses will vary the growing mechanism of phase separation of annealed nanocrystal due to spinodal decomposition. In this study, we control the prepared precursor concentration in order to investigate the solvent effect and film thickness with respect to crystal morphology, charge retention and memory window.

4.2 Experimental

The precursors utilized for the preparation of $ZrHfSi_xO_y$ sol-gel solution were zirconium tetrachloride ($ZrCl_4$, 99.5%, Aldrich), hafnium tetrachloride ($HfCl_4$, 99.5%, Aldrich), and silicon tetrachloride ($SiCl_4$, 99.5%, Aldrich), all of analytical reagent grade. Ethanol and isopropanol (IPA) were utilized as the solvents to dissolve the precursors to fabricate the starting sol-gel solution. Hydrochloric acid (HCl) was added to the solution as a catalyst because acid-catalyzed gels are therefore aggregates of very small ultimate particles. The molar ratio for $ZrCl_4$: $HfCl_4$:$SiCl_4$:solvent in the sol-gel solutions were 1:1:1:100, 1:1:1:500 and 1:1:1:1000. The solution after preparation was stirred for 0.5 hr for well mixing. We used Brookfield viscometer to measure the viscosity of different concentration sol-gel solutions at 20 °C.

After well mixed, spin coating the sol-gel solution (the concentration molar ratio of $ZrCl_4$: $HfCl_4$: $SiCl_4$: solvent = 1:1:1:1000) onto the p-type (100) silicon substrates. Using Tokyo Electron Limited (TEL) system (Clean Track model-MK8) apparatus

spin coated sol-gel film by rotation speed 3000 rpm for 60sec. After thin film deposition, these samples were subjected to rapid thermal annealing (RTA) at 900 ^oC for 60 sec in O_2 ambient to form NCs.

The fabrication of sol-gel spin-coating NC memory was fabricated on a p-type silicon (100) wafer. After a standard RCA process, 10-nm-thick tunnel oxide was thermally grown by a dry oxidation process in a furnace. Subsequently, the sol-gel film was deposited and through RTA process to solidify. To form NCs, the post deposition annealing treatment with temperatures of 900 °C in O_2 ambient was performed. The 20 nm blocking oxide was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD), followed by deposition of a 200-nm-thick poly-Si gate. After the PECVD TEOS deposition, the TEOS oxide was dentified in a N_2 ambient by annealing at 900 °C for 30 sec. Finally, gate patterning, source/drain implanting, and the remaining steps complete the gate stack formation of the NC memory devices.

4.3 Results and discussion

4.3.1 Film thickness effect of spinodal decomposition

Determination of viscosity was a well-defined and straightforward procedure using the Brookfield viscometer. The viscosity of various sol-gel solutions were listed in Table 4.1. The composition of $ZrCl_4$: $HfCl_4$: $SiCl_4$: IPA = 1:1:1:500 or 1:1:1:100 led to the precipitation effect, and the sol-gel film was not obtained. The solution became more viscous as if the amount of ethanol solvent decreased. The sol-gel solution prepared in ethanol solvent exhibited a lower viscosity of 1.15cP. In contrast, the sol-gel solution prepared in IPA solvent exhibited a larger viscosity of 2.45cP. Principles of physical chemistry dictated that in dilute solutions, where solute interaction was negligible, the greater the solvency of a solvent, and lower the solution viscosity. This observation suggested the critical issue of intrinsic solvent

property and dispersing precursor concentration on depositing the sol-gel thin film. In general, a low viscosity fluid generated a thinner film through spin-coating process.*[61]*

High resolution structural characterization of the NCs was carried out by the high-resolution transmission electron microscopy (HRTEM, JEOL2100F) operated at 300 kV. The respective TEM images of the charge trapping layer fabricated from ethanol and IPA solvents was demonstrated in Figure 4.1. The sample in Figure 4.1(a) utilized ethanol as solvent to synthesis sol-gel solution then spin-coating and annealing at 900 ^{o}C in O_2 atmosphere to form NCs. In this condition, phase separation accompanied with the crystallization of the sol-gel film. We observed the film completely transferred into isolated NCs after 900 ^{o}C annealing. The sample in Figure 4.1(b) from IPA solvent behaved quit difference with Figure 4.1(a). The sample in Figure 4.1(b) changed preparation solvent into IPA to synthesis sol-gel solution and through the same deposition and annealing process to form NCs. The morphology obtained from IPA solvent was like the interconnected NCs. What is the growing mechanism of discrete or interconnected NCs for only varying the sol-gel solvent? The mechanism responsible for the formation of discrete or interconnected NCs was dependent on the spinodal decomposition of annealed sol-gel thin film. Seol et al.*[1, 2]* utilized computer simulation to deduce the spinodal decomposition process. They suggested the morphology of decomposed phases on initially homogeneous thin film strongly depends on the film thickness and the composition.*[1]* In our experiment, the composition of precursor was fixed, and only the variable of film thickness is approached. The elemental composition of the binary metal oxides NCs were estimated by energy dispersive X-ray spectroscopy (EDS), showed in Fig 4.2, demonstrated the elemental compositions in NCs combined hafnium, zirconium, silicon and oxygen.

4.3.2 Phase separation mechanism of sol-gel thin film

The mechanism responsible for the formation of NCs was well known to be the transformation of crystalline silicate into spinodal decomposition through high temperature RTA treatment.*[62]* Stemmer and coworkers*[31]* proposed the metastable phase diagram for the zirconium silicate and hafnium silicate. They concluded the film approached the driving force for a thermodynamically metastable state of the spinodal decomposition under annealing temperature at 900 °C, showed in Figure 4.3. Therefore, we depicted a pathway in Figure 4.4 for explaining the thickness phenomenon of spinodal decomposition on sol-gel thin film. As to the thinner film, a series of phase separation steps depicted in Figure 4.4(a). The first step showed initial stage of sol-gel deposited film before annealing. The second step illustrated the film was continuous and smooth, and retained the similar morphology under low temperature annealing (400 °C). Upon 600 °C annealing in step 3, the film started to perturb, and became not only discontinuous but uneven. Finally, at 900 °C annealing, the film approached the driving force for a metastable state of the spinodal decomposition region in the phase diagram.*[31]* The phase transformed by spinodal decomposition induced the completely isolated NCs. Figure 4.4(b) illustrated different preparation solvent of IPA derived phase separation mechanism. On the contrary, the morphology in the thicker film became more three-dimensional and interconnected at 900 °C annealing. We presumed that the solvent property played an important role on deciding the sol-gel film thickness due to the dispersion condition and the viscosity. The spin coating film thickness effected the film transformation into interconnected or discrete NCs.

4.3.3 Comparison of interconnect and discrete NC memory retention

Figure 4.5 showed the charge retention characteristics of the sol-gel derived

memory devices. The electrical characteristics of the samples were performed by HP4156 to observe I-V characteristics. The normalized V_{th} shift in percentage was defined as the ratio of V_{th} shift at the time of interest and at the beginning (t=1 sec). For ethanol system sample at 25 °C measurement, the retention times showed in Figure 4.5(a) was extrapolated up to 10^6 sec with less than 5% charge loss. At 85 °C measurement, the retention times to 10^6 sec demonstrated less than 10% charge loss. Compare to the IPA system sample at 85 °C measurement, a significant amount of 15% charge loss at 10^6 sec was observed. This result indicated the extent of nanocrystal isolation in the charge trapping layer was beneficial for data retention. Therefore, the trapped electrons by isolated NCs were not easily to loss. Additionally, in Figure 4.6, ethanol system performed a relatively large memory window of about 10 V, larger than IPA system sample (~ 3V). We suggested the ethanol system with initially thinner film was beneficial for the better charge trapping performance on tunneling electrons due to isolated NCs formation of spinodal decomposition.

4.4 Summary

In conclusion, we compared the sol-gel film thickness factor that affected the morphology of NCs after annealing. The solvent for dissolving precursors played an important role on controlling viscosity of the sol-gel solution and thickness of the sol-gel spin coated film. The IPA system was more viscous than ethanol system for sol-gel solution under the same concentration preparation. The thinner film formed by ethanol system led to the isolated NCs, while the interconnected NCs morphology was observed of IPA system. The sol-gel derived isolated NCs of ethanol system exhibited better charge trapping performance and memory window.

Table 4.1 Dependence of viscosity and film thickness as a function of compositional molar ratio of sol-gel solutions.

Composition of precursor	Concentration (in molar ratio)	Viscosity (cP)
$ZrCl_4$+$HfCl_4$+$SiCl_4$+Ethanol	1:1:1:1000	1.15
$ZrCl_4$+$HfCl_4$+$SiCl_4$+Ethanol	1:1:1:500	1.19
$ZrCl_4$+$HfCl_4$+$SiCl_4$+Ethanol	1:1:1:100	1.47
$ZrCl_4$+$HfCl_4$+$SiCl_4$+IPA	1:1:1:1000	2.45
$ZrCl_4$+$HfCl_4$+$SiCl_4$+IPA	1:1:1:500	precipitate
$ZrCl_4$+$HfCl_4$+$SiCl_4$+IPA	1:1:1:100	precipitate

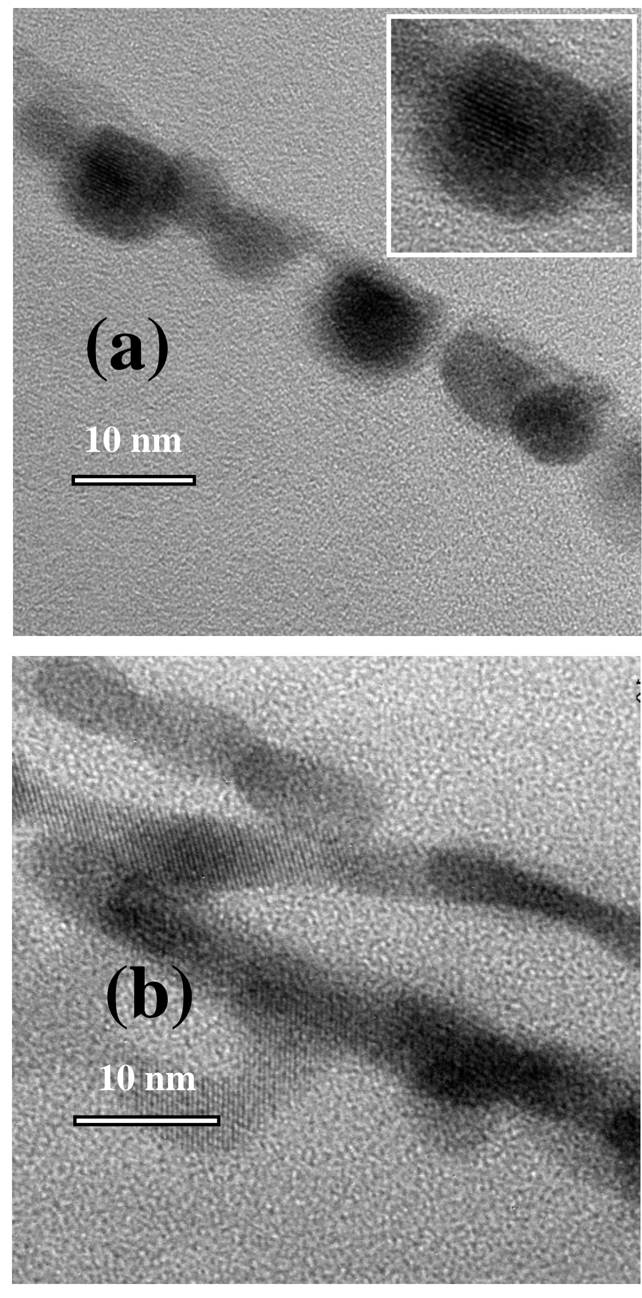
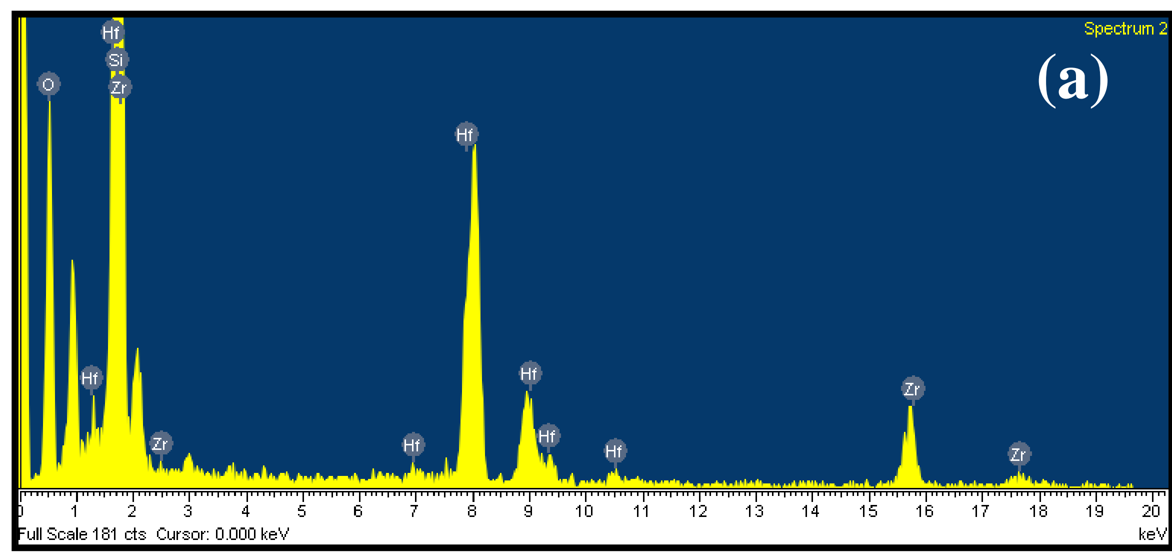


Figure 4.1 The cross-sectional TEM images of the NCs transformation by (a) Ethanol system and (b) IPA system.



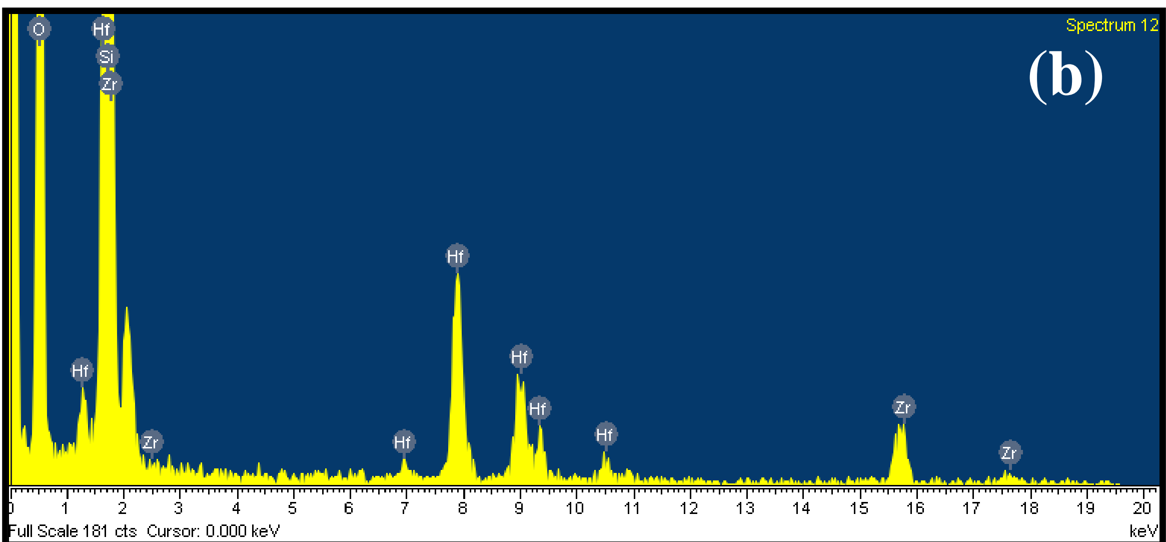


Figure 4.2 (a) Ethanol system (b) IPA system sample elemental composition of the binary metal oxides NCs were estimated by energy dispersive X-ray spectroscopy (EDS).

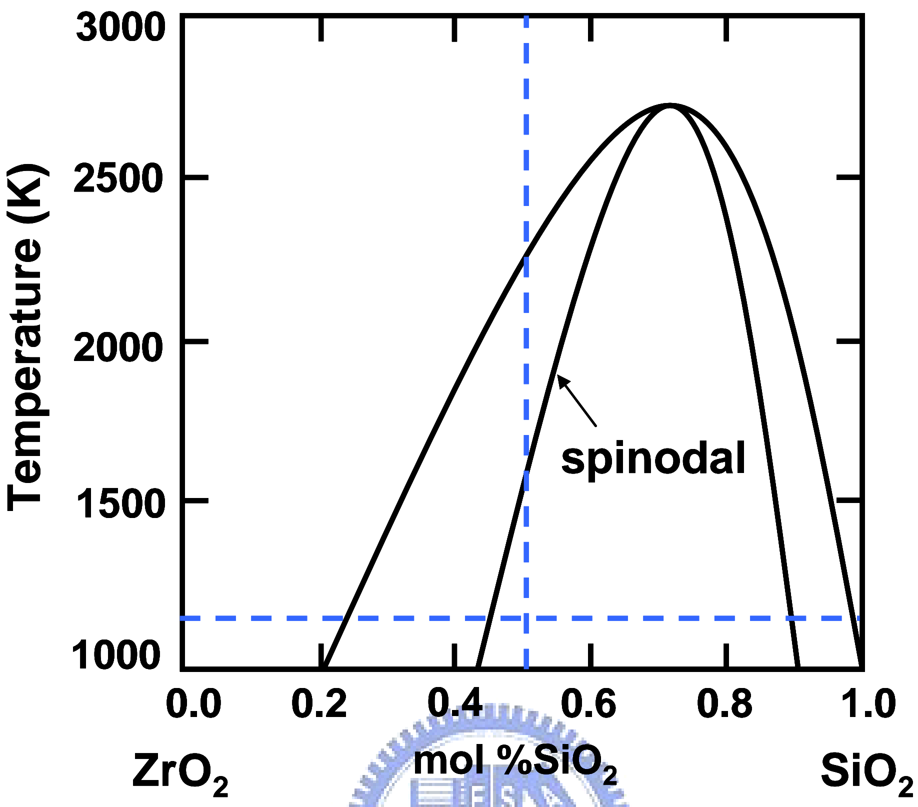


Figure 4.3 The metastable extensions of spinodal region in ZrO_2–SiO_2 phase diagram.

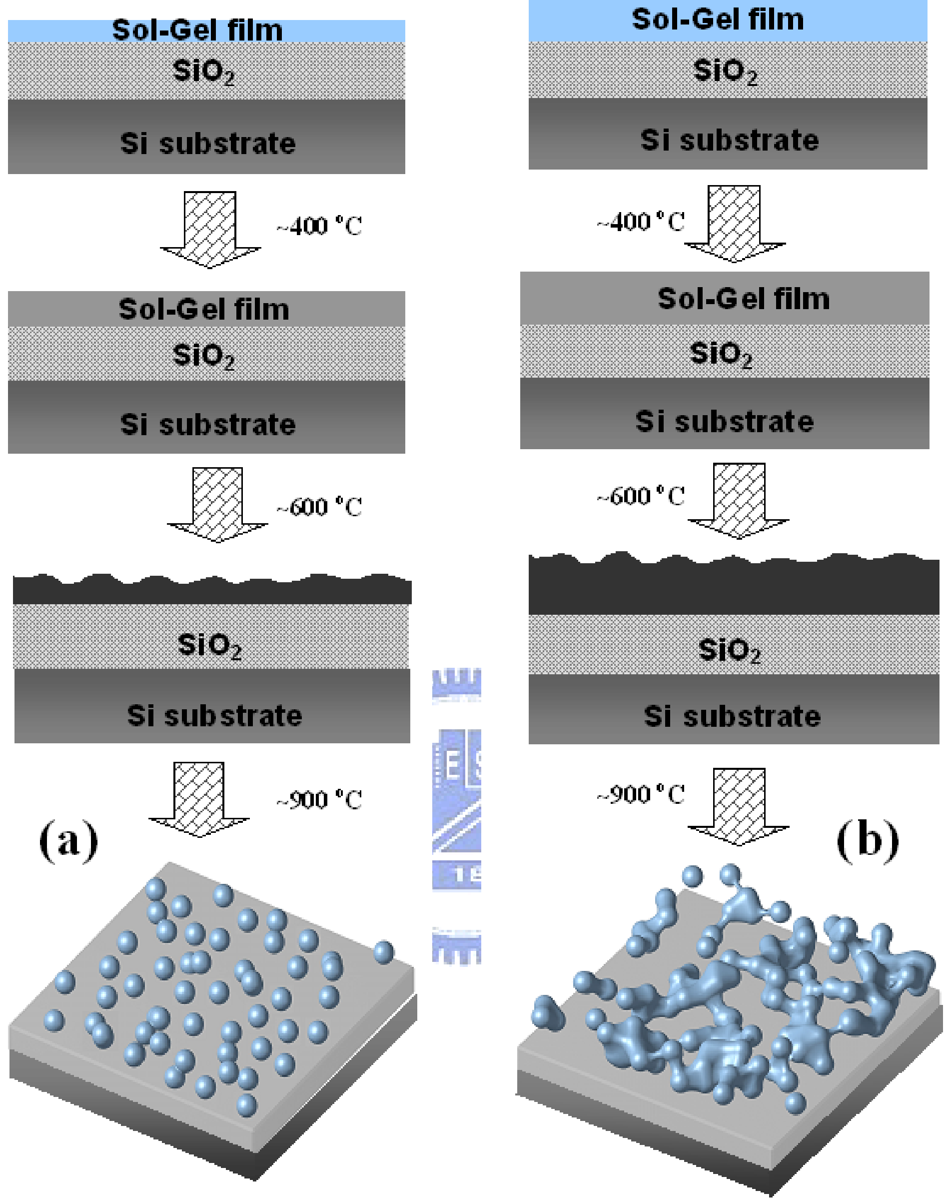


Figure 4.4 Phase separation mechanism of sol-gel derived nanocrystal on (a) ethanol system and (b) IPA system.

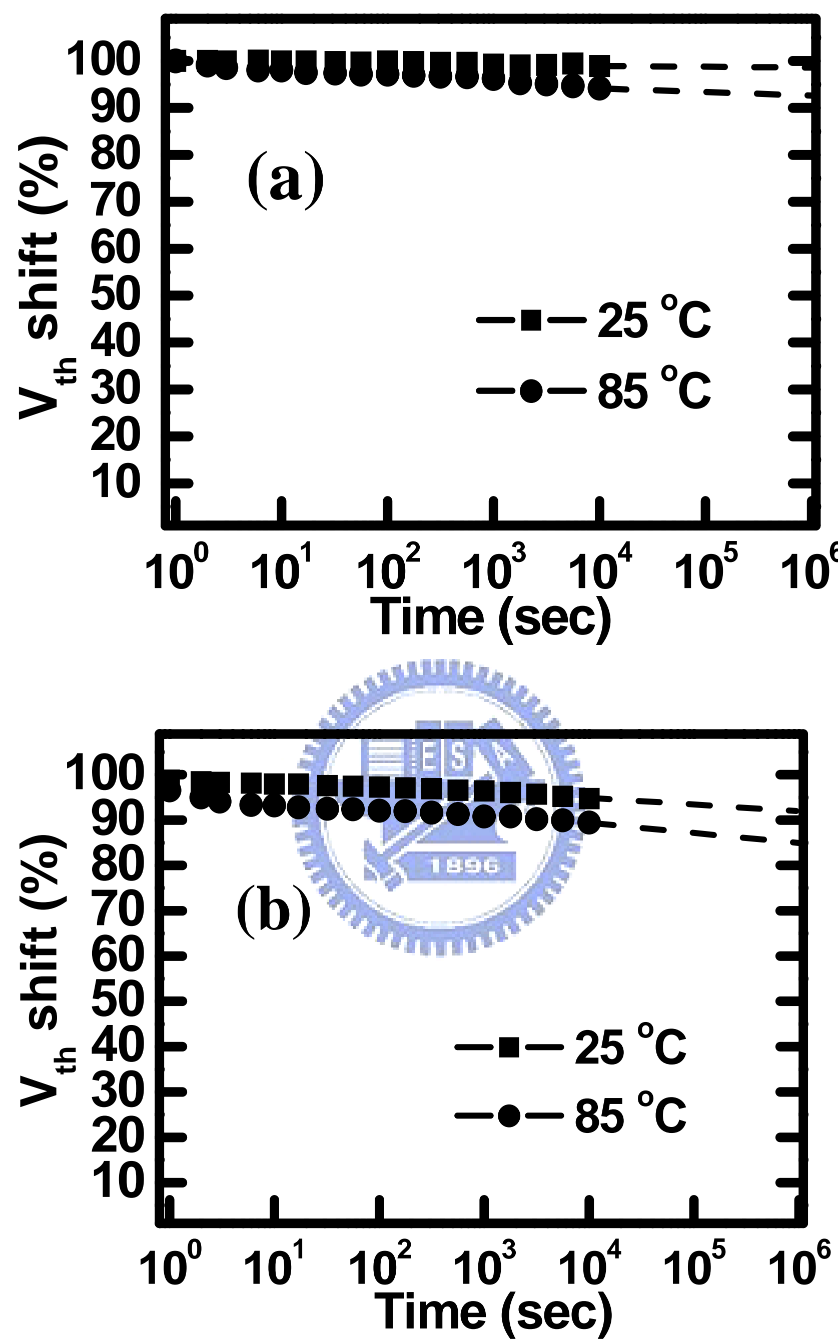


Figure 4.5 Retention characteristics of (a) ethanol system (b) IPA system derived NC memories at measurement temperatures of 25 and 85 °C.

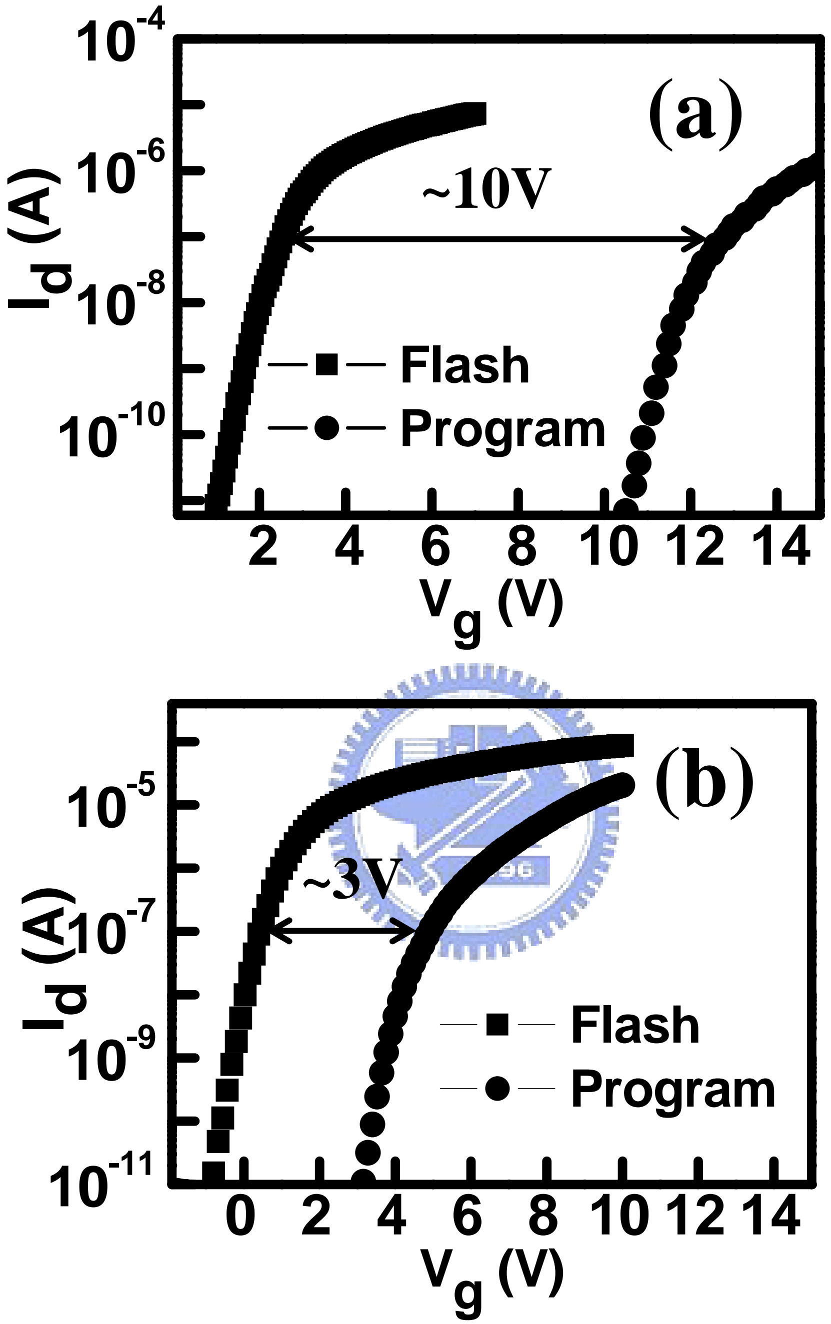


Figure 4.6 Id-Vg curves of (a) ethanol system (b) IPA system derived NC memories in the programmed state of Vd=10V, Vg=15V, pulse time 10ms.

Chapter 5

Application of novel sol–gel spin coating method in SONOS-type flash memory

5.1 Introduction

Memory storage is an important technology that enables the growth in the information world. With the rapid growth of the internet, wireless communication products, personal digital assistants (PDAs), digital cameras, digital camcorders, digital music players, and computers, there is continually a demand for superior information storage technology. The development of portable consumer electronics has spurred the need for high-density nonvolatile memory with low power consumption for system on-chip applications. Considering the flexibility-cost plane, it turns out that the flash memory offers the best compromise between these two parameters, since they have smaller cell size and excellent flexibility (they can be electrically written on field more than 100,000 times, with byte programming and sectors erasing).*[3]* In recent years, flash memories based on charge storage in nitride traps, such as poly-silicon/SiO_2/Si_3N_4/SiO_2/semiconductor (SONOS) structures have been investigated intensively. However, the conventional SONOS memory still suffers from erase saturation and insufficient charge-trapping efficiency, which markedly degrade its performance.*[63, 64]*

Nanocrystal nonvolatile memory (NC-NVM) has predominant advantages when it

was proposed in the early 1990s by Tiwari *et al.[7]*. The only stored charges at the nanocrystals adjacent to the defect leak through the tunneling dielectric, compared to huge charge loss of conventional flash memory due to the lateral charge transport.*[65]* The possibility of exceeding the performance limits of the conventional floating-gate device spurred many subsequent investigations on this approach. Only the electrons stored on the nanocrystal directly above the defect chain will be affected since the nanocrystals are separated from each other. The tunnel oxide thickness of the nanocrystal memory device can be reduced to allow faster programming and lower voltage operation.*[8]*

Various techniques have been developed to form the nanocrystals in the gate oxide. For example, Gerardi *et al.[66]* employed the low pressure chemical vapor deposition (LPCVD) to fabricate Si nanocrystals for density up to 2×10^{12} cm^{-2} ,and then, utilized Si nanocrystals as the memory cell. King *et al.[67]* fabricated Ge nanocystals by oxidation of a $Si_{1-x}Ge_x$ layer formed by ion implantation, and demonstrated quasi-nonvolatile memory operation with a 0.4 V threshold-voltage shift. Lin *et al.[46]* reported co-sputter technique to fabricate high density HfO_2 nanocrystals and utilized to nanocrystal memories with about 4V threshold-voltage shift performance. In this thesis, we proposed a sol-gel spin-coating method to fabricate the charge trapping film or NC for the memory. This approach is relatively cheap, simple, and can be fabricated in a normal atmospheric pressure instead of high-vacuum system. We have successfully achieved the nanocrystal memories with superior characteristics in terms of considerably large memory window, high speed P/E, long retention time, and excellent endurance.

5.2 Experimental

The fabrication of a sol–gel spin-coating derived SONOS-like NC memory was started with a local-oxidation of silicon (LOCOS) isolation process on p-type (100) silicon substrate. At the beginning, a 10-nm tunneling oxide was thermally grown at 925 ^{o}C by furnace oxidation. The charge trapping layer was prepared by a sol-gel spin coating method and annealed at high temperature. The precursors utilized for the preparation of the sol-gel solution were zirconium tetrachloride ($ZrCl_4$, 99.5%, Aldrich), hafnium tetrachloride ($HfCl_4$, 99.5%, Aldrich), and silicon tetrachloride ($SiCl_4$, 99.5%, Aldrich), all of analytical reagent grade. Ethanol (EtOH) was used as the solvent to dissolve the precursors to fabricate the starting sol-gel solution. Hydrochloric acid was added to the solution as a catalyst because acid-catalyzed gels are therefore aggregates of very small ultimate particles. The solution after preparation was stirred for 0.5 hr for well mixing. Initially, we prepared a solution for which the molar ratio of $HfCl_4$:$ZrCl_4$:$SiCl_4$:EtOH equal to 1:1:1:1000. The sol-gel thin film was deposited by spin coating at 3000 rpm for 60 sec at 25 ^{o}C. After spin coating, the wafer was under rapid thermal annealing (RTA) at 900 ^{o}C temperatures for 60 sec in O_2 ambient to form sol-gel derived nanocrystal. Then, the 20-nm-thick blocking oxide was deposited by plasma enhanced chemical vapor deposition (PECVD) tetraethoxysilane (TEOS) oxide. Prior to deposit 200-nm a-Si gate, the TEOS oxide was densified in N_2 ambient at 900 ◦C for 30 s anneal to repair the defects and decrease the number of traps. Finally, gate pattering, source/drain (S/D) implanting, and the rest of the subsequent metal-oxide-semiconductor processes were used to fabricate the NC-NVM devices. Figure 5.1 showed the structure of the fabricated device. The memory characteristics reported in this thesis with device W/L=10μm /0.35μm.

5.3 Results and discussion

Figure 5.2 showed the cross-sectional HRTEM image of sol-gel derived nanocrystals with the sol-gel solution of $ZrCl_4$:$HfCl_4$:$SiCl_4$:EtOH=1:1:1:1000 spin coating at rotation speed of 3000rpm for 60 sec. The insert image showed the lattice fringe image of NC to confirm the crystalline result. We utilized the sol-gel derived NC as charge tapping layer in NC memory devices. The crystal size was estimated to be 6–10 nm in diameter. We inferred that the darker NCs in Figure 5.2 are formed from the high-molecular-weight hafnium silicate, and the bright NCs are from the low-molecular-weight zirconium silicate.

5.3.1 Program/Erase characteristics

In this thesis, the programming scheme was executed by using channel hot electron injection (CHEI) to inject charge into the trapping layer. Figure 5.3 showed the Id-Vg curve of NC memory under the programming state of Vg=10V, Vd=15V, 10ms pulse time and the V_{th} shift after programming can be up to 10 V. Figure 5.4 shows programming speed of the sol-gel derived NC flash memory. The program conditions were (i) Vg= 5V, Vd= 5V; (ii) Vg= 7V, Vd= 7V; (iii) Vg= 9V, Vd= 9V, respectively. The V_{th} shift increased as increasing the applied gate voltage because of more "hot" electrons generated and tunneled gate oxide to reach the trapping layer. The hot electrons were trapped by charge trapping layer and caused V_{th} shift. Relatively high speed (10μs) programming performance can be achieved with a memory window of about 2.2 V. Figure 5.5 displayed the erase characteristics as a function of various operation voltages. We used band-to-band hot hole (BTBHH) to erase, and the erase conditions were (i) Vg= -9V, Vd= 9V; (ii) Vg= -7V, Vd= 9V; (iii) Vg= -5V, Vd= 7V, respectively. Excellent erase speed of around 1ms can be obtained.

More important, there was only a very small amount of overerase observed.

5.3.2 Reliability characteristics

Retention characteristic

The charge retention characteristic of the sol-gel derived NC memory device demonstrated in Figure 5.6. The normalized V_{th} shift was defined as the ratio of V_{th} shift at the time of interest and at the beginning. Using the V_{th} shift as an indicator, the charge loss for the nanocrystal memory was exhibited. At 25 °C measurement, the retention times was extrapolated up to 10^6 sec for only ~5% charge loss, while less then 10% charge loss at 85 °C measurement. The 900 °C annealed sample retained its good retention characteristics for less than 25% charge loss at higher temperature measurement of 125 ^{o}C. This result explained the importance of NC formation for the sol-gel derived memory device. The NC discretely dispersed in the charge trapping layer, which alleviated the charge loss problem when defects existed in the tunneling oxide. The trapped electrons in the sol-gel-derived nanocrystal devices were not easily to escape, and the exhibited charge loss percentage was quite low in our device.

Endurence characteristic

The endurance characteristics after 10^4 P/E cycle was shown in Figure 5.7. The programming and erasing conditions are Vg=Vd=10V for 10ms and Vg=-6V, Vd=10V for 1s, respectively. Despite the occurrence of significant memory window narrowing, a memory window of about 6V was sustained even after 10^4 P/E cycles. The origin of the narrowing over cycling, mainly coming from the increase of V_{th} in erased state, might be due to two factors: The first is the mismatch between the localized spatial distributions for injected electrons and holes by using channel hot-electron programming and band-to-band hot hole erasing. The uncompensated

electrons will then cause the V_{th} to increase gradually over P/E cycling. The other is the stress-induced electron traps generated in the tunnel oxide during cycling. The result illustrated our device has excellent endurance performance.

Disturbance characteristic

Figure 5.8 showed the gate disturb characteristics. We measured the gate disturb on erase state devices and applied Vg=9V or 10V with Vd=Vs=Vb=0V to the device. After 10^4 sec at 25 °C, small extent of less than 0.3V gate disturbs were found. Figure 5.9 illustrated the read disturb characteristics at 25 ^{o}C measurement. We measured the read disturb on erase state devices and operated at Vg=4V, Vd=2V with Vs=Vb=0V, the memory cell almost without any disturb. While at Vg=4V, Vd=4V operate, small read disturb of less than 0.5V were found after 10^4 sec measurement. Finally, we displayed the drain disturb on programmed state and applied Vd=5V or 10V with Vg=Vs=Vb=0V to the device, showed in Figure 5.10. The drain disturb of V_{th} shift after 10^4 sec operation was less than 0.3V at Vd=5V measurement, and less than 0.5V at Vd=10V measurement.

5.4 Summary

In this thesis, we utilized sol-gel spin coating method to fabricate the charge trapping layer of memory device. After high temperature annealing at 900 ^{o}C, the sol-gel thin film transferred into isolation nanocrystals. The size of the sol-gel derived nanocrystal was estimated to be about 6-10 nm. We verified the device performance such as the program/erase speed, charge retention, endurance and disturbs. The quality of the nanocrystals formed by the sol-gel spin coating method and RTA treatment exhibited excellent properties in terms of large memory window, long

retention time, excellent disturbs, and good endurance. Compare to other memory devices that ever reported on national journal paper, our device has excellent performance of memory window, data retention, and high write/erase speed.

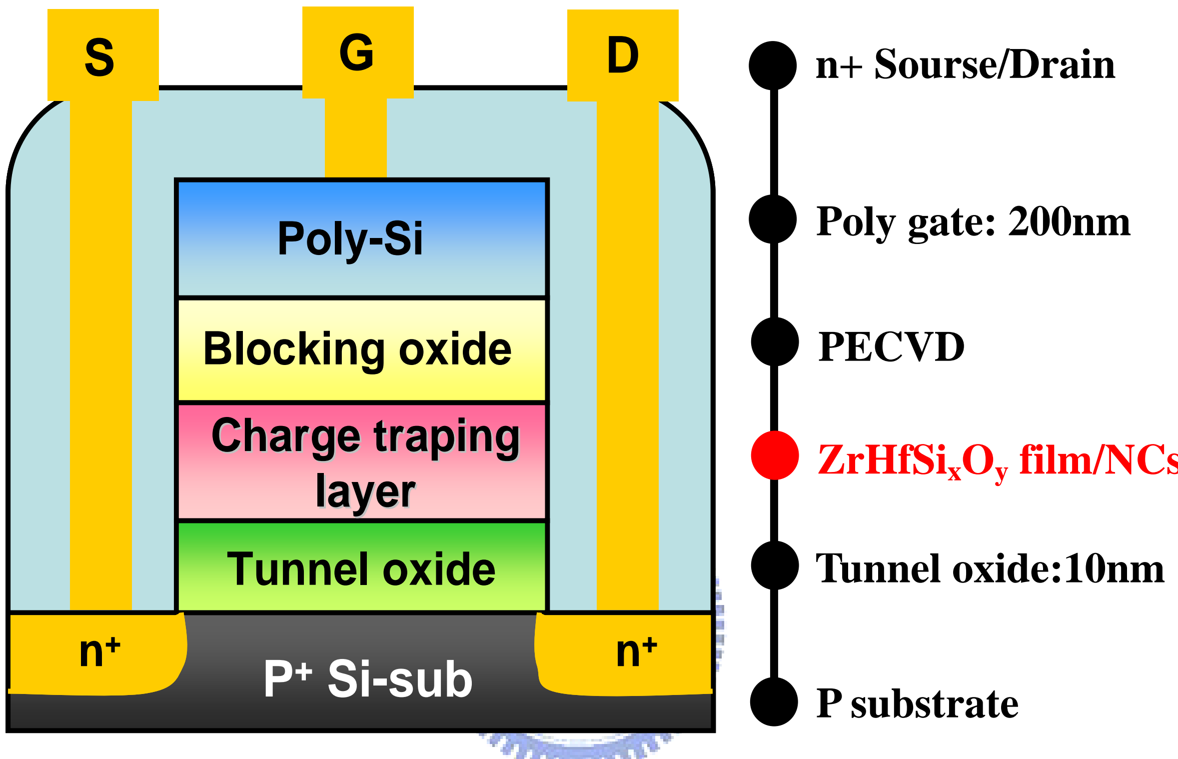


Figure 5.1 Schematic diagram of the device structure for the spin coating charge trapping film/nanocrystal memories.

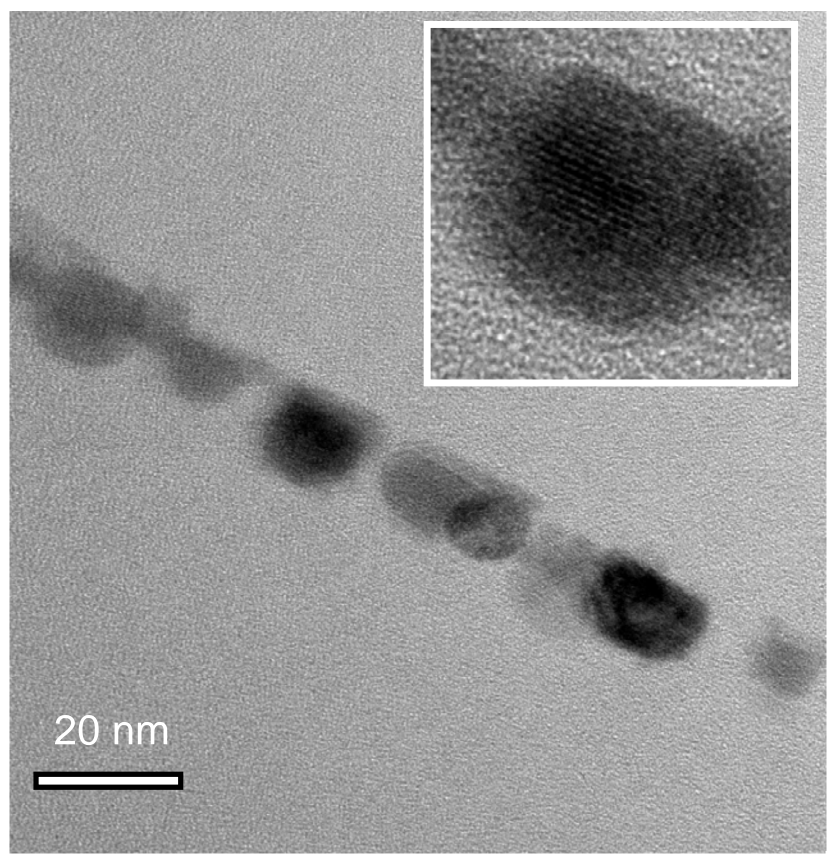


Figure 5.2 Cross-sectional TEM view of sol-gel derived nanocrystals. (Insert: lattice fringe of nanocrystal)

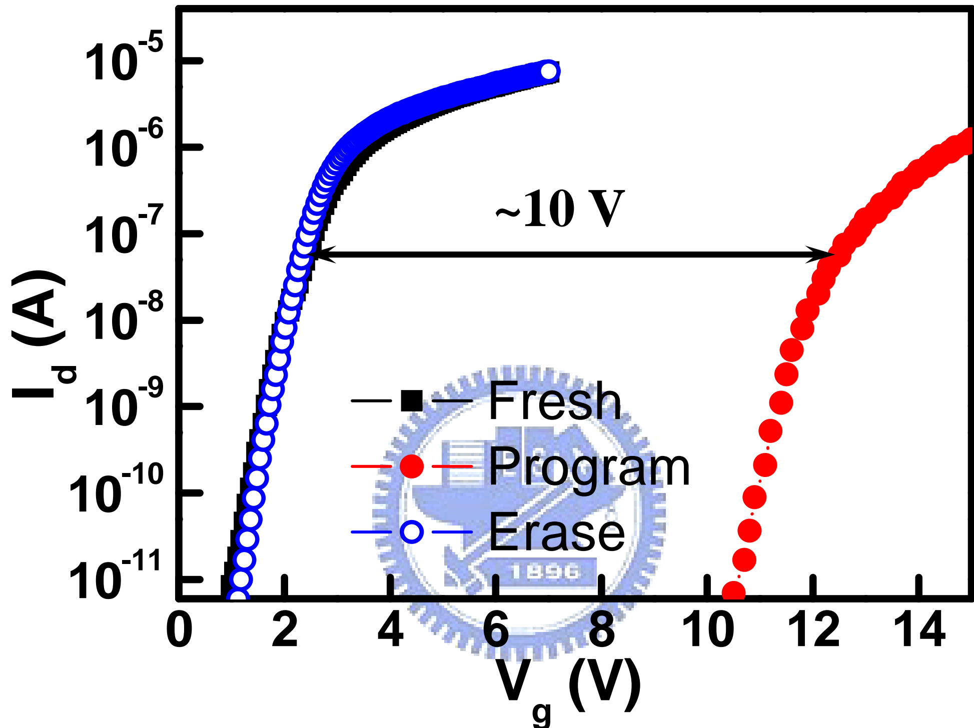


Figure 5.3 Id-Vg curves of sol-gel derived NC memory in the programmed state (Vd=10V, Vg=15V, 10ms).

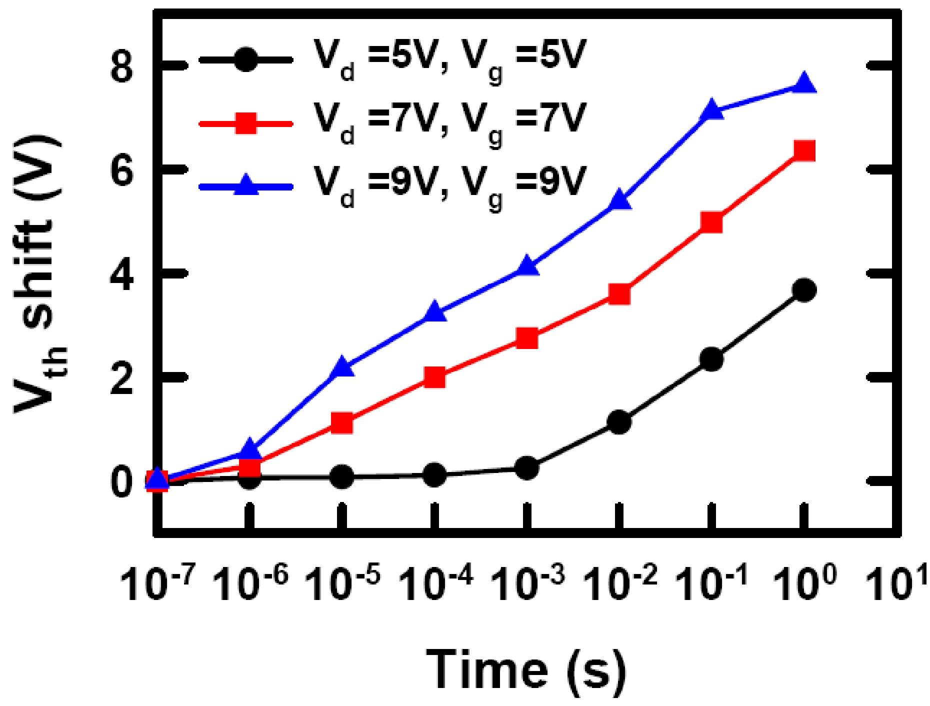


Figure 5.4 Program speed of sol-gel derived NC memory device.

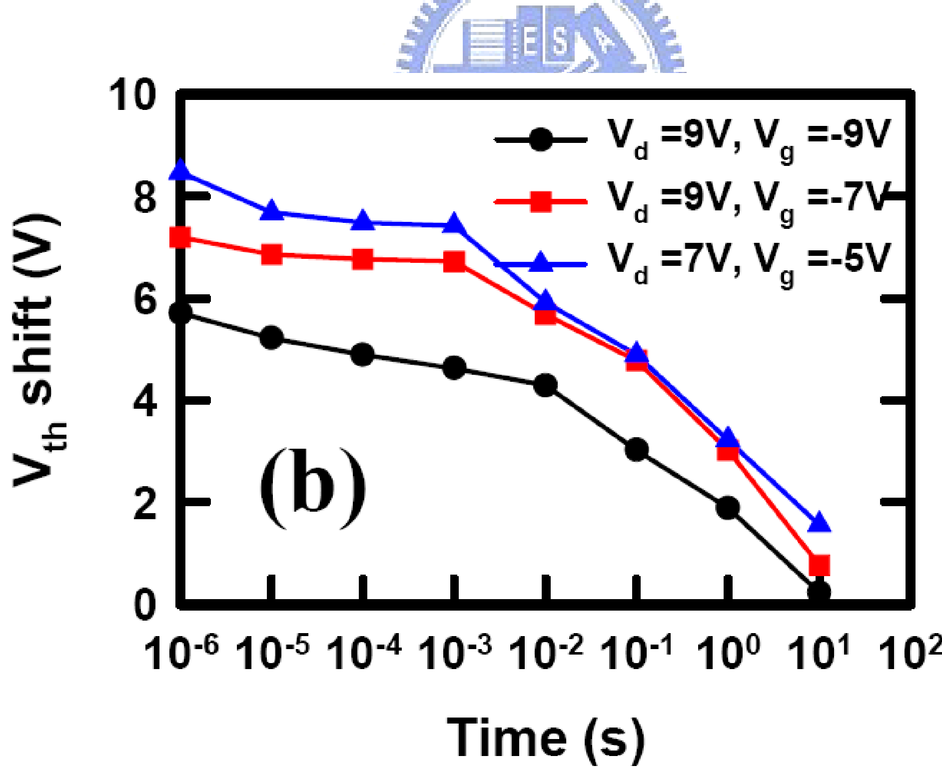


Figure 5.5 Erase speed of sol-gel derived NC memory device.

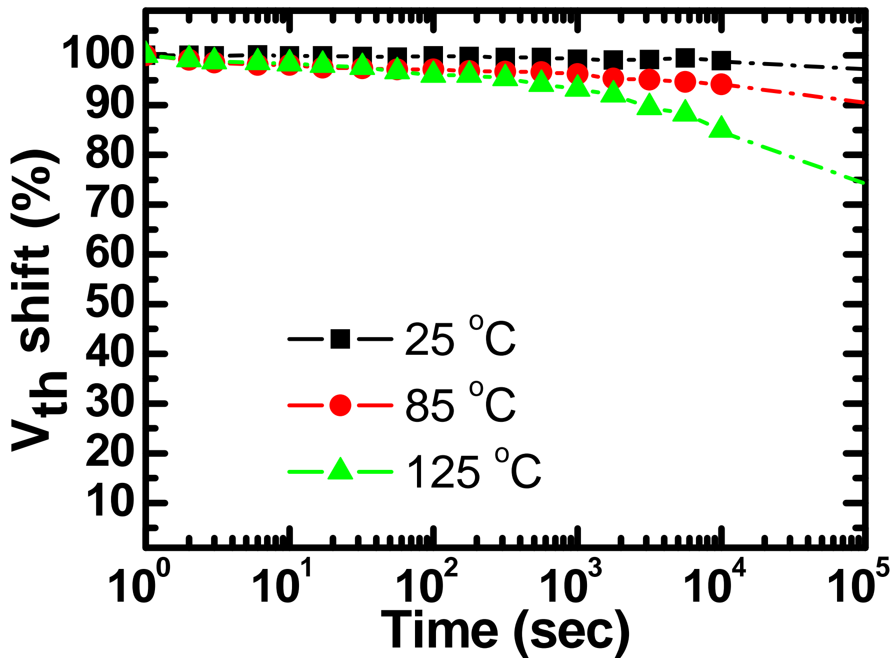


Figure 5.6 Retention characteristics of the NC memory at 25 °C, 85 °C and 125 °C measurement.

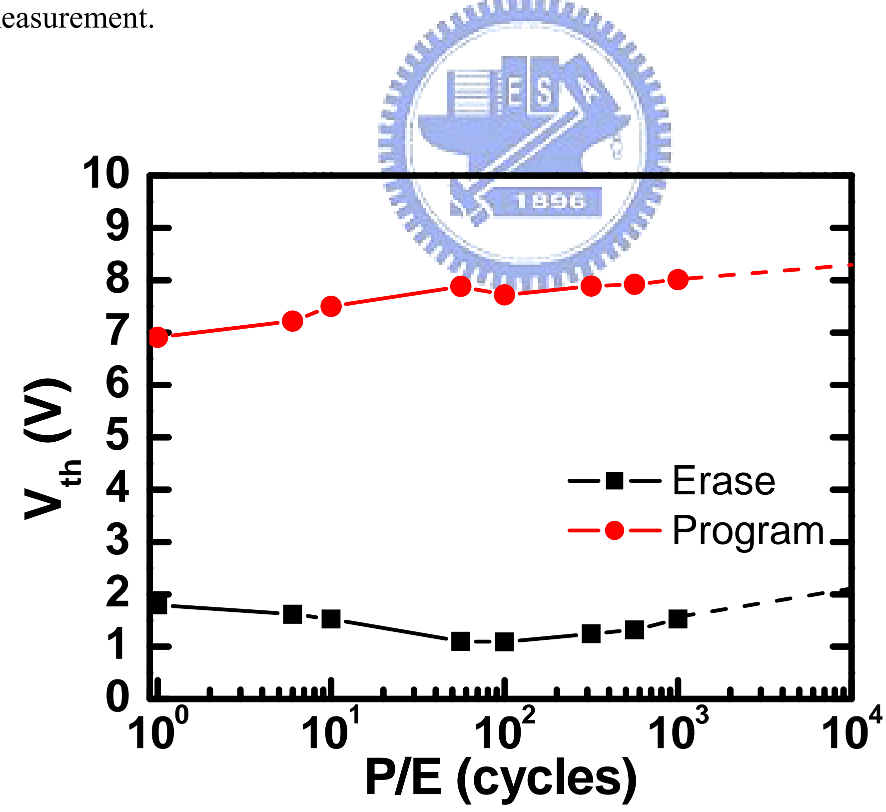


Figure 5.7 Endurance of sol-gel derived memory device. The memory window is about 6V after 10^4 P/E cycles. (Program state: Vd=10V, Vg=10V, t=10ms; erase state: Vd=10V, Vg=-6V, t=1s)

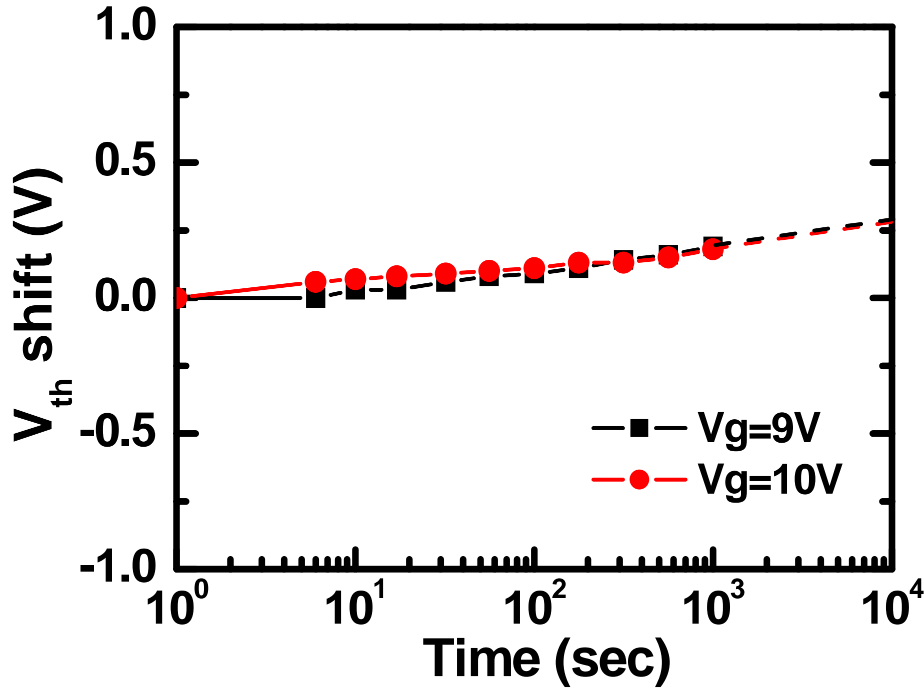


Figure 5.8 Gate disturb characteristics of sol-gel derived memory.

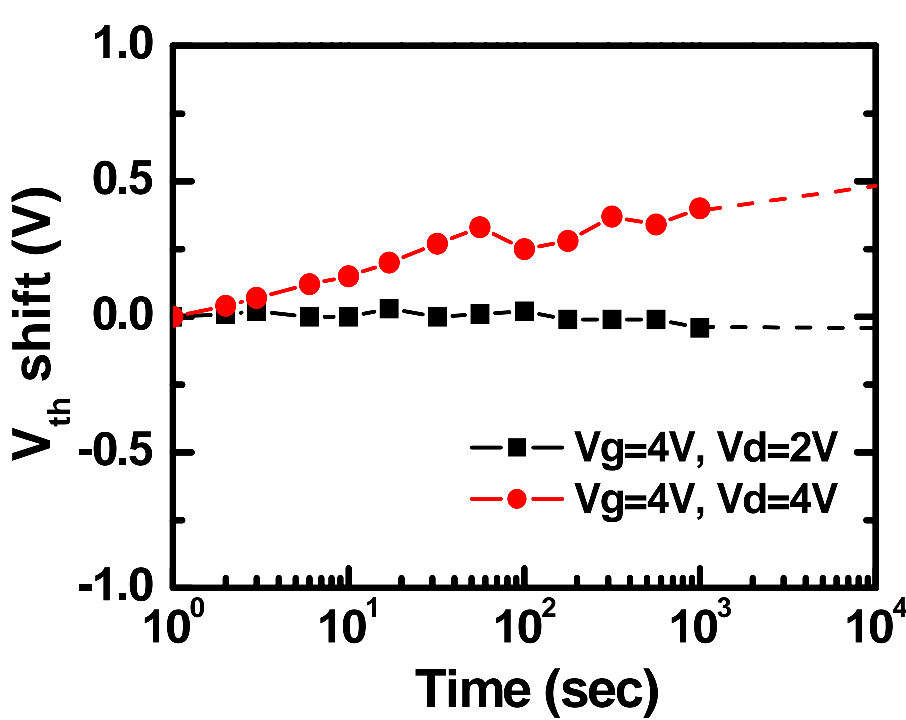


Figure 5.9 Read disturb characteristics of sol-gel derived memory.

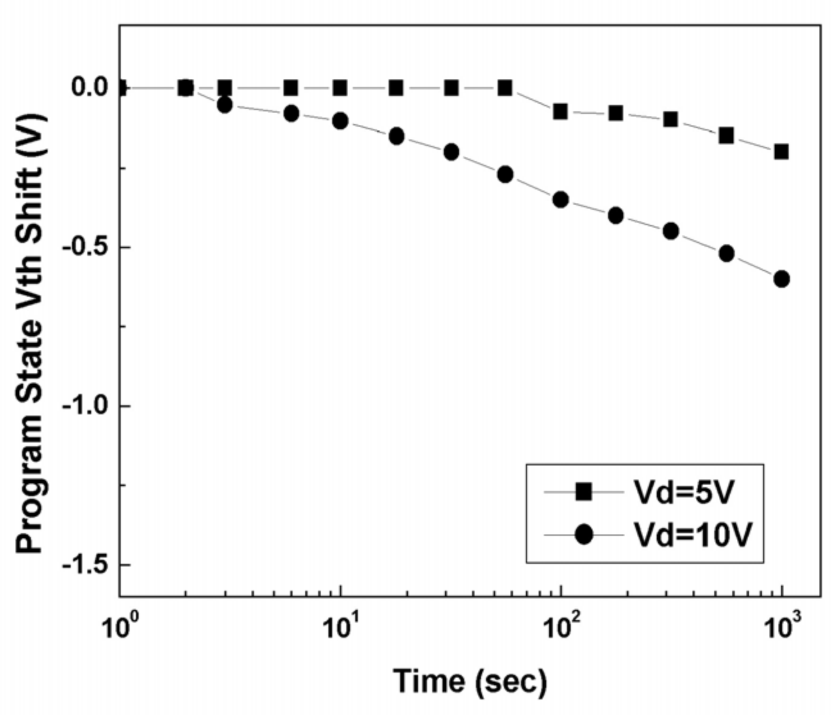


Figure 5.10 Drain disturb characteristics of sol-gel derived memory.

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Table 5.1 Comparison of various nanocrystal memory devices.

	Memory window	20% charge loss (sec)	Write speed (sec)	Leakage path
This Work*[60]*	2.8V~10V	$>10^6$	P: $>10^{-6}$ E: $>10^{-3}$	No
HfO_2*[45]*	1.5V~4V	$>10^4$	P: $>10^{-6}$ E: $>10^{-4}$	Lateral
Si dots*[68]*	0.5V~2.2V	$>10^6$	P: $>10^{-6}$ E: $>10^{-1}$	N/A
Metal dots*[36]*	1V~7V	$>10^4$	P: $>10^{-3}$ E: $>10^{-3}$	N/A
SONOS*[45]*	1.2V~5.2V	$>10^6$	P: $>10^{-6}$ E: $>10^{-5}$	Vertical

Chapter 6

Conclusions

We proposed a novel sol-gel spin-coating method utilized to deposit charge trapping layer for SONOS-like memory. The film formation with a spin coating is a more simple method than ALD, PVD, or CVD due to its cheaper precursor and tool. In addition, the film can be fabricated in the normal pressure system instead of high-vacuum system.

In **Chapter 3**, we discussed the NCs formation of the sol-gel spin-coating thin film at various annealing temperatures. The XPS characterization indicated the annealing treatment under oxygen ambient activated the formation of metal silicates. Together with the TEM images and interfacial energies, we proposed a mechanism to explain the transformation of sol-gel thin film to NCs. At 400 °C annealing, there was no effect occurred on sol-gel film. At 600 °C annealing, the sol-gel film started to be unstable. While annealing temperature was up to 900 °C, phase separation took place on the sol-gel film and made the thin film transformed to nanocrystals. During phase change, the sample surface had higher interfacial energy, and was minimized after crystallize to NCs. According to the data retention, we concluded that using the sol-gel derived NCs (900 ^{o}C annealing sample) as charge trapping layer exhibited better memory performance than thin film (600 ^{o}C annealing sample).

In **Chapter 4**, we investigated the sol-gel film thickness factor with respective to the morphology of NCs from different solvents. The solvent for dissolving sol-gel

solution precursors played an important role on the solution viscosity and film thickness. The IPA as solvent for sol-gel solution was more viscous than ethanol under the same concentration. For this reason, ethanol system can deposit thinner sol-gel film by spin coating method. The thinner film of ethanol system led to form the isolated NCs, while the interconnected NCs was observed in the thicker film of IPA system. The sol-gel derived isolated NCs of ethanol system exhibited better charge trapping performance and memory window.

In view of the sol-gel spin coating method was mature enough in our research. In **Chapter 5**, we utilized the best condition of sol-gel spin coating method for forming isolated NCs as charge trapping layer of a memory device. The sol-gel spin coating thin film transformed to nanocrystals after high temperature annealing (900 ^{o}C RTA) for phase separation of spinodal decomposition. The size of NCs was estimated to be 6-10 nm. We verified the NC memory device performance of the P/E speed, charge retention, endurance and disturbs. The quality of the NCs formed by the sol-gel spin coating method and RTA treatment exhibited excellent properties in terms of larger memory window, long retention time, good endurance, and superior disturbs.

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Publication and award lists

1. International Journal:

[1] Chi-Chang Wu, **Yi-Jen Tsai**, Min-Ching Chu, Shao-Ming Yang, Fu-Hsiang Ko, Pin-Lin Liu, Wen-Luh Yang, Hsin-Chiang You, "Nano-crystallization and interfacial tension of sol-gel derived memory", *Applied Physics Letters*, 92, 123111 **(2008).**

[2] **Yi-Jen Tsai**, Chi-Chang Wu, Pin-Lin Liu, Wen-Luh Yang, Feng-Chih Chang, Wen-Fa Wu, Fu-Hsiang Ko, " Phase separation of charge trapping layer for nanocrystal memory", *Nanotechnology*, submission.

2. Conference:

[1] **Yi-Jen Tsai**, Chi-Chang Wu, Fu-Hsiang Ko, Hsin-Chiang You, Tan-Fu Lei "Sol–gel-derived double-layered nanocrystal memory", *Symposium on Nano Device Technology* **(2007).**

[2] **Yi-Jen Tsai**, Chi-Chang Wua, Hsin-Chiang You, Fu-Hsiang Ko, Wen-Luh Yang, "Novel Coexisted Sol-Gel Derived SONOS-Type Memory" , *Symposium on Nano Device Technology*, **(2008).**

3. Awards:

[1] 15th Symposium on Nano Device Technology, Nano-electronic Devices and Technology section, **Golden Paper Award**.