Realizations of IIR/FIR and N-Path Filters Using a Novel Switched-Capacitor Technique

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Abstract —Applying novel switched-capacitor (SC) differentiators and the synthetic division technique, discrete-time IIR and FIR transfer functions have been realized by sample-data SC analog circuits. The resultant filter structures are simple, compact, and stray insensitive. Moreover, they have a low component sensitivity, good low-frequency noise performance, and large enough dynamic range. Theoretical calculation and SWITCAP simulation results on certain types of filters have shown good consistency with the experimental results, which substantiates both design methodology and circuit functions.

Multiplexing techniques can be directly applied to the SC differentiators without modification. Thus the multiplex differentiators can be used to design filter banks that may save chip area and dc power dissipation. Circuit examples are given and their functions are successfully verified through chip fabrication and measurement. The multiplexed SC differentiators are modified to form three types of N-path circuits, which can be used to design a narrow-band band-pass filter. Because the N-path circuits are based upon SC differentiators rather than SC integrators, they have distinct performance superior to that of SC integrator-based N-path circuits.

I. INTRODUCTION

MONOLITHIC switched-capacitor (SC) circuits in MOS technology have been widely applied to analog signal processing with a good accuracy and less chip area. Most SC circuits are based on the SC integrator, although it has certain limits in realizing analog functions. Recently, SC differentiators have been developed and various applications have been explored [1]–[6]. It is found that many circuits that are not realizable in conventional SC integrators can be implemented by SC differentiators. With both SC differentiators and integrators, therefore, the application field of SC circuits can be extended and their design versatility can be enhanced.

Recently, monolithic inverting and noninverting SC differentiators have been proposed and their noise performance has been analyzed and investigated [4]. It is shown that the SC differentiators have simple structures and are stray insensitive. In addition, they have a good noise

performance and are compatible in both fabrication technology and operation with conventional SC integrators [4]. It is expected that the proposed SC differentiator can be applied to design useful SC circuits and systems. The similar concept of the SC differentiators was also mentioned briefly in [1].

There are two interesting applications of SC circuits. One is the realization of discrete-time transfer functions in both infinite impulse response (IIR) and finite impulse response (FIR) forms. The other is the realization of multiplexed filter banks [7] and N-path filters [8]–[10]. There are two methods [11], [12] to implement an IIR transfer function by using SC integrators. In the first method [11], the SC circuit is first realized from the s-domain transfer function. Then the z-domain transfer function of the circuit is generated and compared to the specified one. Finally, capacitor values of the SC circuit can be determined to satisfy the specified z-domain transfer function. It is difficult, however, to use the proposed SC structure to implement a high-order IIR filter ($n > 2$) [11].

The second method proposed by Davis and Smith [12] relies on the synthetic division. By using this method, SC circuits can be constructed efficiently and directly from z-domain specifications. This method is a good design skill for SC circuits, because the design procedure is clear and easy. However, the proposed canonical structure has a high component sensitivity [12]. In addition, the dc instability phenomenon [6] may appear in some band-pass and high-pass SC integrator-based IIR filters.

In this paper, two canonical and two ladder structures are proposed for the realization of IIR transfer functions using SC differentiators and the synthetic division technique. In the proposed realization method, the differentiator type of the element $z^{-1} - 1$ is used instead of the z^{-1} element. The resultant SC IIR filters have shown the superiority over the conventional structures using z^{-1} in component sensitivity. They can also retain the advantages of SC differentiators, such as simple structure, stray insensitive, low sensitivity to offset voltage and power supply variations, and good noise performance at low frequency. Moreover, the "return to zero" sampling of the SC differentiator completely eliminates the dc insta-

bility problem [6] that may occur in some IIR filters designed by using SC integrators.

Generally an FIR filter cannot be directly implemented by SC integrators. To realize the FIR functions in SC circuits, Enomoto *et al.* [13] and Von Grunigen *et al.* [14] proposed a structure that uses three nonoverlapping clocks. Reddy *et al.* [15] also developed an SC structure based on the delta modulation. In that structure, digital storage elements and improved SC integrators are required. Recently, Lee *et al.* [16] proposed a multiple FIR filter on a single chip. It consists of 32 input signals that need 32 clock control phases. In our approach, SC differentiators are used directly to implement FIR filters [5]. The resultant FIR filters have a concise and simple structure with a low component and coefficient sensitivity. Noise analysis results have shown that the maximum number of stages can be as large as 32 stages and the dynamic range is still 60 dB. Direct use of SC differentiators also makes the SC FIR filters retain the advantageous features of SC differentiators.

The multiplexed filter banks [7] and N-path filters [8]–[10] have the common advantages of using less op amps and thus may save the chip area and dc power consumption in some voice-band applications. In addition, the N-path filters can solve the narrow-band problem [8]–[10]. In this work, the proposed SC differentiators are applied to realize the multiplexed filter banks and N-path circuits. The resultant circuits are quite concise and can retain their inherent advantageous features as well as those of SC differentiators.

In the following sections, the design algorithms for IIR and FIR filters, the multiplexing technique, and N-path circuits will be described. Design examples are also given to verify the algorithms. Part of the designed filters was fabricated in 3.5-μm p-well CMOS technology with poly-n^+ capacitors. Experimental results are in good consistency with theoretical calculation and simulation results, which substantiates the design algorithms and circuit structures.

II. SC DIFFERENTIATORS

Fig. 1 shows the structure of the proposed inverting SC differentiator [1], [4], where two nonoverlapping clocks $\phi 1$ and $\phi 2$ are required to operate the differentiator. It is shown that the structure is simple and stray insensitive. In addition, the sampling method in this circuit is of the "return-to-zero" type. Therefore, the offset voltage and the power supply voltage variation have less effect on the op amp performance. Moreover, the op amp always shows a maximum gain and symmetry when signals enter. Thus a maximum output swing and stable initial state for the transient response can be obtained.

The transfer function $H(z)$ of the SC differentiator can be written as [4]

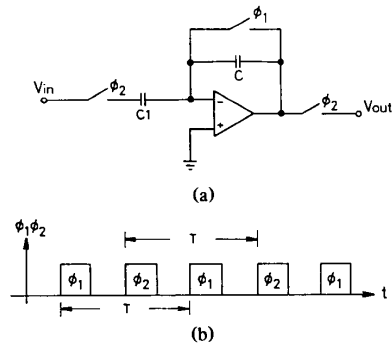$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C1}{C}(z^{-1}-1). \tag{1}$$

Fig. 1. (a) The circuit diagram. (b) The clock waveforms of an SC differentiator.
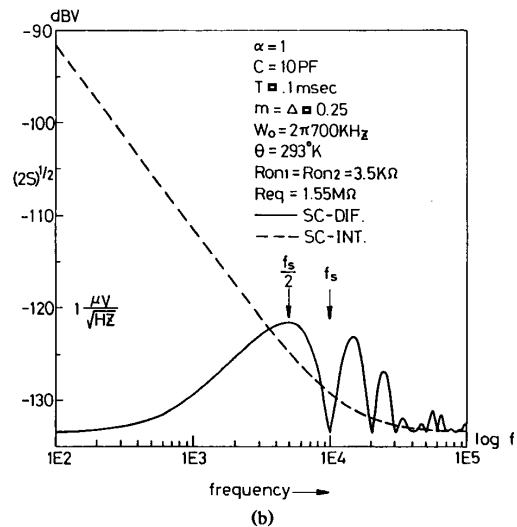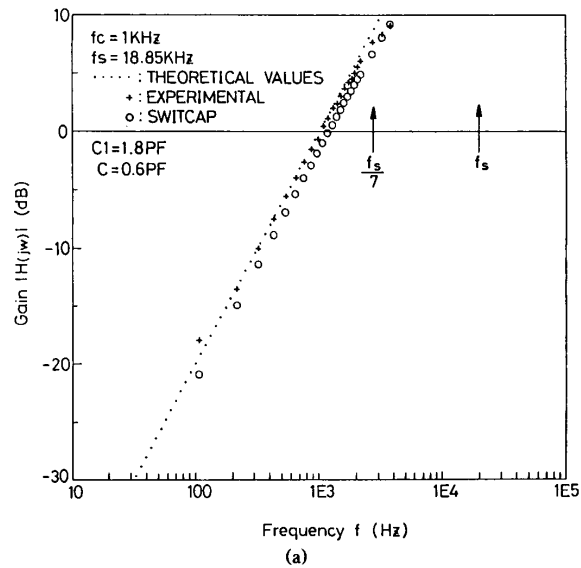

Fig. 2. (a) Frequency characteristics of the SC differentiator of Fig. 1 with $C1 = 1.8$ pF and $C = 0.6$ pF. (b) Noise spectra of the SC differentiator and integrator.

When $sT \ll 1$, we can apply the backward-difference mapping $s = (1/T)(1 - z^{-1})$ to (1). The result is

$$H(s) = -(C1/C)Ts. \tag{2}$$

As may be seen from (2), the time constant of the differentiator is equal to the capacitance ratio $(C1/C)$ times the clock period T, which can be precisely controlled in integrated-circuit technology. Note that the SC differentiator is inherently stable even in the dc case because its pole is located at $z = 0$, as may as seen from (1).

The measured frequency response of the fabricated SC differentiator is shown in Fig. 2(a) [4]. It is seen that the gain is linearly proportional to the frequency f. If the signal frequency f increases toward the sampling frequency f_s, the signal is gradually suppressed by sampling and the deviations from (2) become larger. This is a phenomenon common to all sample-data circuits. Similarly, for the noise with a frequency close to or larger than f_s, it is also suppressed by sampling. Thus the SC differentiator is free from high-frequency noise overriding. The calculated noise spectra of both the SC integrator and the SC differentiator are compared in Fig. 2(b) [4]. It is seen that the SC differentiator retains its inherent noise rejection in the low-frequency range and suppresses the high-frequency noise through the sampling operation. In view of this rejection capability to high-frequency noises, the SC differentiator is quite different from its active-RC version.

To invert a signal, the SC inverter shown in Fig. 3 can be used. This circuit can be conveniently incorporated with SC differentiator circuits to perform signal inversions. The transfer function $H(z)$ of this circuit can be expressed as [4]

$$H(z) = -(C2/C). \tag{3}$$

III. REALIZATION OF IIR/FIR FUNCTIONS USING SC DIFFERENTIATORS

A. IIR Filters

A z-domain IIR transfer function can be written as

$$H(z) = \frac{\sum\limits_{n=0}^{N} \bar{b}_n z^{-n}}{1 - \sum\limits_{n=1}^{N} \bar{a}_n z^{-n}}. \tag{4}$$

Applying the mathematical technique [12], (4) can be transformed into

$$H(z) = \frac{-b_0 + \sum\limits_{n=1}^{N} b_n (z^{-1} - 1)^n}{1 - \sum\limits_{n=1}^{N} a_n (z^{-1} - 1)^n}. \tag{5}$$

It is shown that 2^n distinct direct realizations are possible for an nth-order function [17]. Thus distinct performance
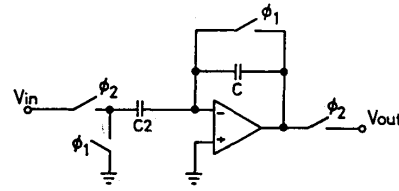

Fig. 3. An SC inverter.

features can be obtained with the realized 2^n network topologies.

As an illustrating example, two canonical and two ladder structures are adopted to realize the transfer function in (5), and the resultant circuits are analyzed. In these sample-data structures, $z^{-1} - 1$ is the basic element. The design procedures in conventional digital structures with z^{-1} as the basic delay element can be applied without modification. Thus the network function of (5) can be generated with summers, multipliers, and the differentiator-type elements, $z^{-1} - 1$.

For the first realization structure, called the observer canonical form, (5) can be realized by the signal flow graph (SFG) shown in Fig. 4(a). In this SFG, all the $z^{-1} - 1$ blocks with their coefficients can be implemented by SC differentiators, whereas the constant coefficient b_0 by an SC inverter. The resultant SC circuit is shown in Fig. 4(b) where the absolute values of filter coefficients are implemented by capacitor ratios. Since filter coefficients may be positive or negative, the switches Sa and Sb are used to choose the correct signal path. If the coefficients a_n and b_n are negative, the signal paths b and w are chosen, respectively. In each of these signal paths, an SC inverter is added to invert the input signal V_{in} or the output signal V_{out}.

In Fig. 4(b), the operational amplifiers OP1 and OP2 have maximum capacitor loads. They are

$$C_{\text{OP1}} = |b_0|Cc1 + |b_1|Cc1 + \cdots + |b_N|CcN + C$$

$$C_{\text{OP2}} = CL + C + |a_1|Cc1 + \cdots + |a_N|CcN + Cc1.$$

So the slew rate and settling time of these op amps should be carefully considered in practical IC design.

A design example is given below to demonstrate the developed design method. Consider a second-order IIR transfer function $H_1(z)$:

$$H_1(z) = \frac{-12 + 12z^{-2}}{38 - 72z^{-1} + 35z^{-2}}. \tag{6}$$

If the sampling frequency is chosen as 37.7 kHz, the gain response of (6) calculated by using $z = e^{jwT}$ is plotted in Fig. 5(a) by the dotted line. Applying the mathematical technique to the transfer function in (6), it can be transformed into the desired form as

$$H(z) = \frac{24(z^{-1} - 1) + 12(z^{-1} - 1)^2}{1 - 2(z^{-1} - 1) - (-35)(z^{-1} - 1)^2}. \tag{7}$$
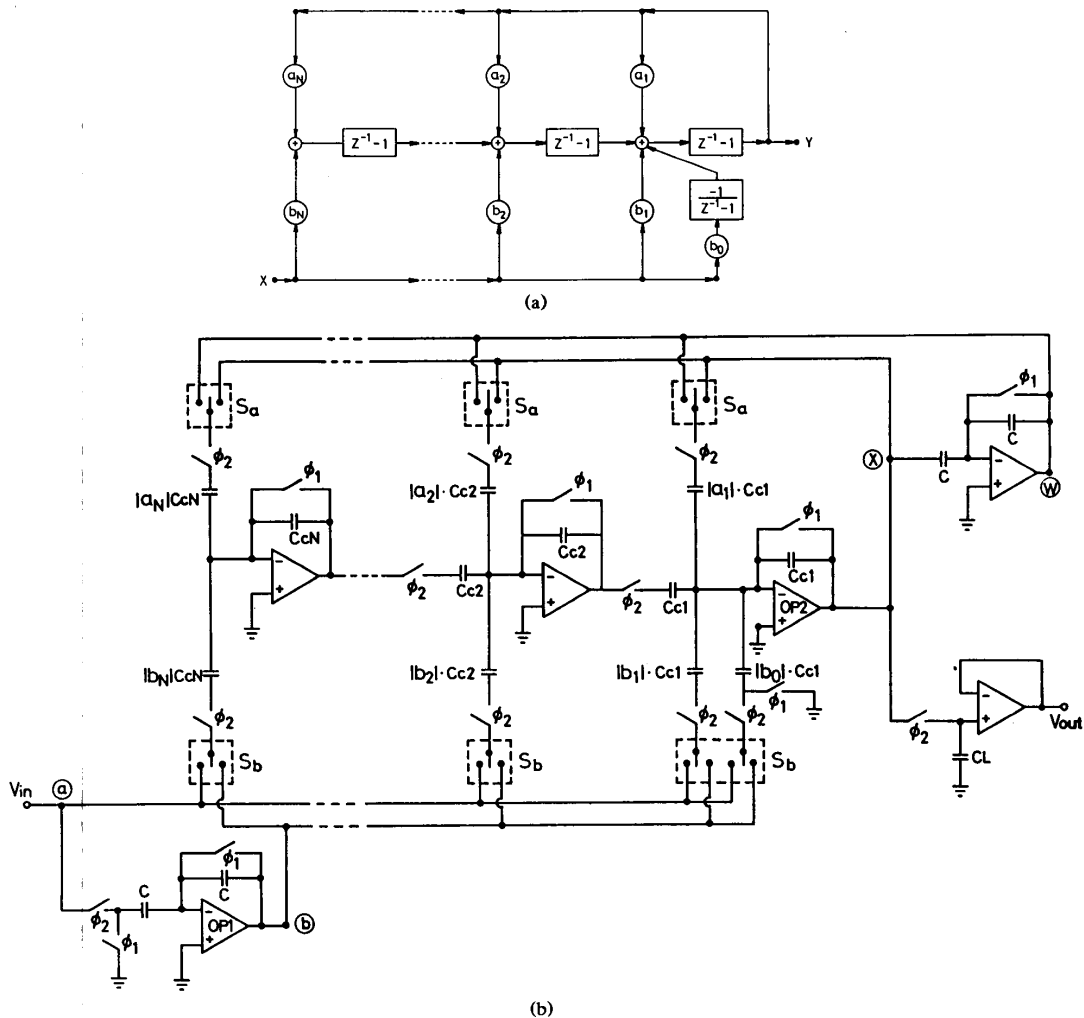
(a)

(b)

Fig. 4. Observer canonical form of IIR filters with the SC differentiator as a basic element. (a) The signal flow graph (SFG). (b) The SC circuit structure.

Matching the coefficients of (5) to those of (7), we have

$$b_0 = 0; \ b_1 = 24; \ a_1 = 2; \ b_2 = 12; \ a_2 = -35.$$

With these coefficients, the circuit is realized from that of Fig. 4(b) and shown in Fig. 5(b). The capacitance values are determined and listed in the same figure. SWITCAP [18], [19] simulation results are plotted in Fig. 5(a), which show a good consistency with theoretical calculation results.

To experimentally verify the operation of the realized IIR filter, a test chip was designed to implement the filter. This chip was designed in analog gate-array style and fabricated by 3.5-μm p-well CMOS technology with poly-n$^+$ capacitors. A photomicrograph of the fabricated chip is shown in Fig. 6, where the unit capacitors, trans-

mission gate arrays, and op amp arrays are indicated. The measured filter response is also shown in Fig. 5(a). Good agreement substantiates the design algorithm.

In the circuit structure of observer canonical form, all multiplications are performed simultaneously. As a consequence, the time taken to process one filter cycle can be as short as the time to perform one multiplication. In addition, the coefficients a_n and b_n of (5) are composed of the coefficients $\bar{a}_n$ and $\bar{b}_n$ of (4). So this observer canonical structure with $z^{-1} - 1$ elements has lower coefficient sensitivities than the observer canonical structure with z^{-1} elements.

Alternatively, the transfer function of (5) can also be realized by using the observability canonical form [20] whose structure is shown in Fig. 7(a). The relations between the coefficient d_n in Fig. 7(a) and the coefficient b_n

fc = 1KHz
fs = 37.7KHz
······ : THEORETICAL
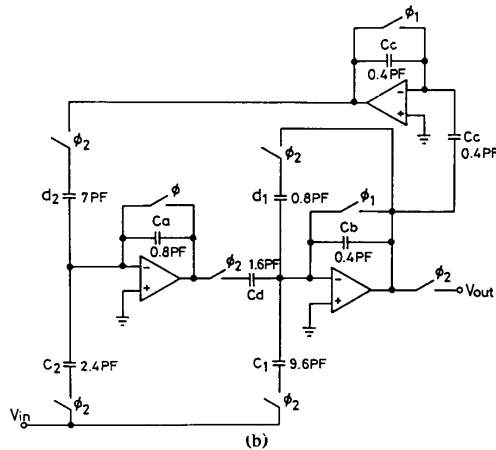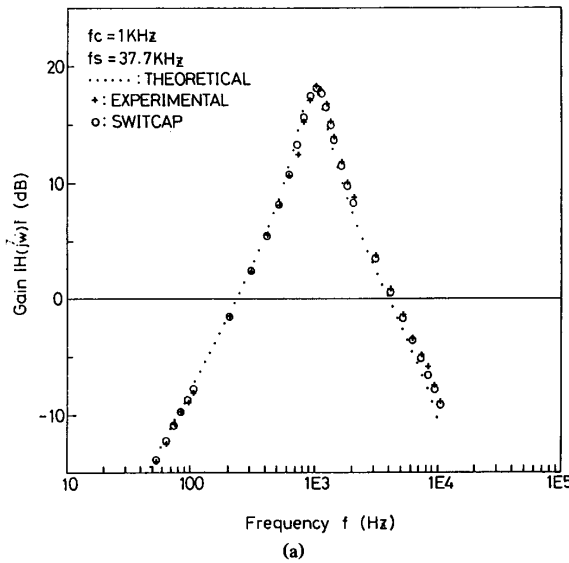+ : EXPERIMENTAL
o : SWITCAP

Frequency f (Hz)

(a)

(b)

Fig. 5. (a) Theoretical, measured, and simulated frequency responses.
(b) The SC circuit diagram of the fabricated second-order IIR filter.

of (5) are given by

$$
\begin{bmatrix}
1 & & & & & \\
-a_1 & 1 & & & & \\
-a_2 & -a_1 & 1 & 0 & & \\
\vdots & \vdots & \cdots & 1 & & \\
-a_{n-1} & -a_{n-2} & \cdots & -a_1 & 1 & \\
-a_n & -a_{n-1} & \cdots & -a_2 & -a_1 & 1
\end{bmatrix}
\cdot
\begin{bmatrix}
-d_0 \\
d_1 \\
d_2 \\
d_{n-2} \\
d_{n-1} \\
d_n
\end{bmatrix}
=
\begin{bmatrix}
-b_0 \\
b_1 \\
b_2 \\
b_{n-2} \\
b_{n-1} \\
b_n
\end{bmatrix}
\tag{8}
$$

On the other hand, the coefficient a_n in Fig. 7(a) is the
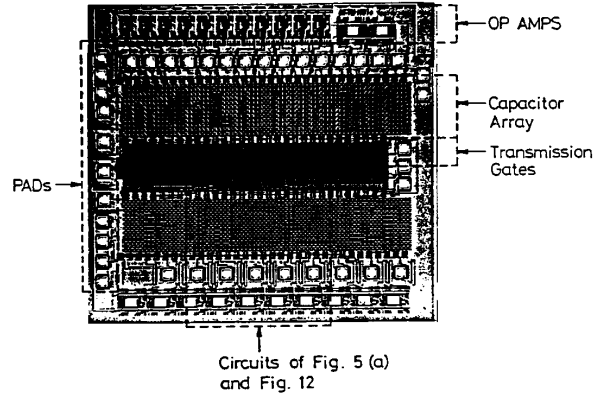

Circuits of Fig. 5 (a)
and Fig. 12

Fig. 6. Photomicrograph of the test chip.

same as the coefficient a_n of (5). Because each coefficient d_n is composed of the forward coefficients b_n's of (5), the transfer function of observability canonical form has a lower sensitivity to the variations of forward coefficients than the observer canonical form.

The other two realization methods to be considered here are of the ladder realization. They are the controller ladder and the observer ladder structures as shown in Fig. 7(b) and (c), respectively. The coefficients of these structures can be directly calculated by using the similar method [21] with $z^{-1}-1$ elements in the modified transfer function of (5) rather than z^{-1} elements in the transfer function of (4). Note that the two realized ladder structures still retain their well-known ultra-low component sensitivity, which is much smaller than the two canonical structures described above.

A design example is given below to demonstrate the filter realization using the observer ladder form. The transfer function of a third-order Butterworth low-pass filter is

$$
H_a(s) = \frac{1}{\left(\dfrac{s}{w_0}\right)^3 + 2\left(\dfrac{s}{w_0}\right)^2 + 2\left(\dfrac{s}{w_0}\right) + 1}
\tag{9}
$$

where $w_0 = 2\pi(1\ \text{kHz})$. Applying the bilinear transformation $s = (2/T)(1 - z^{-1}/1 + z^{-1})$ to (9) yields the following z-domain transfer function:

$$
H(z) = \\
\frac{\dfrac{8}{8} + \dfrac{12}{8}(z^{-1}-1) + \dfrac{6}{8}(z^{-1}-1)^2 + \dfrac{1}{8}(z^{-1}-1)^3}{1 - \dfrac{84}{8}(z^{-1}-1) - \left(-\dfrac{486}{8}\right)(z^{-1}-1)^2 - \dfrac{1463}{8}(z^{-1}-1)^3}.
\tag{10}
$$

The SFG of this z-domain transfer function is given in Fig. 8(a), and the values of coefficients c_n and d_n are also given in the figure. The resultant SC ladder realization is shown in Fig. 8(b), where the capacitor values are also given and the sampling frequency is 37.7 kHz. Suitable
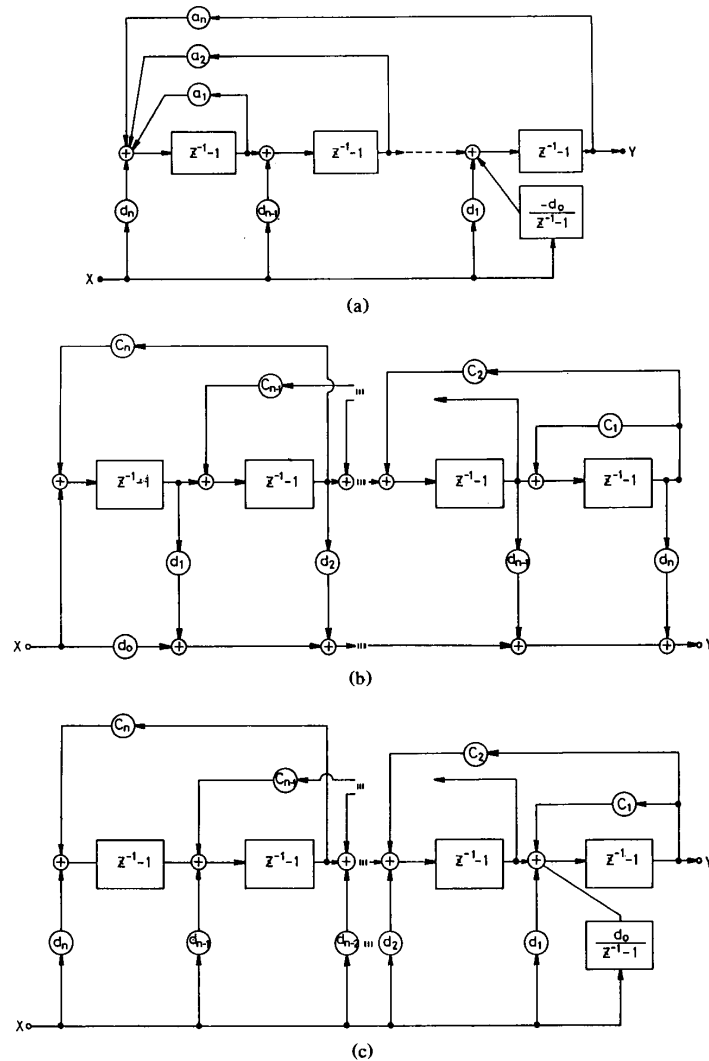
Fig. 7. Three distinct signal flow graphs (SFG's) of an IIR transfer function with the SC differentiator as a basic element. (a) The observability canonical form. (b) The controller ladder form. (c) The observer ladder form.

scaling has been applied to determine the values of those capacitors in Fig. 8(b) so that the filter coefficients a_n and b_n of (10) can be realized exactly and so the capacitor values have an adequate spread. The SWITCAP simulation results of this observer ladder type of IIR filters are given in Fig. 8(c). It can be seen from Fig. 8(c) that SWITCAP simulation results are in good consistency with theoretical calculation results.

It is known that there are many possible structures with different performance features for a given IIR filter transfer function. Based upon the developed design methodology and the differentiator-type elements $z^{-1} - 1$, other network topologies besides the demonstrated four structures, such as cascade, parallel, direct, direct canonic, ladder, wave, or combinations of them can also be used to realize the transfer function of (5).

Just like the LCR ladder filters designed by using SC integrators, the realized IIR filters using SC integrators with $1/(z^{-1} - 1)$ basic blocks have a dc instability problem [6] in some cases such as some bandpass and high-pass IIR filters. Thus dc feedback path checking and circuit structure modification [6] are required before a stable SC-integrator-based IIR filter could be obtained. In realizing those IIR filters using the proposed SC differentiator-based circuits, however, the "return-to-zero" sampling type completely eliminates this dc instability problem. This is a significant advantage of the proposed IIR filters over the conventional SC-integrator-based structures. The other advantage is that the SC-differentiator-based IIR filters have a lower component sensitivity than the SC-integrator-based structures. This will be proved in the following subsection. In addition, these SC-differ-
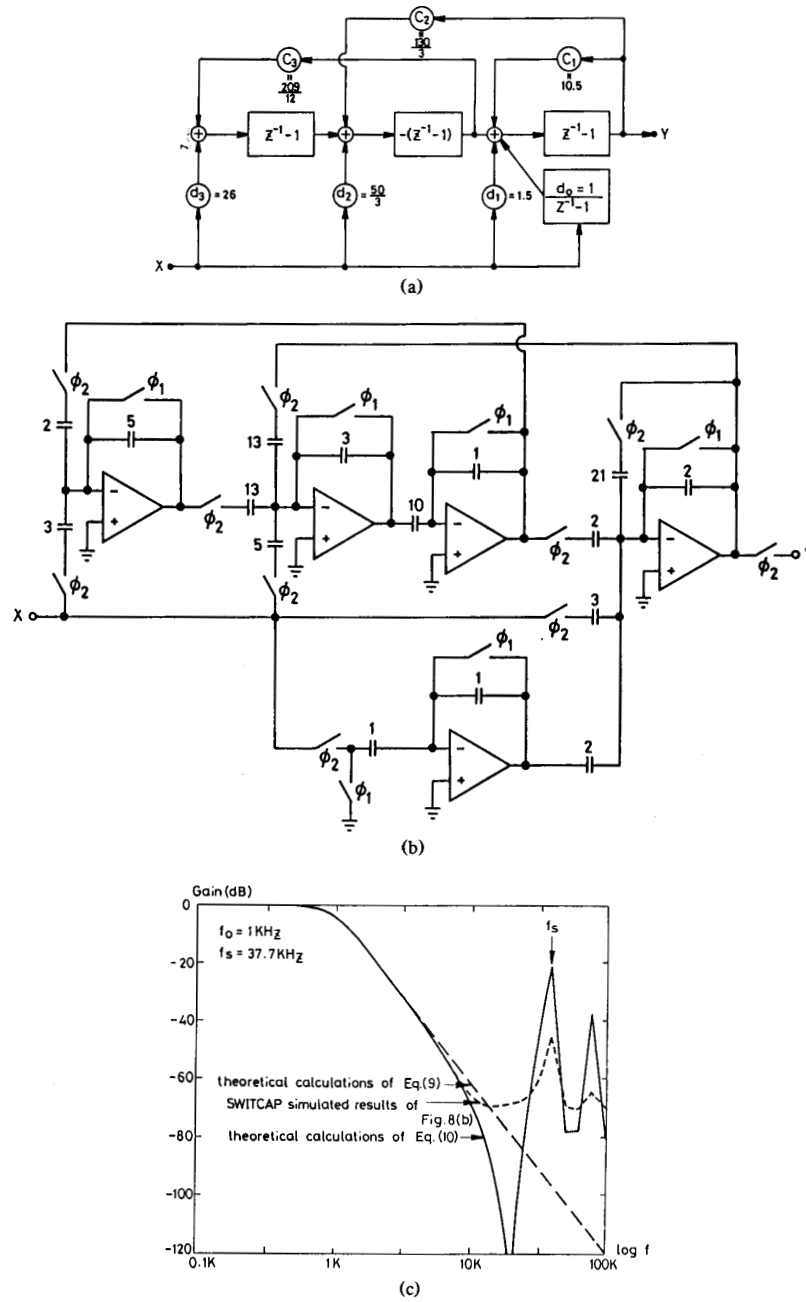
Fig. 8. A third-order observer ladder form of a low-pass IIR filter with the SC differentiator as a basic element. (a) The signal flow graph. (b) The resultant SC circuit structure. (c) The SWITCAP simulated frequency responses with the theoretical calculations.
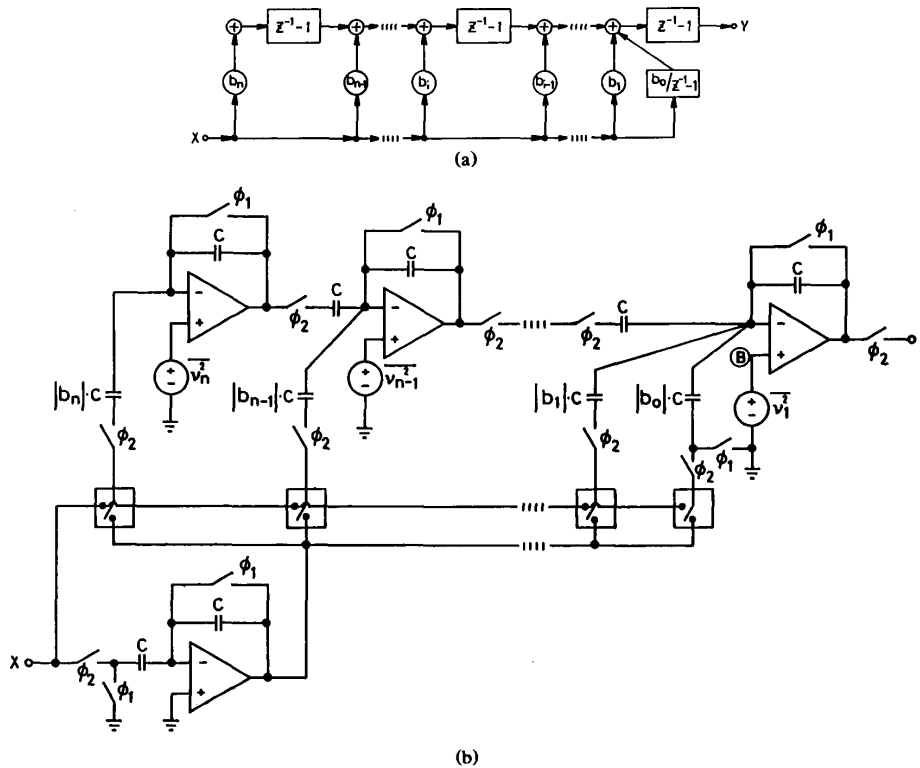
Fig. 9. (a) The signal flow graph. (b) The resultant SC circuit diagram of an FIR filter.

entiator-based IIR filters retain the inherent advantageous performance of the SC differentiator that has been described in Section II.

B. FIR Filters

An FIR filter can be characterized by the z-domain transfer function

$$H(z) = \sum_{n=0}^{N} \bar{b}_n z^{-n}. \tag{11}$$

Applying the above-developed mathematical technique, this polynomial form can be transformed into the form

$$H(z) = \sum_{n=0}^{N} b_n (z^{-1} - 1)^n. \tag{12}$$

Since an FIR filter function is the same as the numerator of an IIR filter function, its signal flow graph and the resultant SC circuit can be implemented as those shown in Fig. 4, but without all the feedback loops. The resultant SFG and SC circuit structure of an FIR filter are shown in Fig. 9(a) and (b), respectively.

In the study of arithmetic errors in this SC FIR structure, the sensitivities to the variations of multiplier constants are considered. The network function of Fig. 9(a) can be characterized by

$$H(z) = f(z^{-1} - 1, b_1, b_2, \cdots) \tag{13}$$

where $b_1, b_2, \cdots$ are the multiplier constants. The sensitivities of this network topology are given by [22]

$$D_{b_i}^H(z) = \frac{\partial H(z)}{\partial b_i}$$

$$= (\text{multiplier input})_{\text{original}}(\text{multiplier input})_{\text{adjoint}}$$

$$= (z^{-1} - 1)^i. \tag{14}$$

If the z-domain transfer function of (11) is directly implemented by a similar structure with the delay elements z^{-1}, the sensitivity of this circuit to the variations of multiplier constants can be obtained as

$$D_{\bar{b}_i}^H(z) = \frac{\partial H(z)}{\partial \bar{b}_i} = (z^{-1})^i. \tag{15}$$

If $|D_{b_i}^H(z)| \leqslant |D_{\bar{b}_i}^H(z)|$, we have $|z^{-1} - 1| \leqslant |z^{-1}|$, which leads to

$$f \leqslant f_s/6 \tag{16}$$

where $f_s = 1/T$ is the sampling frequency. This means that as soon as the signal frequency is smaller than $f_s/6$ or $wT \leqslant \pi/3 \approx 1$, the sensitivity of the proposed FIR circuit to the variations of multiplier constants is less than that of the circuit with the delay element z^{-1}. Since $wT \ll 1$ and $f \ll f_s$ in an SC circuit, we have $|D_{b_i}^H(z)| \ll 1$

and $|D_{b_i}^H(z)| \ll |D_{\overline{b}_i}^H(z)|$. Under the same consideration, one can obtain the conclusion that the normalized sensitivity functions $S_{b_i}^H \equiv \frac{b_i}{H} D_{b_i}^H$ has a much smaller magnitude than $S_{\overline{b}_i}^H$. In view of the sensitivities of this circuit to the variations of multiplier constants, the proposed SC FIR circuit is superior to other circuits implemented by the delay element z^{-1}.

The above sensitivity analysis can be also applied to the IIR filters. It is shown that the realized IIR filters with SC differentiators have much lower component sensitivities than the SC-integrator-based IIR filters. This is because the values of $|z^{-1} - 1|$ in SC-differentiator-based structures is much lower than those of $|1/(z^{-1} - 1)|$ in SC integrator-based structures. Although conventional SC integrators can be used to realize IIR filters, they cannot be applied to realize FIR filters directly using the above described design technique.

As in other analog filters, the noise leads to a fundamental limitation on the dynamic range. Because the dominant noise source of an SC differentiator is the equivalent thermal noise [4], only the equivalent input thermal noise of op amps is considered in analyzing the noise effect of the FIR structure. Assume the mean square value of an equivalent noise source at the input of the ith op amp is $\overline{V_i^2}$ as shown in Fig. 9(b). Since all the noise sources are uncorrelated, the total equivalent noise appearing at the input node B of the last op amp in this SC FIR filter can be determined as

$$\overline{V_B^2} = \sum_{i=1}^{n} \overline{V_i^2} A_i^2 \qquad (17)$$

where $A_i = |z^{-1} - 1|^{i-1}$. Assuming $\overline{V_n^2} = \overline{V_{n-1}^2} = \cdots = \overline{V_1^2}$, the equivalent noise source $\overline{V_B^2}$ can be rewritten as

$$\overline{V_B^2} = \overline{V_n^2} \left[(|z^{-1} - 1|^{2n} - 1) / (|z^{-1} - 1|^2 - 1) \right]. \qquad (18)$$

Note that the value $|z^{-1} - 1|$ has a maximum value $\sqrt{2}$ when the spectra frequency of the equivalent thermal noise is equal to $f_s/2$. Thus (18) has a maximum value of

$$\overline{V_{B(\text{max})}^2} = \overline{V_n^2}(2^n - 1). \qquad (19)$$

The equivalent input thermal noise of an op amp is usually in the range of 4 to 60 nV/$\sqrt{\text{Hz}}$ [23], so the maximum value of the equivalent noise is only 4 mV/$\sqrt{\text{Hz}}$ when the stage number n of the SC FIR filter is as large as 32. If the maximum output swing is ± 5, a dynamic range over 60 dB can be obtained in the last op amp.

In usual applications, the signal frequency is much lower than the sampling frequency f_s. Thus this maximum equivalent noise source of the FIR filter at $f_s/2$ can be easily removed by using an adequate post filter. Moreover, through an adequate design procedure and/or good process technique, a low noise op amp can be designed to increase the maximum number of stages and/or the dynamic range of this SC FIR filter.

A linear-phase low-pass FIR filter is designed in the following example by using the proposed FIR structure.

The transfer function in the jw-domain is

$$H(e^{jwT}) = \begin{cases} e^{-jw\alpha T}, & |w| \leqslant w_c = \dfrac{w_s}{20} \\ 0, & \text{otherwise} \end{cases}$$

where w_s is the sampling angular frequency, αT is the group delay, and w_c is the center frequency. The corresponding impulse response is

$$\overline{b}_n' = \frac{\sin w_c(n - \alpha)}{\pi(n - \alpha)}, \qquad n \neq \alpha.$$

Clearly, $\overline{b}_n'$ has an infinite duration. To create a finite duration linear-phase FIR filter of the length $N = 10$, we choose the Hanning window $w(n) = 1/2[1 - \cos(2\pi n / N - 1)]$. Then, $\overline{b}_n$ can be obtained as

$$\overline{b}_n = \overline{b}_n'^* w(n), \qquad 0 \leqslant n \leqslant N - 1 = 9$$

$$= \frac{\sin w_c(n - \alpha)}{2\pi(n - \alpha)} \left[1 - \cos\left(\frac{2\pi n}{N - 1} \right) \right],$$

$$\alpha = (N - 1)/2 = 4.5.$$

The numerical values of $\overline{b}_n', \overline{b}_n, b_n$, and the truncated numbers of $\overline{b}_n$ and b_n, are listed in Table I. The gain and phase responses are calculated and shown in Fig. 10(a) and (b), respectively. As shown in Fig. 10(a), the passband width of this filter is defined as the center frequency f_c plus the mainlobe transition width of the gain response, which is approximately $(1/20) + (2/10)f_s = (1/4)f_s$. SWITCAP simulation results with both exact b_n and truncated b_n coefficients are also shown in Fig. 10(a) and (b), respectively, where the consistency with theoretical calculation results is quite good, especially in the passband.

From both theoretical calculations and SWITCAP simulations, it is seen that this circuit is a good linear-phase filter. The group delay from SWITCAP simulation results is $4.5T$ ($T = 100$ μs) consistent with the theory. The dc gain of the filter can be adjusted through the feedback capacitor C of the last op amp in Fig. 9(b).

Since the realized FIR filters make use of SC differentiators directly, they all have the advantageous features of SC differentiators as mentioned in Section II. As compared with other FIR filters [13]–[16], the proposed structure is simpler and more concise whereas the design method is easy. This makes the structure quite attractive in many VLSI applications.

IV. MULTIPLEXING TECHNIQUE AND N-PATH CIRCUITS

A. Multiplexing Technique

For the proposed SC differentiator, the multiplexing technique can be developed to allow some op amps servicing many filter channels at a time.

Fig. 11(a) shows the basic multiplexing structure for the proposed SC differentiator circuit. Their control clocks are plotted in Fig. 11(b). As may be seen from Fig. 11, the period of all internal clock signals $\phi_1 \sim \phi_N$ is NT and each clock is successively shifted by T. On the other hand,

TABLE I
NUMERIC VALUES OF $\bar{b}_n', \bar{b}_n, b_n$, TRUNCATED $\bar{b}_n$, AND TRUNCATED b_n

n	$\bar{b}_n'$	$\bar{b}_n$	b_n	Truncated $\bar{b}_n$	Truncated b_n
0	0.069864658507	0	0.43103821256	0	0.430
1	0.081033195801	0.00947908322	1.93967195652	0.009	1.935
2	0.090031631616	0.03719890143	3.92975777200	0.037	3.914
3	0.096339776200	0.07225483215	4.70234973824	0.072	4.669
4	0.099589273524	0.09658628948	3.62883759458	0.097	3.587
5	0.099589273524	0.09658628948	1.84212087273	0.097	1.810
6	0.096339776200	0.07225483215	0.59806147232	0.072	0.583
7	0.090031631616	0.03719890143	0.11303156719	0.037	0.109
8	0.081033195801	0.00947908322	0.00947908322	0.009	0.009
9	0.069864658507	0	0	0	0

the clock ϕ has a period of T and is nonoverlapping to other clocks. It can be easily shown that the output transfer functions in the z-domain are

$$H_1(z) = \frac{V_{out1}(z)}{V_{in1}(z)} = -\frac{C1}{C}(1 - z^{-1})$$

$$H_2(z) = \frac{V_{out2}(z)}{V_{in2}(z)} = -\frac{C2}{C}(1 - z^{-1})$$

$$\vdots$$

$$H_N(z) = \frac{V_{outN}(z)}{V_{inN}(z)} = -\frac{CN}{C}(1 - z^{-1}) \qquad (20)$$

where

$$z = \exp(sNT).$$

Thus N SC differentiators can be implemented by using only one op amp.

The above multiplexing technique can be applied to the design of filter banks. As a demonstrating example, two second-order IIR filters are designed using the developed method. One of the filter transfer functions is given in (6). The other is given below:

$$H_2(z) = \frac{-12 + 12z^{-2}}{37 - 72z^{-1} + 35z^{-2}}. \qquad (21)$$

Using the design algorithm in Section III-A, $H_2(z)$ can be similarly realized. Then the two filters are merged by using the above developed multiplexing method. The realized filter is shown in Fig. 12(a). The control clocks ϕ_1 and ϕ_2 have a frequency of 37.7 kHz and their timing diagrams are plotted in Fig. 12(b). The filter bank was fabricated by using the 3.5 μm analog CMOS process. The measured response of one of the fabricated IIR filters $(H_1(z))$ is shown in Fig. 5(b), whereas that of the

other IIR filter $(H_2(z))$ is shown in Fig. 13. Good agreement among theoretical calculations, SWITCAP simulations, and measured results confirms the correctness of the proposed multiplexing method.

Unlike the case in the multiplexed SCF banks using SC integrators [7], the proposed multiplexing technique using SC differentiators does not require any modification of the original differentiator structure. Thus the resultant multichannel filter bank retains all the advantageous features of the original SC differentiator-based filters as mentioned in Sections II and III.

In a filter bank consisting of N filter channels, only one-Nth of op amps is required as compared to the conventional filter structures. But the control clock frequency of each op amp is N times higher than that in the conventional structure. For voice-band CMOS op amps, N times of increase in clock operation frequency still can be achieved without N times of increase in power dissipation. In this case, the filter bank can save the dc power consumption. As to the chip area, however, it should be noted that like all other multiplexed SCF banks, the saved op amp area might be outweighed by additional clock buses, clock drivers, and interconnection lines.

B. N-Path Filters

The multiplexed SC differentiator shown in Fig. 11(a) can be modified to form a basic-type N-path circuit. This is done by choosing $C2 = C3 = \cdots = CN \equiv C1$ in Fig. 11(a) and merging all the output terminals to form a single output and all the input terminals to form a single input. The resultant circuit structure is shown in Fig. 14(a) where the internal clock signals are the same as those in Fig. 11(b) and repeated in Fig. 14(b). It is evident that the function of the circuit of Fig. 14(a) is similar to that of Fig. 1(a), except that each input capacitor $C1$ is
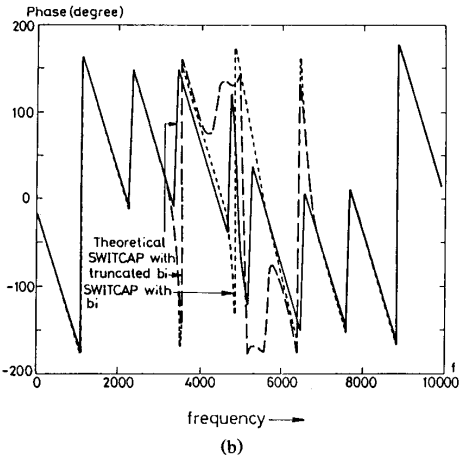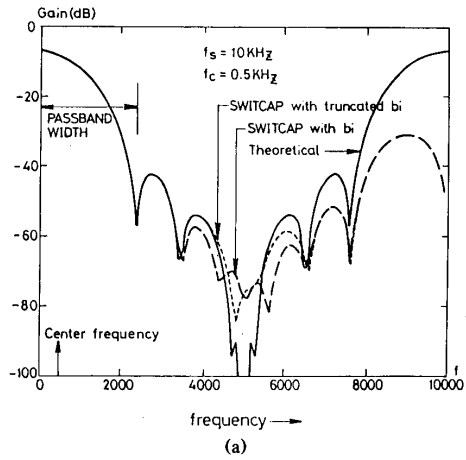
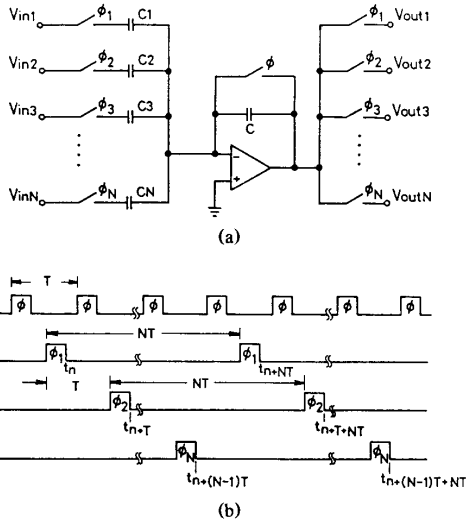Fig. 10. An example FIR filter. (a) The gain. (b) The phase responses.

Fig. 11. (a) Multiplexed SC differentiator circuit. (b) Its clock waveform diagram.

operated by an NT-period clock, rather than a T-period clock.

If all signal paths are identical, they have the same transfer functions as

$$H_p(z) = \frac{V_{out1}(z)}{V_{in1}(z)} = \frac{V_{out2}(z)}{V_{in2}(z)} \qquad (22)$$

where

$$z = \exp(sNT).$$

Since every signal path is activated within a single period T and left open for the other $(N-1)T$ periods, the transfer functions in (22) can be reexpressed as

$$H_p(z) = \frac{V_{out1}(z_a)}{V_{in1}(z_a)} = \frac{V_{out2}(z_a)}{V_{in2}(z_a)} \qquad (23)$$

where

$$z_a = \exp(sT) = z^{1/N}.$$

The overall transfer function can be found as

$$
\begin{aligned}
&H(z_a) \\
&= \frac{V_{out}(z_a)}{V_{in}(z_a)} = \frac{V_{out1}(z_a) + V_{out2}(z_a) + \cdots + V_{out}N(z_a)}{V_{in1}(z_a) + V_{in2}(z_a) + \cdots + V_{in}N(z_a)} \\
&= \frac{H_p(z)V_{in1}(z_a) + H_p(z)V_{in2}(z_a) + \cdots + H_p(z)V_{in}N(z_a)}{V_{in1}(z_a) + V_{in2}(z_a) + \cdots + V_{in}N(z_a)} \\
&= H_p(z) = -\frac{C1}{C}(1 - z^{-1}) = -\frac{C1}{C}\left(1 - z_a^{-N}\right) \qquad (24)
\end{aligned}
$$

where

$$z_a = \exp(sT) = z^{1/N}.$$

The z-plane pole/zero pattern of Fig. 15(a) can be transformed into the z_a-plane pattern shown in Fig. 15(b) for $N = 3$. In the following example, a narrow-band bandpass filter is designed by using this basic-type N-path structure.

Applying the bilinear transformation $s = 2(1 - z^{-1})/T(1 + z^{-1})$ to the analog transfer function in (9) yields the following z-domain transfer function:

$$H(z)$$

$$= \frac{1 + \dfrac{3}{2}(z^{-1}-1) + \dfrac{3}{4}(z^{-1}-1)^2 + \dfrac{1}{8}(z^{-1}-1)^3}{1 - \dfrac{13}{2}(z^{-1}-1) - \dfrac{-99}{4}(z^{-1}-1)^2 - \dfrac{399}{8}(z^{-1}-1)^3} \qquad (25)$$

$$= \frac{z^{-1} + \dfrac{1}{2}(z^{-1}-1) + \dfrac{3}{4}(z^{-1}-1)^2 + \dfrac{1}{8}(z^{-1}-1)^3}{1 - \dfrac{13}{2}(z^{-1}-1) - \dfrac{-99}{4}(z^{-1}-1)^2 - \dfrac{399}{8}(z^{-1}-1)^3} \qquad (26)$$

where $z = \exp(sT)$, the center frequency f_0 is 60 Hz, and the sampling period T is $1/1508$ s. Using the design
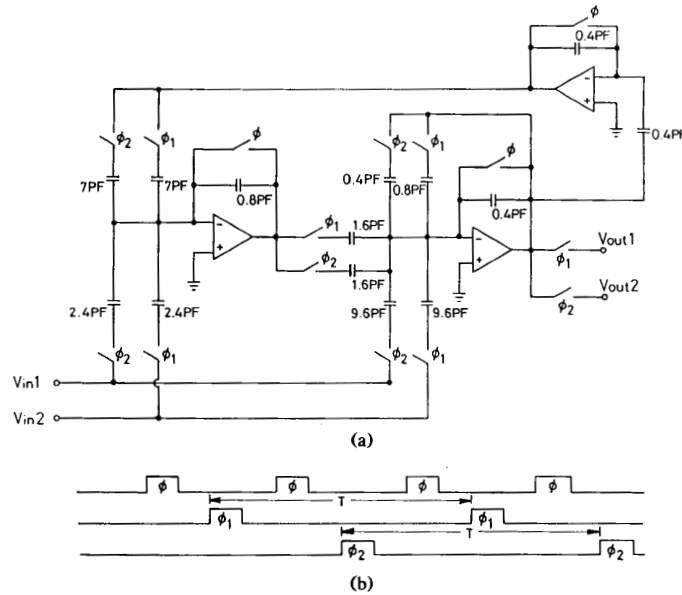
Fig. 12.   (a) Circuit diagrams and (b) clock waveforms of two multiplexed SC-differentiator-based IIR filters.

algorithm in Section III-A, (25) can be realized. The resultant SC low-pass filter (LPF) prototype is shown in Fig. 16(a) and its component spread can be minimized through an adequate weight. The forward element G and the clock waveforms are shown in Fig. 16(b) and (c). The SWITCAP simulation results are shown in Fig. 16(d).

Now, changing the forward element G and the clock waveforms to those shown in Fig. 16(e) and (f), respectively, the resultant transfer function of this basic-type N-path circuit ($N = 3$) becomes

$$H(z)$$

$$= \frac{1 + \frac{3}{2}\left(z_a^{-3} - 1\right) + \frac{3}{4}\left(z_a^{-3} - 1\right)^2 + \frac{1}{8}\left(z_a^{-3} - 1\right)^3}{1 - \frac{13}{2}\left(z_a^{-3} - 1\right) - \frac{-99}{4}\left(z_a^{-3} - 1\right)^2 - \frac{399}{8}\left(z_a^{-3} - 1\right)^3}$$

$$(27)$$

where

$$z_a = \exp\left(s\frac{T}{3}\right) = z^{1/3}.$$

In this three-path bandpass filter, the center frequency of the bandpass filter becomes 1508 Hz, and the passband is in the range of 1508 ± 60 Hz as shown in Fig. 16(g). Note that the center frequency of the bandpass filter response is just the sampling frequency of each LPF and the bandwidth of this N-path circuit is 120 Hz. The loss at the passband edge is due to the sample-and-hold effect, which is about -1.68 dB.

If the basic-type N-path SC differentiator circuits are used to build an N-path circuit like that of Fig. 14(a), the inevitable mismatches among the forward capacitors
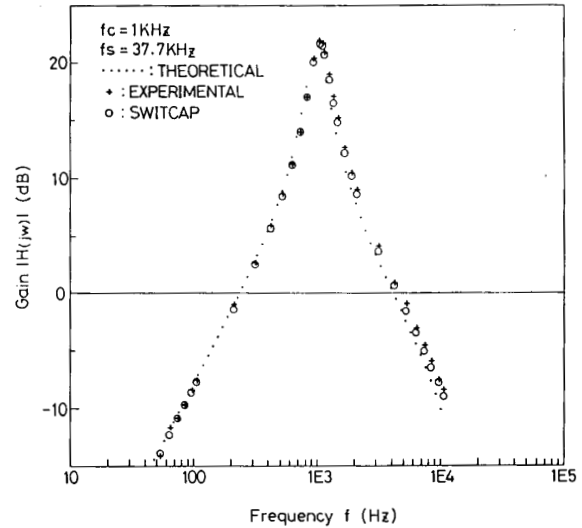

Fig. 13.   The frequency responses of the IIR filter shown in Fig. 12.

($C1$'s) and the multiplexing switches are sufficient to introduce a noise at the center of passband [9]. To solve this problem, the uniformity among signal paths must be enforced. This can be done by using a single forward capacitor $C1$ for all the signal paths. Meanwhile the signal charges are stored on the added extra capacitors when they are not processed in the circuit. Thus a RAM-type [9] N-path differentiator circuit can be formed as shown in Fig. 17(a) where C is the common feedback capacitor shared by all paths, and C_{si} is the storage capacitor used for the path i. The timing diagram is
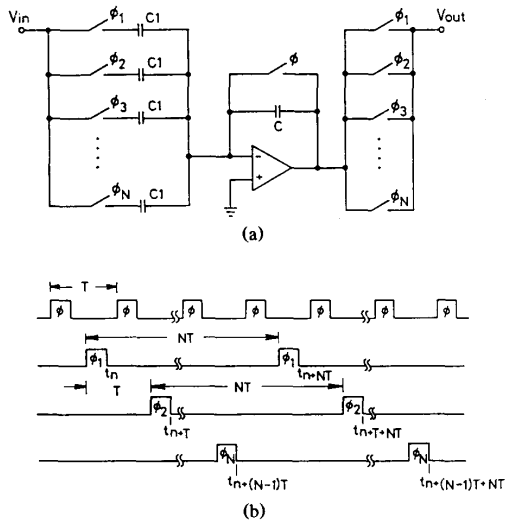
Fig. 14. (a) The circuit diagram and (b) its clock waveforms of a basic-type SC-differentiator-based N-path circuit.
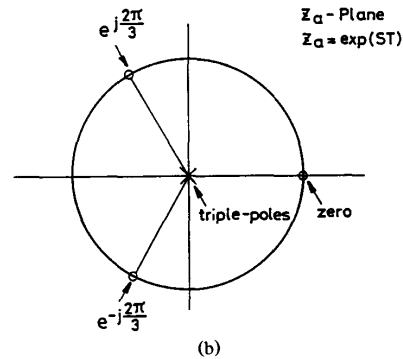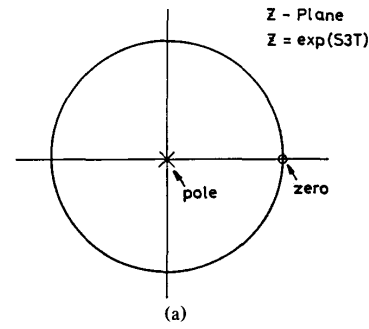

Fig. 15. (a) Pole and zero locations of the SC differentiator in Fig. 1(a). (b) Pole and zero locations of the multiplexed SC differentiator in Fig. 14(a) with $N = 3$.

shown in Fig. 17(b). The operations of this RAM-type N-path circuit are described below.

During the period of the clock ϕ_4 (and the clock ϕ_2), the charge $C1V_{in}(t_{n-T})$ on the capacitor $C1$ is transferred into C_{s1} and the charge on the feedback capacitor C is discharged to zero. The charge on C_{s1} remains unchanged until the clock ϕ_3 (and the clock ϕ_1) is activated after a full cycle. Then the charge $C1V_{in}(t_{n-T})$ of C_{s1} is transferred back into C. Since $C1$ is connected to V_{in} at the same time, the charge $C1V_{in}(t_n)$ on $C1$ also appears on C through induction. Thus the net change of charge on C is $-C1[V_{in}(t_n) - V_{in}(t_{n-T})]$ at the end of the clock ϕ_3 (and the clock ϕ_1). The same operation is performed during the other clock periods (ϕ_5, ϕ_6) and (ϕ_7, ϕ_8). Thus the overall transfer function is given by

$$H(z_a) = \frac{V_{out}(z_a)}{V_{in}(z_a)} = -\frac{C1}{C}(1 - z_a^{-3}) \qquad (28)$$

where

$$z_a = \exp\left(s\frac{T}{3}\right) = z^{1/3}.$$

A delay element can be implemented by using this RAM-type N-path circuit. The circuit is shown in Fig. 17(c) and the timing diagram is the same as that in Fig. 17(a). The overall transfer function of this delay element can be expressed as

$$H(z_a) = \frac{V_{out}(z_a)}{V_{in}(z_a)} = -\frac{C2}{C}z_a^{-3} \qquad (29)$$

where

$$z_a = \exp\left(s\frac{T}{3}\right) = z^{1/3}.$$

As an illustrating example, (26) is implemented by using the RAM-type N-path circuit. First the transfer function in (26) is rewritten as

$H(z_a)$

$$= \frac{z_a^{-3} + \frac{1}{2}\left(z_a^{-3} - 1\right) + \frac{3}{4}\left(z_a^{-3} - 1\right)^2 + \frac{1}{8}\left(z_a^{-3} - 1\right)^3}{1 - \frac{13}{2}\left(z_a^{-3} - 1\right) - \frac{-99}{4}\left(z_a^{-3} - 1\right)^2 - \frac{399}{8}\left(z_a^{-3} - 1\right)^3}$$

$$(30)$$

where

$$z_a = \exp(sT).$$

In (30), the block of $z_a^{-3} - 1$ can be implemented by the circuit of Fig. 17(a) and the block of z_a^{-3} by the delay element of Fig. 17(c). The resultant RAM-type N-path circuit is shown in Fig. 18, where the clocks are all indicated beside the switches without the parentheses. The feedback branch F and the timing diagram can be found from Fig. 17(a) and (b), respectively. Note that this RAM-type N-path circuit uses fewer op amps than the basic N-path structure of Fig. 16(a). Moreover, as mentioned earlier, this N-path circuit is less susceptible to noise at the center frequency as compared to the N-path circuit of Fig. 16(a). The simulation results are shown in Fig. 16(g) also. It can be seen that the response is very consistent with the basic-type N-path circuit of Fig. 16(a).
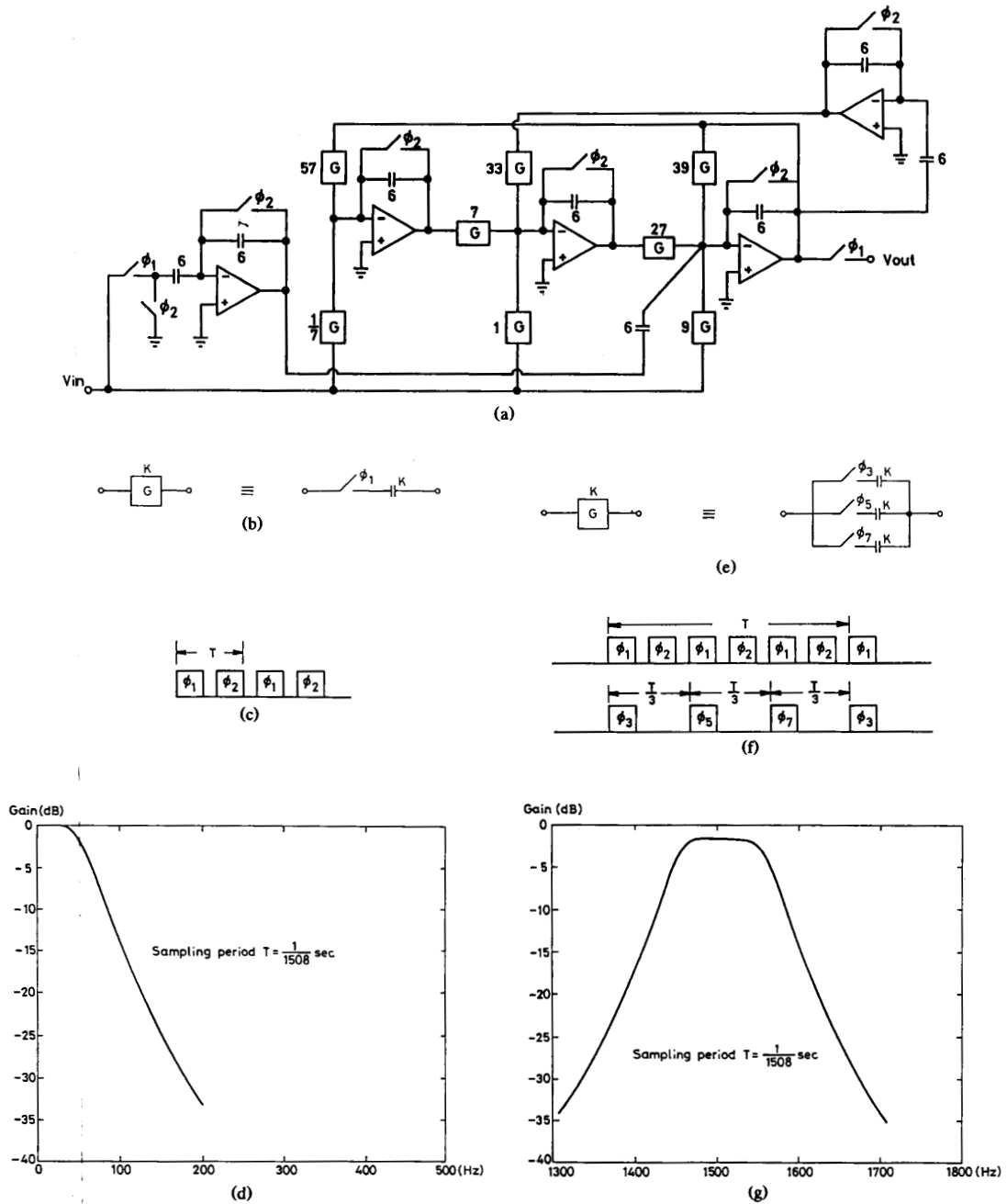
(a)

(b)

(e)

(c)

(f)

(d)

(g)

Fig. 16.   The basic-type N-path filter with $N = 3$. (a) The circuit prototype of both low-pass filter and N-path filter. (b) The forward element of the LPF used in (a). (c) The timing diagram of the LPF circuits in (a) and (b). (d) The frequency response of the LPF circuit in (a) and (b). (e) The forward elements of the three-path filter used in (a). (f) The timing diagram of the three-path filter. (g) The merged frequency response of the three-path filters shown in Figs. 16(a) and 18.
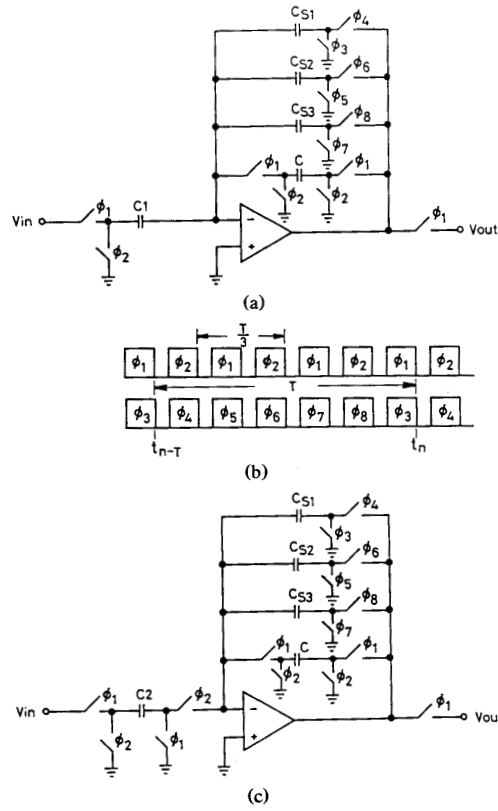
Fig. 17. RAM-type *N*-path differentiator circuit and delay circuit with *N* = 3. (a) The *N*-path differentiator circuit diagram. (b) The timing diagrams of both circuits in (a) and (c). (c) The *N*-path delay circuit diagram.
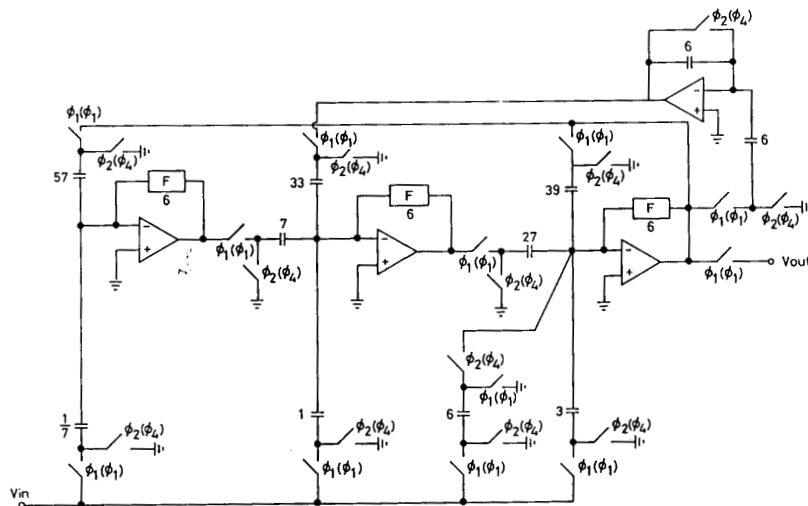

Fig. 18. An improved SC *N*-path filter with *N* = 3 where the feedback branches and the timing diagrams are given in Fig. 17 or 19 and the realized transfer function of (30).
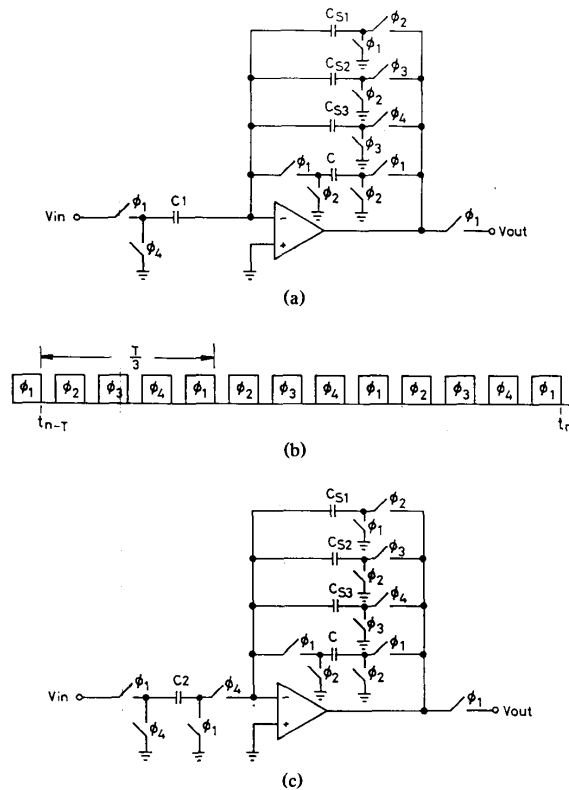
(a)

(b)

(c)

Fig. 19. Circulating-delay N-path differentiator circuit and delay circuit with $N = 3$. (a) The N-path differentiator circuit diagram. (b) The timing diagrams of both circuits in (a) and (c). (c) The N-path delay circuit diagram.

Based on the similar principle in circulating-delay N-path SC integrators [9], a circulating-delay N-path SC differentiator can also be constructed as shown in Fig. 19(a) for $N = 3$. Its timing diagram is shown in Fig. 19(b). The operation is described in the following. When the clock ϕ_1 is on, the stored charge $C1V_{in}(t_{n-T})$ of C_{s1} is transferred into the feedback capacitor C. Meanwhile the charge $C1V_{in}(t_n)$ on $C1$ appears on C through induction. Thus the net charge on C is $-C1[V_{in}(t_n) - V_{in}(t_{n-T})]$ at the end of the clock ϕ_1. When the clock ϕ_2 is on, the charge on C_{s2} is transferred to C_{s1} and the voltage on the feedback capacitor C is discharged to zero. During the period $\phi_3 = 1$, the charge on C_{s3} is transferred to C_{s2}. During the period $\phi_4 = 1$, the charge $C1V_{in}(t_n)$ on $C1$ is transferred to C_{s3}. When $\phi_1 = 1$ again, the above cycle is then repeated. Clearly, it requires $N(N + 1) = 12$ clock phases to perform a full cycle of operation.

From the above description, it is evident that the circuit of Fig. 19(a) has the same transfer function as that of Fig. 17(a), and each stored charged packet is in the memory for a T period. Hence the overall transfer function of the SC differentiator of Fig. 19(a) is the same as (28). A delay element of the circulating-delay N-path circuit is also shown in Fig. 19(c), and the transfer function is given by

(29). Using the circuiting-delay N-path circuit to implement (30), the resultant circuit structure is the same as that of Fig. 18 except that the clocks are those shown in the parentheses beside the switches and the feedback branches F, and the timing diagrams are shown in Fig. 19(a) and (b), respectively. The simulation results are shown in Fig. 16(g), where the responses are exactly consistent with those of the basic-type and the RAM-type N-path circuits.

It should be noted that various designs of low-pass SC prototype filters can also be applied in the synthesis of basic-type, RAM-type, or circulating-delay-type N-path filters. Generally, the RAM-type or the circulating-delay-type N-path filter has less noise effects at the center frequency of passband than the basic-type N-path filter. The voltage gain of the op amps in the RAM-type circuit can be lowered by a factor of four [9] over that in the circulating-type circuit. But the RAM-type circuit needs eight clock signals, twice as many as the circulating-delay type circuit.

Both SC differentiator- and SC integrator-based N-path filters have several common problems, such as the clock feedthrough effect, the open-loop mode of the op amps, and the noises generated from switches and op amps. These problems must be considered in practical design and are worth a deeper analysis. Because all N-path filters generate mirror frequency noise [9] by reflecting the low-frequency noise to the sampling frequency and the basic SC-differentiator-based low-pass prototype filter has a low noise in the low-frequency range, the resultant N-path circuit is expected to have a low mirror frequency noise. From this point of view, they are superior to the conventional SC-integrator-based N-path circuits.

V. CONCLUSION

A novel design methodology has been successfully developed for the realization of IIR filters, FIR filters, multiplexed filter banks, and N-path filters using SC differentiators. All the realized circuits have been verified through SWITCAP simulations. Part of them were fabricated in analog CMOS process and the measured results have shown a good consistency with the simulation results.

The IIR and FIR filters as well as the multiplexed filter banks use the SC differentiators directly without modifications. As compared to the conventional SC-integrator-based design, the proposed IIR filters have a lower component sensitivity and are free from the dc instability problems whereas the proposed N-path filters have a better noise performance. For the analog FIR filters that cannot be realized directly by using SC integrators, they have a simpler and more compact structure with a better performance as compared to other analog FIR filters. Except for these distinct features, all the proposed filter circuits retain other advantageous performance of SC differentiators as well, such as stray insensitive structures, low sensitivity to offset voltage and power supply variations, maximum output swing, and low noise in the low-

frequency range. In conclusion, the inherent good performance and the compact structure of the realized filter circuits using SC differentiators make their applications in signal processing quite promising and feasible.

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Tsai-Chung Yu, photograph and biography not available at time of publication.

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Chung-Yu Wu (S'76–M'88), photograph and biography not available at time of publication.

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Shin-Chi Chang, photograph and biography not available at time of publication.