Two-Dimensional Simulation of Orientation Effects in Self-Aligned GaAs MESFET's

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Abstract—**The stress-induced orientation effects in self-aligned GaAs MESFET's have been studied using a two-dimensional analysis. Devices oriented along different crystal directions, with different gate lengths, and under different stress conditions were studied. It was found that the piezoelectric effect caused by the surface stress plays a very important role in the device characteristics of short-channel self-aligned MESFET's. Structure parameters such as lateral spreading of N^+ ions and p-type impurity concentration in the substrate were found to have great influence on the short-channel effect as well as the orientation effect. The short-channel effects can be suppressed and the device performance improved if the devices are oriented in the right direction and the structure of the devices and the thickness of the surface dielectric layer are properly chosen.**

NOMENCLATURE

a_0	Distance between the edge of N^+ implant to the center of the gate.
D_n	Electron diffusion coefficient.
d_f	Dielectric film thickness.
d_{14}	$= 2.69 \times 10^{-17}$ C/dyn.
E_c	Energy of the bottom of conduction band.
E_0	Critical field.
E_t	Energy level of the deep donor "EL-2."
I_{ds}	Drain-source current.
J_n	Electron current density.
k	Boltzmann's constant.
L_g	Gate length.
L_{gd}	Distance between the gate and the drain.
L_{gn^+}	Distance between the gate and the N^+ region.
L_{sg}	Distance between the source and the gate.
N_a	Acceptor concentration.
N_c	Effective density of states of conduction band.
N_d	Donor concentration.
N_{pz}	Piezoelectric charge density.
N_p	Peak density of implanted profile.
N_t	Deep-donor EL-2 density.
N_t^+	Ionized deep-donor EL-2 density.
n	Electron density.
q	Electron charge.
R_p	Projected range.
R_t	Lateral straggle parameter.
T	Absolute temperature.
V_{ds}	Drain-source voltage.
V_{gs}	Gate-source voltage.
V_t	Threshold voltage.
v_{ns}	Electron saturation velocity.
Ψ	Electrostatic potential.
ϵ	Dielectric permittivity.
γ_b	= 390 electrons/dyn.
σ_f	Stress induced by the dielectric overlayer.
β	= 0.59.
μ_{n0}	Low-field electron mobility.
μ_n	Electron mobility.
ΔR_p	Straggle parameter.

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I. INTRODUCTION

IT HAS BEEN known for some time that the electrical characteristics of GaAs MESFET's depend on the orientation of the gate with respect to the substrate [1]. The threshold voltage, the drain current, and even the device uniformity depend on the gate orientation. The threshold voltage shift at small gate lengths, commonly known as the short-channel effect, is also orientation-dependent. These interesting phenomena, which do not exist for Si FET's, are due to the nature of the zinc-blende crystal structure of GaAs. Because this orientation effect has a large impact on device performance and circuit yield, a lot of work have been done in trying to understand and control this effect [2]–[7]. Initially, it was attributed to an anisotropic stress-enhanced lateral diffusion of N^+ impurities from the source and the drain regions into the channel [2]–[4]. In 1984, Asbeck *et al.* proposed a different explanation which attributed the orientation dependence to the surface stress induced piezoelectric effect [8]. They found that the stress caused by the dielectric overlayer on GaAs MESFET's produces a considerable amount of piezoelectric polarization charges that can effectively vary the doping profile in the FET's channel and therefore shift the threshold voltage and the drain current. This explanation has since been verified experimentally by several authors [6], [7].

In the past the influence of the stress on the FET characteristics was studied mostly with one-dimensional analysis. The threshold voltage shift caused by the piezoelectric effect was estimated by integrating the contributions of the piezoelectric charges in the FET's channel under the midpoint of the gate [8]–[10]. However, the strain field, the piezoelectric charge distributions, as well as the carrier transport in the channel of the FET are two-di-

mensional problems. This is especially true for self-aligned MESFET's and short-gate devices, in which the stress is strong and the short-channel problem is severe. So, for a better understanding of the influence of the stress on FET characteristics, a full two-dimensional analysis is needed. Onodera *et al.* have implemented the Asbeck's piezoelectric model into a two-dimensional simulator for GaAs MESFET to study the orientation effect in GaAs MESFET's and their results were in fair agreement with experimental results [11].

In self-aligned GaAs MESFET's, especially those with short gates, the device characteristics depend very much on the device structure and substrate properties. In order to obtain a clear understanding of the short-channel behavior of these devices, one has to take all the structure parameters as well as the piezoelectric effect into consideration. In self-aligned MESFET's, one of the most important structure parameters is the amount of lateral spreading of N^+ implant into the n channel. This amount, however, depends on the self-aligned structure used. The refractory metal gate structure normally has the N^+ implant right next to the gate and therefore has a stronger lateral spreading than the structures with a spacing between the N^+ implant and the gate. Chen *et al.* have studied the effect of N^+ lateral spreading and the piezoelectric effect using a one-dimensional method [9]. The two-dimensional behavior of the N^+ carrier distribution, however, was not considered. Other important factors influencing the characteristics of the FET's are the amount of EL-2's and the residual shallow acceptor concentration in the semi-insulating substrate. Horio *et al.* have numerically calculated these effects on the characteristics of the FET's [12]. But, piezoelectric effect was not considered in their calculation.

In this paper, we report results from a two-dimensional simulation of self-aligned GaAs MESFET's. The impacts on the device performance due to the piezoelectric effect and the structure and material parameters have all been taken into consideration. Device parameters such as lateral spreading of N^+ ions and residual carbon concentration in the substrate have been taken into account to study the correlation between the short-channel effect and the piezoelectric effect. Devices with different gate lengths, different dielectric thickness, and oriented in different directions were also studied.

II. Device Structure and Physical Model

A. Device Structure and Implantation Profile

A cross-sectional view of the device of the self-aligned MESFET structure used in this study is shown in Fig. 1. This is one of the most popular self-aligned structures used today. The N^+ region next to the gate is implanted in a self-aligned fashion using either the gate metal [6], [7] or the dummy gate [13] as the implantation mask. A 0.1-μm spacing is left between the N^+ region and the gate to resemble some of the more advanced structures for reduced gate capacitance, gate leakage, and short-channel effects

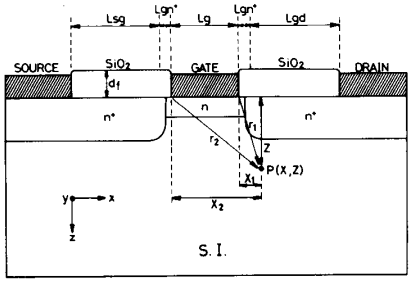


Fig. 1. One of the self-aligned MESFET structure used in the study.

[14]. To compare devices with different lateral spreading of N^+ ions, we have also simulated devices without N^+-gate spacing. Structure parameters of the MESFET used in the calculation are listed in Table I. Different implantation profiles were chosen for the n channel and the N^+ region. In the vertical direction, they are represented by the Gaussian function

$$N(z) = N_p \cdot \exp\left[-\frac{(z - R_p)^2}{2\Delta R_p^2}\right]. \tag{1}$$

The projected range, R_p, is 600 Å for the n channel and 1000 Å for the N^+ region. Two straggle parameters [15] are used for each Gaussian profile. For $z \le R_p$, ΔR_p is 5 μm. For $z \ge R_p$, ΔR_p is 450 Å for the n channel and 700 Å for the N^+ region. The peak concentration, N_p for the channel is 1×10^{17} cm^{-3} and 4×10^{17} cm^{-3} for the N^+ region. The lateral spreading of N^+ ions beyond the edge of the implantation mask has also been considered. This is very important for the self-aligned structure considered here because it can change the source resistance and cause short-channel effect. The expression for the lateral distribution of implanted ions has been derived by Furukawa *et al.* [16]. Following their derivation, the contribution of the lateral distribution of implanted ions to the channel doping is described by

$$N(x, z) = \frac{N(z)}{2}\left[\operatorname{erfc}\left(\frac{a_0 - x}{\sqrt{2}\Delta R_t}\right) + \operatorname{erfc}\left(\frac{a_0 + x}{\sqrt{2}\Delta R_t}\right)\right] \tag{2}$$

where $N(z)$ is the Gaussian profile discussed before. The x dependent terms are the complementary error functions, describing the lateral spreading. a_0 is the distance between the edge of N^+ implant to the center of the gate, i.e., $a_0 = L_{gn}^+ + 1/2\ L_g$. The doping profiles for the n channel and the N^+ region are shown in Fig. 2(a) and the lateral spreading with $\Delta R_t = 350$ Å are shown in Fig. 2(b). The devices are assumed to be fabricated on (1 0 0) substrates. Their orientation relative to the substrates are shown in Fig. 3. The surface dielectric layer on the device (see Fig. 1) is used either as an annealing cap or as a passivation layer. Depending on the dielectric material and the process technique, the dielectric film may be under significant stress. Because the film is not continuous and because the stress in the gate metal is usually negli-

TABLE I
STRUCTURE PARAMETERS

Parameter	Value
L_g	0.5, 0.75, 1, 2, 3, 4 and 5 μm
L_{sg}	0.75 μm
L_{gd}	0.75 μm
L_{gn^+}	0.1 μm or 0 μm
d_f	600 nm or 1200 nm
N_a	1×10^{15} cm^{-3}, 2×10^{15} cm^{-3} or 3×10^{15} cm^{-3}
Ion implantation for N channel	
N_{peak}	1×10^{17} cm^{-3}
R_p	0.06 μm
ΔR_{p1}	5 μm
ΔR_{p2}	0.045 μm
Ion implantation for N^+ layer	
N_p	4×10^{17} cm^{-3}
R_p	0.10 μm
ΔR_{p1}	5 μm
ΔR_{p2}	0.07 μm
ΔR_t	350 Å or 700 Å

gible [8], the strain field and the induced piezoelectric charge distribution in the channel of the FET is not uniform and is greatly intensified along the edges of the gate. Following the derivation of Kirby *et al.* [17] and Asbeck *et al.* [8], we can express the piezoelectric charge density in the channel as (see Fig. 1 for coordinate system)

$$N_{pz} = \gamma_b \sigma_f d_f \left(\frac{x_1 z(x_1^2 - \beta z^2)}{r_1^6} - \frac{x_2 z(x_2^2 - \beta z^2)}{r_2^6} \right) \quad (3)$$

where

$\gamma_b = 2d_{14}(4 - \nu)/\pi = 390$ electrons/dyn
$\nu = 0.23$, Poisson ratio of GaAs
$d_{14} = 2.69 \times 10^{-17}$ C/dyn, the orientation-dependent strain constant, which is positive for [0 1 1] FET's and negative for [0 1 $\bar{1}$] FET's
d_f dielectric thickness
$\beta = (2 + \nu)/(4 - \nu) = 0.59$
σ_f stress in the dielectric film.

These piezoelectric charges can be considered as additional dopants for the FET's channel. Since d_{14} is orientation-dependent, the characteristics of the FET depend on the gate orientation. In this study, the surface dielectric layer is assumed to be SiO_2, which is under compressive stress on GaAs. The magnitude of the stress depends on the techniques of deposition. Here we assume the value being 1×10^9 dyne/cm^{-2} [6].

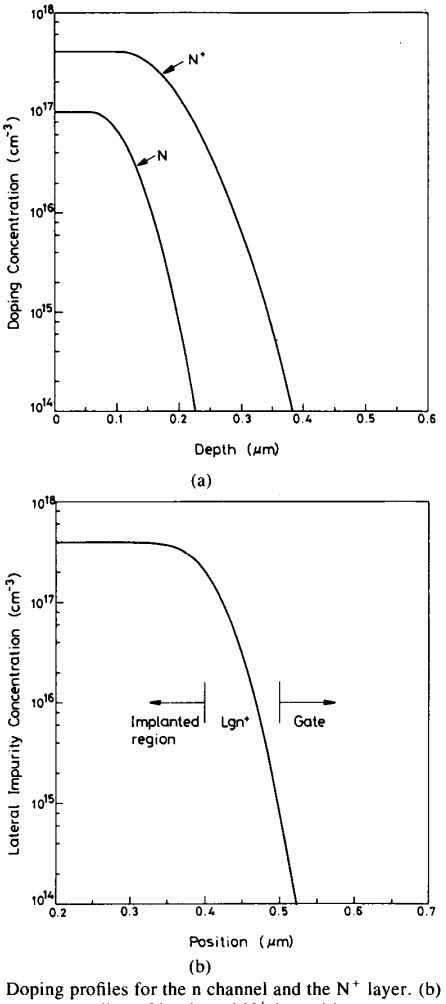


Fig. 2. (a) Doping profiles for the n channel and the N^+ layer. (b) Lateral spreading of implanted N^+ impurities.

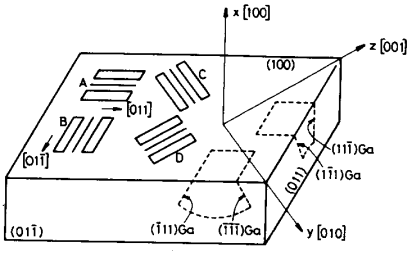


Fig. 3. Schematic drawing of the orientations of the FET's with respect to the GaAs substrate. *A* in the (0 1 1) direction, *B* in the (0 1 $\bar{1}$) direction, *C* in the (0 1 0) direction, and *D* in the (0 0 1) direction.

The deep levels in semi-insulating substrates are also considered in our simulation. In LEC (*L*iquid *E*ncapsulated *C*zochralski) grown GaAs, it is well known that EL-2's, the mid-gap donor states, compensate shallow carbon acceptors to cause the semi-insulating properties. We assume the concentrations for the EL-2 being 1×10^{16} cm^{-3} and carbon being 1×10^{15} cm^{-3}, 2×10^{15}

cm^{-3}, or 3×10^{15} cm^{-3}. These are typical values for commercially available undoped LEC substrates [18].

In the simulated devices, the gate is symmetrically placed between the source and the drain contacts. The spacing between the gate and the source is 0.75 μm. The gate length is varied from 0.5 to 5 μm.

B. Basic Equations and 2-D Simulation

The basic equations used in our calculation are as follows:

1) Poisson's equation

$$\nabla^2 \Psi = -\frac{q}{\epsilon}(-n + N_d - N_a + N_t^+ + N_{pz}) \quad (4)$$

where N_{pz} is the piezoelectric charge density shown in (3) and N_t^+ is the ionized EL-2 concentration. From the relations

$$n = N_c \exp\left[-(E_c - E_f)/kT\right] \quad (5)$$

$$N_t^+ = N_t \cdot \left[1 - \frac{1}{1 + \exp\left[(E_t - E_f)/kT\right]}\right] \quad (6)$$

N_t^+ can be expressed as

$$N_t^+ = \frac{N_c \cdot \exp\left[-(E_c - E_t)/kT\right]}{n + N_c \exp\left[-(E_c - E_t)/kT\right]} \cdot N_t \quad (7)$$

where the EL-2 level, E_t, is taken to be 0.69 eV below the conduction band [12].

2) Current continuity equation

$$\nabla \cdot \vec{J}_n = 0. \quad (8)$$

The hole current is neglected.

3) Drift and diffusion equation

$$\vec{J}_n = -q\mu_n n \nabla \psi + qD_n \nabla n. \quad (9)$$

The field-dependent mobility is given as [19]

$$\mu_n = \frac{\mu_{n0} + (v_{ns}/E)(E/E_0)^4}{1 + (E/E_0)^4} \quad (10)$$

where the critical field $E_0 = 4300$ V/cm, the saturation velocity $v_{ns} = 0.8 \times 10^7$ cm/s, and the low-field mobility $\mu_{n0} = 6000$ $cm^2/V \cdot s$.

The equations described above were discretized by finite difference method. The spacings between mesh points were varied with the highest mesh density under the gate near the drain end to ensure enough spatial resolution and calculation accuracy. The lower boundary of the devices simulated was set at 3 μm below surface to make sure that all physical phenomena studied occur well within this boundary. The Gummel scheme was adopted to solve the discretized equations [20]. The convergence criteria in our calculation are that the relative changes in the magnitude of terminal currents are less than 10^{-4}.

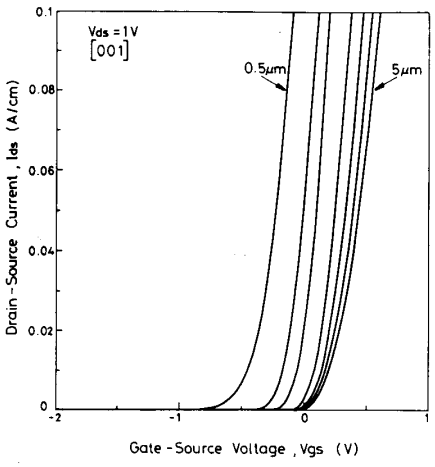
III. Results and Discussions

A. Orientational-Dependent Short-Channel Effects

For short-gate MESFET's, short-channel effects are very important in determining the device characteristics and eventually set the ultimate limit for the smallest dimension that can be used for usable devices. This is especially true for self-aligned structures where the proximity of N^+-implanted regions further enhances the short-channel effects. The piezoelectric effect is also stronger for short-channel devices because the piezoelectric charge density, as indicated in (3), is higher when the gate is smaller.

According to (3), the piezoelectric charges have opposite polarities for FET's oriented along [0 1 1] and [0 1 $\bar{1}$] directions. The threshold voltage shifts caused by the piezoelectric effects, therefore, should be in opposite directions for the FET's in these two orientations. The amount of shift has been calculated using a simple one-dimensional analysis [8]. However, experimentally, the phenomenon discussed here is usually not observed. The threshold voltage of the FET's in one of the directions does not suffer as much shift than that of the FET's in the other direction [1]–[3]. For devices with very short gates (≤ 1 μm), the threshold voltage shift can be even in the same direction. This, of course, cannot be explained by the piezoelectric effect alone. One has to consider the short-channel effects, which are independent of gate orientation, and the piezoelectric effect together in order to satisfactorily explain the observed phenomena.

Before we discuss the influence of piezoelectric effect on the short-channel effect, it is worthwhile to look at the short-channel effect by itself. This actually is the case for devices oriented along [0 0 1] direction on (1 0 0) substrates. Because of crystal symmetry, the piezoelectric charges vanish in this orientation. I–V characteristics were calculated for devices with $L_g = 0.5$, 0.75, 1, 2, 3, 4, and 5 μm. The N^+-gate spacing, L_{gn}^+, the lateral spreading, ΔR_t, and the carbon concentration, N_a, used in the calculation are 0.1 μm, 350 Å, and 1×10^{15} cm^{-3}, respectively. Fig. 4(a) shows the calculated I_{ds} versus V_{gs} curves at $V_{ds} = 1$ V for different L_g's. (The gate width is assumed to be 10 μm.) Short-channel effects can be clearly seen in these figures. For the FET's with gate lengths longer than 2 μm, the threshold voltage is nearly constant. But when the gate length is smaller than 2 μm, the threshold voltage shifts toward negative values as the gate length is reduced. For devices oriented along [0 1 1] and [0 1 $\bar{1}$] directions, because of piezoelectric effect, the results are very different. If the dielectric overlayer thickness is 1200 nm, the calculated I_{ds} versus V_{gs} curves are shown in Fig. 4(b) and (c) for [0 1 1] and [0 1 $\bar{1}$] FET's, respectively. In the [0 1 1] direction, the short-channel effects are greatly enhanced. There is a wider spread in threshold voltage between devices with different gate length. In the [0 1 $\bar{1}$] direction, however, the threshold voltages of different devices have nearly the same value. In other words, the short-channel effects seem to be compensated by the piezoelectric effect.



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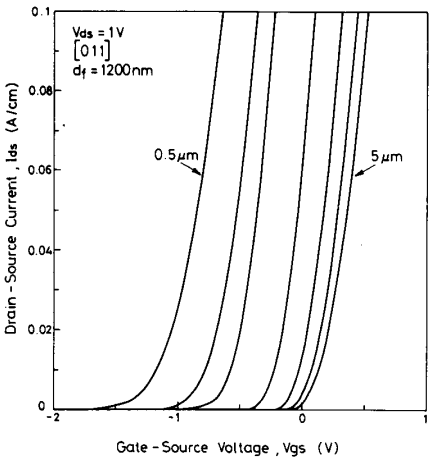

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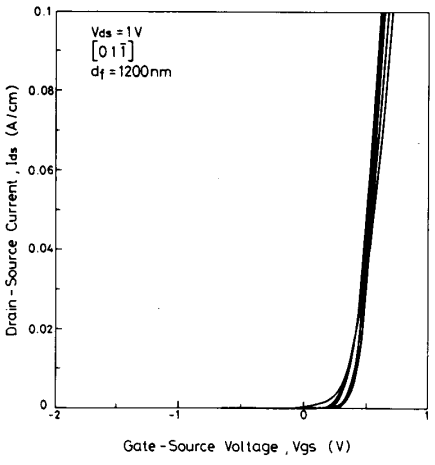


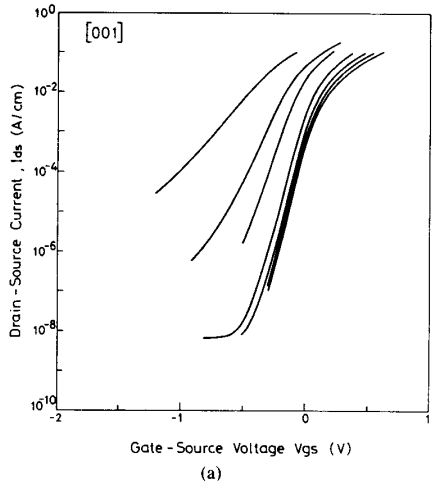
(c)

Fig. 4. The drain-source current I_{ds} versus gate-source voltage V_{gs}. Curves for (a) [0 0 1]-oriented MESFET's, (b) [0 1 1]-oriented MESFET's, (c) [0 1 $\bar{1}$]-oriented MESFET's at V_{ds} = 1 V. The gate lengths are 0.5, 0.75, 1, 2, 3, 4, and 5 μm.

The subthreshold behavior of FET's is also greatly influenced by the short-channel effects. When the gate length shrinks down to the submicrometer regime, the subthreshold leakage often causes poor cutoff characteristics. The calculated subthreshold currents versus gate voltage for devices with the same structures of those used in Fig. 4 are shown in Fig. 5. Fig. 5(a) is for [0 0 1] oriented devices while Fig. 5(b) and (c) presents [0 1 1] and [0 1 $\bar{1}$] oriented devices, respectively. In the [0 0 1] direction, in which the devices are immune from the piezoelectric effect, one can see clearly as the gate length becomes smaller, not only the threshold voltage shifts, the subthreshold conduction also becomes worse. In the [0 1 1] direction, the effect is much worse. The slope of the subthreshold conduction curves (log (I_{ds}) versus V_{gs}) degrade badly at small gate lengths. The best subthreshold behavior is observed for devices oriented in the [0 1 $\bar{1}$] direction. The slopes remain the same except for the FET with 0.5-μm gate length. The improvement in subthreshold conduction for the [0 1 $\bar{1}$] FET's caused by piezoelectric effect has been observed experimentally and agrees well with our calculated results [7].

The orientation-dependent FET behavior can be best illustrated by the two-dimensional contour plots of the potential distribution and the carrier density distribution shown in Figs. 6–8. In these figures the contour plots of self-aligned MESFET's with a 1-μm gate length and a 1200-nm-thick SiO_2 overlayer oriented in [0 1 $\bar{1}$], [0 0 1], and [0 1 1] directions are shown. The devices are biased with V_{ds} = 1 V and V_{gs} = −0.6 V. Based on Fig. 4, we know, under this bias condition, the [0 1 $\bar{1}$] FET and the [0 0 1] FET are below threshold and the [0 1 1] FET is above threshold. From Fig. 6(a) and (b), it can be seen that in the [0 1 $\bar{1}$] FET there is a wide potential barrier in the substrate between the source and the drain and the channel is totally cut off (see Fig. 6(a)). For the [0 0 1] FET, where there is no piezoelectric effect, Fig. 7(a) shows that the width of the potential barrier is narrower and there is some subthreshold current in this case. The carrier density distribution in Fig. 7(b) shows that the current path is deep into the substrate. For the [0 1 1] FET the situation is totally different from those of the other two FET's. Fig. 8(a) shows there is no potential barrier existing between the source and the drain in the substrate. The channel is open and there is plenty of current flowing between the source and the drain contacts. The carrier density distribution shown in Fig. 8(b) indicates again there is a current leakage path in the substrate. Comparing Figs. 6(b), 7(b), and 8(b), we can clearly see the effect of piezoelectric charges on the current conduction in the FET's. In the [0 1 $\bar{1}$] FET the carriers are depleted in the region under the gate, while in the [0 1 1] FET the carrier density increases due to the piezoelectric charges. From Fig. 8(b), one can see that the piezoelectric charge distribution is very deep.

Subthreshold conduction and short-channel effects are closely related problems for the FET devices. When the channel length is small, because of the proximity of the



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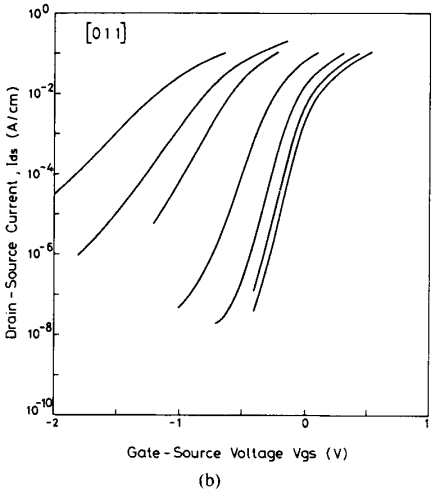

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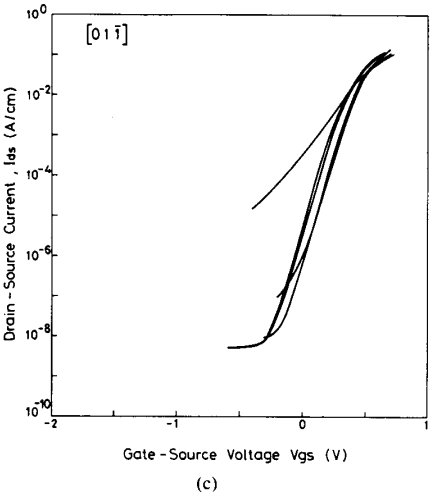
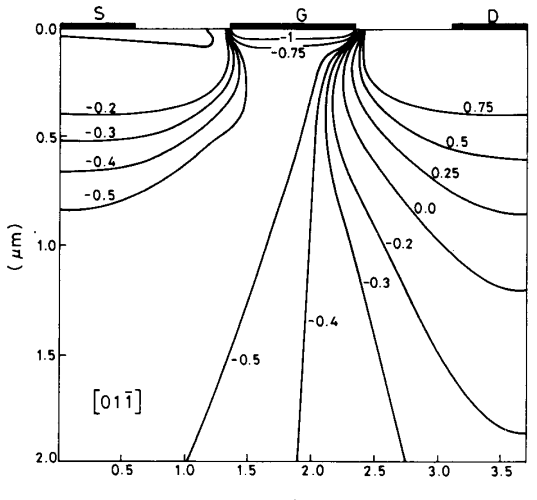
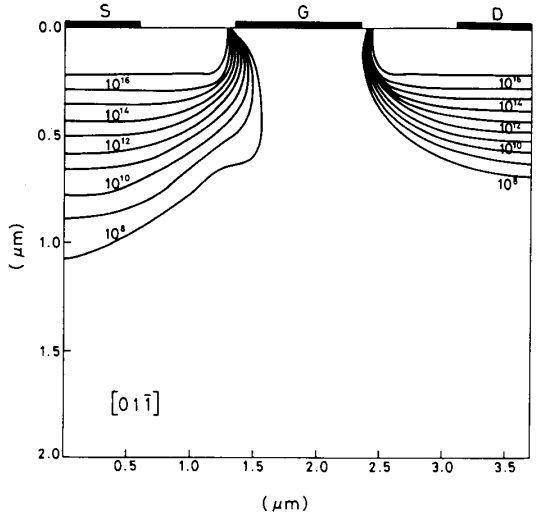


(c)

Fig. 5. Subthreshold conduction behavior (I_{ds} versus V_{gs} curves shown in logarithm scale) for (a) [0 0 1]-oriented, (b) [0 1 1]-oriented, and (c) [0 1 $\bar{1}$]-oriented devices with various gate lengths. Devices and the biased conditions are the same as those described in Fig. 4.



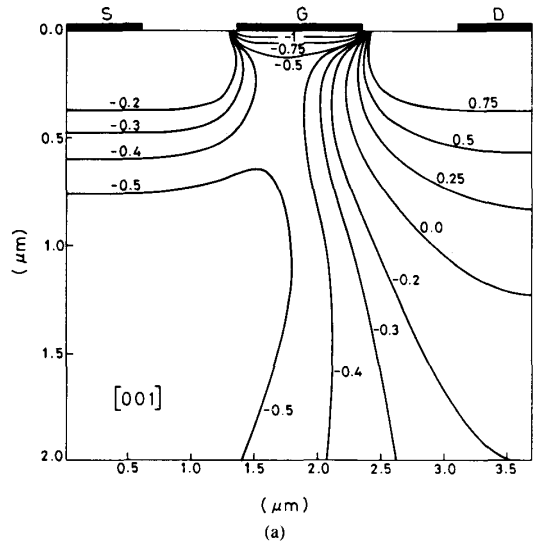
(a)



(b)

Fig. 6. Two-dimensional contour plots of (a) the potential distribution and (b) the carrier distribution for [0 1 $\bar{1}$]-oriented FET's. The FET's have 1-μm gate and 1200-nm SiO_2 overlayer. The sources are grounded; the drain voltage is V and the gate voltage is -0.6 V.

source and drain regions, the potential along the channel of the FET varies with the channel length and the drain voltage. In the subthreshold regime, increasing drain voltage and/or decreasing channel length will lower the potential barrier between the source and the drain and therefore increase the subthreshold current and decrease the threshold voltage. Fig. 9(a) and (b) presents the calculated potential distribution along the potential valley under the gate of the 0.5-, 0.75-, and 1-μm gate MESFET's in the [0 0 1] and [0 1 $\bar{1}$] directions, respectively, at $V_{ds} = 1$ V and $V_{gs} = -0.6$ V, the valley being the lowest potential channel where electrons travel. For the [0 0 1] oriented FET's the barrier heights for the MESFET's with



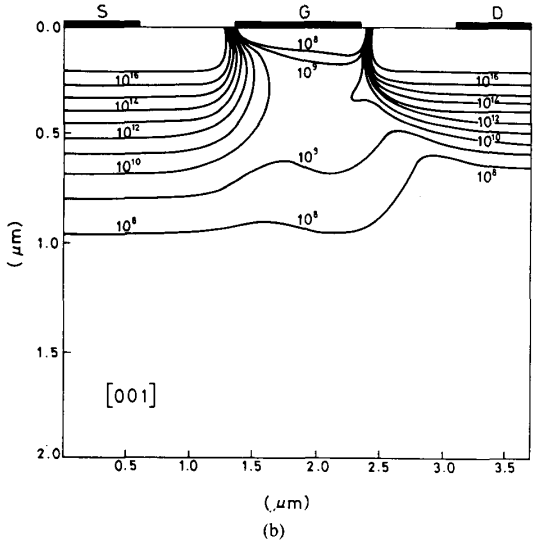
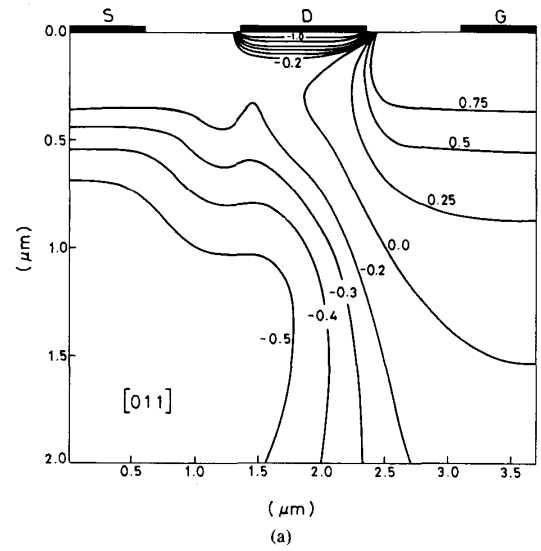


Fig. 7. Two-dimensional contour plots of (a) the potential distribution and (b) the carrier distribution for [0 0 1]-oriented FET's. The FET's have 1-μm gate and 1200-nm SiO_2 overlayer. The sources are grounded; the drain voltage is 1 V and the gate voltage is −0.6 V.



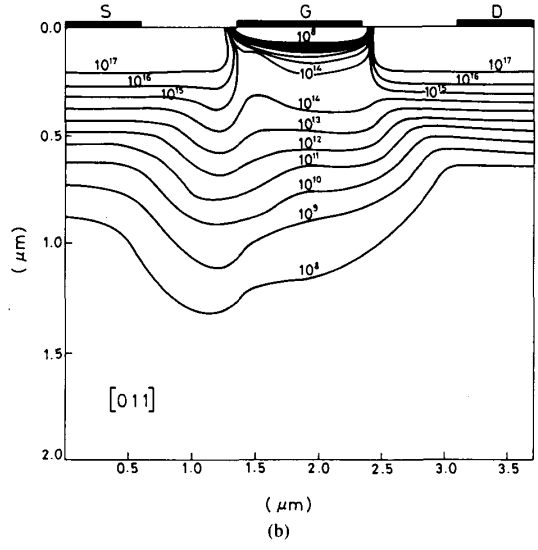
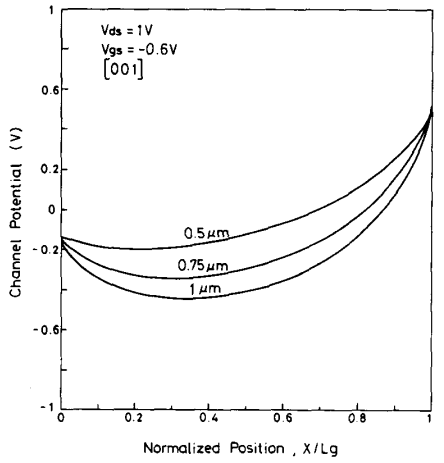


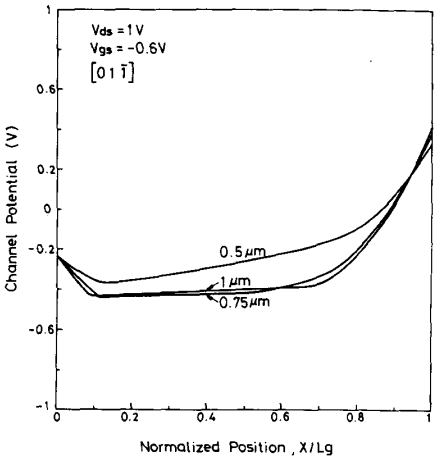
Fig. 8. Two-dimensional contour plots of (a) the potential distribution and (b) the carrier distribution for [0 1 1]-oriented FET's. The FET's have 1-μm gate and 1200-nm SiO_2 overlayer. The sources are grounded; the drain voltage is 1 V and the gate voltage is −0.6 V.

gate lengths equal to 0.5, 0.75, and 1 μm are 0.203, 0.349, and 0.445 eV, respectively. A 0.24-eV difference in barrier height between the 0.5- and 1-μm gate MESFET's is observed. So the amount of carriers that can surmount the barrier to reach the drain is higher for the 0.5-μm gate MESFET. The cause of the difference in the barrier height between devices with different gate lengths is believed to be similar to the drain-induced barrier-lowering effect in the short-channel Si MOSFET's [21]. In the [0 1 $\bar{1}$] direction, the potential barriers in the 1- and 0.75-μm devices, the barriers have nearly flat top, indicating the channel under the gates is totally depleted. For the [0 1 1] oriented FET's (potential distributions not shown in the figure), because the devices are above threshold, the channels are open and no potential barrier exist.

From the potential distribution described above, one can clearly see the relationship between the barrier height and subthreshold conduction. The lower the barrier height, the higher is the subthreshold conduction. The piezoelectric charges in the channels modify the doping profiles and effectively change the potential distributions and, therefore, the subthreshold conduction.

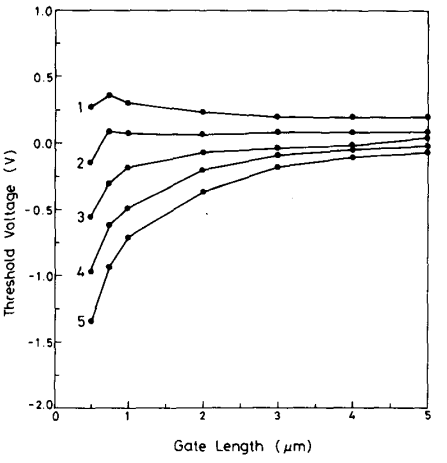


(a)

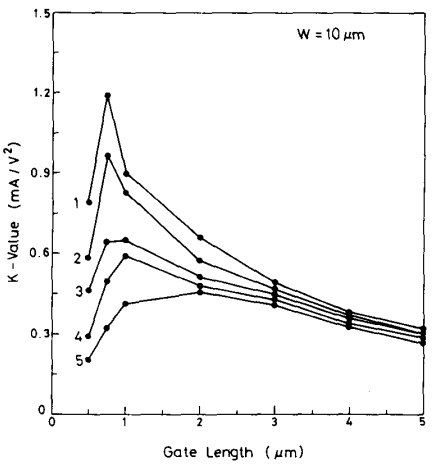


(b)

Fig. 9. The channel voltage along the potential valley under the gate for 0.5-, 0.75-, and 1-μm gate MESFET's in (a) the [0 0 1] direction and (b) the [0 1 1̄] direction at V_{ds} = 1 V and V_{gs} = −0.6 V.



(a)



(b)

Fig. 10. (a) Threshold voltage and (b) K value versus gate length for three different orientations and two different dielectric thicknesses. Curve 1 for the [0 1 1̄] orientation and d_f = 1200 nm; curve 2 for the [0 1 1̄] orientation and d_f = 600 nm; curve 3 for the [0 0 1] orientation; curve 4 for the [0 1 1] orientation and d_f = 600 nm; curve 5 for the [0 1 1] orientation and d_f = 1200 nm. The N_a, $L_{gn}{}^+$ and ΔR_i are 1×10^{15}, 0.1 μm, and 350 Å, respectively.

B. Piezoelectric Effects and Device Structures

1) Dielectric Layer Thickness: Since the stress induced in a device is proportional to the thickness of the surface dielectric layer, devices with different dielectric overlayer thickness are affected differently. In this subsection, results from devices with 1200- and 600-nm SiO_2 layers are presented. Other device parameters are the same as described before.

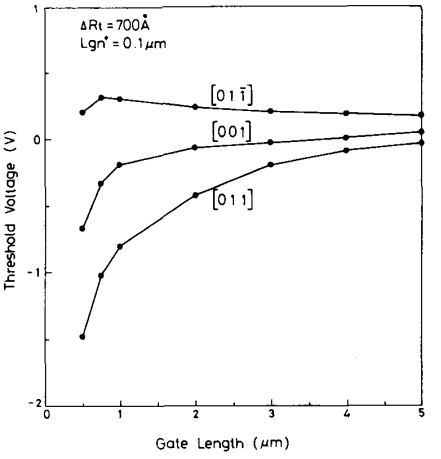
By fitting the I–V characteristics with the relation $I_{ds} = K \times (V_{gs} - V_t)^2$, we have calculated the threshold voltage and the K factors of the devices. Fig. 10(a) and (b), respectively, shows the calculated threshold voltage and K value versus gate length L_g for devices with two different dielectric overlayer thicknesses, d_f = 1200 and 600 nm, and along three different orientations ([0 1 1], [0 0 1], and [0 1 1̄]). Curves 1 and 2 are for devices oriented in the [0 1 1̄] direction, while curves 4 and 5 are for those in the [0 1 1] direction. Curves 1 and 5 are those with d_f = 1200 nm while curves 2 and 4 are with d_f = 600 nm. Curve 3 represents devices oriented in the [0 0 1] direction, which is immune from the piezoelectric effects. Since the piezoelectric effect is proportional to the thickness of the dielectric overlayer (see (3)), curves 1 and 5 correspond to devices with twice the effect as the devices of curves 2 and 4. This is the reason why curve 5 has the lowest threshold voltages, and curve 1 has the highest threshold voltages. Comparing curves 1, 2, 4, and 5 with curve 3 in Fig. 10(a), one can see that the piezoelectric effect has a strong influences on the short-channel effects. In the [0 1 1] direction, the piezoelectric effect enhances the threshold-voltage shift, but suppresses it in the [0 1 1̄] direction. The threshold voltage is nearly constant with gate length for curves 1 and 2. The slight increase

in threshold voltage for $L_g < 2$ μm of curve 1 indicates that for these devices the piezoelectric effect is stronger than the short-channel effect, which would otherwise bend the curve downward. When $d_f = 600$ nm (curve 2), the threshold voltage is constant except for $L_g = 0.5$ μm, where it shifts to a slightly lower value. This is because the piezoelectric effect is not strong enough to totally overcome the short-channel effects.

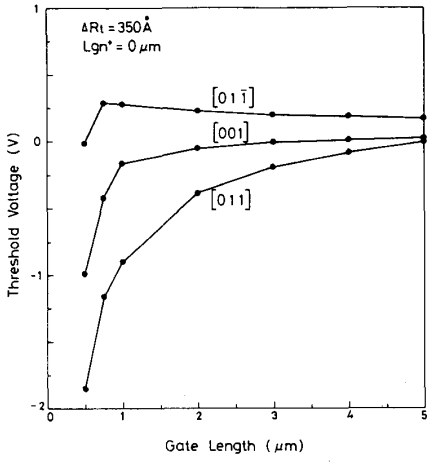
The K value shown in Fig. 10(b) also has a strong dependence on piezoelectric effect. In the [0 1 $\bar{1}$] direction, the K values of the devices are enhanced by the stress, while in the [0 1 1] direction they are depressed by the stress. This can be explained by the modulation of channel depth by piezoelectric charges. In [0 1 $\bar{1}$] direction, the channel doping profile is sharpened by the piezoelectric charge distribution, while in the [0 1 1] direction, the opposite situation takes place, i.e., the effective doping profile becomes broadened. Since the K value is inversely proportional to the channel depth, devices oriented in the [0 1 $\bar{1}$] direction have a higher K value than those oriented in the [0 1 1] direction. The degradation of the K value at very small gate lengths is due to short-channel effects. It should be pointed out that the position of the peak varies for different device orientations and different stress conditions. If we use the peak position of the [0 0 1] devices (curve 3) as a reference, where the peak occurs at a gate length around 1 μm, the gate length where maximum K occurs for the [0 1 1] oriented devices is longer but it is shorter for the [0 1 $\bar{1}$] oriented devices. The difference in the peak position is larger when the SiO_2 layer is thicker or the stress is stronger. This phenomenon has been observed experimentally by Onodera *et al.*, and their results agree with our calculation [6], [7].

2) Effect of Lateral Spreading of the N^+ Ions: The lateral spreading of the N^+ layer can significantly affect the device behavior [13]. We have simulated devices with three different lateral spreading conditions. The results presented in the previous sections are for structures with 0.1-μm spacing (L_{gn^+}) between the N^+ implant and the gate, and a 350-Å standard deviation (ΔR_t) for the lateral spreading of the N^+ ions. To investigate the effects of stronger lateral spreading, we have also stimulated devices with 700 Å and devices with $L_{gn^+} = 0$ μm.

Fig. 11(a) and (b) presents the calculated threshold voltage versus the gate length plots for devices with different condition of lateral spreading. Fig. 11(a) is for $L_{gn^+} = 0.1$ μm and $\Delta R_t = 700$ Å. Fig. 11(b) is for $L_{gn^+} = 0$ μm and $\Delta R_t = 350$ Å. These figures should be compared with Fig. 10(a), where the threshold voltage for devices with $L_{gn^+} = 0.1$ μm and $\Delta R_t = 350$ Å are shown. It is clear from these figures that the short-channel effect and the piezoelectric effect are stronger for devices with larger N^+ lateral spreading. When $L_{gn^+} = 0$ μm, the threshold voltage shift for the [0 1 1] FET with a 0.5-μm gate length is almost 2 V, which is about 0.5 V larger than for the FET with $L_{gn^+} = 0.1$ μm. In the [0 1 $\bar{1}$] direction, the threshold-voltage shift is relatively small except at very small gate lengths. When L_g is less than



(a)



(b)

Fig. 11. Threshold voltage V_t versus gate length L_g for (a) $L_{gn^+} = 0.1$ μm and $\Delta R_t = 700$ Å and (b) $L_{gn^+} = 0$ μm and $\Delta R_t = 350$ Å. The curves for $L_{gn^+} = 0.1$ μm and $\Delta R_t = 350$ Å have been shown in Fig. 10(a).

0.75 μm, the threshold voltage curves bend downward as the short-channel effect overcomes the piezoelectric effect. The downward bending is stronger for devices with larger N^+ lateral spreading due to stronger short-channel effect. From the results presented here, one can see it is very beneficial to have a 0.1-μm spacing between the N^+ implant and the gate for suppressing the short-channel effects.

The relationship between the N^+ lateral spreading and the threshold voltage shift has been studied by Chen *et al.* [9] using a one-dimensional analysis. They attributed the threshold voltage shift to the additional channel dopants under the gate from the lateral spreading of the N^+ ions. The threshold-voltage shift was calculated by integrating the contribution from these additional charges under the midpoint of the gate. In the structure described in this paper, however, we found the threshold-voltage shift cannot be simply explained by the additional charges under

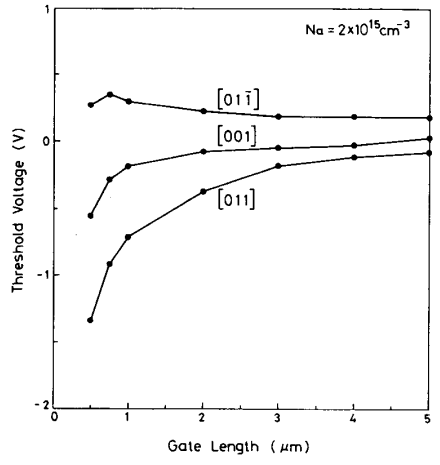


Fig. 12. Threshold voltage V_t versus gate length L_g for (a) $N_a = 2 \times 10^{15}$ cm^{-3} and (b) $N_a = 3 \times 10^{15}$ cm^{-3}. The curve for $N_a = 1 \times 10^{15}$ cm^{-3} has been shown in Fig. 10(a).

the midpoint of the gate. With the parameters chosen in this study, the number of additional charges caused by N^+ lateral spreading under the middle of the gate is too small to cause any significant changes in the threshold voltage. Accurate determination of the threshold voltages is a two-dimensional problem which takes into account of the actual charge distribution in the device channel. This is especially true for devices with small gate lengths and under strong influence of the piezoelectric effect.

3) Impurity Concentration N_a: In LEC semi-insulating GaAs substrates, the shallow carbon acceptors are compensated by deep EL-2 donors. The empty EL-2 concentration is equal to the carbon concentration. At the channel–substrate interface of a MESFET, the empty EL-2's are filled due to the interface band bending creating a negative space-charge region. On the channel side, a positive space-charge region is formed to balance the negative space-charge region on the substrate side. The width of the positive space-charge region depends on the concentration of the shallow acceptors (in the case carbon) in the substrate. As the carbon concentration increases, the positive space-charge region widens leaving a narrower conduction channel for the FET.

In our study, we have simulated devices with three different carbon concentrations in the substrates. They are 1×10^{15} cm^{-3}, 2×10^{15} cm^{-3}, and 3×10^{15} cm^{-3}. The EL-2 concentration is left to be 1×10^{16} cm^{-3}. Other device parameters are the same as those used for Fig. 10. The surface SiO_2 overlayer is taken to be 1200 nm.

The calculated threshold voltage versus gate length plots for devices with $N_a = 2 \times 10^{15}$ cm^{-3} and $N_a = 3 \times 10^{15}$ cm^{-3} are shown in Fig. 12(a) and (b), respectively. These figures should be compared with Fig. 10(a), where $N_a = 1 \times 10^{15}$ cm^{-3} is used. As N_a increases, the threshold voltage shifts toward the positive direction as expected. The short-channel effect is also reduced when N_a increases. This agrees with the results from studies on MESFET's with a buried p-layer under the channel [22], [23]. From Fig. 12(a) and (b), one can see that for the [0 1 $\bar{1}$] FET's, the short-channel effect has been reduced to such a degree that it can no longer compensate for the piezoelectric effect. So the threshold voltage at small gate lengths does not bend downward as that shown in Fig. 10(a).

It is interesting to see that as N_a is increased the orientation effect is also reduced. The threshold voltage difference between the [0 1 $\bar{1}$] FET's and the [0 1 1] FET's is smaller when N_a is higher. This can be qualitatively explained as follows: When N_a is higher, the conduction channel becomes narrower. So less piezoelectric charges reside in the channel and the piezoelectric effect becomes weaker. This phenomenon has been recently observed experimentally on a self-aligned MESFET structure with a buried p-layer [24].

IV. Conclusions

A two-dimensional simulation has been performed on self-aligned GaAs MESFET's with surface stress. The stress-induced piezoelectric effect causes the orientation dependence of the electric characteristics of the FET. The short-channel effects were found to be strongly dependent on the piezoelectric effect. With proper device orientation the piezoelectric effect can compensate for the short-channel effect. Self-aligned MESFET's with different structure parameters such as the lateral spreading of N^+ impurities, the N^+-gate spacing, and the shallow acceptor concentration have been simulated. It was found that lateral spreading of N^+ ions enhances the short-channel effect and the orientation effect. Higher carbon concentration in the substrate, however, reduces both effects. By choosing proper device structure with proper stress in the dielectric overlayer and aligning the devices in the right orientation, the short-channel effect can be effectively suppressed. Constant threshold voltage without gate length dependence can be achieved and the K value of the devices can also be improved. The compensation of the

short-channel effect by the piezoelectric effect, which does not exist for Si devices, may prove to be advantageous for GaAs MESFET's with scaled down dimensions for future semiconductor technologies.

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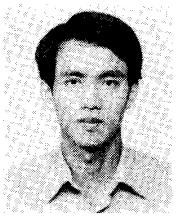

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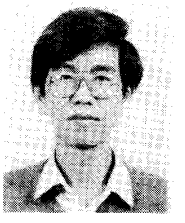

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He was credited with the design and fabrication of several important optoelectronic components, including the first integrated optoelectronic circuit, which consists of a laser and a Gunn device fabricated on a same substrate. After graduation, he joined Bell Laboratories, where he worked on integrated optics and semiconductor lasers. He joined Rockwell International in 1979 and worked on GaAs integrated integrated circuits. He did extensive work on substrate-related effects such as the orientation effect and the backgating effect. In 1982 he was promoted to be a project leader and later a manager with responsibility for the development of ultra-high-speed integrated circuits using high electron mobility transistors. In 1987 he joined National Chiao Tung University, where he is now a professor and the director of the semiconductor research center. He is also the director of the National Sub-micron Device Laboratory in charge of the construction of the first submicrometer device research center in the country. His current research interests are in the areas of III-V optoelectronic devices, MBE technology, heterostructure devices and physics, and device simulation.