Delay Models and Speed Improvement Techniques for *RC* Tree Interconnections Among Small-Geometry CMOS Inverters

CHUNG-YU WU, MEMBER, IEEE, AND MING-CHUEN SHIAU

Abstract—**Physical delay models entirely based upon device equations for small-geometry CMOS inverters with *RC* tree interconnection networks are presented. Through extensive comparisons with SPICE simulation results, it is shown that the maximum relative error in delay–time calculations using the developed model is within 15% for 1.5-μm CMOS inverters with *RC* tree interconnection networks. Moreover, the model has a wide applicable range of circuit and device parameters. Based upon the developed models and the mathematic optimization method, an experimental sizing program is constructed for speed improvement of interconnection lines and trees. In this program, given the size of the input logic gate and its driving interconnection resistances, capacitances, and structures, users can choose one of four speed improvement techniques and determine the suitable sizes and/or number of drivers/repeaters for a minimum delay. The four speed improvement techniques use minimum-size repeaters, optimal-size repeaters, cascaded input drivers, and optimal-size repeaters with cascaded input drivers to reduce the interconnection delay. It is found from the sizing results of the experimental program that the required tapering factor in cascaded drivers is not *e* (the base of the natural logarithm) but a value in the range of 4–8. Moreover, adding a small number of drivers/repeaters with large sizes is more efficient in reducing the interconnection delay. It is also shown that the technique of optimal-size repeaters with cascaded input drivers can lead to the lowest delay.**

I. Introduction

IT IS known that interconnection delay is a critical factor in speed improvement of CMOS VLSI/ULSI [1], [2]. To deal with this problem, efficient and analytical delay models of complicated interconnection nets among logic gates have to be developed first in order to perform the delay analysis. Then, with the aid of the delay models, optimal drivers should be designed to drive interconnection nets and minimize the delay. Evidently, the timing models must be accurate enough in calculating interconnection delay as well as driver's delay. Otherwise, the driver scheme cannot be correctly designed and sized.

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The authors are with the Institute of Electronics and Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan 30039, Republic of China.
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So far, many interconnection delay models [3]–[12] have been proposed. Among them, modeling logic gates and interconnection nets separately [3]–[9] or modeling a logic gate by a single linear *RC* circuit [10]–[12] may lead to a significant error in high-performance design [13]–[15].

Recently, a physical delay model for simple interconnection lines among small-geometry CMOS inverters has been proposed [13], [14] where analytical delay equations were derived together with the input waveshape effects [16], [17] and both the effect of a logic gate on the interconnection delay and the effect of interconnection on the gate delay were considered. It has been shown that the proposed model has a good accuracy and a wide applicable range of circuit and device parameters.

It is the aim of this paper to generalize the modeling techniques [13], [14] for the characterization of the delay of interconnection tree networks among small-geometry CMOS inverters. Through extensive comparisons with SPICE simulation results, the maximum relative error of the developed model is found to be below 15% for the delay times of CMOS inverters with different *RC* values in each branch of tree interconnection networks, different gate sizes, device parameters, and even input excitation waveforms. Moreover, the delay at any output node can also be accurately predicted.

A long interconnection line or tree among the two logic gates degrades the total delay significantly. To improve the speed, a suitable number of drivers and/or repeaters with suitable sizes has to be added to drive the interconnection nets [2], [18]. There are four speed-improvement techniques which use minimum-size repeaters, optimal-size repeaters, cascaded input drivers, and optimal-size repeaters with cascaded input drivers [2]. In these techniques, determining the suitable number and sizes of drivers and/or repeaters is a very important issue in design and optimization.

Based upon the developed interconnection line and tree delay models, the four speed-improvement methods

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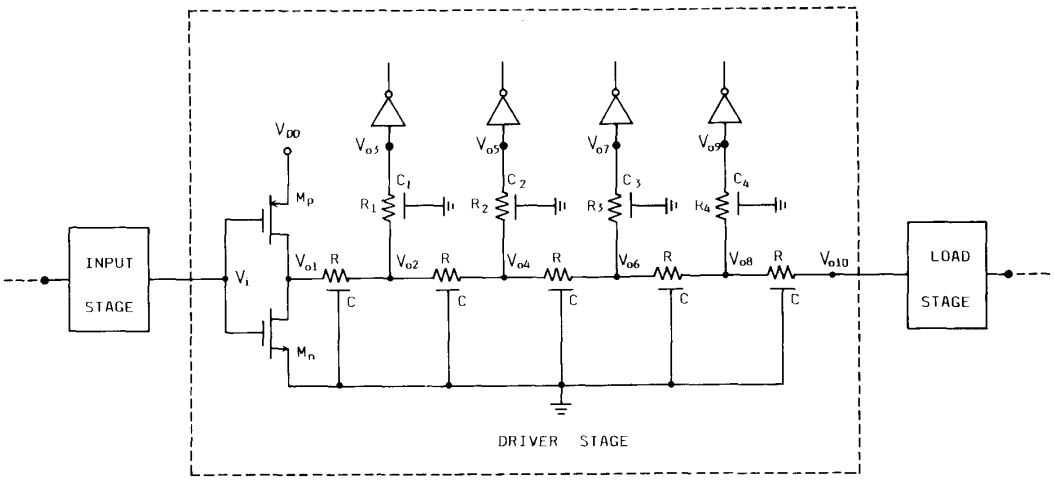


Fig. 1. A chain of identical CMOS inverters with *RC* tree interconnection networks.

[2], and the mathematic optimization technique of the Broyden–Fletcher–Shanno (BFS) [19] method, an experimental CAD program is constructed to determine suitable sizes and/or numbers of drivers/repeaters for interconnection lines and trees. It is shown that the driver and/or repeater schemes can be more accurately designed in this program to achieve a higher speed than those designed by the other approach [2].

In Section II, a model formulation of interconnection trees is presented. Verifications of the developed model are then presented in Section III. The application of the developed delay models in speed improvement is described in Section IV. Finally, the discussion and conclusions are given in Section V.

II. Delay Model of Interconnection Trees

A. Waveform Generation, Timing Definition, and MOSFET Region Location

Consider a string of identical 1.5-μm CMOS inverters with *RC* tree interconnection networks as shown in Fig. 1. To accurately simulate the behaviors of the *RC* tree interconnection networks under various operating conditions, each branch in the tree networks is equivalently represented by a three-step π ladder circuit [11] as will be shown later. If the fall time of the output voltage V_{oj} where $1 \leqslant j \leqslant 10$ is to be characterized, its simulated characteristic waveforms [13], [14], [16] can be illustrated in Fig. 2. At any output node j, the falling waveform of the node voltage V_{oj} has an initial delay time t_{dfj}, fall time T_{Fj}, and fall delay time T_{PHLj}, as indicated in Fig. 2 for $j = 1$ and 10.

During the fall-time period T_{Fj}, the operating regions of the MOSFET's M_p and M_n and those in the load stage are first determined from their drain–source voltages V_{DS} and drain–source saturation voltages V_{DSAT}. According to the MOSFET operating regions, the falling waveform of V_{oj} during the fall-time period T_{Fj} can be divided into Regions I and II as indicated in Fig. 2. In Region I, M_p is nearly off and M_n is saturated. In Region II, however, M_p is off and M_n is linear. For the load stage in both regions, its PMOSFET is saturated and the NMOSFET is in the linear region. Both devices in the load stage are treated as a capacitive load and their capacitances are calculated according to their operating regions.

On the waveform of V_{o1}, the boundary point between Regions I and II can be determined by letting $V_{o1}(=V_{DSN})$ be equal to the saturation voltage V_{DSATN}, which can be calculated from the V_{DSAT} equation in the level-2 model of SPICE with the corresponding $V_i(=V_{GSN})$. The time period t_{fsl} during which the voltage $V_{o1}(t)$ lowers from V_{DD} to V_{DSATN} can then be calculated from the equation of $V_{o1}(t)$ to be derived later. From the calculated t_{fsl}, the corresponding boundary point on each output voltage V_{oj} at any output node can be found. In this way the voltage $V_{oj}(t_{fsl})$ of $V_{oj}(t)$ at the boundary point between Regions I and II can be calculated.

B. Large-Signal Equivalent Circuit Generation and Current / Capacitance Linearization

The overall large-signal equivalent circuit during T_{Fj} is given in Fig. 3 where each branch in the tree interconnection networks is represented by a three-step π ladder circuit to simplify the overall equivalent circuit while retaining the delay accuracy, as will be verified later. In Fig. 3, the linearized equations of the drain current I_{dn} in Region I (saturation) and Region II (linear) are given in Table I [13], [14]. The linearized saturation drain current is obtained by using the lambda model [20] with a fixed value of the parameter λ. In Region I, this value is determined by the slope of the drain currents between $V_{o1} = V_{DSATN}$ and $V_{o1} = (V_{DD} + V_{DSATN})/2$ with the averaged value of V_{GSN} in this region. In Region II, the value of λ can be determined by the slope of the drain currents between $V_{o1} = 0.0$ and $V_{o1} = V_{DSATN}/2$. As compared to

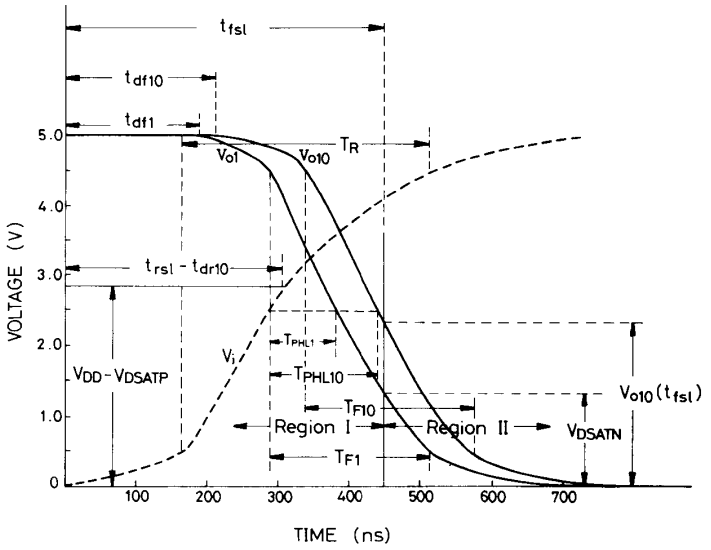
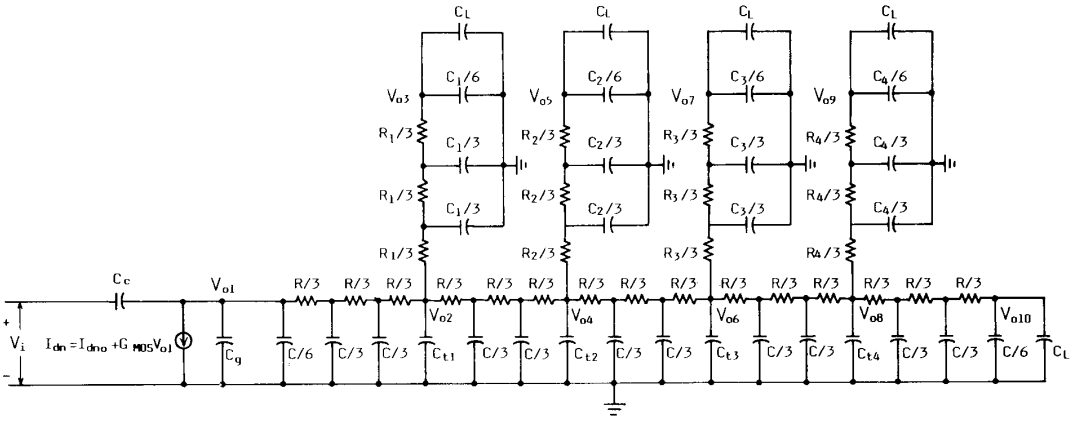


Fig. 2. Typical fall characteristic waveforms of the circuit in Fig. 1.



$C_{t1} = C/6 + C/6 + C_1/6$ $\quad C_c = C_{gdn} + C_{gdp}$

$C_{t2} = C/6 + C/6 + C_2/6$ $\quad C_g = C_{dbn} + C_{dbp}$

$C_{t3} = C/6 + C/6 + C_3/6$ $\quad C_L = C_{gdn} + C_{gdp} + C_{gsn} + C_{gsp}$

$C_{t4} = C/6 + C/6 + C_4/6$

Fig. 3. Large-signal equivalent circuit of the circuit in Fig. 1 during the fall-time period.

SPICE simulations, the linearized drain current equation has a maximum error of 10% at the boundary of saturation and linear regions.

The load capacitance C_L and the device capacitances C_c and C_g are all voltage-dependent. All the voltage-dependent capacitances as well as the voltage-dependent device parameters and the input voltage V_i in the drain current are further linearized by fixing their values at the linearization point [13], [14]. The linearization point in Region I is optimally determined at the center point with $t = t_{fse}$ where $V_{o1}(t_{fse}) = (V_{DD} + V_{DSATN})/2$, whereas that in Region II is at the center point $t = t_{fle}$ where $V_{o1}(t_{fle}) = V_{DSATN}/2$ [13], [14]. After linearization, the equivalent circuit of Fig. 3 becomes a linear circuit.

C. Effective Dominant Pole Calculation

In Fig. 3 the feedthrough current from the input node V_i to the output node V_{oj} is negligibly small so that its effect can be neglected [13], [14], [21], [22]. Then, from the S-domain nodal equations of the circuit in Fig. 3 with the input node short-circuited, the voltage $V_{oj}(S)$ at output

node j can be obtained and written as

$$V_{oj}(S)=\frac{(b_{28}S^{28}+b_{27}S^{27}+\cdots+b_2S^2+b_1S+1)b_0}{S(a_{28}S^{28}+a_{27}S^{27}+\cdots+a_2S^2+a_1S+1)a_0} \quad (1)$$

where b_i and a_i are positive and real coefficients. The effective dominant pole P_{fsj} of V_{oj} in Region I (saturation) during the fall-time period can be calculated from (1) as [13], [14]

$$\frac{1}{P_{fsj}}=\left[(a_1^2-2\times a_2)-(b_1^2-2\times b_2)\right]^{1/2}. \quad (2)$$

In this expression, the second term in the square root represents the effective dominant zero contingent upon the output node position. The effective dominant zero is entirely produced by interconnection networks. Neglecting the effective dominant zero will lead to a significant error.

D. Voltage Waveform Function Calculation

By using the single-pole-response approximation in each region, the output voltage waveform $V_{oj}(t)$ at any output node can be analytically expressed in terms of its initial delay, effective dominant pole, and initial and final voltages of Regions I and II. During the fall-time period T_{Fj}, the initial and final values of the output voltage V_{oj} in Region I are V_{DD} and $-1/\lambda n$, respectively. The initial voltage V_{DD} is due to the full voltage swing of the CMOS logic gates, and the final voltage $-1/\lambda n$ can be obtained by letting the NMOSFET drain current I_{dn} listed in Table I be equal to zero. But in Region II they are $V_{oj}(t_{fsl})$ and 0, where $V_{oj}(t_{fsl})$ is the voltage of $V_{oj}(t)$ at the boundary point between Regions I and II. If the beginning point of the input voltage waveform is chosen as the origin of time axis, the output voltage waveform $V_{oj}(t)$ at any output node j can be expressed as

$$V_{oj}(t)=\begin{cases}\left(V_{DD}+\dfrac{1}{\lambda n}\right)e^{-P_{fsj}(t-t_{dfj})}-\dfrac{1}{\lambda n}, & t_{dfj}\leqslant t<t_{fsl}\ \text{(Region I)}\\ V_{oj}(t_{fsl})e^{-P_{flj}(t-t_{fsl})}, & t_{fsl}\leqslant t<\infty\ \text{(Region II)}\end{cases} \quad (3)$$

where P_{fsj} and P_{flj} represent the effective dominant pole in Regions I and II, respectively, at output node j and t_{dfj} is the initial delay at output node j.

From the waveform function $V_{oj}(t)$, the equations of t_{fsl}, t_{fse}, and t_{fle} as listed in Table I can be derived according to their definitions given in Sections II-A and B. Substituting the expression of t_{fsl} into (3), all the output voltages $V_{oj}(t_{fsl})$ in (3) for $1\leqslant j\leqslant 10$ can be written as

$$V_{oj}(t_{fsl})=\left(V_{DD}+\frac{1}{\lambda_n}\right)\times\left[\frac{V_{DSATN}+\dfrac{1}{\lambda n}}{V_{DD}+\dfrac{1}{\lambda n}}\right]^{P_{fsj}/P_{fsl}}-\frac{1}{\lambda n}. \quad (4)$$

E. Rise / Fall Time and Delay Time Formulation

The characteristic fall time T_{Fj} of the output voltage $V_{oj}(t)$ can be calculated from (3) and written as

$$T_{Fj}=\frac{1}{P_{fsj}}\ln\left[\frac{0.9V_{DD}+\dfrac{1}{\lambda n}}{V_{oj}(t_{fsl})+\dfrac{1}{\lambda n}}\right]+\frac{1}{P_{flj}}\ln\left[\frac{V_{oj}(t_{fsl})}{0.1V_{DD}}\right],$$

$$\text{if } V_{oj}(t_{fsl})\geqslant 0.1V_{DD} \quad (5)$$

$$T_{Fj}=\frac{1}{P_{fsj}}\ln\left[\frac{0.9V_{DD}+\dfrac{1}{\lambda n}}{0.1V_{DD}+\dfrac{1}{\lambda n}}\right],$$

$$\text{if } V_{oj}(t_{fsl})<0.1V_{DD}. \quad (6)$$

In the calculation of T_{Fj}, V_i represents the rising characteristic input waveform which also has two different regions with different effective dominant poles. In formulating $V_i(t_{fse})$ and $V_i(t_{fle})$, single-pole-response approximation is used and $V_i(t)$ can be expressed as

$$V_i(t)=V_{DD}(1-e^{-P_{rk}t}) \quad (7)$$

where

$$P_{rk}=\frac{\ln(9.0)}{T_{Rk}}. \quad (8)$$

In the above equations, P_{rk} and T_{Rk} represent the characteristic rise pole and rise time, respectively, at node k. Substituting the expressions of t_{fse} and t_{fle} into (7), the equations of $V_i(t_{fse})$ and $V_i(t_{fle})$ in Table I can be derived. In these two equations, an empirical and universal constant is given to the pole–delay product $P_{r10}t_{df1}$, which has been proven to be a nearly constant physical parameter [21]–[24].

Through $V_i(t_{fse})$ and $V_i(t_{fle})$, T_{Fj} becomes a function of T_{Rk} and vice versa. Simple iterations are required to solve T_{Fj} and T_{Rk}. Usually the resulting iteration number is less than 5.

According to the delay definition in Fig. 2, the rise propagation delay T_{PLHj} and fall propagation delay T_{PHLj}

between the input node k and any output node j can be expressed as

$$T_{PLHj} = T_{drj} + T_{ROj} - T_{FOk} \quad (9)$$

$$T_{PHLj} = T_{dfj} + T_{FOj} - T_{ROk} \quad (10)$$

where $T_{ROj}(T_{ROk})$ stands for the time interval during which $V_{oj}(t)(V_{ok}(t))$ rises from 0 to $0.5V_{DD}$ at node j (k), and $T_{FOj}(T_{FOk})$ for the time interval during which $V_{oj}(t)$ ($V_{ok}(t)$) lowers from V_{DD} to $0.5V_{DD}$.

For simplicity, empirical laws for the initial delay times t_{drj} and t_{dfj} were found [13], [14], [21]–[24]. As a result, the rise propagation delay T_{PLHj} and fall propagation delay T_{PHLj} at any output node j can be reformulated by the simple relations

$$T_{PLHj} = (0.1256T_{ROj} + 0.5035T_{FOj} + 0.4585T_{FOk}) + T_{ROj} - T_{FOk}, \quad j = 1,2,3,\cdots 10, \quad k = 10 \quad (11)$$

$$T_{PHLj} = (0.1638T_{FOj} + 0.3917T_{ROj} + 0.4874T_{ROk}) + T_{FOj} - T_{ROk}, \quad j = 1,2,3,\cdots 10, \quad k = 10. \quad (12)$$

Note that the above equations are universal and can be used to calculate the delay times under various conditions with a satisfactory accuracy, as will be verified in the next section.

III. Comparisons with SPICE Simulations

A. CMOS Inverters with RC Tree Interconnections

To verify the accuracy of the developed analytical delay models, extensive comparisons between theoretical calculations and SPICE simulations were made for 1.5-μm CMOS inverters with different RC values in each branch of the tree networks, different gate sizes, device parameters, and even input excitations. Part of the comparisons is shown in Fig. 4 for the rise/fall delay times at the first output node of CMOS inverters with smaller RC values in each branch of the RC tree interconnection networks and reduced threshold voltages V_{TOP} and V_{TON}. It is shown that the maximum relative error in the rise/fall delay times at any output node is 15%. Since the delay times are expressed by equations in the developed model, the CPU time consumed in the delay calculation is about two orders of magnitude smaller than that in point-by-point full transient analysis like SPICE.

As mentioned in the previous section, the developed model equations contain the constant product of the input pole and the initial delay. Moreover, the output fall(rise) time is a function of the input rise(fall) time. Through these relations, the input waveform effect has been implicitly incorporated into the model. Thus it can be applied to the cases of the noncharacteristic waveforms not deviating much from the characteristic waveforms. The general relative errors for the delay times are still below 15%. The ability to calculate the noncharacteristic waveform timing makes the developed models more practical and versatile.

TABLE I
The Linearized Equations of the NMOSFET Drain Current I_{dn} in Regions I and II

$$I_{dn}(V_{GSN}=V_i, V_{DSN}=V_{o1}) = I_{dno}(1+\lambda_n V_{o1}) = I_{dno} + G_{MOS}V_{o1}$$

where

in Region I

$$G_{MOS} = \frac{I_{dn}(V_i(t_{fse}),(V_{DD}+V_{DSATN})/2) - I_{dn}(V_i(t_{fse}),V_{DSATN})}{(V_{DD}-V_{DSATN})/2}$$

$$I_{dno} = \frac{I_{dn}(V_i(t_{fse}),V_{DSATN})\frac{V_{DD}+V_{DSATN}}{2} - I_{dn}(V_i(t_{fse}),\frac{V_{DD}+V_{DSATN}}{2})V_{DSATN}}{\frac{V_{DD}-V_{DSATN}}{2}}$$

$$\lambda_n = \frac{G_{MOS}}{I_{dno}}$$

in Region II

$$G_{MOS} = \frac{I_{dn}(V_i(t_{fle}), V_{DSATN}/2) - I_{dn}(V_i(t_{fse}),0.0)}{V_{DSATN}/2}$$

$$I_{dno} = 0.0$$

$$\lambda_n = \infty$$

$$t_{fsl} = t_{dfl} + \frac{1}{P_{fsl}}\ln\left\{\frac{V_{DD}+\frac{1}{\lambda_n}}{V_{DSATN}+\frac{1}{\lambda_n}}\right\}$$

$$t_{fse} = t_{dfl} + \frac{1}{P_{fsl}}\ln\left\{\frac{V_{DD}+\frac{1}{\lambda_n}}{\frac{1}{2}(V_{DD}+V_{DSATN})+\frac{1}{\lambda_n}}\right\}$$

$$t_{fle} = t_{dfl} + \frac{1}{P_{fsl}}\ln\left\{\frac{V_{DD}+\frac{1}{\lambda_n}}{V_{DSATN}+\frac{1}{\lambda_n}}\right\} + \frac{1}{P_{fll}}\ln(2.0)$$

$$V_i(t_{fse}) = V_{DD}\{1-e^{-P_{r10}t_{dfl}}[\frac{\frac{1}{2}(V_{DD}+V_{DSATN})+\frac{1}{\lambda_n}}{V_{DD}+\frac{1}{\lambda_n}}]^{P_{r10}/P_{fsl}}\}$$

$$P_{r10}t_{dfl} = 0.60$$

$$V_i(t_{fle}) = V_{DD}\{1-e^{-P_{r10}t_{dfl}}[\frac{V_{DSATN}+\frac{1}{\lambda_n}}{V_{DD}+\frac{1}{\lambda_n}}]^{P_{r10}/P_{fsl}\,2^{-P_{r10}/P_{fll}}}\}$$

$$P_{r10}t_{dfl} = 0.60$$

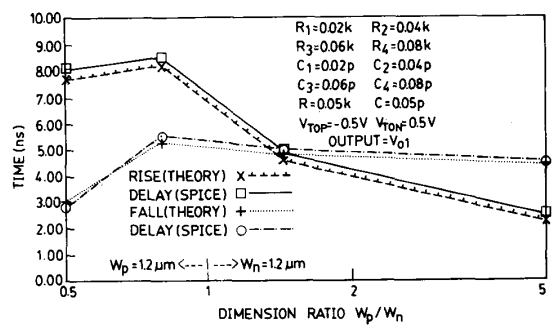


Fig. 4. Calculated and simulated rise/fall delay for 1.5-μm CMOS inverters with smaller RC values in RC tree network and reduced threshold voltages V_{TOP} and V_{TON}.

Although the above comparisons are all based on the demonstrating networks like Fig. 1, the developed model can also deal with the RC tree interconnection networks with different RC values in every branch of the tree networks and retain the same error characteristic.

B. CMOS Inverters with RC Line Interconnections

The developed delay model for interconnection tree networks can also be applied to calculate the signal timing of CMOS inverters with RC line interconnections and the

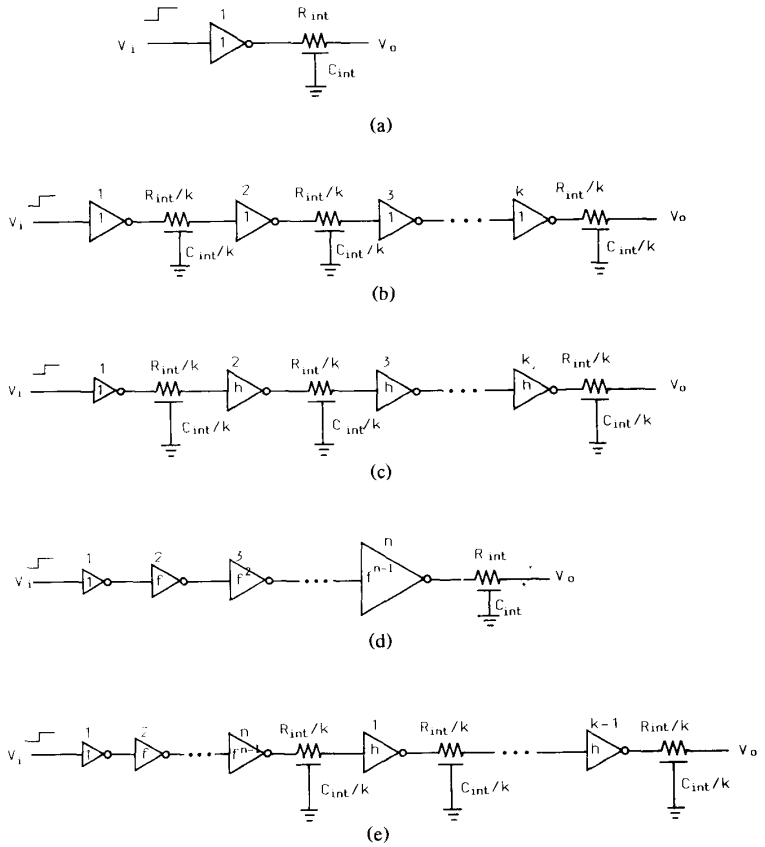


Fig. 5. Speed-improvement techniques for driving interconnection line: (a) original interconnection line; (b) minimum-size repeaters; (c) optimal-size repeaters; (d) cascaded input drivers; and (e) optimal-size repeaters with cascaded input drivers.

same relative error characteristic can be retained. In this sense, the developed timing models are quite general.

IV. Speed-Improvement Techniques

There are many optimization methods to solve the unconstrained problem with a minimum delay [19], [25], [26]. Among them, the Broyden–Fletcher–Shanno (BFS) method is an optimization method with quadratic convergence rates. Thus the CPU time consumption can be reduced. This method uses only the function values and gradient vectors in generating mutually conjugate search direction. From the computation point of view, it is very suitable for the sizing of CMOS inverters with *RC*-tree interconnection networks.

Based upon the developed interconnection delay models and the Broyden–Fletcher–Shanno (BFS) method [19], an experimental program is constructed for speed improvement of the interconnection lines and trees. In this program, given logic gate sizes and its driving interconnection resistances, capacitances, and structures, users can choose one of four speed improvement techniques [2]. The program can calculate the number and/or sizes of drivers/repeaters for a minimum delay. The four improvement techniques use minimum-size repeaters, optimal-size repeaters, cascaded input drivers, and optimal-size repeaters with cascaded input drivers. It is shown that the program can accurately design the number and/or sizes of drivers/repeaters in each scheme. Also, the results are more accurate than those given in the previous literature [2].

A. Speed-Improvement Techniques in RC Line Interconnections

1) Minimum-Size Repeaters: When the resistance of interconnection networks is comparable to or larger than the output resistance of the active driver, propagation delay increases as the square of the interconnection length because both capacitance and resistance increase linearly with the interconnection length [2]. The use of k minimum-size inverters as repeaters makes time delay linear with length by dividing the interconnection lines into k smaller subsections, as shown in Fig. 5(a) and (b). In this figure, R_{int} and C_{int} stand for interconnection resistance and capacitance, respectively, and the minimum W/L ratios of PMOSFET and NMOSFET are 1.2 μm/1.2 μm

TABLE II
THE CALCULATED AND THE SIMULATED TOTAL PAIR DELAY TIMES IN FIG. 5

R_{int} and C_{int} Values	Data Type		Original Interconnection Line	Minimum-Size Repeaters	Optimal-Size Repeaters	Cascaded Input Drivers	Optimal-Size Repeaters with Cascaded Input Drivers
R_{int} =0.10kΩ	THEORY		2.21ns	2.21ns	2.21ns	2.21ns	2.21ns
C_{int} =0.01pF	SPICE	Our Work	2.45ns	2.45ns	2.45ns	2.45ns	2.45ns
		[2]	2.45ns	2.45ns	2.45ns	2.45ns	2.45ns
R_{int} =0.20kΩ	THEORY		5.136ns	5.136ns	4.45ns	3.658ns	3.658ns
C_{int} =0.10pF	SPICE	Our Work	5.55ns	5.55ns	4.83ns	4.018ns	4.018ns
		[2]	5.55ns	5.55ns	5.25ns	4.55ns	4.55ns
R_{int} =2.00kΩ	THEORY		36.13ns	36.13ns	10.3ns	6.806ns	6.806ns
C_{int} =1.00pF	SPICE	Our Work	35.82ns	35.82ns	11.1ns	6.954ns	6.954ns
		[2]	35.82ns	44.2ns	13.56ns	8.22ns	8.06ns
R_{int} =20.0kΩ	THEORY		102.6ns	80.68ns	21.08ns	44.19ns	15.96ns
C_{int} =2.00pF	SPICE	Our Work	100.2ns	82.50ns	22.78ns	42.24ns	18.16ns
		[2]	100.2ns	120.52ns	27.18ns	43.84ns	23.12ns
R_{int} =20.0kΩ	THEORY		498.9ns	361.3ns	43.8ns	194.6ns	33.19ns
C_{int} =10.0pF	SPICE	Our Work	485.9ns	352.8ns	48.2ns	189.7ns	36.17ns
		[2]	485.9ns	444.6ns	64.56ns	194.2ns	51.2ns
R_{int} =200kΩ	THEORY		21380ns	3612ns	325.66ns	17341ns	305.08ns
C_{int} =100pF	SPICE	Our Work	20935ns	3570ns	368.5ns	17198ns	337.9ns
		[2]	20935ns	4438.4ns	531.28ns	17264ns	481.4ns

and 1.2 μm/1.2 μm, respectively. The developed program is constructed together with the input waveshape effects [16], [17] so that it can deal with any input waveform not deviating much from the characteristic waveforms. However, for comparisons with the results in [2], the input waveform V_i uses step-voltage excitation in Fig. 5. Running the developed program, the propagation delay of an interconnection line with k minimum-size inverters as repeaters can be optimized. Table II shows the calculated and the simulated total pair delay of the original interconnection line (Fig. 5(a)) and the interconnection line with k minimum-size repeaters, with the calculated k listed in Table III. It is shown that the speed improvement in total pair delay is significant only when $R_{int}C_{int}$ of the interconnection line is large. When $R_{int}C_{int}$ is small, no minimum-size repeater is added ($k = 1$) and the total delay remains unchanged. This means that using minimum-size repeaters can improve the speed of a very long interconnection line but not a medium or short one.

2) Optimal-Size Repeaters: Total pair delay can be further improved by increasing the size of repeaters because the driving capability of the repeaters is directly proportional to the size of MOSFET's. Running the developed program, the minimum total pair delay of an *RC* interconnection line driven by equally spaced $k-1$ optimal-size inverters as repeaters (Fig. 5(c)) with size factor h can be achieved. The calculated and the simulated total pair delay times are listed in Table II whereas the calculated values of k and h are listed in Table III. Note that the first stage of this scheme must be a minimum-size inverter so that its delay can be compared to other schemes which have the same minimum-size inverter as the first stage.

As may be seen from Table II, adding optimal-size repeaters is very efficient in reducing the overall delay of an interconnection line when $R_{int}C_{int}$ is large. The reduction percentage can be as high as 98% for a long interconnection line with $R_{int} = 200$ kΩ and $C_{int} = 100$ pF.

As a comparison, the number of drivers/repeaters and their sizes in both cases of minimum-size repeaters and optimal-size repeaters are also calculated by using the formulas given in [2]. Then the total delay times of the overall circuit are obtained from SPICE simulations. Table II shows the SPICE simulated total pair delay times whereas Table III gives the corresponding number of drivers/repeaters and their sizes. It can be seen that the SPICE simulated delay times in both schemes designed through the use of the program are smaller than those designed from the formulas in [2]. But the required number of minimum-size and optimal-size repeaters in our work is less than that in [2]. For example, according to the design program, 97 minimum-size repeaters are required for an interconnection line with $R_{int} = 200$ kΩ and $C_{int} = 100$ pF and the resultant SPICE simulated delay is 3570 ns. According to the result in [2], five times more repeaters (500 repeaters) are required but the resultant delay is 24% higher. For optimal-size repeaters, the number of repeaters calculated by using the design program (239) is also much smaller than that (515) in [2] by 53%, whereas the delay can be reduced by 30% through the suitably optimized repeaters sizes. Note that the repeater

TABLE III
THE REQUIRED VALUES FOR THE FOUR SPEED-IMPROVEMENT TECHNIQUES IN OUR DEVELOPED DELAY MODEL AND IN [2]

R_{int} and C_{int} Values	Minimun-Size Repeaters	Optimal-Size Repeaters		Cascaded Input Drivers		Optimal-Size Repeaters with Cascaded Input Drivers				Data Type
	k	h	k	f	n	f	n	h	k	
R_{int} =0.10kΩ	1	0	1	0	1	0	1	0	0	Model
C_{int} =0.01pF	1	0	1	0	1	0	1	0	0	[2]
R_{int} =0.20kΩ	1	7.25	3	6.94	3	6.94	3	0	0	Model
C_{int} =0.10pF	1	17.5	3	e	3	e	3	0	0	[2]
R_{int} =2.00kΩ	1	22.5	9	6.38	3	6.38	3	0	0	Model
C_{int} =1.00pF	5	17.5	15	e	3	e	3	17.5	4	[2]
R_{int} =20.0kΩ	5	27.5	15	4.12	3	4.75	3	43.75	8	Model
C_{int} =2.00pF	25	17.5	29	e	3	e	3	17.5	12	[2]
R_{int} =20.0kΩ	9	31.75	37	5.44	3	6.94	3	44.46	20	Model
C_{int} =10.0pF	36	17.5	65	e	3	e	3	17.5	44	[2]
R_{int} =200kΩ	97	32.25	239	7.06	3	6.94	3	44.48	212	Model
C_{int} =100pF	500	17.5	515	e	3	e	3	17.5	444	[2]
Average CPU Time(S)(IBM PC) for Model	19.2	52.5		40.8		124.4				

size should be properly increased with the increase of $R_{int}C_{int}$ in order to achieve a better speed performance.

3) Cascaded Input Drivers: It is shown that a chain of n drivers that increase in size by a tapering factor f can be used to drive the *RC* loads [2], [27] or interconnection lines as shown in Fig. 5(d). Running the developed program, the optimal total pair delay of an interconnection line driven by such cascaded and tapered drivers can be calculated. Table II shows the calculated and the simulated results; the required values for f and n are listed in Table III. The program shows that the suitable tapering factor is approximately 4–8 instead of e (the base of the natural logarithm) as in the conventional taper buffer [2]. Furthermore, because the number of inverters n must only be an odd integer number [16], all values of n are equal to 3, which is less than those in [2].

It is shown in [16] that the suitable tapering factor of CMOS inverters with pure capacitive loads is in the range 3–5. To drive *RC* loads rather than pure capacitive loads, however, a larger tapering factor has to be used because it leads to a larger transistor size and thus a smaller ON resistance, which can drive *RC* loads efficiently to achieve a minimum delay. So the required tapering factor is in the range 4–8.

Table II shows the SPICE simulated total pair delay times in [2] whereas Table III gives the corresponding number of cascaded drivers and their sizes. It can be seen that cascaded input drivers with a larger f and a smaller n (in our work) are more efficient than those with a smaller f and a larger n (in [2]) in reducing the delay time when $R_{int}C_{int}$ is not large. For example, when an interconnection line has $R_{int} = 2.00$ kΩ and $C_{int} = 1.00$ pF, the delay time of five cascaded drivers with $f = e$ is about 18% higher than that of three cascaded drivers with $f = 6.38$.

As compared to the technique of optimal-size repeaters, cascaded input drivers are less efficient in reducing the interconnection delay when $R_{int}C_{int}$ is large. But cascaded input drivers are still better than minimum-size repeaters when $R_{int}C_{int}$ is not very large.

4) Optimal-Size Repeaters with Cascaded Input Drivers: As illustrated in Fig. 5(e), optimal-size repeaters with cascaded input drivers combine the structure of the optimal-size repeaters and the cascaded input drivers. Table II shows the calculated and the simulated total pair delay times whereas Table III gives the required values of f, n, k, and h.

As compared to the results in [2], a lower delay time can be achieved by optimal-size repeaters with a much less k and a larger h and by cascaded input drivers with the same n and a larger f. For $R_{int} = 200$ kΩ and $C_{int} = 100$ pF, the delay time obtained in this design is about 30% lower than that in [2]. Among the four techniques, this technique can give the lowest delay time, which is 8% lower than that of optimal-size repeaters, as shown in Table II.

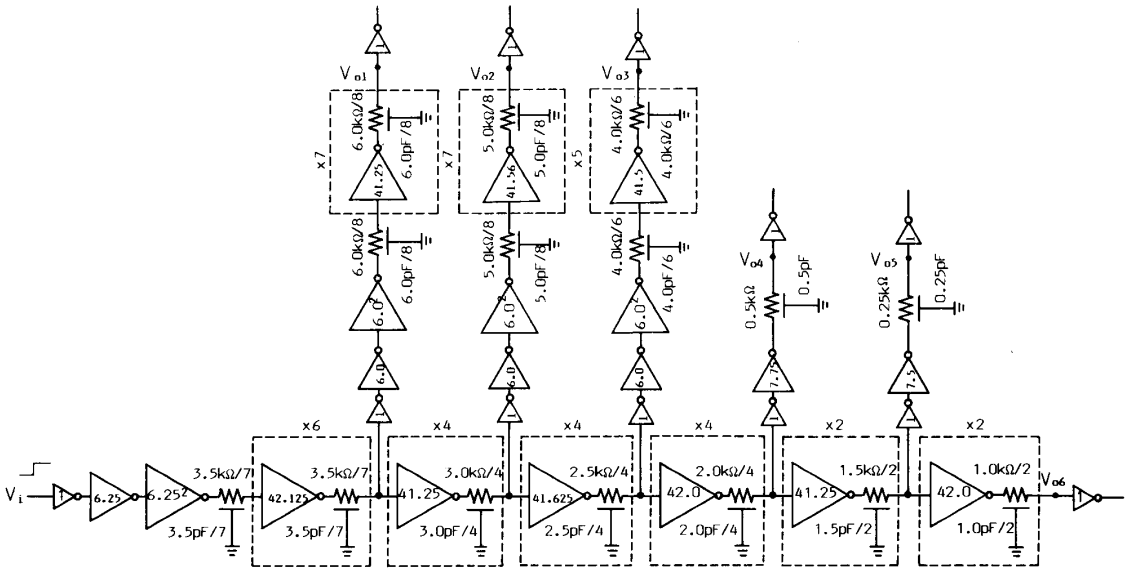


Fig. 6. An example to apply optimal-size repeaters with cascaded input drivers to CMOS inverters with *RC* tree interconnection network where the unit-size CMOS inverter has the minimum W/L ratios which are 2.4 μm/1.2 μm and 1.2 μm/1.2 μm for PMOSFET and NMOSFET, respectively.

B. Speed-Improvement Techniques in RC Tree Interconnection Networks

The previous four driving schemes used in an *RC* interconnection line can also be applied to the *RC* tree interconnection networks. For simplicity, here we only demonstrate the scheme of optimal-size repeaters with cascaded input drivers. Applying this scheme to an interconnection tree, the design guidelines are as follows:

1) apply the developed delay model to determine the maximum-delay path and its connected branches;
2) to reduce the *RC* loads due to the *RC* branches connected to the maximum-delay path, optimal-size repeaters with cascaded input drivers are used to drive these *RC* branches;
3) to reduce the total pair delay time along the maximum-delay path, all the *RC* branches along the maximum-delay path except the leftmost one and those not connected to the maximum-delay path are driven by optimal-size repeaters;
4) the leftmost branch along the maximum-delay path is driven by optimal-size repeaters with cascaded input drivers.

As an example, the delay of an interconnection tree is to be reduced through the above design guidelines. The resultant driver/repeater scheme is shown in Fig. 6 where the number and the sizes of drivers/repeaters are determined from the developed program to reduce the delay. Table IV shows the calculated and the simulated pair delay time before and after applying the speed improvement techniques. It can be seen that pair delay time can be improved by more than an order of magnitude.

TABLE IV
THE CALCULATED AND THE SIMULATED PAIR DELAY IN FIG. 6

OUTPUT	Data Type	Original Interconnection Tree	Adding Drivers/Repeaters
V_{o1}	THEORY	448	29.54
	SPICE	410	31.25
	ERROR	+9.3%	-5.5%
V_{o2}	THEORY	515	32.56
	SPICE	522	36.75
	ERROR	-1.3%	-11.4%
V_{o3}	THEORY	540	35.85
	SPICE	564	40.35
	ERROR	-4.3%	-11.2%
V_{o4}	THEORY	532	32.78
	SPICE	554	36.95
	ERROR	-4.0%	-11.3%
V_{o5}	THEORY	537	35.20
	SPICE	560	40.10
	ERROR	-4.1%	-12.2%
V_{o6}	THEORY	541	34.51
	SPICE	566	38.65
	ERROR	-4.4%	-10.7%

V. Conclusion and Discussion

Physical delay models for 1.5-μm CMOS inverters with *RC* tree interconnection networks have been successfully developed. The CPU time of delay calculations is over two orders of magnitude faster than that of SPICE simulations. The maximum relative error of the delay model is only 15%.

Based upon the developed delay models, the four speed improvement techniques [2], and the BFS [9] optimization method, an experimental program has been constructed to determine the suitable number and the sizes of drivers/repeaters in each technique from the given logic-gate sizes and interconnection structures. It is shown that a tapering factor of 4–8 in cascaded input drivers can obtain a lower delay than a tapering factor of e. Moreover, a small number of drivers/repeaters with large sizes is more efficient in reducing the interconnection delay. Among the four speed improvement techniques, the technique of optimal-size repeaters with cascaded input drivers can lead to the lowest delay. It is also shown that the developed program can determine the number and the sizes of drivers/repeaters more accurately than the formulas in [2].

In future work, the delay model of CMOS inverters with interconnection trees will be generalized to other CMOS logic gates. The design of driving schemes will also be generalized to those gates and those cases with various constraints other than the minimum delay.

References

[1] K. C. Saraswat and F. Mohammedi, "Effect of scaling of interconnections on the time delay of VLSI circuits," *IEEE Trans. Electron Devices*, vol. ED-29, Apr. 1982.

[2] H. B. Bakoglu and J. D. Meindl, "Optimal interconnection circuits for VLSI," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 903–909, May 1985.

[3] R. J. Antinone and G. W. Brown, "The modeling of resistive interconnects for integrated circuits," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 200–203, Apr. 1983.

[4] M. I. Elmasry, "Interconnect delays in MOSFET VLSI," *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 585–591, Oct. 1981.

[5] T. M. Lin and C. W. Mead, "Signal delay in general RC network," *IEEE Trans. Computer-Aided Design*, vol. CAD-3, pp. 331–349, Oct. 1984.

[6] J. L. Wyatt, Jr. and Q. Yu, "Signal delay in RC meshes, trees and lines," in *Proc. IEEE Int. Conf. Computer Aided Design*, (Santa Clara, CA), Nov. 1984, pp. 15–17.

[7] J. L. Wyatt, Jr., "Monotone sensitivity of nonlinear nonuniform RC transmission lines, with application to timing analysis of digital MOS integrated circuits," *IEEE Trans. Circuits Syst.*, vol. CAS-32, pp. 28–33, Jan. 1985.

[8] J. L. Wyatt, Jr., "Signal delay in *RC* mesh networks," *IEEE Trans. Circuits Syst.*, vol. CAS-32, pp. 507–510, May 1985.

[9] Q. Yu, J. L. Wyatt, Jr., C. Zukowski, H. N. Tan, and P. O'Brien, "Improved bounds on signal delay in linear RC models for MOS interconnect," in *Proc. IEEE Int. Symp. Circuits Syst.*, (Kyoto, Japan), June 1985, pp. 903–906.

[10] J. Rubinstein, P. Penfield, Jr., and M. A. Horowitz, "Signal delay in *RC* tree networks," *IEEE Trans. Computer-Aided Design*, vol. CAD-2, pp. 202–211, July 1983.

[11] T. Sakurai, "Approximation of wiring delay in MOSFET LSI," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 418–426, Aug. 1983.

[12] L. A. Glasser, "The analog behavior of digital integrated circuits," in *Proc. 18th Design Automation Conf.*, 1981, pp. 603–612.

[13] C. Y. Wu and M. C. Shiau, "A new interconnection delay model considering the effects of short-channel logic gates," in *Proc. IEEE Int. Symp. Circuits Syst.*, June 1988, pp. 2847–2850.

[14] M. C. Shiau and C. Y. Wu, "The signal delay in interconnection lines considering the effects of small-geometry CMOS inverters," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 420–425, Mar. 1990.

[15] M. D. Matson and L. A. Glasser, "Macromodeling and optimization of digital MOS VLSI circuits," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, no. 4, pp. 659–678, Oct. 1986.

[16] N. Hedenstierna and K. O. Jeppson, "CMOS circuit speed and buffer optimization," *IEEE Trans. Computer-Aided Design*, vol. CAD-6, no. 2, pp. 270–281, 1987.

[17] M. D. Matson, "Optimization of digital MOS VLSI circuits," Mass. Inst. Technol., Cambridge, VLSI Memo. 84-213, Nov. 1984.

[18] L. A. Glasser and L. P. J. Hoyte, "Delay and power optimization in VLSI circuits," in *Proc. 21st Design Automation Conf.*, June 1984, pp. 529–535.

[19] G. V. Reklaitis, A. Ravindran, and K. M. Ragsdell, *Engineering Optimization Methods and Applications*. New York: Wiley, 1984, pp. 116–117.

[20] A. Vladimirescu and S. Liu, "The simulation of MOS integrated circuits using SPICE2," Electronic Res. Lab., Univ. California, Berkeley, Memo. UCB/ERL-M80/7, Oct. 1980.

[21] C. Y. Wu and J. S. Hwang, "A new autosizing algorithm for CMOS combinational logic circuits," in *Proc. Int. Symp. VLSI Technology, Systems and Applications*, May 1989, pp. 242–246.

[22] C. Y. Wu and J. S. Hwang, "Physical timing models of small-geometry CMOS inverters and multi-input NAND/NOR gates and their applications," *Solid-State Electron.*, vol. 32, pp. 449–467, 1989.

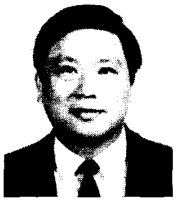
[23] C. Y. Wu, J. S. Hwang, and C. C. Chang, "An efficient timing model for CMOS combinational logic gates," *IEEE Trans. Computer-Aided Design*, vol. CAD-4, pp. 636–650, Oct. 1985.

[24] C. Y. Wu and M. C. Shiau, "General and efficient timing models for CMOS AND-OR-INVERTER and OR-AND-INVERTER gates," to be published in *IEEE Trans. Computer-Aided Design*.

[25] D. Bertsekas, *Constrained Optimization and Lagrange Multiplier Methods*. New York: Academic, 1982.

[26] D. Luenberger, *Introduction to Linear and Nonlinear Programming*. Reading, MA: Addison-Wesley, 1984.

[27] C. Mead and M. Rem, "Minimum propagation delays in VLSI," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 773–775, Aug. 1982.



Chung-Yu Wu (S'76–M'76) was born in Chiayi, Taiwan, Republic of China, on May 31, 1950. He received the B.S. degree from the Department of Electrophysics, and the M.S. and Ph.D. degrees from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, Republic of China, in 1972, 1976, and 1980, respectively.

During 1975–1976 he studied ferroelectric films on silicon and their device applications. During 1976–1979 he engaged in the development of integrated differential negative resistance devices and their circuit applications, with support from the National Electronics Mass Plan (Semiconductor Devices and Integrated Circuit Technologies) of the National Science Council. From 1980 to 1984 he was an Associate Professor at the Institute of Electronics, National Chiao-Tung University. During 1984–1986 he was an Associate Professor in the Department of Electrical Engineering, Portland State University, Portland, OR. Presently he is a Professor in the Department of Electronics Engineering and the Institute of Electronics, National Chiao-Tung University. His research interests have been in device modeling, integrated-circuit technologies, semiconductor memories, analog integrated circuits, digital integrated circuits, and computer-aided circuit design.

Dr. Wu is a member of Eta Kappa Nu and Phi Tau Phi.

Ming-Chuen Shiau was born in Nantour, Taiwan, Republic of China. He received the B.S. and M.S. degrees in electrical engineering from National Chiao-Tung University, Hsinchu, Taiwan, Republic of China, in 1983 and 1985, respectively. Currently, he is working toward the Ph.D. degree at the Institute of Electronics, National Chiao-Tung University. His research concerns computer-aided circuit design and MOS timing analysis and synthesis.