國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

類比電路中之n型金氧半導體場效電晶體元件汲極電流低頻雜訊之探討

Investigation of Drain Current Flicker Noise in Analog n-MOSFETs

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摘要

CMOS 元件技術具有較低成本、高製程整合度、以及低功率的優點；但在類比電路的應用中，卻有一主要缺點，及其汲極電流低頻雜訊過大。為了將金氧半導體場效電晶體成功的運用在類比電路中，元件設計者必須徹底了解低頻雜訊的物理來源。

首先，吾人將先針對金氧半導體場效電晶體元件中汲極電流低頻雜訊的熱載子效應作徹底研究。吾人發現，因熱載子效應的影響，在元件氧化層中會行成局部的氧化層電核累積，此種不均勻的氧化層電核分布，將會造成通道臨界電壓分布的不均勻，此即為造成雜訊衰減的主要原因。除此之外，吾人也提供一簡單之兩區域模型使讀者更加了解我們所提的現象。

接下來，吾人將探討在 0.13μm CMOS 製程中，pocket implantation 製程對於金氧半導體場效電晶體汲極電流低頻雜訊之影響。吾人研究結果顯示，pocket implantation 製程將會嚴重的衰減低頻雜訊特性，其原因如下，因為 pocket implantation 的影響，在元件通道中的臨界電壓之分布已為不均勻。吾人同時提供一兩區域低頻雜訊模型來描述此 pocket implantation 對於元件低頻雜訊的影響。在我們提供的模型中，所有參數均由元件量測資料中萃取出來，無任何可隨意調整之參數。此外，根據此模型模擬之結果與量測資料非常吻合。基於相同的

理論基礎，吾人可以利用元件低頻雜訊的量測，萃取特殊 ONO 記憶體元件介電層中之載子儲存分布，此分布之資料為記憶體電路設計之重要資訊。

再者，吾人同時使用 2-D 元件模擬軟體 (MEDICI) 來驗證不均勻的元件通道臨界電壓分布對於元件低頻雜訊之影響。吾人在模擬時，利用改變基底電壓與 pocket doping profile，來驗證通道載子分布不均勻時，對低頻雜訊之影響，其結果與吾人所提之兩區域低頻雜訊模型預測結果相同。

最後，吾人探討在超薄氧化層 (15Å) 金氧半導體場效電晶體元件中低頻雜訊的物理來源。根據研究結果，吾人提出一種由 valence band tunneling 所導致之低頻雜訊來源。在 strong inversion 的情形下，valence band 中的電子將穿透超薄氧化層，並在 valence band 中留下電洞，如此一來，造成電子電洞的不平衡，並導致電子與電洞的 quasi Fermi-level 分開。所以，在超薄氧化層元件中之低頻雜訊來源為電子與電洞在 interface traps 中 recombination 所產生之 generation/recombination 雜訊。我們同時分析 time-domain 中的雜訊，即所謂 random telegraph signal，其結果與我們所提出之低頻雜訊來源相符合。

Investigation of Drain Current Flicker Noise in Analog n-MOSFETs

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Abstract

CMOS technology is superior in its low cost, high integration, and low power; nevertheless, there is a major drawback in analog applications. The MOSFETs are so noisy although so called “analog low noise” fabrication process is used. Apart from white thermal noise, MOSFETs are notorious for flicker noise in the low frequency range. So as to improve the MOS circuit’s dynamic range and get better circuit performance, a device designer has to understand the physical origin of flicker noise.

First of all, the hot carrier degradation mechanisms of drain current flicker noise in analog n-MOSFETs are investigated. From our observation, the non-uniform threshold voltage distribution generated by local oxide charges after stressing could give rise to series flicker noise degradation. A simple two-region flicker noise model can be used to give better understanding of this behavior.

Next, pocket implantation effect on drain current flicker noise in 0.13μm CMOS process based high performance analog n-MOSFETs is investigated. Our result shows that pocket implantation will significantly degrade device low-frequency noise primarily because of non-uniform threshold voltage distribution along the channel. An analytical two-region flicker noise model to account for a pocket doping effect is proposed. In our model, the local

threshold voltage and the width of the pocket implant region are extracted from measured reverse short channel effect and the oxide trap density is extracted from a long-channel device. Good agreement between our model and measurement result is obtained without other fitting parameters. In addition, non-uniform threshold voltage distribution along the channel resulting from CHE programming in special ONO charge storage cells would increase drain current flicker noise. Based on the same concept of two-region model, one can extract programming charge distribution in NROM memory devices from noise measurement.

Then, we use a two-dimensional device simulator, MEDICI, to simulate the effect of channel carrier distribution variation on flicker noise. The substrate bias and pocket doping profile is changed to verify the relation between channel carrier distribution and drain current flicker noise. The results show good agreement with the analytical model prediction.

Finally, low frequency flicker noise in analog n-MOSFETs with 15Å gate oxide is investigated. A new noise generation mechanism resulting from valence band electron tunneling is proposed. In strong inversion condition, valence-band electron tunneling from Si substrate to poly-gate takes place and results in the splitting of electron and hole quasi Fermi-levels in the channel. The excess low frequency noise is attributed to electron and hole recombination at interface traps between the two quasi Fermi-levels. Random telegraph signal due to capture of channel electrons and holes is characterized in a small area device to support our model.

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List of Symbols

Chapter 2

S_{Id}	drain current noise power spectrum density
S_{Vg}	input referred gate voltage noise power spectrum density
μ_{eff}	carrier mobility
μ_{ox}	mobility limited by oxide charge scattering
μ_n	mobility limited by other scattering mechanisms
q	electron charge
N	channel carrier density
E_x	horizontal electric field
N_t	total trap density
N_{ox}	oxide trap density
N_{it}	interface trap density
N_d	trap density in the depletion region
C_i	inversion layer capacitance
C_d	depletion layer capacitance
C_{it}	interface trap capacitance
α	scattering coefficient
f_t	trap occupation function (factor)
E_{fn}	electron quasi-Fermi level
τ	trap time constant
τ_0	time constant at the interface
γ	attenuation coefficient
g_m	transconductance
G	channel conductance

Chapter 3

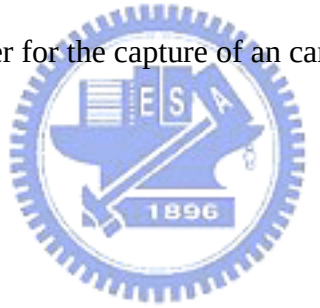
S_{id}/I_d^2	normalized noise power spectrum density
L_{eff}	effective channel length
V_t	threshold voltage

Chapter 4

L_p	Pocket Length
D_c	channel doping concentration

Chapter 5

f_c	corner frequency
ΔE_b	energy barrier for the capture of an carrier
E_t	trap energy



Chapter 1
Introduction

The CMOS technology, which possesses the advantage of low cost, high integration, and low power, is finding more and more important applications in the area of analog IC. The capability of integrating analog and digital circuits on the same chip is crucial to the production of high-performance MOS integrated circuits such as telecommunication circuits [1-1]. Nevertheless, there is a major drawback in analog applications. Compared with bipolar transistors, MOS transistors are so noisy, especially in the low frequency region where the flicker noise dominates [1-2]. Flicker noise will affect the signal-to-noise ratio (SNR) in operational amplifiers and in A/D and D/A converters. Phase noise of VCO originating from flicker noise is another concern for RF applications [1-3]. In order to reduce low frequency noise in analog devices, the physical origin of flicker noise in today's CMOS devices should be further explored.

Studies of hot carrier degradation on low frequency noise indicate that this quantity is extremely sensitive [1-4,5,6]. E. Simoen showed that the increase of the noise spectral density follows a $t^{0.3}$ power law dependence with stress time in a 0.7μm CMOS technology [1-5] and that the RTS amplitude of a particular oxide trap increased after hot carrier stress in 0.5μm×0.5μm p-MOSFETs [1-6]. Some studies show that the low-frequency 1/f noise is correlated with oxide-trapped charge and that the high-frequency 1/f noise is correlated with interface traps [1-7]. Following up these hot carrier degradation effects, we proposed that non-uniform threshold voltage distribution induced by local oxide charges plays an important role on the dominant source of flicker noise.

As we know, pocket implantation in a CMOS process is a key method to reduce the sub-threshold leakage in logic devices. However, it has some drawbacks, such as the increase of drain-substrate coupling, poor Early voltage, lower high frequency output resistance [1-8]

and increased non-linearity [1-9], in analog applications. Recent study has shown that pocket implantation will also degrade drain current flicker noise. The new structure, such us single pocket or asymmetric channel structure [1-8,10] and epitaxial channel MOSFETs [1-11,12], is proposed to have better noise performance because of the elimination of pocket implantation process. Although some researchers attributed the increase of noise to additional oxide trap creation by pocket implantation [1-12], the real cause of pocket implantation induced noise degradation is still not clear.

The purpose of this study is to investigate pocket implantation effect on flicker noise in n-MOSEFTs with various pocket doses and device dimensions. It is suggested that the pocket implantation will change the threshold voltage distribution, so that the noise characteristic is also affected. An analytical flicker noise model taking into account a pocket doping effect will be proposed. In addition, this analytical model can be included into circuit simulators, such as HSPICE, to improve the model accuracy.

In addition to the analytical noise model, we use a two-dimensional device simulator, MEDICI, to simulate the effects of channel carrier distribution on flicker noise. The substrate bias and pocket implantation doping profile is changed to verify the relation between channel carrier distribution and drain current flicker noise.

From now on, the origin of low frequency flicker noise in MOSFETs with relatively thick gate oxides has been extensively studied. A unified noise model [1-13] based on oxide charge tunnel trapping and de-trapping has been adopted. The carrier number and mobility fluctuation induced from trapped oxide charges is thought to be the source of flicker noise. In addition, some studies showed that the low frequency noise may result from charge emission and capture at interface traps in weak inversion condition or in the very high frequency regime of noise power spectral density [1-14]. As gate oxide thickness is scaled into direct tunneling domain, oxide trap density should be much reduced. In addition, channel electrons would likely tunnel through an ultra-thin gate oxide directly without being captured by oxide

traps. However, the low frequency noise in ultra-thin oxide CMOS devices still exhibits a significant level [1-15,16]. The traditional oxide charge tunnel trapping and de-trapping concept seems no longer suitable to explain the noise behavior in ultra-thin oxide MOSFETs.

In addition to the discussions of flicker noise on frequency domain, the time domain presentation of low frequency noise is known as random telegraph signal (RTS) and has been studied in past decades [1-17,18,19,20]. Due to a single charge trapping and de-trapping in a small area device, RTS exhibits two levels. The upper level corresponds to an empty trap, i.e., no electron occupation, and the duration of time is denoted by τ_H. The lower level corresponds to an electron occupied state and is denoted by τ_L. In many cases, τ_H corresponds to the time it takes to capture a carrier, while carrier release (emission) from traps governs τ_L [1-21]. In the ultra-thin oxide case, we will study the τ_L and τ_H behavior instead of the noise behavior in frequency domain. Based on the time domain analysis, a new noise generation model for ultra-thin oxide device is proposed.

Organization of This Thesis

This thesis is organized into six chapters.

In chapter 1, we give a brief introduction about this thesis.

In chapter 2, the hot carrier effect on drain current flicker noise is investigated. Conventional 0.18μm technology CMOS devices and a special ONO charge storage cell are used in this work. The channel length from 0.22μm to 2μm, and a 10μm gate width is used. An ONO cell with 90Å effective gate oxide thickness, 0.58μm channel length, and 1 μm gate width is used to verify the source of degradation. Maximum substrate and gate current stress, FN stress, and double side maximum gate current stress are performed in these devices. All the noise data are measured at linear region. The input referred noise power spectral density (S_{VG}) is used as a monitor of noise degradation, which provides fairer comparison.

In Chapter 3, the pocket implantation effect on drain current flicker noise is investigated.

The input/output n-MOSFETs of a 0.13μm CMOS technology is used in this work. The I/O devices have a 5.8nm gate oxide, a gate length from 0.22μm to 10μm, and a gate width of 10mm. Two pocket implant doses were used. Each noise measurement data point represents an average of 3 to 10 devices. The normalized noise power spectrum density (S_{id}/I_d^2) is chosen as a monitor of drain current noise, which is considered to be a fair index because of the normalization to the drain current. In addition, charge pumping measurement is performed to characterize oxide (interface) trap density for different pocket implant splits.

In Chapter 4, the simulation of the effect of inversion carrier distribution variation on flicker noise through different applied substrate bias and pocket doping profile are investigated. The two-dimensional device simulator, MEDICI, is used.

In Chapter 5, the low frequency noise in a 15Å gate oxide n-MOSFET is investigated. The electron trapping and de-trapping times (τ_H and τ_L) are characterized from RTS in a small area n-MOSFET. The normalized noise power spectral density (S_{id}/I_d^2) is measured as a monitor of drain current noise, which is considered as a fair index because of the normalization to the drain current. In addition, the RTS time constants and noise power spectral density in n-MOSFETs with 33Å gate oxide are also characterized for comparison. The drain bias in RTS and noise measurement in this study is 0.1V to ensure a uniform charge distribution in the channel. Finally, a new noise source due to valence band electron tunneling will be proposed to explain the observed noise behavior.

Conclusions are finally made in Chapter 6.

Chapter 2
Hot Carrier Effect on Drain Current Flicker Noise in Analog n-MOSFETs

2.1 Introduction

Because of its low cost, high integration, and low power, the CMOS technology is finding more and more important applications in the area of analog IC. The capability of integrating low-cost analog circuits and high-speed digital circuits on the same chip is crucial to the production of high-performance MOS integrated circuits such as A/D converters and telecommunication circuits [2-1]. Nevertheless, there is a major drawback in analog applications. Compared with bipolar transistors, MOS transistors are so noisy, especially in the low frequency region where the flicker noise dominates [2-2]. In order to optimize low frequency noise performance in analog applications, the need for further understanding of the noise characteristics of MOS transistors is obvious. In addition, hot carrier degradation is known to significantly increase the flicker noise amplitude of MOS transistors in the linear mode [2-3]. So as to improve the MOS circuit's performance, a device designer has to understand the physical origin of flicker noise.

At present, there are two major theories to explain the physical origins of flicker noise in MOS transistors. One is the number fluctuation theory based on the McWhorter's charge trapping model; the other is the bulk mobility fluctuation theory based on Hooge's hypothesis [2-2]. C. Hu et al. have developed a unified flicker noise model, which incorporated both the number fluctuation and the correlated surface mobility fluctuation mechanisms [2-1,4,5]. Several studies had shown that the flicker noise in n-MOSFETs is dominated by the number fluctuation mechanism [2-6,7,8]; based on this mechanism, the input referred gate voltage noise power spectrum density (S_{Vg}) would be independent of gate bias. On the other hand, the noise is mainly due to the mobility fluctuation mechanism, which suggests gate voltage

dependence in S_{Vg}, in p-MOSFETs [2-9,10].

Studies of hot carrier degradation on the low frequency noise indicate that this quantity is extremely sensitive [2-11,12,13]. E. Simoen showed that the increase of the noise spectral density follows a $t^{0.3}$ power law dependence with stress time in a 0.7μm CMOS technology [2-14]. In addition, the RTS amplitude of a particular oxide trap increased after hot carrier stress in 0.5μm×0.5μm p-MOSFETs [2-13]. Some studies show that the low frequency noise is correlated with oxide-trapped charge and that the high-frequency noise is correlated with interface traps [2-14]. Toshiba Corp. proposed an epitaxial channel MOSFET (without halo implantation) for lower interface traps and better flicker noise performance [2-15].

The purpose of this study is to find out the real source responsible for hot carrier degradation through various kinds of stresses. We will show that non-uniform threshold voltage distribution, which is induced from local oxide charge generation after stressing, along the channel will cause noise degradation. Using this concept as a basis, a device designer can optimize the flicker noise performance through substrate engineering.

2.2 Basic Theory of Flicker Noise

Flicker noise was observed in vacuum tubes by Johnson in 1925 and interpreted by Walter Schottky in 1926. In the present day, flicker noise is found in all active devices [2-2], such as Si BJT, MOSFET, and SiGe HBT. The power spectrum density of such noise often varies as f^{-1} with energy concentrated at low frequencies. Therefore, it is called 1/f noise or low frequency noise as well.

In the past, there were two major models to explain the mechanisms of flicker noise in MOSFETs- McWhorter's [2-16] charge trapping model and Hooge's empirical relation [2-17], but no connection between two models had been explored. According to the carrier number fluctuation theory proposed by McWhoter, flicker noise is explained by the fluctuation of the channel free carrier due to the random capture and emission by the oxide traps near the

Si-SiO_2 interface. Either the surface potential fluctuation resulting from charge fluctuation or the charge exchange between the channel and the oxide traps induces the current fluctuation. Mathematically each oxide trap near the interface provides Lorentzian [2-4] spectrum. For the uniform oxide trap distribution in the bandgap, each Lorentzian component adds up to 1/f noise spectrum. On the other way, the mobility fluctuation theory based on Hooge's hypothesis regards the flicker noise as a consequence of bulk mobility fluctuation; moreover, the fluctuation of bulk mobility in MOSFETs is caused by phonon population through phonon scattering [2-18]. However either theory couldn't verify the noise generation mechanism independently and completely. At present, C. Hu's Unified Flicker Noise Model [2-1,4] has become the main stream to elucidate the origin of flicker noise. They develop I-V and noise models to incorporate both number fluctuation theory and bulk mobility fluctuation theory.

The unified flicker noise model combined number and mobility fluctuation models through the I-V model [2-1,4]. The drain current I_d in strong inversion for a MOSFET with width W and length L is given by

$$I_d = W\mu_{eff} qNE_x \tag{2-1}$$

where μ_{eff} is the carrier mobility, and q is the electron charge, N is the number of channel carriers per unit area, and E_x is the horizontal electric field. In addition, consider a section of channel with width W and length Δx. Fluctuation in the amount of trapped oxide charge will induce correlated fluctuations in the carrier number and mobility. The result fractional charge in the local drain current can be expressed as

$$\delta I_d = I_d \left(\frac{1}{\Delta N} \frac{\delta \Delta N}{\delta \Delta N_t} \pm \frac{1}{\mu_{eff}} \frac{\delta \mu_{eff}}{\delta \Delta N_t} \right) \delta \Delta N_t \tag{2-2}$$

where N_t is the number of occupied traps per unit area, $\Delta N = NW\Delta x$ and $\Delta N_t = N_t W \Delta x$. The sign in front of the mobility fluctuation term in Eq. (2-2) is chosen according to whether the trap is neutral or charged when filled. The ratio of the fluctuations in the carrier number to fluctuations in occupied trap number, $R = \delta\Delta N / \delta\Delta N_t$, is close to unity at strong inversion.

The ratio R can be expressed as

$$R = \frac{\delta \Delta N}{\delta \Delta N_t} = -\frac{N}{N + N_{ox} + N_{it} + N_d} \tag{2-3}$$

where N_{ox} ,N_{it} and N_d are oxide trap density, interface trap density and trap density in the depletion region. Through the relation C=βqN, a general expression for R is

$$R = -\frac{C_i}{C_i + C_{ox} + C_{it} + C_d} \tag{2-4}$$

where C_i, C_d and C_{it} are inversion layer, depletion layer, and interface trap capacitances.

To evaluate $\delta \mu_{eff} / \delta \Delta N_t$, we need to know the relation between carrier mobility and oxide charge density, which based on Matthiessen's rule:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_n} + \frac{1}{\mu_{ox}} = \frac{1}{\mu_n} + \alpha N_t \tag{2-5}$$

where μ_{ox} is the mobility limited by oxide charge scattering, μ_n is the mobility limited by other scattering mechanisms, and α is the scattering coefficient with a typical value of $2 \times 10^{-15} Vs$. On the basis of Eq. (2-5) it can be shown that

$$\frac{\delta \mu_{eff}}{\delta \Delta N_t} = -\frac{\alpha \mu_{eff}^2}{W \Delta x} \tag{2-6}$$

Substituting Eq. (2-4) and Eq. (2-6) into Eq. (2-2) yields

$$\delta I_d = -I_d \left(\frac{1}{N} \pm \alpha \mu_{eff} \right) \frac{\delta \Delta N_t}{W \Delta x} \tag{2-7}$$

Hence, the power spectrum density of the local current fluctuations is

$$S_{\Delta Id}(x, f) = \left(\frac{I_d}{W \Delta x} \right)^2 \left(\frac{1}{N} \pm \alpha \mu_{eff} \right)^2 S_{\Delta Nt}(x, f) \tag{2-8}$$

where $S_{\Delta Nt}(x, f)$ is the power spectral density of the mean-square fluctuations in the number of occupied traps over the area WΔx. According to the conventional theory of number fluctuations, $S_{\Delta Nt}(x, f)$ is given by

$$S_{\Delta Nt}(x,f)=\int_{E_v}^{E_c}\int_0^W\int_0^{t_{ox}} 4N_t(E,x,y,z)\Delta x f_t(1-f_t)\frac{\tau(E,x,y,z)}{1+\omega^2\tau(E,x,y,z)^2}dzdydE \quad (2\text{-}9)$$

where $N_t(E,x,y,z)$ is the distribution of the traps in the oxide and over the energy, $\tau(E,x,y,z)$ is the trapping time constant, $ft=\left[1+\exp(E-E_{fn})/kT\right]^{-1}$ is the trap occupancy function, E_{fn} is the electron quasi-Fermi level, is the angular frequency, t_{ox} is the oxide thickness, and E_c-E_v is the silicon bandgap. In order to evaluate the integral in Eq. (2-9), we make two assumptions: 1) The oxide traps have a uniform spatial distribution near the interface, consequently, $N_t(E,x,y,z)=N_t(E)$. 2) The probability if an electron penetrating into the oxide decreases exponentially with the distance from the interface, thus the trap time constant is given by

$$\tau=\tau_0(E)\exp(\gamma z) \quad (2\text{-}10)$$

where $\tau_0(E)$ is the time constant at the interface, and γ is the attenuation coefficient of the electron wave function in the oxide with a value of $10^8 cm^{-1}$ [2-1,4]. Since $f_t(1-f_t)$ in Eq. (2-9) behaves like a delta function around the quasi-Fermi level, traps level around E_{fn} is the major contribution to the integral. Therefore $N_T(E)$ can be approximated by $N_T(E_{fn})$ and $f_t(1-f_t)$ can be replace by $-kTdf_T/dE$. Then solve the integration yields

$$S_{\Delta Nt}(x,f)=N_t(E_{fn})\frac{kTW\Delta x}{\gamma f} \quad (2\text{-}11)$$

The total drain current noise power spectrum turns out to be

$$S_{Id}(f)=\frac{1}{L^2}\int_0^L S_{\Delta Id}(x,f)\Delta x dx=\frac{kTI_d{}^2}{\gamma f WL^2}\int_0^L N_t(E_{fn})\left[\frac{1}{N(x)}\pm\alpha\mu\right]^2 dx \quad (2\text{-}12)$$

where L is the channel length. Eq. (2-12) is the basic expression of the unified flicker noise model. In strong inversion with very low drain voltage, the carrier density is uniform along the channel. Then Eq. (2-12) simplifies as

$$S_{Id}(f)=\frac{kTI_d{}^2}{\gamma f WL}\left(\frac{1}{N}+\alpha\mu\right)^2 N_t(E_{fn}) \quad (2\text{-}13)$$

Due to the fluctuation of the drain current, the input referred noise power is given by

$$S_{Vg}(f) = \frac{S_{id}(f)}{g_m^{\ 2}} = \frac{kTq^2}{\gamma f WLC_{OX}^{\ 2}}(1+\alpha\mu N)^2 N_T(E_{fn}) \qquad (2\text{-}14)$$

where g_m is the transconductance ($g_m = \delta I_d / \delta V_G = W\mu C_{ox} V_d / L$) and V_d is the drain voltage.

2.3 Device Information and Experimental Setup

Conventional 0.18μm technology CMOS devices and a special ONO charge storage cell are used in this work. In order to emphasize the oxide traps storage capability, CMOS devices with 65Å gate oxide thickness are used. According to a statistical evaluation of the flicker noise, devices with too small area may have a large fluctuation range [2-19], so the channel length from 0.22μm to 2μm, and a 10μm gate width is used. An ONO cell with 90Å effective gate oxide thickness, 0.58μm channel length, and 1μm gate width is used to verify the source of degradation. Maximum substrate and gate current stress, FN stress, and double side maximum gate current stress are performed in these devices. All the noise data are measured at linear region. The input referred gate voltage noise power spectrum density (S_{Vg}) is used as a monitor of noise degradation, which provides fairer comparison. The flicker noise measurement system (100Hz~100KHz) involves a HP4155 semiconductor parameter analyzer, a BTA9603 FET noise analyzer, and a SR780 network signal analyzer. All measurement is controlled automatically through GPIB cards by a computer program named BTA-NoisePro. The block diagram of noise measurement system is shown in Fig. 2-1.

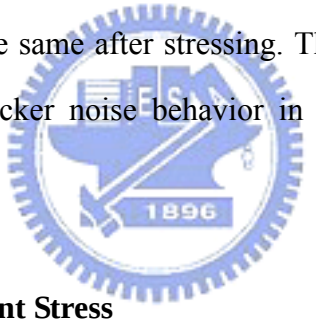
2.4 Flicker Noise Degradation under Different Stress Condition in Analog n-MOSFETs

The source responsible for drain current flicker noise degradation in n-MOSFETs is studied. When the device suffers from hot carrier effects, interface states or oxide traps will be generated. We will verify how they alter the noise behavior by various stress modes. The S_{Vg}

is used as a monitor of degradation before and after stressing. Compared to S_{Id}, it provides fairer comparison as the drain current is normalized. All noise measurements are biased at low gate voltage in the linear region to assure that number fluctuation mechanism dominates the noise behavior.

2.4.1 Maximum Substrate Current Stress

Fig. 2-2 shows the n-MOSFET (W/L=10μm/0.34μm, t_{ox}=65Å) Id-Vg characteristics before and after hot-carrier stress. The stress bias is at Vg=1.64V, Vd=3V, where the maximum substrate current (I_b) occurs. For maximum I_b stress, both interface states and neutral electron traps are generated in the oxide, with the former being dominant. The subthreshold swing degradation is then due to the generation of interface state. The S_{Vg} measured at Vd=0.1V and Vg=1.0V before and after maximum I_b stress are shown in Fig. 2-3. However, the noise remains the same after stressing. That is, the generation of fast interface states will not degrade the flicker noise behavior in the frequency range from 100Hz to 100kHz.



2.4.2 Maximum Gate Current Stress

Fig. 2-4 shows the n-MOSFET (W/L=10μm/0.34μm, t_{ox}=65Å) Id-Vg characteristics before and after hot-carrier stress. The stress bias is at Vg=4.7V, Vd=4.7V, where the maximum gate current (I_g) occurs. After stressing, there are some local electron traps generated near the drain side. The threshold voltage shifts about 0.3V after stressing. The S_{Vg} measured at Vd=0.1V and Vg=1.0V before and after maximum I_g stress are shown in Fig. 2-5. Comparably, the noise increases about an order in the entire range of measurement frequency. These local oxide-trapped charges, which generate non-uniform threshold voltage distribution along the channel, are the source responsible for hot-carrier degradation of flicker noise.

2.4.3 Fower-Nordheim Stress

Fig. 2-6 shows the n-MOSFET (W/L=10μm/0.34μm, t_{ox}=65Å) Id-Vg characteristics after FN stress (stress bias: Vg=8V). We precisely control the stress time so that the threshold voltage shift remains the same (0.3V) with maximum I_g stress. In addition, the sub-threshold swing slightly degrades. That is, there are uniform electron traps and a little amount of interface states generating along the channel. The S_{Vg} measured at Vd=0.1V and Vg=1.0V before and after maximum I_g stress are shown in Fig. 2-7. The noise slightly increases after FN stress. This can be explained by the increase of oxide traps density, so that the probability of trapping/de-trapping increases. And we will show that the uniform oxide-trapped charges will not alter the noise latter.

2.5 Flicker Noise Degradation under Different Stress Condition in Special ONO Charge Storage Cells

In order to make sure the dominant noise degradation source is the non-uniform oxide-trapped charges, a special n-type ONO charge storage cell, which doesn't generate extra oxide traps after hot-carrier stress, is used. The ONO cell structure is shown in Fig. 2-8(a), and the channel length is 0.58μm, the gate width is 1μm, and the gate oxide thickness is 90Å.

2.5.1 Fower-Nordheim Programming

Fowler-Nordheim (FN) program is used for this cell to create uniform nitride charges with negligible generation of oxide traps. Fig. 2-9 shows the ONO cell (W/L=1μm/0.58μm) Id-Vg characteristics after FN programming (program bias: Vg=15V, others 0V). The parallel shift in Fig. 2-9 is attributed to negative trapped charge in the nitride layer. Fig. 2-10 shows the results of noise degradation after FN programming. The noise is measured at linear operation regime. As can be seen, the threshold voltage shifts about 0.5V, and the noise remains just the same as the fresh device. This implies that the generation of uniform electron

traps along the channel doesn't degrade the S_{Vg}.

2.5.2 Maximum Gate Current Programming

Channel hot electron injection and band-to-band hot hole injection are utilized for programming and erasing to generate local oxide charges. Fig. 2-11 shows the ONO cell (W/L=1μm/0.58μm) Id-Vg characteristics after maximum I_g programming (program bias: Vd=4V, Vg=6.5V) and hot hole erasing (erase bias: Vd=7V, Vg=-3V). Fig. 2-12 illustrates the noise behavior after the generation of non-uniform threshold voltage distribution. The noise is measured at linear operation regime. After hot-carrier programming, the noise increases about an order, and the noise turns back after drain-side erasing. So far, it is proved by ONO cell that non-uniform threshold voltage distribution caused from local oxide-trapped charge can seriously enhance the flicker noise.

2.6 Two-Region Model of Noise Degradation

In order to clarify the local oxide charge enhanced flicker noise degradation, the non-uniform threshold voltage method, also called two-region method, is used [2-20]. The effects of channel non-uniformity can be simplified as a MOSFET with two regions of different threshold voltage [2-21]. For the case of maximum I_g stress in an n-MOSFET as shown in Fig. 2-8(b), the higher threshold region (Region 1) near the drain is due to channel-hot electron stress and the lower one (Region 2) is the rest of channel.

The drain voltage and the corresponding noise power for a two-region MOSFET can be modeled as [2-22]

$$V_d = V_1 + V_2 \tag{2-15}$$

thus

$$S_{Vd(stress)} = S_{V1} + S_{V2} \tag{2-16}$$

Converting the drain voltage fluctuations in Eq. (2-16) into drain current (I_d) fluctuations, we

have

$$\frac{S_{Id(stress)}(f)}{G^2} = \frac{S_{I1}(f)}{G_1^{\,2}} + \frac{S_{I2}(f)}{G_2^{\,2}} \tag{2-17}$$

where $G_i = \frac{\mu_i Q_i W}{L_i}$ is the channel conductance associated with region i, $G = (G_1^{-1} + G_2^{-1})^{-1}$ is the total current conductance and $I_d=I_1=I_2$ is the drain current. Assume that the transconductance is constant along the channel, thus the input referred noise power is given by

$$\frac{S_{Vg(stress)}(f)}{G^2} = \frac{S_{Vg1}(f)}{G_1^{\,2}} + \frac{S_{Vg2}(f)}{G_2^{\,2}} \tag{2-18}$$

Because of the higher threshold voltage in Region 1 than in Region 2, it follows that

$$\frac{Q_2}{L_2} >> \frac{Q_1}{L_1} \Rightarrow G_2 >> G_1 \tag{2-19}$$

Consequently,

$$\frac{S_{Vg1}(f)}{G_1^{\,2}} >> \frac{S_{Vg2}(f)}{G_2^{\,2}} \tag{2-20}$$

and

$$G \approx G_1 \tag{2-21}$$

Accordingly, the equivalent total input referred power of the two components can be simplified as

$$S_{Vg(stress)}(f) = S_{Vg_1}(f) \tag{2-22}$$

The noise from Region 1 will dominate, and the total input referred power after maximum I_g stress is given by

$$S_{Vg(stress)}(f) = \frac{kTq^2}{\gamma f C_{OX}^{\,2} W L_1}(1+\alpha\mu_1 N_1)^2 N_{T1}(E_{f1}) \tag{2-23}$$

Comparing with the noise power spectrum in a fresh device., the magnification is given by

$$\frac{S_{Vg(stress)}(f)}{S_{Vg}(f)} \approx \left(\frac{L}{L_1}\right)\left[\frac{N_t(E_{fn1})}{N_t(E_{fn})}\right] \qquad (2\text{-}24)$$

The net result can drastically enhance gate voltage noise due to not only a smaller L_1 but also a large $N_{t1}(E_{f1})$. As a consequence, the non-uniform distribution of the threshold voltage along the channel, such as in maximum I_g stressed device, may enhance serious degradation of the 1/f noise. In contrast, the uniform oxide charge generated by FN stress couldn't cause significant increase of the 1/f noise.

2.7 Summary

The hot carrier degradation mechanisms of drain current flicker noise in analog CMOS devices are investigated. The sources responsible for noise degradation are verified through both submicron CMOS transistors and a special ONO charge storage cell with various kinds of stresses. From our observation, the non-uniform oxide-trapped charges generated by maximum gate current stress could give rise to series flicker noise degradation as the number fluctuation mechanism dominates noise processes, which can be understood through a two-region unified flicker noise model. For n-MOSFETs, the number fluctuation mechanism dominates at low gate bias, so that the noise magnitude seriously increases after hot carrier stressing.

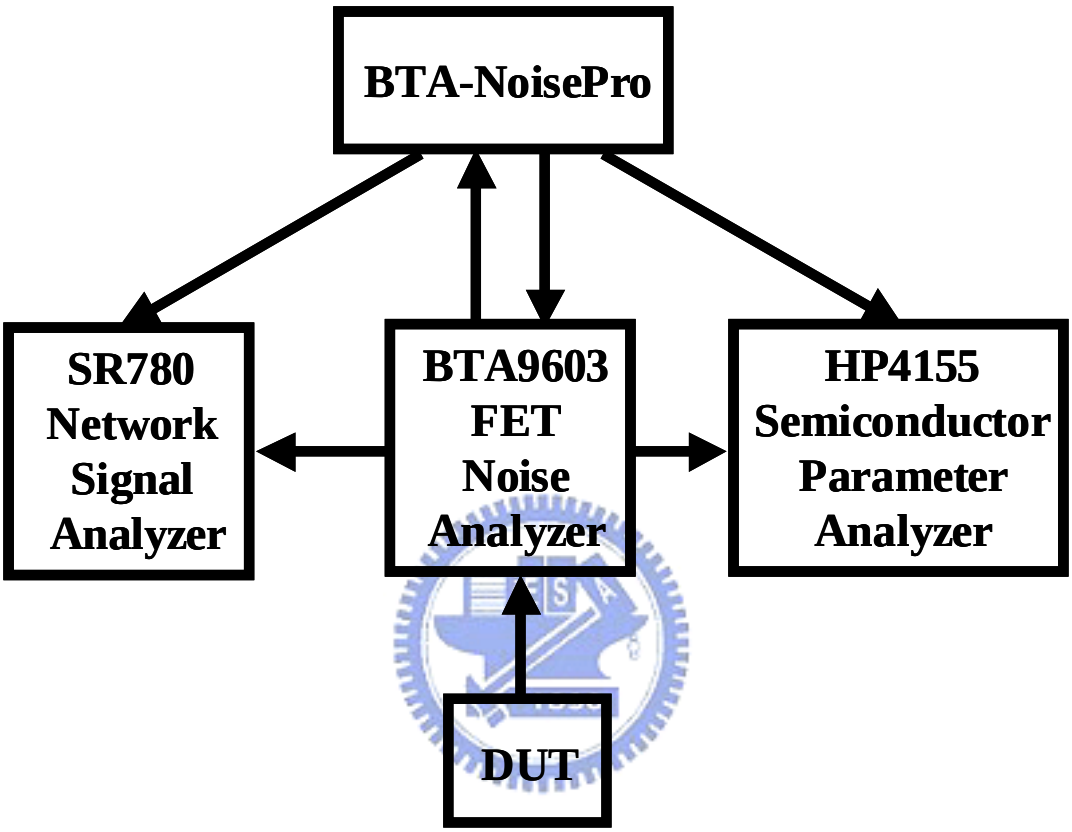


Fig. 2-1 The block diagram of noise measurement system.

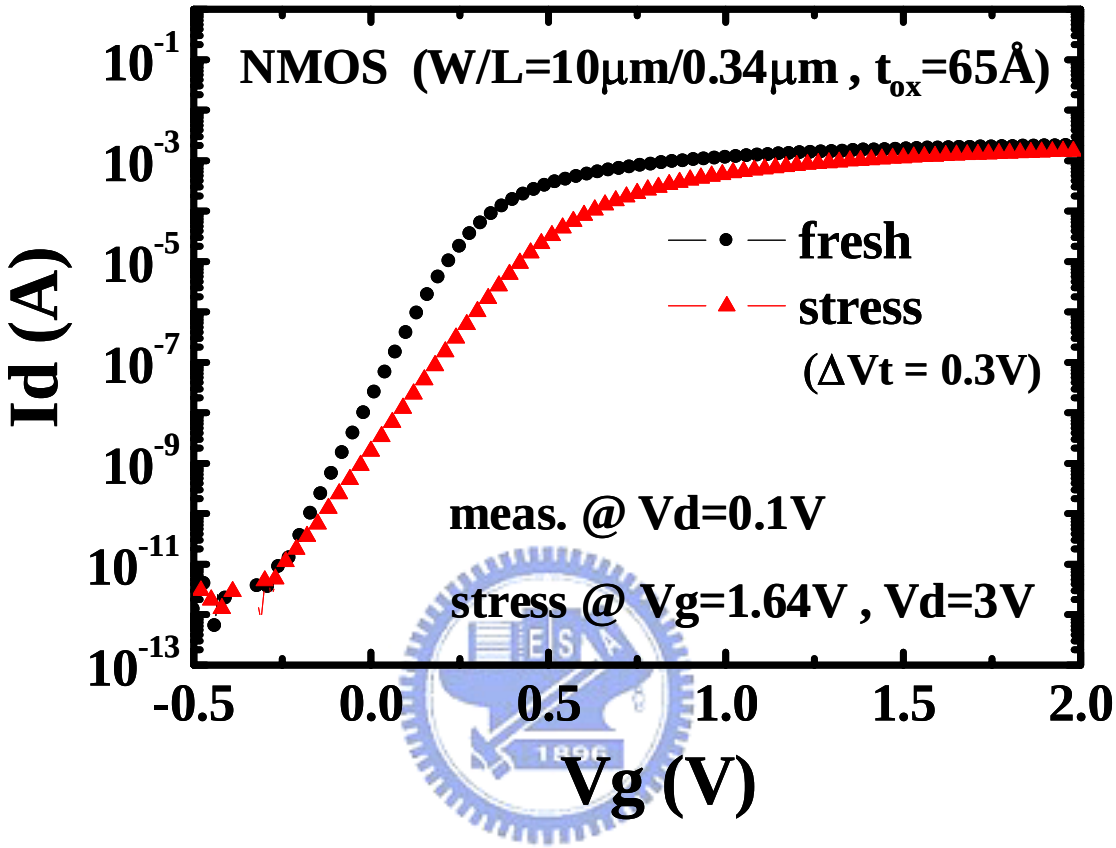


Fig. 2-2 NMOS (W/L=10μm/0.34μm, t_{ox}=65Å) Id-Vg characteristics (measured @ Vd=0.1V) before and after maximum Ib stress (stress bias: Vg=1.64V, Vd=3V).

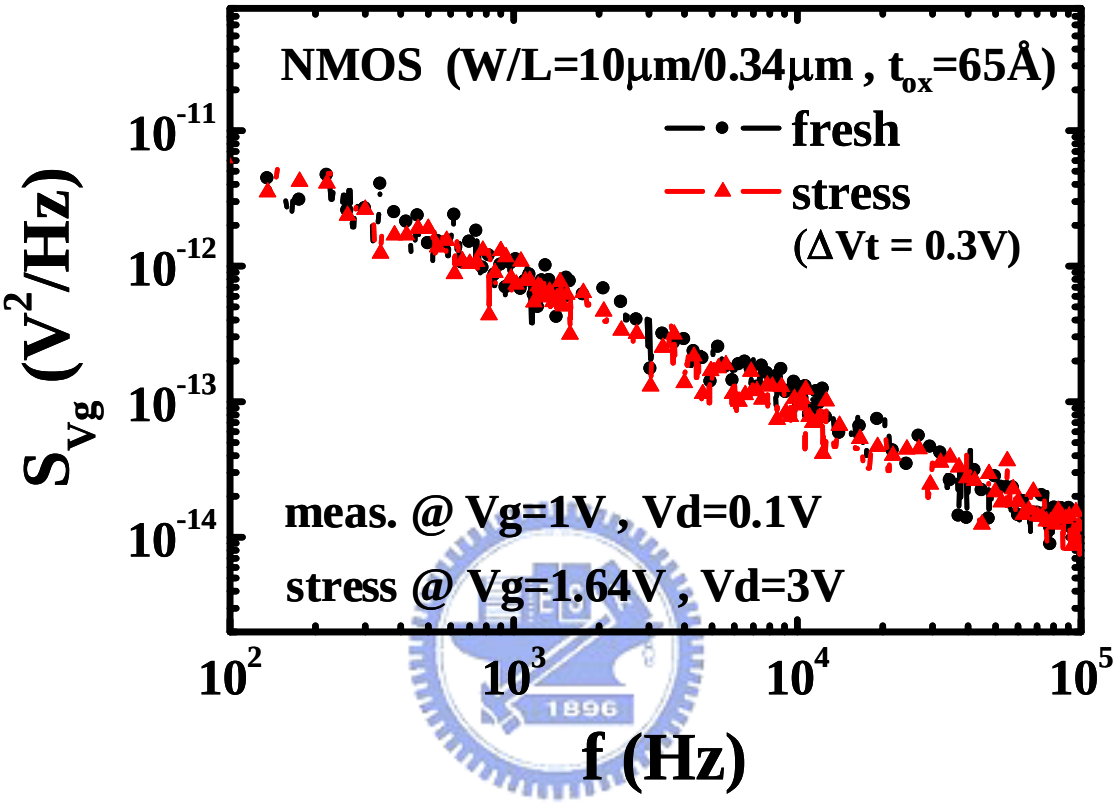


Fig. 2-3 NMOS (W/L=10μm/0.34μm, t_{ox}=65Å) noise characteristics (measured @ Vg=1V, Vd=0.1V) before and after maximum Ib stress (stress bias: Vg=1.64V, Vd=3V).

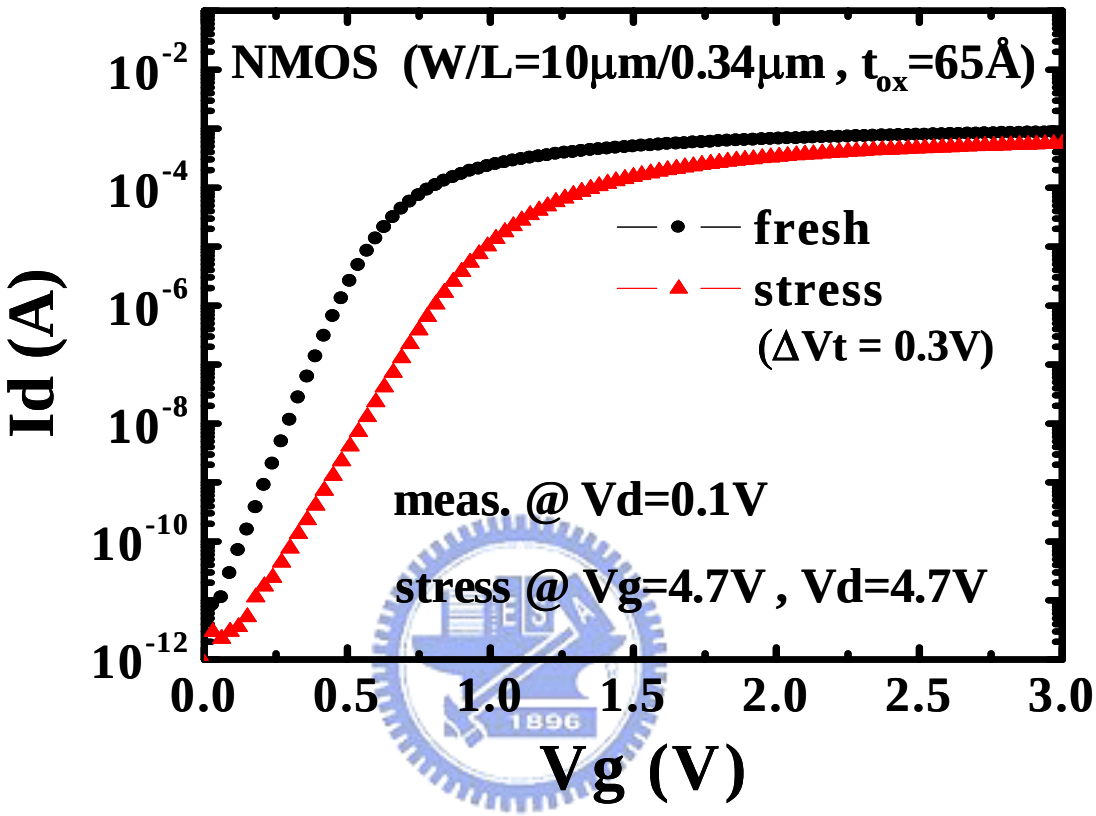


Fig. 2-4 NMOS (W/L=10μm/0.34μm, t_{ox}=65Å) Id-Vg characteristics (measured @ Vd=0.1V) before and after maximum Ig stress (stress bias: Vg=4.7V, Vd=4.7V).

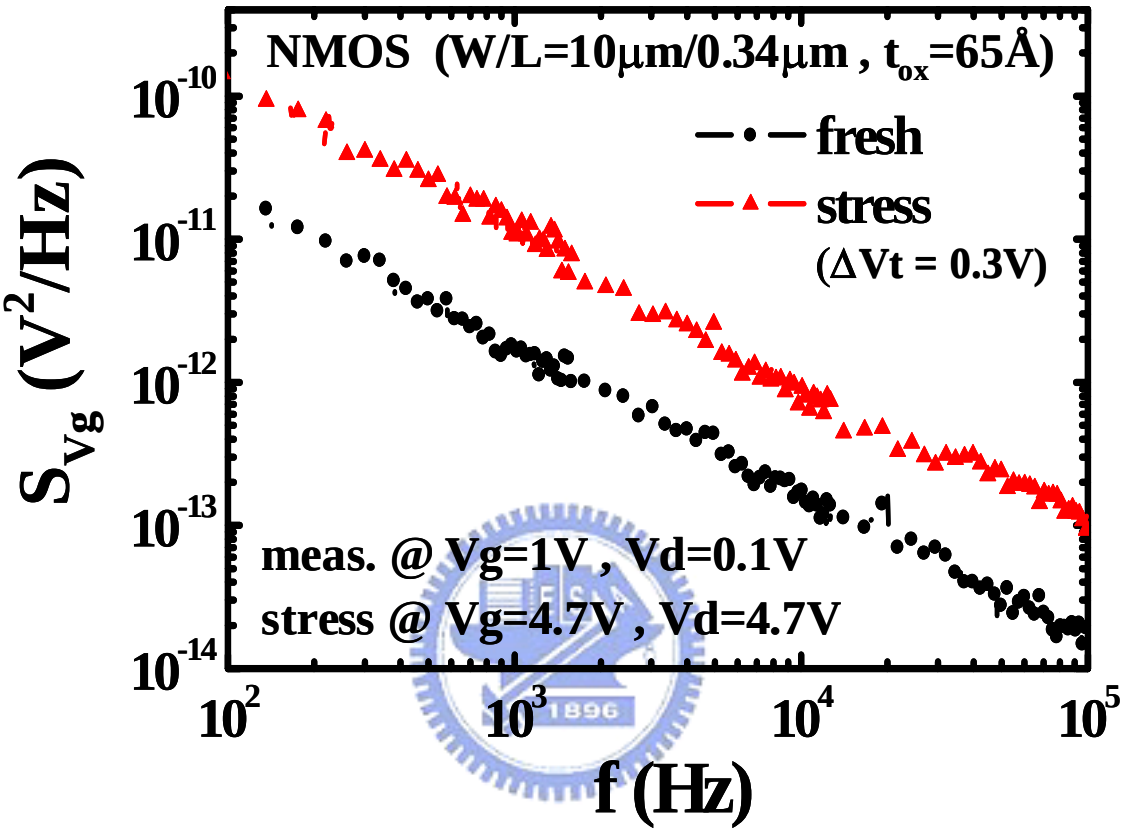


Fig. 2-5 NMOS (W/L=10μm/0.34μm, t_{ox}=65Å) noise characteristics (measured @ Vg=1V, Vd=0.1V) before and after maximum Ig stress (stress bias: Vg=4.7V, Vd=4.7V).

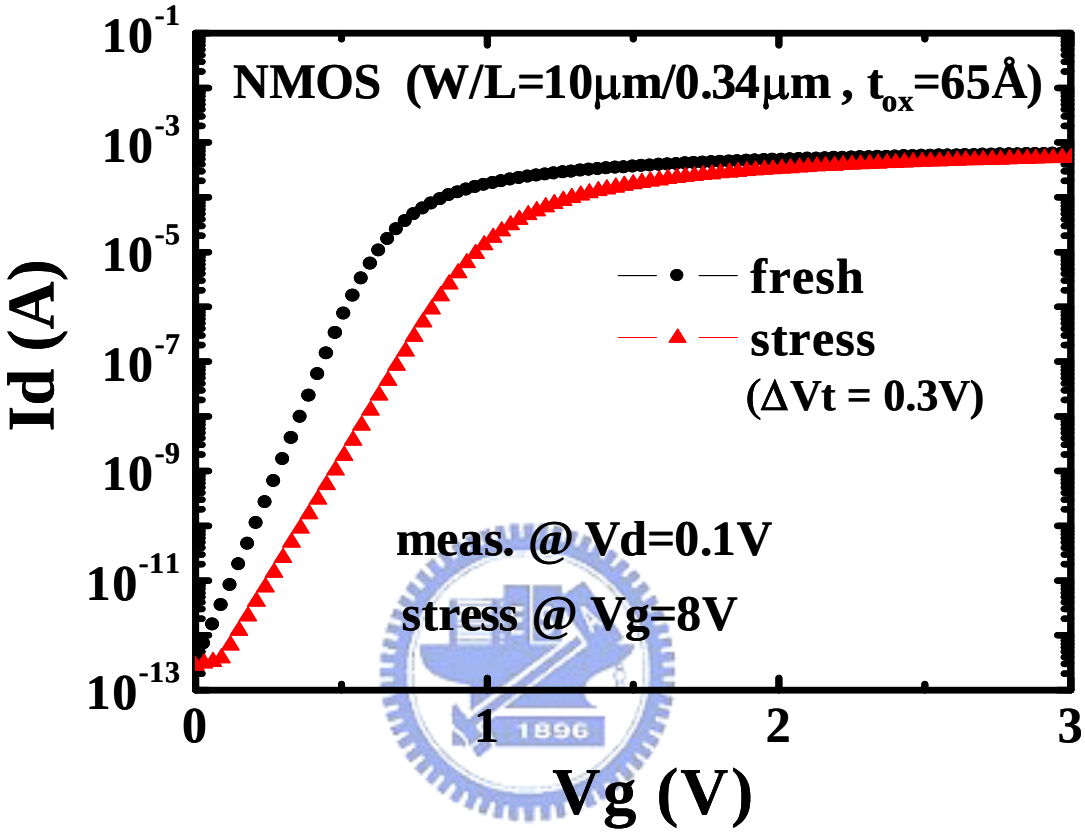


Fig. 2-6 NMOS (W/L=10μm/0.34μm, t_{ox}=65Å) Id-Vg characteristics (measured @ Vd=0.1V) before and after FN stress (stress bias: Vg=8V, others 0V).

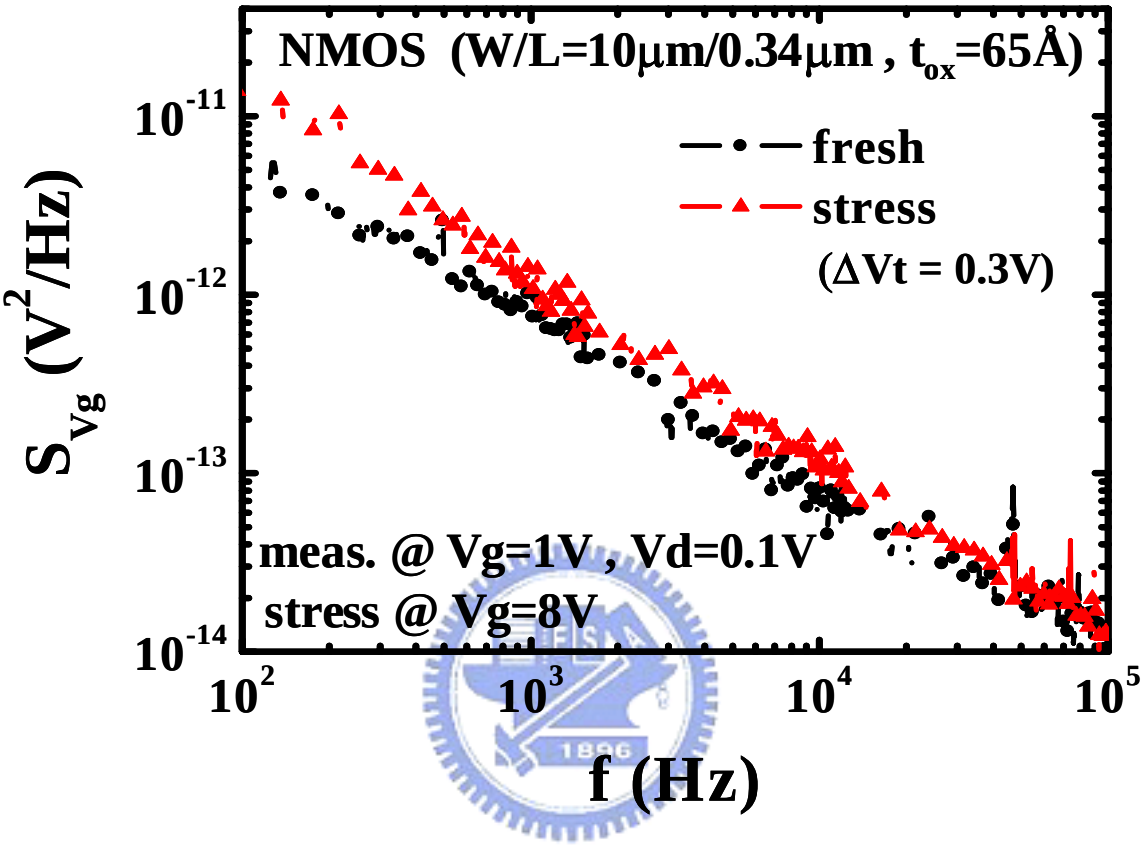
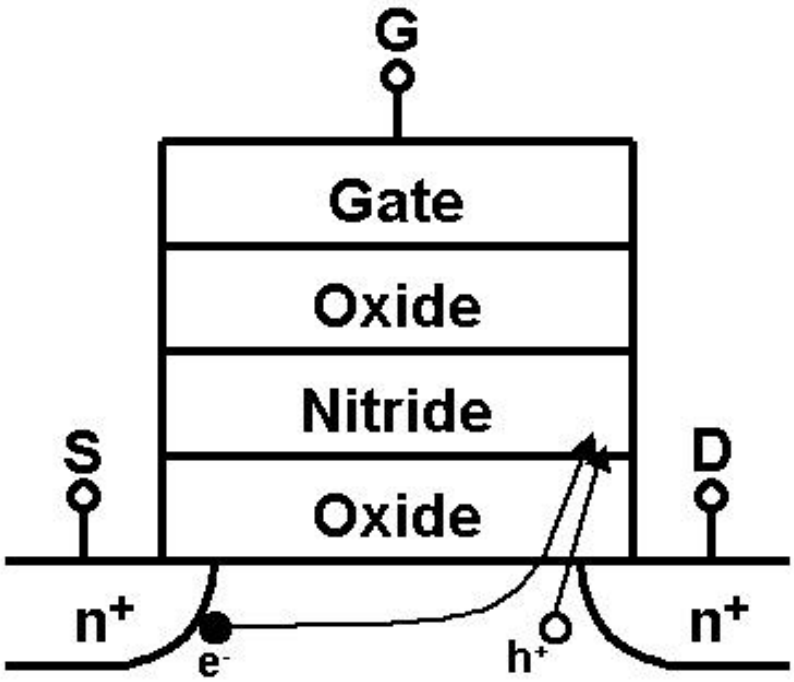
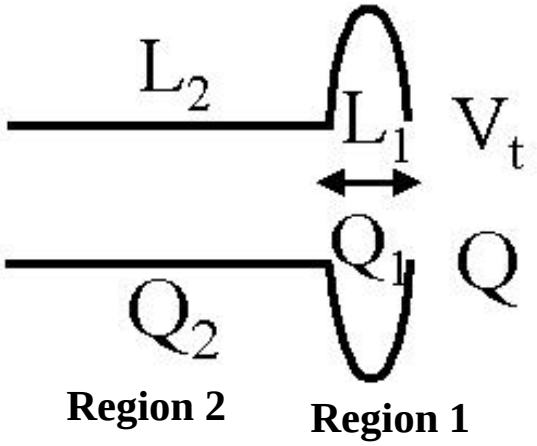


Fig. 2-7 NMOS (W/L=10μm/0.34μm, t_{ox}=65Å) noise characteristics (measured @ Vg=1V, Vd=0.1V) before and after FN stress (stress bias: Vg=8V, others 0V).



(a)



(b)

Fig. 2-8 (a) The diagram of special ONO charge storage cell. (b) The oxide charge and threshold voltage distribution along the channel after hot carrier programming.

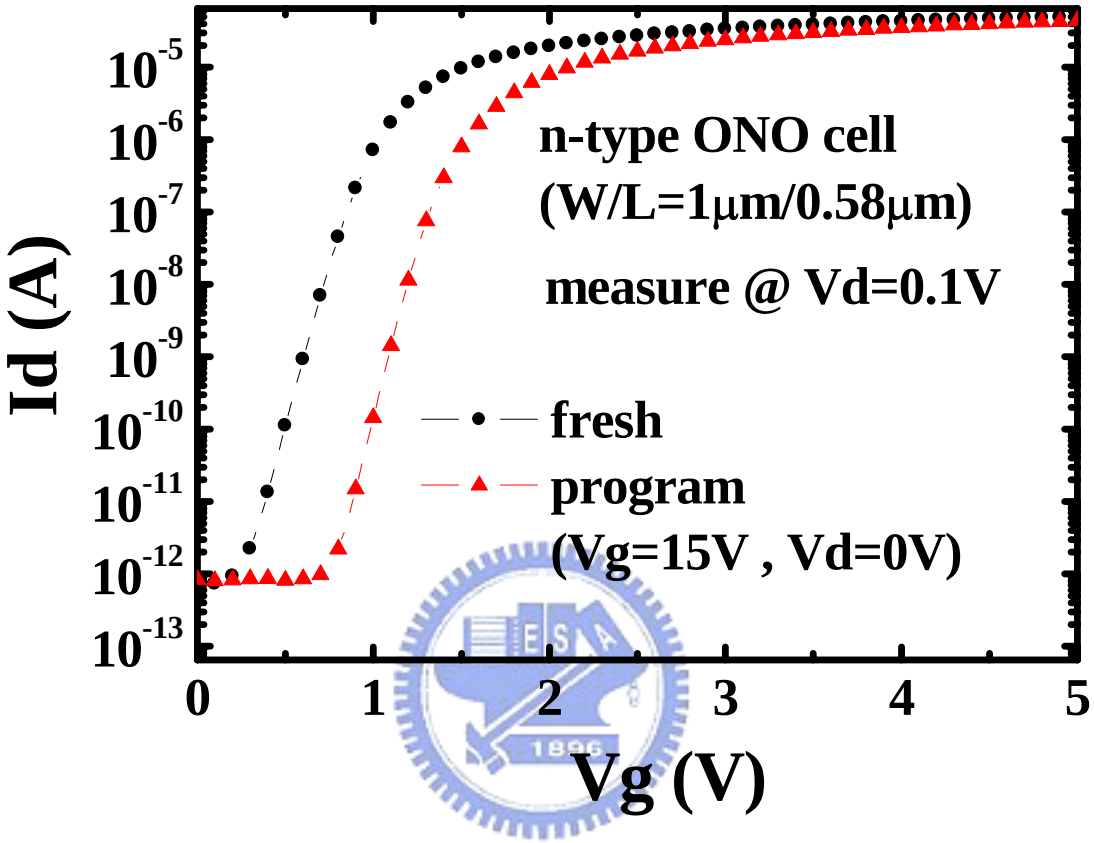


Fig. 2-9 The ONO cell (W/L=1μm/0.58μm) Id-Vg characteristics (measured @ Vd=0.1V) in erase state and FN program state (program bias: Vg=15V).

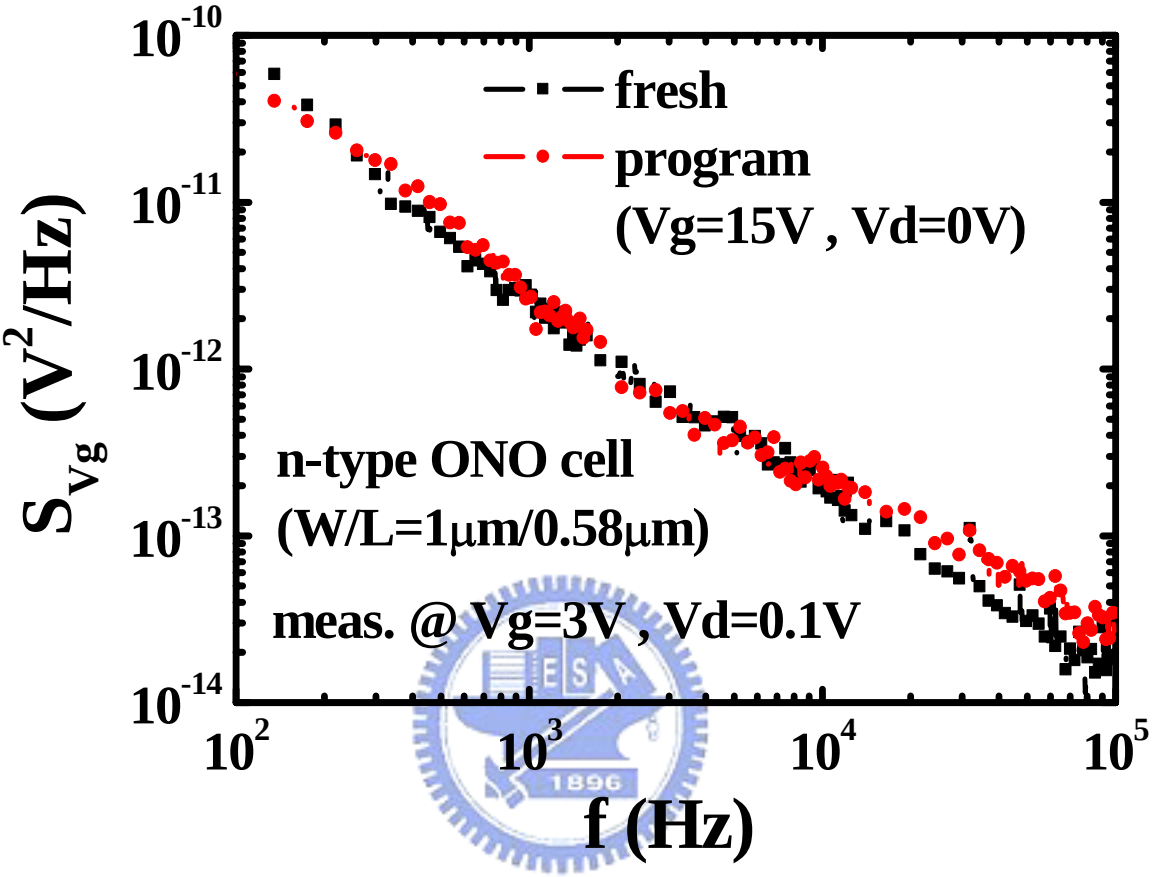


Fig. 2-10 The ONO cell (W/L=1μm/0.58μm) noise characteristics (measured @ Vg=3V, Vd=0.1V) in erase state and FN program state (program bias: Vg=15V).

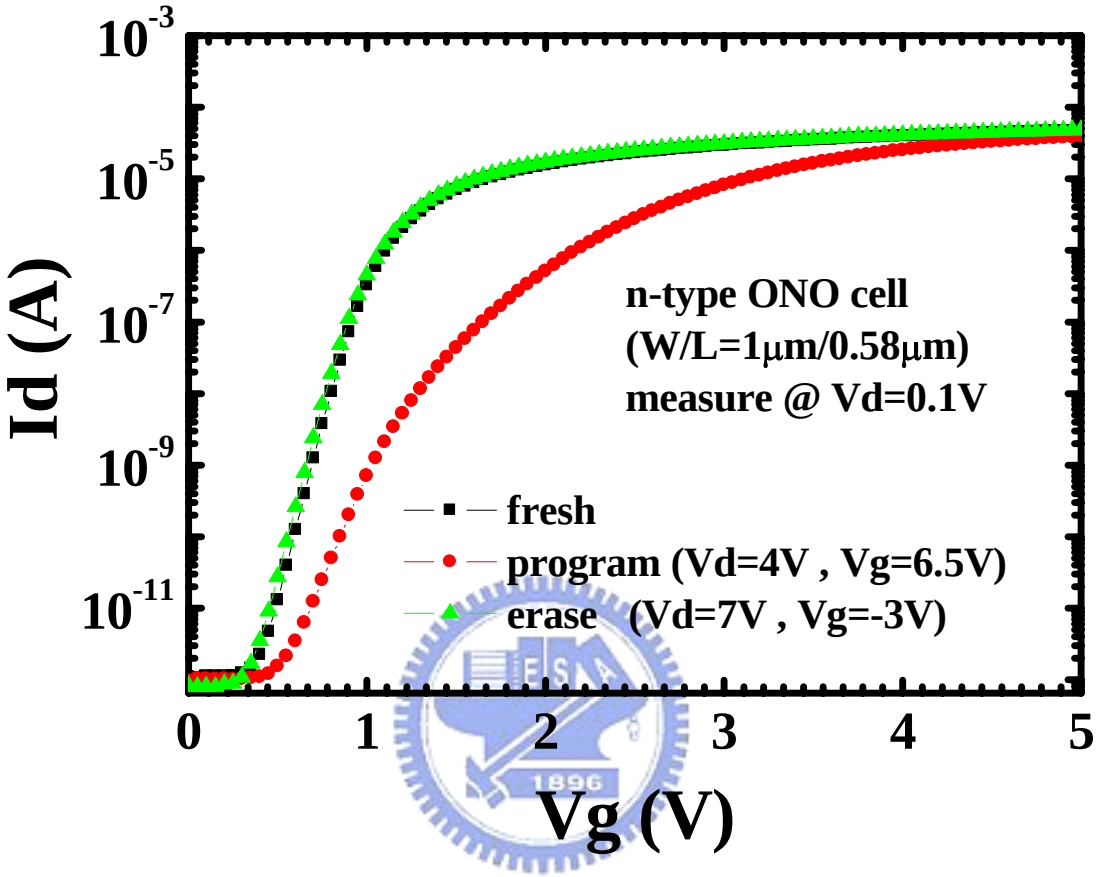


Fig. 2-11 The ONO cell (W/L=1μm/0.58μm) Id-Vg characteristics (measured @ Vd=0.1V) in fresh state, hot carrier program state (program bias: Vd=4V, Vg=6.5V) and erase state (erase bias: Vd=7V, Vg=-3V).

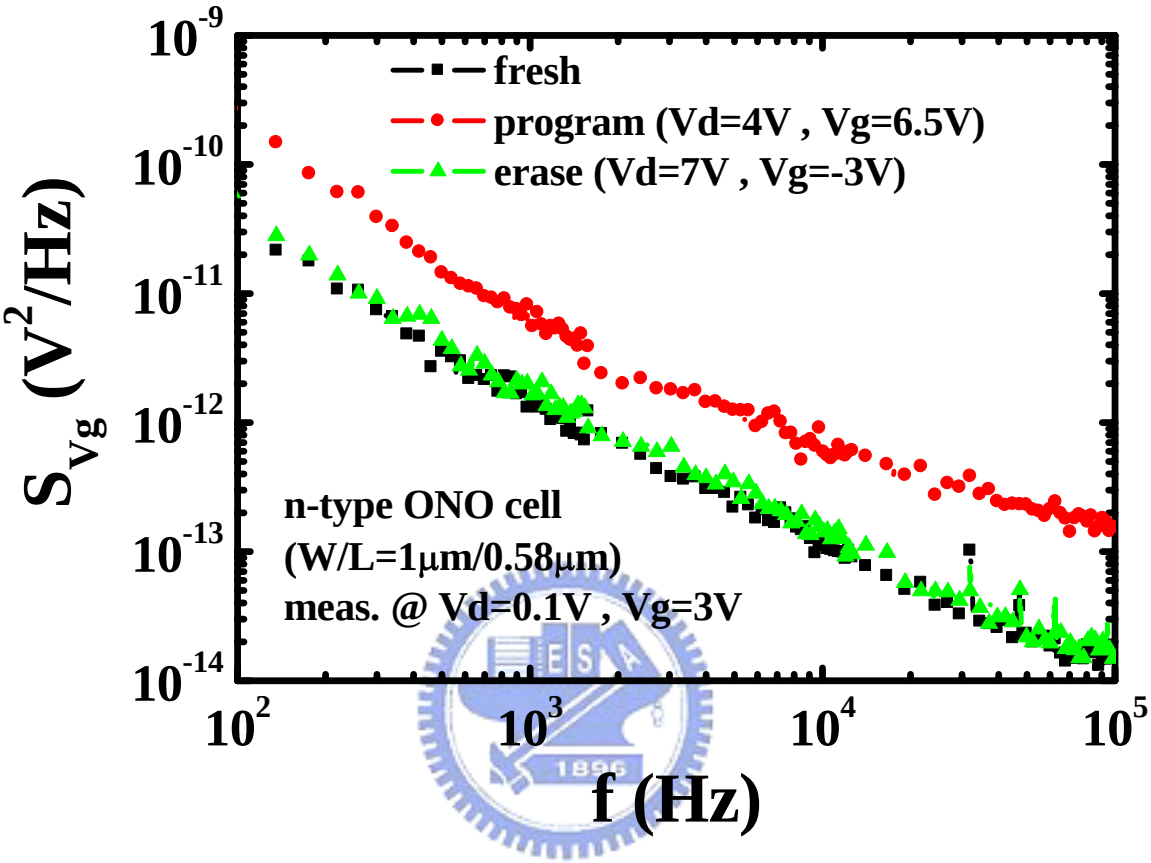


Fig. 2-12 The ONO cell (W/L=1μm/0.58μm) noise characteristics (measured @ Vg=3V, Vd=0.1V) in fresh state, hot carrier program state (program bias: Vd=4V, Vg=6.5V) and erase state (erase bias: Vd=7V, Vg=-3V).

Chapter 3
Pocket Implantation Effect on Drain Current Flicker Noise in Analog n-MOSFETs

3.1 Introduction

The CMOS technology, which possesses the advantage of low cost, high integration, and low power, is finding more and more important applications in the area of analog IC. The capability of integrating analog and digital circuits on the same chip is crucial to the production of high-performance MOS integrated circuits such as telecommunication circuits [3-1]. Nevertheless, there is a major drawback in analog applications. Compared with bipolar transistors, MOS transistors are so noisy, especially in the low frequency region where the flicker noise dominates [3-2]. Flicker noise will affect the signal-to-noise ratio (SNR) in operational amplifiers and in A/D and D/A converters. Phase noise of VCO originating from flicker noise is another concern for RF applications [3-3]. In order to optimize low frequency noise performance in analog applications, a device designer has to understand the physical origin of flicker noise and provide accurate flicker noise model.

As we know, pocket implantation in a CMOS process is a key method to reduce the sub-threshold leakage in logic devices. However, it has some drawbacks, such as the increase of drain-substrate coupling, poor Early voltage, lower high frequency r_o [3-4] and non-linearity [3-5], in analog applications. Recent study has shown that pocket implantation will also degrade drain current flicker noise. The new structure, such us single pocket or asymmetric channel structure [3-4,6] and epitaxial channel MOSFETs [3-7,8], is proposed to have better noise performance because of the elimination of pocket implantation process. Although some researchers attributed the increase of noise to additional oxide trap creation by pocket implantation [3-8], the real cause of pocket implantation induced noise degradation is still not clear.

The purpose of this study is to investigate pocket implantation effects on flicker noise in various gate length n-MOSEFTs. First, the flicker noise behavior for n-MOSEFTs with different pocket implant doses is compared in the linear operation regime. Then, the charge pumping method is also used to verify the cause of noise degradation. It is suggested that non-uniform threshold voltage distribution, which in terms generates non-uniform channel carrier number distribution, caused by pocket implantation is responsible for the noise increasing. Finally, as the number fluctuation mechanism dominates noise behavior in n-MOSFETs, an analytical model based on a non-uniform threshold voltage distribution [3-9,10] is proposed to evaluate noise with different pocket implant doses.

The NROM, a special ONO charge storage cell based on localized charge trapping in a dielectric layer, has been recently proposed in the literature. The localization of the trapped charge is the key factor for 2-bit storing capability of the NROM cell [3-11]. Achieving a correct description of programming charge distribution is essential to prove device functionality and to extrapolate scaling limits of NROM devices. Based on the noise model methodology, the programming charge distribution is extracted from the deviation of flicker noise measured in the linear regime.

3.2 Device Information

0.13μm technology I/O n-MOSFETs with 58Å gate oxide are used in this work. The noise behavior for devices with two large different pocket doses is compared. The channel length from 0.32μm to 10μm, and a 10μm gate width are used. According to a statistical evaluation of the flicker noise, devices with too small area may have a large fluctuation range [3-12], so each data point represents an average of 3 to 10 devices. All noise data are measured in the linear operation regime. The normalized noise power spectrum density (S_{Id}/I_d^2) is used as a monitor of drain current noise, which is considered to be a fair index because of the normalization to the drain current. In addition, charge pumping measurement is

performed to characterize oxide (interface) trap density in different pocket splits. In addition, a special ONO charge storage cell with 90Å effective gate oxide thickness (W/L=0.58μm/0.58μm, 10μm/10μm) is used to extract the programming charge distribution.

3.3 Modeling of Pocket Implantation Effect on Flicker Noise

Fig. 3-1 demonstrates the diagram of an n-MOSFET with pocket implantation. As can be imagined, pocket implantation would induce non-uniform threshold voltage distribution along the channel (shown in Fig. 3-1) and may produce additional oxide traps near the source/drain edge. According to Eq. (3-1), which is illustrated in Chapter 2.2,

$$\frac{S_{id}}{I_d^{\,2}} = \frac{kT}{\gamma f W L_{eff}^{\,2}} \int_0^{L_{eff}} N_t(E_{fn}, x)\left[\frac{1}{N(x)} + \alpha\mu\right]^2 dx \qquad (3\text{-}1)$$

the drain current flicker noise will be affected as the oxide traps distribution ($N_t(E_{fn},x)$) or channel carrier distribution (N(x)) is influenced by the pocket implantation process.

3.3.1 Noise Behavior for Different Pocket Dose

In order to verify the pocket implantation effect on drain current flicker noise, two sets of identical devices only with different pocket doses are used. The higher pocket dose is 2.2 times larger then the lower one. Fig. 3-2 shows the reverse short channel effect (RSCE) for both sets of devices, which is compared to make sure the sufficient of the pocket dose difference. As can be seen, the effective threshold voltage becomes higher when the channel length shrinks. This is caused from pocket implantation induced higher local threshold voltage at the source/drain edge. However, the short channel effect (SCE) becomes dominates as the channel length is smaller than 0.3μm. As can be seen, the raise of threshold voltage induced from RSCE for the higher pocket dose set is about 0.1V, while the lower one is only about 0.05V. Based on this considerably pocket-induced difference, the noise behavior for both sets of devices is compared.

The characteristics of normalized noise power spectrum density (S_{Id}/I_d^2) versus gate overdrive voltage (Vg-Vt, Vt is the device threshold voltage) is used as the monitor of noise behavior, which is considered to be a fair index because of the normalization to the drain current and comparing at the same gate overdrive voltage. Fig. 3-3,4 shows the noise behavior for two different doses. Both long channel (L=10μm) and short channel (L=0.32μm) devices are compared. As mentioned before, the SHE becomes dominant as the channel length is smaller than 0.3μm. Since we focus only on the pocket implantation effect and it is not clear how the SCE affects the drain current flicker noise, so 0.32μm is chosen as the short channel device. The noise is measured at linear operation regime (Vd=0.2V), so that the inversion charge will not affected by the drain bias. All noise data are averaged from 3 to 10 devices until the flicker noise characteristic follows 1/f. In addition, since the noise follows 1/f, the noise data point shown in Fig. 3-3,4 is only at f=100Hz. As can be shown in Fig. 3-3, the noise in the two 10μm devices is almost the same without regard to a considerably different pocket dose. Fig. 3-4 shows the noise in two 0.32μm devices with the same pocket implant split. Unlike the result in the 10mm devices, the higher pocket dose device exhibits much worse noise behavior in the entire range of gate bias. Fig. 3-5 shows the channel length dependence of pocket implant effect on drain current flicker noise. The pocket implant induced noise degradation is larger in a shorter gate length device. As for these devices, the pocket-affected region could take over an important part in the entire cannel region.

3.3.2 Verified by Charge Pumping Method

As mentioned above, the worse noise behavior for higher pocket dose devices may cause from additional oxide traps creation or non-uniform threshold voltage distribution along the channel [3-9,10]. In order to verify whether the pocket implantation process would create additional oxide traps, a charge pumping technique [3-13,14] is used. Fig. 3-6 shows that the oxide (interface) traps density of the two pocket splits is about the same (N_{it} approximates to

1.56×10^{10} at Vg_{high}=0.5V). It is not unimaginable because that the additional oxide traps created from pocket implantation process would be annealed during the latter thermal process. The distinct noise degradation in the higher pocket dose device in Fig. 3-4 therefore cannot be explained simply by implant caused oxide traps creation. Instead, pocket implant will result in a non-uniform threshold voltage distribution along the channel, which should be responsible for noise degradation. A simple analytic model will be illustrated latter to explain non-uniform threshold voltage enhanced noise degradation.

3.3.3 Three-Region Model of Pocket Implant Effect on Flicker Noise

In our model, the channel is divided into three regions, as illustrated in Fig. 3-1. Regions 1 and 3 represent a pocket implant region, where the local threshold voltage (Vt) is increased due to pocket implantation. Region 2 is the rest of the channel region and possesses a lower Vt. As mention above, the number fluctuation mechanism dominates the noise behavior of n-MOSFETs at a relatively low gate overdrive bias. So the mobility fluctuation mechanism can be neglected in Eq. (3-1). In addition, since the oxide (interface) trap density is not affected by the pocket implantation process (shown in Fig. 3-6), it is assumed to be uniform along the channel. Based on these assumptions, Eq. (3-1) can be simplified as follows:

$$\frac{S_{id}}{I_d^{\,2}} \approx \frac{kT}{\gamma f W L_{eff}^{\,2}} \cdot N_t(E_{fn}) \cdot \int_0^{L_{eff}} \frac{1}{N^2(x)} dx \qquad (3\text{-}2)$$

As the local Vt in region 1 and 3 becomes higher due to pocket implantation, the carrier density (N(x)) would be lower in these two regions. Therefore, some parts of the summation term in Eqs. (3-2) would also become higher, and then the normalized noise level would in terms increase. This is not surprised because that the noise (number fluctuation mechanism) would become more sensitive to the variation of carrier numbers as the amount of them is relatively small. In a word, the noise for high threshold region in the channel would be the main source of the drain current flicker noise as the number fluctuation mechanism

dominates.

Based on this concept, the summation term in the noise model can be divided into three regions with their own carrier number density. So Eq. (3-2) can be rewritten as follows:

$$\frac{S_{id}}{I_d^{\,2}} = \frac{kT}{\gamma f W L_{eff}^{\,2}} N_t(E_{fn})\left[\int_{L_1}\frac{1}{N_1^{\,2}(x)}dx + \int_{L_2}\frac{1}{N_2^{\,2}(x)}dx + \int_{L_3}\frac{1}{N_3^{\,2}(x)}dx\right]$$
$$\approx \frac{kTq^2}{\gamma f W L_{eff}^{\,2} C_{ox}^{\,2}} N_t(E_{fn})\left[\frac{L_1}{(V_g - V_{t1})^2} + \frac{L_2}{(V_g - V_{t2})^2} + \frac{L_3}{(V_g - V_{t3})^2}\right] \quad (3\text{-}3)$$

where N_1 and N_3 represent conducting charge density in Region 1 and Region 3, which are modulated by pocket implant dosage. In the long channel devices (L=10μm), the noise component arising from the pocket implantation regions is relatively small. This argument is evident from Fig. 3-3 that the noise is nearly the same for different pocket splits in long channel devices. In other words, the second term in Eq. (3-3), i.e., L_2 region, is dominant in a "long" channel device. From the measured noise and threshold voltage in a long channel device, the oxide trap density, $N_t(E_{fn})$, can be extracted. The result is shown in Table 3-1. The measurement and calculation results of noise level for long channel devices with two different pocket dose are show in Fig. 3-7,8. The noise shows good agreement with the model in the relatively lower gate overdrive voltage regime where the number fluctuation mechanism dominates.

For the noise calculation for short channel devices, the respective parameters in the three regions must be extracted first. The effective channel length is about $L_{eff} = L_{mask}$-0.06μm, which is extracted based on the shift and ratio method [3-15]. To obtain the respective length and local Vt in the pocket implantation regions (i.e., Region 1 and Region 3), we use the method in [3-16,17] to extract them from the reverse short channel effect of the two types of devices (shown in Fig. 3-2). Table 3-1 shows the extraction results for both sets of short channel devices. Based on Eq. (3-3), the measurement and calculation results show good agreement with each other (shown in Fig. 3-9,10).

However, on the assumption of domination of number fluctuation mechanism, the noise can be well modeled for both long and short channel devices except for a higher gate overdrive bias regime. It is believed that the mobility fluctuation mechanism ($\alpha\mu$) should be considered as the gate overdrive bias is relatively high. This can also be deduced from the results shown in Fig. 3-4. As can be seen, the noise increase ratio becomes lower as the gate overdrive voltage is getting higher. This is due to that the level of 1/N(x) will reduce to compatible level to am as the gate overdrive voltage is high enough. That's why the mobility fluctuation mechanism plays a more and more important role as the gate overdrive voltage gets higher. In addition, the mobility for higher pocket dose devices would be smaller than the lower one because of the degradation mechanism of impurity scattering. So the noise increase ratio would reduce in the relatively higher gate overdrive bias regime.

3.4 Application of Three-Region Model in Special ONO Charge Storage Cell

Achieving a correct description of programming charge distribution is essential to prove device functionality and to extrapolate scaling limits of ONO Charge Storage Cell. Based on the noise model methodology, the programming charge distribution is extracted from the deviation of flicker noise measured in the linear regime.

3.4.1 Noise Behavior After Program and Erase

Fig. 3-11 shows the diagram of an n-type ONO Charge Storage Cell. Fig. 3-12 shows the normalized noise characteristics after channel hot electron (CHE) programming and band-to-band hot hole (BTBHH) erasing (shown in Fig. 3-11). The noise increases after CHE programming. As shown in Fig. 3-11, the V_T (device threshold voltage) distribution becomes non-uniform after programming, which in terms produces non-uniform carrier distribution along the channel. We believe this is the cause of noise increasing. After BTBHH erasing, the

noise goes exactly back to the fresh condition because of the disappearance of non-uniform V_T distribution. Fig. 3-13 shows the gate bias dependence of normalized noise characteristics after CHE programming and BTBHH erasing. The noise seriously degrades at low gate bias where the number fluctuation mechanism dominates. Fig. 3-14 shows the normalized noise characteristics versus $V_{over\text{-}drive}$ ($Vg\text{-}V_T$) after FN programming and erasing. The noise remains the same all the time because that the V_T distribution is always uniform. Based on this concept, the noise level will be equal if the $V_{over\text{-}drive}$ is the same if the V_T distribution stays uniform.

3.4.2 Extraction of Programming Charge Distribution through Noise Measurement

The modeling methodology of non-uniform V_T effect after CHE programming is shown in Fig. 3-11. As the number fluctuation mechanism dominates, the unified flicker noise model would be reduced to Eq. (3-2). The channel carrier distribution becomes non-uniform after CHE programming, and Eq. (3-2) can be divided into two parts shown in Eq. (3-4).

$$\frac{S_{Id}}{I_d^{\,2}} \propto \int_{\Delta L} Nt(x)\frac{1}{N_1(x)}dx + \int_{L-\Delta L} Nt(x)\frac{1}{N_2(x)}dx \qquad (3\text{-}4)$$

$$\propto \frac{\Delta L}{L}\cdot\frac{S_{Id}}{I_d^{\,2}}\Bigg|_{\substack{N=N_1(x)\\(V_T=V_{T1})}} + \frac{L-\Delta L}{L}\cdot\frac{S_{Id}}{I_d^{\,2}}\Bigg|_{\substack{N=N_2(x)\\(V_T=V_{T2})}} \qquad (3\text{-}5)$$

Assume that Region 1 occupies a length of ΔL and has a local threshold voltage V_{T1}, the noise of the two regions can be calculated simply by occupied length ratio multiplying the noise level referred to their own $V_{over\text{-}drive}$ (shown in Eq. (3-5)). Based on this extraction methodology, one can easily get the programming charge distribution without any device simulation. Fig. 3-15 shows the calculating results of the non-uniform threshold voltage effect. One can choose an optimal set of V_{T1} and ΔL to fit the measurement results based on the two-region model shown in Fig. 3-11. Because that there are two fitting parameters in Eq. (3-5), we use the error function method to determine the optimal solution of V_{T1} and ΔL. The

result is shown in Fig. 3-16. A global minimum of error is found at V_{T1}=2.9V, ΔL=290Å in our programming condition. Finally, comparison of reverse engineering method [3-18] and extraction by flicker noise is done as Table 3-2.

3.5 Summary

Pocket implantation effects on drain current flicker noise in 0.13μm CMOS process based high performance analog n-MOSFETs is investigated. Our results show that pocket implantation will degrade device noise characteristics primarily due to enhanced non-uniform threshold voltage distribution along the channel. Besides, the oxide quality is not affected by the pocket implantation process through the evidence of charge pumping results. That is, the channel profile engineering would be a key factor for low noise device design instead of the improvement of oxide quality. In addition, an analytical flicker noise model to take into account a pocket doping effect is proposed and shows good agreement with the measurement results. The analytical model is easy to implement in circuit simulators, such as HSPICE, for analog circuit design.

Based on this concept, the programming charge distribution in NROM cells can be extracted from noise measurement in the linear operation regime without any device simulations. In addition, the result shows good agreement with the inverse modeling method.

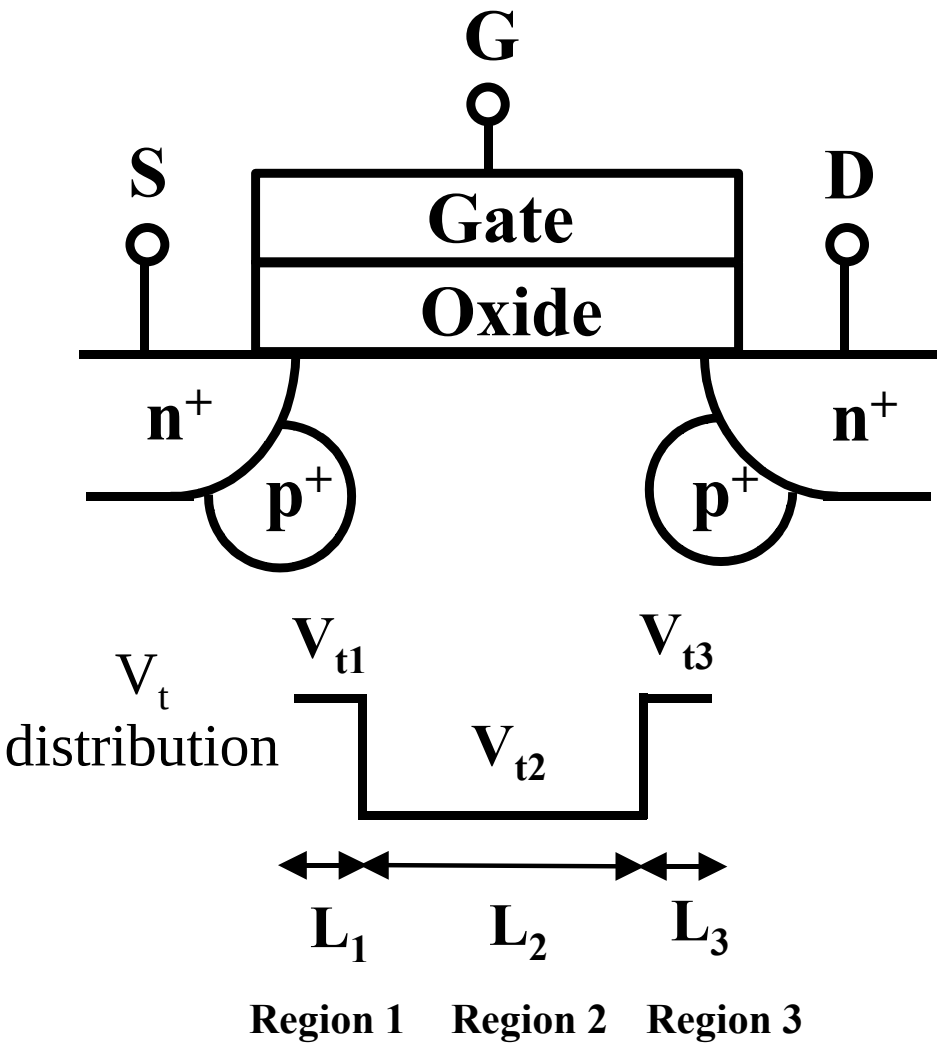


Fig. 3-1 The diagram of pocket implant induced non-uniform threshold voltage distribution along the channel. Region 1 and 3 is the pocket-implant-affected region and possesses a higher threshold voltage. Region 2 is the rest of the channel.

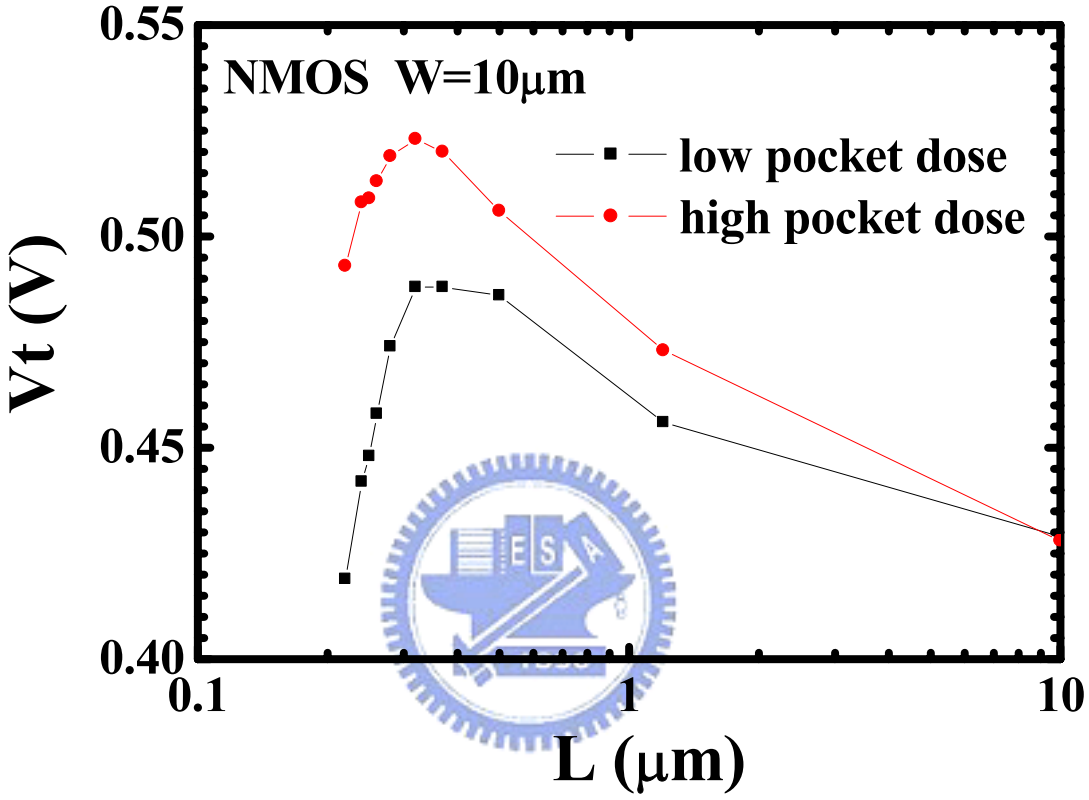


Fig. 3-2 Reverse short channel effect of n-MOSFETs (W=10μm) for low/high pocket doses.

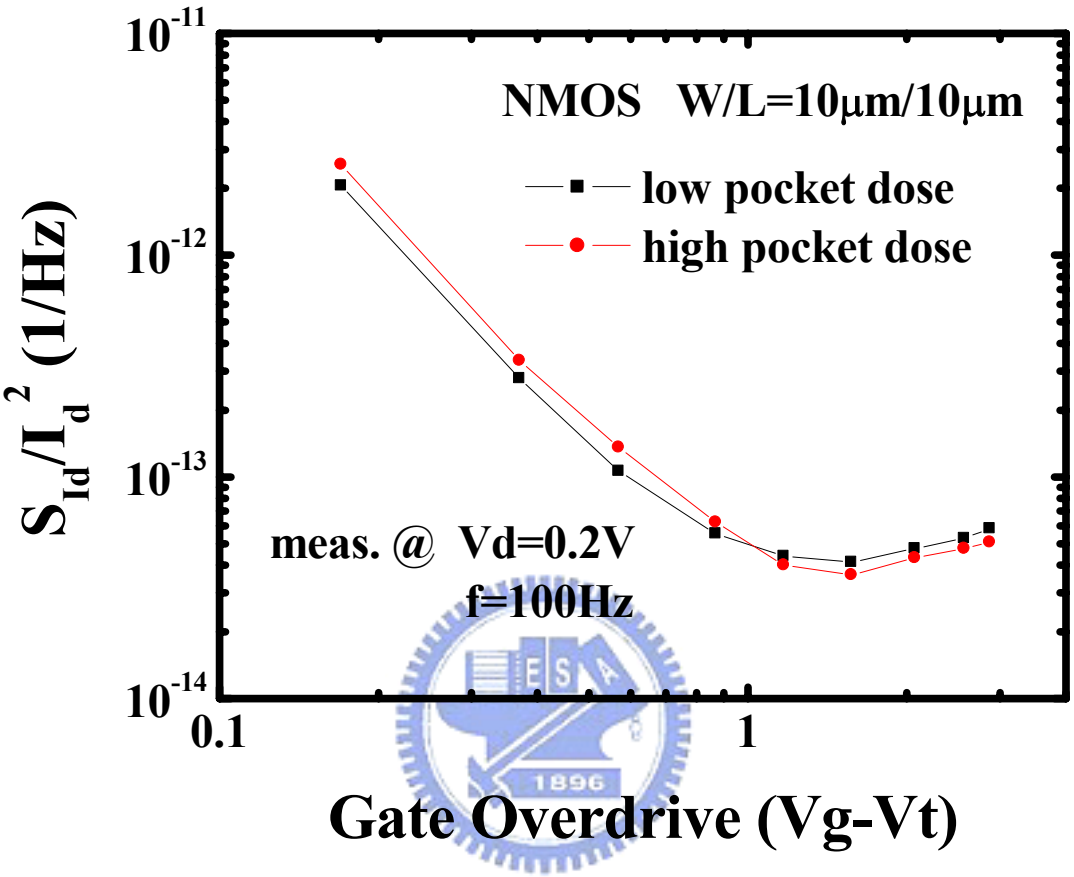


Fig. 3-3 Long channel length NMOS (W/L=10μm/10μm) normalized noise power spectrum density versus gate overdrive voltage (Vg-Vt) for low/high pocket doses. The noise is measured in the linear regime, and all data points are averaged from 3 devices.

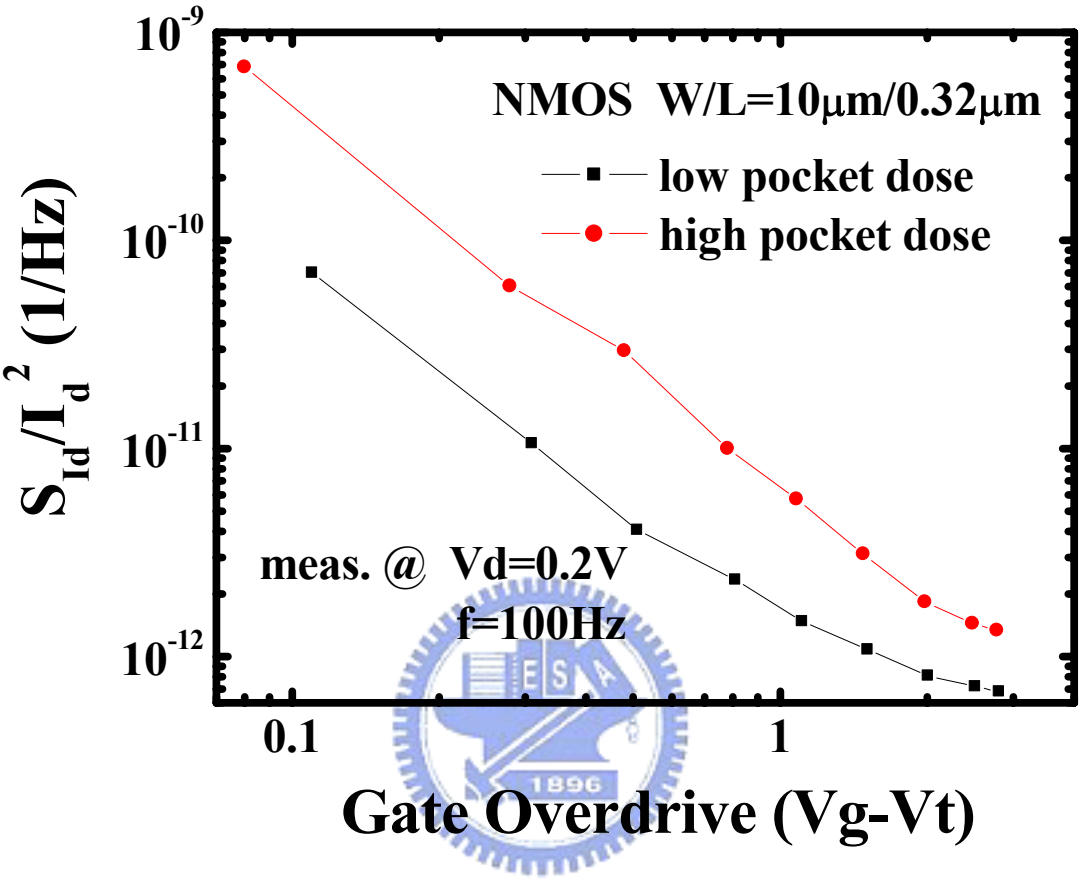


Fig. 3-4 Short channel length NMOS (W/L=10μm/0.32μm) normalized noise power spectrum density versus gate overdrive voltage (Vg-Vt) for low/high pocket doses. The noise is measured in the linear regime, and all data points are averaged from 10 devices.

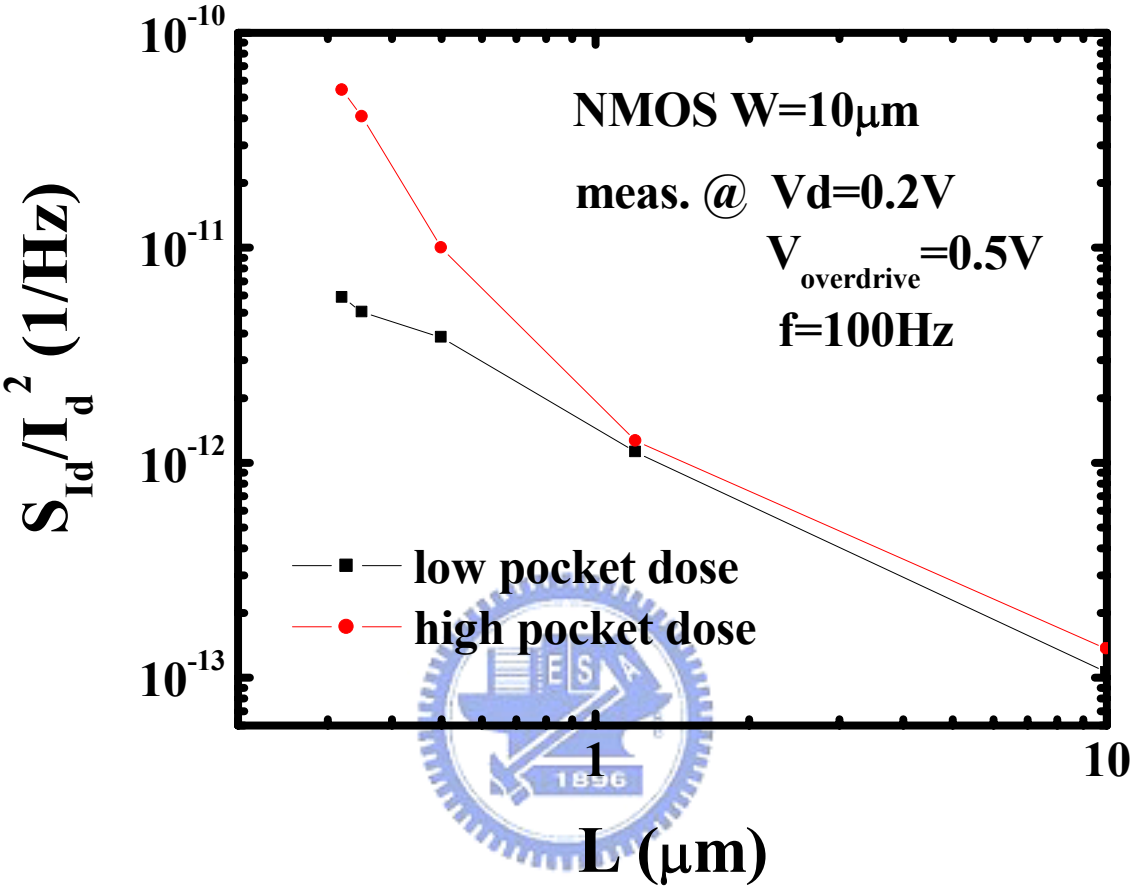


Fig. 3-5 Normalized noise power spectrum density versus gate length for low/high pocket doses. The noise is measured at the same gate overdrive voltage.

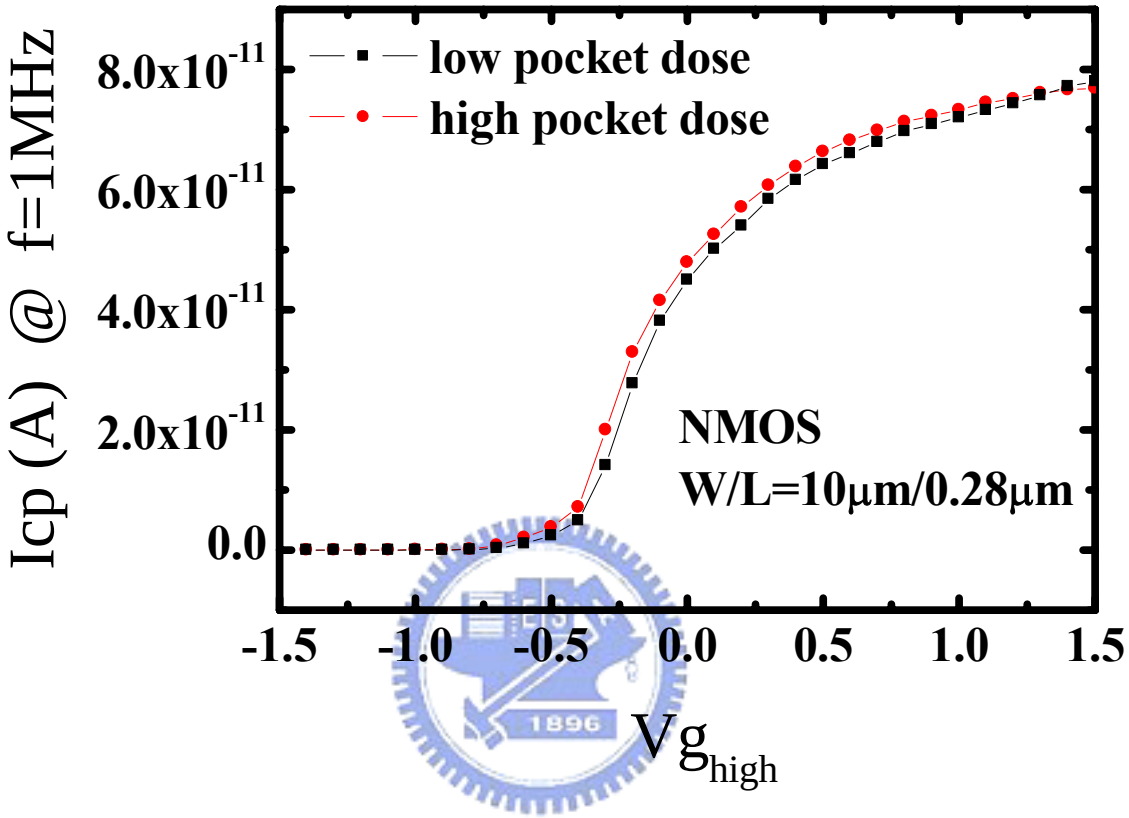


Fig. 3-6 Charge pumping current versus the high level of gate pulse (Vg_{high}) in CP measurement for low/high pocket doses.

	Low Pocket Dose	High Pocket Dose
$N_t(E_{fn})$	1.7E11 cm^{-2}	1.82E11 cm^{-2}
$L_1=L_3$	62nm	71nm
V_{t2}	0.43 V	0.43 V
$V_{t1}=V_{t3}$	0.497 V	0.609 V

Table 3-1 The values of pocket length, threshold voltage and oxide trap density for low/high pocket doses.

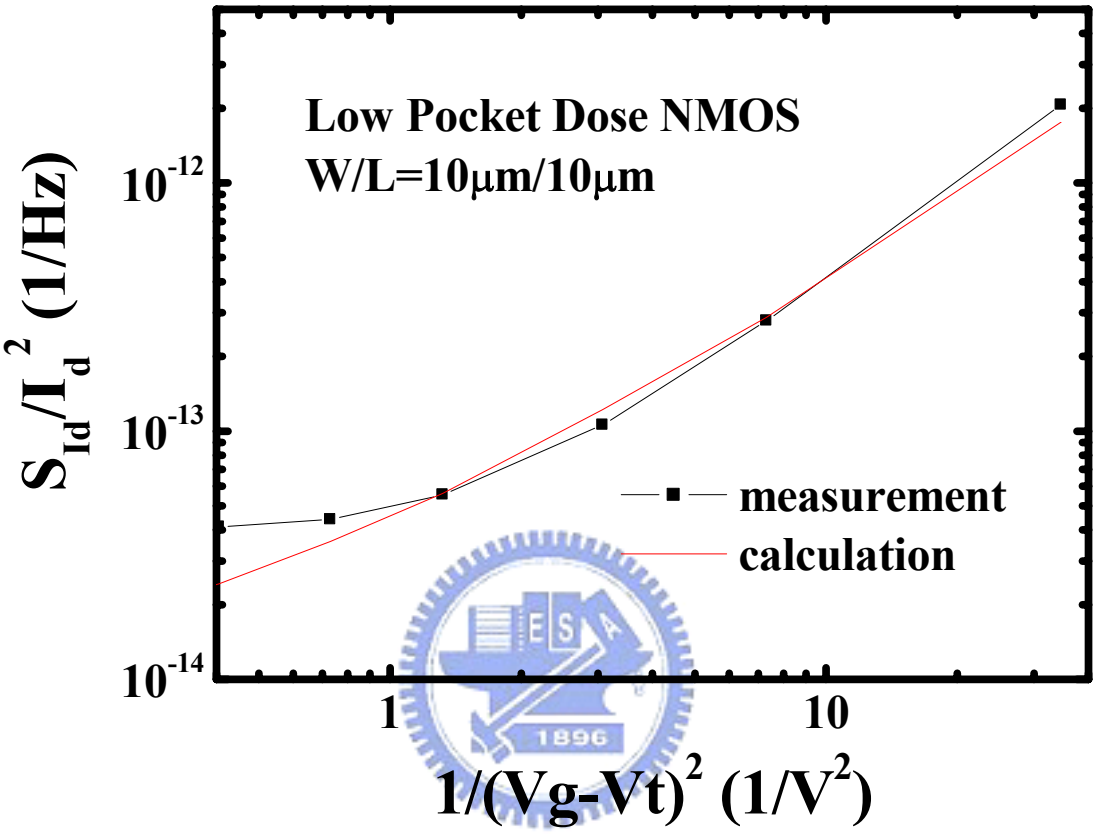


Fig. 3-7 Comparison of calculated and measured noise results for long channel length NMOS (W/L=10μm/10μm) with low pocket dose.

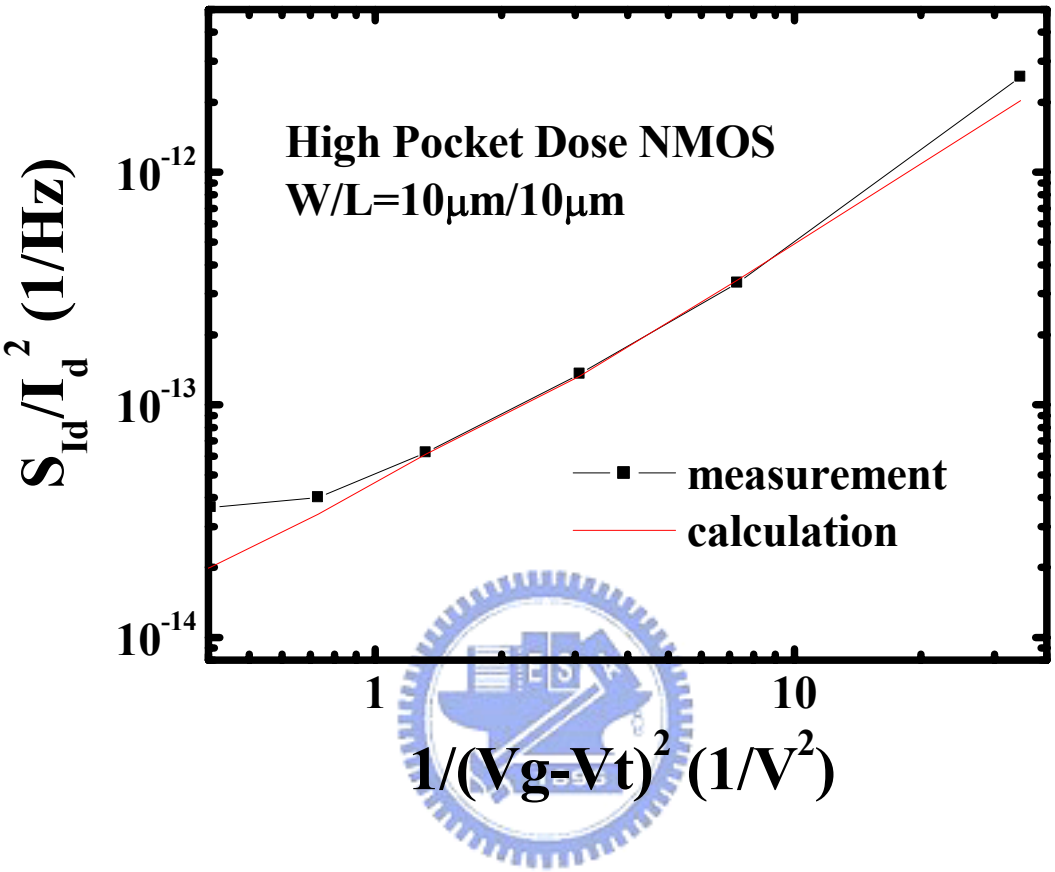


Fig. 3-8 Comparison of calculated and measured noise results for long channel length NMOS (W/L=10μm/10μm) with high pocket dose.

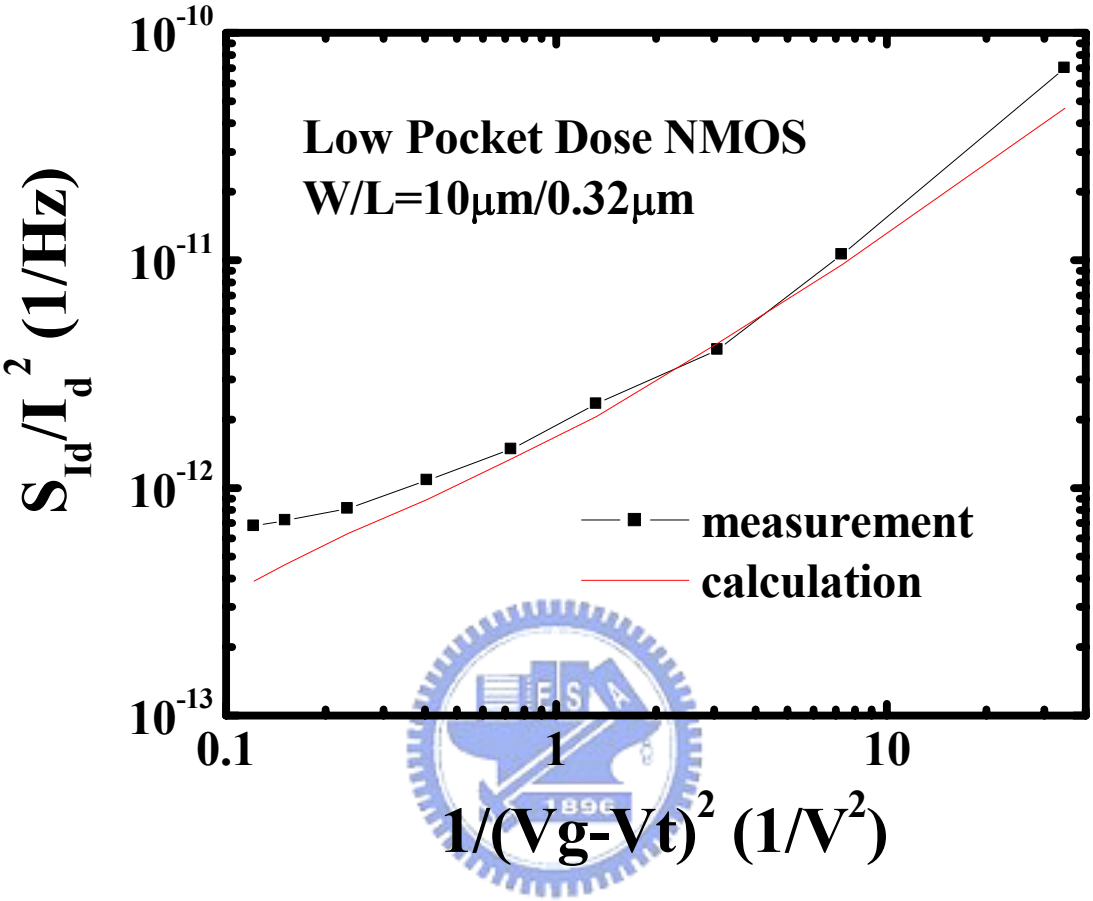


Fig. 3-9 Comparison of calculated and measured noise results for short channel length NMOS (W/L=10μm/0.32μm) with low pocket dose.

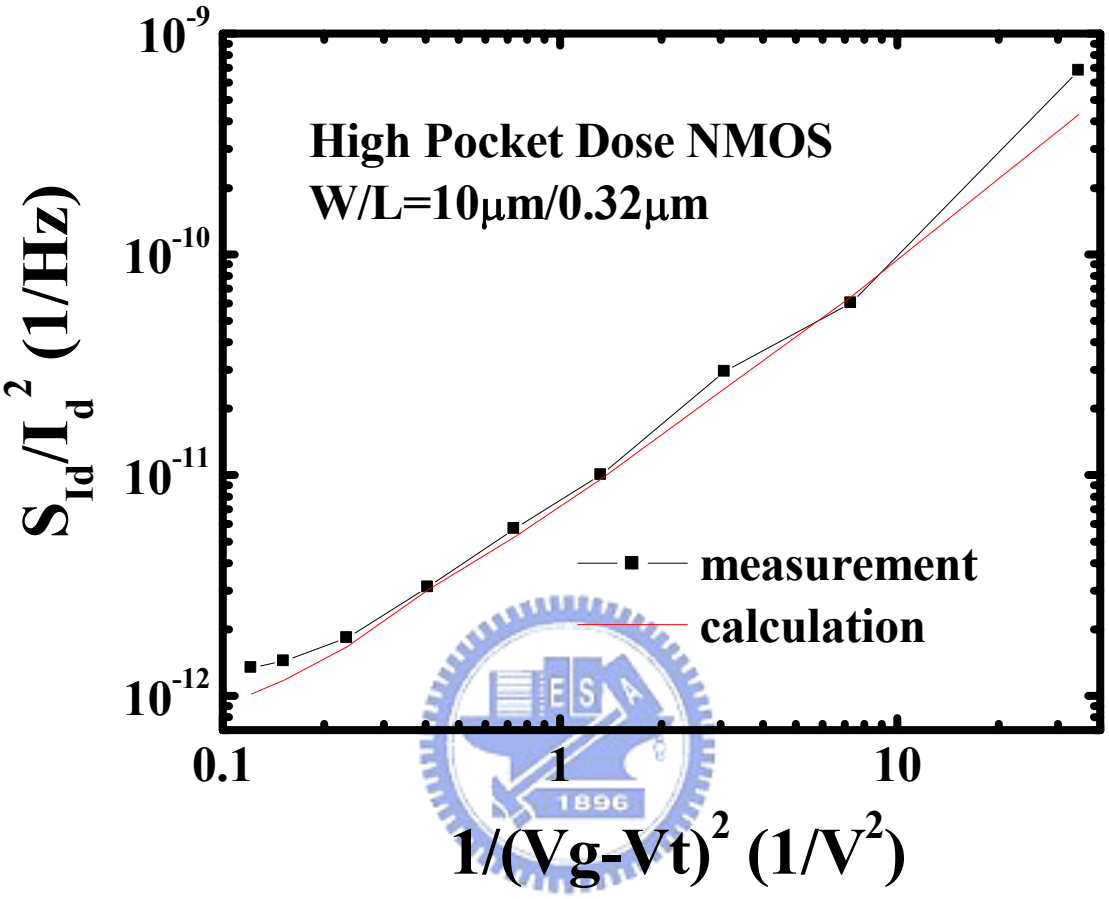


Fig. 3-10 Comparison of calculated and measured noise results for short channel length NMOS (W/L=10μm/0.32μm) with high pocket dose.

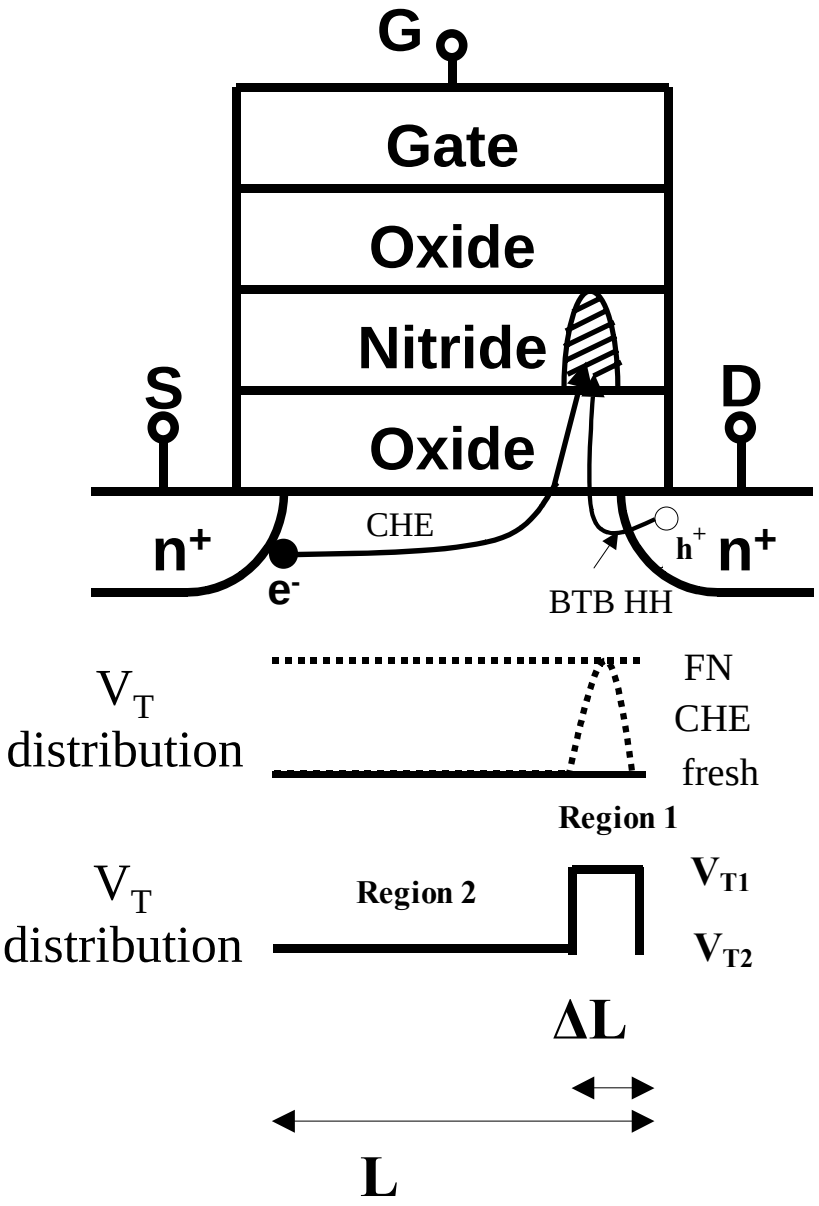


Fig. 3-11 The diagram of an n-type ONO charge storage cell. The V_T distribution before and after CHE/FN programming is also shown. V_{T1} is the local threshold voltage below the CHE programmed region. ΔL is the width of the programmed region. V_{T2} is the threshold voltage of the fresh device.

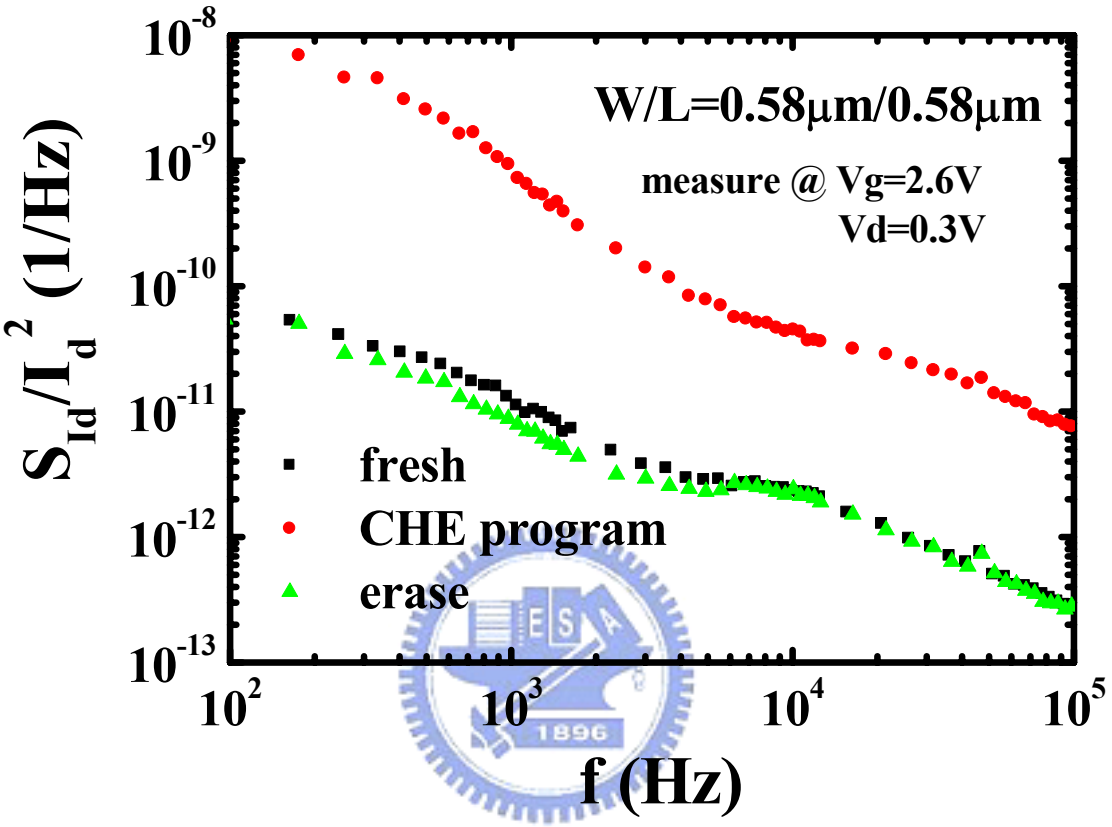


Fig. 3-12 Normalized noise characteristics (meas. @ linear regime) after CHE programming (VT=0.8V) and BTBHH erasing in an n-type ONO charge storage cell. The noise increases after programming and goes back after erasing.

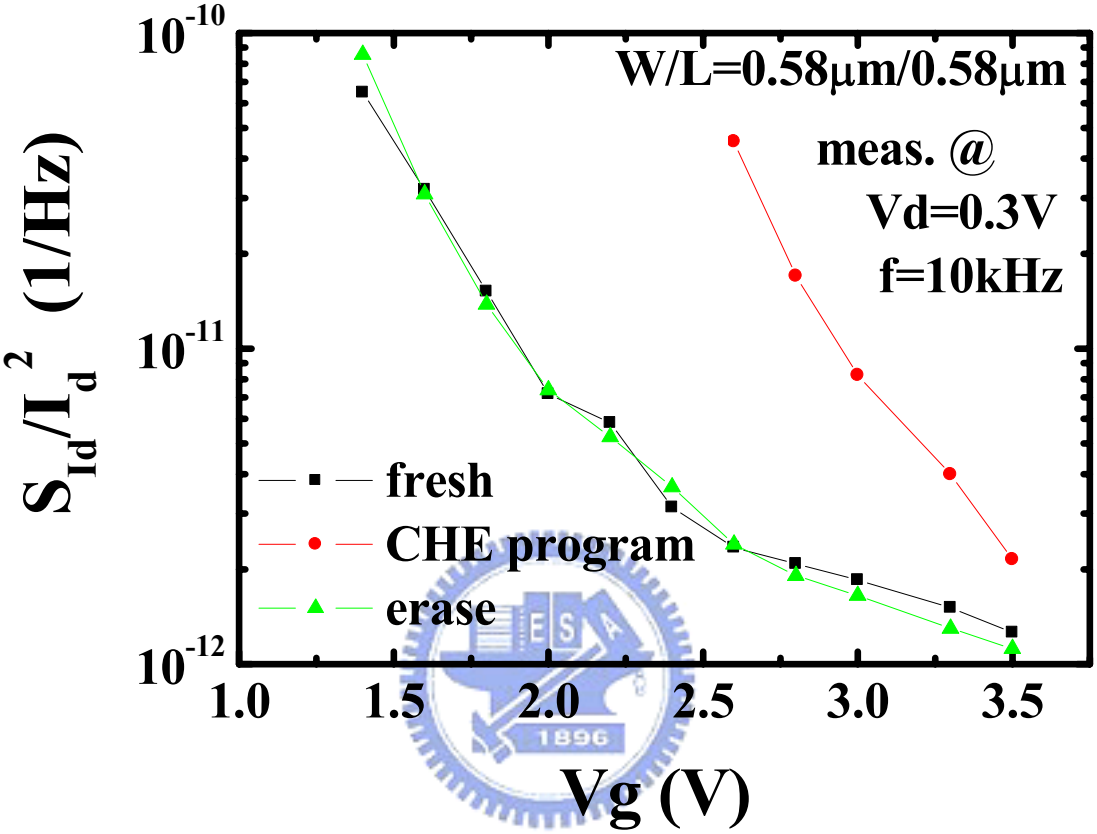


Fig. 3-13 Normalized noise versus Vg characteristics (meas. @ linear regime) after CHE programming and edge erasing in an n-type ONO charge storage cell. The noise seriously degrades at low Vg where the number fluctuation mechanism dominates.

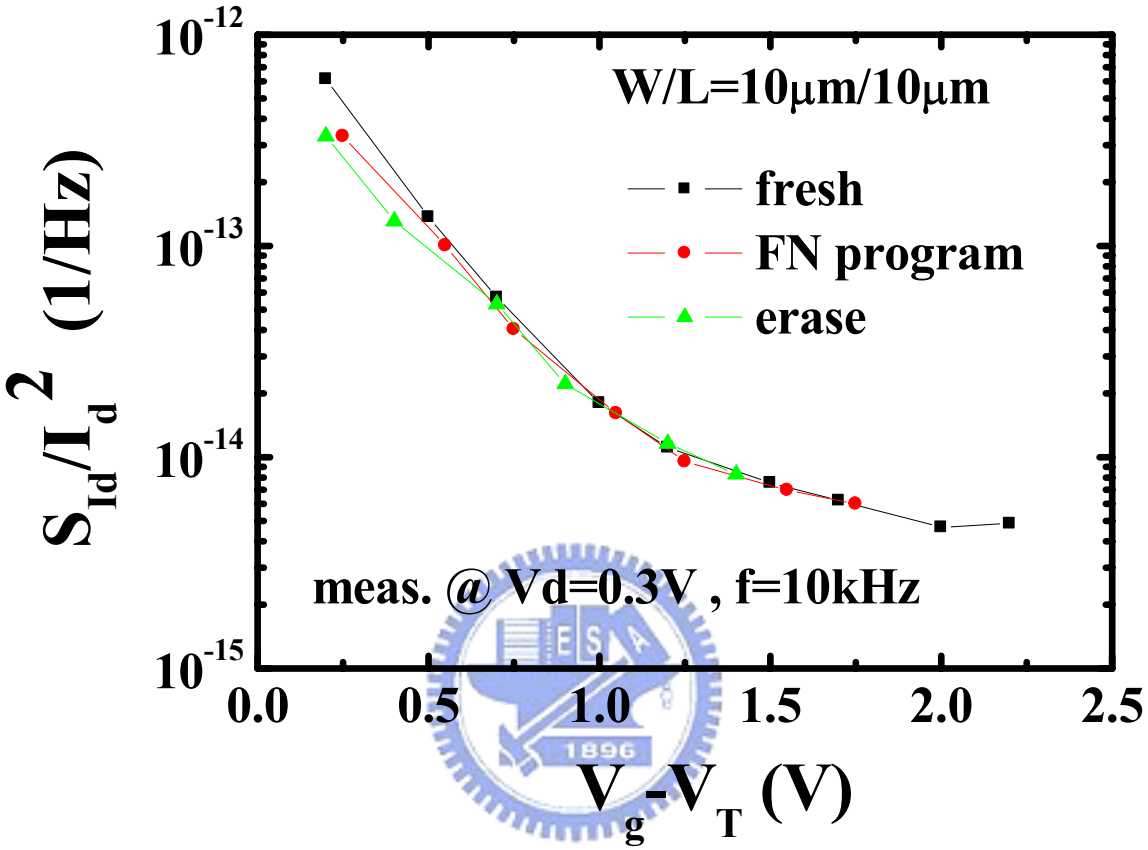


Fig. 3-14 Normalized noise versus $V_{over\text{-}drive}$ ($Vg\text{-}V_T$) characteristics (meas. @ linear regime) after FN programming and erasing in an n-type ONO charge storage cell. The noise remains the same all the time.

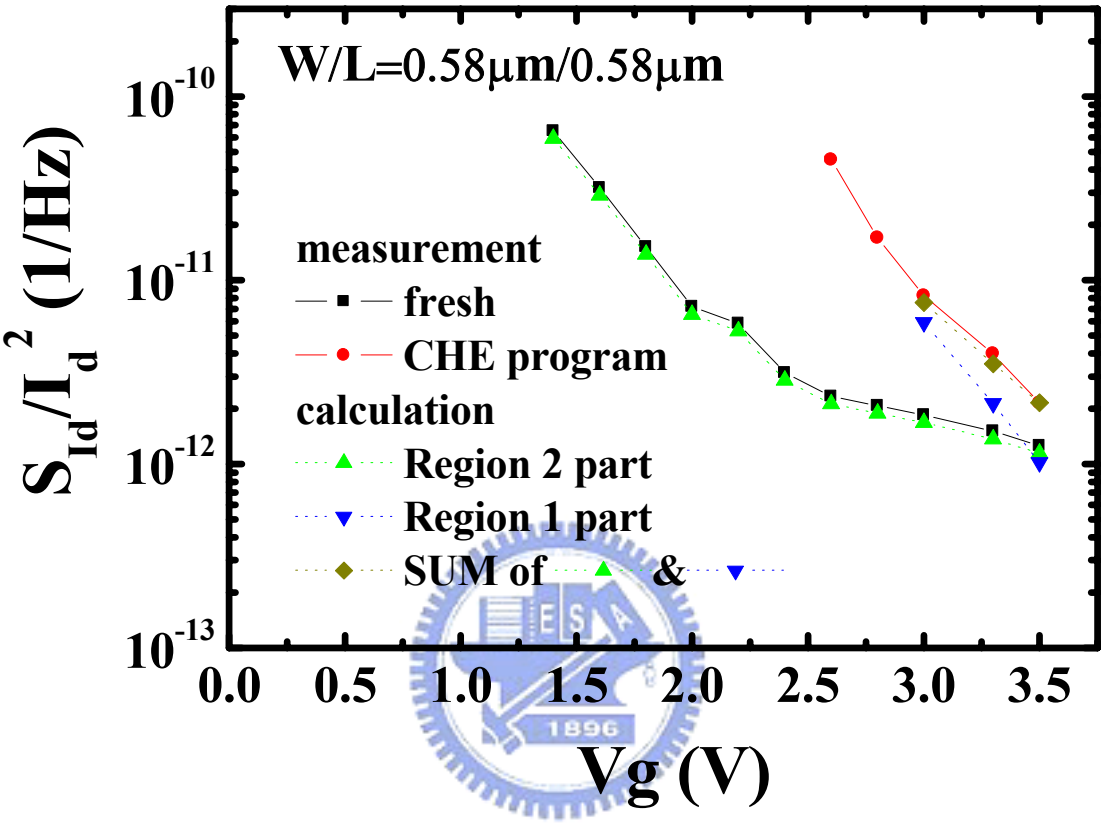


Fig. 3-15 Modeling results of non-uniform threshold voltage effect. One can choose an optimal set of V_{T1} and ΔL to fit the measurement results based on the two-region model.

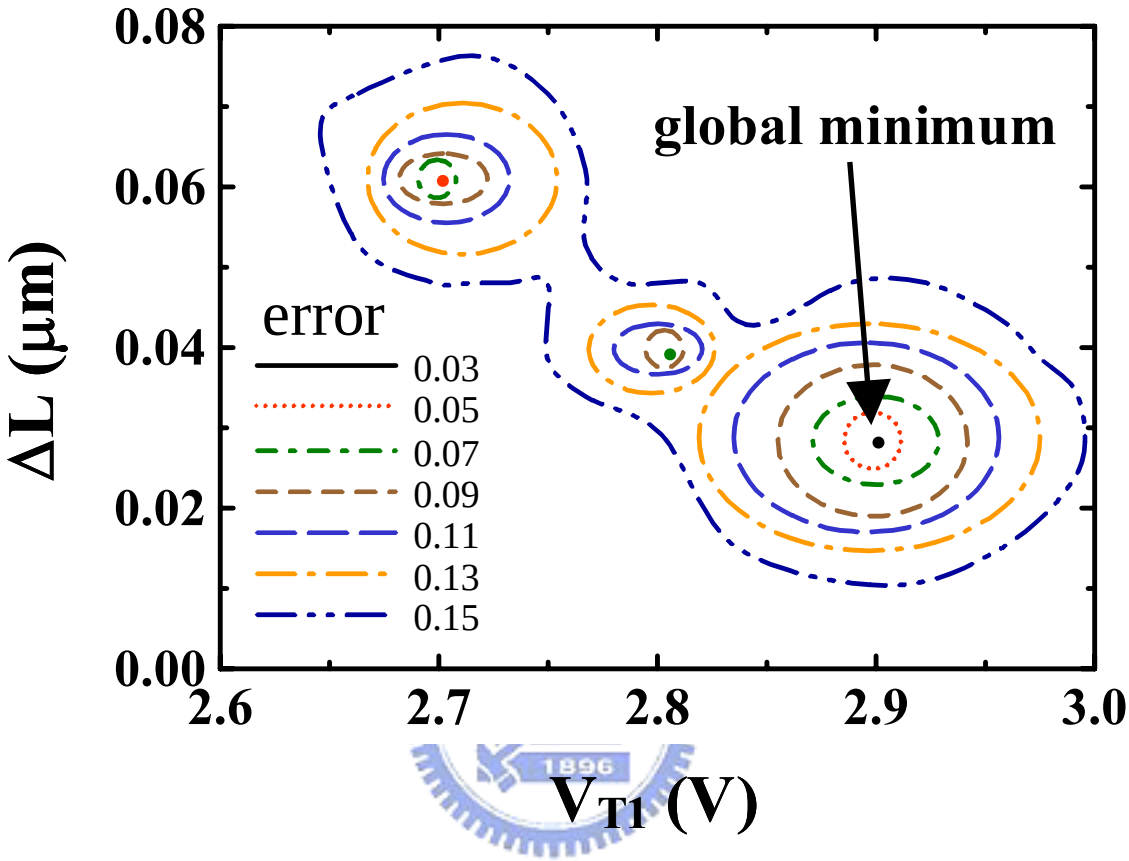


Fig. 3-16 Extraction of V_{T1} and ΔL by the error function method. The global minimum (minimum error=0.03) is located at V_{T1}=2.9V, ΔL=290Å in our CHE program condition.

	Reverse Engineering	Extraction by 1/f Noise
Sensitivity of L_{CHE}	**Higher**	**Lower**
Sensitivity of Vt_{loc}	**Lower**	**Higher**
Accuracy	**Higher**	**Lower**
Complexity	**Complex**	**Simple**

Table 3-2 Comparison of the two extraction method: 1. reverse engineering and 2. extraction by flicker noise measurement.

Chapter 4
Influence of Inversion Carrier Distribution on Drain Current Flicker Noise

4.1 Introduction

Based on the study of Chapter 3, it is found that channel carrier distribution has noticeable influence on drain current Flicker noise. In this chapter, we use a two-dimensional device simulator, MEDICI, to simulate the effect of channel carrier distribution on Flicker Noise for pocket and non-pocket devices. In addition, the pocket implantation effect on drain current Flicker Noise is also calculated based on the simulation results. Finally, the substrate bias effect on Flicker noise is investigated. Some study [4-1,2] has shown that substrate bias can modulate the peak of the carrier concentration in the surface, that is, far away from the surface or near the surface, and will influence the interaction between carriers and oxide traps. Substrate bias not only affects the distribution of channel carrier in the vertical direction but also affects the threshold voltage distribution in the channel direction. In this study, the substrate bias effect on pocket and non-pocket device is also illustrated.

4.2 Simulation of Channel Carrier Distribution with Different Pocket Condition

In this section, the channel carrier distribution with different pocket condition is simulated. The device structure and major parameters for simulation is illustrated in Fig. 4-1. Fig. 4-2 shows the simulated carrier distribution in a non-pocket device at Vg=1V, Vd=0.2V, Vb=0V. The device has a long channel of 1μm. Every line represents the carrier distribution at the distinct depth from the substrate surface. In contrast, Fig. 4-3 shows the simulated carrier distribution in a pocket device (channel doping: 1×10^{18} $1/cm^{-3}$, pocket depth from the substrate surface: 0.1μm) with a channel length of 1μm at Vg=1V, Vd=0.2V, Vb=0V. As can

be seen, the pocket device has a more non-uniform channel carrier distribution than the non-pocket device. That is, the carrier concentration is lower in the source/drain edge compared with that in the channel region.

Next, the pocket implantation effect on channel carrier distribution in short channel device is illustrated. Fig. 4-4 shows the simulated carrier distribution in a non-pocket device at Vg=1V, Vd=0.2V, Vb=0V. The device has a short channel of 0.18μm. Fig. 4-5 shows the simulated carrier distribution in a pocket device (channel doping: 1×10^{18} $1/cm^{-3}$, pocket depth from the substrate surface: 0.1μm) with a channel length of 0.18μm at Vg=1V, Vd=0.2V, Vb=0V. As illustrated, the channel carrier distribution (for example at 10Å and 20Å) is more non-uniform for the pocket device then the non-pocket one.

4.3 Simulation of Pocket Implantation Effect on Flicker Noise

This section focuses on various pocket implantation conditions. We will present the simulation results about threshold voltage trend [4-3] for different pocket depth and calculated noise for different pocket splits based on the simulation results of channel carrier distribution. Device structure used in simulation is illustrated in Fig. 4-1.

Fig. 4-6 shows the simulated threshold voltage trend versus channel length L. The depth of pocket implantation is about 0.13μm. Doping concentration for pocket implantation ranges from 3×10^{17} $1/cm^{-3}$ to 5×10^{18} $1/cm^{-3}$. The channel doping is 2.5×10^{17} $1/cm^{-3}$. As can be seen, the reverse short channel effect (RSCE) is not clear in this simulation condition, that is, the pocket implantation has a small influence on the channel carrier distribution. For comparison, Fig. 4-7 shows the simulated threshold voltage trend versus channel length L. The depth of pocket implantation is about 0.1μm. Doping concentration for pocket implantation ranges from 3×10^{17} $1/cm^{-3}$ to 5×10^{18} $1/cm^{-3}$. The channel doping is 2.5×10^{17} $1/cm^{-3}$. Compared with Fig. 4-6, the RSCE is obvious in this simulation condition, that is, the pocket implantation has a noticeable influence on the channel carrier distribution. In a word, it

is necessary to optimize pocket implantation condition to achieve the best device performance for a device engineer.

As pointed out in Chapter 3, change in channel carrier distribution will affect the behavior of low frequency noise. To simulate the pocket implantation effect on Flicker noise based on the simulation results of channel carrier distribution, new index is required. Following the derivation in section 2.2, Eq. 4-1 is used.

$$\frac{S_{Id}}{I_d^{\,2}} \propto \int \frac{dL}{N^2(x)} \tag{4-1}$$

To investigate the change in noise with different pocket splits, carrier distribution over the channel within 200Å depth are simulated and taking into Eq. 4-1 to calculate the noise level. Fig. 4-8 shows the calculation results for different pocket doping concentration. The pocket depth is 0.13 μm. Two channel length of 1 μm and 0.18 μm are compared. As show in Fig. 4-8, the noise increase slightly with the pocket dose for L=1μm or L=0.18μm devices. This result is consistent with the threshold voltage trend shown in Fig. 4-6, where the RSCE is not obvious as the pocket depth is 0.1μm. For comparison, Fig. 4-9 shows the calculation results for different pocket doping concentration. The pocket depth is 0.13 μm. Two channel length of 1 μm and 0.18 μm are compared. It is obvious that the noise level increases with the increasing of pocket dose for both devices. In addition, the noise degrades more seriously for the short channel case. This result is also consistent with the threshold voltage trend shown in Fig. 4-7, where the RSCE is obvious as the pocket depth is 0.1μm.

We can conclude that

1. Shallower pocket implanting depth causes more serious reverse short channel effect and degradation in low frequency noise.

2. Larger the amount of pocket doping concentration reveals stronger short channel effect and degradation in low frequency noise.

3. The shorter the device length, the more violent the degradation is.

4.4 Substrate Bias Effect On Flicker Noise

Substrate bias effect is an essential property in CMOS circuit design, especially in analog circuits and SOI applications. For example, DTMOSFET [4-4] is a good choice for analog circuits since it can improve device matching characteristics and reduce noise. Another example is the SOI devices. In SOI devices, the body is floating and various body charging process may cause a non-zero body potential. The substrate bias effect on the distribution of channel carrier and thereupon on the Flicker noise is worth further investigation.

The substrate bias effect is profound and many fold; it not only modifies the depth of current flow from the surface but also modulates the concentration of inversion carriers. In addition, it will also affect the non-uniformity of the channel threshold voltage distribution. The combined effect affects mobility, operation current, noise, etc [4-2,5].

4.4.1 Measurement Results of Substrate Bias Effect

Fig. 4-10 shows the comparison of substrate bias effect for different gate voltage in non-pocket n-MOSFETs with L=1.2μm and 0.22μm. The index of noise increase ratio is performed by the dividing of noise level at Vb=-1V and Vb=0.5V. Significant degradation of noise from Vb=0.5V to –1V is observed at low gate bias in the long channel device. The reason is that a Vb of –1V pushes electrons towards the surface and thus channel electrons have larger chance to “see” surface traps. Another reason is that a negative substrate bias reduces the number of channel carriers Thus, the carrier number fluctuation becomes more significant, which is also the cause of the Flicker noise. However, the substrate bias effect is not obvious in the short channel case. We will discuss it through device simulation.

Both of these effects degrade the low frequency noise. So it’s clear that negative substrate bias in NMOS will degrade 1/f noise in a pocket implanted device.

Fig. 4-11 shows the comparison of substrate bias effect for different gate voltage in pocket n-MOSFETs with L=1.2μm and 0.22μm. The index of noise increase ratio is

performed by the dividing of noise level at Vb=-1V and Vb=0.5V. Significant degradation of noise from Vb=0.5V to –1V is observed at low gate bias in both device. It's interesting to note that the substrate bias effect on noise in a non-pocket short channel device is different from that with pocket implantation. To confirm this result, numerical simulation of the channel charge profile in these two devices is performed.

4.4.2 Simulation Results of Substrate Bias Effect

Device structure for simulation is illustrated as Fig. 4-1. pocket length and channel doping concentration, L_p and D_c, are specified as 0.07 μm and 2.5×10^{17} 1/cm^3 in this chapter respectively. Fig. 4-12,13 shows the lateral distribution of the inversion carrier along the channel at different depths. The device has no pocket and the gate length is 1μm. The Vb is 0.5V in Fig. 4-12 and the Vb is –1V in Fig. 4-13. Fig. 4-14,15 shows the lateral distribution of the inversion carrier along the channel at different depths. The device has no pocket and the gate length is 0.18μm. The Vb is 0.5V in Fig. 4-14 and the Vb is –1V in Fig. 4-15. As can be seen, the negative substrate bias reduces the channel carrier concentration and causes the noise to increase in the long channel device [4-6]. However, the negative substrate bias doesn't affect the channel carrier concentration in the short channel device. That is, the noise is not affected by substrate bias in the short channel device as shown in Fig. 4-10.

Fig. 4-16,17 shows the lateral distribution of the inversion carrier along the channel at different depths. The device has pocket and the gate length is 1μm. The Vb is 0.5V in Fig. 4-16 and the Vb is –1V in Fig. 4-17. Fig. 4-18,19 shows the lateral distribution of the inversion carrier along the channel at different depths. The device has pocket and the gate length is 0.18μm. The Vb is 0.5V in Fig. 4-18 and the Vb is –1V in Fig. 4-19. As shown in Fig. 4-16,17, the negative substrate bias reduces the channel carrier concentration and causes the noise to increase in the long channel device. In addition, the non-uniform carrier distribution induced from pocket implantation is enhanced as the negative substrate bias is applied. So the

noise level degrades more compared with non-pocket device. The same results are shown in the short channel device in Fig. 4-18,19. As can be seen, the non-uniform carrier distribution is seriously enhanced by the negative substrate bias. In a word, the noise is degraded in both long and short channel devices because of non-uniform threshold voltage distribution.

4.5 Summary

The pocket implantation would influence the channel carrier distribution and degrade drain current Flicker noise, which is proved by device simulation. In addition, substrate bias has large effect on low frequency noise. The noise level is increased at a reverse substrate bias. This effect is more significant in a pocket device since the reverse substrate bias will result in a more non-uniform threshold voltage distribution. In addition, the reduction of channel carrier number due to a reverse substrate bias also contributes to the increase of noise.

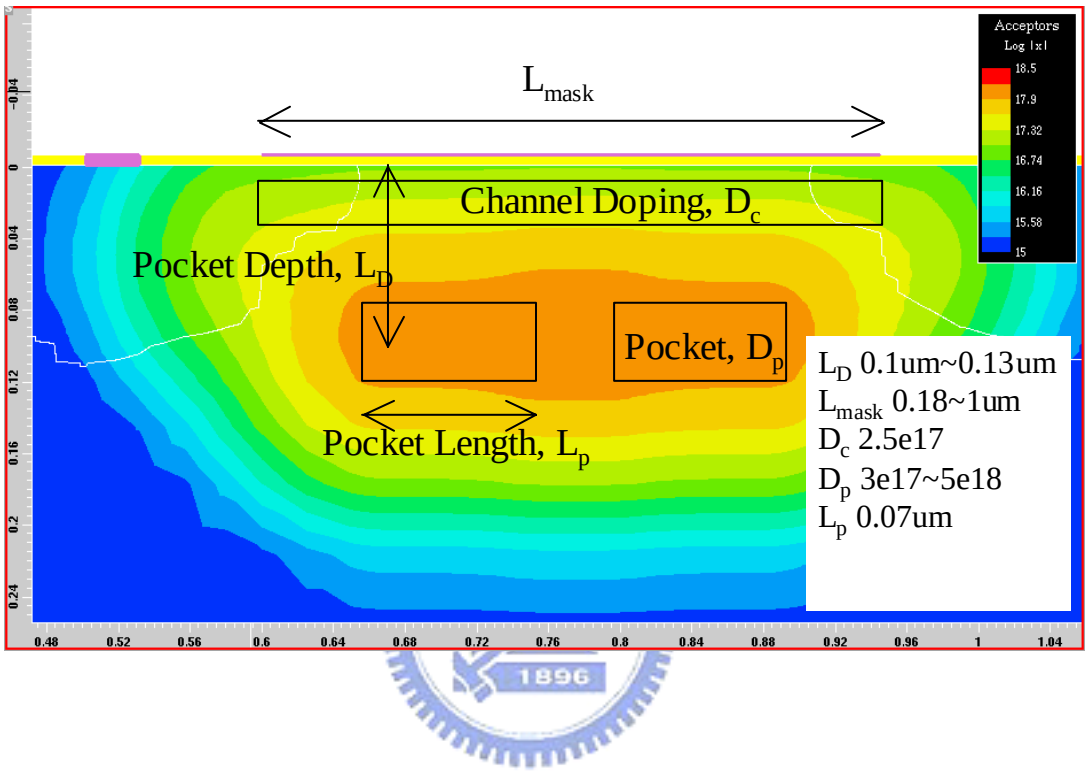


Fig. 4-1 The structure of an n-MOSFET for device simulation.

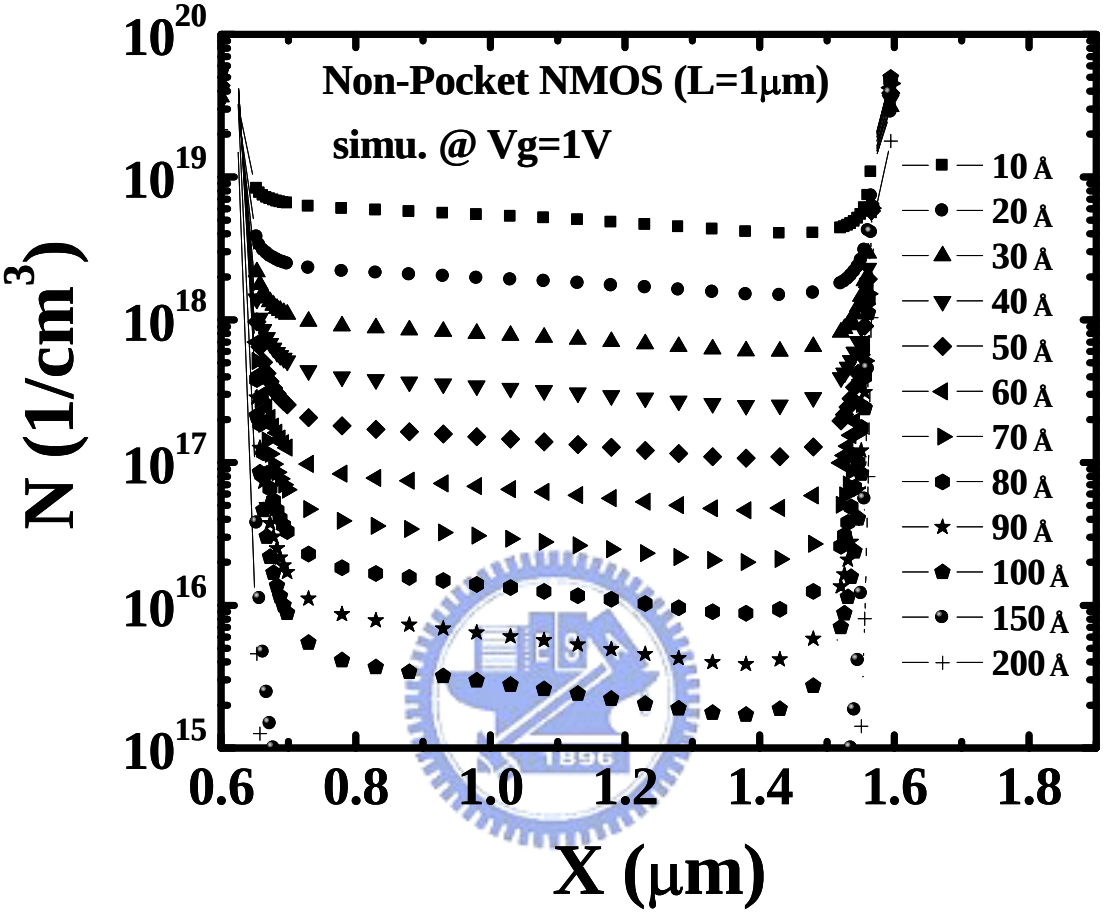


Fig. 4-2 Simulated carrier distribution of a non-pocket n-MOSFET at different depth in the channel region. The channel length is 1μm.

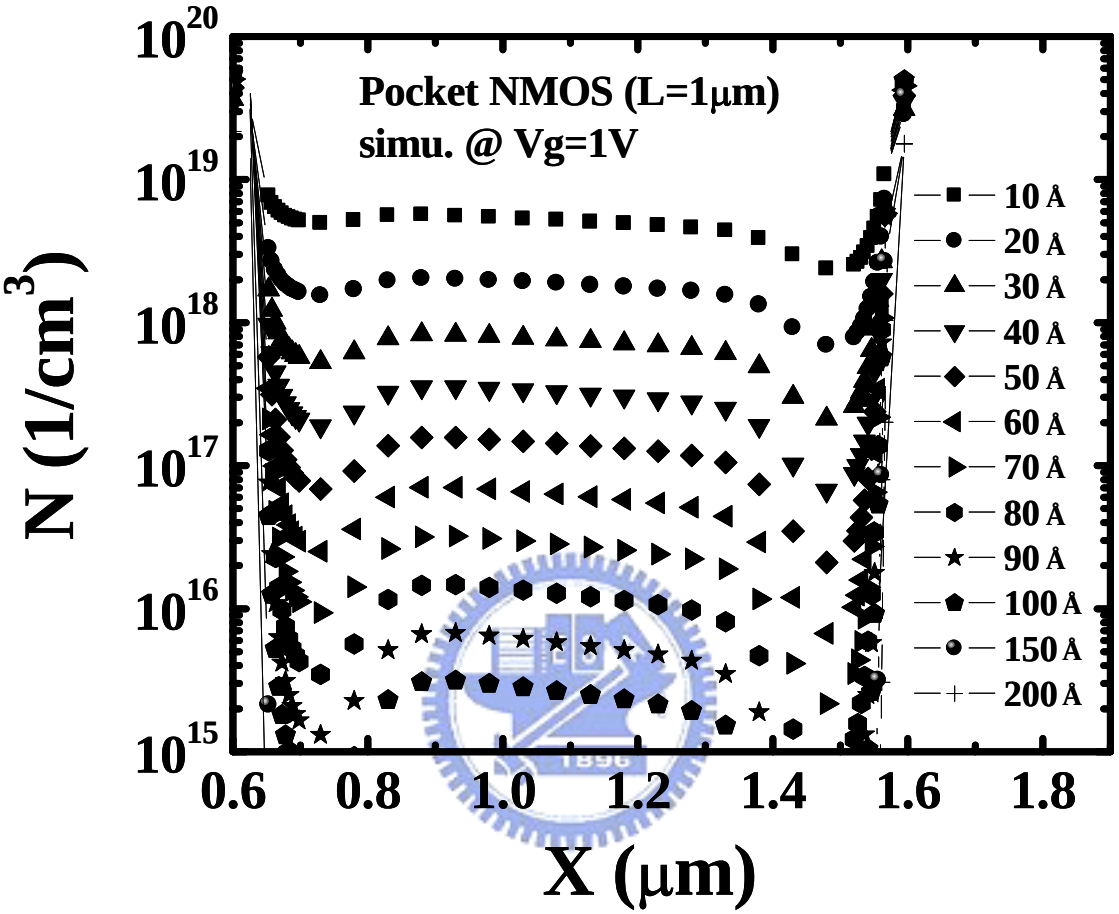


Fig. 4-3 Simulated carrier distribution of a pocket n-MOSFET at different depth in the channel region. The channel length is 1μm.

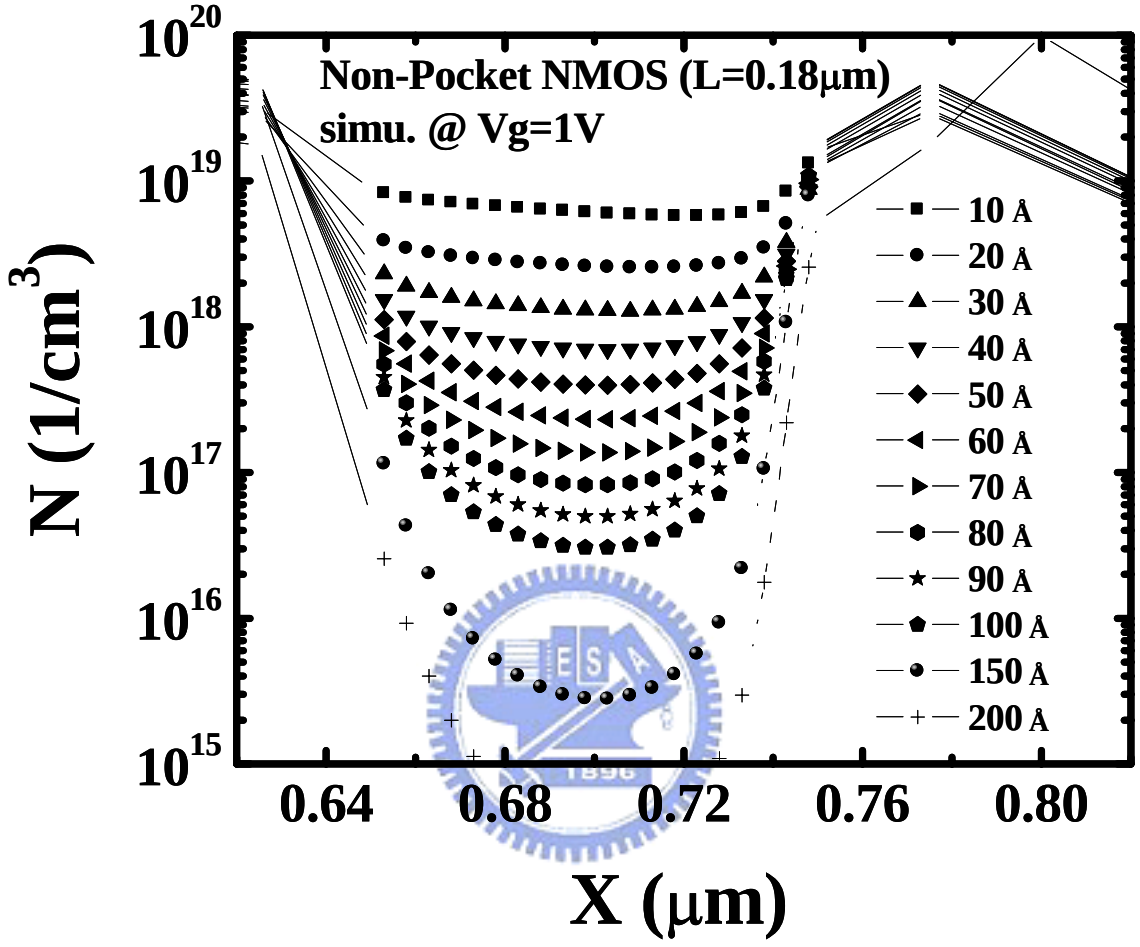


Fig. 4-4 Simulated carrier distribution of a non-pocket n-MOSFET at different depth in the channel region. The channel length is 0.18μm.

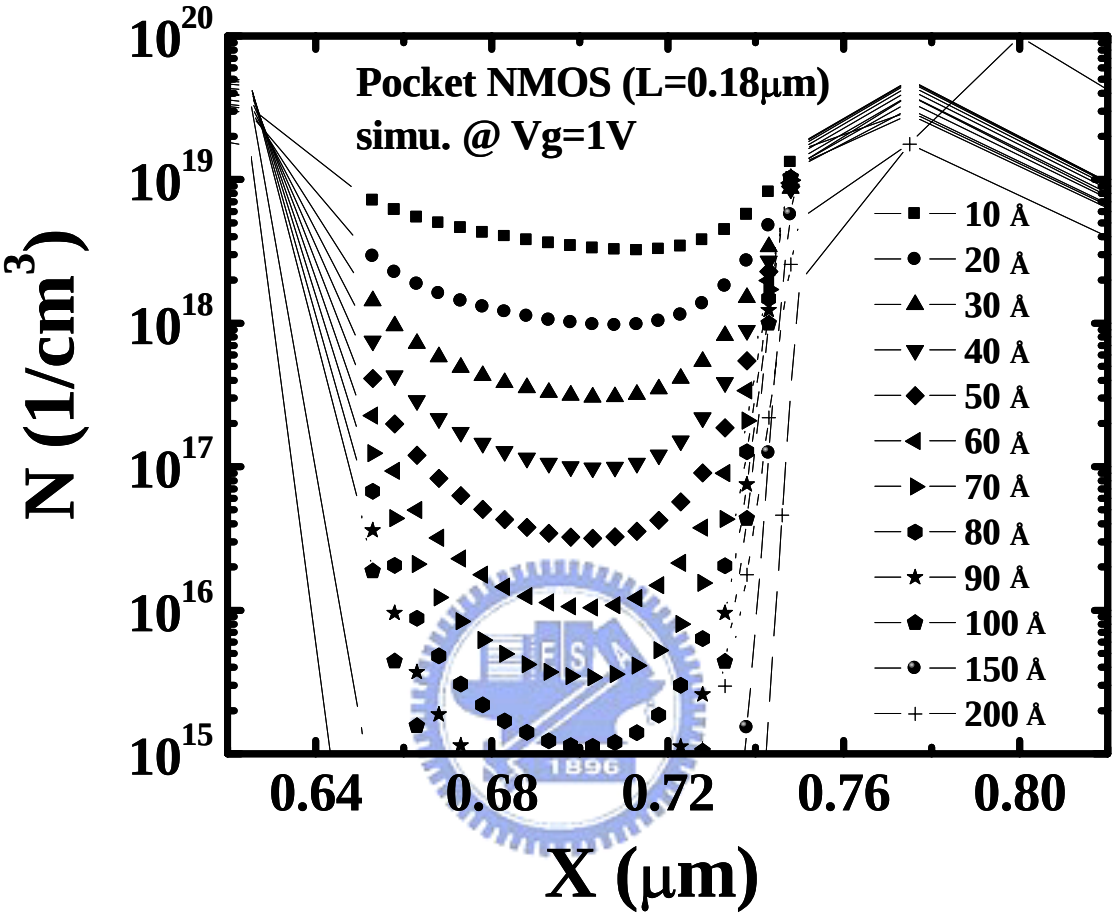


Fig. 4-5 Simulated carrier distribution of a pocket n-MOSFET at different depth in the channel region. The channel length is 0.18μm.

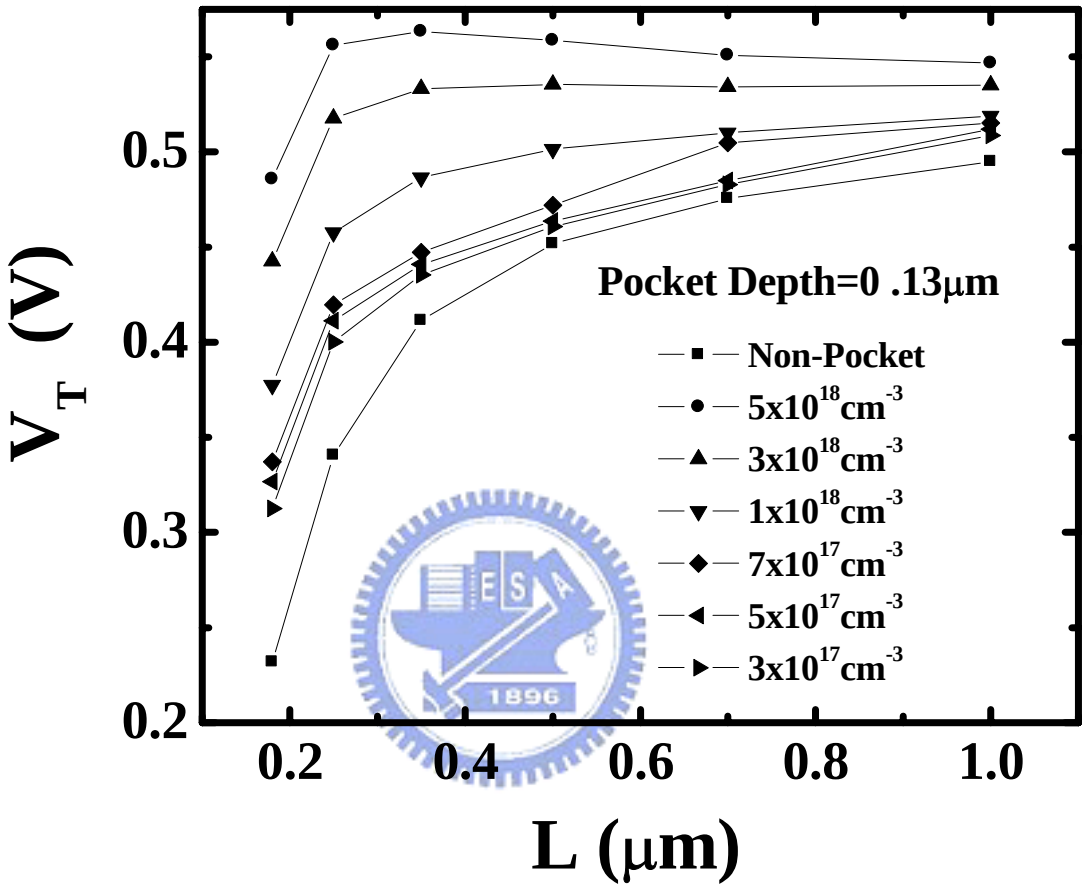


Fig. 4-6 Simulation of threshold voltage roll-off for different pocket splits. The pocket depth is 0.13μm.

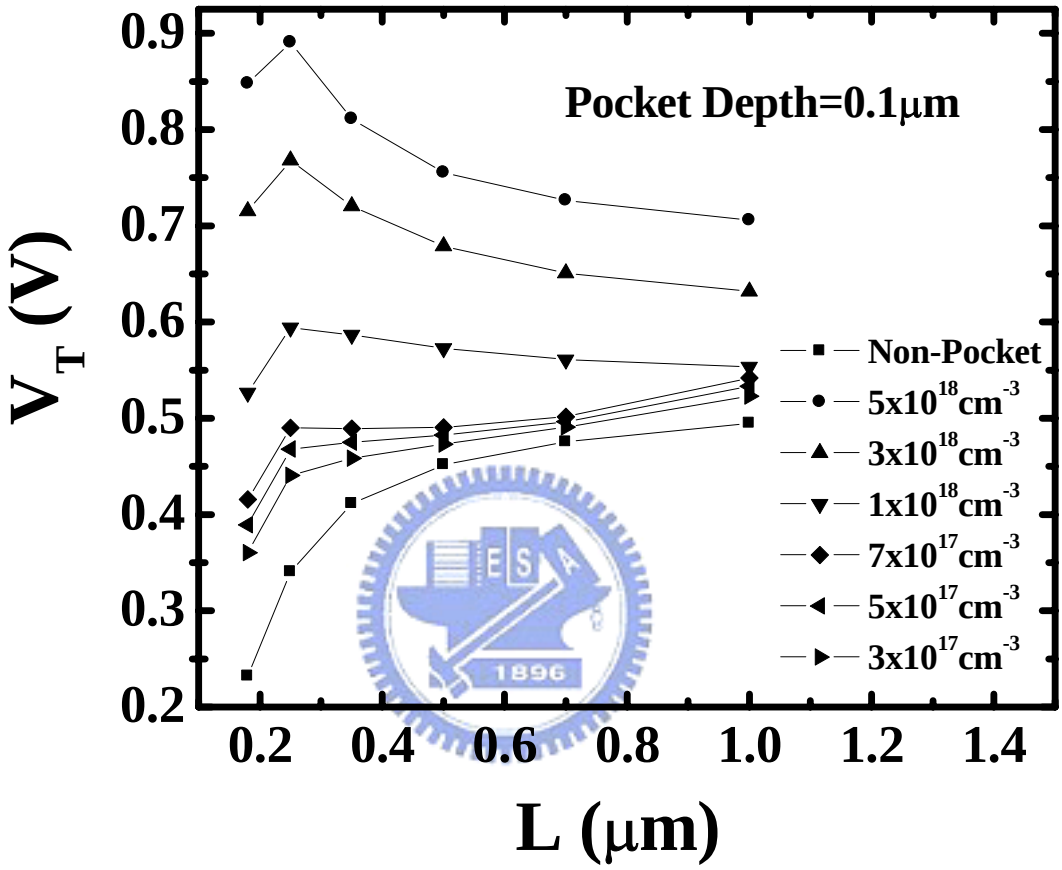


Fig. 4-7 Simulation of threshold voltage roll-off for different pocket splits. The pocket depth is 0.1μm.

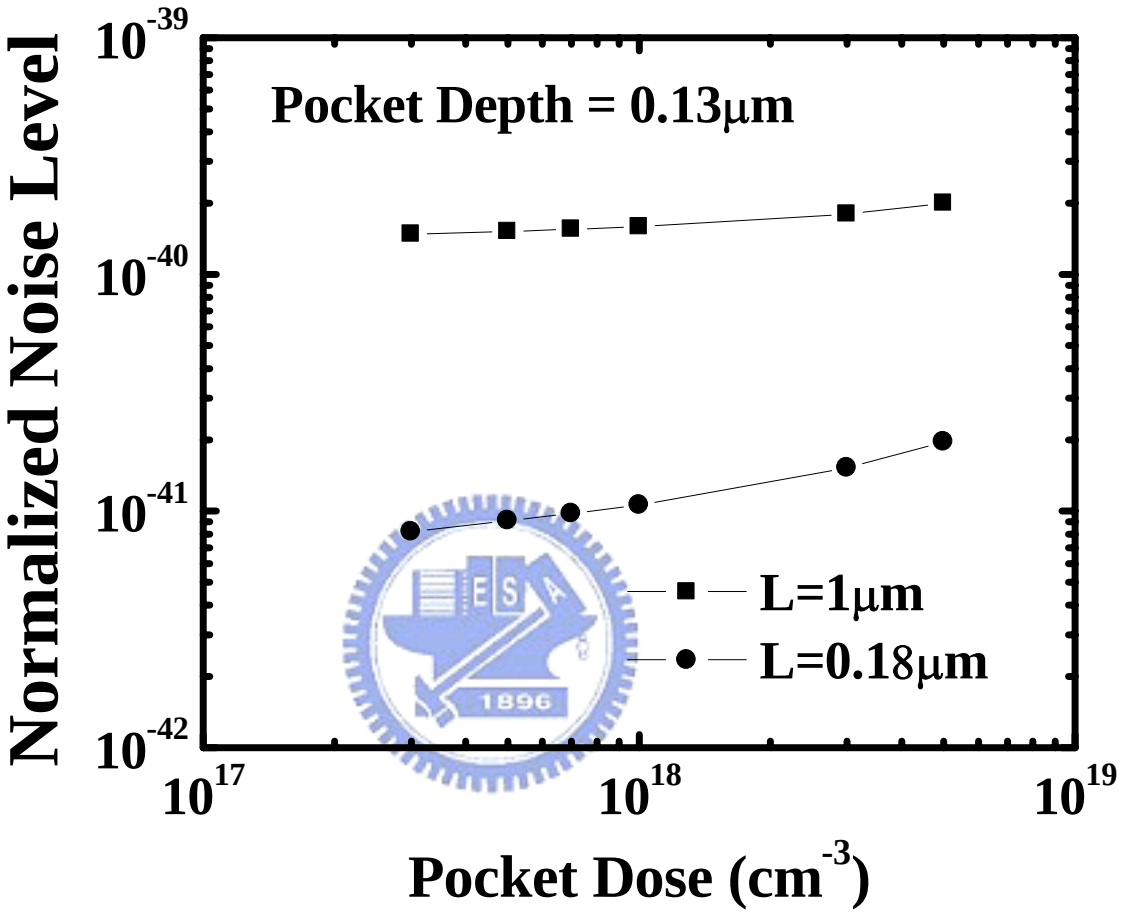


Fig. 4-8 Calculated normalized noise power spectral density for different pocket splits. The pocket depth is 0.13μm.

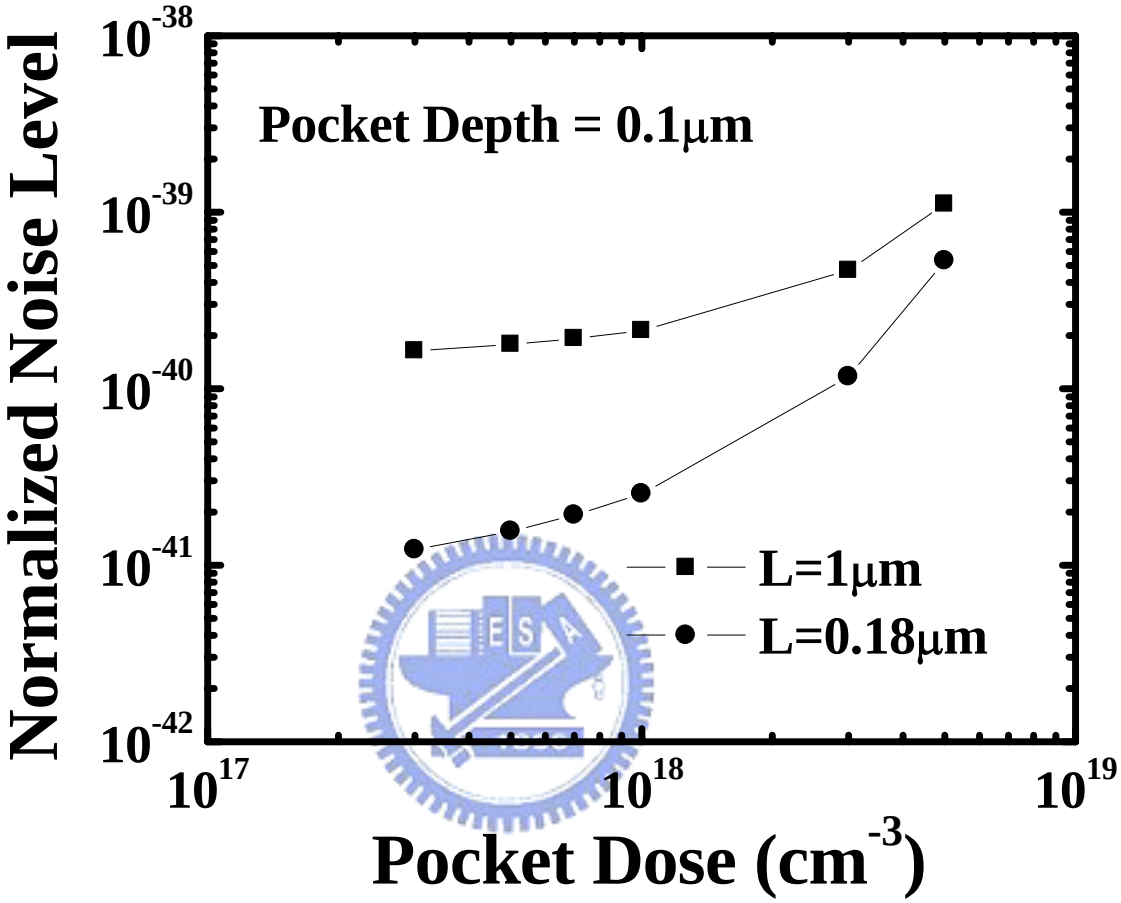


Fig. 4-9 Calculated normalized noise power spectral density for different pocket splits. The pocket depth is 0.1μm.

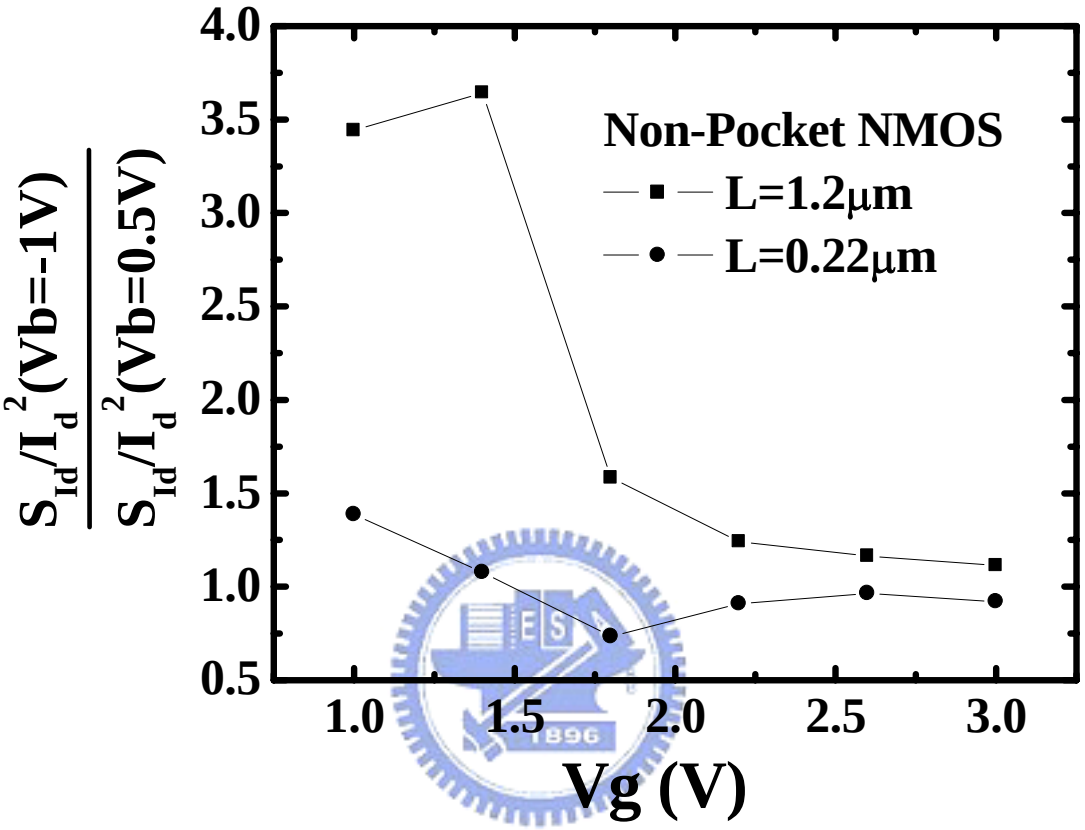


Fig. 4-10 Comparison of substrate bias effect for different gate voltage in non-pocket n-MOSFETs with L=1.2μm and 0.22μm.

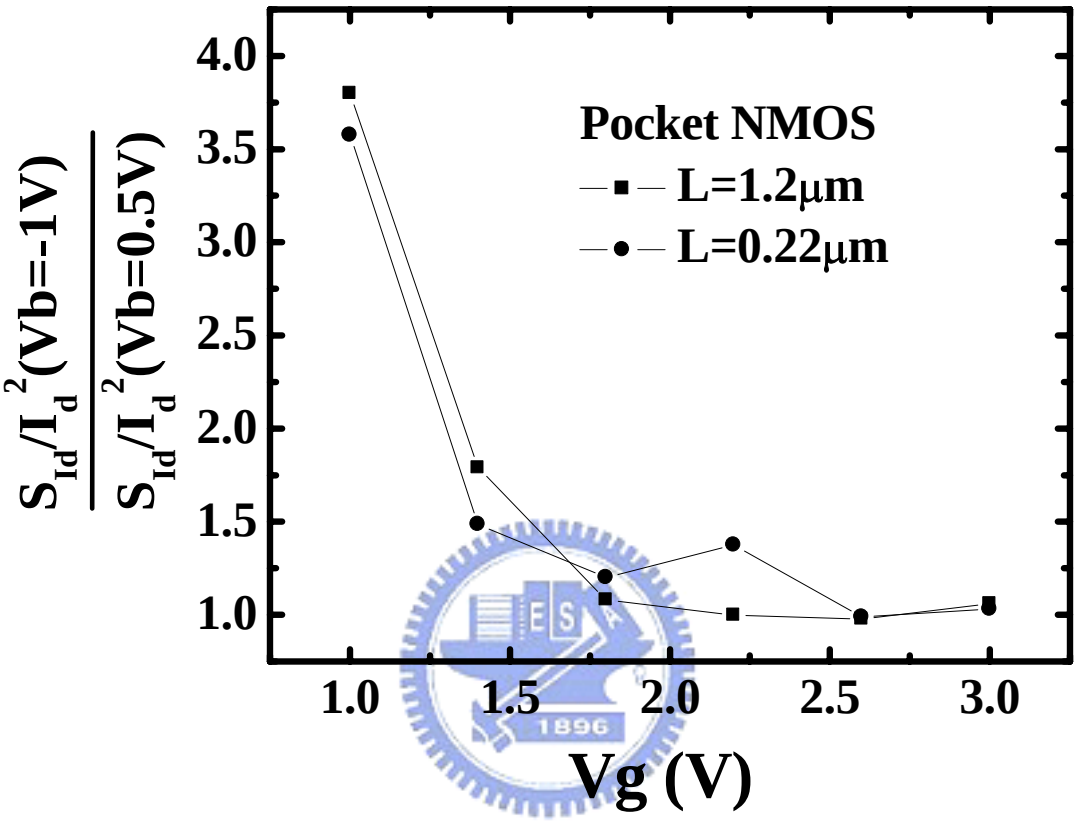


Fig. 4-11 Comparison of substrate bias effect for different gate voltage in pocket n-MOSFETs with L=1.2μm and 0.22μm.

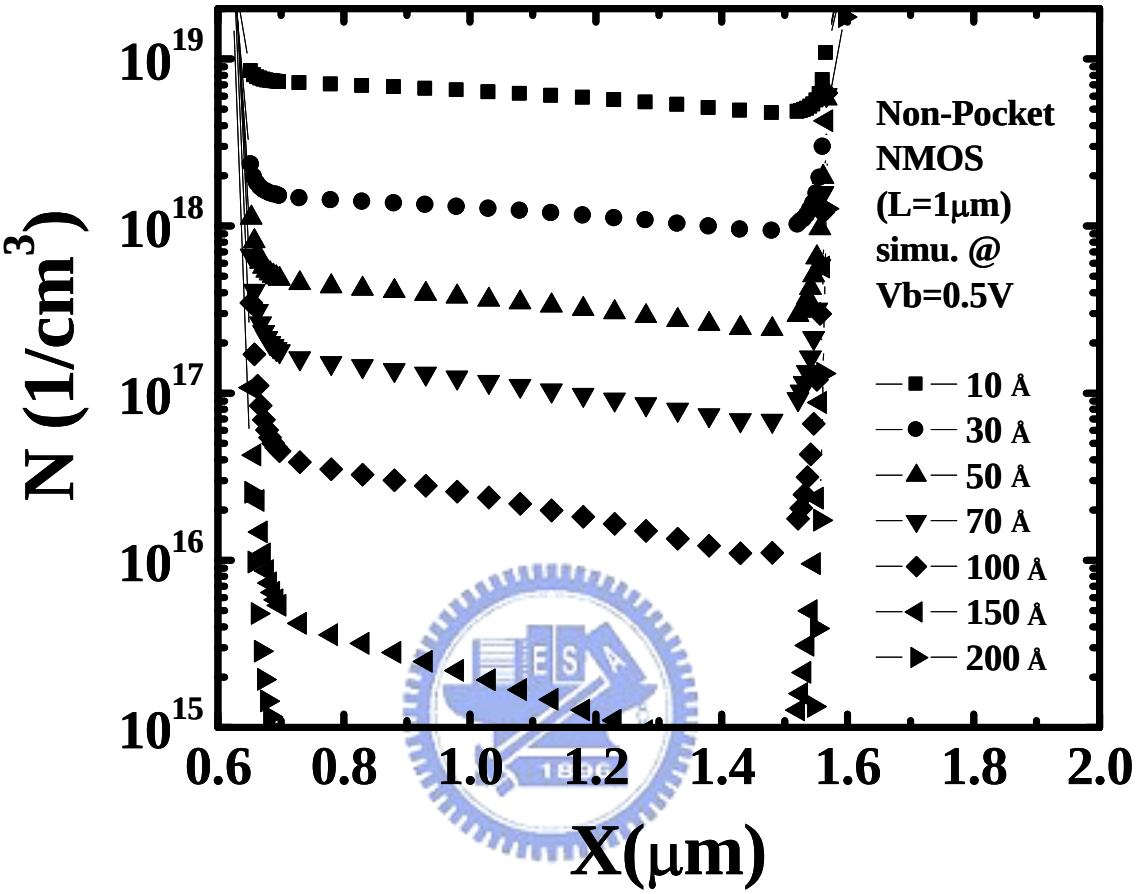


Fig. 4-12 Simulated carrier distribution of a non-pocket n-MOSFET at different depth in the channel region. The channel length is 1μm. The substrate bias is 0.5V.

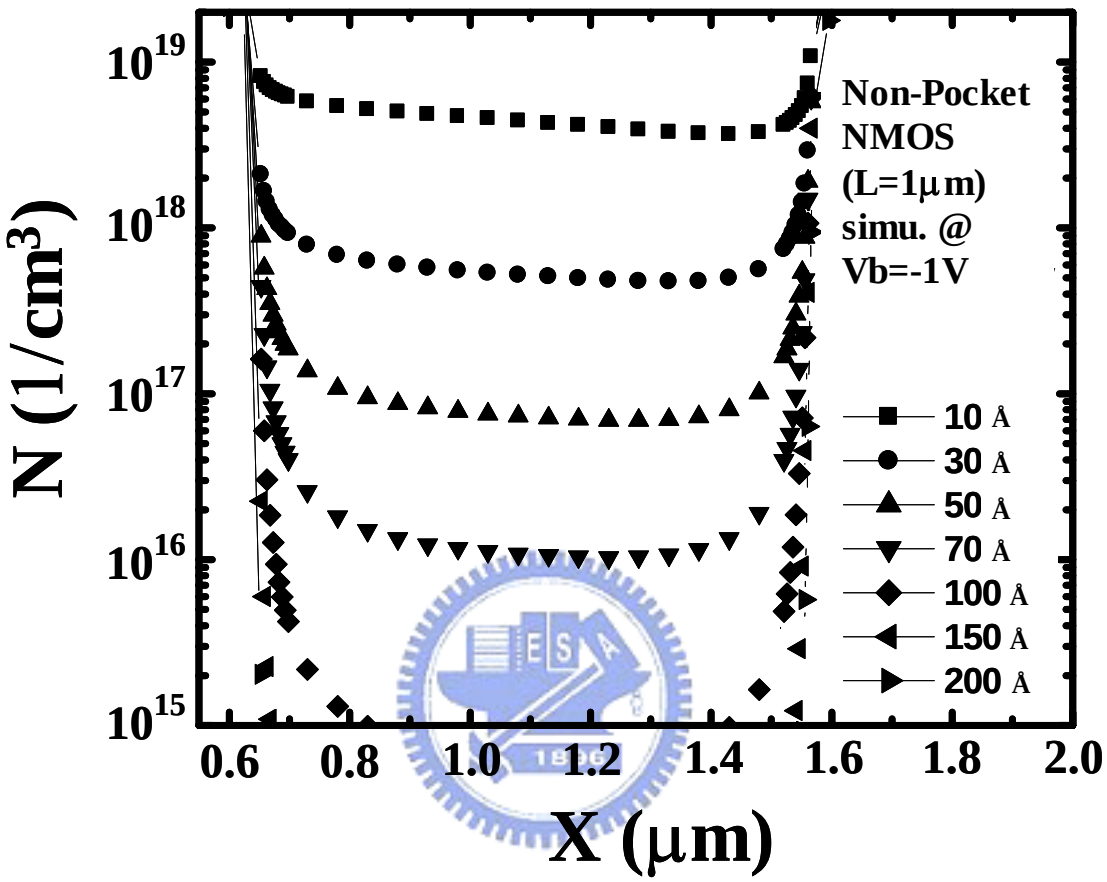


Fig. 4-13 Simulated carrier distribution of a non-pocket n-MOSFET at different depth in the channel region. The channel length is 1μm. The substrate bias is -1V.

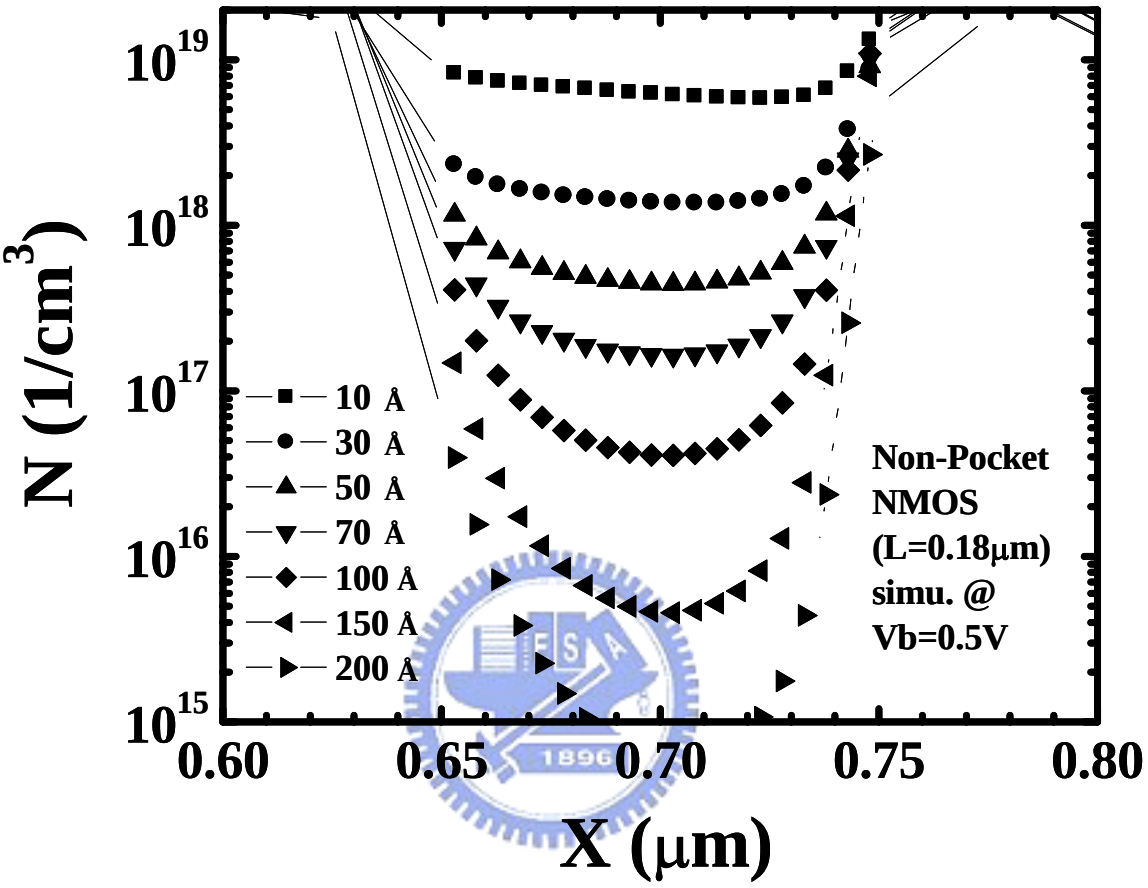


Fig. 4-14 Simulated carrier distribution of a non-pocket n-MOSFET at different depth in the channel region. The channel length is 0.18μm. The substrate bias is 0.5V.

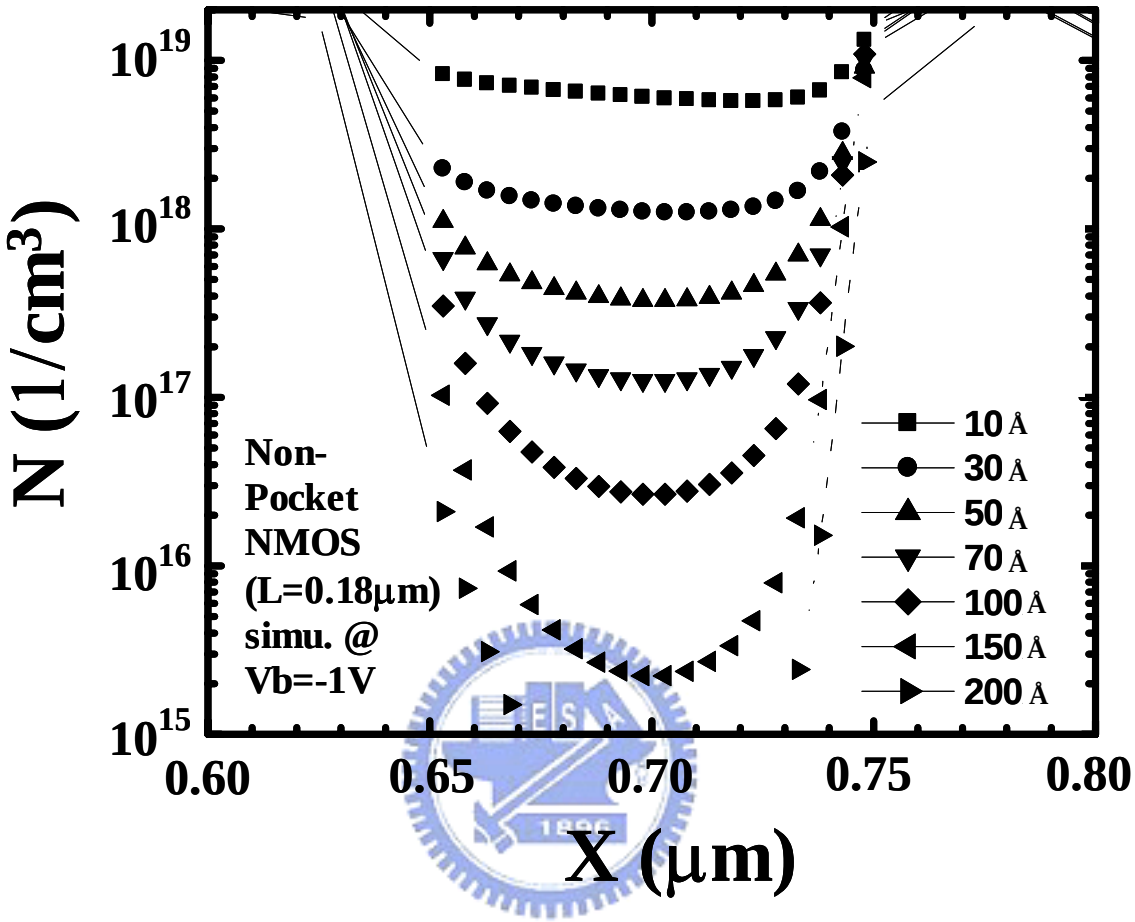


Fig. 4-15 Simulated carrier distribution of a non-pocket n-MOSFET at different depth in the channel region. The channel length is 0.18μm. The substrate bias is -1V.

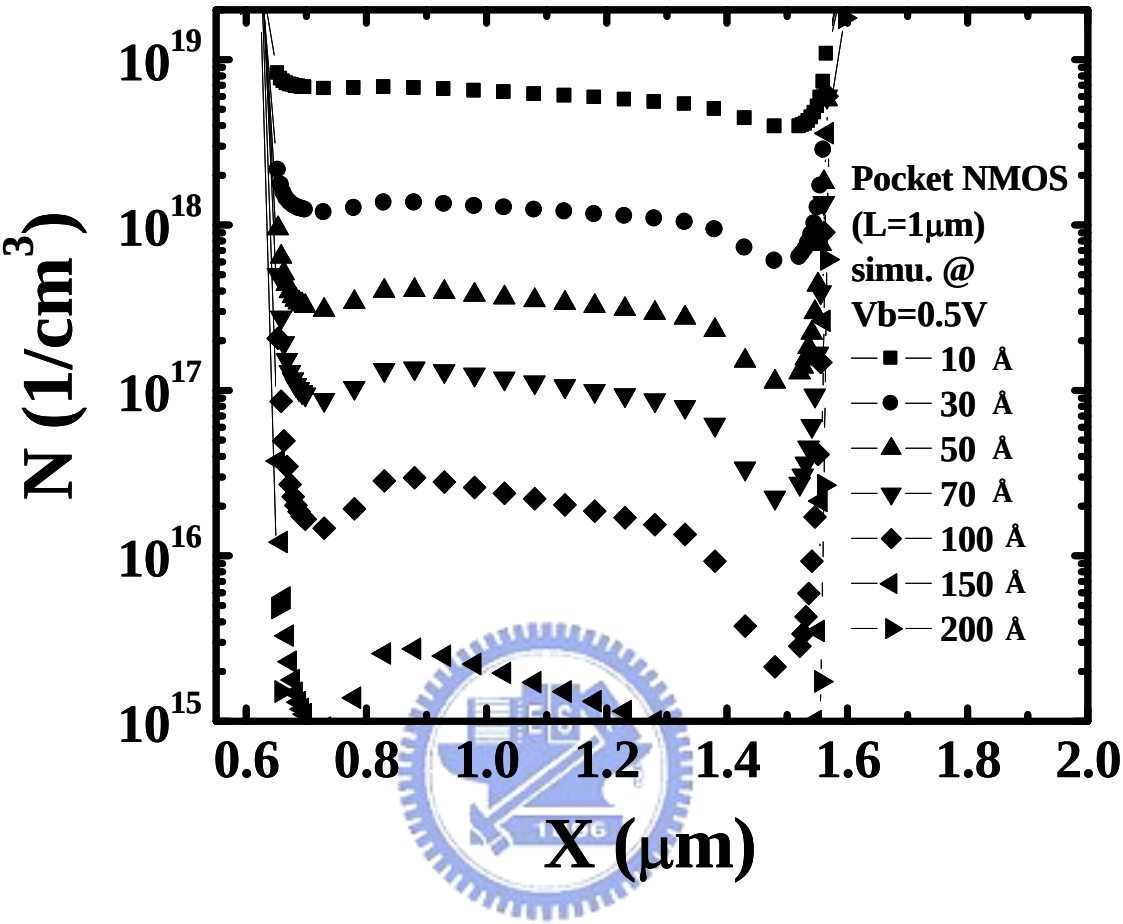


Fig. 4-16 Simulated carrier distribution of a pocket n-MOSFET at different depth in the channel region. The channel length is 1μm. The substrate bias is 0.5V.

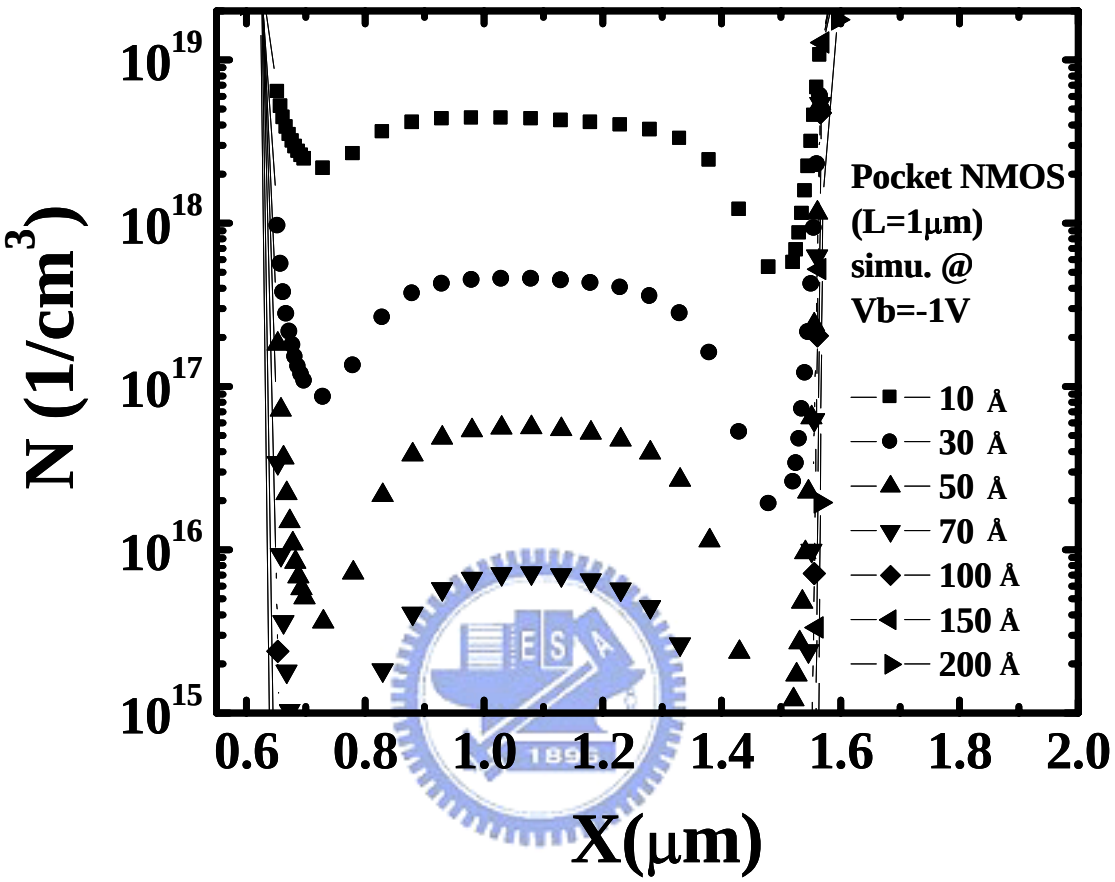


Fig. 4-17 Simulated carrier distribution of a pocket n-MOSFET at different depth in the channel region. The channel length is 1μm. The substrate bias is -1V.

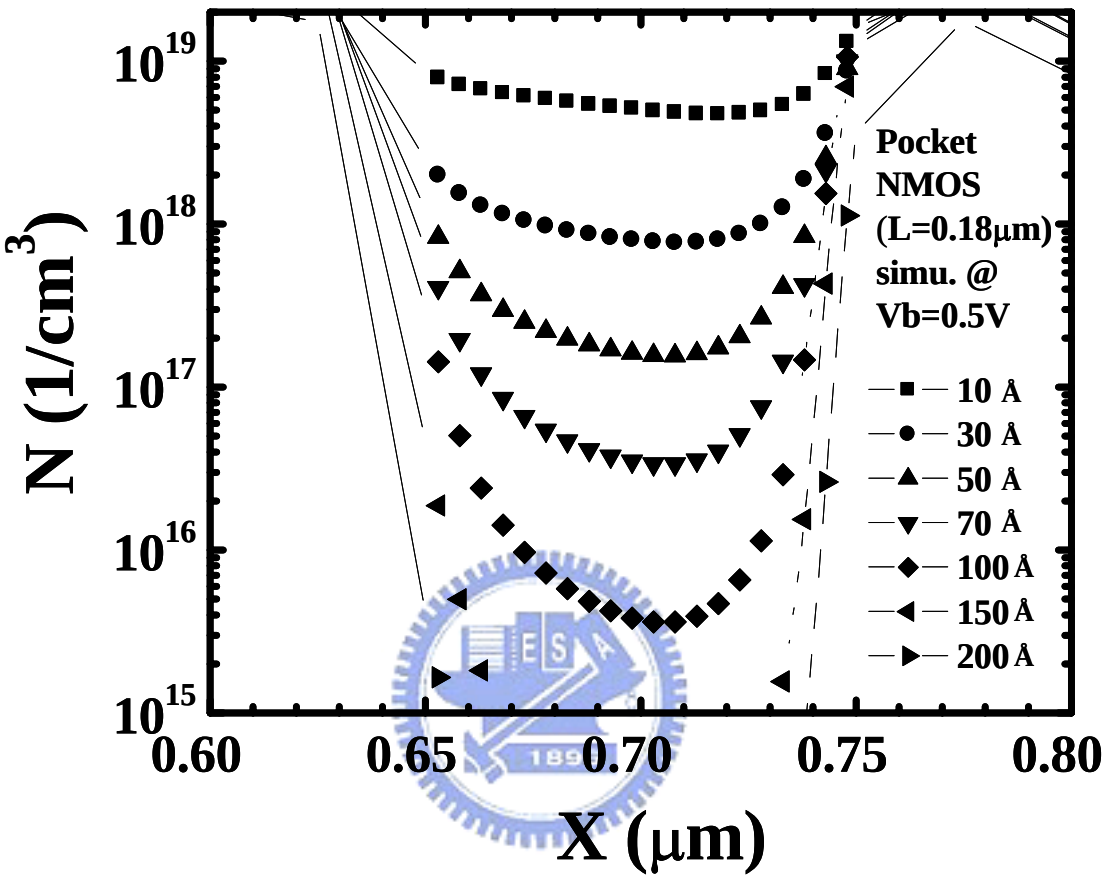


Fig. 4-18 Simulated carrier distribution of a pocket n-MOSFET at different depth in the channel region. The channel length is 0.18μm. The substrate bias is 0.5V.

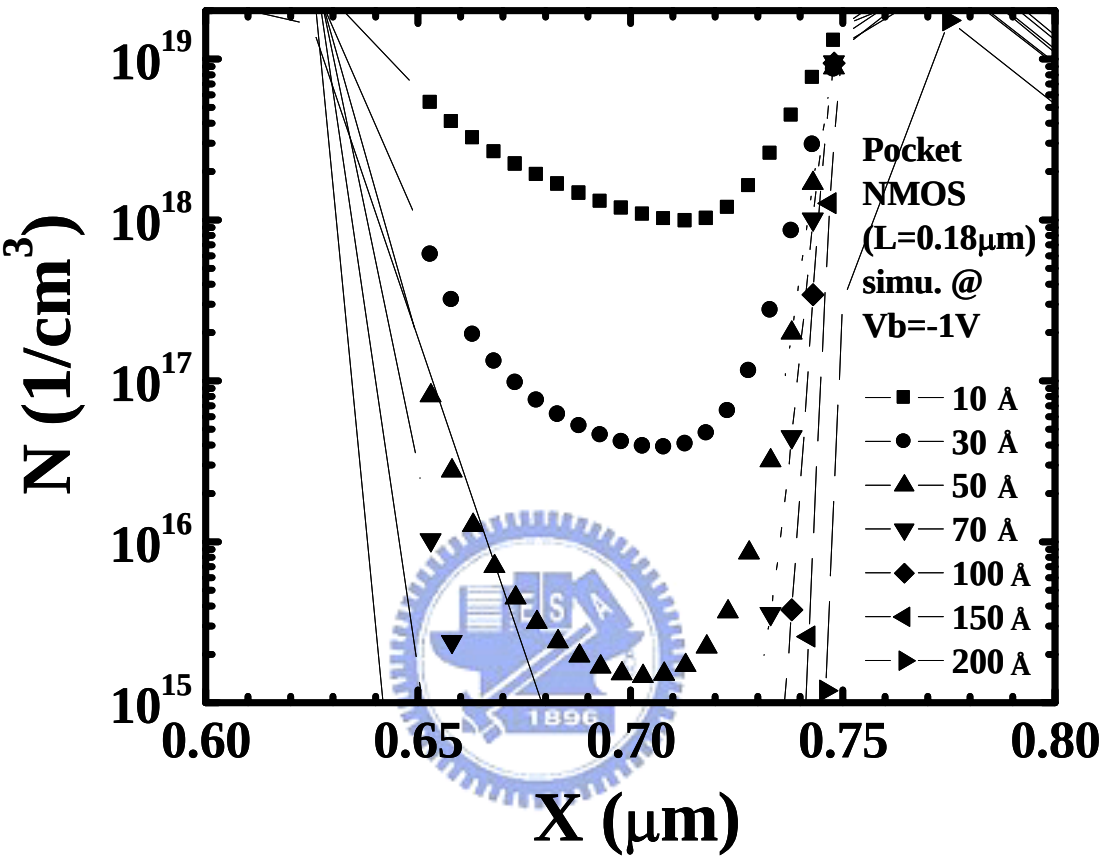


Fig. 4-19 Simulated carrier distribution of a pocket n-MOSFET at different depth in the channel region. The channel length is 0.18μm. The substrate bias is -1V.

Chapter 5
Valence-Band Tunneling Induced Low Frequency Noise in Ultra-Thin Oxide n-MOSFETs

5.1 Introduction

The CMOS technology, which possesses the advantages of low cost, high integration, and low power, is finding more and more important applications in the area of mixed mode and RF ICs. As compared with bipolar transistors, CMOS devices exhibit large noise, especially in the low frequency domain where flicker noise is dominant [5-1]. Drain current flicker noise has become one of the key considerations in device geometrical scaling since it will affect the signal-to-noise ratio in operational amplifiers and in analog/digital and digital/analog converters. In addition, low frequency flicker noise can be up-converted to undesired phase noise in RF circuits [5-2] and limits the channel spacing in communication systems. In order to reduce low frequency noise, the physical origin of flicker noise in today's CMOS devices with gate oxide in direct tunneling regime should be further explored.

The origin of low frequency flicker noise in MOSFETs with relatively thick gate oxides has been extensively studied. A unified noise model [5-3,4] based on oxide charge tunnel trapping and de-trapping has been adopted. The carrier number and mobility fluctuation induced from trapped oxide charges is thought to be the source of flicker noise. In addition, some studies showed that the low frequency noise may result from charge emission and capture at interface traps in weak inversion condition or in the very high frequency regime of noise power spectral density [5-5]. As gate oxide thickness is scaled into direct tunneling domain, oxide trap density should be much reduced. In addition, channel electrons would likely tunnel through an ultra-thin gate oxide directly without being captured by oxide traps. However, the low frequency noise in ultra-thin oxide CMOS devices still exhibits a 1/f spectrum and possesses a significant level [5-6,7]. The traditional oxide charge tunnel

trapping and de-trapping concept seems no longer suitable to explain the noise behavior in ultra-thin oxide MOSFETs. Furthermore, some study in ultra-thin gate oxide FD/PD SOI MOSFETs also demonstrates that "linear kink effect (LKE)" induced by valence-band electron tunneling would increase the low frequency noise spectral density S_I. Similar as for impact-ionization related noise overshoot (perturbation of the body voltage through body impedance), it is observed that the nature of the spectrum changes from 1/f-like to Lorentzian in the LKE region [5-8]. However, the physical mechanism of low frequency noise in ultra-thin gate oxide devices is still unclear.

5.2 Basic Theory of RTS

The time domain presentation of low frequency noise is known as random telegraph signal (RTS) and has been studied in past decades [5-9,10,11,12]. Due to a single charge trapping and de-trapping in a small area device, RTS exhibits two levels. The upper level corresponds to an empty trap, i.e., no electron occupation, and the duration of time is denoted by τ_H. The lower level corresponds to an electron occupied state and is denoted by τ_L. In many cases, τ_H corresponds to the time it takes to capture a carrier, while carrier release (emission) from traps governs τ_L [5-13]. Fig. 5-1(a) shows the typical RTS in the drain current of an n-MOSFET (W/L=0.32μm/0.12μm). Fig. 5-1(b) shows the sampling number versus the drain current, while the total sampling number for a given time is 5×10^4s. Moreover, the current interval between the two max numbers of the drain current can be used to extract ΔI and the two peaks of the drain current represents clearly two-level RTS.

5.3 Device Information

In this work, the low frequency noise in a 15Å gate oxide n-MOSFET is investigated. The electron trapping and de-trapping times (τ_H and τ_L) are characterized from RTS in a small area n-MOSFET. The normalized noise power spectral density (S_{Id}/I_d^2) is measured as a

monitor of drain current noise, which is considered as a fair index because of the normalization to the drain current. In addition, the RTS time constants and noise power spectral density in n-MOSFETs with 33Å gate oxide are also characterized for comparison. The drain bias in RTS and noise measurement in this study is 0.1V to ensure a uniform charge distribution in the channel.

5.4 Results and Discussion

5.4.1 Abnormal Noise Characteristics in Frequency Domain

Fig. 5-2 shows the gate oxide thickness (t_{ox}) dependence of the normalized noise power spectrum density at f=100Hz. Due to a statistical nature of flicker noise, devices with too small area may exhibit a large fluctuation range in noise [5-14]. Therefore, the measured devices have a larger area (W/L=10μm/1μm) and each noise measurement data point represents an average of 5 devices. The noise is measured in the linear operation region (Vd=0.2V, $V_{overdrive}$=0.7V) to make sure the channel carrier distribution is uniform. As shown in Fig. 1, the S_{Id}/I_d^2 decreases as the gate oxide thickness reduces from 65Å to 22Å. This result agrees with the published unified flicker noise model [5-3,4] because oxide trap density is reduced in thinner oxides. However, as gate oxide thickness continuously scales down, the noise level exhibits an abnormal increase. Fig. 5-3 compares the temperature dependence of the 1/f noise in large area n-MOSFETs n-MOSFETs (W/L=10μm/1μm) with t_{ox}=15Å and 65Å. Strong temperature effect in the 15Å oxide device is observed.

The noise characteristic in a small area ultra-thin oxide n-MOSFET with a single trap time constant is first analyzed. Fig. 5-4 shows the measured and calculated noise power spectral density in a W/L=0.16μm/0.12μm n-MOSFET. The gate oxide thickness is 15Å. The noise has Lorentzian-like spectral distribution [5-15], characterized by a constant power spectral density at low frequencies and a roll-off with f^{-2} for high frequencies. The cut-off or

corner frequency (f_c) corresponds to the 3-dB point of the spectrum and is related to the reciprocal characteristic time (t) of the underlying trap ($f_c=1/2\pi\tau$). The calculated result is based on the τ ($1/\tau=1/\tau_H+1/\tau_L$) extracted from associated RTS (will be shown later) and is in good agreement with the measured power spectral density.

In order to investigate the excess noise source in the 14Å oxide n-MOSFETs, the temperature dependence of the noise characteristic in a small area device (W/L=0.36μm/0.12μm) with a single trap is analyzed. The measured noise exhibits a Lorentzian spectrum,

$$\frac{S_{id}}{I_d^{\,2}} \propto \frac{\tau}{1+(2\pi f\tau)^2} \tag{5-1}$$

as expected in a single trap device. Fig. 5-5 shows the temperature dependence of $(S_{Id}/I_d^2)\times$frequency versus frequency. The temperature varies from 25°C to 125°C. Obviously, as temperature increases, the trap time constant decreases, resulting in a higher corner frequency. Based on the Shockley-Read-Hall (SRH) statistics, the capture time constant can be described by:

$$\tau = \frac{1}{N\sigma_0 \upsilon_{th}} \cdot \exp\left(\frac{\Delta E_b}{kT}\right) \tag{5-2}$$

where ΔE_b is the energy barrier for the capture of an carrier and N is the carrier density. The linear behavior of the Arrhenius plot shown in Fig. 5-6 reveals that the source of the noise is related to interface trap assisted generation/recombination, which follows the SRH process.

Fig. 5-7 shows the gate voltage (Vg) dependence of f_c. Obviously, there exist two groups of trap frequency (or two trap energy levels) with one (E_{t1}) observed in weak inversion (Vg<0.9V) and the other (E_{t2}) in strong inversion (Vg>1V). Furthermore, significant substrate current is noticed in the 15Å oxide device in strong inversion regime (Vg>1V) in Fig. 5-8 because valence band electron tunneling from the Si substrate to the poly-gate occurs and generated holes flow to the substrate [5-15].

Fig. 5-9 illustrates valence electron tunneling induced substrate current and interface trap energy levels.

5.4.2 Analysis of RTS Behavior in Time Domain

The gate bias dependence of corresponding RTS is then investigated. Fig. 5-10 shows typical RTS patterns in a small area (W/L=0.16μm/0.12μm) 15Å gate oxide n-MOSFET in weak inversion (Vg<0.9V). As can be seen, τ_L increases and τ_H decreases as Vg increases from 0.65V to 0.9V. Noticeably, RTS vanishes at Vg=0.9V. Fig. 5-11 shows the Vg dependence of average τ_L and τ_H (extracted from RTS). The τ_L and τ_H in weak inversion correspond to the electron emission and capture times at the interface trap E_{t1}, as illustrated in Fig. 5-12(a). As Vg increases, τ_H decreases and τ_L increases because of a larger channel electron population and thus a smaller electron capture time. Our result here is consistent with the findings for thicker gate oxides in previous publications [5-9]. In contrast, Fig. 5-13 shows the RTS patterns in strong inversion from Vg=1.0V to 1.6V. The RTS is still undetectable at Vg=1V and re-appears for Vg>1V. Fig. 5-14 shows the Vg dependence of average τ_L and τ_H extracted from the RTS. Interestingly, we find that the RTS patterns in strong inversion (Vg>1V) exhibit an opposite trend. The Vg dependence of τ_H and τ_L in strong inversion is opposite to that in weak inversion. It should be mentioned that other study [5-16] could also explain the observed RTS behavior based on the assumption of mobility fluctuation domination. However, the ΔId/Id characteristic (mentioned in [5-16]) in our RTS results shows that the RTS behavior is still on the regime where number fluctuation dominates. The real cause of the inversed RTS behavior should be further studied.

5.4.3 Valence-Band Tunneling Induced Noise

In order to find out the opposite charge trapping and de-trapping behavior from weak inversion to strong inversion, the trap electron occupation factor (f_t) is analyzed. The f_t can be

evaluated as follows:

$$f_t = \frac{\tau_L}{\tau_L + \tau_H} \quad (1)$$

Fig. 5-15(a) shows f_t versus Vg from weak inversion to strong inversion. In weak inversion regime (i.e., Vg<0.9V), f_t increases with Vg because of an increased channel electron population. As f_t increases to 1, RTS is undetectable since the trap is always occupied by an electron. In strong inversion regime (i.e., Vg>1V), f_t declines from unity with increasing Vg. This means, at a larger Vg, although the energy level of the interface trap is deeper with respect to the electron Fermi level, the chance of the trap being occupied by an electron becomes smaller. This result is quite different from the equilibrium case that f_t should increase as the trap energy becomes more negative with respect to the Fermi level (see Eq. (2) where E_t is the trap energy, E_f is the Fermi level).

$$f_t(E_t) = \frac{1}{1 + \exp\left(\frac{E_t - E_f}{kT}\right)} \quad \text{under thermal equilibrium} \quad (2)$$

In addition to f_t, Fig. 5-15(b) shows the S_{Id}/I_d^2 (measured at f=100Hz in a small area n-MOSFET) from weak inversion to strong inversion. The S_{Id}/I_d^2 has a peak around f_t ~0.5 for Vg from 0.6V to 1V. As f_t approaches unity, the RTS vanishes and the S_{Id}/I_d^2 reduces because electrons always occupy the trap. However, the f_t begins to decrease as valence band electron tunneling occurs (Vg>1V). Thus, the RTS re-appears and the S_{Id}/I_d^2 reaches another peak.

The possible explanation for the abnormal noise behavior in strong inversion is illustrated in Fig. 5-12(b). In strong inversion regime, a large Vg causes strong valence electron tunneling and leaves more holes behind in the channel. τ_H and τ_L then correspond to electron capture time and hole capture time respectively, as illustrated in Fig. 5-12(b). Because of the increased channel hole concentration at a larger Vg, τ_L is smaller. The non-equilibrium carrier distribution also results in the splitting of electron and hole quasi

Fermi-levels. An interface trap (E_{t2}) between the two quasi Fermi levels serves as the recombination center of electrons and holes. Thus, the local electron concentration in the vicinity of the trap is reduced and τ_H increases. The increase of τ_H and the decrease of τ_L lead to a reduced f_t. The second peak of S_{Id}/I_d^2 in strong inversion condition (Vg>1V) in Fig. 5-15(b) therefore can be well explained.

For comparison, the f_t and S_{Id}/I_d^2 versus Vg in a thicker gate oxide (33Å) n-MOSFET are also characterized. The result is shown in Fig. 8. The f_t stays at unity in strong inversion. Neither RTS nor the second noise peak is observed in strong inversion since valence-bane tunneling is insignificant in such thick gate oxide devices.

5.5 Summary

Low frequency flicker noise in analog n-MOSFETs with 15Å gate oxide is investigated. A new noise generation mechanism resulting from valence band electron tunneling is proposed. In strong inversion condition, valence-band electron tunneling from Si substrate to poly-gate takes place and results in the splitting of electron and hole quasi Fermi-levels in the channel. The excess low frequency noise is attributed to electron and hole recombination at interface traps between the two quasi Fermi-levels. Random telegraph signal due to capture of channel electrons and holes is characterized in a small area device to support our model.

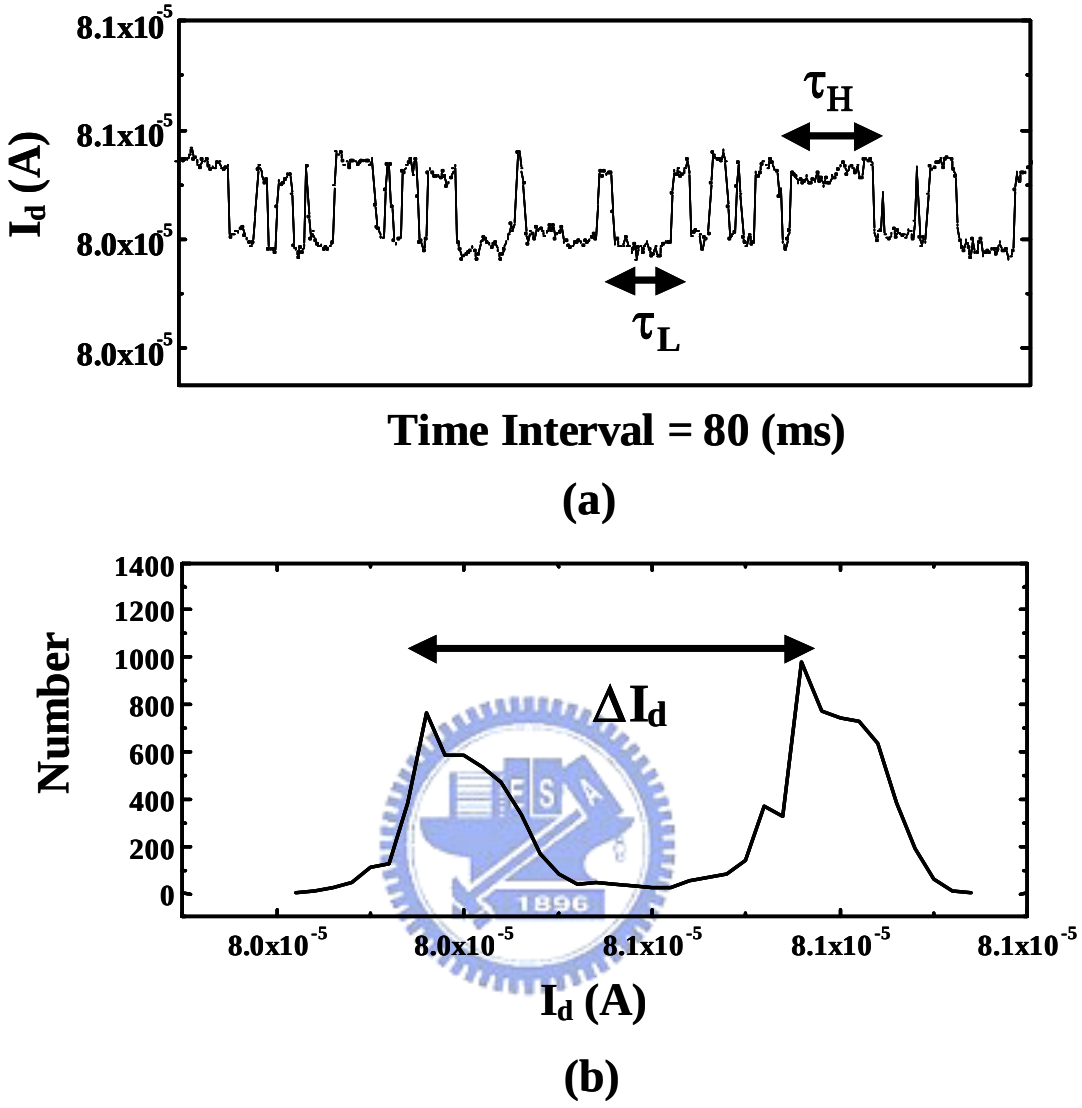


Fig. 5-1 (a) RTS in the drain current of an n-MOSFET (W/L=0.32μm/0.12μm) measured at Vg=0.9V, Vd=0.2V. (b) The ΔId can be extracted from the current interval between the two maximum number and the two peaks can be clearly symbolized as two-level RTS.

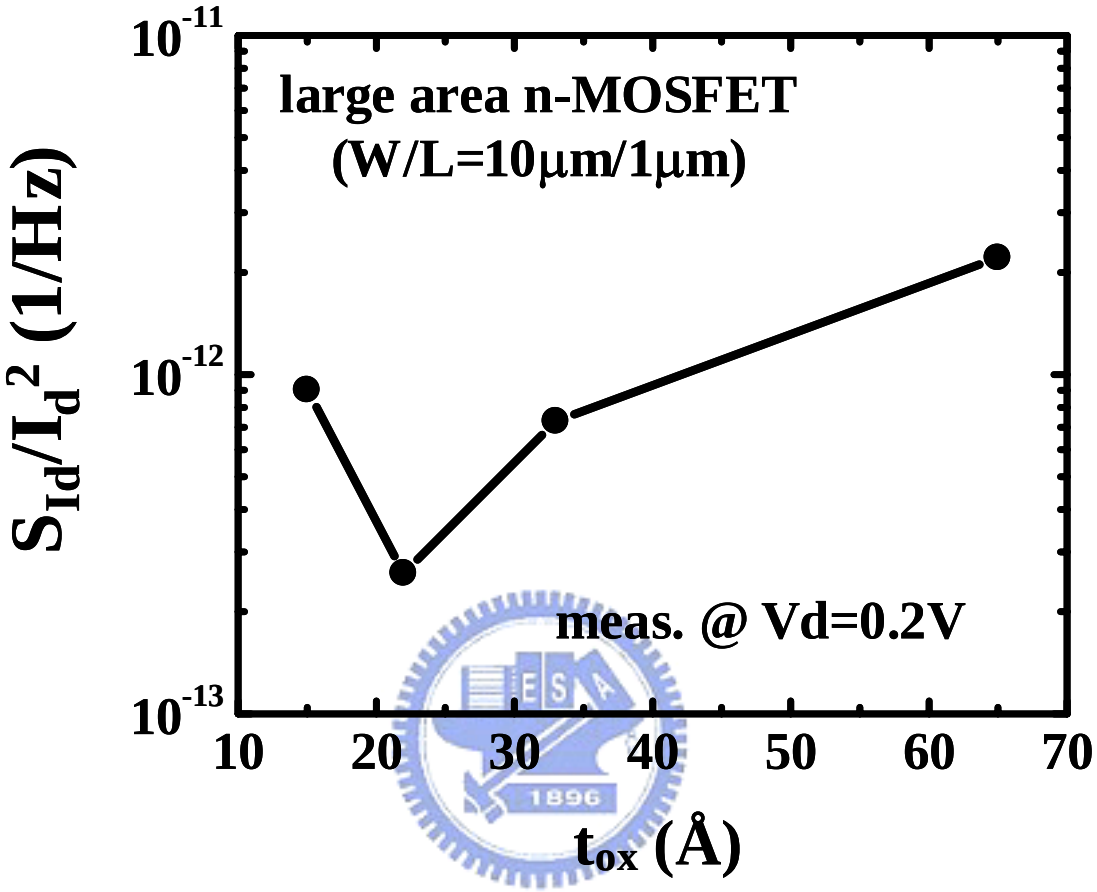


Fig. 5-2 Normalized noise power spectral density (at f=100Hz) versus gate oxide thickness in large area n-MOSFETs (W/L=10μm/1μm). The noise level has an abnormal increase in the 15Å oxide device.

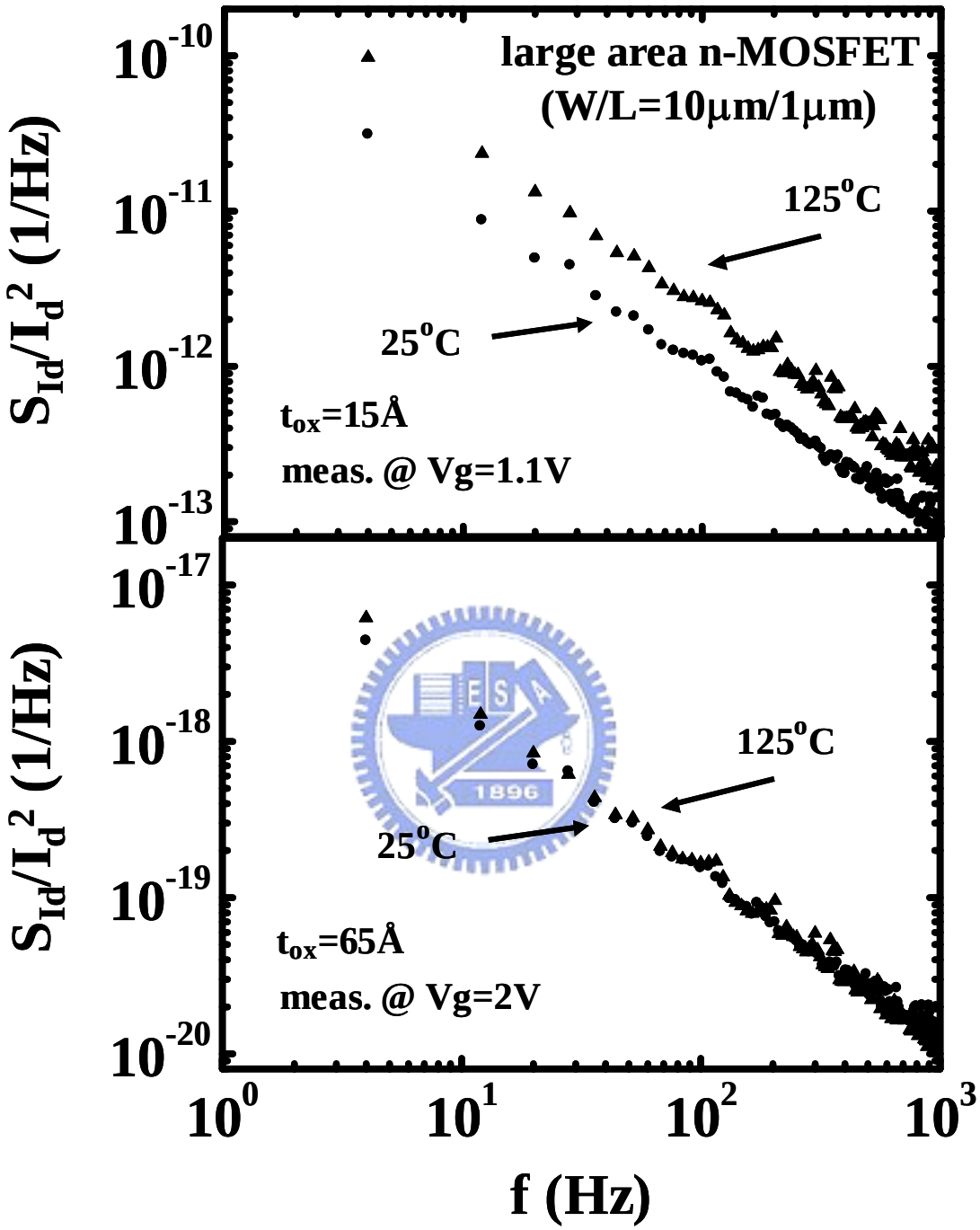


Fig. 5-3 Temperature dependence of the 1/f noise in t_{ox}=15Å and 65Å n-MOSFETs (W/L=10μm/1μm). The noise is measured at Vd=0.2V.

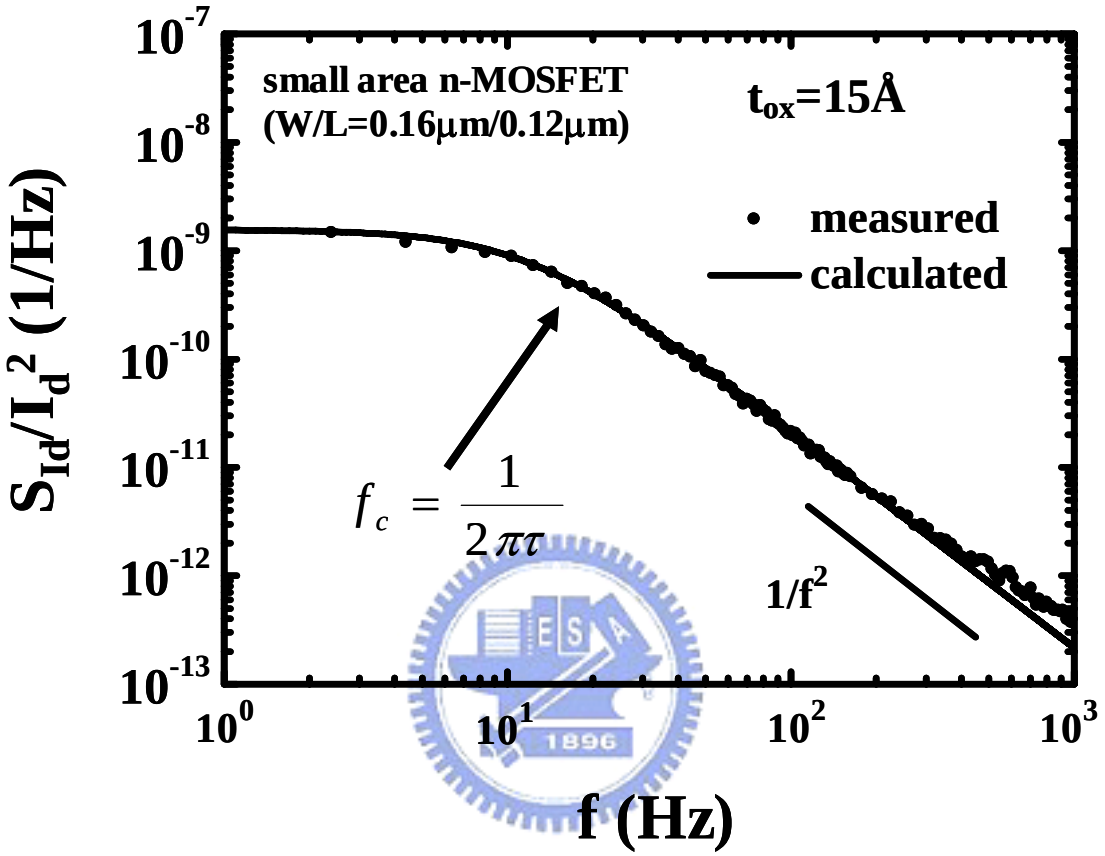


Fig. 5-4 Measured and calculated Lorentzian-like noise power spectral density of a small area n-MOSFET (W/L=0.16μm/0.12μm, t_{ox}=15Å). The noise is measured at strong inversion (Vd=0.2V, Vg=1.1V). The corner frequency (f_c) is also shown in the figure.

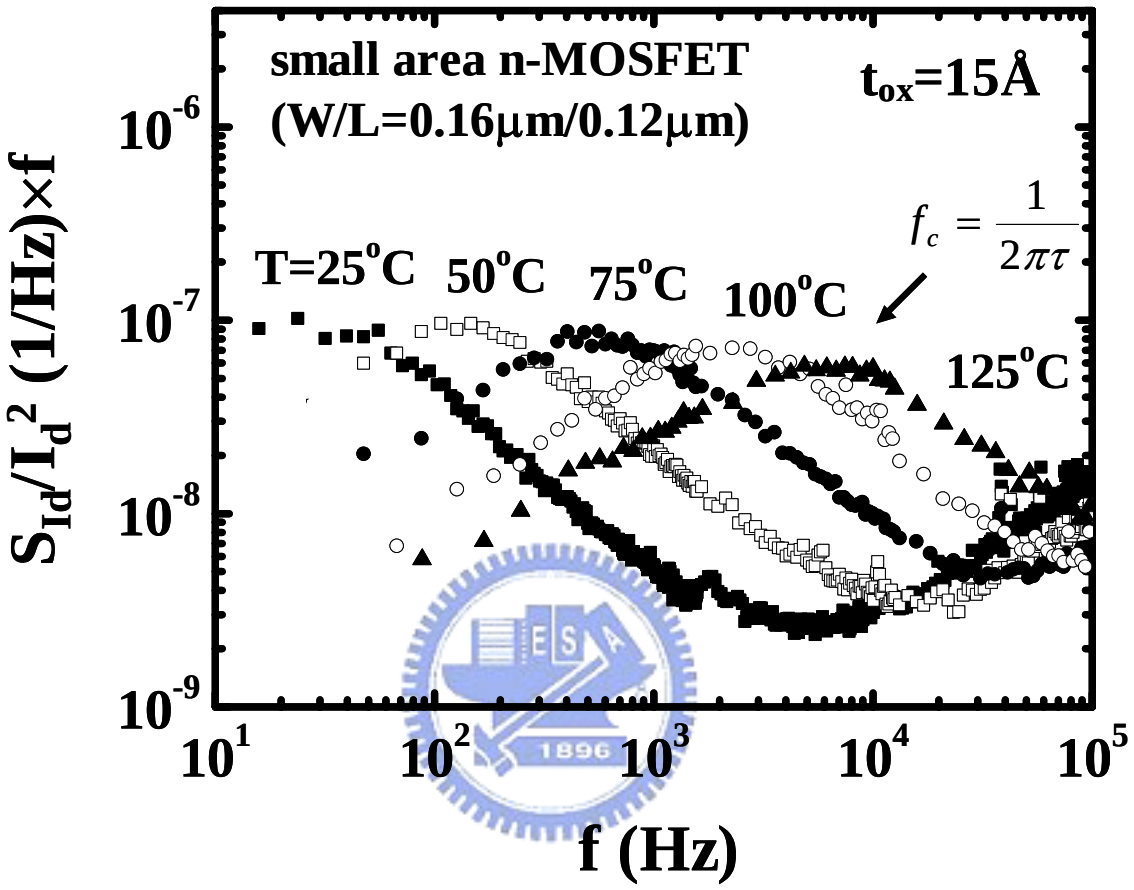


Fig. 5-5 Temperature dependence of the Lorentzian-like noise in a small area n-MOSFET (W/L= 0.16μm/0.12μm, t_{ox}=15Å). The noise is measured at strong inversion (Vd=0.2V, Vg=1.1V). The peak of S_{Id}/I_d^2×f corresponds to the corner frequency.

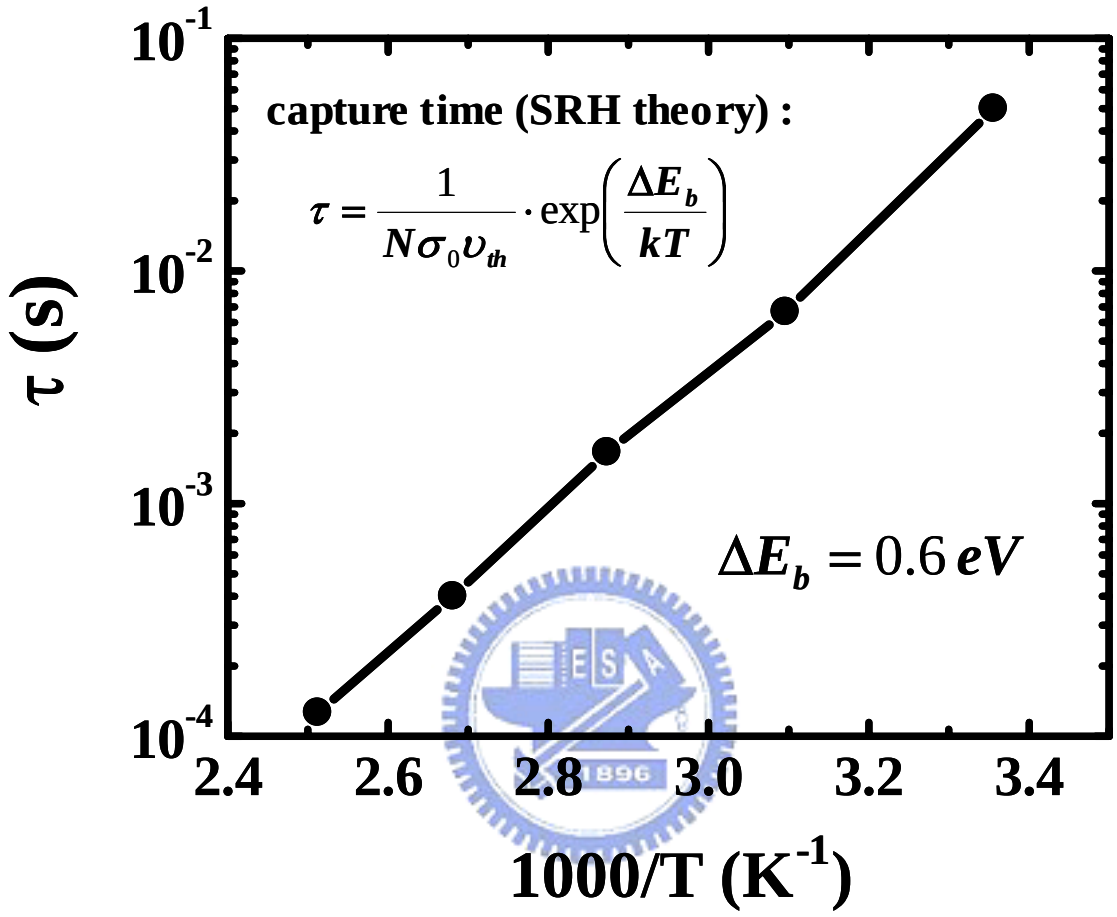


Fig. 5-6 Arrhenius plot of trap time constant versus 1000/T. The linear behavior of the Arrhenius plot shows that the source of the noise is related to carrier capture process by an interface trap.

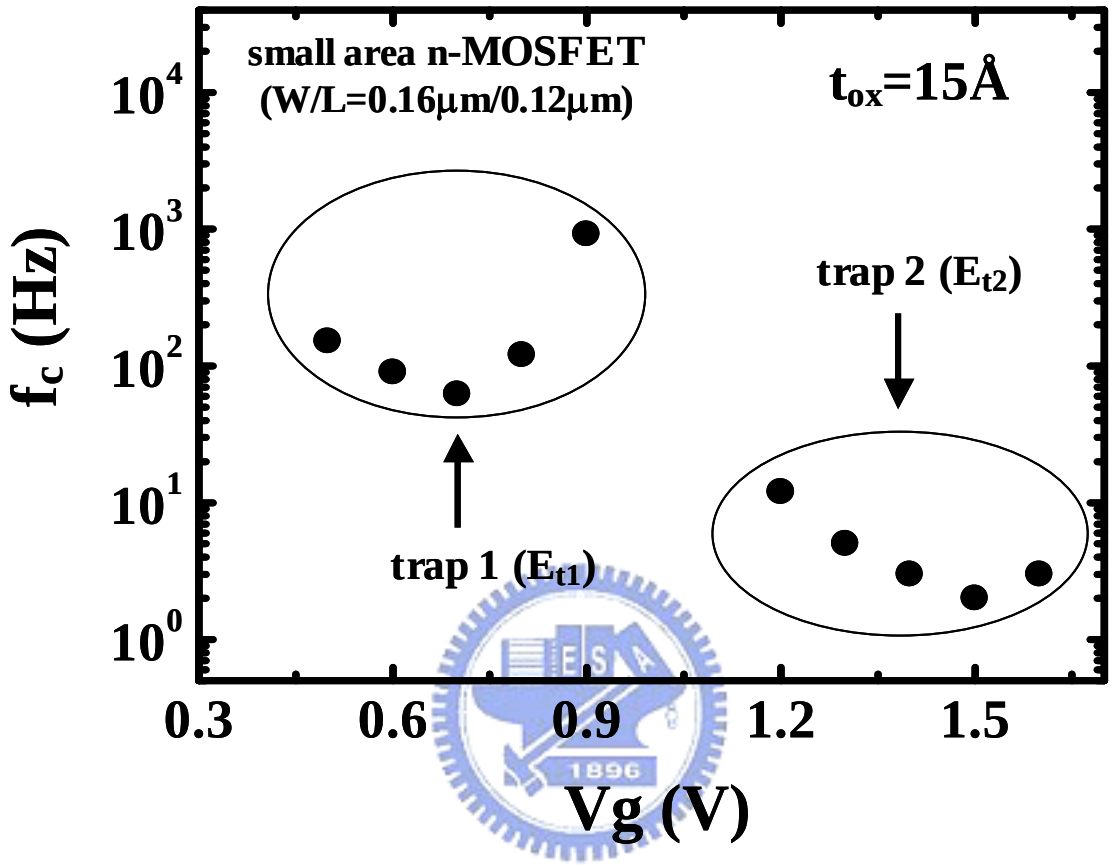


Fig. 5-7 The corner frequency versus gate voltage in a small area n-MOSFET (W/L=0.16μm/0.12μm, t_{ox}=15Å). A shallow trap (E_{t1}) is observed in weak inversion (Vg<0.9V) and a deep trap (E_{t2}) is in strong inversion (Vg>1.0V).

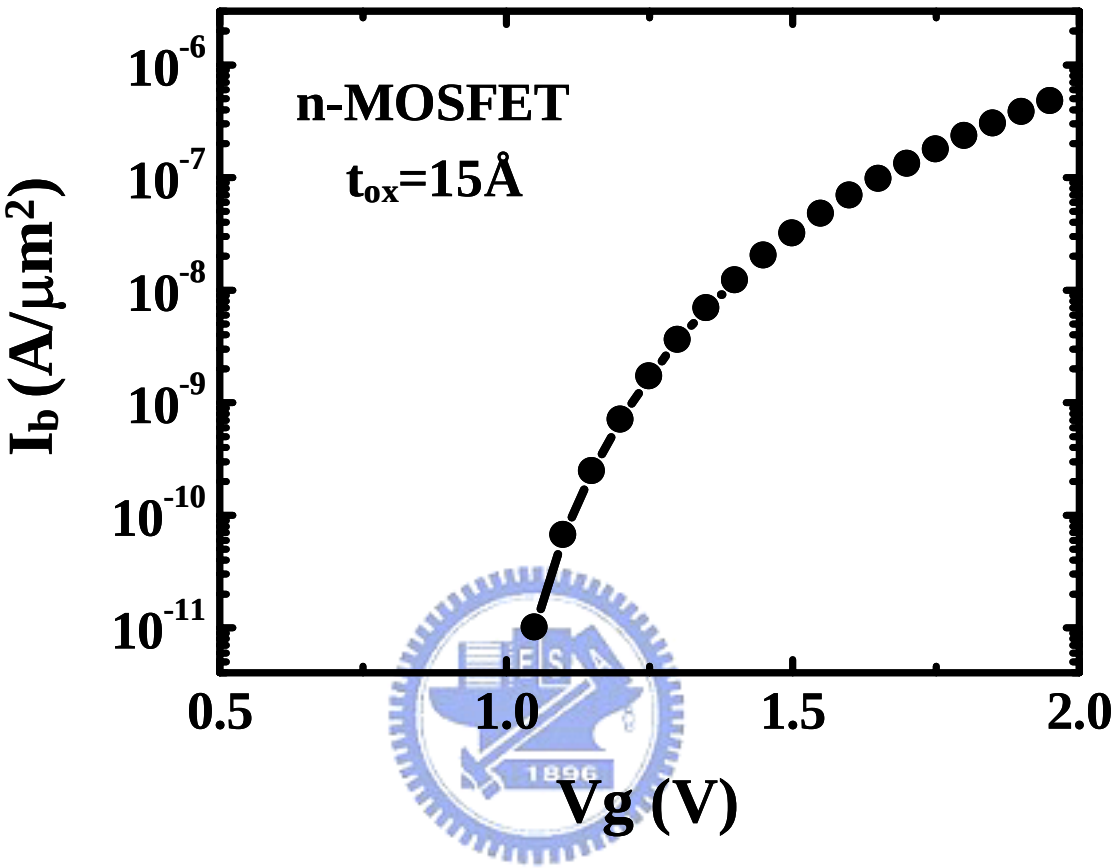


Fig. 5-8 The substrate current (I_b) versus gate voltage in n-MOSFETs. The I_b in the 15Å oxide device drastically increases with Vg>1.0V (strong inversion regime), which indicates the occurrence of valence-band electron tunneling.

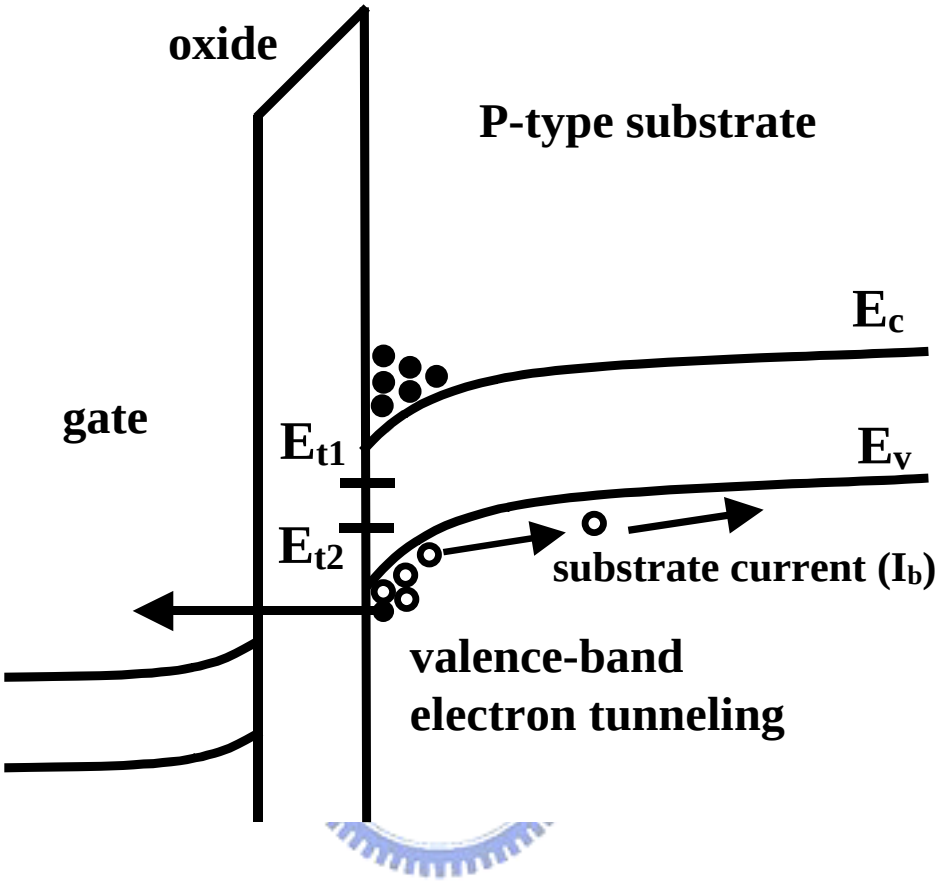


Fig. 5-9 Diagram of valence-band electron tunneling induced substrate current (I_b) in strong inversion. Traps E_{t1} and E_{t2} are also drawn.

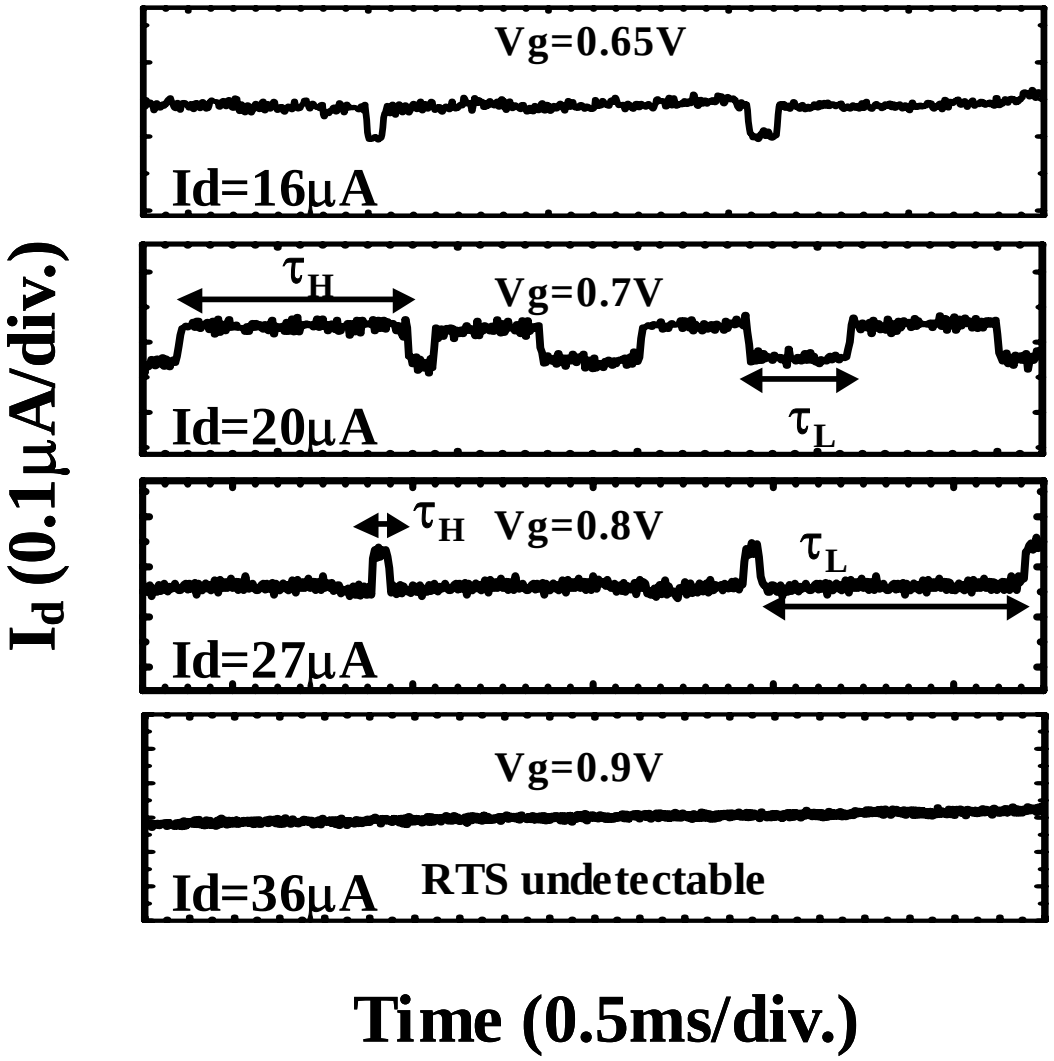


Fig. 5-10 The characteristics of two-level RTS at various gate voltages (in weak inversion) in a small area n-MOSFET (W/L=0.16μm/0.12μm, t_{ox}=15Å). RTS is undetectable at Vg=0.9V.

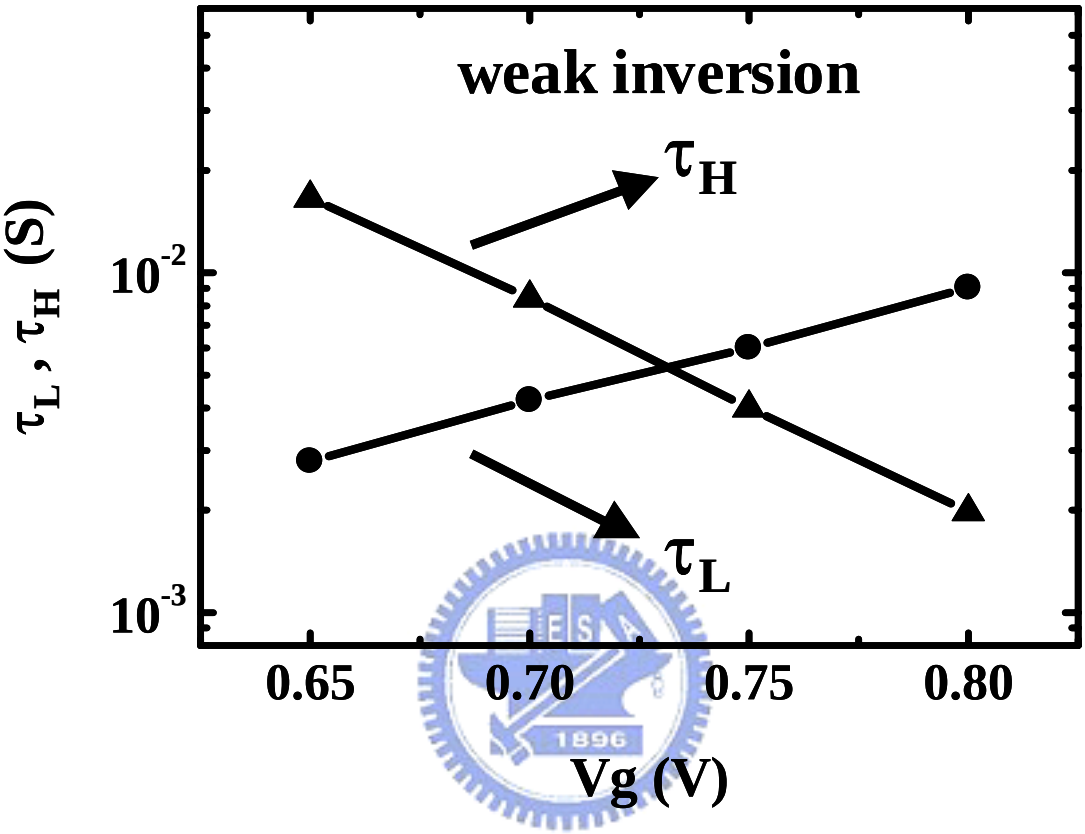
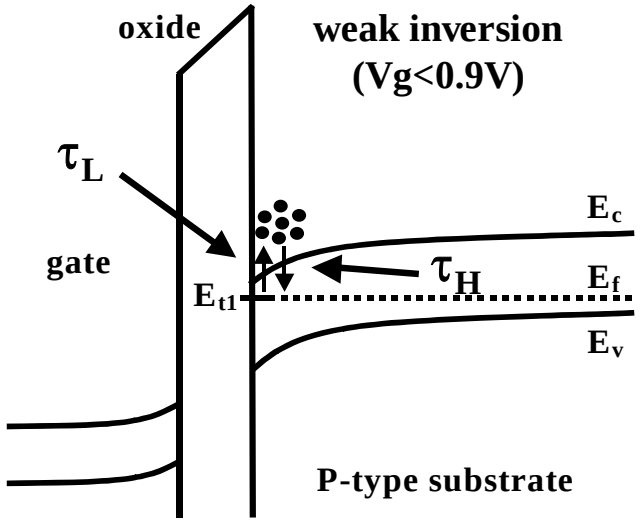
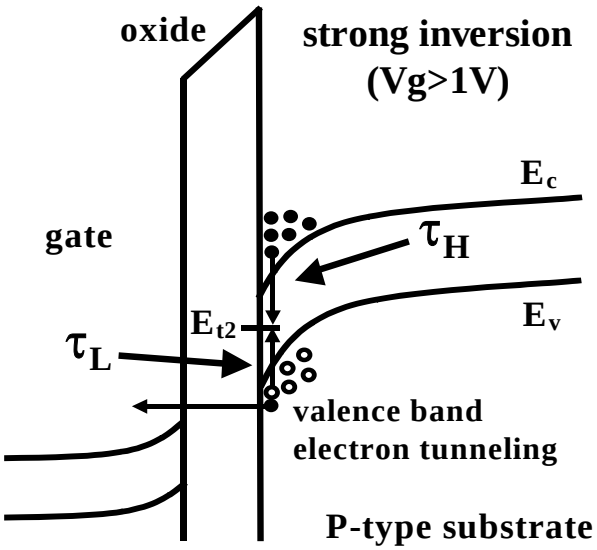


Fig. 5-11 Average τ_L and τ_H (extracted from RTS) versus gate voltage in weak inversion regime.



(a)



(b)

Fig. 5-12 (a) RTS in weak inversion condition. The RTS results from electron capture (τ_H) and electron emission (τ_L) at interface trap E_{t1}. (b) RTS in strong inversion condition. The RTS results from electron capture (τ_H) and hole capture (τ_L) at E_{t2}.

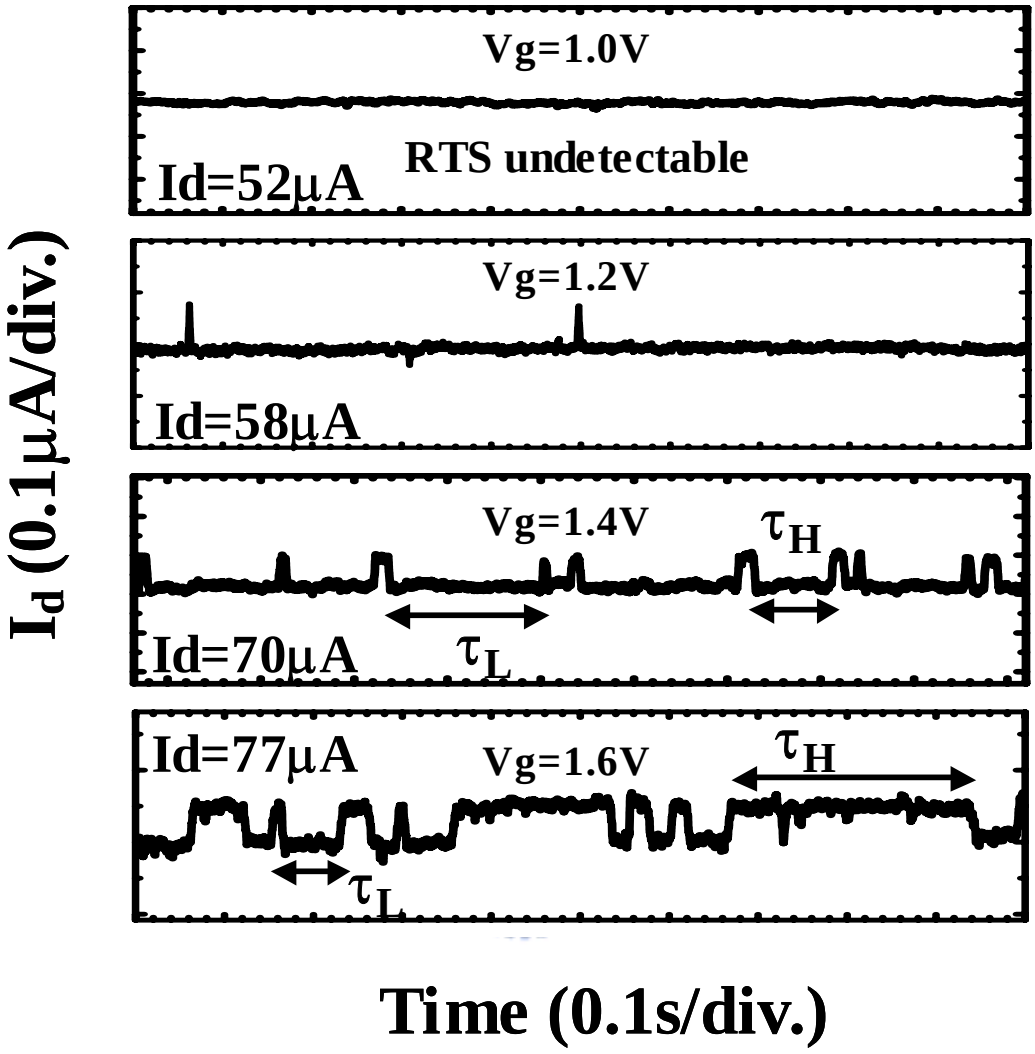


Fig. 5-13 The characteristics of two-level RTS at various gate voltages (in strong inversion regime) in a small area n-MOSFET (W/L=0.16μm/0.12μm, t_{ox}=15Å).

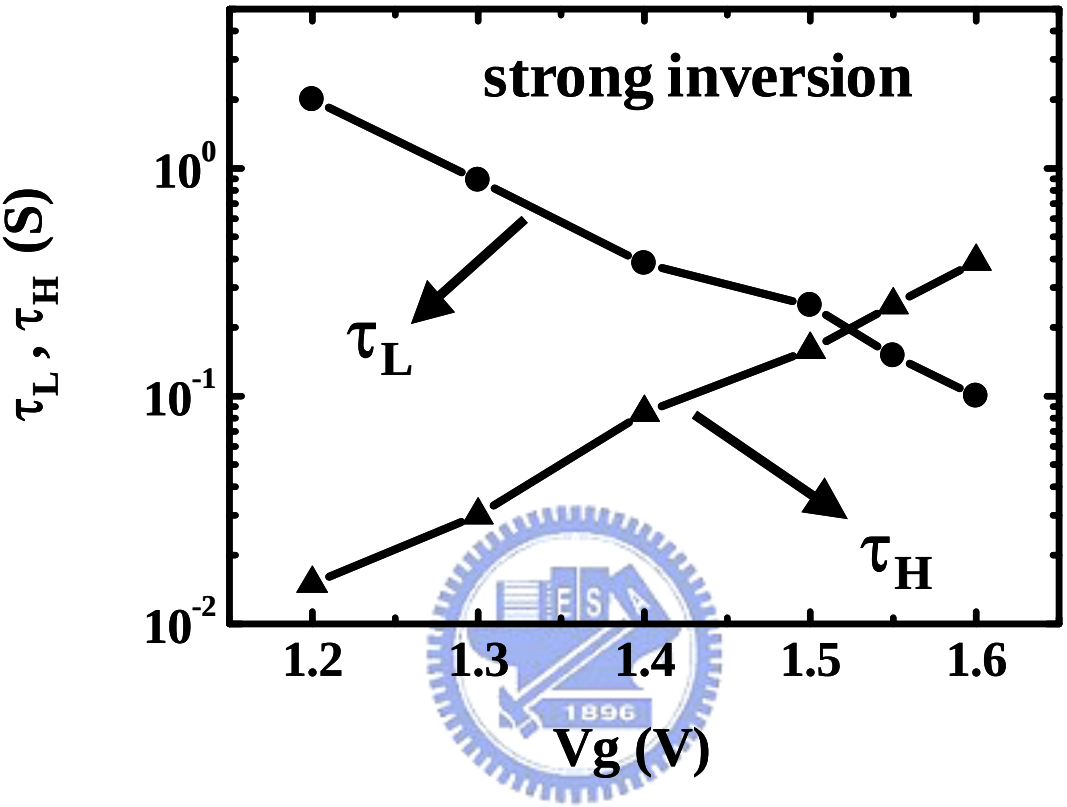


Fig. 5-14 Average τ_L and τ_H (extracted from RTS) versus gate voltage in strong inversion regime.

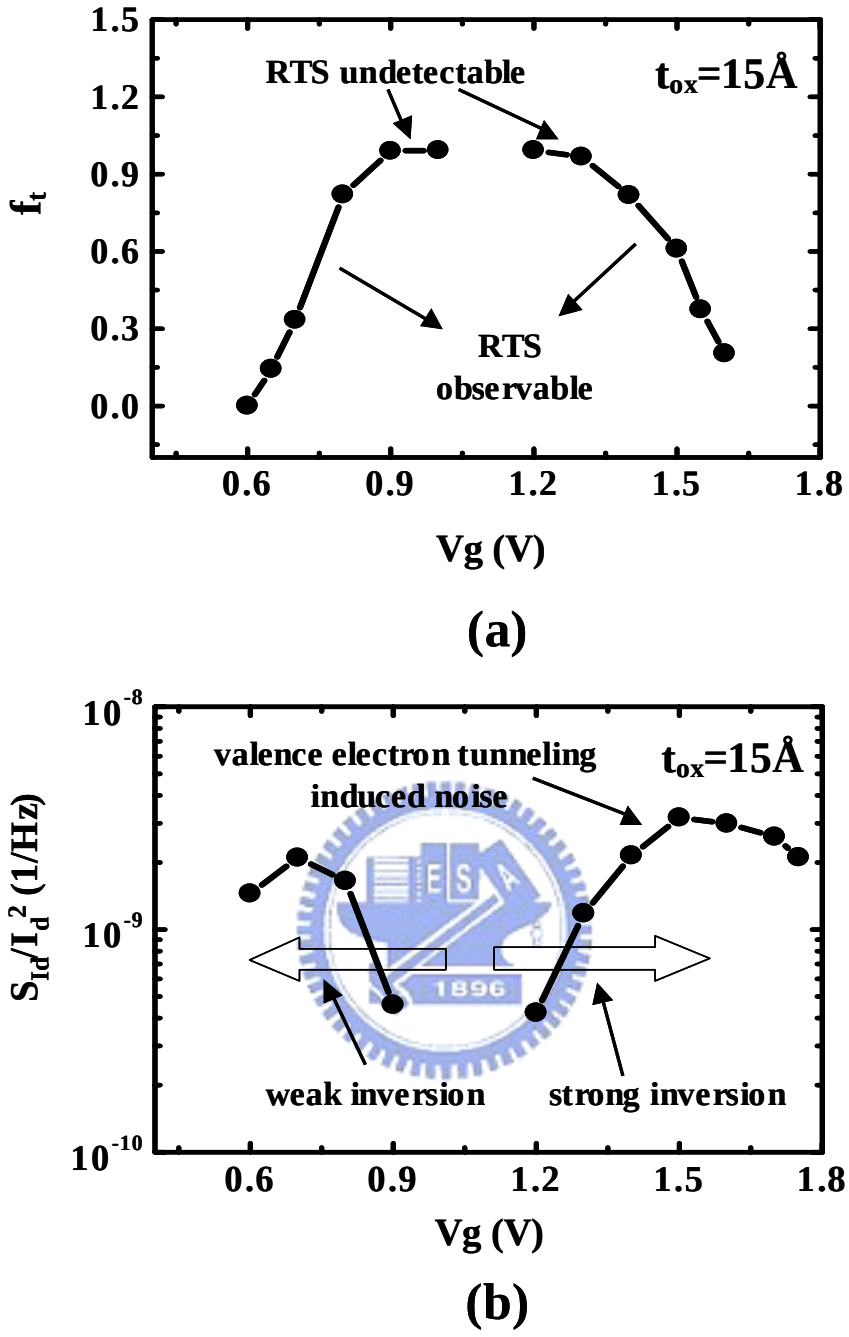


Fig. 5-15 The electron occupation factor (f_t) and normalized noise power spectral density versus gate voltage in a small area n-MOSFET (W/L= 0.16μm/0.12μm, t_{ox}=15Å). The second noise peak in strong inversion is due to valence-band electron tunneling.

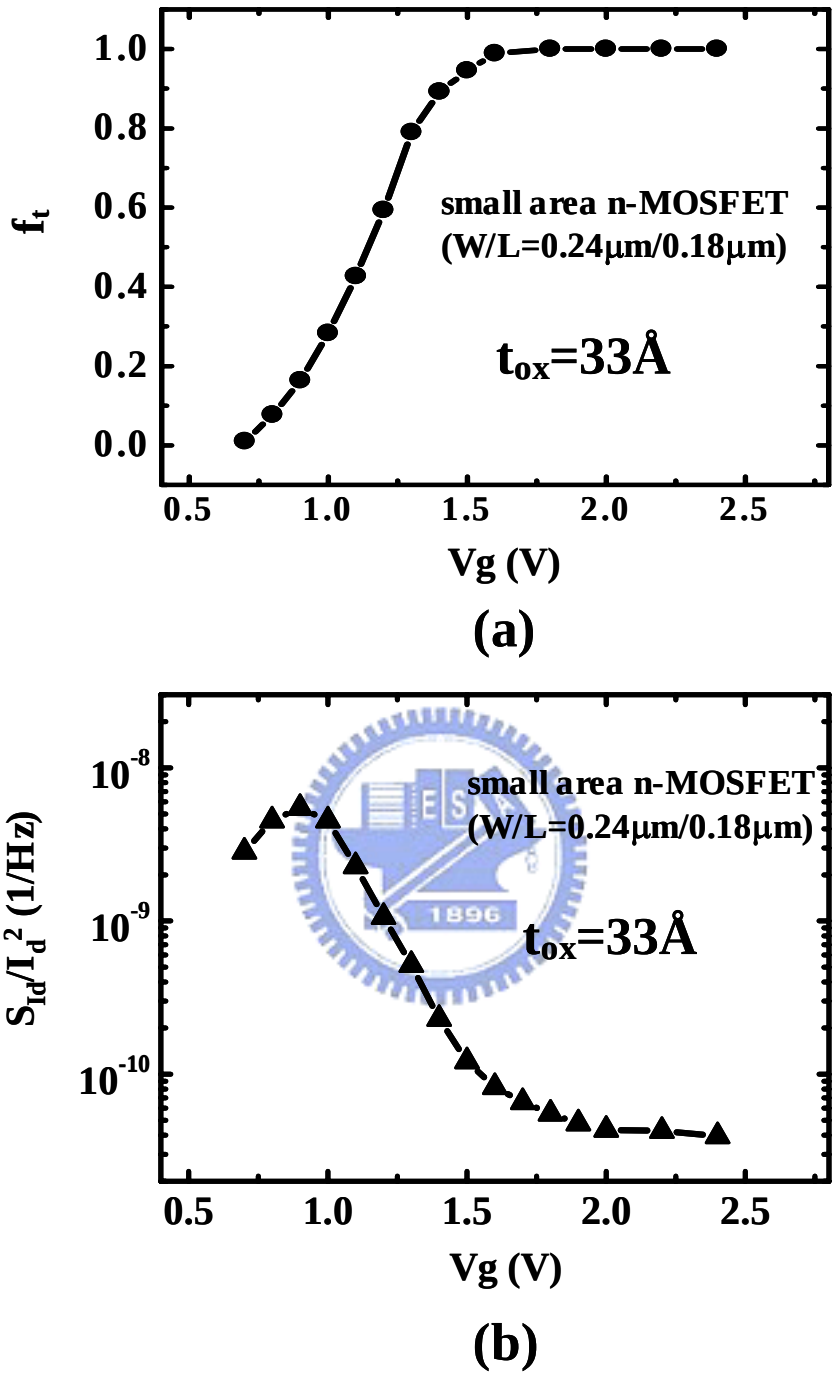


Fig. 5-16 Electron occupation factor (f_t) and normalized noise power spectral density in a small area t_{ox}=33Å n-MOSFET (W/L= 0.24μm/0.18μm,).

Chapter 6
Conclusions

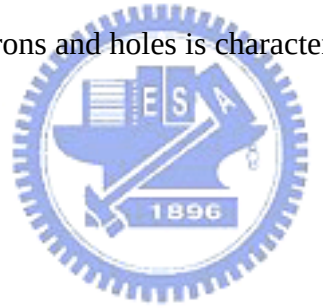
First of all, the hot carrier degradation mechanisms of drain current flicker noise in analog CMOS devices are investigated. The sources responsible for noise degradation are verified through both submicron CMOS transistors and a special ONO charge storage cell with various kinds of stresses. From our observation, the non-uniform oxide-trapped charges generated by maximum gate current stress could give rise to series flicker noise degradation as the number fluctuation mechanism dominates noise processes, which can be understood through a two-region unified flicker noise model. For n-MOSFETs, the number fluctuation mechanism dominates at low gate bias, so that the noise magnitude seriously increases after hot carrier stressing.

Next, pocket implantation effects on drain current flicker noise in 0.13μm CMOS process based high performance analog n-MOSFETs is investigated. Our results show that pocket implantation will degrade device noise characteristics primarily due to enhanced non-uniform threshold voltage distribution along the channel. Besides, the oxide quality is not affected by the pocket implantation process through the evidence of charge pumping results. That is, the channel profile engineering would be a key factor for low noise device design instead of the improvement of oxide quality. In addition, an analytical flicker noise model to take into account a pocket doping effect is proposed and shows good agreement with the measurement results. The analytical model is easy to implement in circuit simulators, such as HSPICE, for analog circuit design. Based on this concept, the programming charge distribution in NROM cells can be extracted from noise measurement in the linear operation regime without any device simulations. In addition, the result shows good agreement with the inverse modeling method.

Then, the pocket implantation would influence the channel carrier distribution and

degrade drain current Flicker noise, which is proved by device simulation. In addition, substrate bias has large effect on low frequency noise. The noise level is increased at a reverse substrate bias. This effect is more significant in a pocket device since the reverse substrate bias will result in a more non-uniform threshold voltage distribution. In addition, the reduction of channel carrier number due to a reverse substrate bias also contributes to the increase of noise.

Finally, low frequency flicker noise in analog n-MOSFETs with 15Å gate oxide is investigated. A new noise generation mechanism resulting from valence band electron tunneling is proposed. In strong inversion condition, valence-band electron tunneling from Si substrate to poly-gate takes place and results in the splitting of electron and hole quasi Fermi-levels in the channel. The excess low frequency noise is attributed to electron and hole recombination at interface traps between the two quasi Fermi-levels. Random telegraph signal due to capture of channel electrons and holes is characterized in a small area device to support our model.



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類比電路中之 n 型金氧半導體場效電晶體元件汲極電流低頻雜訊之探討

Investigation of Drain Current Flicker Noise in Analog n-MOSEFTs

Publication Lists

(a) Journal Papers

3. A 類國際性期刊

(1) J. W. Wu, J. C. Guo, K. L. Chiu, C. C. Cheng, W. Y. Lien, G. W. Huang and T. Wang, "Pocket Implantation Effect on Drain Current Flicker Noise in Analog n-MOSFET Devices," in *IEEE Trans. Electron Devices (TED)*, Vol. 51, pp. 1262-1266, 2004.

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(2) J. W. Wu, J. W. You, H. C. Ma, C. C. Cheng, C. S. Chang, G. W. Huang and T. Wang, "Valence-Band Tunneling Induced Low Frequency Noise in Ultra-Thin Oxide (15Å) N-Type Metal-Oxide-Semiconductor Field Effect Transistors," accepted and to be published in *Appl. Phys. Lett. (APL)*, 2004.

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