國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

低介電常數材料應用於多層導體連線

之電特性分析

Electrical Characteristics Study of Low Dielectric Constant Materials in Multilevel Interconnect System

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中華民國 九十三 年 八 月

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摘要

本論文研究積體電路製造技術中的低介電常數材料與多層銅導線連線整合製程之電特性分析及其相關技術之研究，並探討低介電常數材料應用於下一世代積體電路高頻訊號傳導的可能性。研究對象除了最成熟的 Fluorosilicate Glass (FSG)外，還包括多孔隙型低介電常數材料如有機類的 Nano-porous Carbon doped Oxide (CDO)以及旋轉塗佈型的 Porous SiLK，以及低介電常數阻障層碳化矽 (SiC)。

FSG 是一含氟的氧化矽合物，主要以化學氣相沈積生成，是最接近傳統積體電路製程中二氧化矽的低介電膜，雖然介電係數約 3.6，卻是目前唯一明確應用

於積體電路量產的材料，因此利用 FSG 來討論其它各種低介電常數材料在整合製程時，因製程不同造成介電質表面損傷時，所需注意金屬離子擴散問題，並建立一簡單物理模型解釋此金屬離子擴散所造成介電質電特性不隱定現象。

極低介電常數材料之奈米孔隙含碳氧化矽(CDO)其介電係數約低於 2.3，可以滿足下一世代之更快速訊號傳遞要求，有效降低金屬連線的電阻-電容延遲時間，CDO 介電膜擁有非常好的熱隱定性，非常低的漏電流，非常高的介電崩潰強度(> 5MV/cm)，非常長的本質生命週期。然而其卻也擁有一些電氣不穩性現象，應用先前的金屬載子入射分析、介電極化現象分析和漏電載子入射分析，我們成功的解釋其電氣不穩定特性，結合和上述三種機制提出一合理物理模型解釋之，並可用來解釋其它所有低介電常數材料的電氣不穩定現象。

碳化矽(a-SiC)是一新發展出的低介電常數金屬擴散障礙層，它雖然擁有很好的阻抗金屬離子擴散能力，但是在分析此類介電質材料的電氣特性時，卻也發現了其它不正常現像，將 a-SiC 做成的「金屬/a-SiC/矽」電容結構在高溫長時間偏壓狀態下，出現了一些電性上的不穩定現象，如在電容-電壓量測時，出現的磁滯現象。為此進而分析出此電性不穩定之形成原因：介電質極化效應，和其它如低漏電流之載子入射傳導現象。此電性不穩定性質，出現在大部份的低介電常數材料，為此我們亦建立起一分析模型來解釋此現象。

本論文並討論 a-SiC 介電質和其它低介電常數材料如：CDO 之高溫氧化現象及其晶圓回收應用。金屬擴散阻障介質 a-SiC 可於低至 550 度的環境中氧化，

且其氧化模式亦可用 Deal-Grove Model 來描述。應用此中低溫之介電質氧化現象，吾人發明一新的晶圓回收方法。這些介電質材料於氧化完成後並不會造成後續矽基底氧化損耗，故只要經過氫氟酸(HF)溶液即可蝕刻去除，比起傳統工業應用化學機械研磨方法(CMP)具有更快速更低成本之晶圓回收成效。

最後我們也討論了應用孔隙型旋塗式塗佈低介電常數材料 Porous-SiLK 於未來更新的導線連線觀念，討論其於更高頻的訊號傳輸下，運用現有金屬連線系統形成之金屬介電質結構的微帶線(Microstripline)於高頻的射頻(RF)或是微波(Microwave)下之介電質特性。討論以金屬導線設計之微帶線結構在傳遞高頻微波訊號(6GHz)時，導線之電阻、電容、電感、電導，及分析介質損耗和金屬損耗的效應，藉以分析在高頻訊號傳遞時之金屬導線的小訊號模型，有助於模擬研究之用，以取代傳統導線的電阻-電容結構模型。我們可以淬取 Porous-SiLK 在高頻訊號傳輸下的介電特性及損耗。藉由建立此一高頻分析方式，可應用分析其它低介電常數材料於高頻傳輸時之特性。

Electrical Characteristics Study of Low Dielectric Constant Materials in Multilevel Interconnect System

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Abstract

This dissertation studies the electrical characteristics of low dielectric constant (low-k) materials in back end Cu interconnects of integrated circuits (ICs). It also discusses the possibility of applying low dielectric constant film in high frequency signal transmission. The most mature low-k material, Fluorosilicate Glass (FSG) and several kinds of porous type low-k materials such as nano-porous Carbon-Doped-Oxide (CDO) and spin coated porous SiLK were investigated. In addition, low dielectric constant diffusion barrier amorphous silicon carbide (a-SiC) was also studied.

FSG is a fluorine contained silicon glass. It can be deposited in a chemical vapor

deposition (CVD) system and is most similar to the traditional dielectric (SiO_2) used for integrated circuits. Although the dielectric constant of FSG is about 3.6 and is not low enough, it is the first low-k material that has been used for mass-production. Thus we used FSG to study possible metal ions diffusion behaviors on surface-processed low-k dielectric films during typical damascene process. A simple physical model was proposed to describe the observed metal ion diffusion behavior.

Nano-porous CDO with very low dielectric constant ($k < 2.3$) is very suitable for next generation IC interconnect systems. It could effectively reduce the R-C delay. CDO film shows very good thermal stability, very low leakage current, very high dielectric strength, very good adhesion to TaN, and very long intrinsic lifetime. However, some electrical instability phenomena were observed. We developed a model consisting of dielectric polarization, carrier injections, and metal ion injection. This model can be used to explain most of the porous-type low-k materials' electrical instabilities.

CVD deposited a-SiC film is a low dielectric constant diffusion barrier. Although a-SiC film has a very good resistance to metal ions injections, we also found some unstable phenomena while characterizing its electrical characteristics. As an example, the metal/a-SiC/Si-substrate capacitor exhibits a hysteresis behavior under continuous C-V measurement. A physical model consists of dielectric polarization at high field

and carrier injection at low field and high temperature was proposed. Because the electric field in IMD is always less than 0.5 MV/cm under normal operation, electrical instability will not be issue under normal operation.

Since lots of low-k dielectrics were developed in these years. A universal wafer reclaim method is needed. We observed that a-SiC and CDO films can be easily oxidized at medium temperature and this oxidation follows the Deal-Grove model. Applying this oxidation behavior, a universal wafer reclaim method was invented : oxidation followed by HF etching. This wafer reclaim method could effectively reduce the reclaiming time and lower the cost in comparison with the traditional wafer polishing.

Finally, we considered the future new interconnect concept in this thesis. We studied high frequency signal transmission behavior in a stripline structure with spin-coated porous-SiLK low-k film. We developed a method to extract micro-stripline's parasitic parameters such as resistance, inductance, conductance, and capacitance from S-parameter measurements. These stripline parasitic parameters are useful to build up a more accurate interconnect small signal model than the traditional interconnect R-C based model. We also discussed the dielectric loss and interconnect metallic loss to realize the possible application of porous-SiLK at high frequency. With the same methodology, we could analysis other low-k materials' high frequency

behavior.

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Chapter 1

Introduction

1.1 General Background

With the progress of microelectronics technology, the semiconductor integrated circuits (ICs) devices area becomes smaller. The Moore's Law described well that each new generation approximately doubles the device density and increases performance by about 40% while quadruples memory capacity [1]. Currently, ICs designed with 90 nm design rule are being manufactured. The scaling of transistors has necessitated an increase in wiring density to accommodate increasing transistor densities over large chip areas. Generally, the speed of an electrical signal in an IC is governed by two components; one is the switching time of individual transistor, known as transistor gate delay, and the other is the signal propagation time between transistors, known as interconnect resistance-capacitance (RC) delay [2]. However, the Moore's Law is valid only when RC delay is negligible in comparison with gate delay. Most researches reported that the RC delay would be the dominant factor after 0.25 μm technology node. Interconnect parasitic components at 0.18 μm technology node begin to dominate not only the overall signal delay, as shown in Fig.1.1, but also the packing density, reliability, and manufacturing cost [3-6]. Dissimilar to transistor

scaling, transistor performance can be improved with reduced gate length, backend interconnection scaling results in higher wire resistance (R) for narrower metal line width and higher inter-/intra-level capacitance (C) for shorter metal line spacing. As a result, a larger portion of the actual circuit speed depends more on the characteristics of interconnects than on the scaling of active devices. The interconnect delay must be reduced by using new materials to alleviate the problem and to achieve higher performance and higher circuit density.

According to a basic interconnect cross-section view shown in Fig. 1.2, assuming that interconnect spacing between continuous interconnect metal lines equals metal line width and the distance between top metal layer and interconnect layer is the same as the interconnect line spacing. In a simple first-order model, the interconnect resistance (R), interconnect capacitance (C), the time delay (RC) and the power consumption (P) of an interconnect system can be expressed as the equations from (1.1) to (1.4), respectively.

$$R = \rho \frac{L_m}{W t_m} \tag{1.1}$$

$$C = 2(C_L + C_V) = 2\varepsilon(\frac{L_m t_m}{W} + \frac{L_m W}{t_m}) \tag{1.2}$$

$$RC = 2\rho\varepsilon(\frac{L_m^2}{W^2} + \frac{L_m^2}{t_m^2}) \tag{1.3}$$

$$P \propto 2\pi f V^2 C \tag{1.4}$$

,where ρ is the resistivity of metal line, L_m is the metal line length, W is the interconnect line width, ε is the permittivity of intermetal dielectric, and t_m is the thickness of metal line. In Eq. (1.4), f and V are operation frequency and applied voltage, respectively. According to these equations, it is clear that low-k materials not only lower line-to-line capacitance to reduce the RC delay but also alleviate power dissipation issues [7, 8]. Thus new low-k materials at each level of the interconnect structure (Fig. 1.3) are needed to replace traditional SiO_2 to reduce RC delay.

1.2 Multilevel Copper Interconnect Technologies

1.2.1 Cu Metallization

Recently, Cu has been widely accepted as the only solution to replace Al in multilevel interconnect applications [9-14]. Compare to traditional Al and Al alloys, Cu has a lower resistivity of 1.7 μΩ-cm with respect to Al alloy of around 3 μΩ-cm. Besides, Cu exhibits excellent resistance to electro/stress migration. Cu can be deposited by chemical vapor deposition (CVD) system or electrochemical deposition (ECD) system with great conformity and uniformity at low temperature. Both these two methods supply better step coverage than conventional physical vapor deposition (PVD). In 1997, Cu chips were introduced with SiO_2 as intermetal dielectric (IMD) [15]. Cu is known to have a poor adhesion to IMDS, fast drift speed in dielectrics especially under electrical field, easily reacts with Si, and forms deep level traps in

silicon [16-19]. Thus proper metal/dielectric diffusion barriers are necessary for avoiding Cu ions out diffusion [20-25]. Nowadays, Cu/SiO_2 technology is mature. In order to further optimize ICs performance, new IMD films are required to further reduce RC delay. This perceived need for low-k IMDs in ULSI applications has stimulated great efforts in the development of advanced low-k materials.

1.2.2 Low Dielectric Constant Materials

Although Cu has been successfully integrated with SiO_2 in advanced sub-0.25 μm ICs generation for improved interconnect performance [15]. In order to further improve interconnect RC delay, low-k materials to replace SiO_2 are inevitable. Integration of copper with low-k dielectric can render better ICs performance [26, 27]. Fluorine doped silicon dioxide (FSG) with k~3.6 integrated with Cu was successfully introduced in interconnect system at 0.18 μm technology node as the first Cu/low-k interconnect technology. Because that the k value of FSG is not low enough, others lower dielectric films (k = 2.6~3.0) are being studied and introduced for advanced ICs process.

Except the k value, the impact of low-k materials on process integration, manufacture cost, and device reliability must be considered. Lots of low-k materials have been developed recently and are listed in Table 1-1. These materials may be organic or inorganic. Basic requirements of low-k materials for IC integration are

listed in Table 1-2, and are summarized as follows:

- Low dielectric constant with respect to SiO_2's dielectric constant 4.2
- Good thermal stability
- High mechanical Strength
- Stable Chemical properties
- Good Electrical characteristics

In order to integrate these low-k materials into advanced interconnect processes; the above requirements are needed for all low-k films.

Some ultra-low-k (ULK) films with relative permittivities lower than 2.2 are generally achieved by the introduction of pore structures. The pore structure would further reduce mechanical strength and thermal conduction, and would increase moisture/chemical adsorption as well [28]. Therefore, all kinds of low-k materials have to meet lots of electrical, mechanical, chemical, and thermal integrity requirements so that interconnect system could deliver the desired electrical performance and ensure device reliability. To fulfill these requirements described above, measurement and evaluation of physical, chemical, thermal, and mechanical properties of low-k and low-k/metal interfaces are urgently required.

Though the demand of low-k application in Cu interconnect is very urgent, the

integration of Cu and low-k IMD is not easy. Although some leading companies announced mass-production of Cu-interconnect with IMD of k~2.6, most of the Cu chips were fabricated using FSG as IMD since 1997. Low-k materials with k-value lower than 2.2 are not mature.

1.2.2.1 *Chemical Vapor Deposition of Low Dieletric Constant Materials*

The k-value of SiO_2 used as IMD is about 4.1. In order to reduce the dielectric constant of SiO_2 film, incorporating fluorine into SiO_2 film is a promising method to form fluorinated oxide (FSG) with k~3.6. Because of the polarizability of fluorine in thermal oxide for FSG film, k-value of FSG is thus reduced. FSG could be deposited at different deposition process in atmospheric pressure CVD system (APCVD), plasma enhanced CVD system (PECVD), and high-density plasma CVD system (HDPCVD). Except the CVD deposited FSG low-k film, it leaves us different kinds of CVD low-k films listed in Table 1-1 such as diamond like Carbon (k-value 2.8~3.0), Parylene N (k value 2.6~2.8), Polyimide SSQ hybrids (k value 2.7~3), and ultra low-k porous type carbon doped oxide (Orion^{TM} k value 1.8~2.2). Though the CVD technology is presently used, CVD low-k materials for <65nm technology nodes have not been qualified to date.

1.2.2.2 *Spin-On Deposition of Low Dielectric Constant Materials*

Spin-on deposited low-k materials are the other candidate for semiconductor fabrication. A liquid state material would firstly deposited on a wafer by spin-coating method. Then a series of thermal treatments must be performed to remove solvent from the as-spun film. Finally, the deposited low-k film is well prepared after a curing step. Table 1-1 lists some spin-on low k films with k-value less then 3 such as poly(arylene ethers), and Cylotenes. Table 1-1 also lists some ultra low-k films with k-value less then 2.4 such as silica aerogels and silica xerogels.

Historically, spin-on materials present an important advantage over CVD materials: the ability to introduce a high degree of porosity in the films (up to 50 percent and more), reaching k values as low as 2.0. But CVD materials can reach similar k-value with lower porosity now. The competition between CVD technique and spin-on technique is expected to exist for several technology nodes.

1.2.2.3 *Low Dielectric Constant Diffusion Barrier*

Except the low-k IMDs, there is still another important dielectric in Cu dual damascene structure: Cu dielectric diffusion barrier. Barrier materials used for Cu wiring must prevent Cu from diffusion into the adjacent dielectric and must form a suitable, high quality interface with Cu to limit vacancy diffusion and achieve

acceptable electro-migration lifetime. Chemical vapor deposited (CVD) silicon nitride (SiN) and metal nitrides of refractory metals, such as W, Ta, Ti, and etc. are well known Cu ion diffusion barriers. As for dielectric barrier, SiN has been the most favorable candidate. In addition to being used as a barrier layer, SiN has also been used as an etching stop layer (ESL) and a final capping/passivation layer in Cu dual damascene structures. Yet, SiN with its higher dielectric constant (k~7), other new dielectric barriers with lower dielectric constant (such PECVD amorphous silicon carbide, a-SiC) are proposed for advanced Cu interconnect generations.

1.2.3 Concept of Future Interconnect for High Frequency Signal Transmission

Due to the application of low-k IMD and Cu interconnect, the clock rate has reached to RF frequency range, and the conventional lumped circuit R-C model approaches that used to solve hard-wired metal interconnect problems will eventually encounter fundamental limits and may impede the advance of future ULSIs device modeling. We need to find out the more accurately interconnect model of Cu/low k interconnect system at RF frequency. On the other hand, the interconnect performance must be evaluated at RF frequency rather than at relatively low frequency of around MHz. By using scattering parameter (S-parameter) measurement to extracted out the real transmission stripline parameters, resistance, conductance, inductance and

capacitance would help to build up a real interconnect model and this model would help to predict electrical characteristics more accurately.

1.3 Organization of the Thesis

On the basis of the understanding of issues of multilevel interconnect, this thesis focus on the primary topic of Cu and low-k material integration issues, especially try to establish a general physics model to analysis low-k dielectric electrical instability mechanisms. With this physics model, we could apply these analysis steps to all other newly invented low-k films.

This dissertation is divided into seven chapters. The contents of each chapter are described as followed:

In chapter 1, we introduce the background of this dissertation.

In chapter 2, the metal ions diffusion phenomena in FSG with different surface treated metal contact were study. FSG is the most matured and well-known low-k material that has been applied into real ICs and it is would be the most suitable low-k dielectric to study this metal ion caused electrical instability. In real backend Cu dual damascene process, the surface of FSG dielectric would experience different process steps such as dielectric etch, pre-metal deposition sputtering clean, as well as chemical-mechanical polishing. These process steps may change the surface

properties of FSG film. With different metal-dielectric interface conditions, there were different metal ions diffusion levels under electrical stress. Then, a new metal ion diffusion model could be proposed to explain the observed process effect.

In chapter 3, a ultra low k ($k < 2.3$) dielectric of Carbon-Doped-Oxide (CDO) was evaluated for next generation IC interconnect systems. CDO is a very promising low-k dielectric. The detailed characterization of CDO was performed in this chapter. Besides, the electrical instability mechanisms including metal ions diffusion, dielectric polarization, and carrier injection was discussed in detail. Reliability of CDO was also evaluated.

A newly developed a-SiC was design to replace silicon nitride being a dielectric diffusion barrier in Cu dual damascene structure. Detailed study of a-SiC was performed in Chapter 4. The resistance to Cu diffusion of a-SiC film deposited at different conditions were evaluated at first. Then, the dielectric instabilities due to dielectric polarization and carrier injection was presented and characterized.

In Chapter 5, a new universal method for a-SiC and CDO low-k film reclaim was proposed to replace current chemical and mechanical polishing (CMP) with fast speed, low cost, and low wafer substrate consumption. CDO and a-SiC films can be easily oxidized to SiO_2 in oxidant environment at temperature as low as 550℃. The a simple wet etching of SiO_2 and surface cleaning can finish the wafer reclaim process. The

detail oxidation mechanism and wafer reclaim process as well as the results were presented in the chapter.

In chapter 6, metal/low-k film based co-planar type transmission stripline was used to evaluate the RF performance of the interconnect system. All transmission line parasitic parameters including resistance, inductance, capacitance, and conductance, were extracted from high frequency S-parameters measurements. Both low-k dielectric loss and stripline metallic loss were also extracted and discussed for high frequency application.

In Chapter 7, we summarize all experimental results in this dissertation and suggest some unfinished works and new observed issues for future studies.

References

1 G. E. Moore, “Cramming more components onto integrated circuits”, Electronics, vol. 38, No. 8, pp.114-118, 1965

2. S. P. Jeng, M. C. Chang, and R. H. Havemann, “Process integration and manufacturing issues for high performance interconnect”, MRS Symp. Proc. Adv. Metallization for Devices and circuits, pp.25-30, 1994

3. L. Peters, Semiconductor International, vol. 21, No. 10, pp.64-74, September1998

4. K. Rahmat, O. S Nalagawa, S. Y. Oh, J. Moll, and W. T. Lynch, “A scaling scheme for interconnect in deep-submicron processes”, IEEE International Electron Devices Meeting, pp.245-248, 1995

5. S. Crowder, S. Greco, H. Ng, E. Barth, K. Beyer, g. Biery, J. Connolly, C. Dewan, R. Ferguson, X. Chen, M. Hargrove, E. Nowak, P. McLaughlin, r. Purtell, R. Logan, J. Oberschmidt, A. Ray, D. Ryan, K. Tallman, T. Wagner, V. McGhay, E. Crabbe, P. Agnello, R. goldblatt, L. Su, and B. Davari, “A 0.18 μ m high-performance logic technology ”, Symp. VLSI Tech. Dig. , pp.105-106, 1999

6. R. Hossain, f. Viglione, M. Cavalli, “Designing fast on-chip interconnects for deep submicrometer technologies”, IEEE Trans. on Very Large Scale Integration (VLSI) systems, vol. 11, No.2, pp.276-280, 2003

7. J. Ida, M. Yoshimaru, T. Usami, A. Ohtomo, K. Shimokawa, A. Kita, M. Ino, “Reduction of wiring capacitance with new low dielectric SiOF interlayer film for high speed/low power sub-half micron CMOS”, IEEE Symp. VLSI Technol. Digest, pp. 59-60, 1994

8. T. Sakurai, “Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSIs”, IEEE Trans. on Electron Devices, vol. 40, No.1, pp.

118-124, 1993.

9. T. Takewaki, R. Kaihara, T. Ohmi, and T. Nitta, “Excellent electro/stress-migration-resistance surface-silicide passivated giant-grain Cu-Mg alloy interconnect technology for giga scale integration (GSI)”, IEEE International Electron Devices Meeting, pp253-256, 1995
10. P. Singer, Semiconductor International, pp. 52-56, November, 1994
11. J. Torres, “Cu dual damascene for advanced metallisation (0.18 μm and beyond)”, IEEE Int. Interconnect Tech. Conf., pp. 253-255, 1999
12. T. Ritzodorf, L. Graham, S. Jin, c. Mu, and D. Fraser, “Self-annealing of electrochemically deposited copper films in advanced interconnect applications ”, IEEE Int. Interconnect Tech. Conf., pp.166-168, 1998
13. C. H. Lee, K. H. Shen, T. K. Ku, c. H. Luo, C. C. Tso, H. W. Chou, and C. Hsia, “CVD Cu technology development for advanced Cu interconnect applications”, IEEE Int. Interconnect Tech. Conf., pp. 242-244, 2000
14. J. Zhang, D. Denning, G. Braeckelmann, R. Venkatraman, R. Fiordalice, and E. Weitzman, “CVD Cu process integration for sub-0.25 μm technologies ” IEEE Int. Interconnect Tech. Conf., pp.163-165, 1998
15. D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. McDevitt, W. Motsiff, J. Dukovic, R. Wachnik, H. Rathore, R. Schultz, L. Su, S. Luce, and J. Slattery, “Full Copper Wiring in a Sub-0.25um CMOS VLSI Technology”, International Electron Devices Meeting, pp.773-776, 1997
16. 15. S. M. Sze, Physics of Semiconductor Devices, 2nd ed. New York: John Wiley & Sons, Chap. 6-8, 1981,
16. A. Cros, and K. N. Tu, “Formation, Oxidation, Electronic, and Electrical Properties of Copper Silicides”, J. Applied Physics, vol. 67, No. 7, pp.

3328-3336, 1990

17. L. Stolt and F. D'Heurle, "The Formation of Cu3Si: Marker Experiments",Thin Solid Films, vol. 189, No.2, pp. 269-274, 1990
18. J. Echigoya, H. Enoki, T. Satoh, T. Waki, M. Otsuki, and T. Shibata, "Thin Film Reaction and Interface Structure of Cu on Si", Applied Surface Science, vol. 56-58, Part 1, pp 463-468, 1992
19. T. H. Lee, "Nitridation Effect on the Barrier Property of Mo and Cr Layer in Cu/Barrier/SiO_2/Si MOS Structures", Master Thesis, National Chiao-Tung University, Hsinch, Taiwan, 1997
20. Y. C. Lin, "Barrier Property of W-Silicide and Ta-Nitride for Cu Metallization", Master Thesis, National Chiao-Tung University, Hsinch, Taiwan, 1997
21. Y. S. Diamand, A. Dedhia, d. Hoffstetter, and W. G. Oldham, "Copper Transport in Thermal oxide", J. Electrochem. Soc., vol. 140, No. 8, pp. 2427-2432, 1993
22. A. L. S. Loke, C. Ryu, C. P. Yue, J. S. H. Cho, and S. S. wong, "Kinetics of copper drift in PECVD dielectrics", IEEE Electron Device Letters, vol. EDL-17, pp.549-551, Dec. 1996
23. D. Gupta, "Comparative Cu Diffusion Studies in Advanced Metallizations of Cu and Al-Cu Based Thin Films", Materials Research Society Symposium Proceedings, vol. 337, pp. 209-215, 1994
24. J. D. Mcbrayer, R. M. Swanson, and T. W. Sigmon, " Diffusion of Metals in Silicon Oxide"J. Electrochem. Soc., vol. 133, No. 6, pp-1242-1246, 1986

25 X. W. Lin and D. Pramanik, "Future interconnect technologies and copper metallization", Solid State Technol., pp. 3-79, Oct. 1998

26. The International Technology Roadmap for Semiconductors, Section: Interconnect, 2003

27. K. Maex and G. Groeseneken, “Why we need to rethink copper low-k reliability issues”, Solid State Technology, vol. 46, No.1, pp.30-31, 2003
28. The International Technology Roadmap for Semiconductors, Section: Interconnect, 1997

Table 1-1 Summary of promising low-k candidates

Materials	K value	depostion method
Polymides	3.0-3.6	spin on
Spin-on Glasses	2.7-3.1	spin on
Fluorinated Polymides	2.6-2.9	spin on
DLC (Diamond like Carbon)	2.8-3.0	CVD
Poly(arylene ethers)	2.6-2.9	spin on
Poly(arylenes)	2.6-2.8	spin on
Cylotenes	2.6-2.8	spin on
Parylene N	2.6-2.8	CVD
Poly(norbornenes)	2.5-2.7	spin on
Polyimide SSQ hybrids	2.7-3.0	CVD
Alkyl-silanes/N2O	2.4-2.7	spin on
Ultra-low K		
Teflon-AF	1.9-2.1	spin on
Teflon microemulsion	1.9-2.1	spin on
Orion	1.8-2.2	CVD
Polymide nanofoams	2.2	spin on
Silica aerogels	1.1-2.2	spin on
Silica xerogels	1.5-2.2	spin on
Mesoporous silica	1.9-2.2	spin on

Table 1-2 Basic requirements for low dielectric constant materials

Thermal Properties	Mechanical Strength	Chemical Properties	Electrical Characteristic
Thermal stability	Thickness uniformity	Solvent, acids, PR strippers resistance	Isotropic and stable dielectric constant
Glass transition temperature	Adhesion	No corrosion to metal	Electrical strength
Thermal shrinkage: thickness, weight loss, stress hysteresis	Stress	Moisture adsorption	Breakdown field
Outgassing	Tensile Modulus, tensile strength	Purity	TDDB life-time, activation energy
Thermal expansion coefficient	Strain	Storage life	Leakage
Thermal conductivity	Hardness, density	Gas permeability	Charge
	Crack resistance	Environmental, safety, and health	Dissipation

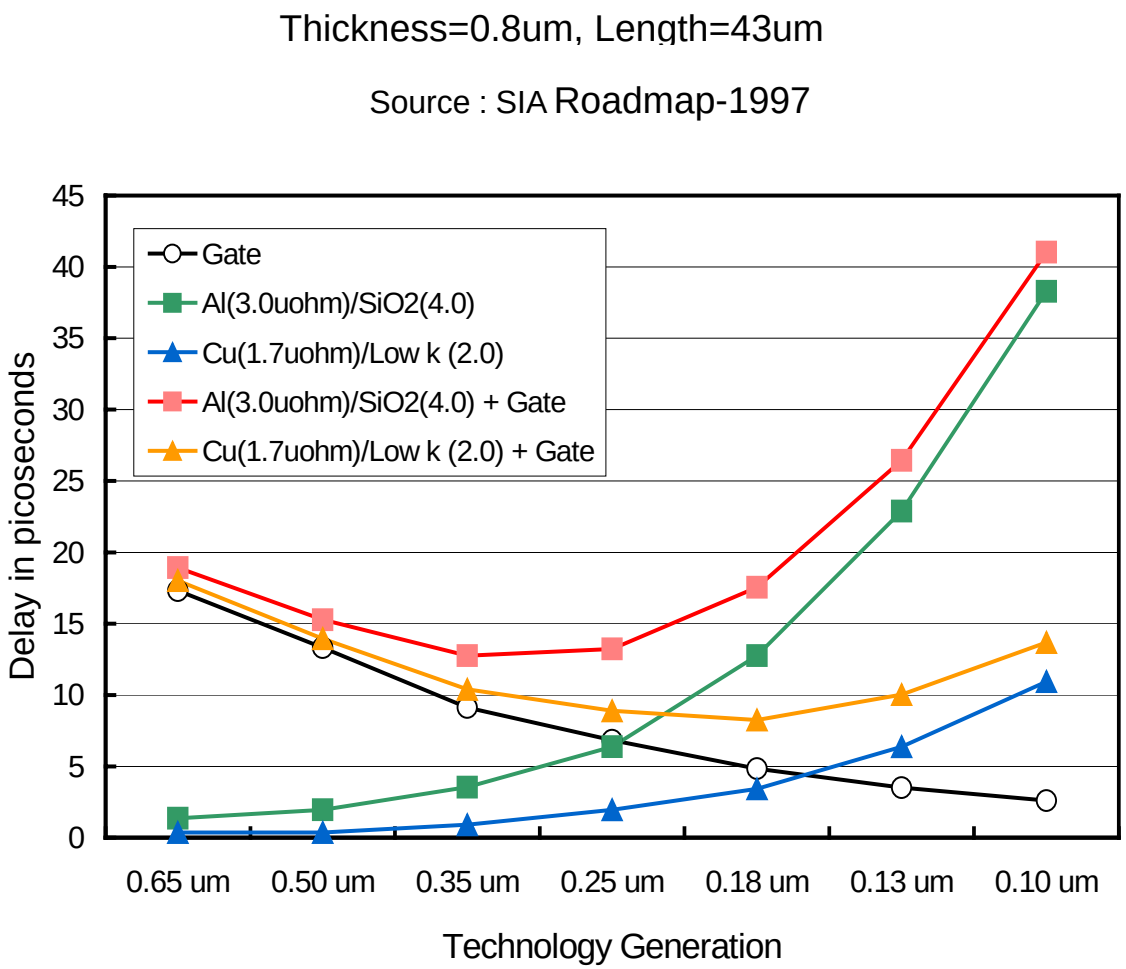


Fig. 1.1 Gate delay and interconnect RC delay at various technology nodes.

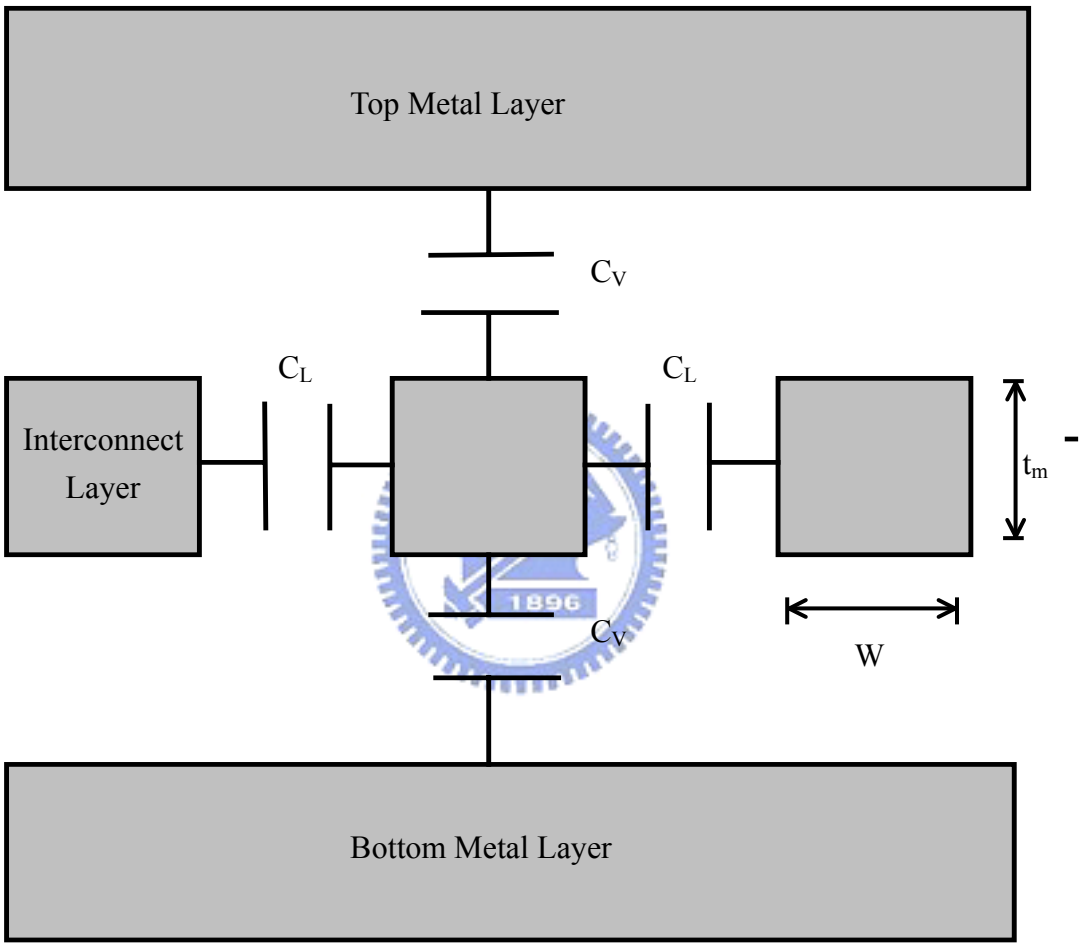


Fig. 1.2 Cross-section of interconnect system showing parasitic capacitance.

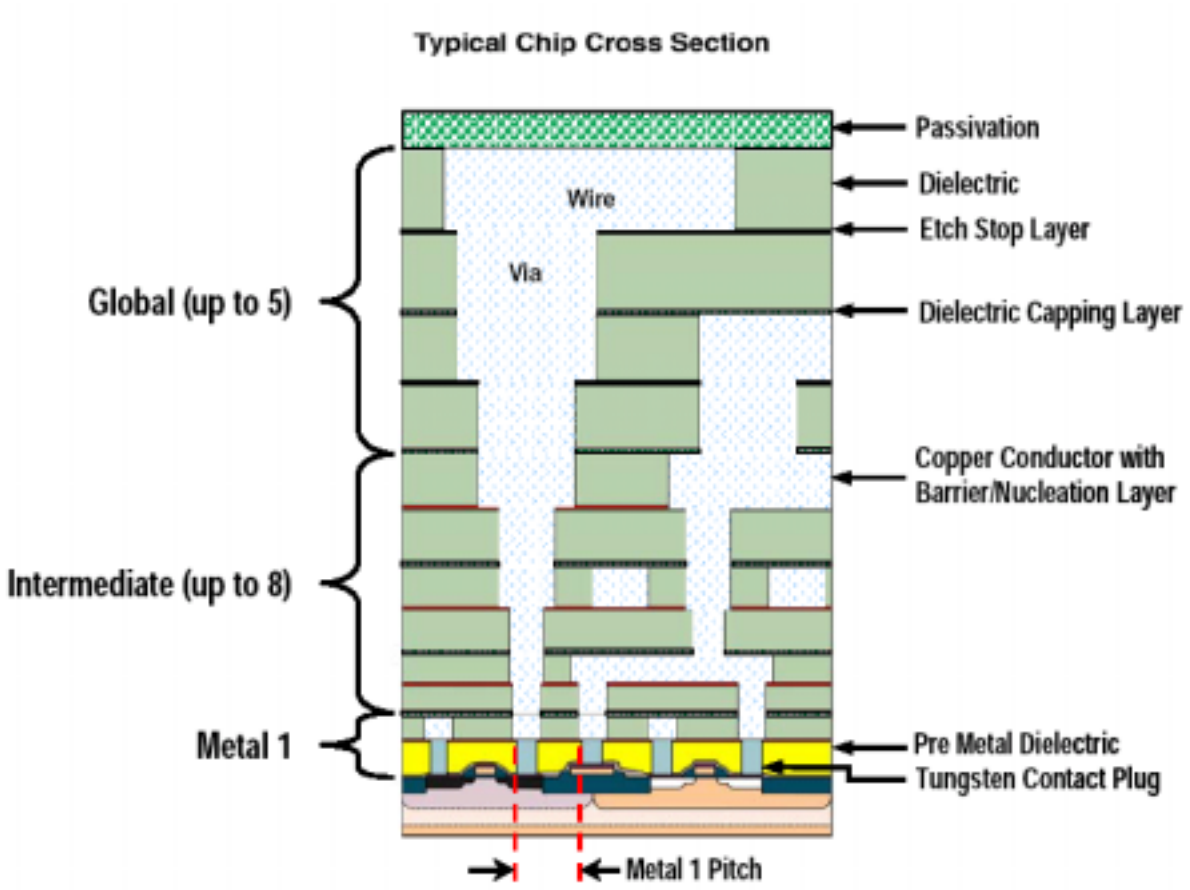


Fig. 1.3 Schematic drawing of a typical multilevel interconnect structure.

Chapter 2

Surface-Processing-Enhanced Copper Diffusion into Fluorosilicate Glass

2.1 Introduction

As mentioned in chapter-1, it is well accepted that copper (Cu) and low dielectric constant (low-k) materials are inevitable at the sub-0.13 micron technology nodes [1,2]. Because Cu is a serious contamination source in silicon and most of the dielectrics, Cu lines must be sealed with suitable diffusion barriers in Cu dual damascene scheme, and Cu contamination during processing must be monitored and controlled [3-6]. Therefore, the meaning of understanding the mechanism of Cu diffusion into the dielectric is twofold. First, if the dielectric shows a good barrier property, diffusion barrier layers can be eliminated. The process can be simplified and the performance can be further improved. Second, if Cu can diffuse into the dielectric, the diffusion behavior must be understood such that contamination during processing can be monitored and controlled.

Many low-k materials have been proposed in the past ten years to reduce interconnect capacitance. Among them, the fluorosilicate glass (FSG) is the most desirable because of its good thermal and chemical stability and its similarity to

silicon dioxide (SiO_2). Hence it can be readily integrated into the fabrication process [7-10]. Recently, Cu and FSG had been successfully integrated together and became standard process [11-13]. However, only a few articles in the literature examined the diffusion behavior of Cu into FSG film [14-18]. Furthermore, quite different results were reported in those articles. It was even reported that Cu does not diffuse into FSG film under the bias-temperature stress (BTS) at 200 ℃ and 3.5 MV/cm for 30 minutes[17].

The major drawback of the previous studies is that they all used as-deposited FSG film to examine the behavior of Cu diffusion in FSG film. This is not appropriate for the following reasons. In the damascene process, FSG film would experience several processes, such as dielectric etching, ion-sputtering clean before metal deposition, and chemical-mechanical polish (CMP) [19]. Fig.2.1 describes the major steps of Cu dual-damascene process. After the first Cu-interconnect layer is finished, inter-metal-dielectric (IMD) Cu-interconnect is deposited as the next layer (Fig.2.1(a)). The sequential photo-lithography process and dielectric etch processes are performed twice to form the via holes and trenches in the IMD (Fig.2.1(b)). After pre-metal deposition cleaning, barrier metal and Cu are then deposited into the via holes and trenches followed by a CMP process to finish the second layer Cu-interconnect (Fig.2.1(c)). Although the CMP process is employed to remove the Cu and barrier

metal, the surface of FSG film is also polished during the over polishing period. It is the behavior of the Cu diffusion into processed FSG film that affects the integration scheme and the contamination control. Therefore, it is important to examine the effects of surface processing on the Cu/FSG interface reaction and the diffusion behavior of Cu into FSG film, which is the focus of this chapter. Realizing this dual damascene process induced effects would be helpful to realize all other low-k films' behaviors in a damascene structure.

2.2 Experimental Details

Simple metal-insulator-silicon (MIS) capacitor structures were used. The starting material is an (100)-oriented p-type silicon wafer. A 10 nm thick oxide was thermally grown before the FSG deposition to minimize the dielectric/silicon interface state density. FSG film of about 750 nm thickness was deposited in a high-density plasma chemical vapor deposition (HDPCVD) system. An inductively coupled plasma (ICP) source was used to generate plasma. The frequency and power of the radio-frequency (RF) generator for the top electrode were 200 MHz and 350 W, respectively. The RF power of the bottom electrode was turned-off such that no ion bombardment occurred during deposition. It should be noted that substrate bias is not necessary for the damascene process because IMD is deposited on a CMP planarized

flat surface. The gases and corresponded flow rates were SiH_4(17 sccm), SiF_4(96 sccm), O_2(190 sccm), and Ar(125 sccm). The chamber pressure was 15 mTorr during deposition.

Wafers were then divided into three categories: without surface processing (the as-deposited sample), argon ion sputtering in an ICP chamber for 1 minute (the ICP sample), and CMP partial polish (the CMP sample). The ICP chamber is the pre-treatment chamber of a clustered metal deposition system. Both of the top and bottom powers were set at 300 W. This is the typical surface sputtering condition before metal deposition. The sputter rate of FSG film at this condition is about 200 nm/min. The CMP partial polish is to simulate the damage that arises during the over-polish period of the Cu CMP process. Clean pad and fresh slurry of Model ECC-1403-1 were used to avoid Cu contamination from pad or slurry. The pad pressure was set at 2 Psi and the polishing time is 50 sec. The thickness of the FSG film was reduced by 200 nm after the ICP process and by 50 nm after the CMP process. Copper film of 500 nm thickness was then deposited in an ionized metal plasma (IMP) chamber without substrate bias. Gate electrodes were then patterned by the wet process. Samples with Al gate were also prepared as reference. The Al film was deposited in a typical high vacuum DC sputter system.

After the metal gate patterning, a 30 nm thick SiN film was deposited to

passivate the MIS structure. This layer is used to avoid moisture absorption in the MIS structure and to prevent the Cu gate from oxidation during high temperature measurement. A 30 minutes annealing in N_2 ambient at 300 ℃, to reduce the process-induced charges in the dielectrics, finalized the sample processing. The temperature of this step is generally at 400℃, but in our experiment it is reduced to 300℃ to avoid Cu diffusion into the FSG during annealing. Table 2-1 summarizes the process condition of the 6 samples.

The total dielectric thickness of each sample was measured by optical interference method. The high frequency capacitance-voltage (HFCV) characteristics of all of the samples were measured at 100KHz. The dielectric constant of each sample was calculated from the measured capacitance at the accumulation mode and the total dielectric thickness was again determined by optical method. The flat-band voltage (V_{fb}) was also extracted from the HFCV characteristic.

A bias-temperature stress (BTS) at +1MV/cm and 200℃ was performed to drive Cu into the FSG film. Secondary-ion-mass-spectroscopy (SIMS) was employed to determine the distribution of Cu in the FSG film. To avoid surface roughness and knock-on effect during SIMS analysis, the capping SiN was removed by CF_4 plasma, and the metal gate was selectively removed by warm HNO_3 before SIMS analysis. Transmitted Fourier Transform Infrared (FTIR) Spectroscopy and Thermal Desorption

Spectroscopy (TDS) were also used to analyze the properties of the surface processed FSG film.

2.3 Metal Ion Diffusion in Surface Processed FSG

The fluorine concentration of the deposited FSG film determined by FTIR is about 4.6 %. Table 2-2 lists the dielectric thickness, effective dielectric constant, and flat-band voltage of the six samples. Although ICP and CMP treatments reduced the film thickness, the dielectric constant is unchanged. These results imply that the two surface processes did not change the composition and structure of the bulk of the FSG film. The magnitudes of V_{fb} of Al-gate devices are small. The slight difference between the samples may be due to surface process induced damages or the fixed charges in the deposited FSG film.

An obvious V_{fb} shift toward the negative voltage axis is observed for the Cu-gate devices. One obvious hypothesis to explain this observation is Cu contamination during the Cu deposition or thermal processes. Fig.2.2 shows the SIMS depth profiles of Cu in the FSG film of the Cu-FSG-1 and Cu-FSG-3 samples. Depth profiles of the Cu-FSG-1 sample and the Cu-FSG-3 sample are almost identical, and only a small amount of Cu atoms were detected at the surface. These results indicated that the trace amount of Cu atoms comes from the residual Cu at the FSG surface after

the stripping of the Cu gate. The concentration of typical mobile ions, such as Na^+ and K^+, were below the detection limit of SIMS analysis. Therefore, the negative V_{fb} is explained by the residual fixed charges in the FSG film generated during Cu deposition [20]. These charges are immobile and will not change at temperatures lower than the final annealing temperature of 300℃.

To drive Cu into FSG film, BTS tests were performed at +1 MV/cm and 200 ℃ for various periods. To exclude the possible instability of the FSG film itself and contamination during the surface processing, Al-gate MIS capacitors were also measured. The flat-band voltage shift (ΔV_{fb}) of the Al gate and the Cu gate samples after BTS were extracted and were denoted as $\Delta V_{fb,Al}$ and $\Delta V_{fb,Cu,}$ respectively. The ΔV_{fb} relevant to Cu was then corrected by subtracting $\Delta V_{fb,Al}$ from $\Delta V_{fb,Cu}$. Fig.2.3 shows the corrected ΔV_{fb} of the three Cu-gate samples after various BTS periods. The $\Delta V_{fb,Al}$ of the Al-FSG-1, Al-FSG-2, and Al-FSG-3 samples are also shown in Fig.2.3. A slightly positive shift of V_{fb} was observed on all of the three Al-gate samples, but the magnitudes of $\Delta V_{fb,Al}$ of the three samples were similar. This phenomenon is attributed to the slight instability of the FSG film itself [18?]. A net negative ΔV_{fb} was observed on all of the three Cu-gate samples. Since the flat-band voltage shift due to the instability of the FSG film and contamination other than Cu after the surface treatment had been subtracted, the ΔV_{fb} should be relative to the Cu only. It is obvious

that the ICP sample (Cu-FSG-3) had the largest ΔV_{fb} and the as-deposited sample (Cu-FSG-1) had the least ΔV_{fb}. Furthermore, the rates of the V_{fb} shift of the three Cu gate samples are Cu-FSG-3, Cu-FSG-2, and Cu-FSG-1 in the sequence from high to low. These phenomena imply that Cu is more easily driven into surface processed FSG films than driven into un-processed FSG film. Since the ICP sputtered sample (Cu-FSG-3) shows the most severe Cu diffusion, the following discussion and analysis will focus on the Cu-FSG-3 sample, with the Cu-FSG-1 sample as reference.

Fig.2.4 shows the SIMS depth profiles of Cu in the FSG film of the Cu-FSG-1 and Cu-FSG-3 samples before and after BTS for 30 minutes. Apparent Cu diffusion into the FSG film to a depth of about 40 nm was observed from the Cu-FSG-3 sample after BTS. According to the SIMS analysis, it is definitely confirmed that the ΔV_{fb} observed after BTS is due to Cu diffusion into the FSG. The amount of Cu in the FSG film of the Cu-FSG-1 sample after BTS is much lower than that of the Cu-FSG-3 sample after BTS. This is consistent with the trend of V_{fb} shown in Fig.2.2. Because the diffusion behavior of Cu in all FSG films should be of the same in the deep inside of FSG films, the only difference among the FSG films is the surface characteristic for Cu diffusion through the Cu/FSG interface. It is thus suspected that the surface processing either increases the Cu ionization rate or reduces the diffusion barrier height and then enhances the Cu diffusion into the FSG film.

FTIR analysis was performed to clarify the FSG property after the surface processing. The transmitted absorption spectrum was detected and the spectra of as-deposited and surface processed FSG films are identical. This confirms the previous postulation based on the dielectric constant and the SIMS profile of Cu that surface processes only modify the properties of the surface layer of FSG film. Fig.2.5(a) and (b) show the H_2O and HF desorption spectra analyzed by TDS, respectively, of as-deposited FSG film, FSG film at 4 days after deposition, and FSG film at 3 days after ICP sputtering. The surface sputtered FSG film shows the strongest H_2O desorption signal. This indicates that the surface sputtering enhances the moisture absorption of the FSG surface layer. It is also observed from Fig.2.5(b) that HF desorption of the ICP sputtered FSG film is more serious than that of the as-deposited FSG film. The controversial result that FTIR does not detect differences between as-deposited FSG film and ICP sputtered FSG film may be attributed to the weak sensitivity of transmitted FTIR on the surface layer property change. In our experience, moisture uptake of as-deposited FSG film cannot be detected by FTIR until 2weeks after deposition.

It has been reported that FSG film with a higher fluorine concentration has a lower dielectric constant, but becomes more easily hygroscopic [21, 22]. The FSG film after moisture absorption will induce a hydrolysis reaction, which is represented

by the following chemical formula [21-23] :

$$\text{—Si—F} + H_2O \text{ —> —Si-OH} + HF$$

The results obtained indicate that all FSG films have a probability of hydrolysis reaction occurrence for the Si—F bonds. The increase in the amount of Si—OH bonds slightly increases the dielectric constant for their low polarity. Moreover, the hydro-fluorine (HF) generated from Si—F bonds would damage other contacted films. Referring to the TDS result, it is postulated that the surface processing produces a surface damage layer. The enhanced moisture absorption at the surface damaged layer causes increased hydrolysis reactions. There can be more Si-OH bonds and HF generation to enhance the copper ionization and erosion rate, and thus more copper ions are generated. This effect, combined with the structural damage due to the CMP and ion sputtering, caused the barrier height for Cu penetration into FSG to roll off and more Cu ions to be driven into FSG under the same BTS condition. Since the FSG film is very thick, it is possible that the increase of the dielectric constant at the surface damaged layer does not affect the effective dielectric constant of the whole film.

Fig.2.6 plots the activation energy of Cu-FSG-3 sample for Cu mobile ions drift in FSG under BTS stress from Cu-FSG-3 samples. It is observed that with longer stress time, larger Cu drift activation energy is needed for Cu ions into FSG bulk

dielectric. It became harder for Cu ions to be driven into FSG films. It is believed that Cu ions which drift into bulk FSG film would finally accumulate at FSG/Si-substrate surface. Fig.2.7 explains the Cu ions behavior model. With initial BTS condition (Fig.2.7 (a)), Cu ions were easily drifted into bulk FSG under high electric field (E-field). Some Cu ions would finally reach and stop at the FSG/Si interface with the large amount of positive Cu ions being driven into FSG. Thus a reverse positive E-field would formed and then even reduced the FSG internal E-field biased from Cu metal gate voltage as shown in Fig.2.7(b).

2.4 Summary

Our investigation discovered that surface processing enhances Cu ion diffusion into FSG film. A surface-damage-layer-enhanced Cu ionization model was proposed. According to the model, the moisture uptake ability of the FSG film greatly affects the Cu diffusion behavior. This may explain the inconsistent reports in the published literature. Furthermore, even if the as-deposited FSG film shows good barrier properties against Cu diffusion, the damascene process will produce a surface damage layer to enhance the Cu diffusion. Thus, in the Cu/FSG integration process, the processed FSG surface must be isolated from any Cu contamination. Therefore, a suitable barrier layer is still necessary because the FSG film has been processed before Cu deposition. Furthermore, it is strongly recommended that the surface

processed film, instead of as-deposited film, be used to evaluate the behavior of Cu diffusion into all of the low k dielectric films.

References

1. R. J. Gutmann, “Advanced silicon IC interconnect technology and design: Present trends and RF wireless implications”, IEEE Transactions on Microwave Theory and Technique, vol. 47, No. 6, pp.667- 764, 1999
2. N. Awaya, H. Inokawa, E. Yamamoto, Y. Okazaki, M. Miyake, Y. Arita, and T. Kobayashi, “Evaluation of a copper metallization process and the electrical characteristics of copper-interconnected quarter-micron CMOS”, IEEE Transactions on Electron Devices, vol. 43, No. 8, pp. 1206-1212, 1996
3. J. D. McBrayer, R. M. Swanson, and T. W. Sigmon, “Diffusion of Metals in Silicon Oxide”, J. Electrochem. Soc., vol. 133, No. 7, pp. 1242-1246, 1986
4. S. P. Murarka, R. J. Gutmann, A. E. Kaloyeros, and W. A. Lanford, “Advanced Multilayer Metallization Schemes with Copper Interconnection Metal”, Thin Solid Film, vol. 236, No. 1-2, pp. 257-266, 1993.
5. D. Gupta, “Diffusion in several materials relevant to Cu interconnection technology”, Materials Chemistry and Physics, vol. 41, No. 3, pp.199-205, 1995.
6. A. S. Loke, J. T. Wetzel, P. H. Townsend, T. Tanabe, R. N. Vrtis, P. Zussman, D. Kumar, C. Ryu, and S. S. Wong, “Kinetics of copper drift in low-kappa polymer interlevel dielectrics”, IEEE Transactions on Electron Devices, vol. 46, No. 11, pp. 2178-2187, 1999
7. T. Homma, R. Yamaguchi, and Y. Murao., “A Room Temperature Chemical Vapor Deposition SiOF Film Formation Technology for the Interlayer in Submicron Multilevel Interconnectrions”, Journal Electrochemical Society, vol. 140, No.3, pp. 687-692, 1993
8. M. K. Bhan, J. Huang, and D. Cheung, “Deposition of stable, low k and high deposition rate SiF4-doped TEOS fluorinated silicon dioxide (SiOF) films”, Thin

Solid Films, vol. 308-309, pp.507-511, 1997

9. C. O. Jung, K. K. Chi, B. G. Hwang, J. T. Moon, M. Y. Lee, and J. G. Lee, "Advanced plasma technology in microelectronics", Thin Solid Films, vol. 341, No. 1-2, pp.112-119, 1999
10. S. P. Kim, and S. K. Choi, "The origin of intrinsic stress and its relaxation for SiOF thin films deposited by electron cyclotron resonance plasma-enhanced chemical vapor deposition", Thin Solid Films, vol. 379, No. 1-2, pp. 259-264, 2000
11. E. P. Barth, T. H. Ivers, P. S. Mlaughlin, A. Mcdonald, E. N. Levine, S. E. Greco, J. Fitzsimmons, I. Melville, T. Spooner, C. DeWan, X. Chen, D. Manger, H. Nye, V. McGahay, G. A. Biery, R. D. Goldblatt, and T. C. Chen, "Integration of copper and fluorosilicate glass for 0.18 μm interconnections", IEEE Int. Interconnect Technol. Conf., pp. 219-221, 2000
12. R.D. Goldblatt, B. Agarwala, M.B.Anand, E. P. Barth, G. A. Biery, Z. G. Chen, S. Cohen, J. B. Connolly, A. Cowley, T. Dalton, S. K. Das, C. R. Davis, A. Deutsch, C. DeWan, D. C. Edelstein, P. A. Emmi,C. G. Faltermeier, J. A. Fitzsimmons, J. Hedrick, J. E. Heidenreich, C. K. Hu, J. P. Hummel, P. Jones, E. Kaltalioglu, B. E. Kastenmeier, M. Krishnan, W. F. Landers, E. Liniger, J. Liu, N. E. Lustin, S. Malhotra, D. K. Manger, V. McGahay, R. Mih, H. A. Nye, S. Purushothaman, H. A. Rathore, S. C. Seo, T. M. Shaw, A. H. Simon, T. A. Spooner, M. Stetter, R. A. Wachnik, and J. G. Ryan, "A high performance 0.13 μm copper BEOL technology with low-k dielectric ", IEEE Int. Interconnect Technol. Conf., pp. 261-262, 2000
13. S. S. Lin, C. W. Chen, S. M. Huang, T. K. Kang, C. N. Yeh, T. L. Li, B. Y. Tsui, and C. C. Hsia., "An optimized integration scheme for 0.13 μm technology node

dual-damascene Cu interconnect", IEEE Int. Interconnect Technol. Conf., pp. 273-275, 2000

14. K. Mikagi, H. Ishikawa, T. Usami, M. Suzuki, K. Inoue, N. Oda, S. Chikaki, I. Sakai, and T. Kikkawa, "Barrier metal free copper damascene interconnection technology using atmospheric copper reflow and nitrogen doping in SiOF film", IEEE Int. Electron Devices Meeting, pp.365-368.1996
15. C.S. Pai, A. N. Velaga, W. S. Lindenberger, W. Y.-C. Lai, K. P. Cheung, "Highly reliable low-ϵ (3.3) SiOF HDP-CVD for subquarter-micron CMOS applications", IEEE Int. Interconnect Technol. Conf., pp. 42-44, 1998
16. G. Passemard, P. Fugier, P. Noel, F. Pires, and O. Demolliens, "Study of fluorine stability in fluoro-silicate glass and effects on dielectric properties", Microelectronic Engineering, vol. 33, No. 1-4, pp. 335-342, 1997
17. A. Labjadh, F. Braud, J. Torres, J. Palleau, G. Passemard, F. Pires, J. C. Dupuy, C. Dubois, and B. Gautier., "Study of the thermal stability at the Cu/SiOF interface", Microelectronics Engineering, vol. 33, No. 1-4, pp. 369-375, 1997
18. A. Abdul-Hak, C. Ahrens, W. Hasse, and J. Ullmann, "Investigation of copper diffusion in SiOF, TEOS oxide and TCA oxide using bias thermal stress (BTS) tests", Microelectronic Engineering, vol. 37-38, No. 1-4, pp. 205-210, 1997
19. S.Wolf, and R. N. Tauber, Silicon Processing for the VLSI ERA Volume1, 2nd., Lattice Press, California, 2000
20. T. P. Ma and P. V. Dressendorfer, "Ionizing Radiation Effects in MOS & Circuits", John Wiley & Sons, New York, pp. 374-374,1989..
21. S. Lee, and J. W. Park, "Effect of fluorine on moisture absorption and dielectric properties of SiOF films", Materials Chemistry and Physics, vol. 53, No. 2, pp.150-154, 1998

22. M. Yoshimaru, S. Koizumi, K. Shimokawa, and J. Ida, “Interaction between water and fluorine-doped silicon oxide film deposited by PECVD”,Proceedings of IEEE Int. Reliability Physics Symposium, pp.234-241, 1997
23. T. Homma, “Instability of Si-F bondss in fluorinated silicon oxide (SiOF) films formed by various techniques”, Thin Solid Films, vol. 278, No. 1-2, pp. 28-31, 1996

Table 2-1 Process conditions of samples used in this work.

Sample ID	FSG Surface Processing	Gate Material
Al-FSG-1	as-deposited	Al
Al-FSG-2	CMP	Al
Al-FSG-3	ICP	Al
Cu-FSG-1	as-deposited	Cu
Cu-FSG-2	CMP	Cu
Cu-FSG-3	ICP	Cu

Table 2-2 Dielectric thickness, effective dielectric constant, and flat-band voltage of all of the six samples.

	Al-FSG-1	Al-FSG-2	Al-FSG-3	Cu-FSG-1	Cu-FSG-2	Cu-FSG-3
Thickness (nm)	788	523	589	761	519	575
Dielectric constant	3.62	3.65	3.69	3.54	3.63	3.55
Flat-band voltage (V)	-1.41	0.57	-2.38	-18.95	-14.18	-27.59

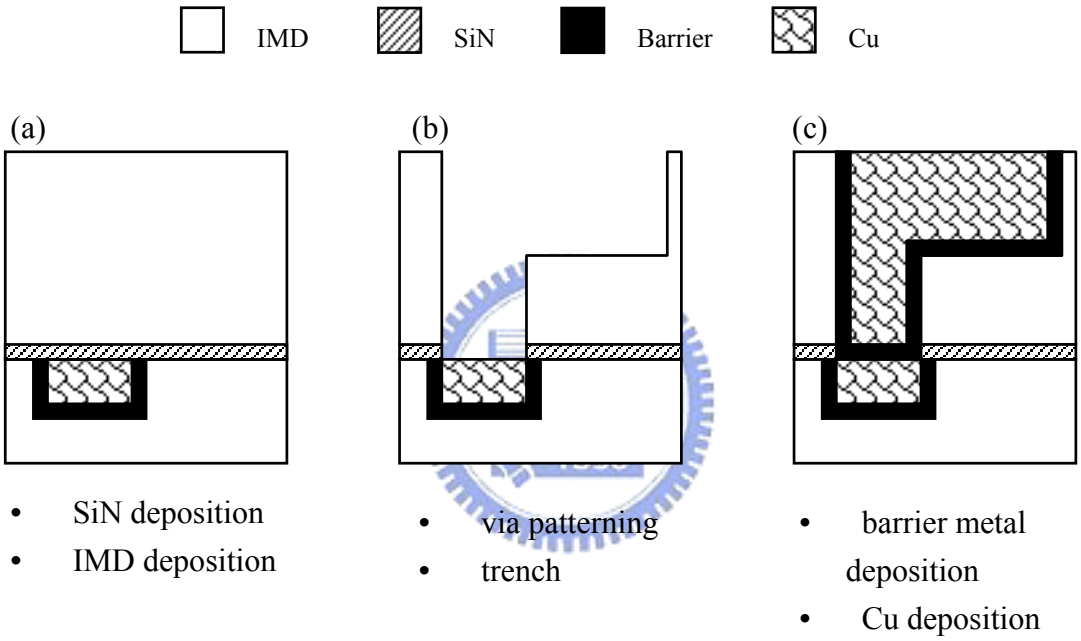


Fig. 2.1 The major process steps of the dual-damascene process: (a) after IMD deposition, (b) after dual-damascene patterning, and (c) after Cu CMP

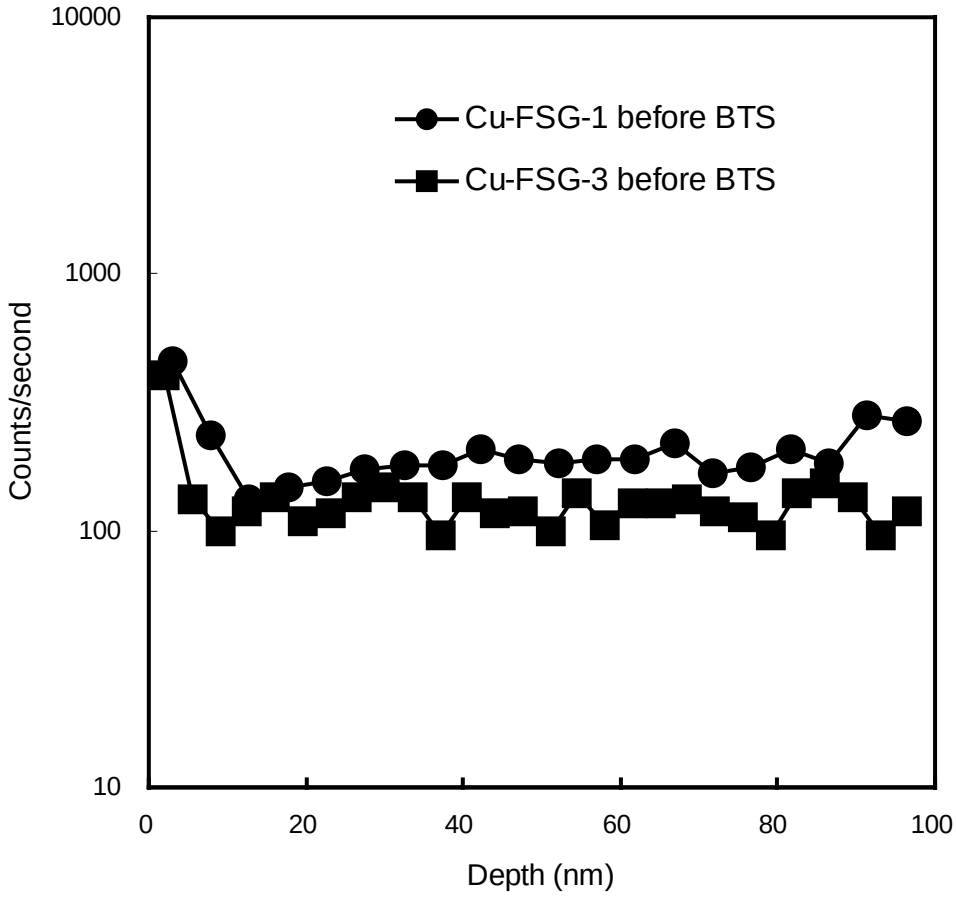


Fig. 2.2 The SIMS depth profiles of Cu in FSG film of Cu-FSG-1 and Cu-FSG-3 samples just after sample preparation. The capping SiN and Cu-gate have been removed

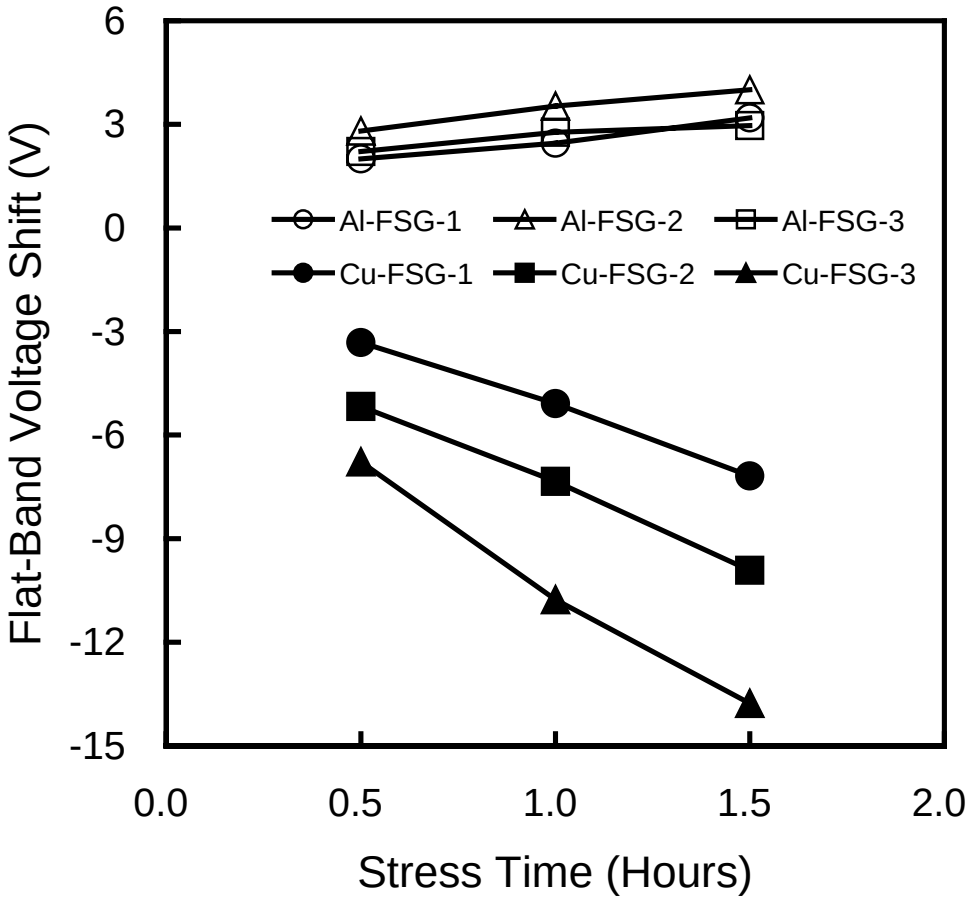


Fig. 2.3 The corrected flat-band voltage shifts of Cu-FSG-1, Cu-FSG-2, and Cu-FSG-3 samples after BTS treatment at +1 MV/cm and 200 ℃ for various time periods. The flat-band voltage shifts of Al-FSG-1, Al-FSG-2, and Al-FSG-3 samples were also shown.

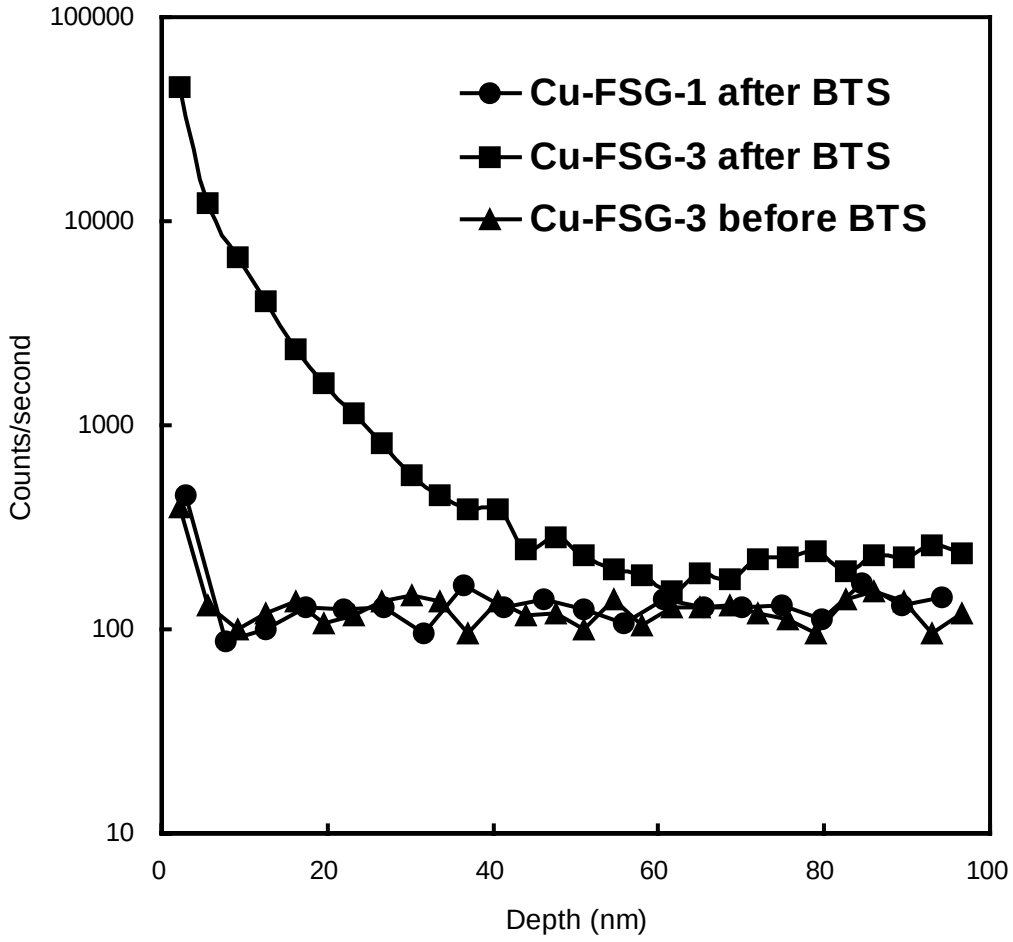


Fig. 2.4 The SIMS depth profiles of Cu-FSG-1 and Cu-FSG-3 samples before and after BTS treatment at +1 MV/cm and 200 ℃ for 30 min.

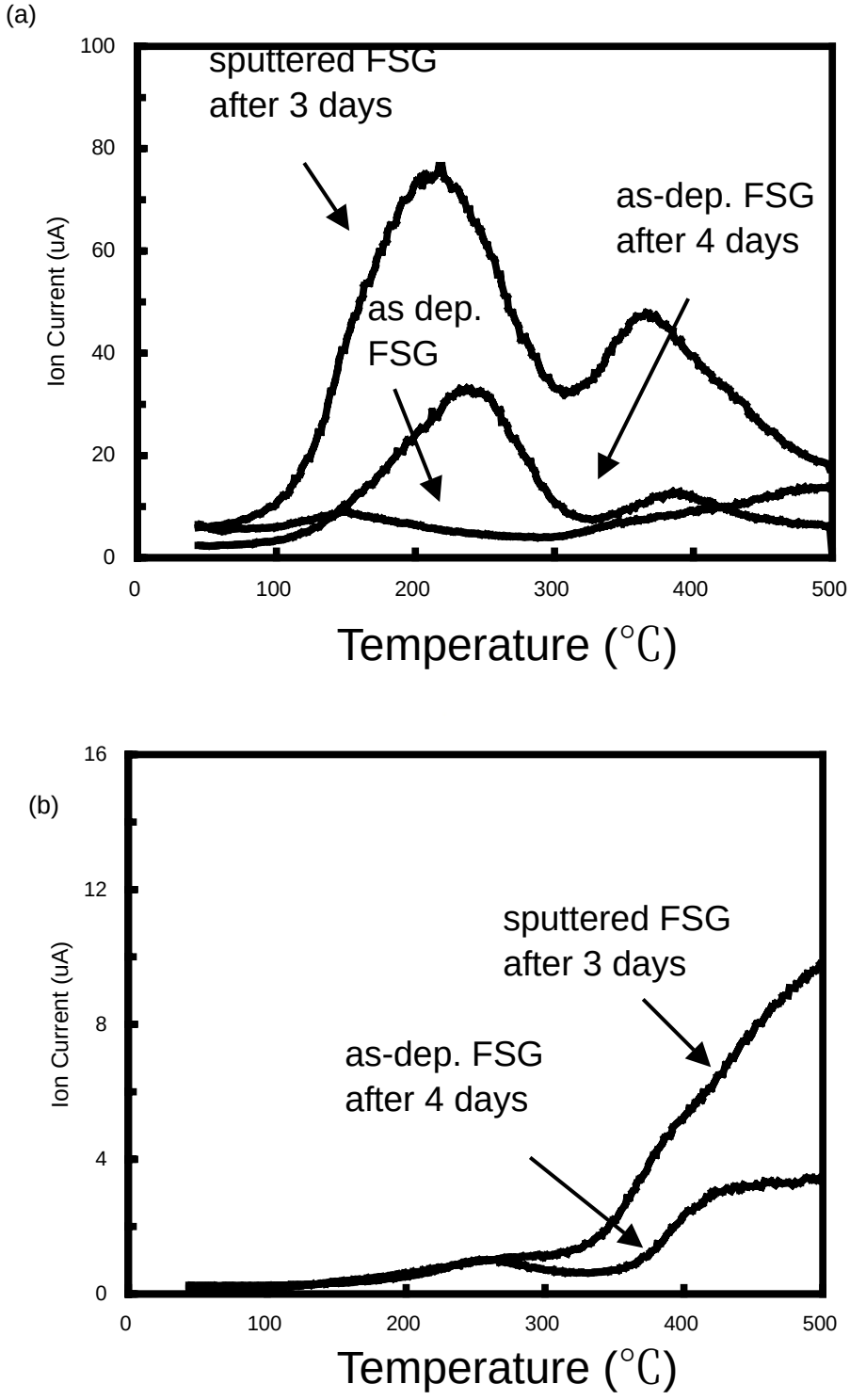


Fig. 2.5 The (a) H_2O and (b) HF desorption spectra measured by TDS analysis on as-deposited FSG film, FSG film at 4 days after deposition, and FSG film at 3 days after surface sputtering.

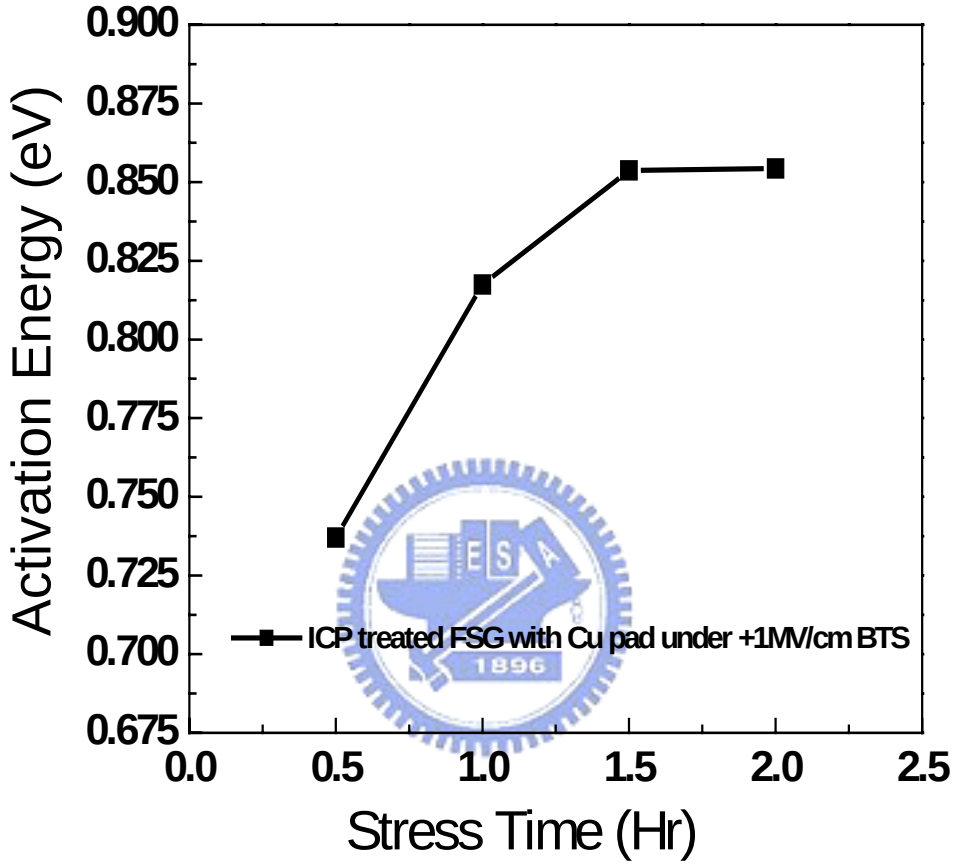


Fig. 2.6 Activation energy of Cu ions drift of Cu-FSG-3 under BTS

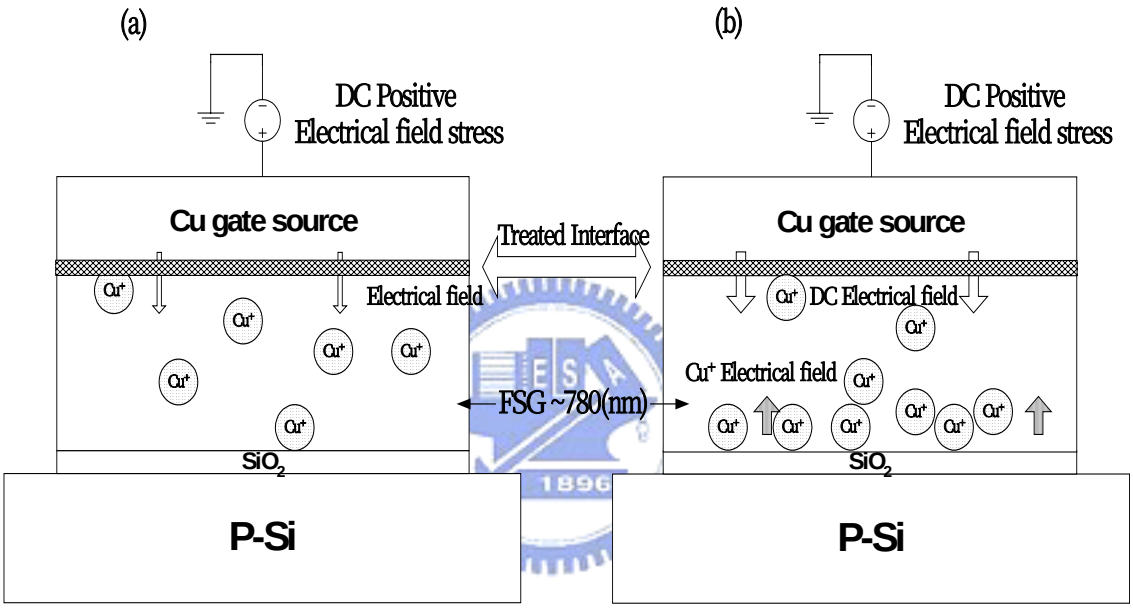


Fig. 2.7 Model of Cu metal ions drift in low-k dielectric under E-field

Chapter 3

Study on Ultra Low Dielectric Constant Film Porous Carbon-Doped-Oxide for Next Generation IC Interconnect

3.1 Introduction

As mentioned in previous chapter, the implementation of copper interconnect structures with low-k inter-metal dielectrics (IMD) and low-k dielectric diffusion barrier (e.g. SiC) is the only solution to reduce overall signal delay in the future [1,2]. Although FSG is a mature low-k dielectric, since Cu is the metal with the 2nd lowest resistivity, adopting lower dielectric constant materials is the only method to further improve the resistance-capacitance (RC) time delay. According to the International Technology Roadmap for Semiconductor published in 2003, the bulk dielectric constant of low-k material must be reduced to lower than 2.4 by 2007 [3]. In the past 10 years, lots of varieties of low-k materials have been developed with different chemical composition. By changing film polarity, changing chemical bonds, or inserting lower weighted molecular atoms, one can intrinsically reduce k value to about 2.3~2.7 [4]. In order to further reduce dielectric constant, there is an

unavoidable trend of developing porous type low-k films. With the free air volume pore structures in bulk low-k film, very low dielectric constant could be reached [5-8].

Among the nano-porous low-k materials, nano-porous carbon-doped oxide (CDO) is one of the most promising porous low-k materials to date [9-12]. CDO could be deposited in a plasma-enhanced chemical vapor deposition (PECVD) system with additional curing process to produce a stable state. Very low dielectric constant of 2.2 has been achieved. It is reported that CDO exhibits very low leakage current (<1nA/cm^2 at 2.5MV/cm), very high thermal stability (>600℃ in N_2 ambient), and strong electrical strength (> 5MV/cm at 200℃). It has been demonstrated successfully integrating with Cu in a full dual damascene structure [13]. The above information indicates that CDO is a very potential material for next generation IMD [14], and not many electrical properties have been discussed in previous literatures.

On the other hand, Cu shows many advantages in comparison with Al [15] but also new problems appear. The drift of Cu ions into IMD is one of the most important issues that should be carefully studied. Cu mobile ions in IMD would always induce defect traps and cause reliability issues and even degrade lifetime of the devices. To understand the Cu drift in IMD is meaningful for not only academic interest but also practical application. Bias temperature stress (BTS) test on Cu/low-k film/Si sandwiched capacitor structure is always employed to study Cu drift behavior in

low-k thin film. Aluminum, being a very stable interconnection metal, was used as reference to distinguish Cu drift and the other issues. Recently, some unusual phenomenon happened to these recently developed porous low-k materials. Al gated capacitor structures exhibit unaccustomed V_{fb} shift after positive electric field stress. Quite different explanations were proposed in those literatures [16-18]. Of all of these proposed models: interface-related charges, instability as Al comes in contact with low-k film, carrier injection and trapped inside low-k film, and Al ions drift in low-k, are not consistent to each other. Besides, all these models were proposed on the basis of electrical analysis data without any material analysis.

The significance of studying metal drift in low-k material is manifold. At first, integration scheme is dependent on metal drift in low-k material. Second, interconnect reliability is strongly affected by metal ions in low-k dielectric. Third, to monitor Cu contamination, metal drift behavior must be known in advance. Therefore, we investigated the drift of metal ions in a nano-porous low-k film and studied the metal ions induced electrical instability in this chapter. A metal-ions-drift model in porous CDO is also proposed. Furthermore, we focused on the electrical stability and reliability issues of the porous CDO film. The experiment procedure will be explained in the next section. Electrical instabilities are shown in section-3.3 and a model is proposed to explain the observed instability. Electrical reliability is also evaluated in

section-3.3. It is concluded that with suitable contact metal, porous CDO film is electrically stable and reliable to be used as inter-metal dielectric (IMD) for the future 2-3 technology nodes.

3.2 Experimental Details

Simple metal-insulator-silicon (MIS) capacitor structure was used in this work. The starting material was (100)-oriented n-type silicon wafer. A 10 nm thick oxide was thermally grown before CDO deposition to minimize the insulator/silicon interface state density. Thin CDO film was deposited in a Trikon Technologies Planar 300 Plasma-enhanced chemical vapor deposition system at room temperature using an organo-silane precursor with He as carrier gas[13]. A 30 minutes nitrogen gas furnace annealing at 400^{o}C was performed before metal gate deposition. A metal mask was use to define gate electrode. The MIS structures are divided into three categories. In the first category, the MIS structure is Metal/CDO(200 nm)/SiO_2(10 nm)/n-Si with various kinds of metal (Al, Cu, TaN, and Pt). These samples are denoted as Al-CDO-1, Cu-CDO-1, TaN-CDO-1 and Pt-CDO-1. All kinds of metal except Al were deposited in a DC sputtering system while Al was deposited in a thermal evaporating system. The second category is reference sample with structure of Al(500 nm)/PECVD SiO_2 (30 nm)/CDO(200 nm)/ SiO_2 (10 nm)/n-Si and is denoted as Al-CDO-2. Because of the existence of thermal oxide and the work function difference between gate and Si

substrate, the above structures are asymmetric. The third category is an almost symmetric MIS structure using Al gate and heavily doped n-type Si substrate. This structure was fabricated to study the carrier transport mechanism. The structure is Al(500 nm)/CDO(200 nm)/n+-Si and is denoted as Al-CDO-MIM. Fig. 3.1 shows the schematic drawings of the structures of the three categories. A 30 nm thick SiNx layer was deposited on sample surface to prevent dielectric from moisture absorption and to prevent Cu gate from oxidation during storage.

The film thickness, refraction index, and porosity of the deposited CDO film were measured by ellipsometry method. The atomic composition was determined by Rutherford Backscattering Spectrometry (RBS) analysis and the major chemical bonds were identified using Electron Spectroscopy for Chemical Analysis (ESCA). Fourier-Transformed Infra-Red (FTIR) spectroscopy was also employed to evaluate the material property.

Both capacitance-voltage (C-V) and current-voltage (I-V) characteristics were measured to evaluate the CDO film using a precision impedance meter of model Agilent 4284A and a semiconductor parameter analyzer of model Agilent 4156C, respectively. Bias temperature stress (BTS) test under various temperatures and electric fields were performed. Nitrogen gas purge was carried out during device measurement to avoid moisture absorption and metal gate oxidation. Flat-band

voltages (V_{fb}) before and after BTS were extracted from high frequency (100 KHz) C-V characteristic with voltage swept either from inversion mode to accumulation mode (forward voltage sweep, FVS) or from accumulation mode to inversion mode (reverse voltage sweep, RVS). Time dependent dielectric breakdown (TDDB) test was performed to extract the lifetime of CDO film.

3.3 Properties of Ultra Low-k CDO films

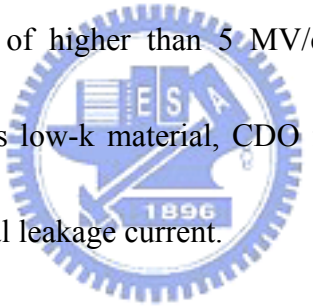
3.3.1 CDO Basic Properties

Fundamental properties of the CDO film were characterized at first. The dielectric constant of the CDO film calculated from Al-CDO-1 sample is about 2.2 and is apparently reach the demand for the next generation IMD [3]. The CDO is composed of Si, C, O, and H atoms and the atomic ratio is Si : C : O : H = 20.5 : 14.5 : 31 : 34. Film volume porosity is about 20% measured by optical ellipsometer with pore size of 1-4 nm measured by cross sectional transmission electron microscopy (XTEM) [13]. It would be these nano-pores that produce the very low dielectric constant with low carbon content of 14.5%.

Fig. 3.2(a) depicts the FTIR spectra of the CDO film after annealing in N2 ambient at various temperatures. No changes are observed even after annealing at 400 °C for 8 hours or at 650°C for 30 minutes. Fig.3.2(b) shows that the thickness shrinkage is less than 3% after 650°C annealing which indicates almost negligible

thermal decomposition. The dielectric constant determined by the C-V method slightly increases to 2.3 after annealing at 600°C for 30 minutes. These results indicate that the thermal stability of CDO is well beyond the requirement of the backend process of line.

Fig. 3.3(a) and 3.3(b) show the current density-electric field (J-E) curves of the Al-CDO-MIM capacitors at different temperatures and the breakdown characteristic of Al-CDO-MIM capacitors at 200°C, respectively. The CDO film exhibits very low leakage current density of 1 nA/cm2 at 2.5MV/cm and room temperature. It also has very high dielectric strength of higher than 5 MV/cm even at 200°C. It is thus concluded that being a porous low-k material, CDO film shows very good thermal stability and very low electrical leakage current.



3.3.2 CDO Electrical Instability Behaviors

Although CDO film exhibit low dielectric constant, high thermal stability, low leakage current, and high dielectric strength, electrical instability was observed during the C-V measurement of the Al-CDO-1 sample. By repeating the C-V measurement on the Al-CDO-1 capacitor at room temperature from inversion mode to accumulation mode (FVS) and then from accumulation mode to inversion mode (RVS), V_{fb} shift with respect to the original C-V curve was observed. The C-V curve shifts toward

positive Vg direction under wide range FVS, while it shifts toward negative Vg direction under wide range RVS. The shifts under FVS and RVS are asymmetric and a net shift toward negative voltage direction was observed (Fig. 3.4). Fig. 3.5 exhibits the C-V curves of Al-CDO-1 sample before and after electrical stress at -2MV/cm and +2MV/cm for 4 minutes. It is also observed that positive electric field stress cause larger V_{fb} shift. All of the metal-CDO-1 capacitors exhibit similar electrical instability under continuous C-V measurements. Because of the asymmetric shift, the C-V instability couldn't be simply explained by the dielectric polarization [21].

BTS test was performed at 30°C and 150°C. The electric field is 0.6MV/cm. The magnitudes of V_{fb} shift after BTS are listed in Table 3-1. The magnitudes of V_{fb} shift of the four kinds MIS capacitors are Al-CDO-1, Cu-CDO-1, TaN-CDO-1, and Pt-CDO-1 in the sequence from high to low. It should be highlighted that the magnitude of V_{fb} shift of the Al-CDO-1 sample is even larger than that of the Cu-CDO-1 sample. This observation is totally different from that as the dielectric is silicon dioxide. The TaN-CDO-1 and Pt-CDO-1 samples exhibit very slight V_{fb} shift. As the BTS was performed at 150°C, the magnitude of V_{fb} shift is enlarged but the sequence remains unchanged.

3.3.3 Metal Ions Drift in CDO Films

The lowest V_{fb} shift of TaN-CDO-1 and Pt-CDO-1 sample are as expected because TaN is stable and acts as very good diffusion barrier of metals and because Pt is a very inert metal. The negative V_{fb} shift of Cu-CDO-1 sample is always explained by Cu drift in dielectric. What is unexpected is that the magnitude of V_{fb} shift of Al-CDO-1 sample is larger than that of Cu-CDO-1 sample.

It is well known that Al is quite stable in contacting with SiO_2 because a very thin self-limiting Al_2O_3 forms between Al and SiO_2 and acts as good diffusion barrier [16-17]. The negligible V_{fb} shift of Al-CDO-2 sample at 30℃ indicates that CDO itself is electrically stable at room temperature. Therefore, the -7.48V V_{fb} shift of Al-CDO-1 sample implies that Al ions can be driven into CDO at room temperature. It is well known that Al ions do not enter SiO_2 under BTS test; the V_{fb} shift of Al-CDO-2 capacitor after BTS at 150℃ would be attributed to the intrinsic instability of CDO, i.e. dielectric polarization [21]. The polarization of CDO film will be discussed in next sub-section. But as Al contacts with the CDO film directly, the V_{fb} shift is well beyond –40V (see Table 3-1). The magnitude of V_{fb} shift of Al-CDO-1 sample excludes the CDO instability effect [V_{fb}(Al-CDO-1) subtracts V_{fb}(Al-CDO-2)] is still very large, and thus the possible cause of this severe instability might be Al ions drifting into CDO film. Fig. 3.6(a) compares the distribution of Al atoms in CDO before and after BTS test at 150℃. It is apparent that

Al ions were driven throughout the whole CDO. Fig. 3.6(b) shows that, similar to Al, Cu can be easily driven into CDO with the same BTS test. It is well known that Cu is a fast diffuser in most of the dielectric materials. This observation confirms that the V_{fb} shift of Cu-CDO-1 sample is due to Cu drift.

TaN is known to be inert in comparison with Al and Cu and is used as a barrier metal between metal interconnect and dielectric thin film. It is not expected to inject ions into dielectric electrical stress. The Ta profiles of TaN-CDO-1 sample are almost identical before and after BTS at 150℃ as shown in Fig. 3.7. This result implies that the V_{fb} shift of the TaN-CDO-1 capacitor listed in Table 3-1 is not due to metal ions. Actually, a slight distortion of C-V curve was observed on the BTS tested TaN-CDO-1 sample. The slightly larger V_{fb} shift of TaN-CDO-1 sample than that of Al-CDO-2 sample is thus attributed to the dielectric polarization together with process damage during TaN deposition.

The apparent Al diffusion into CDO implies the lack of Al_2O_3 formation at the Al/CDO interface [16-17]. Table 3-2 lists the results of pull-stud adhesion test of different metal/CDO and Al/SiO_2 interfaces. As expected, Al shows good adhesion to SiO_2, while both Al and Cu show very poor adhesion to CDO. The poor adhesion between Al and CDO is another side-evidence that no interfacial reaction between Al and CDO occurs. Fortunately, TaN, as a common diffusion barrier material for Cu, is

proved to have good adhesion to CDO.

The lacking formation of self-limited aluminum oxide between Al and CDO film allow Al ions to be driven into CDO film. Besides, the porous structure of CDO film contains nano-pores. Al ions can easily be driven into deep portion of CDO along with these pores. Table 3-3 lists the V_{fb} values of the just fabricated Al-CDO-1 samples after annealing in N_2 ambient at 400℃ for various time periods. The V_{fb} shifts toward negative voltage with the increase of annealing time. This result means that more Al ions diffuse into CDO film under long time thermal anneal. Fig. 3.8 shows the Al depth profile of Al-CDO-1 sample after annealing. The Al metal gate had been removed before SIMS analysis. It is confirmed that Al atoms did diffuse into CDO film after 8 hours annealing. Besides, Al atoms piled-up at CDO/SiO_2 interface and can't diffuse though the SiO_2 layer. This phenomenon is consistent with our hypothesis that the lacking of alumni oxide layer between Al and CDO leads to the drift and/or diffusion of Al into CDO.

3.3.4 Dielectric Polarization Phenomenon of CDO Film

There are four possible mechanisms may cause dielectric C-V instability: (a) the 10 nm thick thermal oxide is unstable; (b) the CDO film is contaminated by mobile ions such as Na, K, Cu, etc.; (c) the CDO film is polarized under electric field; (d)

charges are injected into CDO film under electric field. In the following discussions, these mechanisms are examined one by one.

The quality of the 10 nm thick thermal oxide was examined firstly. A simple Al/ SiO_2 (10nm)/Si MOS capacitor was fabricated (Al-SiO2-1). The dielectric constant obtained from high frequency C-V measurement is around 4.0 with flat-band voltage of -0.2 V. No hysteretic phenomenon was observed during continuous C-V measurements. Therefore, the unstability of the thin thermal oxide is ruled out.

SIMS analysis of blanket CDO film was performed to detect metal contamination. The mobile ions in CDO film, including Na, K, and Cu, are all lower than the detection limit of SIMS analysis. The severe V_{fb} shift after BTS of Al-CDO-1 and Cu-CDO-1 samples can be attributed to the metal ions mainly. However, Pt as a noble metal and TaN as a diffusion barrier metal can not be driven into CDO film but C-V instability phenomenon still occurs. This instability can not be explained by mobile ions and another mechanism must be considered. The dielectric polarization is then thus examined.

It is known that the V_{fb} shift under continuous FVS and RVS may be attributed to dielectric polarization [21]. To avoid the influence of metal gate and metal deposition induced damage, Al-CDO-2 structure with an additional 30nm thick PECVD SiO_2 between CDO and Al metal gate was used to study the role of dielectric polarization

on the electrical instability. Silicon dioxide is known to be a good diffusion barrier of Al metal ions and Al ions can't be drifted across it [16, 17, 22]. The stable C-V characteristics of reference sample Al/ PECVD SiO_2/thermal SiO_2/Si structure indicate that both the PECVD SiO_2 film and the metallization process are well controlled.

Fig. 3.9 shows the high frequency C-V characteristics of the Al-CDO-2 sample measured in both of the FVS and RVS modes for two cycles. The original curve was measured in the FVS mode with voltage swept from –20 V to +10 V. The original C-V curve looks like a normal C-V curve of a typical MIS capacitor. However, as the voltage range expanded to ±40 V, the C-V curve shifted apparently. In the FVS mode, the C-V curve shifted toward the positive voltage axis, while in the RVS mode, the C-V curve shifted toward the negative voltage axis. The magnitudes of V_{fb} shift in both directions are almost identical and the C-V curves are almost overlapped in continuous FVS and RVS measurement cycles. Because the electric field is only about 1.6MV/cm (40V/240nm), the V_{fb} shift can not be explained by electrons (or holes) injection from either gate or substrate through SiO_2 layer. And then it is quite possible that the V_{fb} shift of the Al-CDO-2 sample should be attributed to dielectric polarization [21].

Al-CDO-2 capacitor was electrical stressed at 0.6MV/cm for 30 minutes. The V_{fb}

shifts of Al-CDO-2 sample stressed at 30°C and 150°C are -0.07V and -5.12V, respectively. The C-V curves are shown in Fig. 3.10(a) and (b). The negligible V_{fb} shift of Al-CDO-2 sample at 30°C indicates that the CDO film is electrically stable at room temperature. Fig. 3.11 shows the Arrhenius plot of the magnitude of V_{fb} shift at 0.6 MV/cm. The extracted activation energy for dielectric polarization is 0.39eV. It is observed that the V_{fb} shift of TaN-CDO-1 and Pt-CDO-1 capacitors are slightly larger than the dielectric polarization induced V_{fb} shift so that additional mechanism must be considered.

3.3.5 Carrier Injection in CDO Dielectric

Although the dielectric polarization of CDO film can be used to explain the symmetric C-V shift under electric field and mobile ions can be used to explain the large V_{fb} shift under positive voltage stress with some kinds of metal electrode, there is still another possible mechanism that may cause V_{fb} shift - carrier injection and trapping in CDO film.

For metal-COD-1 samples biased at low electric field such as +0.6MV/cm, it is hard for electron to be injected from Si substrate across thermal oxide into CDO film. Hole-injection from metal gate into CDO film is also unlikely to occur. As metal-CDO-1 samples are biased at –0.6MV/cm, it is still hard for hole to be injected

from Si-substrate across thermal oxide into CDO film, but it is possible for electron to be injected from metal gate into CDO film. To study the carrier transport mechanism, the sample with a nearly quasi metal-insulator-metal (MIM) structure of Al/CDO/N+-Si was fabricated as Al-CDO-MIM. Fig. 3.12(a) shows that the J-E characteristic at low temperature or low electric field can be well fitted with the Schottky emission (SE) model. At high temperature or high electric field, the J-E characteristic could be better fitted with the Frenkel-Poole (FP) model as shown in Fig. 3.12(b). The transition electric field from Schottky emission to Frenkel-Poole emission decreases with the increase of temperature.

Since FP emission is due to field-enhanced thermal excitation of trapped electrons into the conduction band, and the barrier height is the depth of the trap potential well, it is expected that FP emission can occur at lower electric field than Schottky emission. If the low field tunneling mechanism is Schottky emission, it is unreasonable for FP emission to dominate carrier transport at high field. Thus, the observation of Schottky emission at low electric field and FP emission at high temperature is unusual for dielectrics. To explain this phenomenon, the role of Al gate must be considered. It is postulated that the transition of carrier transport mechanism might be attributed to the Al ions induced defects in bulk CDO. As our previous discussion in section 3.3.3, Al ions can be driven into CDO film by electric field [22].

These Al-ions produce trap sites there. More Al ions are driven into CDO film at higher temperature. Therefore, the trap site density increases with the increase of electric field and measurement temperature, and then the carrier transport mechanism changes from Schottky emission to FP emission at high electric field and the transition field decreases with the increase of temperature. This postulation is further verified by the Al-CDO-2 sample. Because of the capped thin PECVD SiO_2 layer on CDO film, Al ions can not enter the bulk CDO. Fig. 3.13 shows that the J-E characteristics of Al-CDO-2 at negative bias can be fitted with the Schottky emission model at high electric field even at 200°C.

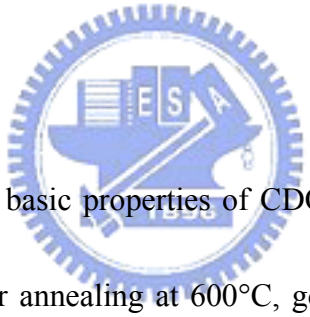
Now the observed electrical instability can be understood with the model proposed in Fig. 3.14. Weak dielectric polarization occurs under electric field at high temperature. If CDO film contacts with metal directly, electrons may be injected from the metal gate as the gate is negatively biased. Both dielectric polarization and electron injection cause V_{fb} shifts toward positive voltage direction slightly. Since the leakage current of CDO film is very low, electron injection can be neglected at typical operation condition of less than 0.2MV/cm. As the gate is positively biased, metal ions such as Cu and Al would be driven into the porous CDO film. The positive metal ions result in large V_{fb} shift toward negative voltage direction. Combined with CDO dielectric polarization phenomenon, V_{fb} shifts seriously.

3.3.6 Electrical Reliability Study of CDO Film

The time-dependent-dielectric-breakdown (TDDB) of Al-CDO-1, Cu-CDO-1 and TaN-CDO-1 capacitors were evaluated at 1MV/cm, 1MV/cm, and 3.5MV/cm, respectively. Fig. 3.15 shows the cumulative failure plot at temperature of 200°C. It is observed that the lifetimes of the three kinds of samples are very close. Since the electric field of TaN-CDO-1 sample is much stronger than that of the other two samples, it means that the lifetime of TaN-CDO-1 sample is much longer than that of the other two samples. It is known that no metal ions were driven into CDO films for the TaN-CDO-1 sample. The long lifetime of the TaN-CDO-1 sample reflects the actual reliability of the CDO film. As discussed in previous section, metal ions trapped in CDO film produce traps so that the carrier injection mechanism changes from Schottky emission to FP emission. It is also known that TDDB lifetime is related to defect density strongly. The short lifetime of the Al-CDO-1 sample and Cu-CDO-1 sample should be related to the injection of Al ions and Cu ions, respectively, into CDO film during TDDB test.

It is known that the carrier transport mechanism at electric field lower than 10MV/cm of the CDO film is Schottky emission but not FN emission and the CDO film is thick enough, it is supposed that the TDDB lifetime of the CDO film follows

the E-model [23-25]. Fig. 3.16 shows the mean-time-to-failure (MTTF) of the TaN-CDO-1 sample as a function of electric field at 200°C. The 10 years MTTF allows an electric field of stronger than 2 MV/cm and the extrapolated MTTF at electric field of 0.5MV/cm is much longer than 10 years by several orders of magnitude. These results indicate that the reliability of CDO film without metal contamination is well beyond the requirement of multi-level interconnection. And, TaN, the commonly used Cu diffusion barrier metal is fully compatible with the CDO film.



3.4 Summary

In this chapter, excellent basic properties of CDO film including low dielectric constant (lower than 2.3) after annealing at 600°C, good thermal stability (no FTIR spectrum change after annealing at 650°C), very little thickness shrinkage (less than 3% after annealing at 650°C), and low leakage current (lower than 1nA/cm^2 at 30°C and 2.5MV/cm) are confirmed in this work.

Our investigation discovered that the lacking formation of Al_2O_3 interfacial layer caused Al ions to migrate into CDO film and CDO porous structure would enhance metal ions movement in it. Although both Al and Cu ions can be driven into CDO under electrical stress, no metal ions are observed in CDO with TaN gate. Furthermore, TaN shows excellent adhesion to CDO. Combining with those good

properties reported previously, CDO is still a very promising material for next generation Cu-interconnect technology. Besides, an electrical instability model considering metal ions diffusion, dielectric polarization, and carrier injection, was proposed to explain the observed electrical instability phenomenon of the CDO film under electrical stress. And this model would be applied to study on all other low-k dielectrics' electrical instability behaviors.

It is concluded that Al and Cu are not suitable metal to contact with CDO film directly because Al ions and Cu ions can be driven into CDO film easily. Fortunately, TaN, a barrier metal for Cu-interconnect system, shows no mobile ions issues when direct contact with CDO film. Electron transport mechanism is identified to be Schottky emission at low electric field and low temperature. As metal ions are injected into CDO film, for example Al and Cu, electron transport mechanism changes to Frenkel-Pool emission at high temperature and high electric field. The injection of metal ions into CDO film also degrades the TDDB lifetime of the film. Fortunately, the commonly used Cu diffusion barrier TaN is an excellent contact metal with CDO film. The 10 years TDDB lifetime allows an electric field stronger than 2 MV/cm and the TDDB lifetime at 0.5MV/cm becomes longer than 10 years by several orders of magnitude. It is thus concluded that the nano-porous ultra low dielectric constant CDO film is a very promising inter-metal dielectric material for

next generation interconnect system.

References

1 R. J. Gutmann, “Advanced silicon IC interconnect technology and design: Present trends and RF wireless implications”, IEEE Transactions on Microwave Theory and Technique, vol. 47, No. 6, pp. 667-774, 1999

2 N. Awaya, H. Inokawa, E. Yamamoto, Y. Okazaki, M. Miyake, Y. Arita, and T. Kobayashi, “Evaluation of a copper metallization process and the electrical characteristics of copper-interconnected quarter-micron CMOS”, IEEE Transactions on Electron Devices, vol. 43, No. 8, pp. 1206-1212, 1996

3 The National Technology Roadmap for Semiconductors, Semiconductor Industry Association, San Jose, CA, 2001

4 H. Golden, C. J. Hawker, and P. S. Ho, ”Designing Porous Low-k Dielectrics”, Semiconductor International, May First, 2001.

5 N. Aoi, “Novel porous films having low dielectric constants synthesized by liquid phase silylation of spin-on glass sol for intermetal dielectrics”, Japan Journal of Applied Physics, Part 1, vol. 36, No. 3B, pp. 1355-1359, 1997

6 W. Wu, W. E. Wallace, E. K. Lin, G. W. Lynn, C. J. Glinka, E. T. Ryan, and H. M. Ho, “Properties of nanoporous silica thin films determined by high-resolution x-ray reflectivity and small-angle neutron scattering”, Journal of Applied Physics, vol. 87, No. 3, pp. 1193-1200, 2000

7 M. H. Jo, H. H. Park, D. J. Kim, S. H. Hyun, S. Y. Choi, and J. T. Paik, “SiO_2 aerogel film as a novel intermetal dielectric”, Journal of Applied Physics, vol. 82, No. 3, pp. 1299-1394, 1997

8 D. R. Denison, J. C. Barbour, and J. H. Burkart, “Low dielectric constant, fluorine-doped SiO_2 for intermetal dielectric”, J. Vac. Sci, Technology A, vol. 14, No. 3, pp. 1124-1126, 1996

9 M. Tada, Y. Harada, K. Hijioka, H. Ohtake, T. Takeuchi, S. Saito, T. Onodera, M. Hiroi, N. Furutake, and Y. Hayashi, “Cu dual damascene interconnects in porous organosilica film with organic hard-mask and etch-stop layers for 70 nm-node ULSIs”, IEEE Int. Interconnect Technology Conf., pp. 12-14, 2002

10 J. C. Lin, R. Augur, S. L. Shue, C. H. Yu, M. S. Liang, A. Vijayendran, T. Suwwan de Felipe, and M. Danek, “CVD barriers for Cu with nanoporous ultra low-k: integration and reliability”, IEEE Int. Interconnect Technology Conf., pp. 21-23, 2002

11 H.J. Lee, Y. H. Kim, J. Y. Kim, E. K. Lin, B. J. Bauer, W.l. Wu, and H. J. Kim, “Structural characterization of porous low-k SiOC thin films using x-ray porosimetry”, IEEE Int. Interconnect Technology Conf., pp. 54-56, 2002

12 C. Waldfried, Q. Han, O. Escorica, A. Margolis, R. Albano, and I. Berry, “Single wafer RapidCuringTM of porous low-k materials”, IEEE Int. Interconnect Technology Conf., pp. 226-228, 2002

13 K. Buchanan, K. Beekmann, K.Giles, J-C. Yeoh, H.Donohue, “Characterisation and integration of CVD ultra low k films (k<2.2) for dual damascene IMD Applications”, Proceeding of Advanced Metallization Conference, pp. 73-77, 2001

14 K. L. Fang, B. Y. Tsui, C. C. Yang, M. C. Chen, S. D. Lee, K. Beekmann, T. Wilby, K. Giles, and S. Ishaq, “Electrical and material stability of OrionTM CVD ultra low-k dielectric film for copper interconnection”, IEEE Int. Interconnect Technology Conf., pp. 60-62, 2002

15 S. P. Murarka, and S. W. Hymes, “Copper metallization for ULSI and beyond”, Critical Review of Solid State Materials Science, vol. 20, No. 2, pp. 87-124, 1995

16 A. L. S. Loke, J. T. Wetzel, P. H. Townsend, T. Tanabe, R. N. Vrtis, M. P. Zussman,

D. Kumar, C. Ryu, and S. S. Wang, “Kinetics of copper drift in low-kappa polymer interlevel dielectrics”, IEEE Transactions on Electron Devices, vol. 46, No. 11, pp. 2178-2187, 1999

17 A. Mallikarjunan, S. P. Murarka, and T. M. Lu, “Metal drift behavior in low dielectric constant organosiloxane polymer”, Applied Physics Letters, vol. 79, No. 12, pp. 1855-1857, 2001

18 A. Jain, S. Rogojevic, S. Ponoth, N. Agarwal, I. Matthew, W. N. Gill, P. Persans, M.Tomozawa, J. L. Plawsky, E. Simonyi, “Porous silica materials as low-k dielectrics for electronic and optical interconnects”, Thin Solid Films, vol. 398-399, No. 1-2, pp. 513-522, 2001

19 SIA International Technology Roadmap for Semiconductors, Semiconductor Industry Association, San Jose, CA, 2001

20 K. Buchanan, K. Beekmann, K.Giles, J-C. Yeoh, H.Donohue, “Characterisation and integration of CVD ultra low k films (k<2.2) for dual damascene IMD applications,” Proc. Advanced Metallization Conference, pp. 73-77, 2001

21 B. Y. Tsui, K. L. Fang, S. D. Lee, “Electrical instability of low-dielectric constant diffusion barrier film (a-SiC : H) for copper interconnect”, IEEE Transactions on Electron Devices, vol. 48, No. 10, pp. 2375-2383, 2001

22 K. L. Fang and B. Y. Tsui, “Metal Drift instability in Porous Low dielectric Constant Film”, Journal of Applied Physics, vol. 93, No. 9, pp 5546-5550, 2003

23 J. W. McPeherson and H. C. Mogul, “Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in SiO_2 thin films”, Journal of Applied Physics, vol. 84, No. 3, pp 1513-1523, 1998

24 K. C. Boyko, and D. L. Gerlach, “Time Dependent Dielectric Breakdown of 210A Oxides”, IEEE Int. Reliability Physics Symposium, pp. 7-12, 1989

25 K. F. Schuegrapf and C. Hu, “Hole injection oxide breakdown model for very low voltage lifetime extrapolation”, IEEE Int. Reliability Physics Symposium, pp. 7-12, 1993

Table 3-1 Flat band voltage shift of MIS structures with various metal gate materials after BTS test at 0.6MV/cm for 30 minutes

Temperature	Al-CDO-1	Cu-CDO-1	TaN-CDO-1	Pt-CDO-1	Al-CDO-2 (V)
30°C	-7.48 V	-3.2 V	-2.74 V	-1.59 V	-0.07
150°C	＜-40 V	-40 V	-9.6 V	-6.23 V	-5.12

Table 3-2 Results of pull-stud adhesion test of different metal/CDO interface and Al/SiO_2 interface

	Al/CDO	Cu/CDO	TaN/CDO	Al/SiO_2
Average (MPa)	16.82	19.1	51.92	47.02
Standard Deviation (MPa)	5.62	9.53	11.46	7.37

Table 3-3 Flat band voltage shift of Al-CDO-1 sample after annealing at 400℃ for various time periods

CDO	0 hour	2 hours	8 hours
Average (V)	-1.59	-2.73	-3.52
Standard deviation (V)	0.24	0.31	0.33

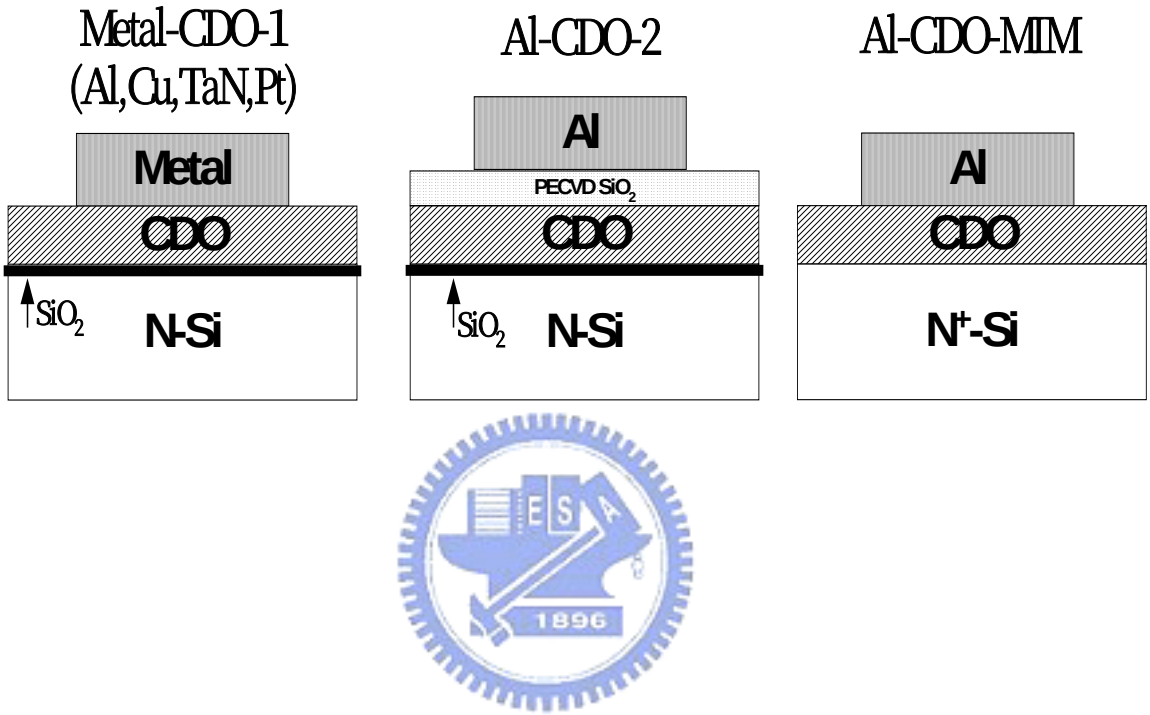


Fig. 3.1 Schematic drawings of the MIS structures used in this work. Metal-CDO-1 : Metal/ CDO (200 nm)/ SiO_2 (10 nm)/n-Si. Al-CDO-2 : Al(500 nm)/ PECVD SiO_2 (30 nm)/ CDO (200 nm)/ SiO_2 (10 nm)/n-Si. Al-CDO-MIM : Al (500 nm)/ CDO (200 nm)/n+-Si.

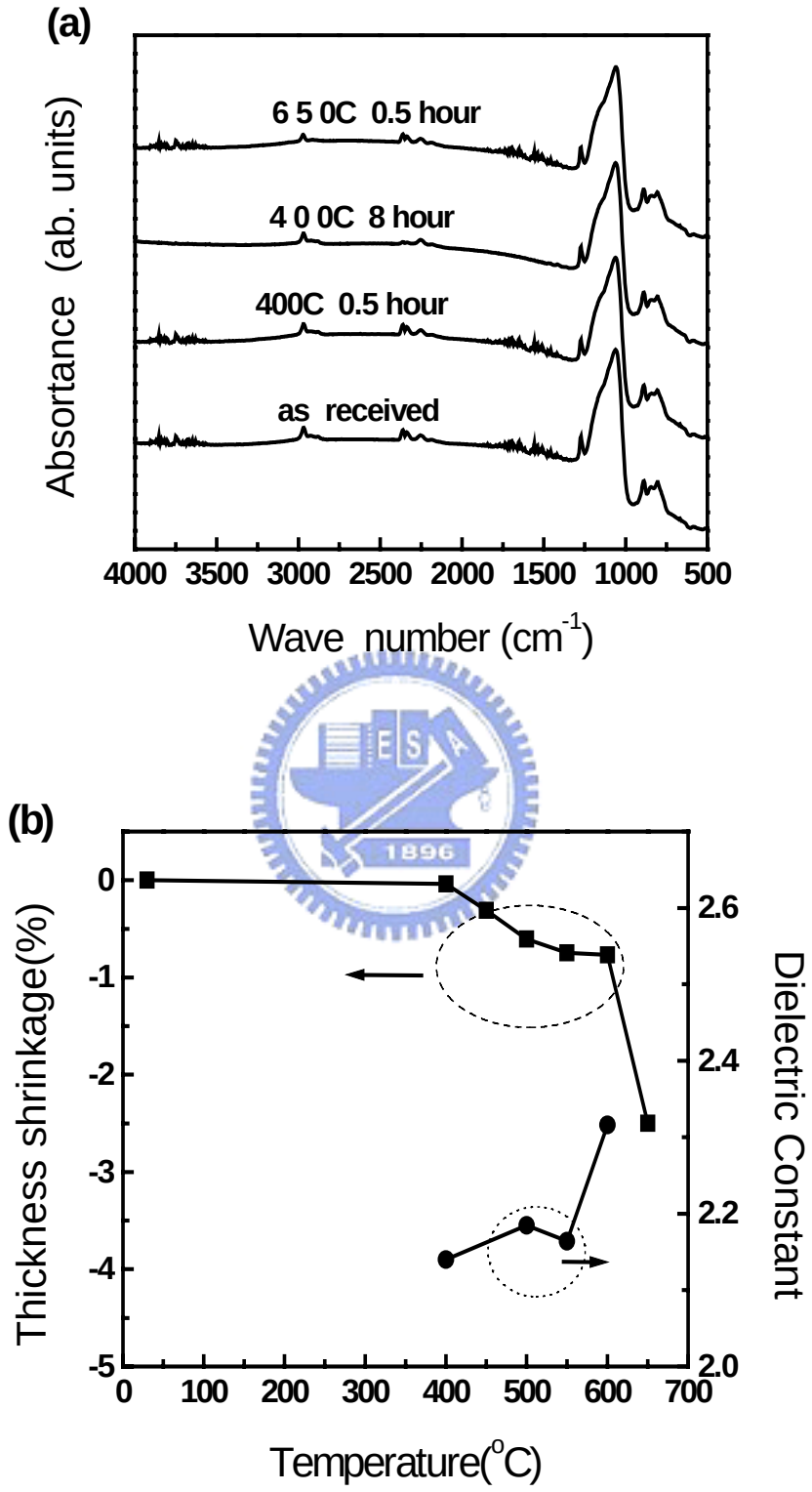


Fig. 3.2 (a) FTIR spectra and (b) thickness shrinkage and dielectric constant variation of CDO film after thermal annealing at different temperatures.

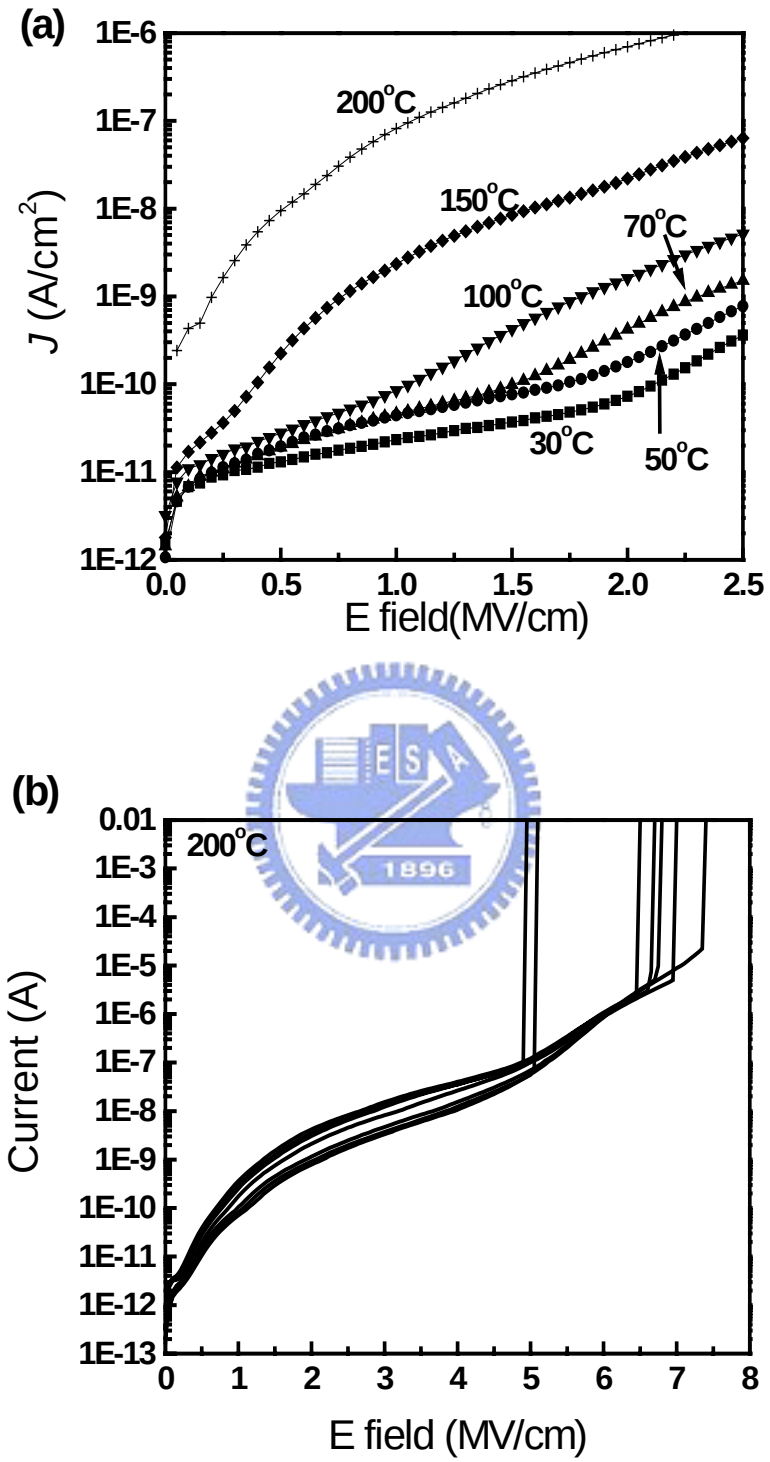


Fig. 3.3 (a) Current density-electric field characteristic of Al-COD-MIM sample measured at different temperatures. (b) The breakdown characteristics of Al-CDO-MIM capacitors at 200°C

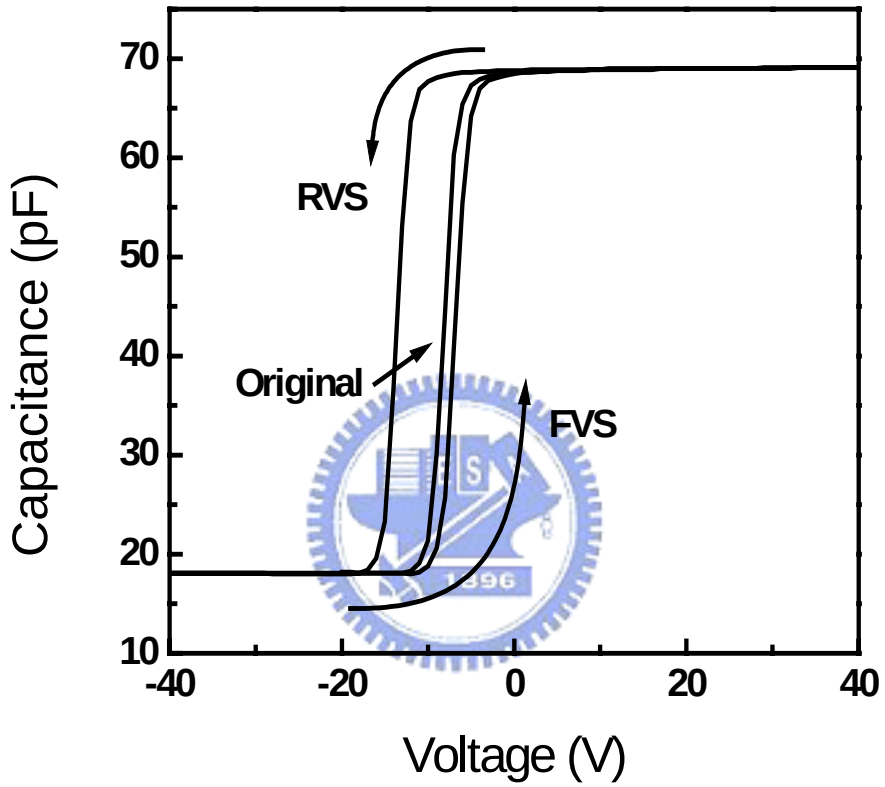


Fig. 3.4 Capacitance-voltage curves of Al-CDO-1 sample measured from inversion mode to accumulation mode (FVS) and from accumulation mode to inversion mode (RVS)

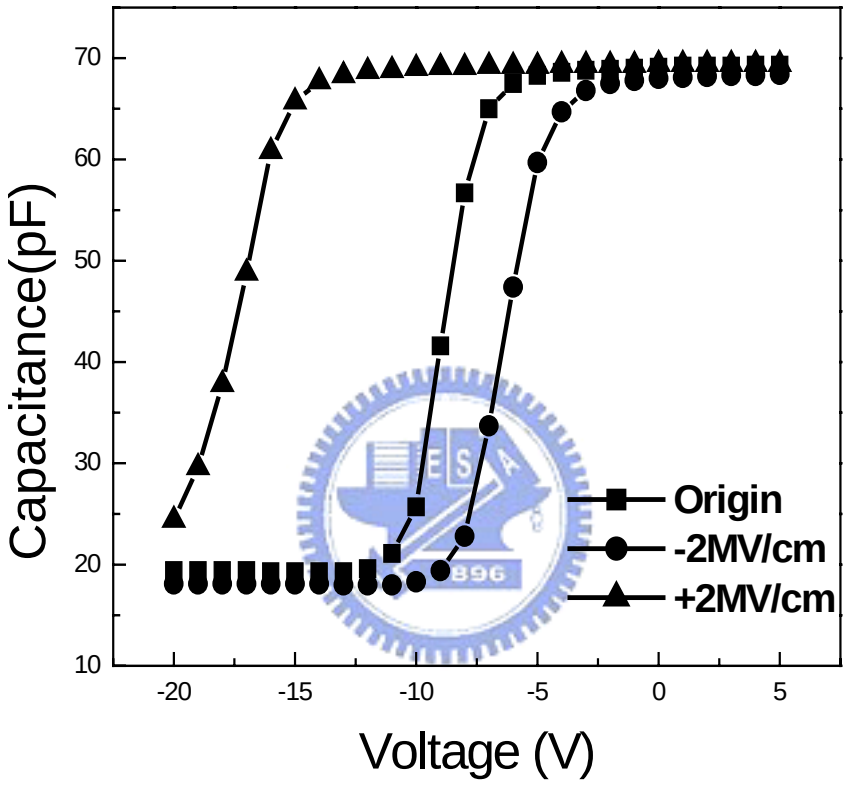


Fig. 3.5 Capacitance-voltage curves of Al-CDO-1 sample after electrical stress at -2MV/cm and +2MV/cm fro 4 minutes.

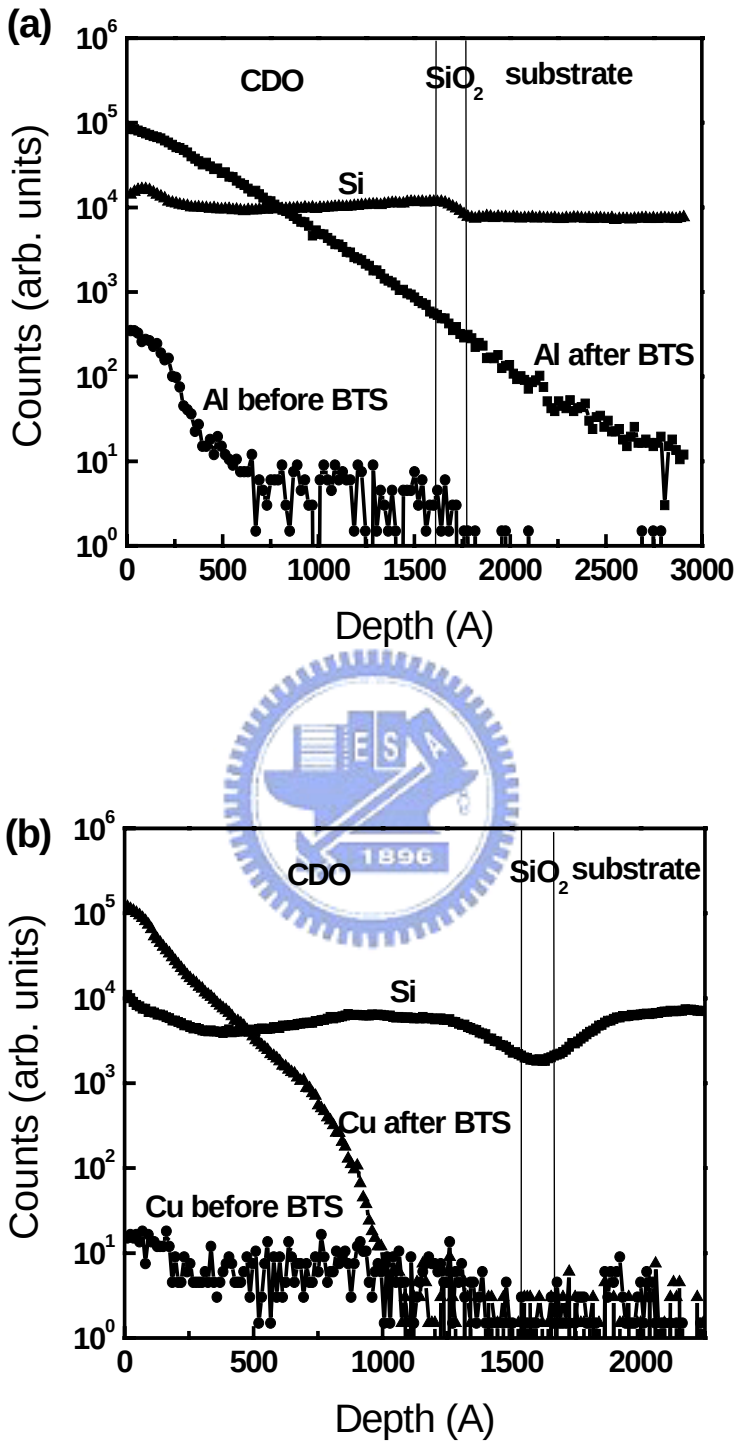


Fig. 3.6 SIMS depth profiles of (a) Al-CDO-1 sample and (b) Cu-CDO-1 sample before and after BTS test at +1 MV/cm and 200℃ for 60 min.

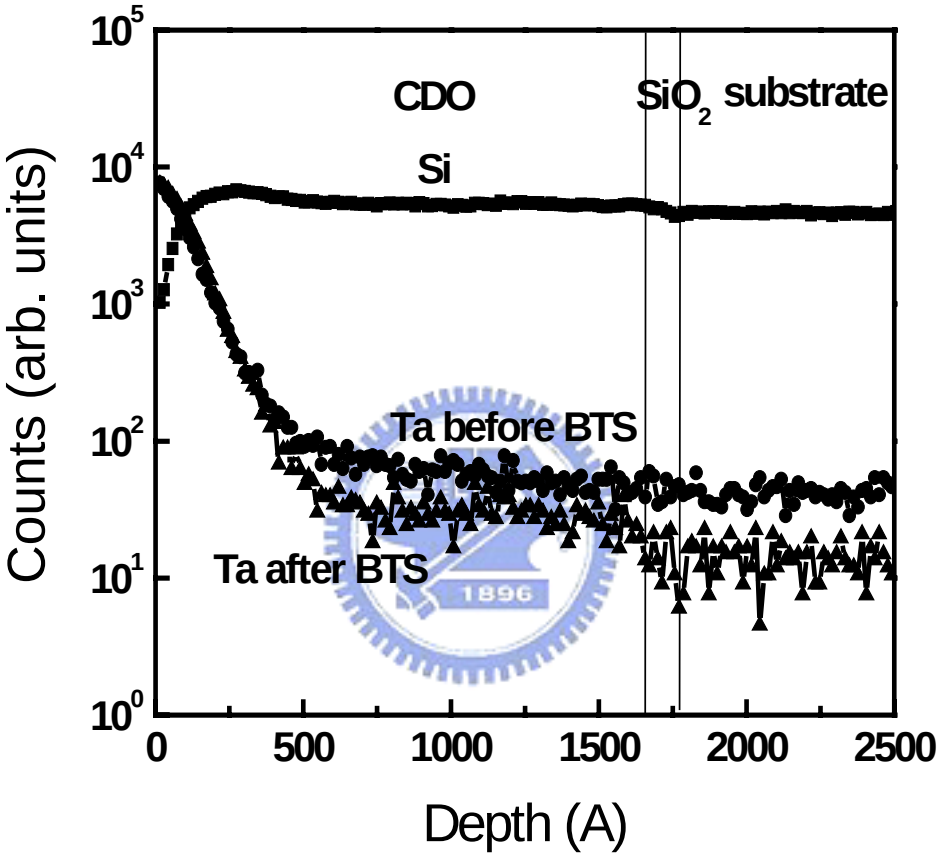


Fig. 3.7 SIMS depth profiles of TaN-CDO-1 sample before and after BTS test at +1 MV/cm and 200℃ for 60 min.

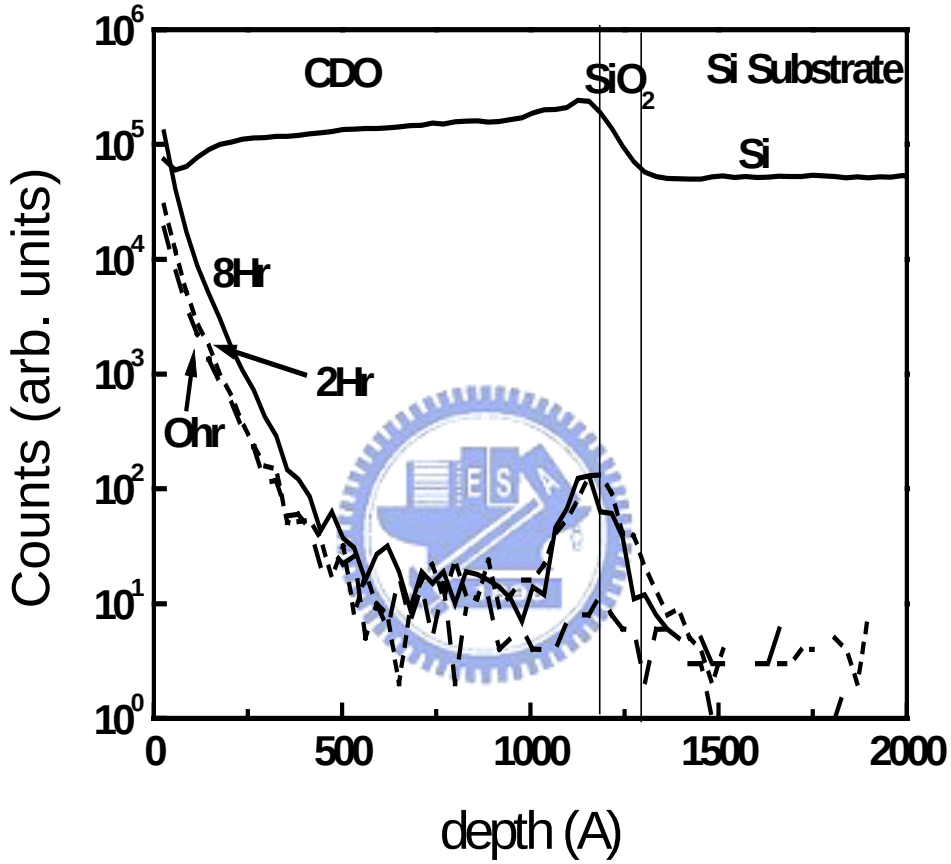


Fig. 3.8 SIMS depth profiles of Al-CDO-1 samples after annealing at 400℃ for various time periods

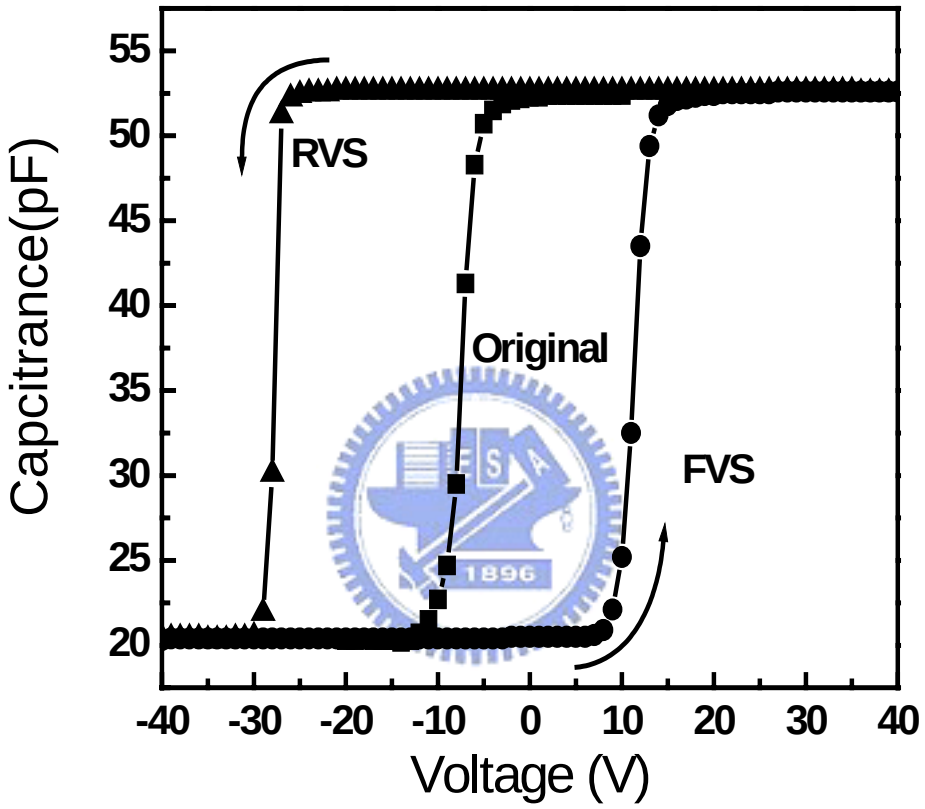


Fig. 3.9 Capacitance-voltage curves of Al-CDO-2 sample with different voltage ranges and different sweep directions.

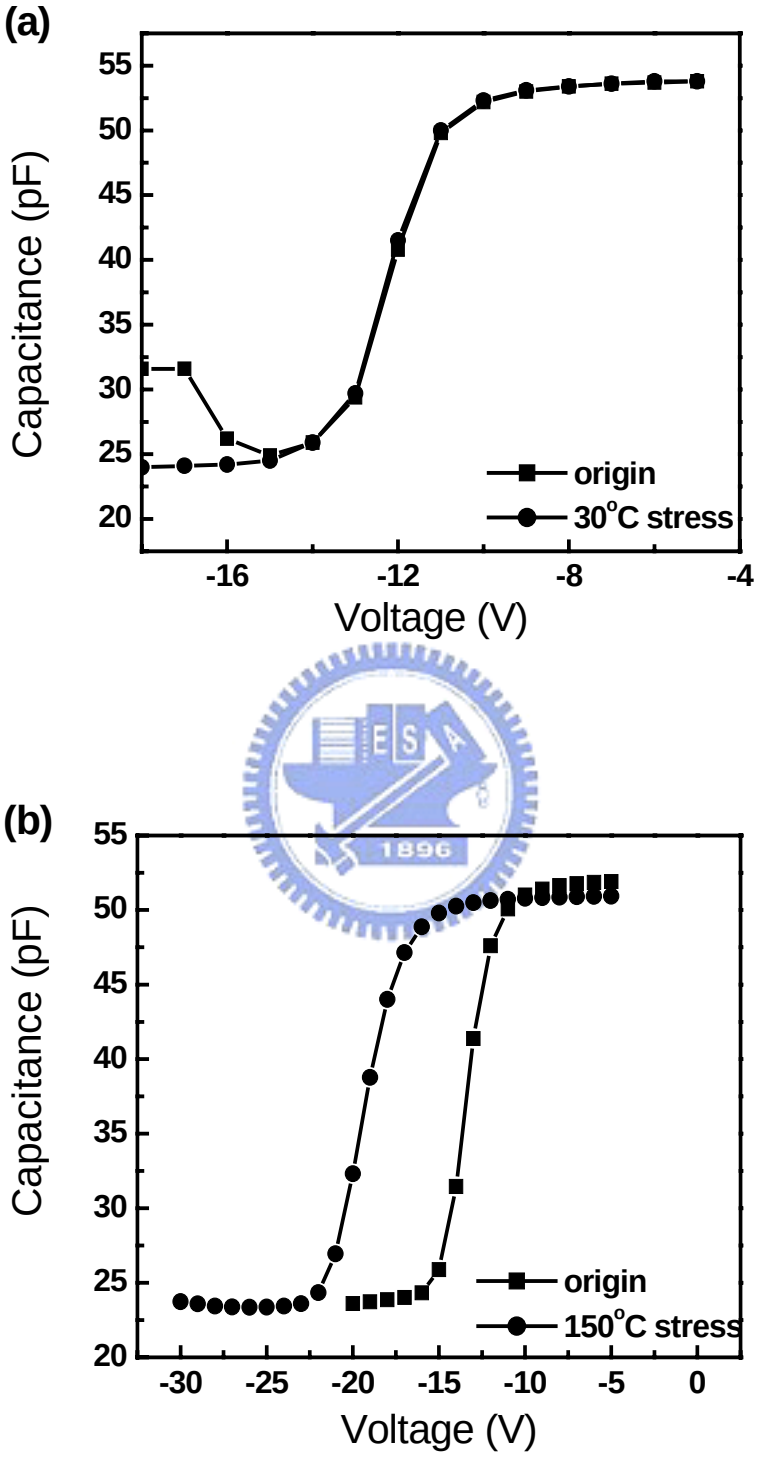


Fig. 3.10 Capacitance-voltage curves result of Al-CDO-2 sample after BTS at (a) room temperature and (b) 150°C. The electric field is 0.6MV/cm

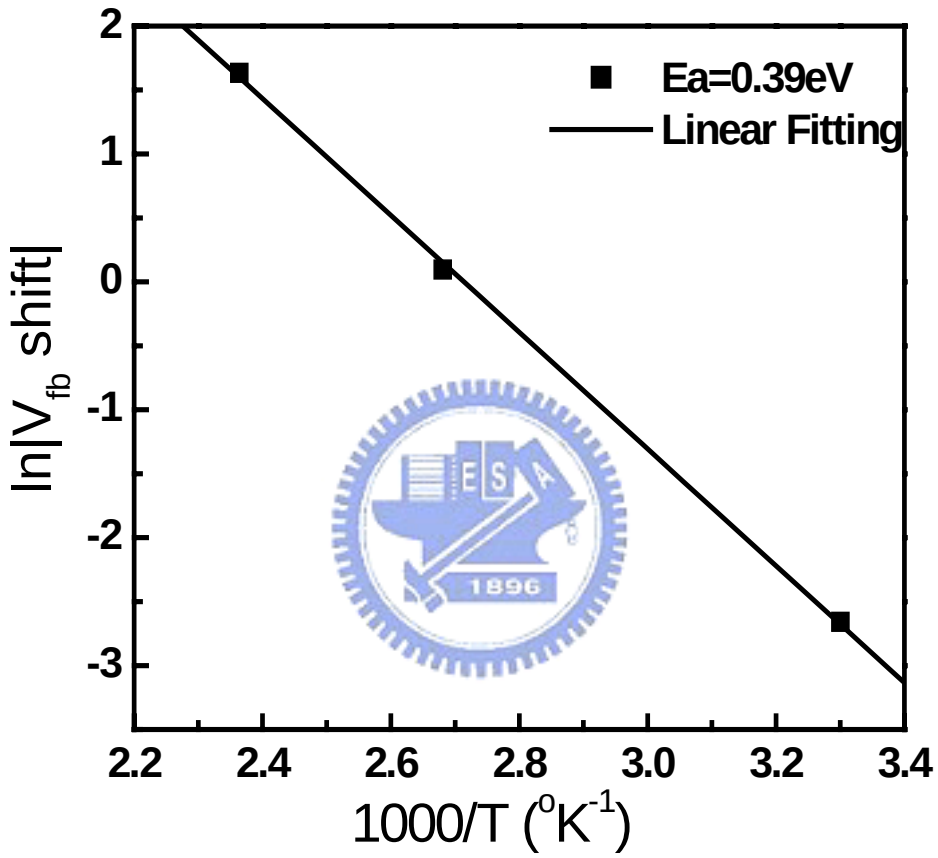


Fig. 3.11 Arrhenious plot of the dielectric polarization of CDO film.

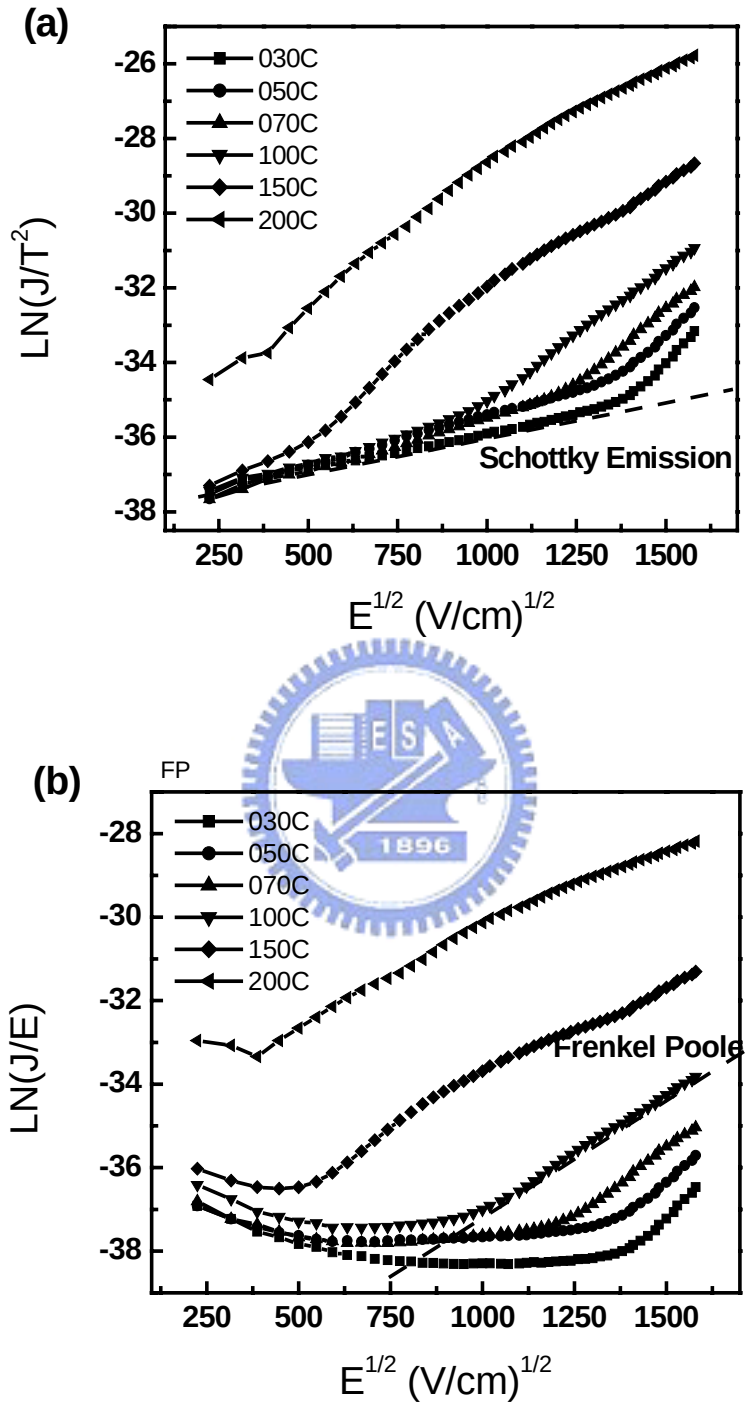


Fig. 3.12 The J-E characteristic of Al-CDO-MIM sample can be well fitted by (a) Schottky emission model at low temperature and low electric field and (b) Frenkel-Poole model at high temperature and high electric field.

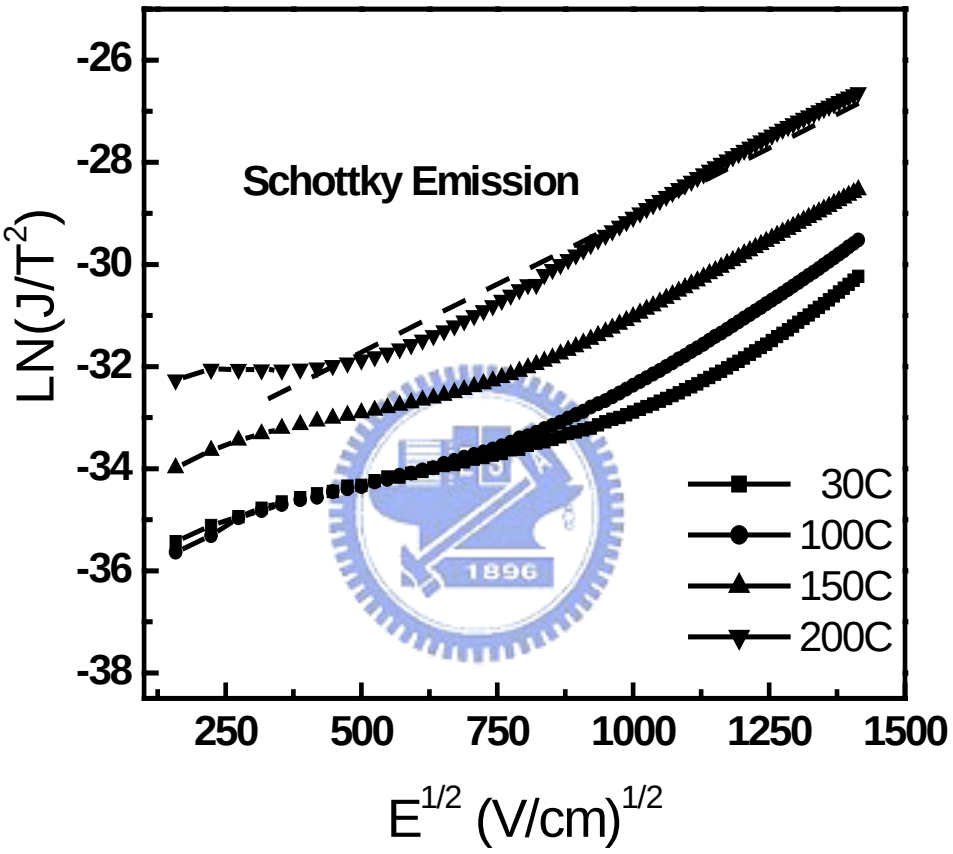


Fig. 3.13 The J-E characteristic of Al-CDO-2 sample at negative gate voltage can be well fitted by Schottky emission model from room temperature to 200°C.

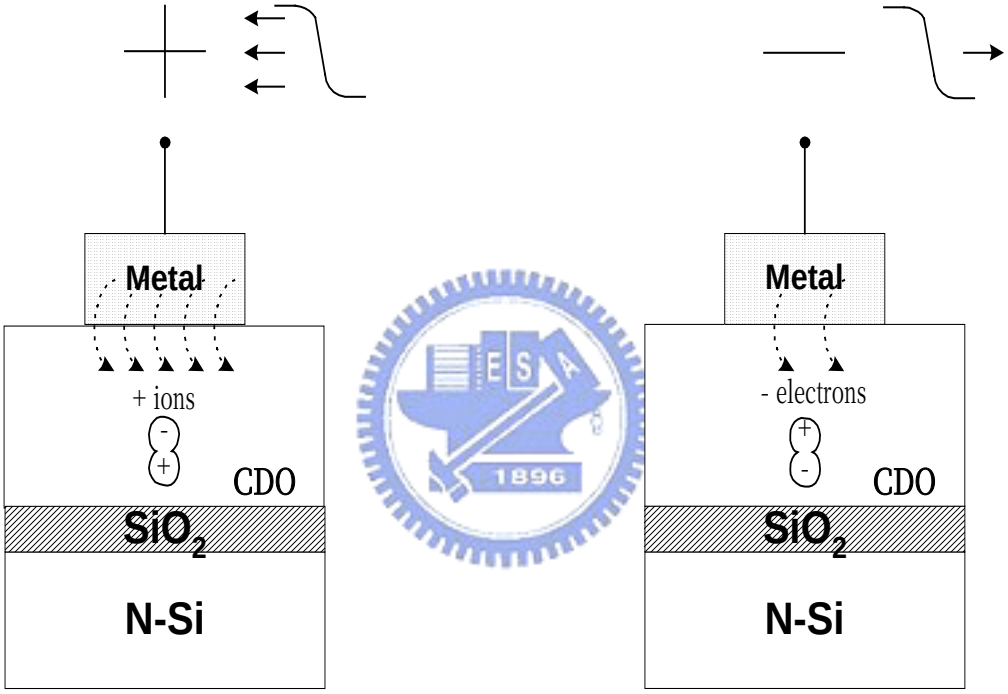


Fig. 3.14 Proposed model to explain the observed electrical instability of Metal-CDO-1 capacitors.

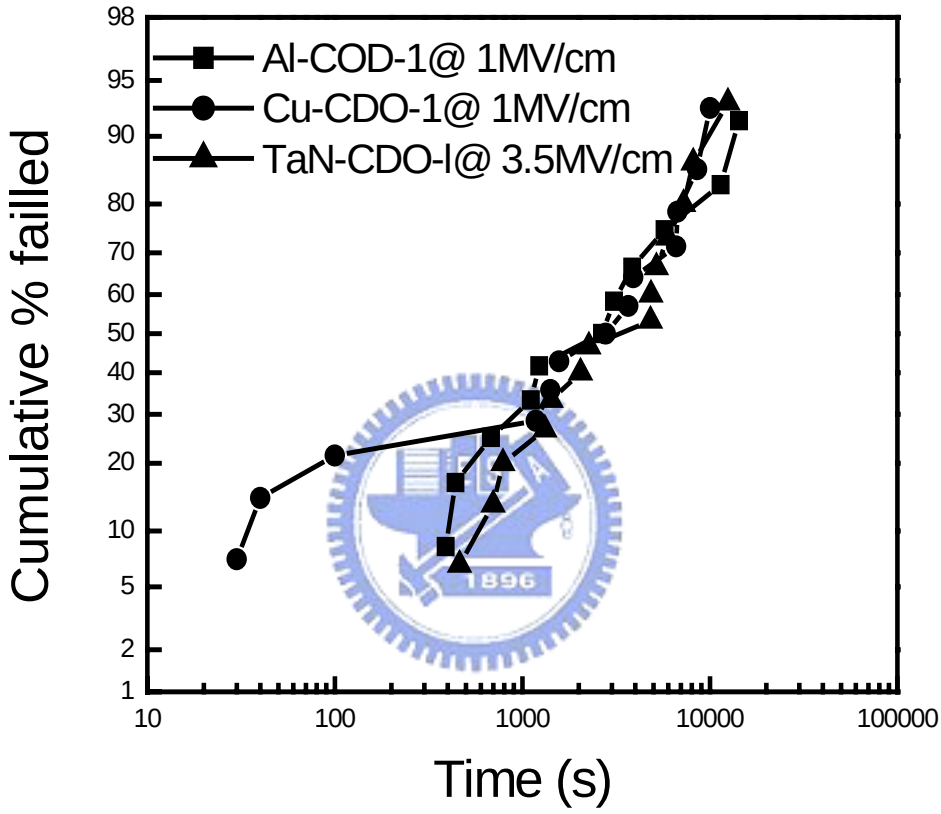


Fig. 3.15 The cumulative TDDB failure of Al-CDO-1, Cu-CDO-1 and TaN-CDO-1 samples stressed at 1MV/cm, 1MV/cm, and 3.5MV/cm, respectively. The temperature is 200°C.

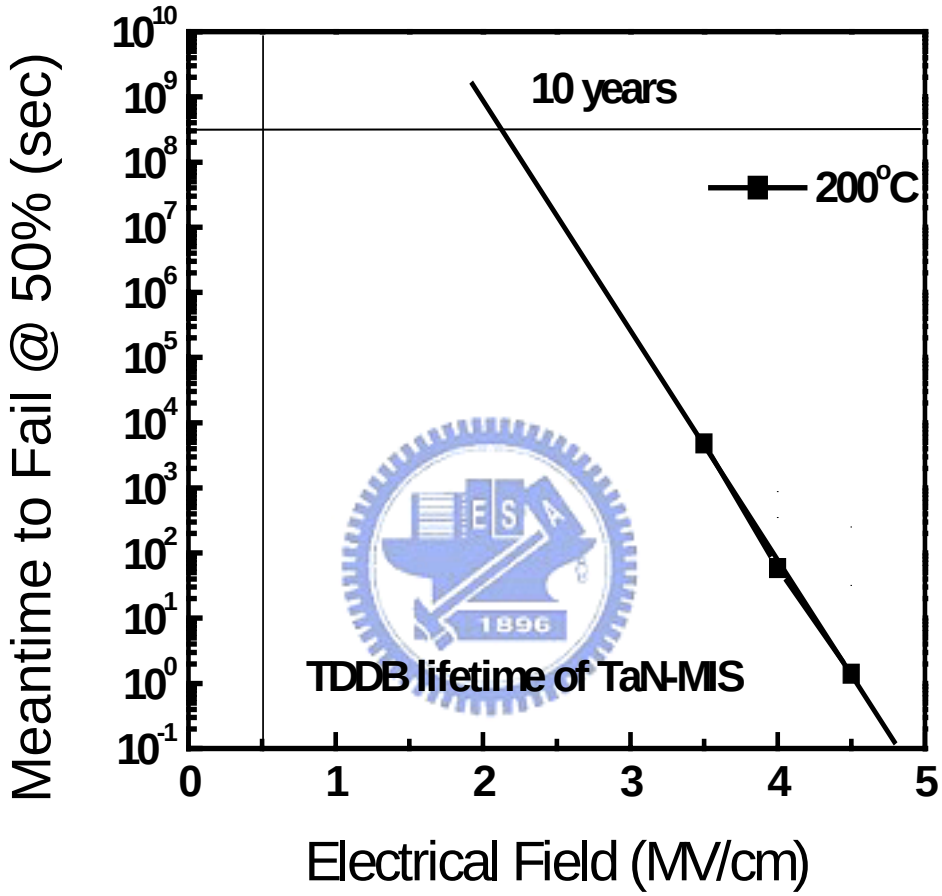


Fig. 3.16 Extrapolation of TDDB lifetime of TaN-CDO-1 sample at 200°C according to E-model.

Chapter 4

Low Dielectric Constant Diffusion Barrier Film Silicon Carbide For Copper Interconnect

4.1 Introductions

Copper (Cu) has been recognized as the most suitable alternative for aluminum as wiring material because of its low electrical resistivity and excellent electromigration resistance [1,2]. Dual damascene process is the well-accepted patterning technology because Cu film is hard to be patterned by plasma etches. It is also known that Cu is a serious contamination source for both silicon and silicon dioxide. To prevent Cu from diffusion into IMD, Cu must be sealed using diffusion barriers. Fig. 4.1 shows the typical Cu interconnect structure. The main IMD is some kind of low dielectric constant (low-k) materials. A dielectric diffusion barrier layer must be deposited on Cu wires to seal Cu and serve as etch stop layer during via hole etch of the next metal layer. The same material is usually used as etch stop layer during trench etch if necessary. Silicon nitride (SiN) is the currently used material because it has been used as a masking and passivating layer for a long time to against diffusion of metal ions and moisture [3-5]. Unfortunately, the relative high dielectric constant (~7) of silicon nitride conflicts with the requirement of low dielectric

constant IMD [6]. The impact of SiN on interconnection capacitance increases with the decrease of dielectric constant of main IMD. Therefore, a newly developed dielectric barrier material amorphous SiC (a-SiC, simplified as SiC herein after) attracts more attentions recently [7]. It is also regarded as the only one candidate to replace SiN as dielectric diffusion barrier and etch stop layer [6-7].

The SiC film can be deposited in chemical vapor deposition (CVD) system using Trimethylsilane (3MS) as a precursor. Film with good material properties of low dielectric constant (<5), low film stress, high thermal stability, high breakdown field (>2MV/cm), and low leakage current at room temperature had been reported [12]. However, almost no study has been performed to electrically emphasize the stability and reliability issues of SiC film.

In this chapter, we evaluate the dielectric barrier effectiveness for Cu penetration with regard to SiC film with different deposition conditions. The electrical reliability and electrical instabilities of SiC film were reported for the first time. The film was stressed at various electric field and temperature. The instabilities were evaluated by the capacitance-voltage (C-V) characteristic of the metal/insulator/Si (MIS) capacitor. The effects of electric field, polarity, and temperature were studied. Two mechanisms were proposed to explain the observed electrical instabilities at high and low electric field. The carrier transport mechanism through SiC film was also identified.

4.2 Experimental Details

Simple MIS capacitor structure was used to study the electrical stability of SiC film. The starting material is boron-doped (100)-oriented 8-inches Si wafer. The resistivity is 2-4 ohm-cm. To minimize the influence of interface instability, a 10 nm thick SiO_2 was thermally grown before the deposition of SiC film. The MIS structures can be divided into three categories. The film structure of Al-SiC-1 sample is Al(500 nm)/SiC(90 nm)/ SiO_2 (10 nm)/Si. Most samples are in this structure and they were used to study the electrical stability of SiC film. MIS structure using Cu gate and heavily doped n-type Si substrate was fabricated (Cu-SiC-MIM) to study the SiC barrier properties. The sandwiched structure is Cu(500 nm)/SiC(90 nm)/n+-Si. The film structure of Cu-SiC-1 sample is Cu(500 nm)/SiC(90 nm)/Fluorinated Silicate Glass (FSG)(450 nm)/ SiO_2 (10 nm)/Si. It is used to evaluate the barrier ability of SiC against Cu diffusion. The structure of reference sample is Cu(500 nm)/FSG(750 nm)/ SiO_2 (10 nm)/Si and is denoted as Cu-FSG-1. Because of the existence of thermal oxide and the work function difference between gate and substrate, the above structures are asymmetric. Almost symmetric MIS structure using Al gate and heavily doped n-type Si substrate was fabricated (Al-SiC-MIM) to study the carrier transport mechanism. The sandwiched structure is Al(500 nm)/SiC(90 nm)/n+-Si The simplest Al(500 nm)/ SiO_2(10 nm)/Si structure (Al-SiO2-1) was also fabricated to make sure

the quality of the 10 nm thick SiO_2 and the SiO_2/Si interface. Fig.4.2 shows the schematic drawings of the six sample structures.

FSG film was deposited in a high-density-plasma chemical vapor deposition system (HDPCVD) and SiC films were deposited plasma-enhanced chemical vapor deposition system (PECVD). The SiC films were deposited at 400 ℃ using 3MS organosilicon gas as a precursor with N_2 and/or N_2O as carrier gas. Table 4-1 lists the deposition conditions of three different SiC films denoted as SiC(1), SiC(2), and SiC(3). The metal gate is wet etched to 800umx800um in square shape. For those samples will receive high temperature measurement, a 30 nm thick SiN layer was deposited on sample surface to prevent samples from oxidation.

The thickness of the deposited SiC film was measured by ellipsometry method with multi-angle and multi-wavelength. The dielectric constant of the SiC film was calculated from the capacitance of MIS-2 structure at zero voltage or MIS-1 structure at accumulation mode. The effect of 10 nm thick thermal oxide was corrected using the MIS-3 structure. Moisture uptake was evaluated by thermal desorption spectroscopy (TDS). The atomic composition was determined by Rutherford Backscattering Spectrometry (RBS) analysis and the major chemical bonds were identified using Electron Spectroscopy for Chemical Analysis (ESCA).

Capacitance-voltage (C-V) measurement was performed to evaluate the SiC film

stability using an impedance meter of model Agilent 4284A. Bias temperature stress (BTS) tests under various temperatures and electric fields were performed. Flat-band voltages before and after BTS were extracted from high frequency (100 KHz) C-V characteristic with voltage swept either from accumulation mode to inversion mode (forward voltage sweep, FVS) or from inversion mode to accumulation mode (reverse voltage sweep, RVS).

4.3 Study on Silicon Carbide Films

4.3.1 Fundamental Properties of Silicon Carbide Films

Fundamental properties of the deposited SiC film were characterized at first. The dielectric constant of the SiC films calculated from Al-SiC-1 structure is listed in Table 4-2 and is apparently lower than the dielectric constant of silicon nitride. TDS analysis shows the moisture out-gassing of three different SiC films after storage in cleanroom environment for 2 weeks. SiC(1) film exhibits a little more moisture out-gassing then the others two SiC films (Fig. 4.3). Because the deposited SiC(2) and SiC(3) films are very inert to moisture, the Al-SiC-1 samples with SiC(2) film stored in non-cleanroom environment show identical high frequency C-V characteristics to the as-fabricated samples.

In order to evaluate the barrier property of SiC films again Cu diffusion, continuous BTS were performed on Cu-SiC-MIM structure at +2MV/cm and 200℃

for 500 minutes. Fig. 4.4 shows the BTS results of the three SiC films. SiC(2) shows the best Cu barrier property then SiC(3) and SiC(1) shows the worst barrier property. Besides, continuous BTS tests of SiC(2) at +1 MV/cm and 200 ℃ were performed on the Cu-SiC-1 and Cu-FSG-1 samples. Fig. 4.5(a) compares the flat-band voltage (V_{fb}) shift of the two samples. It is obvious that Cu was driven into FSG film during BTS and cause flat-band voltage shift on the samples without diffusion barrier layer (Cu-FSG-1). On the contrary, very small V_{fb} shift was observed on the samples with SiC barrier layer after BTS for two hours. Fig. 4.5(b) shows the C-V characteristics of the Cu-SiC-1 sample after BTS for various lengths of time. Only slightly C-V shift was observed after BTS. Although the small flat-band voltage shift might be attributed to slightly Cu ions drift into SiC film, we will show that the instability of SiC film also plays role on the small flat-band voltage shift later at next section.

Fig. 4.6(a) and (b) show the leakage current versus time of the Cu-SiC-MIM capacitors biased at 2 MV/cm and 150℃ and 3 MV/cm and 200℃, respectively. It is observed that by increasing the nitrogrn content, the leakage current can be suppressed effectively. But moderate nitrogen content (SiC(2)) results in the longest TDDB lifetime. It is possible that the gas ratio and composition during SiC deposition affect the micro-structure of the film which in turn affect the dielectric constant, leakage current, and TDDB lifetime. Table 4-2 listed the summarized basic

characteristics of three different SiC films.

4.3.2 Electrical Instability of SiC Films

In previous section, SiC films deposited at different deposition conditions were compared. SiC(2) film was chosen for further study. All of the above results indicated that the SiC(2) film is similar to or better than that reported in [6]. However, the hysteresis phenomenon was coincidentally found. During the measurement of C-V characteristics of the Al-SIC-1 samples, we found it unexpectedly that there was serious V_{fb} shift after wide range voltage sweep.

Fig. 4.7 shows the high frequency C-V characteristics measured in both of the FVS and RVS modes for two cycles. The original curve was measured in the FVS mode with voltage swept from –10 V to +10 V. Because the total dielectric thickness including SiC film and thermal oxide is 100 nm, the maximum electric field is about 1MV/cm. The original C-V curve looks like a normal C-V curve of a typical MIS capacitor. However, as the voltage range is expanded to ±40 V, the C-V curve shifted apparently. In the FVS mode, the C-V curve shifted toward the positive voltage axis, while in the RVS mode, the C-V curve shifted toward the negative voltage axis. The magnitudes of V_{fb} shift in both directions are almost identical and the C-V curves are almost overlapped in continuous FVS and RVS measurement cycles. Table 4-3 lists

the flat band voltages measured by FVS and RVS sweep modes with various voltage ranges. It is found that there is a threshold voltage of about 18 V (~1.8 MV/cm). With electric field lower than 1.8 MV/cm, no hysteresis phenomenon would occur.

Although the C-V characteristic is stable under room temperature and low field measurement, low electric field stress at high temperature still results in instability of the Al-SiC-1 capacitor. Fig.4.8(a), (b), and (c) show the C-V curves measured at room temperature after BTS at 200 ℃ and ±0.4, ±0.5, and ±0.6 MV/cm, respectively, for 3 hours. It is obvious that the C-V curves distorted and shifted after BTS. Except serious increase of interface state density, the magnitudes of V_{fb} shift after positive and negative electrical field stress are asymmetric. It is quite different with that shown in Fig.4.7. Fig.4.9(a) and (b) show the C-V curves measured at room temperature after BTS at 150 and 175 ℃, respectively, for 3 hours. The electric field was fixed at ±0.5 MV/cm. The shift and distortion of C-V curves were also observed but the magnitude decreased with the decrease of the BTS temperature. These results indicate that a much lower electric field at high temperature can cause asymmetric instability. Furthermore, the mechanism of asymmetric instability should be temperature dependent.

4.3.3 Dielectric Polarization

Preliminary C-V measurements of the SiC film (Al-SiC-1 structure) demonstrated certain instabilities that are not typical of MIS structures incorporating clean thermal oxides. The instabilities are prevalent, even at room temperature, to such a degree that reliable C-V characteristic is difficult to be measured. There are four possible mechanisms may cause dielectric instability : (a) the 10 nm thick thermal oxide is unstable; (b) the SiC film is contaminated by mobile ions such as Na, K, Cu, etc.; (c) the SiC film is polarized under electric field; (d) charges are injected into SiC film under electric field. In the following subsections, these mechanisms are examined by further experiments.

The quality of the 10 nm thick thermal oxide was examined firstly. A simple Al/ SiO_2 (10nm)/Si MOS capacitor (Al-SiO2-1) was fabricated. The dielectric constant obtained from high frequency C-V measurement is around 4.0 with flat-band voltage of -0.2 V. There is no any hysteretic phenomenon was observed. Therefore, the unstable of the thin thermal oxide is ruled out. Mobile ion contamination in SiC film is improbable. The SiC film had demonstrated very good barrier ability against Cu diffusion. If the room temperature instability should attribute to mobile ion, apparent C-V shift should have been observed in Fig. 4.5(b). SIMS analysis was performed to detect metal contamination of the Al-SiC-1 samples after etching away of the Al gate. The mobile ions in SiC film, including Na, K, and Cu, are lower than the detection

limit of SIMS analysis.

Since the possibility of thermal oxide instability and mobile ion contamination are both ruled-out. We now examine the mechanism of dielectric polarization and charge injection.

The polarization of dielectrics in MIS structure had been reported long ago [8-10]. It is characterized by a shift of the C-V curve in the same direction as that caused by positive ion migration. The amount of shift will depends on the applied electric field and is symmetric for both polarities. The polarization rate is increased with temperature. Re-examining Table 4-3, it is observed that the shift of the C-V curve becomes more symmetric as the electric field becomes stronger. An electric field stress at ±20 V (2 MV/cm) and 25 ℃ was performed on the Al-SiC-1 samples. The electric field was chosen based on the prerequisite that the V_{fb} would not shift to beyond ±15 V so the C-V measurement after stress can be limited in a voltage range that will not alter the C-V curve furthermore. Fig. 4.10 shows the C-V curves after continuous stress. It is found that the V_{fb} shift tends to be saturated with the increase of stress time. The final V_{fb} is approximately symmetric to the original value. It is thus possible to attribute the instability at high electric field to the polarization of the SiC film.

Fig. 4.11 schematically shows the effect of polarization on the shift of C-V

curve. As the electrical field exceeds threshold strength (about 1.8MV/cm at room temperature), the SiC film becomes polarized. This polarization should be attributed to the agreement of electrical dipoles' orientation in the SiC film. The field due to these dipoles induces a charge in the silicon substrate, which is reflected by a shift in the C-V curve. As the C-V curve is measured at FVS mode, the SiC film was firstly polarized by the negative electric field and cause a positive flat-band voltage shift and vice versa.

The dielectric constant of a polarized dielectric should be increased according to the well-known polarization equation [11] :

$$P=\{[3(k-1)]/[4\pi(k+2)]\} \quad (1)$$

, where P is the volume polarization and k is the dielectric constant. As the polarity of a material becomes higher, the dielectric constant of this material should become higher, too. However, the measured capacitances at strong accumulation mode before and after electric field stress are not increased (refer to Fig. 4.7-4.10). It should be mentioned that the capacitance is measured at high frequency while the time constant for polarization at room temperature is estimated to be 5 minutes from Fig.4.10. The molecular dipoles can not follow the AC signal such that the measured capacitance and the corresponded dielectric constant does not changed after electric field stress.

To clarify this point, dielectric constant of SiC film were measured at lower frequencies and higher temperatures. The Al-SiC-1 capacitor was heated-up to the targeted temperature on a thermal chuck. The capacitor was then biased at –40 V (-4 MV/cm) for 2 minutes to polarize the SiC film before C-V measurement. The accumulated capacitance at 0V was then measured at various frequencies ranging from 1MHz to 100 HZ. The simple Al/ SiO_2 (10 nm)/Si capacitor (Al-SiO2-1) was also measured. The dielectric constant of the thermal oxide was calculated from the capacitance at accumulation mode. This value was used to correct the dielectric constant of SiC film from the capacitance of Al-SiC-1 capacitor. Fig. 4.12 shows the extracted dielectric constant as a function of frequency with temperature as parameters. The Al-SiC-1 capacitor shows temperature independent dielectric constant because thermal oxide is known as an un-polarized dielectric. The slight increase of dielectric constant with decrease of frequency should be attribute to the parasitic effect of the measurement system. The dielectric constant of Al-SiC-1 capacitor at 100℃ is identical to that at 30℃ at all frequencies. However, as the temperature is higher than 150℃, the dielectric constant increases with the decrease of frequency below 500 Hz. These results are consistent with the prior addressed equation (1) and strongly support the proposed mechanism that the observed instability at high electric field is due to dielectric polarization.

It is still interesting to know why the SiC film is polarizable. It is well known that the pure SiC is a tetrahedral molecule such that it is impossible to be polarized. However, with the additive of nitrogen in SiC film, Si-N chemical bond may be formed and no longer pure tetrahedral structure presents. The nitrogen content in the SiC film determined by RBS and ESCA analysis are 7.62% and 13%, respectively. The electron binding energies of both silicon and nitrogen atoms determined by XPS analysis are shown in Fig. 4.13(a) and (b), respectively. The Si(2p) peak is centered at 100.98 eV between the binding energies corresponding to SiC (100.6 eV) and SiN (101.8 eV), which indicates Si atoms link to both C and N atoms. The N(1s) peak centered at 397.4 eV also indicated Si-N like chemical bonds [12-13]. It is postulated that these chemical bonds distort the symmetry of the tetrahedral SiC structure and result in polarization phenomenon.

4.3.4 Carrier Injection

Although the instability at high field can be explained by dielectric polarization, the asymmetric V_{fb} shift at low and medium electric field can not be simply attributed to polarization. Since the Al-SiC-1 capacitor is not a symmetric structure, the asymmetric flat-band voltage shift may be correlated to the asymmetric structure. Thus another instability mechanism combining carrier injection and weak polarization

is proposed and is illustrated in Fig. 4.14.

As the Al-SiC-1 capacitor is biased at a low positive voltage (<10V), electrons must overcome the energy barrier between Si substrate and the 10 nm thick thermal oxide to be injected into the SiC film. At low electric field (<1 MV/cm), both of direct tunneling and F-N tunneling currents are negligible. Therefore, the small V_{fb} shift can not be explained by electron injection from substrate. It should be noted that the energy required to rotating the molecular dipole decreases with the increase of temperature. As the Al-SiC-1 capacitor is biased at low electric field but high temperature, slight polarization may occur. This may explain the small V_{fb} shift after positive electric field stress. Hole injection from gate can also result in a negative V_{fb} shift, but the possibility is low because the gate material is metal.

As the Al-SiC-1 capacitor is biased at a low negative voltage, hole injection from substrate is still suppressed by the thermal oxide but electron can be injected easily from gate into SiC film. These electrons are blocked by the thermal oxide and are accumulated in SiC film until the electric field across oxide allows these electrons to tunnel through the oxide layer. Therefore, both of the high temperature enhanced dielectric polarization and the injected and trapped charges in SiC film would cause larger flat band shift after negative electric field stress.

Because the low field instability depends on temperature as shown in Fig. 4.9,

the electron tunneling mechanism must not be F-N tunneling. To find out the exactly carrier injection mechanism for the metal/SiC system, the I-V characteristic of Al-SiC-1 capacitor was analyzed furthermore. Fig. 4.15(a) shows the current density-electric field (J-E) curve of Al-SiC-1 sample at 30℃. The breakpoint around 1.8 MV/cm may be explained by the setup of polarization induced displacement current. The breakpoint around 3 MV/cm might be explained by the turn-on of electron tunneling through thermal oxide because the internal field becomes strong enough. To verify the assumption needs more quantified analysis, which is beyond the scope of this work. Here we only focus on the carrier injection mechanism at electric field below 1 MV/cm. By fitting the J-E characteristic to all possible mechanisms, it is found that the J-E characteristic can be best fitted with the Schottky emission model. Fig. 4.15(b) shows the fitted result using Schottky emission model.

Because the A1-SIC-1 structure is asymmetric, the behavior of carrier injection is more complicated. An additional confirmation experiment was performed using Al-SiC-MIM structure. Because the Fermi energy of Al is close to that of degenerated n-type Si, the Al-SiC-MIM structure can be treated as a symmetric structure. Fig. 4.16(a) shows the J-E characteristics of the Al-SiC-MIM sample with both of gate injection and substrate injection. The two J-E curves are almost identical especially at electric field lower than 1 MV/cm as expected. The best-fitted carrier injection

mechanism is still the Schottky emission model (Fig. 4.16(b)). It is thus concluded that the dielectric instability at low electric field and high temperature is due to the combination of weak polarization and electron injection via the Schottky emission process, where the electron injection plays the major role.

4.4 Summary

In this chapter, a detail study of SiC electrical properties and instabilities were observed for the first time. It is expected that amorphous SiC deposited by CVD system is the most promising dielectric diffusion barrier to replace SiN in the Cu-interconnect structure. It can also serve as a good etch stop layer if etch stop layer is needed. The basic properties including low dielectric constant, good Cu barrier ability, and low moisture uptake are confirmed in this work and summarized in Table 4-2. By incorporating nitrogen into SiC film, the dielectric constant and leakage current can be reduced. However, the longest TDDB lifetime occurs at moderate nitrogen content. These results indicate that the SiC deposition condition must be carefully controlled to compromising material, electrical and reliability performances

Furthermore, at electric field higher than 1.8 MV/cm, independent of the polarity, charges will be built-up in the SiC film and the V_{fb} of the MIS structure will shift. The magnitude of V_{fb} shift in both positive voltage and negative voltage directions saturates to a certain extent, which depends on the electric field strength. A

dielectric polarization model was proposed to explain this high field instability. The origin of dipole is attributed to the incorporated nitrogen atoms, which distort the symmetric tetrahedral SiC molecule. The dielectric polarization is further verified by the symmetric C-V shift under both positive and negative electric field and by the increase of dielectric constant at high temperature and low measurement frequency after electric field stress.

As the stress temperature is raised, C-V shift can be observed at electric field as low as 0.4 MV/cm. If the film structure is asymmetric, Al-SiC-1 structure for example, the magnitudes of C-V shift at positive field and negative field will be quite different. A carrier injection model combined with the polarization was proposed. It is assumed that slight polarization occurs at such a low electric field because dipole is easier to be aligned at high temperature. But the dominant mechanism is electron injection from metal gate into SiC film via the Schottky emission process. The mechanism is further confirmed using a symmetric test structure of Al-SiC-MIM structure.

Although the metal pitch is scaled down rapidly, the operating voltage is reduced simultaneous. Therefore, the electric field in IMD is always less than 0.5 MV/cm under normal operation. High field polarization will not be issue under normal operation. But, electro-static discharge (ESD) events may expose the IMD to a transient high temperature and high electric field. The dielectric may be polarized by

the transient events. On the other hand, metal contacts with SiC at sidewall of damascene structure directly. The carrier injection from the sidewall contact may result in instability of underlying devices. It is thus recommended that the film properties must be improved and the stability must be carefully evaluated at real circuit level.

Except the metal mobile ions effect in dielectric discussed in Chapter-2, in this chapter we also demonstrate two other different type of mechanisms, dielectric polarization and carrier injection, that would cause dielectric electrical instability. And these two mechanisms model were shown in Fig. 4.11. Table4-4 also summaries the C-V shift behaviors of three different electrical instability mechanisms.

References

1 N. Awaya,; H. Inokawa,; E. Yamamoto; Y.Okazaki,; M. Miyake, Y. Arita, T. Kobayashi, “Evaluation of a copper metallization process and the electrical characteristics of copper-interconnected quarter-micron CMOS,” IEEE Trans. on Electron Devices, vol. 43, No. 8, pp. 1206-1212, 1996

2 J. Tao, N. W Cheung, C. Hu, ”Electromigration characteristics of copper interconnects”, IEEE Electron Device Letters, vol. 14, No.5, pp. 249-251, 1993

3 T. Lauinger,; J. Moschner,; and A.G. Aberle, “UV stability of highest-quality plasma silicon nitride passivation of silicon solar cells”, R. Photovoltaic Specialists Conference, Conference Record of the Twenty Fifth IEEE, pp.413-416, 1996

4 S.M. Hu, ”Properties of Amorphous Silicon Nitride”, Journal of Electrochemical Society, vol. 113, No. 7, pp. 693-698, 1966

5 V.Y. Doo, D.R. Nichols, and G.A. Silvey, “Preparation and Properties of Pyrolytic Silicon Nitride”, Journal of Electrochemical Society, vol. 33, pp. 1279-1281, 1966

6 The National Technology Roadmap for Semiconductors, Semiconductor Industry Association, San Jose, CA, 1999

7 P. Xu, K. Huang, A. Patel, S. Rathi, B. Tang, J. Ferguson, J. Huang and C. Ngai, “BLOK- A Low-K Dielectric Barrier/Etch Stop Film for Copper Damascene Applications”, IEEE Int. Interconnect Technology Conf., pp. 109-111, 1999

8 E. H. Snow and B. E. Deal, “Polarization Phenomena and Other Properties of Phosphosilicate Glass Films on Silicon”, Journal of Electrochemical Society, vol. 113, No. 7, pp.263-269, 1966

9 E. H. Snow and M. E. Dumesnil, “Space-Charge Polarization in Glass Films”, Journal of Applied. Physics, vol. 37, No.5, pp. 2123-2131, 1966.

10 B. E. Deal, P. J. Fleming, and P. L. Castro, “ Electrical Properties of Vapor-Deposited Silicon Nitride and Silicon Oxide Films on Silicon”, Journal of Electrochemical Society, vol. 115, No. 3, pp. 300-307, 1968.

11 J. D. Jackson, “Classical Electrodynamics”, 3rd. ed., New York: John Wiley & Sons, pp. 51-162, 1999.

12 J. L. Andujar, G. Viera, M. C. Polo, Y. Maniette, and E. Bertran, “Synthesis of nanosize Si-C-N powder in low pressure plasmas”, Vacuum, vol. 53, No. 1-2, pp. 153-156, 1999.

13 M. M. Guraya, H. Ascolani, G. Zampieri, J. I. Cisneros, J. H. dias da Silva, and M. P. Cantao, “Bond densities and electronic structure of amorphous SiN_x:H,” Physical Review B, vol. 44, No. 2, pp. 5677-5684, 1990

Table 4-1 The deposition conditions of three SiC films.

Sample	N_2O (sccm)	N_2 (sccm)	He (sccm)
SiC(1)	300	5000	0
SiC(2)	0	5000	0
SiC(3)	0	2500	2500

Table 4-2 The summarized characteristics of three different SiC films (○: good, △:medium, ㄨ: bad)

	SiC(1)	SiC(2)	SiC(3)
Dielectric constant	4.09	4.6	5.64
Moisture Immunity	ㄨ	○	○
Cu barrier property	ㄨ	○	△
Leakage current	○	△	ㄨ
TDDB reliability	△	○	ㄨ

Table 4-3 The flat-band voltage measured with various DC voltage sweep range. FVS : from accumulation mode to inversion mode. RVS : from inversion mode to accumulation mode.

Sweep range	FVS	RVS
10V~-10V	-2.06	-2.08
15V~-15V	-2.04	-2.09
18V~-18V	-1.8	-2.08
20V~-20V	-0.6	-1.76
25V~-25V	3.22	-4.32
30V~-30V	10.2	-14.72
35V~-35V	15.27	-17.43
40V~-40V	20.12	-21.24

Table 4-4 C-V shift behaviors of three different electrical instability mechanisms

Instability Mechanism	Flatband Voltage (C-V) Shift				Dielectric Constant
Mobile Ions	Asymmetric	Saturation (limited source) No-Saturation (unlimited source)	Voltage independent	History dependent	Unaltered
Carrier Injection	Symmetric (Asymmetric Structure)	Saturation (blocked) No-Saturation (unblocked)	Voltage dependent	Strong history dependent	Unaltered
Polarization	Symmetric	Saturation	Voltage dependent	History independent	Altered

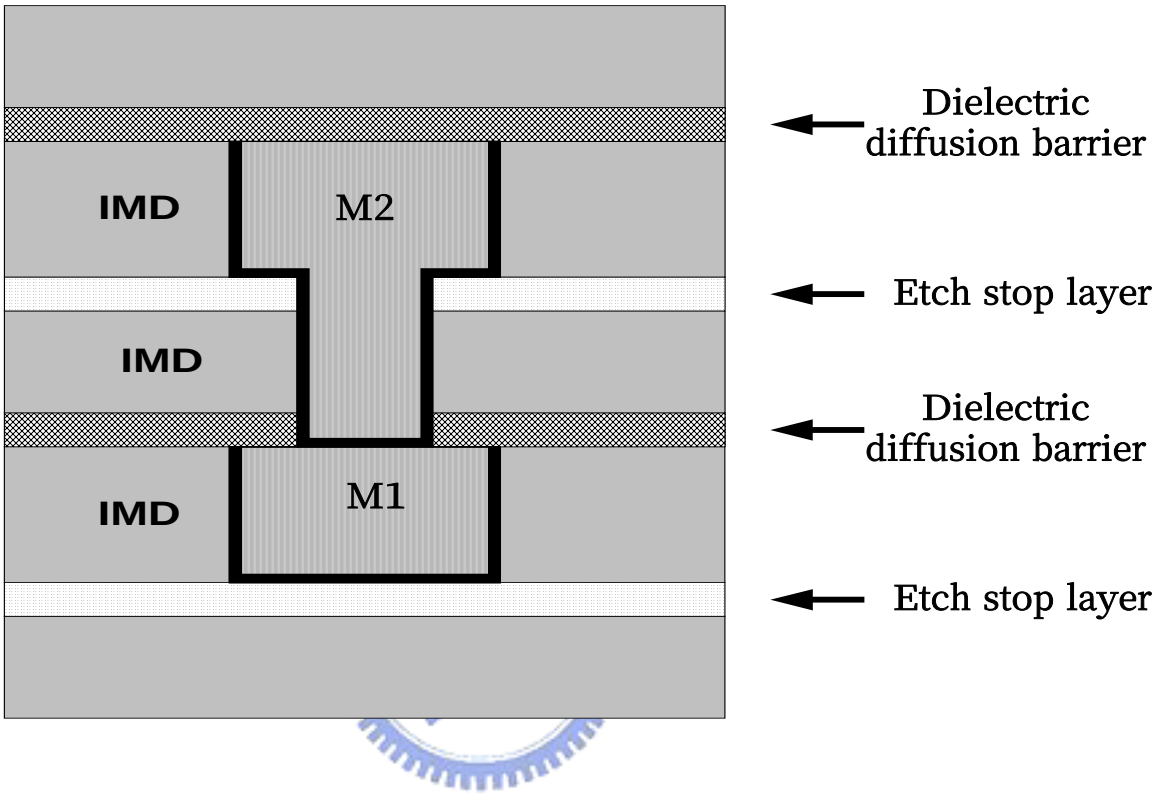


Fig. 4.1 Schematic structure of Cu-interconnect fabricated by dual-damascene process.

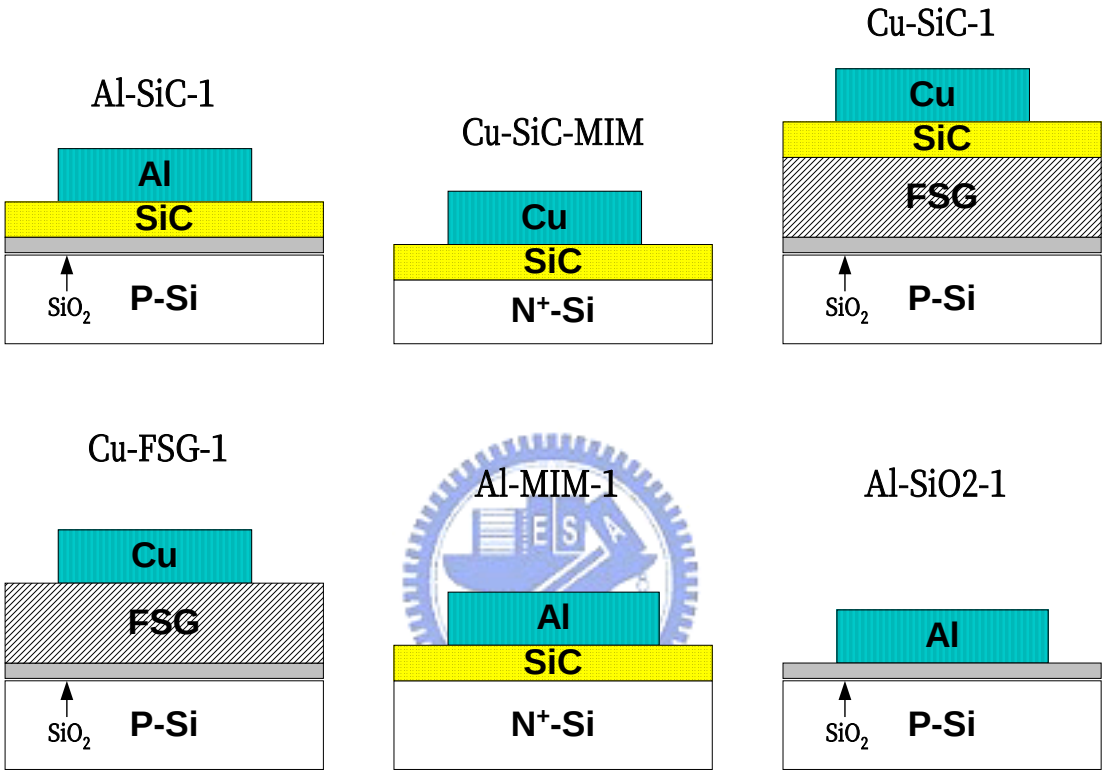


Fig. 4.2 Schematic structures of the MIS capacitors used in this work. Al-SiC-1 : Al (500 nm)/ SiC (90 nm)/ SiO_2 (10 nm)/ Si. Cu-SiC-MIM : Cu (500 nm)/ SiC (90 nm)/n+-Si. Cu-SiC-1 : Cu (500nm)/ SiC (90nm)/ FSG(750nm)/ Si. Cu-FSG-1: Cu (500nm)/ FSG(750nm)/ Si. Al-SiC-MIM : Al(500nm)/ SiC (90nm)/ n+-Si. Al-SiO2-1 : Al / SiO_2 (10 nm)/ Si

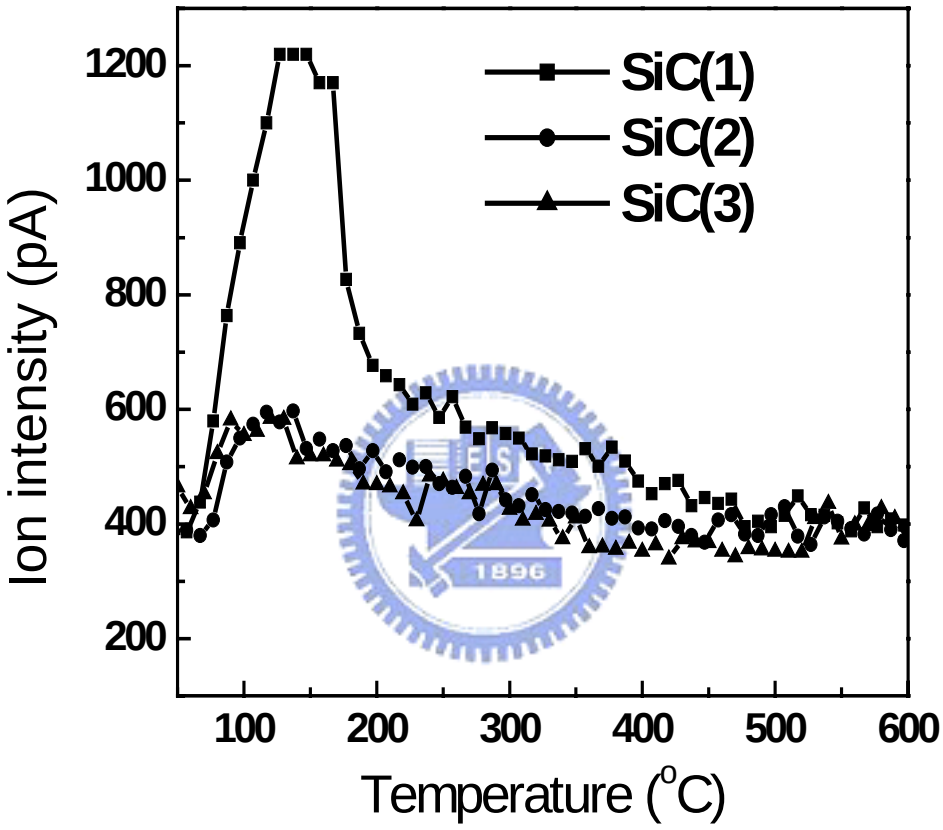


Fig. 4.3 TDS analysis of H_2O molecules of the three different SiC films stored in cleanrrom for 2 weeks

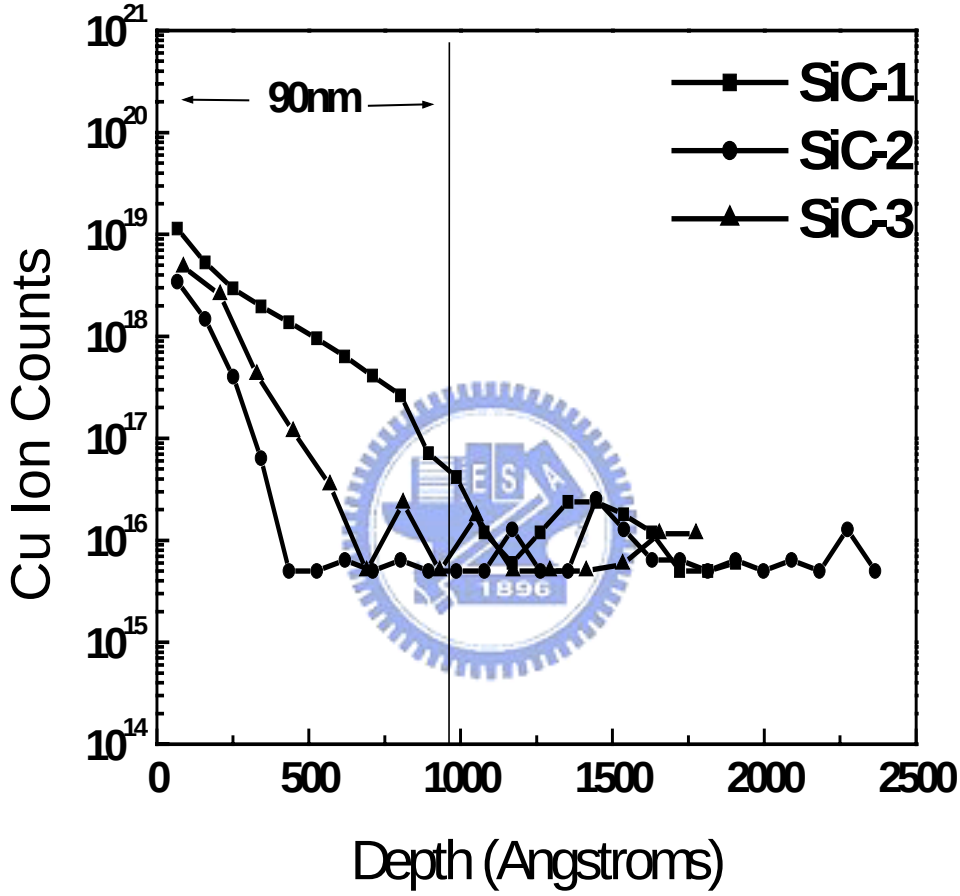


Fig. 4.4 SIMS depth profiles Cu ions in the three different SiC films after BTS at +2MV/cm and 200℃ for 500 minutes stress.

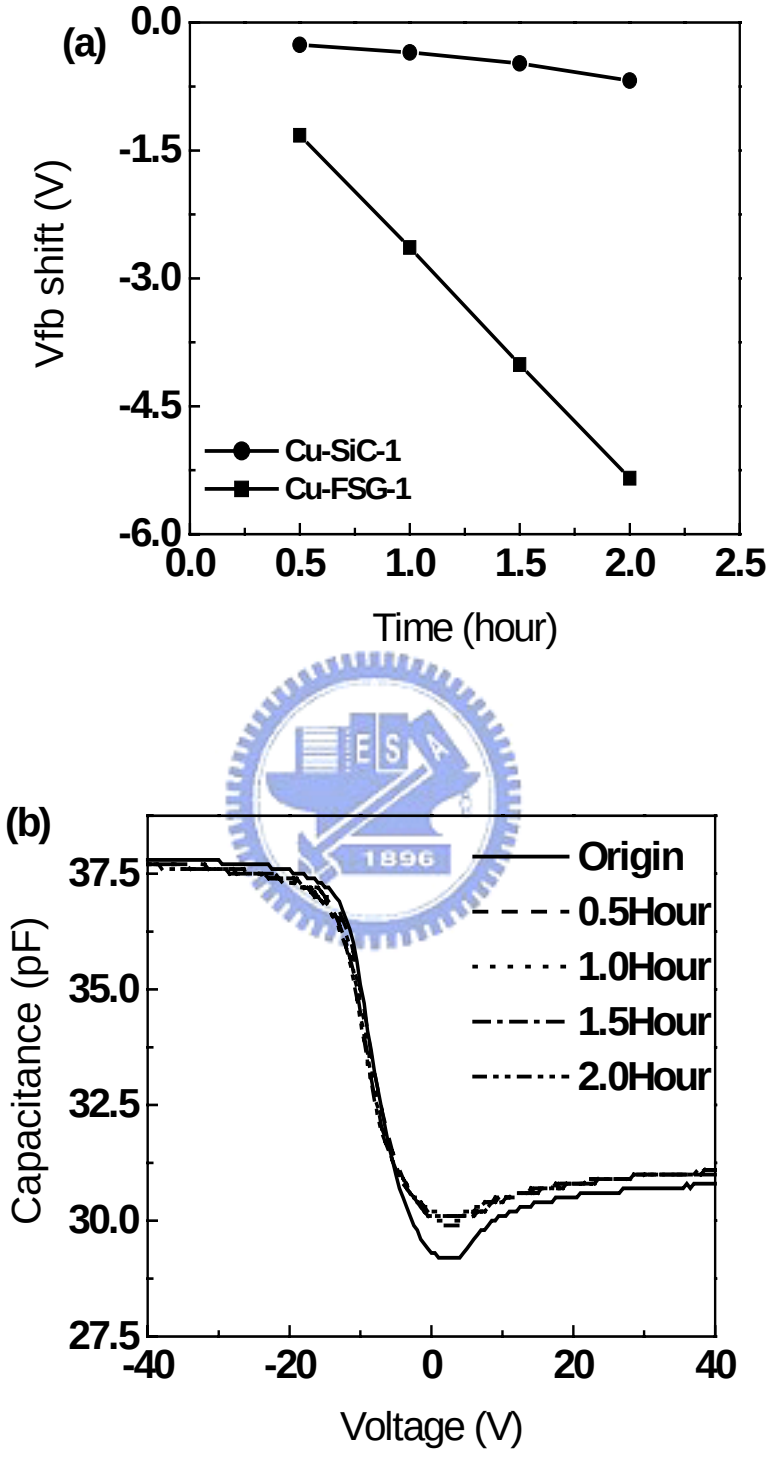


Fig. 4.5 (a)V_{fb} shift value of Cu-SiC-1 and Cu-FSG-1 capacitors after BTS (b) C-V characteristics of the Cu-MIS-1 sample after BTS for various lengths of time.

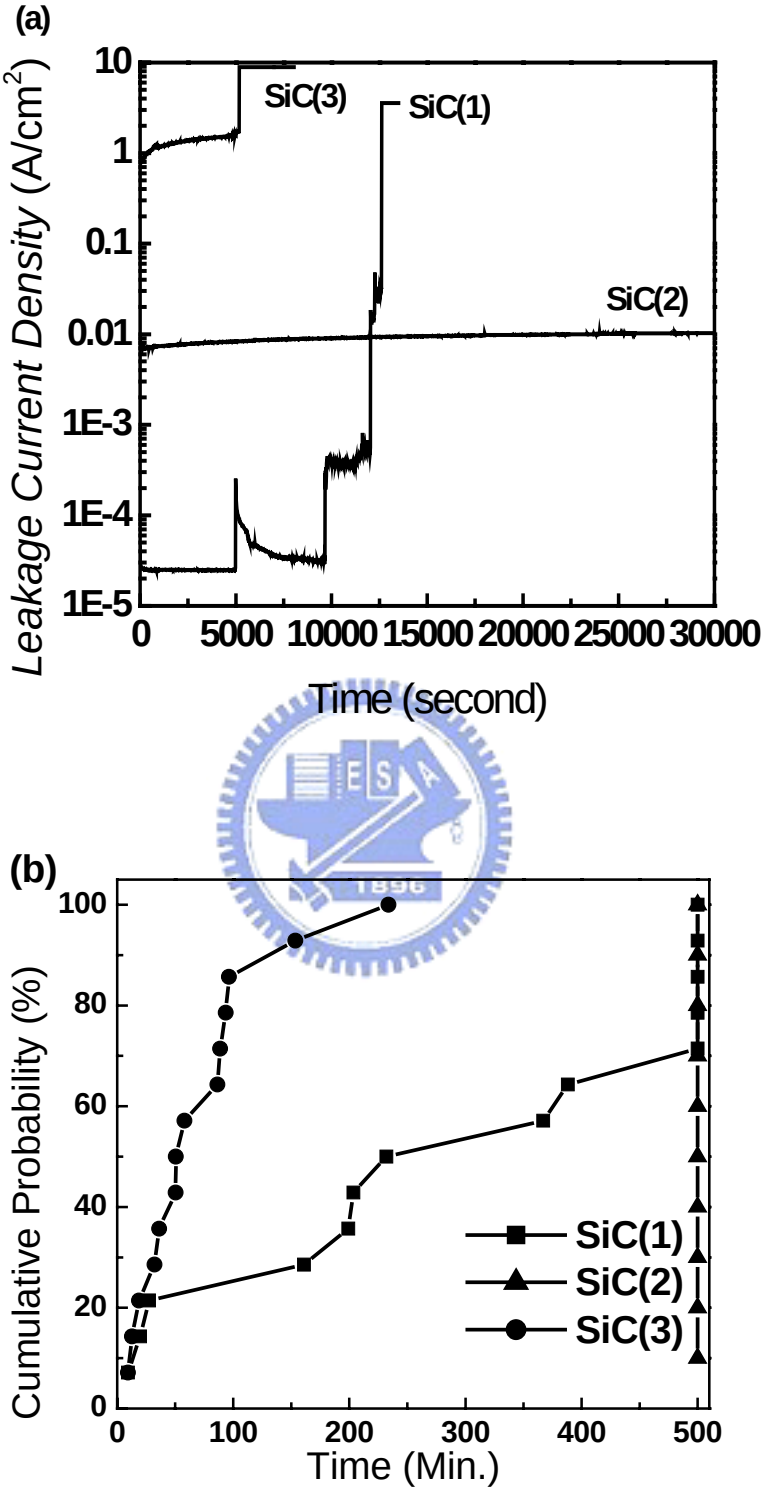


Fig. 4.6. The leakage current and breakdown phenomenon of Cu-SiC-MIM capacitors under electric field stress at (a) 2MV/cm and 150℃ (b) 3MV/cm and 200℃.

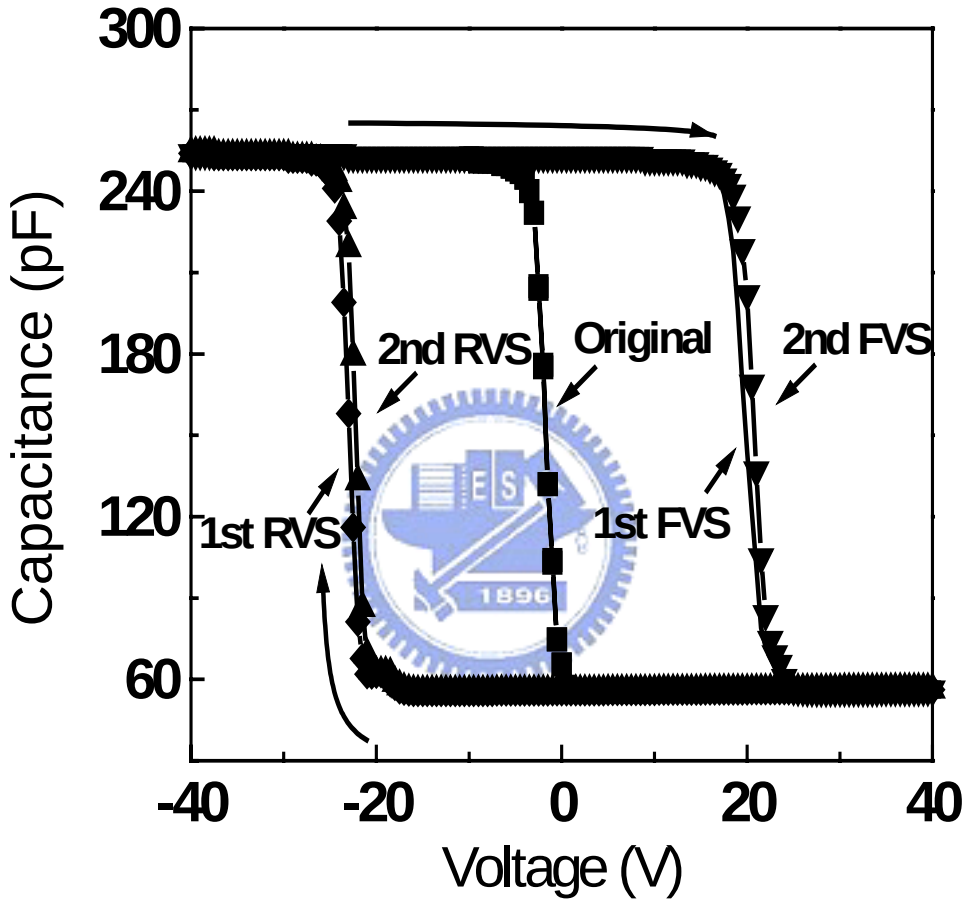
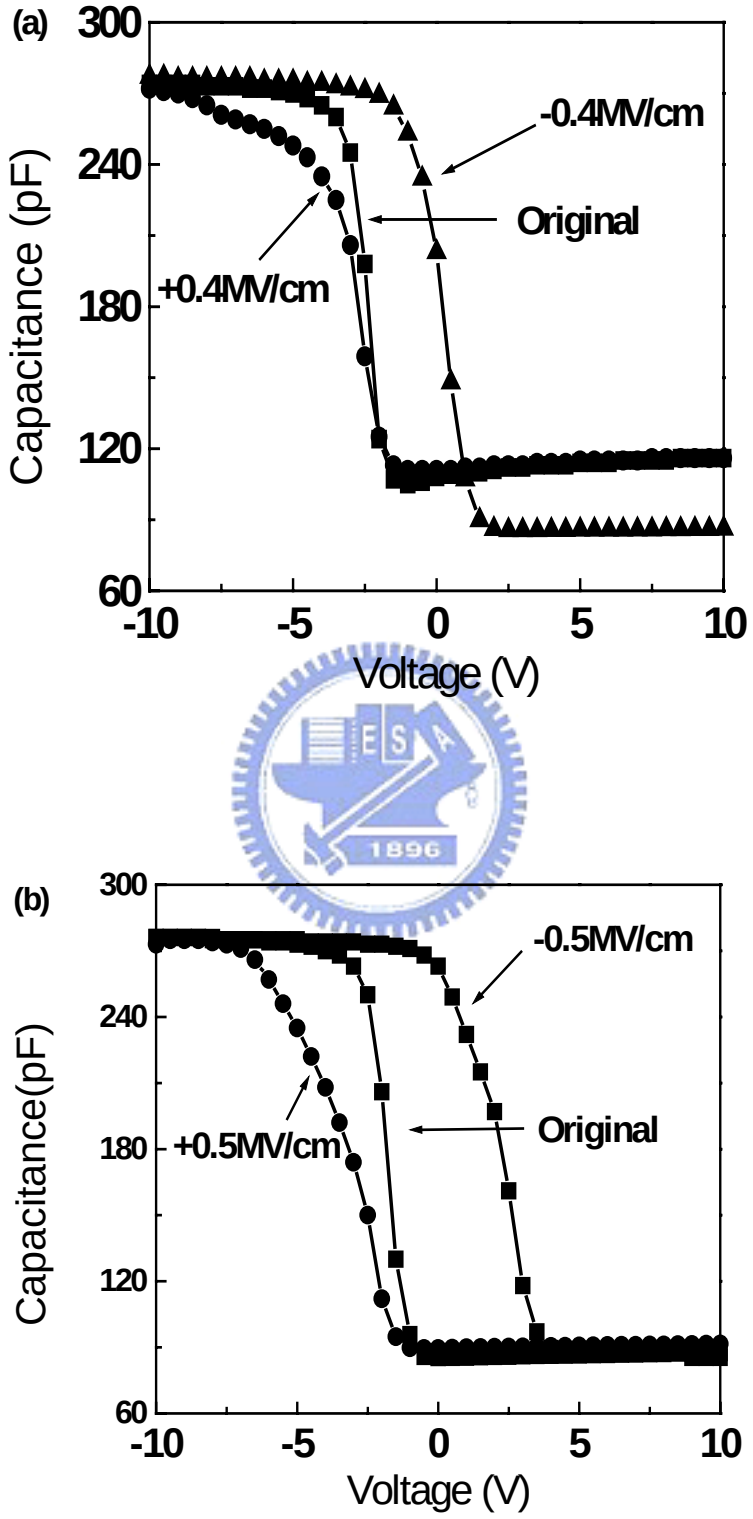


Fig. 4.7 The high frequency C-V characteristics of Al-SiC-1 sample measured in both of the FVS and RVS modes for two cycles. The voltage range is –40 to 40 V.


(a)
300
240
180
120
60
Capacitance (pF)
-0.4MV/cm
Original
+0.4MV/cm
-10
-5
0
5
10
Voltage (V)
(b)
300
240
180
120
60
Capacitance(pF)
-0.5MV/cm
Original
+0.5MV/cm
-10
-5
0
5
10
Voltage (V)

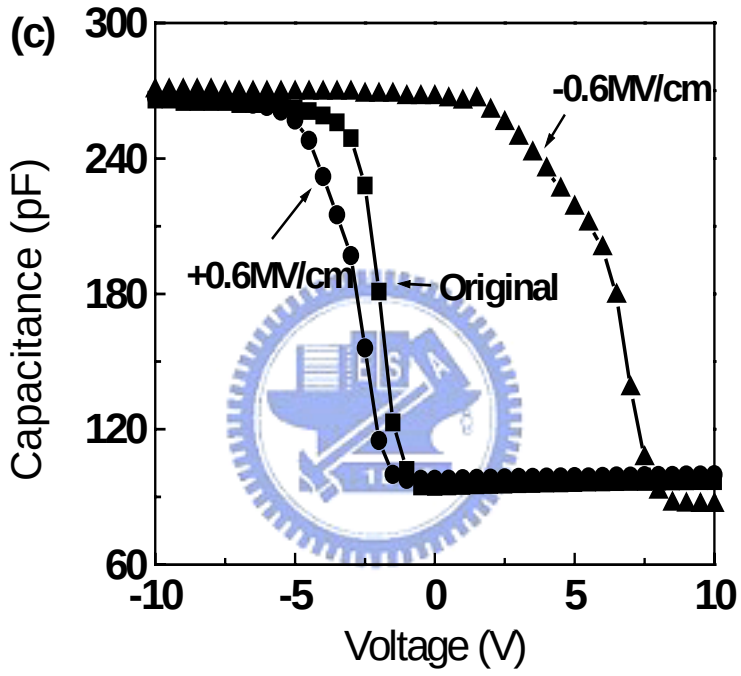


Fig. 4.8 Capacitance-voltage curves of Al-SiC-1 samples measured at room temperature after BTS at 200 ℃ for 3 hours. The electric field strengths are at (a) ±0.4; (b) ±0.5, and (c) ±0.6 MV/cm.

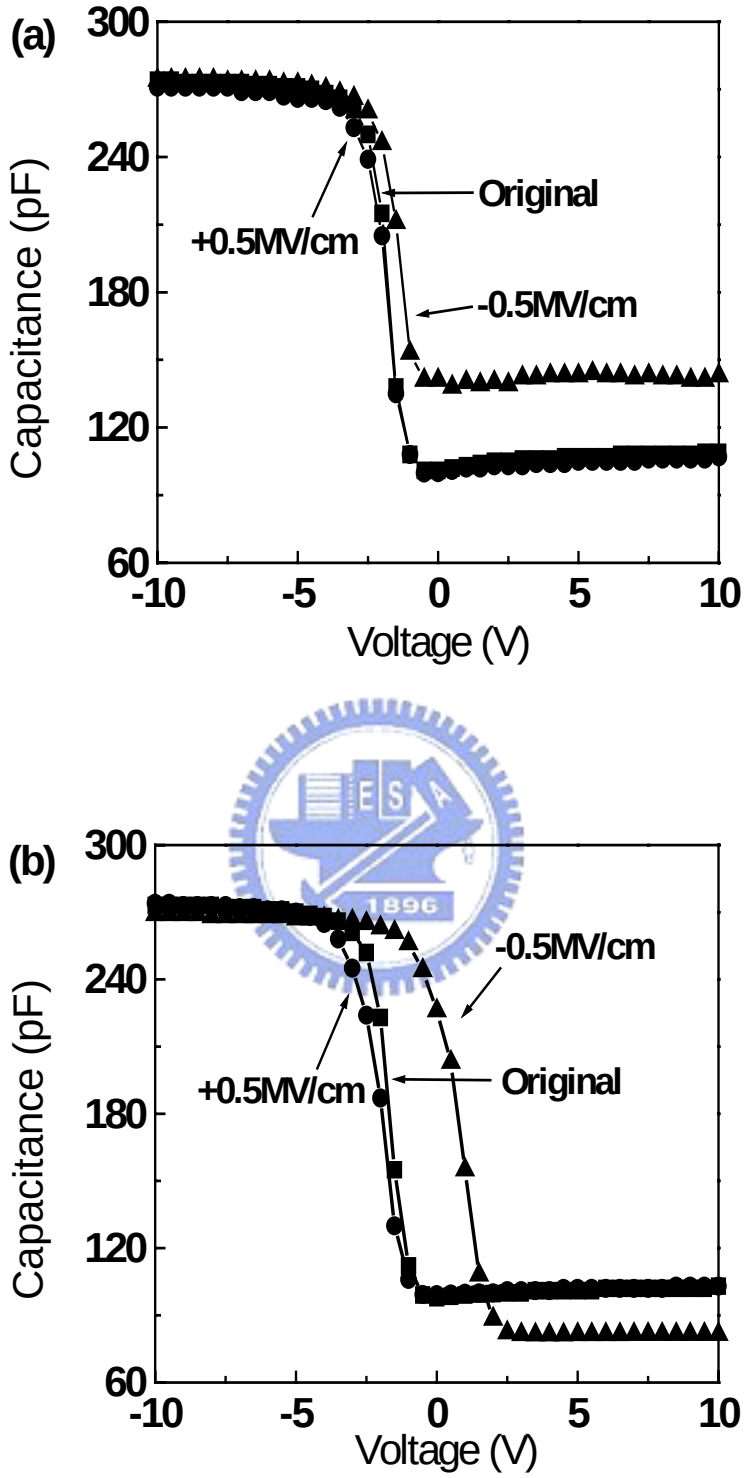


Fig. 4.9 Capacitance-voltage curves of Al-SiC-1 samples measured at room temperature after BTS at (a) 150 and (b) 175 ℃ for 3 hours. The electric field was fixed at ±0.5 MV/cm.

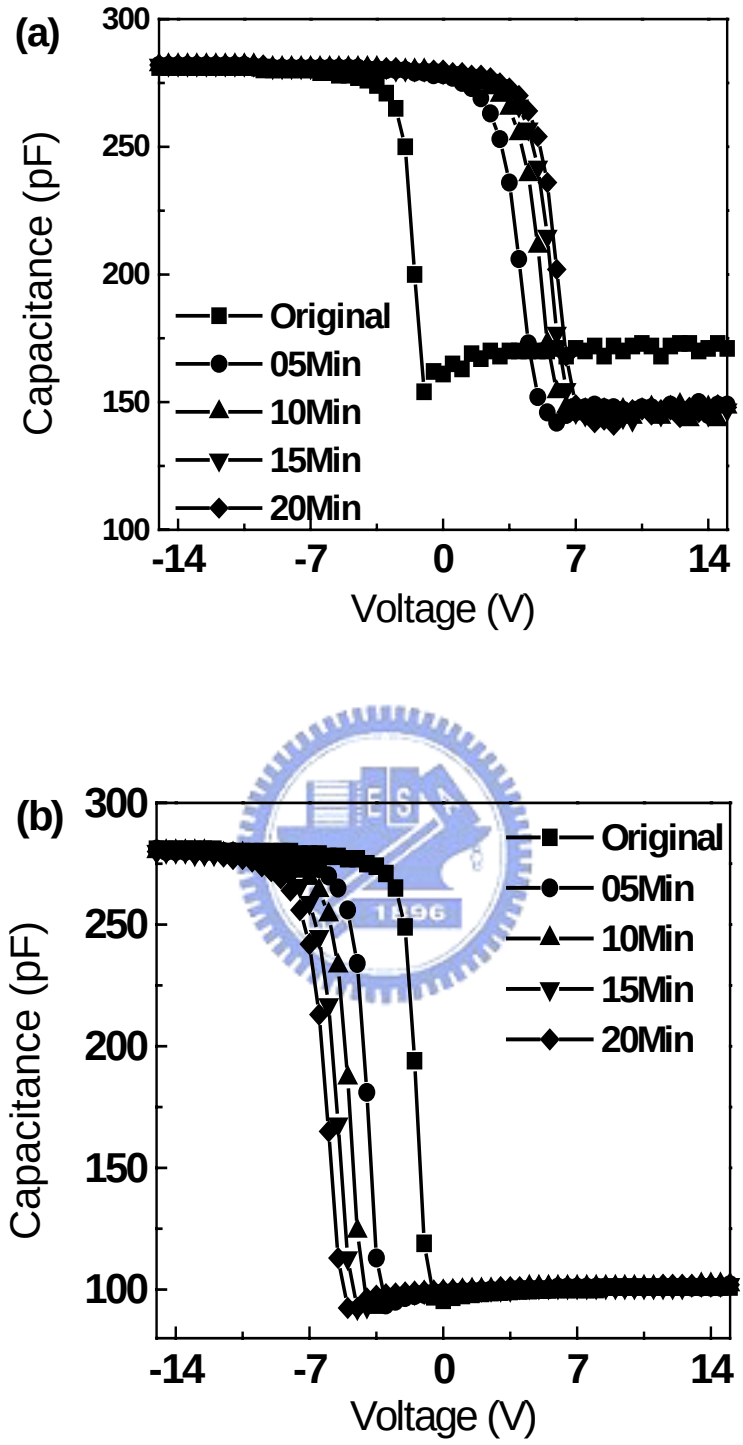


Fig. 4.10 Capacitance-voltage curves of Al-SiC-1 sample after continuous electric field stress. At (a) –20 V (-2 MV/cm) and (b) +20 V (+2 MV/cm). The temperature was fixed at 25 ℃.

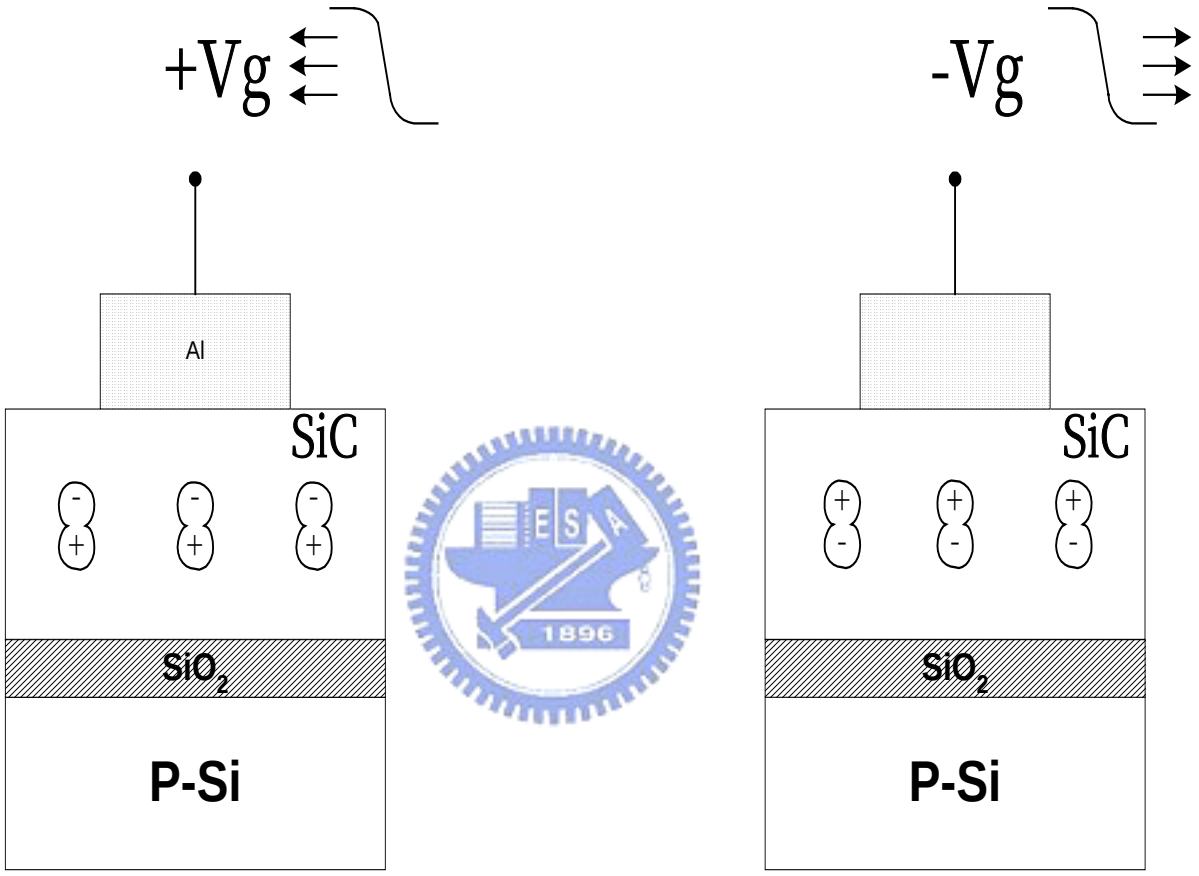


Fig. 4.11 Schematic illustration of proposed polarization model for electrical instability of SiC film at high electric field and low temperature.

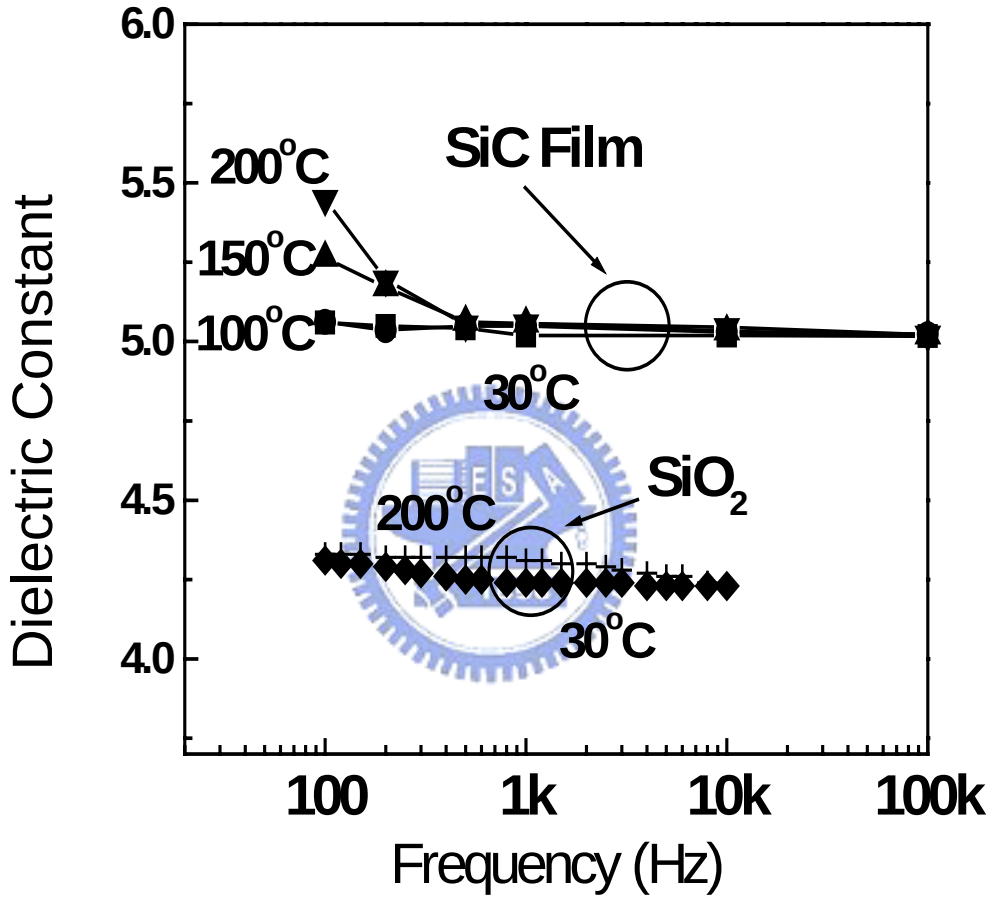


Fig. 4.12 Extracted dielectric constant of SiC film as a function of frequency with temperature as parameters. Before measurement, Al-SiC-1 samples were biased at –40 V for 2 minutes at room temperature. Results of SiO_2 measured from Al-SiO2-1 sample are also shown in the figure.

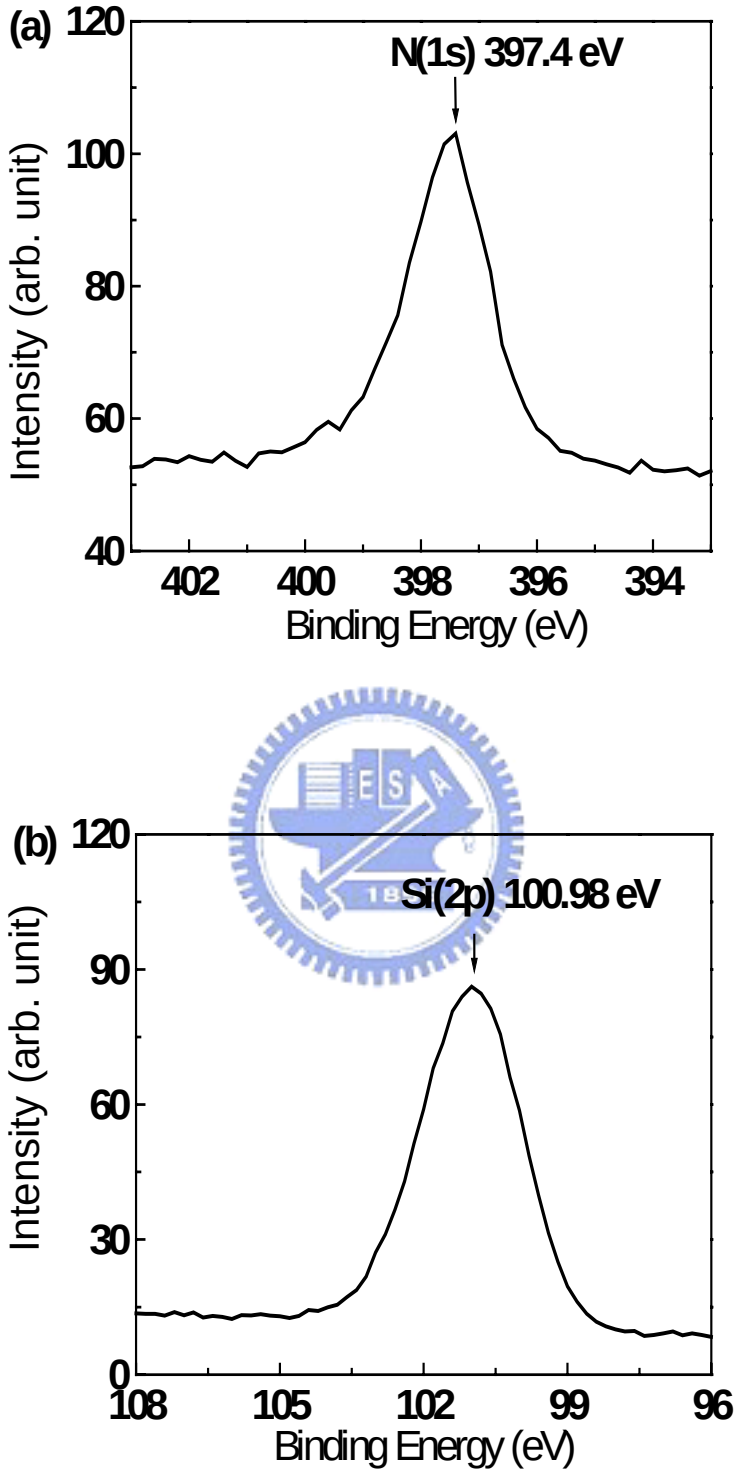


Fig. 4.13 XPS spectrum of SiC film shows (a) Si(2p) and (b) N(1s) electron binding energy.

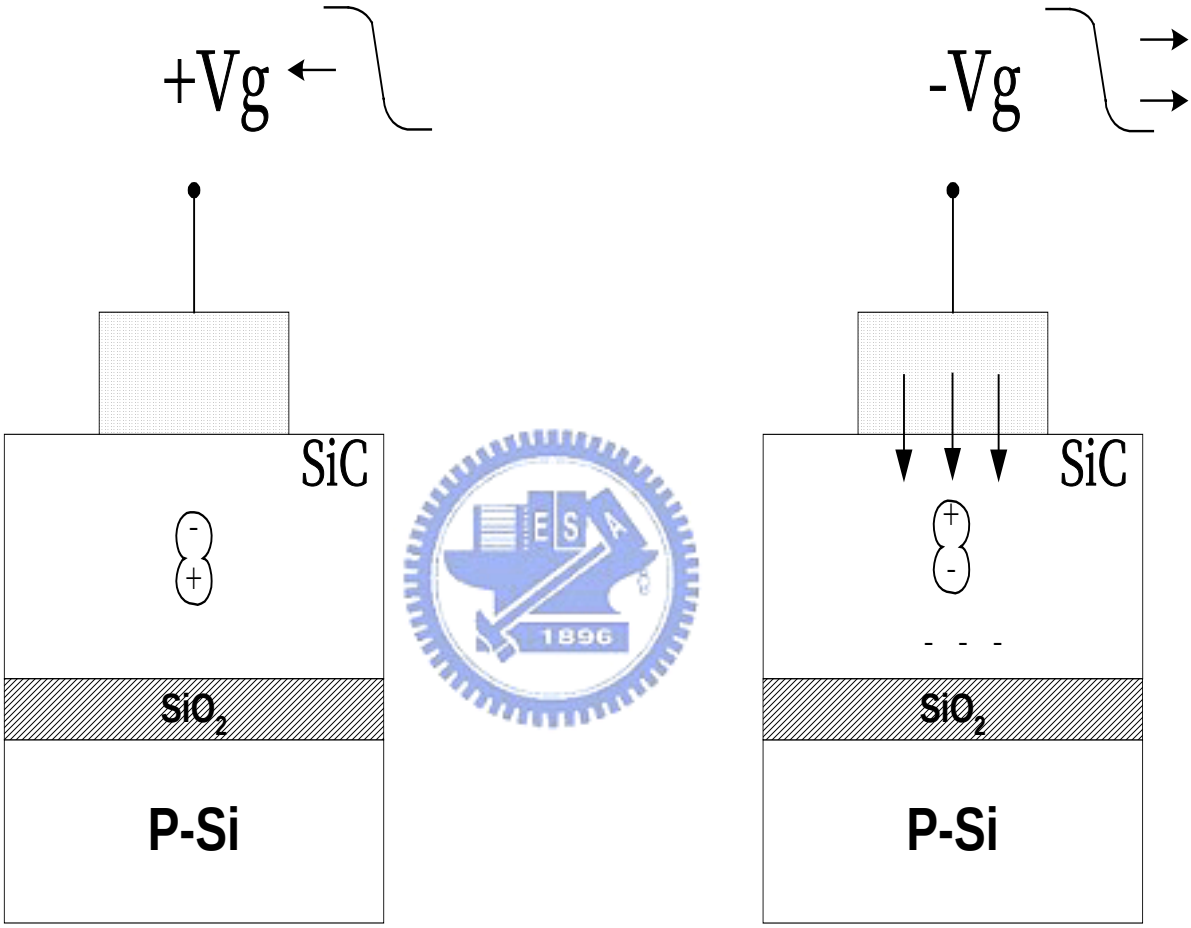


Fig. 4.14 Schematic illustration of proposed instability mechanism combining carrier injection and weak polarization to explain electrical instability at low electric field but high temperature.

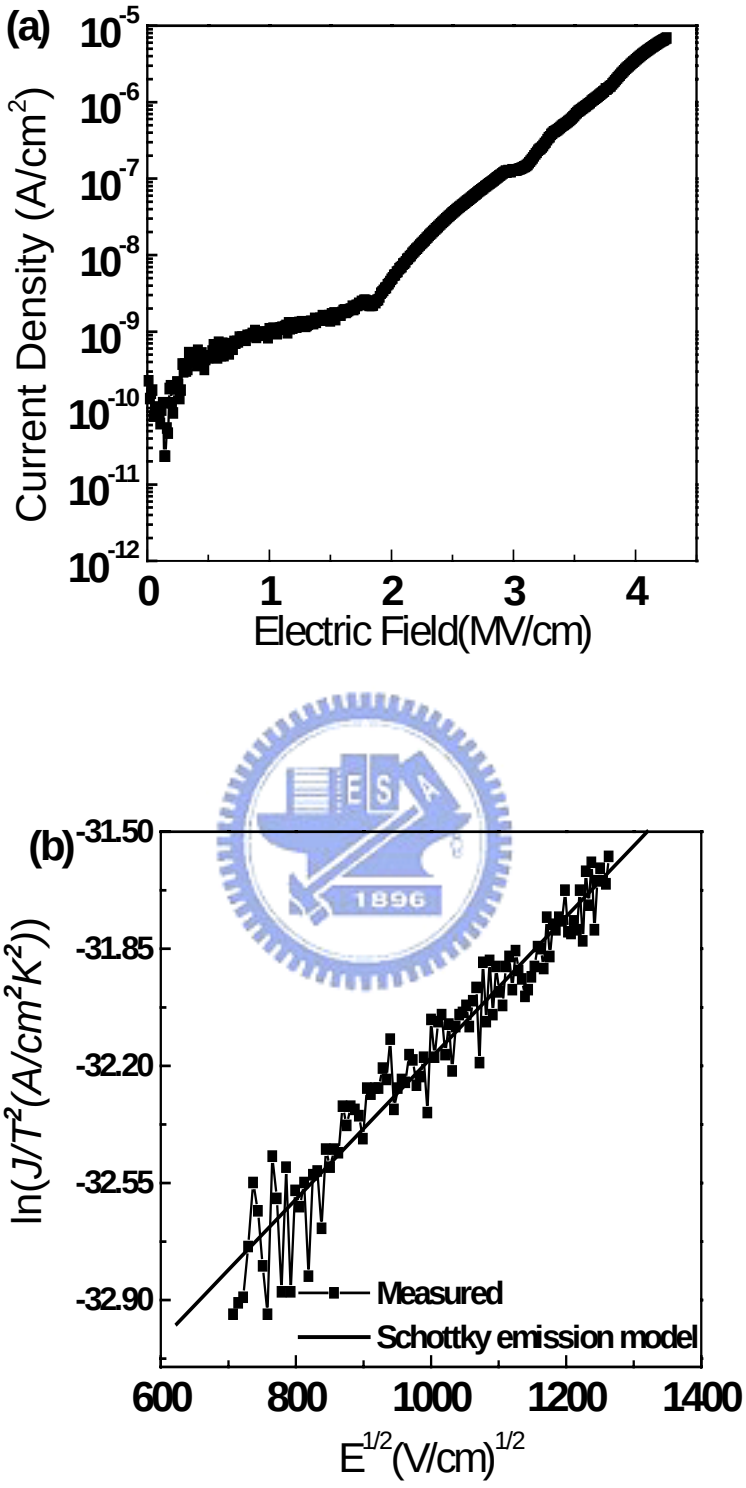


Fig. 4.15 (a) Current density-electric field (J-E) curve of Al-SiC-1 sample at 30℃. (b) The measured J-E curve at low electric field (<1 MV/cm) can be well fitted by Schottky emission model.

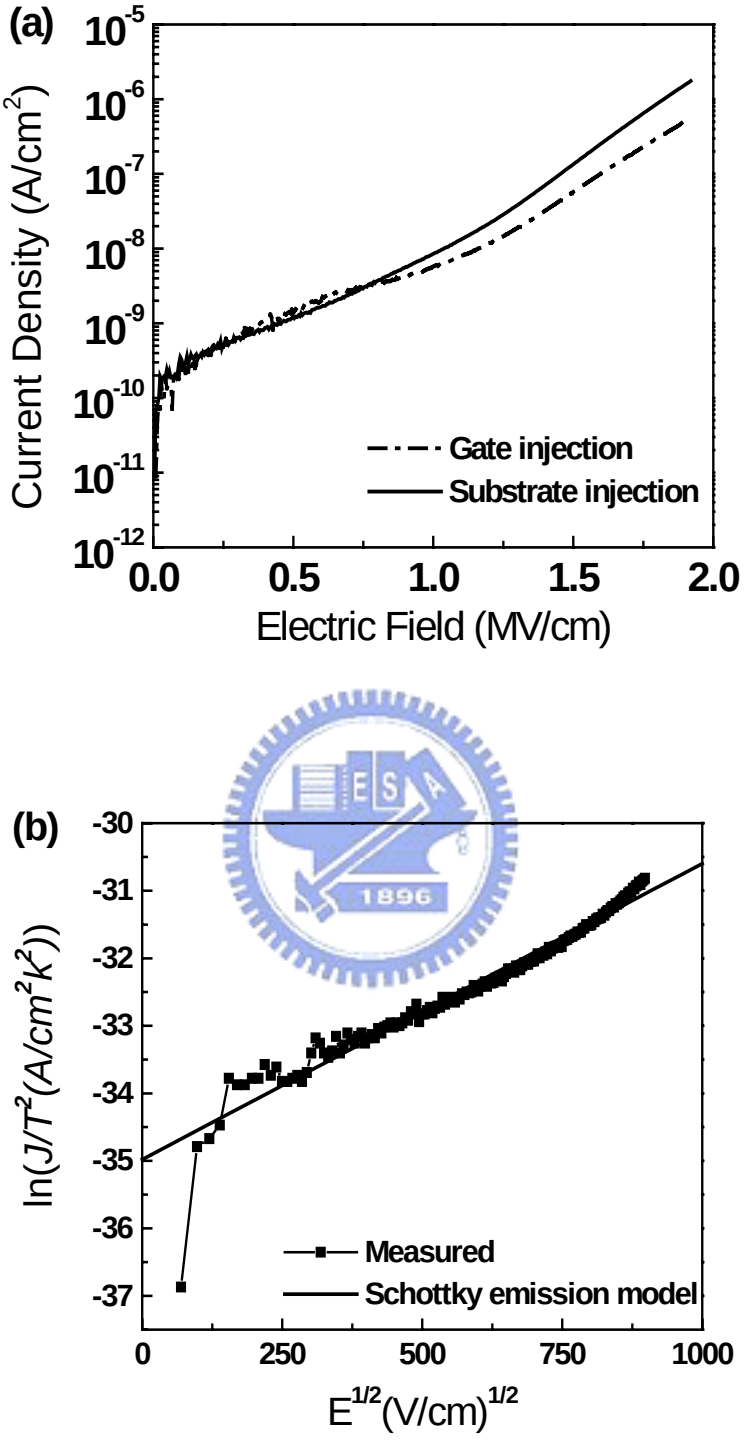


Fig. 4.16 (a) Current density-electric field (J-E) curve of Al-SiC-MIM sample at 30℃. (b) Because of the quasi-symmetric sample structure, the measured J-E curve at all electric field range can be well fitted by Schottky emission model.

Chapter 5

A Novel Wafer Reclaim Method for Silicon Carbide Film and Carbon Doped Oxide Low Dielectric Constant Films

5.1 Introduction

According to the results presented in chapter 4, it is expected that amorphous SiC (a-SiC) film deposited by chemical vapor deposition method will replace SiN in the Cu dual-damascene structure as a Cu dielectric diffusion barrier and/or etching-stop layer in order to further reduce circuit delay and thus improve circuit performance [1-2]. The a-SiC film is chemically inert and hard to etch by wet processing. These properties are benefits from the process point of view. However, they become adverse effects from the wafer reclaim point of view. On the other hand, lots of low-k materials are developed every year. We have demonstrated in chapter 3 that carbon doped oxide (CDO) and porous carbon doped oxide are very promising low-k materials for different generations Cu interconnect applications [3-8].

In the back-end-of-line (BEOL) process, fabrication parameters such as film thickness, thickness uniformity, film composition, particle counts, etc. must be

carefully and precisely controlled. Therefore, lots of monitor wafers must be used to optimize the film deposition condition during process development and to monitor the process stability during mass-production daily. Wafers deposited with a-SiC or low-k films must be reclaimed to reduce wafer cost. Unfortunately, there is no universal chemical solution that can etch a-SiC film and various low-k films. Wafer polish becomes the only method to reclaim these wafers, but the cost of wafer polish is high. Furthermore, the over polish of Si substrate limits the reclaim times.

In this chapter we report the phenomenon and kinetics of thermal oxidation of a-SiC film and CDO thin films at medium high temperatures for the first time. And then a universal wafer recycling method, thermal oxidation followed by HF etching, is proposed for stripping a-SiC and CDO films.

5.2 Experimental Details

Blanket wafers deposited with thin dielectric films were used in this study. The substrate material is (100)-oriented 8-inches Si wafer. Amorphous SiC film of thickness between 50nm and 100nm was deposited on Si wafer in a plasma-enhanced chemical vapor deposition system with organosilicon as precursor. Two kinds of a-SiC:N films with various nitrogen contents were prepared to check the effect of nitrogen on the oxidation rate. The SiC:N(5%) sample was deposited with N_2 as carrier gas 5000sccm, and the SiC:N(9.3%) sample was deposited with N_2 flow rate

2500sccm and He flow rate 2500sccm. Both dry O_2 oxidation and steam oxidation were performed in a simple furnace system at medium temperatures ranging from 550 ℃ to 950℃. To examine the efficiency of reclaiming a-SiC film deposited wafer by the oxidation method, some wafers were oxidized in a vertical furnace with H_2 flow rate of 4 SLM and O_2 flow rate of 4 SLM. The particles in this furnace are well controlled to mass-production level. Furthermore, plasma oxidation of a-SiC film was also evaluated at the conditions of O_2 flow rate 900 sccm, RF power 300W, and substrate temperature 250℃. Finally, two kinds of CDO films with k-value of 2.6 and 2.2 were prepared to evaluate if the oxidation method can be adapted to general CDO films.

The thickness of dielectric layer was measured with a spectrophotometer of model N&K analyzer 1200. Thermal Desorption Spectroscopy (TDS) was use to analyze the thermal stability of a-SiC film. Auger Electron Spectroscopy (AES) and Fourier-Transformed Infra-Red (FTIR) spectroscopy were used to analyze the chemical composition and chemical bonding of the oxidized a-SiC film. Surface roughness after stripping the oxidized layer was monitored with an Atomic Force Microscope (AFM). The particle counts of post etched and cleaned wafer surface were measured with a surface scan system of model KLA-Tencor SP1.

5.3 Oxidants Transport and Oxidation Phenomena of SiC and Low-k films

5.3.1 Oxidation Phenomenon of SiC

Being a dielectric barrier, SiC shows as good thermal stability in N_2 ambient as Si_3N_4 does. Fig. 5.1 shows that the TDS analysis on the a-SiC film in N_2 ambient up to 800℃ doesn't detect any desorbed contents. Even after being annealed at 950℃ in N_2 ambient for one hour, the thickness shrinkage is only 1 nm, i.e. less than 2%. However, unlike Si_3N_4, the a-SiC film does not dissolve in HF solution or boiling H_3PO_4. Adding oxidants such as H_2O_2, H_2SO_4, or $HOCl_4$ does not help. Up till now, there is no proper chemical solutions can be used to remove a-SiC film from monitoring wafers at production line. Therefore, physical polishing is the only solution to stripping a-SiC film. But the number of times the film can be reclaimed is limited due to the unavoidable over-polishing which depletes the Si substrate. Fortunately, it is observed that although it is hard to oxidize crystalline SiC at temperatures lower than 1100℃ [9-11], the a-SiC film can be oxidized at much lower temperatures in oxygen contained ambient.

Fig. 5.2 shows the AES depth profile of a partial oxidized a-SiC film, where the original SiC film thickness is 94nm. The oxidation is performed in dry O_2 ambient at 850℃ for 60 minutes. High purity SiO_2 layer is formed and clear SiO_2/SiC interface

is observed. These results indicate that the a-SiC film is oxidized to SiO_2 from the top surface uniformly. Fig. 5.3 exhibits the FTIR spectrum of a fully oxidize a-SiC film. Before oxidation, only Si-C peaks can be detected. After steam oxidation at 950℃ for 1 hour, Si-C peaks disappear and strong Si-O peaks occur [12]. Amorphous SiC film is not as dense as crystalline SiC film and the density is about 1.5 g/cm^3 [13]. Knowing that the density of the SiO_2 film is 2.2 g/cm^3, the volume transformation ratio from a-SiC to SiO_2 can be calculated to be around 1 to 1. This ratio is very close to the experimental observation in Fig. 5.2 that the total dielectric thickness of the partially oxidized SiC/SiO_2 stack is closely equal to the original SiC thickness by N&K analyzer measurement

5.3.2 Oxidation Kinetics

Both dry oxidation and steam oxidation can convert a-SiC to SiO_2. Equations (1) and (2) express the possible reaction formula of a-SiC with O_2 and H_2O. Most of the carbon in SiC film reacts with oxygen to form CO_2 and diffuses into ambient. The oxidation model for a-SiC follows the Deal-Grove analysis on the oxidation of Si [14-16]. The Deal-Grove model assumes that oxidation proceeds in three steps: (a) the oxidants are absorbed into the outer surface where they react or remain absorbed, (b) the oxidants are transported through grown oxide film toward the SiO_2/SiC interface,

and (c) the oxidants react at the SiC surface to form a new layer of SiO_2.

$$SiC + 2O_2 \rightarrow SiO_2 + CO_2 \quad (5.1)$$

$$SiC + 2H_2O \rightarrow SiO_2 + CO_2 + 4H_2 \quad (5.2)$$

Fig. 5.4(a) and 5.4(b) show the grown oxide thickness on a-SiC film in dry O_2 ambient and steam ambient, respectively, at various temperatures. It's obvious that, similar to the case of Si, the oxidation rate of a-SiC film in steam ambient is much faster than that in dry O_2 ambient. According to the Deal-Grove model, the correlation between grown oxide thickness and oxidation time can be expressed as $X_0^2 + AX_0 \rightarrow Bt$, where X_O represents grown oxide thickness and t represents oxidation time. The coefficient B is the parabolic rate constant of a-SiC oxidation while the ratio B/A is the linear rate constant of a-SiC oxidation.

By plotting X_O versus t/X_O, the coefficients of A and B can be extracted as shown in Fig. 5.5(a) and (b), respectively. Table 5-1 and Table 5-2 summarize the rate constants in dry O_2 ambient and steam ambient. The temperature dependence of parabolic rate constant is plotted in Fig. 5.6. The activation energy (E_a) of the parabolic rate constant is 0.72eV in dry O_2 ambient and 0.53eV in steam ambient. The E_a value of the parabolic rate constant of Si oxidation is about 1.1eV in dry O_2 ambient and 0.7eV in steam ambient [13]. By comparison, both E_a values of a-SiC oxidation are smaller than those of Si oxidation, but the trend that E_a is higher in dry

ambient than in steam ambient is consistent. It is known that the parabolic rate constant is related to the diffusion of oxidants in grown SiO_2. The low E_a of a-SiC oxidation might result from the fact that the SiO_2 grew on a-SiC at medium temperature is not as dense as one that grew on Si because the residual carbon content. It should be noted that the refractive index of the SiO_2 grown on SiC is about 1.45, which is slightly smaller than the refractive index of the SiO_2 that grown on Si.

A-SiC film's properties such as adhesion, thermal stress, barrier ability, and etch rate change with added nitrogen atoms [2, 17, 18]. To show that, two kinds of a-SiC:N films with various nitrogen contents were oxidized in steam ambient at 950℃ for 1 hour. In the case of the SiC:N(5%) sample, 80.3nm thick SiC was consumed while in the case of the SiC:N(9.3%) sample, only 43.6nm SiC:N was consumed. This result means higher nitrogen content results in higher oxidation resistance. It is postulated that a Si-N bond was formed in the a-SiC:N film, and the oxidation rate was reduced due to the stronger Si-N bond (470 KJ/mole) in comparison with the Si-C bond (450 KJ/mole)[19]. Although, a-SiC and a-SiC:N could be oxidized easily at medium temperature or high temperature, for the purpose of wafer reclaim, it is not preferable to over-oxidize the silicon substrate. Fortunately, it is well known that Si oxidizes very slow at temperatures lower than 800℃. Thus, it is expected that the oxidation process will almost self-stop when a-SiC or a-SiC:N film is consumed. Fig. 5.7 shows

the grown oxide thickness of a 54nm a-SiC on Si substrate at 600℃. As the a-SiC film was oxidized completely, the oxide thickness increased minimally because the oxidation rate of Si at 600℃ is very low no matter whether it is in dry O_2 ambient or steam ambient. This result proves that a-SiC oxidation at medium high temperature is a self-stop process.

Fig. 5.8(a), (b), and (c) show the surface images of the as-deposited a-SiC surface, the partially oxidized surface, and the fully oxidized a-SiC deposited wafer after removing the SiO_2 layer, respectively. The oxidation is performed in dry O_2 ambient at 800℃. For the partially oxidized wafer (Fig. 5.8(b)), the post-etched surface is relatively rough with root-mean-square (RMS) roughness of 1.27nm. The column-like morphology comes from the non-uniformity of the as-deposited a-SiC surface as shown in Fig. 5.8(a). Meanwhile, the fully oxidized wafer (Fig. 5.8(c)) shows very smooth Si surface with RMS roughness of 0.23nm, which is similar to the background noise level. These results imply that Si does not oxidize as easily as SiC does in lower temperature. All of these results indicate the SiC oxidation is clean and self-stopping.

5.3.3 Examples of Oxidation Application

The most direct application of the a-SiC oxidation is wafer reclaim. To

demonstrate the efficiency of wafer reclaim, four 200mm wafers capped with a 70nm-thick a-SiC film were oxidized in a vertical furnace system of model ASM advance 400 with H_2 flow rate of 4 SLM and O_2 flow rate of 4 SLM at 950℃ for 2 hours. Bare Si wafer was processed simultaneously as control. Table 5-3 lists the grown oxide thickness. Because of the high temperature and the long oxidation time, an a-SiC film was consumed at very early stage and then the Si substrate was also oxidized. The thick SiO_2 layers on the a-SiC deposited wafers compare to the SiO_2 layer on Si reference wafer confirms that the oxidation rate of a-SiC is faster than that of Si. The small thickness deviation (1-2%) indicates that the a-SiC was oxidized uniformly. In this experiment, only the 5 wafers we mentined were processed in the oxidation furnace and the other slots were not filled with dummy wafers. The Si control wafer is the first wafer so that the uniformity is the poorest among the 5. Particle counts after removing the SiO_2 layer in diluted HF followed by standard RCA-clean process are summarized in Table 5-4. The particle counts of all four a-SiC deposited wafers are close to, or lower than that of the Si reference wafer. These results prove that the oxidation followed by HF etching is an efficiency technique to reclaim the a-SiC deposited wafers.

In view of the a-SiC oxidation results, we presumed that CDO films could be oxidized in the same manner. Wafers with 360nm-thick CDO (K=2.6) or 180nm-thick

porous-CDO (K=2.2) were oxidized in dry O_2 ambient at 950℃ for 1 hour followed by diluted HF etching and standard clean. No CDO or porous-CDO films were left on the Si wafer. It should be mentioned that CDO films not only oxidized but also suffered thickness shrinkage due to thermal decomposition under such a thermal process [8, 12]. It is hard to describe the oxidation processes with the Deal-Grove model. However, since CDO films are more thermally unstable than a-SiC films, similar oxidation followed by oxide etching technique can be used as well to reclaim the CDO film deposited wafers. Fig.5.9(a) and (b) displays the schematic layout of SiC and CDO low-k reclaim equipment with combined vertical furnace and wet chemical bench tank and the final prototype equipment, respectively.

Except thermal oxidation, we also observed that a-SiC film could be oxidized in O_2 plasma environment. An approximately 10 nm-thick a-SiC layer is converted to SiO_2 after a 2-hours O_2 plasma treatment at room temperature. The oxidation of a-SiC and CDO films provides an obvious answer to the question arising from an observation reported in previous literature [20], i.e. why would there be a new layer formed at outer CDO surface after O_2 plasma treatment? This new layer should be SiO_2 and it should be carefully controlled in Cu damascene process because a photoresist removal process is commonly incorporated with O_2 plasma ashing. During the O_2 plasma process the dielectric properties and surface layers of a-SiC and CDO

films would change [21]. The existence of the SiO_2 layer will increase the effective dielectric constant of the inter-metal dielectric.

5.4 Summary

This chapter is the first time to report that a-SiC film can be oxidized to SiO_2 at medium temperature. The oxidation process can be described with the Deal-Grove model. Our experiments prove that the oxidation process is clean and uniform. This property allows for a simple method to reclaim a-SiC film deposited wafers. It is also observed that CDO films can be oxidized easily as well. Therefore, oxidation followed by HF etching could be a universal process to reclaim wafers with either a-SiC or CDO films. Since the oxidation rate of Si substrate at medium temperature is much lower than that of the a-SiC and CDO films, the oxidation process is almost a self-stopped process. Compared to the traditional reclaim method for wafer polishing, this universal oxidation-etching method provides great benefits of low cost, high throughput, and almost unlimited times of reclaiming.

The easy oxidation of a-SiC film also opens up opportunity for SiC to be used for another purpose. For example, it can be used as a hardmask of high etch rate selectivity to an underlayer of SiO_2 or poly-Si. In this application, it can be 1:1 converted to SiO_2 to reduce parasitic capacitance at temperatures lower than 550℃ to

prevent the underlayer from being oxidized.

Finally, because of the easy oxidation property, O_2 plasma treatment such as photoresist stripping processes must be carefully controlled to minimize the dielectric degradation or the surface change of a-SiC and CDO films. These changes may affect the integration of Cu/low-k integration and the designed circuit performance.

References

1 P. Xu; K. Huang; A. Patel, S.Rathi, B. Tang, J. Ferguson, J. Huang, C. Ngai, and M. Loboda, “BLOKTM-a low-k dielectric barrier/etch stop film for copper damascene applications”, IEEE Int. Interconnect Technology Conf., pp. 109-112, 1999.

2 B. Y. Tsui, K, L. Fang, and S. D. Lee,”Electrical Instability of Low Dielectric Constant Diffusion Barrier Film (a-SiC:H) for Copper Interconnect”, IEEE Transactions of Electron Devices, vol. 48, No.10, pp. 2375-2383, 2001,

3 M. Tada, Y. Harada, K. Hijioka, H. Ohtake, T. Takeuchi, S. Saito, T. Onodera, M. Hiroi, N. Furutake, and Y. Hayashi, ”Cu dual damascene interconnects in porous organosilica film with organic hard-mask and etch-stop layers for 70 nm-node ULSIs”, IEEE Int. Interconnect Technology Conf., pp. 12-14, 2002

4 J. C. Lin, R. Augur, S. L. Shue, C. H. Yu, M. S. Liang, A. Vijayendran, T. Suwwan de Felipe, and M. Danek, “CVD barriers for Cu with nanoporous ultra low-k: integration and reliability”, IEEE Int. Interconnect Technology Conf., pp. 21-23, 2002,

5 H. J. Lee, Y. H. Kim, J. Y. Kim, E. K. Lin, B. J. Bauer, W.l. Wu, and H. J. Kim,” Structural characterization of porous low-k SiOC thin films using x-ray porosimetry”, IEEE Int. Interconnect Technology Conf., pp. 54-56, 2002.

6 C. Waldfried, Q. Han, O. Escorica, A. Margolis, R. Albano, and I. Berry, “Single wafer Rapid Curing^{TM} of porous low-k materials”, IEEE Int. Interconnect Technology Conf., pp. 226-228, 2002

7 K. Buchanan, K. Beekmann, K.Giles, J-C. Yeoh, H.Donohue, “Characterisation and integration of CVD ultra low k films (k<2.2) for dual damascene IMD applications” Proceeding of Advanced Metallization Conference, pp. 73-77, 2001.

8 K. L. Fang, B. Y. Tsui, C. C. Yang, M. C. Chen, S. D. Lee, K. Beekmann, T. Wilby, K. Giles, and S. Ishaq, "Electrical and material stability of OrionTM CVD ultra low-k dielectric film for copper interconnection", IEEE Int. Interconnect Technology Conf., pp. 60-62, 2002.

9 D. M. Brown, M. Ghezzo, J. Kretchmer, E. Downey, J. Primbley, and J. Palmour, "SiC MOS Interface Characteristics", IEEE Transactions on Electron Devices, vol. 41, No. 4, pp. 618-623, 1994

10 H. Yano, F. Katafuchi, T.U. Kimoto, and H. Matsunami, "Effects of Wet Oxidation/Anneal on Interface Properties of Thermally Oxidized SiO_2/SiC MOS System and MOSFET's", IEEE Transactions on Electron Devices, vol. 46, No. 3, pp. 504-150, 1999

11 J. Champi, Y. Shi, Y. Luo, F. Yan, and J. H. Zhao, "Study of Interface State Density and Effective Oxide Charge in Post-Metallization Annealed SiO_2/SiC Structures", IEEE Transactions on Electron Devices, vol. 46, No. 3, pp. 511-519, 1999

12 X. Jun, C. S. Yang, H. R. Jang, and C. K. Choi, "Chemical Structure Evolution of SiOCH Films with Low Dielectric Constant During PECVD and Postannealing", Journal of The Electrochemical Society, vol. 150, No. 12, pp. F206-F210, 2003

1 S. G. Lee, Y. J. Kim, S. P. Lee, H. S. Oh, S. J. Lee, M. Kim, I. G. Kim, J. H. Kim, H. J. Shin, J. G. Hong, H. D. Lee, and H. K. Kang, "Low Dielectric Constant 3MS α-SiC:H as Cu Diffusion Barrier Layer in Cu Dual Damascene Process", Japan Journal of Applied Physics, vol.40, No. 4B, pp. 2663-2668, 2001

2 B. E. Deal and A. S. Grove, "Relationship for The Thermal Oxidation of Si", Journal of Applied Physics, vol. 36, No.12, pp. 3770-3778, 1965.

3 H. Z. Massoud, J. D. Plummer, and E. A. Irene, "Thermal Oxidation of Silicon in

Dry Oxidation - Growth Rate Enhancement in the Thin Regime, Ⅰ Experiment results", Journal of Electrochemical Society, vol. 132, No.11, pp. 2685-2693, 1985.

4 H. Z. Massoud, J. D. Plummer, and E. A. Irene," Thermal Oxidation of Silicon in Dry Oxidation - Growth Rate Enhancement in the Thin Regime, Ⅱ Physical Mechanisms", Journal of Electrochemical Society, vol. 132, No.11, pp. 2694-2703, 1985

5 C. C. Chiang, M. C. Chen, Z. C. Wu, L. J. Li, S. M. Jang, C. H. Yu, and M. S. Liang, "TDDB Reliability Improved in Cu Damascene by using a Bilayer-Structured PECVD SiC Dielectric Barrier", IEEE Int. Interconnect Technology Conf., pp. 200-202, 2002

6 M. Fayolle, J. Torres, G. Passemard, F. Fusalba, G. Fanget, D. Louis, L. Arnaud, V. Girault, J. Cluzel, H. Feldis, M. Rivoire, O. Louveau, T. Mourier, and L. Broussous", Integration of Cu/SiOC in dual damascene interconnect for 0.13um technology using a new SiC material as dielectric barrier", IEEE Int. Interconnect Technology Conf., pp. 39-41, 2002,

7 D. R. Lide, "CRC handbook of chemistry and physics", 83rd edition 2002-2003, CRC Press, Cleveland, Ohio, pp. 9-53, 2002

8 Y. H. Wang, D. Gui, R. Kumar, and P. D. Foo, "Reduction of Oxygen Plasma Damage by Postoxidaiton Helium Plasma Treatment for Carbon-Doped Silicon Oxide Low Dielectric Constant Films", Electrochemical and Solid-State Letters, vol. 6, No.1, pp. F1-F3, 2003.

9 H. Cui; H. Lu; Bhat, I.; Murarka, S.; Lanford, W.; and Weidan Li, "Characterization of methyl-doped silicon oxide film for inter-layer dielectrics application", IEEE Int. Interconnect Technology Conf., pp. 45-47, 2001.

Table 5-1 Oxidation rate constants of SiC in dry O_2 ambient.

SiC	550°C	650°C	750°C	850°C
A	4.28	15.17	17.57	30.05
B	7.60	23.64	44.31	127.56

Table 5-2 Oxidation rate constants of SiC in steam ambient.

SiC	650℃	750℃	850℃
A	116.18	78.47	64.27
B	406.73	574.53	1379.29

Table 5-3 Results of reclaimed wafers

Mean	SiC#1	SiC#2	SiC#3	SiC#4	Si
SiC thickness(nm)	70	70	70	70	0
SiO_2 thickness(nm)	377	390	410	391	351
Deviation(nm)	3.37	6.41	6.7	7.89	12.4

Table 5-4 Particle counts after cleaning

Particle radius	SiC#1	SiC#2	SiC#3	SiC#4	Si
0.2um	24	27	68	44	58
0.3um	1	6	28	13	10
0.4um	2	6	6	6	10
0.5um	3	2	6	2	21
Total counts(>0.2μm)	36	43	112	73	132

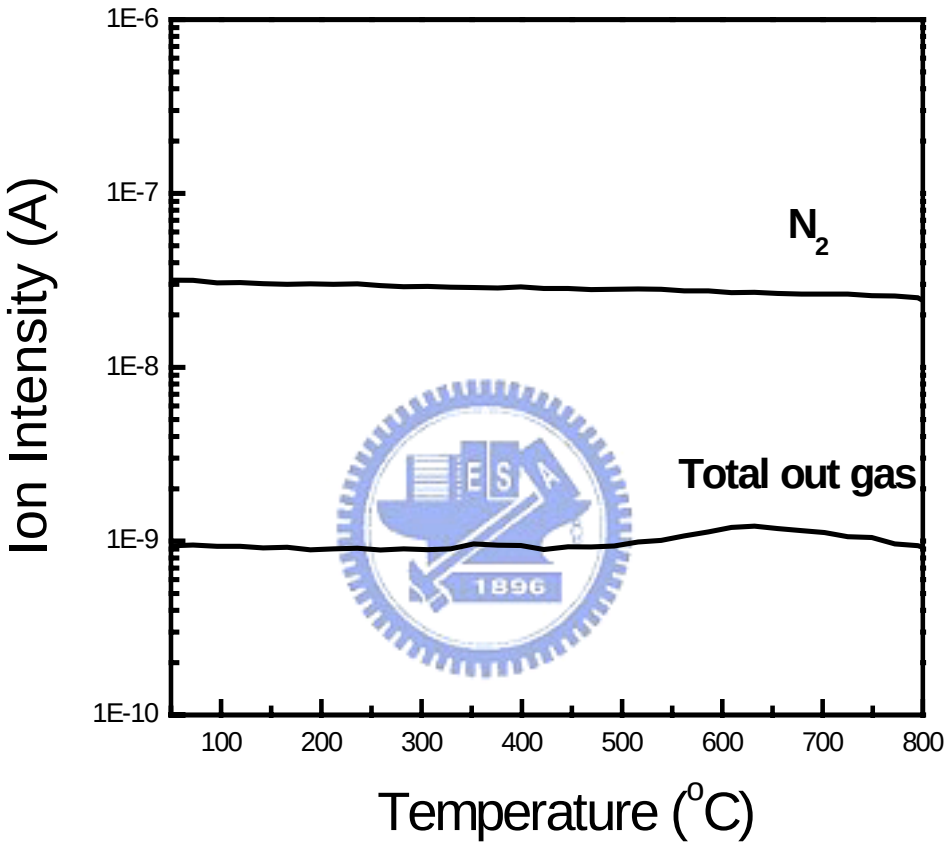


Fig. 5.1 Thermal Desorption Spectroscopy result of SiC outgas

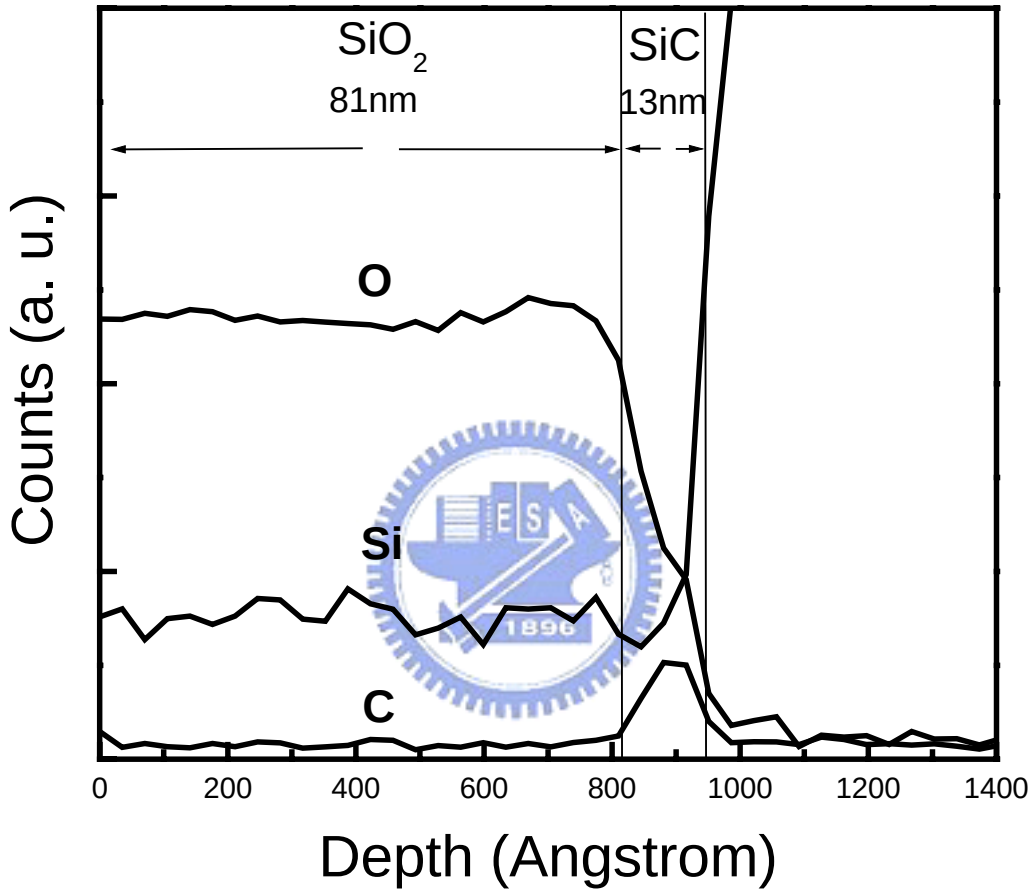


Fig. 5.2. Auger electron spectrum of a partially oxidized SiC film. No carbon content is detected in SiO_2 layer.

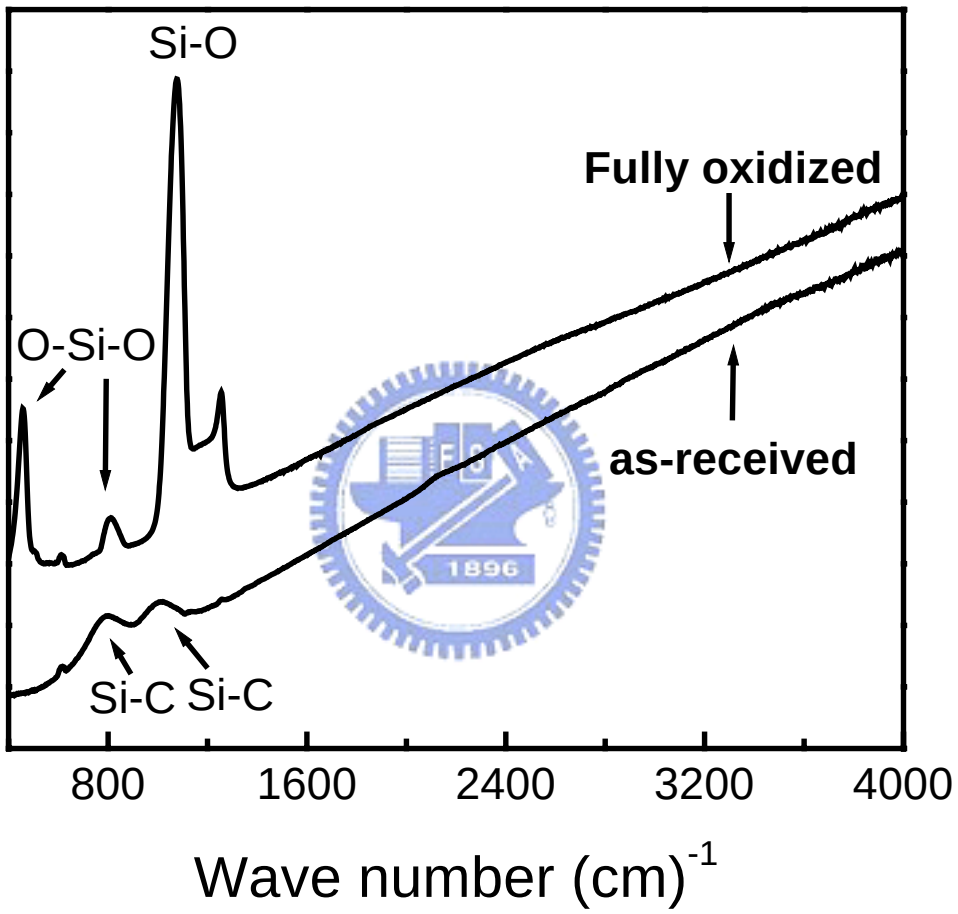


Fig. 5.3 Fourier-transformed infra-red (FTIR) spectrum of a fully oxidized SiC film.

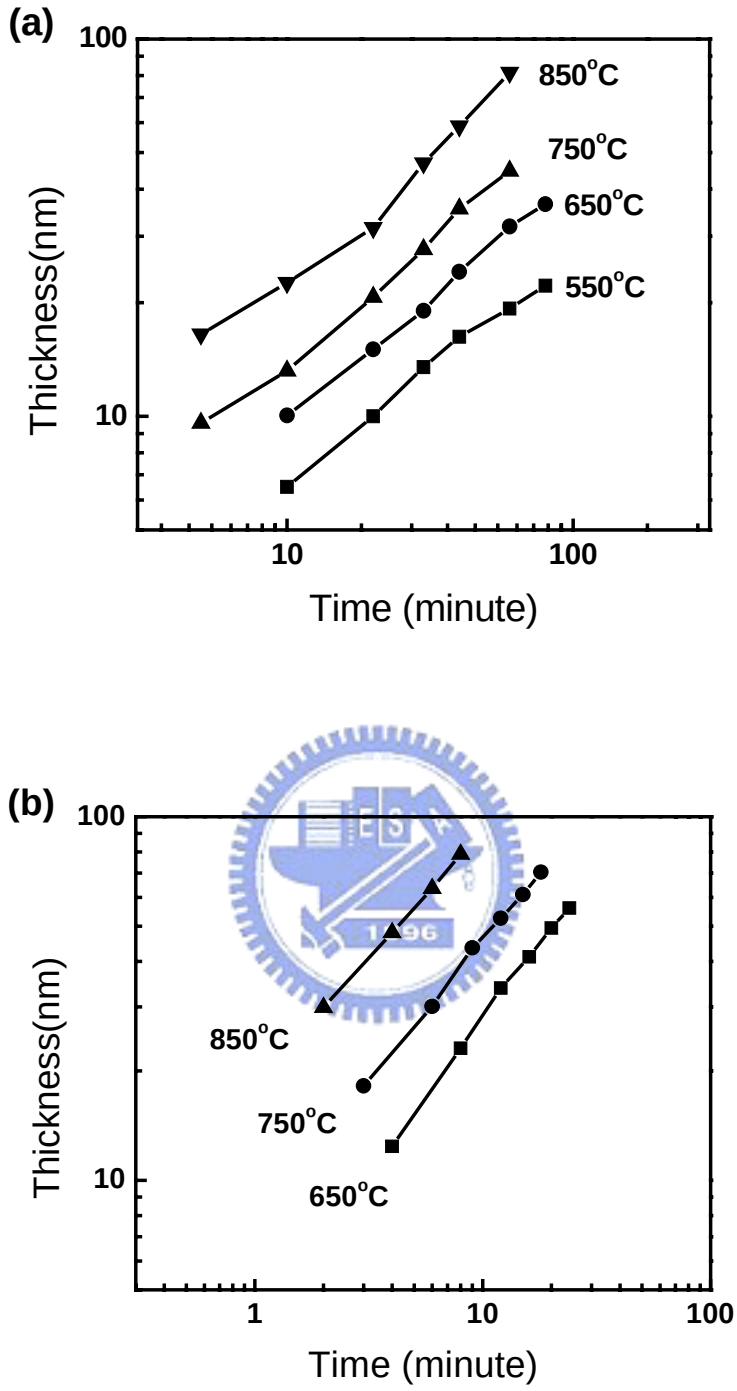


Fig. 5.4 Oxide thickness versus oxidation time of SiC film oxidized in (a) dry O_2 ambient and (b) steam ambient. Steam oxidation is much faster than dry O_2 oxidation. Oxidation occurs at temperature as low as 550℃ at acceptable oxidation rate.

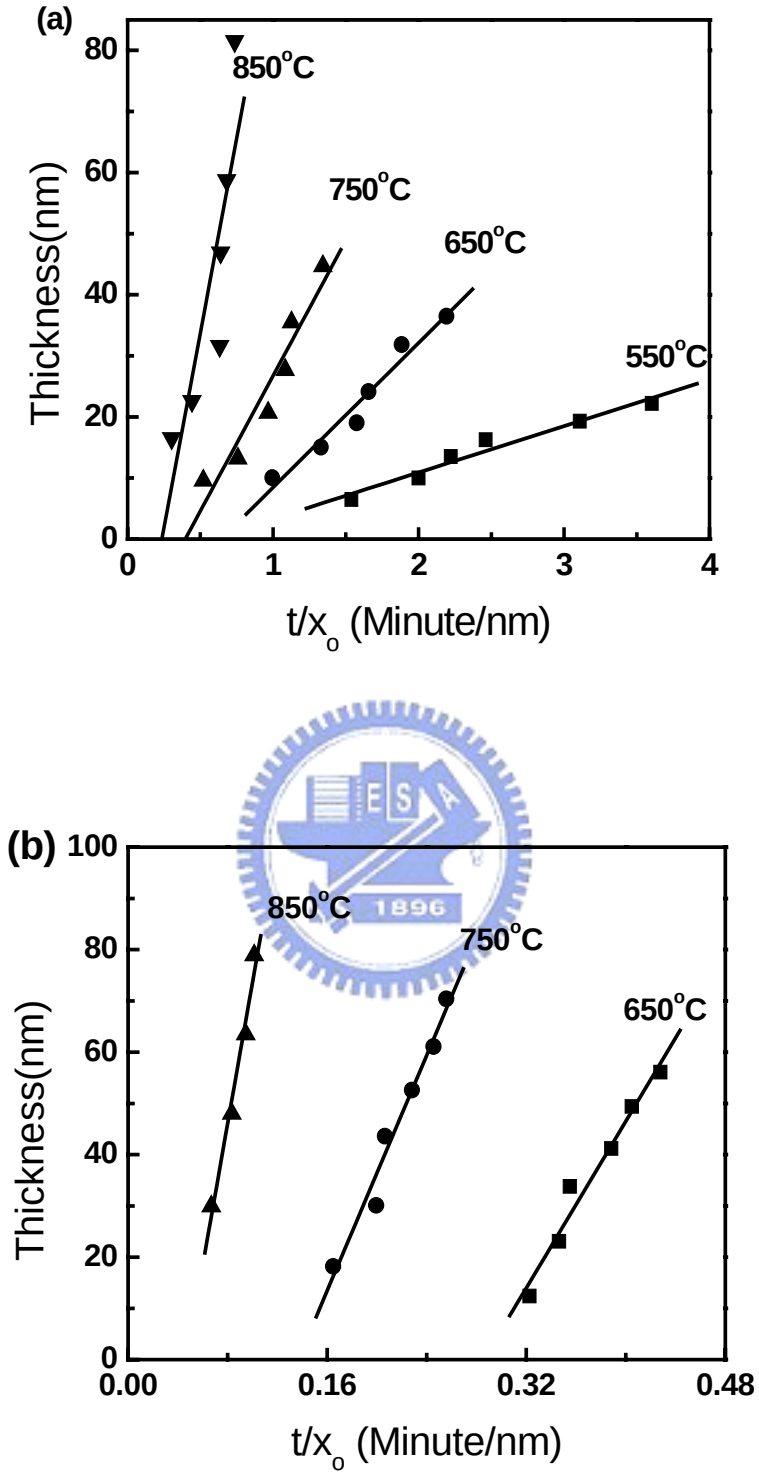


Fig.5.5 Extraction of oxidation rate constants of SiC in (a) dry O_2 ambient and (b) steam ambient. Good linearity indicates that the Deal-Grove model can be used.

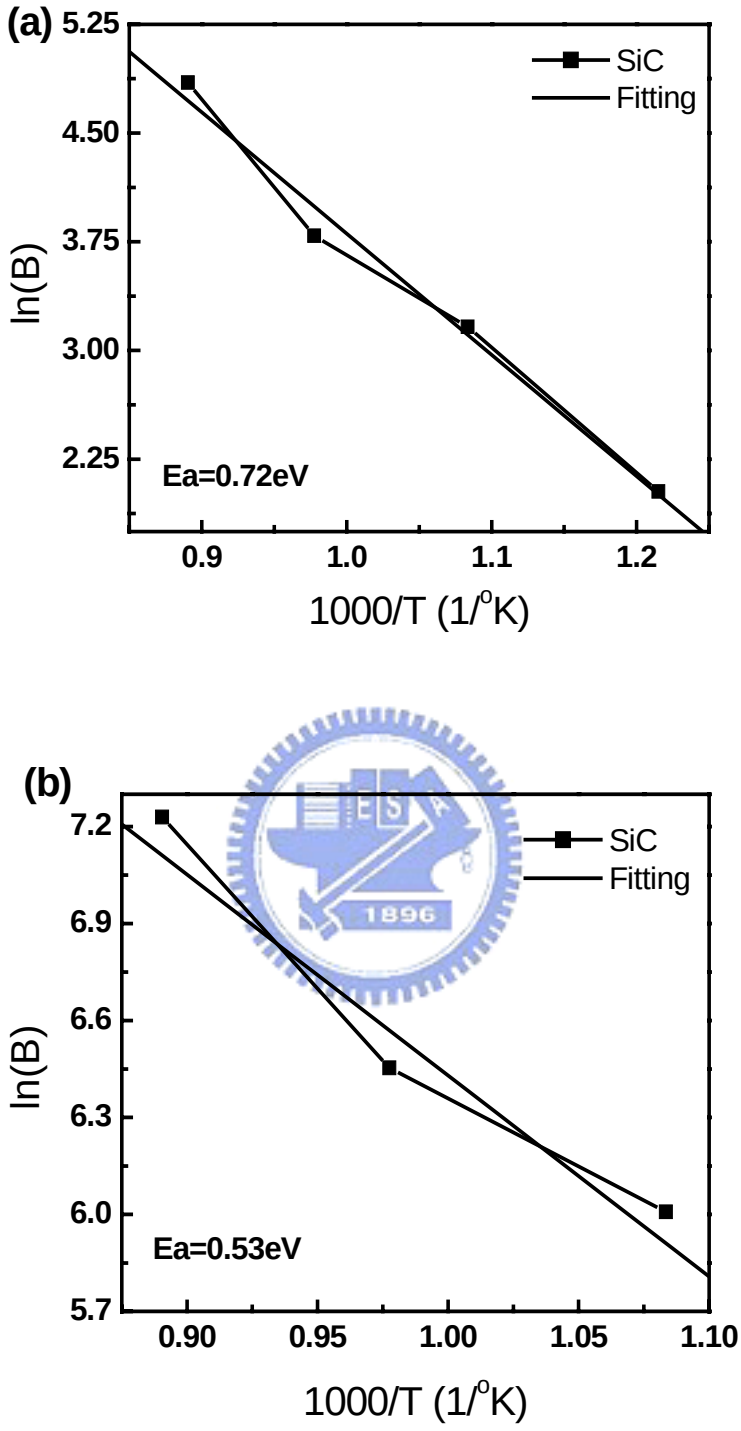


Fig. 5.6 Arrhenius plot of parabolic rate constant of SiC oxidation in (a) dry O_2 ambient and (b) steam ambient. The activation energy is 0.72eV and 0.55eV in (a) and (b),respectively.

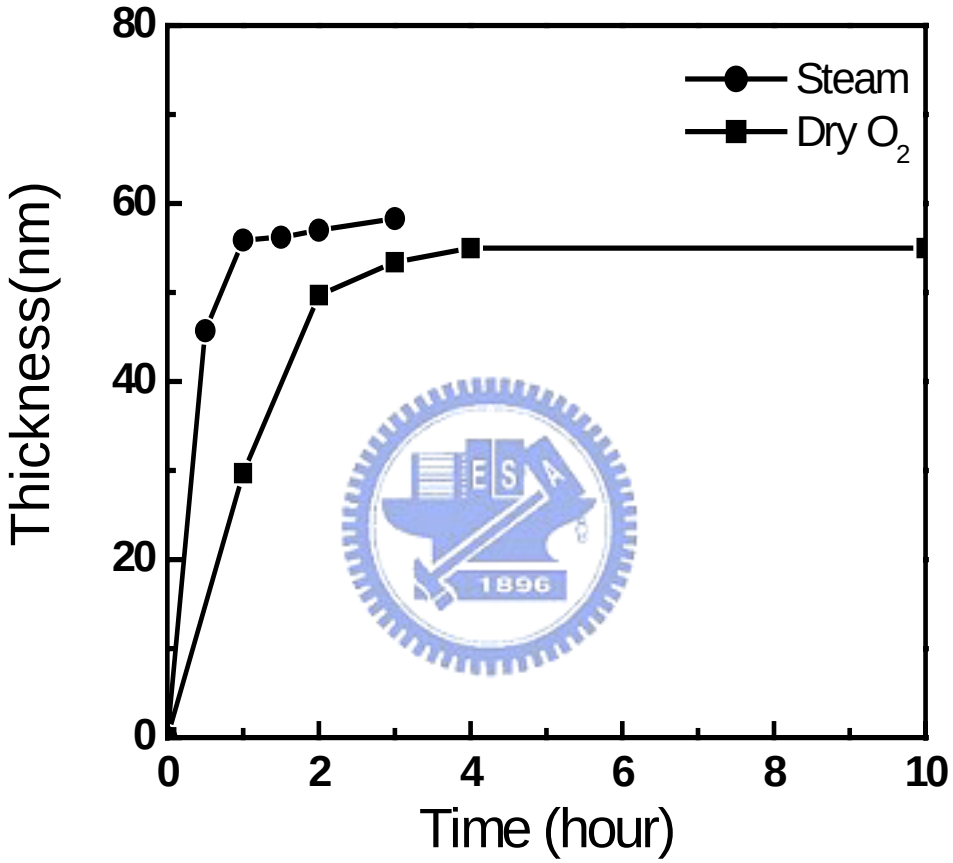
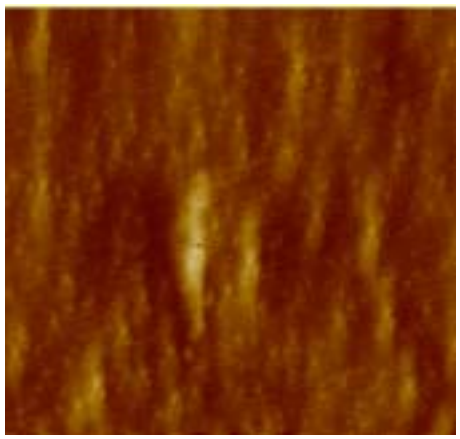
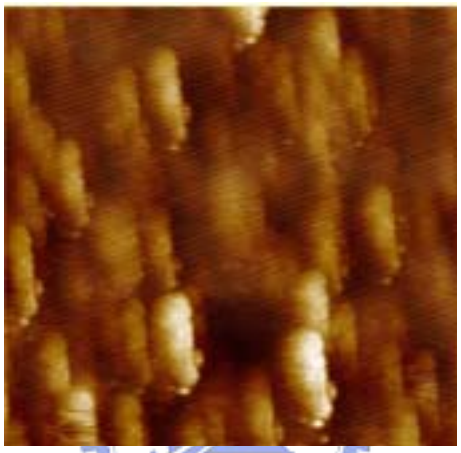


Fig. 5.7 The grown oxide thickness of 54nm thick a-SiC on Si substrate at 600℃

(a)



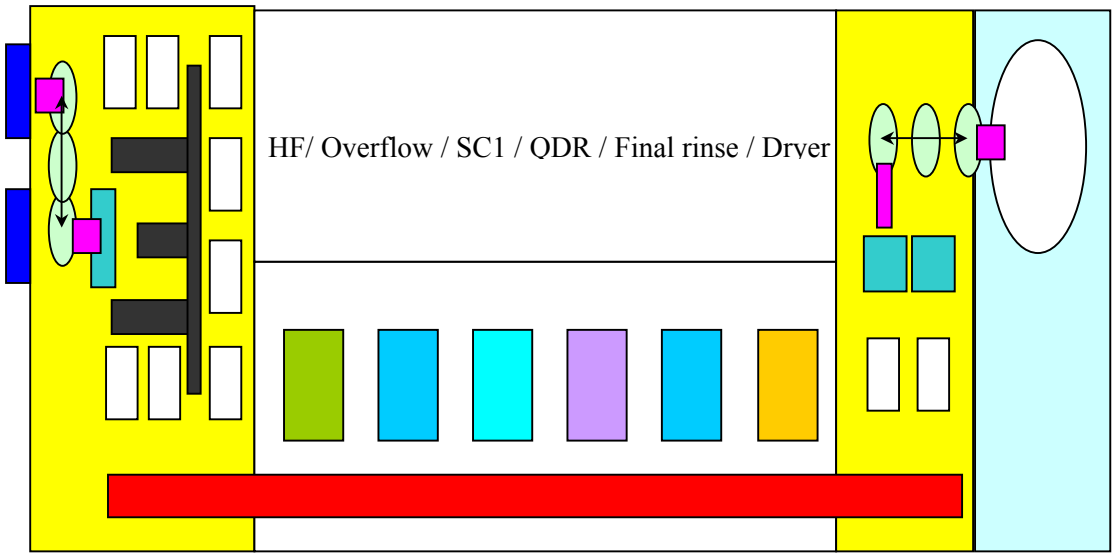
(b)



(c)

Fig. 5.8 Atomic force microscope surface images of (a) the as-deposited SiC surface, (b) the partially oxidized and (c) the fully oxidized a-SiC deposited wafer after oxidation and etching of the oxidized layer.

(a)



(b)

Fig. 5.9(a) the prototypal design of SiC and CDO low-k reclaim instrument with combined vertical furnace and wet chemical bench tank and 5.9(b) final practical instrument model

Chapter 6

Application of Porous Low-k in a High Frequency for Future Generation Transmission Line Interconnect

6.1 Introduction

In order to obtain shorter RC time delay, lower crosstalk noise, and continuously scale down device structures in microelectronics, low dielectric constant materials are used to replace silicon dioxide as an interlevel dielectric [1-3]. To meet the requirements in ultra large scale integration (ULSI) circuit generations, some promising ultra low dielectric constant materials have been developed or are still under development (e.g. Porous CDO and Porous SiLK (P-SiLK)). A spin-coated porous type low dielectric film, such as P-SiLK, is also a promising candidate to be used as a high speed and low noise interconnect material [4].ing candidate to be used as a high speed and low noise interconnect material [4].

Increasing circuit clock rate and increasing complexity of the integration scheme require accurate and verified IC interconnect models for circuit simulations. Modern

IC circuits design, which has to enable nanosecond switching, is limited by the interconnect performance. Simple RC based modeling of the interconnects is no longer adequate [5,6]. An R-L-G-C (Telepgrapher) parasitic model covers the high frequency (RF) (up to giga-hertz) behavior of the interconnect more accurately. With higher frequencies and smaller devices geometries, the demand for a new future interconnect concept becomes more and more important. A relatively radical alternative to the usual metal/dielectric interconnect is to use transmission of signal via RF or microwaves [1]

In this work, the performance of P-SiLK in a transmission line interconnect structure under high frequency was studied for the first time. Distributed transmission line parameters, and stripline losses of P-SiLK interconnects were extracted and discussed. A high frequency P-SiLK dielectric constant fitting extraction was also performed in this work. This characterization technology can be applied to another low k dielectric.

6.2 Experimental Details

A 670nm thick P-SiLK layer was spin-coated on p-type (100)-oriented 6-inches Si wafers. The resistivity of the Si substrate is 1 ohm-cm. Within a lift off process, a 500nm thick PVD Al metal was patterned on the thin P-SiLK film to manufacture the

microstripline test structures. Two basic test structures were used. The major devices under investigation were 1800um co-planar micro-striplines (Fig. 6.1(a)). Besides, single micro-stripline structure was also used (Fig. 6.1(b)). Both types of striplines include 4 different line widths. They are 10um, 15um, 20um, and 25um. In addition, some pad-only structures were used for de-embedding, which is necessary to increase the accuracy of the extracted interconnect parameters. The pad-only test structures consist of ground-signal-ground co-planar metal squares of 25um x 25um in size. A 30 nm thick CVD silicon nitride layer (SiN_x) was deposited on wafer to protect the structure for further measurement and storage. After fabrication of the stripline test structures, an Al-backside metallization was realized including the removal of the native oxide to obtain a reliable ground contact. The cross-sectional view of the test structure is shown in Fig. 6.1(c). In addition, the same preparation sequence was applied to wafers with thermally grown oxide as dielectric instead of P-SiLK. These samples were used as a reference.

Full two-port S-parameters matrix measurements of micro-striplines were performed using a vector network analyzer, of model HP 8753D. The schematic diagram of the two port measurements is shown in Fig. 6.2(a). These measurements were carried out in a frequency range from 60MHz to 6GHz. A full two-port calibration method called Open-Short-Load-Thru (OSLT) was applied with a 50 ohm GGB CS-15 calibration

substrate. The signal propagation in single line interconnect was modeled by the Telegrapher's equation as shown in Fig. 6.2(b). According to this model, the interconnect line parasitic parameters, such as propagation constant (γ), line characteristic impedance (Z), resistance (R), inductance (L), Conductance (G), and capacitance (C) could be calculated from S-parameters measurements.

The stripline propagation constant and characteristic impedance were used to calculate the distributed resistance, inductance, conductance, and capacitance per unit length by the relationships:

$$R + j\omega L = \gamma Z \tag{6.1}$$

and

$$G + j\omega C = \gamma / Z \tag{6.2}$$

High frequency interconnect model parameters, R, L, G, and C were then extracted from the followed equations.

$$R = \mathrm{Re}\{\gamma Z\} \tag{6.3}$$

$$L = \mathrm{Im}\{\gamma Z\}/\omega \tag{6.4}$$

$$G = \mathrm{Re}\{\gamma / Z\} \tag{6.5}$$

$$C = \mathrm{Im}\{\gamma / Z\}/\omega \tag{6.6}$$

6.3 Analysis of Low-k Stripline Structure at High Frequency Domain

To study the low-frequency dielectric constant of P-SiLK, initially different diameter P-SiLK and oxide metal-insulator silicon capacitors were characterized by C-V measurements at 100KHz. As a result, the measured mean dielectric constant values (ε_{SiLK}) of P-SiLK is 2.21 - 2.25 and the dielectric constant value of thermal oxide is 4.02 – 4.06.

6.3.1 High Frequency Interconnect Parasitic Parameters

Since there are many sources of disturbance for S-parameter data such as external noise, and poor calibration, there is a main major criterion to judge the measured data. Since the test structure of striplines are symmetrical, the measured S-parameters have to be also symmetrical, i. e. $S_{ij}=S_{ji}$ and $S_{ii}=S_{jj}$. In order to determine all four R-L-G-C interconnect line parasitic parameters of the Telepgrapher's equation, the stripline propagation constant (γ), and line characteristic impedance (Z) were first calculated from the stripline S-parameters measurement [7-9]. The propagation constant is separated into the attenuation constant (real part of γ) and the phase constant (imaginary part of γ). Fig. 6.3(a) and (b) shows the extracted attenuation, and phase constant of the four stripline width versus frequency. The attenuation constant increases approximately logarithmically with frequency. This means that the signal power loss increases with increasing frequency in this non-ideal

stripline structure. The phase constant ($(2\pi/\lambda) \propto frequency$) as expected shows a linear relationship with frequency. These data are then combined with the impedance data (Fig. 6.4(a) and 6.4(b)) to determine the distributed circuit parameters of the Telegrapher's Equation. The inset illustration in Fig. 6.3(a) and 6.3(b) is the result of oxide reference sample and it has very similar behavior to P-SiLK interconnect co-planar stripline. Furthermore, the real part of characteristic impedance tends to be constant at frequency larger than 1GHz, and the imaginary part of characteristic approaching zero at frequency larger than 1GHz. The impedance data within 1GHz is not so accurately due to the too small electrical length value of short stripline at lower frequency. To obtain more accurate stripline impedance data below GHz range, an impedance meter (such as: HP 4395A system) instead of a network analyzer is suggested to be employed. Besides, the inset of oxide reference sample in Fig. 6.4(a) and 4(b) exhibits very similar behavior. Then R, L, G and C values were extracted from equation (1) to equation (6). Of these four extracted parameters, R and L are related primary to the transmission line conductors, while G and C are related to the dielectric materials [10]. Samples without calibration and with only single stripline structure exhibited non-consistent, irregular data. Only co-planar stripline structures show reliable results.

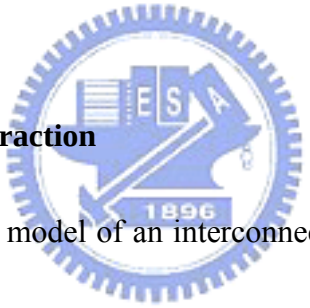
Fig. 6.5, Fig. 6.6, Fig. 6.7 and Fig. 6.8 show the extracted results on co-planar

samples of R, L, G, and C for P-SiLK at different frequencies. The resistance keeps constant with a slight increase towards about 6GHz. As expected, as the linewidth of the microstrip line decreases, the resistance increases accordingly. Both inductance and conductance (dielectric loss) become important in IC interconnect signal propagation parameters as the frequency increase. Fortunately, the inductance keeps unchanged and seems to be independent of the frequency below 6GHz. Although the inductance is not a strong function of frequency below 6GHz [8,9,11], the reactive effect of a constant value of inductance on signal propagation increases linearly with frequency. The conductance stays very small and slightly increases at higher frequency, but it seems to be much more affected by external noise. The slightly increase of conductance would cause a little higher dielectric loss. Capacitance appears initially flat with a slight decrease in the upper 0.1GHz range.

6.3.2 Dielectric Loss and Metallic Loss

Since the measured conductance of the microstriplines are the result of a combination of the upper interlevel dielectric and bottom silicon substrate, both measured oxide and P-SiLK striplines' conductance values are very small and sensitive to small noise levels. Also the extracted P-SiLK stripline dielectric loss ($\tan(\delta_C)$) from the well known equation $\tan(\delta_c) = G/\omega C$, is very small (~0.1). We

observe a slight increase with increasing frequency (Fig. 6.9(a)). The unit free metallic loss ($R/\omega L$) of the stripline conductor is about 2 orders of magnitude higher than the dielectric loss which is shown in Fig. 6.9(b). However it decreases with increase of frequency. We also observed that wider striplines result in higher dielectric loss and lower metallic loss. Although the calculated dielectric loss is induced by the combination of P-SiLK and the Si-substrate, it still proves that the P-SiLK loss can be neglected, since the metallic conductor is the primary source of total loss in the transmission line.



6.3.3 Dielectric Constant Extraction

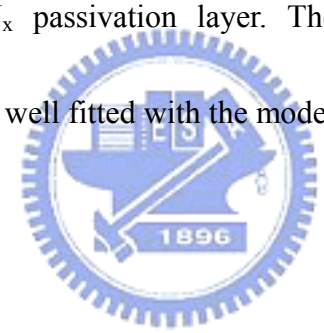
The R-L-G-C parameters model of an interconnect transmission stripline of Fig. 6.2(b) have been well derived in previous publications in considering Si substrate effect [8,9].

$$C = \frac{\omega C_1 C_2 (C_1 + C_2) + C_1 G_S^2}{G_S^2 + \omega^2 (C_1 + C_2)^2} \tag{6.7}$$

where C is the total capacitance, C_1 is the P-SiLK capacitance which is related to ε_{SiLK} , C_2 is the silicon substrate capacitance, G_s is the silicon substrate conductance, ω is the angular frequency. Considering the stripline edge fringing effect, the capacitance of stripline is modeled again in equation (6.8) [8,12].

$$C=\frac{\omega C_1C_2(C_1+C_2)+C_1G_S^2}{G_S^2+\omega^2(C_1+C_2)^2}+\varepsilon\frac{2\pi}{\ln[1+\frac{2h}{t}+\sqrt{\frac{2h}{t}+(\frac{2h}{t}+2)}]}\qquad where\qquad \varepsilon=\frac{\varepsilon_{Si}\varepsilon_{SiLK}}{\varepsilon_{Si}+\varepsilon_{SiLK}}\varepsilon_o \qquad (6.8)$$

,where ε is the averaged dielectric constant of the double layer dielectrics, ε_{Si} is Silicon dielectric constant, and ε_o is the vacuum permittivity, *t* is the stripline width, *h* is the total thickness of P-SiLK and Silicon substrate. After linear regression, P-SiLK and oxide dielectric constants were extracted as 2.51 and 4.6, respectively (Fig. 6.10 (a), (b)). The effective k values of P-SiLK and oxide are both about 10% higher than the (100 KHz) C-V measurement results (2.25 and 4.02) which to the additional thin (30nm) SiN_x passivation layer. The extracted frequency related interconnect capacitances are well fitted with the modeled capacitances.



6.4 Summary

The on wafer high frequency transmission line characterization methodology of low-k film was presented at frequency reach to 6GHz for the first time. P-SiLK is employed to demonstrate the methodology. A reliable parameter extraction was possible with calibrated co-planar micro-striplines. A systematic high frequency Interconnect parameters (R, L, G and C) were derived from S-parameters. Both, metallic and P-SiLK dielectric loss was extracted and demonstrated within the analysis. The low dielectric loss of P-SiLK shows that it is well suitable for high frequency operation. P-SiLK dielectric constant modeled from S-parameters

measurement was also presented and compared with traditional capacitance-voltage (C-V) result. Considering the presence of a thin SiN_x passivation layer, the extracted P-SiLK dielectric constant (2.51) as well as that for oxide (4.6) match with the 100KHz C-V measured result (2.25 and 4.02). Within the investigated frequency range, no resonance was observed with P-SiLK.

References

1 The National Technology Roadmap for Semiconductors, Semiconductor Industry Association, San Jose, CA, 2003.

2 A. T. Kohl, R. Mimna, R. Shick, L. Rhodes, Z. L. Wang, P. A. Kohl, “Low k, porous methyl silsesquioxane and spin-on-glass”, Electrochem. Solid-State Letter, vol. 2, No. 2, pp. 77-79, 1999

3 A. M. Padovani, L. Rhodes, L. Riester, G. Lohman, B. Tsuie, J. Conner, S. Allen, P. A. Kohl, “Porous methylsilsesquioxane for low-k dielectric applications”, Electrochem. Solid-State Letter, vol. 4, No. 11, pp. F25-F28, 2001.

4 J. J. Waterloos, H. Struyf, J. V. Aelst, D. W. Castillo, S. Lucero, R. Caluwaerts, C. Alaerts, G. Mannaert, W. Boullart, E. Sleeckx, M. Schaekers, Z. Tokel, I. Vervoort, J. Steenbergen, B. Sijmus, I. Vos, M. Meurs, F. Iacopi, R. A. Donaton, M. V. Hove, S. Vanhaelemeersch, and K. Maex, “Integration feasibility of porous SiLK* semiconductor dielectric”, IEEE International Interconnect Technology Proceeding, pp. 253-254, 2001.

5 T. Sakurai and K. Tamaru, “Simple Formulas for Two- and Three-Dimensional Capacitances”, IEEE Trans. On. Dlectron Devices, vol. 30, No. 2, pp. 183-185, 1983.

6 C. P. Yuan and T. N. Trick, “A simple Formula for the Estimation of the Capacitance of Two-Dimensional Intercoonects in VLSI Circuits”, IEEE Electron Device Letter, vol. EDL-3, no.12, pp. 391-393, 1982

7 K.C. Gupta, Ramesh Garg, and Rakesh Chadha, “Computer Aided Design of Microwave Circuits”, Dedham, Ma: Artech House, pp.25-43, 1981.

8 Y. Eo and W. R. Eisenstadt, “High-speed VLSI interconnect modeling based on S-parameter measurements”, IEEE Trans. on Components, Hybrids, and

Manufacturing Technology, vol. 16, No. 5, pp. 555-562, 1993

9 W. R. Eisenstadt, and Y. Eo, “S-parameter-based IC interconnect transmission line characterization”, IEEE Trans. on components, Hybrids, and Manufacturing Technology, vol. 15, No. 4, pp.483-450, 1992

10 R. Marks and D. Williams, “A general Waveguide Circuit Theory”, Journal of Research of the National Institute of Standards and Technology, vol. 97, no.5, pp.533-562, 1992

11 H. Hasegawa, M. Furukawa, and H. Yanai, “Properties of Microstrip Line on Si-SiO_2 System”, IEEE Trans. on. Microwave Theory Tech., vol. 19, No. 11, pp. 869-881, 1971

12 C. P. Yuan and T. N. Trick, “A simple Formula for the Estimation of the Capacitance of Two-Dimensional Intercoonects in VLSI Circuits”, IEEE Electron Device Letter, vol. EDL-3, no.12, pp. 391-393, 1982

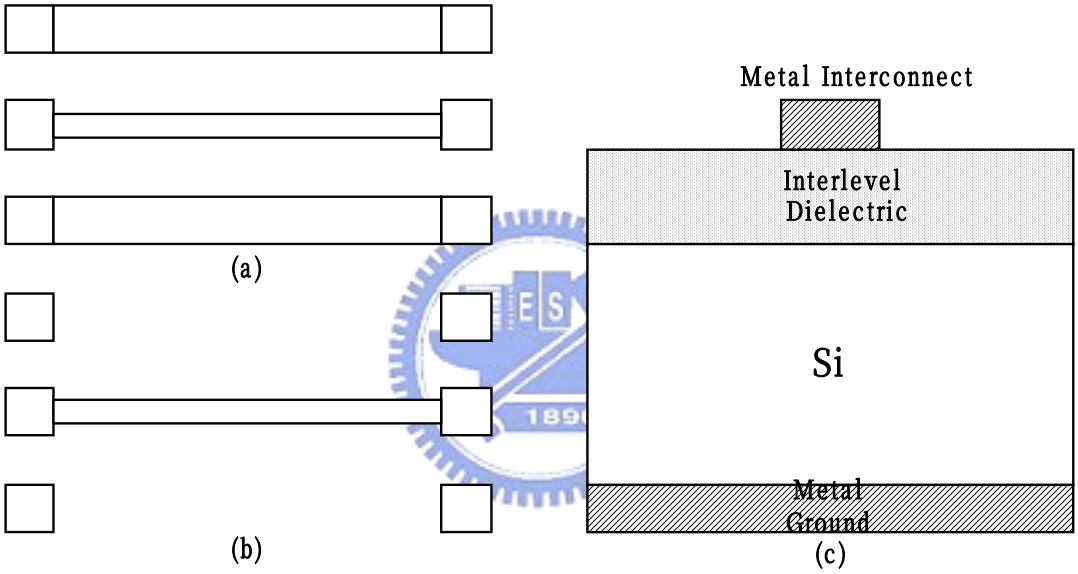


Fig. 6.1. (a) IC interconnect high frequency test structure layout (a) Test structure with co-planar structure (b) Test structure without co-planar structure (c) Wafer interconnect stripline cross section

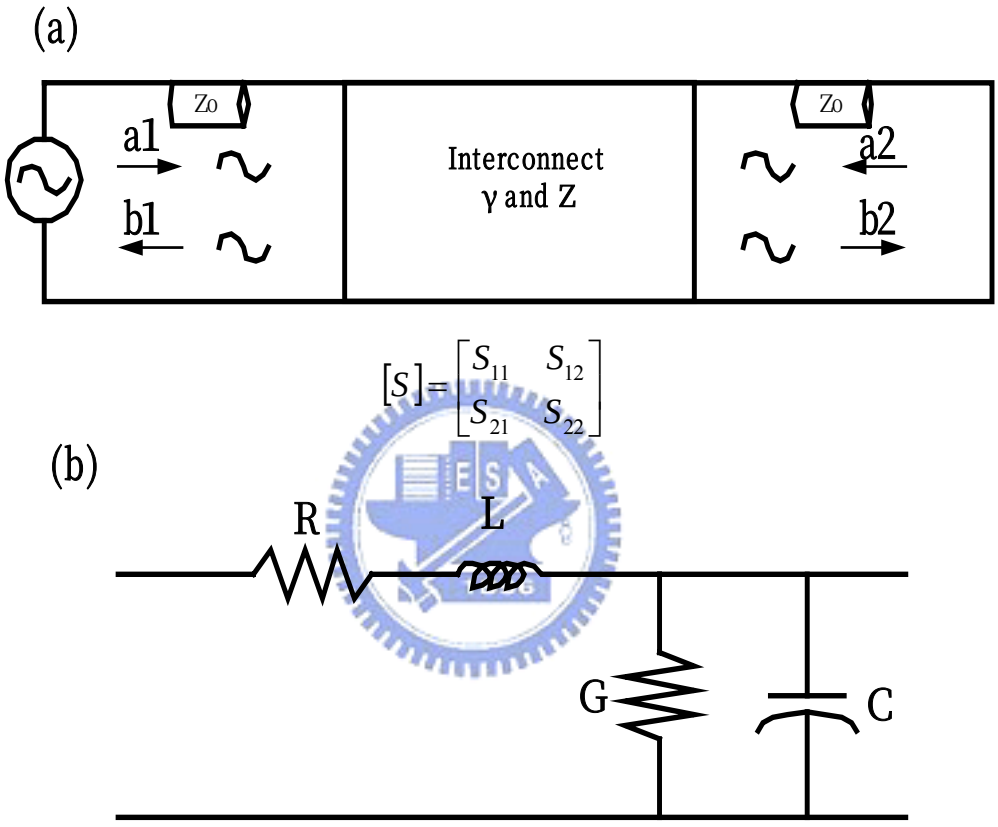


Fig. 6.2. (a)Two port S-parameter measurement network (b) Single conductor interconnect represent model.

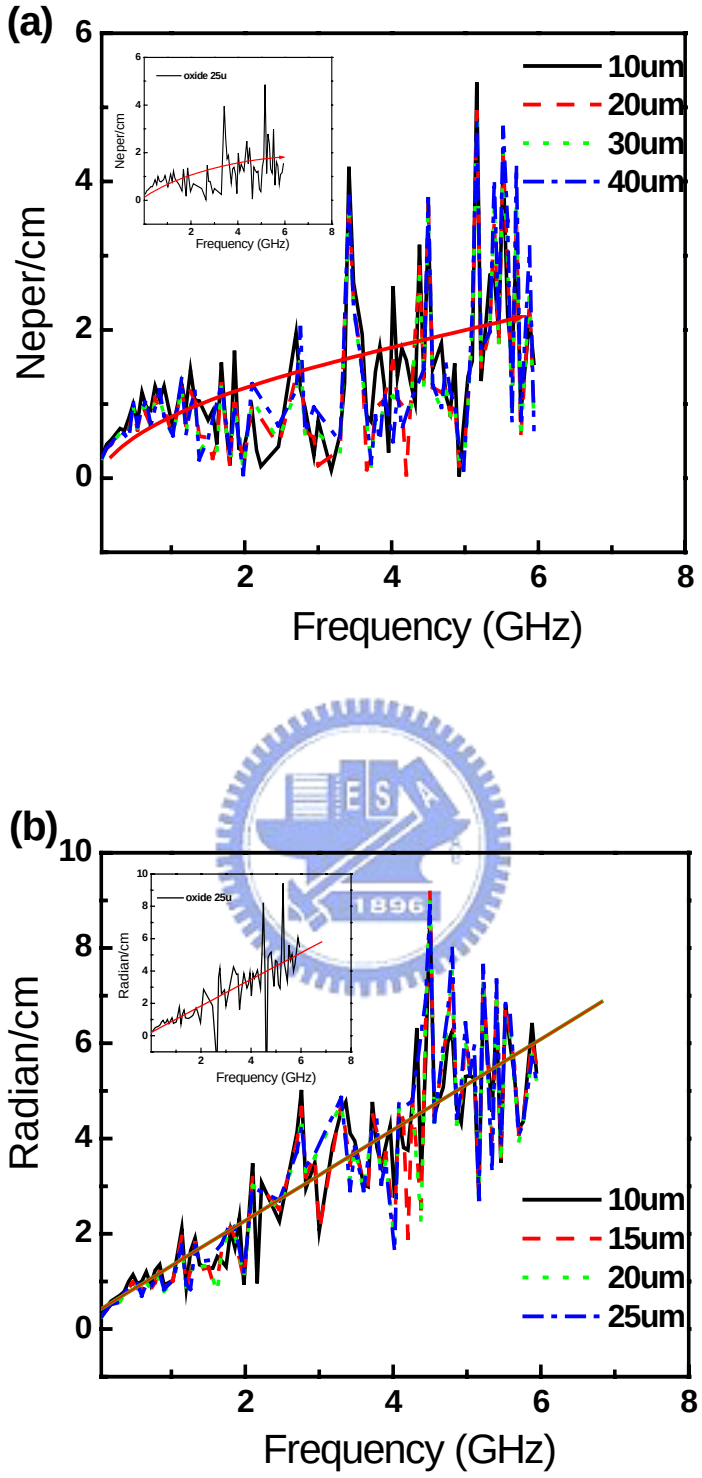


Fig. 6.3 P-SiLK co-planar stripline interconnect (a) attenuation and (b) propagation constant versus frequency. The sub-inlet illustration is the Oxide interconnect reference sample.

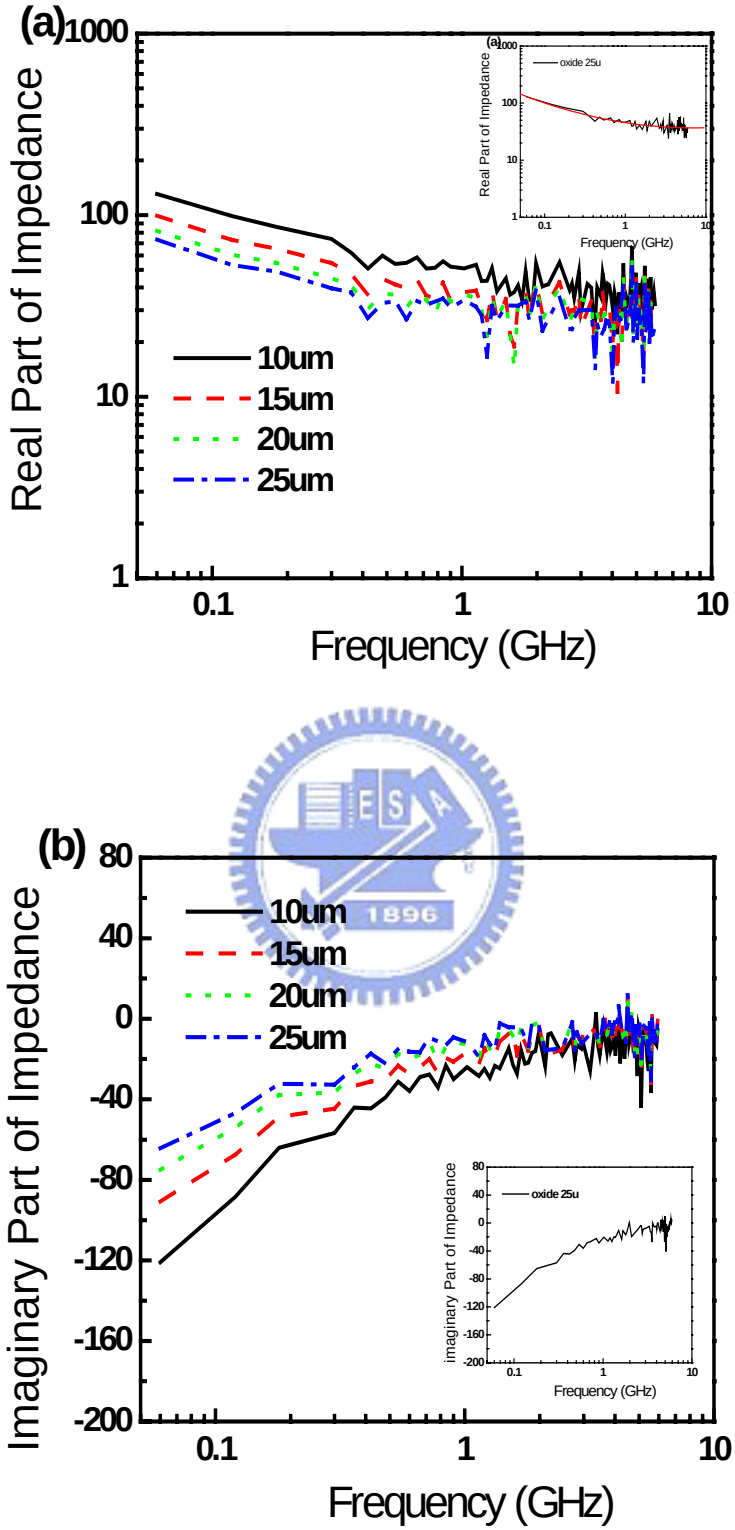


Fig. 6.4(a) real part and (b) imaginary part of P-SiLK co-planar stripline interconnect characteristic impedance. The sub-inlet illustration is the Oxide interconnect reference sample.

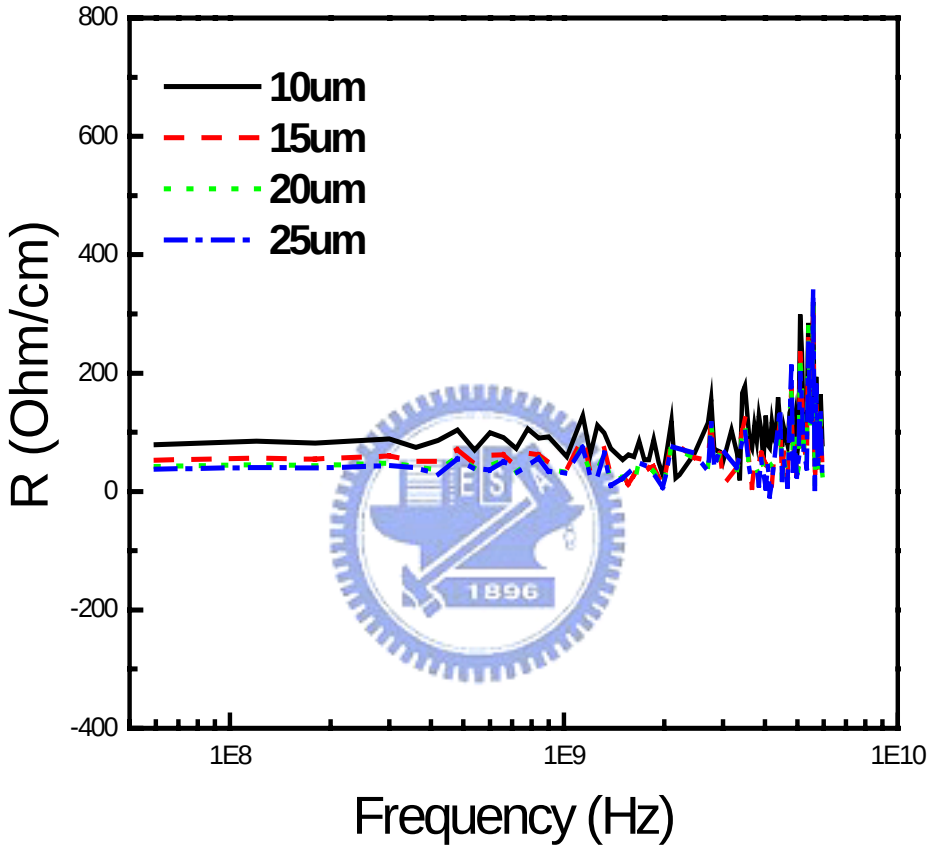


Fig. 6.5 Resistance variation versus frequency from S-parameter measurement of P-SiLK co-planar stripline interconnect

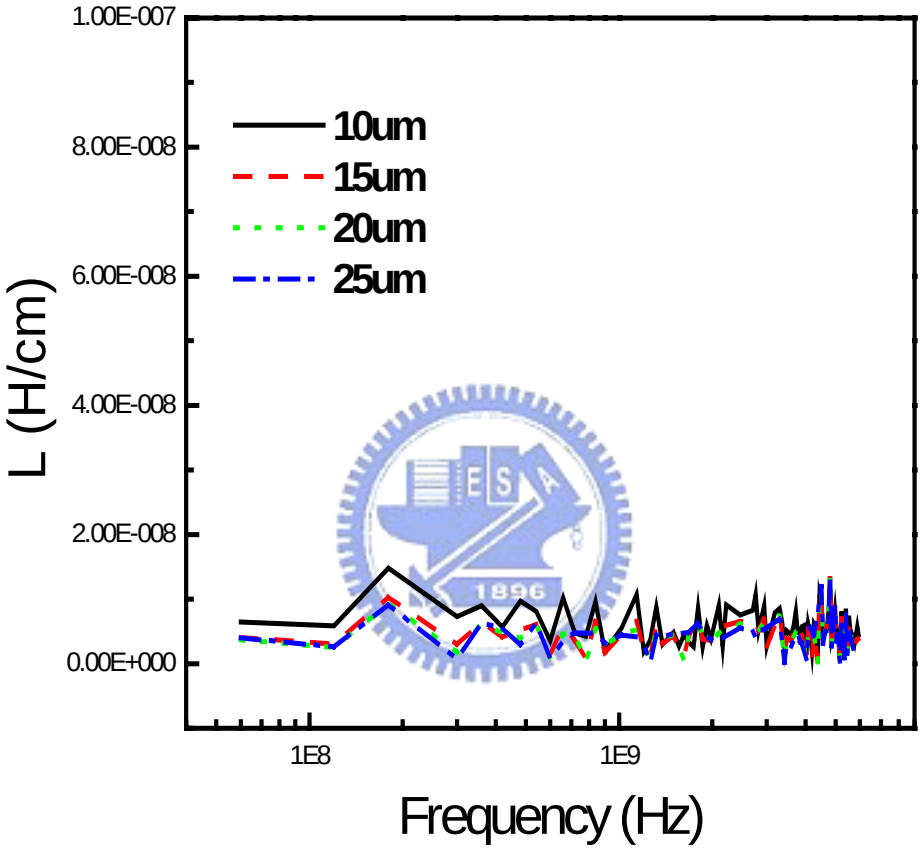


Fig. 6.6 Inductance variation versus frequency from S-parameter measurement of P-SiLK co-planar stripline interconnect

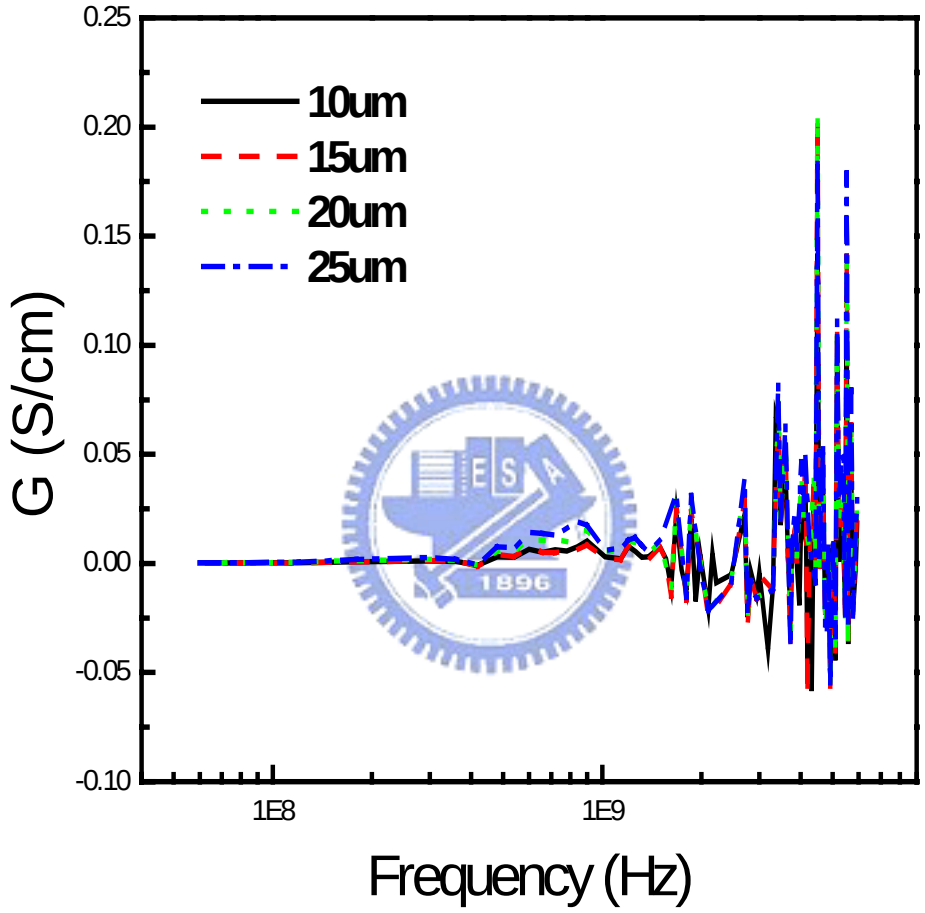


Fig. 6.7 Conductance variation versus frequency from S-parameter measurement of P-SiLK co-planar stripline interconnect

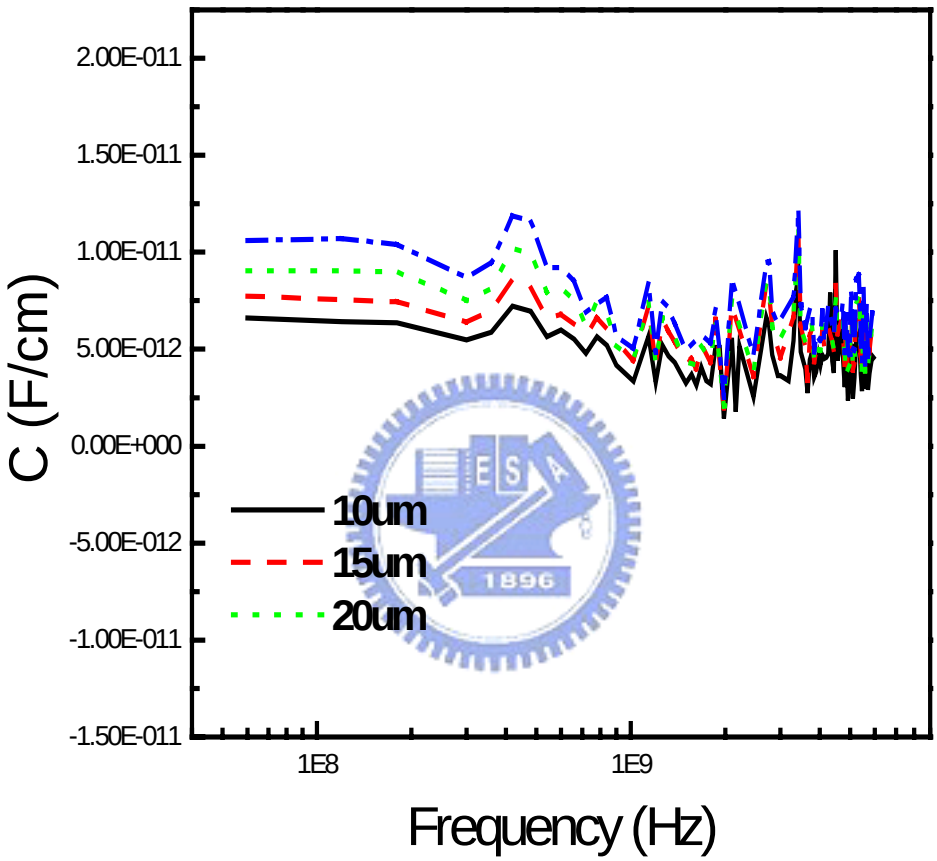


Fig. 6.8 Capacitance variation versus frequency from S-parameter measurement of P-SiLK co-planar stripline interconnect

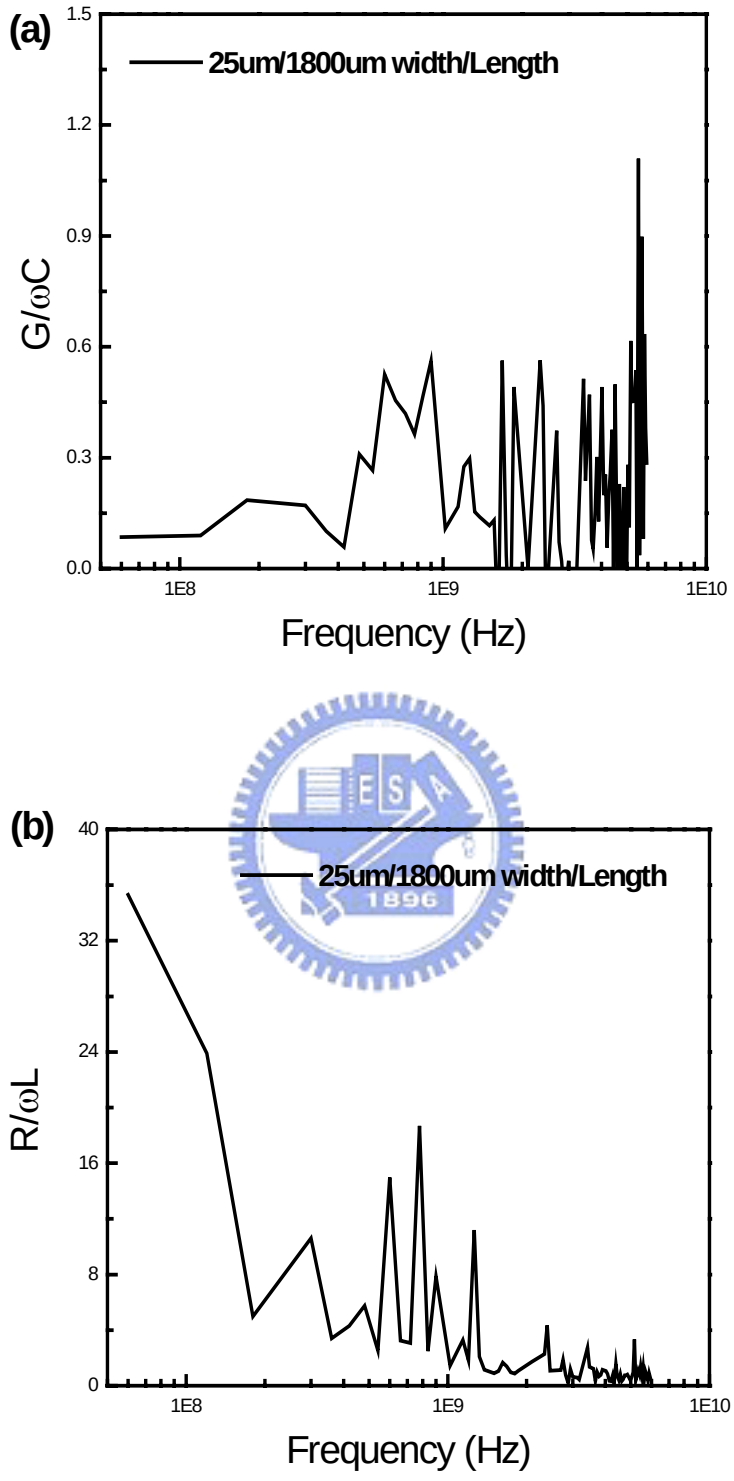


Fig. 6.9 (a) Extracted loss tangent and (b) metal loss of P-SiLK co-planar stripline interconnect

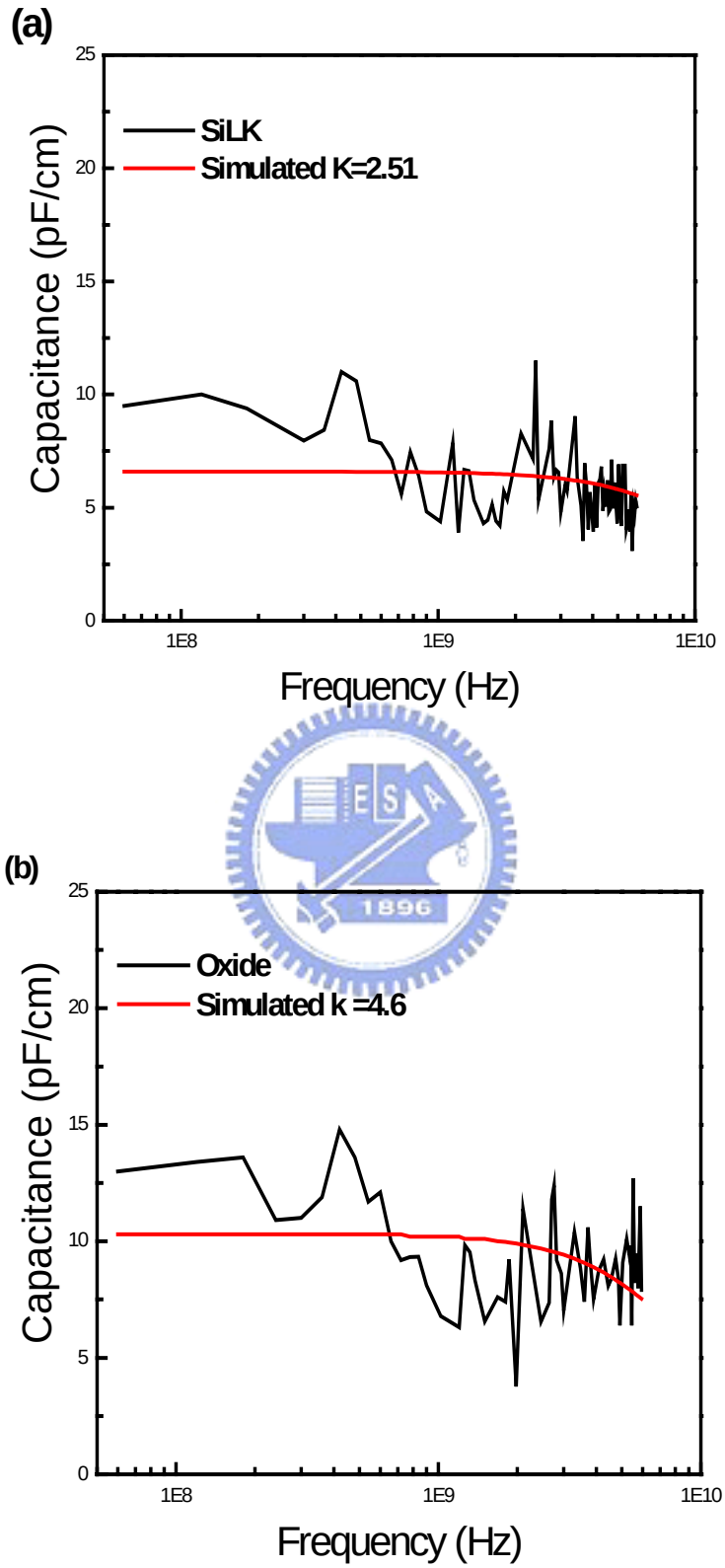


Fig. 6.10 Simulated (a) P-SiLK and (b) oxide co-planar stripline interconnect dielectric constant

Chapter 7

Conclusions and Suggestions for Future Work

7.1 Conclusions

In the first part of this dissertation, electrical instability mechanisms of various low dielectric constant dielectrics are studied. They are low-k material (FSG), ultra-low-k material (porous CDO), and low-k dielectric Cu diffusion barrier (a-SiC). Instability model combining metal ion diffusion, dielectric polarization, and carrier injection was proposed to explain the instable phenomenon of all kinds of low k dielectric.

The most serious electrical instability would be the Cu ion diffusion into low-k dielectric. It is observed that surface processing enhances Cu ion diffusion into FSG film. A surface-damage-layer-enhanced Cu ionization model was proposed. This surface process damaged FSG film greatly affects the Cu diffusion behavior. This may explain the inconsistent results reported in the literature. Furthermore, even if the as-deposited FSG film shows good barrier properties against Cu diffusion, the damascene process will produce a damaged surface layer to enhance the Cu diffusion. Thus, a suitable barrier layer is still necessary because the FSG film has been

processed before Cu deposition. Thus, it is strongly recommended that the surface processed film be used to evaluate the behavior of Cu diffusion into all of the low k dielectric films.

The ultra low-k porous CDO film is a very promising material for next generation ICs IMD for its low dielectric constant (k~2.2). CDO exhibits a very high thermal stability (no FTIR spectrum change after annealing at 650°C/30min N_2 annealing), and a very low leakage current (lower than 1nA/cm^2 at 30°C and 2.5MV/cm). The electrical stability of CDO was carefully studied. We found that the lack of Al_2O_3 interfacial layer formation resulted in Al ions diffusion into CDO film. The porous structure of CDO film would enhance metal ions movement in it. Although both Al and Cu ions can be driven into CDO under electrical stress, no metal ions are observed in CDO with TaN gate. Combining with those good properties reported previously, CDO is still a very promising material for next generation Cu-interconnect technology. Besides, a physical model combined with dielectric polarization, leakage carrier injection, and metal ions diffusion are proposed to explain the observed electrical instability of the CDO film. With the same analysis methodology, we also suggest that all possible causes of electrical instabilities can be clarified for all other low-k films.

It is expected that the amorphous SiC (a-SiC) deposited by CVD system is the

most promising low dielectric constant diffusion barrier to replace SiN in the Cu-interconnect structure. SiC integrated with Cu and low-k materials could further reduce interconnect RC delay. The basic properties including low dielectric constant, good Cu barrier ability, and low moisture uptake are confirmed in this work. Furthermore, detailed a-SiC electrical instability behavior is discussed. At electric fields higher than 1.8MV/cm, charges irrespective of the polarity will be built-up in the SiC film. The total polarity charges depend on the applied electric field. It is also found that V_{fb} shift occurred for the Al-SiC-1 capacitor under a 0.4MV/cm electric field stress at high temperature. It is confirmed that electron injection from gate metal via Schottky emission process in the Al-SiC-1 capacitor. A model combined with dielectric polarization and leakage carrier injection is proposed to explain the electrical instability of a-SiC films.

The medium temperature oxidation process of a-SiC was reported for the first time. The oxidation can be described with Deal-Grove model. Our study also found that the oxidation process of a-SiC would self-stop at Si surface after a-SiC was fully consumed out at a temperature as low as 550℃. Besides, we also found the same oxidation behavior of Carbon Doped Oxide films. All these oxidized films could easily wet etch out by HF solution. This two steps sequence, oxidation followed by HF etching, provides a universal low-k film stripping method. This new wafer reclaim

solution provides faster, lower cost, and less wafer damages than traditional chemical mechanical polishing (CMP) or reactive ion etch (RIE)

The on wafer high frequency transmission stripline characterization methodology of low-k film was presented at frequencies up to 6GHz for the first time. Porous-SiLK (P-SiLK) was employed to demonstrate the methodology. A systematic high frequency interconnect parameters (R, L, G and C) were derived from S-parameters. The low P-SiLK dielectric loss shows that it is well suitable for high frequency operation. P-SiLK dielectric constant modeled from S-parameter extraction was also compared with that obtained from the traditional capacitance-voltage (C-V) method. By this methodology, we could also provide a basic characterization method for other low-k films to find out the possibility being applied in a high frequency transmission condition.

7.2 Suggestions for Future Work

Although several issues have been clarified and some breakthrough have been achieved in this dissertation, there are a number of topics which deserve future studies:

1. Though the details properties of CDO have been characterized, but the behaviors of real interconnect dual damascene structure integrating Cu with CDO are still unknown. Problems happened during process integration, electric characteristics

of CDO film after integration, and interconnect device reliability of Cu/CDO damascene structure has to be carefully studies.

2. Those nano-porous structure that effectively reduce CDO k value to ~2.2 make CDO film a promising IMD candidate. On the other hand, it degrades the thermal conductivity of CDO film. This hardly radiated heat produced during device operation would seriously degrade device and interconnect lifetime. Thus more detail study of CDO thermal conduction behaviors is unavoidable.

3. The use of a-SiC together with Cu and CDO film in a dual damascene structure becomes more attractive to reduce RC delay. More study on this integrated interconnect-structure would help to realize the possibility of put both a-SiC and CDO into practice ICs.

4. During the high frequency micro-stripline characterization process in chapter-6, the ground signal contact was located at backside Si-substrate. Thus this lossy Si-substrate contributes the stripline capacitance, conductance, and dielectric loss variations. It is suggested that using a metal/low-k P-SiLK/metal cross-section structure to characterize P-SiLK would obtain more accurate high frequency dielectric characteristics.

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(民國 87 年 9 月~民國 93 年 9 月)

論文題目：低介電常數材料應用於多層導體連線之電特性分析及其相關技術之研究

Electrical Characteristics Study of Low Dielectric Constant Materials in Multilevel Interconnect System and Its Application

經歷：

1.工研院電子所(ERSO/ITRI)建教合作“銅及低介電常數材料之電性量測及分析” (89 年 1 月~89 年 9 月)

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Publication List

A. International Regular Journals:

1. B. Y. Tsui, **Kuo-Lung Fang**, and S. D. Lee, "Electrical Instability of Low Dielectric Constant Diffusion Barrier Film (a-SiC:H) for Copper Interconnect", IEEE Trans. On Electron Devices, vol.48, NO. 10, pp2375-2383, 2001
2. B. Y. Tsui, **Kuo-Lung Fang**, and S. D. Lee, "Surface-Processing-Enhanced Copper Diffusion into Fluorosilicate Glass", Journal of Electrochemical Society, vol.148, ppG616-G619, 2001
3. **Kuo-Lung Fang**, and B. Y. Tsui, "Metal drift instability in Porous Low dielectric constant Film", Journal of Applied Physics, vol. 93, NO. 9, pp5546-5550, 2003
4. B. Y. Tsui, C.C. Yang, **Kuo-Lung Fang** "Anisotropic Thermal Conductivity of Nano-Porous Silica Film", IEEE Trans. On Electron Devices, Vol 51, NO. 1, pp20-27, 2004.
5. **Kuo-Lung Fang**, and B. Y. Tsui, "Oxidation Mechanisms of Silicon Carbide and Carbon Doped Low Dielectric Constant Thin Films", Accept for publication in IEEE Trans. On Semiconductor Manufacturing
6. **Kuo-Lung Fang**, and B. Y. Tsui, "Electrical Properties of Ultra Low Dielectric Constant Porous CVD film for Copper Interconnect", IEEE Trans. On Electron Devices, in 2nd revision

7. **Kuo-Lung Fang**, B. Y. Tsui, Konrad Melzer, and Johann W. Bartha, "Application of Porous low-k in a High Frequency Transmission Line Interconnect", Japan Journal of Applied Physics, in 2nd revision

B. Conference Papers:

1. Z.Wu, Z. Shiung, C. Wang, **Kuo-Lung Fang**, R. Wu, Y. Liu, B. Tsui, M. Chen, "Electrical Reliability Issues of Integrating low-k dielectrics with Cu Metallization", IEEE International Interconnect Technology Conference,pp82-84, 2000
2. **Kuo-Lung Fang**, B. Y. Tsui, C.C. Yang, S. D. Lee, "Electrical Reliability of Low Dielectric Constant Diffusion Barrier (a-SiC:H) for Copper Interconnect", IEEE International Interconnect Technology Conference, pp250-252, 2001
3. **Kuo-Lung Fang**, B. Y. Tsui, C.C. Yang, M. C. Chen, S. D. Lee, K. Beekmann, t. Wilby, K. Giles, S. Ishaq, "Electrical and Material stability of Orion™ ultra low-k dielectric film for copper interconnection", IEEE International Interconnect Technology Conference, pp60-62, 2002
4. **K. L. Fang**, B. Y. Tsui, C.C. Yang, K. Beekmann, "Electrical Stability of Nano-Porous Low Dielectric Constant Film", Symposium on Nano Devices Technology, pp48-51 2002

5. **Kuo-Lung Fang**, and B. Y. Tsui, “Metal Drift Induced Electrical Instability of Porous Low Dielectric constant Film”, Symposium on Nano Devices Technology, pp325-328, 2003

6. **Kuo-Lung Fang**, B. Y. Tsui, C. H. Wu and Y. H. Li, “Kinetics of Oxidation of Silicon Carbide and Low Dielectric Constant Carbon Doped Oxide”, Symposium on Nano Devices Technology, pp127-130, 2003

7. B. Y. Tsui, C.C. Yang, **Kuo-Lung Fang**, “Anisotropic Thermal Conductivity of Nano-Porous Silica Film”, IEEE International Symposium on VLSI Technology System and Application, pp251-254 2003.

8. B. Y. Tsui, **Kuo-Lung Fang**, C. H. Wu and Y. H. Li, “A Novel Wafer Reclaim Method for Silicon Carbide Film”, IEEE Symposium on Semiconductor Manufacturing, pp191-194, 2003.

C. Others:

1. **方國龍**，崔秉鉞，“低介電常數材料之基本電性量測分析介紹”，電子月刊 92 年 10 月號第 99 期 133 至 152 頁。

D. Patents:

1. 崔秉鉞，**方國龍**，黎源欣，吳志鴻，“碳化矽及低介電常數薄膜之清除方法與裝置”，中華民國專利(ROC 561540)及美國專利(申請中)。