國立交通大學

電機學院微電子奈米科技產業研發碩士班

碩 士 論 文

電流重複用之超寬頻金氧半低雜訊放大器應用於 3.1-10.6GHz

An Ultra-Wideband CMOS LNA with Current-Reused Technique for 3.1 to 10.6GHz

研 究 生：李富國

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中 華 民 國 九十七 年 六 月

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A Thesis

Submitted to College of Electrical and Computer Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

In

Industrial Technology R & D Master Program on

Microelectronics and Nano Sciences

June 2008

Hsinchu, Taiwan, Republic of China

中華民國九十七年六月

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摘　　要

本論文研製之一個電流重複使用低雜訊放大器，此低雜訊放大器具有高增益、低功率、低雜訊且小面積之優點。我們採用三級方式有別於一般電流重複使用低雜訊放大器，來擴充高頻的頻寬，使增益更為平坦，在第一級部分，我們是利用帶通慮波器來做input matching，接著第二級部分，利用疊接方式來達到電流重複使用，以降低功率消耗，最後我們採用一個LC並聯共振電路方式，來增強高頻部份的增益並增加頻寬作為第三級，在輸出部分則是利用current buffer的方式來達到output matching。供應電壓V_{DD}為 1.8 伏特時，整個電路功率消耗約為 10.3mW，及包含pad的情況下整個電路大小約為 0.89 mm^2。本研究的低雜訊放大器所量測的規格，平均順向增益(S_{21})在 3.1~10.6GHz時為 10dB，逆向隔離(S_{12})為-33dB以下，S11 為-9dB以下，S22 約為-11dB以下，而平均雜訊指數約為 3.6dB。

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ABSTRACT

A procedure is for an Ultra-Wideband CMOS LNA with Current-Reused Technique for 3.1 to 10.6GH$_Z$. It has an advantage of high gain, low power consumption, low noise performance and small size. We utilize three-stage amplifier to get a flat gain at high frequency. The first stage introduces the band pass filter for input matching, the second stage introduces a current-reused cascaded common-sources structure to lower power consumption. The last stage introduces shunt-LC resonance to improve gain and the bandwidth. The current buffer configuration is used for output matching. The total power dissipation of the chip is about 10.3 mW at power supply 1.8 volt. The chip size included pad is 0.89 mm^2. The measurement result of this study expect that the average forward S_{21} is 10dB at 3.1~10.6GHz, the reverse isolation S_{12} is under -33dB, the magnitude of S_{11} is under -9 dB, the magnitude of S_{22} is under -11dB, and the noise figure is 3.6dB.

誌　　謝

本篇碩士論文順利完成，首先感謝指導老師荊鳳德教授，老師熱誠的態度與對研究的敏銳度感染了實驗室每位同學，在老師的指導下順利完成學業，讓我學習到很多。在此致上我最深的尊敬與感謝。

感謝交通大學 ED633 實驗室的全體同學，感謝高瑄苓博士，張慈慷博士，李佩諭學姐 給予我的建議與關心，提供我許多寶貴經驗。感謝同屆同學陳膺任，劉思麟 在學業上一起經歷這兩年，一起修課，一起寫作業，一起接受嚴厲考試的試煉;在生活互相砥礪，在研究中有討論的同伴，一起經歷了美好的日子。還有感謝實驗室所有學長姐和學弟妹們所給予我實驗室的新鮮有活力的研究風氣。還要感謝我的家人，我的努力的動力，我不敢忘記家裡的需要與父母的辛苦，是你們讓我能有美好的環境，有機會挑戰自我的理想。

最後感謝新竹，感謝交大，感謝那些幫助我關心我的人。

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Chapter 1

Introduction

1.1 UWB CMOS Receivers

UWB (Ultra Wideband) is a new wireless technology capable of transmitting data over a wide frequency bands with low power and high data rates. It communicates with short pulses on the order of nanoseconds, thus spreading the energy of the radio signal over a very wide bandwidth. Compared to traditional narrow band communication systems, UWB technology has the promising ability to provide high data rate at low cost with relatively low power consumption. The FCC has allocated 7.5 GH_Z of spectrum for unlicensed use of UWB devices in the 3.1 to 10.6 GH_Z frequency band. The low noise amplifier needs to amplify the received UWB signal with sufficient gain and as little as possible. From Shannon's equation C = B log $(1+=\frac{BSo}{BNo})$ for the channel capacity, we know that a UWB wireless network, the bandwidth will likely be much higher than the data rate, so that the system can operate at very low signal to noise ratio[1].

The majority implementation of the RF integrated circuit used for wireless devices are encounter with various possibilities: CMOS, Bi CMOS, and GaAs MESFET, bipolar (BJT), hetero-junction bipolar transistor (HBT), and PHEMT, etc,.

We just focus on the CMOS technology, CMOS process reduce the minimum channel length from the present years, so the unity gain cut off frequency (f_t) is increasing. For example, a deep sub-micron prototype CMOS technology has realized devices with f_t exceeding 100 GHz [2] and minimum noise figures less than 0.5-dB at 2 GHz. The more commercially available sub-micron CMOS technologies have display f_t's of 20GHz and minimum noise figures of 1.6-dB at 2 GHz [3]. The VLSI capabilities of CMOS make it proper to very high levels of mixed signal radio integration while increasing the functionality of a single chip radio to cover multiple RF standards [4]. Due to the advancement of circuit design technology, circuit size is small and cost down consideration. With low cost and low power devices of RF front-end system implemented by CMOS technology, the prospect of a single chip CMOS system has received considerable interest. Even the SOC is difficult and hard to implement at this time, but a set of separate chips in the same CMOS technology may bring significant economic benefits [5].

1.2 motivation

For portable wireless communication devices has given great push to the development of a next generation of low power radio frequency integrated circuits (RFIC) product. Such as wireless phones, cordless and cellular, global positioning satellite (GPS), pagers, wireless modems, wireless local area network (LAN), and RF ID tags, etc., require more low cost, low noise and high power efficiency solutions to supply the demand for low-price product [6].

Chapter 2 discusses the basic concepts in RF design. Chapter 3 presents the basic low-noise amplifiers design for UWB. Chapter 4 discusses the design procedures of this circuit by using of the band pass filter , the current buffer configuration, the shunt-LC resonance, Current-Reused Technique to get a good input and output matching, broadband, a low power consumption, and also reveals the simulations and the measurements .The last chapter, Chapter 5 is the summary.

Chapter 2

Basic Concepts in RFIC Design

2.1 Noise Sources in MOSFETs

2.1.1 Drain Current Noise

There are three main sources which contribute the thermal noise of MOSFETs [7]. And the dominate noise source of RF MOSFETs is the drain current noise which is expressed as:

$$\overline{i_{nd}^2} = 4KT\gamma g_{d0}\Delta f \tag{2.1}$$

where g_{d0} is the drain-source conductance at zero V_{DS}. The coefficient γ has a vale of unity at zero V_{DS} and, in long channel devices, decrease toward a value of 2/3 in saturation [8]. Some measurements show that short-channel devices exhibit noise considerably in excess of values predicted by long-channel theory, sometimes by an order of magnitude in extreme cases. Some of the literature attributes this excess noise to carrier heating by the large electric fields commonly encountered in such devices. In this view, the high fields produce carriers with abnormally high energies. No longer in quasi-thermal equilibrium with the lattice, these hot carriers produce abnormal amount of noise. But in contrast to other groups, we find only a moderate enhancement of the drain current noise for short-channel MOSFETs by our good

measurements.

2.1.2 Substrate Thermal Noise

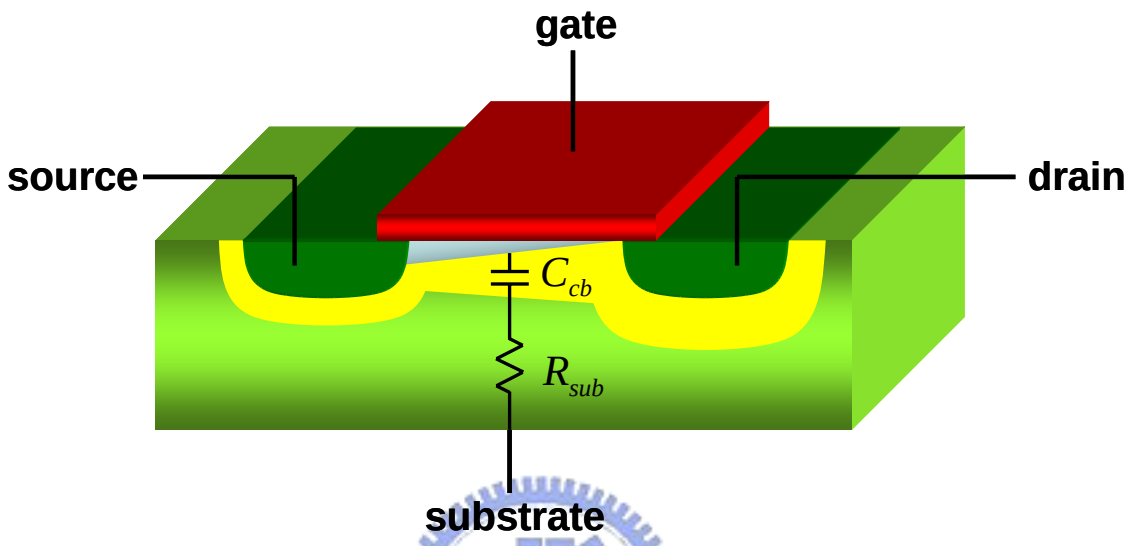


Figure 2-1 Substrate thermal noise

Figure 2-1 shows a simplified picture of how the thermal noise associated with the substrate resistance can produce measurable effect at the main terminals of the devices. At frequencies low enough that we may ignore C_{cb} (open), the thermal noise of R_{sub} modulates the potential of the back gate, contributing some noisy drain current:

$$\overline{i_{nd,sub}^2} = 4KTR_{sub}g_{mb}^2\Delta f \qquad (2.2)$$

Depending on bias conditions – and also on the magnitude of the effective substrate resistance and size of the back-gate transconductance – the noise generated by this mechanism may actually exceed the thermal noise contribution of

the ordinary channel charge. In this regime, layout strategies that reduce the substrate resistance have a noticeable and beneficial effect on noise.

At frequencies well above the pole formed by C_{cb} and R_{sub}, however, the substrate thermal noise becomes unimportant, as is readily apparent from inspection of the physical structure and the corresponding frequency-dependent expression for the substrate noise contribution [8]:

$$\overline{i_{nd,sub}^2} = \frac{4KTR_{sub}g_{mb}^2}{1+(\omega R_{sub}C_{cb})^2}\Delta f \qquad (2.3)$$

The characteristics of many IC processes are such that this pole is often around 1 GHz. Excess noise produced by this mechanism consequently will be most noticeable below about 1 GHz.

2.1.3 Drain Induced Gate Noise

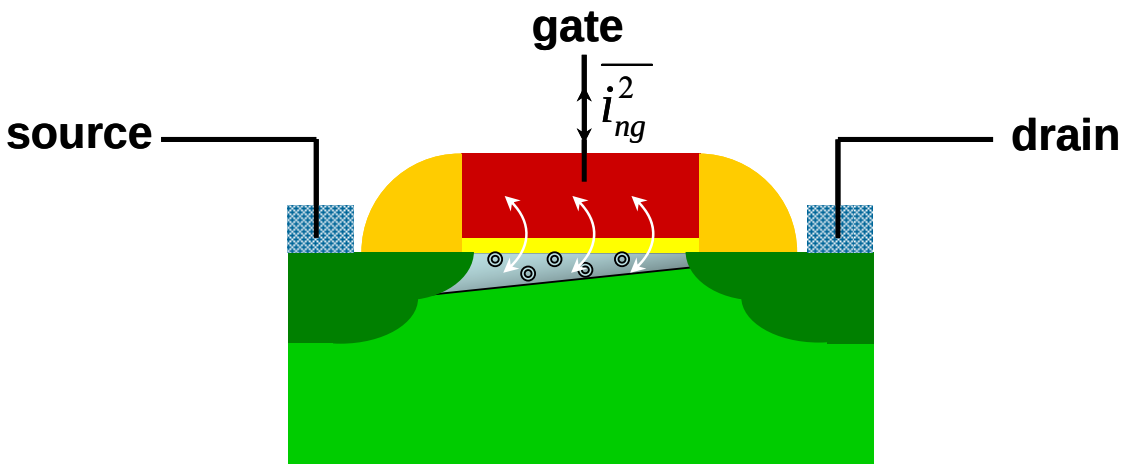


Figure 2.2 Drain induced gate noise

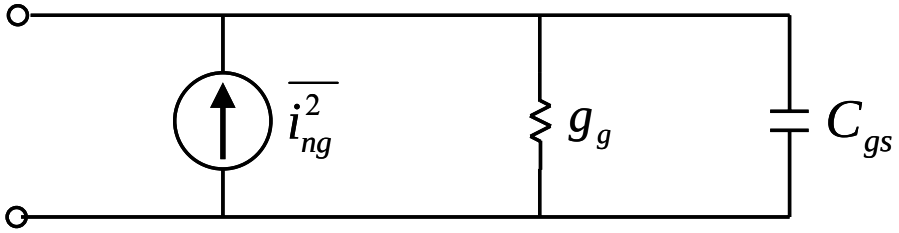


Figure 2.3 Equivalent circuits

In addition to drain noise, the thermal agitation of channel charge has another important consequence: gate noise. The fluctuating channel potential couples capacitively into the gate terminal, leading to a noisy gate current (see Figure 2-2). Noisy gate current may also be produced by thermally noisy resistive gate material. But this noise source will be separately discussed later, even though it is more and more important in nano-scale devices. Although the drain-induced-gate-noise is negligible at low frequencies, it can dominate at radio frequencies. Van der Ziel has shown that the drain-induced-gate-noise may be expressed as:

$$\overline{i_{ng}^2} = 4KT\delta g_g \Delta f \tag{2.4}$$

where the parameter g_g is:

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{2.5}$$

Van der Ziel gives a value of 4/3 (twice γ) for the gate noise coefficient, δ, in long channel devices [8].

The circuit model for the drain-induced-gate-noise is a conductance

connected between gate and source, shunted by a noise current source (see Figure 2-3). This noise current clearly has a spectral density that is not constant. In fact, it increases with frequency, so perhaps it ought to be called “blue noise” to continue the optical analogy. Because the drain thermal current noise and the drain-induced-gate-noise do share a common origin, they are correlated. That is, there is a component of the gate noise current that is proportional to the drain noise current on an instantaneous basis.

Although the noise behavior of long-channel devices is fairly well understood, the precise behavior of δ and γ in the short-channel regime is still unknown at present. That’s why we have to do more research on the thermal noise of MOSFETs. Thermal noise of deep sub-micrometer MOSFETs has received considerable attention lately, which is mainly triggered by publications that report a severe enhancement of the thermal noise with respect to long-channel theory [9]-[10]. In the earliest of these publications [9], thermal noise was found to be enhanced by a factor up to 12 in n-channel devices with 0.7μm gate length and hot electrons were proposed to explain these results. Evidently, the reported noise enhancements would seriously limit the viability of RF CMOS and a detailed study is called for. Therefore, in this paper, we perform an extensive study of the RF noise in 0.18μm RF CMOS technology.

2.2 Noise Analysis

2.2.1 The Concept of Noise Figure

Noise is usually generated by the random motions of charges or charge carriers in devices and materials. Because the noise process is random, one cannot identify a specific value of voltage at a particular time, and the only recourse is to characterize the noise with statistical measures, such as the mean-square or root-mean-square values. Because of having various noise sources in the circuit, we need to simplify calculation of the total noise at the output [11]. Obviously, the output-referred noise does not allow a fair comparison of the performance of different circuits because it depends on the gain. According the circuit theory, we can use the input-referred noise of circuits to represent the noise of behavior in the circuits.

The signal-to-noise ratio (SNR), defined as the ratio of the signal power to the total noise power, is an important parameter. In RF circuit, most of the front-end receiver blocks are characterized in terms of their "noise figure" rather than the input-referred noise. Noise figure has many different definitions. The most commonly accepted definition is

$$\text{noise figure} = \frac{SNR_{in}}{SNR_{out}}, \tag{2.6}$$

Noise figure is a measure of how much the SNR degrades as the signal passes through a circuit. If a circuit has no noise source, the $SNR_{out} = SNR_{in}$, regardless of the gain.

Noise added by electronics will be directly added to the noise from the

input. Thus, for reliable detection, the previously calculated minimum detectable signal level must be modified to include the noise from the active circuitry. Noise from the electronics is described by noise factor *F*, which is a measure of how much the signal-to-noise ratio is degraded through the system. We note that

$$S_o = G \cdot S_i \tag{2.7}$$

where S_i is the input signal power, S_o is the output signal power, and G is the power gain S_o/S_i. We derive the following equation for the noise factor:

$$F = \frac{SNR_i}{SNR_o} = \frac{S_i/N_{i(source)}}{S_o/N_{o(total)}} = \frac{N_{0(total)}}{G \cdot N_{i(source)}} \tag{2.8}$$

where $N_{o(total)}$ is the total noise at the output. If $N_{o(source)}$ is the noise at the output originating at the source, and $N_{o(added)}$ is the noise at the output added by electronic circuitry, then we can write:

$$N_{o(total)} = N_{o(source)} + N_{o(added)} \tag{2.9}$$

Noise factor can be written in several useful alternative forms:

$$F = \frac{N_{o(total)}}{G \cdot N_{i(source)}} = \frac{N_{o(total)}}{N_{o(source)}} = 1 + \frac{N_{o(added)}}{N_{o(source)}} \tag{2.10}$$

This shows that the minimum possible noise factor, which occurs if the electronics add no noise, is equal to 1.Noise figure NF is related to noise factor *F* by

$$NF = 10 \log_{10} F \tag{2.11}$$

Thus, while noise factor is at least 1, noise figure is at least 0 dB. In other words,

an electronic system that adds no noise has a noise figure of 0 dB.

In the receiver chain, for components with loss (such as switches and filters), the noise figure is equal to attenuation of the signal. For example, a filter with 3 dB of loss has a noise figure of 3 dB. This is explained by noting that output noise is approximately equal to input noise, but signal is attenuated by 3 dB. Thus, there has degradation of SNR by 3 dB [12].

2.2.2 Linearity in RF Circuits

Mathematically, any nonlinear transfer function can be written as series expansion of power terms unless the system contains memory. While many RF circuits can be approximated with a linear model to obtain their response to small signals, nonlinearities often lead to interesting and important phenomena. For simplicity, we assume that:

$$v_{out} = k_0 + k_1 v_{in} + k_2 v_{in}^2 + k_3 v_{in}^3 + \dots \qquad (2.12)$$

One common way of characterizing the linearity of a circuit is called the two-tone test. In this test, an input consisting of two sine waves is applied to the circuit.

$$v_{in} = v_1 \cos \omega_1 t + v_2 \cos \omega_2 t = X_1 + X_2 \qquad (2.13)$$

When this tone is applied to the transfer function given in (2.12), the result is a

number of terms:

$$v_0 = k_0 + \underbrace{k_1\left(X_1 + X_2\right)}_{desired} + \underbrace{k_2\left(X_1 + X_2\right)^2}_{\text{sec } ond \ \ order} + \underbrace{k_3\left(X_1 + X_3\right)^3}_{third \ \ order} \tag{2.14}$$

$$\begin{aligned} v_0 = & k_0 + k_1\left(X_1 + X_2\right) + k_2\left(X_1^2 + 2X_1X_2 + X_2^2\right) \\ & + k_3\left(X_1^3 + 3X_1^2X_2 + 3X_1X_2^2 + X_1^2\right) \end{aligned} \tag{2.15}$$

These terms can be further broken down into various frequency components. For instance, the X_1^2 term has a zero frequency (dc) component and another at the second harmonic of the input:

$$X_1^2 = \left(v_1 \cos \omega_1 t\right)^2 = \frac{v_1^2}{2}\left(1 + \cos 2\omega_1 t\right) \tag{2.16}$$

The second-order terms can be expands as follows:

$$\left(X_1 + X_2\right)^2 = \underbrace{X_1^2}_{dc+HD2} + \underbrace{2X_1X_2}_{IM2} + \underbrace{X_2^2}_{dc+HD2} \tag{2.17}$$

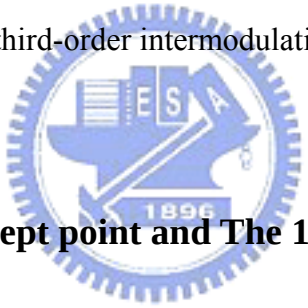
where second-order terms are composed of second harmonics HD2, and mixing components, here labeled IM2 for second-order intermodulation. The mixing components will appear at the sum and difference frequencies of the two input signals. Note also that second-order terms cause an additional dc term to appear.

The third-order terms can be expanded as follows:

$$\left(X_1 + X_2\right)^3 = \underbrace{X_1^3}_{FUND+HD3} + \underbrace{3X_1^2X_2}_{IM3+FUND} + \underbrace{3X_1X_2^2}_{IM3+FUND} + \underbrace{X_2^3}_{FUND+HD3} \tag{2.18}$$

Third-order nonlinearity results in third harmonics HD3 and third-order intermodulation IM3. Expansion of both the HD3 and IM3 terms shows output signals appearing at the input frequencies. The effect is that third-order nonlinearity can change the gain, which is seen as gain compression. This is summarized in Table 2.1.

Note that in the case of an amplifier, only the terms at the input frequency are desired. Of all the unwanted terms, the last two at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are the most troublesome, since they can fall in the band of desired output if ω_1 is close in frequency to ω_2 and therefore cannot be easily filtered out. These two tone are usually referred to as third-order intermodulation terms (IM3 products)



2.2.3 Third-Order Intercept point and The 1-dB Compression Point

One of the most common ways to test the linearity of a circuit is to apply two signals at the input, having equal amplitude and offset by some frequency, and plot fundamental output and intermodulation output power as function of input power as show in Figure 2-5. From the plot, the *third-order intercept point* (IP3) is determined. The third-order intercept point is a theoretical point where the amplitudes of the fundamental tones at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are equal to the amplitudes of the fundamental tones at ω_1 and ω_2.

From Table 2.1, if $v_1 = v_2 = v_i$, then the fundamental is given by

$$\text{fund}= k_1 v_i + \frac{9}{4} k_3 v_i^3 \tag{2.19}$$

The linear component of (2.19) given by

$$\text{fund}= k_1 v_i \tag{2.20}$$

can be compared to the third-order intermodulation term given by

$$\text{IM3}= \frac{3}{4} k_3 v_i^3 \tag{2.21}$$

The small v_i, the fundamental rise linearity (20dB/decade) and that the IM3 terms rise as the cube of the input (60dB/decade). A theoretical voltage at which these two tones will be equal can be defined:

$$\frac{\frac{3}{4} k_3 v_{IP3}^3}{k_1 v_{IP3}} = 1 \tag{2.22}$$

This can be solved for v_{IP3} :

$$v_{IP3} = 2\sqrt{\frac{k_1}{3k_3}} \tag{2.23}$$

That (2.23) gives the input voltage at the third-order intercept point. The input power at this point is called the *input third-order intercept point* (IIP3). If IP3 is specified at the output, it is called the *output third-order intercept point* (OIP3).

The third-order intercept point cannot actually be measured directly, since by the time the amplifier reached this point, it would be heavily overloaded. Therefore,

it is useful to describe a quick way to extrapolate it at a given power level. Assume that a device with power gain *G* has been measured to have an output power of P_1 at the fundamental frequency and a power of P_3 at the IM3 frequency for a given input power of P_i, as illustrated in Figure 2-5. On a log plot of P_3 and P_1 versus P_i, the IM3 terms have a slope of 3 and the fundamental terms have a slope of 1. Therefore,

$$\frac{OIP\ 3 - P_1}{IIP\ 3 - P_i} = 1 \tag{2.24}$$

$$\frac{OIP\ 3 - P_3}{IIP\ 3 - P_i} = 3 \tag{2.25}$$

since subtracation on a log scale amounts to division of power.

Also note that

$$G = OIP3 - IIp3 = P_1 - P_i \tag{2.26}$$

These equations can be solved to given

$$IIP3 = P_1 + \frac{1}{2}[P_1 - P_3] - G = P_i + \frac{1}{2}[P_1 - P_3] \tag{2.27}$$

In addition to measuring the IP3 of a circuit, the 1-dB compression point (Figure 2-4) is another common way to measure linearity. This point is more directly measurable than IP3 and requires only one tone rather than two. The 1-dB compression point is simply the power level, specified at either the input or the output, where the output power is 1dB less than it would have been in an ideally linear device. It is also marked in Figure 2-5[12].

2.3 Cascaded Nonlinear Stages

Since in RF systems, signals are processed by cascaded stages, it is important to know how the nonlinearity of each stage is referred to the input of the cascade. Consider two nonlinear stages in cascade, as shown in Figure2-6. Assuming that the input-output relationship is

$$y_1(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.28}$$

$$y_2(t) = \beta_1 y_1(t) + \beta_2 y_1^{\,2}(t) + \beta_3 y_1^{\,3}(t) \tag{2.29}$$

Substitute (2.28) into (2.29) results in the relation

$$y_2(t) = \alpha_1\beta_1 x(t) + (\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^{\,3}\beta_3)x^3(t) \tag{2.30}$$

If we consider only the first- and third-order terms, then

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1\beta_1}{\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^{\,3}\beta_3}\right|} \tag{2.31}$$

From equation (2.31) can be simplified if the two sides are inverted and squared:

$$\frac{1}{A^2_{IP3}} = \frac{1}{A^2_{IP3,1}} + \frac{3\alpha_2\beta_2}{2\beta_1} + \frac{\alpha_1^{\,2}}{A^2_{IP3,2}}, \tag{2.32}$$

where $A_{IP3,1}$ and $A_{IP3,2}$ represent the input IP_3 points of the first and second stages, respectively. From the above result, we note that as α_1 increases, the overall IP_3 decreases. This is because with higher gain in the first stage, the second stage senses larger input levels, thereby producing much greater IM_3 products [13].

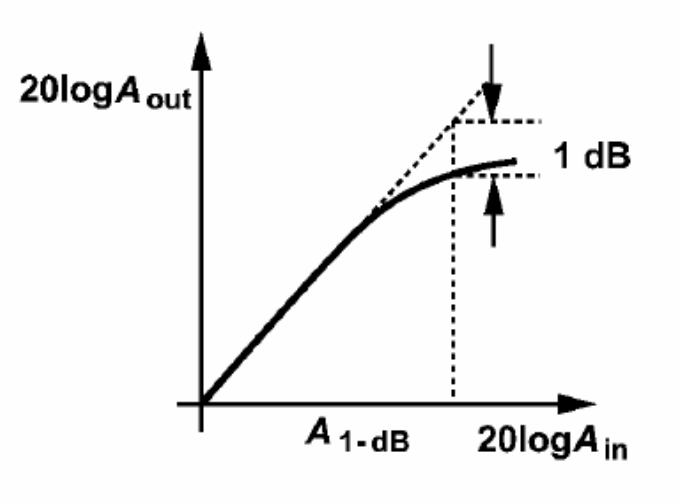


Figure 2-4 Definition of the 1-dB compression point

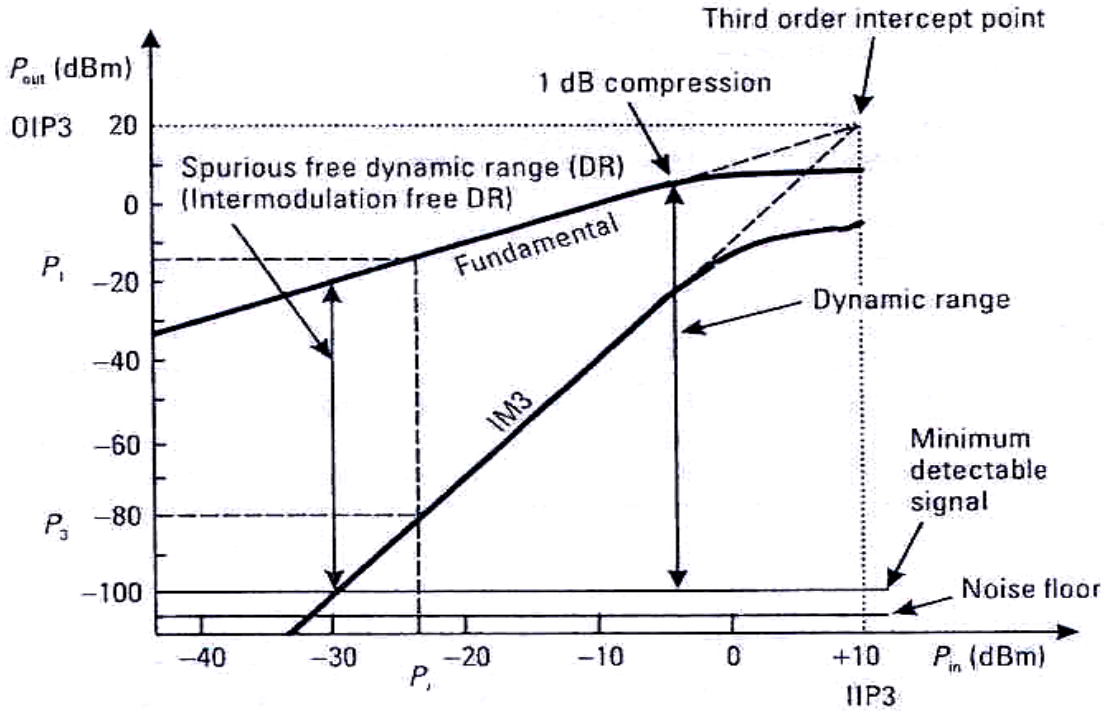


Figure 2-5 Plot of input output power of fundamental and IM3 versus input power.

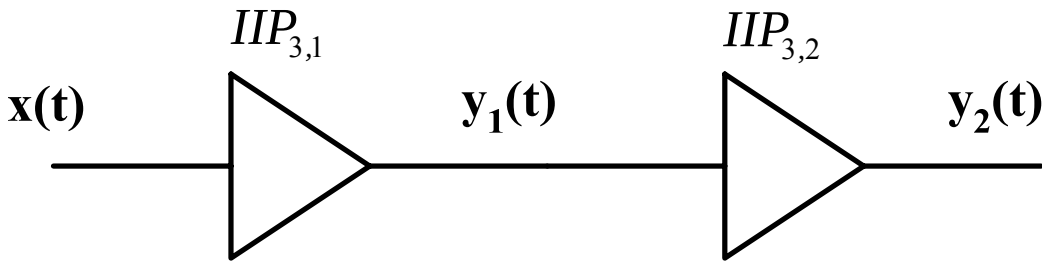


Figure 2-6 Cascaded nonlinear stages

Table 2.1

Frequency	Component Amplitude
dc	$k_0 + \frac{k_2}{2}\left(v_1^2 + v_2^2\right)$
ω_1	$k_1 v_1 + k_3 v_1\left(\frac{3}{4}v_1^2 + \frac{3}{2}v_2^2\right)$
ω_2	$k_1 v_2 + k_3 v_2\left(\frac{3}{4}v_2^2 + \frac{3}{2}v_1^2\right)$
$2\omega_1$	$\frac{k_2 v_1^2}{2}$
$2\omega_2$	$\frac{k_2 v_2^2}{2}$
$\omega_1 \pm \omega_2$	$k_2 v_1 v_2$
$\omega_2 \pm \omega_1$	$k_2 v_1 v_2$
$3\omega_1$	$\frac{k_3 v_1^3}{4}$
$3\omega_2$	$\frac{k_3 v_2^3}{4}$
$2\omega_1 \pm \omega_2$	$\frac{3}{4}k_3 v_1^2 v_2$
$2\omega_2 \pm \omega_1$	$\frac{3}{4}k_3 v_1 v_2^2$

Chapter 3

General Consideration in LNA Circuit Design

3.1 Low Noise Amplifier Basic

Low noise amplifier is the first gain stage in the receive path so its noise figure directly adds to that of the system. Therefore, there are several common goals in the design of LNA. These include minimizing noise figure of the amplifier, providing enough gain with sufficient linearity and providing a stable 50 ohm input impedance to terminate an unknown length of transmission line which delivers signal from antenna to the amplifier [9]. Among LNA architectures, inductive source degeneration is the most popular method since it can achieve noise and power matching simultaneously, as shown in Figure 3-1. The following analysis in 3.2 is based on this architecture. The LNA basic considerations are introduced as follows.

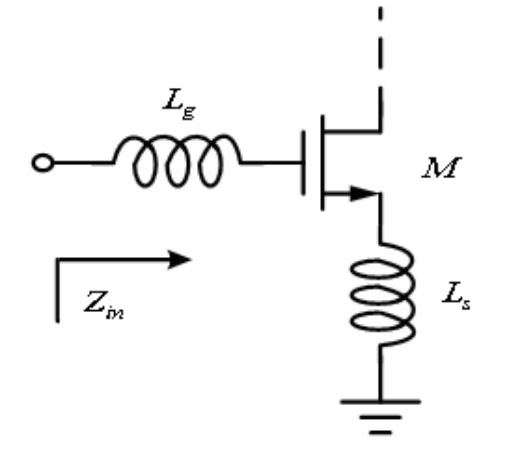


Figure 3-1 Common-source input stage with inductive source degeneration.

3.1.1 Impedance Matching Network

The need for impedance matching network becomes more important. In order to deliver maximum power to a load, it must be properly terminated at both the input and the output ports. The input impedance of a circuit can be any values in order to have the best power transfer into the circuit. It is necessary to match this impedance to the impedance of the source driving the circuit. The output impedance also must be similarly matched in order to deliver maximum power to the 50 ohm load, it must have the terminations Z_S and Z_L. The input matching network is designed to transforms the generator impedance to the source impedance Z_S, and the output matching network transforms the 50 ohm termination to the load impedance Z_L. Consider the RF system shown in Figure 3-2. Here the source and load terminations are 50ohm, as the transmission lines leading up to the circuit for optimum power transfer, prevention of ringing and radiation, and good noise behavior. For example, we needs the circuit input and output impedances matched to the system. In general, some matching circuit must almost always be added to the circuit, as shown in Figure 3-3. Typically, reactive matching circuits are used because they are lossless, adding no noise to the circuit, and will only be matched over a range of frequencies and not at others. If a broadband matching is required, then other techniques may need to be used. An example of matching a transistor amplifier with a capacitive input is shown

in Figure 3-4. The series inductance adds an impedance of $j\omega L$ to cancel the input capacitive impedance. Note that, in general, when the impedance is complex $(R + jX)$, then to match it, the impedance must be driven from its complex conjugate $(R - jX)$.

The input, output impedance of a circuit is very common in using reactive components to achieve impedance transformation, as they will not absorb any power or add any noise. Thus, series or parallel inductance or capacitance can be added to the circuit to provide an impedance transformation. Series components will move the impedance along a constant resistance circle on the Smith Chart. Parallel components will move the admittance along a constant conductance circle. Table 3.1 summarizes the effect of each component.

With the proper choice of two reactive components, any impedance can be moved to a desired point on the Smith Chart. There are eight possible two-components matching networks, also known as Ell networks, as shown in Figure 3-5. Each will have a region in which a match is possible and a region in which a match is not possible.

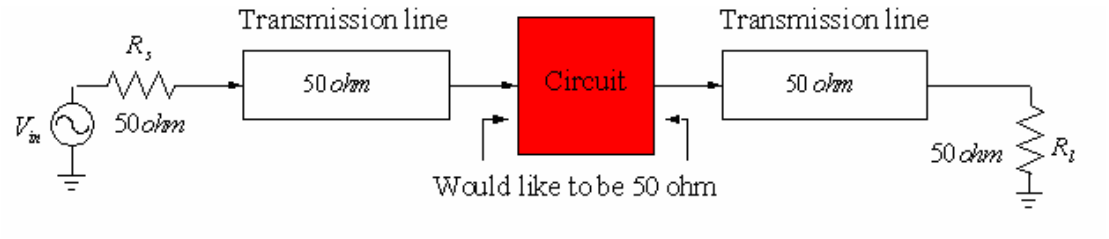


Figure 3-2 Circuit embedded in a 50 ohm system

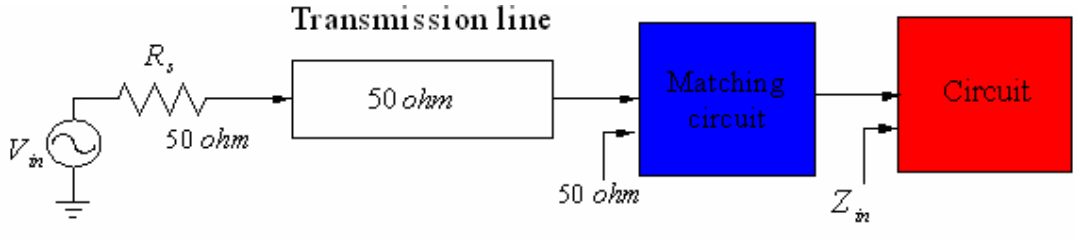


Figure 3-3 Circuit embedded in a 50 ohm system with matching circuit

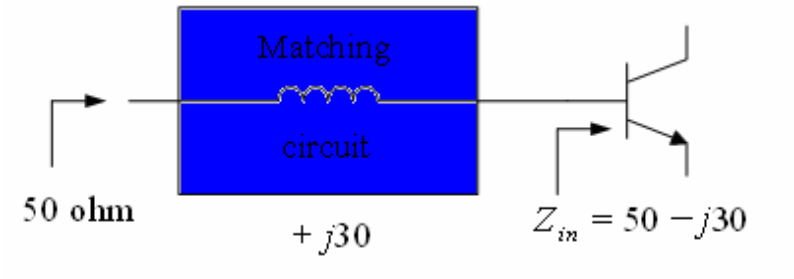


Figure 3-4 Example of a very sample matching circuit network

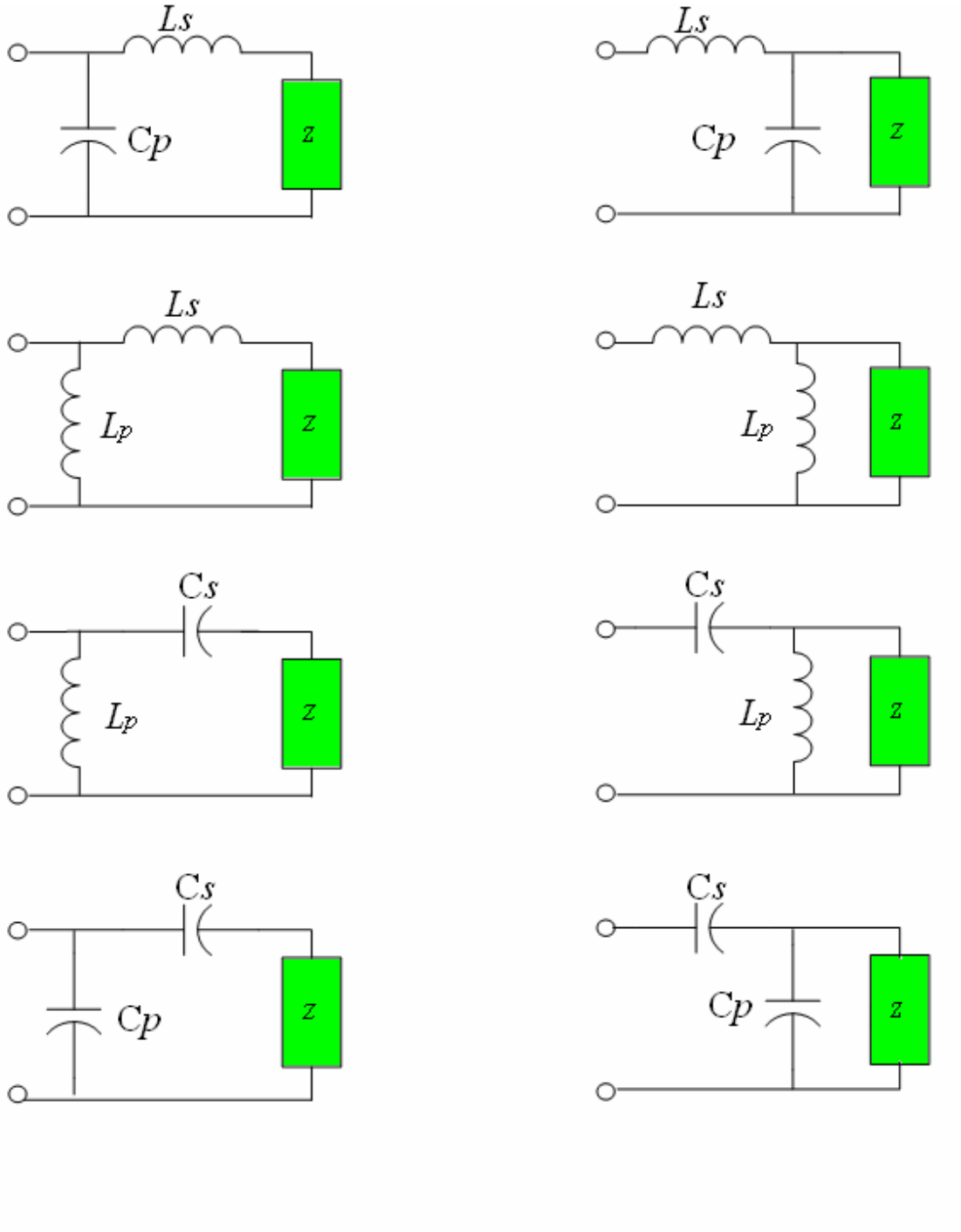


Figure 3-5The eight possible impedance-matching networks with two reactive components

Table 3.1

Component Added	Effect	Description of Effect
Series inductor	$z \rightarrow z + j\omega L$	Move clockwise along a resistance circle
Series capacitor	$z \rightarrow z - j/\omega C$	Smaller capacitance increases impedance $(-j/\omega C)$ to move counterclockwise along a conductance circle
Parallel inductor	$y \rightarrow y - j/\omega L$	Smaller inductance increases admittance $(-j/\omega L)$ to move counterclockwise along a conductance circle
Parallel capacitor	$y \rightarrow y + j\omega C$	Move clockwise along a conductance circle

3.1.2 Stability

The stability of an amplifier is a very important consideration in a design and can be determined from the S parameters, the matching networks, and the terminations. A two-port network to be unconditionally stable can be derived from (3.1) to (3.4) .

$$\left|\Gamma_s\right| < 1 \tag{3.1}$$

$$\left|\Gamma_L\right| < 1 \tag{3.2}$$

$$\left|\Gamma_{IN}\right| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| < 1 \tag{3.3}$$

$$\left|\Gamma_{OUT}\right| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_S}\right| < 1 \tag{3.4}$$

The two-port network is shown in Figure 3-6. For unconditional stability any passive load or source in the network must produce a stable condition. The solution of (3.1) to (3.4) gives the required conditions for the two-port network to be unconditionally stable [4].

$$k = \frac{1 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2 + \left|\Delta\right|^2}{2\left|S_{12}S_{21}\right|} \tag{3.5}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.6}$$

A convenient way of expressing the necessary and sufficient conditions for

unconditional stability is $k > 1$ (3.7)

$$|\Delta| < 1 \tag{3.8}$$

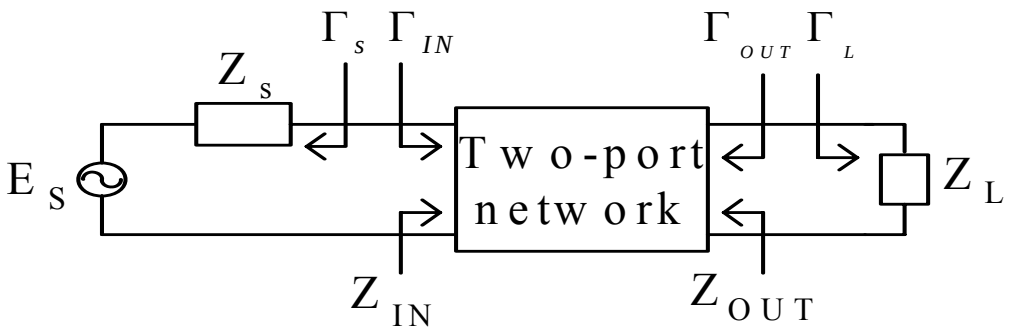


Figure 3-6 Stability of two-port networks

3.2 Low Noise Amplifier Architecture Analysis

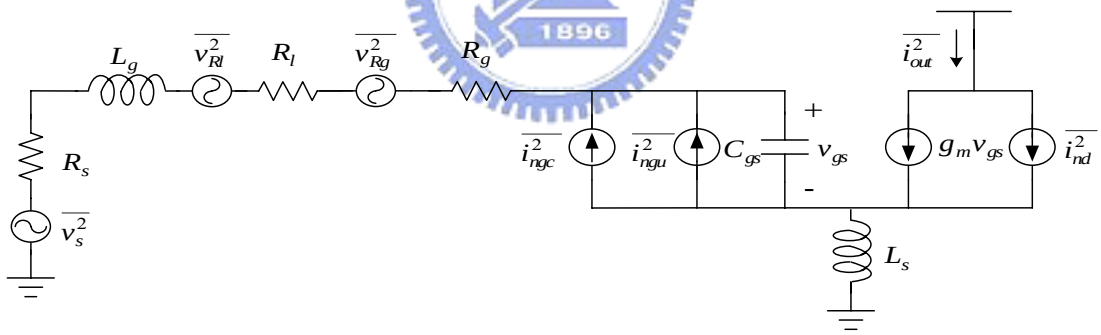


Figure 3-7 Equivalent noise model of Figure 3-1

In Figure 3-7, the input impedance can be expressed as

$$\begin{aligned} Z_{in} &= s(L_g + L_s) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \\ &= \left(\frac{g_m}{C_{gs}}\right)L_s \approx \omega_T L_s \quad at \quad \omega = \omega_o = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \end{aligned} \tag{3.9}$$

as shown in equation (3.9), the input impedance is equal to the multiplication of cutoff

frequency of the device and source inductance at resonant frequency. Therefore it can be set to 50 ohm for input matching while resonant frequency is designed to be equal to the operating frequency.

According to prior introduction, the equivalent noise model of common-source LNA with inductive source degeneration can be expressed as Figure 3-7, where R_l is the parasitic resistance of the inductor and R_g is the gate resistance of the device. Note that the overlap capacitance C_{gd} has also been neglected in the interest of simplicity. Then the noise figure can be obtained by computing the total output noise power and output noise power due to input source. To find the output noise, we first evaluate the trans-conductance of the input stage. With the output current proportional to the voltage no C_{gs} and noting that the input circuit takes the form of series-resonant network, the transconductance at the resonant frequency can be expressed as

$$G_m = g_m Q_{in} = \frac{g_m}{\omega_o C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{2\omega_o R_s} \tag{3.10}$$

where Q_{in} is the effective Q of the amplifier input circuit. So the output noise power density due to the source can be expressed as

$$S_{a,Rs}(\omega_o) = S_{Rs} G_{m.eff}^2 = \frac{4kT\omega_T^2}{\omega_o^2 R_s (1 + \frac{\omega_T L_s}{R_s})^2} \tag{3.11}$$

In the similar way, the output noise power density due to R_g and R_l is

$$S_{a,R_g,R_l}(\omega_o) = \frac{4kT(R_g + R_l)\omega_T^2}{\omega_o^2 R_s^2 (1 + \frac{\omega_T L_s}{R_s})^2} \tag{3.12}$$

Furthermore, channel current noise of the device is the dominant noise contributor, and its noise power density associated with the correlated portion of the gate noise can be expressed as

$$S_{a,i_{nd},i_{ngc}}(\omega_o) = \frac{4kT\gamma\kappa g_{do}}{(1 + \frac{\omega_T L_s}{R_s})^2} \tag{3.13}$$

where γ is the coefficient of channel thermal noise, $\alpha = g_m / g_{d0}$ and

$$\kappa = \frac{\delta\alpha^2}{5\gamma}|c|^2 + \left[1 + |c|Q_L\sqrt{\frac{\delta\alpha 2}{5\gamma}}\right]^2 \tag{3.14}$$

$$Q_L = \frac{1}{\omega_o R_s C_{gs}} \tag{3.15}$$

The last noise term is the contribution of the uncorrelated portion of the gate noise, and its output noise power density can be expressed as

$$S_{a,i_{ngu}}(\omega_o) = \frac{4kT\gamma\xi g_{do}}{(1 + \frac{\omega_T L_s}{R_s})^2} \tag{3.16}$$

where

$$\xi = \frac{\delta\alpha^2}{5\gamma}(1 - |c|^2)(1 + Q_L^2) \tag{3.17}$$

According to equations (3.11), (3.12), (3.13) and (3.16), the noise figure at the resonant frequency can be expressed as

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma\chi}{\alpha Q_L}\left(\frac{\omega_o}{\omega_T}\right) \tag{3.18}$$

where

$$\chi = 1 + 2 \mid c \mid Q_L \sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L^2) \tag{3.19}$$

From equation (3.19), we observe that χ includes the terms which are constant, proportional to Q_L, and proportional to Q_L^2. It follows that equation (3.19) will contain terms which are proportional to Q_L as well as inversely proportional to Q_L. A minimum noise figure, therefore, exits for a particular Q_L.

Chapter 4

UWB CMOS LNA Design

4.1 Design Procedures

This architecture is for an Ultra-Wideband CMOS LNA with Current-Reused Technique for 3.1 to 10.6 GH_Z. It has an advantage of high gain, low power consumption, low noise performance and small size. We utilize three-stage amplifier to get a flat gain at high frequency. The first stage introduces the band pass filter for input matching, it includes two inductances, one capacitor and one inductance at gate. The second stage introduces a current-reuse cascaded common-sources structure to lower power consumption. The last stage introduces LC in shunt connection to improve gain and bandwidth for high frequency. The current buffer configuration is used for output matching. Its circuit diagram is shown in Figure 4.1 and chap layout is shown in Figure 4-2.

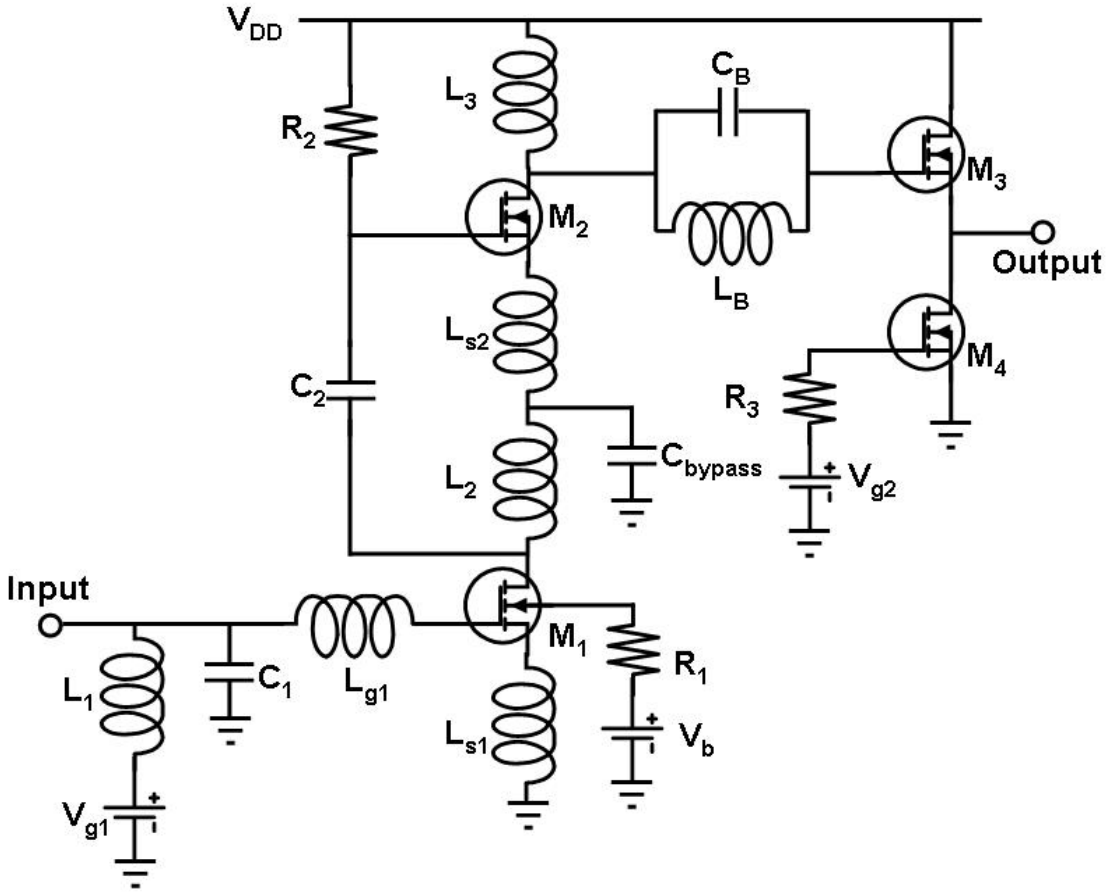


Figure 4-1 Circuit diagram

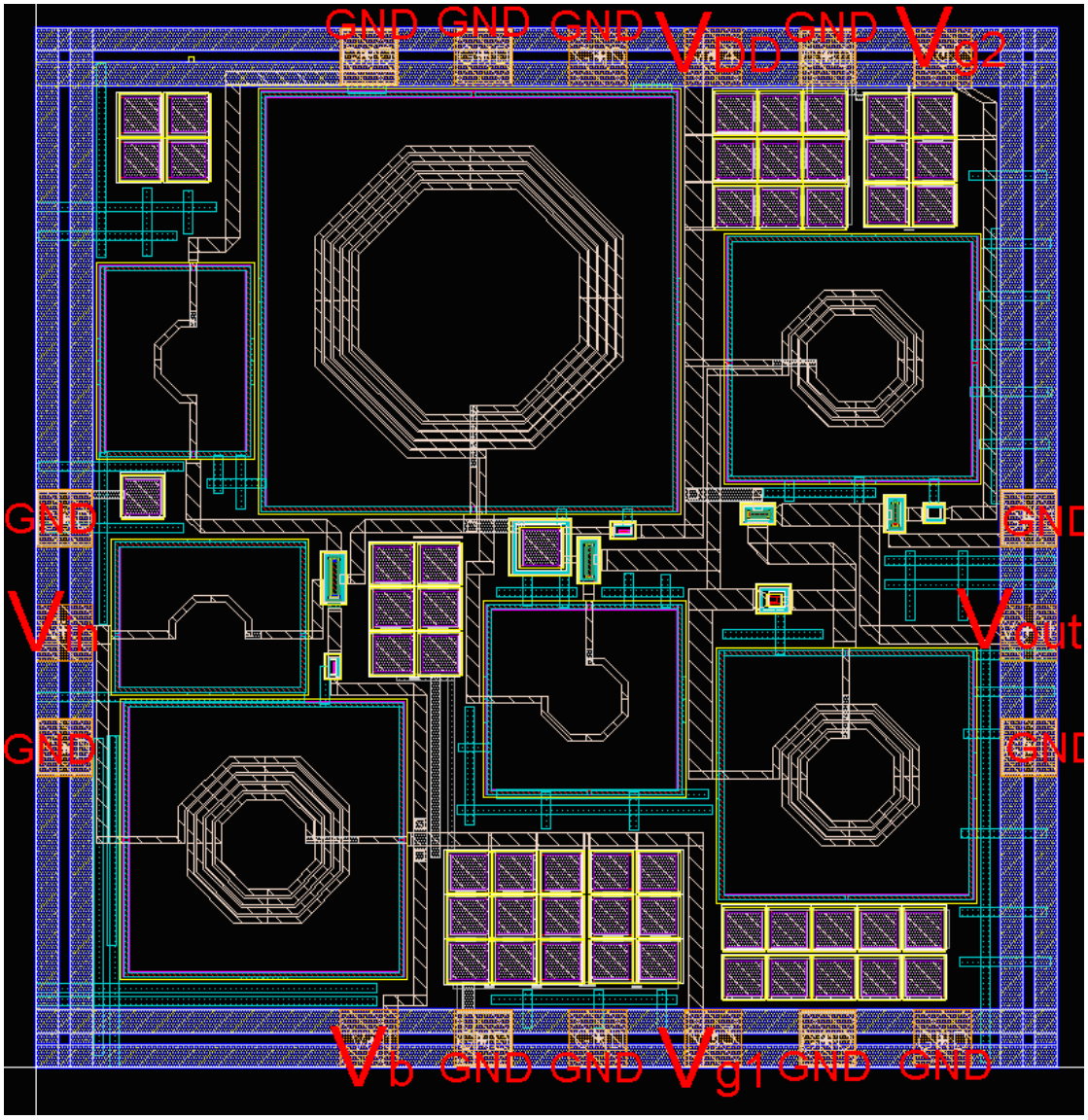


Figure 4-2 Chip layout

4.1.1 Analysis of Input Matching

In input part, we adopt a common-source amplifier, by introducing matching components to let the frequency resonate at which we want. We also simplify the first stage as in Figure 4-3, and the circuit can be viewed form point A to the right, we get the impedance Z_1 in equation (4.1).

$$Z_1 = \frac{1}{sC_{gs1}} + s(L_{g1} + L_{s1}) + \frac{g_{m1}}{C_{gs1}} L_{s1} \tag{4.1}$$

In addition, we put a shunt-LC resonance in input part, following with the equivalent circuit Z_1, to make it have a good resonance in the imagine part, and get real part impedance-matching $(R_s = g_{m1}L_{s1}/C_{gs1})$ at the same time. Form figure 4-4 we can get the input matching impedance Z_{in} in equation (4.2).

$$Z_{in} = \frac{(sL_2 // \frac{1}{sC_2})Z_1}{(sL_2 // \frac{1}{sC_2}) + Z_1} \tag{4.2}$$

We can also keep a very low noise to procure a band-pass amplifier for an entire Ultra-Wideband.

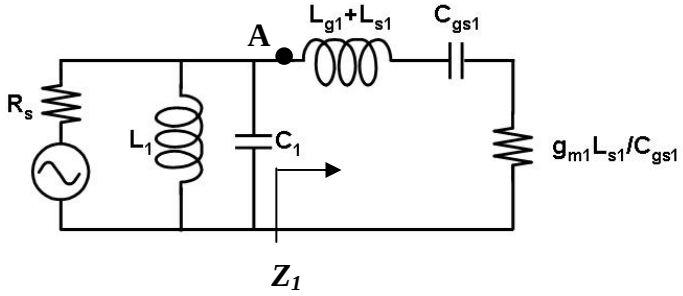


Figure 4-3 simplification of the first stage

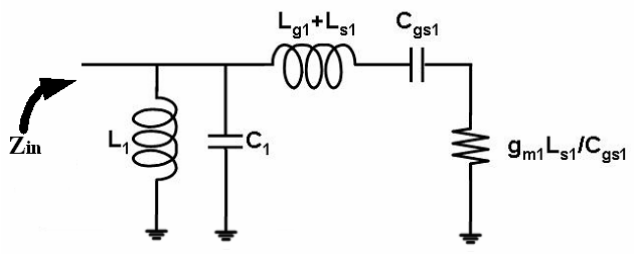


Figure 4-4 the input impedance Z_{in}

4.1.2 Analysis of Output Matching

The current buffer configuration is used for output matching as shown in Figure4-5，and make the entire frequency matching to 50 Ω.In this circuit, M_3 is the source follower, and the steady current of M_3 is provided by M_4.We only need to control the supply voltage and the size of the transistor, and then a good output matching will be obtained as equation below.

$$Z_{out} = \frac{1}{g_{m3}} \| r_{o4} \approx \frac{1}{g_{m3}} \tag{4.3}$$

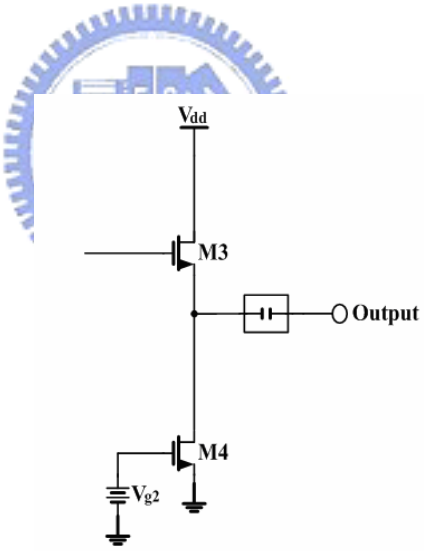


Figure 4-5 the current buffer

4.1.3 Gain Analyzing

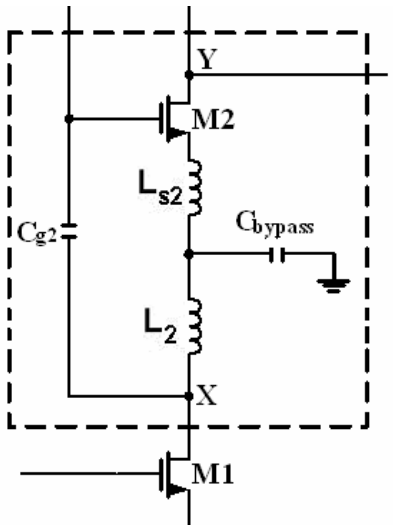


Figure 4-6 Current-reused two stage cascade amplifier with series inter-stage resonance

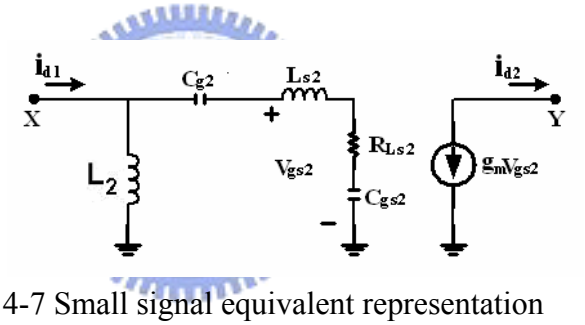


Figure 4-7 Small signal equivalent representation of the circuit from node X to Y

In Figure 4-6 is the Current-reused two stage cascade amplifier with series inter-stage resonance, and the Small signal equivalent representation of the circuit from node X to Y is in Figure 4-7. If we divide id2 to id1, we can get the gain as in equation (4.4).

$$\frac{id_2}{id_1} = \frac{g_{m2}}{sC_{gs2}} \times \frac{L_2}{L_2 + (1/sC_{g2} + 1/sC_{gs2}) + sL_{S2} + R_{LS2}} \tag{4.4}$$

so we can see that L_{S2} resonates with $1/sC_{g2} + 1/sC_{gs2}$ at high frequency

and. If L_2 provides high impedance, $L_2 >> R_{LS2}$ then, we can get $\frac{id_2}{id_1}$ as below.

$$\frac{id_2}{id_1} \cong \frac{g_{m2}}{sC_{gs2}} \cong \frac{\omega_T}{\omega} \tag{4.5}$$

where ω_T is M2's cutoff frequency, ω is the operation frequency.

4.1.4 Bandwidth Analyzing:

In order to get a low power consumption low noise amplifier LNA, we cascade the second amplifier M2 on the first amplifier M1 to use the same dc current to achieve the goal of power saving. Besides we also utilize substrate bias at M_1 to enhance the gain, at the same time reduce the power consumption.

For gain and the bandwidth, we utilize three-stage amplifier to achieve a high gain and the flat bandwidth design. In the circuit, the requirement of the current-reused structure is Coupling capacitor (C_2) which is connected to the output of the first stage amplifier (at drain) and also connected to the input of the stage second stage amplifier (at gate) .Therefore it can provide signal coupling between the two stages and the Bypass capacitor (C_{bypass}) functions as an ac ground at the source of transistor M2, for avoiding the coupling effect to the first stage. Aside from, we join the shunt-LC resonance C_B and L_B, by this LC resonance the bandwidth and the gain can be improve a lot in order to get a high gain Ultra-Wideband circuit. In Figure 4-8, we can see the gain combined by the three state amplifiers.

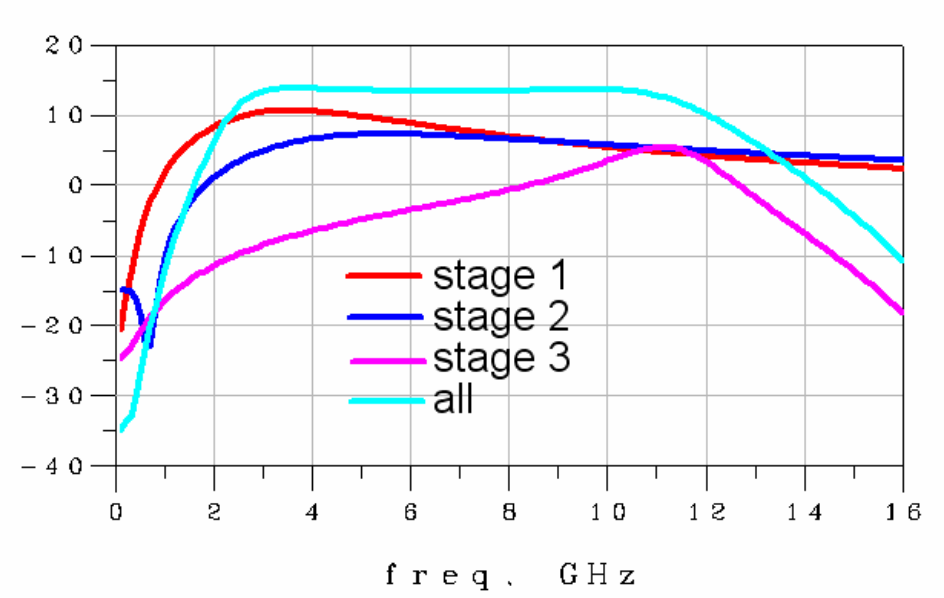


Figure 4-8 the gain of the circuit

4.2 Simulation Results

Figure 4-9 shows the Return loss Simulation. S11 is lower than -9.4dB between 3.1 and 10.6GHz. The output buffer achieves excellent matching such that S22 is lower than -11dB from 3.1GHz to 10.6 GHz in Figure 4-10. Figure 4-11 is the power gain versus frequency, the gain at 3.1GHz is 13.567dB and at 10.6GHz is 13.319, so the different between the wideband is only 0.25dB.The reverse isolation S21 is lower than -38dB shown in Figure 4-12. The noise figure (NF) of this UWB LNA is shown in Figure 4-13.The NF at 3.1GHz is 2.686dB, at 10.6GHz is 2.842dB and the minimum noise figure (NFmin) at 5.7GHz is 2.146dB. The stability factor (MuPrime1, Mu1) both are greater than 1, implying that have a stable circuit in Figure

4-14.The third-order intermodulation distortion(IIP3) is -3dBm and shown in Figure 4-15 ,the test is performed at 4 GHz. These results imply excellent linearity of our LNA. The proposed UWB LNA dissipates 10.3mW with a power supply of 1.8V.

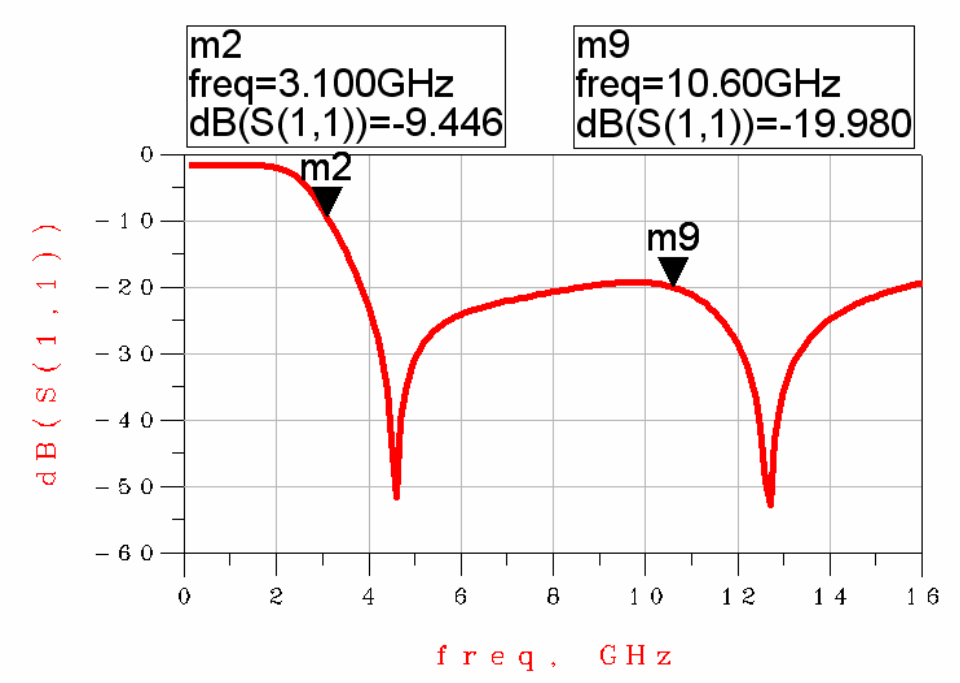


Figure 4-9 Simulated S11

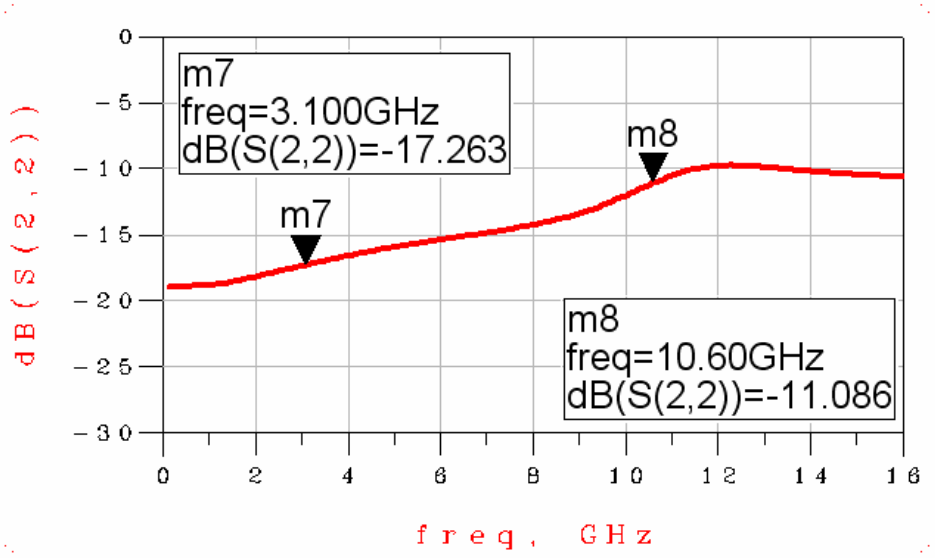


Figure 4-10 Simulated S22

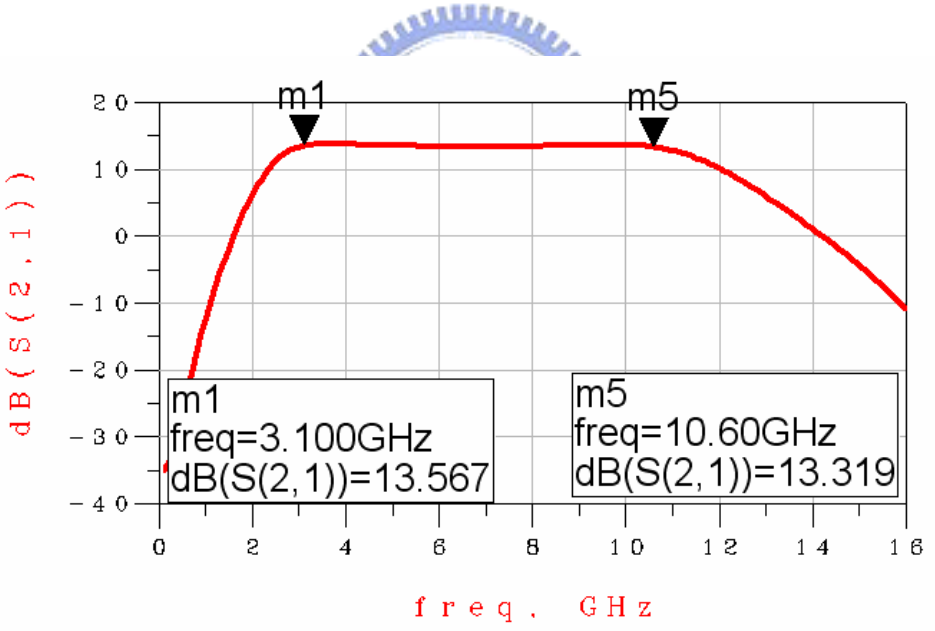


Figure 4-11 Simulated S21

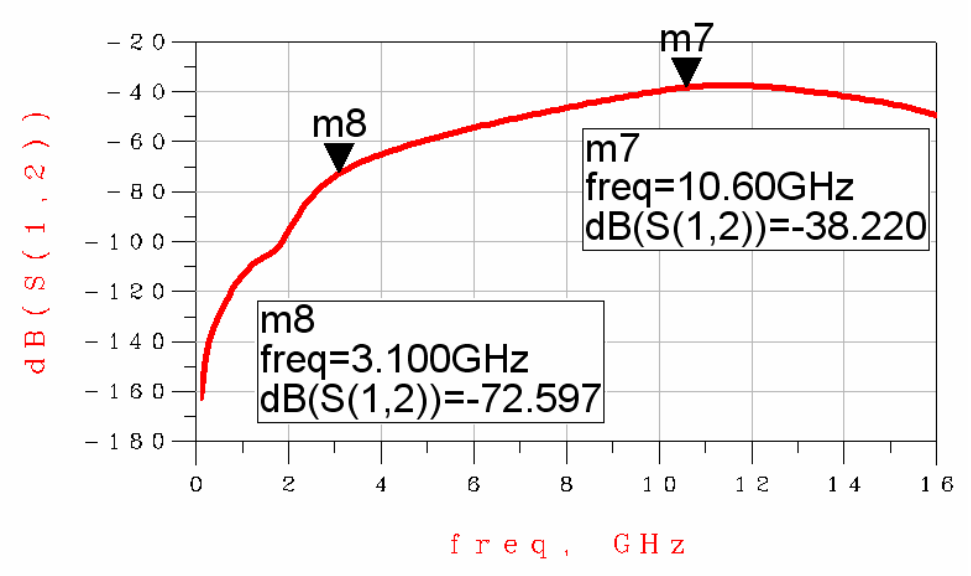


Figure 4-12 Simulated S12

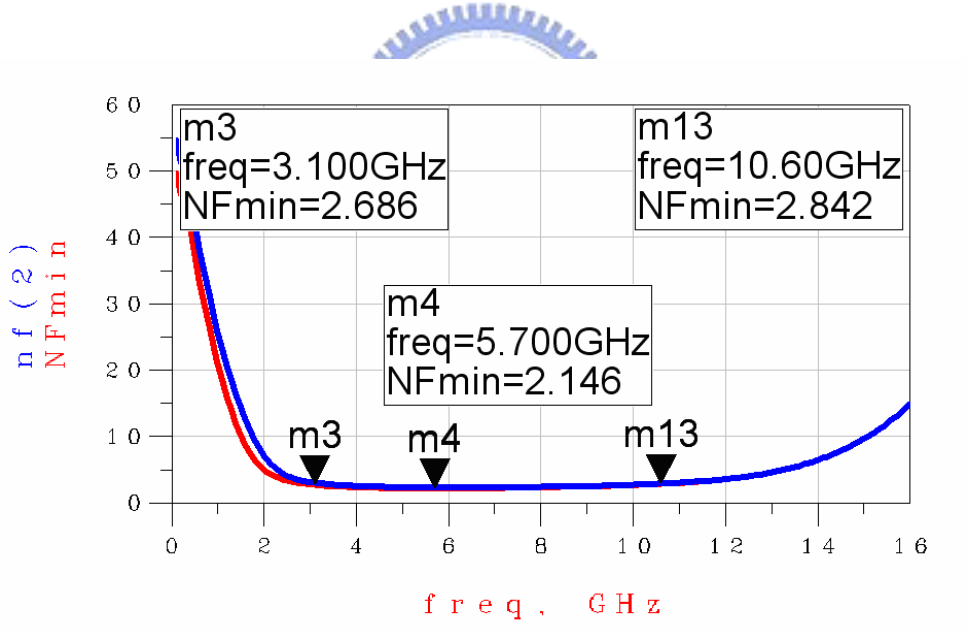
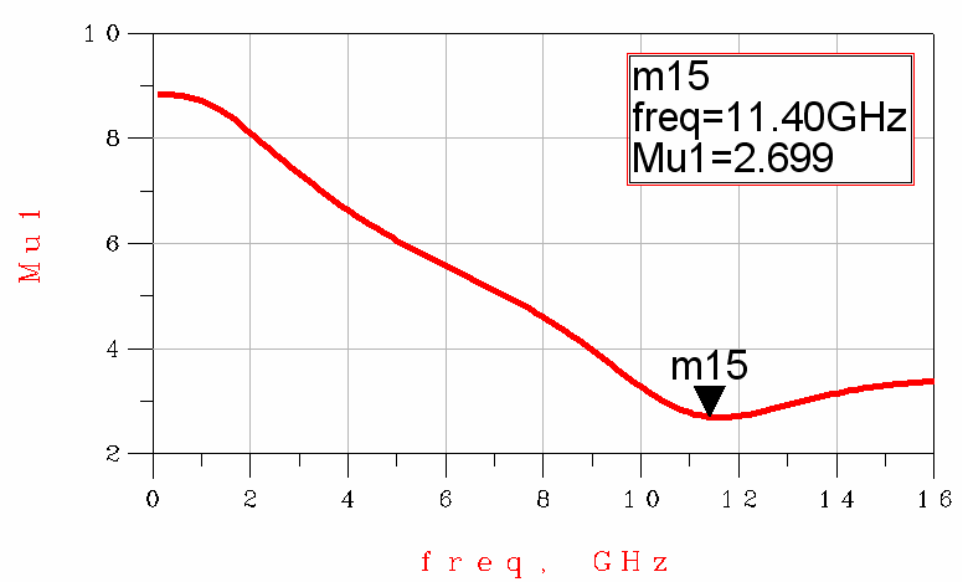


Figure 4-13 Simulated Noise Figure



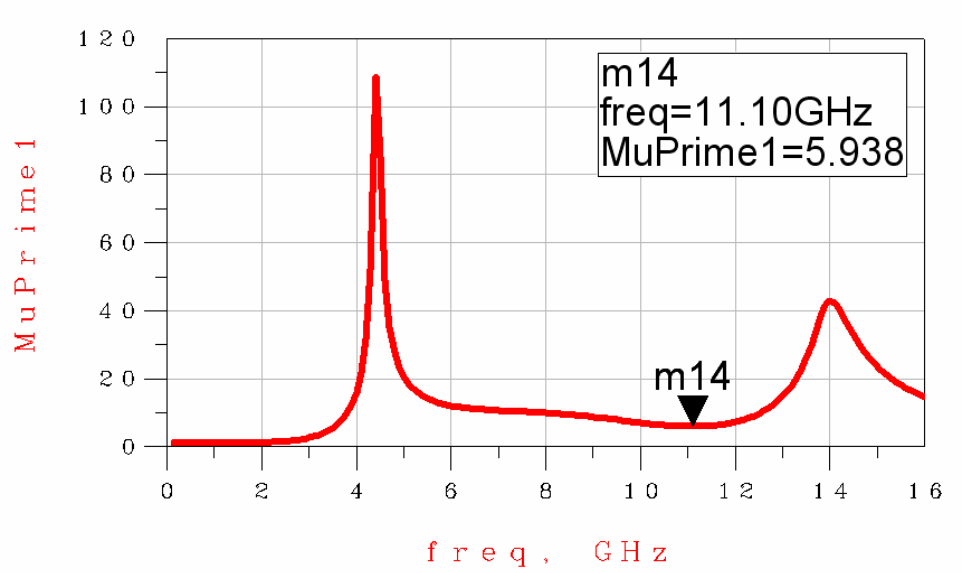


Figure 4-14 Simulated stability

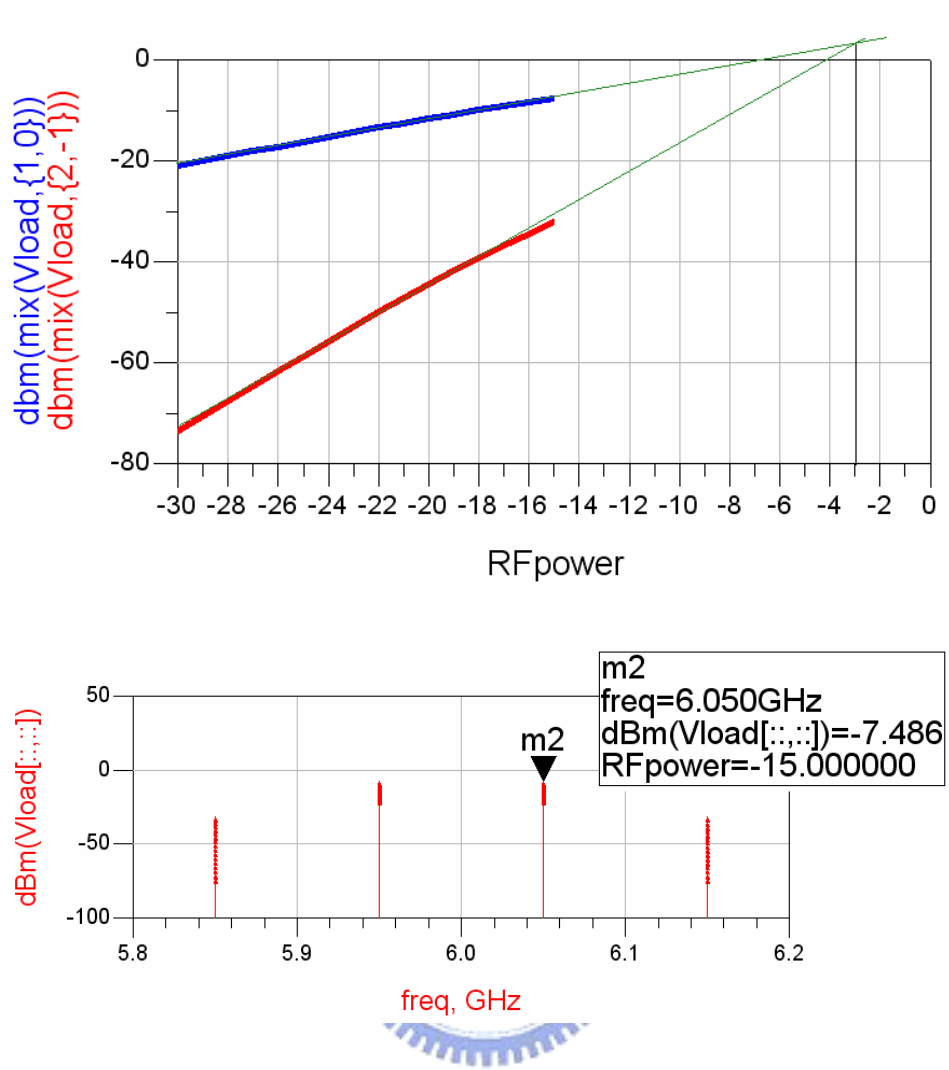


Figure 4-15 simulated IIP3

4.3 Measurements and Conclusions

The following Figure4-16 ~ Figure4-21 are the measurement result which are slightly different from simulation. Which imply good accuracy of simulation and good circuit design. But the gain dropping at high frequency (in Figure 4-16) is due to TSMC model at high frequency is not accurate.

The bandwidth of this work with considering matching and gain is from 3.1 to 10.6 GHz, while the average gain is about 10dB. Figure 4-17 and Figure 4-18 show the measurement results of S11 and S22. Input and output matching are achieved very well from 3.1 to 10.6 GHz, so S11 can bellow -9dB and the S22 can bellow -11dB.S12 below up to -33dB in Figure 4-19. The noise figure is about 3.6 shown in Figure 4-20.The noise performance is very flat and the minimum noise figure is 2.85dB at 5GHz. The noise figure can be better if we solve the resistor parasitic. The linearity of the third-order intermodulation distortion(IIP3) is -3dBm as measurement and shown in Figure 4-21. Figure 4-22 shows the die photo of this circuit. Total power consumption is 10.3 mW which the V_{dd} is 1.8V.In the chip, the apply V_b is 0.1V, V_{g1} is 0.61V and V_{g2} is 0.61V. Table 4.1 is the measurement result summary. By the band pass filter, the current buffer configuration, the shunt-LC resonance, Current-Reused Technique we proposed, a good input and output matching, broadband, a low power consumption LNA is developed for UWB system applications.

Figure 4-16 Measured S21

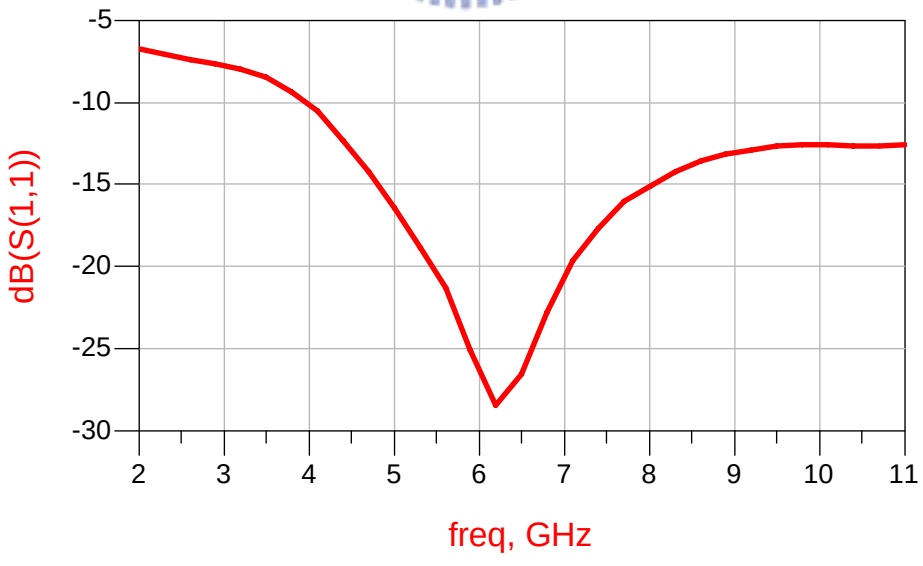


Figure 4-17 Measured S11

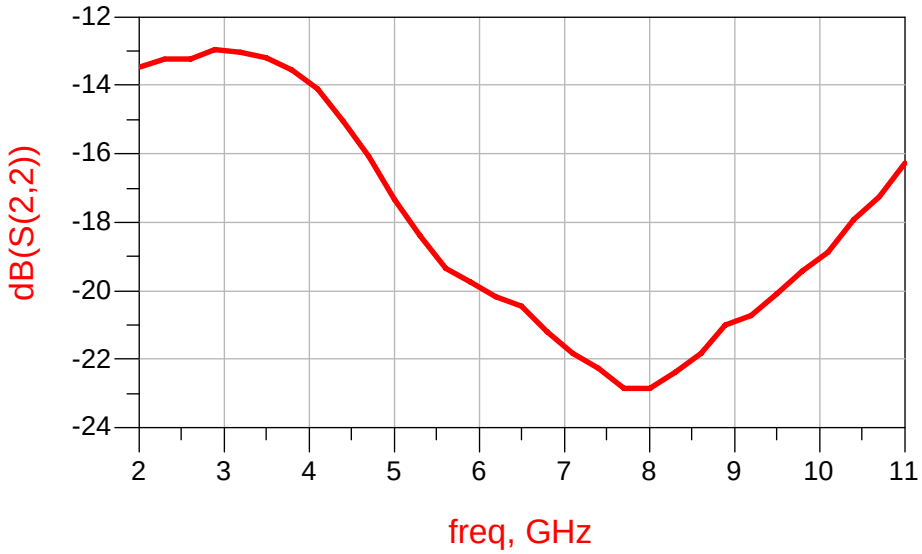


Figure 4-18 Measured S22

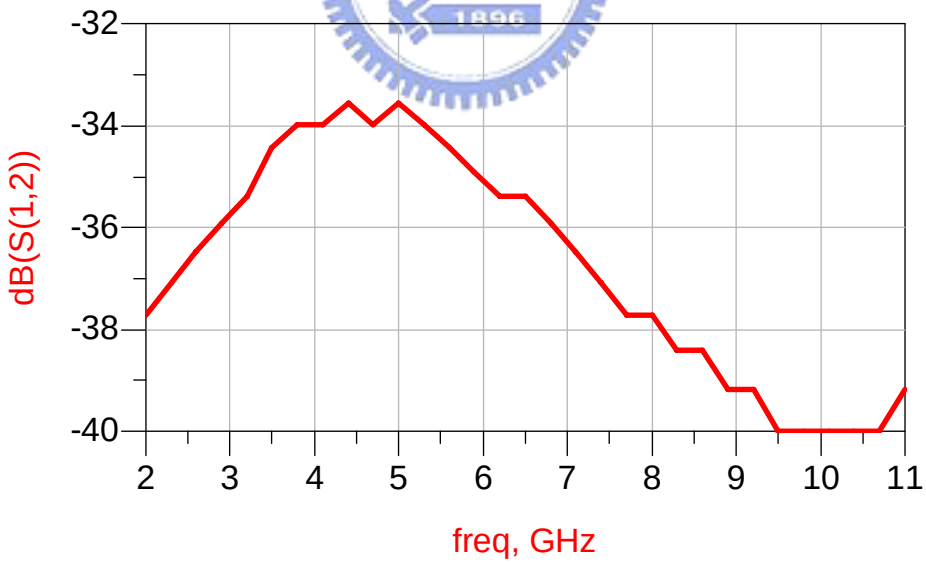


Figure 4-19 Measured S12

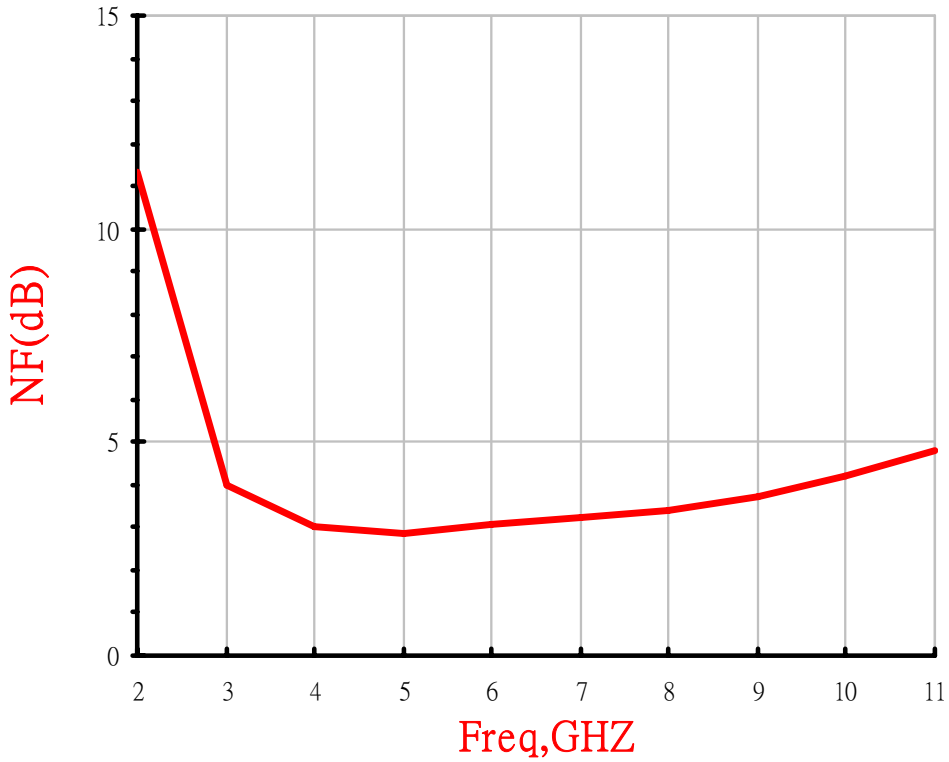


Figure 4-20 Measured noise figure

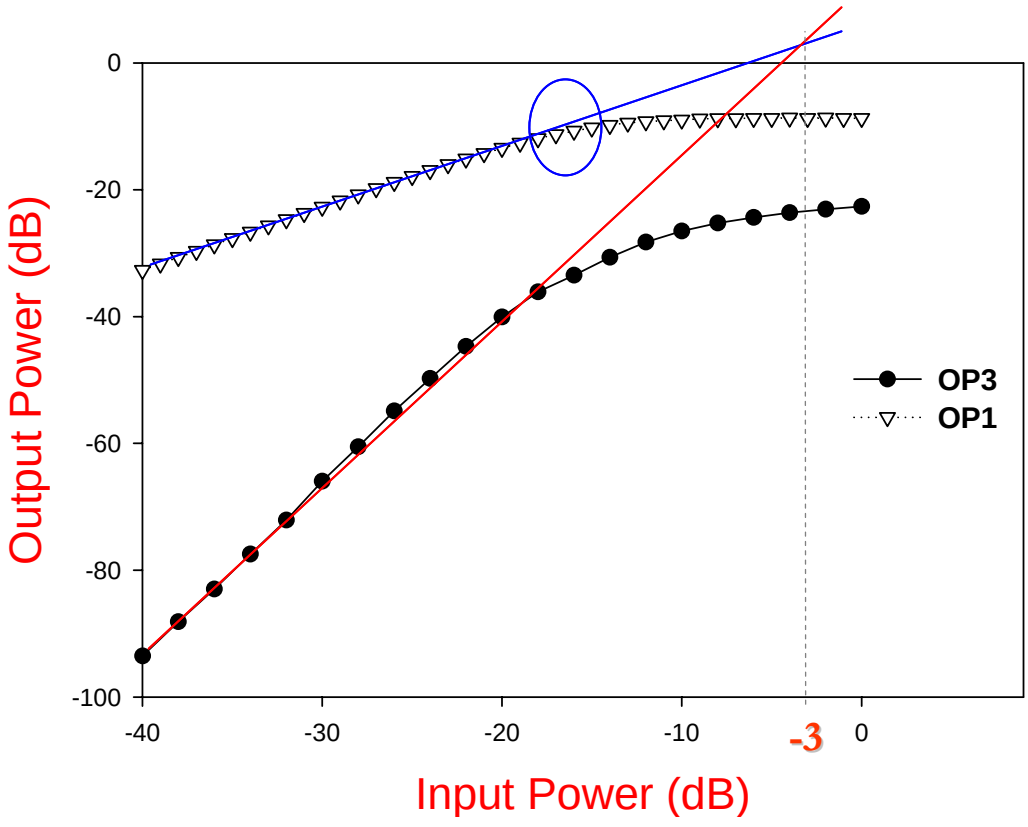


Figure 4-21 Measured linearity

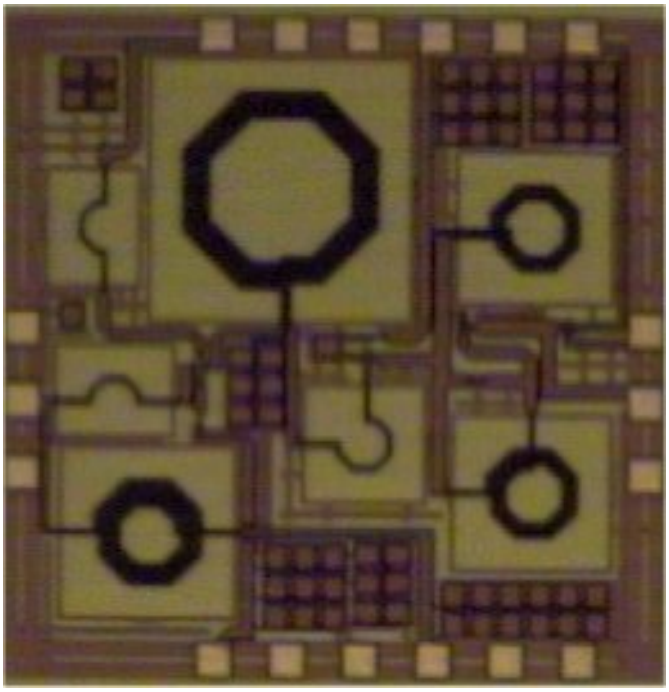


Figure 4-22 Die photo

B.W (GHz)	**Gain (dB)**	**NF (dB)**	**S11 (dB)**	**S22 (dB)**	**IIP3 (dBm)**	**Pdc (mW)**
3.1~10.6	10	3.6	< -9	< -13	-3	10.3

Table 4.1 Measured results summary

Chapter 5

Summary

By the Current-Reused Technique for 3.1 to 10.6GHz we proposed, a good input and output matching, broadband, a low power consumption amplifier is developed for UWB system applications.

Table 5.1 is the comparison of broadband LNA performance. We can find out by this table, by using Current-Reused Technique and shunt-LC resonance, can pull to being wide very big arrival 3.1~10.6GHz frequently. All the advantages are important for UWB system considerations.

specifications	This work	Ref. [14]	Ref. [15]	Ref. [16]	Ref. [17]
Process	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Frequency (GHz)	3.1~10.6	2.4~9.5	2~4.6	2~6.5	3.1~10.6
S_{11} (dB)	<-9	<-9	<-9	<-7.8	<-8
S_{22} (dB)	<-13	<-20	<-10	<-16	----
Gain (dB)	10	9.3	9.8	11.9	13.5~16
NF (dB)	2.85~4.5	4~9	2.3~6	4.1~4.6	3.1-6
IIP3 (dBm)	-3	-6.7	-7	4	-7
P_{diss} (total) (mW)	10.3	18	12.6*	27	11.9
Die size (mm^2)	0.89	1.1	0.9	0.88	1.2

Table 5.1 Comparison of broadband LNA performance (*Only core LNA)

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（95 年 9 月~97 年 6 月）

論文題目：

電流重複用之超寬頻金氧半低雜訊放大器應用於3.1-10.6GHz

An Ultra-Wideband CMOS LNA with Current-Reused Technique for 3.1 to 10.6GHz