國 立 交 通 大 學

電機學院微電子奈米科技產業研發碩士班

碩 士 論 文

氟鈍化效應在高介電常數複晶矽層間介電層特性及可靠度研究

Characteristics and Reliabilities Research of Fluorine Passivation Effect on Inter-Poly High-k Dielectrics

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摘要

根據半導體的微縮定律，隨著系統晶片（System on Chip, SOC）的半導體製造逐漸的微小化，持續降低 CMOS 元件中的閘極介電層及非揮發性記憶體(non-volatile memories)中的複晶矽層間介電層（inter-poly dielectric）厚度，以達到高元件密度及低操作電壓的趨勢。傳統的極薄二氧化矽介電層因量子穿遂效應而導致極大的直接穿遂漏電流，對整個元件產生了可靠度的問題。為了解決這嚴重的直接穿遂漏電流現象，本篇論文利用高介電常數材料（high-κ）來替換傳統的二氧化矽。因為高介電常數材料在相同的等效二氧化矽厚度之下，有較大的實際物理厚度可以抵擋因量子的穿遂效應而產生的直接穿遂漏電流。

但使用高介電常數材料仍有遭遇其它的缺點。例如:在相同的二氧化矽電壓下，高介電常數材料有較高的界面狀態產生及較多的電荷補捉，這對於元件操做時臨限電壓的漂移有嚴重的影響。本篇論文利用高介電常數材料做為堆疊式快閃記憶體(stacked-gate flash memory)的複晶矽層間介電層上的穿隧

介電層，並用氟摻雜的鈍化處理來討論對複晶矽層間電容的影響。在複晶矽層成長後以離子佈值的方式來植入氟摻雜，使氟原子在後續的高溫摻雜的活化過程中，使其擴散至複晶矽和複晶矽層間的高介電常數材料（high-κ）介電層。利用氟的摻入探討有機金屬化學氣相沉積(metal organic chemical vapor deposition)所成長的三氧化二鋁(Al_2O_3)和二氧化鉿(HfO_2) 來改進其可靠度和元件特性。

我們提出了以矽表面氟離子值入法(silicom surface fluorine implantation),將氟離子導入複晶矽和複晶矽層間的高介電常數材料（high-κ）介面處。從實驗結果可充份證明，含氟摻雜的元件有較低的界面狀態產生，和較少的電荷補抓，對三氧化二鋁和二氧化鉿複晶矽層間電容，不論是漏電流、電子補捉率、崩潰電場和崩潰電荷，及熱穩定度，複晶矽層間電容的特性都有顯著的提昇。本篇論文中，非揮發堆疊記憶體的懸浮閘(Floating Gate,FG) 和控制閘(Control Gate,CG) 最好的氟劑量條件分別為 5e13 cm^{-2} 和 5e15 cm^{-2}。對於元件的可靠度和穩定性有明顯的改善。因此，等效氧化層厚度為 5 奈米及 3 奈米的三氧化二鋁和二氧化鉿將是 45 奈米及 32 奈米世代以下堆疊式快閃記憶體的絕佳候選複晶矽層間介電質。

Characteristics and Reliabilities Research of Fluorine Passivation Effect on Inter-Poly High-k Dielectrics

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Abstract

According to the semiconductor scaling rule, for the semiconductor made of system on a chip (SOC) has become very little gradually, a continuously scaling of the gate dielectrics for complementary metal oxide semiconductor (CMOS) and inter-poly dielectrics (IPD) for electrically-erasable programmable read only memory (EEPROM) and stacked –gate flash memory is needed to achieve high density and low operation voltage trend. In tradition, the ultra-thin silicon dioxide (SiO_2) which the quantum effect and then cause more directly tunneling current, which is the issue of the reliability in all devices. In order to solve seriously directly tunneling current, this dissertation is to apply the high dielectric constant materials to replace SiO2. Because high dielectric constant materials compare with SiO2 at the same equivalent oxide thickness (EOT), have thicker physical thickness which can resist directly tunneling current from quantum effect.

But using the high dielectric constant materials still has experienced other problems. For example , high dielectric constant materials have higher interfacial states and charge traps, these will cause more serious threshold voltage shift when working device as the same voltage compare with SiO2.In this thesis, we used high-k materials serving as the IPDs and tunnel dielectrics (TDs) on the stacked-gate flash memories. The influence of fluorine passivation effects on IPD capacitance was investigated. At post-IPD deposition, we incorporate fluorine with fluorine implantation method which was subsequently diffused into the IPD and high-k materials of tunnel dielectrics. The objective of this dissertation was to apply the fluorine incorporation to discuss deposition aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) with metal organic chemical vapor deposition (MOCVD) for improving reliability and device characteristics.

We describe the characteristics of silicon surface fluorine implantation (SSFI) for IPD and high-k materials interface with incorporation of fluorine. By experimenting, we found that lower generation rate of interface states and lower charge trapping rate are observed for device with fluorine incorporated. For Al_2O_3 and HfO_2 inter-poly capacitors, the sample exhibits optimal quality in terms of leakage current, electron trapping rate, effective breakdown field and charge-to-breakdown (Q_{BD}) and the thermal stability of high temperature, the IPDs characteristics result of improving effect significantly. In this thesis, we investigated the most effective fluorine dosage condition respectively is 5e13cm^{-2} and 5e15cm^{-2} on floating gate, (FG) and control gate, (CG) of the non-volatile stacked –gate flash memory. Thus enhances the reliability and the stability of high-k devices. As thin as 5nm and 3nm equivalent oxide thickness (EOT) of Al_2O_3 and HfO_2 IPDs are suitable to meet the requirement of 45nm and 32nm generation stacked-gate flash memories respectively.

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CHAPTER 1

Introduction

1.1 Background

As the scaling rule keeps going, the dimension of gate oxide for complementary metal oxide semiconductor (CMOS) has decreased dramatically for the past decade. The integrated circuit technology nowadays makes devices with high density and low operation voltage for the system-on-chip (SOC) application. We want such requirements like high performance (speed), low static (off-state) power and a wide range of power supply and output voltages [1], The density of devices on silicon chip has been following the “Moore’s law”. It meant that doubling the circuit density about every two or three years since 1980 [2]-[4]. The density improvement combines ont only the progress in lithography but also the innovation in device fabrication technology. Form this trend results in a dramatic expansion in technology and communication markets including the market associated with high-performance microprocessor and low static-power applications, such as wireless systems. Because we knew, the key element of keeping the scaling rule of Si-based metal-oxide-semiconductor field effect transistor (MOSFET) going is the materials and resultant electrically properties associated with the dielectric employed to isolate the transistor gate from the Si channel for decades: silicon dioxide (SiO_2). We can benefit several key advantages in CMOS and memory processing including a

thermodynamically and electrically stable high-quality Si-SiO_2 interface as well as superior electrical isolation properties by using thermally grown amorphous SiO_2 as the gate dielectric. ~10^{10} cm^{-2} defect charge density, ~10^{10} $cm^{-2}eV^{-1}$ midgap interface state density and 15 MV/cm hard breakdown field are routinely obtained and therefore expected in spite of dimensions. These outstanding electrical properties clearly present a significant challenge for any other alternative gate dielectric candidates [5], [6].

Over the years, the industry' demand for greater integrated circuit functionality and performance for lower cost and increased circuit density, this has translated into a higher density of transistors on a wafer. So, there have been several major evolutions in silicon digital logic technology. The MOS technology, expecially CMOS technology became the most important digital logic technology for all IC industry, and silicon is the main semiconductor material[7].The scaling of oxide thickness has long been recognized as one of determinant factor for devices scaling. High driving current and thereby improved performance can be achieved by reducing the oxide thickness. At the current rate of progressing, Figure 1.1 show the scaling limits of various gate dielectrics trends from the published 2003-ITRS roadmap (International Technology Roadmap for Semiconductor). The imperative need for a nitrided oxide (SiO_xN_y) and high dielectric constant (κ) gate dielectrics for low standby power application after the year 2002 and 2006, respectively [8]. However, the direct tunneling current increases exponentially by about one order of magnitude for every 0.2nm ~ 0.3nm reduction in oxide thickness. This additional leakage current not only causes increased power dissipation but also affect the circuit functionality due to the decreased operation margins.

For this reason, several alternative materials for silicon dioxide are currently being investigated. Ultrathin nitrided oxides are, at this moment, the best choices to replace pure SiO_2 [9]-[15]. Figure 1.2 shows the expected equivalent oxide thickness (EOT) trends from the published 2004-ITRS roadmap. It indicated that nitrided oxides can extend SiO_2 limitation to 2006 without massive change in production technologies. Nitrided oxides have several properties superior to those of conventional thermal SiO_2, and it deserves to mention the suppression of boron penetration from the poly-Si gate and enhanced reliability. Nitrogen also reduces hot-electron-induced degradation [16]. The dielectric constant of the oxynitride increases linearly with the percentage of nitrogen from κ (SiO_2) = 3.9 to κ (Si_3N_4) = 7.8 [17], though one should note that most SiO_xN_y films grown currently by thermal methods are lightly doped with N (< 10 at.%) and therefore have a dielectric constant only slightly higher than that of pure SiO_2. The other potential candidates to replace silicon dioxide are high-κ materials, including aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) etc [18]-[21]. The most important advantage of high-κ dielectric is the several orders reduction of magnitude of leakage current compared to SiO_2 at the same EOT. However, in device performance point of view, a suitable gate dielectric candidate should also meet the other requirements, including high thermal stability, high carrier mobility, small oxide charges, good stress immunity and CMOS compatible.

On the other hand, high-κ dielectrics are paid much attention on the flash memory applications [22]-[28].The thickness of inter-poly dielectric (IPD) and tunnel dielectric (TD) in stacked-gate flash memory had met intrinsic limitation [29]. It is not sufficient to meet the stringent data retention requirement of IPD while applying thermal or CVD oxynitride technologies due to the unavoidable leakage current

[30]-[33]. By increasing the floating gate coupling ratio, high-κ IPD can lead to a high electric field across tunnel oxide (TOX) even at very low control gate voltage. For the tunnel dielectric engineering of stacked-gate flash memories, the issue is closely related to dielectric material selection itself. Flash tunnel dielectric has two roles. One is a barrier to suppress charge leakage under read and retention. Second role is a charge transfer path. In order to avoid trap-assisted tunneling via one trap site, the minimum TOX thickness of conventional FG structure will be limit to 8 nm. This limits the tunnel SiO_2 scaling and program/erase voltage reduction. Nitrided oxides have been intensively studied, but so far only 5 to 10 times improvement for low field leakage is achieved [34]. This is not enough, because it only achieves 1 nm reduction even with suit fluorine dosage.

Figure 1.4 shows the calculated band offsets for most high-k dielectrics. To successfully employ the high-κ IPD and TD into flash memory, one must take charge retention issues into consideration and make sure that the barrier height (φ_B) between Si and the new adopted high-κ dielectrics should be larger than 1.5eV for effectively suppressing the loss of floating gate charges through electron thermal emission [34]. Usually, dielectrics with higher κ inherently have lower φ_B. Therefore a trade-off between dielectric constant and barrier height is inevitably required in trying to implement the high-κ dielectrics in flash memories.

As the scaling of flash memories devices have developed, high-k dielectrics instead of conventional silicon dioxide or oxy-nitrides. Because high-k materials can maintain the same EOT in thicker physical thickness, therefore they can resist effectively for the direct-tunneling current to across the insulator and reduces the amount of off-state leakage current density [35].

The relationship between dielectrics constant and thickness is followed:

$$EOT = \frac{3.9 \times \varepsilon_o \times A}{C_m} \qquad \text{[eq-1]}$$

$$K_{high\text{-}k} = \frac{K_{ox} \times t_{high\text{-}k}}{EOT} \qquad \text{[eq-2]}$$

The continuing miniaturization of stacked-gate flash memory devices requires inter-poly dielectrics (IPD), the dielectrics constants (k) of which are larger than the conventional used silicon dioxide. Example of such high-k materials are aluminum oxide (Al_2O_3) [18], hafnium oxide (HfO_2) [36][37], zirconium oxide (ZrO_2) [38] [39], Table 1-1 summarizes the properties of potential high-k candidates.

Among high-k materials, HfO_2 and Al_2O_3 are the most promising candidates due to high k (HfO_2~25) and large band gap (Al_2O_3~6.02eV) respectively. They are suitable to be integrated into DRAM process. Because they are researched in this thesis. And the crystallization temperature of them are quite higher with nitrogen 950℃, which is able to resist the thermal stress leakage current effectively.

1.2 Motivation

In the early age of DRAM development, two dimensional cell structure was widely applied on the DRAM cell. Memory cell capacitance plays a important role, which can determine the data retention time, store charge, writer and erase speed. In the design bit generation, the minimum cell capacitance should be 25fF/cell. The measure of capacitance capacity can be described as the following equation:

$$C = \varepsilon_0 \varepsilon_r A/d$$

Where C: the dielectric capacitance

ε_0: the vacuum permittivity

ε_r: the relative dielectric constant of dielectric material

A: the surface area of capacitor

d: the dielectric thickness

In order to get high memory density and high capacitance in the DRAM chip,increasing the surface area of capacitor and the relative dielectric constant of dielectric material can be used to increase capacitance. Three-dimensional cell structure was introduced to 4MB-above generation, trench capacitor cell and stacked capacitor cell (STC). Both of the trench and the stacked cell techniques are still used in commercial DRAM products now. Three-dimension cell structure of DRAM increases the surface area of capacitor to get high capacitance; nevertheless, it is not enough to keep the DRAM dimension shrinking. It is another way to replace

dimension shrinking with high-k materials.

As memory trend develop in future. The low-power nonvolatile memories control are important trend in communication products. In the recent flash memory technologies, short program/erase times and operating voltage reductions are the most important issues to realize high speed/low power operation [29], [40]-[42]. For EEPROM and flash memory devices, the IPD requires a high charge-to-breakdown (Q_{BD}), high breakdown field and low leakage current to obtain good data retention characteristics [43]-[45]. It is not sufficient to meet the stringent data retention requirement of IPD while applying fluorine passivated silicon surface technologies due to the unavoidable leakage current [46]. In order to accomplish this without a trade-off between low power and high speed operations, high coupling ratio should be achieved by increasing the floating gate capacitance [47]-[54].

There are three different approaches can be used to increase coupling ratio. First, decrease the IPD thickness. Oxide/nitride/oxide (ONO) multi-layered films had been extensively investigated and frequently used as the dielectric layer in the flash memory devices and other applications [55]-[57]. However, decreasing the thickness of the IPD to increase the coupling ratio may cause serious leakage and reliability problems which are fatal in the retention time of flash memories. Secondly, increase the area of the IPD capacitor. High capacitive-coupling ratio cell [47]-[49], 3-dimension inter-poly dielectric [51], and hemisphere grain [52], [53] had been proposed to effectively increase the capacitance area and lower the control gate bias. Although the coupling ratio of above mentioned cell structure could be dramatically improved, they must be fabricated with many additional process steps for fabrication such complex structures and be difficult to control well. The final approach is to increase the dielectric constant (κ) of IPD materials [23], [24], [28], [58]-[65].

Therefore, it is straightforward and effective to incorporate alternative high dielectric constant (high-κ) materials on nonvolatile memories to replace oxide/nitride/oxide IPD for increasing floating gate capacitance without increasing cell area and complexity of fabrication while suppressing charge loss. By increasing the floating gate coupling ratio, high-κ IPDs can lead to a high electric field across tunnel oxide even at very low control gate voltage.

Recently, aluminum oxide (Al_2O_3) [18], [66]-[68] and hafnium oxide (HfO_2) [21], [69]-[72] had been proved as promising candidates for the gate dielectrics of sub-0.1 μm device due to their higher κ, relatively high φ_B and superior thermal stability, shown in Table 1.1. Thanks to the high dielectric constant and high thermal stability, Al_2O_3 and HfO_2 are suitable to be integrated into stacked-gate flash memories. Nonetheless, the effects of these kinds of high-κ dielectrics on flash memories are seldom investigated. To further realize the dielectric properties of these high-κ dielectrics, some reliability issues such as breakdown field, charge trapping and temperature-dependence behaviors are extensively studied for both gate dielectric and flash memories applications.

Many deposition methods such as physical vapor deposition (PVD), metal-organic chemical vapor deposition (MOCVD), atomic layer chemical vapor deposition (ALCVD) [73], [74], and molecular beam epitaxial method (MBE), etc. have been employed to prepare high-κ IPDs. The pros and cons of each deposition techniques are demonstrated in Table 1.2. For industrial application, PVD and MBE are not appropriate tools for high-κ film deposition. Since MOCVD has the advantage of superior step coverage, high deposition rate, good controllability of composition, excellent uniformity of film thickness over large area, we, therefore, choose the MOCVD technology as our tool to deposit thin high-κ IPDs. A detail schematic

structure is shown in Fig. 1.3. The MOCVD chamber is equipped with a turbomolecular pump and a liquid injection system, which has four independent-controlled injectors. The latter is consisted of a liquid pump to pump the precursors through a hot nickel frit with a proper rate because the pump is unreliable at low pump rates. The vapors are carried with a 200sccm flow of Ar to a gas distribution ring which is located at a proper distance from the substrate. In contrast to the conventional bubble system, the liquid injection is with sufficient temperature window to alleviate the thermal aging of the precursor. This is because the precursor remains in liquid state at room temperature until it is pumped into the vaporizer and injected into the deposition chamber. However, the precursor should be kept at long-term chemical stability in solvent and non-reactive with other precursors solvent [75], [76]. The components of the vaporizer, the gas ring and the connecting tube are maintained at a temperature of 190ºC with heating tapes and blankets, while the substrate temperature is controlled at 500ºC with quartz-halogen lamps and a thermocouple. A rotating suspensor is used for uniform heating during processing. A flow of 100sccm N_2 is maintained throughout the deposition cycle. The base pressure of the MOCVD chamber is ~10^{-8}Torr. The deposition pressure of the deposition is at the 5mTorr where the gas-phase collisions are scarce.

As many reports indicated, the direct contact of high-κ materials and Si-substrate will be imperfect and debatable. The dominance of the Si MOSFETs over competing technologies has largely been attributed to the high quality of thermally grown SiO_2 and the resulting Si/SiO_2 interface [77]. The Si/SiO_2 interface is known to have a very low density of interface states (D_{it}~2×10^{10} ststes/cm^2) arising from unsaturated surface bonds and other electrically active imperfections [77]. Interface states lead to degradation of on-current, since carrier mobility is limited by scattering at the

interface due to the strong vertical electric field present in the channel. For maintaining the excellent transport properties at the Si interface, a possible method to suppress the interfacial layer thickness is to passivate the Si surface before the high-κ IPD deposition. One of the methods is to passivate the Si surface with fluorine implant surface, then nitrogen-contained ambient activation. Passivation of the Si surface using fluorine treatment after the deposition of polysilicon has been shown to be effective in achieving the low EOT and preventing the boron penetration [78], [79]. However, this technique results in higher interface charges which leads to higher hysteresis and reduced channel mobility [80]. The Si-F is a superior barrier for H_2O and oxygen, and it can suppress oxygen to diffuse into Si substrate [78]. After the fluorine passivation treatment, a thin interlayer layer ($<$ 20 Å) was deposited and measured by optical measurement system (Ellipsometer). As reports, passivation of the Si surface is prior to the deposition of high-κ gate dielectrics and it shows the result to achieve the low EOT and increase reliability by making the interface smoother [81].

1.3 Organization of This Thesis

There are five chapters in this thesis. In chapter 1, we present a conceptive introduction to describe the background of the semiconductor technology and discuss the possible issues that we may meet during the dimension scaling down. In addition, we would concern about the hopeful solutions to overcome the physical limits in the ITRS, discuss and explain the reasons for high-κ IPD application in the nonvolatile flash memories.

In chapter 2, the effects of fluorine passivation on inter-poly characteristics of MOCVD Al_2O_3 dielectrics are examined. The basic electrical properties, electric field, leakage current, and reliability characteristics are presented and discussed.

In chapter 3, the effects of fluorine passivation on inter-poly characteristics of MOCVD HFO_2 dielectrics are examined. The basic electrical properties, electric field, leakage current, and reliability characteristics are presented and discussed.

Finally, in chapter 4, the conclusions are made and the recommendations describe the topics which can be further researched .

Table 1.1 Materials properties of high-κ dielectrics, Al_2O_3, ZrO_2 and HfO_2.

	High-κ Dielectrics		
	Al_2O_3	**ZrO_2**	**HfO_2**
Bandgap (eV)	**8.3**	**5.82**	**6.02**
Barrier Height to Si (eV)	**2.9**	**1.5**	**1.6**
Dielectric Constant	**9**	**~ 25**	**~ 25**
Heat of Formation (Kcal/mol)	**399**	**261.9**	**271**
ΔG for Reduction ($MO_x + Si \rightarrow M + SiO_x$)	**63.4**	**42.3**	**47.6**
Thermal expansion coefficient (10^{-6} $^oK^{-1}$)	**6.7**	**7.01**	**5.3**
Lattice Constant (Å) (5.43 Å for Si)	**4.7 - 5.2**	**5.1**	**5.11**
Oxygen Diffusivity at 950^{o}C (cm^2/sec)	**5×10^{-25}**	**1×10^{-12}**	**$\sim10^{-12}$**

Table 1.2 Comparisons of deposition techniques: sputtering, ALD, MOCVD and MBE.

Physical Vapor Deposition (PVD)	Chemical Vapor Deposition (CVD)		Epitaxial Method
	MOCVD	ALDCVD	
Pros： **1. Convenient for new materials screening.** **2. Easy to fabricate experimental data.** **3. Low cost for ownership.**	**Pros：** **1. superior step coverage.** **2. High deposition rate.** **3. Good controllability of composition.** **4. Uniformity of film thickness over large area.**	**Pros：** **1. Better thin film quality than PVD or CVD.** **2. Excellent coverage and conformity.**	**Pros：** **1. Permit single crystal, high-k dielectric system.**
Cons： **1. Planar, line-of-sight process, damage.** **2. Not likely to be used in ULSI gate process.** **3. Poor conformity, especially for high aspect ratio.**	**Cons：** **1. Hard to deposit ultra-thin films.** **2. Poorer conformity than ALCVD.** **3. C-, H-, OH-impurity contamination.**	**Cons：** **1. Low throughput.** **2. Mechanism-related surface sensitivity.** **3. Chemistry-limited final products (only binary materials are available now.)**	**Cons：** **1. Require submonolayer control.** **2. Poor throughput for ULSI standard.** **3. UHV tool and the cost of maintenance.**

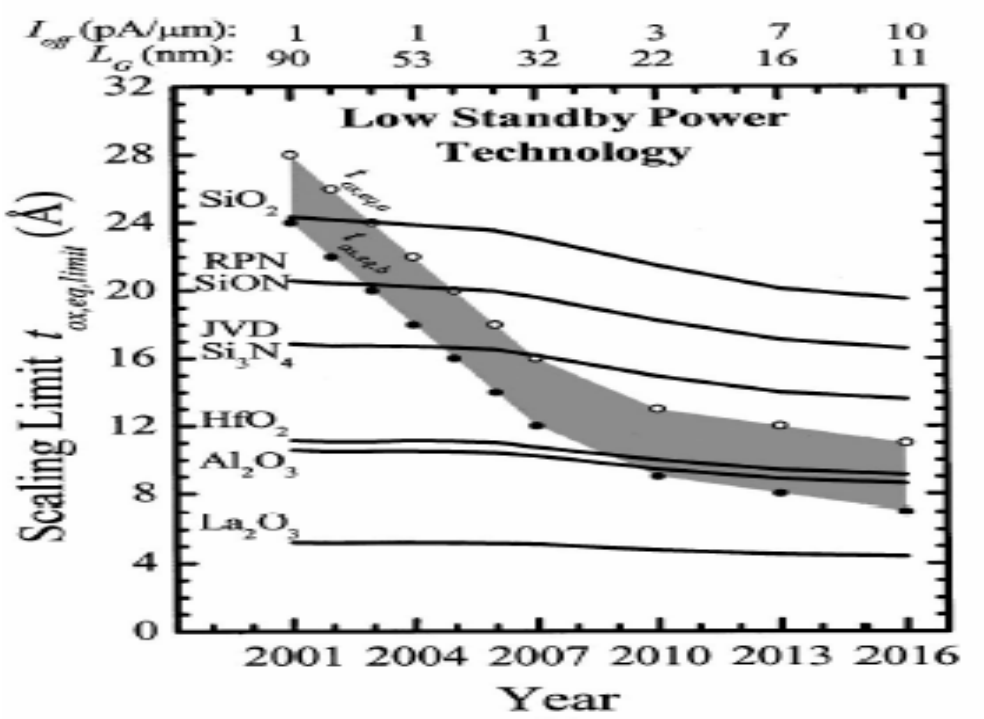


Fig. 1.1 Scaling limits of various gate dielectrics as a function of the technology specifications for low stand-by power technologies [Ref. 7].

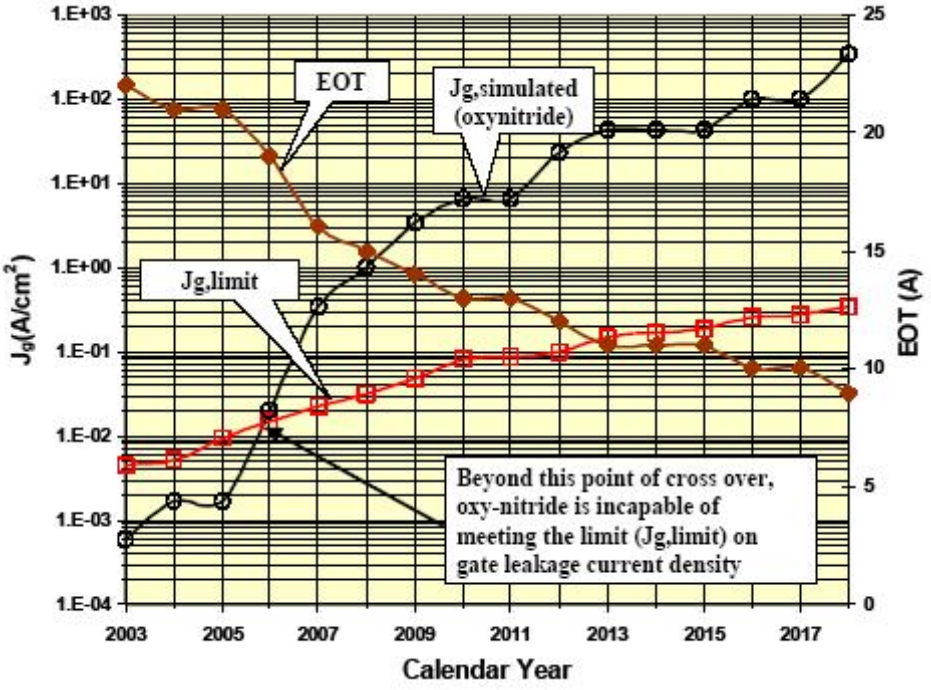


Fig. 1.2 Leakage current density and EOT projection of nitrided oxides from ITRS roadmap 2004 update.

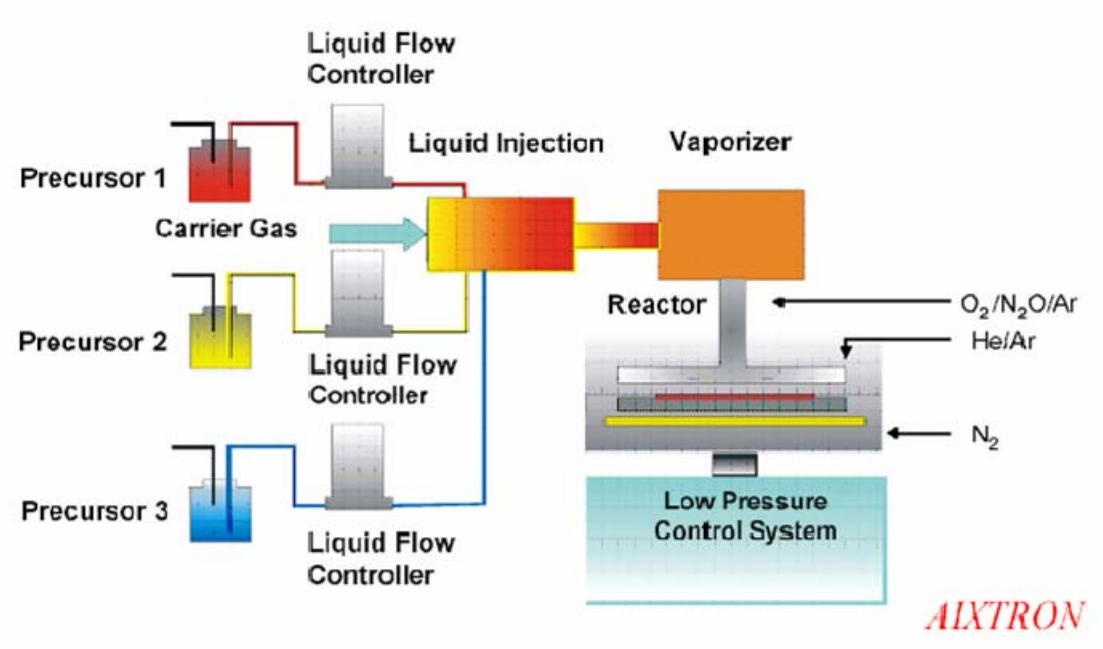
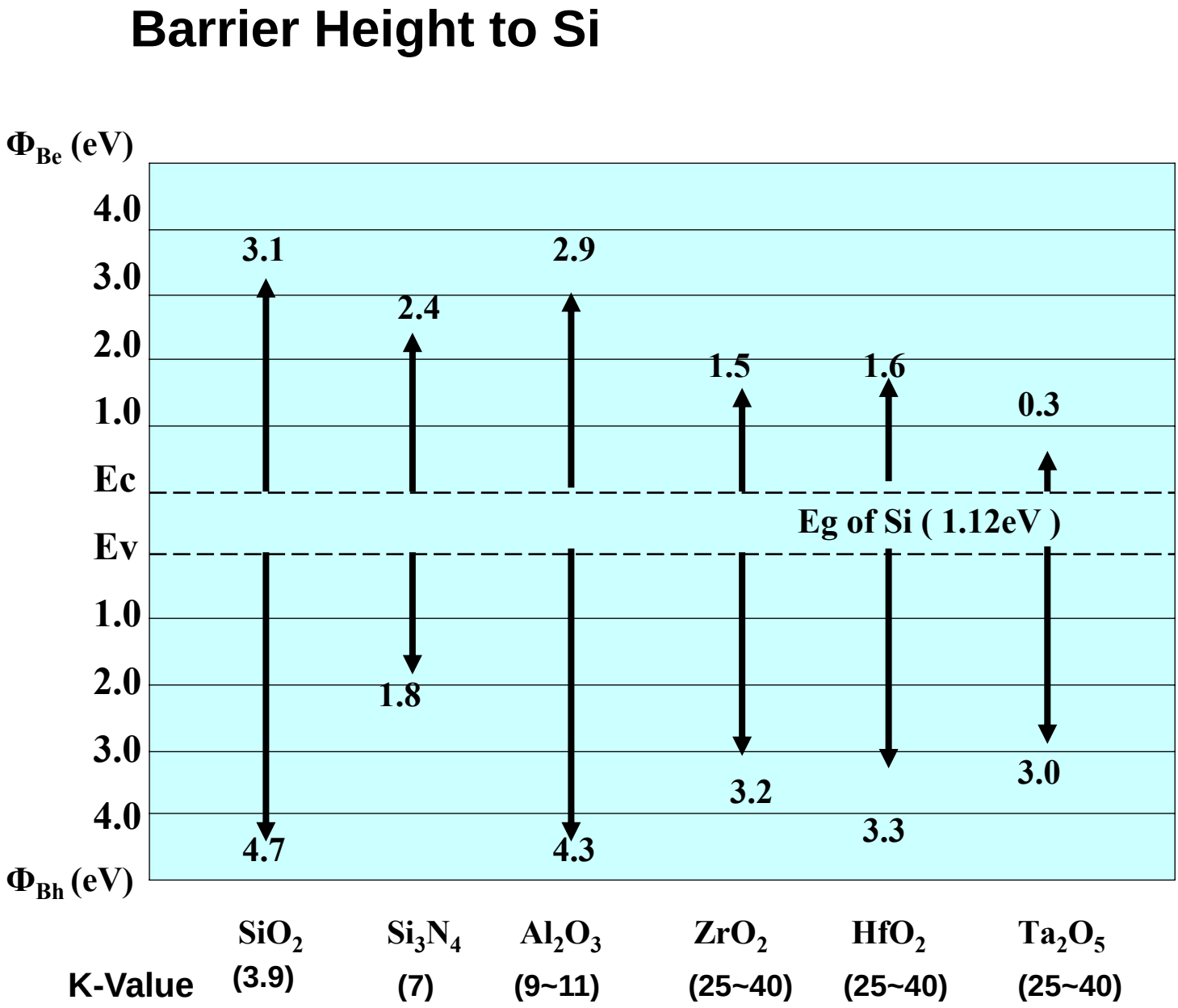


Fig. 1.3 A schematic diagram of typical MOCVD system structure.

Fig. 1.4 Band alignment of topical high-k dielectrics.



CHAPTER 2

Characteristics of Al_2O_3 Inter-Poly Dielectrics With Fluorine Passivation

2.1 Introduction

Recently, Devices with high dielectric constant materials (high-k dielectrics materials) such as aluminum oxide (Al_2O_3) have been studied intensively. However, investigation of the materials shows that fluorine dopant penetration through dielectrics is a significant problem due to the improved characteristics and reliability.

In tradition, ultra-thin oxide will undergo tunneling effect and then cause gate leakage current, which cause reliability probes. High dielectric constant materials, Al_2O_3 are used to replace SiO_2 has widely studied. Compare with SiO_2 at the same equivalent oxide thickness (EOT), high dielectric constant materials have thicker physical thickness which can stop from tunneling effect, and avoid more leakage current. Using the high dielectric constant materials is expected to have reduced leakage current and increase breakdown field and the charge-to-breakdown (Q_{BD}) as well. But high dielectric constant materials are not perfect that have some problems. High dielectric constant materials have more stress-induced leakage current and charge trapping characteristics problems. Because of the improvements in stress-induced leakage current (SILC) and charge trapping characteristics are realized

in the Al_2O_3 inter-poly dielectrics (IPD) film with the poly surface fluorine implantation (PSFI) method. The incorporation of fluorine atoms into the Al_2O_3 inter-poly dielectrics (IPD) film reduces not only interface dangling bonds but also bulk traps, which is responsible for the improvements in electrical properties. Among these materials, Al_2O_3 inter-poly dielectric is a promising candidate because of its compatibility with Fluorine implantation.

With the scaling down of thickness of the inter-poly dielectrics (IPD), the quality of dielectric becomes very critical for the application of the EEPROM and flash nonvolatile memories. Lower leakage of the dielectric means longer data retention time. As many reports indicated that high dielectric constant materials with fluorine implantation has been shown improved electrical properties [82]-[84]. It is found that the incorporation of fluorine on the bottom poly-Si surface can not only reduce leakage current by one order of magnitude, but also enhance the breakdown field and the charge-to-breakdown (Q_{BD}) as well. This is ascribed to the resultant smoother interface between the dielectric and the floating gate by surface fluorine passivation and less electron charge traps in the bulk. However, the Q_{BD} is better than other only sputter and NH_3 nitridation method. Moreover, the effect of fluorine dosage on the electrical properties and reliability characteristics of Metal Organic Chemical Vapor Deposition (MOCVD) Al_2O_3 inter-poly capacitors with surface fluorine passivation are studied in this chapter. The electrical properties of the Al_2O_3 IPD are strongly influenced by the fluorine passivation. The optimum floating gate is 5e13cm^{-2} and control gate is 5e15cm^{-2} in terms of leakage current, electron trapping rate and Q_{BD}.

2.2 Experimental Details

The n^+-polysilicon/Al_2O_3 IPD/n^+-polysilicon capacitors were fabricated on 6-inch p-type (100)-oriented silicon wafers. Silicon wafer was thermally oxidized at 980^{o}C to grow a 2000Å buffer oxide. 2000Å bottom polysilicon film (Poly-I) was deposited on the buffer oxide by low pressure chemical vapor deposition (LPCVD) system using SiH_4 gas at 620^{o}C and subsequently implanted with phosphorous at 5e15cm^{-2}, 20keV and implanted with fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV. Then activated with N_2 RTA at 950°C for 30s. Prior to the growth of Al_2O_3 IPDs, the native oxide covered Poly-I was cleaned by the conventional RCA cleaning and diluted HF etching in sequence for the removal of particles and native oxides. The surface of Poly-I prepared in this matter was known to be contamination free and terminated with atomic hydrogen. After being wet cleaned and dipped in HF solution, and 10nm Al_2O_3 IPD was deposited by Metal-Organic Chemical Vapor Deposition (MOCVD) system at 500°C with Ar/O_2 ambient. Annealing of aluminum oxide (Al_2O_3) IPDs was carried out by rapid thermal annealing (RTA) at 950^{o}C temperatures ranging in an N_2 atmosphere for 30s. Subsequently, a 2000Å top polysilicon layer (Poly-II) was deposited by LPCVD and implanted with phosphorous at 5e15cm^{-2}, 20keV. Then, implanted with fluorine dosage ranging from 5e13cm^{-2} to 5e15cm^{-2} at 20keV. Dopants were then activated with N_2 RTA at 950°C for 30s. Finally, 5000Å TEOS oxide passivation and Al metal pads were defined. The cross-sectional view and key process steps of Al_2O_3 inter-poly capacitor with fluorine passivation effect are show the in Fig. 2.1 and 2.2, respectively.

The equivalent oxide thickness (EOT) was obtained from the high frequency (1MHz) capacitance-voltage (*C-V*) measurement using a Hewlett-Packard (HP) 4284

LCR meter. Moreover, the physical thickness was estimated by high resolution transmission electron microscopy (HRTEM). The electrical properties and reliability characteristics of the inter-poly capacitors were measured using a HP4156C semiconductor parameter analyzer.

2.3 Results and Discussions

In this chapter, the Characteristics and Reliabilities of Fluorine Passivation Effect on the MOCVD Al_2O_3 capacitors with various Fluorine Dosage show to investigated in terms of store of capacitance, leakage current and dielectric reliabilities.

2.3.1 The Basic Electrical Properties on the MOCVD Al_2O_3 IPD

Figure 2.3(a) shows the high frequency *C-V* curves (1MHz) of the floating Gate (FG) corresponding EOT of Al_2O_3 inter-poly capacitors with surface Fluorine Passivation Effect that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV. Figure 2.3(b) shows the high frequency *C-V* curves (1MHz) of the control Gate (CG) corresponding EOT of Al_2O_3 inter-poly capacitors with surface fluorine passivation Effect that fluorine dosage ranging from 5e13cm^{-2} to 5e15cm^{-2} at 20keV. The EOT is decreased as raising Fluorine passivation effect, which can be ascribed to the fluorine itself physical factors. Because of fluorine atoms inter wafer lattices and to fill vacancy and cause AlF_3 formation, therefore are able to increased capacitance. As the fluorine dosage of floating gate continually increases to 1e14cm^{-2} and the fluorine dosage of control gate continually increases to 5e15cm^{-2}, Al_2O_3 film can reduce

defects and slightly increase permittivity, smaller EOT value is therefore obtained as compared effectively with 1e14cm^{-2} and 5e15cm^{-2} samples.

2.3.2 Electric Field and Leakage Current Density Characteristics

Figure 2.4(a) and Figure 2.4(b) that compares the *J-E* characteristics of the Al_2O_3 inter-poly capacitors with fluorine Passivation at various fluorine dosage. It is found that the sample with floating gate fluorine 5e13cm^{-2} and control gate 5e15cm^{-2} can effectively reduce the low-field leakage current about one to two orders of magnitude than other samples, which is helpful to increase effective breakdown field from the floating gate and control gate sample. The leakage current in negative polarity is smaller than that in positive polarity due to asymmetric band diagram. It can be explained by the reduced damage generated and assistance in the interface of the inter-poly dielectrics and polysilicon film. Because thermal stress and atoms impact on lattice of crystal cause various crystal defects that like interstitial impurity atoms, edge dislocation, self- interstitial, dislocation loop, vacancy etc. Using fluorine passivation not only can reduce defect but also increase electrical properties.

2.3.3Relation of Trapping Density and Defect

Figure 2.5(a) , Figure 2.5 (b) show the Positive and Negative trap densities evaluation at 2 V constant voltage stress (CVS) of Al_2O_3 floating gate inter-poly capacitors with surface fluorine passivation effect that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV. Figure 2.5(c) , Figure 2.5 (d) show the positive and negative trap densities evaluation at 2 V constant voltage stress (CVS) of Al_2O_3 Control Gate inter-poly capacitors with surface fluorine passivation effect that

fluorine dosage ranging from 5e13cm^{-2} to 5e15cm^{-2} at 20keV. Presents the transient currents for the fluorine passivation effect of Al_2O_3 IPDs under a low field of 2 MV/cm in order to suppress the creation of stress-induced traps. Filling of the pre-existing electron traps in the high dielectric constant materials leads to the decrease of the current leakage magnitude over time for all samples [85], [86]. Moreover, the rate of leakage current reduction in either polarity is nearly identical, suggesting that the traps are distributed uniformly across the films. Incorporation of Fluorine atoms tends to segregate at Poly and Poly/ HfO_2 interface after activation. The N_2 950℃ can effectively assist the crystal lattice atoms arranges in order again, and the stress levels on the fluorine implanted case are consistently higher which result from the much stronger Al-F bonds relative to Al-Al, Al-O or even Al-Si bonds. The Al-F bonds strength are 159Kcal/mole whereas the Al-Al bonds strength are only 45 Kcal/mole. This is perhaps manifest best in the relative melting points of AlF3 (1291℃) than Al (660℃) or other bonds samples. Therefore, we believe that the dependence of the IPD characteristic on fluorine passivation effect is closely related to the bulk defects in the high-k dielectric. Figure 2.5(c) , Figure 2.5 (d) show the 100Å Al_2O_3 gate dielectric under a 2V constant voltage stress (CVS) for 1000 sec, and good reliability evidenced to show fluorine passivation is better than without fluorine passivation from the small current charge and stress-induced leakage current (SILC) respectively. Moreover, Al_2O_3 inter-poly capacitors fluorine passivation effect exhibits small electron trapping rate than without fluorine passivation effect. But in Figure 2.5(a) , Figure 2.5 (b) the fluorine passivation effect is bad than without fluorine passivation. Because of the process was outdiffusion by rapid thermal annealing (RTA) three time in Floating Gate. The result of the process produced more defect and influenced electrical properties characteristics.

2.3.4 Reliability Characteristics

Figure 2.6(a), Figure 2.6 (b) show Q_{BD} Weibull plots of Al_2O_3 inter-poly capacitors with surface fluorine passivation effect in positive and Negative CVS that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV in floating Gate. The Weibull distributions of the charge-to-breakdown (Q_{BD}) field in both polarities as the magnitude of gate bias is 5.7MV/cm. Effective charge to breakdown(Q_{BD}) field exhibits nearly independent in various fluorine dosage. Because the process was outdiffusion by rapid thermal annealing (RTA) three time in floating gate, so caused more dangling bond and defects in the crystal. The increase of most fluorine passivation effect was due to the increase of fluorine dosage magnitude in floating gate. But fluorine dosage 1e14cm^{-2} was too much, and 1e12cm^{-2}, 5e12cm^{-2} was not enough to reach to fit the process of floating gate. This was ascribed to the resultant not smooth interface between the high dielectric and the floating Gate polysilicon by more or less fluorine implantation caused stress defect. The fluorine dosage 5e13cm^{-2} sample had best performance in preventing charge loss from floating Gate. The lesser leakage current means that retaining data time longer and higher charge breakdown field.

Figure 2.6(c), Figure 2.6 (d) show Q_{BD} Weibull plots of Al_2O_3 inter-poly capacitors with surface fluorine passivation effect in positive and negative 5.7MV/cm CVS that fluorine dosage ranging from 5e13cm^{-2} to 5e15cm^{-2} at 20keV in control gate. Fluorine was incorporation in the Al_2O_3 IPD stack by activation the samples causing Al-F bonds formal. In the IPD system, extensive studies have been performed to understand and improve the (Q_{BD}) for date retention by forming Si-F bonds in control gate (CG), which is more stable against hot carrier stressing than Si-H

bonds. For positive and negative gate bias, capacitors with fluorine surface passivation effect can significantly increase charge-to-breakdown (Q_{BD}) characteristics one order compared without fluorine passivation effect at 5e15cm^{-2} dosage in control gate inter-poly capacitors.

We believe that the dependence of the IPD characteristic on fluorine passivation is closely related to the bulk defects in the high dielectric material. In control gate, fluorine passivation can effectively reduce dislocation, voied, vacancies, interstitial and dangling bond result in the less interface defect density. By the result of Q_{BD} can evidence that 5e15cm^{-2} dosage is the optimized dosage at 20keV in control gate.

2.3.5 Temperature Characteristics of the fluorine passivation Al_2O_3 IPD

Figure 2.7(a) , Figure 2.7 (b) show illustrates the temperature dependence of gate current density at 3 MV/cm of Al_2O_3 inter-poly capacitors with surface fluorine passivation that dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV in floating gate. Figure 2.7(c) , Figure 2.7 (d) show illustrates the temperature dependence of gate current density at 3 MV/cm of Al_2O_3 inter-poly capacitors with surface fluorine passivation that dosage ranging from 5e13cm^{-2} to 5e15cm^{-2} at 20keV in control gate. In general, floating gate and control gate samples reduce about one order leakage current density, exhibited considerably weak measuring temperature dependence on the leakage current density in either polarity. By the Figures implying that the tunneling mechanism for the Al_2O_3 IPD is Fowler Nordheim-like, rather than Frankel Poole-like. On the other hand, the magnitude of the leakage current was found to be strongly depended on the fluorine passivation temperature. As high temperature, the electron obtained more energy and surpassed the energy barrier of Poly-I to inject into Al_2O_3 IPD. At the time, the electron mechanism was Schottky Emission.

In Poly-II/high-k dielectric/ Poly-I sandwich structure, the interface between the Poly and the high-k dielectric thin films plays significant roles by fluorine passivation in the functional performance of the thin films. It was found that fluorine passivation can effective to resist leakage current density breakdown and promote the Al_2O_3 IPD performance, because fluorine passivation can mend damaged lattices.

At the process due to the work function difference of the Poly electrodes, and the degree of asymmetry increases with the increasing work function difference. For the samples with high work function Poly as both or at least one of the electrodes, the passivation switching is much faster. The current–voltage curves at various fluorine dosages indicated the interface-controlled asymmetric phenomena are mainly determined by the Schottky emission and charge injection at the Poly/high-k dielectric polymer interface in high temperature. Fig. 2.8 Band diagrams of Al_2O_3 inter-poly capacitors with surface fluorine passivation under (a) positive and (b) negative gate voltage biased to the Poly-II.

2.3.6 Results and Compare

In this chapter, the effects of fluorine passivation on the MOCVD Al_2O_3 IPDs are investigated in terms of EOT, κ-value, dosage-EOT, dosage-average breakdown current, effective breakdown field and 63%-failure Q_{BD} values and temperature under (a) Positive V_G (b) Negative V_G Floating Gate and Control Gate compare.

At first, incorporation of fluorine is closely related to EOT, κ-value. Fluorine is believed in stronger Hf-F and Si-F bonds than Hf-H and Si-H bonds, which can reduce the EOT and increase the κ-value of Al_2O_3. The EOT increases as fluorine

passivation effect rising up to 5e13cm^{-2} in floating gate. Figure 2.9 (a) show over fluorine dosage 1e14 cm^{-2} is contrary effect that causes more dangling bond easily in Al_2O_3/poly interface. But in control gate, the fluorine passivation effect can rise up to 5e15cm^{-2} . This is ascribed to that only polysilicon can store more capacity of fluorine atoms, as seen in Figure 2.9 (b). Besides, we use 20kev in control gate than 10kev in floating gate causing implanted distance farther. Figure 2.9 (c) and Figure 2.10 illustrates show floating gate and control gate compared. The evidences we know, EOT and κ-value of control gate is more effectively than floating gate from the same dosage condition at 5e13 cm^{-2} or 1e14 cm^{-2}.

Figure 2.11(a), (b), (c), (d), Al_2O_3 IPD capacitors with fluorine incorporation could also exhibit better dielectric performance and reliability. Incorporation of fluorine into Al_2O_3/poly interface has been highly effective in lower leakage current and higher breakdown voltage from floating gate than control gate in the same condition. The evidences show in Figure 2.12(a), (b) and Figure 2.13. The stacked-gate flash memories with Al_2O_3 by using Fowler-Nordheim(FN) tunneling are helpless in operation voltage reduction. In general, the dielectric constant increased, the bandgap decreased. Because we used fluorine passivation to improve device performance and repair defect. By increasing the floating gate coupling ratio, fluorine passivation Al_2O_3 IPD capacitors can lead to a high electric field across tunnel oxide (TOX) even at very low control gate voltage.

Figure. 2.14 show the charge to breakdown (Q_{BD}) images of Al_2O_3 IPDs with surface fluorine passivation under (a) Positive V_G (b) Negative V_G Floating Gate and Control Gate compare. We believe that the dependence of the IPD characteristic with fluorine passivation is closely related to the bulk defect s in the dielectric. By fluorine passivation into FG Al_2O_3/poly interface and CG poly interface that incorporation

of suitable fluorine atoms can repair bulk defect, increase data retention, suppress electron trapping rate and interfacial layer growth.

Figure. 2.15 (a),(b) show the Al_2O_3 IPD capacitors has better performance at high temp. We describe the characteristics with silicon surface fluorine implantation (SSFI) for Al_2O_3 IPD films. The thermal stability of Al_2O_3 IPD capacitors is much improved owing to the incorporation of fluorine into Al_2O_3 thin films. The gate leakage current of the SSFI Al_2O_3 films is about one to two orders less than that of samples without any fluorine implantation. In addition, improvements in stress-induced leakage current (SILC) and charge trapping characteristics are realized in the Al_2O_3 films with the SSFI. The incorporation of fluorine atoms into the Al_2O_3 films reduces not only interface dangling bonds but also bulk traps, which is responsible for the improvements in properties. These results clearly reveal Al_2O_3 floating gate with fluorine passivation can effectively reduce electron loss as well as obtain better average breakdown voltage, high Q_{BD} and resist high-temperature than control gate.

As the Al_2O_3 IPD capacitors process had completed the work. We used high-resolution transmission electron microscopy (HRTEM) to confirm Al_2O_3 IPD thickness and interfacial layer thickness. Before HRTEM, We must be cutting and digging a hole with focused ion beam (FIB). Figure.2.16 show the FIB cross-sectional images of Al_2O_3 IPD capacitors. The FIB top images of Al_2O_3 inter-poly dielectric device thickness must be smaller than 500Å to do HRTEM, show in Figure. 2.17. After finishing FBI, Figure. 2.18 show the TEM all cross-sectional images of Al_2O_3 inter-poly dielectric. The Al_2O_3 dielectric thickness is about 100 Å ~120Å. And the interfacial layer thickness as fluorine passivation effect as short. Figure. 2.19 show (a) without fluorine. (b) FG with 5E13 cm^{-2} (c) CG with 5E15 $cm^{-2.}$ Sample with 5E15 cm^{-2} not only smoothes interface but also reduces interfacial

layer thickness.

2.4 Summary

The effects of fluorine dosage on the electrical properties and reliability characteristics of the Al_2O_3 inter-poly capacitors with surface fluorine passivation are evaluated in this chapter. It was found that the electrical properties of Al_2O_3 IPD capacitors strongly depend upon the fluorine passivation effect. The floating gate with 5e13cm^{-2} and control gate with 5e15cm^{-2} are respective the best condition for the Al_2O_3 IPD capacitors electrical characteristics in terms of leakage current, temperature, Q_{BD} and electron trapping rate of control gate. The capacitance as increase as fluorine dosage that the consequences indicate closely related to the fluorine passivation effect and fluorine dosage when changing fluorine dosage concentration. The results apparently demonstrate Al_2O_3 IPD capacitors with surface fluorine passivation effect can effectively reduce charge transfer between control gate and floating gate, better retention and disturb characteristics are expected by replacing ONO IPD to Al_2O_3 IPD. The Al_2O_3 dielectric with surface fluorine passivation thus appears to be very promising for future flash memory devices. Table 2.1 lists several physical and electrical parameters, including EOT, κ-value, interfacial layer thickness, and effective breakdown field and 63%-failure Q_{BD} values of the Al_2O_3 IPD capacitors with surface fluorine passivation under positive and negative CVS at various fluorine dosage effects.

Table 2.1 EOT, κ-value, interfacial layer thickness, effective breakdown field and 63%-failure Q_{BD} values of the Al_2O_3 capacitors with surface fluorine passivation under positive and negative CVS at various fluorine dosage effects.

F Dosage (cm^{-2})	κ	EOT (Å)	E_{BD} (MV/cm)		Interfacial Layer	63% QBD (C/cm^2)	
			positive	negative	Thickness (Å)	positive	negative
0	8.5	45.9	16.8	16.3	15	2.05	1.91
FG 5E13	9.1	42.8	19.2	18.9	10.5	2.11	2.16
CG 5E15	15.8	24.6	30.1	28.9	7.9	10.23	4.32

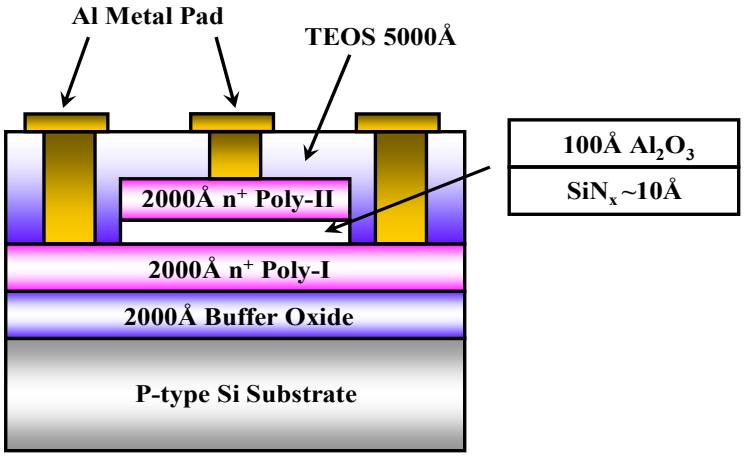


Fig. 2.1 Cross-sectional view of Al_2O_3 inter-poly capacitors with surface fluorine passivation . The fluorine was implanted on Poly-I (Floating Gate) and Poly-II (Control Gate).

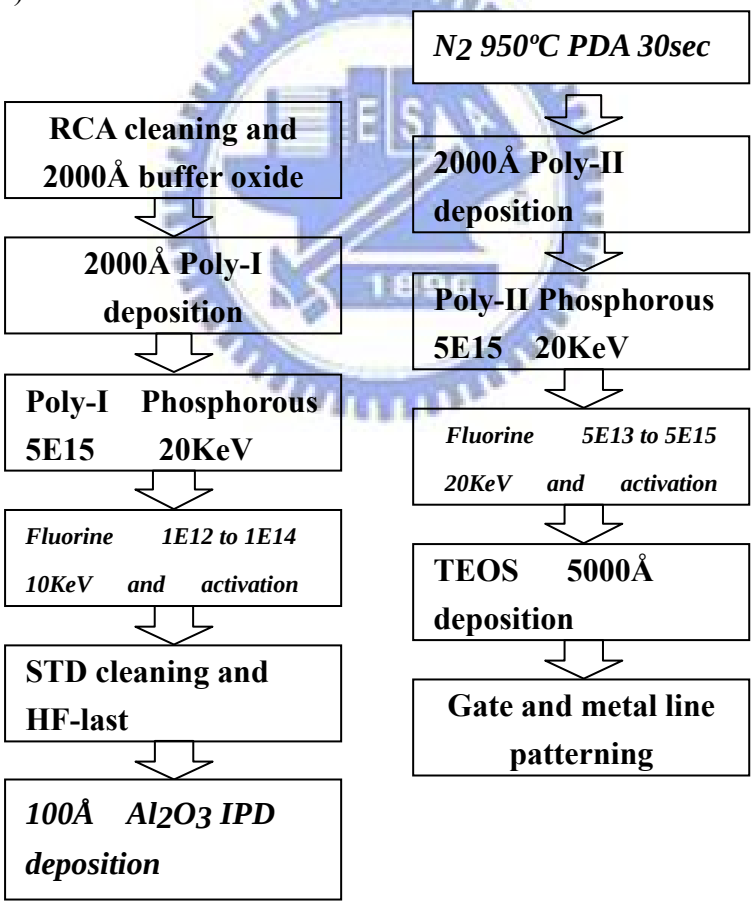
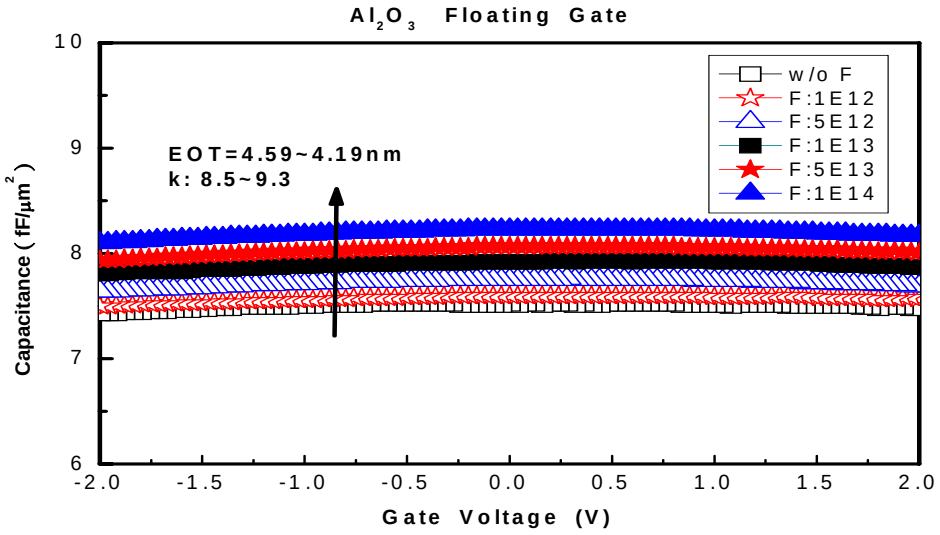
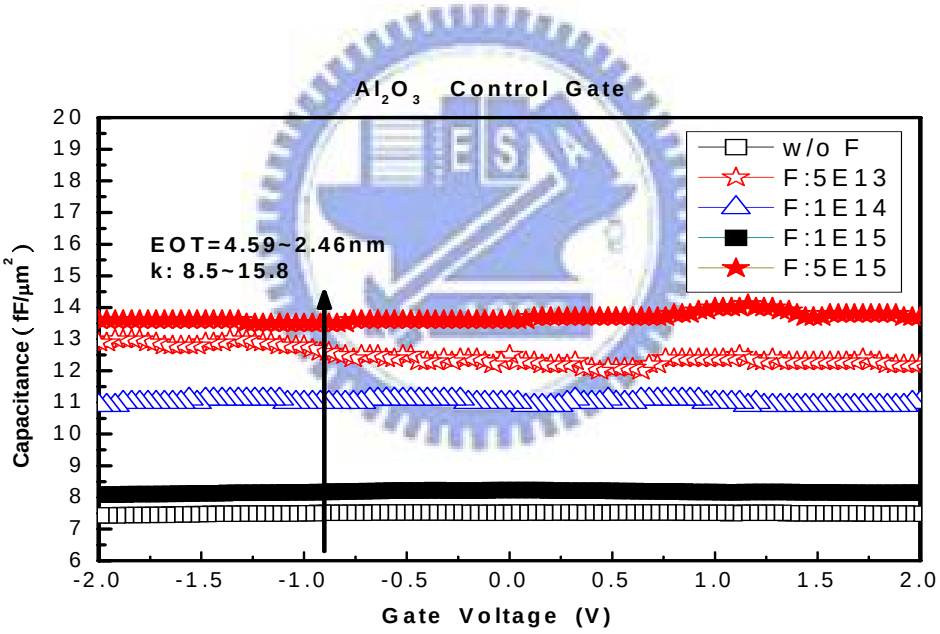


Fig. 2.2 Key process steps of Al_2O_3 inter-poly capacitors with surface fluorine passivation.

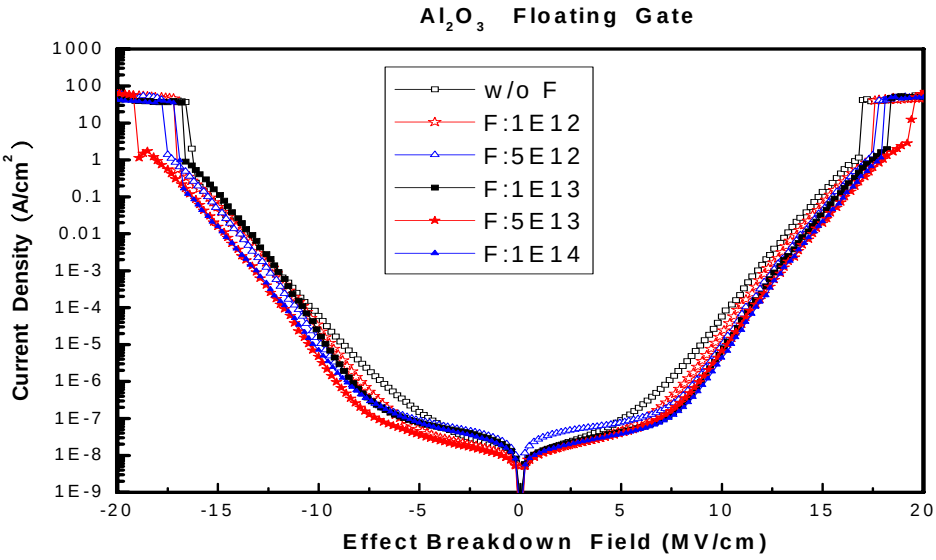


(a)

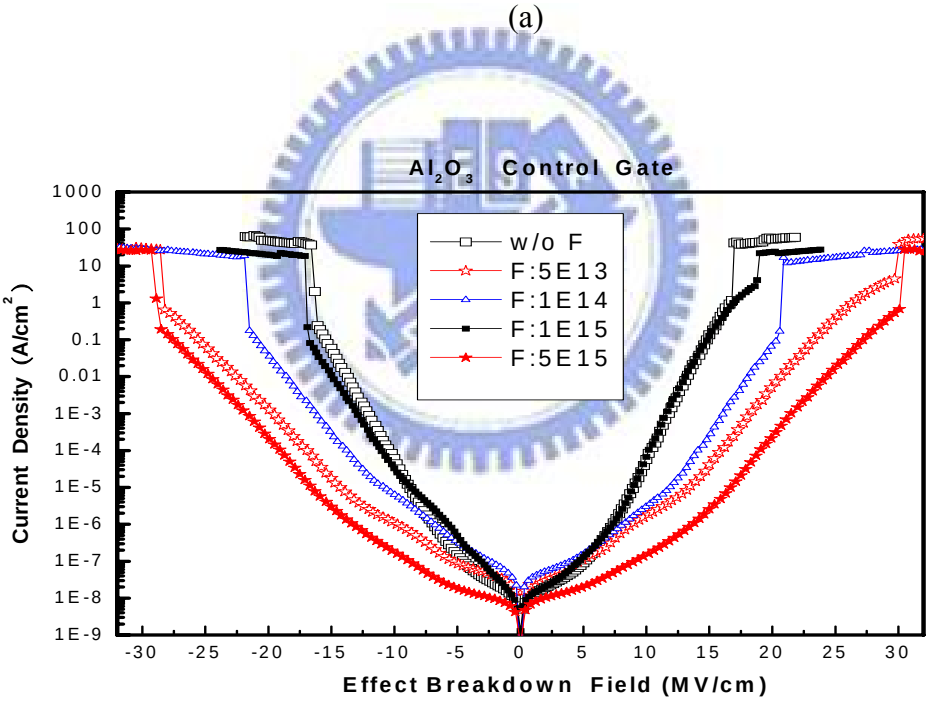


(b)

Fig. 2.3 (a) Floating Gate *C-V* curves. *C-V* characteristics of Al_2O_3 floating gate inter-poly capacitors with surface fluorine passivation effect is beneficial in scaling EOT that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV. Fig. 2.3 (b) Control Gate *C-V* curves . *C-V* characteristics of Al_2O_3 floating gate inter-poly capacitors with surface fluorine passivation effect is beneficial in scaling EOT that fluorine dosage ranging from 5e13cm^{-2} to 5e15cm^{-2} at 20keV.

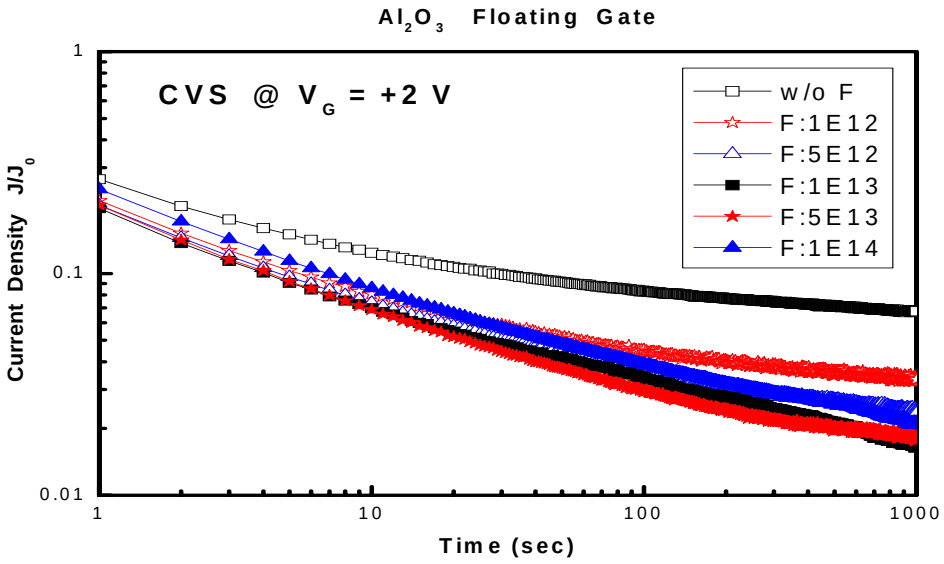


(a)

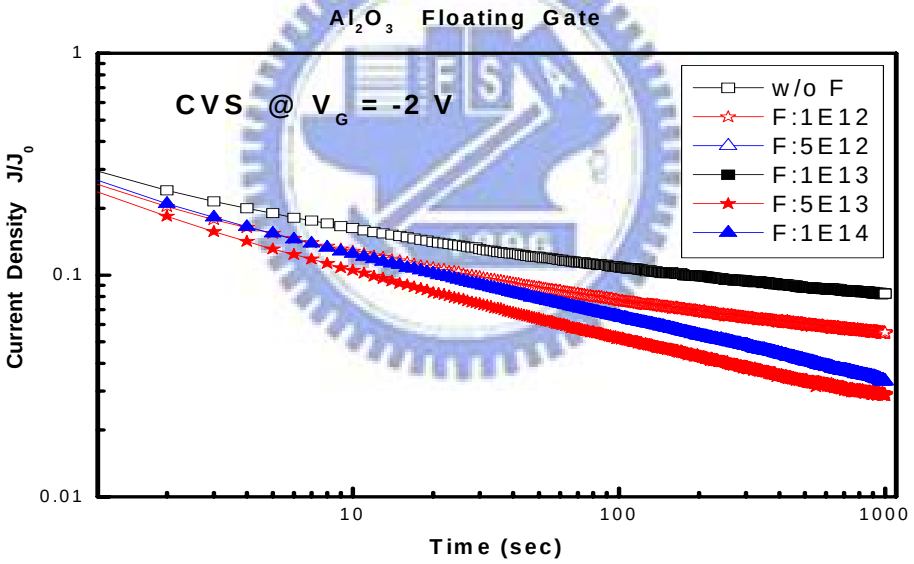


(b)

Fig. 2.4 (a) *J-V* characteristics of Al_2O_3 floating gate inter-poly capacitors with surface fluorine passivation effect is beneficial in suppressing low-field leakage current density that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV. Fig. 2.4 (b) *J-V* characteristics of Al_2O_3 control gate inter-poly capacitors with surface fluorine passivation effect is beneficial in suppressing low-field leakage current density that fluorine dosage ranging from 5e13cm^{-2} to 5e15cm^{-2} at 20keV.

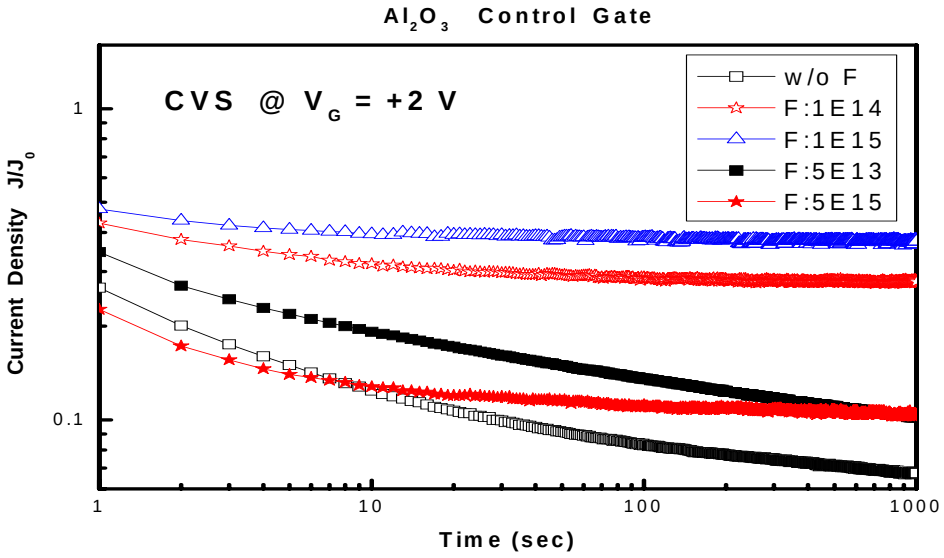


(a)

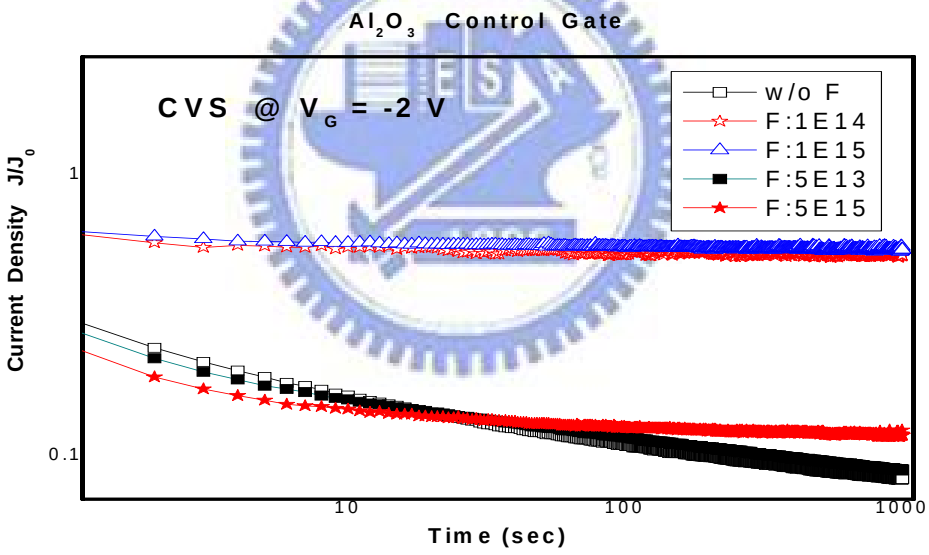


(b)

Fig. 2.5 As-fabrication trap densities evaluation at 2 V constant voltage stress (CVS) of Al_2O_3 floating gate inter-poly capacitors with surface fluorine passivation effect that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV under (a) positive 2V (b) negative 2V trap densities. The effect of fluorine passivation is bad than without fluorine passivation. Because of the process was outdiffusion by rapid thermal annealing (RTA) three time in Floating Gate.

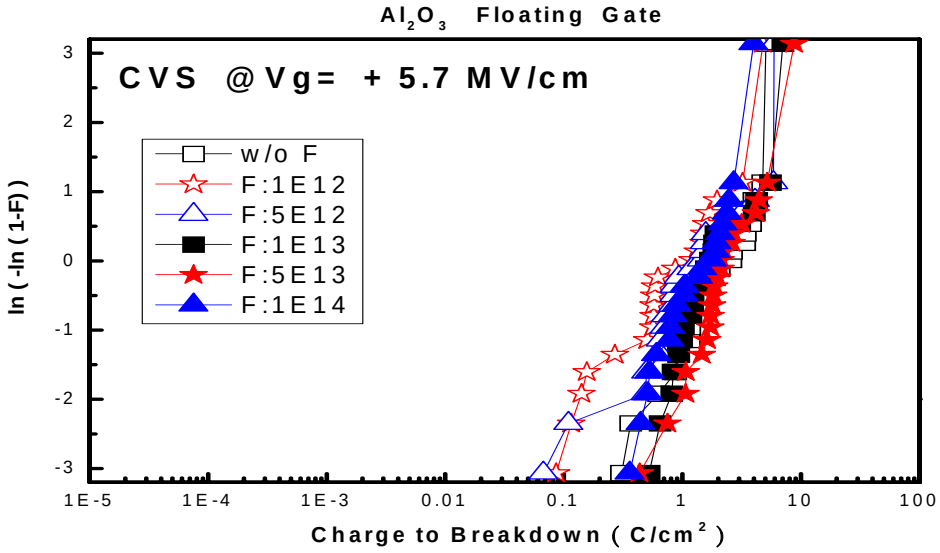


(c)

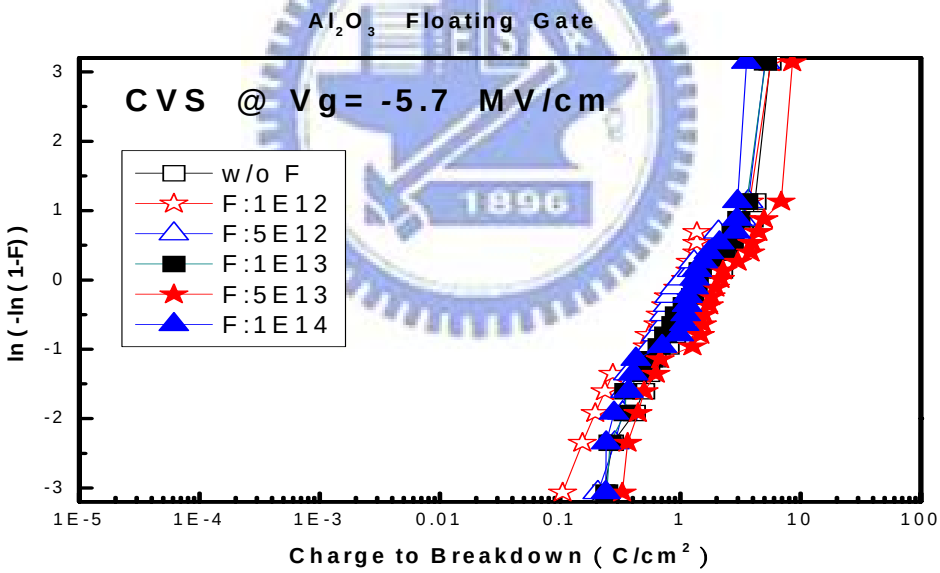


(d)

Fig. 2.5 As-fabrication trap densities evaluation at 2 V constant voltage stress (CVS) of Al_2O_3 control gate inter-poly capacitors with surface fluorine passivation effect that fluorine dosage ranging from 5e13cm^{-2} to 5e15cm^{-2} at 20keV under (c) positive 2V (d) negative 2V trap densities. Al_2O_3 inter-poly capacitors with fluorine passivation can reduce As-fabrication trap densities.

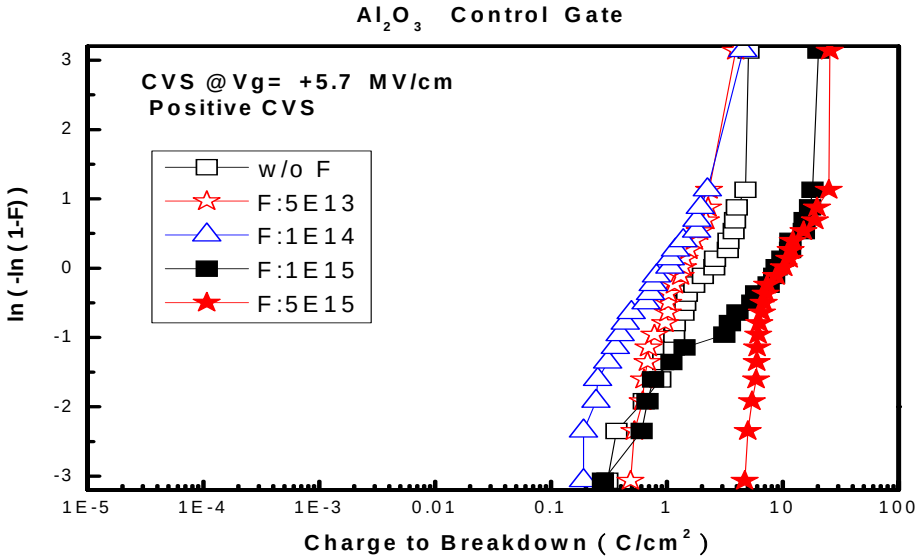


(a)

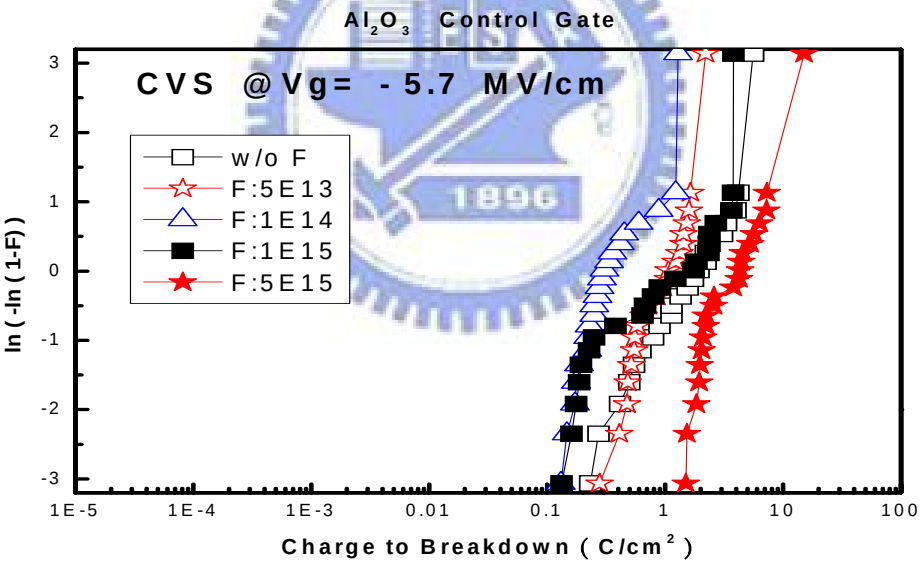


(b)

Fig. 2.6 Q_{BD} Weibull plots of Al_2O_3 inter-poly dielectric with surface fluorine passivation effect under (a) positive CVS and (b) negative CVS that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV . Al_2O_3 inter-poly capacitors with surface fluorine passivation effect can lightly increase Q_{BD} in floating gate.

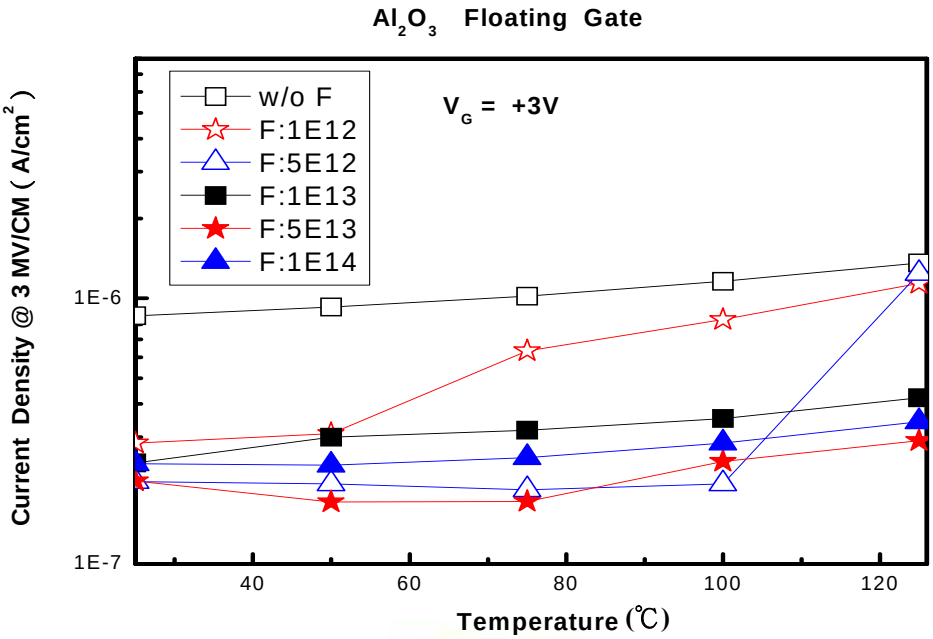


(c)

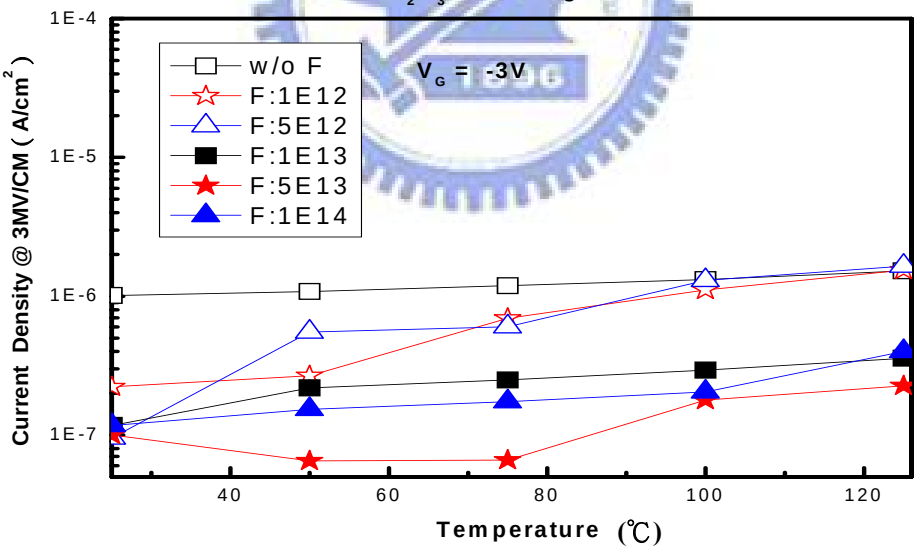


(d)

Fig. 2.6 Q_{BD} Weibull plots of Al_2O_3 inter-poly capacitors with surface fluorine passivation effect under (c) positive CVS and (d) negative CVS that fluorine dosage ranging from 5e13cm^{-2} to 5e15cm^{-2} at 20keV. Al_2O_3 inter-poly dielectric with surface fluorine passivation effect can significantly increase Q_{BD} in Control Gate.

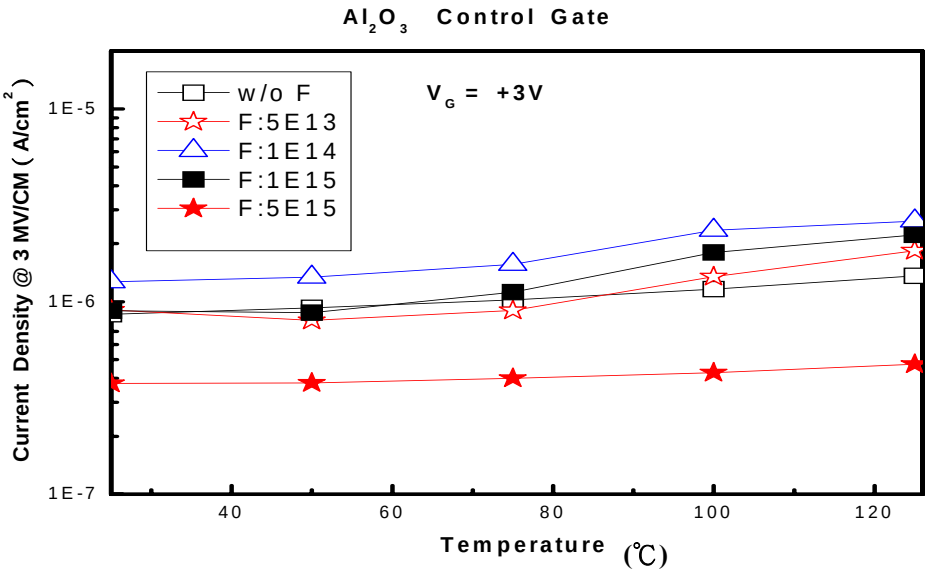


(a)

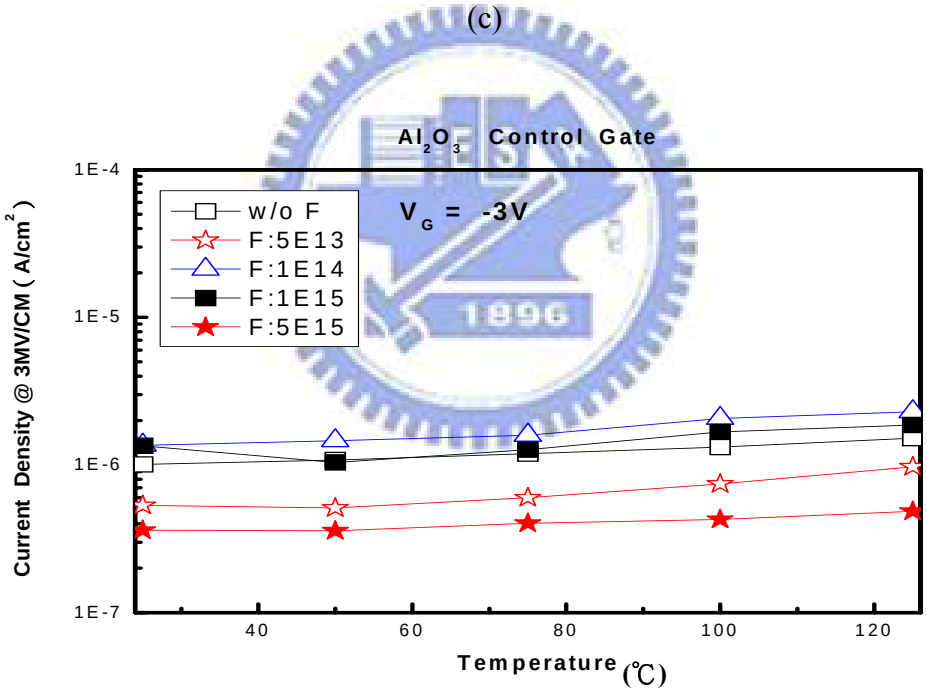


(b)

Fig. 2.7 Temperature dependence of gate current density at 3 MV/cm of Al_2O_3 inter-poly capacitors with surface fluorine passivation that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV in floating gate under (a) positive and (b) negative polarities.



(c)



(d)

Fig. 2.7 Temperature dependence of gate current density at 3 MV/cm of Al_2O_3 inter-poly capacitors with surface fluorine passivation that fluorine dosage ranging from 5e13cm^{-2} to 5e15cm^{-2} at 20keV in control gate under (c) positive and (d) negative polarities.

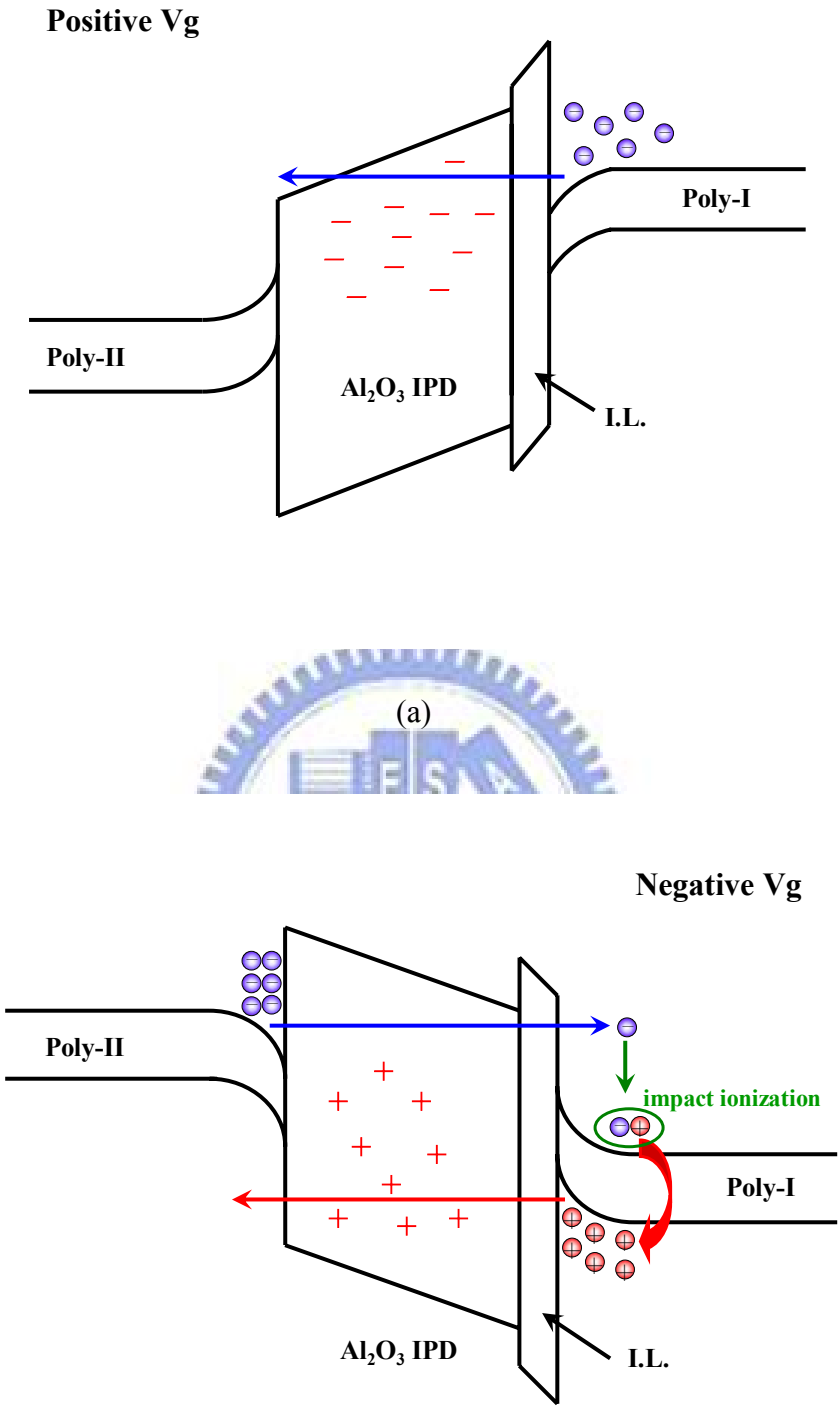
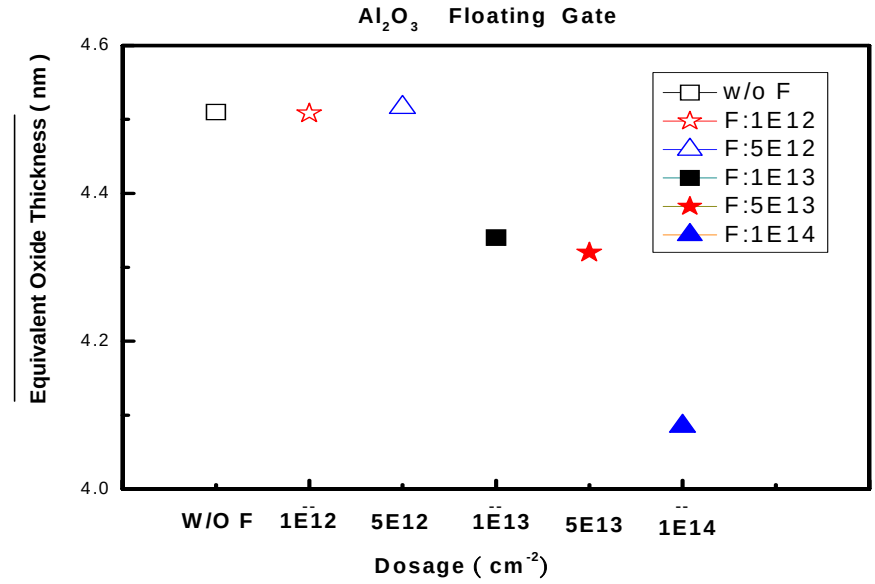
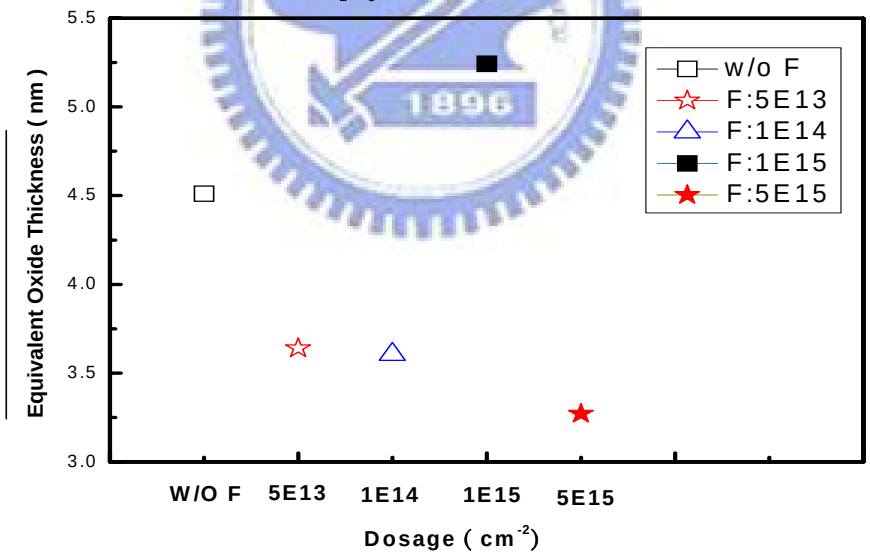


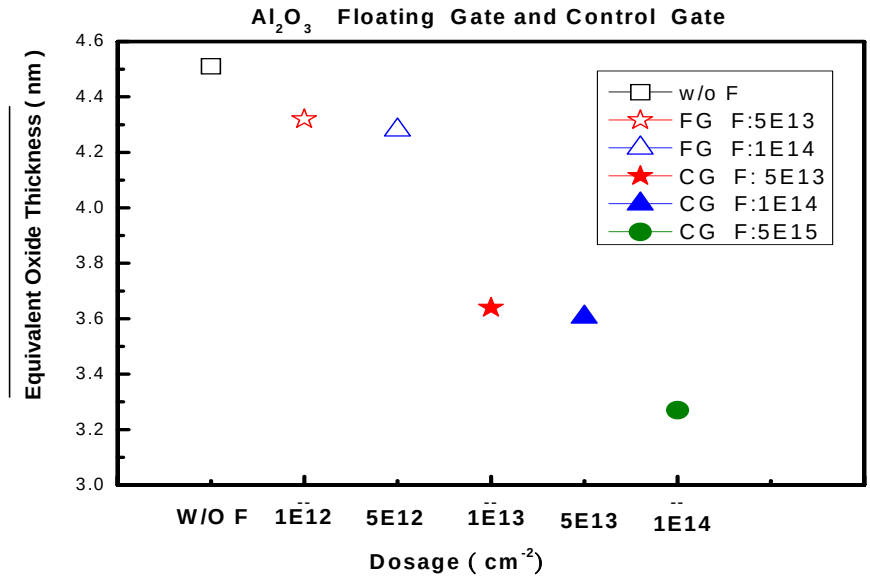
Fig. 2.8 Band diagrams of Al_2O_3 inter-poly capacitors with surface fluorine passivation under (a) positive and (b) negative gate voltage biased to the Poly-II.


Al2O3 Floating Gate
Equivalent Oxide Thickness (nm)
4.6
4.4
4.2
4.0
w/o F
F:1E12
F:5E12
F:1E13
F:5E13
F:1E14
W/O F
1E12
5E12
1E13
5E13
1E14
Dosage (cm-2)

(a)


Al2O3 Control Gate
Equivalent Oxide Thickness (nm)
5.5
5.0
4.5
4.0
3.5
3.0
w/o F
F:5E13
F:1E14
F:1E15
F:5E15
W/O F
5E13
1E14
1E15
5E15
Dosage (cm-2)

(b)



(c)

Fig. 2.9 The average EOT of Al_2O_3 IPD capacitors with surface fluorine passivation under(a) floating gate (b) control gate (c) floating gate and control gate compared.

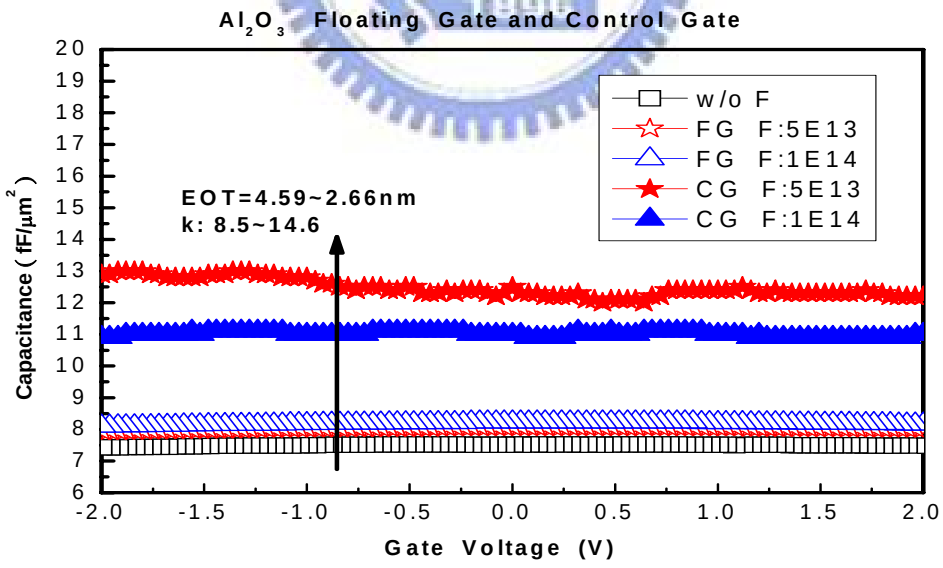


Fig. 2.10 The Capacitance of Al_2O_3 IPD capacitors with surface fluorine passivation under floating gate and control gate compared.

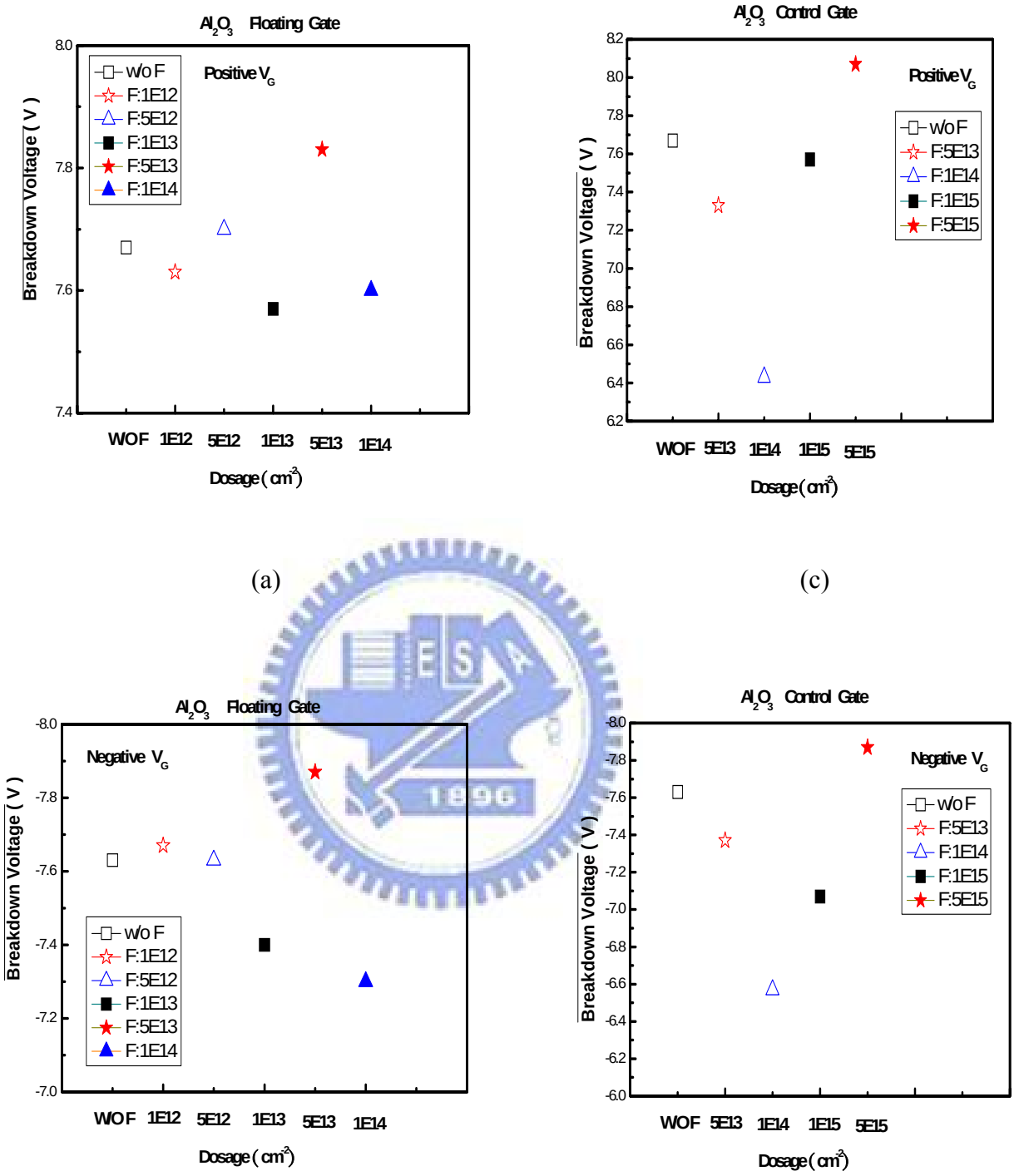
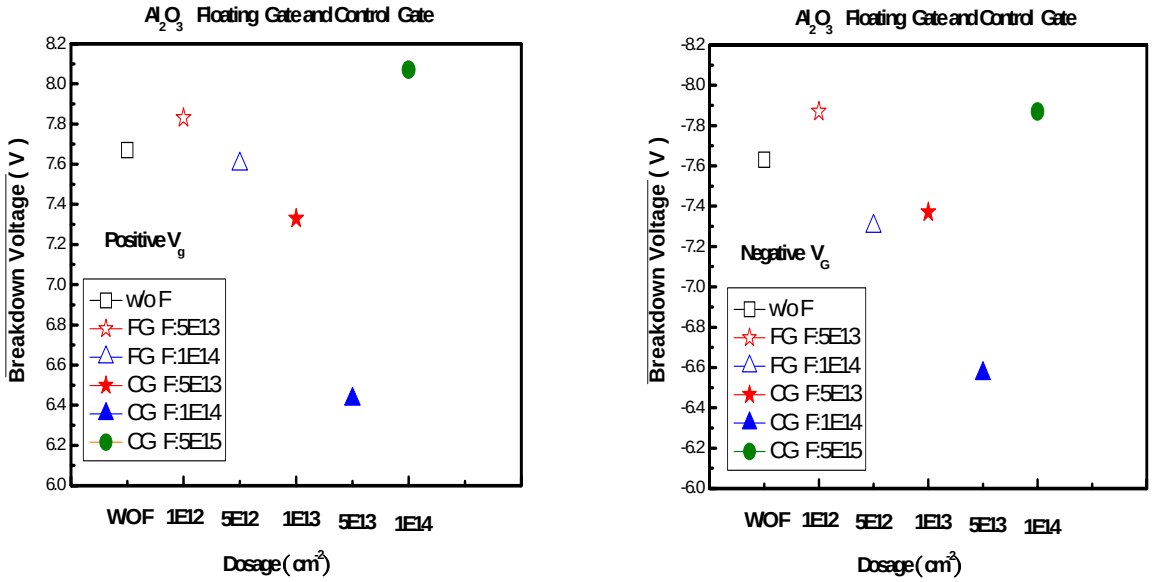


Fig. 2.11 The dosage-average breakdown voltage images of Al_2O_3 capacitors with surface fluorine passivation under (a) Positive V_G floating gate (b) Negative V_G floating gate (c) Positive V_G control gate (d) Negative V_G control gate.



(a) (b)

Fig. 2.12 The dosage-average breakdown voltage images of Al_2O_3 capacitors with surface fluorine passivation under (a) Positive V_G floating gate and control gate compare (b) Negative V_G floating gate and control gate compare.

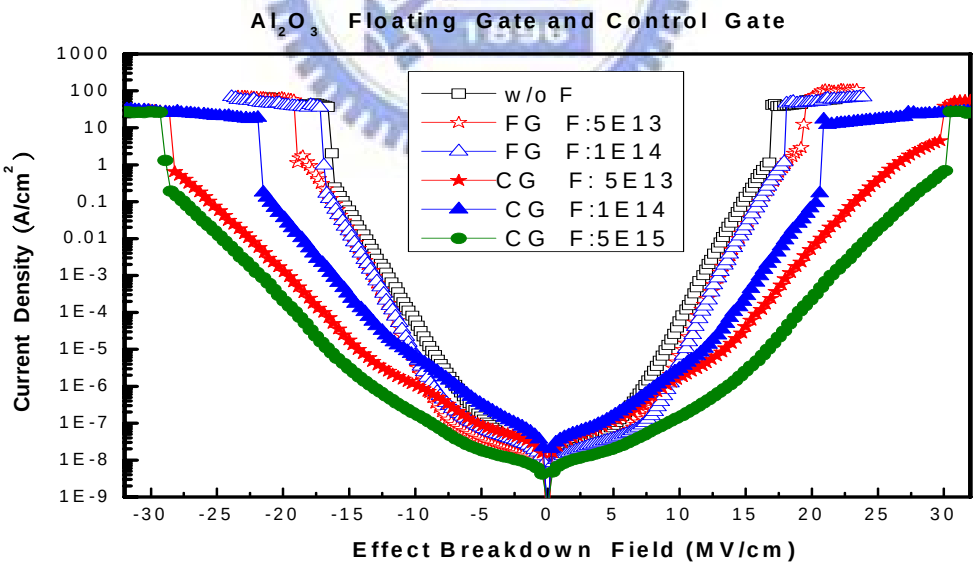
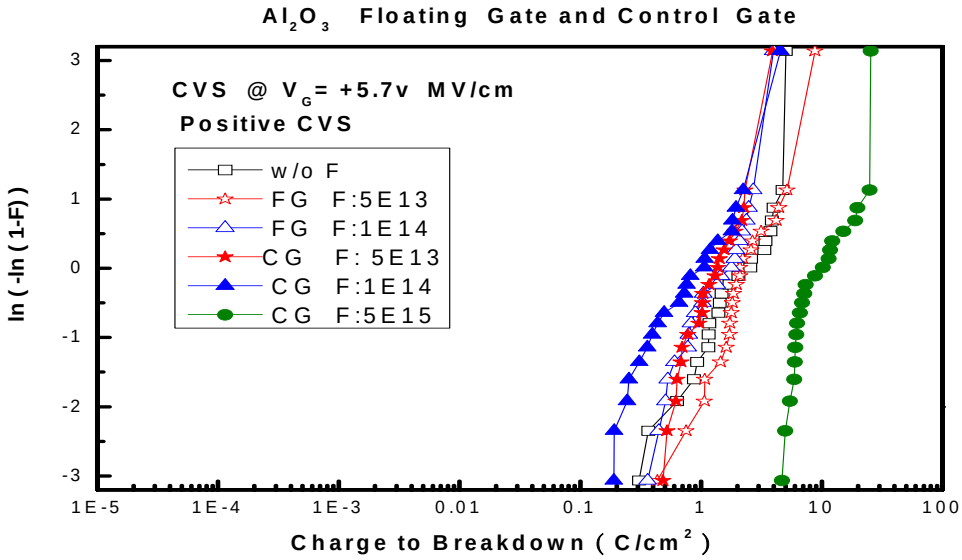
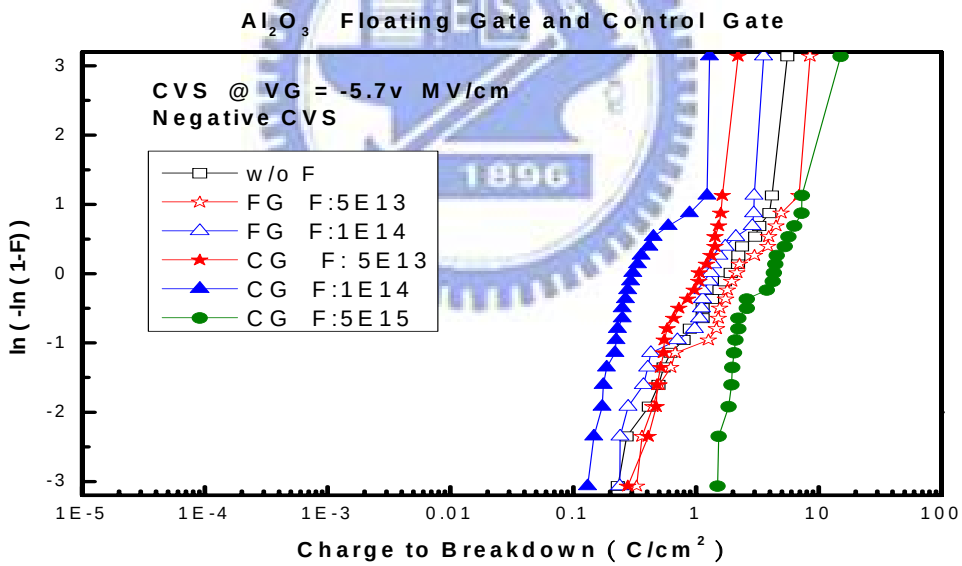


Fig. 2.13 The effect breakdown field of Al_2O_3 capacitors with surface fluorine passivation under floating gate and control gate compared.

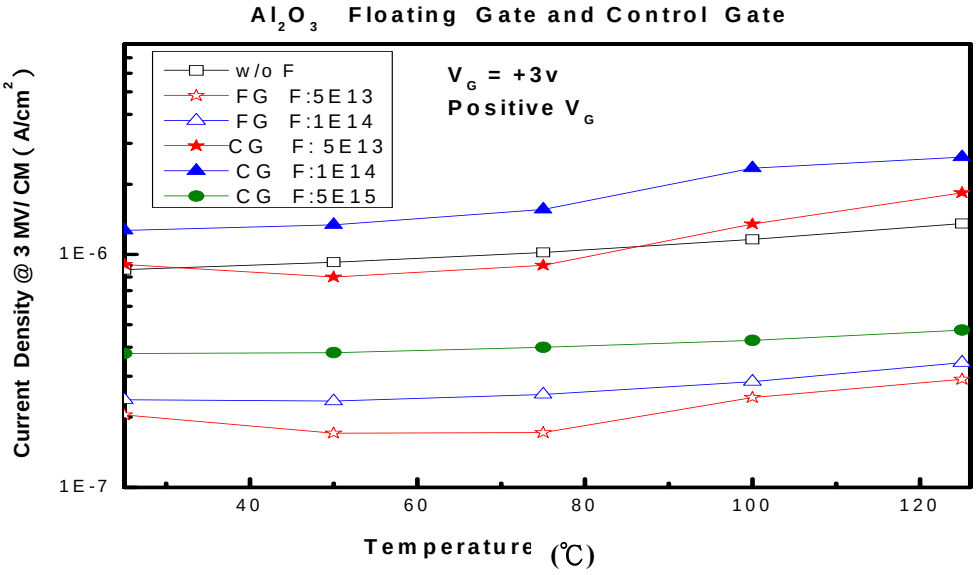


(a)

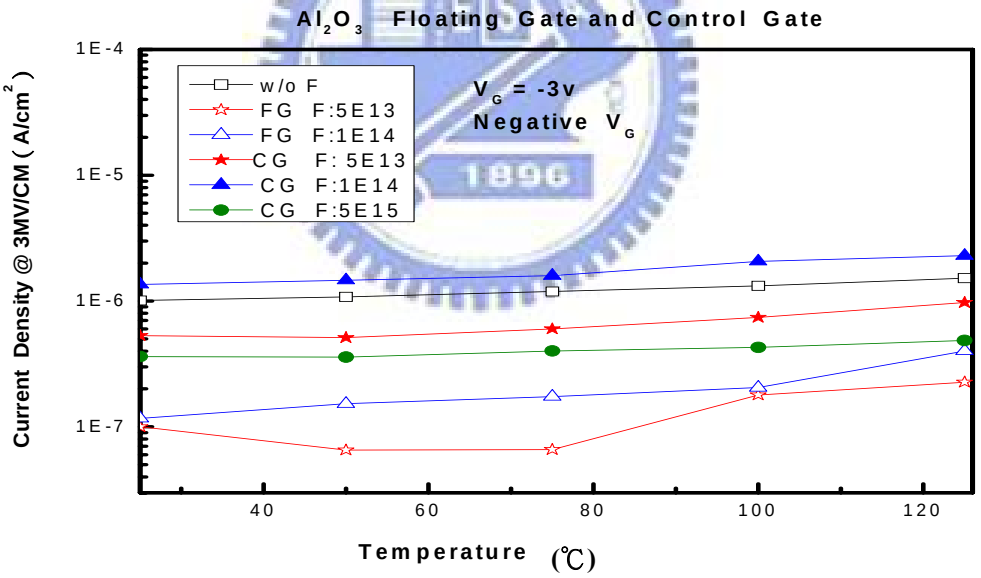


(b)

Fig. 2.14 The charge to breakdown (Q_{BD}) images of Al_2O_3 capacitors with surface fluorine passivation under (a) Positive V_G (b) Negative V_G floating gate and control gate compare.



(a)



(b)

Fig. 2.15 The temp images of Al_2O_3 capacitors with surface fluorine passivation under (a) Positive V_G (b) Negative V_G floating gate and control gate compare.

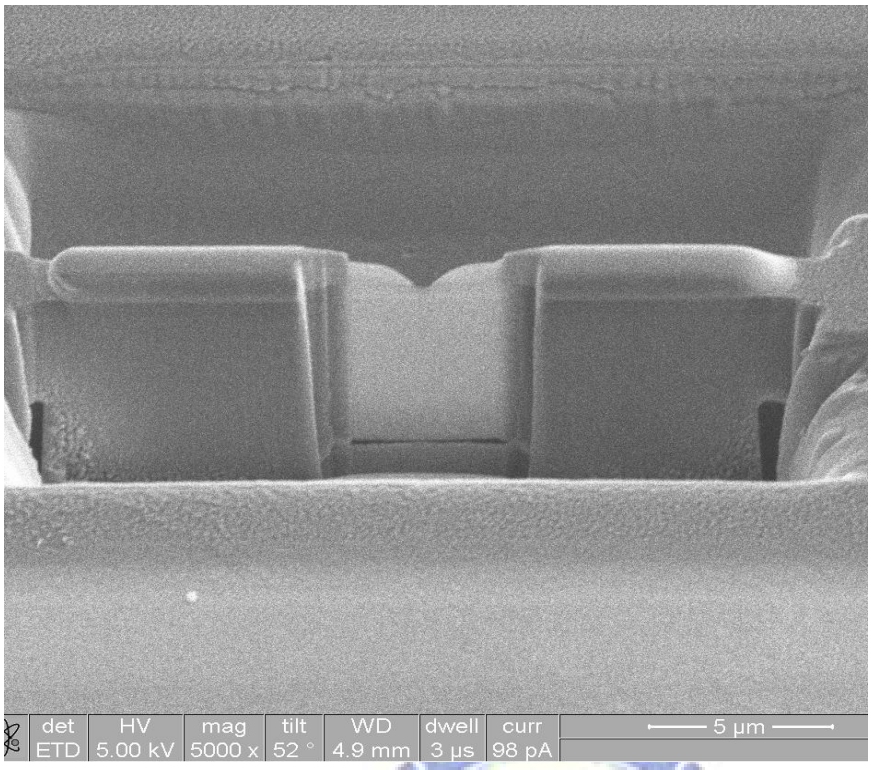


Fig. 2.16 The FIB cross-sectional images of Al_2O_3 inter-poly capacitors.

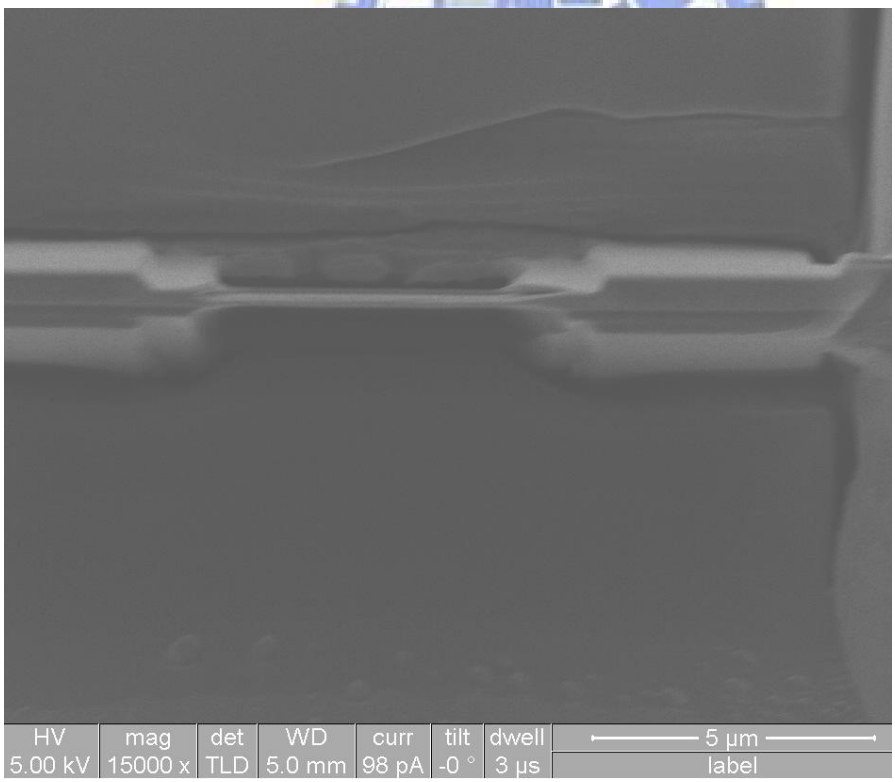


Fig. 2.17 The FIB top images of Al_2O_3 inter-poly capacitors thickness must be smaller than 500Å to do HRTEM.

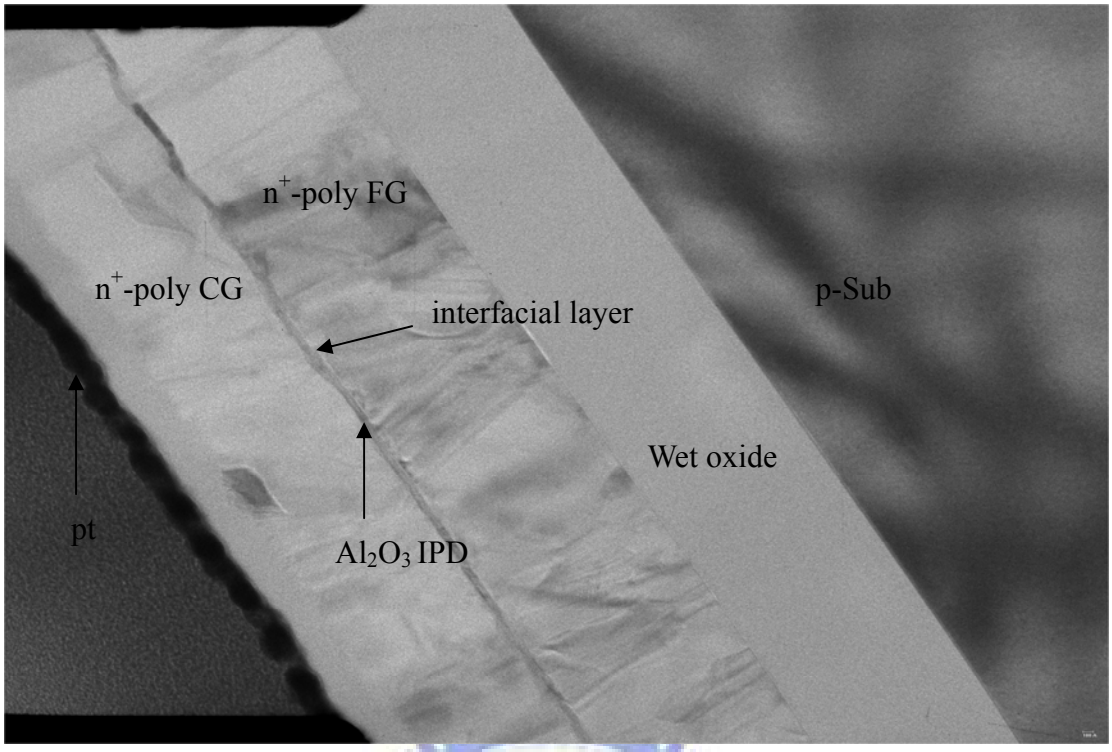


Fig. 2.18 The TEM all cross-sectional images of Al_2O_3 inter-poly capacitors.

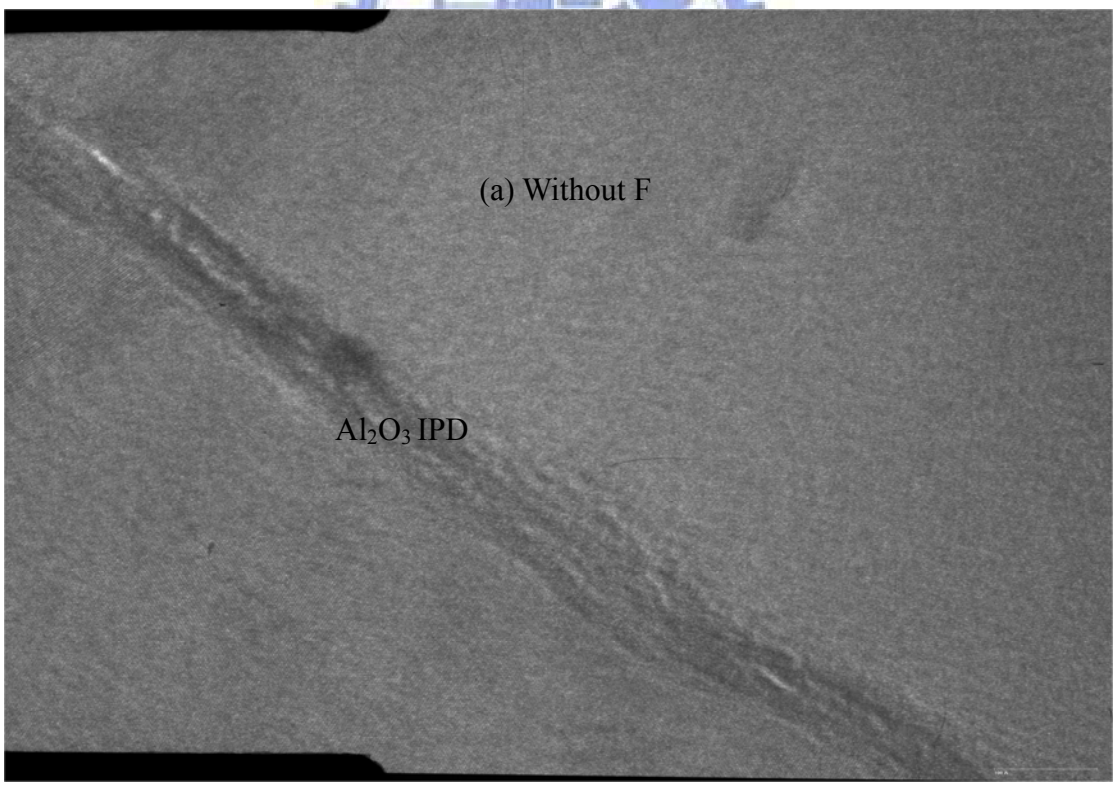
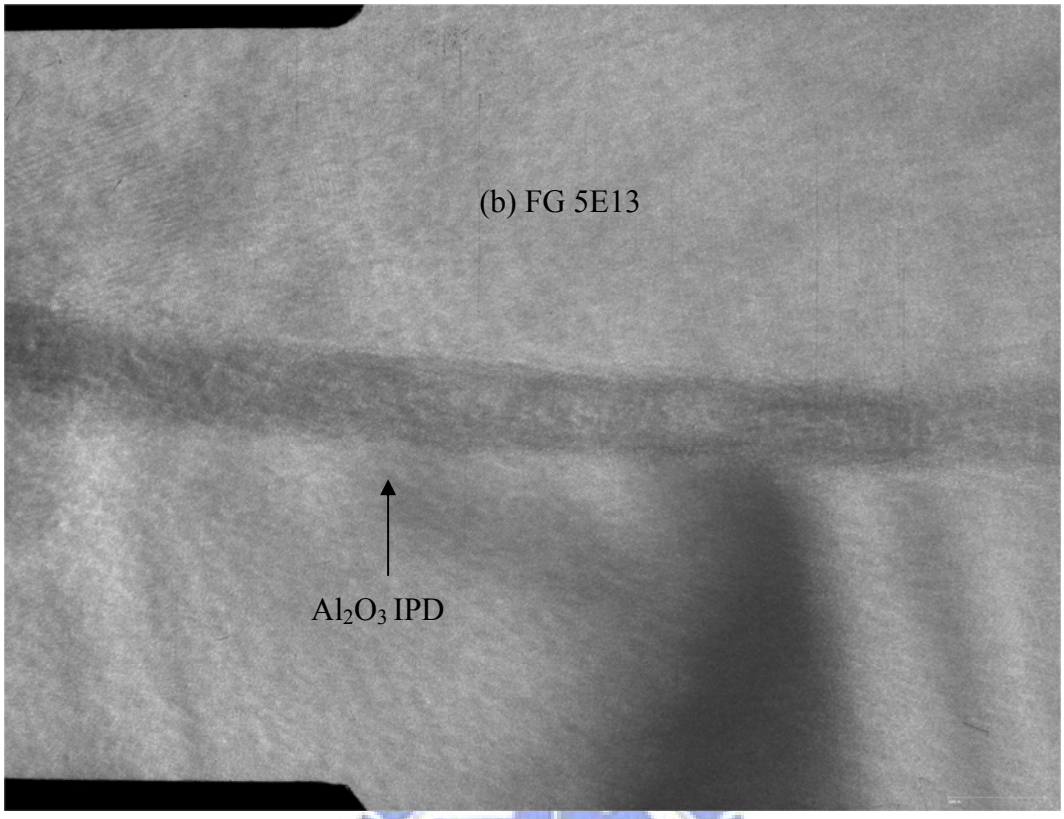
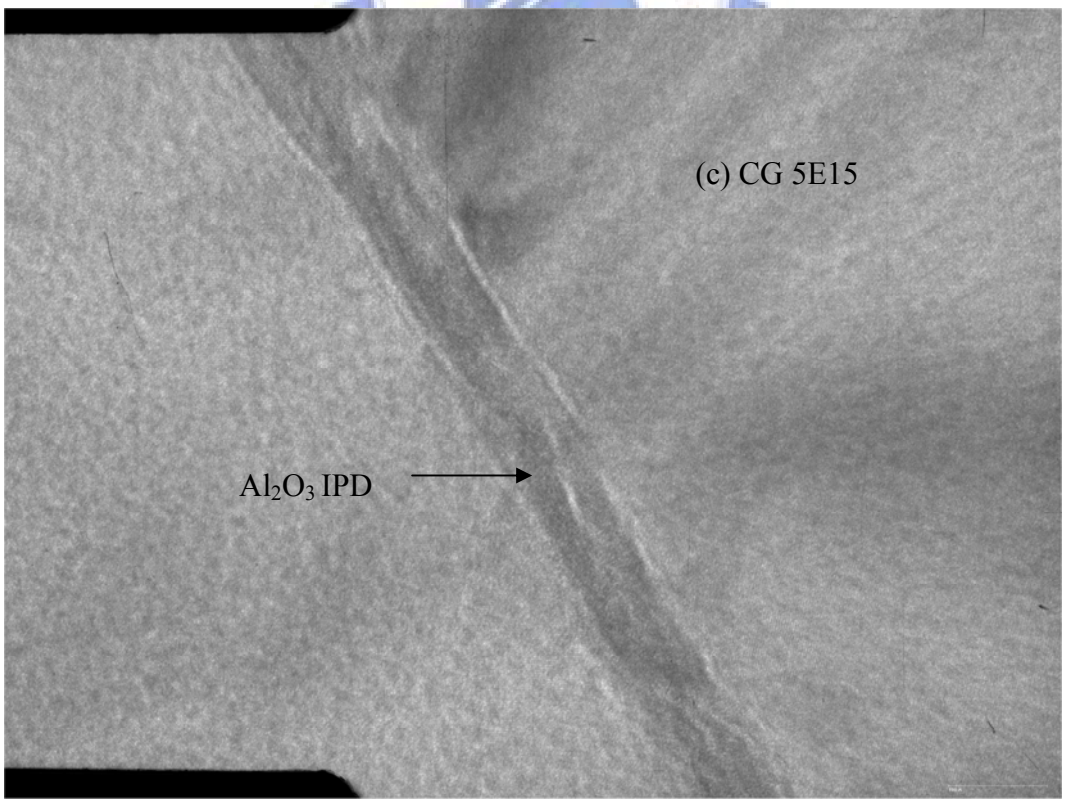


Fig. 2.19 The TEM cross-sectional images of Al_2O_3 inter-poly capacitors about 100Å ~120Å. (a) without fluorine. (b) FG with 5E13 cm^{-2} (c) CG with 5E15 cm^{-2}.


(b) FG 5E13
Al_2O_3 IPD


(c) CG 5E15
Al_2O_3 IPD

CHAPTER 3

Characteristics of HfO_2 Inter-Poly Dielectrics with Fluorine Passivation

3.1 Introduction

In the recently, for pursuing the high speed, short program/erase times and low control power operation of nonvolatile flash memories products, the employment of high-permittivity (k) inter-poly dielectrics (IPDs) into flash memories has attracted much attention. For EEPROM and flash memories devices, by increasing the fluorine passivation effect, high-k IPDs can lead to a high electric field across tunnel oxide even at very low control gate voltage. The high-k IPDs of fluorine passivation can increase charge retention, because of the barrier height (φ_B) between Si and the adopted high-k dielectrics should be large than 1.5eV for effectively suppressing the loss of floating gate charges through electron thermal emission. Usually, high-k IPDs with fluorine passivation can repair only high-k IPDs defects in flash memories. The effects of fluorine passivation on the electrical properties and reliability characteristics of the HfO_2 and Al_2O_3 inter-poly capacitors with polysilicom surface fluorine implantation are evaluated in this chapter.

Recently, flash memories with high-k dielectrics such as aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) have been studieds intensively. However, investigation of HfO_2 material with fluorine passivation is new science and technology in recent years. This thesis will find best fluorine implantation dosage and discuss some electrical

property. The high dielectric constant (high-k) material shows that fluorine atom implantation and combination of silicon are significant problem due to the passivation effect.[87] In addition, to find suit fluorine dosage is important for less or more dosage resulted in bad electrical characteristic. For this reason, the HfO_2 of fluorine passivation is expected to have higher capacitance, k-vale, EOT, effect breakdown field and reduced leakage current, breakdown voltage, electric trapping, improved charge-to-breakdown (Q_{BD}) and interfacial layer. Among these high-k materials, HfO_2 with fluorine passivation is a promising candidate, because of its compatibility with HfO_2 inter-poly dielectrics (IPDs) and tunnel dielectrics (TDs) on flash memories performance.

The most commonly reported high-k materials are ZrO_2, Al_2O_3 and HfO_2, that shown in Table1.1. Comparison of the high-k materials with HfO_2, HfO_2 has gained much attention as promising insulation. The reasons are briefly as follows.

(1) Suitable high dielectric constant：

The reported dielectric constant of HfO_2 is about 25~30. This magnitude of κ-value is higher than that of Si_3N_4 (κ~7) and Al_2O_3 (κ=8~11.5). It is not high enough to induce severe fringing-induced barrier lowering effect.

(2) Wide bandgap：

In general, as the dielectric constant increases, the bandgap decreases. The narrower bandgap would increase leakage current through thermal emission. The energy bandgap of HfO_2 is about 6.02eV, which is higher than the other high-κ materials such as Si_3N_4 and Ta_2O_5.

(3) Acceptable band alignment：

Band alignment determines the barrier height for electron and hole tunneling from gate or Si substrate. For SiO_2 the band offset of conduction band and valence band is ~9eV, and the barrier height for electrons is 3.1eV and the barrier height for holes is 4.7eV. The high band offset for both electron and hole has the benefit of low leakage current. Figure 1.4 shows the calculated band offsets for most high-κ dielectrics [88]. For HfO_2, barrier height for electron and hole is 1.6eV and 3.3eV, respectively. This band alignment is acceptable for nonvolatile memory requirement and better than other high-κ materials such as Ta_2O_5 [89].

(4) High free energy of reaction with Si：

For HfO_2, the free energy of reaction with Si is about 47.6 kcal/mole at 727ºC (see Table 1.1), which is higher than that of TiO_2 and Ta_2O_5. Therefore, HfO_2 is a more stable material on Si substrate as compared to TiO_2 and Ta_2O_5.

(5) High heat of formation：

Among the elements in IVA group of the periodic table (Ti, Zr, Hf), Hf has the highest heat of formation (271 kcal/mole). Unlike other silicides, the silicide of Hf can be easily oxidized. And it means that Hf is easy to be oxidized to form HfO_2 and the oxide of Hf is usually stable on Si substrate.

(6) Superior thermal stability with poly-Si：

Unlike ZrO_2, HfO_2 shows a good thermodynamic stability with poly-Si[90].[91] The HfO_2 would not react easily with poly-Si in high temperature as ZrO_2 [92].

According to these profits discussed above, we choose HfO_2 as one of the major high-κ IPDs in our investigation for next decade flash memories.

3.2 Experimental Details

The n^+-polysilicon/ HfO_2 IPD/n^+-polysilicon capacitors were fabricated on 6-inch p-type (100)-oriented silicon wafers. Silicon wafer was thermally oxidized at 980°C to grow a 2000Å buffer oxide. 2000Å bottom polysilicon film (Poly-I) was deposited on the buffer oxide by low pressure chemical vapor deposition (LPCVD) system using SiH_4 gas at 620°C and subsequently implanted with phosphorous at 5e15cm^{-2}, 20keV and implanted with fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV .then activated with N_2 RTA at 950°C for 30s. Prior to the growth of Al_2O_3 IPDs, the native oxide covered Poly-I was cleaned by the conventional RCA cleaning and diluted HF etching in sequence for the removal of particles and native oxides. The surface of Poly-I prepared in this matter was known to be contamination free and terminated with atomic hydrogen. After being wet cleaned and dipped in HF solution, and 10nm HfO_2 IPD was deposited by Metal-Organic Chemical Vapor Deposition (MOCVD) system at 500°C with Ar/O_2 ambient. Annealing of hafnium oxide (HfO_2) IPDs was carried out by rapid thermal annealing (RTA) at 950°C temperatures ranging in an N_2 atmosphere for 30s. Subsequently, a 2000Å top polysilicon layer (Poly-II) was deposited by LPCVD and implanted with phosphorous at 5e15cm^{-2}, 20keV. Then, implanted with fluorine dosage ranging from 5e13cm^{-2} to 1e15cm^{-2} at 20keV . Dopants were then activated with N_2 RTA at 950°C for 30s. Finally, 5000Å TEOS oxide passivation and Al metal pads were defined. The cross-sectional view and key process steps of HfO_2 inter-poly capacitor with fluorine passivation effect are show the in Fig. 3.1 and 3.2, respectively.

The equivalent oxide thickness (EOT) was obtained from the high frequency (1MHz) capacitance-voltage (*C-V*) measurement using a Hewlett-Packard (HP) 4284

LCR meter. Moreover, the physical thickness was estimated by high resolution transmission electron microscopy (HRTEM). The electrical properties and reliability characteristics of the inter-poly capacitors were measured using a HP4156C semiconductor parameter analyzer.

3.3 Results and comparison between Al_2O_3 and *HfO2*

In this chapter, the effects of fluorine passivation on the MOCVD Al_2O_3 IPDs and HfO_2 are compared in terms of EOT, κ-value, dosage-EOT, dosage-average breakdown current, effective breakdown field and 63%-failure Q_{BD} values and temperature under (a) Positive V_G (b) Negative V_G Floating Gate and Control Gate.

3.3.1 Basic Electrical Properties

A high capacitance density is important for using in memories store to increase the circuit density and reduce the cell area and lower cost. Therefore, adoption of high-k materials like Al_2O_3 and HfO_2 are a very efficient way to increase the capacitance density. The evidence is showed in Figure 3.3 (a) and (b) in HfO_2 IPD capacitors. By using silicon surface fluorine implantation (SSFI) method [93], the fluorine atoms inter polysilicon lattices and fluorine itself physical property, which causing increased capacitance. The EOT is decreased as raising Fluorine passivation effect, which can be ascribed to the interfacial layer (IL) thickness suppression. The maximum k value of the experiment with Al_2O_3 and HfO_2 are 9.3 and 14.6 in floating gate. And such, control gate are 15.8 and 13.8 value, respectively. Average EOT of HfO_2 IPD capacitors show in Figure 3.4 (a) floating gate (b) control gate (c) floating

gate and control gate compared. In general, as the dielectric constant increases, the bandgap decreases. The narrower bandgap would increase leakage current through thermal emission. So, we know that HfO_2 is higher k value than Al_2O_3, that Al_2O_3 is more capacitance density. On other hand in Figure 3.5 and Finger 2.10 Comparison of HfO_2 IPD and Al_2O_3 IPD capacitors with surface fluorine passivation under floating gate and control gate. The coupling rate formula in Figure 3.6 as follows.

(1) control gate > > floating gate

(2) (control gate / floating gate + control gate) ～1

By the coupling rate formula, Al_2O_3 IPD capacitors have coupling rate more efficiently than HfO_2 IPD capacitors.

3.3.2 Electric Field and Leakage Current Density Characteristics

Figure 3.7 depicts the effective breakdown field of HfO_2 inter-poly capacitors with surface fluorine passivation in different dosages under (a) floating gate (b) control gate. Both of floating gate and control gate are beneficial in suppressing low-field leakage current density, but floating gate is smaller than control gate. The factor is ascribed Hf-F than Si-F band slightly reduces interface dangling bonds and better performance. Figure 3.8 (a), (b), (c), (d) and Figure 3.9 (a), (b) show the dosage-average breakdown voltage images of HfO_2 capacitors, these image can evidence 5e13cm^{-2} and 1e15cm^{-2} are optimal dosage in floating gate and control gate, respectively. Compared Figure 3.10 and Figure 2.13, Al_2O_3 IPD capacitor is lesser low-field leakage current density than HfO_2 IPD capacitor. The result for two important focus. First, the HfO_2 IPD capacitor narrower bandgap would increase leakage current through thermal emission. Second, the lower barrier is caused electron tunneling and charge loss easily.

3.3.3 Relation of Trapping Density and Defect

Effects of fluorine incorporation on the reliabilities of stack-flash memories with SSFI have been studied. In this chapter, fluorine was incorporated during the poly implant step and was diffused into the poly/HfO_2 IPD interface during subsequent dopant activation. Figure. 3.11 (a) show the fluorine concentration and depth profiles with implantation [94]. Fluorine can easily penetrate the poly and HfO_2 IPD film and react on their interface. For explain, Figure. 3.11 (b) showed F tends to segregate at HfO_2/SiO_2 interface after FGA [95]. In the reason, F diffuses toward Poly/HfO_2 interface as HfO_2/SiO_2 . By this SSFI method, interface was incorporated with fluorine, and reach to repair defect of crystal in the bulk of HfO_2 IPD film. The effects include solving mobility degradation and threshold voltage instability, as well as reducing the number of dangling bonds and charge traps [96]-[99]. Figure 3.12 (c), (d) Control Gate adopted constant voltage stress (CVS) of HfO_2 IPD under (c) positive 2V (d) negative 2V trap densities. Low traps slope can be explained fewer defect and better performance. The fluorine atoms into Hf-based films were caused Hf-F and Si-F bands so as to improve quality of the film. These stronger bonds improve Fowler Nordheim (FN) tunneling and smoother interface, which results in less interface states generation and reduced traps of electron and hole in both polarities. The results clearly reveal HfO_2 IPD with polysilicon surface implantation, optimized control gate (CG) dosage was 1e15cm^{-2}, which can significantly reduce trapping rate and less bulk defect density compared without fluorine passivation samples. But in floating gate (FG), the fluorine passivation effect was not obviously, that can be ascribed to outdiffusion by rapid thermal annealing (RTA) three times, showed in Figure 3.12 (a) and (b).

3.3.4 Reliability Characteristics

In this part, the effect of fluorine incorporation into the Poly and Poly/ HfO_2 films on the charge-to-breakdown (Q_{BD}) distribution under Flowler-Nordheim (F-N) stressing was systematically studied. It was found that fluorine incorporation relaxes the lattices structure of interface, especially near Poly/ HfO_2 interface. In addition, appropriate fluorine incorporation can improve the Q_{BD} distribution of stacked-gate flash memories device, too. A straight line symbolizes has better quality film. The charge-to-breakdown with Weibull slope can be explained fewer defect and better performance. We also discussed a possible mechanism for the Q_{BD} distribution improvement.

Figure 3.13 (a), (b), (c) , (d) were shown Q_{BD} Weibull distributions of HfO_2 inter-poly capacitors with surface fluorine implantation at various fluorine dosages from FG and CG under constant current stress (CVS) in both polarities. Fluorine atoms were implanted into Poly and segregated into Poly and Poly/ HfO_2 interface by activation, respectively. The most effectively of fluorine dosage is 5e13cm^{-2} and 1e14cm^{-2} in FG and CG, respectively, and more about one to two order magnitude of enhancement in Q_{BD} compared without fluorine passivation. Excess fluorine incorporation caused outdiffusion and degraded not only the reliability of Poly/ HfO_2 interface but also dielectric-breakdown immunity, showed in floating gate 1e14cm^{-2}. Figure 3.14 (a), (b), we found, that appropriate fluorine 5e13cm^{-2} incorporation into Poly/ HfO_2 films (FG) could dramatically improve about one order Q_{BD} compared only poly (CG). HfO_2 Q_{BD} as lower value as HfO_2 leakage current density characteristics was compared to Al_2O_3 IPD film. The HfO_2 IPD film lesser about two order in $Q_{BD,}$ ascribed to two important focuses. First, HfO_2 material is narrower bandgap and the lower barrier without effectively suppressing the loss of charge

through electron thermal emission. Second, HfO_2 IPD arising from unsaturated interface bonds and other electrically active imperfections [100].

3.3.5 Temperature Characteristics of the fluorine passivation

In this part, the carrier transportation of poly gate with and without fluorine incorporation characteristics will by investigating. Figure 3.15 (a), (b), (c), (d) were shown temperature dependence of gate current density at 1.73 MV/cm of HfO_2 inter-poly capacitors with surface fluorine passivation that under floating gate and control gate both polarities. The FG and CG leakage current increase with increasing measuring temperature under both poly-gate incorporation of fluorine, show obvious high temperature dependence. As the fluorine implant dosage increases to $5e13cm^{-2}$ and $1e15cm^{-2}$ during FG and CG, respectively. The increase in the effectively trapping level is easily observed, meaning that most of the shallow traps in HfO_2 IPD film with fluorine passivation can effectively resist leakage current density in higher temperature. Besides, the low leakage current density can ascribe the bulk defect really perfect with fluorine repair. Comparing the with fluorine and without fluorine passivation samples, we find, the poly gate leakage current density of the SSFI HfO_2 IPD films is about one to two orders less than that of samples without any fluorine implantation in over 125℃. The schottky emission current of poly gate depended on temperature variation. However, because the barrier height extracted from Schottky emission is larger than the trap energy extracted from Fowler Nordheim (F-N) conduction. The higher temperature result in Schottky emission.

In addition, the evidences are shown in Figure 3.16 (a), (b) and Figure 2.15 (a), (b) images. As best as most other electrical properties of Al_2O_3 capacitors, Al_2O_3 films

is more about two orders thermal stability compared to HfO_2 films. Table 1.1 show both of HfO_2 and Al_2O_3 IPDs have good thermodynamic stability with poly-Si in high temperature. The high heat of formation, Al_2O_3 films has the highest heat of formation (399 Kcal/mole) than HfO_2 films (271 Kcal/mole), the mean are not be oxidized easily. Besides, Al_2O_3 films for free energy chemical reduction function is (63.4 Kcal/mole) higher than that HfO_2 films (47.6 Kcal/mole), causing Al_2O_3 IPDs more thermal stable about one order compare with HfO_2 IPD. By the result, the thermal stability of HfO_2 IPDs and Al_2O_3 IPDs both are much improved owing to the incorporation of fluorine.

3.4 Summary

In this thesis, we demonstrate that incorporation of SSFI method by N_2 950℃ RTA activation after HfO_2 IPDs deposition remarkably improves inter-poly dielectrics behavior such as significantly less EOT, charge trapping rate and interface states generation. We found that fluorine tends to segregation into the poly/ HfO_2 and poly interface and fluorine atoms diffusion into lattice generation strong Si-F, Hf-F and Al-F bonds compared to Si-H, Hf-H and Al-H. Both floating gate and control gate compare, we evidence that fluorine more effective passivation at poly/ HfO_2 (FG), beside C-V, EOT and k value characteristics. Flash memories with Al_2O_3 IPDs and HfO_2 IPDs can clearly exhibit significant improvement in data retention, leakage current and charge-to-breakdown (Q_{BD}) to replace conventional silicon oxide or oxide/nitride/oxide (ONO) IPDs. Table 3.1 lists several physical and electrical parameters, including EOT, κ-value, interfacial layer thickness, effective breakdown field and 63%-failure Q_{BD} values of the HfO_2 IPD capacitors with surface fluorine passivation under positive and negative CVS at various fluorine dosage. After understanding flash memories trend need, the thesis is adopted as Al_2O_3 IPDs and HfO_2 IPDs. The fluorine passivation effect of Al_2O_3 IPD and HfO_2 IPD had been

proved as promising candidates for the gate dielectrics of 45nm and 32nm generation stacked-gate flash memories device.

As the HfO_2 IPD capacitors process had completed the work. We used high-resolution transmission electron microscopy (HRTEM) to confirm HfO_2 IPD thickness and interfacial layer thickness. Before HRTEM, We must be cutting and digging a hole with focused ion beam (FIB). Figure.3.17 shows the FIB cross-sectional images of HfO_2 IPD capacitors. The FIB top images of HfO_2 inter-poly dielectric device thickness must be smaller than 500Å to do HRTEM. After finishing FBI, Figure. 3.18 show the TEM all cross-sectional images of HfO_2 inter-poly dielectric. The HfO_2 dielectric thickness is about 120 Å ~150Å. Figure. 3.19 show FG with 5E13cm^{-2}. Sample not only smoothes interface but also reduces interfacial layer thickness.

Table 3.1 EOT, κ-value, effective breakdown field and 63%-failure Q_{BD} values of the HfO_2 capacitors with surface fluorine passivation under positive and negative CVS at various fluorine dosage effects.

F Dosage (cm^{-2})	**κ**	**EOT (Å)**	**E_{BD} (MV/cm)**		**63% QBD (C/cm^2)**	
			positive	**negative**	**positive**	**negative**
0	**12.6**	**46.6**	**7.73**	**7.21**	**0.00271**	**0.0035**
FG 5E13	**14**	**4.16**	**9.04**	**8.07**	**0.0508**	**0.11742**
CG 5E15	**13.8**	**42.3**	**8.32**	**8.13**	**0.144**	**0.11065**

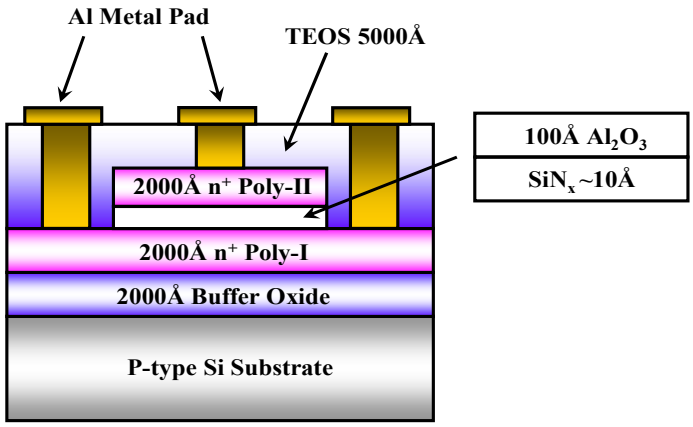


Fig. 3.1 Cross-sectional view of HfO_2 inter-poly capacitors with surface fluorine passivation. The fluorine was implanted on Poly-I (Floating Gate) and Poly-II (Control Gate).

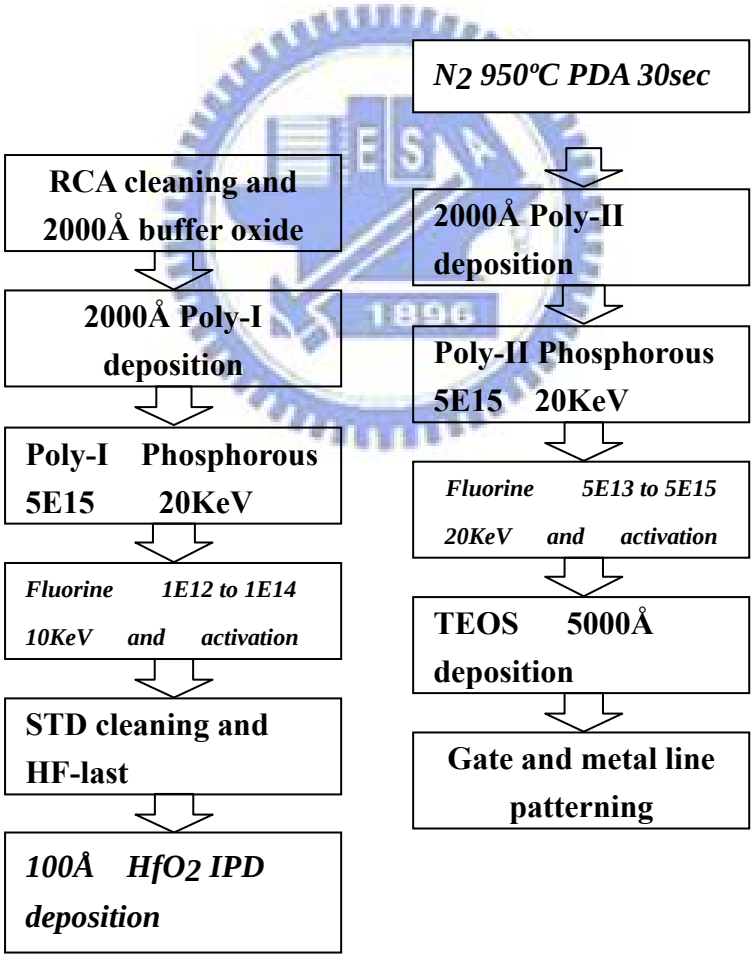
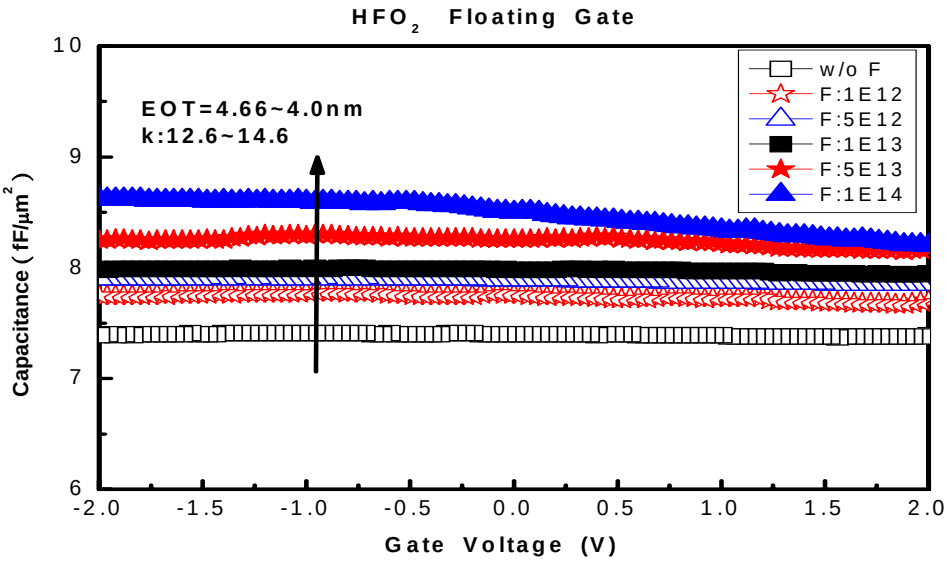
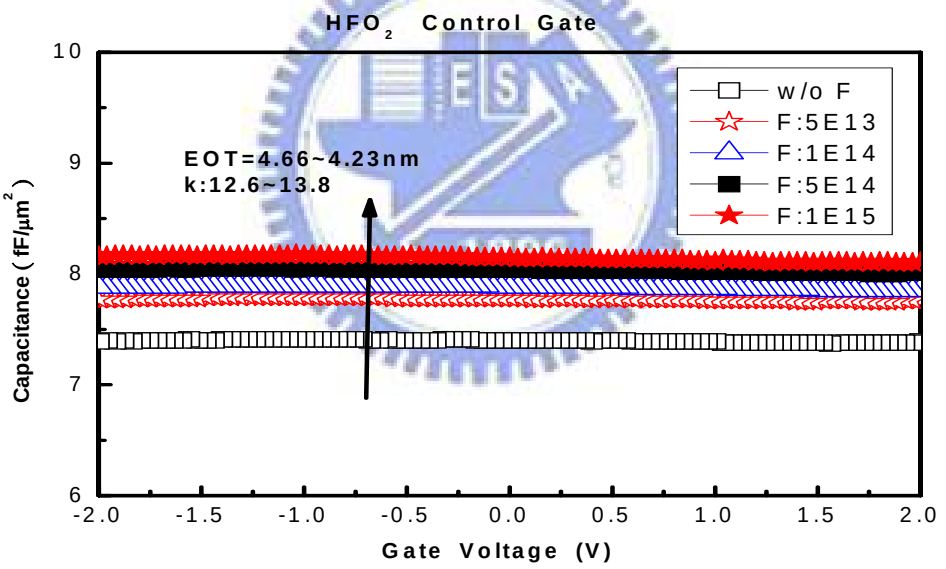


Fig. 3.2 Key process steps of HfO_2 inter-poly capacitors with surface fluorine passivation.

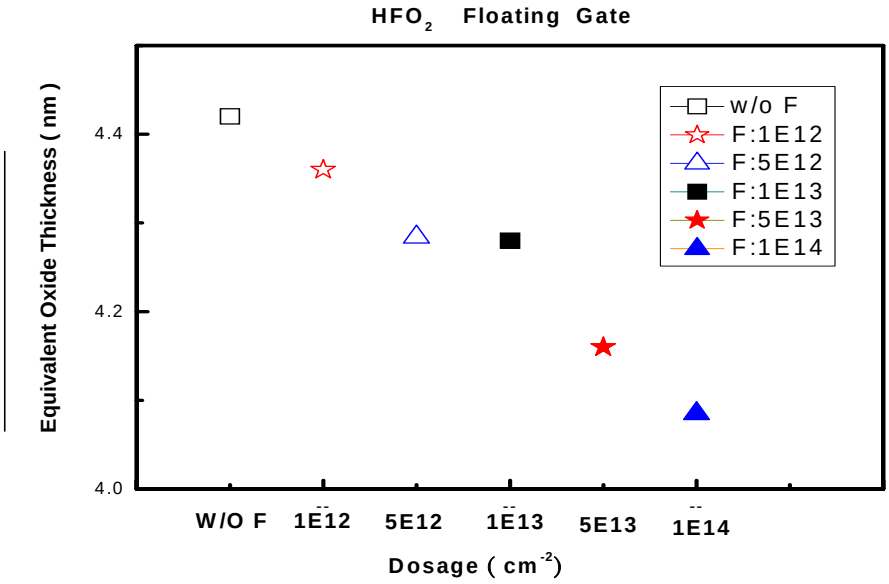


(a)

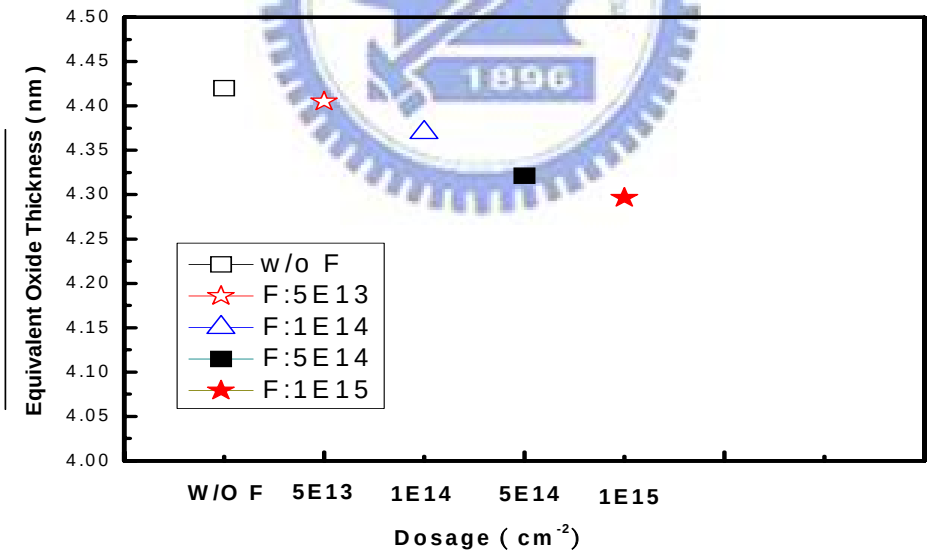


(b)

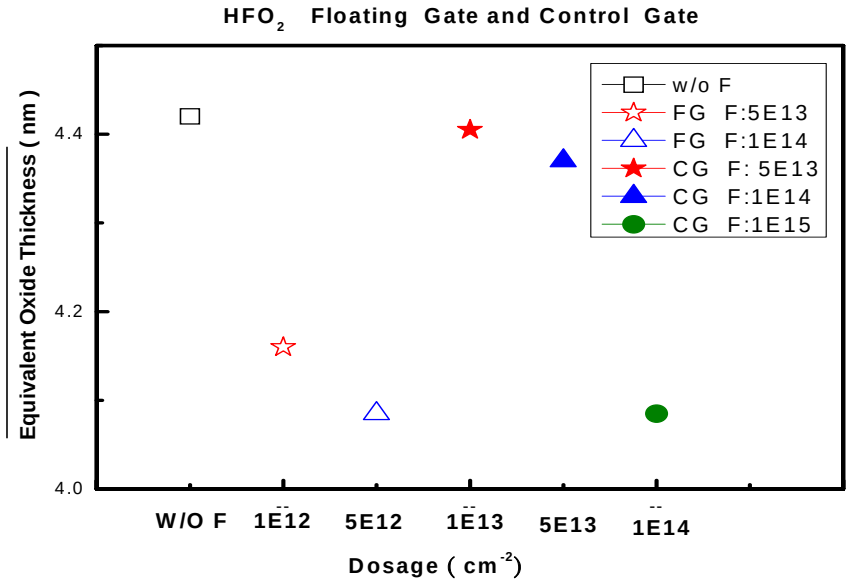
Fig. 3.3 (a) *C-V* characteristics of HfO_2 floating gate inter-poly capacitors with surface fluorine passivation effect is beneficial in scaling EOT that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV. (b) *C-V* characteristics of HfO_2 control gate inter-poly capacitors with surface fluorine passivation effect is beneficial in scaling EOT that fluorine dosage ranging from 5e13cm^{-2} to 1e15cm^{-2} at 20keV.


HFO2 Floating Gate
Equivalent Oxide Thickness (nm)
4.4
4.2
4.0
w/o F
F:1E12
F:5E12
F:1E13
F:5E13
F:1E14
W/O F
1E12
5E12
1E13
5E13
1E14
Dosage (cm-2)

(a)


HFO2 Control Gate
Equivalent Oxide Thickness (nm)
4.50
4.45
4.40
4.35
4.30
4.25
4.20
4.15
4.10
4.05
4.00
w/o F
F:5E13
F:1E14
F:5E14
F:1E15
W/O F
5E13
1E14
5E14
1E15
Dosage (cm-2)

(b)



(c)

Fig. 3.4 The average EOT of HfO_2 IPD capacitors with surface fluorine passivation under(a) floating gate (b) control gate (c) floating gate and control gate compared.

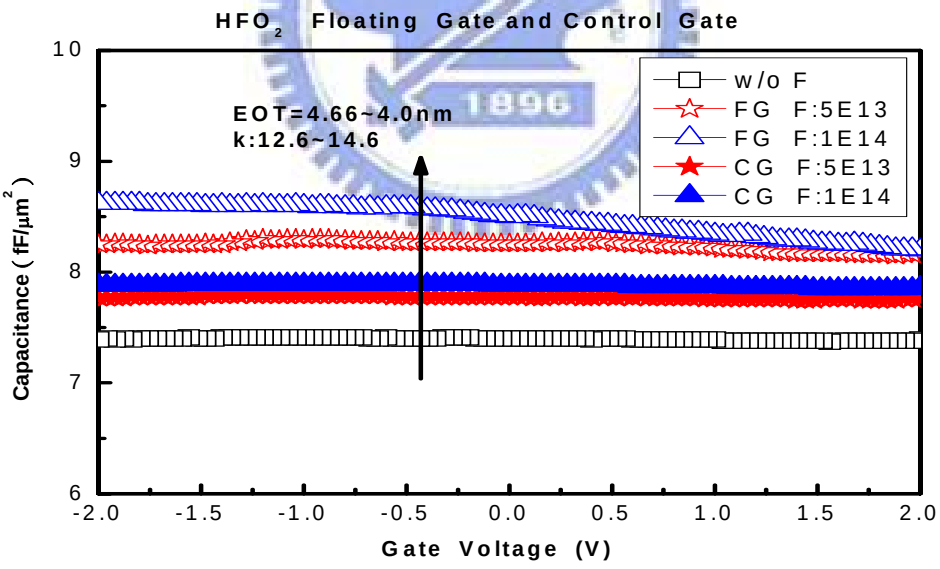
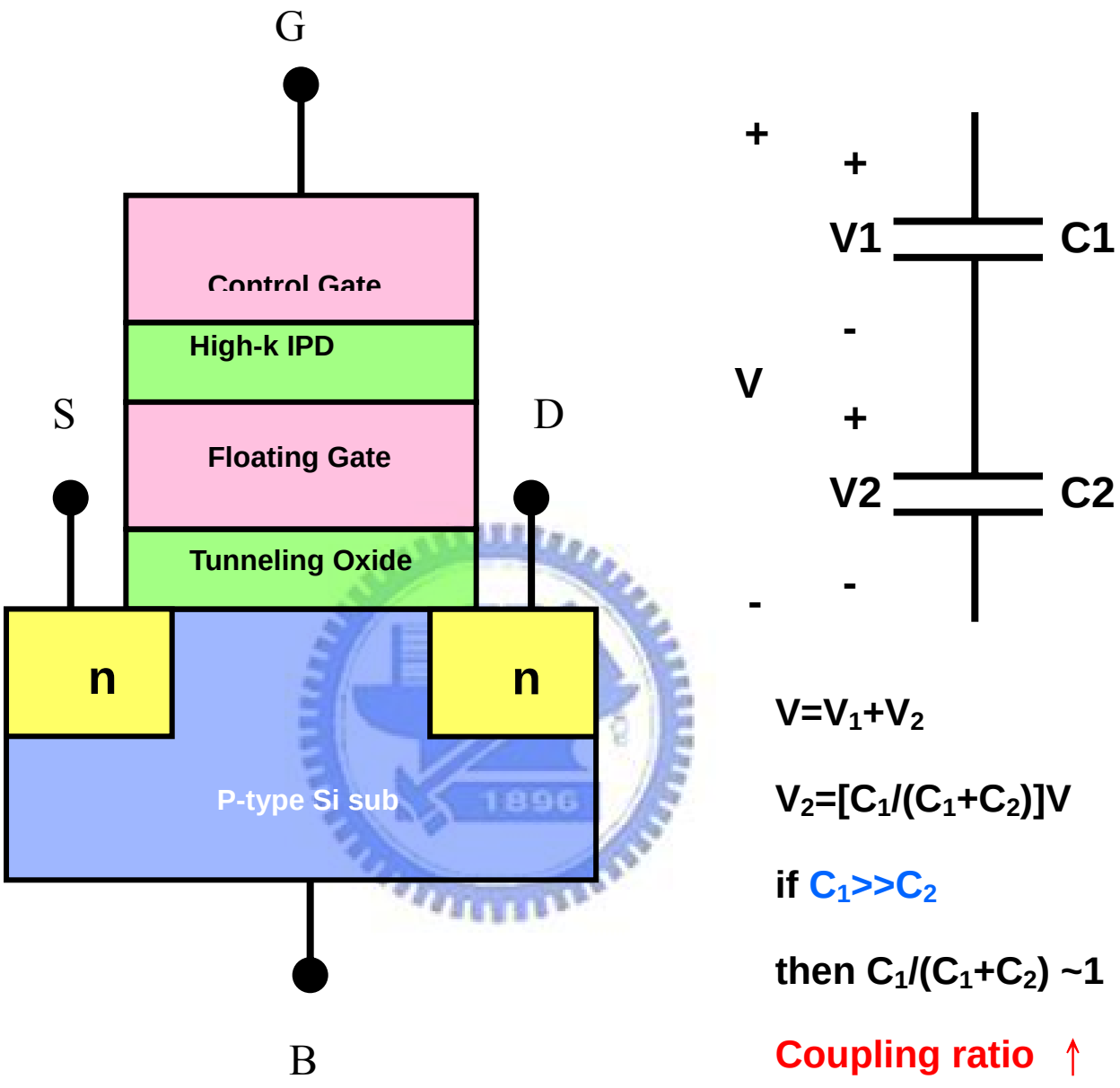


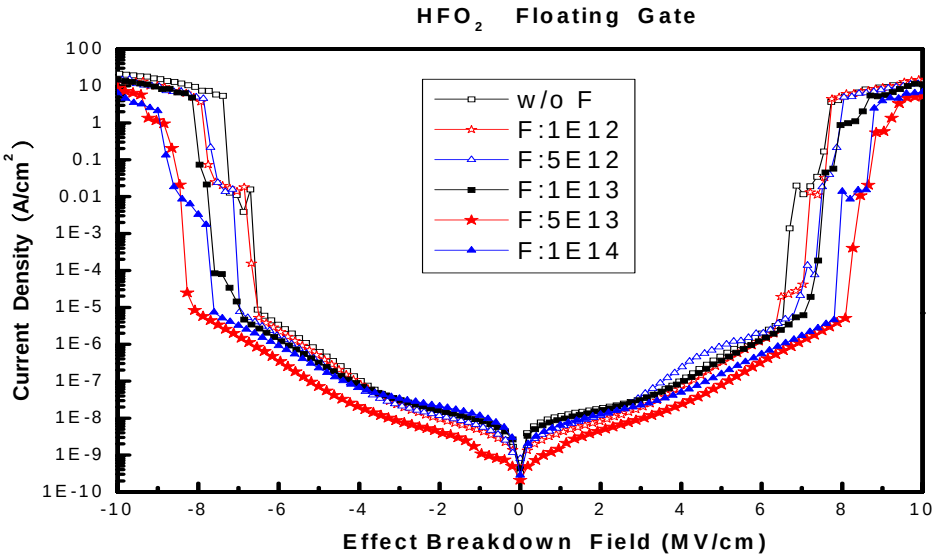
Fig. 3.5 The Capacitance of HfO_2 IPD capacitors with surface fluorine passivation under floating gate and control gate compared.

Stacked-gate Flash Structure

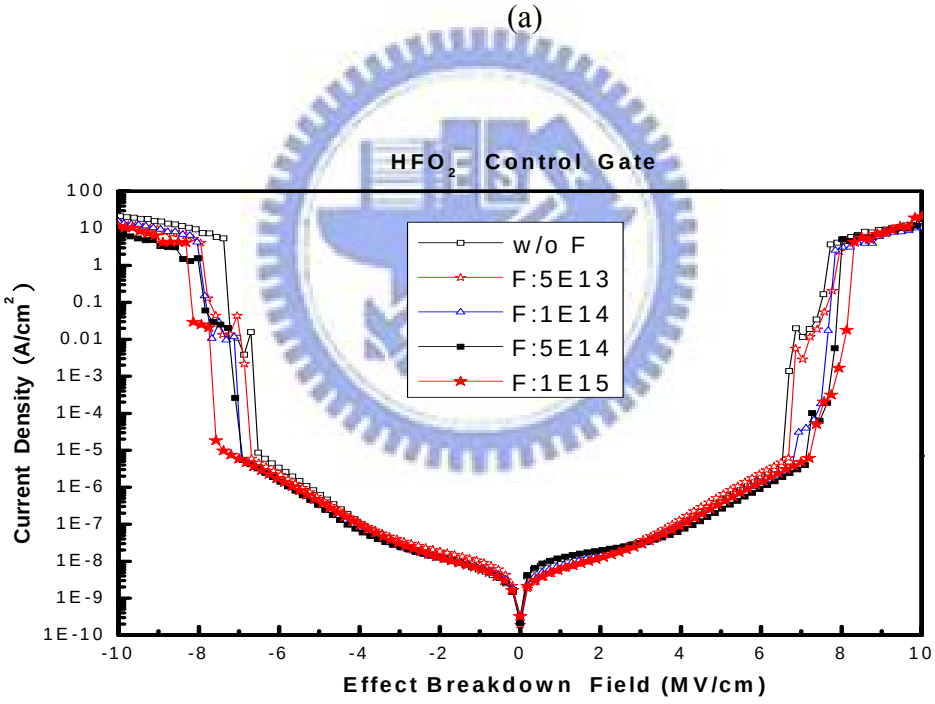


(a) (b)

Fig. 3.6 (a) The stacked-gate flash memories structure. (b) A formula for the IPD capacitors coupling ratio.



(a)



(b)

Fig. 3.7 (a) *J-V* characteristics of HfO_2 floating gate inter-poly capacitors with surface fluorine passivation effect is beneficial in suppressing low-field leakage current density that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV. Fig. 3.4 (b) *J-V* characteristics of HfO_2 control gate inter-poly capacitors with surface fluorine passivation effect is beneficial in suppressing low-field leakage current density that fluorine dosage ranging from 5e13cm^{-2} to 1e15cm^{-2} at 20keV.

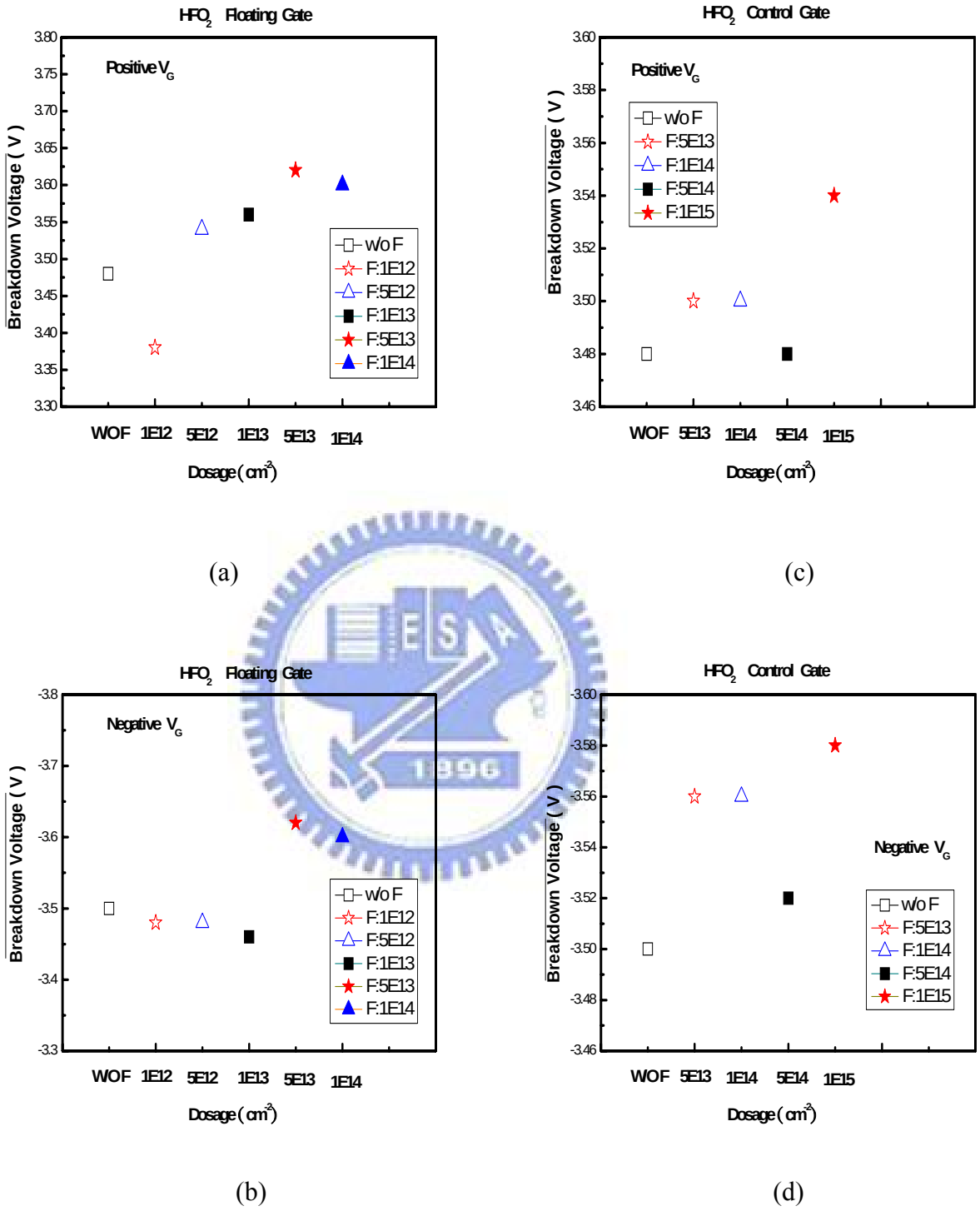
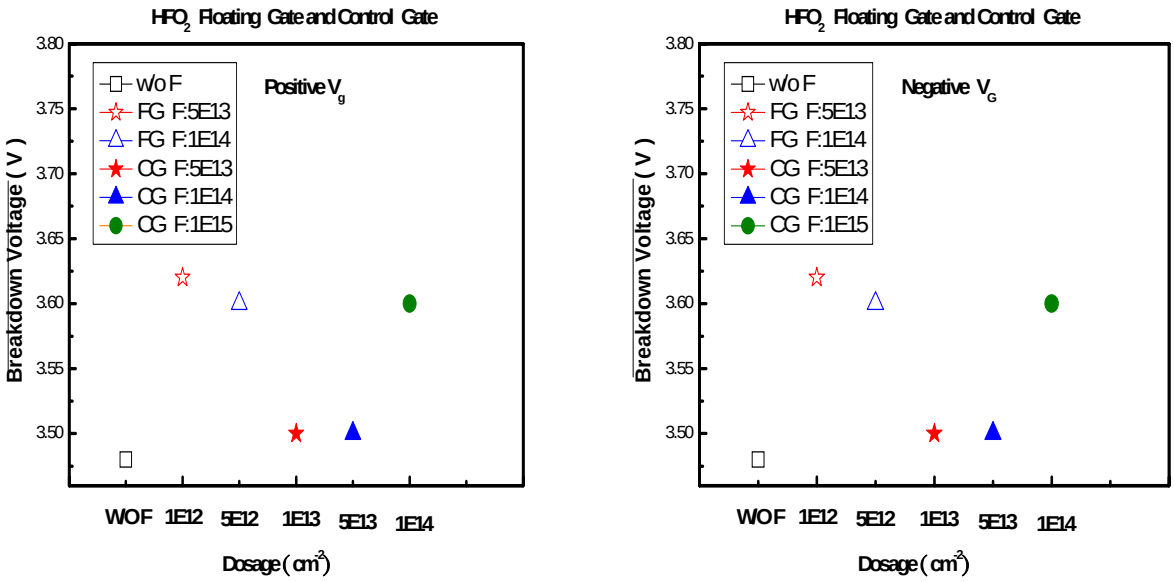


Fig. 3.8 The dosage-average breakdown voltage images of HfO_2 capacitors with surface fluorine passivation under (a) Positive V_G floating gate (b) Negative V_G floating gate (c) Positive V_G control gate (d) Negative V_G control gate.



(a) (b)

Fig. 3.9 The dosage-average breakdown voltage images of HfO_2 capacitors with surface fluorine passivation under (a) Positive V_G (b) Negative V_G floating gate and control gate comparison.

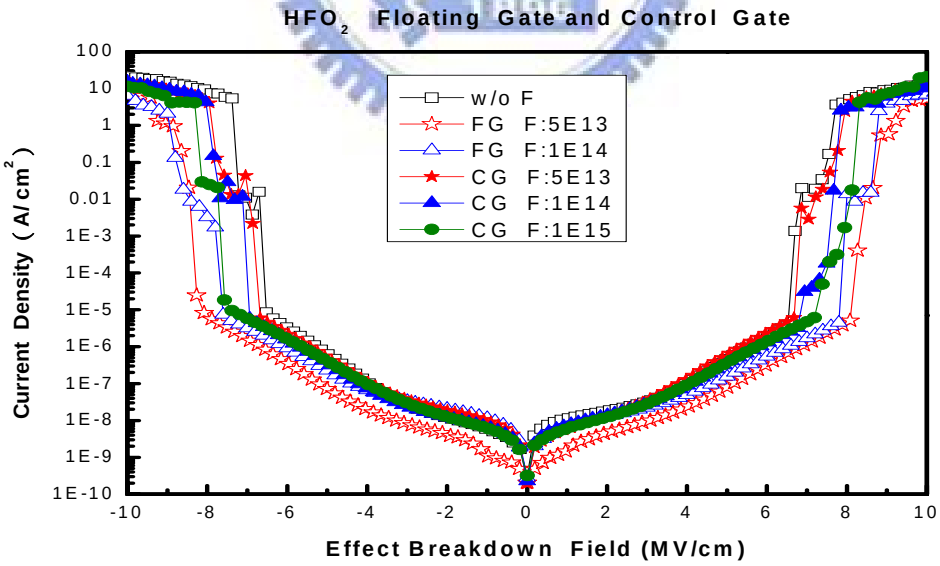
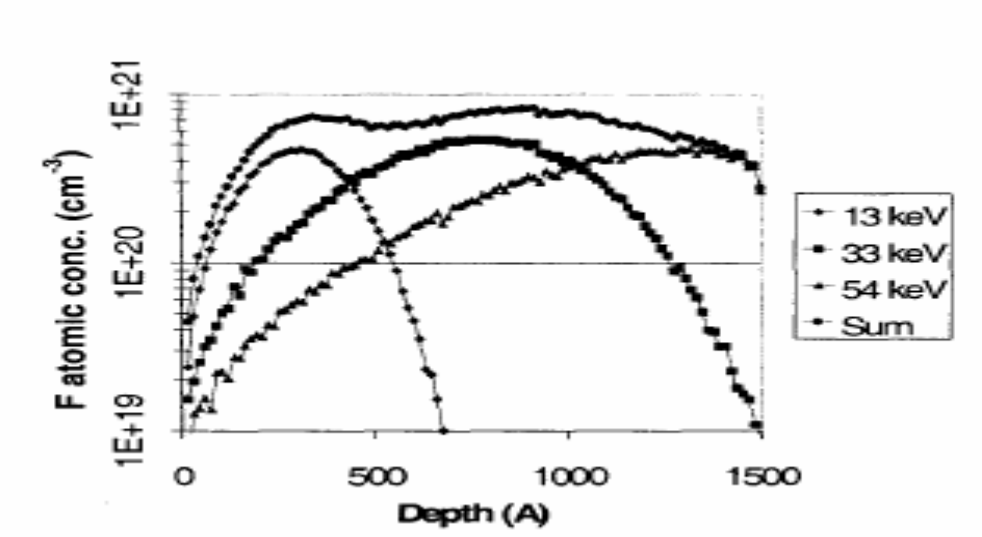
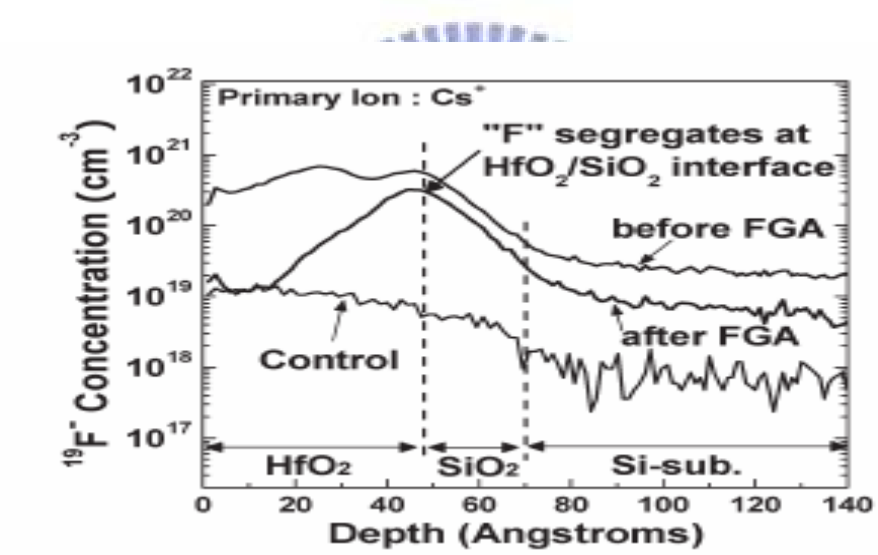


Fig. 3.10 The effective breakdown field of HfO_2 capacitors with surface fluorine passivation under floating gate and control gate comparison.

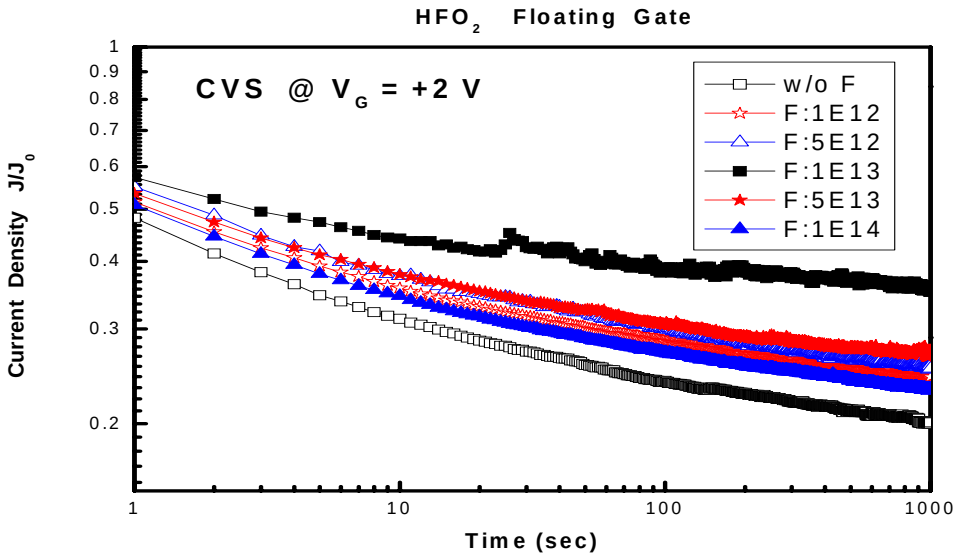


(a)

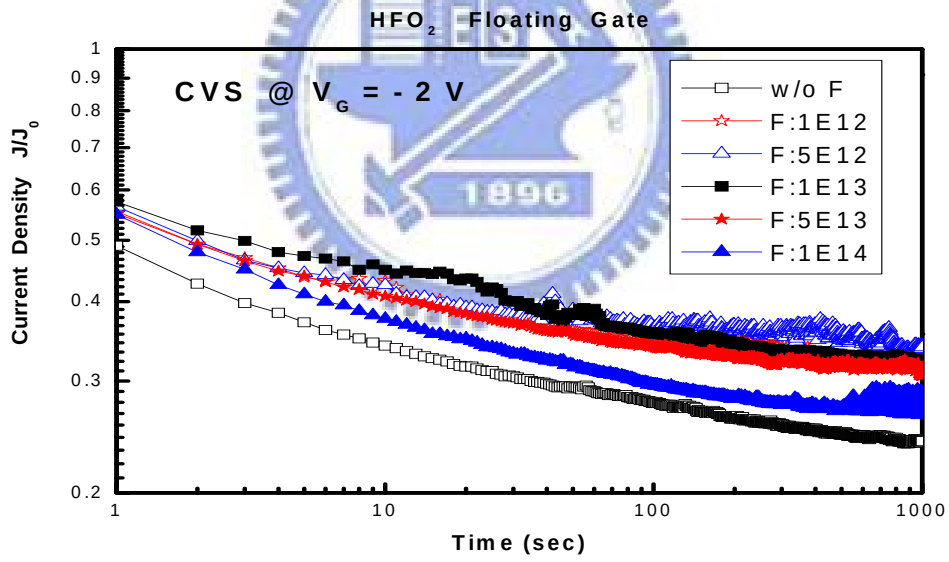


(b)

Fig. 3.11 (a) The fluorine concentration and depth profiles for the three individual implants, and their sum for 1% fluorine in 1500 SiO_2 film [94]. (b) SIMS depth profile of 19 F- in the local F sample before and after FGA (400℃, 30 min). F tends to segregate at HfO_2/ SiO_2 interface after FGA. F diffuses toward HfO_2/ SiO_2 interface [95].

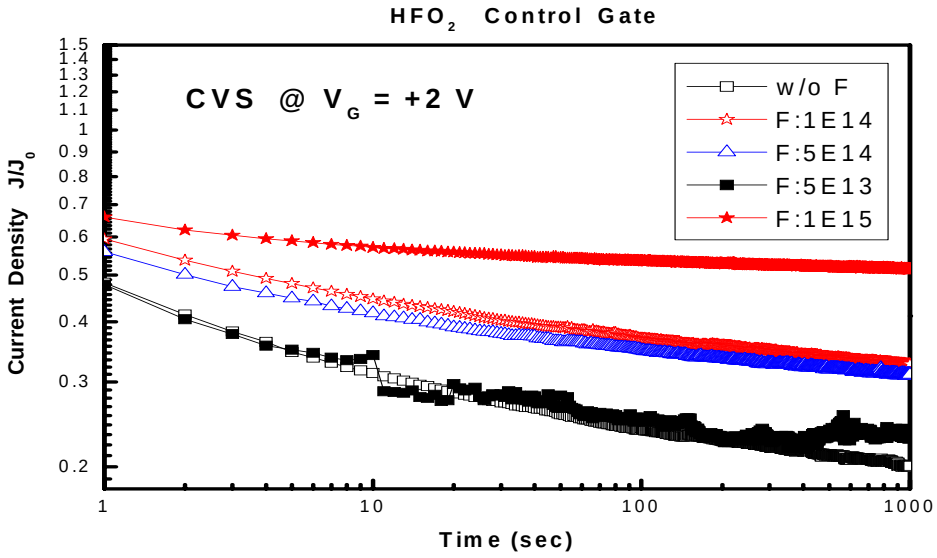


(a)

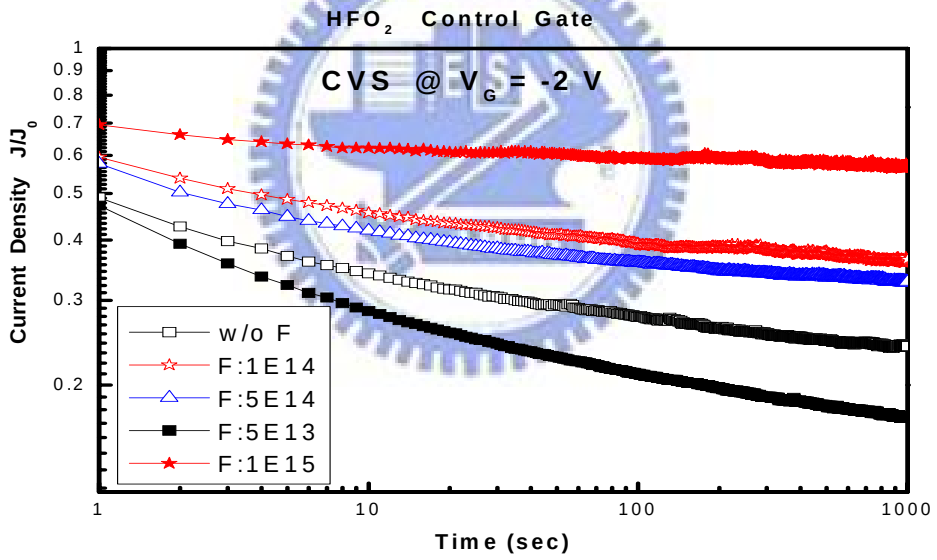


(b)

Fig. 3.12 As-fabrication trap densities evaluation at 2 V constant voltage stress (CVS) of HfO_2 Floating Gate inter-poly capacitors with surface fluorine passivation effect that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV under (a) positive 2V (b) negative 2V trap densities. The effect of fluorine passivation is bad than without fluorine passivation. Because of the process was outdiffusion by rapid thermal annealing (RTA) three time in Floating Gate.

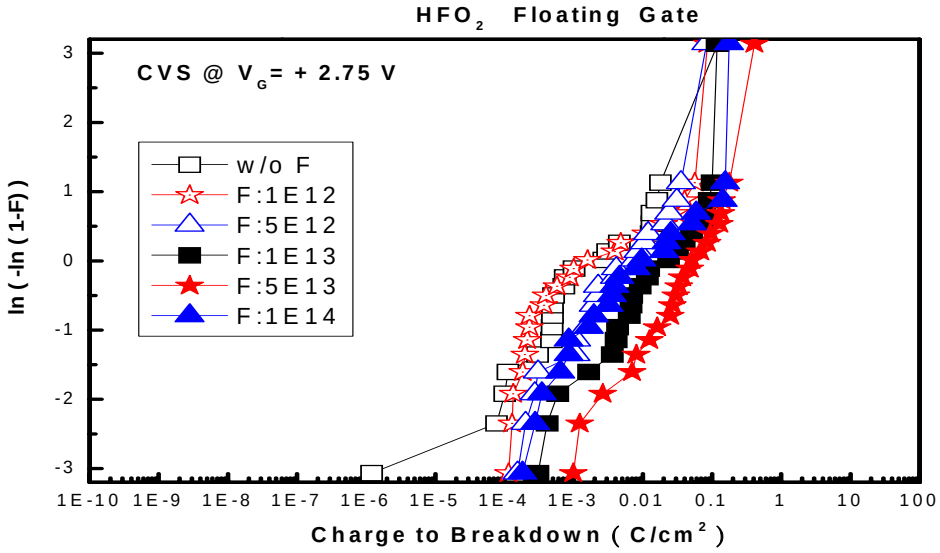


(c)

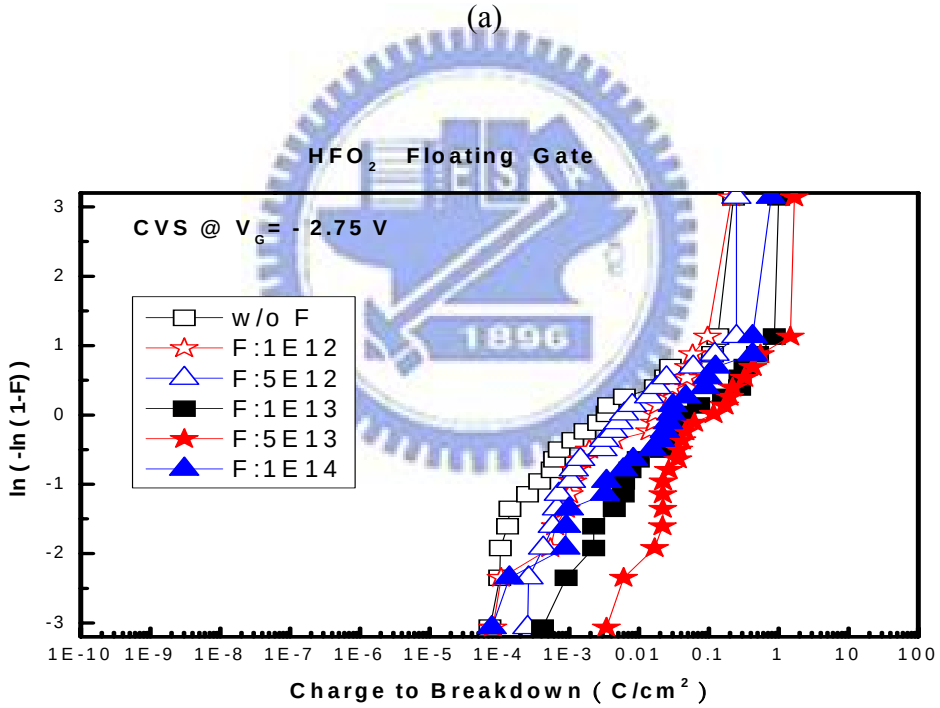


(d)

Fig. 3.12 As-fabrication Positive trap densities evaluation at 2 V constant voltage stress (CVS) of HfO_2 Control Gate inter-poly capacitors with surface fluorine passivation effect that fluorine dosage ranging from 5e13cm^{-2} to 1e15cm^{-2} at 20keV under (c) positive 2V (d) negative 2V trap densities. HfO_2 inter-poly capacitors with fluorine passivation can reduce As-fabrication trap densities.

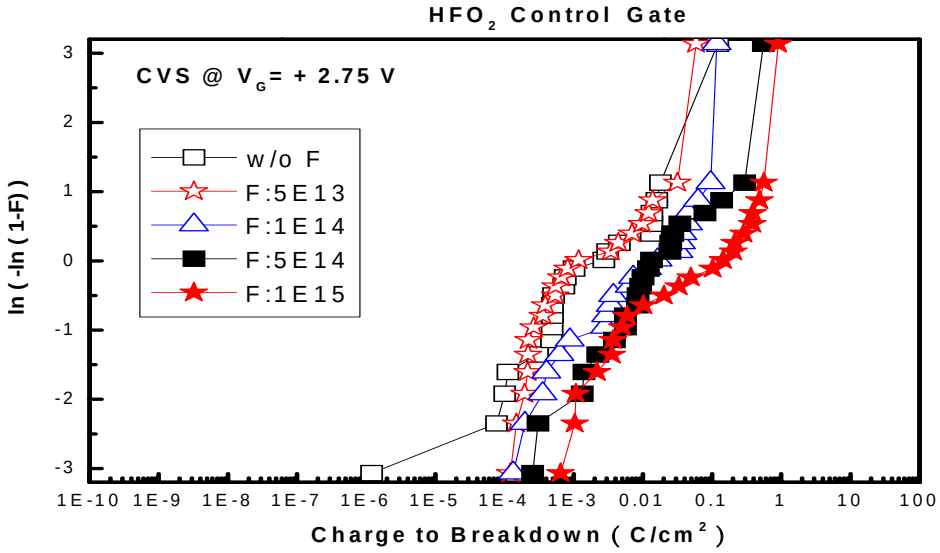


(a)

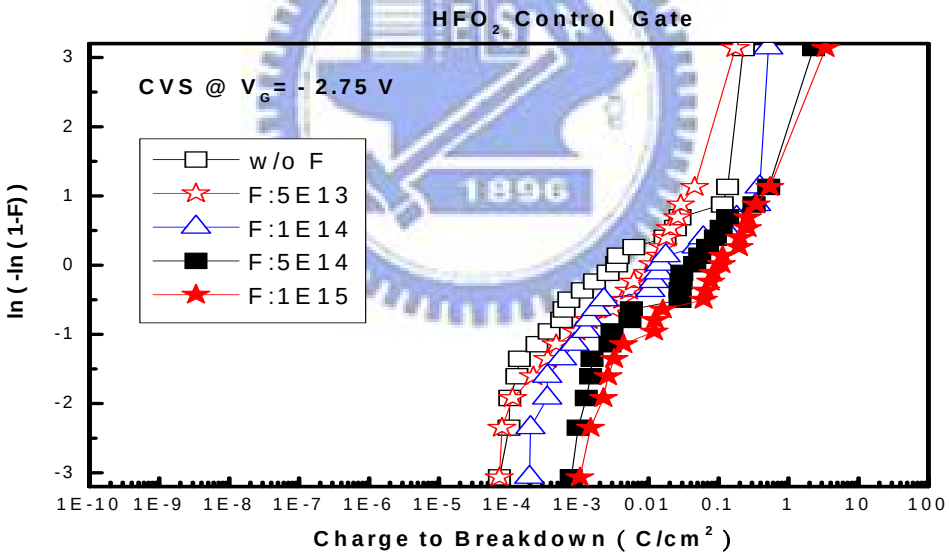


(b)

Fig. 3.13 Q_{BD} Weibull plots of HfO_2 inter-poly dielectric with surface fluorine passivation effect under (a) positive CVS and (b) negative CVS that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV . HfO_2 inter-poly capacitors with surface fluorine passivation effect can lightly increase Q_{BD} in Floating Gate .

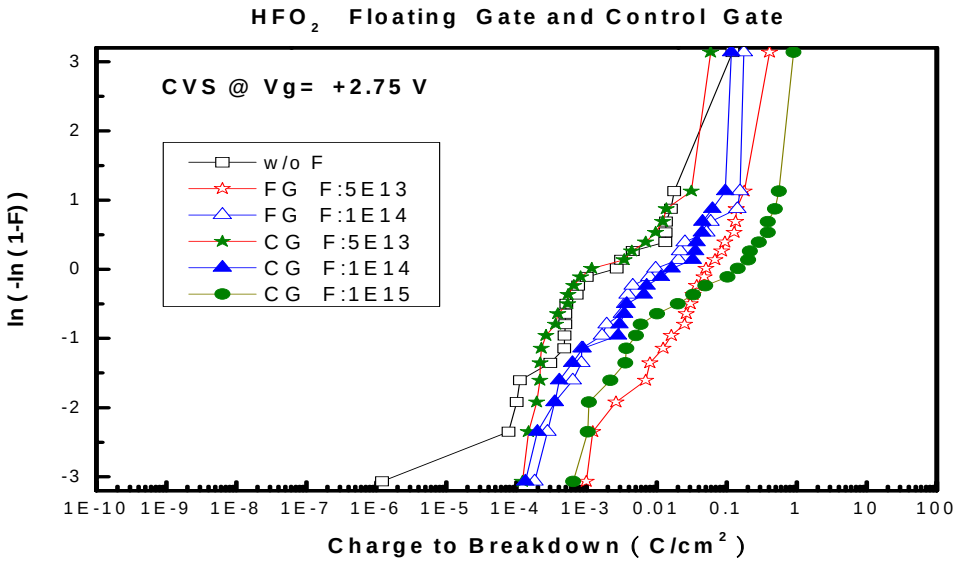


(c)

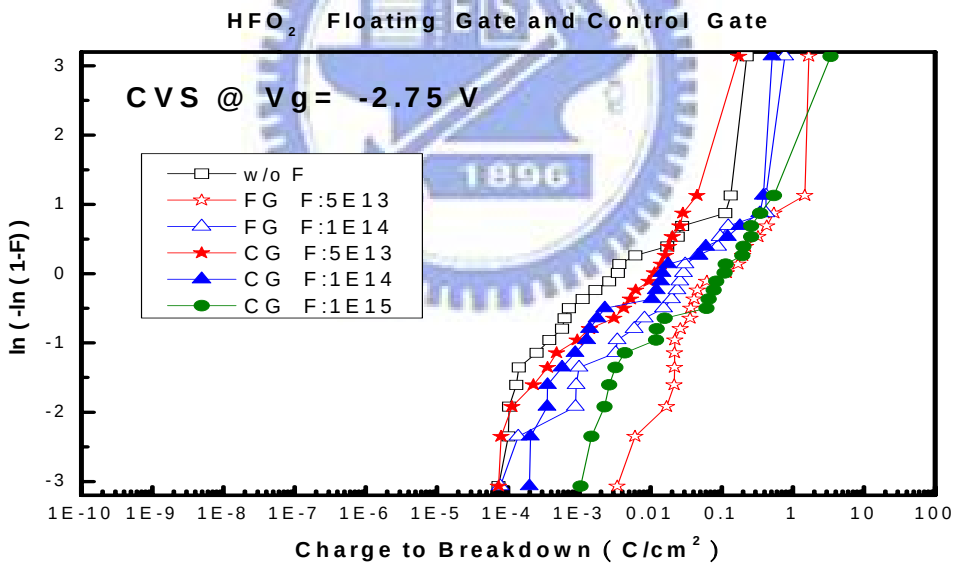


(d)

Fig. 3.13 Q_{BD} Weibull plots of HfO_2 inter-poly capacitors with surface fluorine passivation effect under (c) positive CVS and (d) negative CVS that fluorine dosage ranging from 5e13cm^{-2} to 1e15cm^{-2} at 20keV. HfO_2 inter-poly dielectric with surface fluorine passivation effect can significantly increase Q_{BD} in Control gate .

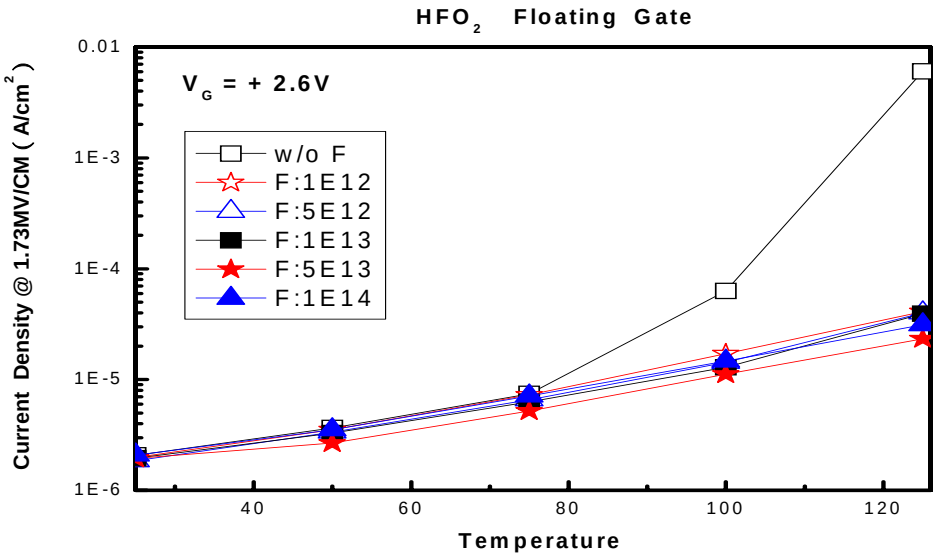


(a)

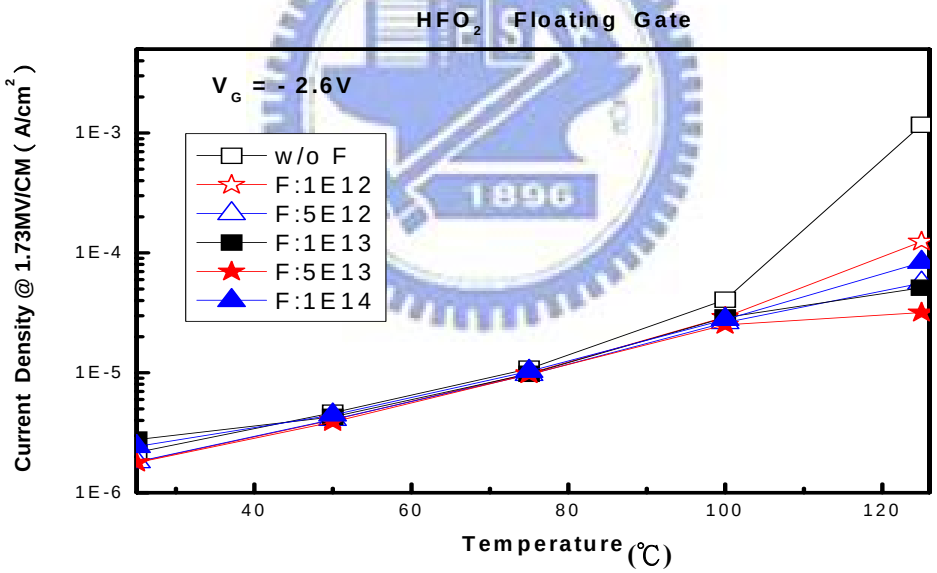


(b)

Fig. 3.14 The charge to breakdown (Q_{BD}) images of HfO_2 capacitors with surface fluorine passivation under (a) Positive V_G (b) Negative V_G floating gate and control gate compare.

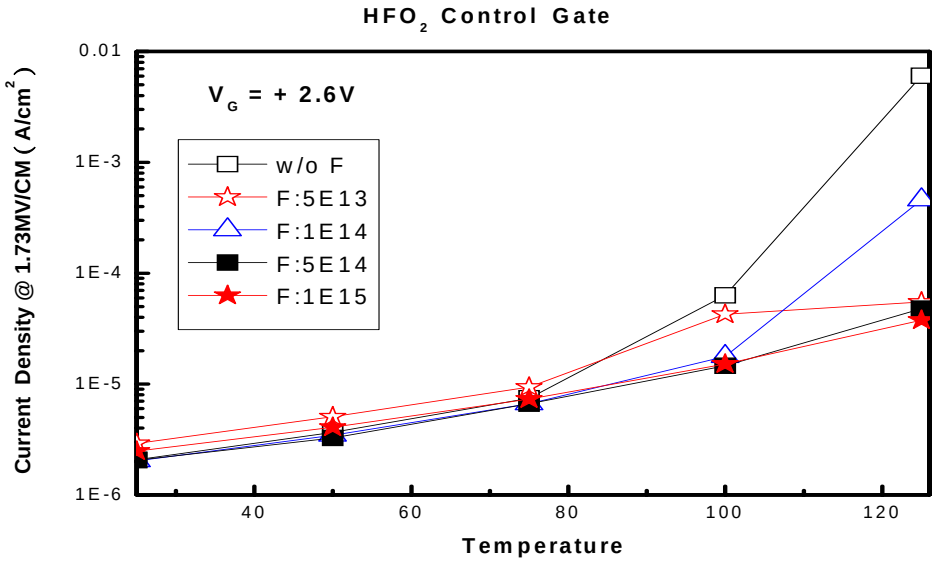


(a)

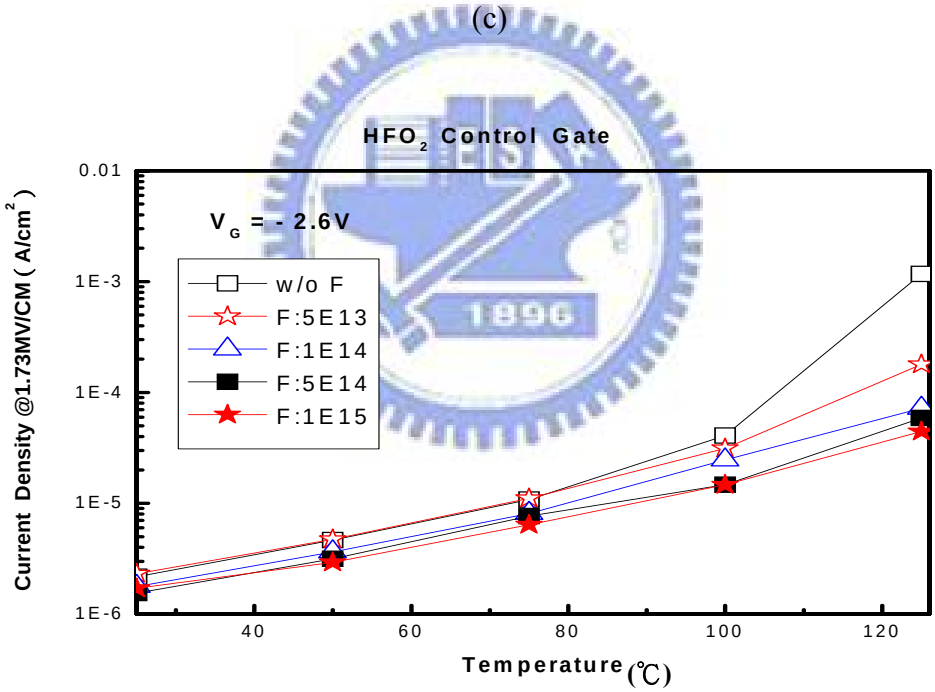


(b)

Fig. 3.15 Temperature dependence of gate current density at 1.73 MV/cm of HfO_2 inter-poly capacitors with surface fluorine passivation that fluorine dosage ranging from 1e12cm^{-2} to 1e14cm^{-2} at 10keV in Floating Gate under (a) positive and (b) negative polarities.

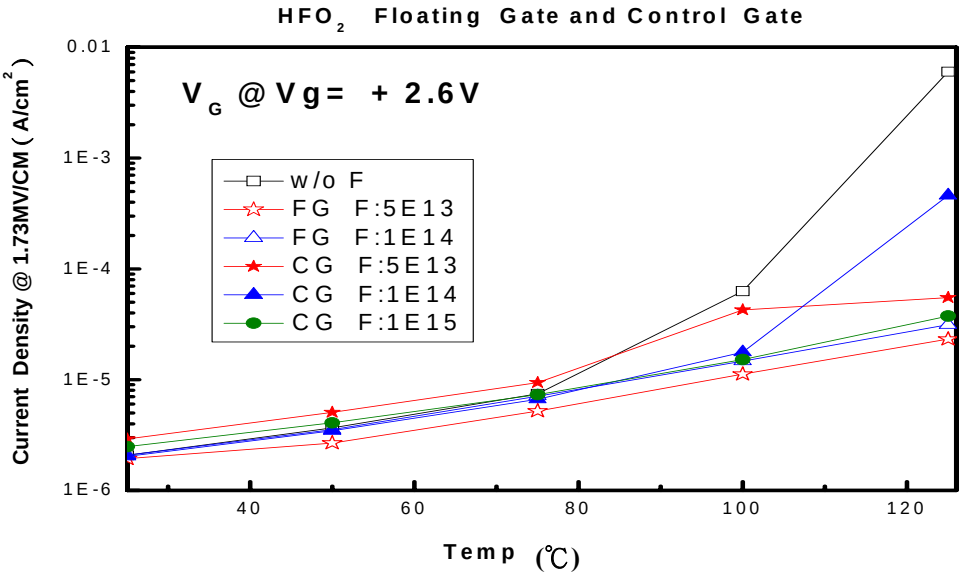


(c)

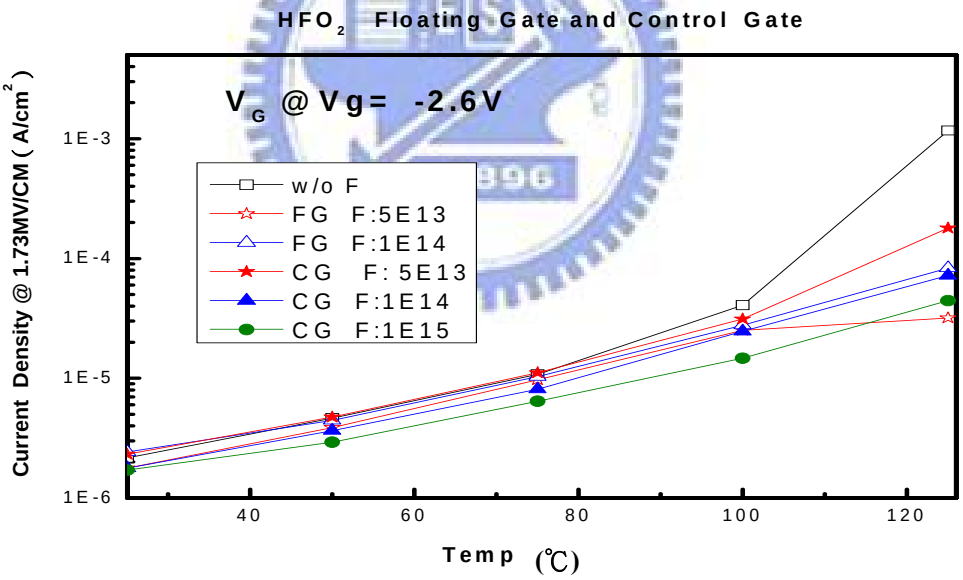


(d)

Fig. 3.15 Temperature dependence of gate current density at 1.73 MV/cm of HfO_2 inter-poly capacitors with surface fluorine passivation that fluorine dosage ranging from 5e13cm^{-2} to 1e15cm^{-2} at 20keV in Control Gate under (c) positive and (d) negative polarities.



(a)



(b)

Fig. 3.16 The Temperature images of HfO_2 capacitors with surface fluorine passivation under (a) Positive V_G (b) Negative V_G floating gate and control gate compare.

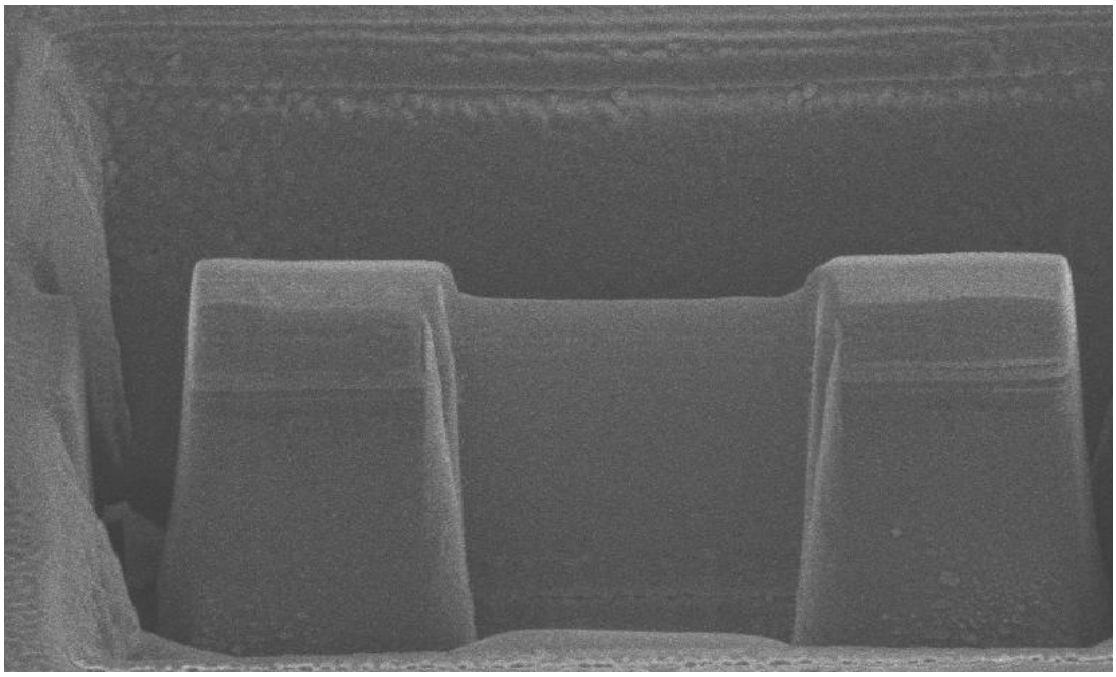


Fig. 3.17 The FIB cross-sectional images of HfO_2 inter-poly capacitors.

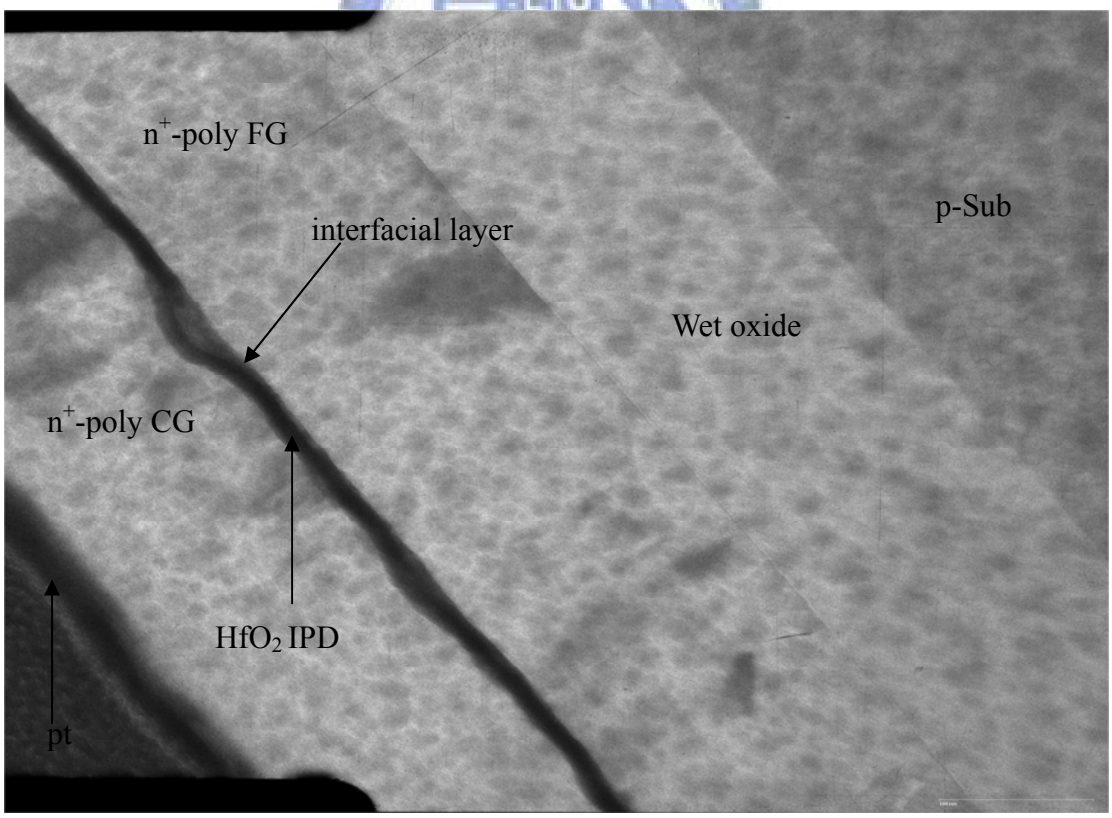


Fig. 3.18 The TEM all cross-sectional images of HfO_2 inter-poly capacitors.

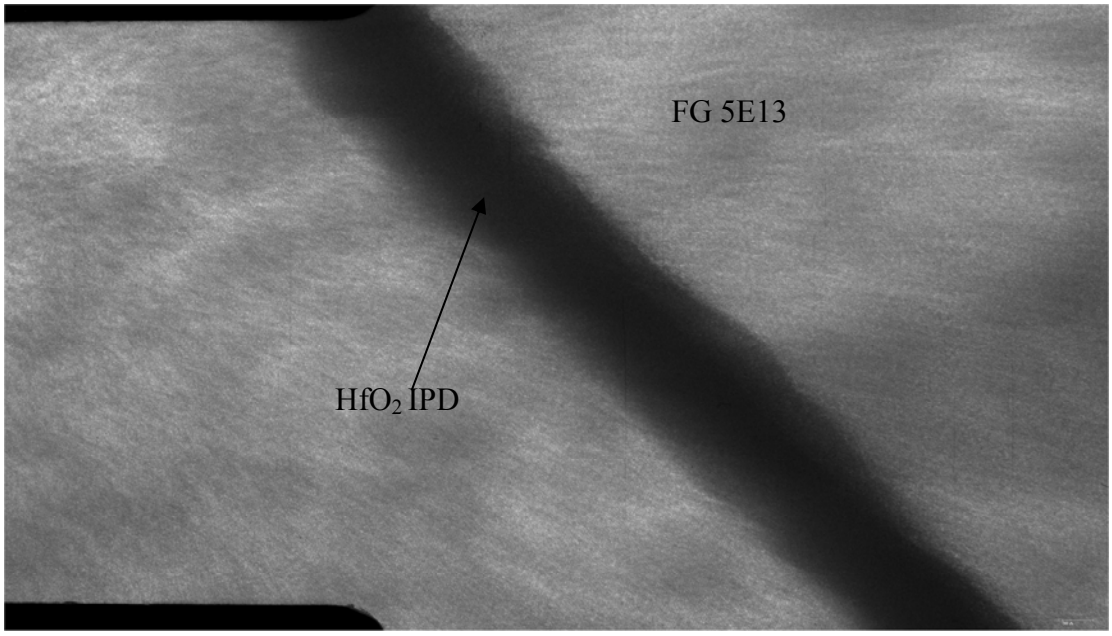


Fig. 3.19 The TEM cross-sectional images of HfO_2 inter-poly capacitors about 150Å with FG 5E13 cm^{-2} sample.

CHAPTER 4

Conclusions and Recommendations for Future Works

4.1 Conclusions

According to ITRS roadmap, the conventional SiO_2 can't meet the requirement due to the large tunneling current for thickness small than 20Å. So, a continuously scaling of the tunnel oxide and IPD thickness for Flash memories is needed to obtain high-k materials. In tradition, high-k materials are imperfect materials. In this thesis, it was found that the electrical properties of Al_2O_3 and HfO_2 IPD strongly depend on the fluorine passivation. Form the experiment results, the fluorine passivation with FG (5E13) and CG (5E15) are the best condition which to make Al_2O_3 and HfO_2 IPD film working moer effectively. As a result, the smoother interface and smaller electron trapping rate contribute to the drastically reduced leakage current, enhanced effective breakdown field, charge to breakdown (Q_{BD}) and significantly reduce the charge loss of leakage current from floating gate at 150℃ by using MOCVD.

Finally, the fluorine passivation effects of Al_2O_3 and HfO_2 IPD were found to significantly suppress the formation of an interlayer (IL) and were beneficial to improve thin film quality because Si-F can combine to reduce the damage generated on the IPD and poly interface. In the future, the fluorine passivation method will be applied widely and enhanced the reliability and the stability of flash memories.

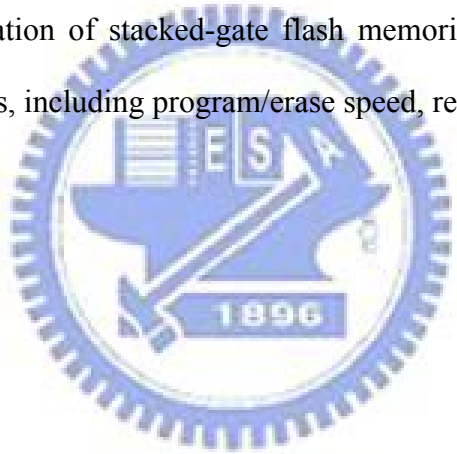
4.2 Recommendations for Future Works

1. More HRTEM images to evidence thickness variation and interfacial layer reaction.

2. More physical analyses are found with the Fluorine passivation effect in other high-K materials in Future.

3. The Fluorine passivation effect Dosage of Al_2O_3 IPD and HFO_2 IPD can use in Flash menories or other devices.

4. The fluorine passivation of stacked-gate flash memories with IPD to study the device characteristics, including program/erase speed, retention time and charge.



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氟鈍化效應在高介電常數複晶矽層間介電層特性及可靠度研究

Characteristics and Reliabilities Research of Fluorine Passivation Effect on Inter-Poly High-k Dielectrics