國立交通大學

電機學院 IC 設計產業研發碩士班

碩　士　論　文

嵌入式晶體振盪器之時脈產生器設計

Design of A Clock Generator Based on Embedded Silicon Oscillator

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摘要

隨著製程技術的提升，電晶體尺寸持續縮小化，電壓、製程和溫度的對電路產生的偏移，以及市場對於低成本、低功率消耗以及高製程整合的大型積體電路需求呈現指數的上升，使得設計日益困難。於現今的電子系統中，石英晶體振盪電路是唯一沒有被整合在積體電路中的元件之一。然而，石英晶體振盪電路不相容於製程的結果，造成額外的製造成本、電路層級的整合體積與高功率消耗。

本論文提出一種基於嵌入式晶體振盪器之全數位時脈產生器。所提出的全數位式鎖相迴路可以使嵌入式晶體振盪器的輸出獲得更準確的頻率，而且可以確定嵌入式晶體振盪器不需要使用任何外在的元件，仍然有能力去對頻率誤差做校正。另外，全數位式鎖相迴路在工作於 5 百萬赫茲時僅消耗 125uW。另外，為了達成某些特殊的脈波寬度以及適用於低功率消耗、低傳輸速率的通訊系統，本論文提出一種全數位式脈波寬度可控制迴路及工作週期調整之電路，可接受輸入時脈的頻率從 5 百萬到 6 億赫茲，而且不需要任何的查表。輸出時脈的工作週期不但可以產生 50%的工作週期，還可以調整從 10%到 90%之間於每隔 10%的工作週期。

Design of A Clock Generator Based on Embedded Silicon Oscillator

Student: Chih-Chao Yang Advisor: Dr. Chen-Yi Lee

Industrial Technology R & D Master Program of Electrical and Computer Engineering College, National Chiao Tung University

ABSTRACT

With the deep sub-micron CMOS technology continues to scale, the presence of the voltage, process and temperature variations make the circuit design more difficult. Furthermore, the market demand for low-cost, lower power consumption and higher integration density VLSI systems have grown exponentially. The quartz crystal (XTAL) oscillator is one of the last components in electronic systems that have yet to be integrated. However, the incompatibility in the process results in extra cost and volume in the board-level integration and, hence, large power is wasted from the external crystal oscillator.

This thesis proposes an all-digital clock generator based on embedded silicon oscillator. The proposed all-digital phase-lock-loop (ADPLL) can achieve more accuracy in output frequency of eCrystal. This ADPLL can ensure the embedded silicon oscillator is able to calibrate the frequency error without any external component. Moreover, it has lower power consumption which consumes 125uW at 5MHz. The all-digital pulse-width-control-loop (ADPWCL) with adjustable duty cycle is adopted to meet the demand for pulse-width-specific, low power consumption and low data rate communication systems. This ADPWCL provide a wide operation range without look-up-table, covering from 5MHz to 60MHz operation range. The output clock is not only achieved 50% duty cycle, but can also be adjusted duty cycle from 10% to 90% in steps of 10%.

誌　　謝

本論文得以順利完成，首先，要感謝我的指導教授李鎮宜老師在我三年的研究生活中，對我的指導與照顧，並且在研究主題上給予我寬廣的發展空間，在我最徬徨無助的時刻給予我指引。而SI2實驗室所提供完善的軟硬體設備與環境，讓我在三年碩士班研究中，學習到如何開始設計積體電路，乃至於量測電路，甚至單獨面對及思考問題。此外要感謝陳紹基教授、許騰尹教授、鍾菁哲教授撥冗擔任我的口試委員並提供寶貴意見，使得本論文更為完整。也感謝國家晶片系統設計中心提供先進的半導體製程，讓我有機會將所設計的電路加以實現並完成驗證。

另一方面，要感謝所有SI2實驗室的成員兩年來的互相照顧與扶持。首先，感謝博士班的學長游瑞元、鍾菁哲、盛鐸、余建螢、陳燦文、許書餘以及已畢業的碩士班學長洪建州、陳俊庭、張琇茹和蕭清峰在研究上或是精神上所給予我的幫助與鼓勵。另外我要感謝學弟妹馬曉涵、和郭時明等諸位同窗，兩年來陪我一塊努力奮鬥，一起渡過同甘苦的日子。此外也感謝我朋友們劉偉正、李清安、廖德文、陳俊瑋、鄭宇、羅肇裕、楊詔詠、劉建文、簡文明、王威傑、林建辰、劉經弘的支持，也因為你們，讓我的碩士班生活更加多采多姿，更有活力與朝氣。

到這邊，特別要致上最深的感謝給我的父母及家人們，謝謝你們從小到大所給予我的栽培、照顧與鼓勵，讓我得以無後顧之憂地完成學業，朝自己的理想邁進，衷心感謝你們對我的付出以及支持我的任何決定，並給我無限的信任。

最後，對於所有關心我、愛護我和曾經幫助過我的人，願我在未來的人生能有一絲的榮耀歸予你們，謝謝你們。

楊智超 于 電資大樓SI2實驗室

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Chapter 1
Introduction

1.1 Motivation

As the technology continuously scales down, more and more nonlinear effects make the circuit design more difficult. The short channel effects and the presence of the voltage, process and temperature variations make the engineers much intractable to handle. As a result, a common challenge to process engineers and circuit designers who tried to meet the demand for low-cost, lower power consumption and higher integration density VLSI systems from market has grown exponentially.

In the synchronous clock system, the quartz crystal oscillator is widely used for computers, consumers and communication products. The quartz crystal (XTAL) oscillator is one of the last components in electronic systems that have yet to be integrated [1]. A major reason for using of quartz crystal oscillators is their high Q factor. A typical Q value for a quartz crystal oscillator ranges from 10^4 to 10^6, compared with perhaps 10^2 for an LC oscillator. However, the disintegrable quartz crystal oscillator occupies large size and more power consuming, also hardly to be integrated in a SoC. The incompatibility in the process results in extra cost and volume in the

board-level integration, hence, large power consumption is wasted from the external oscillator. As a result, the patent for the crystal-less oscillator generator has been applied in many countries [31-34]. The eCrystal [35] oscillator has a tunable clock generator which is capable of compensating process, voltage, and temperature (PVT) variation without using the external crystal or any RC components. More important is that fully compatible with standard CMOS process, providing a stable frequency generation under the variations of PVT conditions. To acquire the accurate clock and to ensure the embedded silicon oscillator of the clock result in the growth of the phase locked loops (PLLs) to calibrate. In order to generate a free run clock source within small frequency error, the proposed embedded silicon oscillator namely eCrystal oscillator needs one shot calibration to record the process dependent parameters (PDPs) into the chip before sale to market. Therefore, an all-digital phase locked loop (ADPLL) design for the eCrystal process calibration is demanded.

Furthermore, the clock signal is used to synchronize different parts of digital system. The quality of the clock signal which is based on frequency, phase, and duty cycle, undoubtedly influences the system performance. With the advanced technology, many digital clocks not only have low jitter, but also need 50% duty cycle to double the data rate, such as DDR SDRAM. Some special analog-to-digital (ADC) or digital-to analog (DAC) systems [2] need the clock generators with programmable duty cycles. Moreover, in the low power and low data rate communication systems such as Wireless Body Area Network (WBAN) application, the duty cycle control (DCC) [3-4] reduces the energy requirements for a specified network latency and can provide significantly improved node availability with reduced communications latency for a specified energy budget. In order to achieve the adjustable duty cycle, several phase-width control loops (PWCLs) have been presented. However, as analog approach, PWCLs require accurate matched analog devices [31-32] and the capacitors that may occupy a large active area. Owing to the PVT variations, the analog PWCLs may become unstable if the loop gain is not properly controlled. In addition, for analog PWCLs, the locked time will be too long [32] to have the desired duty cycle. Therefore, the

adjustable duty cycle circuit is proposed in all-digital scheme for more reliability and performance improvement.

1.2 Thesis Organization

The rest of this thesis is organized as follows. At first, the basic knowledge of the embedded silicon (eCrystal) [35] oscillator will be described in Chapter 2. Then, we propose an all digital phase locked loop for eCrystal calibration designed in Chapter 3. In Chapter 4, we present an all digital pulse-width control loop with adjustable duty cycle. Finally, Chapter 5 summarizes our work and discusses some design topics in the future.

Chapter 2
THE BASICS OF THE EMBEDDED SILICON OSCILLATOR

Quartz crystal frequency references have long been recognized as the most cost effective method of maintaining frequency accuracy in signals for wireless communications. In consumer communications products, such as cellular telephones and televisions, the cost of the crystal routinely accounts for no more than of 1% of the total material cost of the unit [5].

To meet high integration, low power consumption and low cost for computers of consumers and communication products, an embedded silicon oscillator (eCrystal) [35] is desired to replace existing crystal and external components. In this chapter, the basic knowledge of the embedded silicon oscillator is briefly described.

2.1 Introduction to Embedded Silicon Oscillator

FIG. 1 shows the concept of eCrystal oscillator to replace the external components. By the use of eCrystal oscillator, the external and existing crystal can be eliminated and integrated into a single

function chip. A remote reference tone is used to calibrate the initial frequency offset of clock generator which illustrates in section 3.2. FIG. 2 shows the accuracy of eCrystal system for possible different applications after calibrated.

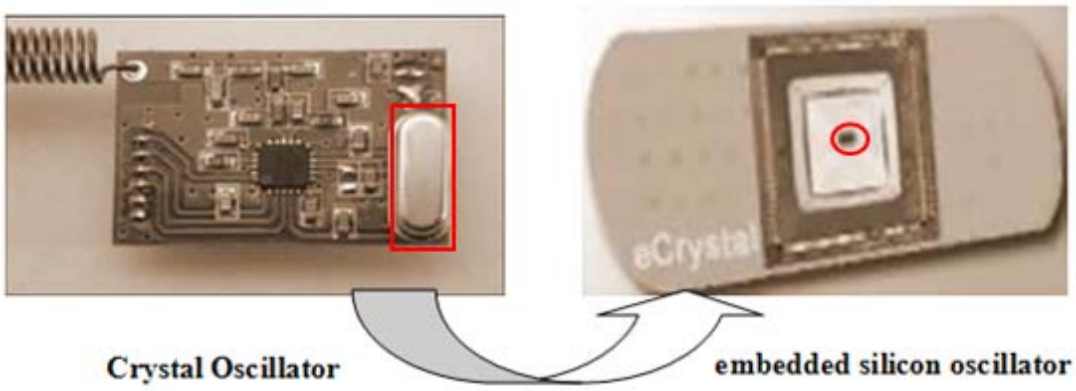


FIG. 1. The concept of eCrystal oscillator to replace the external components

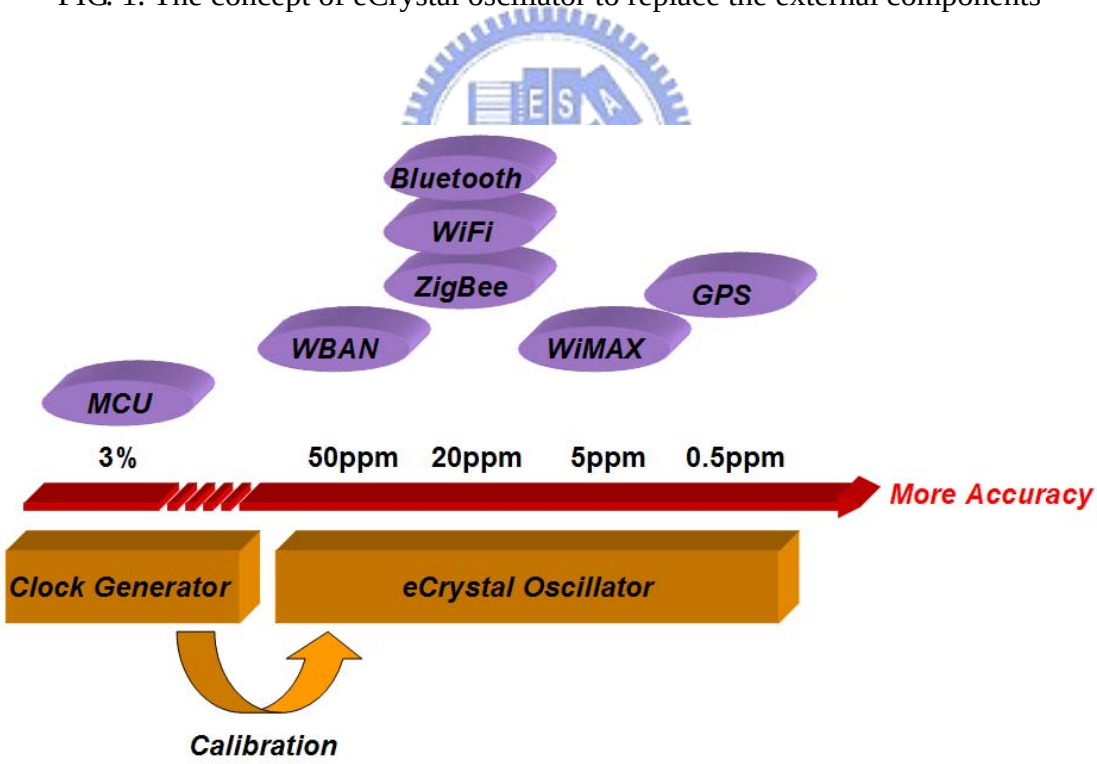


FIG. 2. The accuracy of eCrystal system for possible different applications

Several approaches have been proposed to replace the quartz crystal, including Micro Electro Mechanical Systems (MEMS) oscillator, LC tank oscillator and Ring oscillator. Unfortunately,

there are many disadvantages in each approach. MEMS [6-7] oscillators have certain disadvantages which include limited power-handling capability, and special process and package. LC tank oscillator [8] is suitable for low-noise radio frequency synthesis, but the drawback is high power consumption, large area on the top layer metal of a die, and poor portability. Ring oscillator [9] seems to a better solution to chip integration power budget and area, but the disadvantage is the operational amplifiers in voltage regulator and comparator consume large power. Moreover, when the CMOS technology scaling to the next advanced generation, the violent frequency variation rate of ring oscillator is about 60 ~ 70% under the worst case PVT corners in 90nm process. TABLE 1 shows the comparison of state of the arts.

	Proposed eCrystal oscillator	Quartz crystal	JSSC'06 [9]	SBCCI'03 [10]	ICECS'07 [11]
Process	CMOS 90nm	with 90nm oscillator pad	CMOS 0.25um	CMOS 0.5um	CMOS 0.13um
Approch	Ring OSC	with 90nm oscillator pad	Ring OSC	RC	TDC-based
Frequency	40MHz	40MHz	7MHz	12.8MHz	10MHz
Area	0.4mm^2	1cm^2	1.6mm^2	0.185mm^2	160um^2
Power	237uW*	14mW	1.5mW	400uW	30uW
PVT Range	P SS ~ FF V 0.9 ~ 1.1 T 0 ~125	Very wide	P SS~ FF V2.4~2.7 5 T - 40~125	P SS ~ FF V 3 ~ 5 T -40~ 125	P SS ~FF V 1.2 T 0 ~ 70
Frequency Accuracy	3.5%	50ppm	2.6%	5%	6%

TABLE 1: The Comparison of each Proposed.

2.2 Design Challenge

The key challenge of an on-chip oscillator design is to maintain the stability of frequency due to process, voltage, and temperature (PVT) variations. The bandgap regulator techniques [9-10] are applied for suppressing the supply voltage variation. The process and temperature variations are sensed or compensated by carefully refining the transistor configurations. The current limiting technique [11] is proposed to compensate temperature variation. Nevertheless, these methods are not easily portable when fabrication process migrates toward deep sub-micron (DSM) scale. Moreover, there is a design barrier when the conventional bandgap regulator operates under 1.2-V supply voltage [12], whereas the all-digital design approach is power efficient, portable with process migrations, and easily to be adopted in low supply voltage.

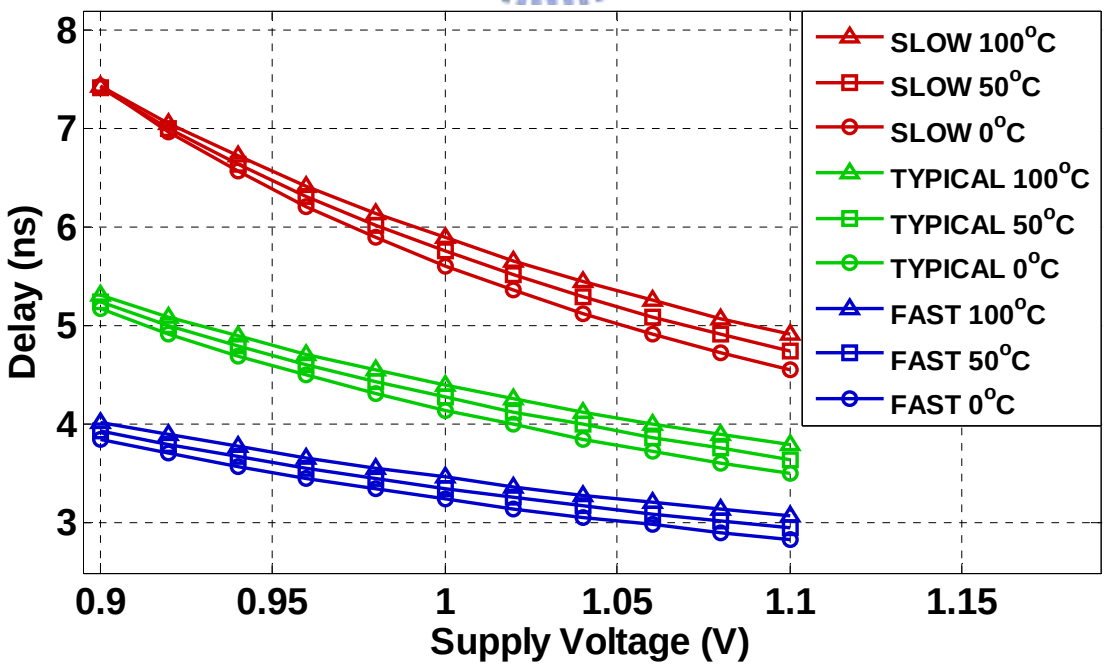


FIG. 3. Delay spread of a delay line composed of 100 buffers connected in a series under PVT variations.

In CMOS process, gate delay is strongly affected by PVT variations and it can be modeled as a function of PVT described as *D(P,V,T)*. FIG. 3 shows the delay spread of a delay line composed of 100 buffers connected in a series of a 90-nm CMOS process. The delay varies widely from 2.8ns to 7.5ns with different supply voltage and temperature across process corners of SLOW, TYPICAL, and FAST which are provided by foundry. If the delay line is applied in a free running ring oscillator, PVT variations make the oscillation frequency unstable. Even if the process variation is calibrated in a post process testing, the frequency variation is still high and unpredictable due to the unknown supply voltage and operation temperature.

2.3 Architecture

A simple architecture is shown in FIG. 4. It is composed of three blocks, including delay ration estimator, mapper and digitally controlled oscillator. The delay ratio estimator calculates the delay ratio of two different delay cells (DVAR (P.V.T)/ DREF (P.V.T)). The delay ratio of these two delay cells is aimed to estimate the delay of the reference delay cell. To strengthen the difference of the delay behavior to PVT conditions in these two delay cells, we adopt NAND gate as the compared delay cell and BUFFER gate as the reference delay cell. Sweeping the PVT conditions of three process corners with voltage range from 0.9V to 1.1V and temperature range from 0℃ to 75℃, the delay of the reference delay cell to the delay ratio is plotted in FIG. 6. The curve of the reference delay can be approximated by $\tilde{D}_{ref}(P,V,T)$, which is a second order function of the delay ratio R(P,V,T), that is $\tilde{D}_{ref}(P,V,T) = aR^2(P,V,T) + bR(P,V,T) + c$,where a, b, and c are process dependent parameters (PDPs). Three process corners are fitted by three sets of PDPs. The PDPs can be obtained by a post-process testing with at least three voltage and temperature conditions in the curve. The delay of the reference delay cell is estimated. The DCO is based on a ring oscillator with

adjustable hysteresis delay cell (HDC) length in the delay line. The desired frequency, f_{des}, as shown in Equation. 1.

$$f_{des} \cong \frac{1}{2 \cdot [CD_{ref}(P,V,T) + D_{extra}]} \quad \text{.....} \quad \text{Equation.1.}$$

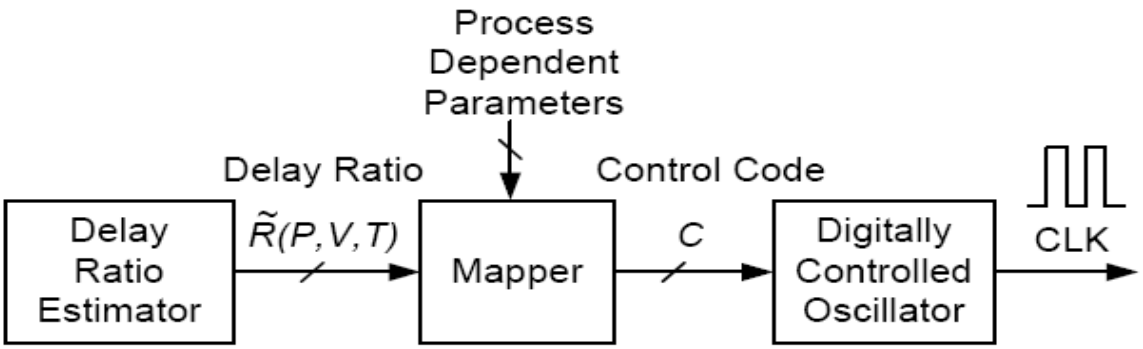


FIG. 4. System Architecture of the eCrystal oscillator.

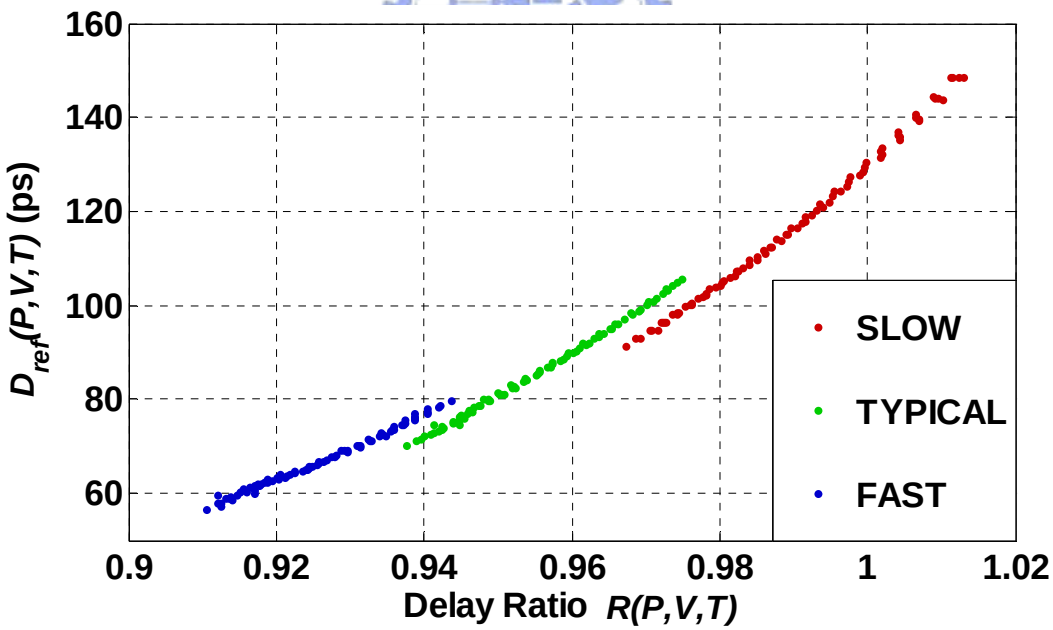


FIG. 5. Relation between the delay of the reference delay cell and the delay ratio.

From Equation. 1, the extra combinational delay can be neglected, because the variation is far less than the main delay line in the delay path. We can fix the target frequency, f_{des}, and

according to the locked codeword representing the target frequency, to solve a, b, and c parameters. These behave like a phase lock loop (PLL) which controls the DCO and compare the CLK frequency to the external reference frequency. So, we propose an all digital phase lock loop (ADPLL) to provide an accurate lock code. The details will be illustrated in chapter 3. According to the delay ratio and process dependent parameters, mapper is able to transfer the control code for calibrating the PVT variations. The DCO receives the digital control code from the mapper and generates the target frequency clock without any external components

The quality of the clock signal which is based on frequency, phase, and duty cycle, undoubtedly influences the system performance. With the advanced technology, many digital clocks not only have low jitter, but also need 50% duty cycle to double the data rate, such as DDR SDRAM. Some special analog-to-digital (ADC) or digital-to analog (DAC) systems [2] need the clock generators with programmable duty cycles. In order to achieve a better performance in the clock system, an all digital pulse width control loop (ADPWCL) design will be further discussed in Chapter 4.

Chapter 3
ALL DIGITAL PLL FOR ECRYSTAL PROCESS CALIBRATION

Phase locked loops (PLLs) are widely used in modern communication systems and high performance microprocessors because of their remarkable versatility. PLLs are used to lock or track input signals in phase and frequency. The digital approach has low design complexity for power minimization, and easy integration in SoC applications. Also, it achieves fast lock times by using all-digital PLLs (ADPLLs). The ADPLLs have better testability, programmability, stability, and portability. Therefore it is suitable to acquire the accurate process dependent parameters (PDPs) for eCrystal calibration.

In this chapter, a process calibration circuit using an all-digital phase locked loop (ADPLL) technique is realized in UMC 1P9M 90nm CMOS process. The proposed ADPLL for eCrystal calibration achieves a capable of calibrating PVT variations. According to the lock code from the proposed ADPLL, the testing machine will calculate the a, b, c parameters and will be recorded into a one-time programming (OTP) or register files. The mapper will combine the delay ratio and pick up PDPs from OTP or register files to calibrate the frequency error without any external components. In section 3.1, we will simply introduce four kinds of PLL applications, and pick item

three (clock generator) which is similar with our system requirement. In section 3.2, we will give an overall system overview and design specification. The details in ADPLL for eCrystal process calibration are illustrated in the following sections.

3.1 Introduction to Phase Locked Loop

The APLL (also know as Linear Phase-Lock Loop (LPLL) is a traditional PLL, which was proposed back in 1930s by French Engineer, H. de Bellescize. The initial ideas started as early as 1919 in the context of synchronization of oscillators. The theory of phase-locked loop was based on the theory of feedback amplifiers.

A PLL is a circuit which causes a particular system to track with another one. More precisely, it is a feedback loop which synchronizes an output signal with a reference or input clock in frequency as well as in phase. In the locked stated, the phase error between the oscillator's output and the reference clock is either zero or an arbitrary constant.

Due to the rapid development of integrated circuit (IC's) since 1970's, PLLs are widely used in modern signal processing and communication systems, and it is expected that PLL will contribute to improvement in performance and reliability of future communication systems. The main applications of PLL are as follows:

1. Clock recovery: Some data streams, especially high-speed serial data streams, (such as the raw stream of data from the magnetic head of a disk drive) are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase-aligns to

the transitions in the data stream with a PLL. In order for this scheme to work, the data stream must have a transition frequently enough to correct any drift in the PLL's oscillator.

2. Deskewing: If a clock is sent in parallel with data, that clock can be used to sample the data. Because the clock must be received and amplified before it can drive the flip-flops which sample the data, there will be a finite, and process-, temperature-, and voltage-dependent delay between the detected clock edge and the received data window. This delay limits the frequency at which data can be sent. One way of eliminating this delay is to include a de-skew PLL on the receive side, so that the clock at each data flip-flop is phase-matched to the received clock.

3. Clock generation: Most electronic systems include processors of various sorts that operate at hundreds of megahertz. Typically, the clocks supplied to these processors come from clock generator PLLs, which multiply a lower-frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of the processor. The multiplication factor can be quite large in cases where the operating frequency is multiple gigahertzes and the reference crystal is just tens or hundreds of megahertz.

4. Spread spectrum: All electronic systems emit some unwanted radio frequency energy. Various regulatory agencies (such as the FCC in the United States) put limits on this emitted energy and any interference caused by it. The emitted noise generally appears at sharp spectral peaks (usually at the operating frequency of the device, and a few harmonics). A system designer can use a spread-spectrum PLL to reduce interference with high-Q receivers by spreading the energy over a larger portion of the spectrum. For example, by changing the operating frequency up and down by a small amount (about 1%), a device running at hundreds of megahertz can spread its interference evenly over a few megahertz of spectrum, which drastically reduces the amount of noise seen by FM receivers which have a bandwidth of tens of kilohertz.

3.2 System Overview

The embedded silicon (eCrystal) communication system is composed of a master node and a slave node, which is compatible in most of the current communication systems. The slave node in the eCrystal communication system can eliminate the use of an external quartz crystal oscillator and replace by an eCrystal oscillator. The eCrystal oscillator applies a standard CMOS process and can be directly integrated into a single chip. A remote reference tone is used to calibrate the initial frequency offset of clock generator As a result, the cost of board level integration and external power consumption are reduced. FIG. 7 shows a simple eCrystal communication system.

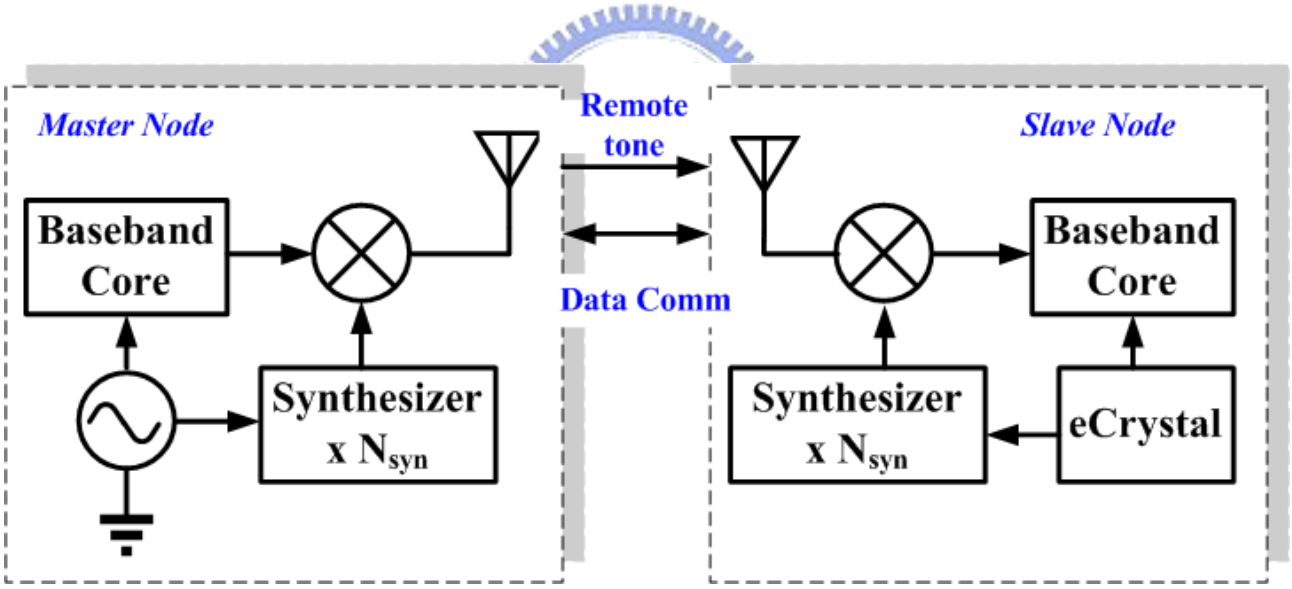


FIG. 6. A simple eCrystal communication system

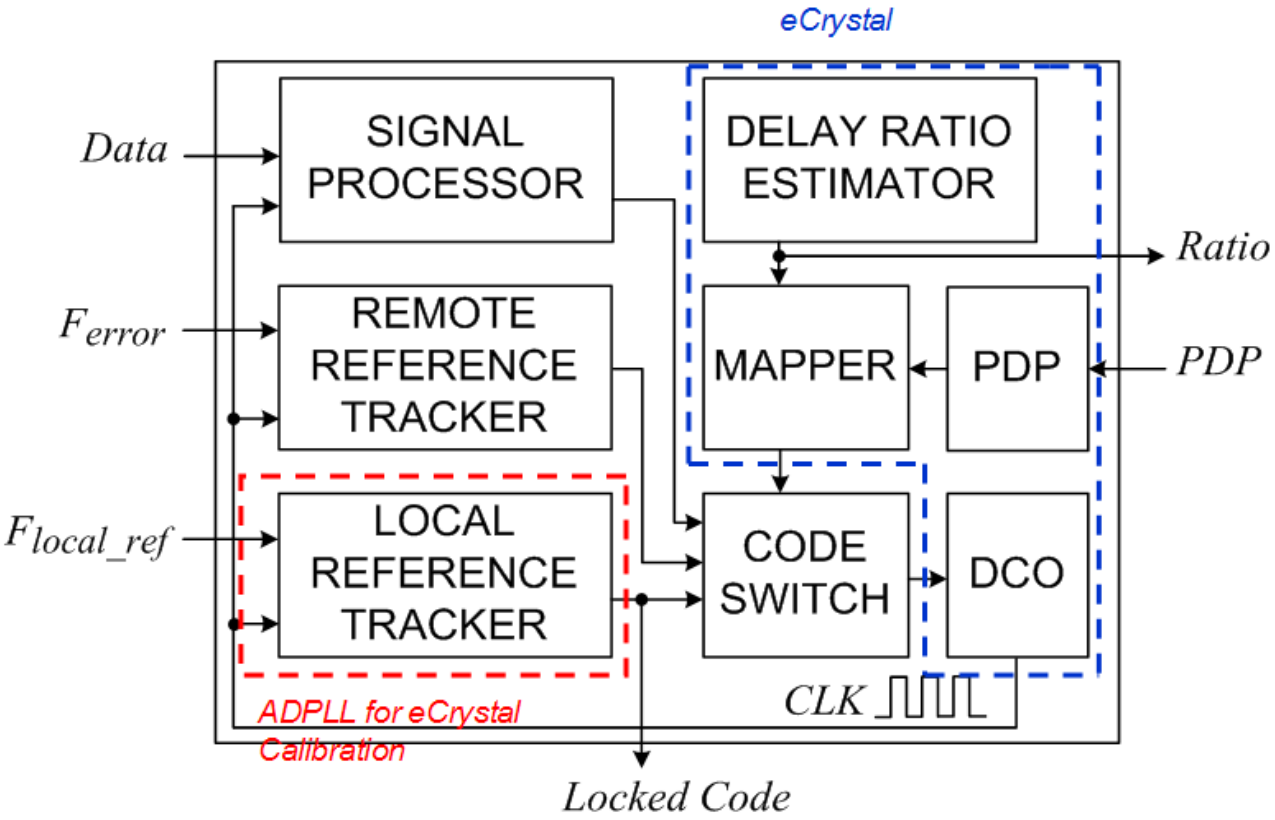


FIG. 7. The proposed all-digital phase locked loop for process calibration

The slave node baseband of the embedded silicon (eCrystal) oscillator communication system with proposed all-digital phase locked loop for eCrystal process calibration is depicted at red sub-area in FIG. 8. The slave node baseband contains an eCrystal including delay ratio estimator, mapper, and digitally control oscillator (DCO) and PDP. The eCrystal is designed to provide 5MHz frequency for the baseband clock and radio frequency carrier synthesis.

After a chip is fabricated, the standard logical or functional test will be executed on a testing machine. Meanwhile, the accurate reference frequency (F_{local_ref}) is available, and the testing cycle is adequate for the local reference tracking. The local reference tracker behaves like a phase lock loop (PLL) which controls the DCO and compare the CLK frequency to the external reference frequency. After the frequency is locked, the Locked Code is provided along with the Ratio from delay ratio estimator. Besides, the chip will be tested under different operation corners. Collecting

the different corner Locked Code and Ratio data, we are able to calculate the process dependent parameters (PDPs) which will be recorded into a one-time programming (OTP) device or register files.

The master node of a communication system provides a reference carrier frequency in the down-link communication for calibration. The received remote reference frequency is then down-mixed with the local oscillation signal which is synthesized from the eCrystal oscillator clock. If the local frequency is exact the same as the remote reference frequency, the residual frequency error (F_{error}) will be zero. The remote reference tracker needs 2ps resolution of DCO. Otherwise, the residual frequency error fed to the slave node baseband is tracked by the remote reference tracker, and it will adjust the DCO until the frequency error shrinks to a tolerable value which baseband signal processor can handle.

The remote reference tracker is on the frequency calibration behavior combined with a 420-430MHz band FSK module. The remote frequency tracker is a common system block in both eCrystal FSK solution and eCrystal OFDM-based WiBoC (Wireless & Imaging Business Owners Consortium) solution and can be applied to both designs. The design challenge is to track and calibrate the frequency error within 5% which is quite high in a communication system. By adjusting the DCO, the final calibrated frequency error will be within 0.3%. The calibration time should be small than 10ms to reduce the communication traffic overhead. The baseband signal processor including a synchronizer, channel equalizer, and an Orthogonal Frequency Division Multiplexing (OFDM) modulator and demodulator is developing a synchronizer which can detect the down-link signal and to synchronize through adjusting the DCO. The signal processor can tolerate frequency error up to 0.3% and adjust the DCO frequency to below 20ppm. After synchronization, the up-link communication can transmit data. This block and the remote reference tracker block target on reducing frequency error between a master node and a slave node.

The local reference tracker is to track the reference frequency and provide the locked code under testing procedure. The power and locked time is less critical due to its operating occasion is only once. The proposed design will be illustrated in next section. The design specification of local reference tracker is listed in TABLE 2, including 5MHz reference clock source and 5MHz target output Locked Code with 20ppm frequency error.

Reference Clock Source	5MHz
Output 19 bits Locked Code@5MHz	V
Locking Time	< 100us
Frequency Error	=< 20 ppm

TABLE 2: Specification of ADPLL for the eCrystal process calibration.

The DCO adopts the HDC (Hysteresis Delay Cell)-based [16-17][36] delay cell which can achieve an excellent performance on power consumption. However, the most concerned issue on the HDC-based DCO is the linearity under PVT variations. The hysteresis delay cell has a worse PVT variation than a typical delay cell, also it has a non-monotonic phenomenon.

The delay ratio estimator along with a mapper will provide an initial control code for DCO under PVT variations. The design challenge is to estimate the delay ratio within 0.1% and to map the DCO frequency with as little error as possible. If the error is reduced, the calibration effort will be relaxed and the overhead in communication is reduced.

3.3 Architecture

This proposed all-digital phase locked loop for process calibration architecture is shown in FIG. 9. This all-digital phase locked loop (ADPLL) consists of phase frequency detector (PFD), hysteresis delay cell based-digitally controlled oscillator (HDC-DCO), control unit (CU) and digital loop filter (DLF).

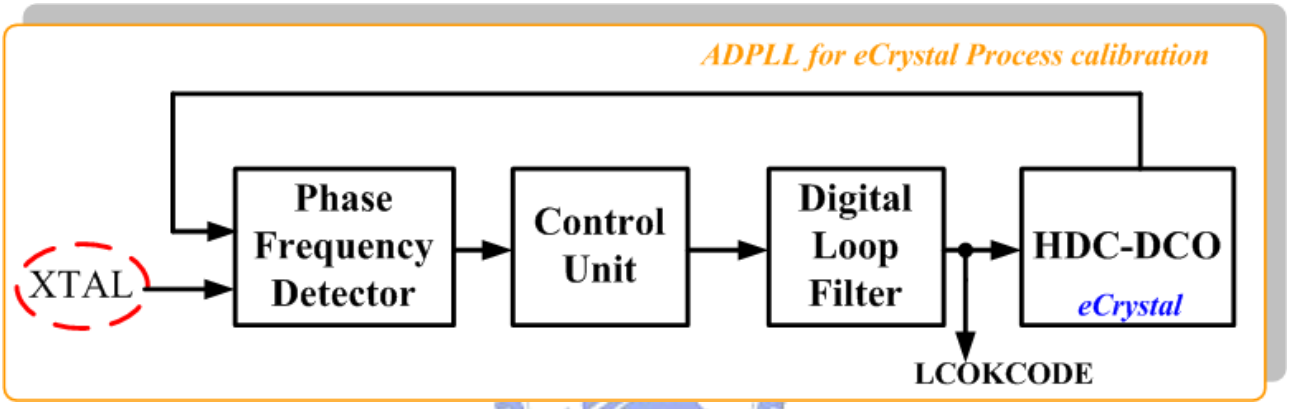


FIG. 8. The proposed all-digital phase locked loop for process calibration architecture.

There are two operations in the system; one is used for the embedded silicon oscillator calibration named calibration mode and the other is used for generating the output clock without the reference clock source named operation mode. The difference between the operation mode and the calibration mode is reference clock source. One is for quartz crystal oscillator and the other is for eCrystal without any reference source.

In the operation mode, by using the power gating cell which can be gated the power consumption from PFD, CU and DLF, the output clock is generated at 5MHz by the embedded silicon oscillator which is a small and a highly integrated circuit. In the calibration mode, the output clock is directly connected to the PFD which detects the difference of frequency and phase between

the clock of external quartz crystal and HDC-DCO output. Then, it generates an up (UP) and down (DOWN) signal to indicate CU that adjusts HDC-DCO control codeword to speed up or slow down the output frequency of HDC-DCO, respectively. According to the developed search algorithm [14-15], the whole all-digital PLL operation mechanism is illustrated in FIG. 10.

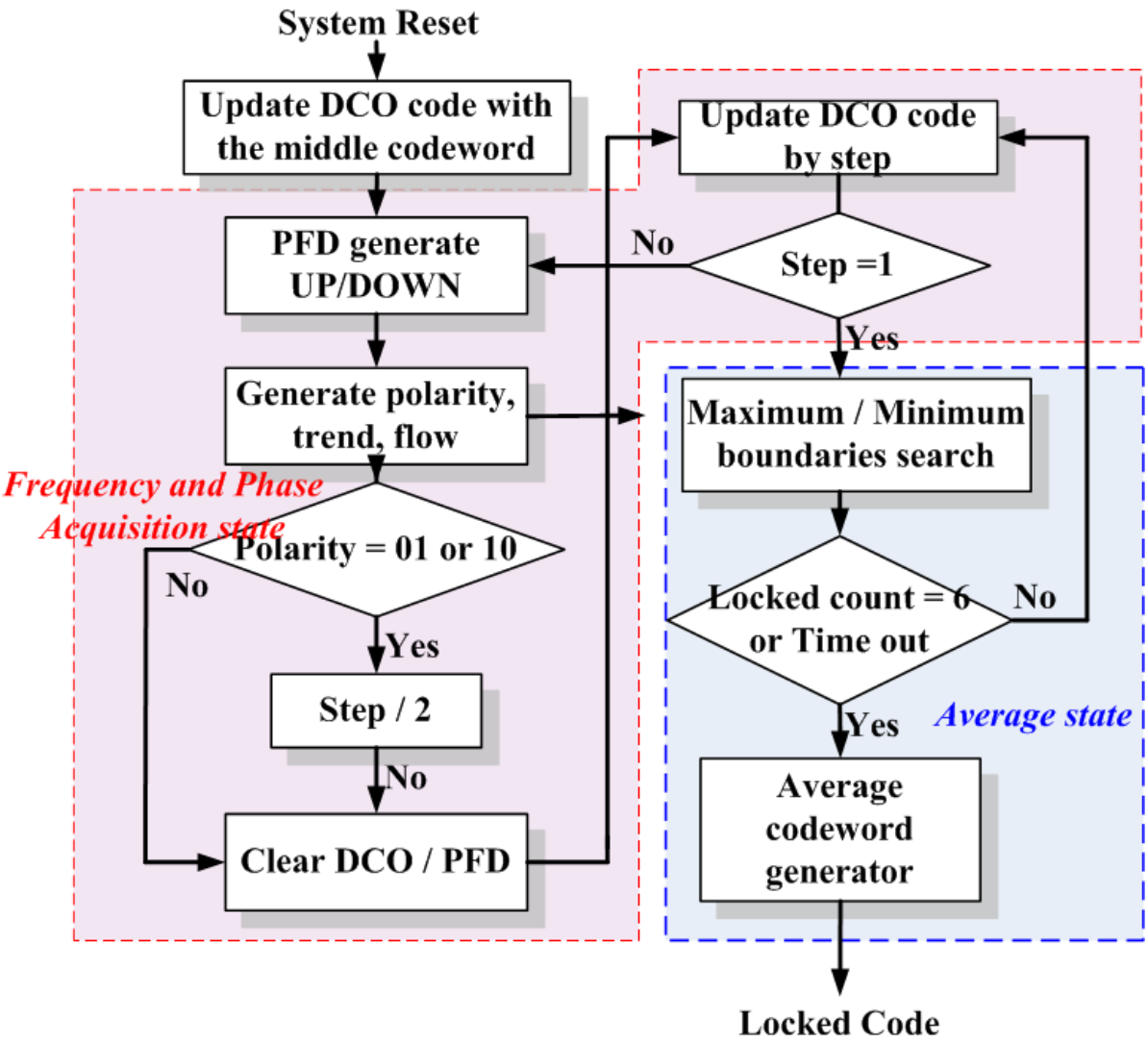


FIG. 9. All-digital PLL operation mechanism

After the system reset, the CU sets the DCO at the middle of delay path. The initial search step of DCO is n/4, where n is the number of frequencies provided by the DCO. The binary search will pass through the three states to converge the output frequency as close as possible to reference

clock. Each state employs different tuning range and resolution as shown in FIG. 11.

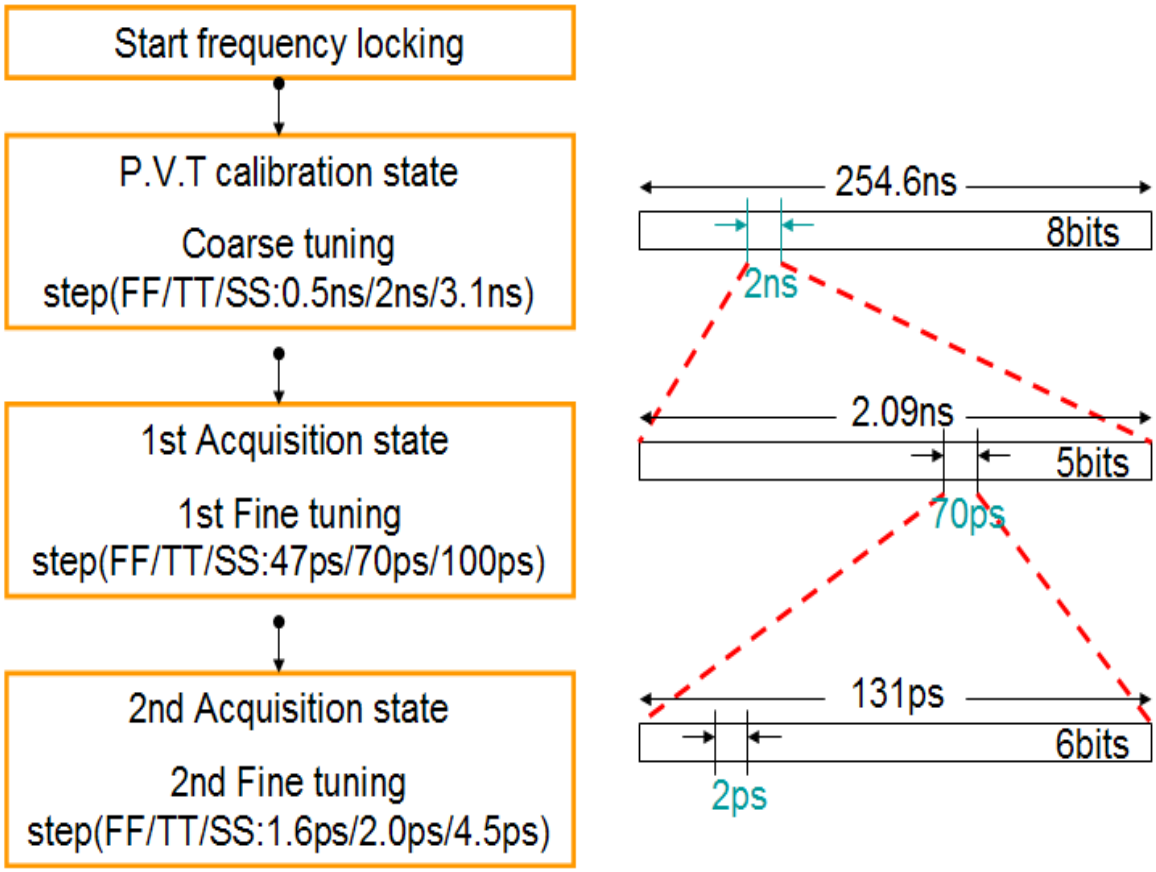


FIG. 10. The tuning range and resolution of each three state

While the PFD detects from lead to lag, the search step is divided by two, and vice versa [14]. Each time when a new DCO code is calculated, the current DCO and PFD control signals will be cleared before the DCO is updated. Clearing DCO signal avoids glitches which result from directly updating DCO codeword. At the same time, clearing PFD signal keeps the coarse-tuning loop from frequency and phase divergence [16].

When the search step becomes to one, ADPLL finishes frequency and phase acquisition. Then ADPLL will become the average state which will search the maximum and minimum DCO code to generate more accuracy average Locked Code. According to polarity, trend and flow signals, the

digital loop filter (DLF) will detect the maximum and minimum DCO codeword with 2nd fine tuning range during the multi-reference clock cycles, which the output (DCO codeword (max + min) /2) is the average DCO Locked Code. If the lock-counting signal of the controller is inversed by six times cumulatively, or time out signal occurs, the clock-in maintenance will be completed. In the meantime, the lock signal will enable the eCrystal. According to collecting the different corner Locked Code and Ratio data, mapper will provide an initial control code for DCO under PVT variations. After the process calibration maintenance is completed, we can remove the reference clock source to generate the frequency error within 3% accuracy by eCrystal.

3.4 Circuit Design

3.4.1 Digitally Controller Oscillator

The DCO design follows the circuit topology proposed in [17] with power of two-hysteresis delay cell (P2-HDC) as the block diagram is shown in FIG. 11. The property of HDC can provide a large delay with a small amount of gates and in a simple topology compared to conventional cascaded inverters. In order to preserve the DCO control code resolution and wide operation range under PVT variations from several tens of nanoseconds to the ten picoseconds scale, the HDC-based DCO is separated into three tuning stages.

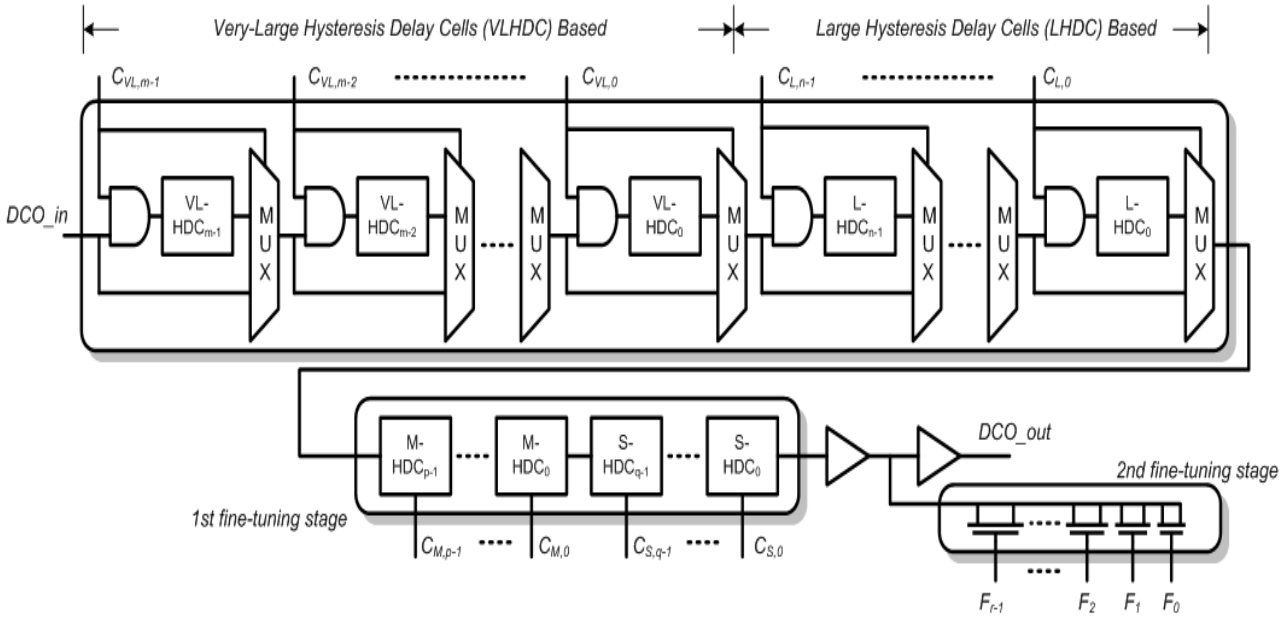


FIG. 11. Architecture of HDC-based DCO

The power-of-two delay is designed that every segment in the delay line has a delay in the power-of-two descending order. Thus each segment performs a propagation delay either half of previous segment or twice of the next one. The P2-Delay is partitioned in a coarse-tuning stage and first fine-tuning stages. The coarse-tuning stage contains two circuit forms, LHDC and VLHDC. The LHDC (or VLHDC) is designed to generate a delay which is several tens (or hundreds) times larger than a minimum-sized inverter in the same manufacturing process. The fine delay tuning is achieved by two stages. The first stage is composed of MHDC and SHDC that generate delays about 0.01~10 times of a minimum sized inverter. The second fine-tuning stage is designed by the MOS gate capacitance (MGC) for sub-pico-scale delay tuning. Each HDC-based circuit details are illustrated in section 4.3.1.1.

Coarse Tune(8 bit)	TT/1.0V/25	FF/1.1V/-25	SS/0.9V/125
range	2.53E-07	6.97E-08	6.34E-07
resolution	9.87E-10	2.72E-10	2.48E-09
max gap	3.5E-09	7.67E-10	6.81E-09
1st Fine Tune(5 bit)			
range	2.01E-09	1.58E-09	2.96E-09
resolution	6.29E-11	4.93E-11	9.24E-11
2nd Fine Tune(6 bit)			
range	1.3E-10	9.47E-11	2.26E-10
resolution	2.04E-12	1.48E-12	3.54E-12

TABLE 3: Controllable range and delay resolution of DCO

Max Freq	239.2MHz	340.13MHz	150.6MHz
Min Freq	3.89MHz	13.9MHz	1.56MHz

	TT/1.0V/25	FF/1.1V/-25	SS/0.9V/125
Min Freq	3.89MHz	13.9MHz	1.56MHz
Power	5.21uW	17.1uW	2.3uW
Max Freq	239.2MHz	340.13MHz	150.6MHz
Power	75.9uW	119uW	32.1uW

TABLE 4: The power consumption in minimum and maximum output frequency

By post-simulation, the tolerance maximum output frequency of the proposed DCO is 3.89MHz (71.6 ns) and the minimum output frequency of the DCO is 239.2MHz (4.18 ns) under PVT corners (TT, 1V, 25℃). As a result, total power consumption of the P2-HDC based DCO is 5.21uW and 75.9uW under 1.0V in UMC 90nm CMOS process. TABLE 3 shows that the

controllable range of each stage is larger than the step of the previous stage, and the DCO power consumption in minimum and maximum output frequency is shown in TABLE 4.

3.4.2 Phase Frequency Detector

The PFD design follows the circuit topology proposed in [14] and [18] with standard cell library as the block diagram is shown in FIG. 13. While the feedback clock (FB) which is generated from DCO leads the input reference clock source (IN), the signal “qd” generates a high pulse until IN arrives the D filp-flops (DFFs) and triggers for “qu”. The generated signal “qu” first goes back to the reset branch on DFF and then clears the “qu” and “qd”. At the same time, “outu” brings about a low pulse and “outd” remains high. Finally, the flags UP and DOWN will be triggered by these signals and be sent to the control unit (CU) for slowing down the DCO. On the other hand, if FB lags IN, DOWN becomes high and UP remains low.

The dead zone phenomenon is generally known in PFD, which is caused by the limited response time of transistors. When the pulse width of “qu” or “qd” is not long enough to turn on the following circuits, the characteristic of PFD becomes discontinuous. To minimize the dead zone, a digital pulse amplifier [14] is proposed in FIG. 14. It uses the cascaded two-input AND gates architecture to enlarge the pulse width of “outu” and “outd”. There is another method to eliminate the dead zone with an inserted delay buffer in the feedback path of the reset branch. The increasing response time for DFF would effectively generate a wide enough pulse width to minimize the dead zone of the PFD, and then the following DFFs can detect it. When the phase error between IN and FB is less than 8ps in typical case, both UP and DOWN will remain in high, and no trigger signal

will be sent to the CU.

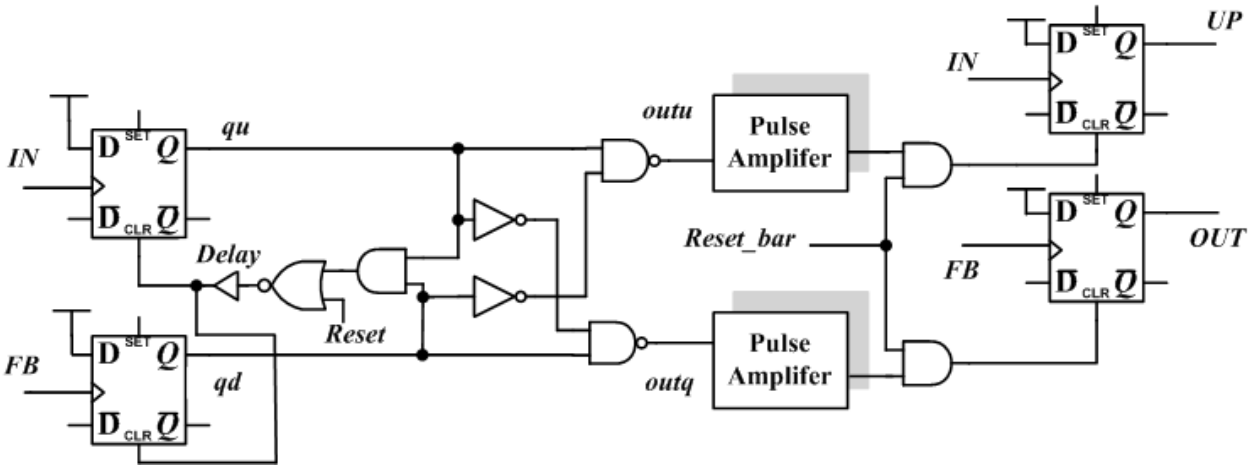


FIG. 12. Schematic of PFD

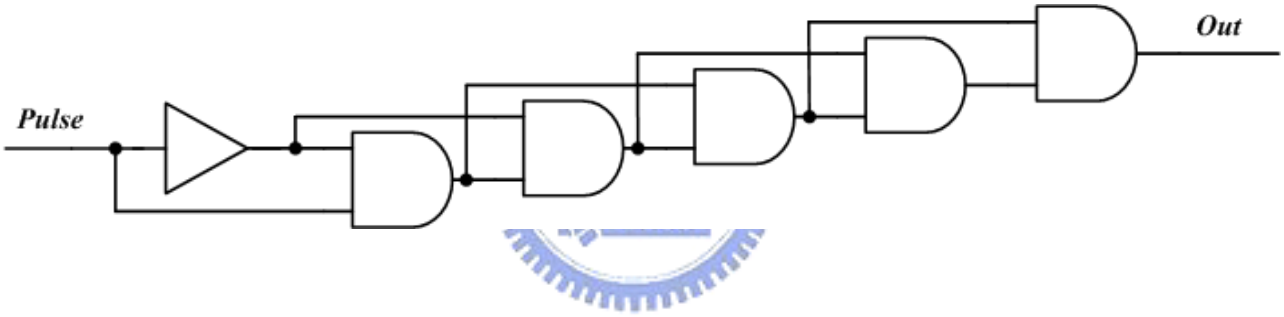


FIG. 13. Schematic of Pulse Amplifier

3.4.3 Controller and Loop Filter

After post simulation of the P2-HDC-DCO, we can create the look-up table for mapping the DCO control code and frequency. Hardware Description Language (HDL) is used to describe the ADPLL control unit (CU) and digital loop filter (DLP). We use a logic synthesizer to synthesize those modules to gate-level circuits with UMC 90nm 1P9M CMOS cell library.

	State	Description
Trend (2bits)	00	Slow
	01	Fast
	10	*
	11	Initial
Polarity (2bits)	00	Same trend
	01	Slow than fast
	10	Fast than slow
	11	Initial
Flow signal (2bits)	00	Underflow
	01	Initial
	10	Normal
	11	overflow

TABLE 5: The truth table of polarity, trend and flow check signals.

The PFD will compare the phase and frequency between IN and FB, which generate UP and DOWN signals to the CU. According to UP and DOWN signals, the CU will generate polarity, trend and flow check. The truth table is shown in TABLE 5. Each state which compares previous and present UP and DOWN signals will generate trend and polarity signals. According to trend, polarity and flow signals indicate whether DCO should be increased or decreased in speed respectively.

The ADPLL's close-loop response time is determined by response time of DCO, delay time of the CU and some wire delay. After n (response time / small tuning step) cycles, the PFD will detect right angle for CU, and the control code can only update at every n reference cycles. The n is equal to 16 in our proposed design, because the HDC-DCO have worse jitter performance about 1% of total period which dominants the ADPLL's close-loop response time. In search algorithm, we use

the binary search method proposed in [14]. Every time when polarity signal is inversed, the search step reduces to ¼ of the previous search step. When polarity transition happens twice, the upper bound and lower bound for target frequency has been determined. After frequency and phase acquisition state are finished, only DCO fine-tuning codeword will be changed. DLF will detect the maximum and minimum DCO codeword into the registers. The average DCO code ($CODE_{MAX}$ + $CODE_{MIN}$) /2) will enhance the accuracy in the eCrystal.

3.5 Simulation

FIG. 15 shows the transient response of the proposed ADPLL operation scenario, which the reference clock (IN) is 5MHz. When the reset is triggered, the ADPLL starts to track the frequency and phase of reference clock. The DCO control codeword (codeword [18:0]) is converged to desired 5MHz until the lock signal is enabled. By using binary search step in process calibration state, 1st acquisition and 2nd acquisition state as described in Section 3.3, the ADPLL can finish the tracking state in 608 (n*(2*log(2^N) + 6) + s*2^F +64) reference clock cycles in this worst case. Here , n is determined by the closed-loop's response time; N is control bits of DCO; F is fine tuning control bits; s is collected of previous UP/DOWN in each tuning stage. The total tap length of the DLF is 256 cycles. During the tracking time, it is found that RESET_DCO signal is sent frequently to update the DCO loop to a new delay path to avoid the glitches in the loop.

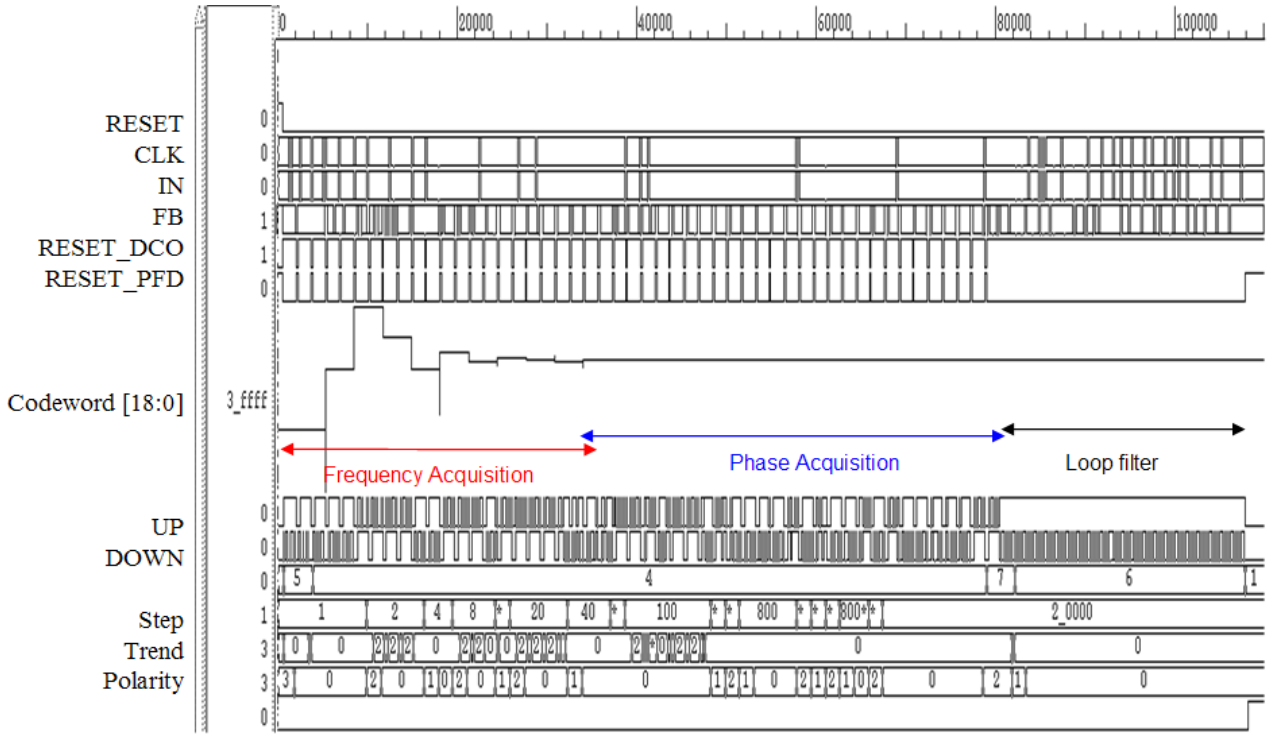


FIG. 14. Simulated waveforms of APDLL for eCrystal process calibration

3.6 Implementation

This design is implemented in the UMC 90nm 1P9M regular threshold voltage (SPRVT) CMOS technology. The generated codeword are 19bits at 5MHz output frequency. The lock-in time is designed within 544 cycles. The delay cell resolutions of 1st ~ 3rd tuning stage in the HDC-based DCO circuit are 98.7ns, 62.9ps and 2.04ps, respectively. With the scaled 1.0V, the average total power consumption is 125uW in the calibration mode. The total area of this design without the DCO circuits is 200 x 135 $um^{2.}$ This is integrated in a test system for system verification with the ADPLL for eCrystal process calibration, where the chip layout of the ADPLL for eCrystal process calibration is shown in FIG. 15.

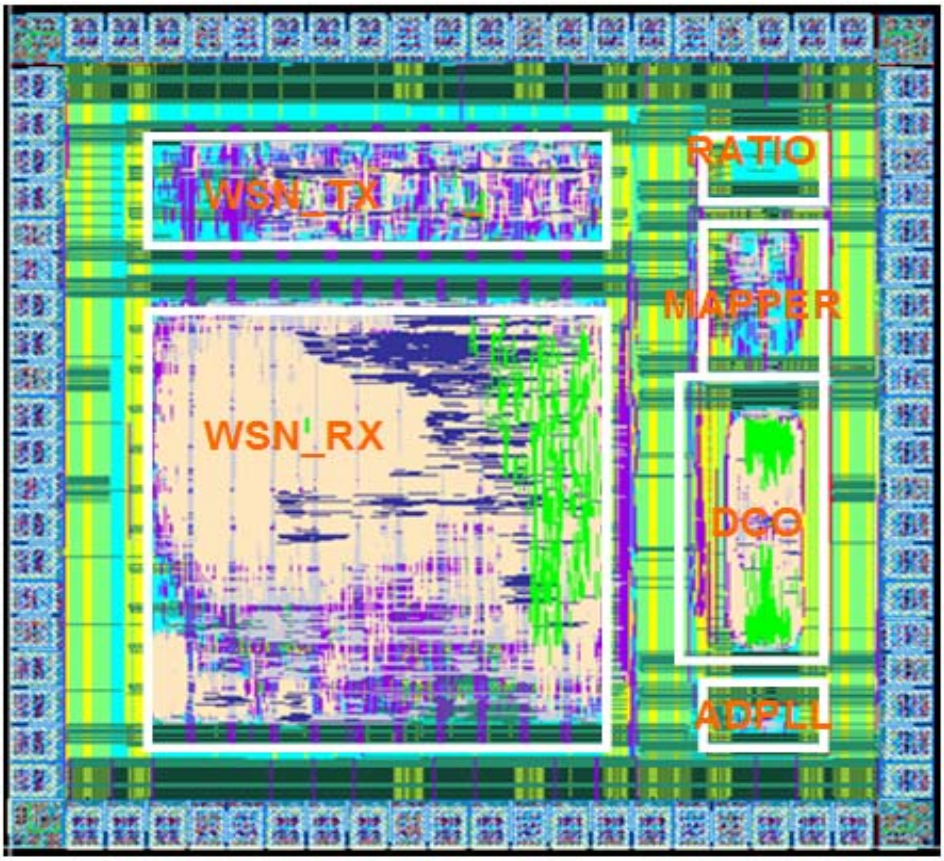


FIG. 15. Test system for system verification with the ADPLL for eCrystal process calibration

FIG. 16 lists the overall comparison with the state-of-the-art in the PLL. The proposed ADPLL has the lowest power dissipation compared with other designs. As a result, the proposed ADPLL indeed has the benefits of better area, high resolution for low power applications.

	This Work	[37] JSSC'03	[38] ISSCC'04	[39] ISCAS'05	[40] ISCAS'09	[14] JSSC'03	[41] MIRC'06
Control method	digital	analog	digital	analog	digital	digital	digital
Process	90nm	0.13um	90nm	0.18um	0.18um	0.35um	0.13um
Power (mW@MHz)	0.125 @5MHz 0.205 @200MHz	7 @240MHz	1.7 @520MHz	15 @378MHz	5.4 @160MHz	100 @500MHz	2.9 @1000MHz
Operation (MHz)	3.8~239	30~650	0.18~600	2.4~378	87~50	45~510	300~1000 (6 frequencies)
Supply	1	1.5	1	1.8	1.8	3.3	1.2
Resolution (ps)	2.04	N/A	N/A	DFC	N/A	5	20
Control (bits)	19	12	N/A	N/A	9	12	11
Area (mm^2)	0.135	0.182	0.18	0.16	0.724	0.71	0.012
Lock time (cycles)	worst case 608	N/A	> 150	< 75	72	46	15
Jitter	1.3% @5MHz	2.8% @143MHz	1.2% @30.7MHz	4.8% @30.4MHz	2.4% @160MHz	70 ps	120 ps @300MHz

TABLE 6: Comparison with the state-of-the-art (PLLs)

3.7 Summary

An ADPLL for embedded silicon oscillator process calibration is presented in this chapter. The proposed circuits can help the eCrystal to collect the Locked Code under different operation corners. By collecting the different corner Locked Code and Ratio data from delay estimator, the eCrystal is able to calculate the process dependent parameters (PDPs) which will be recorded into a one-time programming (OTP) or register files. Based on this information, it can ensure the embedded silicon oscillator which is able to compensate the frequency error without any external components. Therefore, this proposed ADPLL for eCrystal process calibration can provide an accurate Locked

Code for embedded silicon oscillator which enables more robust and more convenient solutions in the manufacture of the semiconductor back-end.

At present, our researches still can be improved in many aspects, the locked time is limited by the response time of each blocks, the average codeword also spends some settle time. It can add some blocks to improve the locked time such as time to digital convertor (TDC) or new search algorithm [13]. Hence, it can reduce the calibration time for more systems.

Chapter 4
All Digital Pulse Width Control Loop

In this chapter, an all-digital pulse width control loop (ADPWCL) with adjustable duty cycle is proposed in UMC 90nm 1P9M CMOS technology. Based on the proposed circuit, not only the 50% duty cycle of the clock can be generated but also does not need a look up table. The duty cycle of the output clock can be adjusted form 10% to 90% in step of 10%. The operation frequency of each proposed circuit is from the range of 5MHz to 60MHz. In order to work in a wide operation range, the hysteresis-delay-cell (HDC) based have been adopted to replace a lot of cascading buffers or inverters [19-20] which can enhance the power efficiency and area efficiency.

4.1 Introduction to Pulsewidth Control Loop

The pulsewidth control loop (PWCL) is a feedback loop [21]. The duty cycle can be kept the same in input clock and output clock, or be forced to any percentage according to the desired control code. The configuration of the PWCL is shown in FIG. 17. Assume the CK_{IN} has a 50% duty cycle and it generates V_{REF} for the differential pair amplifier. The CK_{OUT} will have deviation after passing through the buffer. Therefore, the duty cycle of CK_{OUT} is converted into a voltage, V_C.

The differential pair amplifier is used to produce a final voltage V_{CTR} that is proportional to the pulsewidth difference between CK_{IN} and CK_{OUT}.

We assume that the pulse width of the clock buffer is controllable. It means that when the pulse width of clock buffer output derivates an offset from a required duty cycle, it should be possible to adjust the control voltage, so that the offset is removed It implies that the controllable dynamic range will cover that range of possible offset. The number of stages in the clock buffer must meet a condition that negative feedback is guaranteed. In order to reduce the control power and the static current, it is preferable to choose the first stage of the clock buffer as the controllable stage.

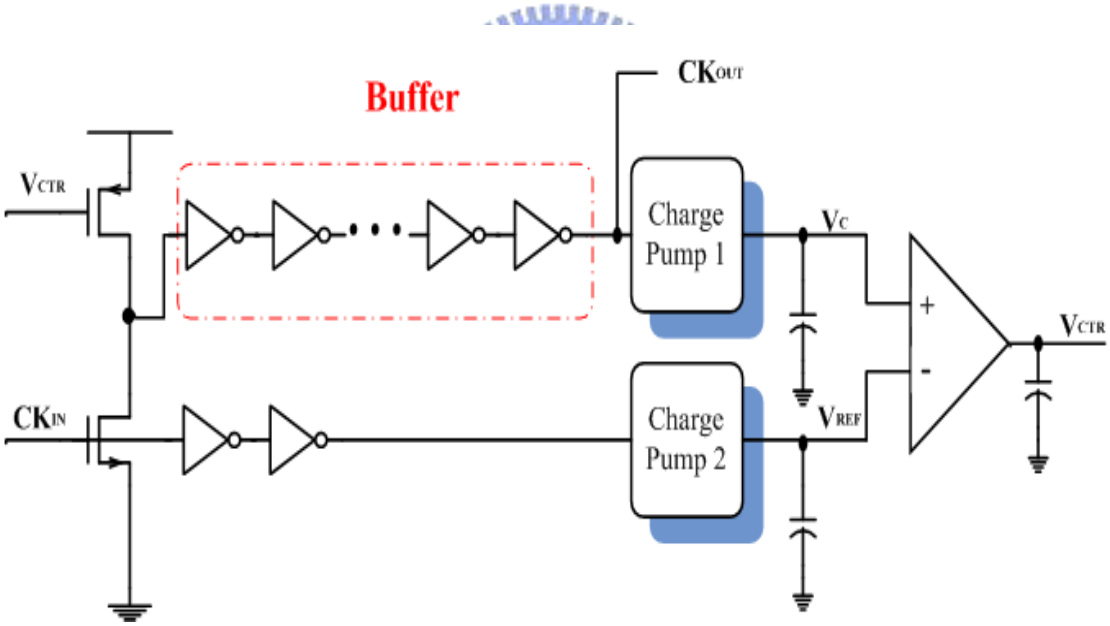


FIG. 16. Configuration of the PWCL

4.2 Architecture

This proposed all-digital PWCL is shown in FIG. 18. This ADPWCL consists of a one-shot circuit, pulse generator, counter, delay generator, PVT compensator, mapping delay line (MDL) and auto calibration circuit (ACC).

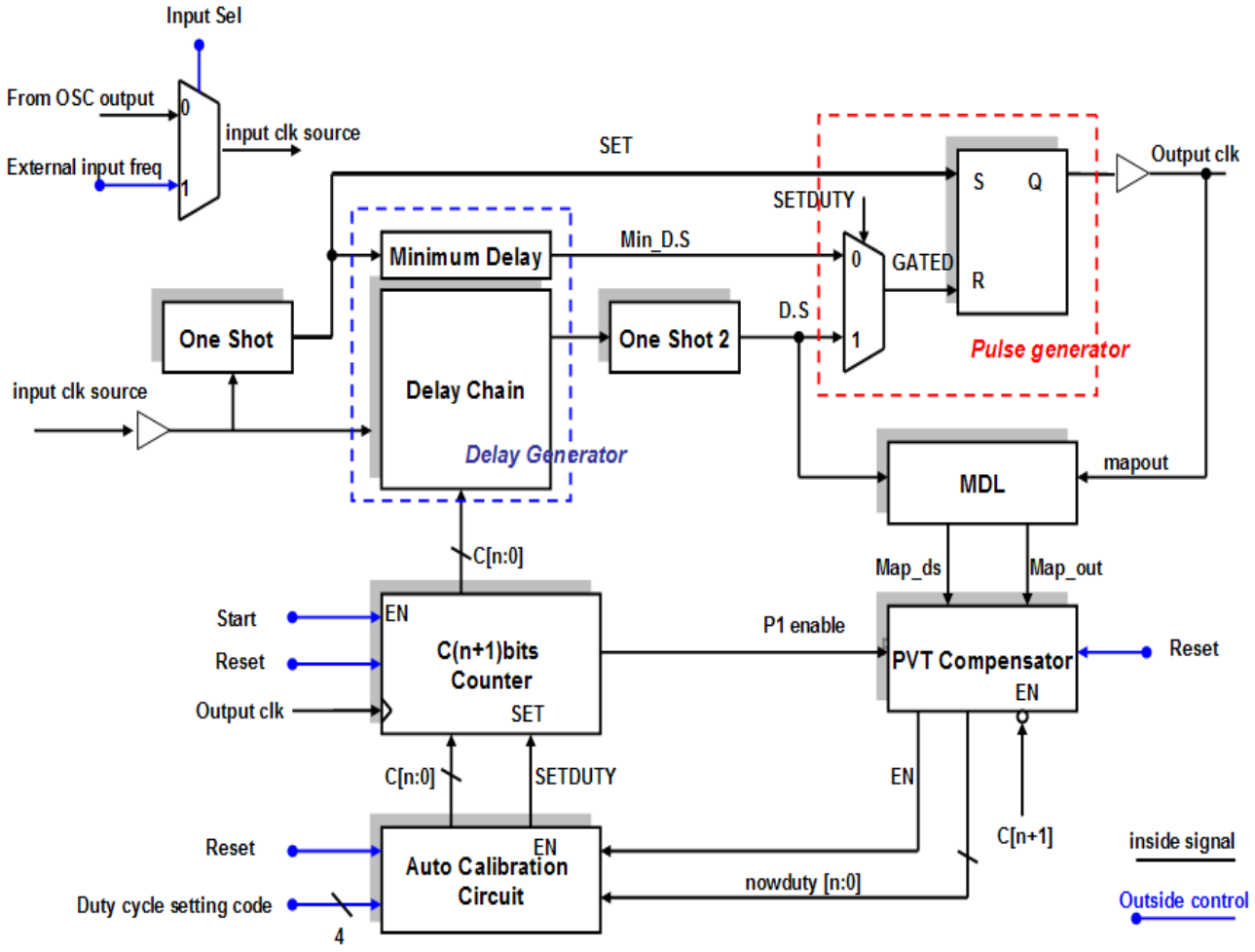


FIG. 17. Proposed ADPWCL

The operation of the proposed ADPWCL can be briefly described as follows. The input clock source is selected from eCrystal or external input clock by “Input Sel” signal. After the system reset, PVT compensator will send “EN” signal to ACC that will set the path select (MUX) of pulse generator to choose the minimum delay by “SETDUTY”. At this moment, ACC will be turned off

for power saving. After passing input clock buffer, the “input clock source” will pass through the delay chain and one shot 2 to generate the delay sequence, “D.S”. The one shot circuit [22] generates the internal clock, “SET”, to set the SR-latch. The internal clock, “SET”, will pass through the minimum delay to generate the minimum delay sequence (Min_D.S). One of the delay sequences is selected by multiplexer (MUX) of the pulse generator to gate the SR-latch, “GATED”. While the input clock source passes through the one shot circuit, the SR-latch and output buffer, the output clock will be generated. The duty cycles of the input and output clocks may be different due to the distortion caused by the one shot, pulse generator and buffer.

When the “Start” signal active, the counter will generate the signal, “P1”, to enable the PVT compensator. After “D.S” passes through the MDL, the signal, “Map_ds” will allow the PVT compensator to receive, and then converts the duty cycle at the moment and the period of the output clock into digital codes by using two internal counters. There are two converted codes which are able to calculate the digital codes of the total period, “period”, and “nowduty”. The digital codes of the total period represent how many delay cells passed in whole period of the input clock source. The phase of D.S and output clock are not synchronous due to the propagation delay caused by pulse generator, one shot circuit, clock buffer and some logical gate. MDL tries to align the phase between the D.S and output clock that can enhance the accuracy in the value of the digital code. After searching the total period of the input clock source, the PVT compensator will trigger the “EN” signal to high level which can wake up the ACC. According to the searched codes and desired digital codes of the duty cycle, ACC will calculate the signals “SETDUTY” to Counter. The calculated information is able to choose how many propagations interval delay time to decide if triggering the signal, “GATED”. The “GATED” signal is used to rest the falling edge of the output clock without influencing the duty of the input clock. Thus the desired duty cycle can be obtained. The detail timing diagram of the proposed architecture is shown in FIG. 19.

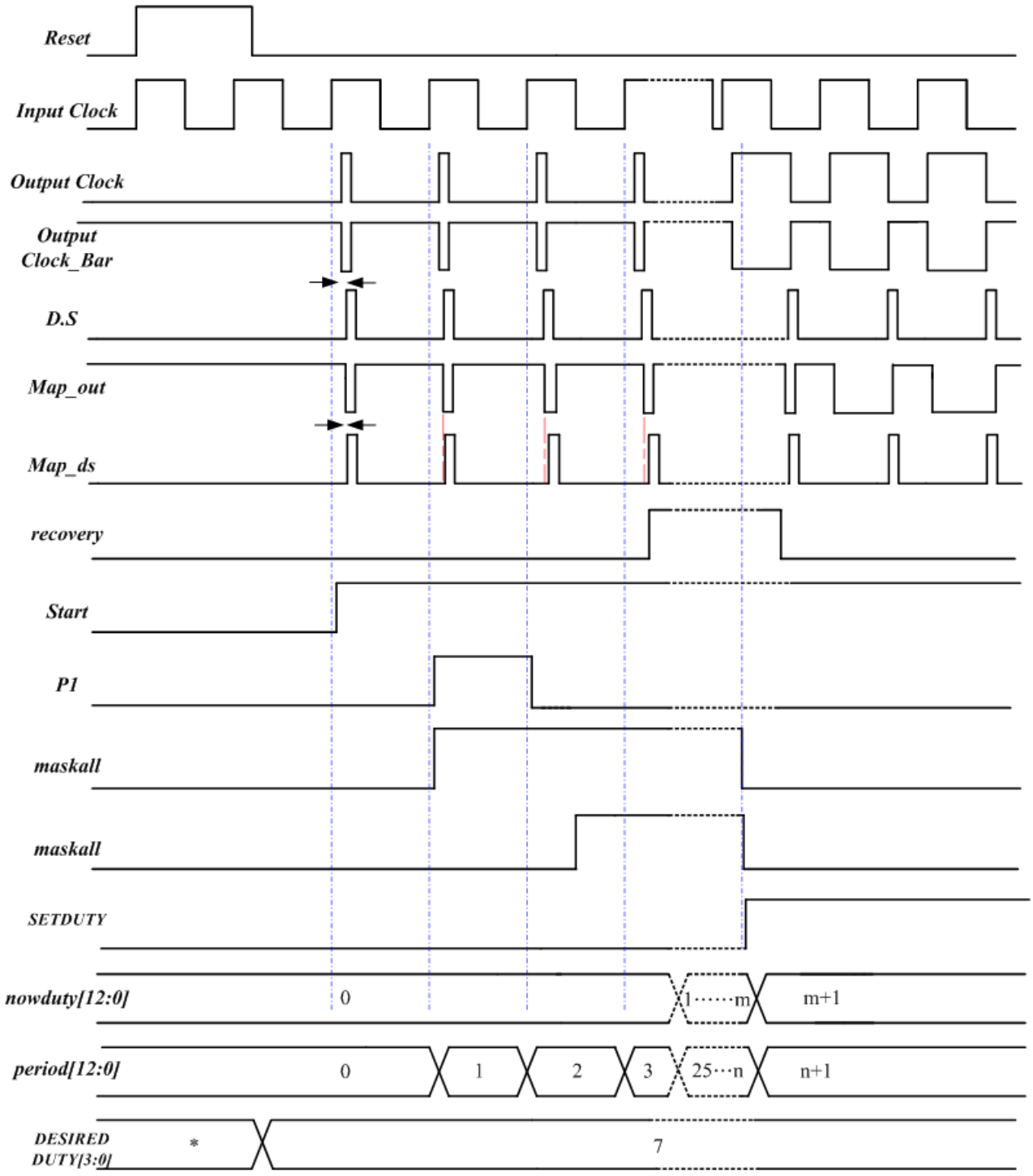


FIG. 18. The timing diagram of the proposed architecture

4.3 Circuit Design

4.3.1 Delay Generator

To meet power-critical or battery-less systems, a low power delay cell is required. We propose two different delay generators; one is using Hysteresis-delay-cell (HDC) [23-25] to replace a lot of cascading buffers or inverters which can enhance the power efficiency and area efficiency; the other is using standard cell base delay chain which can improve the non-monotonic effect from HDC base delay chain and accuracy in duty cycle.

Operation range	time period	Delay line tuning range (x 80%)	Resolution (error < 1%)	Cover range with delay number (pcs)
5M	200ns	160ns	1.6ns	100
5M~10M	100ns	160ns~80ns	0.8ns	200
5M~20M	50ns	160ns~40ns	0.4ns	400
5M~50M	20ns	160ns~16.7ns	167ps	1000
5M~60M	16ns	160ns~13.3ns	133ps	1200

TABLE 7: The relationship between operation range and delay chain

Wide operation range we used represents more delay cell we want. There has always been a trade-off between the power and resolution in the clock systems [19-20][28]. TABLE. 6 shows the relationship between operation range and the number of the delay. In the same accurate system, when the resolution is getting higher, the delay chain will also be increased causing longer locked

time, more area and more power consumption. According to specification of application or type, we can extend the stage number of each delay stage which may include coarse tune and fine tune stages.

4.3.2 Hysteresis Based Delay Cell

The hysteresis delay cells (HDCs), or named Schmitt triggers, have been widely used in digital and analog circuit for waveform shaping under noisy environment. The HDC based delay design follows the circuit topologies are proposed in [25]. The power-of-two delay is designed that every segment in the delay line has a delay in the twice descending order. So, each segment performs a propagation delay either half of previous segment or twice of the next one. FIG. 20 illustrates the architecture of the P2-Delay that is partitioned in a coarse-tuning stage and one fine-tuning stages. The coarse-tuning stage applies HDC as essential delay elements in variant topologies (cascade and nested). According to the HDC delays that cover a specific range, they are further defined as very-large-scale HDC (VLHDC), large-scale HDC (LHDC), medium-scale HDC (MHDC), and small-scale HDC (SHDC), in terms of delays.

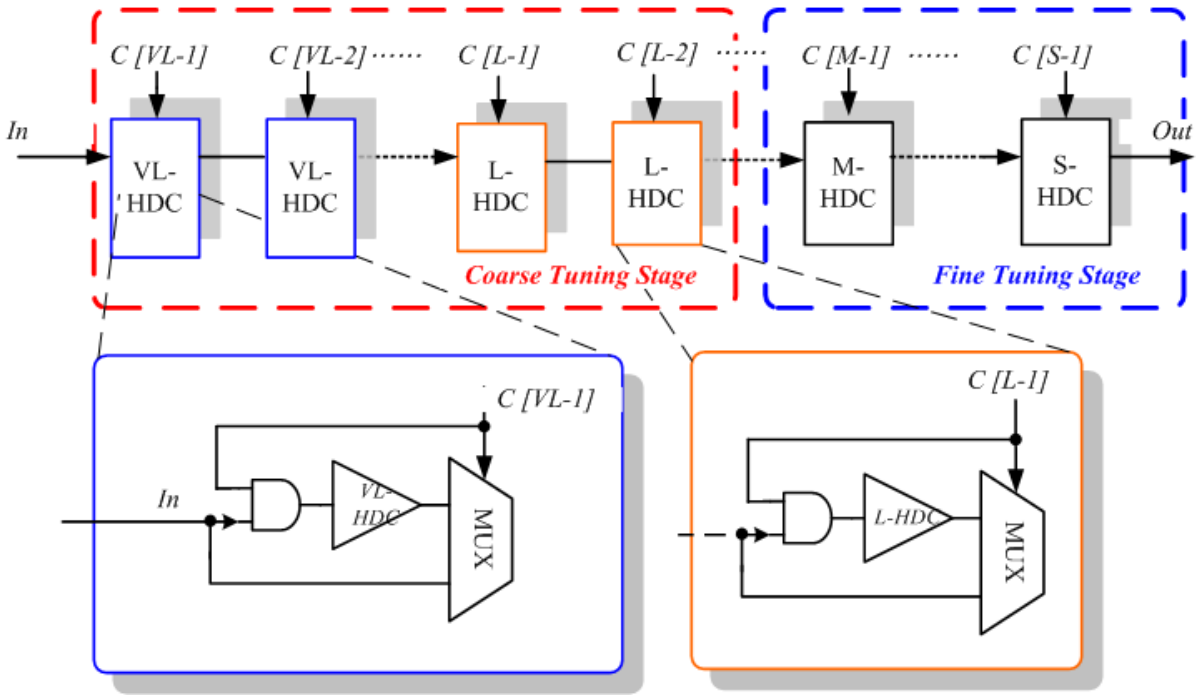
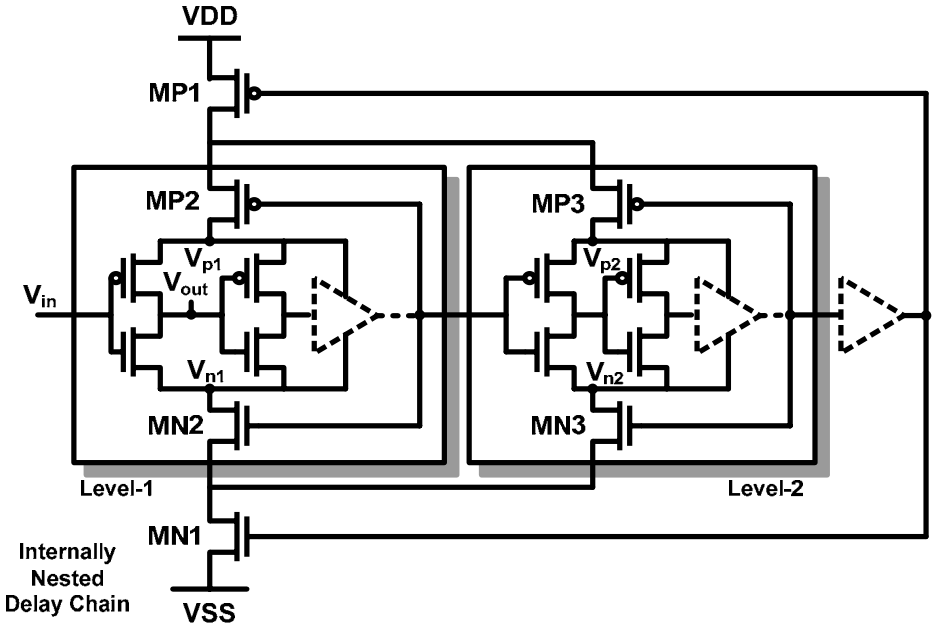
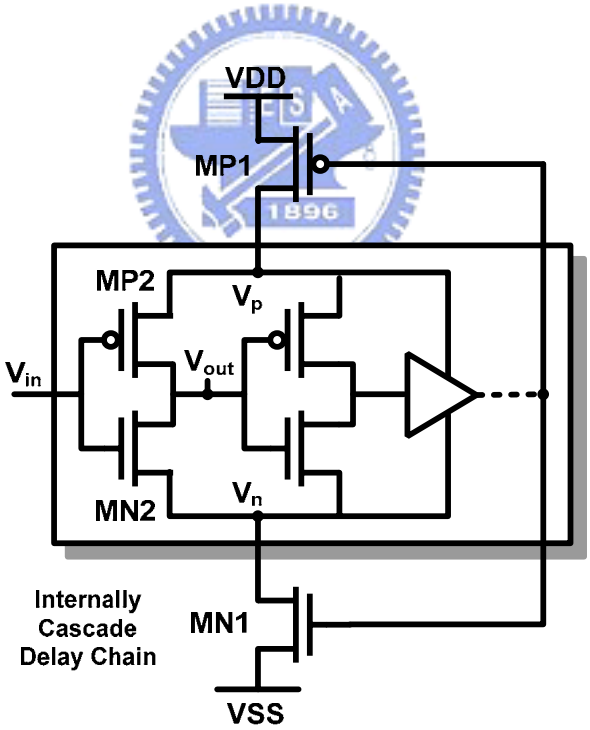


FIG. 19. The power of two delay stage block diagrams

The coarse-tuning stage is composed of VLHDCs and LHDCs, and multiplexers are used to determine if a VLHDC or a LHDC is in the signal propagation path or not. Moreover, an AND logic gate is used to block an input signal transition when the VLHDC or the LHDC is not selected. Both the VLHDC and LHDC can be internally sized and concatenated for different delay generation. The LHDC (or VLHDC) are designed to generate a delay that is several tens (or hundreds) times larger than a minimum-sized inverter in the same manufacturing process. This is achieved by increasing output rise-time or fall-time and at the same time avoiding large short current sink in the next stage to maintain the low power purpose. This is achieved by the use of Schmitt-trigger cells with the hysteresis phenomenon [25]. The architectures of the VLHDC and LHDC are shown in FIG. 21. The fine-tuning stage is composed of MHDC and SHDC that generate delays about 0.01~10 times of a minimum-sized inverter in the same manufacturing technology. Both the MHDCs and SHDCs are able to switch the propagation delay internally, instead of the use of multiplexers. The architectures of the MHDC and SHDC are illustrated in FIG. 22.

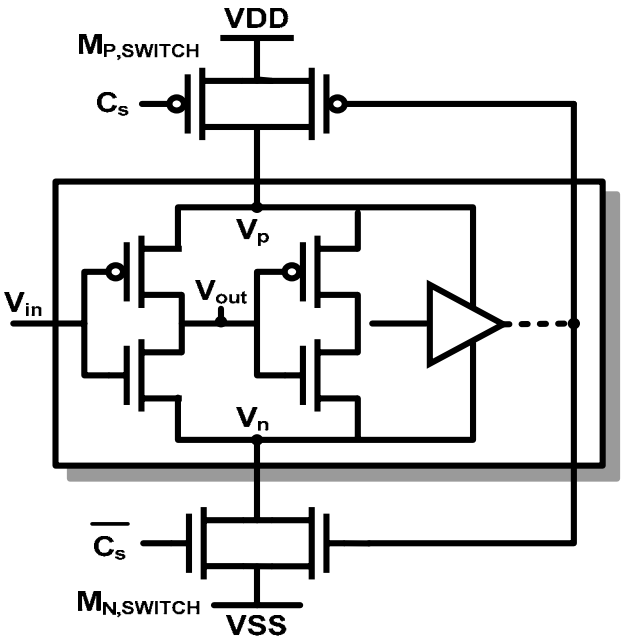


(a) Very-Large-scale Hysteresis Delay Cell (VLHDC);

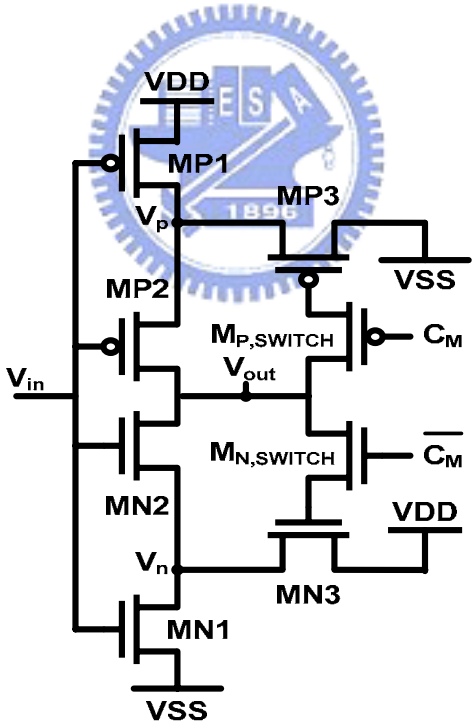


(b) Large-scale Hysteresis Delay Cell (LHDC)

FIG. 20. Very-Large-scale and Large-scale Hysteresis Delay Cell



(a) Medium-scale Hysteresis Delay Cell (MHDC);



(b) Small-scale Hysteresis Delay Cell (SHDC)

FIG. 21. Medium-scale and Small-scale Hysteresis Delay Cell

The summation of tune range is about 117.56ns to 0.458ns in coarse tune stage in typical corner cases, the fine tune tuning range is about 0.934ns to 47ps in typical corner by HSPICE simulation.

4.3.3 Standard Cell Delay Line

The proposed II uses cell-based delay cell. The block diagram is shown in FIG. 22. The coarse tune stage employs cascading structure [26] with path selector to maintain delay linearity and extend operation range easily. There are 8 bits of coarse tuning control codes for the 256-to-1 path selector. The difference of the delay time between two neighbor paths is determined by one coarse tuning delay cell including one buffer (BUF) and one multiplexer (MUX) as shown in FIG. 23. The summation of propagation delay is about 1.32ns in coarse tune stage under PVT conditions (TT, 1V, 25℃); 2.367ns under PVT conditions (SS, 0.9V, 100℃); 0.877ns under PVT conditions (FF, 1.1V 0℃) by ULTRASIM simulation. Moreover, the fine tune stage is constructed after the coarse tune stage to achieve better resolution of the proposed II delay chain. The circuit topology in the fine tune stage follows the coarse stage except that the minimum delay resolution is 125ps under PVT conditions (TT, 1V, 25℃); 222ps under PVT conditions (SS, 0.9V, 100℃); 85.4ps under PVT conditions (FF, 1.1V 0℃) with 5bits control code. There are 5 bits of fine tuning control code for the 32-to-1 path selector. In addition, both tuning stage need extra encoders to translate the control code to each control signal of MUX.

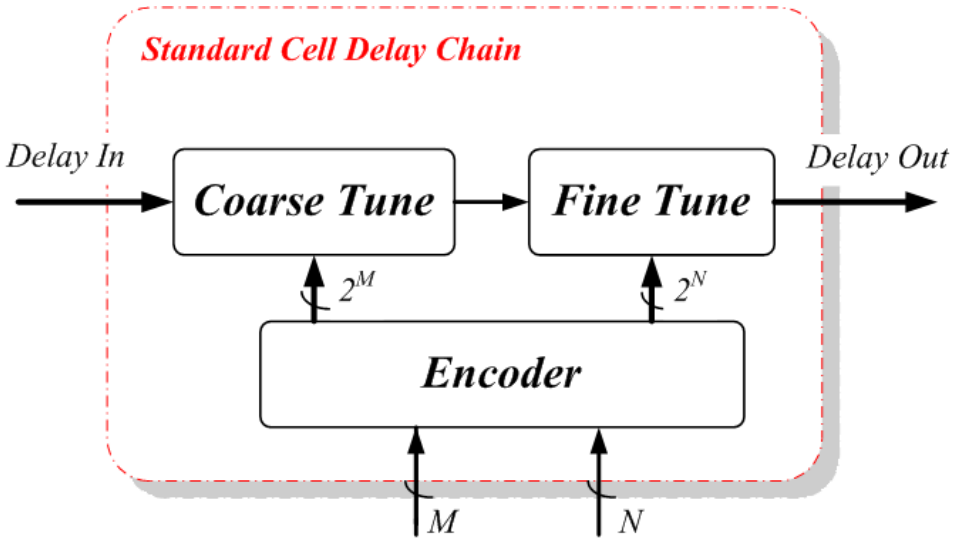


FIG. 22. Standard Cell Delay Line

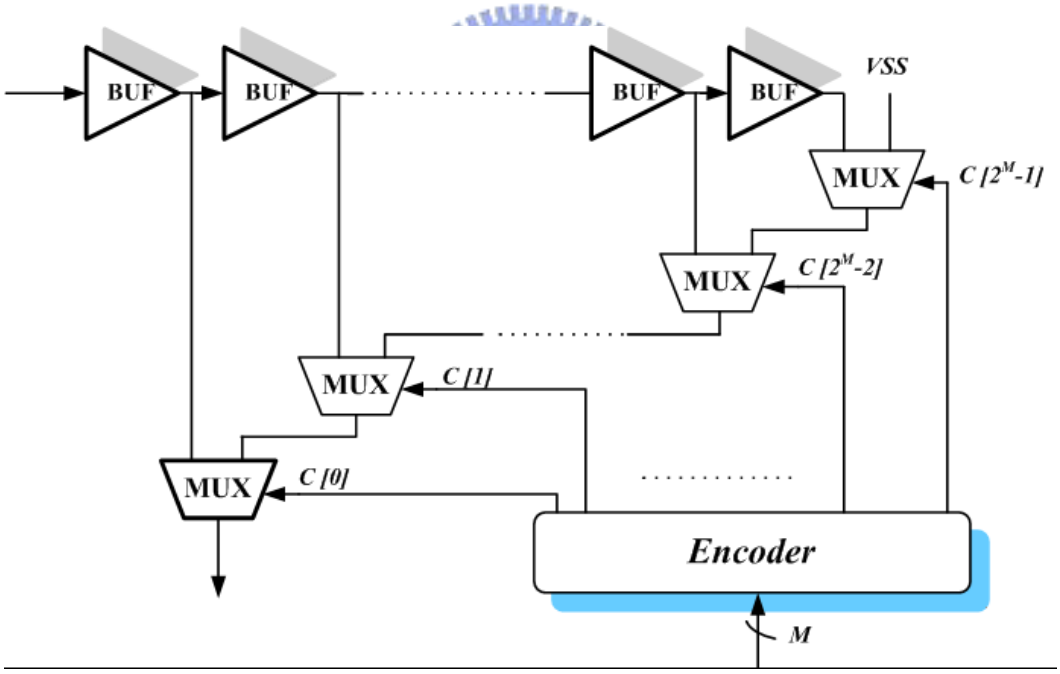


FIG. 23. Architecture of coarse tuning stage and fine tuning stage.

4.3.4 One Shot

The one-shot circuit [22] is shown in FIG. 24. It produces an internal clock with a fixed pulse width, and it means fixed duty cycle no matter what the duty cycle of the input clock is. The buffer delay Δt decides the width of the pulse output.

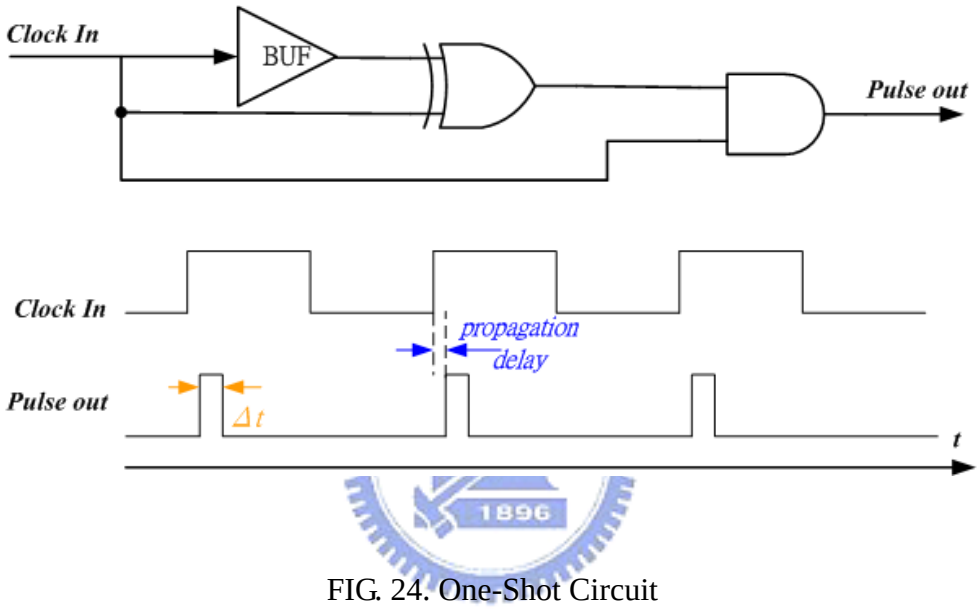


FIG. 24. One-Shot Circuit

4.3.5 Pulse Generator

The pulse generator is composed of an SR-latch and 2-to-1 multiplex (MUX) shown in FIG. 17. In the compensation periods, the MUX selects the minimum delay from the delay generator by controlling signal, “SETDUTY”, and the pulse generator produces an internal clock with a fix duty cycle which is equal to minimum delay from the delay generator. After the compensation period is finished, according to duty cycle setting code, auto calibrator circuit will decide when to reset the SR- latch which is able to adjust the duty cycle of the output clock by desired duty cycle.

4.3.6 PVT Compensator

The main function of PVT compensator is converting the period and duty cycle of the output clock into a digital code. This design follows the circuit topology proposed in [30]. The block diagram is shown in FIG. 26. After the enable signal (P1) is activated by the (n+1 bits) counter, the signal, “Map_ds”, is sequentially generated from the delay generator after passing through the one shot 2 circuit and MDL to sample the signal. “Map_out” is generated from output clock after passing through the MDL and one inverter. The sampled output signal “recovery” will be generated and its duty cycle is equal to an arbitrary as constant *K* that of the inverse output clock. However, the frequency of the signal, “recovery”, is much slower than that of the output clock. The counter designs based on time to digital convertor (TDC) are used to convert the period and duty cycle of the signal, “recovery”, into the digital code.

The counters are activated by two signals, “maskmin” and “maskall”. Following the signal, the counter will decide whether taking count of once or not in every input clock cycle relatively. Each series consists of two edge detectors and one SR-latch used to generate the signals including the “maskmin” and the “maskall”. When the signal “Start” is activated, P1 signal makes the “maskall” signal remaining high until “recovery” touches the falling edge. Besides, the signal “maskmin” remains low level until “recovery” touches the rising edge, and following the “recovery” signal goes down. Both signals will enable two counters to count within a time interval. Both counters will count the digital code; one is inversed from output clock called “period”, and the other from internal clock named “nowduty”. Two counting values will represent the duty cycle of the internal clock and inverse output clock.

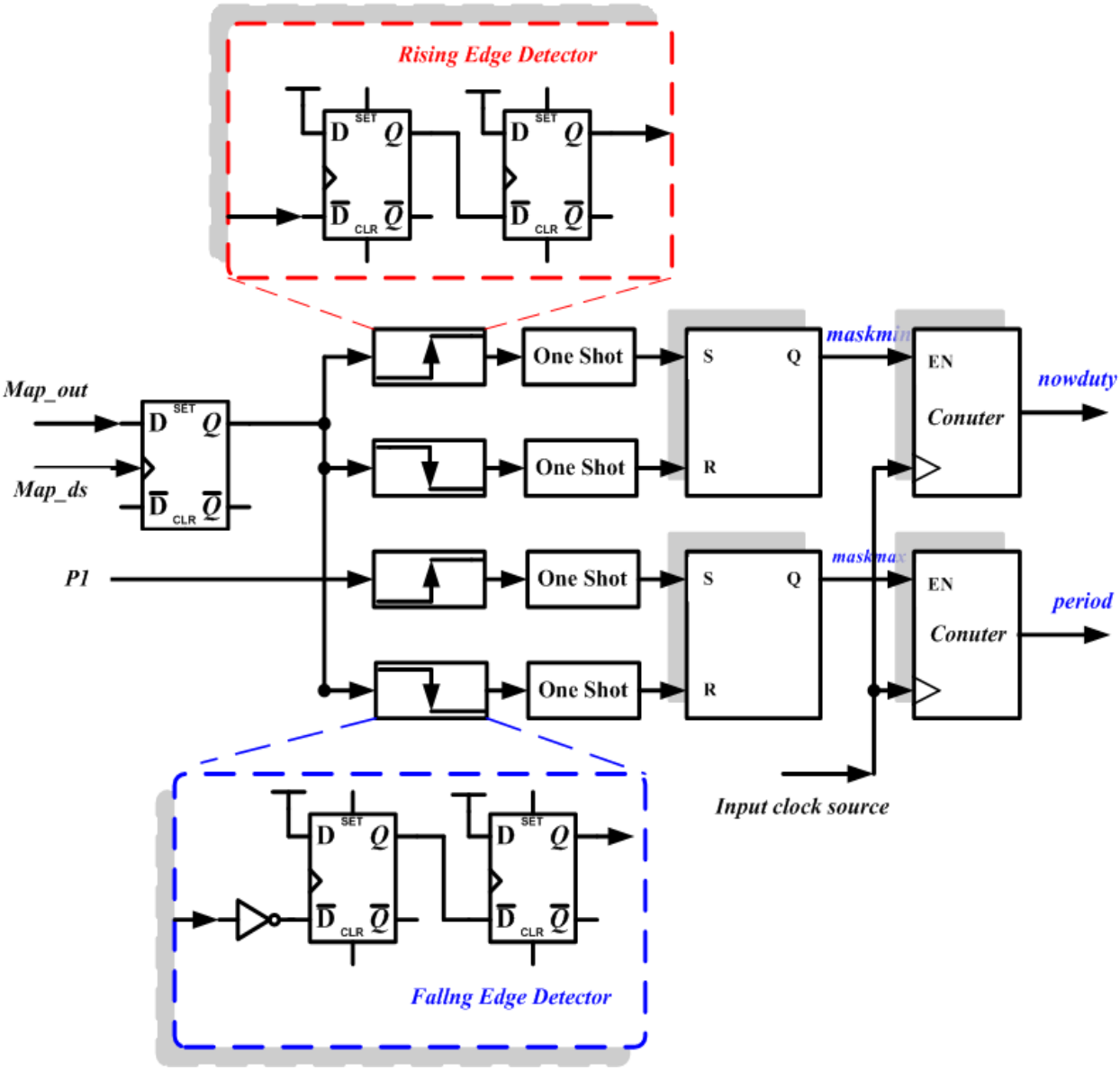


FIG. 25. PVT compensator block diagram

4.3.7 Mapping Delay Line

The mapping delay line (MDL) consists of a few AND gates, MUX and inverters. Timing diagram is shown in FIG. 17. Due to the propagation delay caused by pulse generator, one shot circuit, clock buffer and some logical gates, the phase of mismatch causes the duty cycle error from

time to digital convertor (TDC). Therefore, the proposed MDL is able to align the phase between the delay sequence (D.S) and output clock as close as possible. In order to balance the two phases, we use a dummy delay, similar to each propagation delay path. According to the different path between the D.S and output clock, most of the difference comes from the Pulse Generator and MUX which is composed of one SR-Latch and a few logical gates. The proposed mapping delay line uses the similar architecture to generate a same propagation delay.

4.3.8 Auto Calibration Circuit

Hardware Description Language (HDL) is used to describe the auto calibration circuit (ACC). The ACC is composed of one divider, a few multipliers and substraters. The ACC will calculate the desired duty cycle. It will combine the “nowduty” from the PVT compensator and external duty cycle setting code as shown in FIG. 17. The digital code “nowduty” denotes how far the current duty cycle is away from the duty cycle of 100%. We can follow the equation, “SETDUTY = desired duty cycle (%) * nowduty”, to calculate the duty cycle as we need. After four output clock cycles, ACC will generate the signal “SETDUTY” which chooses how many delay we want from the delay chain. The SETDUTY is a relative code which represents the desire duty cycle. The delay generator will be selected from the “SETDUTY” to reset the falling edge of the output clock. The final duty cycle can be adjusted from 10% to 90% in steps of 10% within a small error.

4.4 Simulation

This section will show the fully system simulation results. TABLE. 8 shows the results from proposed I and proposed II. The main difference of the proposed I and proposed II designs is delay generator shown in the red block. The leakage power takes about 6.5% and 4.1% of the total power consumption in the proposed I and proposed II designs.

	Proposed I			Proposed II		
Process	Cells	Area(um^2)	Total Power (nW)	Cells	Area(um^2)	Total Power (nW)
P2-HDC	N/A	1800	17913	None		
DEL1M1N	None			256	768	16013
Encoder 8 to 256	None			323	1039	8806
Multiplexer 256 to 1	None			383	1620	44820
13 bits Counter	69	510	81729	69	510	81729
ACC	1774	8995	147444	1774	8995	147444
PVT Compensator	138	782	30337	138	782	30337
Pulse Generator	5	17	357	5	17	357

TABLE 8: Resource Comparism between Proposed I and II

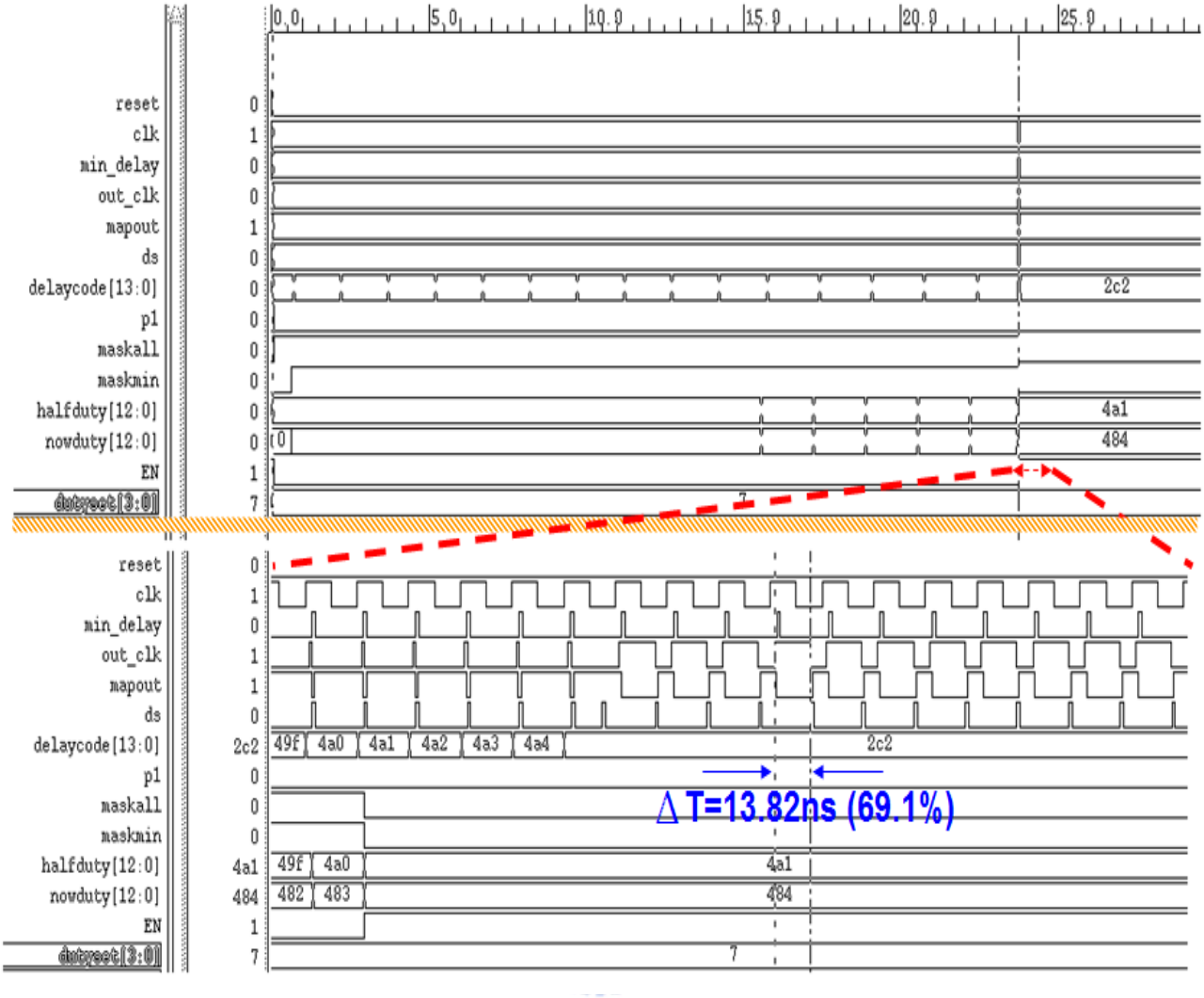


FIG. 26. Simulated waveforms of ADPWCL operation scenario.

FIG. 26 shows the transient response of the proposed ADPWCL operation scenario, where the input clock source (clk) is 50MHz at 50% duty cycle, and the desired duty cycle is 70%. The total locked time is about 23.5us, and the output duty is 68.7% with 1.3% error. FIG. 27 to FIG. 29 show the output clock with different desire duty cycle from 10% to 90% with input clock at 50MHz which with 50% duty cycle under different PVT corners.

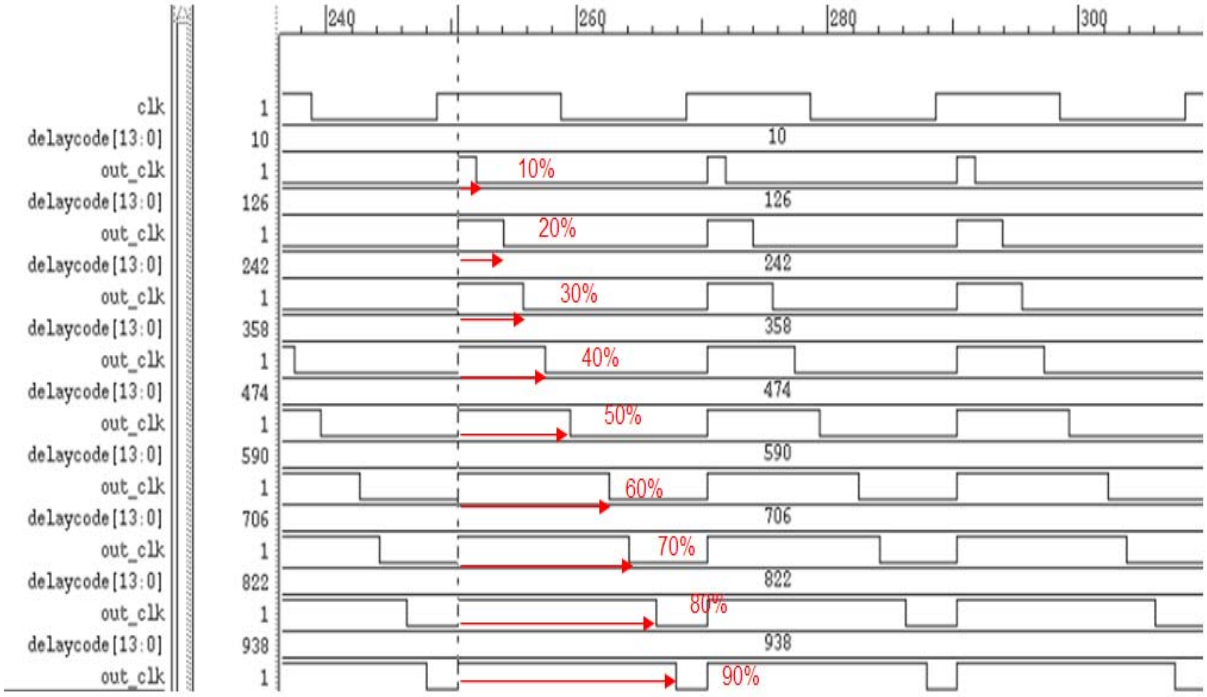


FIG. 27. Output clock with different duty cycle setting code under typical corner

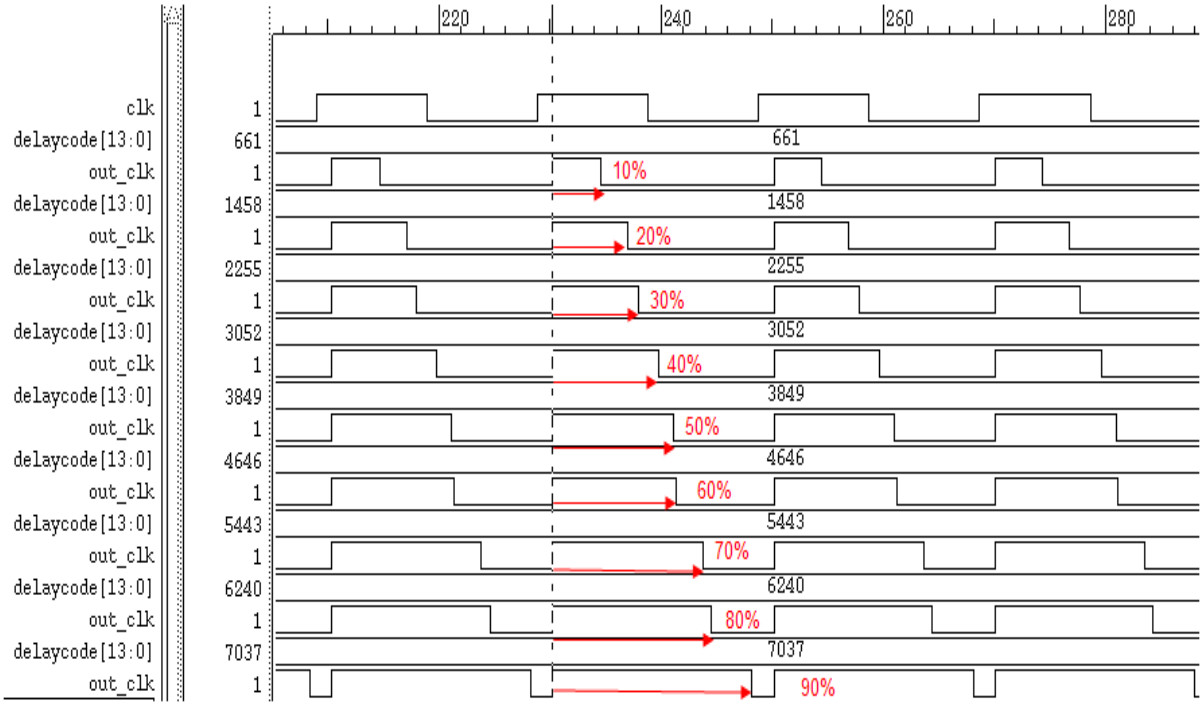


FIG. 28 Output clock with different duty cycle setting code under fast corner

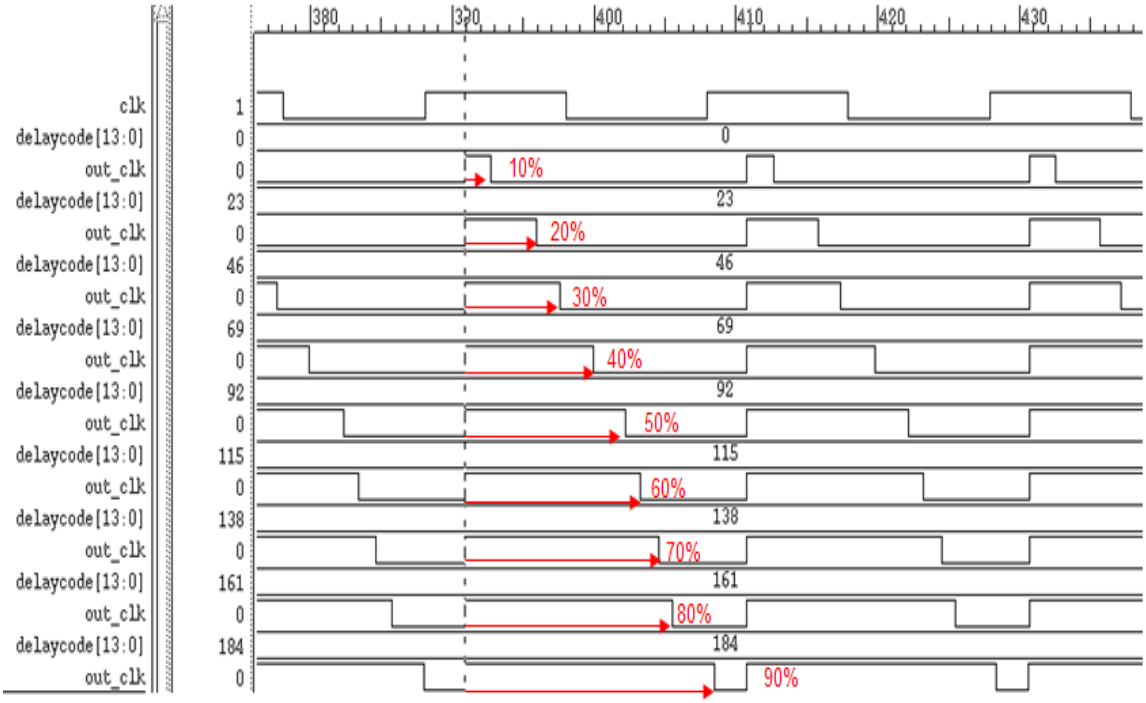


FIG. 29.Output clock with different duty cycle setting code under slow corner

FIG. 30 shows the area distribution between Proposed I and Proposed II Design. In the area of Proposed I and Proposed II, Auto Calibration Circuits takes mainly scale resulting from using multiplier and divider. In the rest of the area, it mainly comes from the delay cells because the long delay line has multiple delay stages to be controlled and it requires lots of circuits to decode the control signals. FIG. 31 shows the power distribution between Proposed I and Proposed II Design. In the power of Proposed I and Proposed II, a major part comes from an auto calibration circuits. The second part comes from the 13 bits counter which consumes a lot of power consumption in many flip-flops (DFFs), because the inverter is to make an edge-triggered DFF out of the two level-triggered.

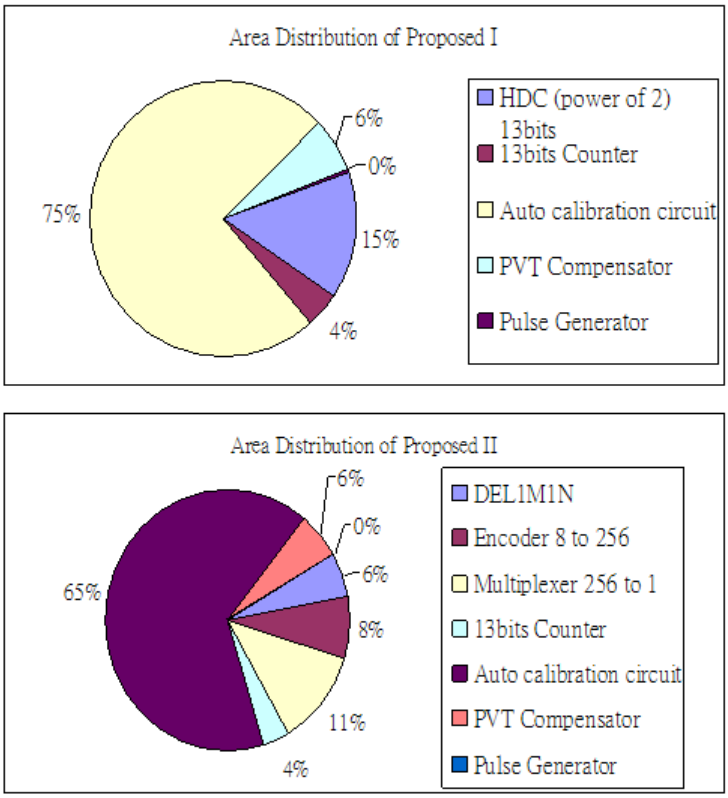


FIG. 30. shows the Area distribution in Proposed I and Proposed II Designs

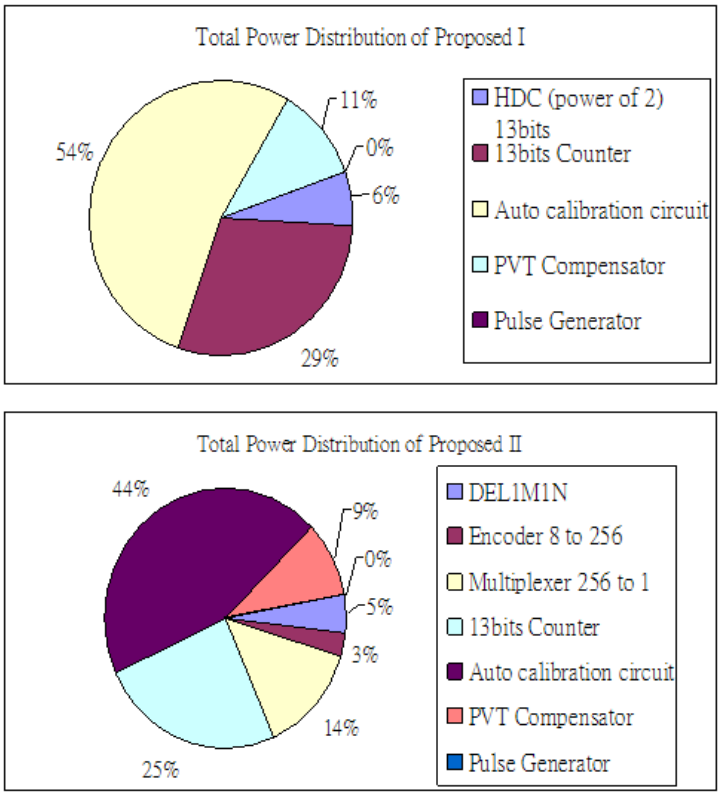


FIG. 31. shows the Power distribution in Proposed I and Proposed II Designs

TABLE 9 lists the overall comparison with the state-of-the-art in the PWCLs. The proposed ADPWCL has the second power dissipation compared with other designs, and also achieves wide duty cycle tuning range (x12). As a result, the proposed ADPWCL indeed has the benefits of better operation and tuning range, without look up table for low power applications.

	Proposed II (standard cell)	[19] JSSC 2006	[20] ASSC 2007	[28] VDAT 2006	[30] ISSCC 2004	[29] JSSC 2005
Control method	digital	digital	digital	digital	analog	analog
Process	90nm	0.35um	0.18um	0.35um	0.35um	0.35um
Power (mW)	0.13 @ 50MHz	20 @ 500MHz	2.7 @ 800MHz	16 @ 600MHz	270	150
Area (mm^2)	0.014	0.68	0.054	0.35	0.28	0.141
Operating range (MHz)	5~60	400~600	300~800	400~600	500~1250	1000~1270
Synchronous with input clock	NO	NO	YES	NO	NO	YES
Input duty range (%)	10~90	30~70	NA	25~75	50	N/A
Need of OP Amplifier	NO	NO	NO	NO	YES	YES
Adjustable duty cycle (%)	10~90/ step of 10 < 1%	30~70/ step of 10 < +/-0.64%	16.7~83.2 @300MHz/ <1%	50	35~70/ step of 5	35~70/ step of 5/ <6%
Lock cycle	2052 cycles (worst case)	28 cycles	N/A	8ns @ 500MHz	800~ 310 ns	N/A
Control bits	4	4	7	NO	7	N/A
Need look up table	NO	YES	YES	NO	NO	YES

TABLE 9: Comparison with the state-of-the-art (PWCLs)

4.5 Summary

In this chapter, we introduce low power consumption, small area and wide operation range all-digital pulse-width control loop (ADPWCL) without the input control codeword modified by look up table [26-27, 31]. The proposed ADPWCL does not need an operational transconductance amplifier [31-32]. A PVT compensator utilizes the counter-based time-to-digital conversion (CB-TDC) to detect the duty cycle and the period of the clock. Moreover, the requirement of the input clock with 50% duty cycle is eliminated. In proposed I adopting Hysteresis-delay-cell (HDC) to replace lots of cascading buffers or inverters [19-20] can enhance the power efficiency and area efficiency. The operation frequency range is from 30MHz to 60MHz. Unfortunately Hysteresis-delay-cell (HDC) based delay still has some drawbacks such as the non-monotonic effect and the necessity of covering all possible corners due to large PVT variations even if HDC has a good delay efficiency on the area and power. In the proposed II ADPWCL design, it uses standard cell based delay chain which not only enhances the duty cycle error coming from the non-monotonic effect than Proposed I, but also achieves more wide operation range. The operation frequency range is from 5MHz to 60MHz. Both the proposed circuits have been designed in a 90nm CMOS process. The simulated duty cycle of the output clock can be adjusted from 10% to 90% in steps of 10% within 5% and 1% duty cycle error in proposed I and proposed II. The locked time depends on the input clock frequency and the longest locked time needs 2^{12} cycles. TABLE. 6 shows the relationship between operation range and the number of the delay.

At present, our researches still can be improved in many aspects, A PVT compensator utilizes the counter-based time-to-digital conversion (CB-TDC) to detect the duty cycle and the period of a clock, and respectively, the locked time will be longer by using wide operation range. If we can using some block to detect what input frequency is, according the detected information, it can

decide different search step which can reduce the locked time.

Chapter 5
Conclusion and Future Work

5.1 Conclusion

With the continued and aggressive scaling of deep sub-micron CMOS technologies to the 65nm node and beyond, the cost of transistors or logic gates becomes cheaper. Also, in the noisy SoC (System on a Chip) environment, analog component is easily influenced by temperature, and crosstalk and leakage capacitance voltage. It is quite obvious that some circuits are implemented with digital approach algorithm. Also with the explosive growth of the wireless communication industry, more and more circuits can be integrated into a single chip and successfully realized by the System on a Chip (SoC) design technology.

This thesis consists of two parts: One is an ADPLL for the embedded silicon oscillator PVT calibration, the other is the ADPWCL with adjustable duty cycles. Although the operations are different, their basic concepts are similar. By means of this analogy, the design method and the analysis can refer to each other.

First, to meet high integration, low power consumption and low cost for computer, consumer

and communication products, an embedded silicon oscillator is desired to replace existing crystal and external components. An ADPLL for the embedded silicon oscillator calibration to overcome the variation of process, voltage and temperature (PVT) is proposed in Chapter 3.

Secondly, reducing the energy is also required in the low power and low data rate communication systems such as WBAN application, duty cycle control (DCC) [3-4]. Some special analog-to-digital (ADC) or digital-to analog (DAC) systems [2] need the clock generators with programmable duty cycles. We proposed a low power consumption, low cost and wide operation range ADPWCL with adjustable duty cycles in chapter 4. In proposed I circuit, we introduced a Hysteresis-delay-cell (HDC) based delay chain to enhance the power efficiency and area efficiency. The operation frequency range is from 30MHz to 60MHz. In proposed II circuit, we use standard cell base delay chain which can not only improve the non-monotonic effect from HDC base delay chain, but also have more accuracy and widely operation range. The operation frequency range is from 5MHz to 60MHz. Both proposed circuits have been designed and simulated in a 90nm CMOS process. Moreover, our proposed architecture does not need look up table. The simulated duty cycle of the output clock can be adjusted form 10% to 90% in steps of 10%.within 5% and 1% duty cycle error in each design. The locked time of the proposed ADPWCL depends on the input clock frequency, and the longest locked time needs 2052 cycles.

5.2 Future Work

In the future, the following work is to replace the discrete components in the hardware prototype of eCrystal Oscillator by ASIC designs, such as crystal oscillator, resistors and capacitance. And this eCrystal oscillator can be further integrated into baseband of the receiver

node. For better performance of wireless communication system, we can figure out a delay cell which is independent of temperature variation to replace the standard cell.

Through these integrations, we can implement an ultra low power and low cost clock generator module with frequency and duty cycles tunable capability, which can improve the reliability and provide the competitiveness in many wireless communication systems.

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