共鍍銅鈦金屬在三維接合連線之電性分析及可靠度測量

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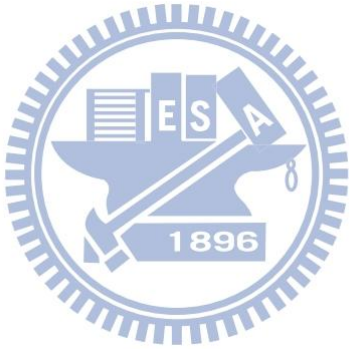
摘　　要

這幾年來因為電晶體的微縮已經快要到達物理上和光學上的極限，半導體製程需要新的技術以繼續維持產業的進步和功能的提升。有鑑於此，三維電路整合的技術被廣泛的討論研究，這項技術被認為是未來半導體發展的主流。三維電路整合有兩大關鍵，其一是接合技術的發展，另外是矽穿孔的製程。

本篇論文著重於利用共鍍銅/鈦金屬作為三維電路整合之接合材料。根據先前的研究，共鍍銅/鈦金屬在高溫下擴散的機制，會有金屬分層的情況，並適合做為三維結構的接合金屬。在這篇論文中將探討共鍍銅/鈦金屬在不同接合環境下的金屬分布情形，還有在晶片及

晶圓接合上的結果比較。在經過接合之後，我們發現有自動形成的鈦黏接層，可能的鈦氧化物側壁保護層，以及主要的銅-銅接合/導電層。

在本篇論文中，我們也有提供關於此結構的電性量測結果，而所測得的結果和一般傳統銅銅接合有相近的電性特質。除此之外，我們也利用許多不同的實驗來測試此結構的可靠度。實驗包含:濕度測試，溫度變化測試，劣化測試…等。各個實驗結果也都顯示，此結構有良好的穩定性及可靠度。



Electrical Performance and Reliability Investigation of Co-sputtered Cu/Ti as 3D Bonded Interconnect

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Abstract:

Due to the physical and lithographical limitations, current scaling of transistors is reaching its bottleneck. To overcome this obstacle and continue to improve performance, the concept of 3D integration has been proposed. Current major efforts in 3D integration include the reliability of the bonding technology and the fabrication of TSV.

This thesis is dedicated to the research of using co-sputtered Cu/Ti as bonding medium in 3D integration, for its interesting properties exhibit after thermo-compression bonding. The study covers the analysis of diffusion mechanism of co-sputtered Cu/Ti under different bonding conditions at both chip and wafer level. It is proved that a self-formed adhesion layer is presented during bonding, possible Ti oxide is formed as sidewall passivation layer, and Cu is the major bonding/conducting

medium.

Electrical analysis is also performed on the structure, and the result is comparable to the direct Cu-Cu bonding case. In addition, the structure is also examined under various reliability tests, and is verified as a stable bonding structure in all tests.

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Outline

Table Caption

Chapter1 Introduction

Chapter 3

Characteristic of Co-sputtered Cu/Ti Bonded Interconnect

Figure Captions

Chapter 1 Introduction

Chapter 2 Experimental Instruments

Chapter 3

Process Evaluation and Material Selection of Hybrid Bonding for Three-dimensional Integrated Circuit

Chapter 4

Reliability Evaluation of Co-sputtered Cu/Ti Bonded Interconnects