Chapter 1
Introduction

1-1 Background

Ever since the invention of the first transistor, semiconductor industry has thrived in the past few decades. The development of semiconductor industry has followed the prediction of Moore's Law, with the number of transistors on a chip doubles every 18 months. However, the conventional method of shrinking the size of the transistor is approaching its physical limit.[1-3] In order to solve this problem and continue to meet the requirement of Moore's Law, various methods are proposed. Among all, 3D integration circuits(3DIC) is the most promising solution. By stacking convention 2D IC in the vertical direction, and invoking through silicon vias(TSV) for inter-chip communication, 3DIC exhibits numerous advantages over other technologies.[4-5] Intel roadmap has announced to introduce the 3D integration technology to the picture, as shown in Fig.1-1. This announcement verified the importance of 3D integration, and the future trend for semiconductor industry for the next generation.

With TSV to assemble the 2D chips, the global interconnect length can be greatly reduced, for the 2D layout extended with an extra dimension, the reroute and detour on the original 2D plane can be avoided. Moreover, the number of I/O pins is largely increased, as shown in Fig.1-2.

In addition, the stacking of ICs provides the advantages of heterogeneous integration. Due to different substrates and technology nodes used in different applications, heterogeneous integration has always been a appealing but challenging task. Now, as in Fig.1-3, with the help of 3D integration, by connecting different chips into a single 3DIC, heterogeneous integration is no longer a dream.

Although 3D integration shows great potential in many aspects, current development of the technology is still immature and needs further investigation. The major issues for 3D integration lay in the fields of bonding technology and TSV fabrication. A general overview of different 3D integration methods are shown in Table. 1.

1-2 Bonding Technology for 3D Integration

There are three major types of bonding medium, metal-to-metal,

oxide-to-oxide, and polymer-to polymer bonding. Each type has its own advantages and disadvantages. In brief, metal-to-metal bonding has the features of good electrical performance, and less cleanliness requirement. Oxide-to-oxide bonding and polymer-to-polymer bonding, on the other hand, could provide better bonding quality and tighter pitch. Among all these bonding materials, metal-to-metal bonding is the most prominent, for it serves as an extra metal layer, unlike the other two with the sole purpose of bonding.

However, the greatest concern of metal-to-metal bonding is the sparse region in between the metal lines, as in the illustration of metal bonding in Fig.1-4. Those regions may contain air and especially oxygen that could leads to oxidation and deterioration of the metal interconnects. Due to this problem, hybrid bonding of metal-to-metal bonding combined with oxygen-to oxygen bonding or polymer-to-polymer bonding is proposed.[6] Nevertheless, hybrid bonding requires more complicated fabrication technology and thus higher cost. Therefore, the search for the most suitable bonding medium is still an on-going topic.

1.3 Motivation

According to previous description, we understand that the search for suitable bonding medium is one of the most important tasks for 3D integration. In addition, with the advantages of metal-to-metal bonding, we could likely achieve a great performance. Cu-based interconnects are the mainstream of current semiconductor fabrication technology. 3D integration as an extension of current fabrication techniques, should be founded on previous knowledge and technology. Therefore, it is highly expected that 3D integration to be compatible with conventional fabrication methods, and inherit the usage of Cu interconnect.

Hence, our studies on metal-to-metal bonding are focus on using Cu as the main bonding material. However, copper is easily oxidized and prone to corrosion when exposed to air, reliability is a great issue for copper bonding. We thus seek our answers in co-sputtered metals, and based on their diffusion behavior under different annealed conditions, we believed that co-sputtered Cu/Ti is a promising candidate for 3D integration bonding medium.[7] Therefore, in this thesis, we study in detail on the characteristics and features of co-sputtered Cu/Ti as bonding interconnect in 3D integration.

1-4 Organization of The Thesis

In chapter 1, we give brief introduction to 3D integration, and especially 3D bonding technologies.

In chapter 2, we introduce the experimental instrument we use in this thesis.

Chapter 3 is to explain the characteristics of co-sputtered Cu/Ti as bonding material under different bonding temperature and bonding ambient. The evaluation is carried out on both chip level and wafer level, and the result is explained through TEM images, EDX analysis, Auger depth profile, SAT images, and etc….

In chapter 4, we discuss the reliability of co-sputtered Cu/Ti as bonded interconnect. The electrical property of the proposed structure is investigated under varies tests, including, temperature cycling test, humidity test, and current stressing tests. The result of each tests is compared to direct Cu-Cu bonding under the same conditions.

In chapter 5, we discuss about the future work that could be done to the proposed structure, and an outlook for 3D integration.

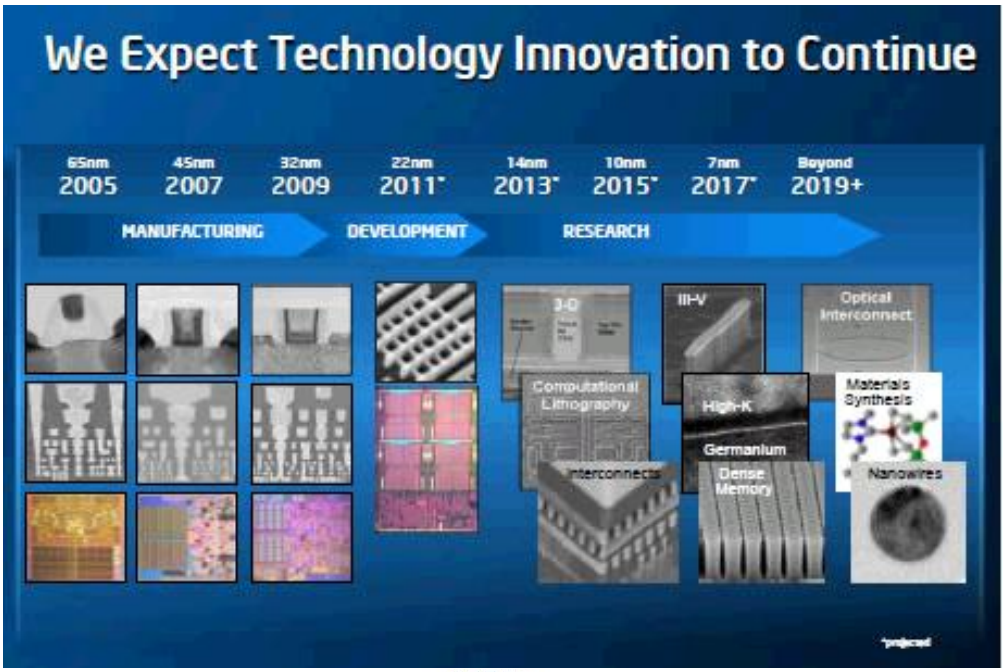


Fig 1-1 Intel roadmap for future semiconductor development

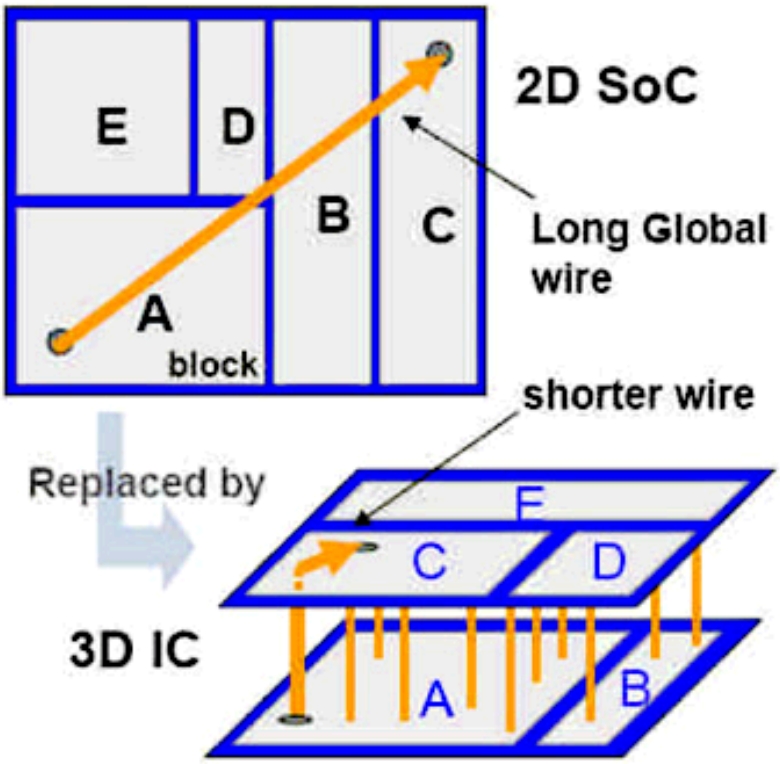
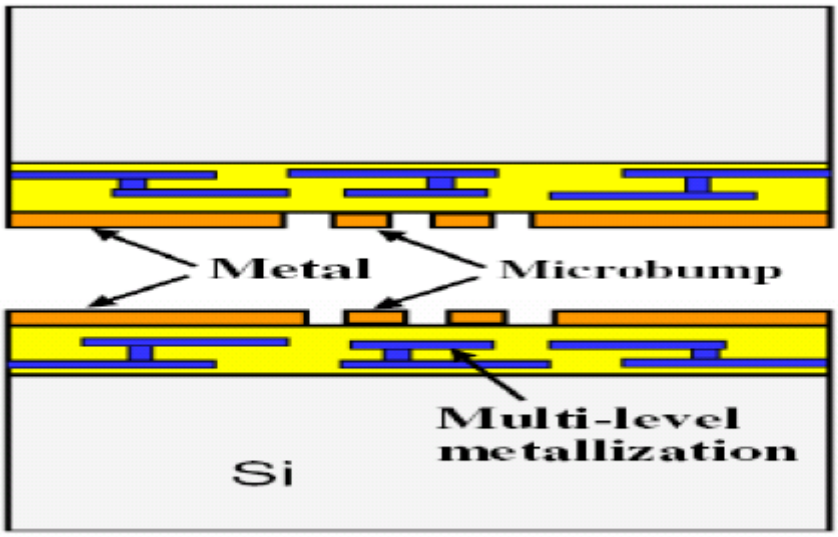


Fig 1-2 Schematic of 3D integration

Fig. 1-3 Heterogeneous Integration by 3D integration



(TOHOKU University)

Fig. 1-4 Schematic of metal bonding in 3D integration

Category	Detail Terms
Stacking Approach	A. Die-to-Die (D2D) B. Die-to-Wafer(D2W) C. Wafer-to-Wafer (W2W)
Substrate Selection	A. Bulk(Si, Ge, GaAs…..) B. SOI
Bonding Medium	A. Metal-to-Metal B. Oxide-to-Oxide C. Polymer-to-Polymer
Stacking Direction	A. Face-to-Face B. Face-to-Back
Fabrication of TSV	A. Via-First B. Via-Last

Table 1-1 Category of different 3DIC fabrication

Chapter 2
Experimental Instruments

2-1 Introduction

In this chapter we introduce the different instruments we used in this thesis. The instruments are categorized into two parts, the first parts is process instruments used for the preparation of the co-sputtered Cu/Ti bonding structure, and the second part is material analysis instruments used to analyze the bonding structure. All of the work is carried out in Nano Facility Center of National Chiao Tung University, MA-Tek, and Nano Device Laboratories. The condition of the instrument described in the thesis is based on the instruments provided in these places.

2-2 Process Instrument

2-2-1 Flip Chip Bonder

Fineplacer Pico Ma is the flip chip bonder used for all chip bonding in this thesis. This bonder provides the flexibility of manual control on bonding temperature, bonding time, and bonding force. Alignment methods for bonding instrument can be categorize into six types: 1) Wafer

back side alignment 2) Smart View method 3)Inter-substrate microscope 4) Infrared transmission microscope 5) Transparent wafer and optical microscope 6)Through-wafer holes and optical microscope. A detailed illustration for each type of alignment method is shown in Fig. 2-1 and the picture and schematic of the bonder are in Fig. 2-2 and 2-3. The alignment method of this bonder is type 3 inter-substrate microscopes, with two set of microscopes capturing the image of top and bottom bonding samples. By overlapping the two images, an alignment is made.

The spec of the bonder is as following: (according to the manual)

- ✧ Placement accuracy 5 µm
- ✧ Components from 0.125 mm x 0.125 mm to 100 mm x 100 mm
- ✧ Working area up to 450 mm x 234 mm
- ✧ Supports wafer/substrate sizes* up to 8"
- ✧ Supports bonding forces up to 100 N
- ✧ Can be configured as a hot air rework system
- ✧ Manual and semi-automatic configurations

2-2-2 I-line Stepper

The stepper used in this thesis is ASML pas 5500/100 i-line stepper.

Stepper is an important instrument used in lithography to pattern the wafer with circuit design. It acts as projector that contains lens to reduce the size of pattern on the mask and transform onto the sample. With photoresistance coated on wafer surface prior to projection, and the light passes through the mask and lens inside the stepper, a miniature image on the mask can be developed on the sample.

The spec of the stepper is as following: (citied from NFC website)

Stepper Applications:

- 4" Silicon wafers stock
- 6" Silicon wafers stock
- Customer supplied wafers can also be written

Stepper Specifications:

- 5 x 1 reduction
- Minimum resolution 400 nm
- Up to 6" wafers
- Quartz halogen lamp
- 1" by 1" steps

2-2-3 Sputter

Ion Tech Microvac 450CB was used for depositing all metal materials. The sputtering system is composed of the following: (1) Sputtering chamber (2) vacuum pumps, consisting of one cryo pump and mechanical pump (3) DC power (4) 4-inch magnetron gun (5) gas flow meter (6) pressure gauges (7) film thickness monitor. The 4-inch or 6-inch Si substrates are placed in the spin holder driven by a motor. The targets (metals such as Cu, Ti, Fe, etc.) are 4-inch. The DC source can provide up to 200 W powers. Normally the base pressure is around 3.0×10^{-6} torr and the working pressure is around 7.6 mtorr. The flow rate of Ar is around 24 sccm. The sputtering DC source is kept at 150W for our experiment.

Its basic principle is physical vapor deposition. PVD is driven by momentum exchange between the ions and atoms in the materials, due to collisions. The incident ions set off collision cascades in the target. When such cascades recoil and reach the target surface with energy above the surface binding energy, an atom can be ejected.

2-2-4 Wafer Bonder

We use EVG520IS as our wafer bonder in this thesis. The EVG520IS has the feature of symmetric rapid heating and cooling , and with independent top and bottom side heater, high pressure bonding capability and material and process flexibility as on manual systems contribute to the success of all wafer bonding processes.

Features

✧ Fully-automated processing with manual loading and unloading including external cooling station

✧ Single or double chamber automated system

✧ Fully automated bond process execution and bond cover movements

✧ Multi-stack bonding options

✧ Integrated cooling station for high throughput

✧ Options:

- Turbo molecular pump

- High vacuum capability

- Programmable mass flow controller

Technical data

✧ Heater size = Max. wafer diameter: 150mm or 200mm

- ✧ Min. wafer diameter: 150mm heater: single chips; 200mm heater: 100mm
- ✧ Bond chuck system / Alignment system:

  150 mm heater: EVG620, EVG6200, IQ Aligner, SmartView

  200mm heater: EVG6200, IQ Aligner, SmartView
- ✧ Max. contact force: 3.5kN, 7kN, 10 kN, 20 kN, 40 kN, 60 kN
- ✧ Max. temperature: 550℃ (650℃ optional)
- ✧ Vacuum: 1E-3 mbar (standard), 1 E-5 (optional), vacuum controller and process gas lines optional
- ✧ Power supply for anodic bonding: 0-2.000V / 50mA
- ✧ Loading chamber: manual
- ✧ Process (recipe) compatible with GEMINI
- ✧ Max. number of bond chambers: 2
- ✧ Customer / application: R&D, pilot-line + manufacturing

2-2-5 Furnace

NDL T17 backend vacuumed annealing furnace is used in this thesis**.** The annealing process is carried out in a high temperature and high vacuumed chamber. Chamber temperature can reach 600 ˚C and chamber

pressure can be lower than 10^{-6} Torr. Due to the high cleanness environment, the metal sample after annealing will not interact with atmosphere ambient and result in any metal oxidation. In addition, nitrogen and oxygen can be injected into the chamber during annealing.

2-3 Material Analysis Instrument

2-3-1 Auger Electron Spectrometer

Auger electron spectrometer with depth profile analysis is used in this thesis for characterizing the changes of metal layer after annealing in different conditions. The result of Auger electron spectrometer is based on the detection of energetic electrons emitted from an excited atom after a series of internal relaxation events. With the different energetic electron peaks, the spectrometer can then decide the combination or portion of each atom/material detected. An illustration is shown in Fig. 2-4. However, the depth profile can only give a relative depth but not an absolute one, for its etching time is strongly dependent on the substrate material.

2-3-2 Scanning Electron Microscopy

Scanning electron microscopy (SEM) depicts the surface topology, the cross section image, and different material region based on detection of secondary electrons. Hitachi S-4700 has a resolution of 1.5 nm operated at 15 kV. The accelerated electron beam, emitted from a cold-cathode electron gun with the extract voltage in the range from 0.5 kV to 30 kV, collides with DUT, and the secondary electrons originated within a few nanometers from the surface of the DTU are detected and rendered into a bright SEM image, which is as shown in Fig 2-5.

2-3-3 Focused Ion Beam

Focused ion beam (FIB), is a technique used particularly in the semiconductor and materials science fields for site-specific analysis, deposition, and ablation of materials. FIB systems have been produced commercially for approximately twenty years, primarily for large semiconductor manufacturers. Its setup is a scientific instrument that resembles SEM. However, while SEM uses a focused beam of electrons to image the sample in the chamber, FIB setup instead uses a focused beam of ions. It can also be incorporated in a system with both electron and ion beam columns, allowing the same feature to be investigated using

either of the beams. It should not be confused with using a beam of focused ions for direct write lithography, where the material is modified by different mechanisms.

FIB systems use a finely focused beam of ions (ex. Ga) that can be operated at low beam currents for imaging or high beam currents for site specific sputtering or milling. Figure 2-6 shows the gallium primary ion beam hits the sample surface and sputters a small amount of material, which leaves the surface as either secondary ions or neutral atoms. The primary beam also produces secondary electrons. As the primary beam rosters on the sample surface, the signal from the sputtered ions or secondary electrons is collected to form an image. At low primary beam currents, very little material is sputtered and modern FIB systems can easily achieve 5 nm imaging resolution. At higher primary currents, a great deal of material can be removed by sputtering, allowing precision milling of the specimen down to a sub micrometer scale. If the sample is non-conductive, a low energy electron flood gun can be used to provide charge neutralization. In this manner, by imaging with positive secondary ions using the positive primary ion beam, even highly insulating samples may be imaged and milled without a conducting surface coating, as

would be required in a SEM.

At lower beam currents, FIB imaging resolution begins to rival the more familiar scanning electron microscope (SEM) in terms of imaging topography, however the FIB's two imaging modes, using secondary electrons and secondary ions, both produced by the primary ion beam, offer many advantages over SEM.

FIB secondary electron images show intense grain orientation contrast. As a result, grain morphology can be readily imaged without resorting to chemical etching. Grain boundary contrast can also be enhanced through careful selection of imaging parameters. FIB secondary ion images also reveal chemical differences, and are especially useful in corrosion studies, as secondary ion yields of metals can increase by three orders of magnitude in the presence of oxygen, clearly revealing the presence of corrosion

2-3-4 Transmission Electron Microscopy:

The thickness, the interface layer, and the specific local region of the resistive switching device are investigated by transmission electron microscopy (TEM, JEOL JEM-2100F). Accelerated electron beam from

electron gun are focused on the DUT by the condenser lenses, and the DUT, here, is necessary to be sufficiently thin and transparent enough for incident electrons to transmit. The transmitted and forward scattered electrons form a diffraction pattern in the back focus plane and a magnified bright image in the main screen. Figure 2-7 is the schematic illustration of the TEM. Moreover, the DUT for TEM analyses is prepared by the focus ion beam (FIB, FEI Nova 200) with resolution of 7 nm.

2-3-5 Scanning Acoustic Tomography

In this thesis, we use scanning acoustic tomography (SAT) to evaluate the bonding quality of the bonded sample. Based on the color contrast of the SAT result, we could decide the percentage of the well bonded area and the region that has better bonding quality. Scanning acoustic tomography is a failure analysis technique for defects and de-bonded area. By sending a sound wave through the sample, and detect the interaction of the sound wave and the sample, it can distinguish the difference inside without causing any damages. A pulse echo or through transmission inspection is often used for detecting de-bonds or

delamination. A pulse echo detect the wave reflected by the sample while the through transmission inspection detects the wave that penetrate through the sample. The ultrasonic wave frequency used ranges from 5 to 150 MHz. A schematic of SAT is given in Fig.2-8.

2-4 Electrical Analysis

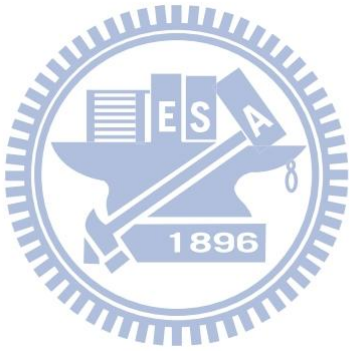
2-4-1 Four-Point Probe

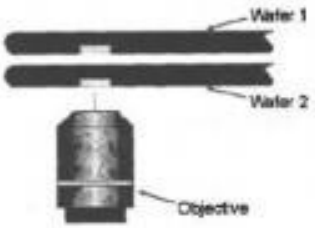
Four-point probe is used to measure the sheet resistance changes at the bonding interface after different bonding conditions. The setup of four-point probe is quite simple, a high impedance current source is applied between the outer two probes, and then by measuring the voltage difference in between the inner two probes, the sheet resistance can be calculated. A schematic of four-point probes is shown in Fig. 2-9.

2-4-2 Precision Semiconductor Analyzer

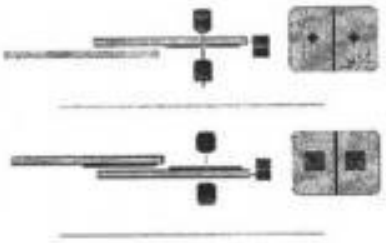
Agilent 4156C precision semiconductor analyzer is used to measure the electrical properties of the bonded structure. The 4156C provides highly accurate laboratory bench top parameter analyzers for advanced device characterization. The superior low-current and low-voltage

resolution and built-in quasi-static CV measurement capability of the 4156C provide a firm foundation for future expansion with other measurement instruments. A picture of 4156C is shown in Fig. 2-10.

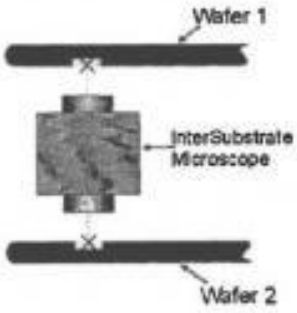




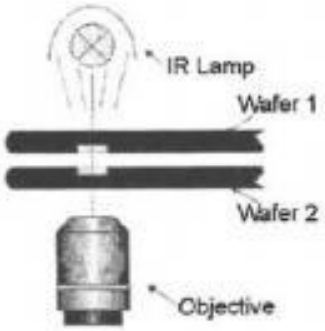
(a) Wafer back-side alignment



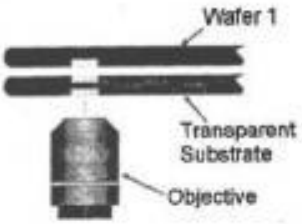
(b) SmartView® method



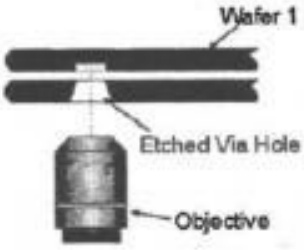
(c) Inter-substrate microscope



(d) Infrared transmission microscopy



(e) Transparent wafer and optical microscope



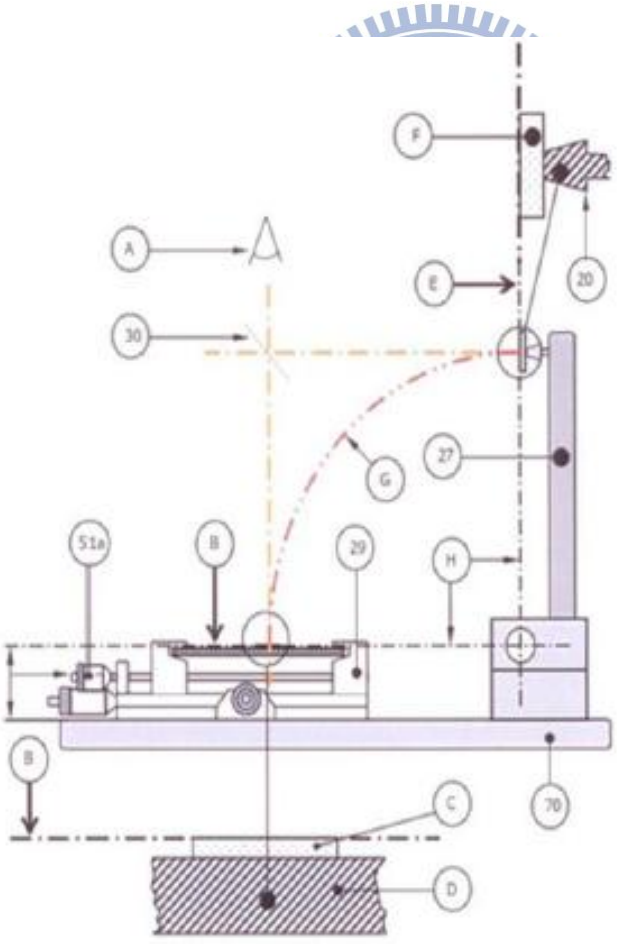
(f) Through-wafer holes and optical microscope

(AP review Adhesive wafer bonding)

Fig. 2-1 Illustration of different alignment methods

(Fine Tech)

Fig 2-2 Chip-level bonding instrument



A Observation Point

B Working Level

C Substrate

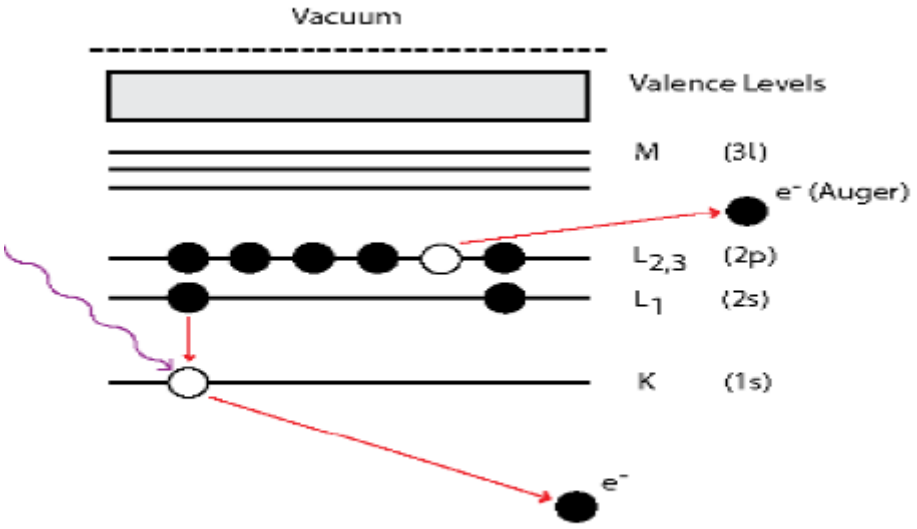
D Surface of Heating

E Upper Arm Position

F Top Glass Scale

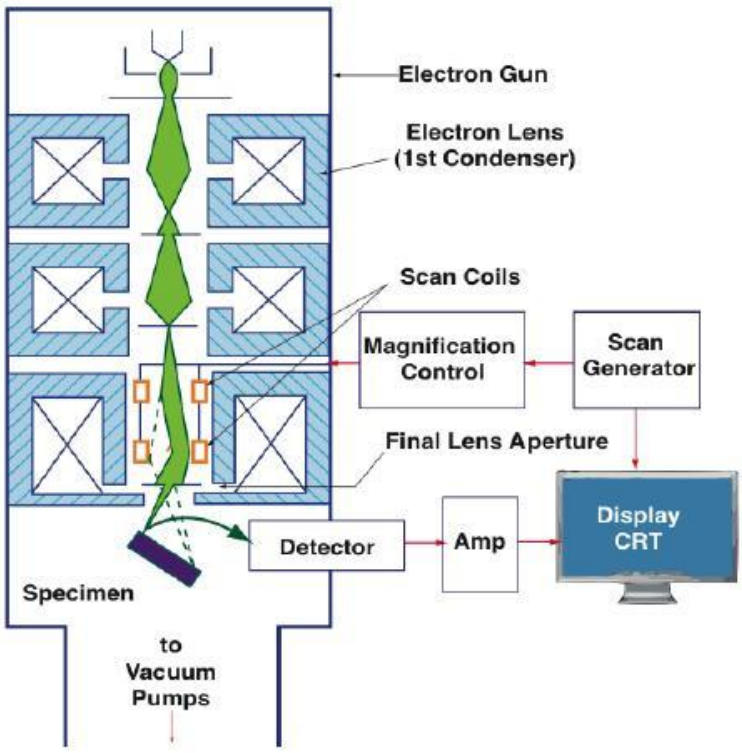
(FINETECH)

Fig. 2-3 Schematics of Fineplacer Pico MA



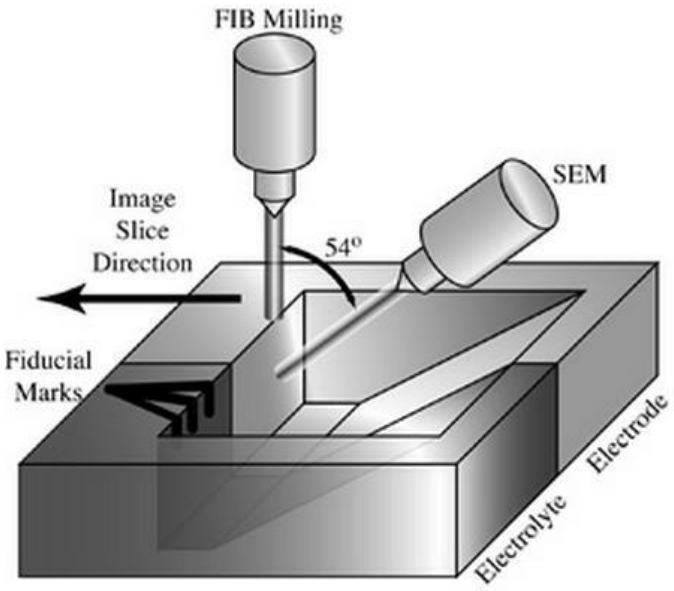
(The University of Warwick, Department of Physics)

Fig. 2-4 Explanation of Auger electron



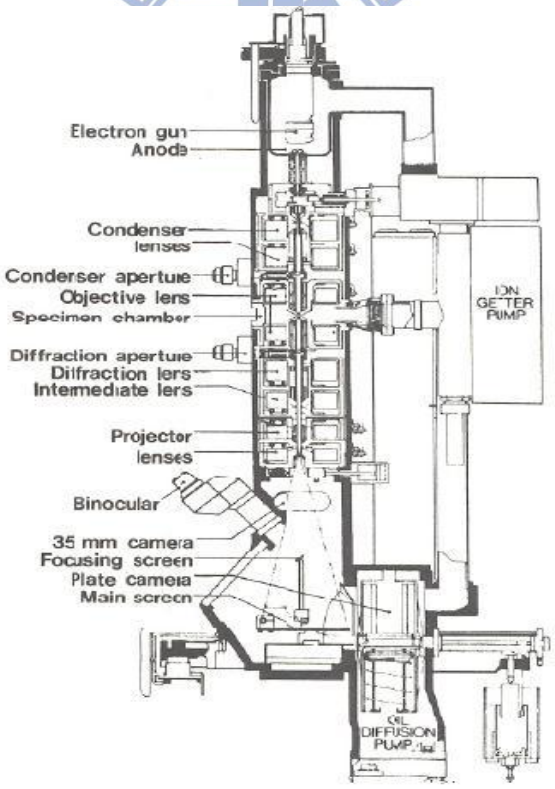
(The University of California Riverside)

Fig. 2-5 Schematic of SEM



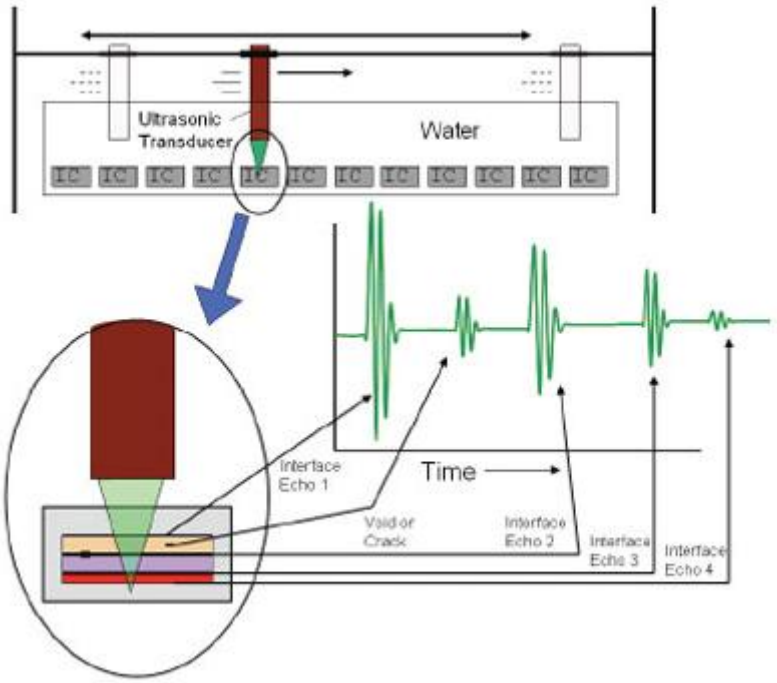
(Imperial college, London)

Fig. 2-6 Schematic of FIB



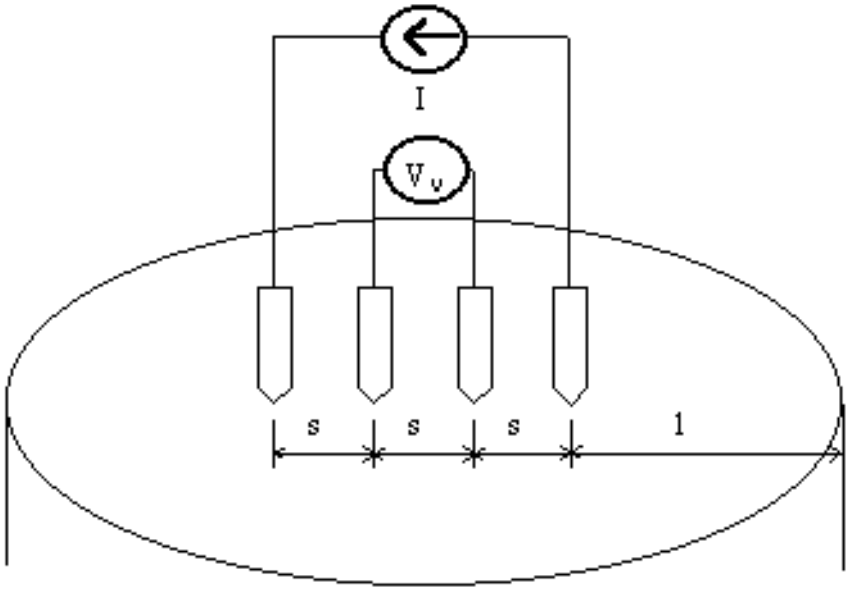
(The University of California Riverside)

Fig. 2-7 Schematic of TEM



(Evaluation Engineering)

Fig. 2-8 Illustration of SAT



(UIUC)

Fig. 2-9 Schematic of four-point probe

Fig. 2-10 Picture of Agilent 4156C

Chapter 3
Characteristic of Co-sputtered Cu/Ti Bonded Interconnect

3-1 Introduction

For 3D integration, various types of bonding approaches have been proposed, including wafer-to-wafer, die-to-wafer and die-to-die bonding. Each type subjects to different throughput and yield. In addition, numerous bonding medium has been evaluated. The most prominent bonding medium can be categorized as oxide-to-oxide, adhesive-to adhesive, metal-to-metal, and hybrid bonding. Among all, metal-to-metal bonding is the mainstream for current bonding technology, due to its higher tolerance to surface cleanliness, better heat dissipation, and also serving as an additional metal layer.

Among all metal materials, copper is the preferred candidate for its outstanding electrical properties [8]. In 3D metal bonding technology, Cu as bonding material provides numerous advantages over other metal and eutectic bonding technology. In addition to the great electrical performance of Cu, high compatibility with semiconductor fabrication is

also a major merit for 3D integration. Moreover, Cu bonding avoids the formation of intermetallic compound (IMC) in many other metal alloy bonding, which in turns provides higher resistance toward electro-migration, mechanical forces, and thermal stressing [9].

Although Cu bonding has been widely studied [10-11], there is only a limitation research on co-sputtered Cu-based metals studied for bonding medium. The interdiffusion of co-sputtered metals leads to segregation of the co-sputtered metals at high temperature [12-13], which provides a good foundation for metal to metal bonding. In this chapter, co-sputtered copper and titanium as bonding materials are investigated. Due to the segregation of co-sputtered copper and titanium at thermal compression bonding condition, an automatically formed adhesion layer and copper to copper bonding structure is demonstrated. With the excellent bonding result, it is suggested that co-sputtered copper and titanium bonding is a promising approach for 3D bonding technology. The quality and morphology co-sputtered thin films and bonded bonding structure were analyzed through Auger, TEM, EDX analysis and SAT mappings.

3-2 Experimental

Standard RCA cleaning is applied to the wafer before 500nm TEOS deposition. Co-sputtered Cu/Ti samples were prepared by co-sputtering Cu and Ti simultaneously in a multi-target chamber at 150W for 90 minutes, under a working pressure of $7x10^{-3}$ Torr and with a base pressure of $1x10^{-6}$ Torr. The approximate sputtering rates for Cu and Ti are 0.6 Å /s and 0.1 Å /s respectively. However, when the prepared sample is exposed in atmosphere, a considerable amount of native copper oxide will be formed on the surface. According to previous studies [14], copper oxide on the bonding interface would greatly affected bonding quality and bonding strength. Therefore, prior to bonding, an acetic acid cleaning was applied to the sample to remove copper oxidation following the reactions: [15]

$$CuO + 2CH_3COOH \rightarrow Cu(CH_3COO)_2 + H_2O \quad (1)$$

$$Cu_2O + 4CH_3COOH \rightarrow 2Cu(CH_3COO)_2 + H_2O + H_2 \quad (2)$$

Two groups of sample are evaluated, one is bonded at wafer level and the other at chip level. Wafer level samples are bonded face-to-face at 350 °C for 60 min, with 10000N force, and in vacuum. Chip level samples are bonded face-to-face at 400 °C for 100 min, with 145 psi, and in atmosphere ambient.

3-3 Investigation on the bonding structure

3.3.1 Ideal Structure

Based on previous studies, we observed that when annealed at high temperature in nitrogen ambient, copper atoms tend to move toward the surface while titanium atoms tend to move toward the substrate. With this particular phenomenon, we purposed a bonding structure with co-sputtered Cu/Ti to form a self-adhesion layer with copper as the bonding medium. A schematic illustrating this bonding structure is shown in Fig. 3-1.

At first, Cu and Ti atoms are uniformly distributed throughout the layer. When bonding process starts, copper atoms start to move toward the bonding interface of the two layers, while Ti atoms diffuse toward the substrate side. As the heating process goes on, Cu atoms at the bonding interface start to diffuse and form into a continuous layer. The diffusion occurs at the bonding interface, where Cu atoms from the top and bottom samples diffuse to the other sample and coalesce into grains connecting the two layers. At last, a continuous Cu layer is formed and the interface is eliminated.

3.3.2 Electrical Evidence of Copper Bond

Sheet resistance measurement of different bonding time in Fig. 3-2 was conducted to verify the bonding mechanism of the proposed method. For Cu film of 3000 Å and Ti film of 500Å, the sheet resistance are 350mΩ/□ and 225Ω/□, respectively. Given the fact that the film is majorly composed of Cu, the starting sheet resistance of Cu/Ti film is 3Ω/□. The value of sheet resistance of Cu/Ti film gradually reduces from 3Ω/□ to below 1.5Ω/□ after 60 min of bonding. Due to the higher sheet resistance of Ti than the co-sputtered metal, we can thus conclude that the decrease of sheet resistance of Cu/Ti film implies that Ti atoms diffuse away and a Cu layer starts to form at the bonding interface.

3.3.3 Investigation of Co-sputtered Cu/Ti Bonding at Wafer Level

A SAT examination is made on the boned sample and is shown in Fig.3-3. The dark region is the well-bonded area, while the region with lighter color is partially bonded or not bonded at all. We take a well-bonded sample for its SEM image in Fig. 3-4. The total bonding thickness is about 859nm which is approximate the deposition thickness

of the co-sputtered metal, and no cracks or voids are presented in the structure. The TEM image and illustration sample are given in Fig. 3-5, with 500nm of SiO_2 on top of Si wafer and bonded with co-sputtered Cu/Ti. The initial bonding interface is nowhere to be seen in the TEM images in Fig 3-5 and Fig. 3-6. A continuous layer is observed throughout the sample at the bonding interface and no voids present in the structure, which implies the good bonding quality of the proposed method.

Line scan of the bonded sample in given in Fig. 3-7, and the broken line in Fig. 3-7 indicates the continuous layer (origin bonding interface) in between the top and bottom sample. Between the two broken line, copper signal is more significant, while Ti is less observed. It can be concluded that Cu is highly concentrated at the bonding interface, while Ti on the other hand, is much less detected at the interface and mostly observed outside the bonding region. EDX analysis given in Fig. 3-8 shows a similar result. Region A and C in Fig. 3-8 are near the substrate, and Region B is at the bonding interface. According to result, Ti is detected in region A and C, however, copper is 100% at region B and no Ti is detected. The analysis indicates a continuous copper layer is formed at the bonding interface, and Cu is the major bonding medium. However,

contradictory to our previous assumption, no self-adhesive layer is formed. The cause of this problem is believed to be related to the bonding temperature and will be further discussed in Chapter 3.4.

3.3.4 Investigation of Co-sputtered Cu/Ti Bonding at Chip Level

SEM images before and after bonding are shown in Fig. 3-9 and Fig.3-10. Before bonding, the thickness of the co-sputtered metal is 546nm. The total thickness after bonding is 1.103um close to twice the original thickness on one side of the sample. A 135nm continuous layer occurs at the original bonding interface, which is later proved as a Cu-bonded layer. TEM images and EDX analysis of a bonded sample are shown in Fig. 3-11 to Fig. 3-13. According to EDX analysis, Ti has a higher composition near the substrate (region 1 in Fig. 3-12). Cu composition, on the other hand, gradually increases toward the bonding interface. The accumulation of Ti atoms close to the substrate forms a self-adhesive layer during bonding, which not only improves adhesion of the bonding structure but also reduces fabrication complexity [16]. A copper-rich layer is formed between the two samples (region 4 in Fig.3-13) and eliminates the original bonding interface. The copper-rich layer at the bonding interface suggests that Cu is the major bonding

medium in this structure, and it could provide the good electrical properties that are expected for Cu interconnects.

Line scan of the bonded sample is shown in Fig. 3-14 and Fig. 3-15. It is clear that the composition at the boundary close to the substrate is very different from the composition in between. As we expected, a self-formed adhesion layer composed of Ti atoms is observed at the boundary, and copper is the dominant component in middle of the structure. However, a Cu peak is also presented near the substrate and is sandwiched between the adhesion layer and the substrate. The result indicates that the adhesion layer cannot prevent the diffusion of copper into the substrate. Therefore, a diffusion barrier is still required for this material.

3.3.5 Titanium Oxides as Passivation Layer of Cu/Ti Interconnects

According to previous studies, Ti oxide is formed on the surface of co-sputtered Cu/Ti after annealing in oxygen ambient.[17] With this interesting property, Ti oxide is expected to serve as a passivation layer for Cu interconnects to prevent corrosion and increase reliability. In 3D integration, the annealed surface expose to oxygen would be the sidewall

of interconnect during bonding, and if Ti oxide is formed as expected, the ideal structure would be as Fig.3-16.

To investigate the behavior of the co-sputtered metal, a patterned sample is annealed at 400°C , in oxygen ambient of 24 sccm, and for 20min. Region 2 and 9 in the TEM images of Fig. 3-17 refer to the surface and sidewall of the metal line, and is detected with a large amount of Ti and oxygen compared with other parts of the sample. Therefore, the results is consistent with our previous assumption, that Ti oxide is formed at the region where co-sputtered metal line is in contact with oxygen. In 3D structure, the area exposed to oxygen is not the surface of the sample but the sidewall of the bonded metal line, since the sample surface is tightly compressed with each other during bonding. In addition, the inner part of the metal line (region 3 to region 6, and region 8), has a lower Ti composition, but with a higher Cu composition, and oxygen signal at the inner part of the metal line is also greatly reduced. The reduction of oxygen signal indicates oxygen is mainly consumed by Ti, and Cu in the inner structure is mostly intact and remain highly conductive. Ti oxide is well known for its high resistance against corrosion, for its stable, highly adherent, continuous, and protective film. The distribution of metal

atoms in this particular experiment proves the existence of a passivation layer using co-sputter Cu/Ti as bonding interconnect.

Line scan of the bonded sample are provided in Fig.3-18. Line scan analysis is consistence with EDX result. Ti peak and O peak are observed at the surface, and Cu is found mostly in between Ti oxide and substrate. The large decrease of oxygen composition with Ti composition near surface is clearly observed in the line scan result. In addition, self–formed adhesive layer is also observed in Fig. 3-18. The second Ti peak is near the substrate, right above silicon dioxide. Unlike other part of the sample, Ti composition near substrate is much higher than Cu composition, and much higher than the average composition throughout the sample.

We also like to note that, the copper oxide at the surface of the annealed sample, is believed to be cause by native copper oxide and limitation on instrument, and is not related to the diffusion mechanism of co-sputtered Cu/Ti. Hence, for a well prepared sample, the surface copper oxide should not be presented.

3.4 Temperature Dependence of Diffusion for Co-sputtered Cu/Ti

In this section, we like to discuss the temperature dependence of

diffusion mechanism of co-sputtered Cu/Ti. A series of Auger analysis is conducted on co-sputtered Cu/Ti sample annealed in different ambient circumstances.

Auger analysis prior to annealing is shown in Fig. 3-19, and the composition of Cu and Ti is uniformly distributed in the sample. Fig. 3-20 and Fig. 3-21 are the Auger result of sample annealed on hot plate and furnace of 400℃ respectively. The results heated on heat plate and in furnace have a great discrepancy of surface oxide. Copper oxide is formed on hot plate heated circumstance, while Ti oxide is formed in the furnace annealed case. The difference of surface oxide is believed to be caused by the ramping rate of hot plate. As we know, hot plate takes a much longer time compare to furnace to reach a high temperature, as in our case 400 ℃. Before the reaching 400℃, the co-sputtered metal already starts to interact with oxygen. But due to the low temperature, interdiffusion of the co-sputtered metal is not fully activated, and thus Ti does not diffuse to the surface and interact with oxygen and is Cu instead. From the result, we concluded that Cu is more likely to diffuse inside the sample low temperature (below 400℃), while at high temperature Ti becomes more active. The bonding temperature in chapter 3.3.3 is 350℃

lower than 400°C, which could leads to less mobilized Ti atoms, and thus no self-formed adhesive layer is observed .

3.5 Summary

In this chapter, we discuss the bonding structure of co-sputtered Cu/Ti as 3D interconnect on both chip level and wafer level. We proved that the major bonding medium of co-sputtered Cu/Ti interconnect is copper and gave evidence to the self-formed adhesion Ti layer during bonding. The effect of different bonding temperature was also investigated. Moreover, an indication of TiO_2 passivation layer in 3D interconnect is also presented. With the above mentioned advantages, we believed that co-sputtered Cu/Ti is a suitable bonding material for 3D integration.

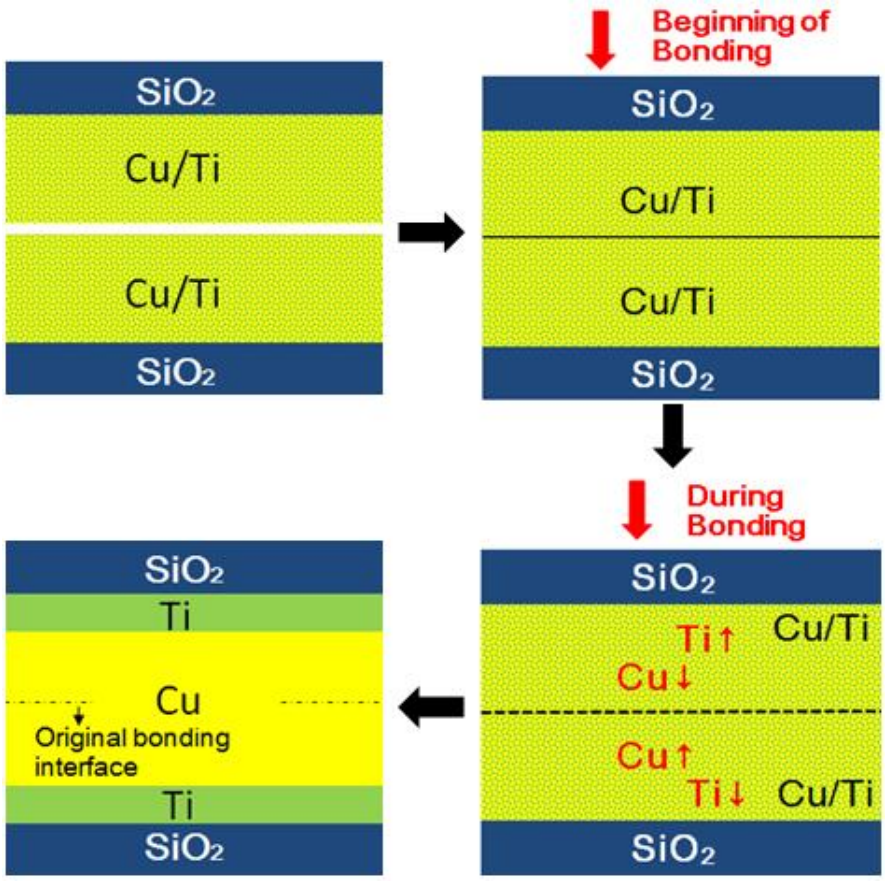


Fig. 3-1 Diffusion mechanism of co-sputtered Cu/Ti

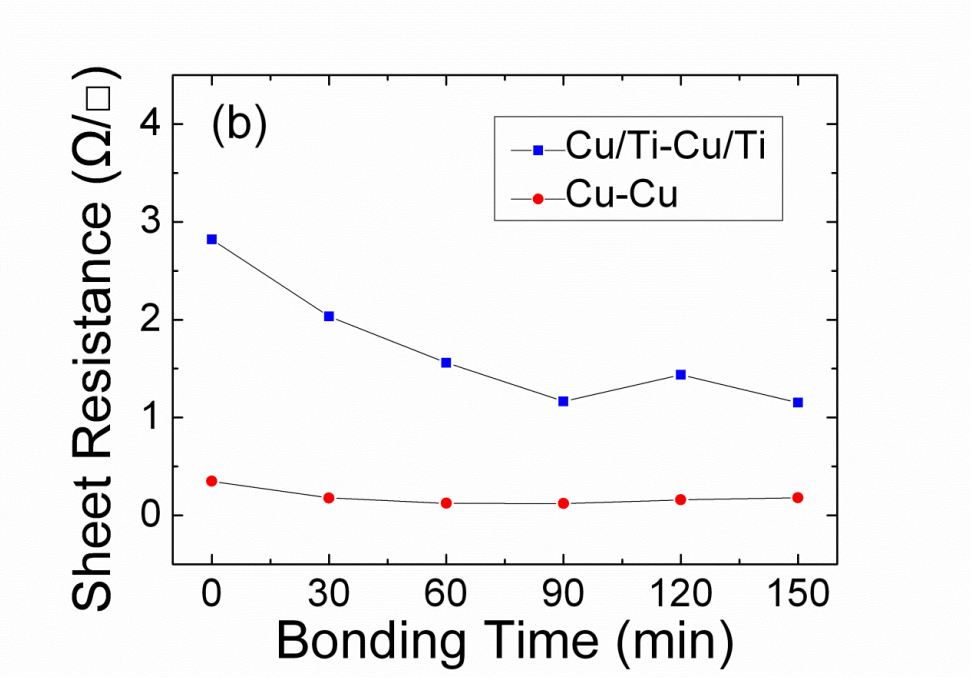


Fig. 3-2 Sheet resistance changes with different bonding time

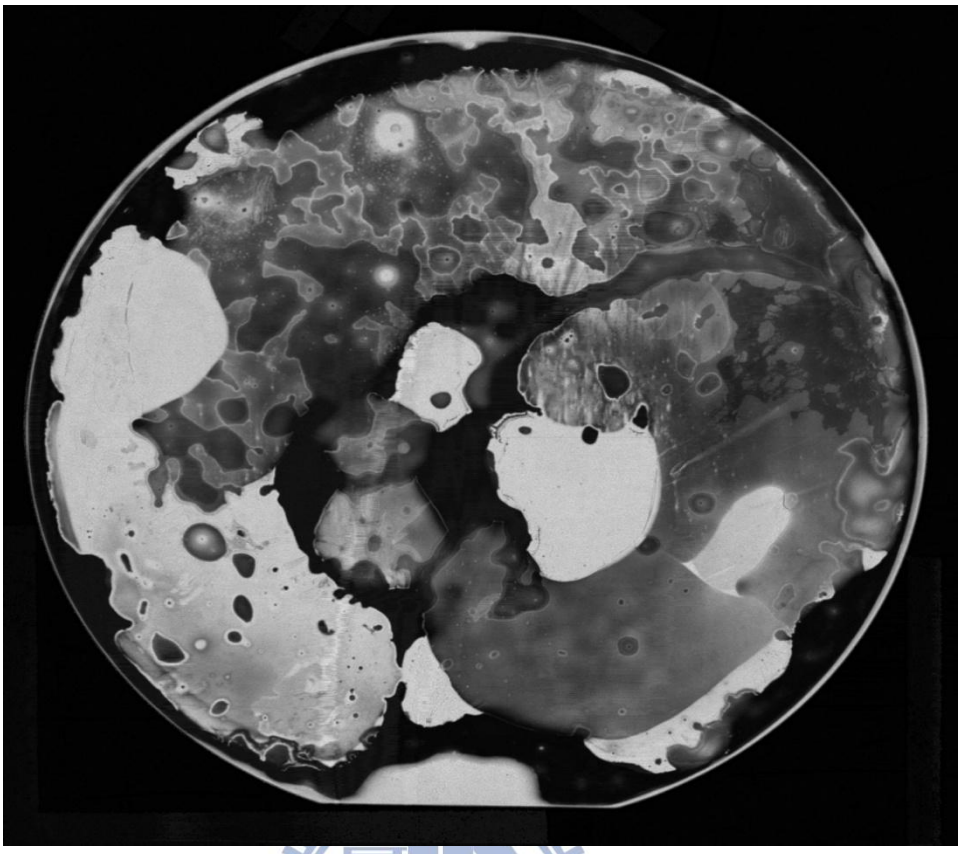


Fig. 3-3 SAT image of bonded sample at wafer level

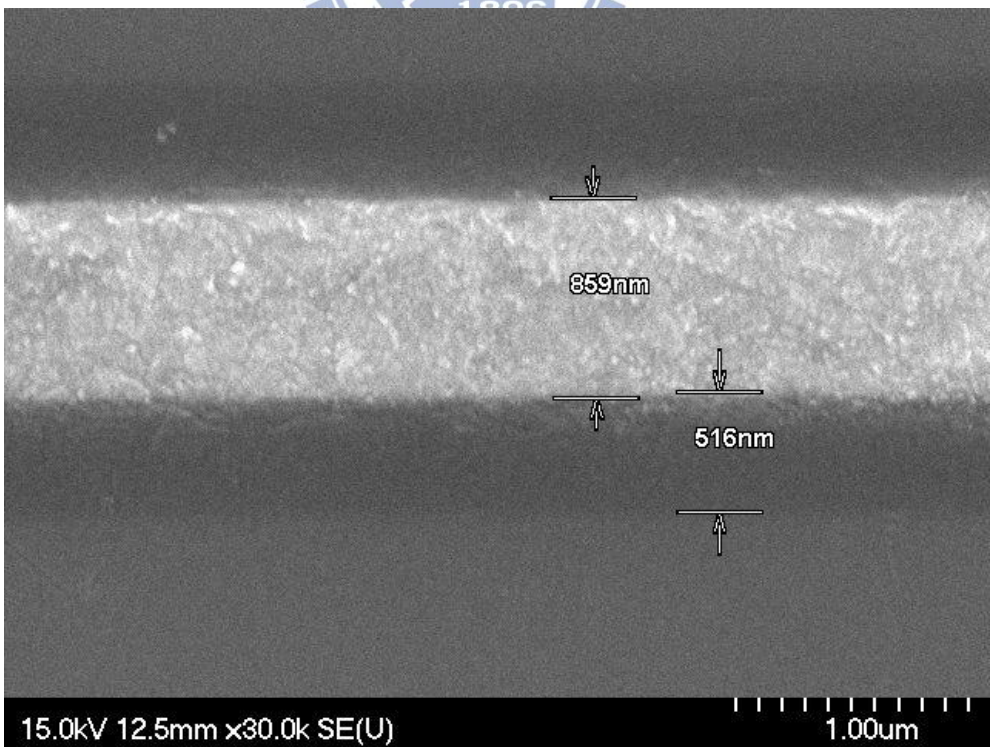


Fig. 3-4 SEM image of bonded co-sputtered Cu/Ti

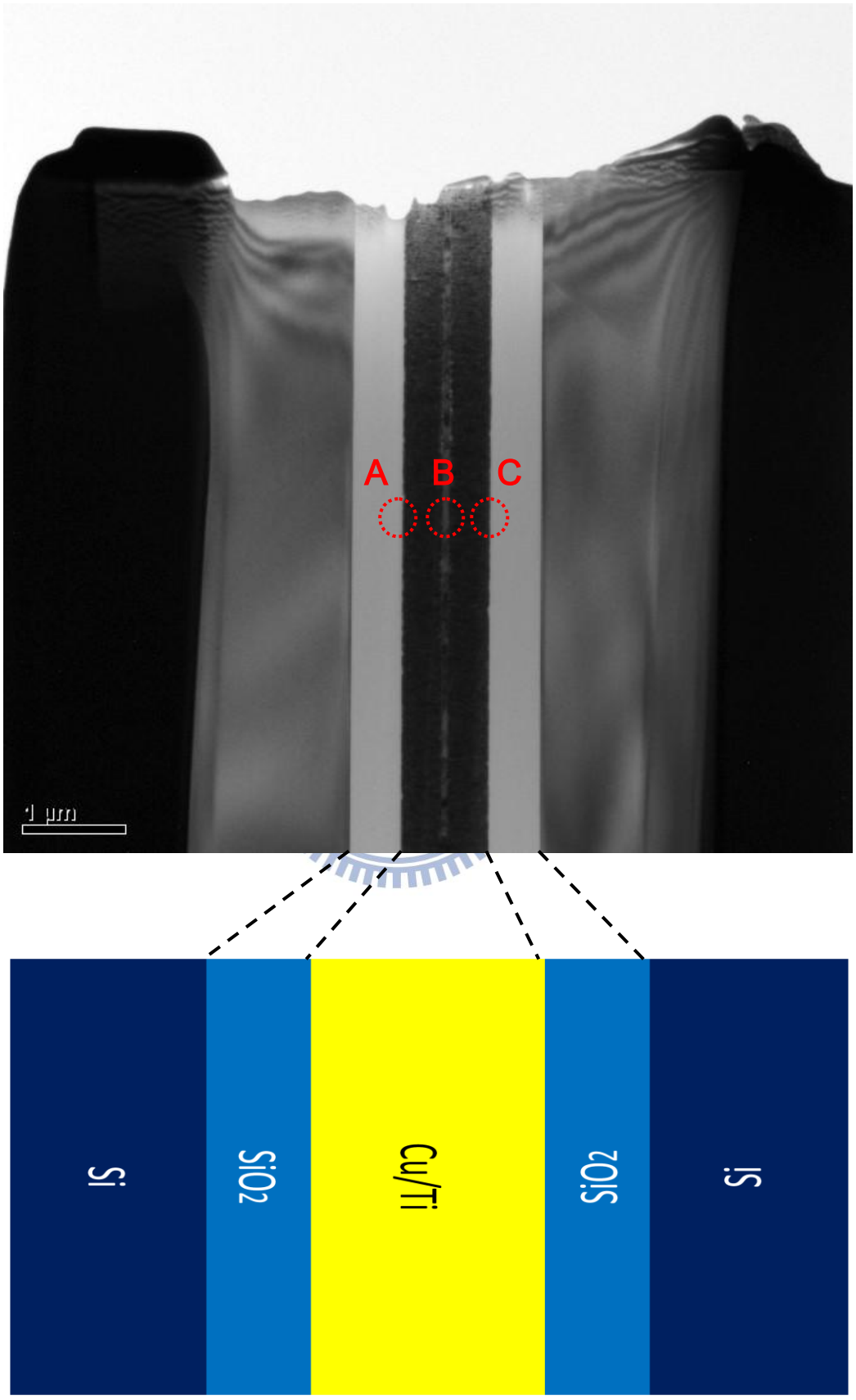


Fig. 3-5 TEM image and illustration of a bonded sample

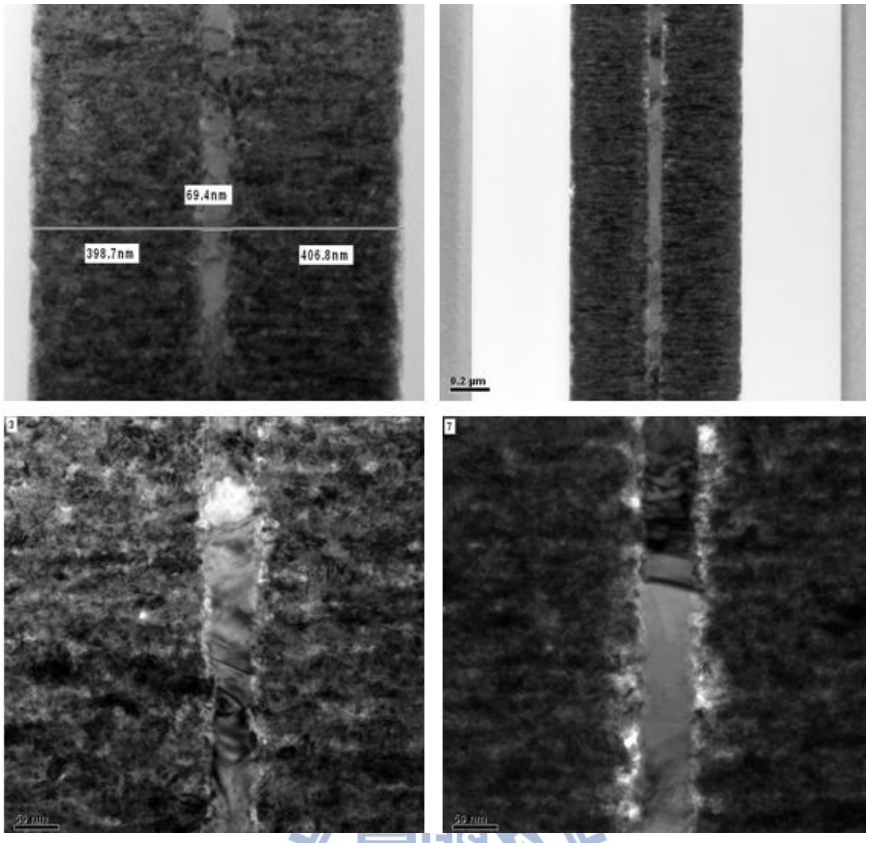


Fig. 3-6 TEM images focus at bonding interface

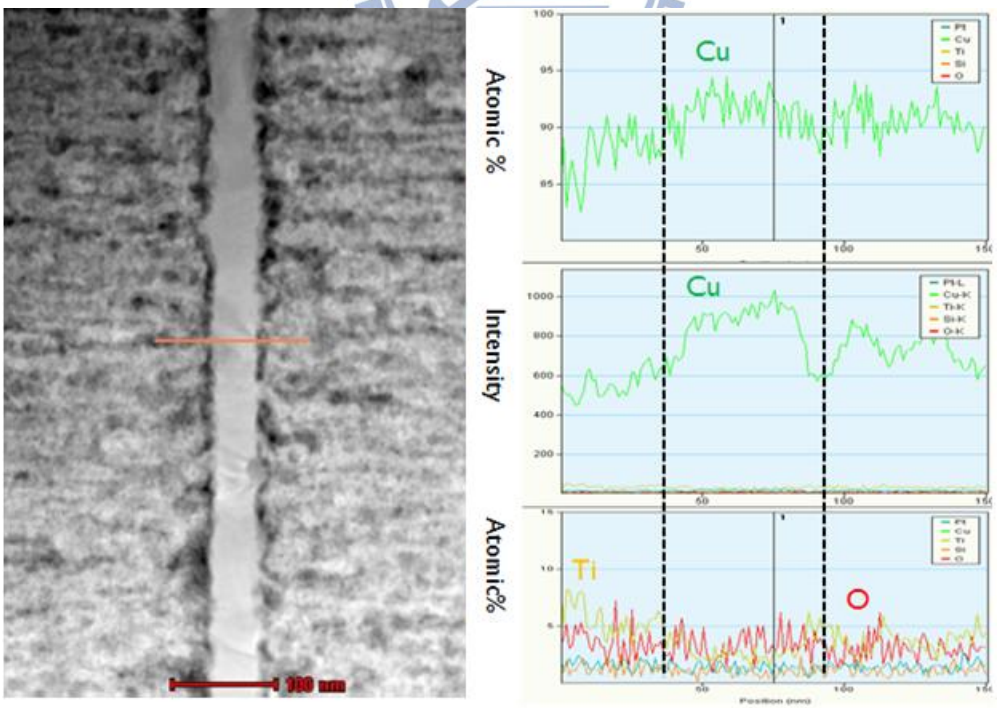


Fig. 3-7 Result of line scan at orange line on the left

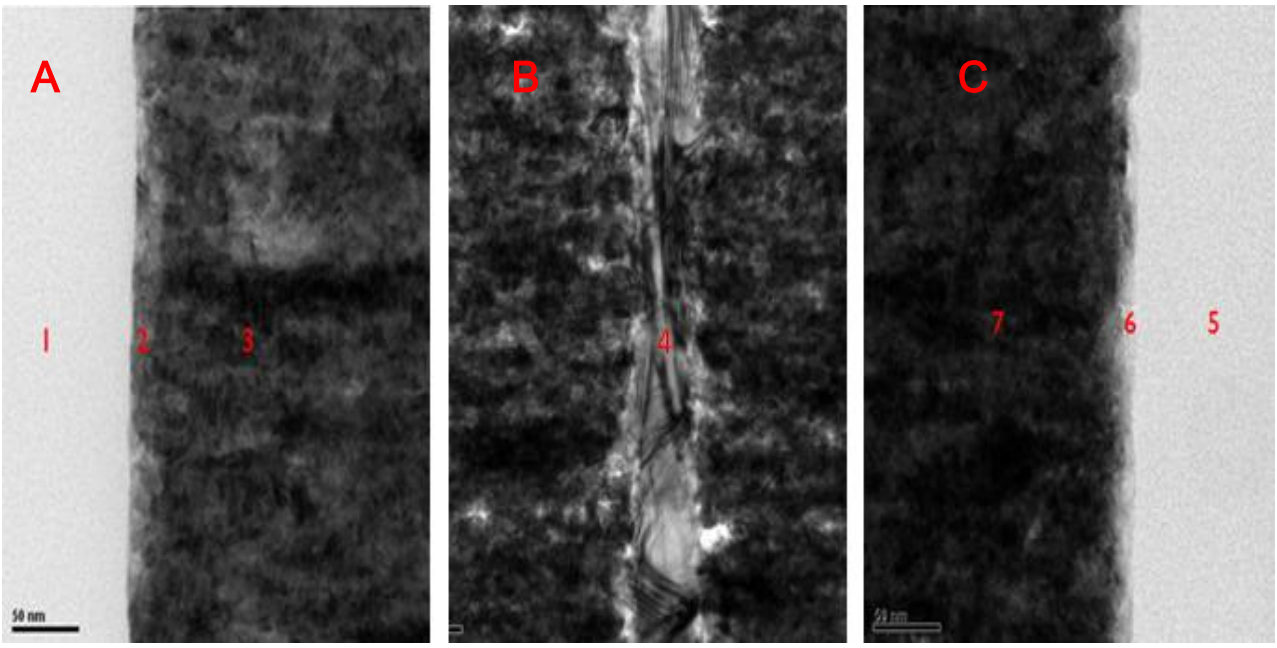


Fig. 3-8 TEM image of a wafer level bonded sample

	Cu (%)	Ti(%)	Si(%)	O(%)
1	0	0	30.5	60.5
2	49.5	6.1	5.8	38.6
3	69.6	10.4	0	20
4	100	0	0	0
5	0	0	29.1	70.9
6	44.8	7.8	3.2	44.2
7	64.2	10.7	0	25.2

Table 3-1 EDX analysis on region marked in fig. 3-8

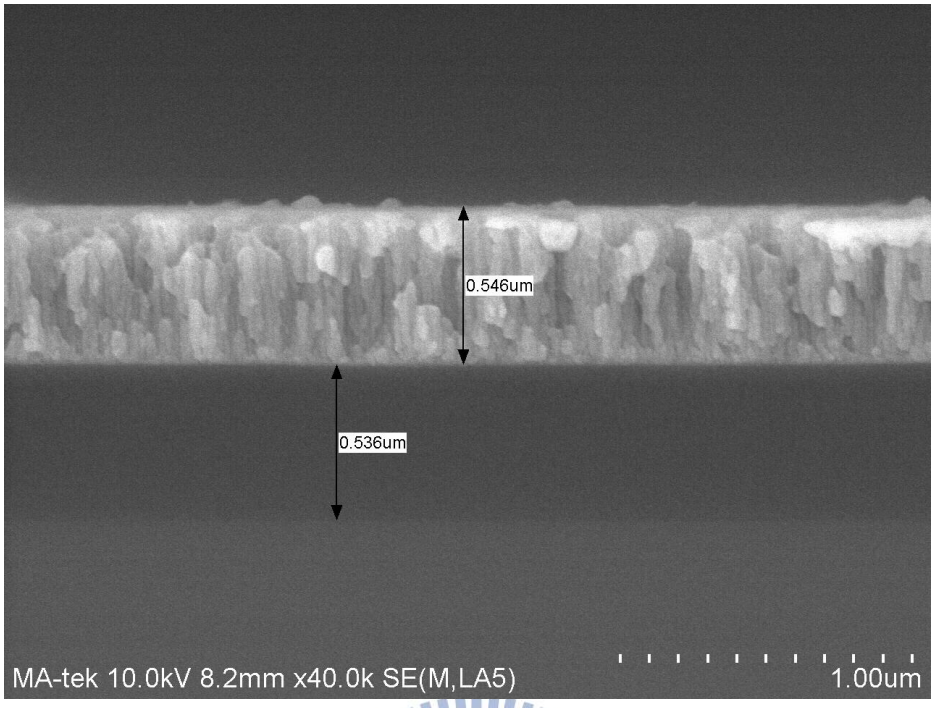


Fig. 3-9 SEM image of sample prior to bonding

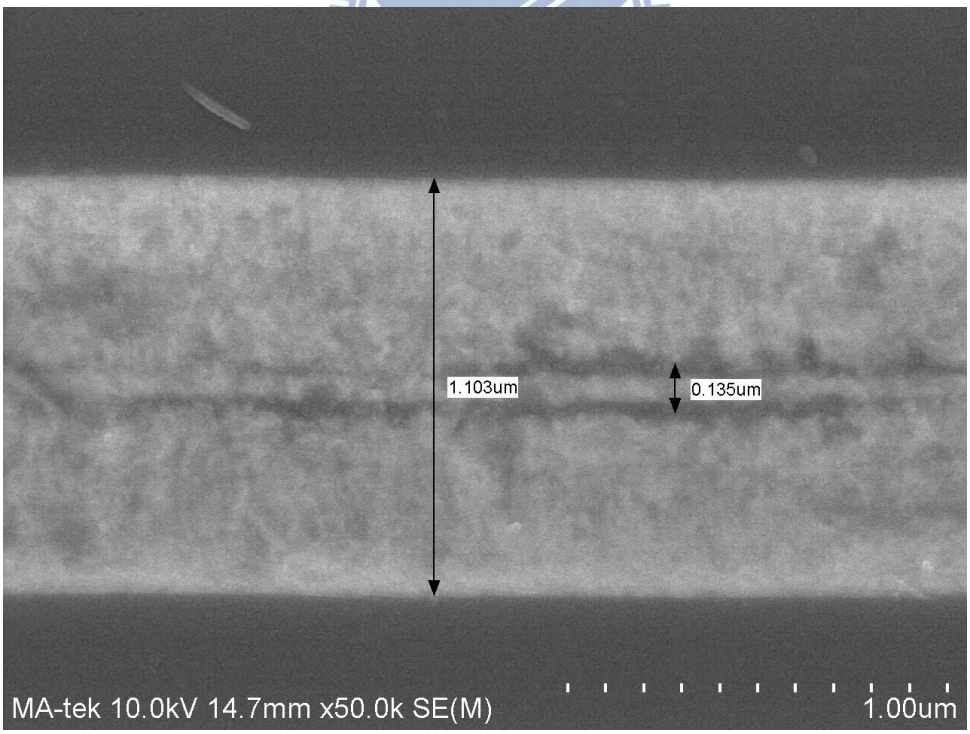


Fig. 3-10 SEM image of sample after bonding

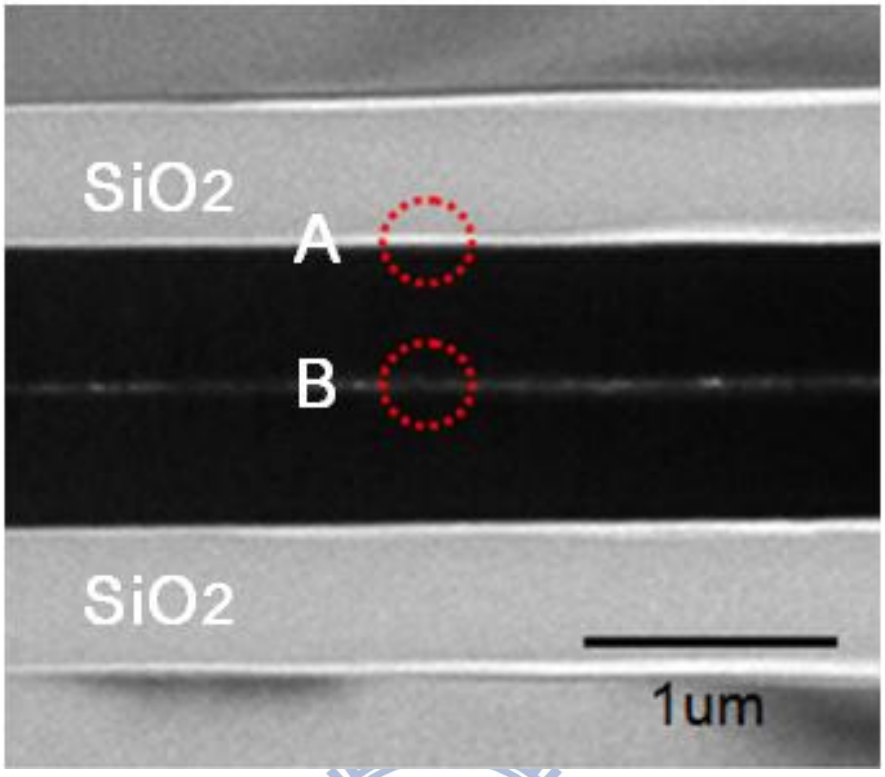


Fig. 3-11 TEM image of sample bonded at chip level

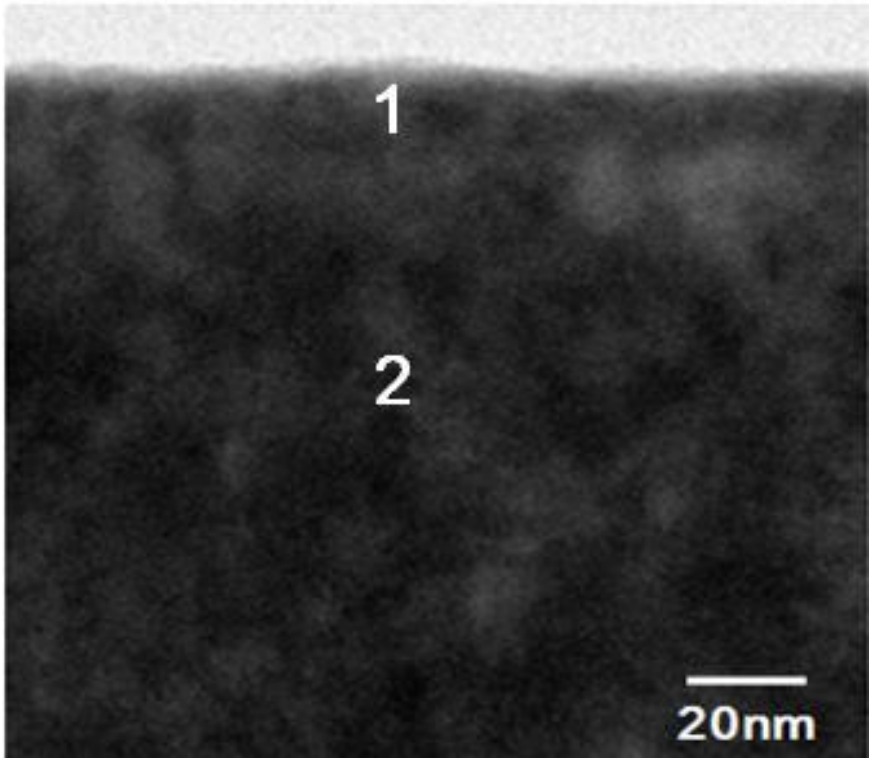


Fig. 3-12 Enlargement on region A in fig. 3-11

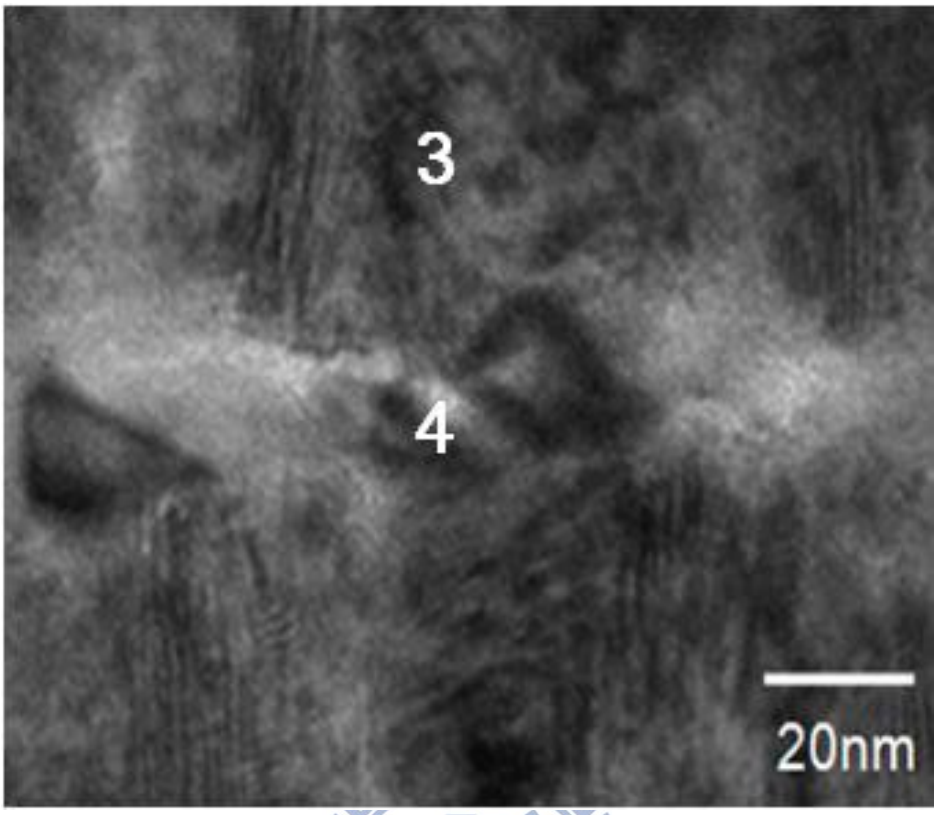
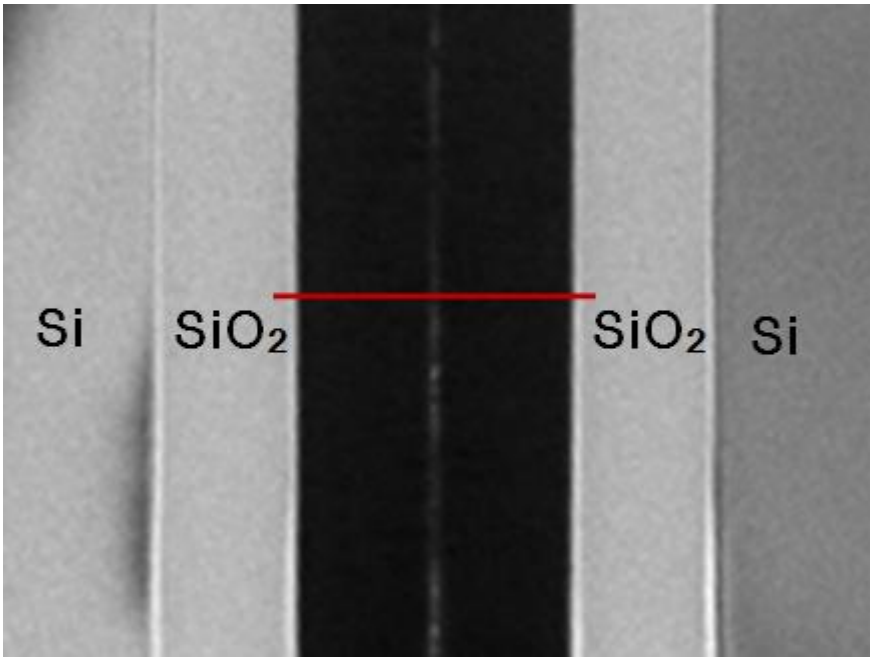


Fig. 3-13 Enlargement on region B in fig. 3-11

Spectrum	Ti (%)	Cu (%)
1	17.87	64.11
2	8.28	91.72
3	5.72	94.27
4	5.36	94.63

Table 3-2 EDX analysis on marked area in fig. 3-12 and 3-13



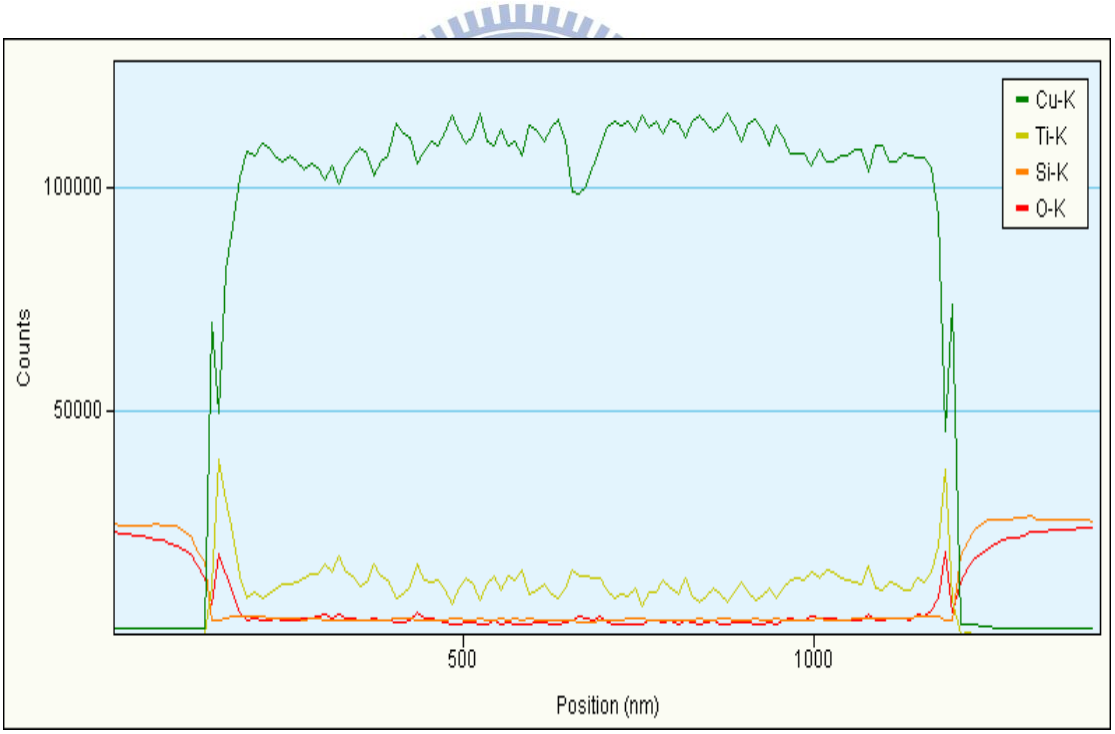
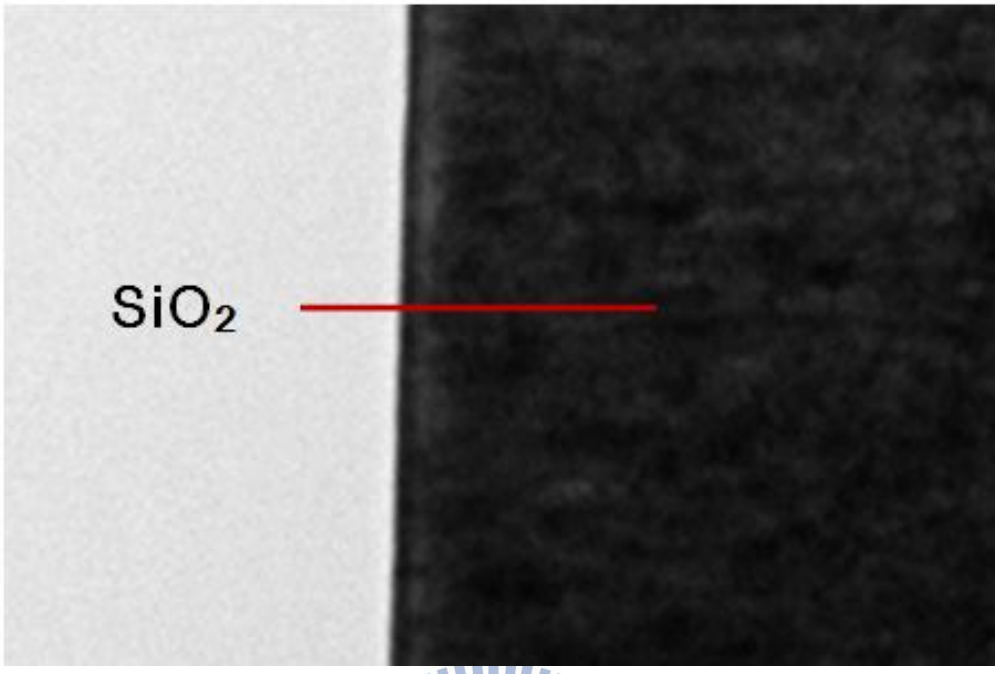


Fig. 3-14 Result of line scan at the red line on the top graph(near bonding interface)



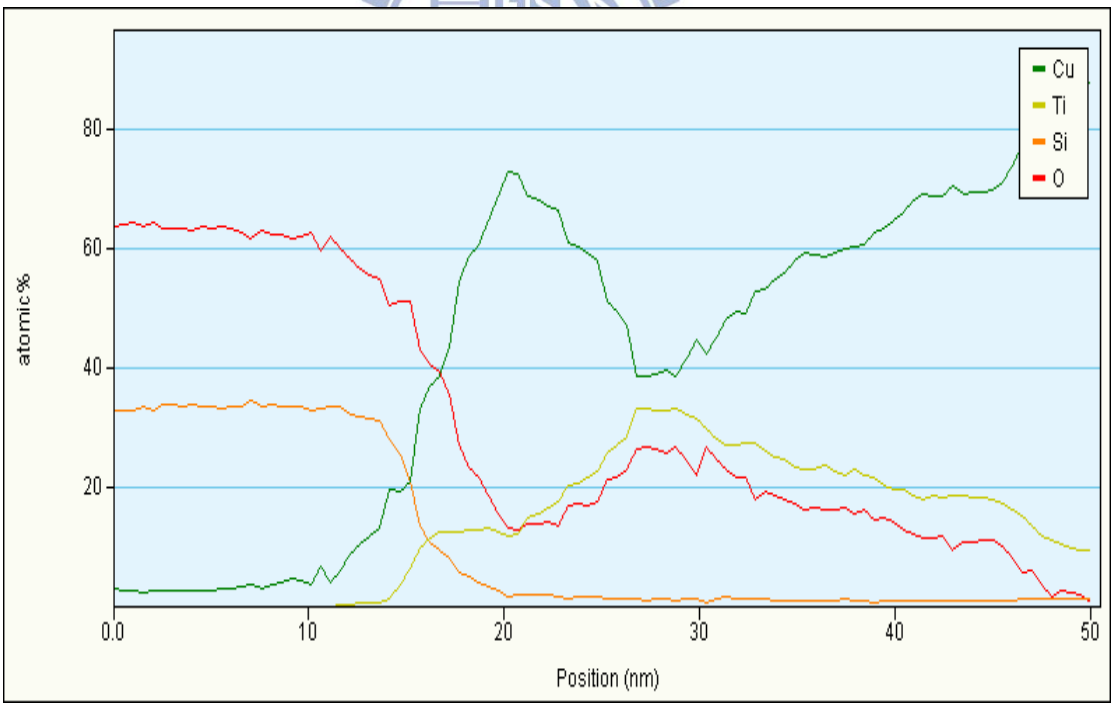


Fig. 3-15 Result of line scan at the red line on the top graph(near substrate)

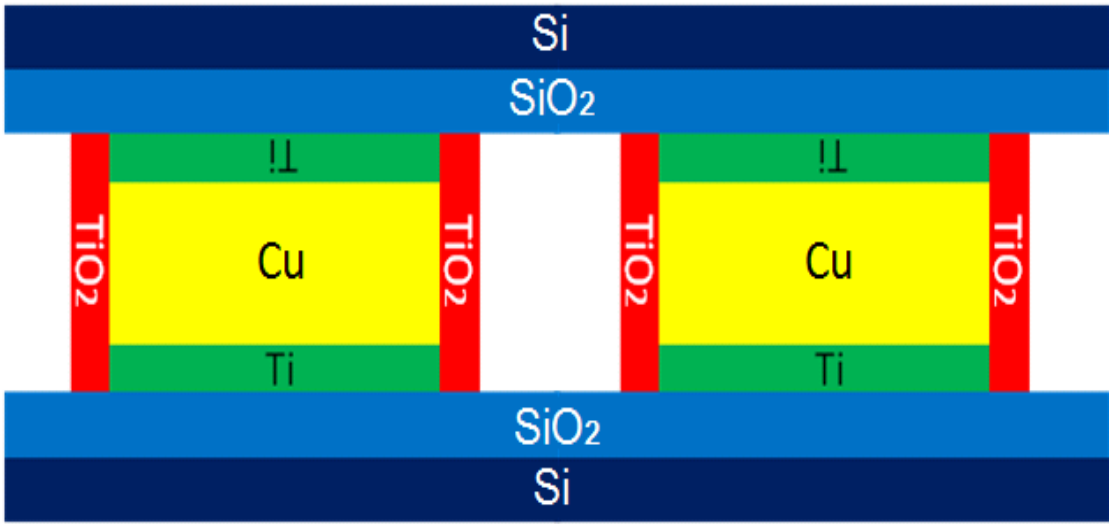


Fig. 3-16 Schematic of ideal co-sputtered interconnect

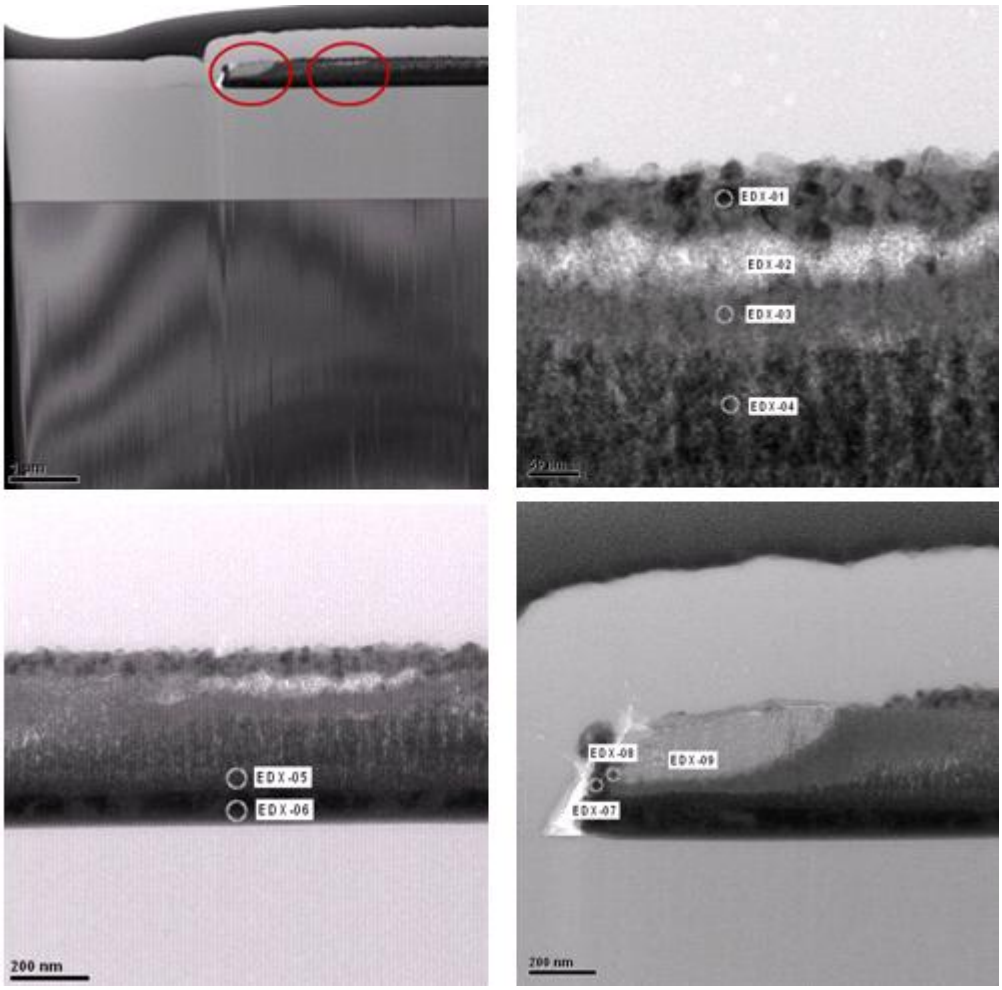


Fig.3-17 TEM of annealed co-sputtered Cu/Ti in oxygen ambient

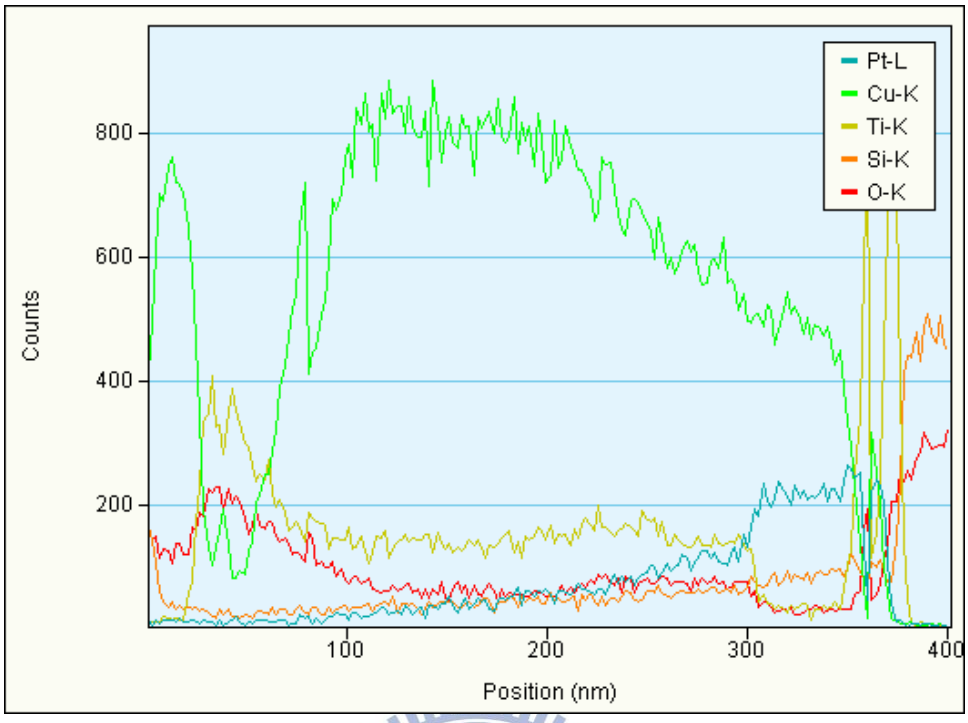


Fig. 3-18 Line scan of annealed co-sputtered Cu/Ti

	Cu(%)	Ti(%)	O(%)	Si(%)	Pt(%)
1	56.9	0	41.5	1.6	0
2	15.4	19.9	64.7	0	0
3	43.3	13.2	43.5	0	0
4	47	16.2	31.4	0	5.4
5	55.2	9.9	23.5	0	11.5
6	53.2	0	10.3	3	33.4
7	58.1	5.7	10.9	2.2	23.1
8	35.6	10.3	54.1	0	0
9	8.2	20.9	70.9	0	0

Table 3-3 EDX analysis of the marked area in fig. 3-17

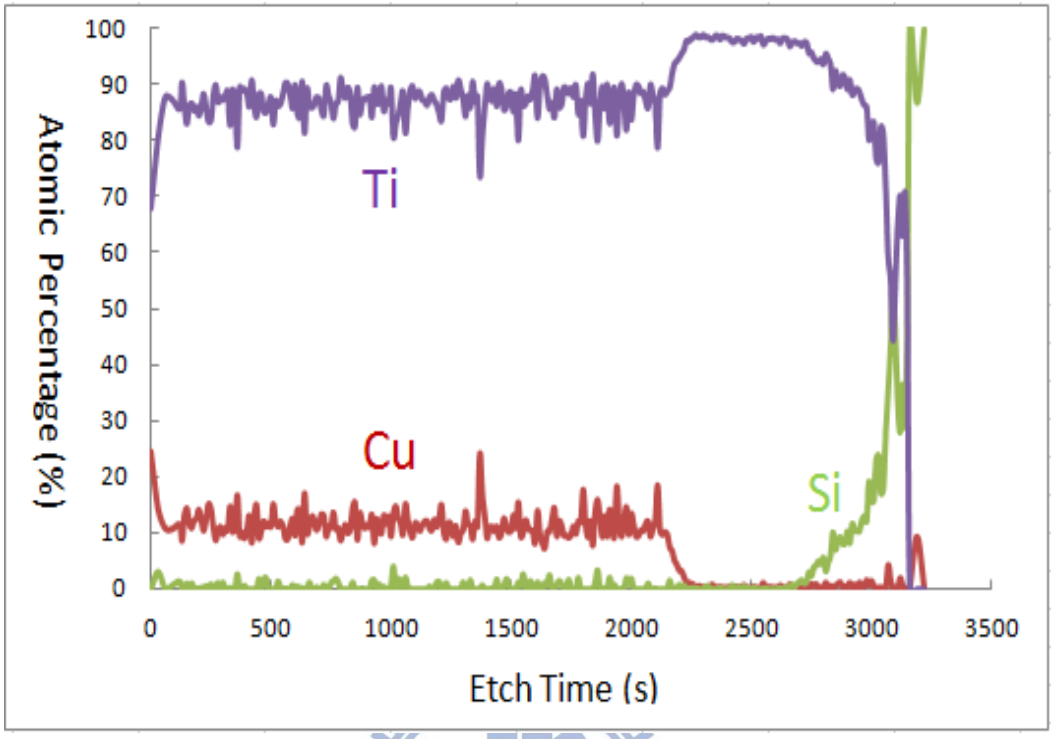


Fig. 3-19 Auger analysis of co-sputtered Cu/Ti on Ti silicide

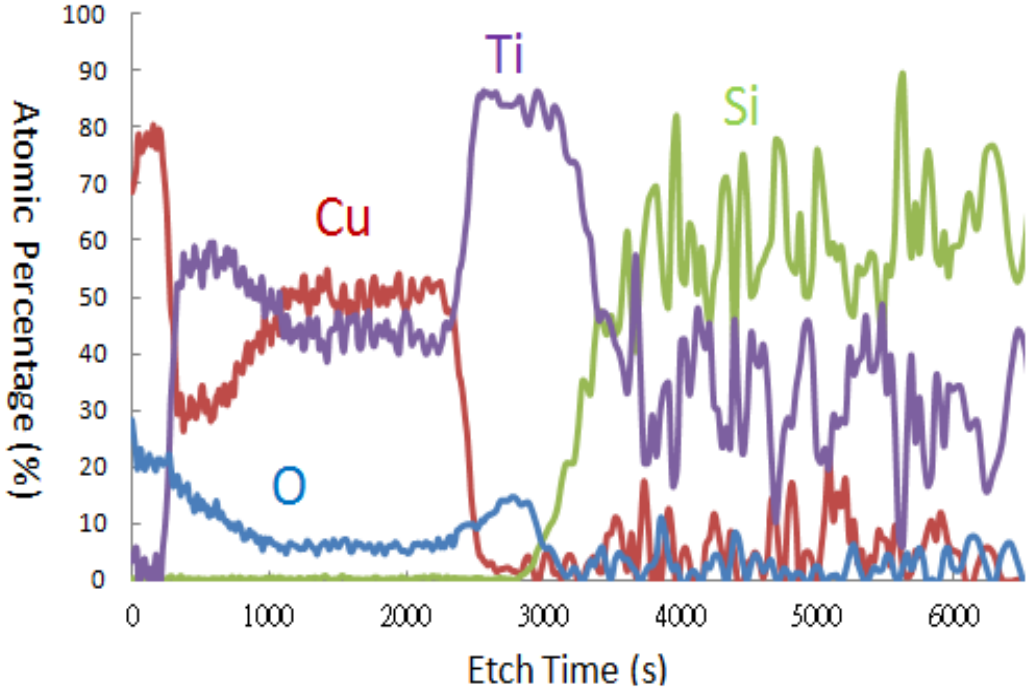


Fig. 3-20 Auger analysis after annealed in oxygen ambient for 20min

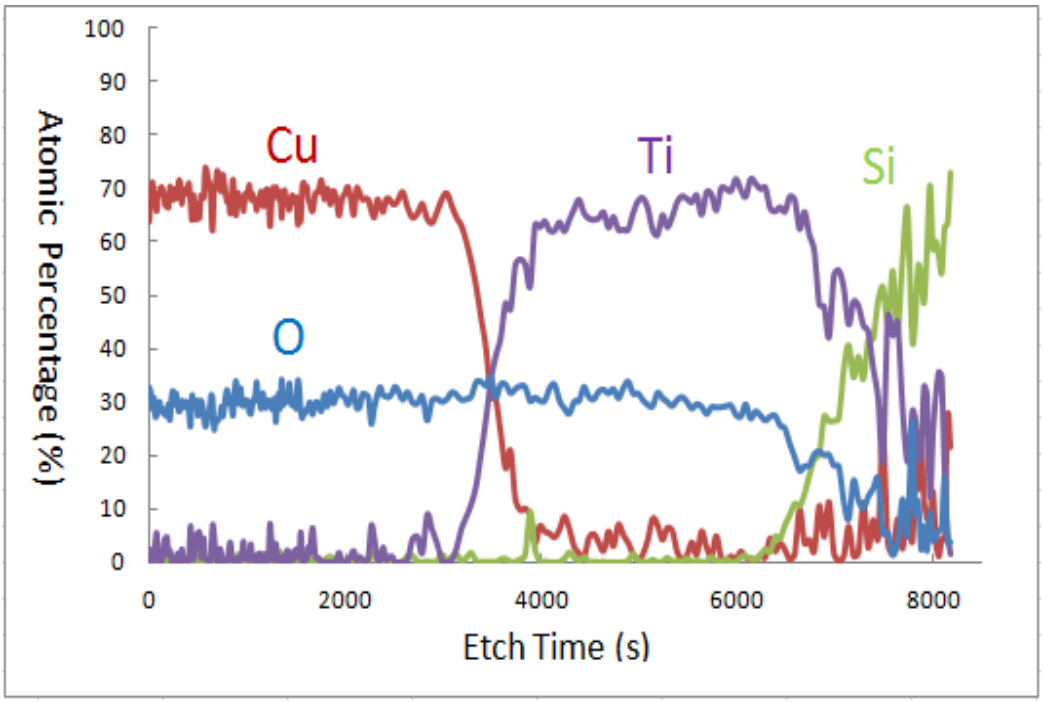


Fig. 3-21 Auger analysis of co-sputtered Cu/Ti after heated on hot plate for 100min in atmosphere ambient

Chapter 4
Reliability Evaluation of Co-sputtered Cu/Ti Bonded Interconnects

4.1 Introduction

Co-sputtered Cu/Ti bonded interconnect with Cu as major bonding/conduction layer, self-formed adhesion layer, and possible Ti oxide as passivation layer is consider a potential candidate for 3D integration. Therefore, in order to verify the capability of co-sputtered Cu/Ti interconnect for commercial usage and mass production, reliability test is strongly required.

In this chapter, we investigated co-sputtered Cu/Ti bonded interconnect with various electrical reliability test including: contact resistance measurement, AC current stressing test, DC current stressing test, humidity test, and temperature cycling test. In addition, structural changes of the bonded sample are also investigated with SAT analysis and TEM images after applying to different test conditions. Comparisons of each test between co-sputtered Cu/Ti bonding and conventional direct Cu-Cu bonding are also presented in this chapter.

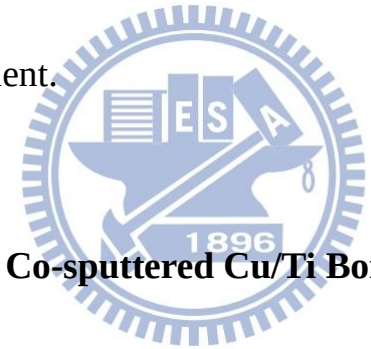
4-2 Experimental

Standard RCA cleaning is applied to the wafer before 500nm TEOS deposition. A thin film of HMDS is deposited, and a layer of photo-resistance of designed pattern for Kelvin structure measurement shown in Fig. 4-1 or Fig. 4-2 is developed. 30nm of Ti layer and Pt layer of 50nm are deposited by E-Gun Evaporation. Co-sputtered Cu/Ti were prepared by co-sputtering Cu and Ti simultaneously in a multi-target chamber at 150W for 90 minutes, under a working pressure of $7x10^{-3}$ Torr and with a base pressure of $1x10^{-6}$ Torr. The approximate sputtering rates for Cu and Ti are 0.6 Å/s and 0.1 Å/s respectively. At last, the metal line pattern is revealed using lift-off in a micro sonic tank, and immerse in acetone. A structural depiction is given in Fig. 4-4.

The test structure of the upper sample is in Fig.4-1 and the lower sample is Fig 4-2. The patterned is designed for the lower layer to have a longer metal line than the upper layer, such that the metal lines of the lower layer are exposed and can served as probing pads for further measurement. The structure after bonding is shown in Fig. 4-3, and red area represent the bonded area. The square area of 62500 um^2 is the test structure in the following tests. This test structure is designed according

to ref[18], which have a large tolerance of miss alignment along the y-axis (parallel to the metal lines).

However, when the prepared sample is exposed in atmosphere, a considerable amount of native copper oxide will be formed on the surface. According to previous studies, copper oxide on the bonding interface would greatly affected bonding quality and bonding strength. Therefore, prior to bonding, an acetic acid cleaning was applied to the sample for 60s. Samples are bonded face-to-face at 400°C for 100 min, with 145 psi, and in atmosphere ambient.



4.3 Reliability Tests of Co-sputtered Cu/Ti Bonded Interconnect

4.3.1 Contact Resistance Measurements

The contact resistance of Cu/Ti bonded interconnects were evaluated by fabricating and measuring a Kelvin structure of a bonding area subjected to 62500 um^2. Contact resistance measurement under the first current ramping of the co-sputtered Cu/Ti bond structure and Cu-Cu bond structure are shown in Fig. 4-5 and 4-6. Both structures have high contact resistance from the beginning, and then trend to decrease with respect to higher applied current. The reduction of contact resistance according to

higher applied current was also observed in other related research [19]. This reduction is believed to be related to a large amount of Joule heat induced by high applied current, which simulates rearrangement at the partial bond interface. Since TEM and EDX results have shown Cu is the major bond material, it is expected to observe the similar behavior in contact resistance between the two structures.

Although contact resistance is highly related to the applied current at the first few measurements, contact resistance reaches a stable value after a few times of measuring and will no longer be affected by the applied current. Stable contact resistances of co-sputtered Cu/Ti interconnect and conventional direct cu-cu interconnect are shown in Fig. 4-7 and Fig. 4-8. From Fig. 4-7 and Fig. 4-8, the contact resistances have shared a similar resistance range, around 5 to 6 ohms. The result implies the two cases have a similar atom composition, structure, and most importantly, electrical behavior. In addition, the deviation of resistance is small under different applied currents, indicating a stable bonded structure.

The stable electrical contact resistance measurement result under different applied current suggests Cu/Ti structure has completed the diffusion process of Cu and Ti atoms and formed a reliable bonded

structure during bonding. Therefore, the atomic distribution is not changed across the bond structure, and the contact resistance remains in the same range.

However, if we calculate the specific contact resistance of the bonded structure with the following equation:

$$\rho_c = R_c \times A_c \qquad (3)$$

where ρ_c is specific contact resistance, R_c is contact resistance, and A_c is contact area , the value is a few orders larger than the ideal value.[18] The reason of this great discrepancy is poor uniformity of our present method, which is believed to be caused by uneven bonding pressure of our bonder. A SAT image of a bonded interconnect is given in Fig. 4-9, with the dark area as the bonded area and vice versa. As we can see in the SAT image, the actual bonded area is a lot smaller than the purposed 62500 um^2 used in Eq. 3.

4.3.2 AC Current Stressing Test

The stability of the bond structure is significant for 3D integration applications, especially its electrical performance after multiple operations. Therefore, the Cu/Ti bonded structures were evaluated for

stability against current stressing, with each cycling consists of a sweeping of current from 100 mA to -100 mA. The average contact resistance after multiple loops of current stressing were measured and shown in Fig. 4-10. It is shown that the deviation of resistance is small within the entire range of 450 current stressing loops. This result implies that the bonded contact is stable and could also endure a long term of electrical current.

A comparison of conventional direct Cu-Cu bonding is also presented in Fig. 4-11. The result of direct Cu-Cu bonding has a similar resistance with co-sputtered Cu/Ti bonding. As expected, Cu has a great resistance against electro-migration, and the resistance is stable within the 400 current stressing loops.

4.3.3 DC Current Stressing Test

A DC current stressing test for more than 20 hours is applied to the bonded interconnect, with stressing current density of 3.2×10^2 A/cm^2. The contact resistance had been recorded after each period of time, and the resistance changes are shown in Fig. 4-12 The resistance deviation in Fig. 10 is small and are mostly confined in a small range. The result suggests

that the structure is stable under large current density and could stand for long operating time. This is an important indicator for structure reliability, since most interconnect is concerned for its electro-migration resistance. Same as the AC current stressing case, the stability of the bond structure is significant for 3D integration applications, especially its electrical performance after multiple operations. However, the endurance under DC current stressing is a more major concern. In the AC current stressing case, the structure is likely to recover the defects with the alternation applied current. DC current stressing , on the other hand, can be more truthful of showing the reliability of the structure. In our case, the results of DC and AC current stressing test both prove that the structure is stable and has a high resistance toward electro-migration.

The result of DC current stressing test of conventional direct Cu-Cu interconnect is given in Fig. 4-13. The resistance of direct Cu-Cu bond is stable and has small deviation during the test. Since both structure use Cu as the major bonding medium, it is no surprise that both structure have a stable resistance under current stressing. The test also implies that for the case of co-sputtered Cu/Ti, the bonding material is copper but not Cu-Ti alloy, where for most alloys, the issue of electro-migration is severe, and

could lead to great reliability problems. [20]

4.3.4 Temperature Cycling Test

A temperature cycling test (TCT) ranging from -40℃ to 125℃ was applied to the Cu/Ti bond structure. Figure 4-14 shows resistance behaviors of one Cu/Ti bond sample before and after a thousand cycles of TCT under current sweeping. The results in Fig. 4-14 show that the contact resistance varies only a little after the TCT test. Hence, it is suggested that the Cu/Ti bond structure can endure temperature variation from -40℃ to 125℃ without fatigue failure, such as wire break or bond separation, which was induced/accelerated during the test. There is no observation of die cracking or bond pad lifting, which suggest that the co-sputtered metal has an matching coefficient of thermal expansion (CTE) with the substrate. In other words, even under temperature variation, the bonding structure would not induce mechanical stress to cause defects or damages on other devices. Therefore, even at extremely high or low temperature, integration using the purposed bonding structure could still be functional and effective.

4.3.5 Humidity Test

Humidity test is subjected to evaluate the effect of moist to the test subject. Depending on the absorbing rate of moist of the material, and the interaction of the material to moist, the resistance of material against moist can be analyzed. Humidity test is done by placing a sample in a environment of high humid and temperature, in order to simulate an accelerated aging condition to the sample.

A humidity test of 55℃/80% RH was performed on the Cu/Ti and direct Cu bond structure for over 200 hours, and the result is shown in Fig. 4-15 and 4-16. According to the result, the average contact resistance was stable within the whole test without deterioration and corrosion in the bond structure. Therefore, it is implied the Cu/Ti structure and Cu-cu bond structure exhibit a good bonding quality and good resistance to moisture and heat environment.

Although in the previous section, the test samples show a high resistance toward moisture and heat, there are other samples that show a different behavior under humidity test. Another set of samples of co-sputtered Cu/Ti and Cu bonding structure was tested under the previous condition, and the results are given in Fig. 4-17 and 4-18. As we

can see, the resistance increases a large amount from around 10 ohms to 20ohms after a period of time, and remains stable at the higher value. This phenomenon is observed in both cases, and thus we believe this type of deterioration is not caused by the material or diffusion mechanism of the metal. The deterioration is believed to be affected by interfacial void at the bonding interface and will be further discussed in chapter 4.3.6.

4.4 Investigation of Interconnect Degradation

Degradation of one partially bonded structure at room temperature was evaluated by the resistance change measurement, as shown in Fig.4-19. From the TEM images of one well-bonded sample in Fig.4-20 and another one with degradation in Fig.4-21, the degraded sample has voids at the interface, unlike the continuous copper layer in the well-bonded one. Other images of voids are shown in Fig. 4-22 to 4-25. In these images, we can found that all voids are presented at the bonding interface, and the size of each voids are different. Some have the size of few microns, like the ones in Fig.4-22 and 4-23, while others are only few nanometers large, as in Fig. 4-24 and 4-25.

The presence of voids has been reported in other researches, and it is

proved to have a severe impact on device reliability.[21-22] Formation of voids might due to several reasons, including high surface roughness of the sample prior to bonding or uneven pressure during bonding. In metal alloy, different diffusion rate of the metal atoms might lead to Kirkendall effect, and in turns causes Kirkendall voids. However, in our case, no metal alloys are formed and the bonding interface is dominated by copper atoms, and thus Kirkendall voids are not our major concern. In conventional direct Cu-Cu bonding, interfacial voids are also observed, and was assumed to be caused by thermal stress relaxation.[21] Due to our bonding mechanism resembles to direct Cu-Cu bonding, voids found in our study is believed to be caused by the same reason. Therefore, if some oxygen remains inside the void after bonding, oxidation of copper continues until oxygen is exhausted. This result explains the increase of the resistance in the first few days of the experiment and the reach of a stable value afterwards in Fig. 4-19.

The result of degradation of these particular samples is consistent with the one that we discussed in chapter 4.3.5.2. While the samples in chapter 4.3.5.1 remains at a stable resistance during the whole humidity test, the resistance of samples in chapter 4.3.5.2 increase a large amount

and stay a stable value afterward. We believed this discrepancy is also due to the absent and present of interfacial voids in the two sample, since the increase in resistance in chapter 4.3.5.2 has shared such a similar change with the degraded sample discussed here.

4.5 Summary

In this chapter, we discussed the result of reliability tests of the proposed structure. Our structure is proved to be robust and the electrical performance has not been degraded after each tests. We have also discussed the cause and impact of interfacial voids to our proposed structure. An appropriate bonding temperature to simulate diffusion but also prevent formation of interfacial voids is the key for the proposed bonding interconnect to be success.

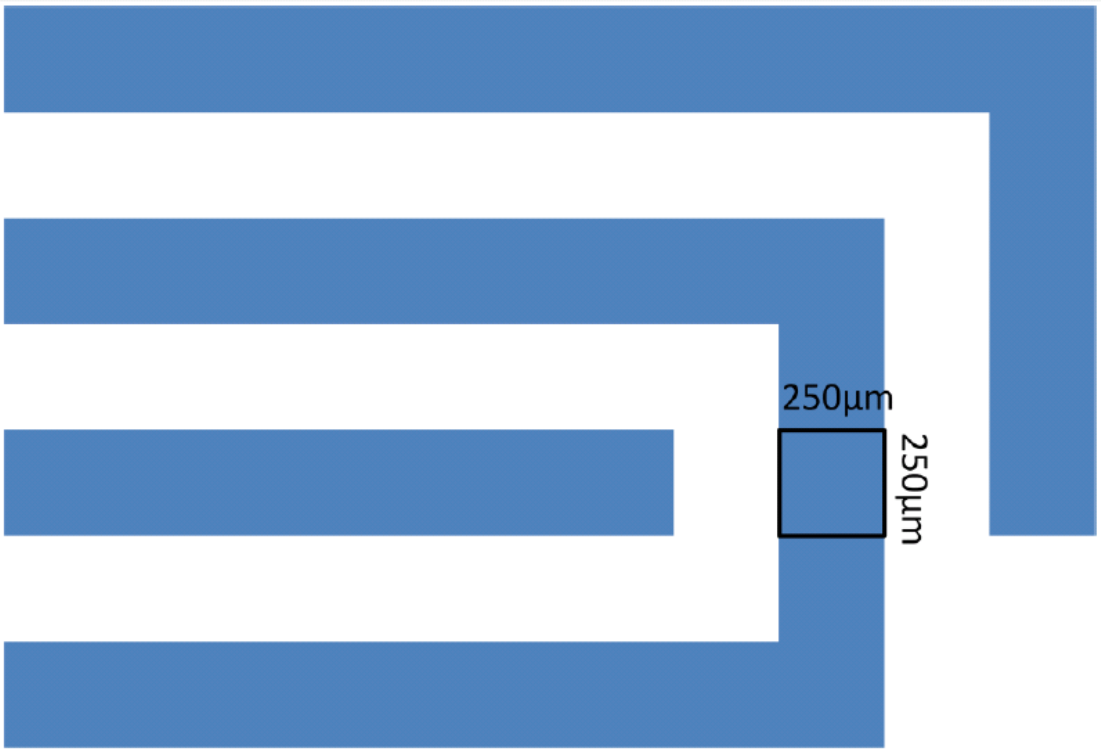


Fig. 4-1 Mask for the top bonding sample

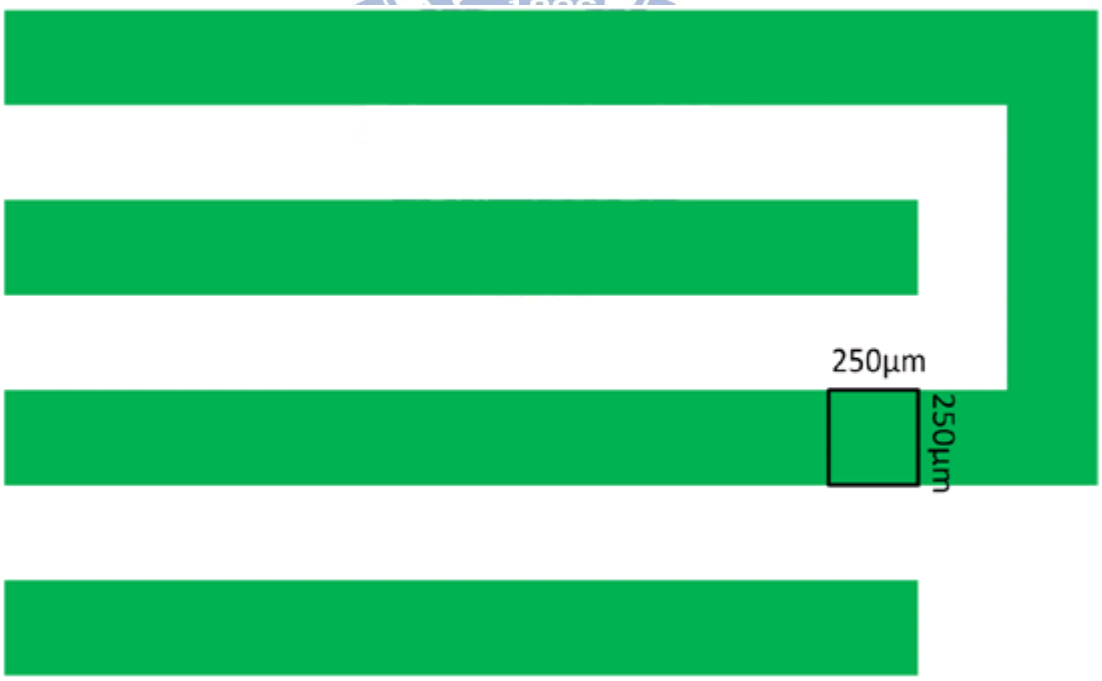


Fig. 4-2 Mask for the bottom bonding sample

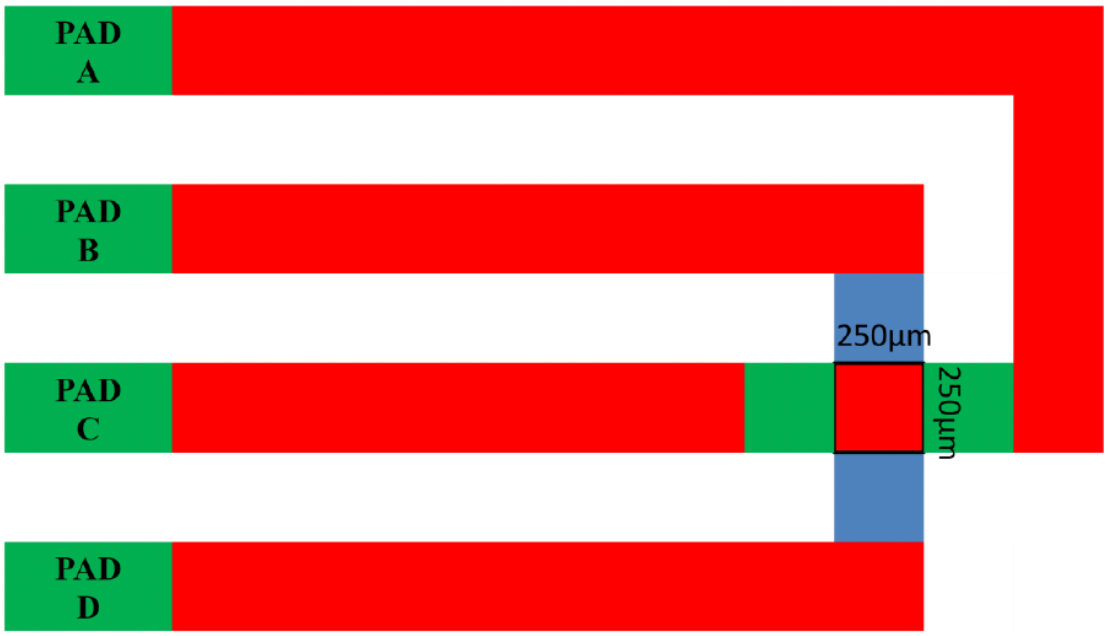


Fig. 4-3 Schematics for the bonded sample

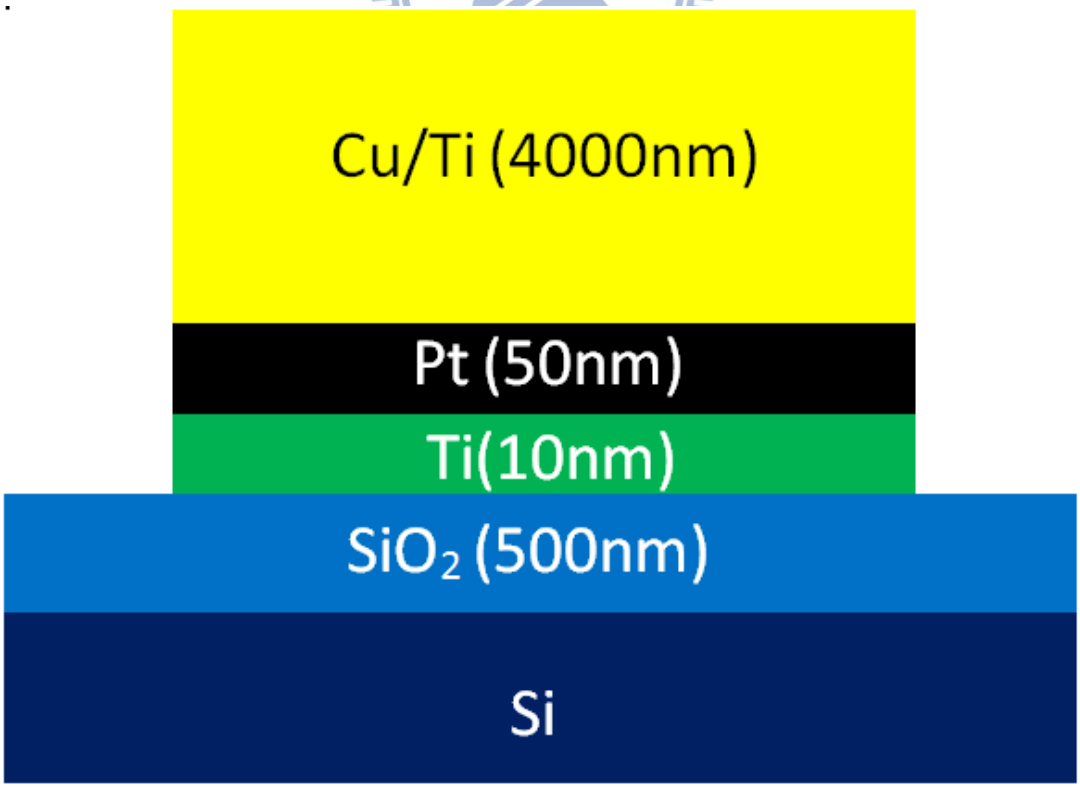


Fig. 4-4 Structure of single side of the bonded sample

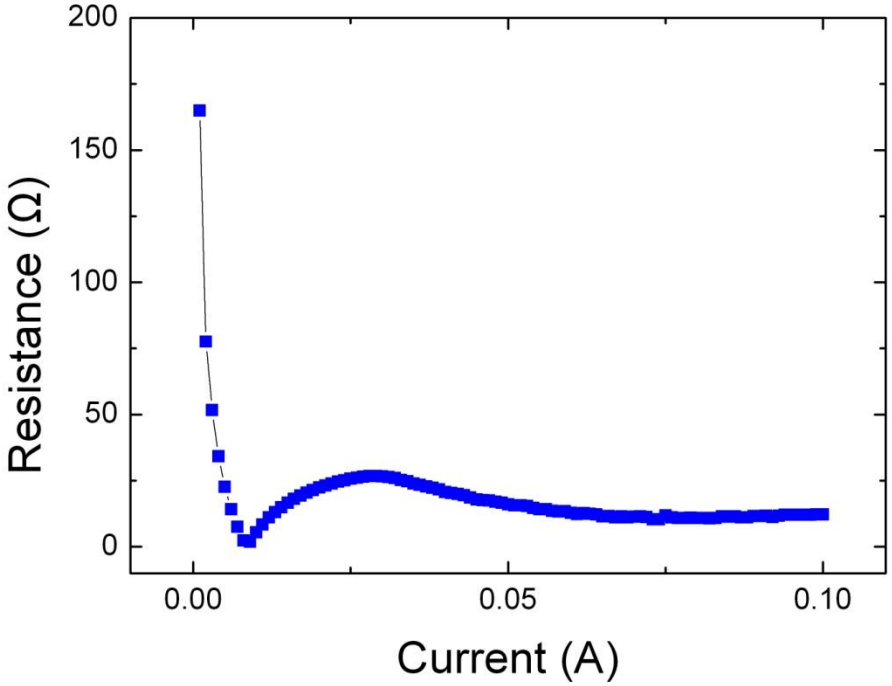


Fig. 4-5 Contact resistance of co-sputtered Cu/Ti

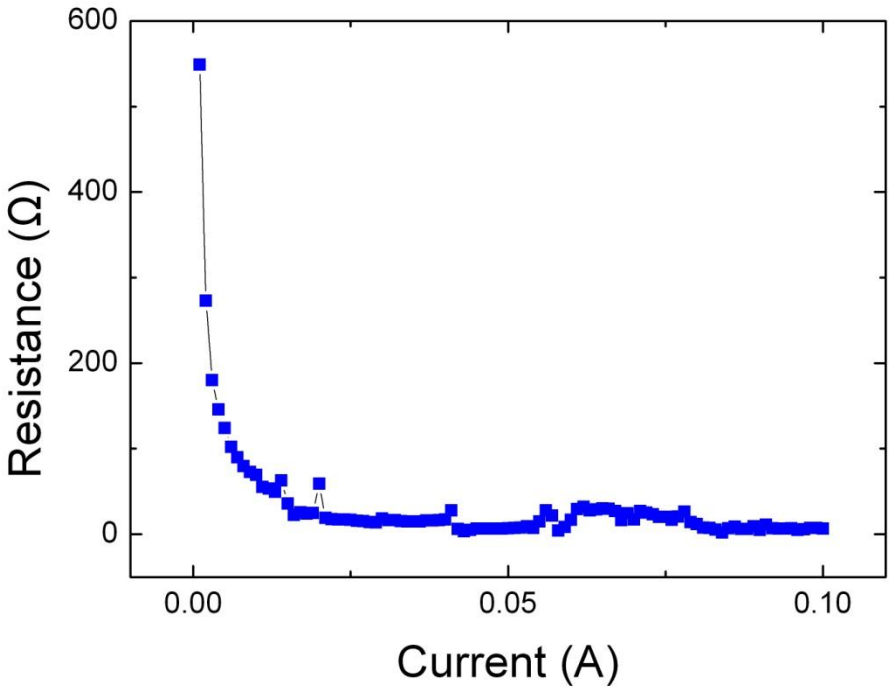


Fig. 4-6 Contact resistance of direct Cu-Cu bonding

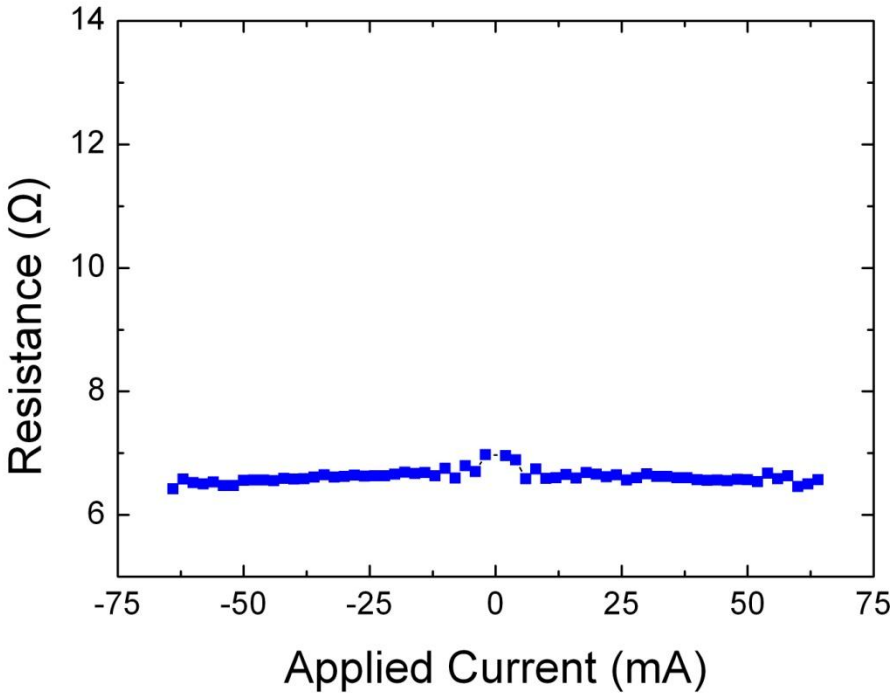


Fig. 4-7 Stable contact resistance of co-sputtered Cu/Ti interconnect

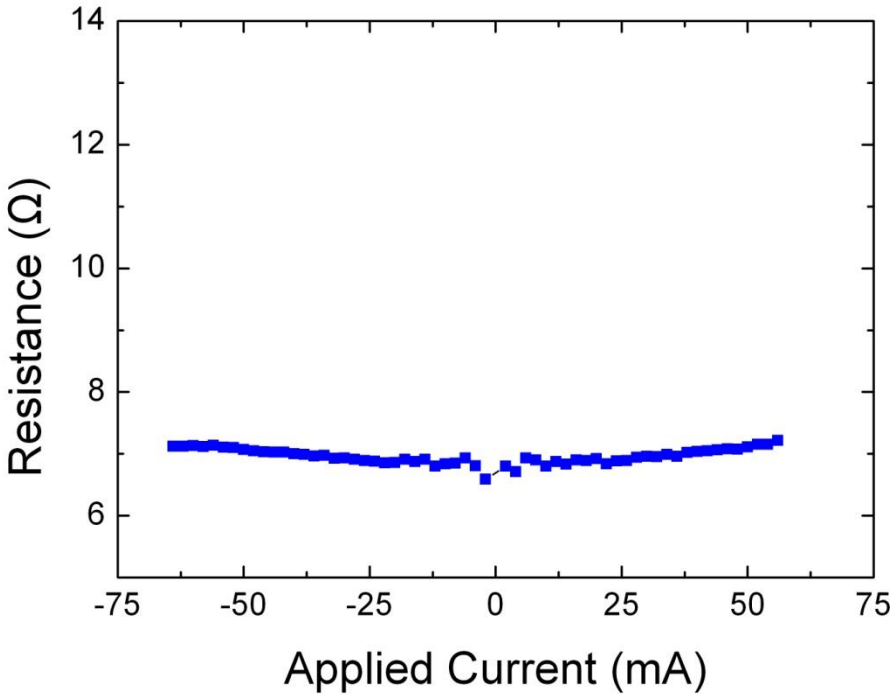


Fig. 4-8 Stable contact resistance of conventional Cu interconnect

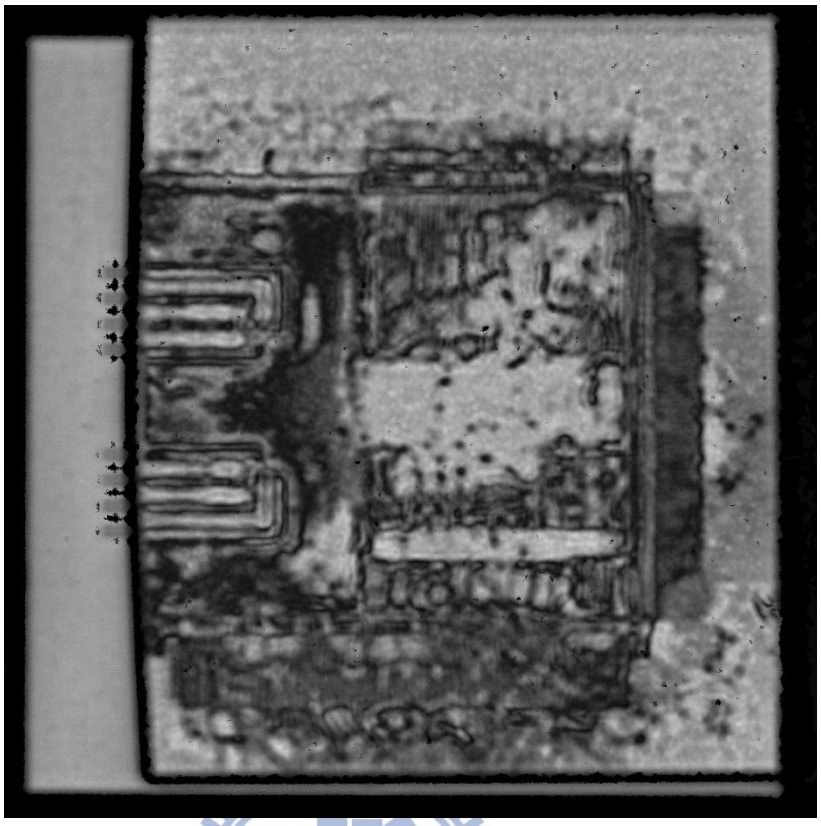


Fig. 4-9 SAT image of patterned sample

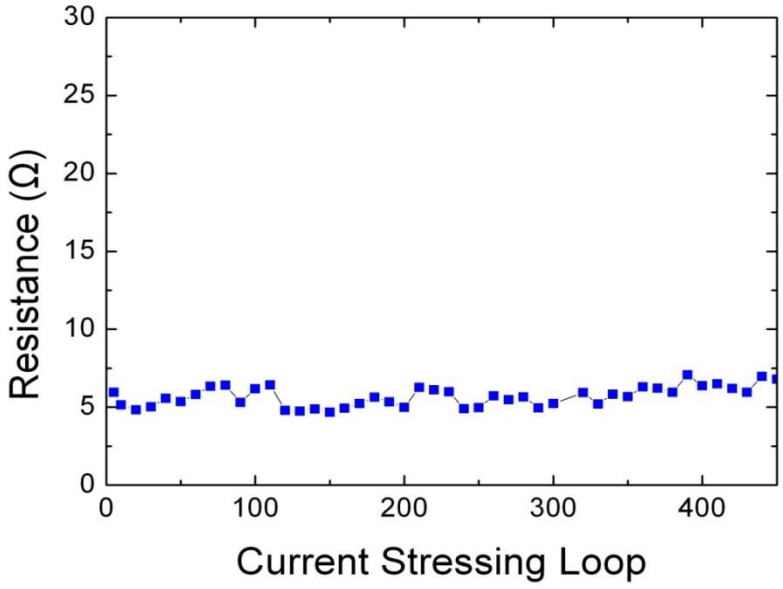


Fig. 4-10 Co-sputtered Cu/Ti resistance change after each current stressing cycle

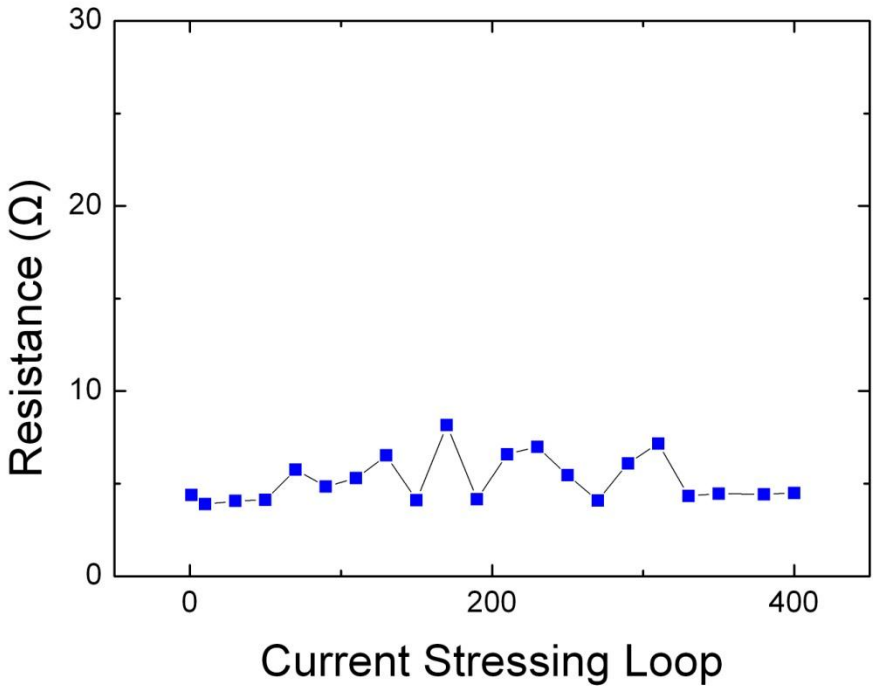


Fig. 4-11 Conventional Cu-Cu interconnect resistance changes after each current stressing cycle

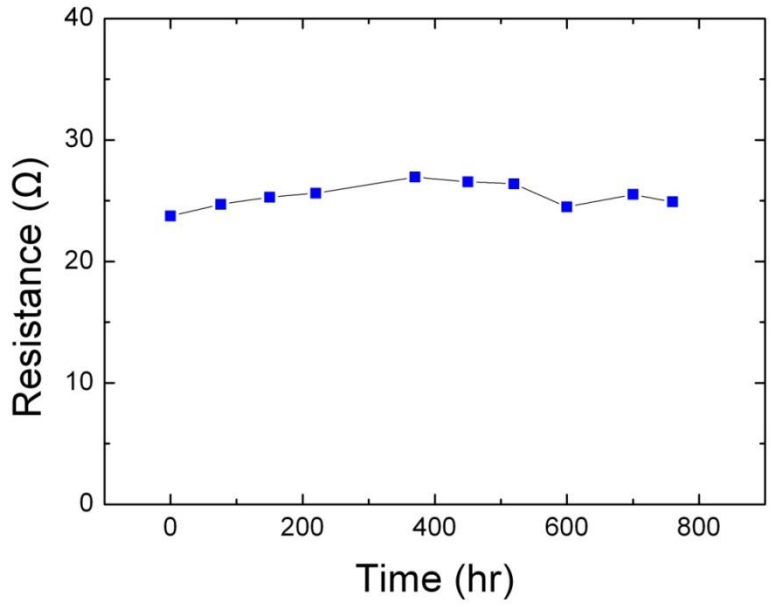


Fig. 4-12 Co-sputtered Cu/Ti resistance vs. DC current stressing time

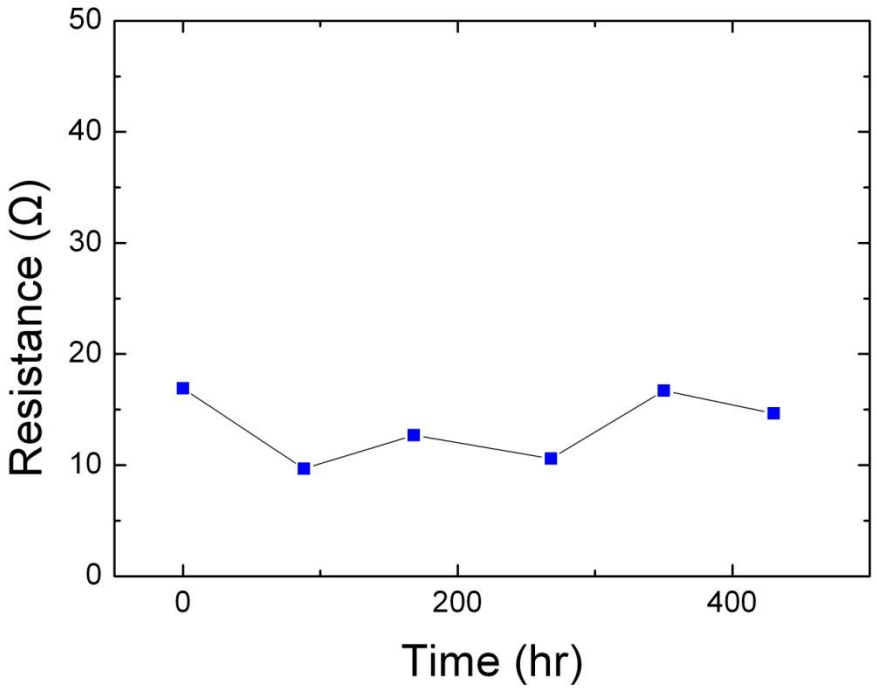


Fig. 4-13 Cu-Cu interconnect resistance vs. DC current stressing time

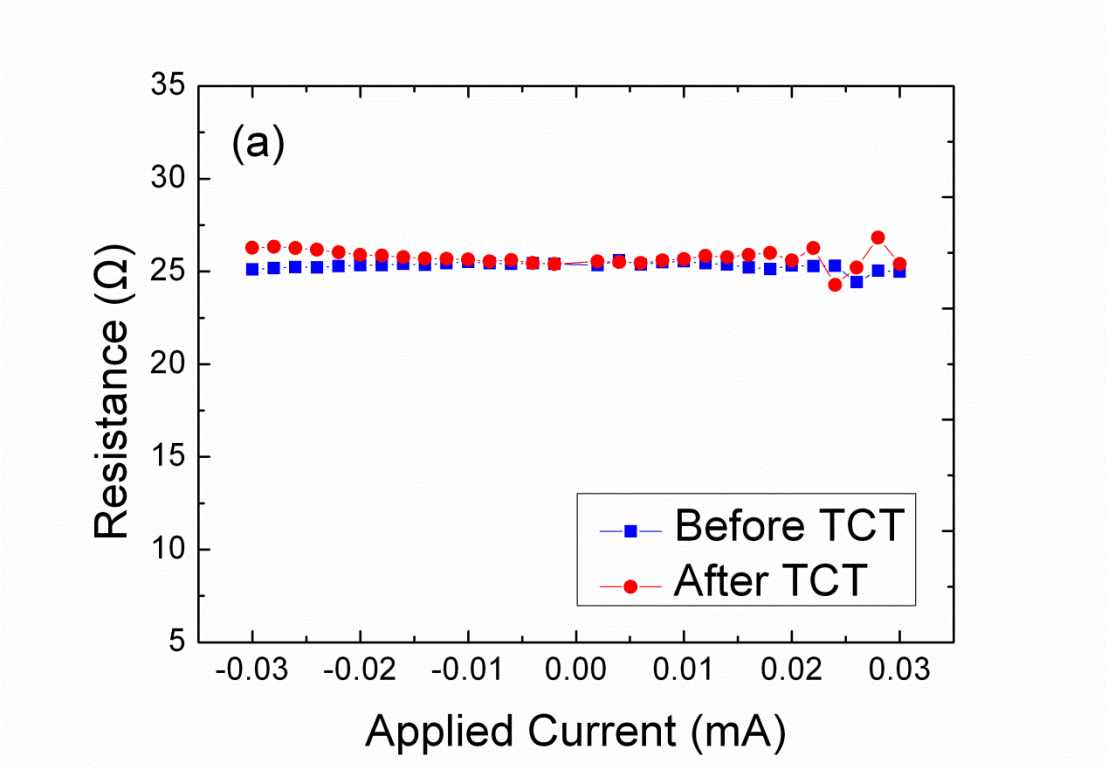


Fig. 4-14 Resistance of co-sputtered Cu/Ti before and after TCT

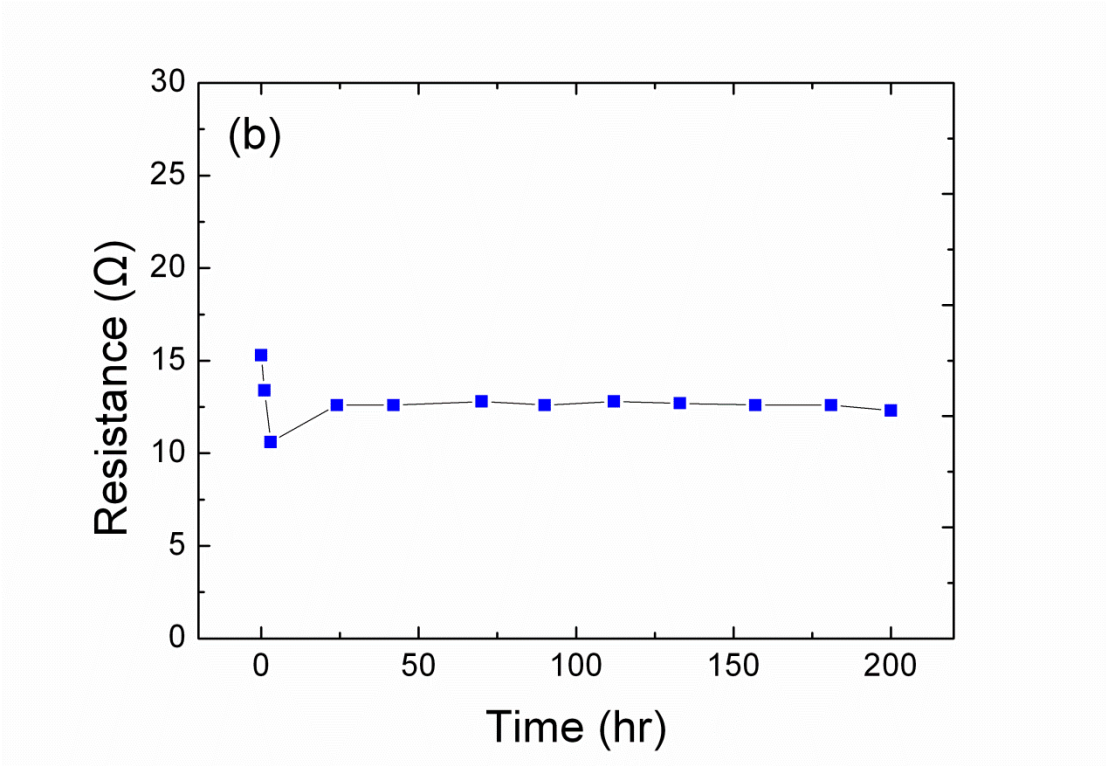


Fig. 4-15 Resistance of co-sputtered Cu/Ti during humidity test

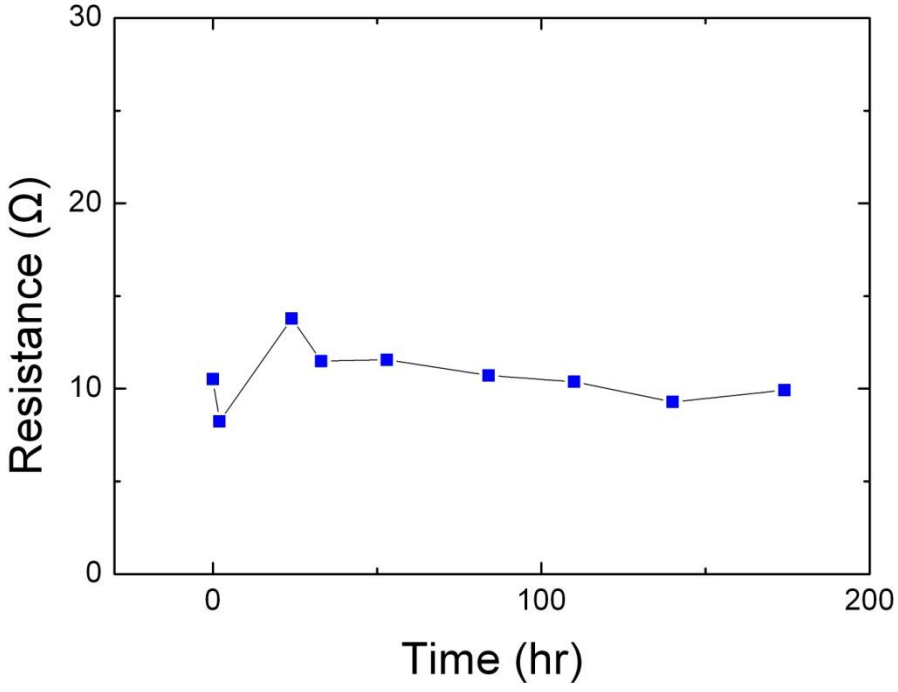


Fig. 4-16 Resistance of Cu-Cu interconnect during humidity test

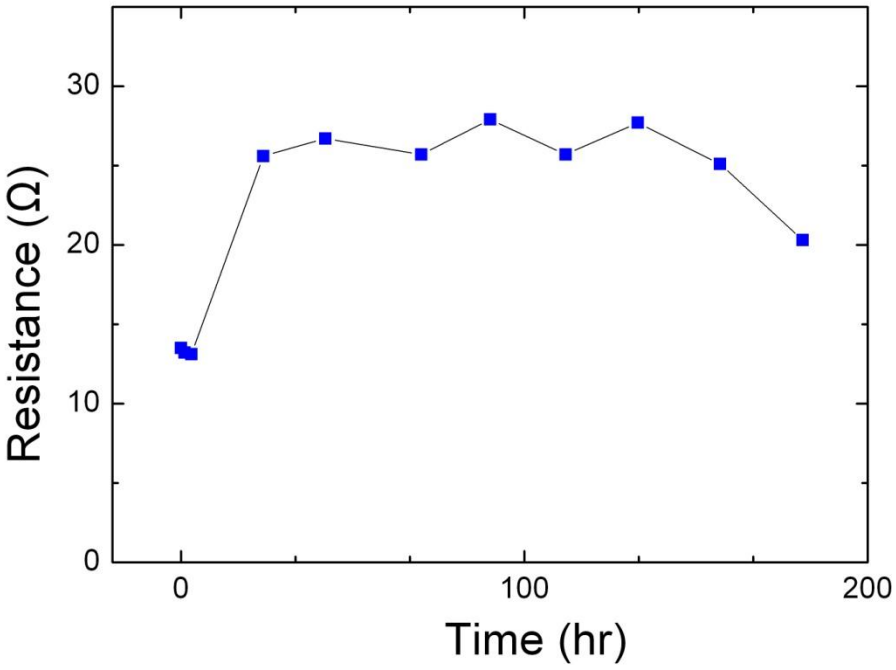


Fig. 4-17 Degraded Cu/Ti interconnect during humidity test

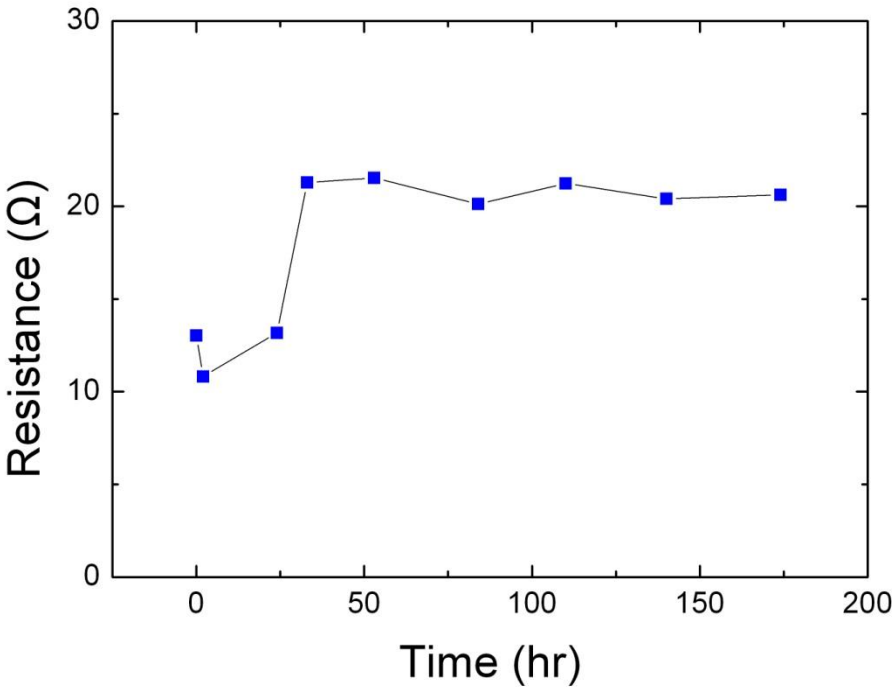


Fig. 4-18 Degraded Cu-Cu interconnect during humidity test

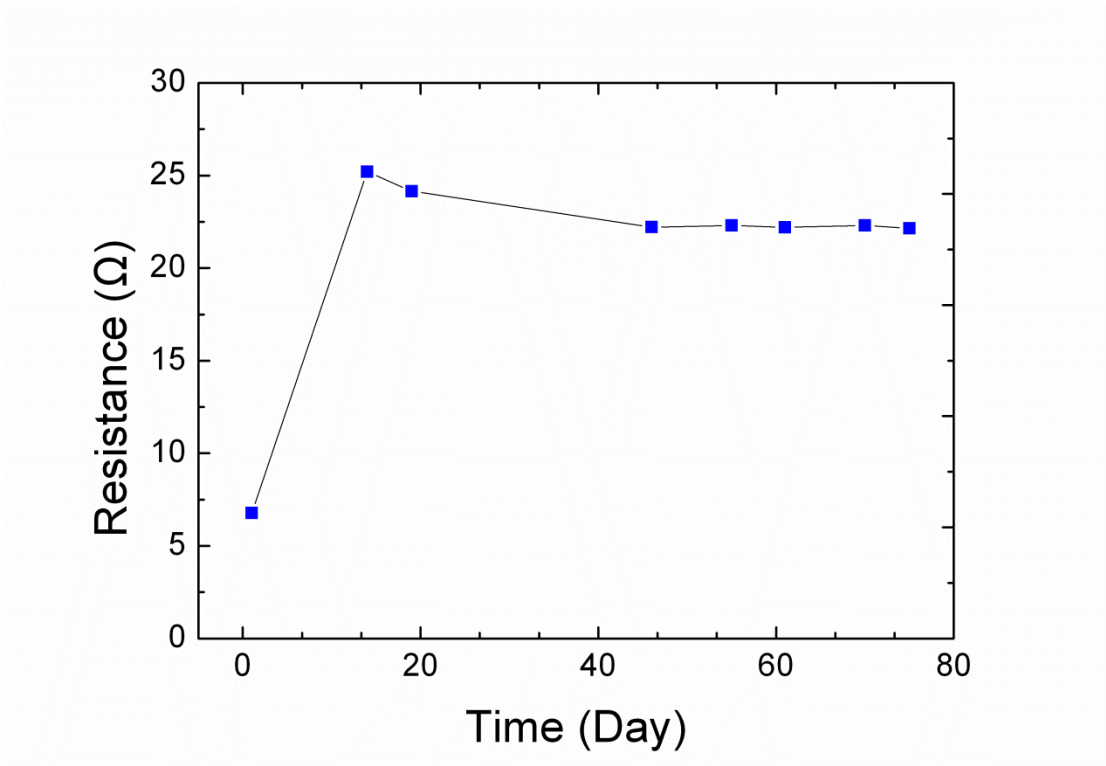


Fig. 4-19 Degraded Cu/Ti interconnect at room temperature

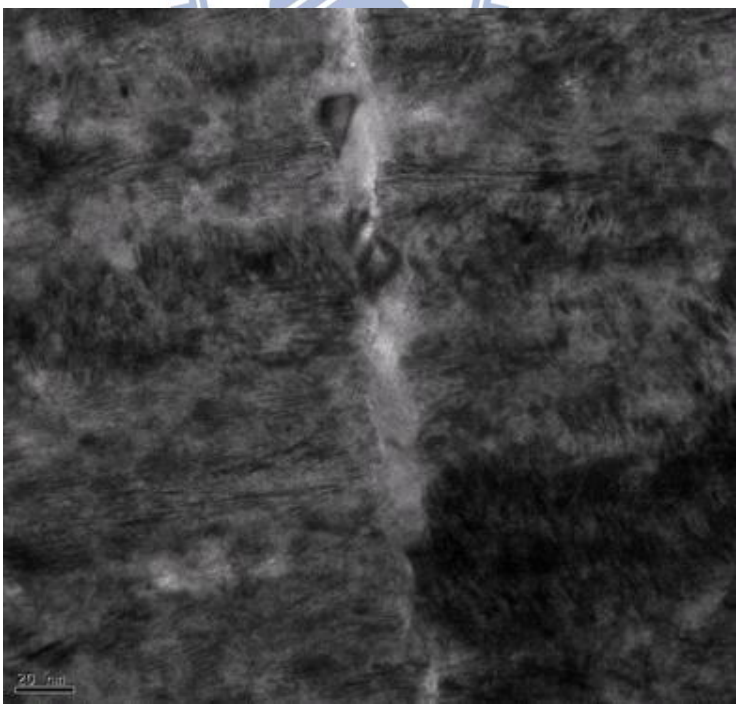


Fig. 4-20 TEM image of void-free bonding interface

Fig 4-21 TEM image of bonding interface with viods

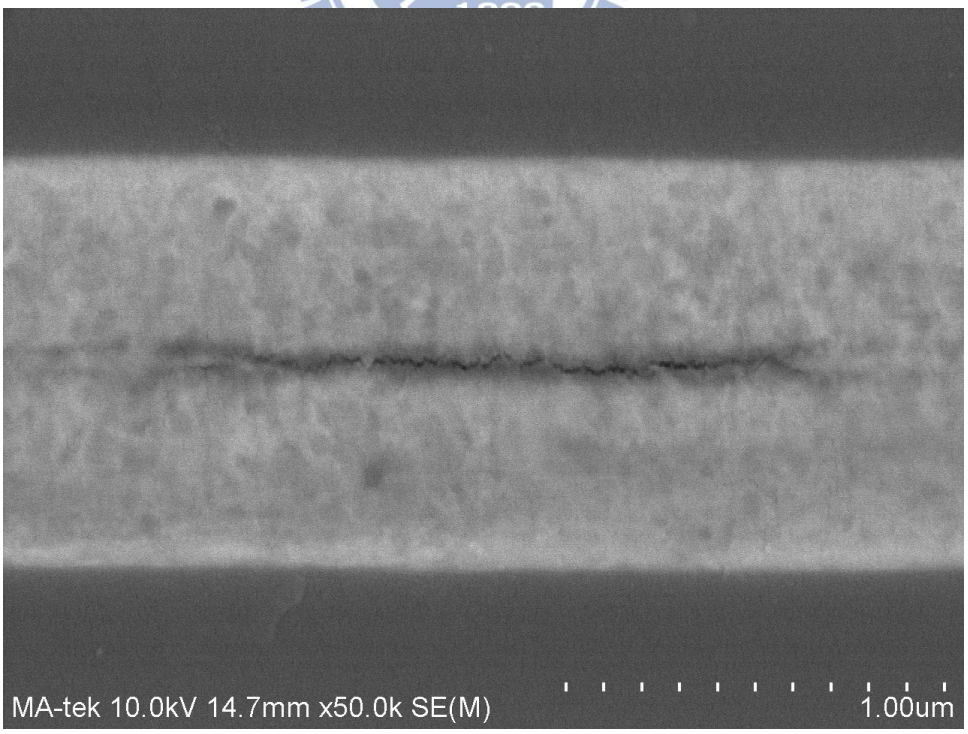


Fig. 4-22 SEM image of crack at bonding interface

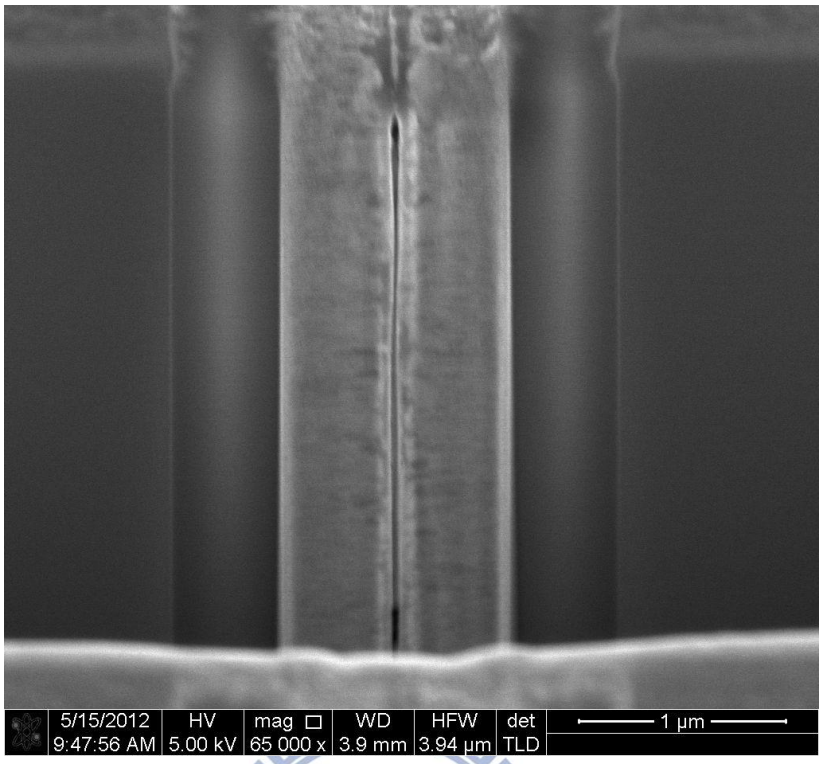


Fig. 4-23 FIB images of interfacial voids

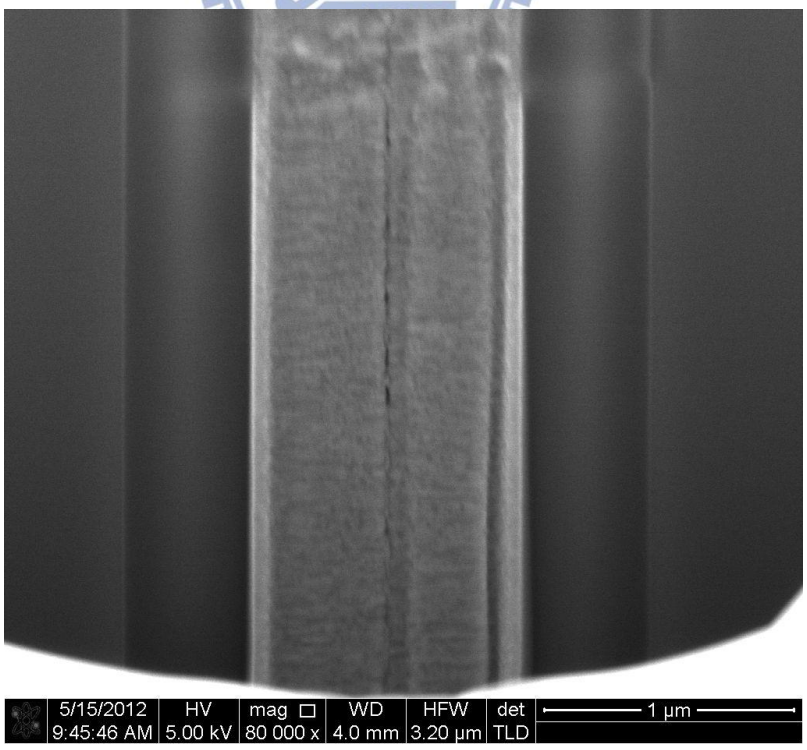


Fig. 4-24 FIB image of voids at bonding interface

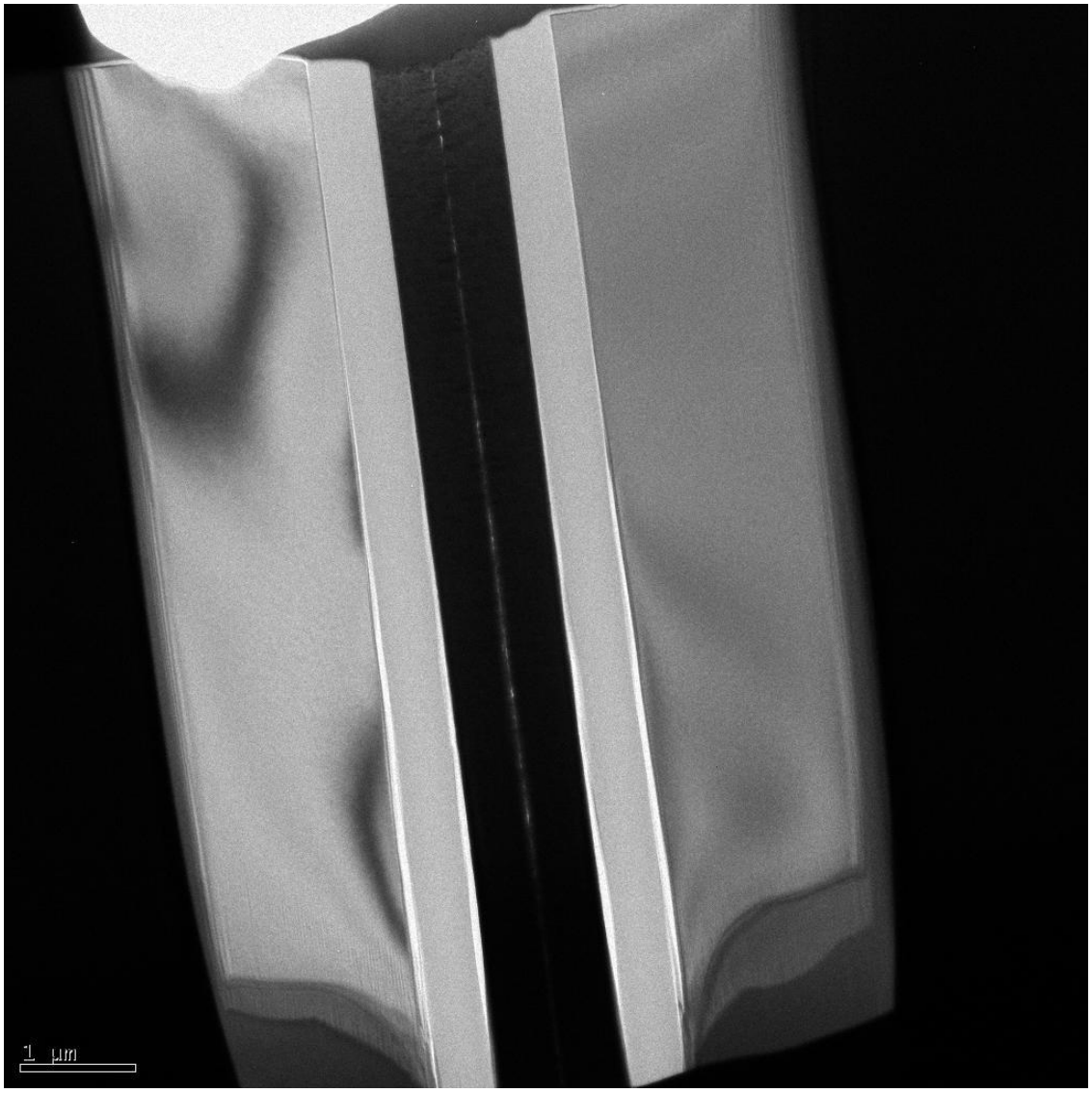


Fig.4-25 TEM image of interfacial voids(white spots)

Chapter 5

Future Work

5-1 Conclusion

In this thesis, an investigation on 3D integration of co-sputtered Cu/Ti as bonded interconnect is present. Both the material analysis and electrical evaluation are studied. Moreover, the structural changes under different bonding temperature, different bonding level (chip and wafer level), different bonding time, and different bonding ambient are also discussed.

Due to the interdiffusion of copper and titanium at high temperature, segregation of the two metals is observed. For this interesting property, a Ti self-formed adhesive layer is formed at the substrate side, and copper bonding is formed at the bonding interface after thermal compression process. In addition, when the co-sputtered metal is annealed under oxygen ambient, Ti oxide is observed at the surface and sidewall, which could prevent the inner structure, namely copper, from corrosion. With these features, we believed that co-sputtered Cu/Ti is a suitable candidate for 3D bonded interconnects.

For mass production and further applications, electrical evaluation is

also performed on the presented structure. A revised kelvin structure is used to investigate the electrical properties of co-sputtered Cu/Ti bonded interconnect under various reliability test and conditions. According to the result, the contact is verified to be stable after each test, and the contact resistance is comparable to conventional direct Cu-Cu bonding method. Therefore, co-sputtered Cu/Ti is proved to have a great potential as the bonding material in 3D integration.

5-2 Future Work

In the scope of this research, possible Ti oxide as passivation layer has been observed. However, current research of passivation layer is performed under oxygen ambient annealing but not during actually bonding process. Therefore, the features and properties of Ti oxide passivation layer still needs further investigation.

In addition, the occurrence of interfacial voids after bonding leads to deterioration of the bonded interconnects. To avoid or reduce the formation of such voids is also a major issue for further applications.

Reference

[1] D. Sylvester and C. Hu, “Analytical modeling and characterization of deep-submicrometer interconnect,” Proc. IEEE, vol. 89, no. 5, pp. 634–664, May 2001.

[2] A. Rahman and R. Reif, “System-level performance evaluation of threedimensional integrated circuits,” IEEE Trans. Very Large Scale Integr.(VLSI) Syst., vol. 8, no. 6, pp. 671–678, Dec. 2000.

[3] Semicond. Ind. Assoc., International Technology Roadmap for Semiconductors, San Jose, CA2001.

[4] V. Subramanian, M. Toita, N. R. Ibrahim, S. J. Souri, and K. C. Saraswat, “Low-leakage germanium-seeded laterally-crystallized single-grain 100-nm TFTs for vertical integration applications,” IEEE Electron Device Lett., vol. 20, no. 7, pp. 341–343, Jul. 1999.

[5] V. W. C. Chan, P. C. H. Chan, and M. Chan, “Multiple layers of CMOS integrated circuits using recrystallized silicon film,” IEEE Electron Device Lett., vol. 22, no. 2, pp. 77–79, Feb. 2001.

[6] G. Katti et al., “3D Stacked ICs using Cu TSVs and Die to Wafer Hybrid Collective Bonding,” Technical Digest of the International Electron Device Meeting, pp. 357-360, 2009.

[7] S. Y. Hsu, H. Y. Chen and K. N. Chen, “Diffusion of Co-Sputtered Metals as Bonding Materials for 3D Interconnects during Thermal Treatments,” Journal of Nanoscience and Nanotechnology, 12, pp.2467-2471, Mar 2012.

[8] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, “3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration,” Proc. IEEE, vol. 89, no. 5, pp. 602–633, May 2001.

[9] C. T. Ko and K. N. Chen, “Low temperature bonding technology for 3-D integration,” Microelectron. Reliab., vol. 52, no. 2, pp. 302–311, Feb. 2012.

[10] K.-N. Chen, Z. Xu, and J.-Q. Lu, “Demonstration and electrical performance investigation of wafer-level Cu oxide hybrid bonding schemes,”IEEE Electron Device Lett., vol. 32, no. 8, pp. 1119–1121, Aug. 2011.

[11] K. N. Chen, A. M. Young, S. H. Lee, and J.-Q. Lu, “Electrical performances and structural designs of copper bonding in wafer-level three-dimensional integration,” J. Nanosci. Nanotechnol., vol. 11, no. 6, pp. 5143–5147, Jun. 2011.

[12] P. A. Korzhavyi, I. A. Abrikosov, B. Johansson, A. V. Ruban, and H. L. Skriver, “First-principles calculations of the vacancy formation energy in transition and noble metals,” Phys. Rev. B, vol. 59, no. 18, pp. 11 693–11 703, May 1999.

[13] E. S. Machlin, *An Introduction to Aspects of Thermodynamics and Kinetics Relevant to Materials Science.* Burlington, MA: Elsevier, 2007, p. 251.

[14] K. N. Chen, C. S. Tan, A. Fan, R. Reif, “Copper Bonded Layers Analysis and Effects of Copper Surface Conditions on Bonding Quality for Three-Dimensional Integration,” J. Elec. Mater., vol. 34, no. 12., pp. 1464-1467, December 2005.

[15] K. L. Chavez and D. W. Hess, “A novel method of etching copper oxide using acetic acid,” J. Electrochem. Soc., vol. 148, no. 11, pp. G640–G643, Oct. 2001.

[16] S. Y. Hsu, H. Y. chen, and K. N. Chen, “Cosputtered Cu/Ti bonded interconnects with a self-formed adhesion layer for three-dimensional integration applications,”to be publish in IEEE Electron Device Letter, 2012.

[17] S. TSUKIMOTO, T. KABE, K. ITO, and M. MURAKAMI, "Effect

of Annealing Ambient on the Self-Formation Mechanism of Diffusion Barrier Layers Used in Cu(Ti) Interconnects," J. Elec. Mater., vol. 36, no. 3, pp 258-265, March 2007.

[18] K. N. Chen, A. Fan, C. S. Tan, and R. Reif, “Contact resistance measurement of bonded copper interconnects for three-dimensional integration technology,” IEEE Electron Device Lett., vol. 25 , no. 1, pp.10-12, Jan. 2004.

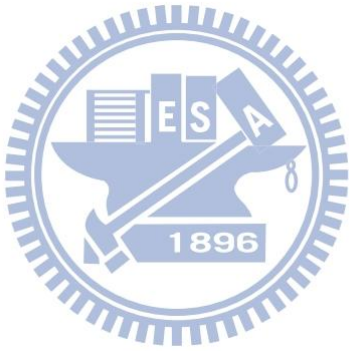
[19] K. N. Chen, C. S. Tan, A. Fan, and R. Reif, “Abnormal contact resistance reduction of bonded copper interconnects in three-dimensional integration during current stressing,” Appl. Phys. Lett., 86, 011903, 2005.

[20] Jae-Woong Naha, Fei Ren, Kyung-Wook Paik, and K.N. Tu, “Effect of electromigration on mechanical shear behavior of flip chip solder joints,” Journal of Materials Research, vol. 21, no.3, pp 698-702, 2006.

[21] C. S. Tan, R. Reif, N. D. Theodore, and S. Pozder, “Observation of interfacial void formation in bonded copper layers,” Appl. Phys. Lett. 87, 201909, 2005.

[22] B. Li, T.D. Sullivan, T.C. Lee, D. Badami, “Reliability challenges

for copper interconnects,” Microelectronics Reliability, vol. 44, no. 3, pp.365-380, March 2004.



簡歷(Vita)

姓名: 陳小予(Hsiao-yu Chen)

性別: 女

出生年月日: 民國 78 年 10 月 10 日

籍貫: 高雄市

學歷: 國立交通大學電機資訊學士班 (2007.9-2011.6)

國立交通大學電子工程研究所 (2011.9-2012.8)

碩士論文題目:

共鍍銅鈦金屬在三維接合連線之電性分析及可靠度測量

Electrical Performance and Reliability Investigation of Co-sputtered Cu/Ti as 3D Bonded Interconnect