具場引效汲極的蕭特基能障薄膜電晶體之研製與特性分析

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摘要

蕭特基能障金氧半場效電晶體擁有較簡單且適用於低溫的製程。它同時也具有雙極性操作與短通道效應控制力。然而，嚴重的漏電流是它的缺點。如果該缺點能夠改善，則蕭特基能障金氧半場效電晶體的雙極性操作特性將使其製程與電路設計更具彈性。如果這種構想能夠用在薄膜電晶體，則蕭特基薄膜電晶體的低製程溫度與金屬化接面將使此一元件非常適用於主動式陣列液晶顯示器之製造。此外，金屬矽化物製程不但可以降低熱預算，亦可減少源極/汲極的寄生電阻。

在本論文中，我們成功的研發出一種新式具有金屬矽化物源極/汲極與場引效汲極的蕭特基能障薄膜電晶體。該結構在鈍化氧化層有一金屬 field-plate（或稱為副閘極），對其施以固定偏壓，以在金屬矽化汲極與元件主通道間引伸出一層載子作為補償通道。經由副閘極偏壓極性的轉換，則該元件即可展現雙極性操作特性。相較於傳統結構的蕭特基能障薄膜電晶體在關閉狀態時展現嚴重的閘極引致汲極漏電流，我們的新結構可以成功的將該漏電流抑制住。進而在 p-型與 n-型元件操作下提高開關電流比達 10^6。更甚者，因為不用離子佈植，與雙極性的展現，使得該製程能在極少的光罩數下就完成 CMOS 製程。上述特性使該元件特別適用於大面積的電子產品應用。

接著，我們利用實驗上的方式去分別分析傳統與新式元件的漏電流機制。結果顯示傳統元件的漏電流的活化能隨汲極和主閘極壓差的增加而下降。這暗示在汲極區的場發射隨電場增強而增強，並使類似 GIDL 的現象更強。相對的，具場引效汲極結構的元件的漏電活化能就和汲極和主閘極壓差的相關性甚低。因為其費米能階會因高副閘極電壓而靠近導電或價電帶，而使高電場區遠離汲極接面。所以熱離子發射將主導關閉狀態的漏電機制，進而抑制類似 GIDL 的漏電流。

為大幅提高元件特性，我們將準分子雷射結晶技術應用於元件上。因為薄膜特性之改善，開關電流比可提升至 10^8。我們發現對具有較高能障的 n-型元件而言，源極的載子穿透效應比熱離子發射佔有較重要的比重。以其優越的開關特性

和簡單化製程，使致這種新式結構確實適用於 AMLCD 和 SOP 應用。

在今日奈米等級元件的研製已是非常普及。我們發現蕭特基薄膜電晶體的特性可因縮減元件寬度至奈米等級而更獲改善。我們的結果顯示，儘管在 620℃ 直接沉積的複晶矽擁有高度的缺陷密度，元件仍能展現高開關電流比與低次臨限擺幅。顯然若將諸如準分子雷射結晶技術應運於複晶矽薄膜上，則類似 SOI 的元件表現將是很可以預期的。

最後，我們開發出一種可量得薄膜電晶體通道層之全能障內缺陷態位密度的新穎方法。在這種方法中，我們以場效應電導法的原理來求取態位密度。微分法與溫度法分別用以在蕭特基薄膜電晶體和傳統的離子佈植薄膜電晶體上。我們發現在同樣的通道材料上，不同的元件結構與方式都可以獲得良好的相似結果。這證明了這種新方式的可行性與可靠度。我們也分析了量測結果與元件結構的相依性，以獲適當的量測條件。我們發現只要有寄生電阻的出現，就容易高估缺陷密度的結果。若加以足夠高的汲極電壓，副閘極偏壓或較短的通道都可以減緩上述現象。此外，採用靠近能障中間的金屬矽化物材質如矽化鈷，將有助於分析的可靠性。

我們也分析了諸如再結晶法與電漿處理等製程步驟對缺陷態位密度的影響。使用這種新方法可完整真實反映出該製程的效應。而前述提及的具奈米級寬度通道的電晶體之良好閘極控制力亦可由缺陷密度之分析來獲得合理解釋。最後，我們證實元件的平帶電壓可由 p-型與 n-型元件之電流-閘極電壓特性圖曲線的交點來求得。這樣大大提昇了流程的簡單性，並且，從業界觀點而言可大幅降低成本，因為只要單一顆元件與室溫下的兩條特性曲線即可求出缺陷態位密度，其實用性不可言喻。

The Fabrication and Characterization of Schttoky Barrier Thin Film Transistor with Field-Induced-Drain

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Abstract

Schottky Barrier MOSFET is simpler in processing and inherently suitable for low temperature processing. It is also capable of ambipolar operation and short channel control. However, it suffers from deleterious off-state leakage current. If the shortcomings of SB-MOSFET could be improved, the inherent ambipolar property of SB-MOSFET will make fabrication process and circuit design more flexible. If the idea is applied to thin film transistors, the low process temperature of metallic junction formation will make SB-TFT compatible with middle temperature active matrix liquid crystal display (AMLCD) manufacture. In addition, salicidation process will not only reduce the thermal budget, but also decrease the source/drain parasitic resistance. This is quite appropriate for low temperature poly-Si application.

In this dissertation, a novel Schottky barrier thin-film transistor (SBTFT) with silicided source/drain and field-induced drain (FID) extension was proposed and demonstrated. In the new device configuration, a metal field-plate (or sub-gate) lying over the passivation oxide is employed to induce a sheet of carriers in a channel offset

region located between the silicided drain and the active channel region underneath the main-gate. The new device thus allows ambipolar device operation by simply switching the polarity of the bias applied to the field plate. In contrast to the conventional SBTFT that suffers from high GIDL (gate-induced drain leakage)-like off-state leakage current, the new SBTFT with FID is essentially free from the GIDL-like leakage current. In addition, unlike the conventional SBTFT that suffers from the low on/off current ratio, the new device exhibits high on/off current ratio of up to 10^6 for both *n*- and *p*-channel modes of operation. Moreover, the implantless feature and the ambipolar capability of the new device also result in extra low mask count for CMOS processes integration. These excellent device characteristics, coupled with its simple processing, make the new device very promising for future large-area electronic applications.

Second, we have experimentally investigated the conduction mechanisms of the off-state leakage current for Schottky Barrier TFTs with FID and conventional structure. The results show that the activation energy of the off-state leakage decreases significantly with increasing $|V_{GD}|$ for SBTFT with conventional structure. This indicates that field-emission conduction plays a major role as the field strength in the drain junction becomes high, and results in the strong GIDL-like phenomenon. In contrast, the activation energy of the off-state leakage shows only minor dependence on V_{GD} for SBTFT with FID. This is ascribed to the fact that the high-field region can be pulled away from the silicided drain for the FID structure. As a result, the field-emission conduction will be eliminated, and thus the GIDL-like leakage current can be effectively suppressed.

Next, SBTFT devices with ELA poly-Si active channel were successfully fabricated. Excellent device performance in terms of steep subthreshold slope and high on/off current

higher than 10^8 for both p- and n-channel operations are demonstrated, for the first time, on a single poly-Si TFT device. Source-side tunneling process is found to be important for device operation, especially for the n-channel operation that has a larger barrier height. The stellar performance with on/off current ratio larger than 10^8 for both n- and p-channel modes of operation, together with its inherent ambipolar capability, implantless process, silicided source/drain, low thermal budget, and simplified CMOS integration scheme, makes this kind of device a promising candidate for future AMLCD and SOP applications.

Applications of nano-scale device are very popular nowadays. We will show that the ambipolar performance of SB poly-Si TFTs can be improved by scaling the channel width into the nano-scale regime. Our results indicate that, despite the high trap density in poly-Si films, high on/off current ratio and small subthrehold swing can be achieved. It appears therefore possible to achieve SOI-like device characteristics if poly-Si film improvement methods, such as excimer laser annealing and metal-induced crystallization scheme, are adopted.

Finally, we proposed and successfully demonstrated a novel approach to obtain the full band-gap DOS in the channel of TFT devices. In this approach, the field-effect conductance method is performed on an SB poily-Si TFT which has the capability of ambipolar operation. Both incremental and temperature methods are adopted on the SB and conventional implanted devices to construct the relationship between DOS and the energy level in the gap. For devices with the same channel material, the results are in good agreement among the different extraction schemes, indicating the novel approach is very reliable.

We have also characterized the dependence of both electrical and structural parameters on the measurement results in order to set suitable test conditions. Our results indicate that the

parasitic resistance presenting in the channel would result in the overestimation of tail state density. A sufficiently high drain and sub-gate biases and short electrical junction length are thus needed. In addition, for reliable full band-gap DOS analysis, near-mid-gap silicide material like $CoSi_2$ is desirable.

In addition, the effect of process treatment like the re-crystallization and plasma hydrogenation steps on the DOS characteristics has also been characterized. Their impacts are clearly identified using the new approach. Benefits of using a nano-scale fin channel for promotion of the controllability of gate voltage over the channel potential is also clearly demonstrated.

Finally, we show that the flat-band voltage could be obtained by simply measuring the gate voltage at the intersection point of p- and n-mode I-V curves. The overall process is thus greatly simplified and cost-saving comparing to conventional approach, since only one device and two I-V measurements performed at room temperature are needed. We strongly believe that the novel method is extremely useful for practical applications.

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List of Symbols

E	Energy
d	Polysilicon thickness
E_F	Fermi energy
k	Boltzmann constant
n	Electron concentration
n_0	Equilibrium electron concentration
Ng(E)	Density of gap states (DOS)
q	Electronic charge
t_{ox}	Gate dielectric thickness
Xo	Unmodulated bulk length (or depletion width in the channel)
k	Boltzmann constant
T	Temperature (K)
V_{FB}	Flat band voltage
V_G	Gate voltage
Vth	Threshold voltage
ε_{ox}	Gate dielectric constant
ε_{si}	Silicon dielectric constant
μ	Electron mobility
ψ	band bending
ψs	surface band bending of the channel
ρ	charge density
G	conductance
G_0	conductance at flat band condition