Chapter 1

Introduction

1.1General Background

1.1.1 Schottky Barrier MOSFET

The phenomenal proliferation of integrated circuits in the past 40 years depends largely on the continuous scaling of MOSFETs. Reducing the gate length is essential to density increase per chip and performance improvement. However, process-related issues in shrinking the device size and the control of short-channel effects (SCE) have become major challenges, especially for the fabrication of 0.1 μm MOSFETs and beyond. In line with the above challenges, Schottky barrier (SB) MOS transistor is interesting and potentially promising. It was first proposed by Lepselter and Sze in 1968 [1]. By employing SB contacts for the source and drain, SB-MOSFETs possess both performance and fabrication advantages. The effective junction depth can be reduced to nil with Schottky contact, so SCE is minimized. SB-MOSFETs are therefore potentially suitable for nanometer technology node [2-8]. In addition, the high conductivity of the silicided contact also minimizes the series resistance [7-8]. In fact, several groups have recently proposed using Si SB-MOSFET with its superior scaling properties and ease of fabrication as a viable approach in relaxing the aforementioned constraints [9-10].

The Schottky-barrier structure is moe scalable because an extremely short channel can be achieved with the abrupt silicon/silicide interface. Since such device employs a silicide source/drain (S/D) instead of an implanted one, it features shallow junction depth, lower S/D series resistance and contact resistance, lower junction capacitance than conventional MOSFETs. Latch-up phenomenon is also eliminated in CMOS-like devices [11-12], thus reducing the floating body effect in silicon-on-insulator (SOI) devices [13], and avoiding process instabilities associated with the low-energy implant. Formation of silicide can be done at a low temperature while no post-implant annealing is necessary, it is thus very suitable for future low-temperature manufacturing [14-15]. The

SB devices fabricated on SOI substrates offer further improvement in performance over those fabricated on bulk Si wafers. In addition, it also offers a simpler process, better device isolation and lower parasitic capacitance, compared with the devices fabricated on bulk Si wafers. The reduced parasitic capacitance with SOI devices is conducive to a higher circuit operation and lower power consumption. For SOI CMOS inverter, the latch-up path is completely eliminated. From the viewpoint of ULSI product, SOI technologies are thus very attractive for future-high speed operation of CMOSEFTs [16]. Self-aligned silicide (salicide) technique has also been widely employed to improve the device performance by reducing the parasitic resistance in the gate and source/drain regions simultaneously.

Nevertheless, conventional SB MOSFETs suffer from a high off-state leakage current and poor on/off current ratio. This is manly due to the large gate-induced-drain-leakage (GIDL) in the Schottky junctions, compared with conventional p/n junction [17]. Accordingly, development of advanced structure and improvement in the process control are therefore very important to realize high-performance SB MOSFETs for ULSI applications.

1.1.2 Overview of Poly-Si Thin Film Transistor Channel Film

Polycrystalline silicon deposited by low-pressure chemical vapor deposition (LPCVD) technique is wildly used in modern very large scale integrated circuit (VLSI) [18-20]. The first polycrystalline silicon thin-film transistors (poly-Si TFTs) were fabricated by Fa et al [21] in 1966. Since then, electrical properties, conduction mechanism and fabrication process of polysilicon films were widely and extensively studied [22-25]. The development of technology in polycrystalline silicon thin film transistors (poly-Si TFTs) over the past decades has been stimulated by the rapid commercial development of active matrix-addressed flat-panel liquid-crystal displays (AMLCDs) [26-29]. Moreover, poly-Si TFTs also had been expending in applications to high-density static random access memories (SRAMs) [30-31] and 3-dimensional integrated circuit [32-33], etc.

AMLCD is one of the most promising candidates for realizing high-quality large-area flat panel

displays [34]. The first-generation AMLCDs relied predominantly on hydrogenated amorphous silicon (a-Si:H) TFTs for the pixel switching devices. A-Si:H TFTs can reduce the leakage current because of their high OFF-state resistivity, and they are also compatible with large glass substrates with low processing temperature [35]. Unfortunately, the extremely low electron field effect mobility (typically below 1 $cm^2/V*sec$) in a-Si:H TFTs limits their application in the switching elements (pixel) only. In order to reduce the cost and improve the circuit and system reliability, integrating the pixels with the driver circuits together on the same substrate is very desirable. Considering of this, using poly-Si TFTs to replace a-Si:H TFTs is a future and desirable trend. There are many advantages of poly-Si TFTs, such as superior carrier mobility, CMOS capability, lower photocurrent [29] and better device reliability [37]. These qualities enable the integration of peripheral circuits as well as the active-matrix switching elements on the same glass substrate. With such virtues, poly-Si TFTs have been extensively studied for applications to AMLCDs.

Most poly-Si TFTs with high carrier mobility were fabricated by processing temperature above 900℃ and required quartz-based substrates in the early days. However, for large-panel LCDs, quartz substrates are not economically competitive because of their much higher cost. Thus, low temperature fabrication process with the use of glass substrates and low-temperature high-mobility poly-TFTs were investigated [38-39].

In addition to AMLCDs, recently poly-Si TFTs are extensively used in organic electroluminescence (OEL) display [40-41]. Similar to LCDs, low temperature processes and high mobility of poly-Si TFTs are essential for low cost and high performance of OEL display.

1.1.2.1 Solid-Phase Crystallization of Amorphous Silicon

Because of the temperature constraint for glass substrate, low temperature process (LTP) must be performed. Besides, grain boundaries and intragranular defects greatly deteriorate the performance of poly-Si TFTs [42-43]. Taking into consideration of both factors, increasing the grain size of poly-Si films in low-temperature process is the only promosing approach. Here, we will only introduce two silicon film crystallization methods, which are adopted in this thesis. One of the common methods of

preparing poly-Si films is solid-phase crystallization (SPC) of amorphous Si films at 600℃ for 20-48 hours [44]. The grain size obtained by solid-phase crystallization (SPC) of a-Si is larger by several times and has smoother surface morphology than those of as-deposited poly-Si films. Early works showed that larger fine grain size resulted in a higher electron field effect mobility. TFTs fabricated by SPC method can show better performance.

Traditionally, silicon deposition in LPCVD reactors is performed at a temperature around 550℃ using SiH_4 gas, followed by SPC at 600℃. An alternative to the silane-based LPCVD a-Si material is the use of disilane (Si_2H_6) which was recently studied [44-45]. It was reported that poly-Si films with larger grains can be obtained at a lower deposition temperature while enjoying a higher deposition rate. Under such conditions, the nucleation rate during annealing is low and therefore grains can grow to a larger size [44].

The structure of crystallized silicon film is closely related to the structural disorder of the initial material. By increasing the initial disorder of the silicon network, a significant enlargement of the grain size of the crystallized film can be achieved. The deposition rate for a-Si films might also affect a-Si structural disorder. With a high deposition rate for a-Si films, the high influx density suppresses the surface migration. Films deposited at a high deposition rate have a wide range of bond lengths and bond angles. On the other hand, with a low deposition rate, the low influx density enhances the surface migration. Films deposited at a low deposition rate therefore do not have such a wide range of bond lengths and bond angles. When the deposition temperature is higher, the surface migration due to the increase in the deposition temperature is more prominent than the increase in the structural disorder of Si network due to increased deposition rate. On the other hand, when the deposition temperature is lower, the surface migration due to decreased deposition rate is more prominent than the enhancement in the structural disorder of Si network due to decreased deposition temperature. Therefore, the disorder of the underlying silicon network can be increased by using low deposition temperature and high deposition rate. Disilane has been shown to depict high deposition rate compared with SiH_4 (which is usually deposited above 530℃) even at temperature below 500℃.

After SPC, larger grain poly-Si films can be obtained by using disilane as gas precursor compared with silane.

1.1.2.2 Crystallization by Excimer Laser Annealing

Although SPC method can enlarge the grain size of poly-Si film, intragranular defects are still abundant in poly-Si film. Recently, a novel technology, i.e., excimer laser annealing (ELA), was developed. The standard gas mixtures and output wavelengths are ArF (193 nm), KrF (248nm) and XeCl (308nm). These are all short-duration pulsed lasers (10-30ns) operating in the ultraviolet waveband, and have been found to be well suitable to the crystallization of silicon on glass substrate. This is because the optical absorption depth, at these wavelengths, in amorphous silicon, is about 6 nm, so the radiation is strongly absorbed in the silicon surface and can readily cause melting, whilst the short pulse duration results in a correspondingly small heat diffusion length of ~100nm in the silicon itself and ~200nm in films of SiO_2 [46] which can be used to cap the glass substrate and thereby protect it from excessive temperature excursions. Measurements and calculations [47] have demonstrated that with suitable SiO_2 film capping the temperature of the underlying glass surface can be kept below ~400℃.

ELA method is a very promising technology for two reasons. First, it is still a low temperature process, so glass substrate will not be damaged. Second, it can crystallize the film selectivity by partially irradiating the film surface, so both poly-Si TFTs and amorphous TFTs can be formed on the same substrate [48-49]. The laser beam melts the silicon thin film in a very short time (usually tens of nanoseconds), which makes the silicon film melt and crystallize without significantly heating the glass substrate. Most important of all, by this melting and recrystallizing process, significantly high filed effect mobility can be achieved. These mobility values are greater than those obtained by solid-phase crystallization of a-Si. The obvious improvement is believed to result from the difference in grain quality between the two processes. The laser-crystallized material has few lines or plane defects within the grain, whereas the SPC material consists of large dendritic grains which are rich in integration defects such as twins, microtwins, stacking faults, etc.

1.1.3 Development of SOI FinFETs

As the complementary metal-oxide-semiconductor (CMOS) transistor' feature size is scaled down to below 0.1 um, the challenges to overcome the short channel effect (SCE) and dopant fluctation effect become more and more difficult [50]. To relax these constraints, some advanced structures, such as FinFETs [51-54], ultra-thin body SOI [55], and silicided source/drain SOI [56], have been proposed.

Specifically, FinFETs belong to the family of double-gate (DG) silicon-on-insulator (SOI) transistors, in which two gates are employed to control the channel carrier charges. FinFETs thus exhibit attractive advantages in comparison with the conventional bulk MOS or single-gate SOI counterparts. The device displays high transconductance, nearly-ideal subthreshold swing, improved current drive capability, and lower direct-tunneling gate leakage current. Moreover, the double-gate structure provides better controllability of the drain electrostatic field lines, thus minimizes drain-induced barrier lowering (DIBL) and threshold variation with channel length [57]~[61]. As a result, DG MOSFET offers the potential for scaling the channel length down to 10 nm node [59][62].

Since the channel doping concentration in bulk MOSFETs needs to be increased to alleviate the short channel effects when the device dimension is scaled down. For a device with gate length of less than 0.1 um, the required channel concentration is higher than 10^{18} cm-3 [63]. Such a high doping concentration would degrade device performance in terms of reduced mobility and increased junction capacitance. Because of the inherent robustness to the short channel effects, and the feasibility of threshold voltage adjustment by using metal-gate with suitable work function [2][12], the DG MOSFET device could be built with an un-doped channel. All of the aforementioned features highlight the important role of the DG SOI in the nano-scale era.

Nevertheless, most approaches proposed for the DG SOI are very difficult in fabrication. From the view point of state-of-art manufacturing, FinFET [51] is the most promising since it allows the formation of the "front" and "backside" gates simultaneously, and is much simpler than the costly wafer bonding processes.

Particular attention is called for on the parasitic series resistance in the source/drain regions of SOI FinFET devices, since it would increase significantly as the fin width is scaled down. A folded-channel with non-planar raised source/drain to reduce the resistance has been demonstrated for improving the performance of FinFETs [51], but it requires a very complex and difficult fabrication process. Quasi-planar FinFETs using simpler process and lower gate-to-drain capacitance was subsequently proposed [65]. The fan-out source/drain pattern was designed to minimize the proximity problem of lithography and shrink the source/drain space as short as possible. This improvement was demonstrated to yield devices with excellent current drive and minimal short-channel effects down to 50-nm gate length.

Another approach for reducing the source/drain series resistance is to employ the salicide materials. The popular self-aligned silicidation (salicide) technique has been widely applied to conventional bulk MOS devices since gate length falls below 0.3 um [66]. For nano-scale FinFET device, Schottky barrier source/drain formed by low-resistivity silicide represents a promising alternative to the heavily doped source/drain due to the low S/D series resistance and simpler fabrication process. The superior controllability in short-channel effect, owing to the inherently sharp silicon/silicide interface, is another merit for adopting Schottky junction in nano device applications [67]. The advantage of using metallic Source/Drain has been explained in Section 1.1.1. This approach will be addressed in more detail in the next section.

1.2 Motivation of This Study

As mentioned in the last section, Schottky Barrier MOSFET is simpler in processing and inherently suitable for low temperature processing. When microelectronics enters the deep sub-micron technology node, traditional CMOS process becomes extremely complicated. Besides, it is more and more difficult to control the short channel effect of conventional MOSFET. If the shortcomings of SB-MOSFET mentioned above could be improved, the ambipolar operation capability and simple process make SB-MOSFET device a good candidate to replace sub-micron CMOS process. We can

simply assign the operation mode of SB-MOSFET by appropriate bias. The inherent ambipolar property of SB-MOSFET makes fabrication process and circuit design more flexible. If the idea is applied on thin film transistors, the low process temperature of metallic junction formation makes SB-TFT compatible with middle temperature active matrix liquid crystal display (AMLCD) manufacture. In addition, salicidation process will not only reduce the thermal budget, but also decrease the source/drain parasitic resistance. This is quite appropriate for low temperature poly-Si application.

In order to investigate the possibility of previously mentioned idea, we have proposed and successfully demonstrated a novel SBTFT structure, which overcomes the disadvantages of conventional SB-MOSFET and reduces the thermal budget of poly-Si TFT process. This structure features a top field plate over the passivation oxide, which is employed to induce a drain-side electron extension, i.e., field induced drain (FID), and to modulate the drain side electrical field. With proper bias, the off-state leakage current can be suppressed. In this study, we will try to explain leakage current mechanisms by different channel preparation methods. Then we explore the application of SBTFT to FINFET structure. Finally, we will use the "field effect conductance" method to analyze the full band-gap density of states (DOS) distribution in poly-Si channel, which also provides a convenient way for defect analysis.

1.3 Thesis Organization

The dissertation is divided into seven chapters.

In Chapter 1, the backgrounds and motivations of the thesis are reviewed.

In Chapter 2, a novel Schottky-barrier metal-oxide-semiconductor thin-film transistor (SBTFT) is successfully demonstrated and characterized. The new SBTFT device features a field-induced-drain (FID) region, which is controlled by a metal field-plate lying on top of the passivation oxide. The FID region is sandwiched between the silicided drain and the active channel region. Carrier types and the conductivity of the transistor are controlled by the metal field-plate. The device is thus capable of ambipolar operation. Excellent ambipolar performance with on/off current ratios over 10^6 for both *p*-

and *n*-channel operations is realized simultaneously on the same device fabricated with polysilicon active layer. Moreover, the off-state leakage current shows very weak dependence on the gate-to-drain voltage difference with the FID structure. Finally, the effects of FID length are also explored.

In Chapter 3, detailed conduction mechanisms in a conventional Schottky barrier thin-film transistor (SBTFT) and the novel SBTFT with field-induced drain (FID) extension described in Chapter 2 are studied in this chapter. The new SBTFT device with FID extension shows excellent ambipolar performance with effective suppression of gate-induced drain leakage (GIDL)-like off-state leakage that plagues conventional SBTFT devices. By characterizing the activation energy of the conduction process in the off-state for conventional SBTFT devices, it is suggested that field emission of carriers from the drain junction is the major conduction mechanism. While for the new FID SBTFT devices, owing to the effect of Fermi level pinning in the FID region, thermionic emission rather than field emission becomes the dominant conduction mechanism, resulting in the effective suppression of the undesirable GIDL-like leakage current.

In Chapter 4, we investigate and compare the characteristics of poly-Si SB TFTs with channel layer prepared by excimer laser crystallization (ELA) and solid-phase crystallization (SPC). It is shown that the use of ELA greatly improves the device characteristics, comparing with the SPC counterparts. Excellent device performance, with steep subthreshold slope and on/off current ratio higher than 10^8 for both p- and n-channel operations, is demonstrated on a single device with ELA channel. The effects of sub-gate bias, channel length, and channel offset length on device characteristics are also explored. In addition, we also carry out further study on characterizing the off-state current at different temperatures in order to clarify the leakage conduction mechanisms. The thermionic emission is found to be dominating the off-state current.

In Chapter 5, we propose and demonstrate SB poly-Si TFT device with nano-scale fin-like channel. The fin-like channel, which is consisted of as-deposited LPCVD poly-Si material, is surrounded on three sides by the main-gate, forming the “tri-gate” configuration. The use of nano-scale poly-Si channel allows a stronger control of the channel potential by the gate bias, and

better subthreshold characteristics over the planar SB TFTs. The fabricated devices indeed exhibit stellar ambipolar device performance in terms of high on/off current ratio and sharp subthreshold swing.

In Chapter 6, we propose a novel method to extract full band-gap density-of-state (DOS) in the channel layer of a thin-film transistor (TFT). In this new approach, only a single Schottky barrier thin-film transistor (SB-TFT) device is needed, in contrast to the conventional methods that require both n- and p- channel devices, for characterization. Field-effect conductance (FEC) method is applied to analyze the ambipolar subthreshold current-voltage characteristics and acquire full band-gap DOS. Experimentally, we have also observed that the gate voltage at the intersection point of n- and p-channel subthreshold current-voltage characteristics coincides well with the flat-band voltage measured using the conventional temperature method. We thus propose to exploit this new finding, in lieu of the conventional method, to extract the flat-band voltage, which further simplify our methodology, as only two current-voltage measurements at room temperature are needed for the construction of full band-gap DOS. Our proposed method has been demonstrated to be useful on characterizing and understanding the impacts of different process treatments on the device characteristics. Accompanied with its simplicity and significant saving of both analysis cost and time, this method could be vital to TFT device modeling and circuit simulation works for both R&D and practical manufacturing.

In Chapter 7, we conclude with summary of the experimental results. Recommendations for future research are also given.

References :

[1] M. P. Lepselter, and S. M. Sze, “SB-IGFET: An Insulated-Gate Field-Effect Transistor Using Schottky Barrier Contacts as Source and Drain,” *Proc. IEEE,* 56, p.1088, 1968.

[2] C. Wang, J. P. Synder, and J.R. Tucker, “Sub-40nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistors,” *Appl. Phys. Lett.*, vol. 74, p.1174, 1999.

[3] J. R. Tucker, “Schottky barrier MOSFETs for silicon nanoelectronics,” *WOFE’97 Proceedings., Frontiers in electronics*, p.97, 1997.

[4] Q. Z. Zhao, F. Klinkhammer, M. Dolle, L. Kappius, S. Mantl, “A novel silicide nanopatterning method for the fabrication of ultra-short channel Schottky-tunneling MOSFET’s,” *Microelec. Engineering*, vol.50, p.133, 2000.

[5] C. K. Huang, W. E. Zhang, and C. H. Yang, “Two-dimensional numerical simulation of Schottky barrier MOSFET with channel length to 10nm,” *IEEE Trans. Electron Devices*, vol.45 p.842, 1998.

[6] B. Winstead and U. Ravaioli, “Simulation of Schottky barrier MOSFET’s with a coupled quantum injection/Monte Carlo Technique,” *IEEE Trans. Electron Devic*es, vol.47, p.1241, 2000.

[7] W. Saitoh, A. Itoh, S. Yamagami and M. Asada, “ Analysis of short-channel Schottky source/drain metal-oxide-semiconductor field-effect-transistor on Silicon-on-insulator substrate and demonstration of sub-50-nm n-type devices with metal gate,” *Jpn. J. Appl. Phys.*, vol. 38, p.6226, 1999.

[8] J. Kedzierski, P. Xuan, E. H. Anderson, J. Boker, T. J. King, and C. Hu, “Complementary silicide source/drain thin-body MOSFETs for the 20 nm gate length regime,” in *IEDM Tech. Dig.*, p.57, 2000.

[9] J. R. Tucker, C. Wang, and S. Carney, “Silicon field-effect transistor based on quantum tunneling,” Appl. Phys. Lett., vol. 65, p.618, 1994.

[10] J.P. Snyder, C.R. Helms and Y.Nishi, “ Experimental investigarion of a PtSi source and drain

field emission transistor ”, Appl. Phys. Lett., vol. 67, p1420, 1995

[11] M. Sugino, L.A. Akers, and N.E. Rebeschini, “ CMOS latch-up elimination using Schottky barrier PMOS”, in IEDM Tech. Dig., p.462, 1982”

[12] M. Sugino, L.A. Akers, and N.E. Rebeschini, “Latch-up-free Schottky barrier CMOS”, in IEEE Trans. Electron Devices, vol.30 , p.110, 1983.

[13] M. Nishisaka and T. Asano, ‘ Reduction of the floating body effect in SOI MOSFETs by using Schottky Source/Drain contacts’, Jpn. J. Appl. Phys., vol.37, 1998, pp.1295

[14] H. C. Lin, C. Y. Lin, K. L. Yeh, R. G. Huang, M. F. Wang, C. M. Yu, T. Y. Huang, and S. M. Sze, “A novel implantless MOS thin-film Transistor with simple processing, excellent performance and ambipolar operation capability”, in *IEDM Tech. Dig.* , 2000, pp.857-859..

[15] A. Itoh, M. Saitoh, and M. Asada, “Very short channel metal-gate Schottky source/drain SOI-POSFET and their short channel effect”, in *Proc. Device Res. Conf. (DRC)*, pp.77-78, 2000

[16] J. P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, 2nd ed. Norwell, MA:Kluwer,1997

[17] L. E. Calvet, H. Luebben, and M. A. Ree, “ Suppression of leakage current in Schottky barrier metal-oxide-semiconductor field-effect transistors ” , J. Appl. Phys., vol 91, pp.757-759, 2002

[18] Ichio Yudasaka and Hiroyuki Ohshima, “polysilicon thin film transistor,” Mat. Res. Soc. Symp. Proc., vol. 182, 1990.

[19] S. Wolf and R. N. Taauber, “Silicon processing for the VLSI Era,” Lattice Press, California, vol.1, chap.6, p.161, 1986.

[20] S.D. Brotherton, “Polycrystalline silicon thin film transistors,” Semicond. Sci. Technol., 10, 1995.

[21] C.H. Fa and T.T. Jew, “The polysilicon insulated-gate field-effect transistors,” IEEE Trans. Electron Devices, vol.13,no.2,p.290, 1966.

[22] T.I. Kamins, “Hall mobility in chemical deposited polycrystalline silicon,” J. Appl. Phys., vol.42, p.4357, 1971.

[23] G. Baccarani, B. Ricco and G. Spadin, “Transport properties of polycrystalline silicon films,” J. Appl. Phys., vol.49,p.5565, 1978.

[24] I-Wei Wu, Alan G. Lewis, Tiao-Yuan Huang, Warren B. Jackson and Anne Chiang, “Mechanism and device-to-device variation of leakage current in polysilicon thin film transistors,” IEDM 90, pp867-870.

[25] C. F. Yeh, T.Z. Yang, C. L. Chen, T. J. Chen and Y. C. Yang, “Experimental comparison of off-state current between high-temperature- and low-temperature-processed undoped channel polysilicon thin-film transistors,” Jpn. J. Appl. Phys., vol.32, 1993, pp.4472-4478.

[26] J. Ohwada, M. Takabatake, Y. a. Ono, A. Mimura, K. Ono and N. Konish, IEEE Trans. Electron Devices, vol.36, no.9, p.1923, 1989.

[27] A. G. Lewis, David D. Lee and R. H. Bruce, “Polysilicon TFT circuit design and performance,” IEEE J. Solid-State Circuit, vol.27, no.12, p.1833, 1992.

[28] T. Morita, Y. Yamamoto, M. Itoh, H. Yoneda, Y. Yamane, S. Tsuchimoto, F. Funadda and K. Awane, “VGA driving with low temperature processed poly-Si TFTs,” IEDM tech. Dig. p.841, 1995.

[29] M. J. Edwards, S. D. Brotherton, J. R. Ayres, D. J. McCulloch and J. P. Gowers, “Laser crystallized poly-Si circuits for AMLCDs,” Asia Display, p.335, 1995.

[30] S.D.S. Malhi, H. Shichijo, S. K. Ganerjee, R. Sundaresan, M. Elehy, G. P. Pollack, W. F. Richardson, A. H. Shah, L. R. Hite, R. H. Womack, P. K. Chatterjee, and H. W. Lam, IEEE Trans, Electron Device, vol.32, p.258, 1985.

[31] M. Kiungawa, M. Kakumu, T. Yoshida, T. Nagayama, S. Morita, K. Kubota, F. Matsuoka, H. Oyamatus, K. Ochiii and K. Maeguchi, “TFT cell technology for 4 Mbit and more high density SRAMs,” 1990 Symp. On VLSI Tech., p23.

[32] K. Y. Lee, Y. K. Fang, C. W. Chen, K. C. Huang, M.S, Liang and S. G. Wuu, “To suppress UV damage on the subthreshold characteristics of TFT during hydrogenation for high density TFT SRAM,” IEEE Electron Device Lett., vol.18, no.1, pp.4-6, 1997.

[33] N. D. Toung, G. Harkin, R. M. Bunn, D. J. McCulloch and I. D. French, “The fabrication and characterization of EEPROM arrays on glass using a low-temperature poly-Si TFT process,” IEEE Electron Device Lett., vol.43, no.11m pp.1930-1935, 1996.

[34] P. Migliorate, “Progress in active matrix addressing of LCDs,” in Proc. Int. display Res. Conf., 1987, p.44.

[35] T. Tsukada. “Amorphous Silicon TFTs and flat panel displays,” Materials Res. Soc. Sympo. Proc., vol.,424 (Flat Panel Display Materials II)pp3-8, 1997

[36] Tadashi Serikawa, Seiiti Shirai, Akio Okamoto and Shiro Suyama, “Low temperature fabrication of high-mobility poly-Si TFTs for large area LCDs,” IEEE Transaction on electron devices, vol.36, no.9, pp.1929-1933, 1989.

[37] J. R. Ayres and N. D. Young, “Hot carrier effects in device and circuits formed from poly-Si,” IEEE Proc. Circuit Device Syst., vol.141, no.1, p.38, 1994.

[38] C. F. Yeh, C. L. Chen, Y. C. Yang, S. S. Lin, T. Z. Yang and T. Y. Hong, “Low-temperature-processed poly-Si thin-film transistors using solid-phase-crystallization and liquid-phase-deposited gate oxide,” Jpn. J. Appl. Phys., vol.33, pp. 1798-1802, 1994.

[39] H. Y. Lin, C. Y. Chang, T. F. Lei, M. Liu, W. L. Yang, J. Y. cheng, H. C. Tseng and L. P. Chen, “Low-temperature and low thermal budget fabrication of polycrystalline silicon thin-film transistors,” IEEE Electron Device Lett., vol.17, no.11, pp.503-505, November 1996.

[40] M. Stewart, L. Pires, R. Howell, M. Hatalis, O. Prache, W. Howard, “Polysilicon VGA Active Matrix OLED Display-Technology and performance,” IEDM Proceedings p.871, 1998.

[41] R. M. A. Dawson et al. “Design of an improved Pixel for a Polysilicon Active Matrix Organic EL Display,” SID Digest 4.2, 1998.

[42] Shunji Seki, Osamu Kogure and Bunjiro Tsujiyama, “Effects of crystallization on trap state densities at grain boundaries in polycrystalline silicon,” IEEE Electron Device Lett., vol.8, no.8, August 1987, p.368-370.

[43] T. J. King, M. G. Hack and I-Wei Wu, “Effective density-of-states distributions for accurate

modeling of polycrystallization-silicon thin-film transistors," J. Appl. Phys., vol.75, no.2, 15 January 1994, p.908-913.

[44] K. Nakazama, "Recrystallization of amorphous silicon films deposited by low-pressure chemical vapor deposition from Si_2H_6 gas," J. Appl. Phys. Vol.69, pp.1703, 1991.

[45] T. Vouttsas and M. K. Hatalis, "Deposition and crystallization of a-Si low-pressure chemical vapor deposited films obtained by low-temperature pyrolysis of disiline," J. Electronchem. Soc., vol.140, pp.871-877, 1993.

[46] Incropera F. P. and de Witt D. P. "Fundamentals of heat transfer," New York: Wiley, 1983.

[47] Fogarassy E., Pattyn H., Elliq M., Slaoui A., Prevot B., Stuck R., de Unamuno S., and Mathu E. L., Appl. Surf. Sci., 69,231,1993.

[48] K. Sera, F. Okumura, H. Uchida, S. Itoh and K. Hotta, "High performance TFTs fabricated by XeCl excimer laser annealing of hydrogenated amorphous-silicon film," IEEE Trans, Electron Device, vol.36, pp.2868-2872, 1989.

[49] K. Shimizu, O. Sugiura and M. Matsumura, "On-ship bottom-gate polysilicon and amorphous silicon thin-film transistors using excimer laser annealing," Japan J. Appl. Phys., vol.29, pp.L1775-L1777, 1990.

[50] H.S. Wong, D.J. Frank, and J.M.C. Stork, "Design and Performance considerations for sub-0.1um double-gate SOI MOSFET," in IEDM Tech. Dig., 1994, pp.747-750.

[51] D.Hisamoto, W.C. Lee, and J.Kedzier et al., "A Folded-channel MOSFET for Deep-sub-tenth Micron Era", IEDM Tech. Dig., pp. 1032-1034, 1998.

[52] D. Hisamoto, W.C. Lee, J. Kedzierski, H. Takezuhci, K. Asano, c. Kuo, E. Anderson, T.J. King, J. Boker, and C. Hu, "FinFET-A self-aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Trans Electron Device, vol.47, p.2320, 2000.

[53] X. Huang, et al., "Sub-50 nm P-Channel FinFET," IEEE Trans. Electron Device, vol.48, p.880, 2001.

[54] Y. K. Choi, T.J. King, and C. Hu, "A Spacer Patterning Techonology for Nanoscale CMOS,"

IEEE Electron Device Lett., vol.49, p.436, 2002.

[55] H-S.P. wong, D. J. Frank, and P. Solomon, “Device Design consideration for Double-gate, Ground-Plane, and Single-gated Ultra-Thin SsOI MOSFET’s at the 25 nm Channel Length Generation,” in IEDM Tech. Dig., p.407, 1998.

[56] J.Kedzierski, P. Xuan and E. H. Anderson et al., “Complementary silicon source/drain thin-body MOSFETs for the 20nm gate length regime”, IEDM Tech. Dig., pp.57-60, 2000.

[57] S.-I. Takagi, J.Koga and A. Toriumi. “Subband Structure Engineering for Performance Enhancement of Si MOSFETs”, IEDM Tech. Dig., pp. 219-222, 1997.

[58] H.-S.P.Wong, D.J.Frank, and P.M.Ssolmon, “Device Design Considerations for Double-Gate, Ground-Plane,and Single-Gate Ultra-Thin SOI MOSFET’s at the 25nm Channel Length Generation”, IEDM Tech. Dig., pp.407-410,1998.

[59] L.Chang, S.Tang and T.-J.King et al.,”Gate Length Scaling and Threshold Voltage Control of Double-Gate MOSFETs”, IEDM Tech. Dig., pp.719-722, 2000.

[60] B.Majkusiak, T.Janik and J.Walczak, “Semiconductor Thickness Effects in the Double-Gate SOI MOSFET”, IEEE Trans. Electron Devices, Vol. 45, pp.1127-1134, May1998.

[61] L.Chang, K.J.Yang and Y.-C Yeo et al., “Reduction of Direct-Tunneling Gate Leakage Current in Double-Gate and Ultra-Thin Body MOSFETs”, IEDM Tech. Dig.,2001.

[62] X.Huang, W.-C Lee and C.Kuo et al., “Sub 50-nm FinFET:PMOS”, IEDM Tech. Dig., pp.67-70, 1999.

[63] R.-H.Yan, A.Ourmazd and K.F.Lee, “Scaling the Si MOSFET:From Bulk to SOI to Bulk”, IEEE Trans. Electron Devices, Vol. 39,pp.1704-1710,July 1992.

[64] Y.-K Choi, D.Ha and T.-J King et al., “Ultra-Thin Body PMOSFETs with Selectively Deposited Ge Source/Drain”, Symposium on VLSI Tach.,pp.19-20,2001.

[65] N.Lindert, L.Chang and Y.-K.Choi et a;., “Sub-60-nm Quasi-Planar FinFETs Fabricated Using a Simplified Process”, IEEE Electron Device Letters, Vol.22,pp.487-489,Oct.2001.

[66] T.Ohguro, M.Saito and Morifuji et al., “Thermal Stability of CoSi2 Film for CMOS Scalicide”,

IEEE Trans. Electron Devices, Vol. 47,pp.2208-2213,Nov.2000.

[67] C.Wang, J.P.Snyder and J.R.Tucker, “Sub-40nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistor”, Applied Physics Letters, Vol.74,pp.1174-1176,Feb.1999.

Chapter 2

General Fabrication, Operation and Characteristics of Ambipolar Schottky-Barrier Thin-Film Transistors (SBTFT)

2.1 Introduction

Schottky barrier (SB) MOS transistor, which employs metallic source and drain [1], eliminates the source/drain implantation and subsequent annealing steps. It is therefore simpler in processing and inherently suitable for low temperature processing. It is also excellent in short-channel effect control, due to the inherently shallow silicide junction [2-3]. Moreover, it is also capable of bi-channel operation [4]. With these advantages, it thus appears to be quite attractive for applications to nano-scale devices as well as large-area electronics.

Conventionally, SB MOS devices employ a self-aligned silicidation (salicide) process to form the silicided S/D. Gate sidewall spacers are required to avoid bridging between the gate electrode and the silicided S/D [1-7]. However, the resultant SB MOS transistors generally suffer from severe leakage current and poor on/off current ratio. This is due to the much larger junction leakage current inherent in Schottky diodes, compared with p-n junction diodes. Another shortcoming is that it is almost impossible to fabricate SB MOS transistors with acceptable *n*- and *p*-channel characteristics simultaneously for ambipolar operation [4]. This is due to the constraint imposed by the fixed barrier height of the Schottky contact of a given metallic layer.

In this work, we have demonstrated a novel poly-Si Schottky barrier thin-film transistor (SBTFT) device that can effectively improve the on/off current [8]-[11]. The new device employs a field-plate (or sub-gate) to induce an electrical drain extension in the active poly-Si layer. The unique field-induced drain (FID) feature reduces the off-state leakage effectively while maintaining a reasonable on-current value, resulting in significant improvement in the device performance. Excellent ambipolar operations are demonstrated, for the first time, on the same SBTFT with FID structure.

2.2 Device Fabrication and Structures

The cross section figures of conventional and proposed FID SB-TFTs are depicted in Fig.2.1 (a) and (b). We discuss the process in brief. First, we grew a thick thermal oxide layer (200 nm) on the starting wafer to serve as the glass-like substrate used in AMLCDs. An amorphous silicon channel layer (50 nm) was then deposited at 550 ℃ by LPCVD system. To enlarge the grain size, the amorphous silicon layer was then subsequently transformed into polycrystalline phase by solid phase crystallization (SPC) at 600 ℃ in N_2 ambient for 24 hours. After defining active device area, LPTEOS gate oxide layer (20 nm) and poly-Si layer (200 nm) were deposited sequentially. The poly-Si layer was doped by arsenic ion implantation. The n^+ dopant was active at 600 ℃ in N_2 ambient for 24 hours. The n^+ poly-Si layer was then patterned as the main-gate. Next, another LPTEOS oxide layer (200 nm) was deposited as spacer layer. Additional lithographic step was needed to define the offset region of the novel SB-TFTs (Fig. 2.1(b)). By anisotropic etching step, offset region of novel SB-TFTs and self-aligned spacer of conventional SB-TFTs were formed simultaneously (Fig. 2.1(a)). Such spacer layers could prevent bridging between source/drain and main-gate during silicidation.

The source/drain region was formed by self-aligned silicidation step instead of ion implantation. Thin Co (15 nm) and TiN (30 nm) layers were sputtered on the entire wafer, followed by rapid thermal annealing at 550 ℃ for 30 sec. Only the bare source/drain region was silicided. After removing the non-reacted metal by selective wet etching (H_2SO_4:H_2O_2 = 3:1 for 10 min at 120 ℃), the self-aligned Schottky source/drain junction was formed. Passivation PETEOS oxide (300 nm) and contact pad formation were subsequently performed. Finally, NH_3 plasma treatment (1 hr at 250 ℃) was used to reduce the dangling bonds. The overall mask counts for fabricating the proposed SB-TFTs are only five in number. The number could be reduced to four for conventional SB-TFTs.

There are a few points worthy of note. First, no extra lithographic step is required to define the sub-gate of our novel structure since it can be formed simultaneously with regular contact pad patterning step. Second, the implantless fabrication saves additional lithographic step, costly ion

implantation, and the accompanying long term annealing process. Third, all the process temperatures mentioned above are kept below 600 ℃, making it compatible with mid-temperature AMLCD fabrication. Fourth, the poly-Si channel layer is thin enough to reduce leakage current. Finally, the bottom width of spacer (either self-aligned spacer or offset spacer) is designed so that the silicided source/drain junction will not reach the channel region under the main-gate.

2.3 Operation of SBTFT With Field-Induced Drain

The new structure (Fig. 2.1(b)) features an undoped Si active channel, a top metal field-plate (i.e., the sub-gate), and Schottky source/drain. For device operation, a fixed bias is applied to the sub-gate to form a field-induced drain (FID) extension under the sub-gate region. So depending on the sub-gate bias polarity, the device can function as either an n-channel transistor with positive sub-gate bia or a p-channel transistor with negative sub-gate bias.

The new device is structurally similar to conventional SB MOSFETs [1]~[7], except that a field-induced drain extension is created between the channel and the Schottky drain. The field-induced drain extension serves to reduce the undesirable off-state leakage that has plagued all previous SB MOSFETs. Concomitantly, the new device can also be viewed as MOSFETs with FID [12][13], with the exception that the heavily-doped source/drain region is now replaced by Schottky source/drain. The new structure thus retains all the advantages of FID such as low off-state leakage and low junction leakage. Finally, the use of Schottky source/drain can greatly reduce processing steps (i.e., implant and subsequent annealing), and allows ambipolar operation, which further simplifies CMOS process integration.

2.4 Results and Discussion

2.4.1 Characteristics of Ambipolar Operation

Figure 2.2 depicts the ambipolar operation of the FID SBTFT [8]. Excellent on/off current ratios of over 10^6 are achieved for both *n*- and *p*-channel operations under proper bias conditions. It is interesting to note here that the turn-on behavior is somewhat retained for *n*-channel operation even when a zero sub-gate bias is applied. Meanwhile, the off-state leakage in p-channel operation is higher

for sub-gate bias of zero volt than that of –50 V. These phenomena will be addressed later.

Figures 2.3 compares the ambipolar (i.e., both *n*- and *p*-channel) subthreshold characteristics of the conventional and FID SBTFTs. It can be seen that SBTFT with conventional structure exhibits very poor performance for both *p*- and *n*-channel modes of operation (Fig. 2.3(a)). On/off current ratios are around or less than 10^3. Moreover, the strong GIDL (gate-induced drain leakage)-like leakage current results in the V-shaped current-voltage curves. In contrast, superior *p*- and *n*-channel device performances are simultaneously realized on the SBTFT with FID structure under proper sub-gate biases. As shown in Fig. 2.3(b), on/off current ratio as high as 10^6 is observed for both *n*- and *p*-channel modes of operation. In addition, the GIDL-like leakage current is effectively suppressed. It should be emphasized that these characteristics are obtained on the same device by simply changing the polarity of the sub-gate bias.

Output characteristics of the two types of devices are shown in Fig. 2.4. It is seen that the implementation of FID in the device improves the on-state current for both *p*- and *n*-channel operations. The improvements can be ascribed to the elimination of the un-gated channel region existing under the sidewall spacer in the conventional devices. Since the bottom width of the sidewall spacer (~ 150 nm) is larger than the silicide thickness (~ 55 nm), the silicided source/drain portion does not reach the channel region beneath the main-gate, leading to an increase in the parasitic resistance along the channel in the conventional device. This feature is quite different from that of SB MOS devices reported previously [4]-[7], in which the silicided source/drain region overlaps with the gate. Although a self-aligned sidewall spacer also exists at the source side of our new device, however, the overlying metal sub-gate effectively covers the channel region underneath the spacer, so the parasitic resistance is reduced when a high sub-gate bias is applied.

2.4.2 Leakage Mechanisms

As mentioned earlier, the GIDL-like leakage current is also effectively eliminated, further highlighting the effectiveness of FID. A more detailed study on the conduction mechanisms of the leakage current was reported in the next chapter. Here we briefly present

qualitative conduction mechanisms with the band diagrams shown in Fig. 2.5 to explain the effectiveness of FID in reducing the leakage. In the figure, we concentrate only on the *n*-channel operation. Similar results could also be deduced for *p*-channel operation. For the conventional device, a high electric field is developed in the channel region near the drain side (Fig. 2.5(a)). Such a high field would enhance the field emission as well as thermionic emission of holes from the silicided drain. On the other hand, the formation of FID with the band diagram shown in Fig. 2.5 (b) tends to suppress the emission of holes from the drain. As a result, GIDL-like leakage could be eliminated.

2.4.3 Effects of FID Length

The *n*- and *p*-channel subthreshold characteristics for devices with a fixed main-gate length (e.g., 3 μm) but different X_D ranging from 1 to 10 μm are shown in Figs. 2.6 and 2.7, respectively. It can be seen that the leakage currents in the off-state and the subthreshold regions are essentially independent of the FID length. On the other hand, the on-state current increases as X_D becomes shorter. This trend is reasonable, since the parasitic resistance decreases with decreasing X_D. Nevertheless, the dependence on X_D is much stronger for the *p*-channel operation. This phenomenon will be addressed in more detail later.

In Figs. 2.8 and 2.9, the drain currents for *n*- and *p*-channel operations are shown as a function of the sub-gate voltage. Devices with different X_D ranging from 1 to 6 μm were characterized. Drain voltages were 3 and –3 V for *n*- and *p*-channel operations, respectively. Two main-gate voltages $V_{G,main}$ were measured for each operation mode, i.e., 10 and 0 Volt for the *n*-channel and –10 and 0 Volt for the *p*-channel, to represent the ”on” and “off” states, respectively. When a large $|V_{G,main}|$ was applied, I-V curves in Figs. 2.8 and 2.9 could be regarded as the operation of FETs with the metal field-plate (or the sub-gate) serving as the transistor gate, while X_D became the transistor channel length, since the channel region underneath the main-gate acted simply as a “pseudo source”.

V_{th} extracted from the “on” I-V curves of Figs. 2.8 and 2.9 is shown in Fig. 2.10 as a function of X_D. It is seen that the absolute value of V_{th} in long-channel (i.e., large X_D) devices is larger for

p-channel operation mode. In addition, the short-channel effects (i.e., V_{th} roll-off shown in Fig. 2.10 and subthreshold punchthrough shown in Figs. 2.8 & 2.9) are much more severe for *n*-channel operation.

The asymmetrical V_{th} values for long-channel *p*- and *n*-channel operations can be ascribed to the existence of positive fixed charge normally observed at the oxide/Si channel interface [14]. However, this alone can not explain the asymmetrical short-channel effects shown in Fig. 2.10. Since *n*-channel operation shows much more severe short-channel effects, it strongly suggests that the background doping in our channel is *n*-type! After carefully reviewing the process history used in the device fabrication, we indeed found that the solid-phase crystallization (SPC) step was performed in a furnace previously used for n^+ diffusion. This reasonably explains the *n*-type background doping found in the channel, and illustrates the importance of carefully controlling the process environment, as it could significantly influence the device operation.

The *n*-type background doping in the channel can also explain the results shown in Figs. 2.6 and 2.7. As mentioned above, the on-state current for *p*-channel operation shows a much stronger dependence on the FID length, compared with the *n*-channel operation. This is because during the *p*-channel operation, conduction of holes in the offset channel is confined in the narrow inversion layer near the channel/oxide interface. In contrast, cross-sectional width for conduction of electrons in the offset channel during n-channel operation is wider due to the *n*-type background doping. The former case thus shows a stronger dependence on the FID length.

Current ratios between the “on” and “off” states shown in Figs. 2.8 and 2.9 are depicted in Fig. 2.11. Owing to the severe short-channel effects and the *n*-type background channel doping mentioned above, ratio much larger than unity is retained at zero sub-gate bias in *n*-channel operation. This is consistent with the results shown in Fig. 2.2.

For long-channel (i.e., large X_D) devices, the drain current becomes non-sensitive to the main-gate bias, and the ratio approaches unity as the sub-gate bias becomes negative and positive for *n*- and *p*-channel operations, respectively. Band diagrams illustrated in Fig. 2.12 can be used to

explain this phenomenon. In the figure, we concentrate only on the *p*-channel operation, although similar results can also be deduced for *n*-channel operation. When the sub-gate bias becomes positive, a strong electric field will be developed near the drain side. As a result, electron emission from the drain will be the dominant leakage mechanism, while the condition in the channel region underneath the main-gate (or the "pseudo source") has negligible effect. This could well explain why the off-state leakage is higher for p-channel operation with zero sub-gate bias than that with –50 V.

Finally, it should be pointed out that the drive performance of the proposed ambipolar device is not optimized in our experiment. This is because of the high barrier height (~0.5 eV) for both *p*- and *n*-channel operations used in our devices. Improvement could be made specifically for either *p*- or *n*-channel operations by adopting silicide materials with low barrier-height. For examples, ErSi and PtSi can be used for *n*-and p-channel operations, respectively. However, such improvement in drivability is achieved by compromising the capability of bi-channel operation.

2.5 Summary

In summary, a novel implantless Schottky barrier thin-film transistor (SBTFT) with silicided source/drain and field-induced drain (FID) extension capable of ambipolar operation is successfully demonstrated and compared with conventional SBTFTs. We found that while the conventional SBTFTs depict large GIDL-like leakage current and low on/off current ratio of less than 10^3, the new devices depict GIDL-free current characteristics with on/off current ratio as high as 10^6. This is achieved for both n- and p-channel modes of operation on the same device.

The proposed structure and its fabrication possess many advantages. First of all, all dopings (i.e., including the channel and source/drain) and accompanying annealing steps are eliminated altogether, resulting in a much simplified overall process flow which is very suitable for low-temperature manufacturing. Second, the new structure is compatible with metal-gate processing, making feasible for the first time a fully implantless CMOS process, if metallic material such as TiN is adopted as the gate material. Third, no additional masking or processing steps is needed in the new structure. This is

because the silcidation for forming Schottky source/drain can be performed simultaneously during the regular salicidation step, while the metal sub-gate can be formed simultaneously with metal interconnect. Fourth, the fully implantless process coupled with the ambipolar operation can greatly simplify CMOS process integration, resulting in an extremely low mask-count CMOS flow that is previously impossible. Finally, ambipolar modes of operation with superior characteristics are demonstrated for the first time, due to the unique device structure. The low current required for the sub-gate bias also allows the use of on-chip bias generator to simplify external power supply.

We also found that the channel region underneath the sub-gate has a lower Vth value and depicts much more severe short-channel effects for *n*-channel operation. These trends are ascribed to the positive fixed charges at the oxide/channel interface and the *n*-type background channel doping, the latter could be explained by the prior furnace history used in the SPC step of the device fabrication.

References :

[1] M. P. Lepselter and S. M. Sze, “SB-IGFET: An Insulated-Gate Field-effect transistor using Schottky barrier contacts for source and drain”, *Proc. of IEEE*, pp.1400-1401, 1968

[2] J. R. Tucker, C. Wang, and P. A. Carney, “ Silicon field-effect transistor based on quantum tunneling”, *Appl. Phys. Lett.*, vol.65, pp.618-620, 1994.

[3] W. Saitoh, A. Itoh, S. Yamagami, and M. Asada., “Analysis of short-channel Schottky source/drain metal-oxide-semiconductor field-effect transistor on SOI substrate and demonstration of sub-50 nm n-type device with metal gate”, *Jpn. J. Appl. Phys.*, vol.38, pp.6226-6231, 1999.

[4] M. Nishisaka, Y. Ochiai, and T. Asano, “Pt-Si source and drain SOI-MOSFET operating in bi-channel mode”, in *Proc. Device Res. Conf. (DRC)*, 1998, pp.74-75.

[5]C. Wang, J. P. Snyder, and J. R. Tucker, “Sub-40 nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistor”, *Appl. Phys. Lett.*, vol.74, pp.1174-1176, 19

[6] A. Itoh, M. Saitoh, and M. Asada, “A 25-nm-long channel metal-gate p-type Schottky source/drain MOSFET on SOI substrate”, *Jpn. J. Appl. Phys.* (Part I), vol.39, pp.4757-4578, 2000.

[7] J. Kedzierski, P. Xuan, E. H. Anderson J. Bokor, T. J. King, and C Hu, “Complementary silicided source/drain thin-body MOSFETs for the 20 nm gate length regime”, in *IEDM Tech. Dig.*, 2000, pp.57-60.

[8] H. C. Lin, C. Y. Lin, K. L. Yeh, R. G. Huang, M. F. Wang, C. M. Yu, T. Y. Huang, and S. M. Sze, “A novel implantless MOS thin-film Transistor with simple processing, excellent performance and ambipolar operation capability”, in *IEDM Tech. Dig.* , 2000, pp.857-859.

[9] H. C. Lin, K. L. Yeh, R. G. Huang, C. Y. Lin, and T. Y. Huang, “Schottky barrier thin-film transistor (SBTFT) with silicided source/drain and field-induced drain extension”, *IEEE Electron Device Lett.*, Vol.22, pp.179-181, 2001.

[10] H. C. Lin, K. L. Yeh, R. G. Huang, and T. Y. Huang, “Impacts of field-induced drain

(FID) on the ambipolar operation of poly-Si Schottky-barrier thin-film transistors (SBTFTs)", in *AMLCD Tech. Dig.*, 2001, pp.247-250.

[11] K. L. Yeh, H. C. Lin, R. G. Huang, R. W. Tsai, and T. Y. Huang, "Conduction mechanisms for off-state leakage Current of Schottky Barrier thin-film transistors", *Appl. Phys. Lett.*, Vol.79, pp.635-637, 2001.

[12] T. Y. Huang, I.W. Wu, A. G. Lewis, A. Chiang, R. H. Bruce, "A simpler 100-V polysilicon TFT with improved turn-on characteristics", *IEEE Electron Device Lett.*, Vol.11, pp.244-246, 1990.

[13] T. Y. Huang, I.W. Wu, A. G. Lewis, A. Chiang, R. H. Bruce, "Device sensitivity of field-plated polysilicon high-voltage TFT's and their application to low-voltage operation", *IEEE Electron Device Lett.*, Vol.11, pp.541-543, 1990.

[14] S. M. Sze: *Physics of Semiconductor Devices* (John Wiley & Sons, Inc., New York, USA, 1981) 2nd ed., p.279

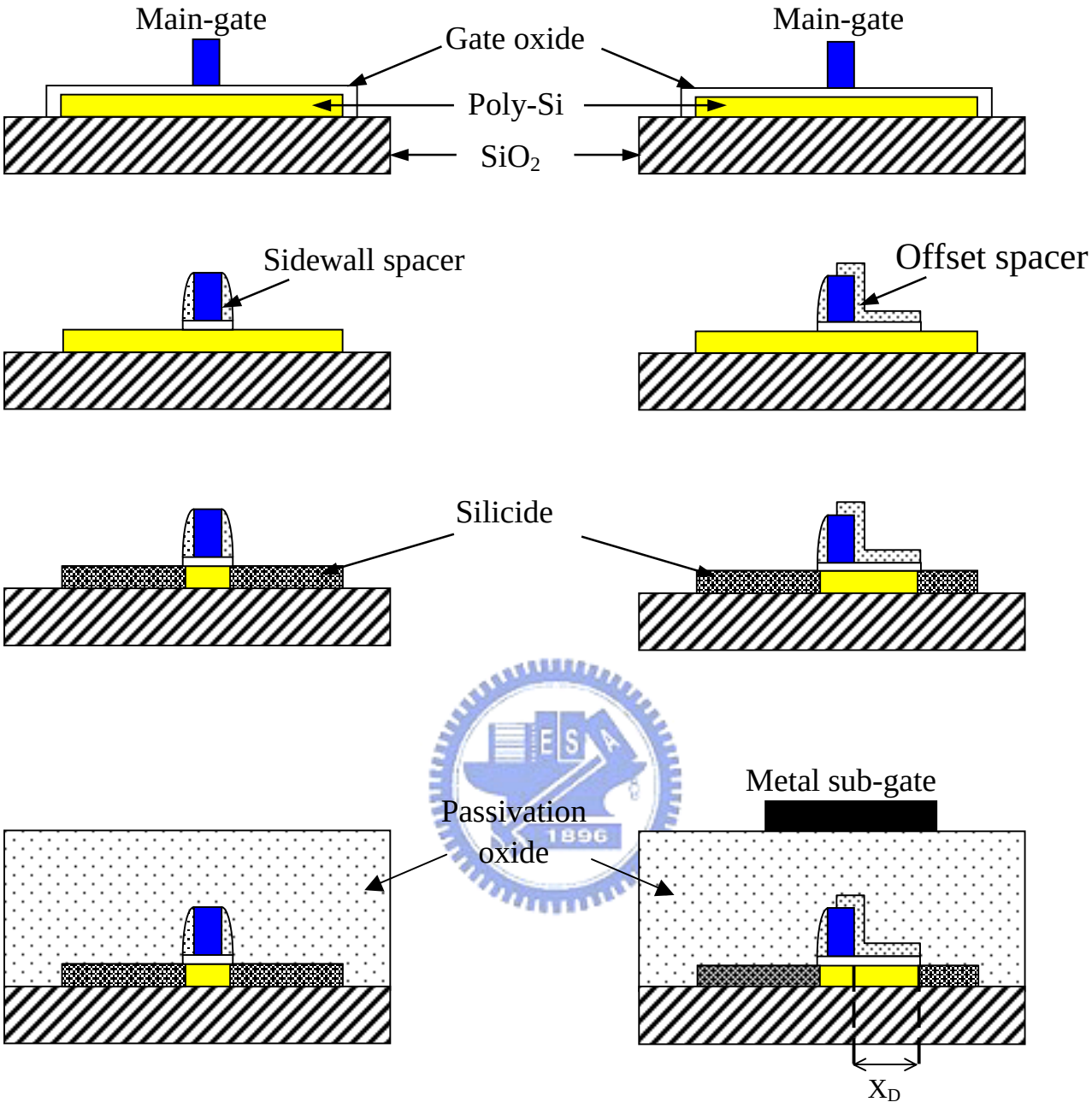


Fig. 2.1 Key fabrication steps for SBTFT devices with (a) conventional and (b) the new structure with field-induced drain (FID). X_D in (b) is the length of FID region in the channel.

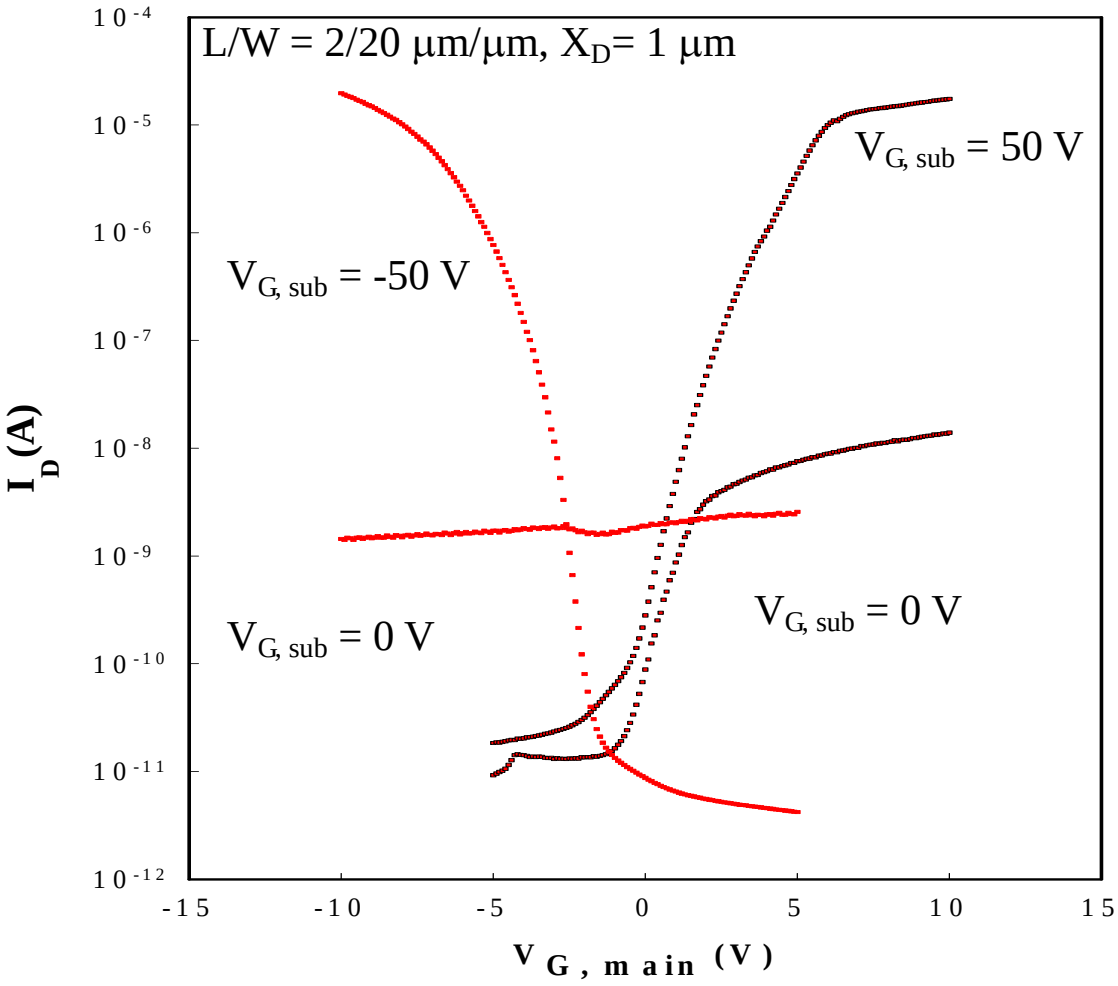


Fig. 2.2 Ambipolar subthreshold characteristics of a FID SBTFT. V_D is 5 and –5 V for *n*- and *p*-channel operations, respectively.

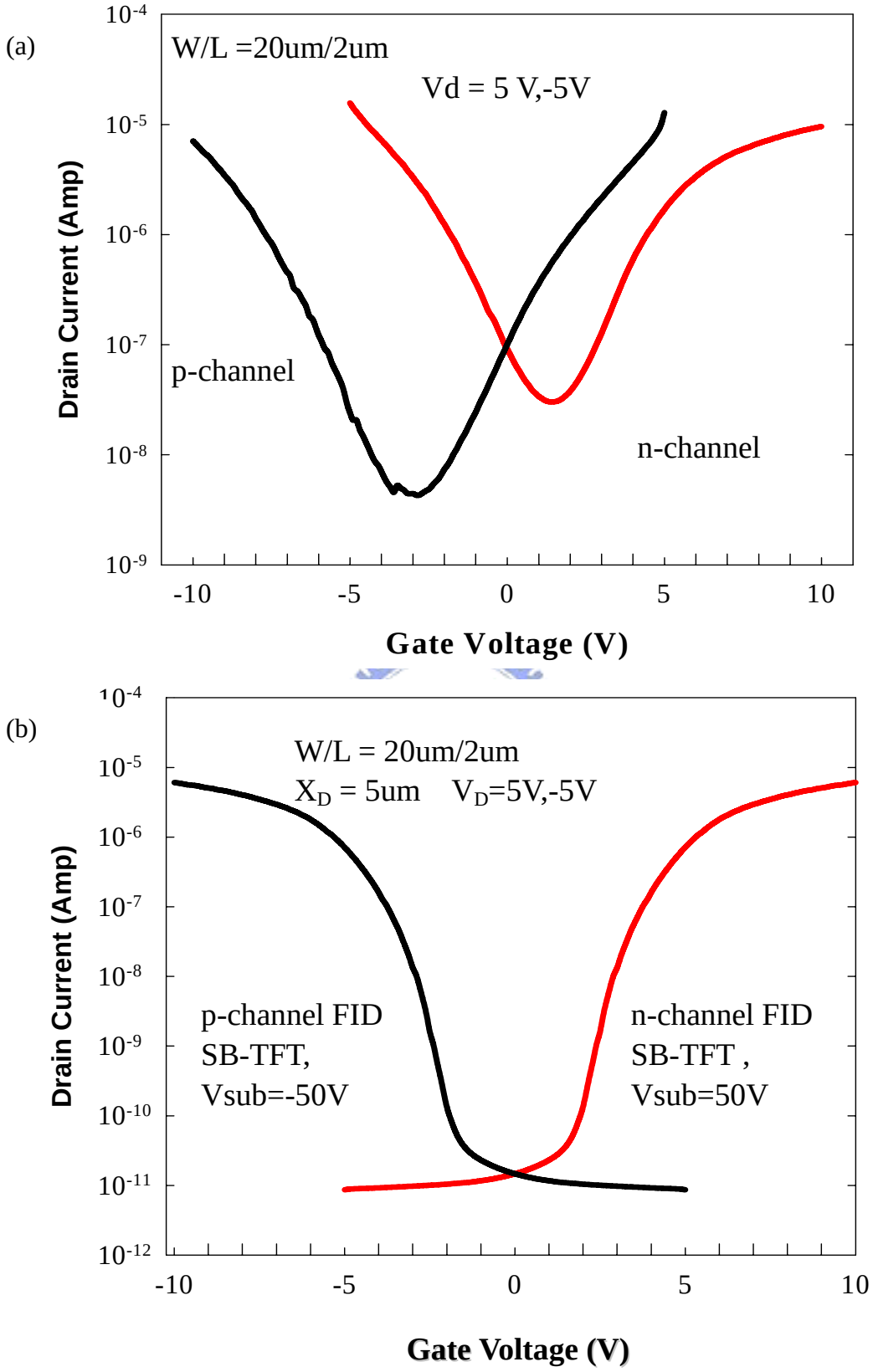


Fig. 2.3 **Typical *p*- (Vd = -5V) and *n*-channel (V_D = 5V) subthreshold characteristics of SBTFT with (a) conventional and (b) FID structure. L/W = 2/20 μm/μm. X_D in (b) is 5 μm.**

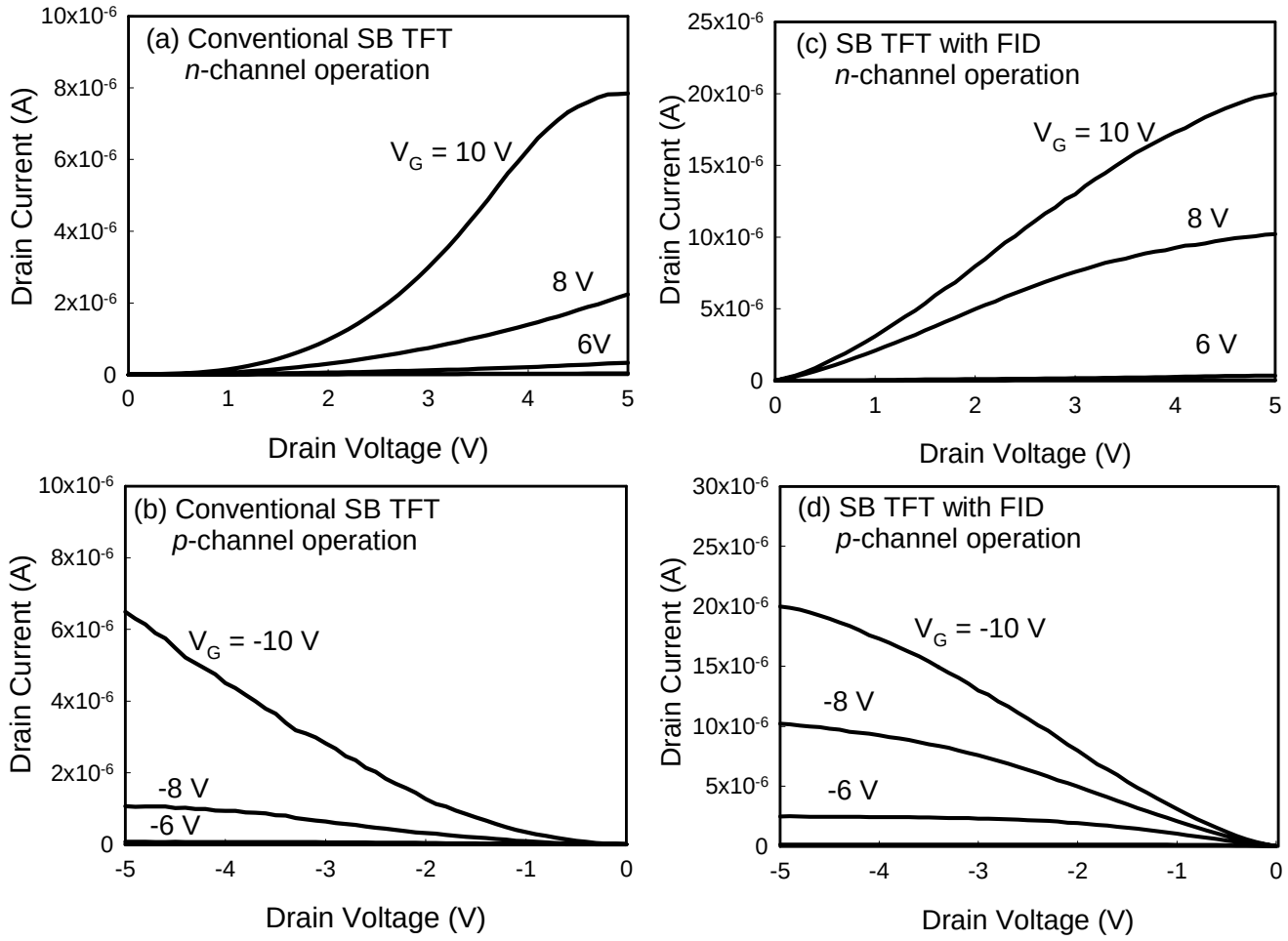


Fig. 2.4 Typical *p*- and *n*-channel output characteristics of SBTFT with (a)&(b) conventional and (c)&(d) FID structure. L/W = 2/20 μm/μm. X_D in (c) and (d) is 1 μm.

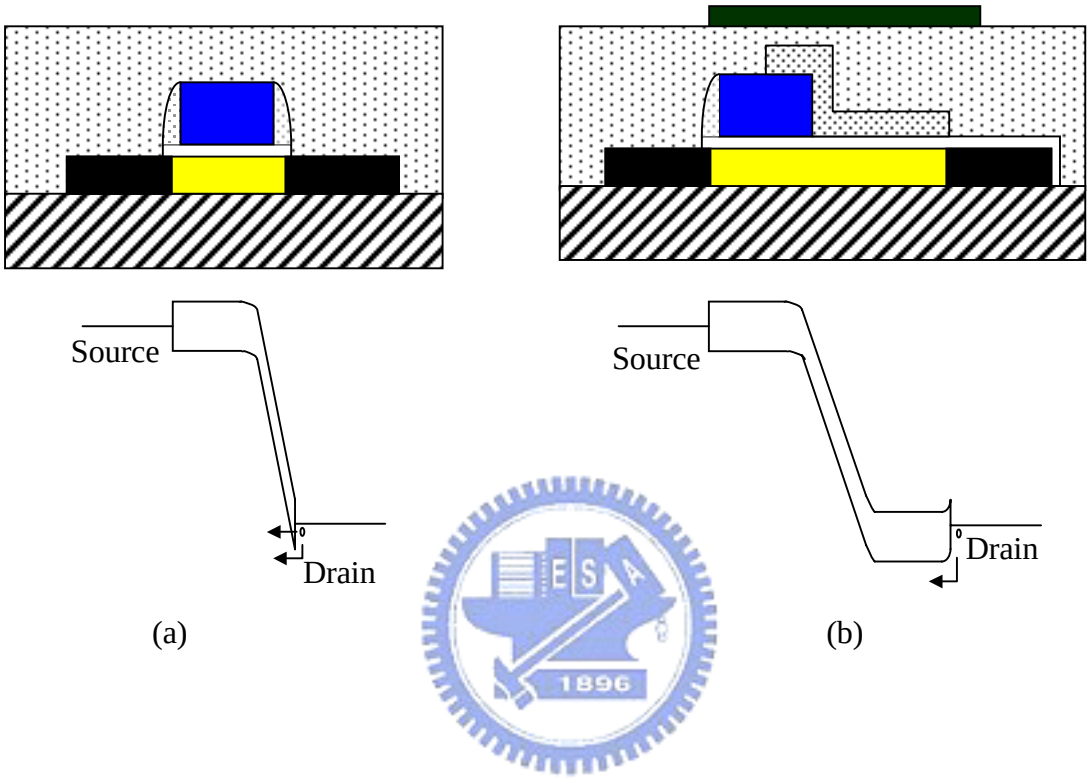


Fig. 2.5 Band diagrams for *n*-channel operation of SBTFTs with (a) conventional structure, and (b) FID at off-state (i.e., $V_{G,\,main} = 0$, $V_D = V_{DD}$, and $V_{G,\,sub} >> 0$).

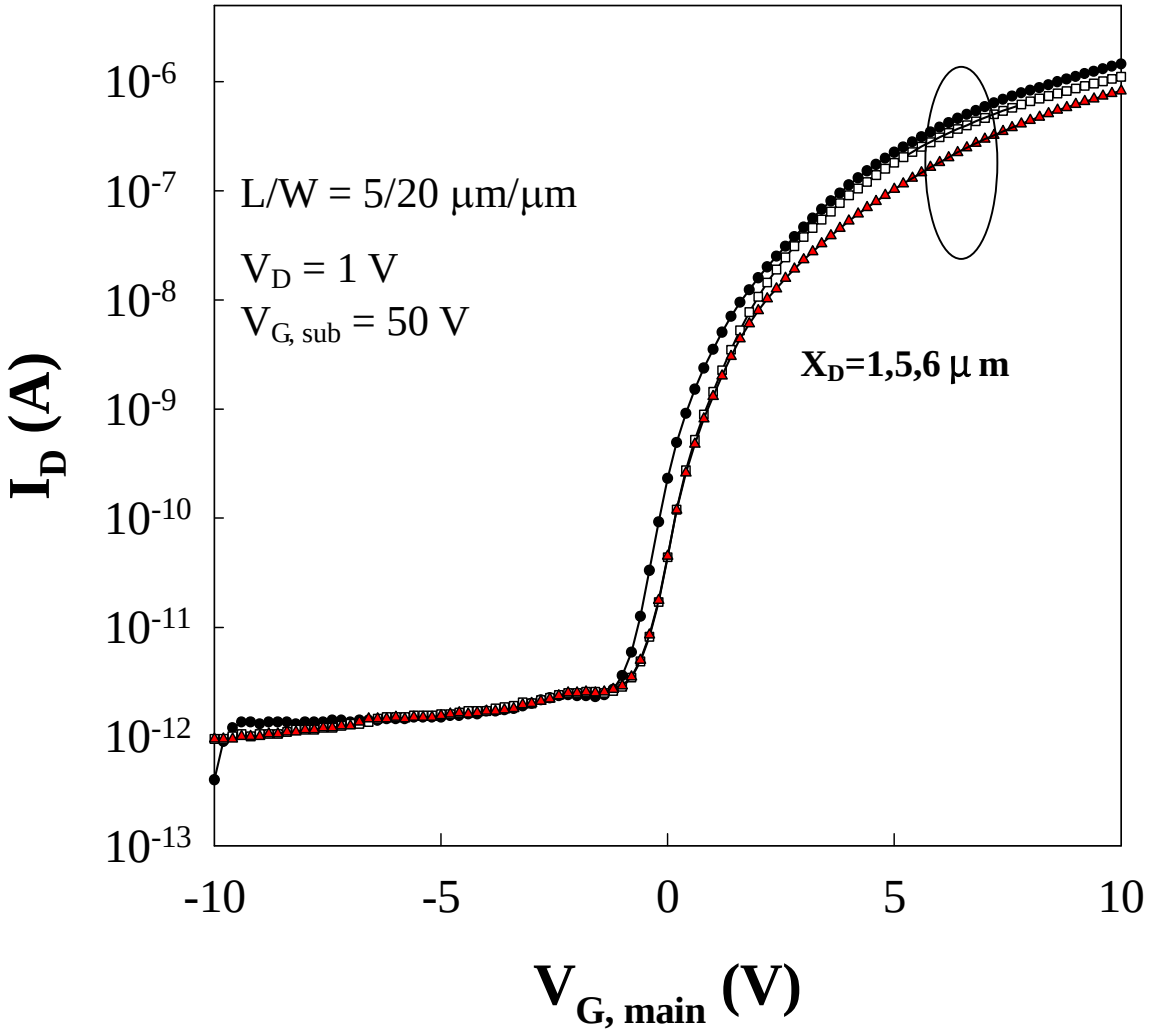


Fig. 2.6 **Typical *n*-channel (Vd = 1V) subthreshold characteristics of SBTFT devices with various X_D (e.g., 1, 5, and 6 μm). L/W = 5/20 μm/μm.**

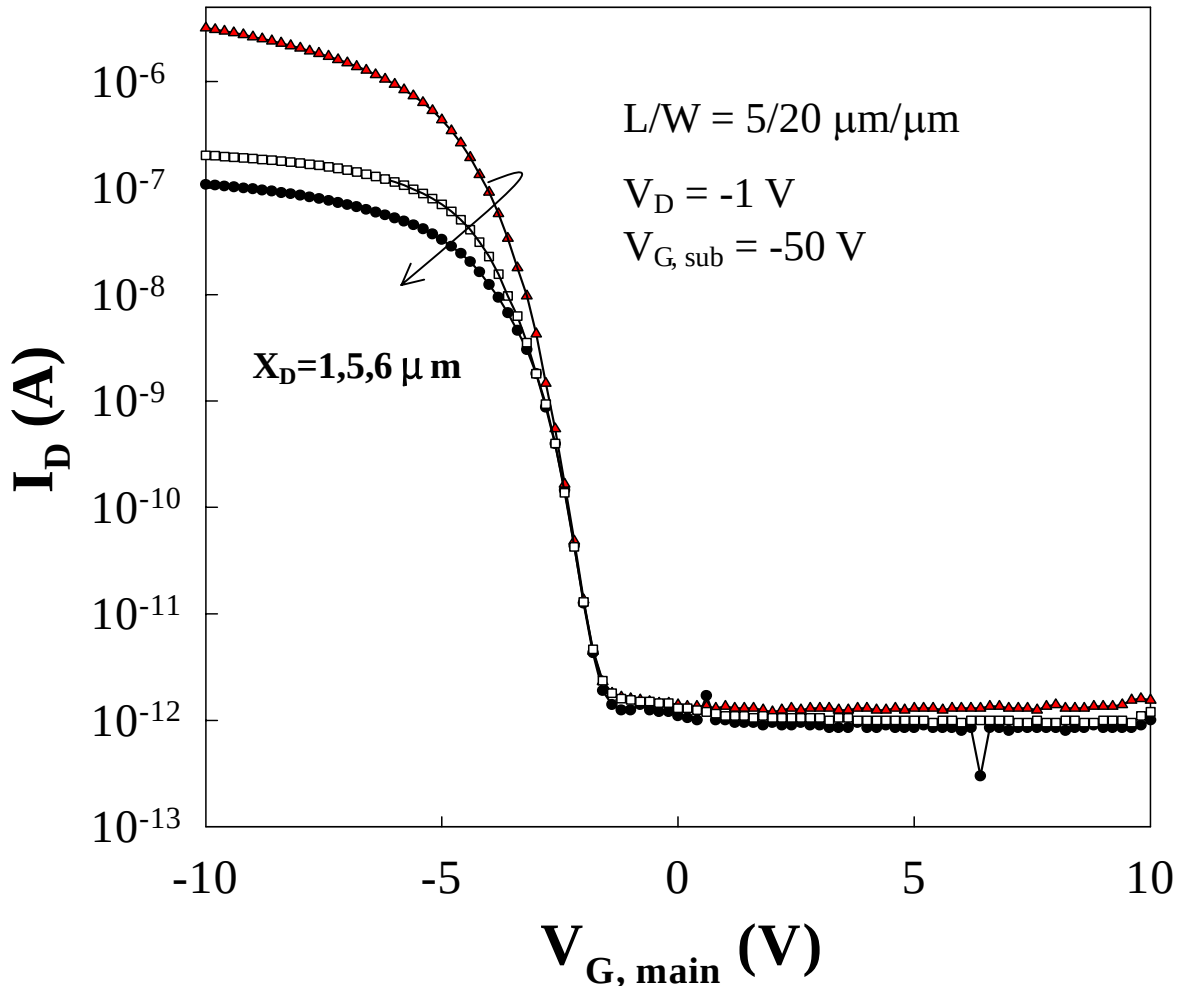


Fig. 2.7 **Typical *p*-channel (Vd = -1V) subthreshold characteristics of SBTFT devices with various X_D (e.g., 1, 5, and 6 μm). L/W = 5/20 μm/μm.**

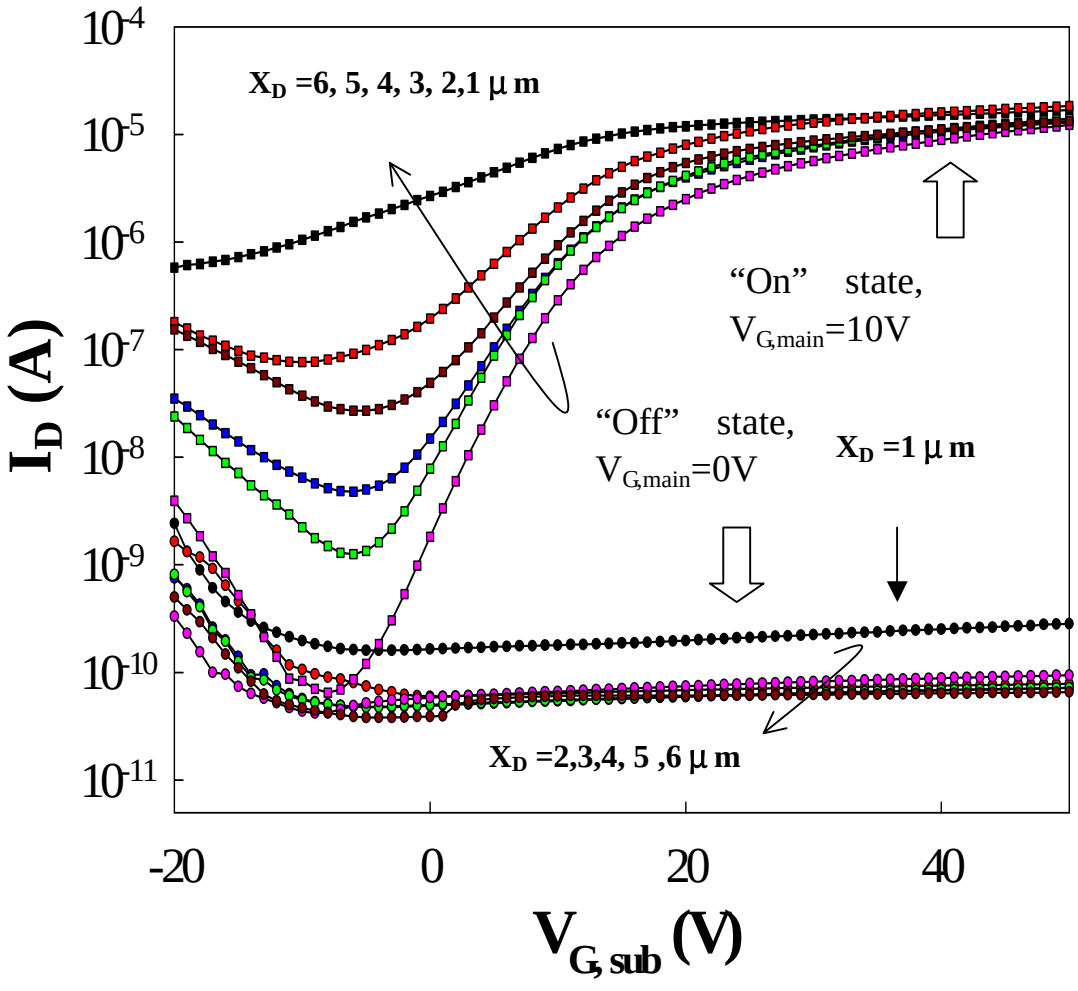


Fig. 2.8 Effects of the sub-gate bias and X_D on the *n*-channel operation of FID SBTFTs. L/W =5/20 μm/μm.

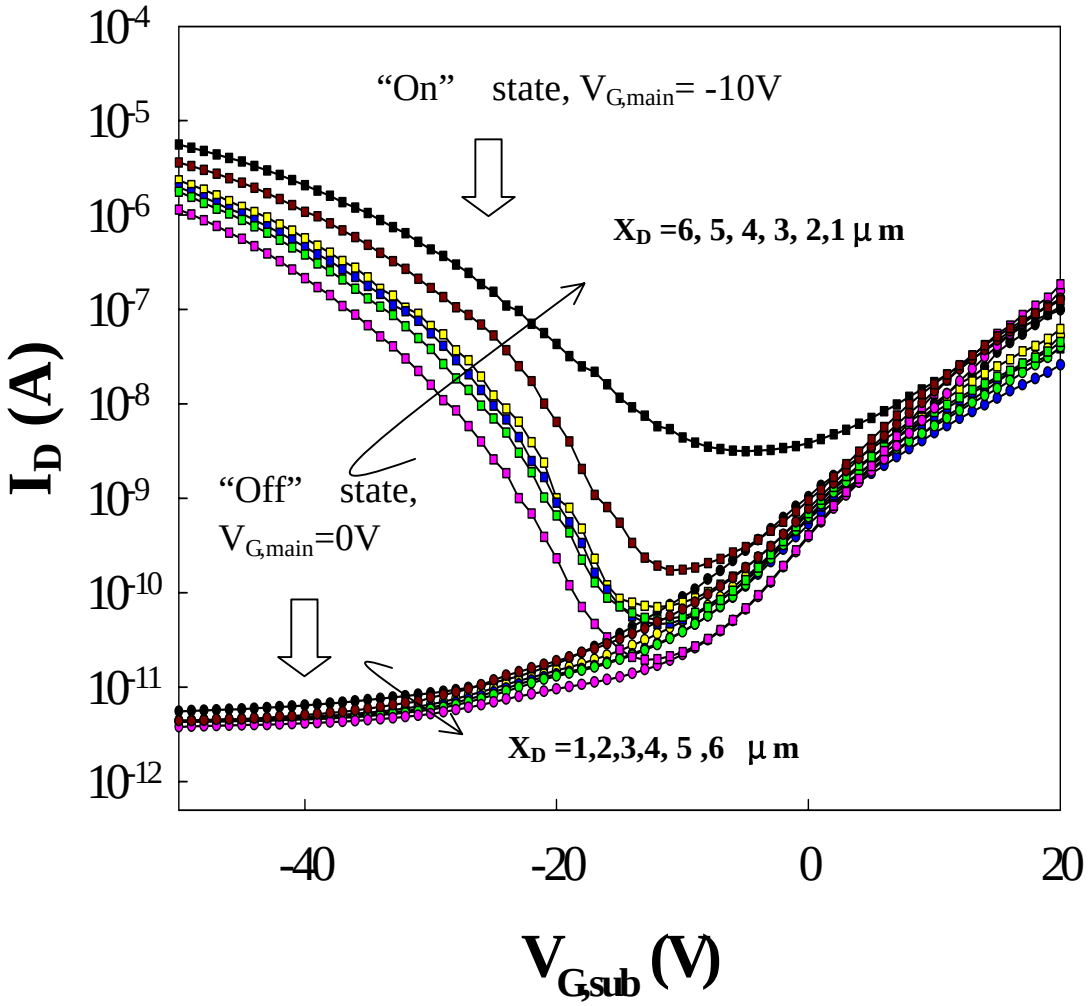


Fig. 2.9 Effects of the sub-gate bias and X_D on the *p*-channel operation of FID SBTFTs. L/W =5/20 μm/μm.

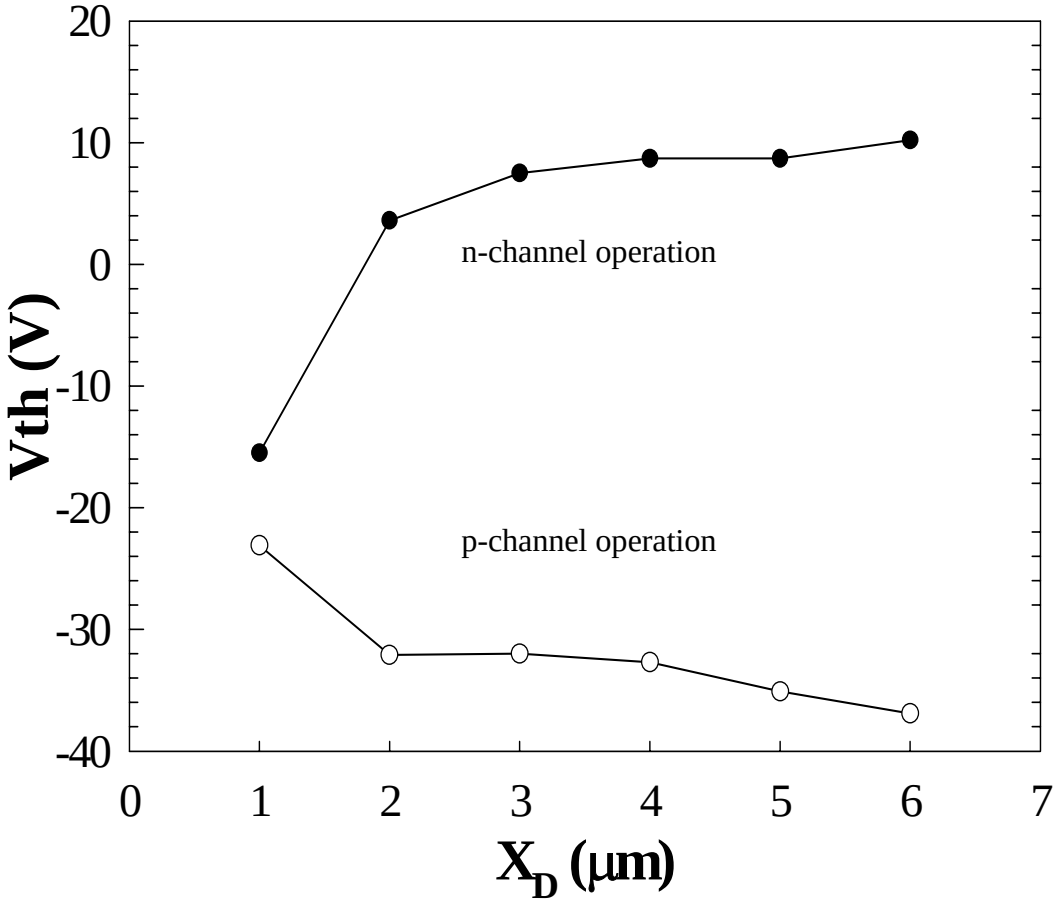


Fig. 2.10 **Vth extracted from the "on" state I-V curves of Figs. 2.8 and 2.9 as a function of X_D.**

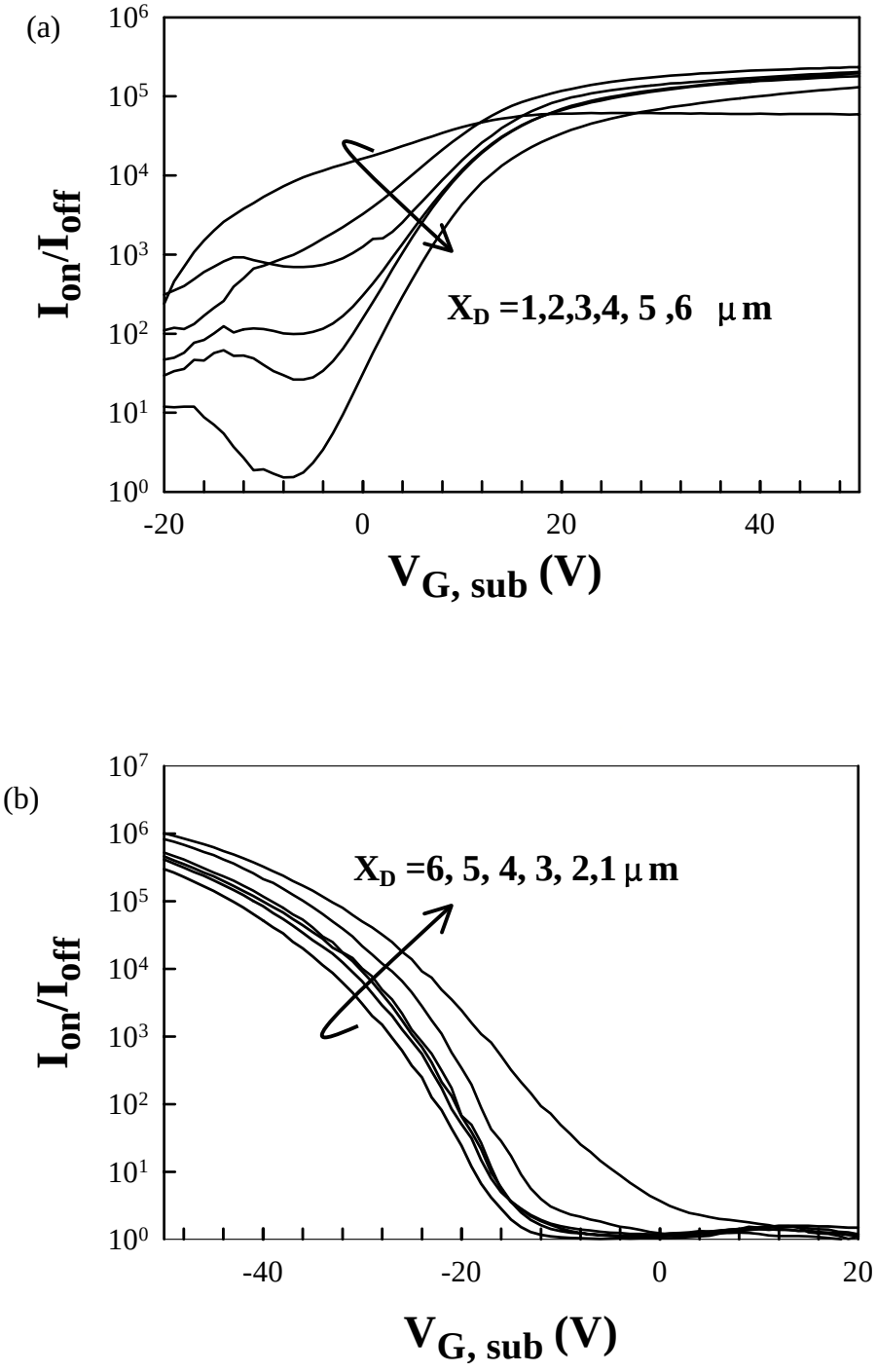


Fig. 2.11 Ratio between the "on" and "off " state currents (Figs. 8 & 9) for (a) *n*- and (b) *p*-channel operations.

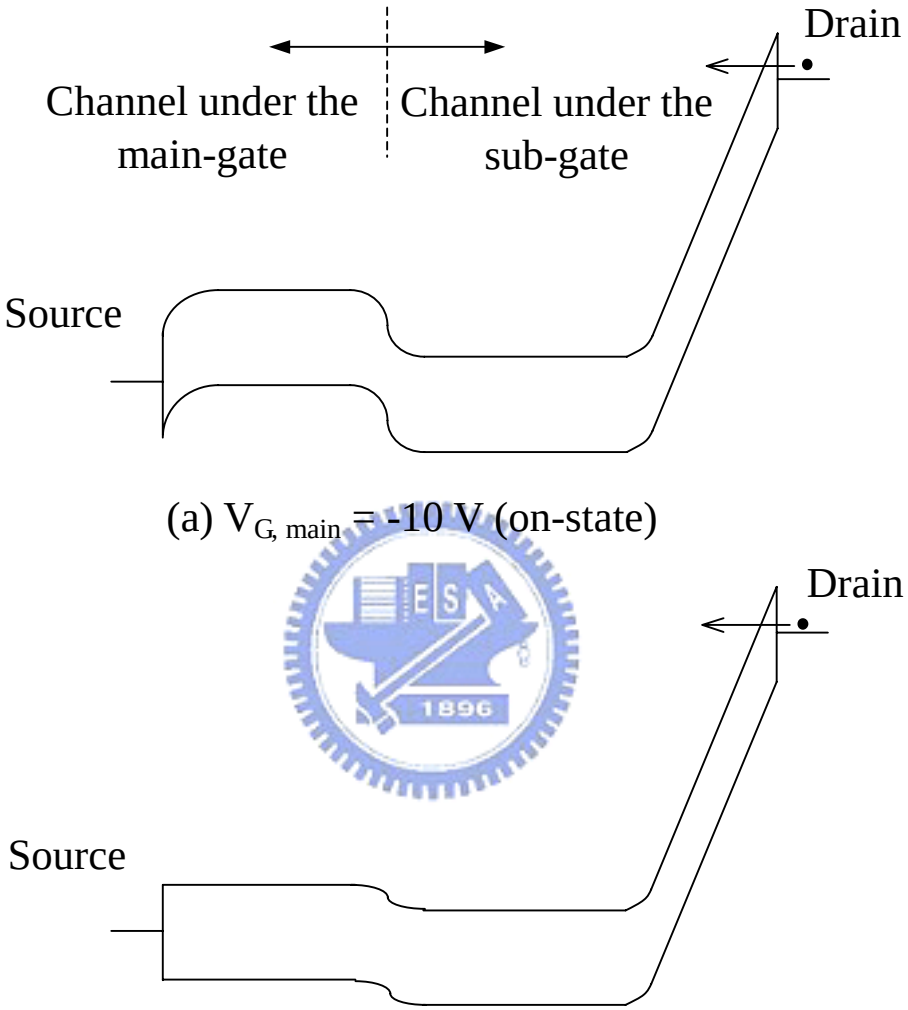


Fig. 2.12 Band diagrams for *p*-channel operation (V_D= -3 V) of FID SBTFT with a high positive sub-gate bias.

Chapter 3

Leakage Current Mechanisms in Schottky Barrier Thin-Film Transistors

3.1 Introduction

Our experimental results in the last chapter showed that an excellent on/off current ratio higher than 10^6 for both p- and n-channel operation could be realized on the same device. More importantly, the GIDL-like off-state leakage current encountered in a conventional SBTFT [1-6](i.e., without a field plate, using a sidewall spacer to isolate the source/drain and the gate during silicidation, as shown in Fig. 3.1(b)) could be completely suppressed. Though the improvement is significant and encouraging, a detailed understanding of the leakage mechanisms for both conventional and FID SBTFT devices is in order. In this chapter, we pursue this issue by characterizing the off-state leakage of the devices at different temperatures and under different bias conditions for both structures. Based on the obtained results, the conduction mechanisms for leakage are discussed and identified.

3.2 Experiment and Measurement

Figures 3.1(a) and 3.1(b) show the cross-sectional view for the proposed novel structure with FID and the conventional SBTFT, respectively. Detailed device fabrication can be found in the previous chapter. The major difference in the fabrication of these devices occurs in the step after the poly-Si main-gate formation. For the FID device [7-11] (Fig. 3.1(a), a chemical-vapor-deposition (CVD) oxide layer was deposited and a photolithographic step was used to define the offset channel region with length X_D. During the subsequent reactive-ion etching (RIE) step, self-aligned gate sidewall spacers were simultaneously formed in the device with a conventional structure (Fig. 3.1(b)). Subsequently, a self-aligned silicidation (salicidation) treatment was performed to form the silicide source/drain. Wafers then followed a standard back-end processing to form contact pads, and received a plasma treatment at 250°C in NH_3 for 1 hr before measurement. It is worth noting that the metal sub-gate was formed during the regular metal patterning, so no extra steps were required.

Devices were characterized using an HP4156 parametric analyzer. Drain current was measured by sweeping the gate voltage from 5 to –5 V. The temperature range was from 25°C to 150°C. In order to investigate the effects of electric field near the drain side, different drain voltage values, $|V_D|$ = 1 and 3 V, were applied. For the novel structure operated under *p*-channel mode, the sub-gate voltage was maintained at –50V. While for *n*-channel operation, the sub-gate voltage was maintained at 50V. For comparison, measurements with the same main-gate and drain bias conditions were also performed on conventional SBTFT devices.

3.3 Experimental Results

Figures 3.2 and 3.3 show subthreshold characteristics of *n*- and *p*-channel operations characterized at temperatures ranging from 25 to 150℃ for a SBTFT with conventional structure. As can be seen in these figures, the device depicts very poor performance with intolerable off-state leakage current. In fact, the off-state leakage current is very sensitive to the voltage difference applied between the main gate and the drain, i.e., $|V_{GD}|$, and results in the V-shaped I-V curves.

Activation energy, E_A, of the conduction process could be extracted from the Arrhenius plots. Typical examples for *n*- and *p*-channel operations are shown in Fig. 3.4 and Fig. 3.5, respectively. In these cases, $|V_G|$ = 0 or 4.5 V, and $|V_D|$ = 1 or 3 V, were applied. Basically, E_A decreases with increasing $|V_D|$ at a fixed V_G, or decreases with increasing $|V_G|$ at a fixed V_D. This trend is further highlighted in Fig. 3.6, in which the extracted E_A values are plotted as a function of the gate voltage. The results clearly indicate that E_A is also very sensitive to $|V_{GD}|$. This implies that the field strength of the drain junction is crucial to the leakage.

Typical I_D-V_G characteristics for *n*- and *p*-channel operations of FID SBTFTs at different temperatures are depicted in Figs. 3.7 and 3.8, respectively. The channel length and width of the device are 5 and 20 μm, respectively. The length of X_D is 4μm unless otherwise stated. It is seen that, regardless of the temperature, the off-state leakage current shows only a very weak dependence on V_G, which is in strong contrast to the behavior of the SBTFTs with conventional structure (Figs. 3.4 and 3.5). However, the leakage current seems to be very sensitive to the temperature and increases

significantly as temperature rises, implying that the conduction mechanism is most likely a thermally activated process.

Typical examples of Arrhenius plots for the FID SBTFT under n- and p-channel operations are shown in Figs. 3.9 and 3.10, respectively. The drain and the main-gate bias conditions are the same as those used in Fig. 3.6. The sub-gate bias is 50 V for n- and –50 V for p-channel operation. The extracted E_A results are presented in Fig. 11. In strong contrast to the trend shown in Fig. 3.8, E_A shows only a very weak dependence on $|V_{GD}|$ in the off-state for either p- or n-channel operation, as expected from Figs. 3.9 and 3.10. In addition, E_A is close to the barrier height of CoSi/Si [12].

3.4 Leakage Mechanisms

Based on the above results, we propose the band diagrams shown in Figs. 3.12 and 3.13 to explain the leakage mechanisms for conventional and FID SBTFT devices, respectively. Note that in these figures, only *n*-channel operation is considered, however, similar conclusions with opposite bias polarity and carrier type could be deduced for *p*-channel operation. For conventional SBTFT devices, most of the voltage drop in the channel is developed near the drain junction, as shown in Fig. 3.12. As a result, field emission and thermionic emission processes both contribute to off-state leakage. When V_{GD} increases, however, field emission of holes from the drain junction dominates the conduction process, due to a decrease in the tunneling distance. This explains why E_A decreases with increasing $|V_{GD}|$.

On the other hand, the mechanisms for FID SBTFT devices shown in Fig. 3.13 are very different from those of the conventional SBTFTs. The highly positive bias applied to the sub-gate would pin the Fermi level of the offset channel region close to the conduction band edge. Under this situation, the high electric-field region would be pulled away from the drain junction. As a result, only holes with sufficient energy could overcome the Schottky barrier. In other words, the thermionic emission process becomes the major conduction mechanism. This explains why E_A is higher than that of conventional SBTFT devices. Moreover, since the barrier height is not significantly affected by the main-gate bias, the GIDL-like leakage can be suppressed.

Note that, in Fig.3. 11, the sum of the activation energies for *p*- and *n*-channel operations in the off-state is slightly larger than the band gap of Si (~ 1.1 eV), which is the sum of Schottky barrier heights for electrons and holes. We believe that this is due to the large bias applied on the sub-gate that would shift the Fermi level in the offset channel region closer to the conduction band edge for n-channel operation, and similarly closer to the valence band edge for p-channel operation. This would result in a barrier height for thermionic emission that is slightly higher than the Schottky barrier height (see Fig.3. 13).

3.5 Summary

In this work we have experimentally investigated the conduction mechanisms of the off-state leakage current for SBTFTs with FID and conventional structure. The results show that the activation energy of the off-state leakage decreases significantly with increasing $|V_{GD}|$ for conventional SBTFTs. This indicates that field emission plays a major role as the field strength in the drain junction becomes high, and results in strong GIDL-like phenomenon. In contrast, the activation energy of the off-state leakage shows only a minor dependence on $|V_{GD}|$ for SBTFT devices with FID. This is ascribed to the fact that the high sub-gate bias would pin the Fermi level of the offset channel near the conduction band edge for n-channel operation, and near the valence band edge for p-channel operation, thus pulling the high field region away from the drain junction. As a result, the thermionic emission process will dominate the off-state current conduction, thus eliminating the GIDL-like leakage encountered in SBTFT with a conventional structure.

References :

[1] M. P. Lepselter, and S. M. Sze, “SB-IGFET: An Insulated-Gate Field-Effect Transistor Using Schottky Barrier Contacts as Source and Drain,” *Proc. IEEE*, 56, p.1088, 1968.

[2] J. R. Tucker, C. Wang, and S. Carney, “Silicon field-effect transistor based on quantum tunneling,” Appl. Phys. Lett., vol. 65, p.618, 1994.

[3] W. Saitoh, A. Itoh, S. Yamagami and M. Asada, “ Analysis of short-channel Schottky source/drain metal-oxide-semiconductor field-effect-transistor on Silicon-on-insulator substrate and demonstration of sub-50-nm n-type devices with metal gate,” *Jpn. J. Appl. Phys.*, vol. 38, p.6226, 1999.

[4] M. Nisisaka, Y. Ochiai and T. Asano,: **“**Pt-silicide source and drain SOI-MOSFET operating in bi-channel modes” *Proc. Device Res. Conf (DRC)* (1998). p.74-75

[5] C. Wang, J. P. Synder, and J.R. Tucker, “Sub-40nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistors,” *Appl. Phys. Lett.*, vol. 74, p.1174, 1999.

[6] A. Itoh, M. Saitoh, and M. Asada, “A 25-nm-long channel metal-gate p-type Schottky source/drain MOSFET on SOI substrate”, *Jpn. J. Appl. Phys.* (Part I), vol.39, pp.4757-4578, 2000.

[7] H. C. Lin, K. L. Yeh, R. G. Huang, C. Y. Lin, and T. Y. Huang, “Schottky barrier thin-film transistor (SBTFT) with silicided source/drain and field-induced drain extension”, *IEEE Electron Device Lett.*, Vol.22, pp.179-181, 2001.

[8] H. C. Lin, K. L. Yeh, R. G. Huang, C. Y. Lin, and T. Y. Huang, “Schottky barrier thin-film transistor (SBTFT) with silicided source/drain and field-induced drain extension”, *IEEE Electron Device Lett.*, Vol.22, pp.179-181, 2001.

[9] K. L. Yeh, H. C. Lin, R. G. Huang, R. W. Tsai, and T. Y. Huang, “Conduction mechanisms for off-state leakage Current of Schottky Barrier thin-film transistors”, *Appl. Phys. Lett.*, Vol.79, pp.635-637, 2001.

[10] T. Y. Huang, I.W. Wu, A. G. Lewis, A. Chiang, R. H. Bruce, “A simpler 100-V polysilicon TFT with improved turn-on characteristics”, *IEEE Electron Device Lett.*, Vol.11, pp.244-246, 1990.

[11] T. Y. Huang, I.W. Wu, A. G. Lewis, A. Chiang, R. H. Bruce, “Device sensitivity of field-plated polysilicon high-voltage TFT’s and their application to low-voltage operation”, *IEEE Electron Device Lett.*, Vol.11, pp.541-543, 1990.

[12] S. M. Sze: *Physics of Semiconductor Devices* (John Wiley & Sons, Inc., New York, USA, 1981) 2nd ed., p.279

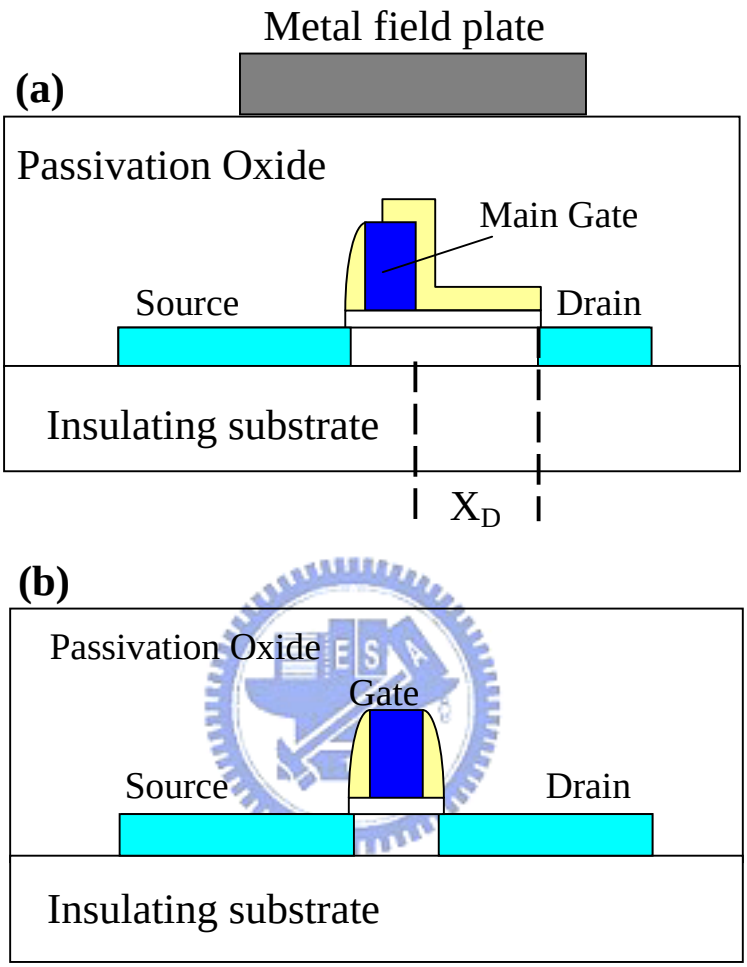


Fig. 3.1 Cross-sectional views of SBTFT devices (a) with and (b) without the field plate. X_D in (a) is the length of the offset region in the channel.

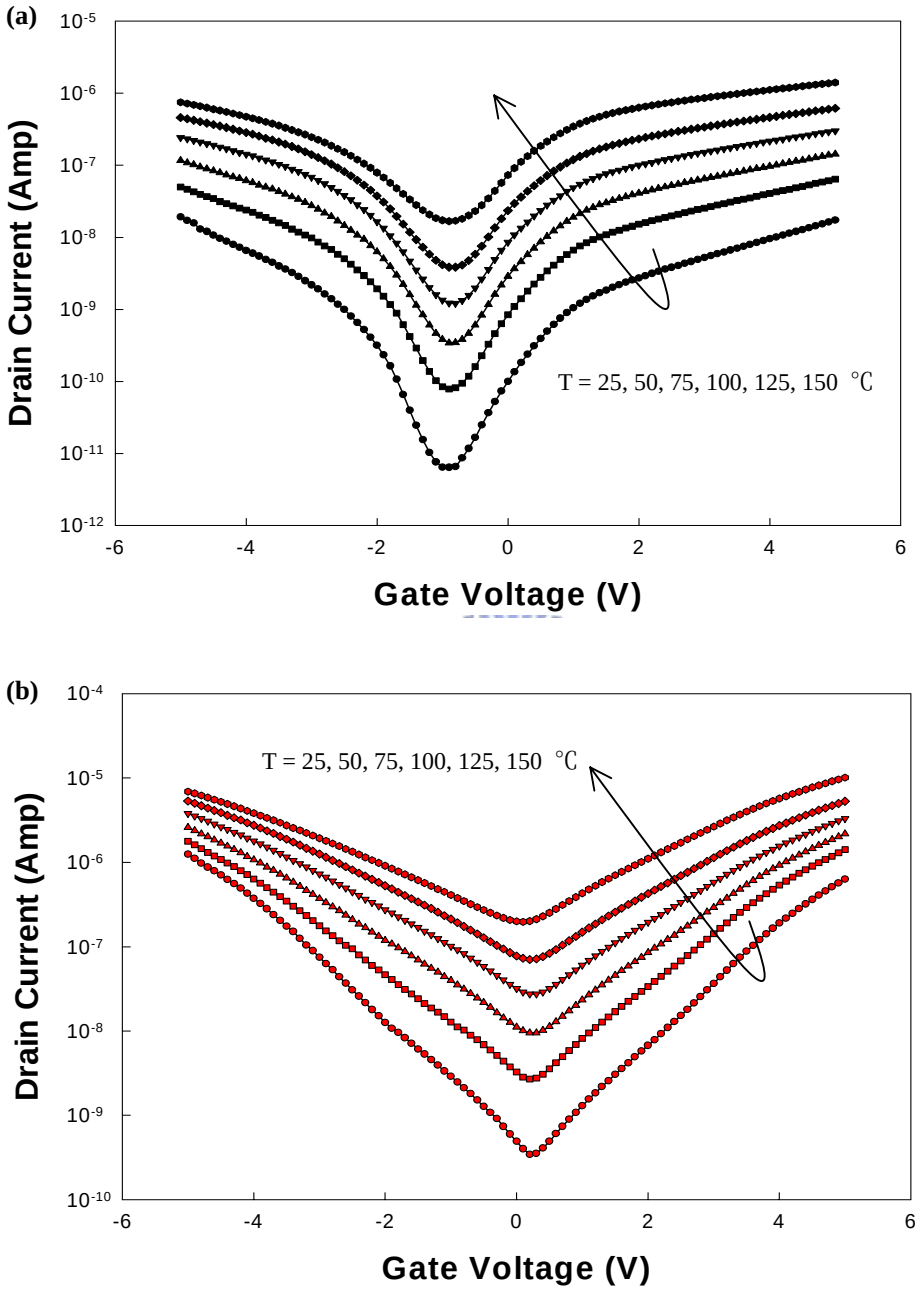


Fig. 3.2 I_D-V_G characteristics for *n*-channel operation of a SBTFT with conventional structure: (a) V_D=1V; (b) V_D=3V. Channel length and width are 5 and 20 μm, respectively.

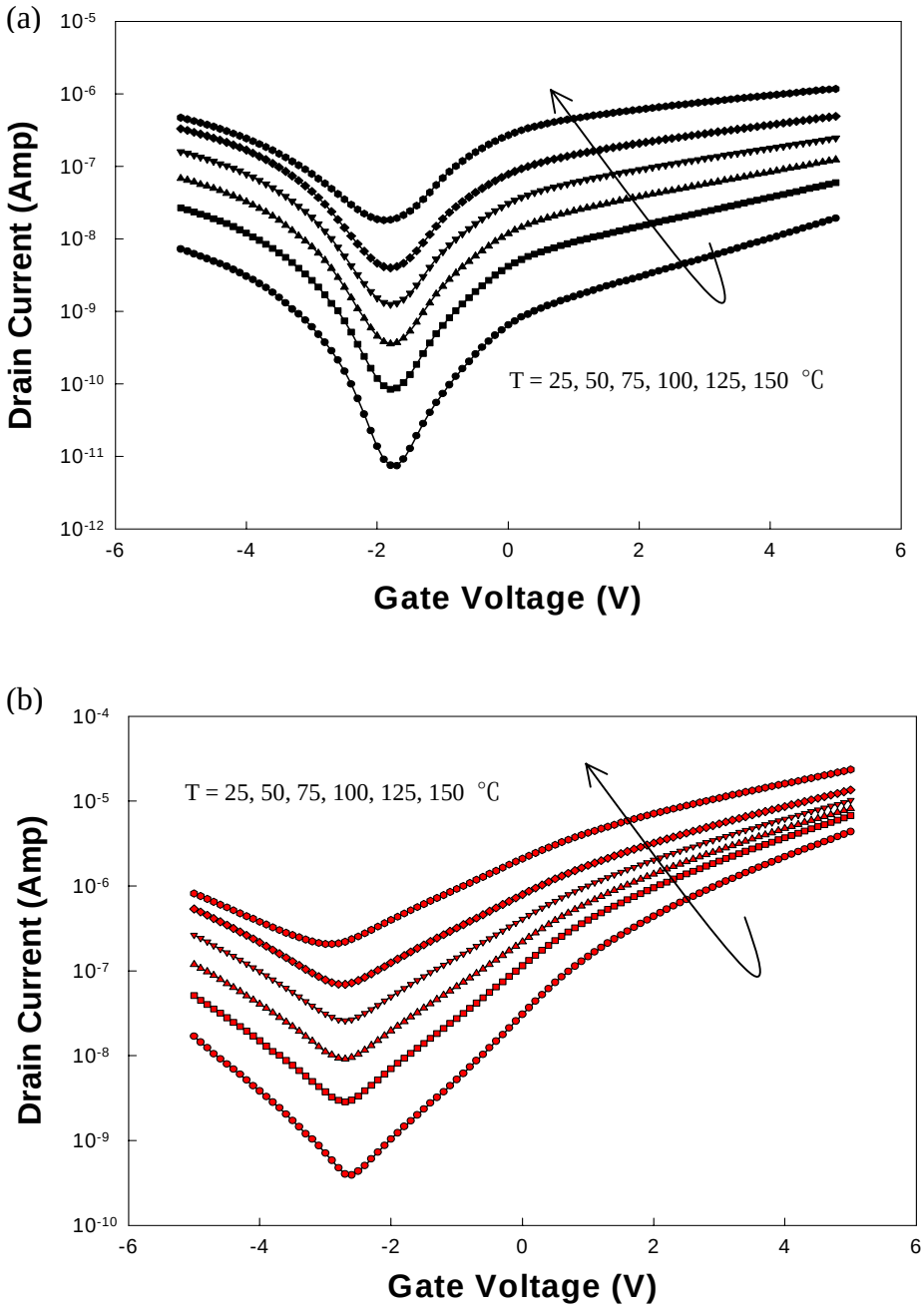


Fig. 3.3 **I_D-V_G characteristics for *p*-channel operation of a SBTFT with conventional structure: (a) V_D=-1V; (b) V_D=-3V. Channel length and width are 5 and 20 μm, respectively.**

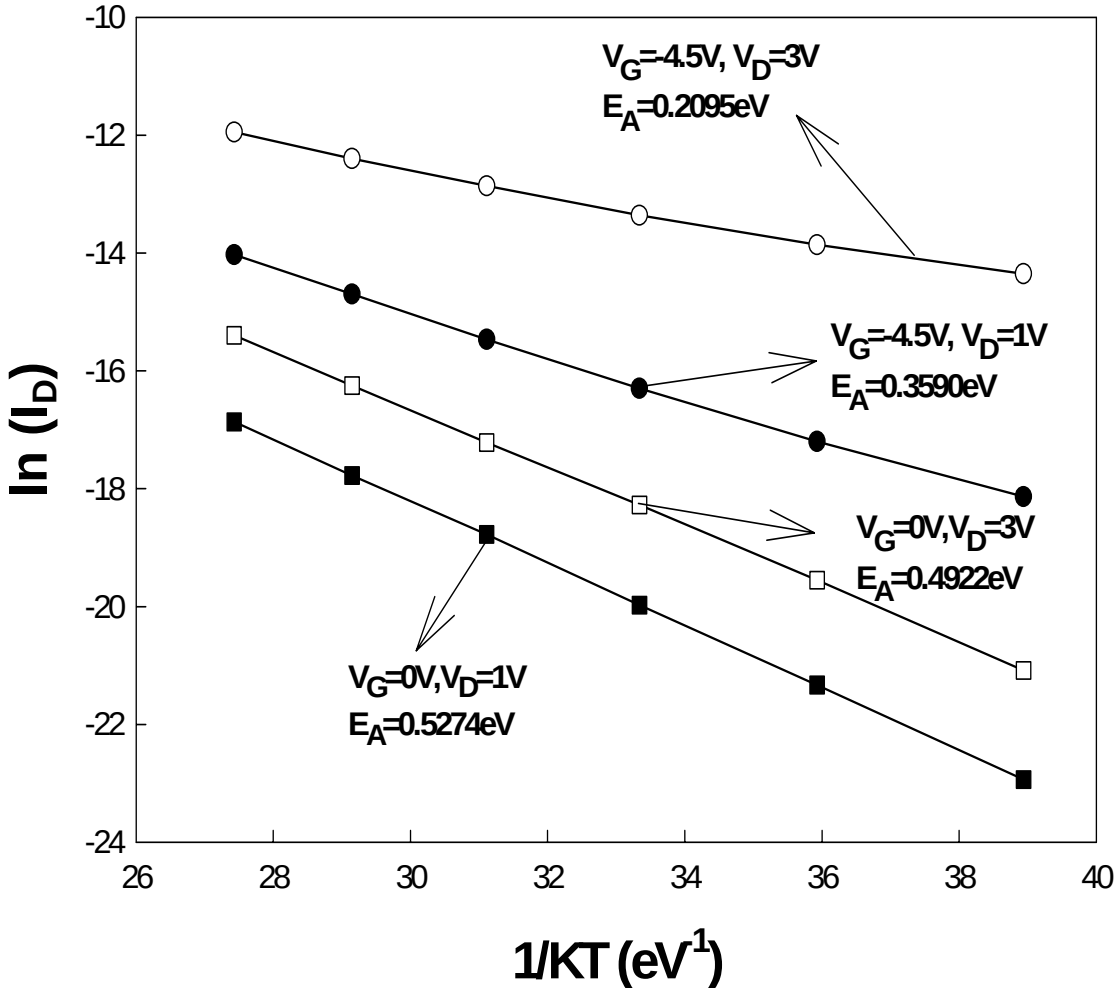


Fig. 3.4 Arrhenius plots for *n*-channel operation of a SBTFT with conventional structure.

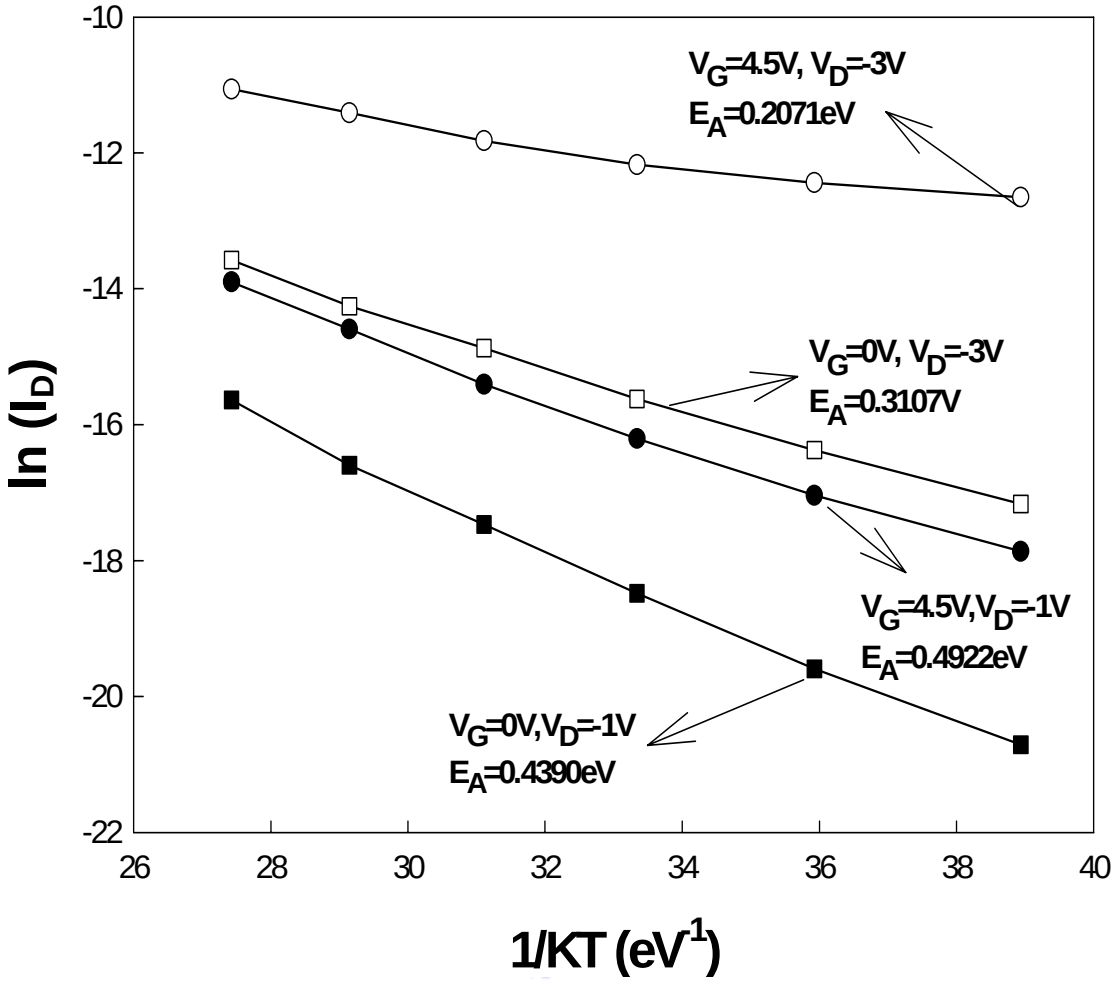


Fig.3.5 **Arrhenius plots for *p*-channel operation of a SBTFT with conventional structure**.

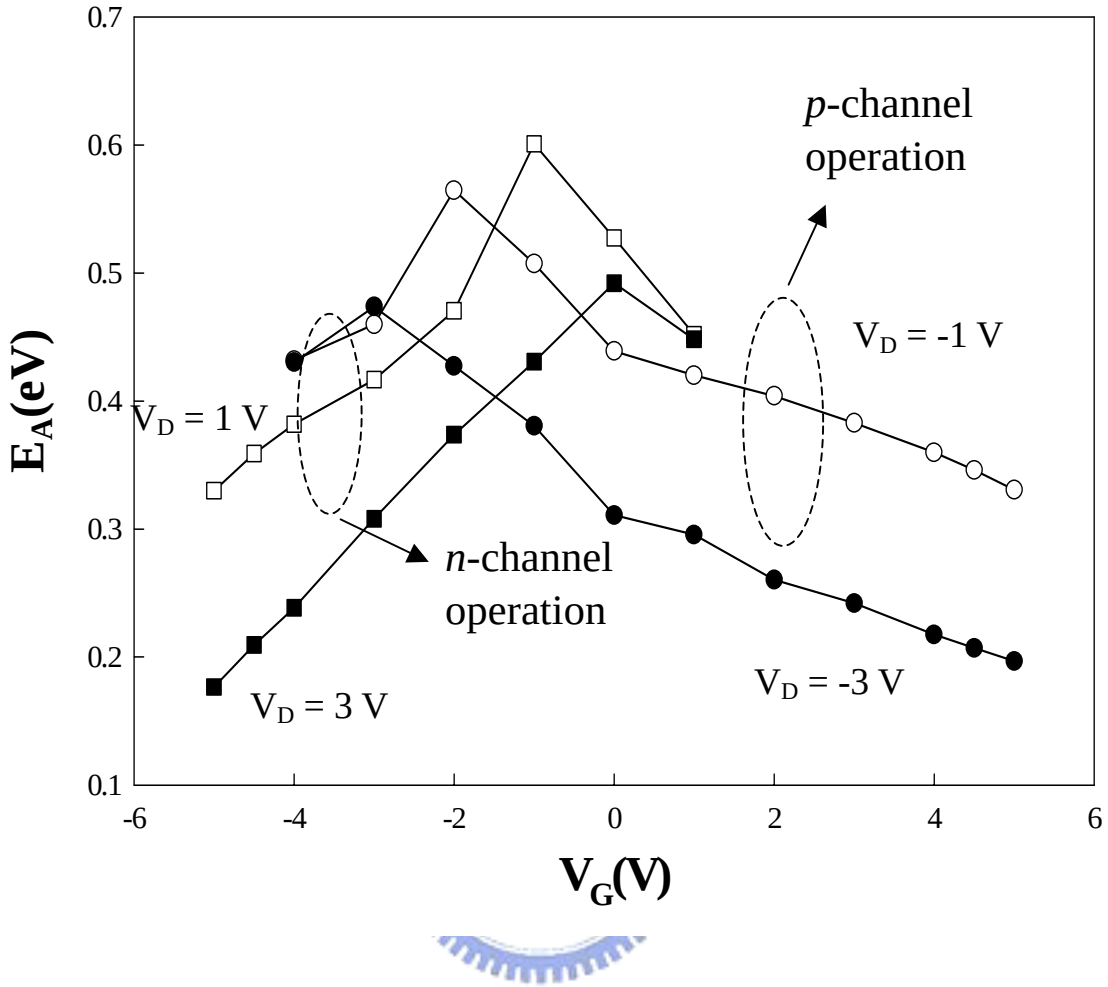


Fig. 3.6 **E_A as a function V_G for *n*- and *p*-channel operations of a SBTFT with conventional structure.**

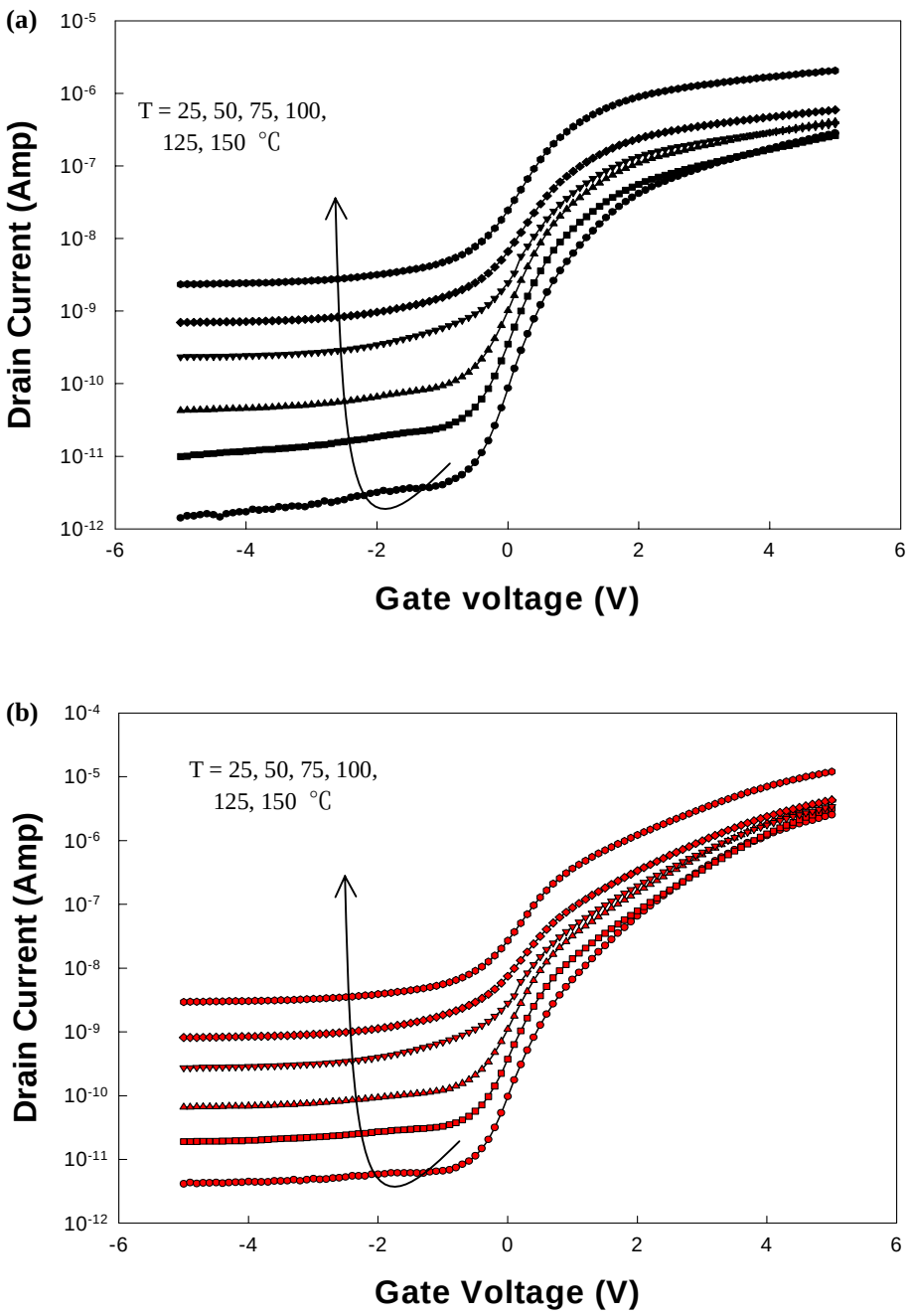


Fig. 3.7 **I_D-V_G characteristics for *n*-channel operation of a SBTFT with FID structure: (a) V_D=1V; (b) V_D=3V. Channel length and width are 5 and 20 μm, respectively. X_D is 4μm.**

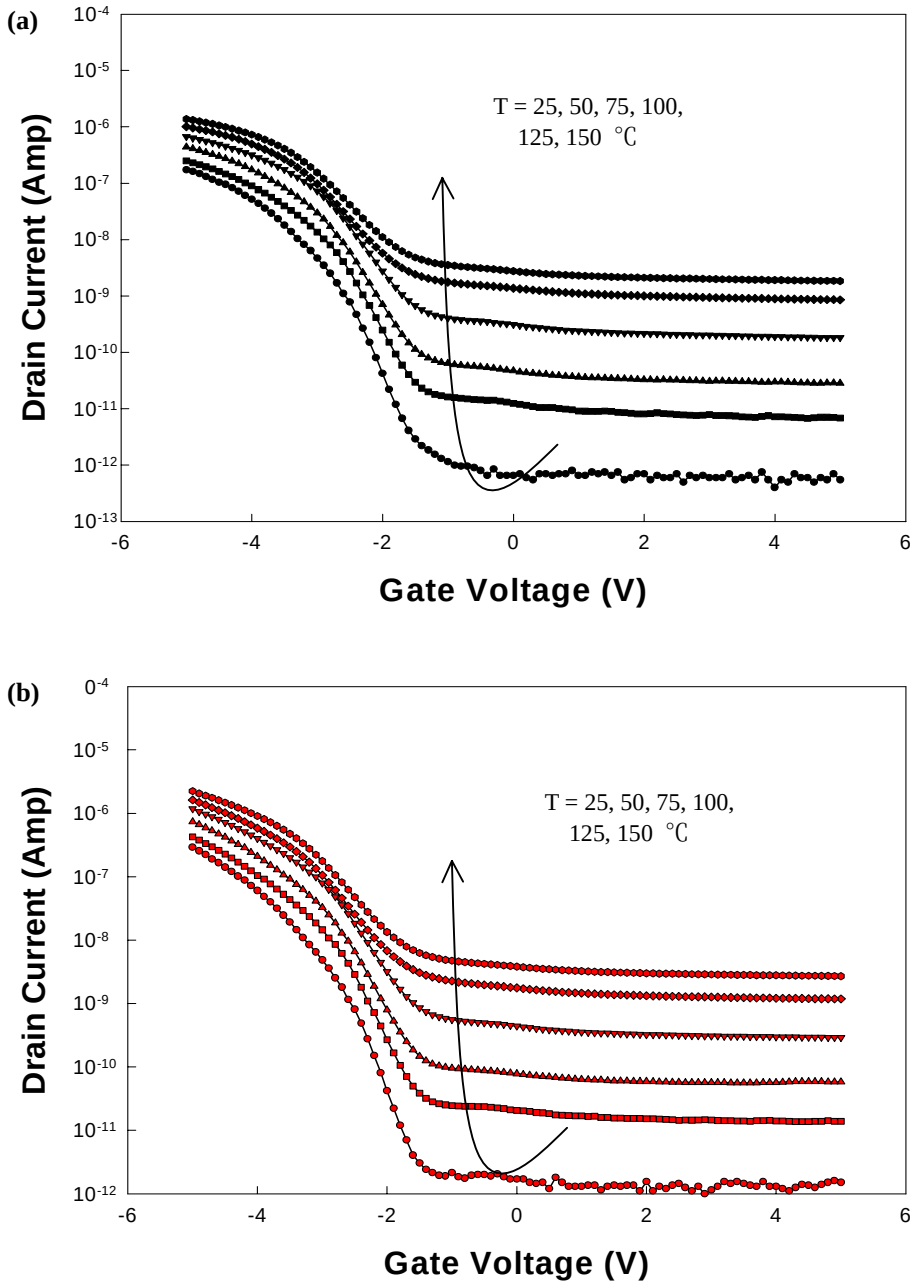


Fig. 3.8 **I_D-V_G characteristics for *p*-channel operation of a SBTFT with FID structure: (a) V_D=-1V; (b) V_D=-3V. Channel length and width are 5 and 20 μm, respectively. X_D is 4μm.**

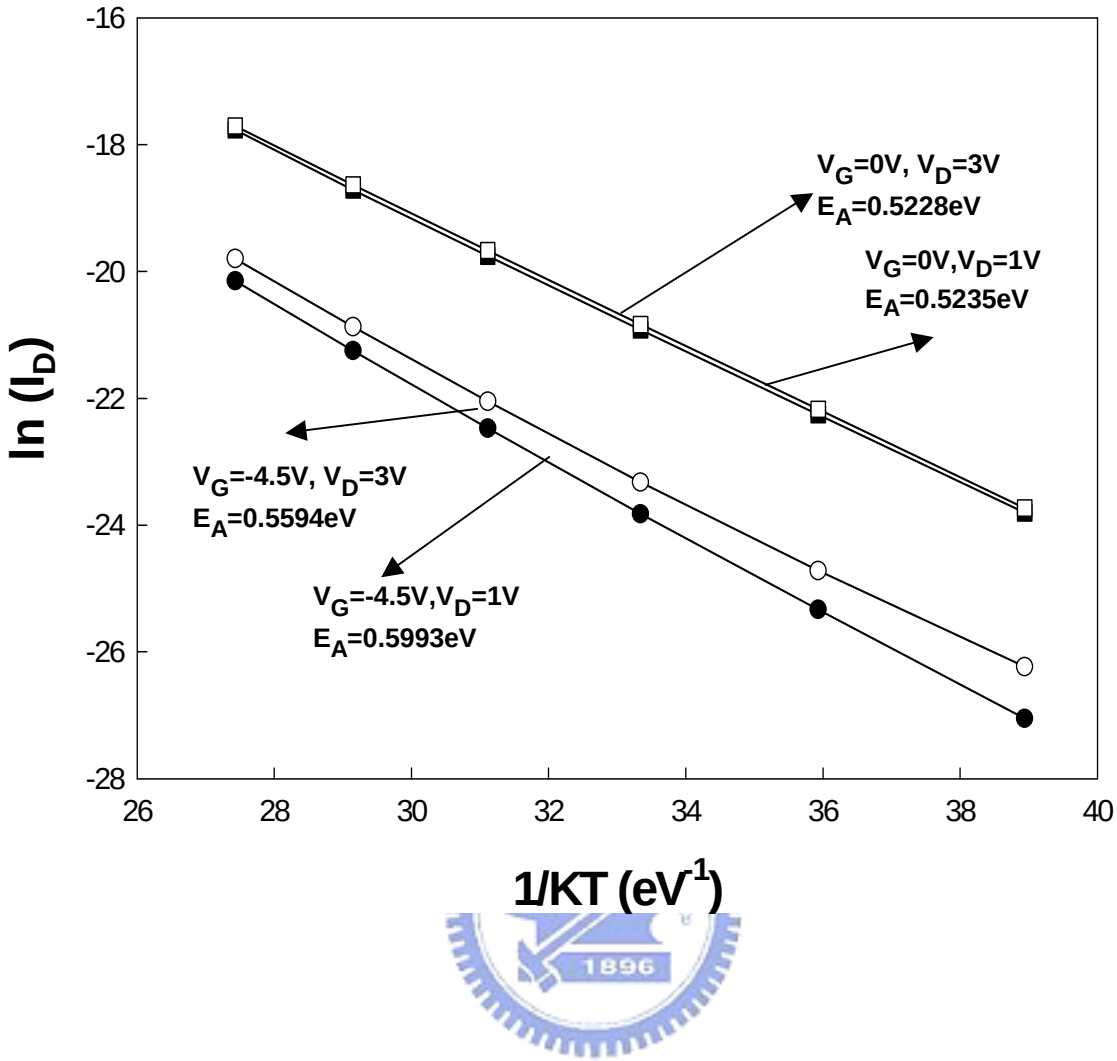


Fig. 3.9 **Arrhenius plots for *n*-channel operation of a SBTFT with FID structure.**

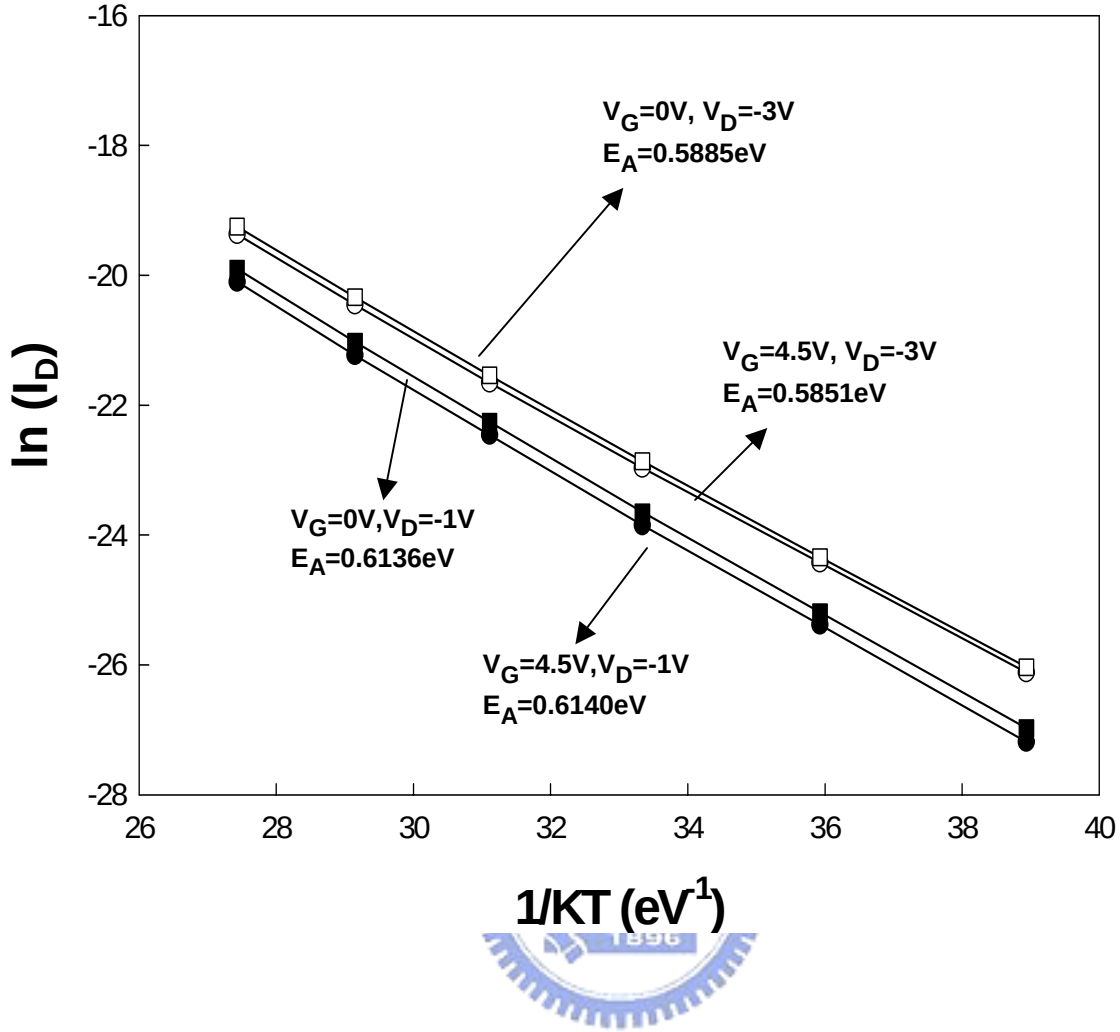


Fig. 3.10 **Arrhenius plots for *p*-channel operation of a SBTFT with FID structure.**

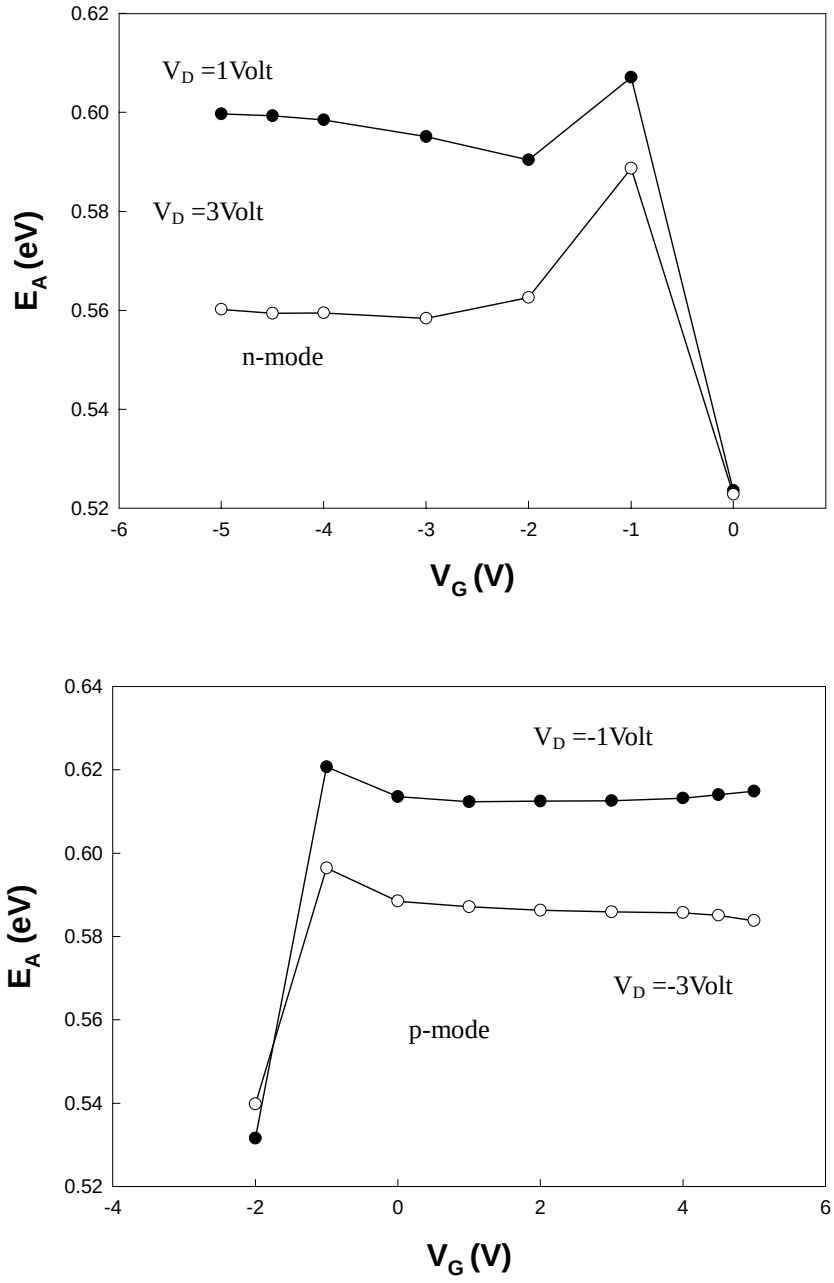


Fig. 3.11 E_A as a function V_G of a SBTFT with FID structure for *n*- (top figure) and *p*-channel (bottom figure) operations.

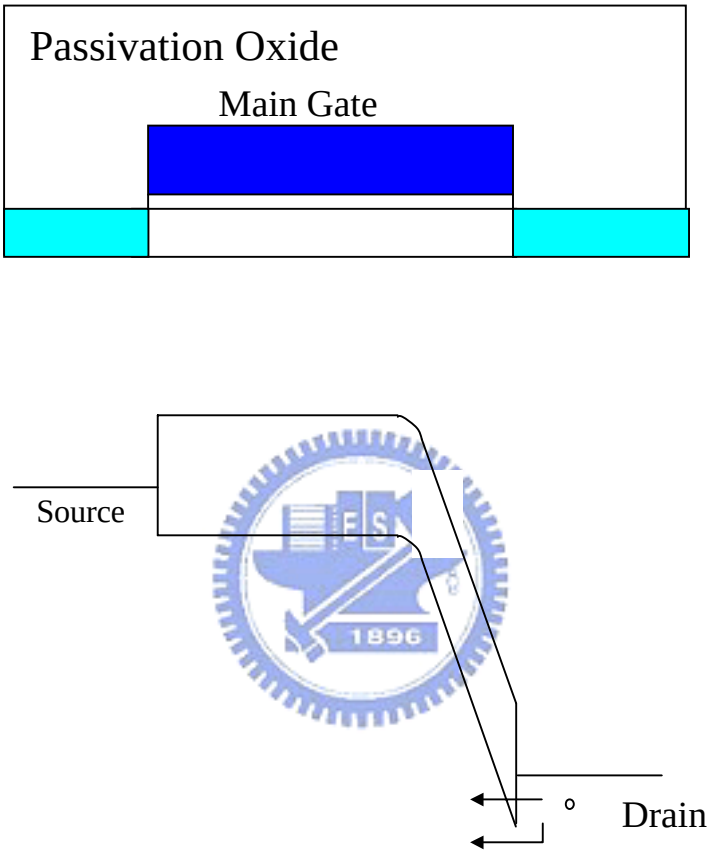


Fig. 3.12 Band diagram for off-state n-channel operation of SBTFT with conventional structure.

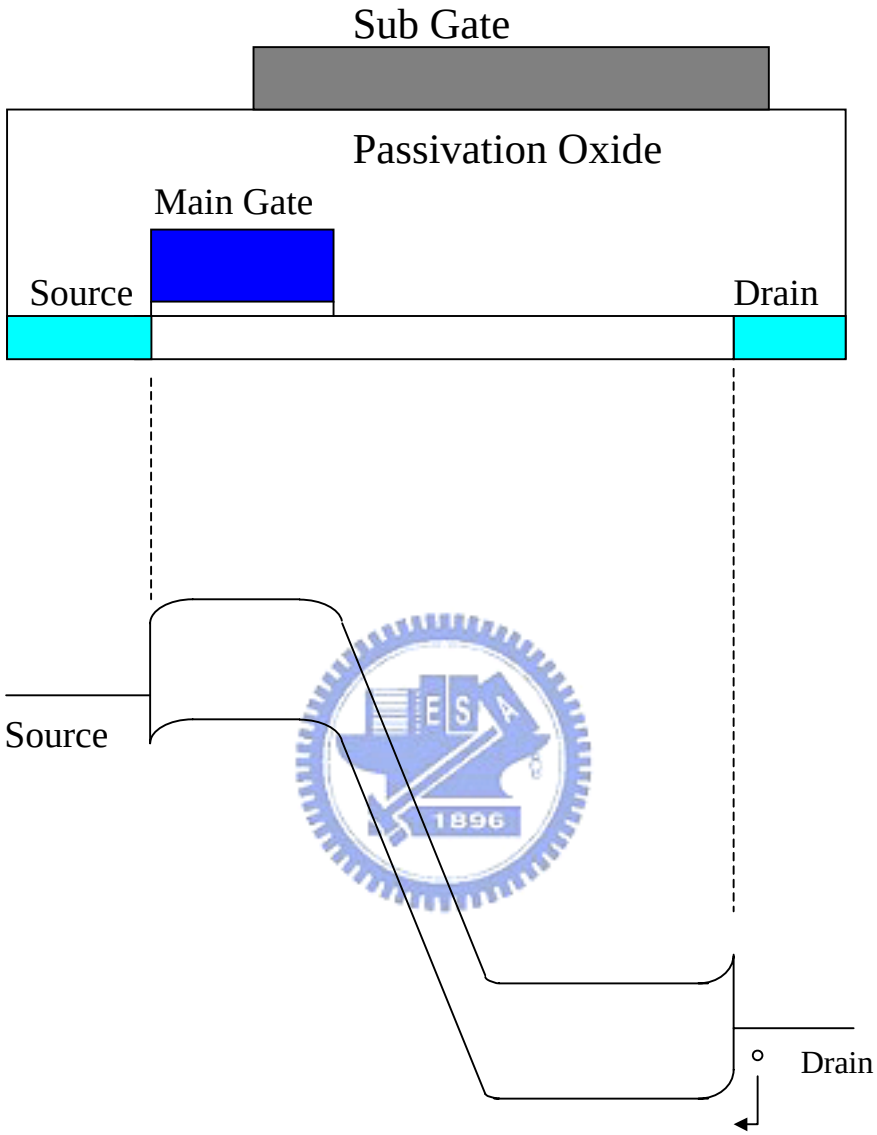


Fig. 3.13 Band diagram for off-state n-channel operation of SBTFT with FID structure.

Chapter 4

Characteristics of SBTFTs with ELA Channel

4.1 Introduction

Our previous experimental results described in previous chapter [1-3] showed that on/off current ratio higher than 10^6 for both p- and n-channel operation could be realized on the SB TFT with FID structure. More importantly, the GIDL-like off-state leakage current that has plagued conventional SBTFTs (i.e., without a field plate, using a sidewall spacer to isolate the source/drain and the gate during silicidation) could be completely suppressed [4-7]. However, the poly-Si channel that was prepared using solid-phase crystallization (SPC) technique in our previous study is known to suffer from the small grain size and large amount of defects at the grain boundaries or inside the grains [8-11]. These defects will no doubt degrade the carrier mobility and increase the off-state leakage [12-17]. On the other hand, excimer laser annealing (ELA) has recently attracted much attention due to the superior properties of the recrystallized thin films. The grains of the ELA poly-Si thin films can be grown as large as several micrometers with proper laser conditions. In addition, by solidification from the molten phase, the intra-grain defects such as stacking faults and microtwins in the ELA poly-Si films are also reduced [18-27]. With these attractive features, ELA has in fact become very popular for manufacturing high-performance poly-Si TFTs.

To further enhance SB device performance, in this study we have fabricated and characterized FID SBTFTs with poly-Si channel layer prepared by ELA. We will compare the device characteristics and investigate the factors that will affect the device operation. Meanwhile, it should be mentioned that, to serve as control we also fabricate SPC channel devices described already in previous chapter. This is because for fair comparison, we have to fabricate the devices in the same lot to cancel out any possible process variations except the channel material preparation.

4.2 Device Structure and Fabrication

A cross-sectional view of the proposed FID SBTFT is depicted in Fig. 4.1. All the process flow

and the operation are essentially the same as those mentioned in the last two chapters. Here, we will only address some key points about the process and film characteristics in this chapter. The structure features an un-doped poly-Si channel layer with an offset channel region, a top field-plate (i.e., the sub-gate) lying on top of the passivation oxide and overlapping the entire offset channel region, and silicide source/drain. X_D is the length of the offset region in the channel. Detailed process flow for fabricating the device can be found in previous chapters. In this study, an amorphous silicon channel layer (50 nm) was deposited at 550℃ by low-pressure chemical vapor deposition (LPCVD), which was subsequently transformed into polycrystalline silicon by either ELA or SPC method. For the split that received ELA treatment, ELA was performed by irradiating the amorphous Si layer with energy density of 250 mJ/cm^2 for 100 shots and 99% overlap. While for the SPC split, wafers were recrystallized at 600℃ in N_2 ambient for 24 hours. Gate oxide (100 nm) and passivation oxide (400 nm) were deposited using PECVD. Co silicide serving as the metallic source/drain of SB TFTs was formed using the self-aligned silicidation (salicide) method. Next, the sub-gate and metal gate deposited and patterned simultaneously. It is worth noting here that all processing steps were done at a temperature no higher than 600 ℃, i.e., it is compatible with mid-temperature active-matrix liquid-crystal display (AMLCD) manufacturing. The overall process thermal budget could be further lowered if the metal-gate processing is adopted.

4.3 Characteristics of SB-TFTs with ELA Channel

4.3.1 Transfer Characteristics of ELA and SPC Samples

Fig. 4.2 and Fig. 4.3 show the ambipolar transfer characteristics of devices with ELA and SPC channel, respectively. These two devices have nominally the same structural parameters and bias conditions. The extracted device parameters are given in Table 4.1. It is worthy to note that the off-state current shown in Fig. 4.2 is comparable to the thermal noise current of the measurement system which is about several tens of fA. This suggests that the actual off-state leakage current of the SBTFTs with ELA channel could be even lower.

With the use of FID, no gate induced drain leakage (GIDL)-like leakage current is observed in both ELA and SPC channels [4-7]. It can be seen that the threshold voltages for p- and n-channel operations are not symmetric (i.e., their absolute values are not comparable), and shift to the more negative side. Such asymmetry can be ascribed to the existence of positive fixed oxide charges at the oxide/channel interface and the work-function of n^+ doped poly-Si main-gate.

Also shown in Fig. 4.2, excellent device performance with steep subthreshold slope and higher than 10^8 on/off current ratio for both p- and n-channel operations are demonstrated, for the first time, on a poly-Si TFT device. These characteristics are much better than those of the device with SPC poly-Si channel, as shown in Fig. 4.3. This is because the grain size of ELA poly-Si films is much larger than that of SPC poly-Si films, and thus ELA poly-Si films have much fewer inter-grain defects. The inter-grain defects would trap carriers when the carriers flow through the grain boundaries. Therefore, the devices with ELA channel have higher channel conductivity and on-state current. In addition, the more defects the channel layer has, the more applied main-gate voltage is needed to overcome the defect sites. This results in the poor subthreshold swing and larger threshold voltage for the devices with SPC channel.

Moreover, the grain boundaries also provide leakage current paths when the devices are turned off. This is why the devices with ELA channel depict much lower off-state current. All the advantages mentioned above indicate that ELA is very effective in enhancing the performance of SBTFTs.

It is also noted in Fig. 4.2 that the on-state current of *p*-channel operation is higher than that of *n*-channel operation. Since the on-state current conduction mechanism is mainly governed by tunneling of carriers through the source-side Schottky barrier, such phenomenon could be ascribed to a lower barrier height for holes (Φ_{Bp}) than for electrons (Φ_{Bn}) at the $CoSi_2$/ Si junction [28].

By contrast, similar trend is not observed in Fig. 4.3 for devices with SPC channels. This can be qualitatively explained as following: Although the barrier height is important for determining the on-current, another important factor that should be taken into account is the tunneling distance. During the on-state operation, most of the voltage drop across the channel would occur near the

source side and affects the tunneling distance, and thus modulates the tunneling distance [29]. For the device having an ideal crystalline channel (i.e., no grain boundaries) and biased with a high drain voltage, the source-side silicide/channel junction will become “transparent”, since the tunneling distance has been reduced significantly so that the carriers could tunnel through freely [29]. Under such condition, the barrier height is important in affecting the conduction current. This case could be applied to the results shown in Fig. 4.2, since the ELA channel has a quality closer to the crystalline channel. On the other hand, since more traps exist in the SPC channel than in the ELA channel, penetration of drain-field would become more difficult for the SPC channel. As a result, the tunneling distance could still be large even when a high drain bias is applied. The effect of barrier height and thus the source-side junction would thus not be as important as for the ELA channel. Instead, the channel resistance of the devices should also be considered for on-state operation of devices having SPC channel. Since it is well known that the mobility of electrons in poly-Si is larger than that of holes, the channel resistance of SBTFTs in the on-state for n-channel operation might be lower than that for p-channel operation. This could explain why the on-state current of the device with SPC channel is higher for n-channel operation.

Note that the transfer curve for p-channel operations shown in Fig. 4.2 depicts two different slopes in the subthreshold region. This phenomenon is not clear at this stage and may be related to the nature of the ELA poly-Si layers used in this work.

4.3.2 Effects of Sub-Gate Bias

It has been shown that the applied sub-gate bias tends to increase the on-state current [4]. This is ascribed to the fact that the sub-gate bias could induce carriers supplying from the source at the offset channel region where the main-gate and silicide source do not overlap. As a result, the sub-gate bias could also modulate the carrier tunneling distance of source-side Schottky barrier during on-state operation and thus the on-state current.

Fig. 4.4 and Fig. 4.5 depict the effects of sub-gate bias on the p- and n-channel operations, respectively, of the FID SBTFT with ELA channel. It is found that the major improvement appears on

the on-state current of n-channel operation. This could be explained by using the qualitative on-state band diagram illustrated in Fig. 4.6. In this figure, we concentrate only on the n-channel operation, though similar explanation could also be deduced for p-channel operation. The major on-state conduction mechanisms include thermionic emission (path (1) in Fig. 4.6) and field emission (path (2) in Fig. 4.6). The key factor affecting thermionic emission is barrier height ϕ_B. On the other hand, both barrier height and tunneling distance (d) are important for field emission. The barrier height for electrons when the device is under n-channel operation in on-state is larger than that for holes when the device is under p-channel operation, and thus the thermionic emission current plays a more important role in on-state current for p-channel operation. This explains why the effect of modulating the tunneling distance at the source-side Schottky barrier is more significant for n-channel operation.

4.3.3 Effects of Main-Channel Length

The p- and n-channel transfer characteristics of ELA-treated FID SBTFTs with a fixed X_D, but with main-channel length ranging from 1 to 5 μm are shown in Fig. 4.7 and Fig. 4.8, respectively. The major differences appear at the subthreshold region and the on-state region of p-channel operation. In contrast, there is very weak dependence on main-channel length for n-channel operation. Since the effect of Schottky junction on n-channel operation is more significant than for p-channel operation owing to larger electron barrier height, it is reasonable that n-channel operation shows less dependence on channel length.

4.3.4 Effects of Channel Offset Length

Fig. 4.9 and Fig. 4.10 show the transfer characteristics of ELA-treated FID SBTFTs with various X_D for the p- and n-channel operation, respectively. For the same reason, the results are similar to the effects of main-channel length that the p-channel operation exhibits higher dependence on X_D.

Nevertheless, in contrast to Fig. 4.7, the effects of X_D have more influence on the on-state current than the subthreshold current in Fig. 4.9. This is because the resistance of offset channel is higher than that of main-channel only when the devices are turned on.

4.4 Conduction Mechanisms for Off-State Leakage

All the transfer characteristics shown in section 4.4 were measured at room temperature (i.e., about 25°C). The off-state leakage currents of devices with ELA channel at room temperature, which are comparable to the thermal noise current of the measurement system, are so low that prevent us from studying the conduction mechanisms of off-state leakage currents. Therefore, we characterize the off-state currents at higher temperature up to 150°C to discuss and identify the conduction mechanisms for off-state leakage currents of devices with ELA channel. The off-state characteristics of devices with SPC channel are also studied to serve as the control.

4.4.1 Devices with Excimer-Laser-Annealed (ELA) Channel

From our previous study in chapter 3, it could be understood that the off-state current of SBTFTs could be ascribed to the combination of field emission and thermionic emission. If the thermionic emission dominates the off-state current, the extracted activation energy (E_A) would be close to the barrier height of Schottky junction. In such case, the activation energy should be independent of the gate voltage. On the other hand, when the field emission dominates the conduction, the extracted activation energy would be much lower than the barrier height of Schottky junction.

The off-state characteristics of the FID SBTFT with ELA channel measured at different temperatures ranging from 50°C to 150°C under n- and p-channel operations are depicted in Fig. 4.11 and Fig. 4.12, respectively. The off-state currents are almost independent of the main-gate bias. This implies that the thermionic emission dominates the leakage conduction mechanisms.

Fig. 4.13 shows the corresponding Arrhenius plots. It should be noted that the off-state currents measured at 50°C are still so low that the thermal noise currents could not be neglected. Thus, the data obtained at 50°C is excluded in the Arrhenius plots. The activation energies extracted from Fig. 4.13 show weak dependence on the drain bias.

The activation energies extracted at different main-gate voltages are shown in Fig. 4.14. It can be seen that the activation energies are weakly dependent on the main-gate bias, except for $V_{main\text{-}gate}$ =

-3 V under n-channel operation where the device is near the subthreshold region. This confirms our deduction that the thermionic emission is the dominant mechanism responsible for the leakage.

Qualitative off-state band diagrams illustrated in Fig. 4.15 are used to explain the above results. For n-channel operation, the high positive bias applied to the sub-gate pins the Fermi level of the offset channel region close to the conduction band edge. Under this situation, the high electric-field region is pulled away from the drain junction, as shown in Fig. 4.15(a). As a result, only holes with sufficient energy can overcome the Schottky barrier. In other words, thermionic emission process, rather than field emission, is the major conduction mechanism. Moreover, since the barrier height is not significantly affected by either the main-gate or drain bias, the activation energies show very weak dependence on the main-gate or drain bias.

Similarly, the high negative bias applied to the sub-gate serves to pin the Fermi level of the offset channel region close to the valence band edge for the p-channel operation, as shown in Fig. 4.15(b). Again, the high electric-field region is pulled away from the drain junction. Only electrons with sufficient energy can overcome the Schottky barrier and contribute to the leakage.

4.4.2 Devices with Solid-Phase-Crystallized (SPC) Channel

Fig. 4.16 and Fig. 4.17 depict n- and p-channel off-state characteristics, respectively, of the FID SBTFT with SPC channel at various temperatures ranging from 25℃ to 150℃. The off-state currents are much larger than those of ELA-treated counterparts. The discussions made in Section 4.4 can be used to explain this phenomenon. The corresponding Arrhenius plots are shown in Fig. 4.18. The activation energies extracted at different main-gate voltages are given in Fig. 4.19. Similar to devices with ELA channel, it can be found that thermionic emission dominates the off-state conduction mechanisms.

It is worthy to note that the extracted activation energies shown in Fig. 4.19 are lower than those in Fig. 4.14 for both n- and p-channel operations. This can be ascribed to the high concentration of deep states within the band gap in SPC poly-Si channel layer. These deep states would pin the Fermi level of the offset channel region at mid-gap, and thus the sub-gate bias could not shift the Fermi level

close to the conduction or valence band edge. Consequently, the barrier height for thermionic emission of devices with SPC channel would be lower than that of devices with ELA channel, as illustrated in Fig. 4.20.

Because ϕ_{Bp} is lower than ϕ_{Bn} at the $CoSi_2$/ Si junction, it can be seen in Fig. 4. 14 and Fig. 4.19 that the activation energies for n-channel operation is lower than those for p-channel operation.

4.5 Summary

FID SBTFT devices with ELA poly-Si active channel were successfully fabricated and characterized in this thesis. Excellent device performance in terms of steep subthreshold slope and on/off current ratio higher than 10^8 for both p- and n-channel operations are demonstrated, for the first time, on a single poly-Si TFT device.

Source-side tunneling process is found to be important for on-state device operation, especially for the n-channel operation that has a larger barrier height. On the other hand, it is identified that the thermionic emission process is the major conduction mechanism responsible for the off-state leakage current.

The stellar performance with on/off current ratio larger than 10^8 for both n- and p-channel modes of operation, together with its inherent ambipolar capability, implantless process, low thermal budget, and simplified CMOS integration scheme, make this kind of device a very promising candidate for future AMLCDs and system-on-panel (SOP) applications.

References :

[1] H. C. Lin, C. Y. Lin, K.L. Yeh, R.G. Huang, M.F. Wang, C.M. Yu, T. Y. Huang, and S. M. Sze, "A Novel Implantless MOS Thin-Film Transistor with Simple Processing, Excellent Performance and Ambipolar Operation Capability," IEDM Tech. Dig., 2000, pp. 857-859.

[2] H. C. Lin, K.L. Yeh, R.G. Huang, and T. Y. Huang, "Schottky Barrier Thin-Film Transistor (SBTFT) with Silicided Source/drain and Field-Induced Drain Extension," IEEE Electron Device Lett., vol. 22, pp. 179-181, 2001.

[3] H. C. Lin, K.L. Yeh, R.G. Huang, T. Y. Huang, and S. M. Sze, "Ambipolar Schottky Barrier Thin-Film Transistor (SBTFT)," IEEE Trans. Electron Devices, vol. 49, pp. 264-270, 2002.

[4] K.L. Yeh, H. C. Lin, R.G. Huang, R. W. Tsai, and T. Y. Huang, "Reduction of Off-State Leakage Current in Schottky Barrier Thin-Film Transistors (SBTFT) by a Field-Induced Drain," to appear in the Jpn. J. Appl. Phys., April, 2002.

[5] H. C. Lin, Kuan-Lin Yeh, R.G. Huang, and T. Y. Huang, "Impacts of Field-Induced Drain (FID) on the Ambipolar Operation of Poly-Si Schottky Barrier Thin-Film Transistors (SBTFT's)", Proc. Active–Matrix Liquid-Crystal Display (AM-LCD), 2001, pp. 247-250.

[6] K. L. Yeh, H. C. Lin, R. G. Huang, R. W. Tsai, and T. Y. Huang, "Conduction mechanisms for off-state leakage Current of Schottky Barrier thin-film transistors", *Appl. Phys. Lett.,* Vol.79, pp.635-637, 2001.

[7] K. L. Yeh, H. C. Lin, R. G. Huang, R. W. Tsai, and Tiao-Yuan Huang:" Conduction Mechanisms for Off-State Leakage Current of Schottky Barrier Thin-Film Transistors (SBTFT)" SSDM, pp.273, Tokyo, Japan (September. 2001)

[8] Shunji Seki, Osamu Kogure and Bunjiro Tsujiyama, "Effects of crystallization on trap state densities at grain boundaries in polycrystalline silicon," IEEE Electron Device Lett., vol.8, no.8, August 1987, p.368-370.

[9] T. J. King, M. G. Hack and I-Wei Wu, "Effective density-of-states distributions for accurate modeling of polycrystallization-silicon thin-film transistors," J. Appl. Phys., vol.75, no.2, 15 January 1994, p.908-913.

[10] K. Nakazama, "Recrystallization of amorphous silicon films deposited by low-pressure chemical vapor deposition from Si_2H_6 gas," J. Appl. Phys. Vol.69, pp.1703, 1991.

[11] T. Vouttsas and M. K. Hatalis, “Deposition and crystallization of a-Si low-pressure chemical vapor deposited films obtained by low-temperature pyrolysis of disiline,” J. Electronchem. Soc., vol.140, pp.871-877, 1993.

[12] W. G. Hawkins, “Polycrystalline-silicon device technology for large-area electronics,” IEEE Trans. Electron Device, vol.33, p.477, 1986.

[13] J. G. Fossum, A. O. Conde, H. Shichijo and S. K. Banerjee, “Anomalous leakage current in LPCVD polysilicon MOSFETs,” IEEE Trans. Electron Device, vol.33, p.1518, 1986.

[14] T. I. Kamins and Marcoux, “Hydrogenation of transistors fabricated in polycrystalline-silicon films,” IEEE Electron Device LETT., vol.1, no.8, pp.159-161, 1980.

[15] I-Wei Wu, Alan G. Lewis, Tiao-Yuan Huang, Warren B. Jackson, and Anne Chiang, “Mechanism and device-to-device variation of leakage current in polysilicon thin film transistors,” in IEDM Tech. Dig., 1990, pp.867-870.

[16] K. R. Olasupo, M. K. Hatalis, “Leakage current mechanism in sub-micron polysilicon thin-film transistors,” IEEE Trans Electron Devices, vol.43, pp.1218-1223, 1996.

[17] M. Lack, I-W. Wu, T. J. King, A. G. Lewis, “Analysis of leakage currents in poly-silicon thin film transistors,” in IEDM Tech. Dig., 1993, pp. 385-388.

[18] K. Shimizu, O. Sugiura, and M. Matsumura: IEEE Trans. Electron Devices, vol. 40, pp. 112, 1993.

[19] Laser Annealing of Semiconductors, edited by J. M. Poate and J. W. Mayer (Academic Press, New York, 1982).

[20] Y. F. Tang, S. R. P. Silva, and M. J. Rose, “Super sequential lateral growth of Nd:YAG laser crystallized hydrogenated amorphous silicon,” Appl. Phys. Lett., vol.78, pp.186-188, 2001.

[21] Akito Hara, Fumiyo Takeuchi, Michiko Takei, Katsuyuki Suga, Kenichi Yoshino, Mitsuru Chida, Yasuyuki Sano, and Nobuo Sasaki, “High-performance polycrystalline silicon thin film transistors on non-alkali glass produced using continuous wave laser lateral crystallization,” Jpn. J. Appl. Phys., Part 2, vol.41, pp. L311-L313, 2002.

[22] Bohuslav Rezek, Christoph E. Nebel, and Martin Stutzmann, “Polycrystalline silicon thin films

produced by interference laser crystallization of amorphous silicon," Jpn. J. Appl. Phys., Part 2, vol. 38, pp. L1083-L1084, 1999.

[23] Y. Helen, R. Dassow, M. Nerding, K. Mourgues, F. Raoult, J. R. Kohler, T. Mohammed-Brahim, R. Rogel, O. Bonnaud, J. H. Werner, and H. P. Strunk, "High mobility thin film transistors by Nd:YVO4-laser crystallization," Thin Solid Films, vol. 383, pp. 143-146, 2001.

[24] P. M. Smith, P. G. Carey, and T. W. Sigmon, "Excimer laser crystallization and doping of silicon films on plastic substrates," Appl. Phys. Lett., vol.70, pp. 342-344, 1997.

[25] S. D. Brotherton, D. J. McCulloch, J. P. Gowers, J. R. Ayres, C. A. Fisher, and F. W. Rohlfing, "Excimer laser crystallization of poly-Si TFTs for AMLCDs," Mat. Res. Soc. Symp. Proc., vol. 621, Q7.1.1-Q7.1.12, 2000.

[26] James S. Im, H. J. Kim, and Michael O. Thompson, "Phase transformation mechanisms involoved on excimer laser crystallization of amorphous silicon films," Appl. Phys. Lett., vol. 63, pp. 1969-1971, 1993.

[27] James S. Im and H. J. Kim, "On the super lateral growth phenomenon observed in excimer laser-induced crystallization of thin Si films," Appl. Phys. Lett., vol.64, pp.2303-2305, 1994.

[28] S. M. Sze, *Physics of semiconductor devices, 2ed*, p.279

[29] B. Winstead, U. Ravaioli, "Simulation of Schottky Barrier MOSFETs with a Coupled Quantum Injection/Monte Carlo Technique," IEEE Trans. Electron Devices, vol.47, pp.1241-1246, 2000.

	Fig. 3.1 (ELA sample)		Fig. 3.2 (SPC sample)	
	n-channel	p-channel	n-channel	p-channel
S.S. (V/dec.)	0.193	0.132	1.5	1.1
I_{on}	2.68 μA	26 μA	608 nA	73.8 nA
I_{off}	< 10 fA	< 10 fA	2.69 pA	3.39 pA
I_{on}/I_{off}	$> 2.68 \times 10^{8}$	$> 2.6 \times 10^{9}$	2.26×10^{5}	2.18×10^{4}

Table 4.1 The extracted characteristic parameters of Fig. 4.2 and Fig. 4.3

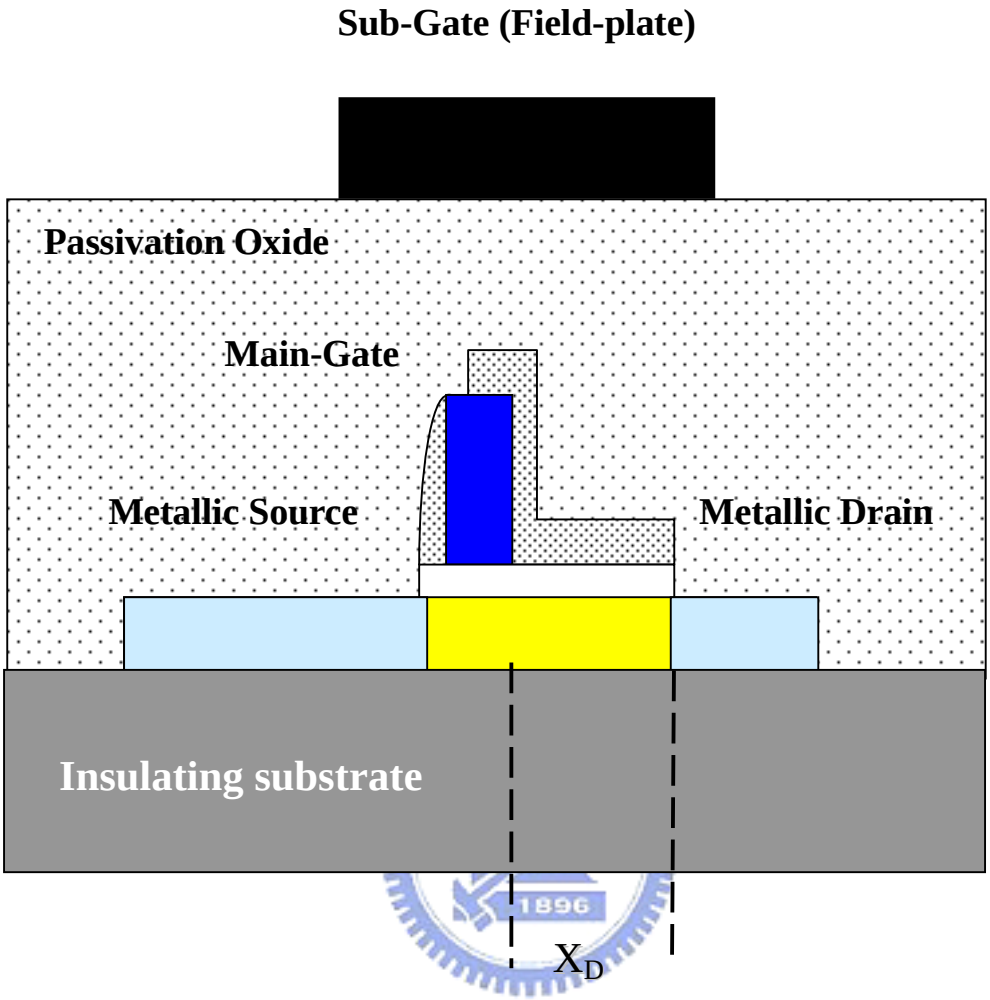


Fig. 4.1 **Cross section of FID SBTFT.**

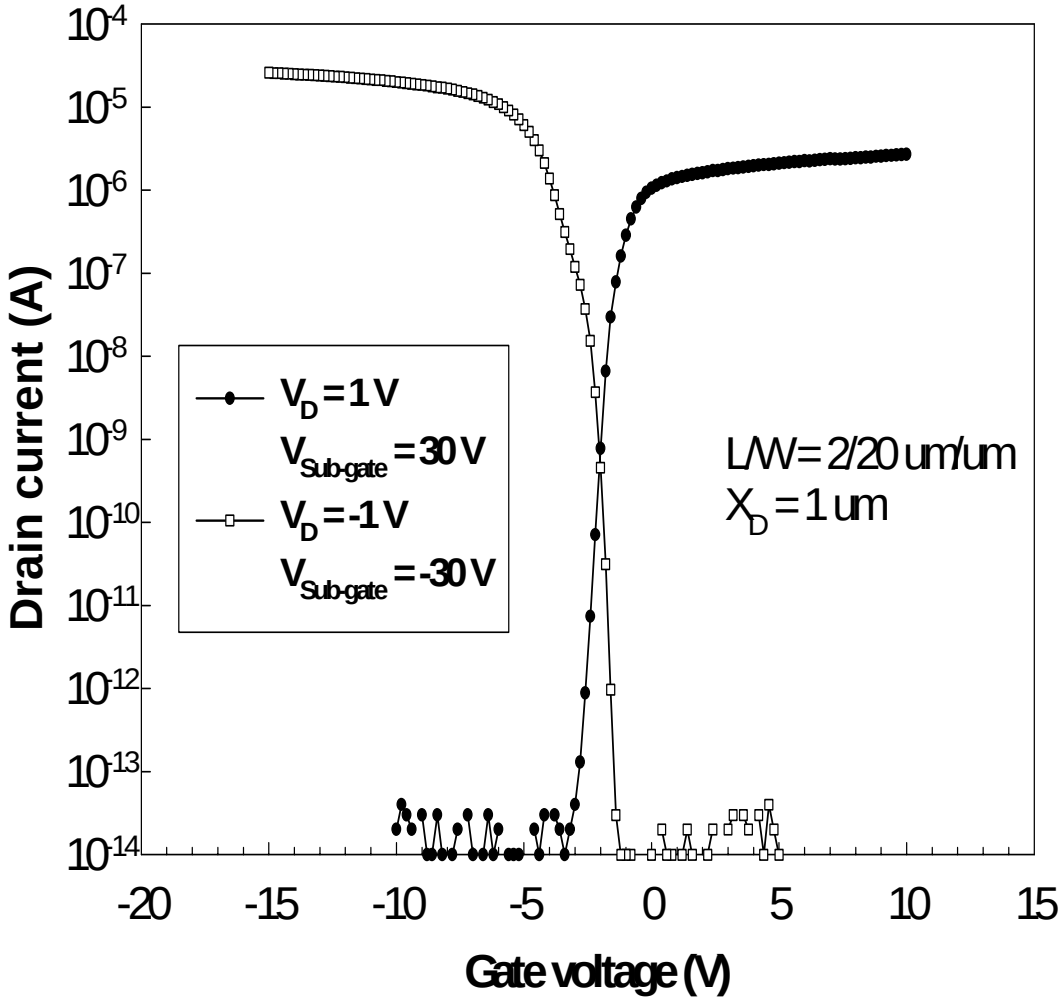


Fig. 4.2 **Ambipolar transfer characteristics of FID SBTFT with ELA channel.**

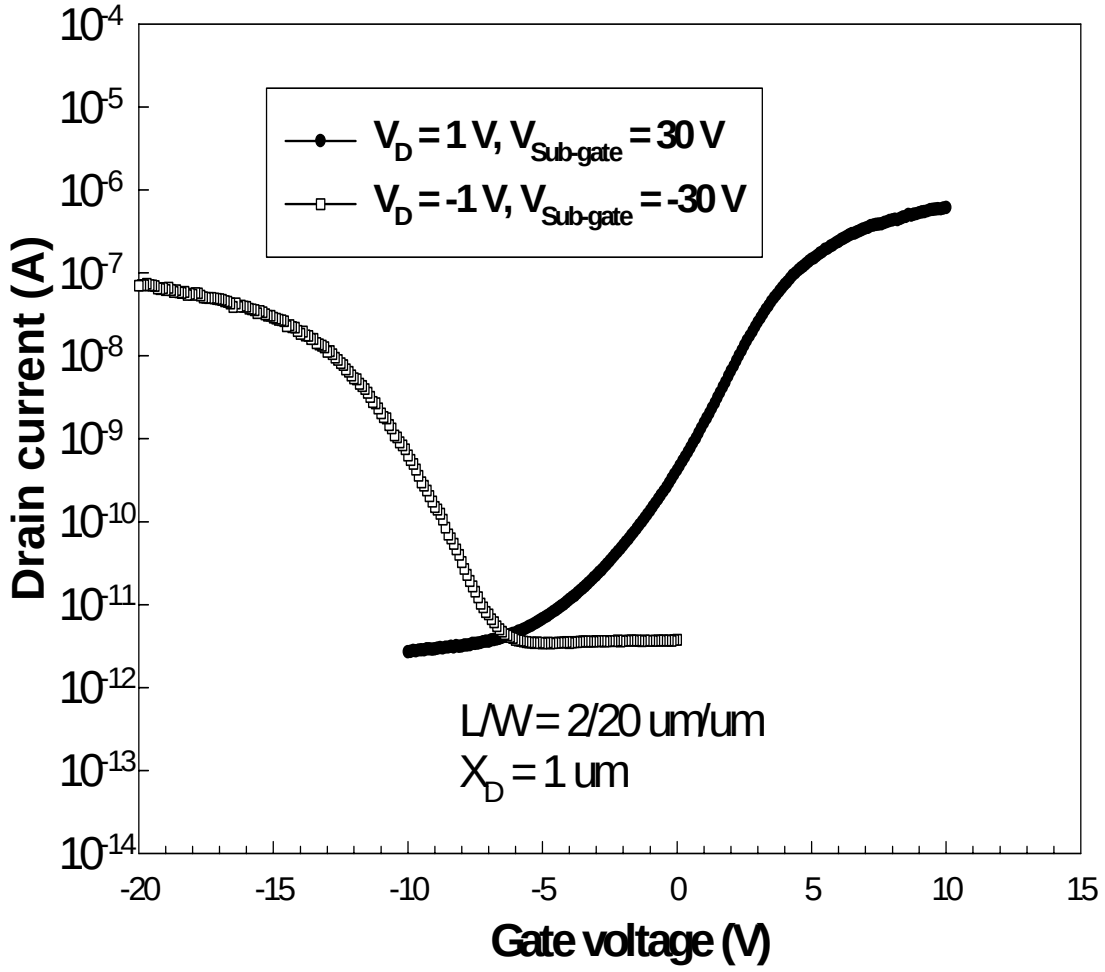


Fig. 4.3 **Ambipolar transfer characteristics of FID SBTFT with SPC channel.**

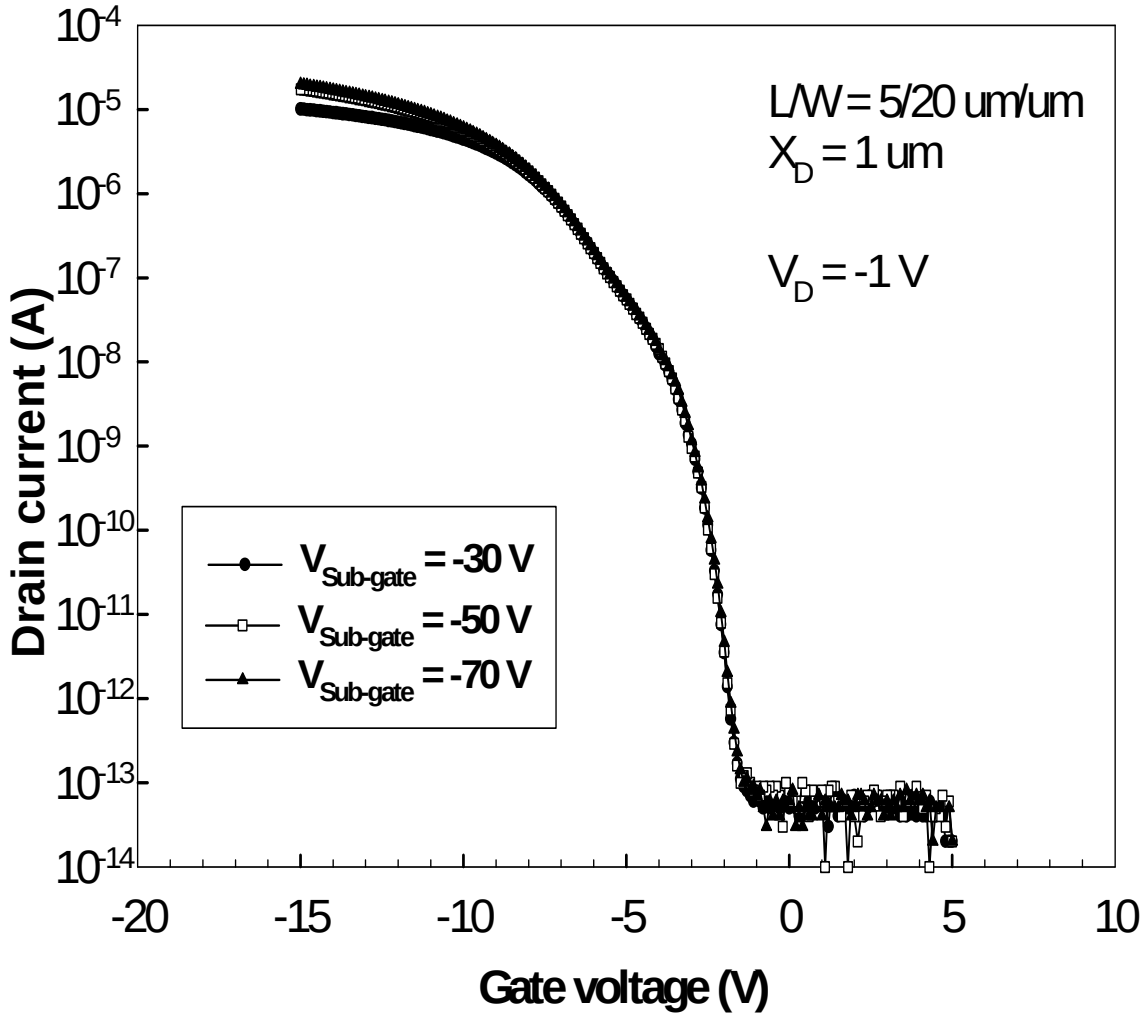


Fig. 4.4 **Effects of sub-gate bias on p-channel operation of FID SBTFT with ELA channel.**

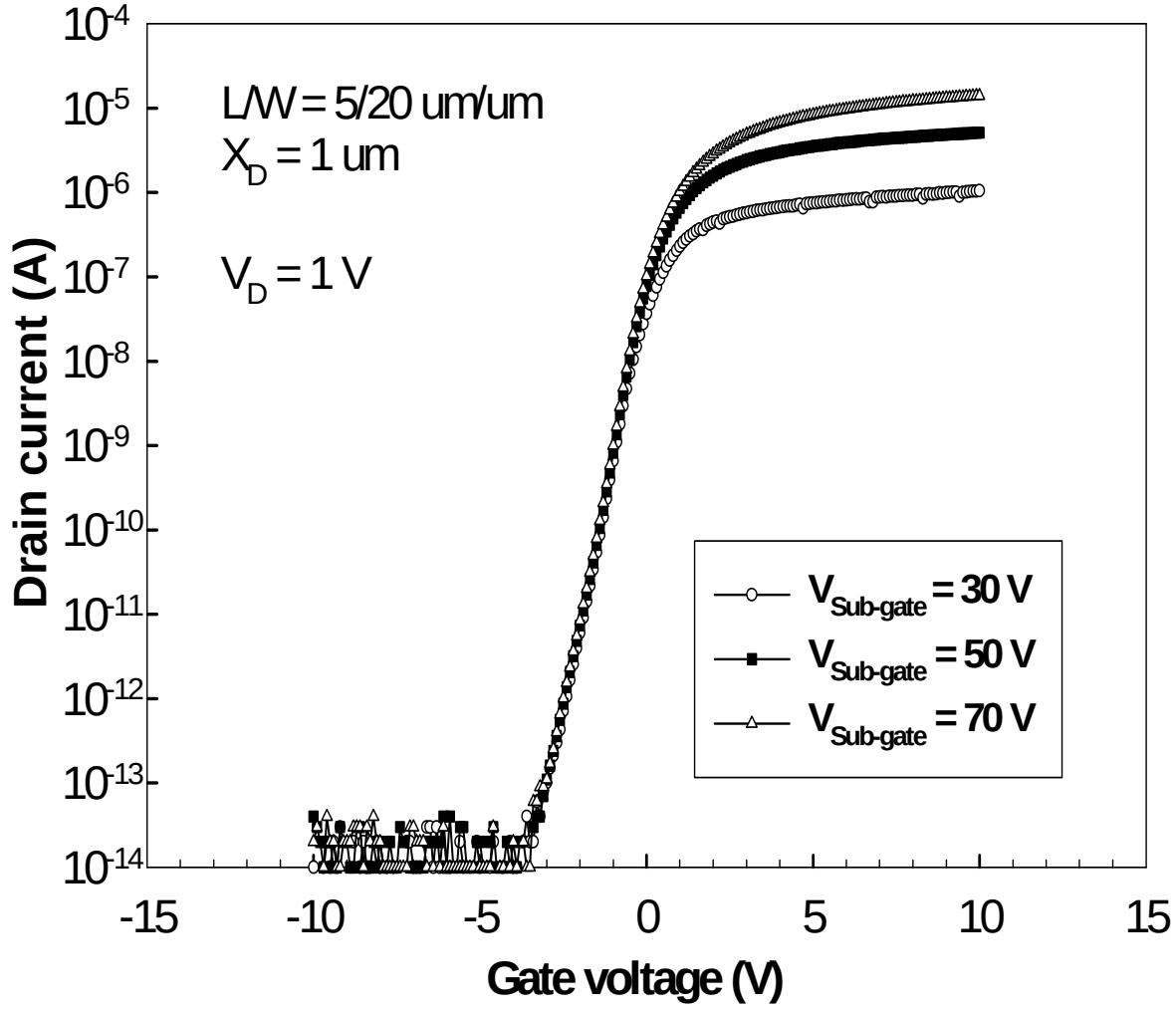


Fig. 4.5 **Effects of sub-gate bias on n-channel operation of FID SBTFT with ELA channel.**

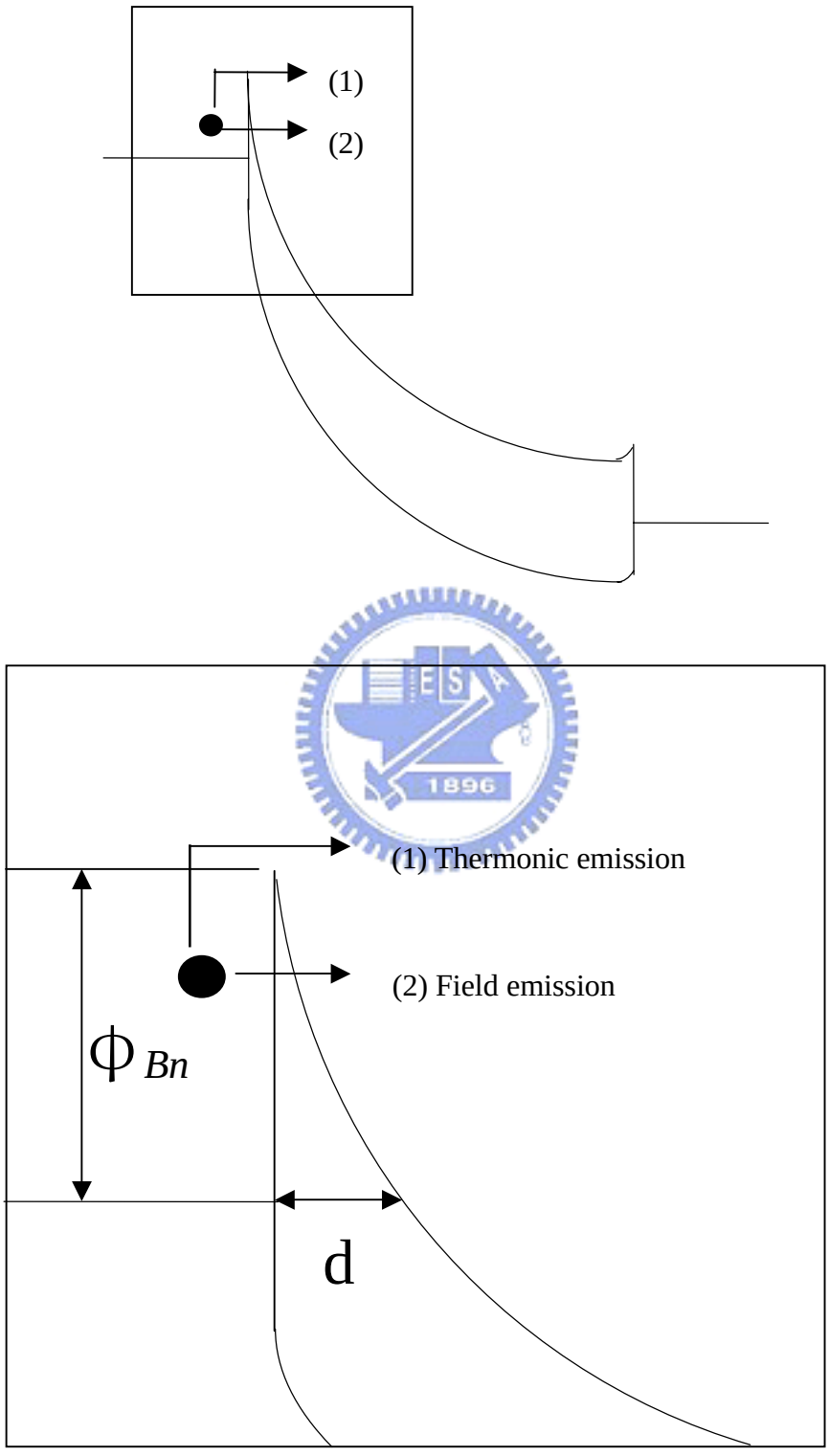


Fig. 4.6 **Qualitative on-state band diagram for n-channel operation.**

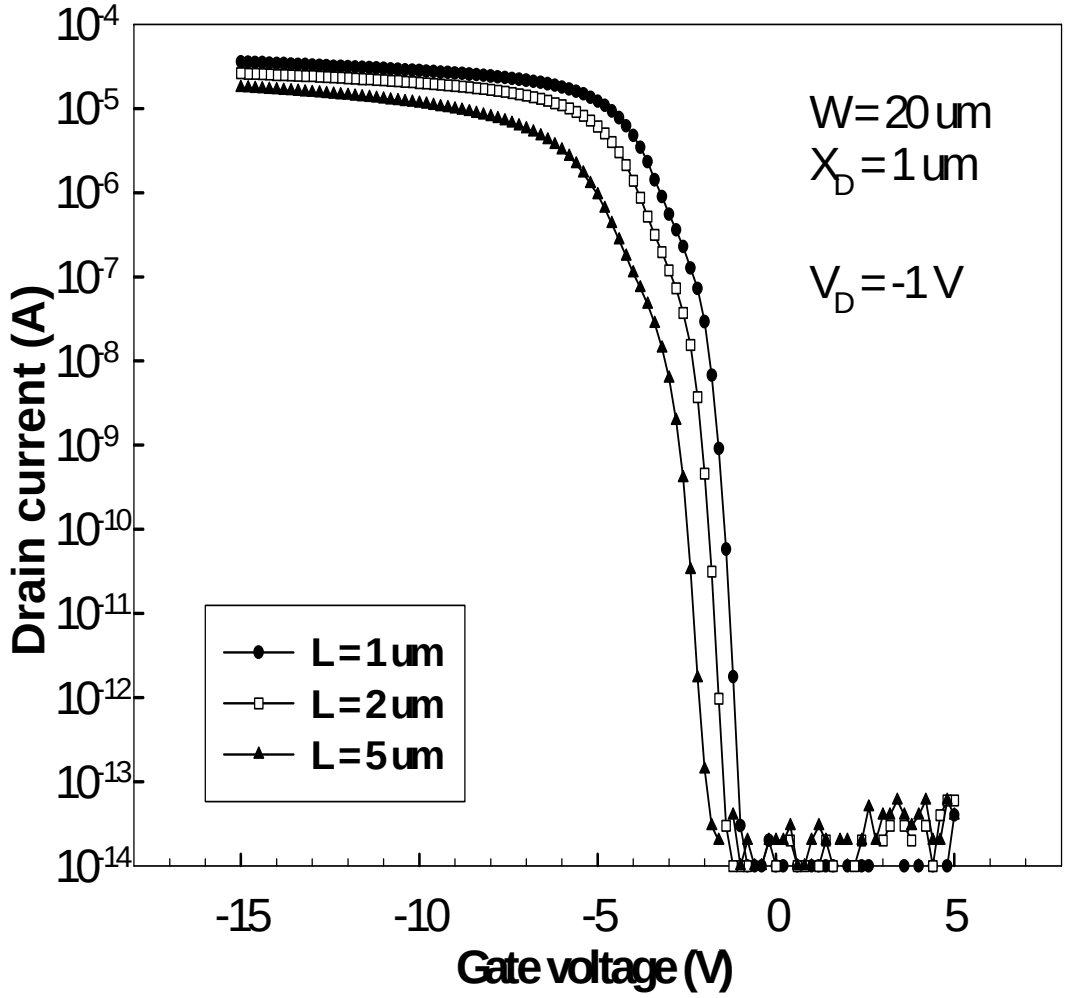


Fig. 4.7 **Effects of main-channel length on p-channel operation of FID SBTFT with ELA channel.**

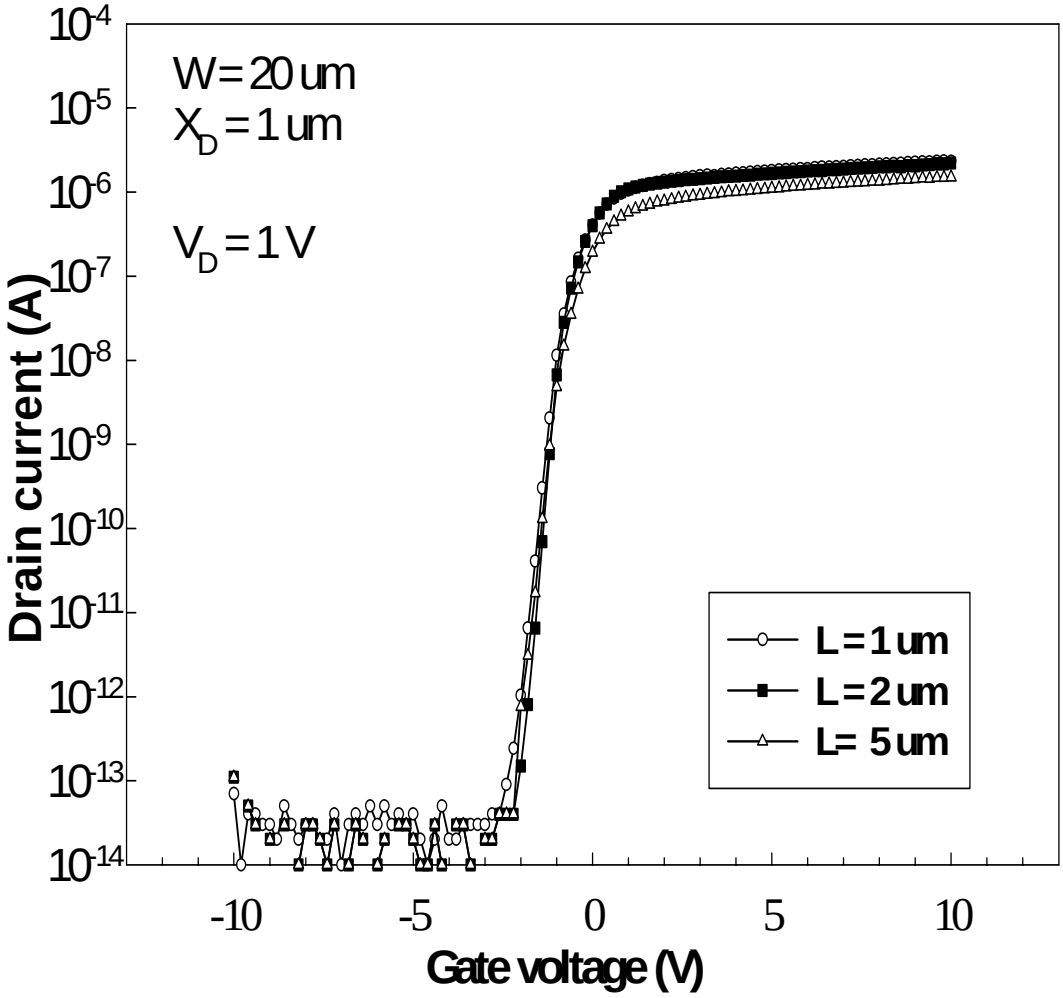


Fig. 4.8 **Effects of main-channel length on n-channel operation of FID SBTFT with ELA channel.**

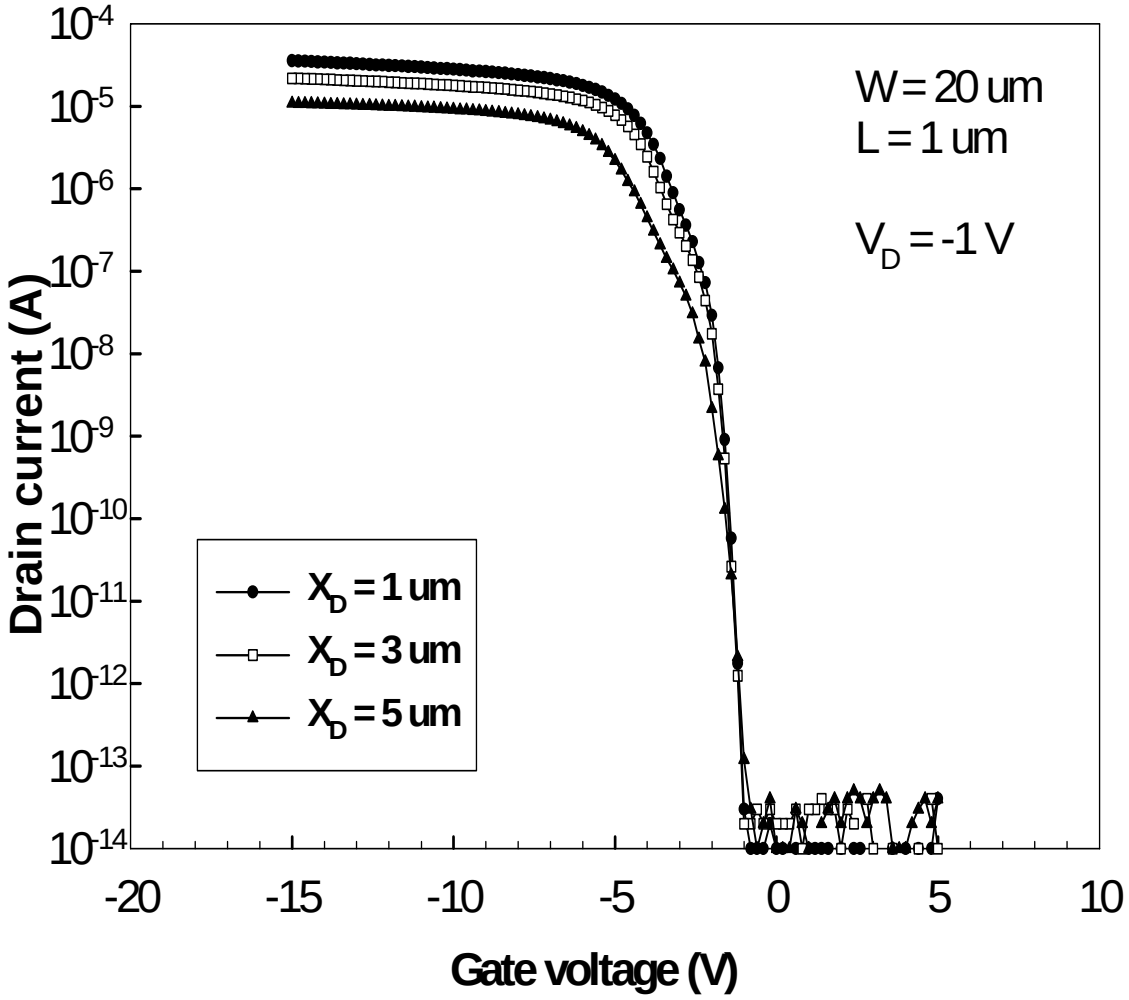


Fig. 4.9 **Effects of offset-channel length on p-channel operation of FID SBTFT with ELA channel.**

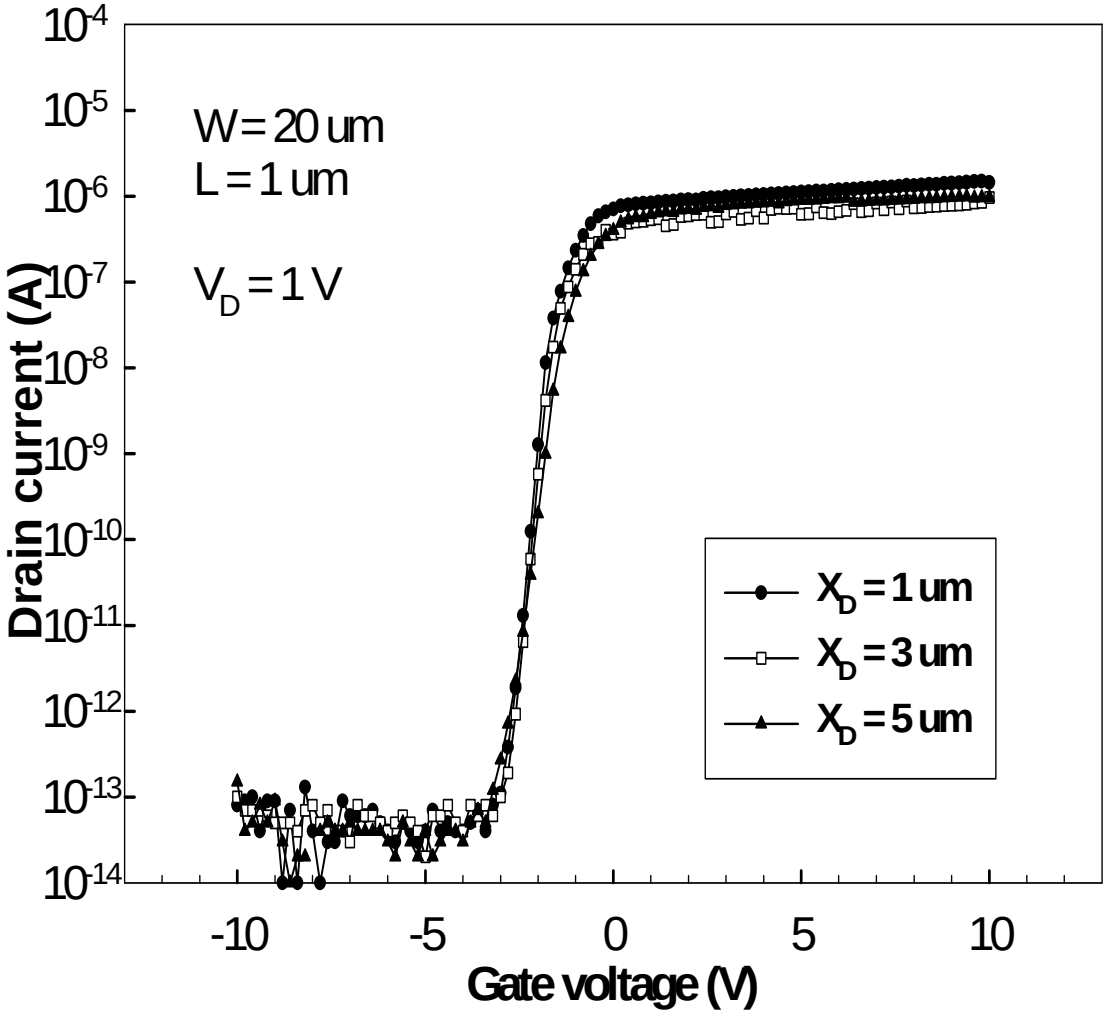
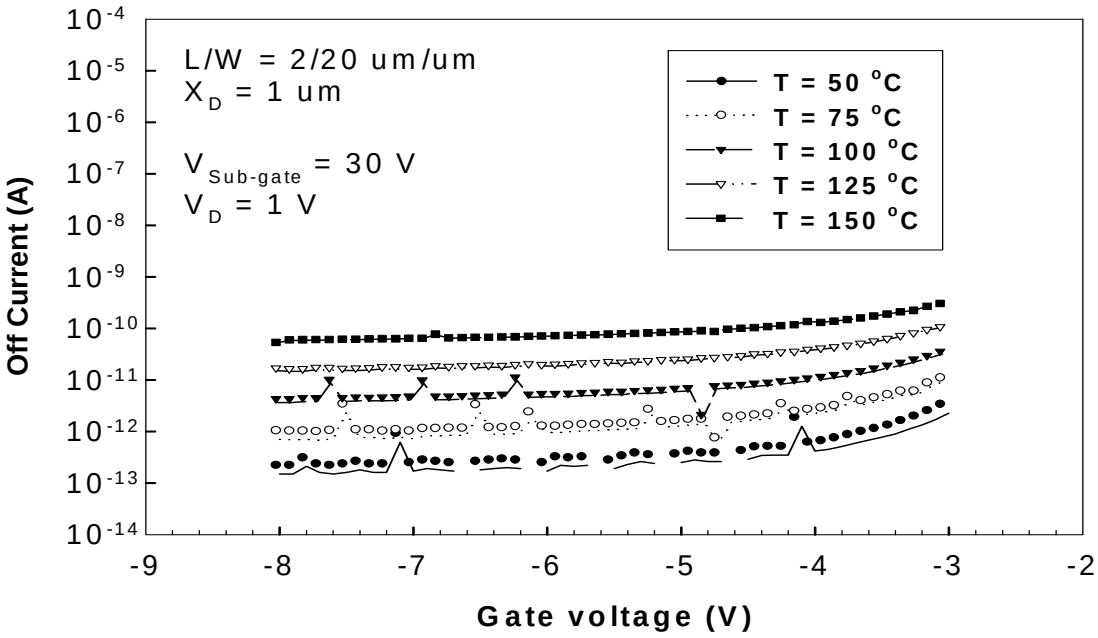
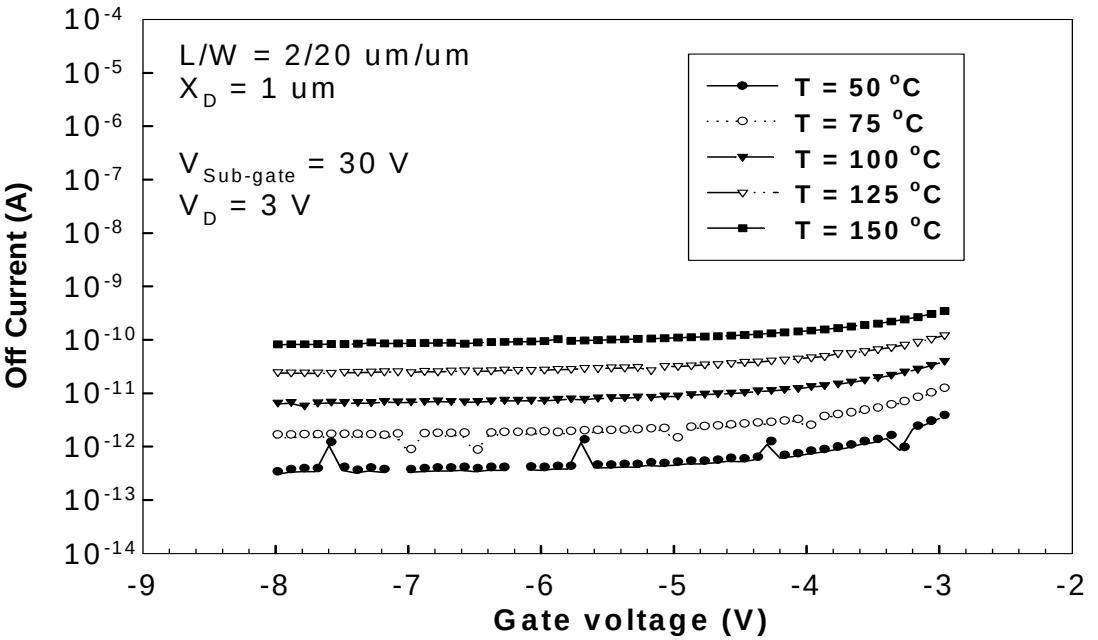


Fig. 4.10 **Effects of offset-channel length on n-channel operation of FID SBTFT with ELA channel.**

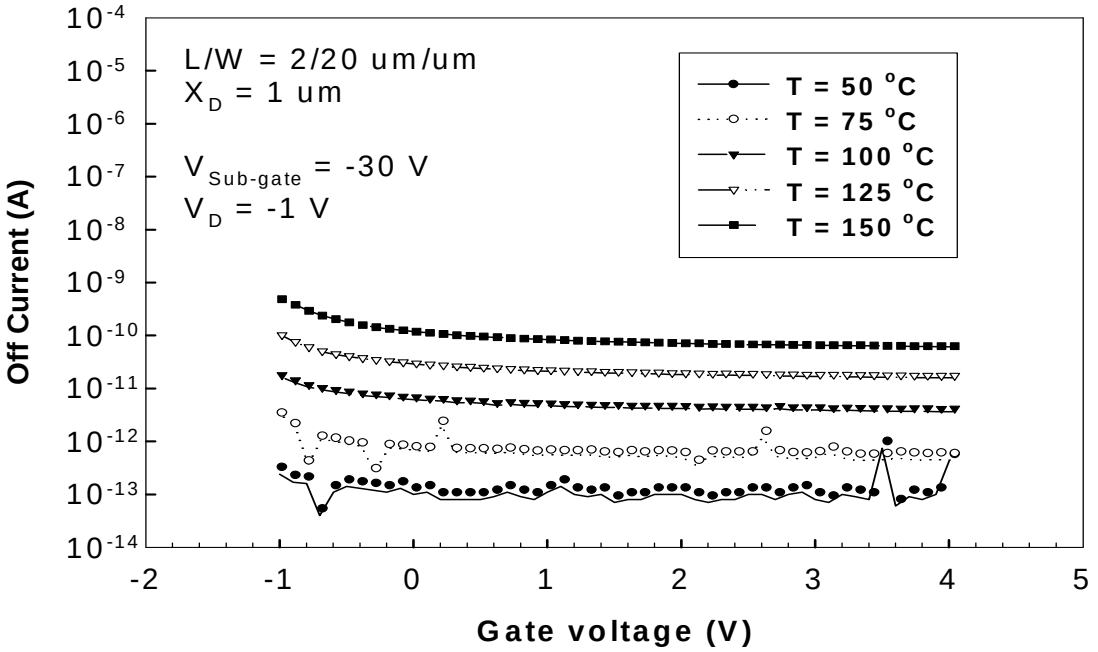


(a)

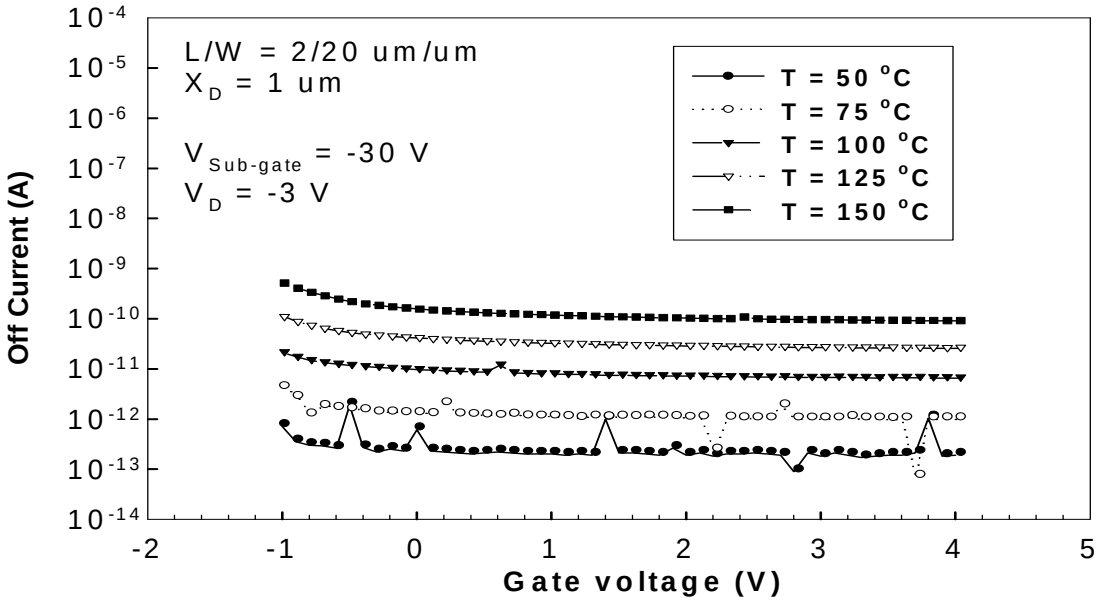


(b)

Fig. 4.11 **Off-state characteristics of FID SBTFT with ELA channel at different temperatures under n-channel operation (a) V_D = 1 V and (b) V_D = 3 V.**

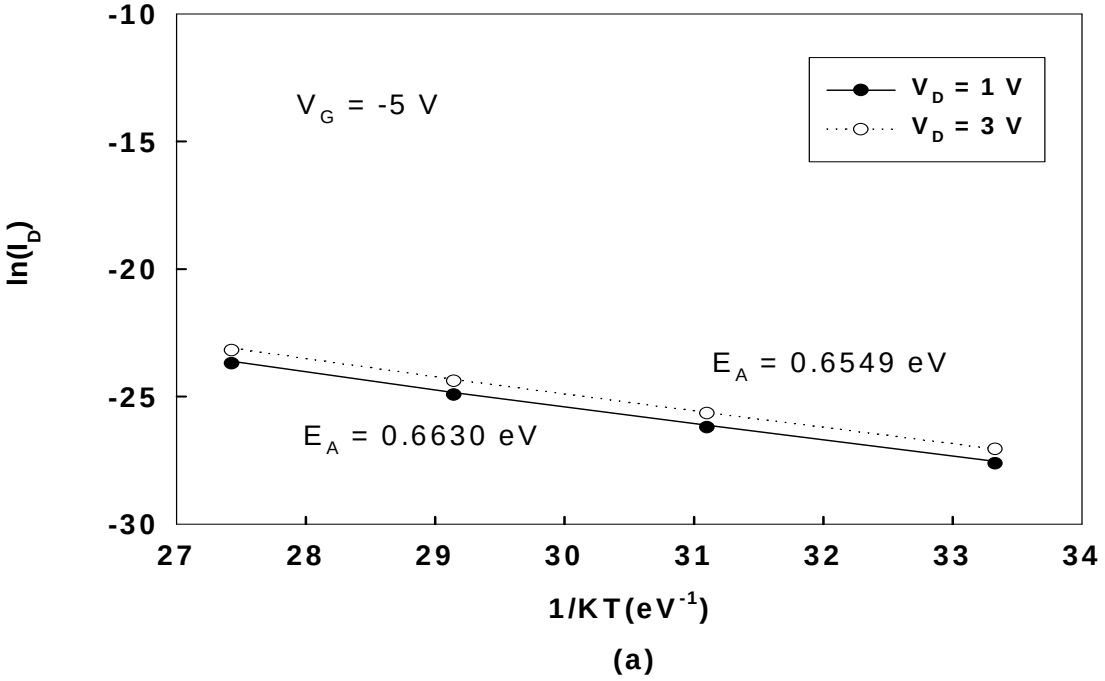


(a)



(b)

Fig. 4.12 **Off-state characteristics of FID SBTFT with ELA channel at different temperatures under p-channel operation (a) V_D = -1 V and (b) V_D = -3 V.**



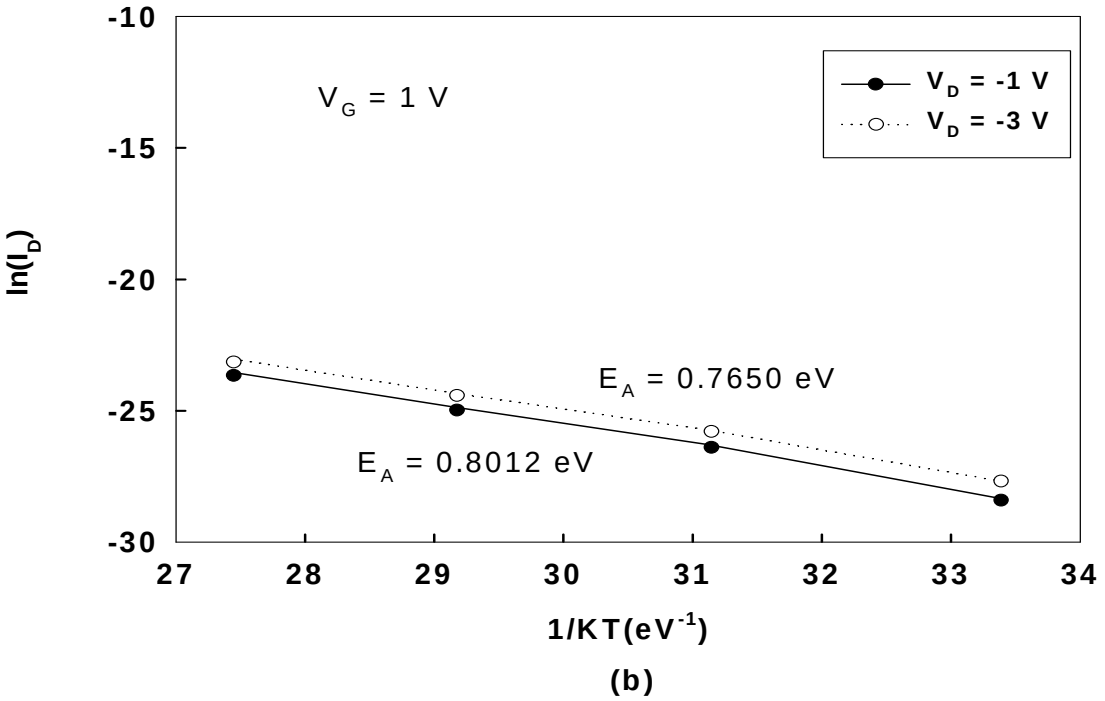


Fig. 4.13 **Arrhenius plots of FID SBTFT with ELA channel under (a) n- and (b) p-channel operations.**

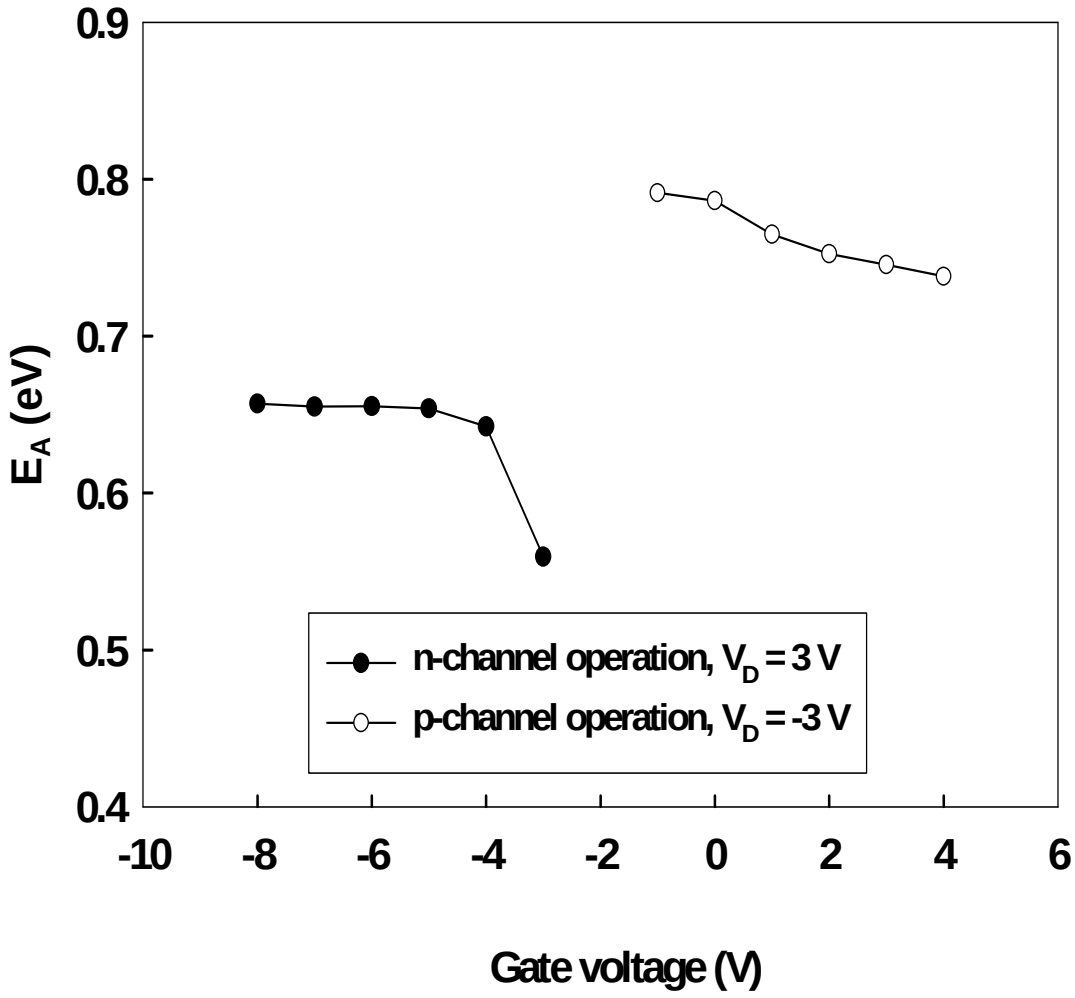


Fig. 4.14 **Activation energies extracted at different main-gate voltages of FID SBTFT with ELA channel.**

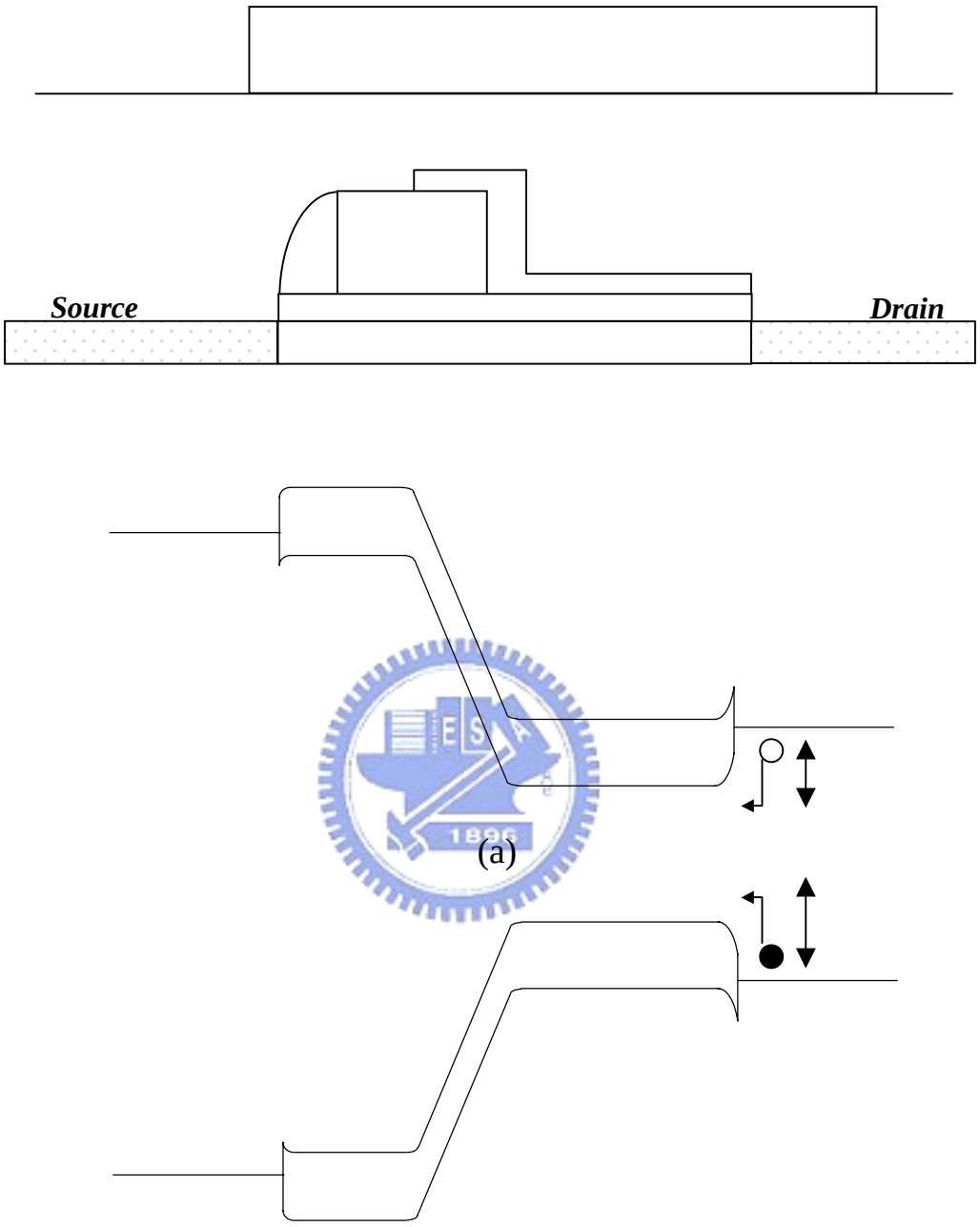


Fig. 4.15 **Qualitative off-state band diagrams for (a) n-channel operation and (b) p-channel operation.**

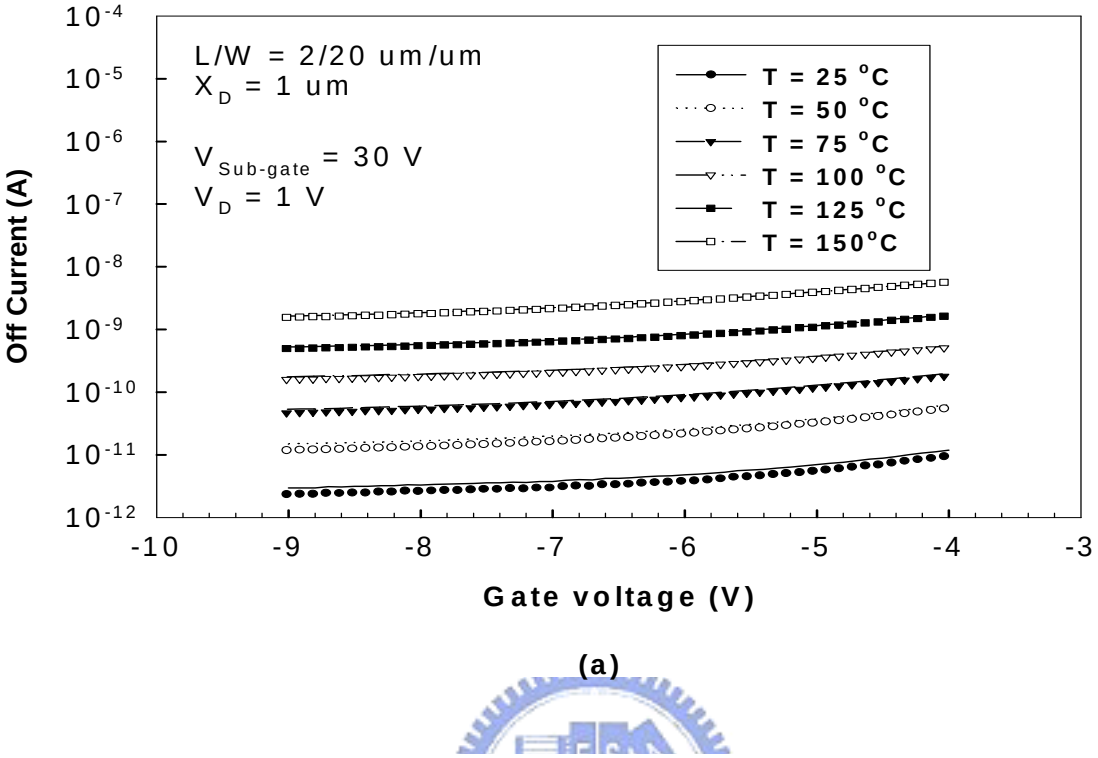
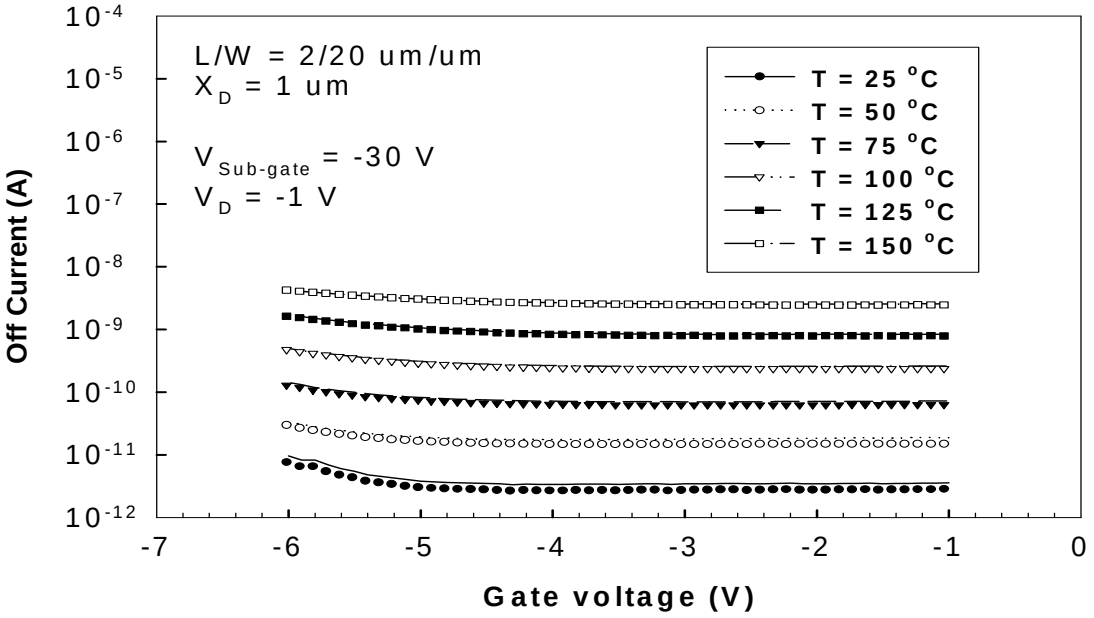
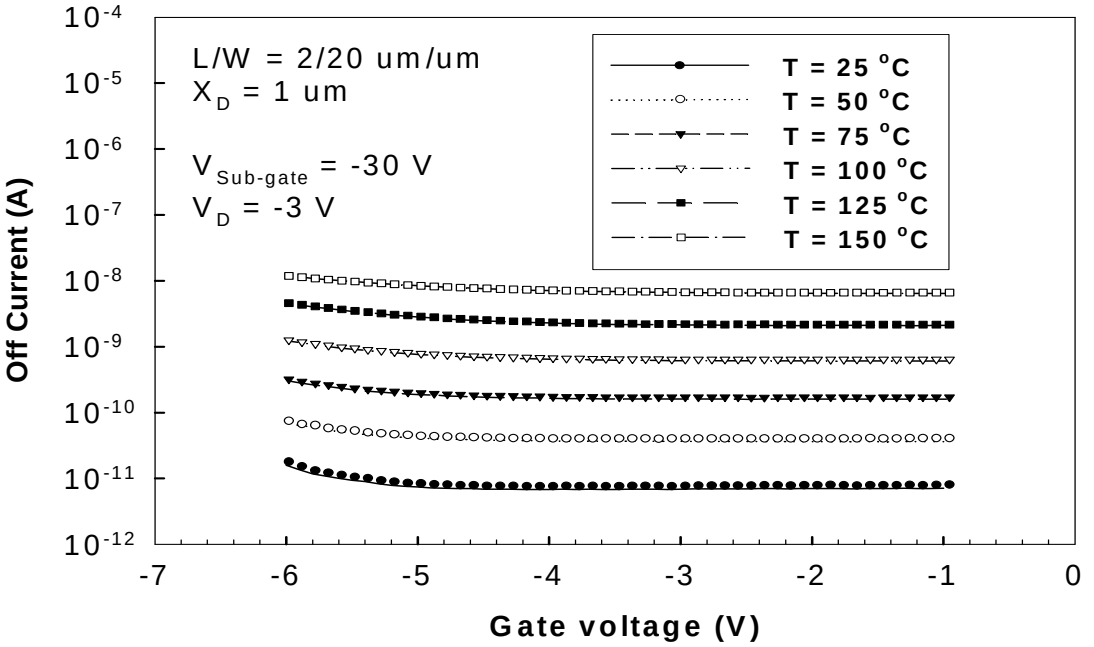


Fig. 4.16 **Off-state characteristics of FID SBTFT with SPC channel at different temperatures under n-channel operation (a) V_D = 1 V and (b) V_D = 3 V.**

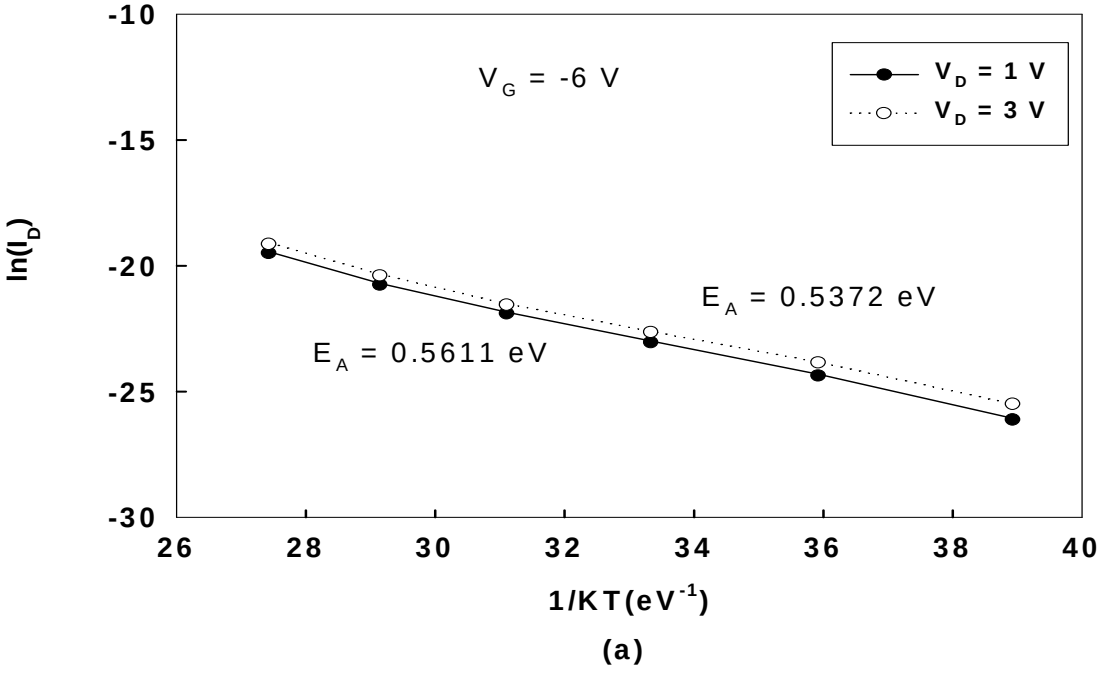


(a)



(b)

Fig. 4.17 **Off-state characteristics of FID SBTFT with SPC channel at different temperatures under p-channel operation (a) V_D = -1 V and (b) V_D = -3 V.**



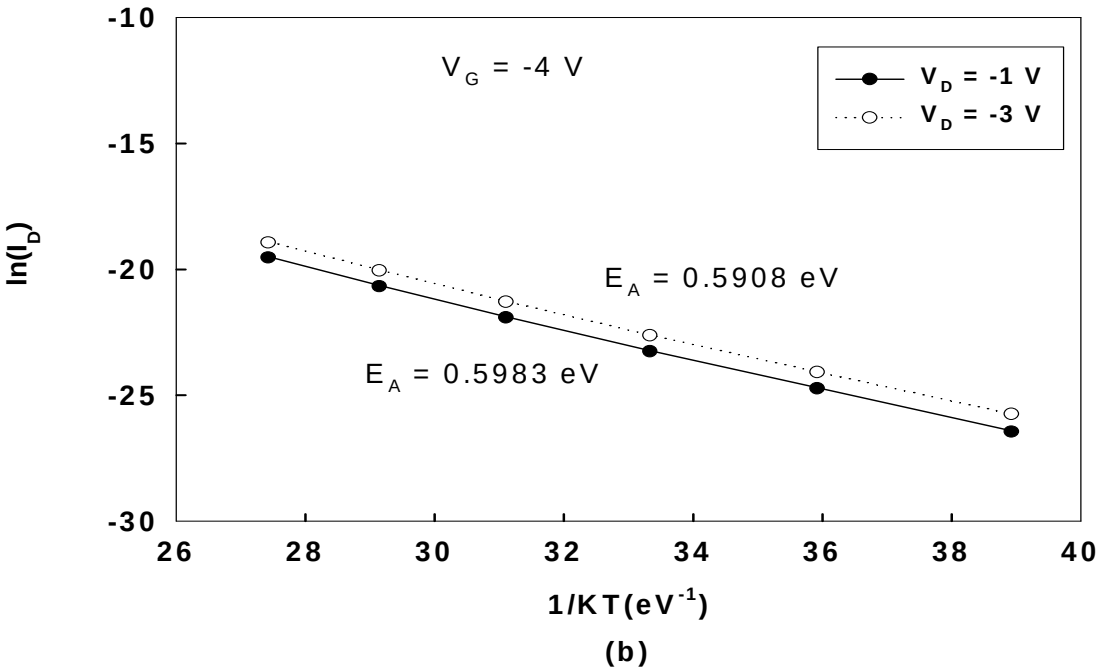


Fig. 4.18 **Arrhenius plots of FID SBTFT with SPC channel under (a) n- and (b) p-channel operations.**

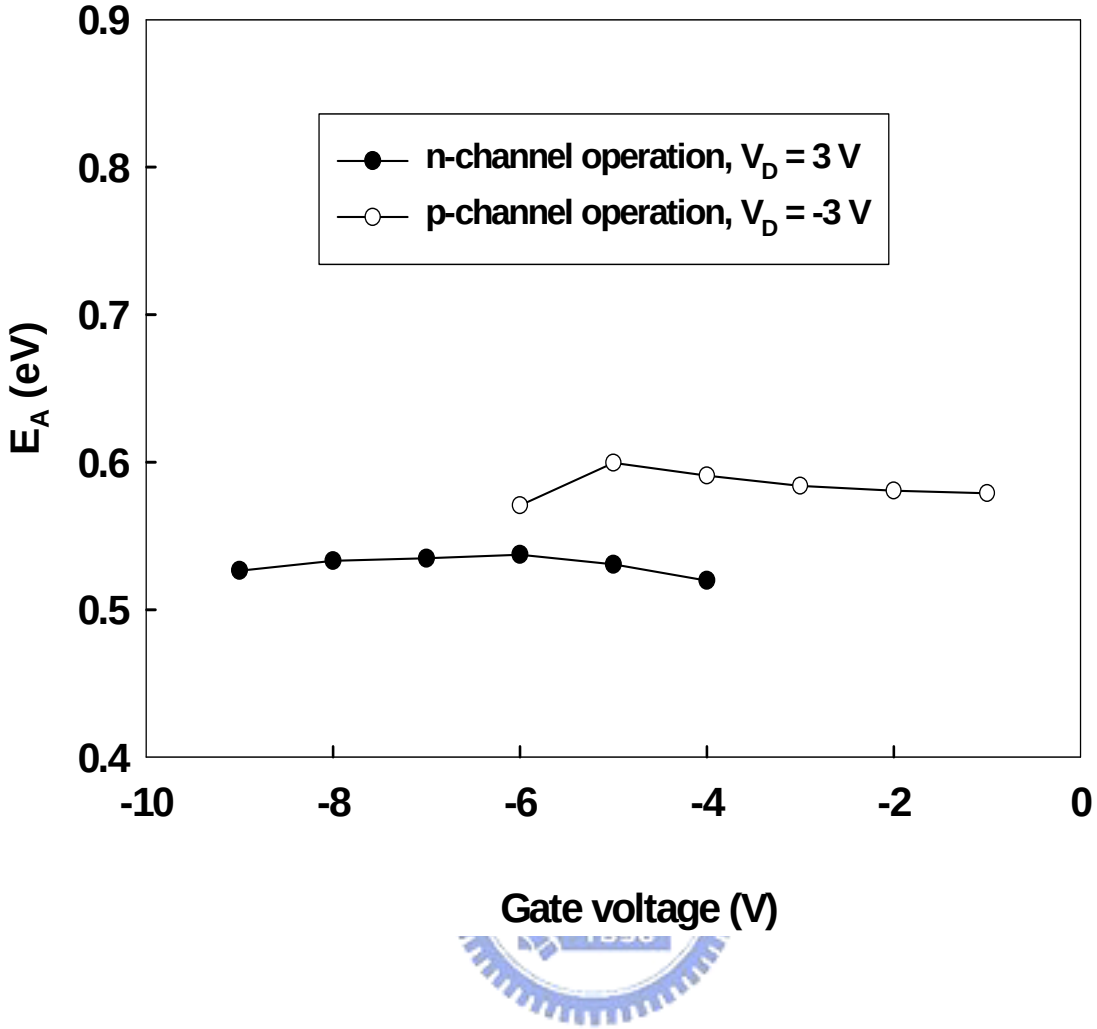


Fig. 4.19 **Activation energies extracted at different main-gate voltages of FID SBTFT with SPC channel.**

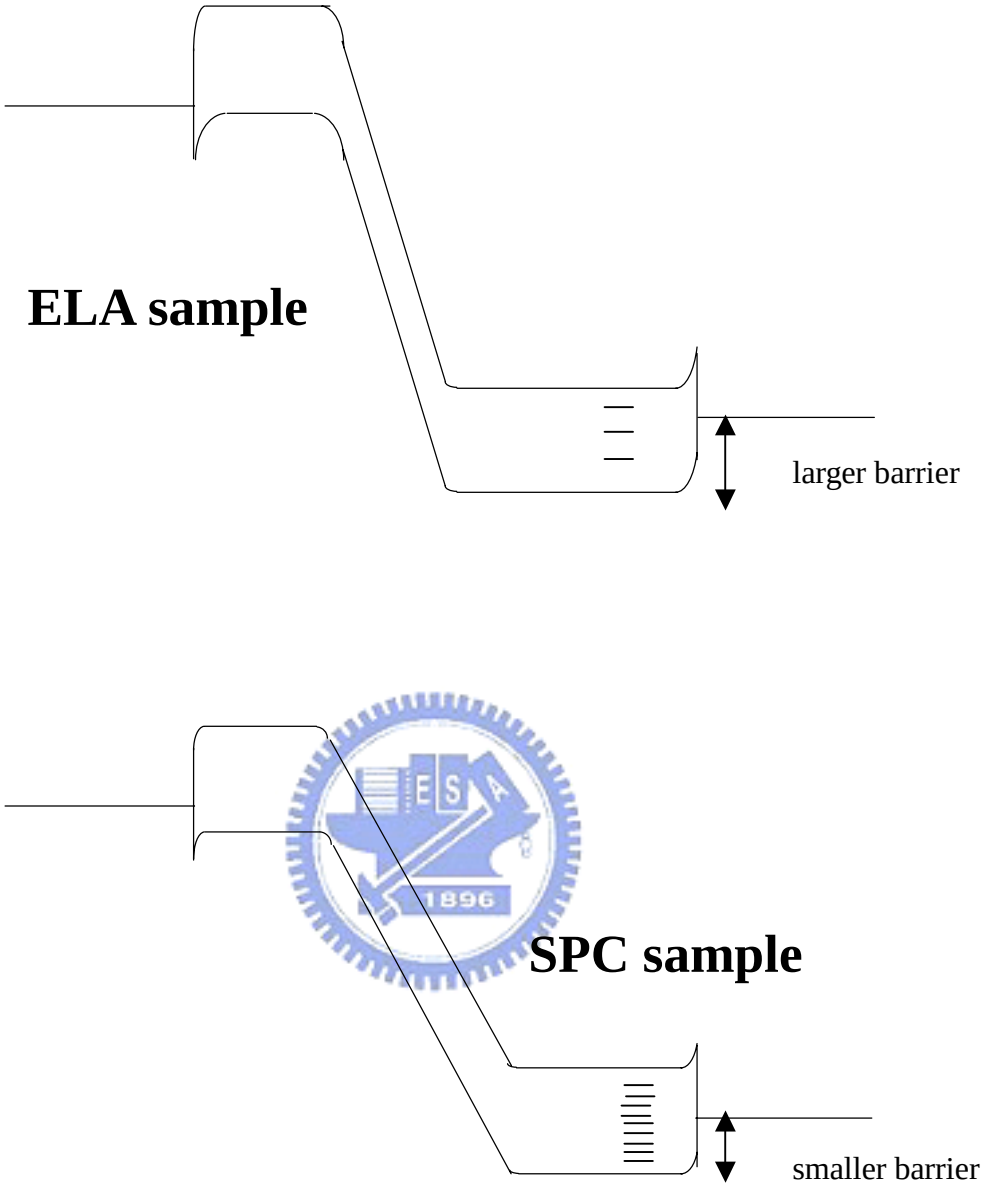


Fig.4-20 Energy band diagrams depicting lower E_A for SPC samples due to barrier pinning by defects in SPC channel.

Chapter 5

Schottky Barrier TFTs with Nano-Scale Channel Width

5.1 Introduction

As our study demonstrated in the last three chapters, we find that the novel SB-TFTs with field-induced-drain can successfully suppress off-state leakage current. Considering the advantages of FinFET [1-4] mentioned in Section 1.1.3, a combination of Schottky Barrier FinFET and FID-structure would be a promising device. This is because FinFET suffers from insufficient current driving capability caused by the nature of the fin structure with large series resitance which seriously impedes its application. Concomitantly, Schottky-barrier S/D junction formed by low resistivity silicide is attractive in reducing the unwanted source/drain series resistance with conventional MOSFET using heavily-doped S/D. The process flow is inherently low temperature in nature, because no post-implant annealing step is required [5-7]. This feature makes it compatible with future technologies employing high-k gate dielectric and metal gate. Moreover, the inherently abrupt and shallow silicide junction is also conducive to the suppression of short-channel effect, which is another acclaimed feature for its implementation in nano device applications.

Also from the perspective of AMLCD application, FinFET structure will also increase the aspect ratio. In addition, adopting the FinFET structure will improve SB TFT devices' performance. This is because the amount of defects in the channel is significantly reduced owing to the ultra-thin fin body. Besides, the double-gate scheme is very effective in enhancing the gate control over the channel potential, minimizing drain-induced barrier lowering and threshold voltage roll-off [8-12]. This is very helpful for peripheral driving circuit performance. With these motivations in mind, we carried out in this work the feasibility study of SBTFT devices with a fin-like channel. So, in this chapter, we fabricated and characterized poly-Si SBTFTs with nano-scale poly-Si channel width. As-deposited poly-Si films were used as the channel layer. Top and cross-sectional views of the device are show in

Fig. 5.1. It is worth noting that when the planar channel width becomes comparable to the channel thickness, the device is similar to the double-gated FinFET reported previously [1]. In fact, the new device actually has a triple-gated structure [13], i.e., both the top (planar) and the two sidewalls of the Si film underneath the main gate serve as the conduction channel, since no hard mask was employed on the Si channel (see Fig. 1(c)). As a result, the current drive can be increased due to a larger effective channel width. Furthermore, the subthreshold characteristics of the device are expected to improve since the controllability of gate bias over the channel potential is greatly enhanced.

5.2 Device Fabrication

Figure 2 shows key process flow and the device structure. E-beam lithography was employed for device patterning throughout the fabrication. The starting substrates were 6 in. Si wafers capped with thermal oxide (400nm). The active poly-Si layer was first deposited at 620℃ using SiH_4 low-pressure chemical vapor deposition (LPCVD). The thickness of poly-Si active layer was around 80 nm. Poly-Si channel with planar channel width down to 50 nm was defined using e-beam lithography and plasma etching. After the device island (including S/D contact regions and Si channels) was defined, a 10 nm-think sacrificial oxide was grown and wet-etched to remove the damage created by dry-etching processes on the sidewall surfaces of the Si fins. After cleaning, a 3nm-thick gate oxide was thermally grown in diluted oxygen ambient, followed by the deposition of a 150nm-thick, *in situ* phosphorus-doped polysilicon. The polysilicon gate was then etched in a high-density plasma etcher with an etching selectivity to the under oxide layer larger than 100. A 20nm-thick TEOS (tetra-ethyl-ortho-silicate) oxide layer was then deposited using LPCVD, and patterned to define the offset (i.e., source/drain extension) regions (Fig. 2(a)). After Ti (20nm)/Co (20nm) deposition by sputtering, Co self-aligned silicidation (salicide) process was subsequently performed in the S/D regions (Fig. 2(b)). Next, a 40nm-thick TEOS oxide layer was deposited using plasma-enhanced chemical vapor deposition (PECVD), followed by contact holes and aluminum pads/sub-gate formation (Fig. 2(c)). Finally, wafers received an annealing in forming gas at 400℃. Electrical

characterizations were performed after the device fabrication using an HP4156A semiconductor analyzer. Note that no plasma hydrogenation step was performed on the devices.

5.3 Results and Discussion

Figure 3 depicts typical ambipolar characteristics of the fabricated devices for both FinFET (Fig. 3(a)) and planar (Fig. 3(b)) structures. Though no plasma hydrogenation was performed, high on/off current ratios (~ 10^7) is achieved for both p- and n-channel operations in a single device. The high on/off current ratio is ascribed to the application of the sub-gate bias, which has been shown to be effective in not only increasing the on-state current [2], but also suppressing the off-state leakage current. The subthreshold swing (SS) is also sharper for FinFET structure than the planar structure, due to the better controllability of Tri-gate.

Figure 5.4 describes the effect of sub-gate bias (Vsub). The On-current increases as |Vsub| increases. Figure 5.5 shows the effect of drain side extension X_D. While the drain extension region is necessary for leakage current reduction, a longer X_D results in significant on-current reduction, due to the associated series resistance.

Figure 5.6 illustrates the short channel controllability, i.e., SS as a function of channel length, for FinFET and planar devices. We can see that FinFETs depict smaller SS. Moreover, and the SS degradation at shorter channel length is also reduced for FinFETs. The dependence of SS on fin width is depicted in Figure 5.7. For devices with channel length of 470nm, reducing fin width results in a smaller SS, again confirming the improved SCE control for nano-scale channel width. This could be explained using the schematic drawings shown in Fig. 5.8. When the channel width is smaller than two times the depletion width (Wdep) in the channel, the channel becomes fully depleted and thus the subthreshold swing could be lowered. Effective trap densities per unit area, Nt, in the poly-Si channel extracted from the subthreshould swing, $SS = \ln[10 \times (kT/q) \times (1 + Cd/Cs)]$, where $Cd = q \times Nt$, with channel width larger than 120 nm are found to be around 8.8×10^{12} cm^{-2} and 11.4×10^{12} cm^{-2} for n- and p- channel operations, respectively. From the results shown in Fig. 5.7,

Wdep is around 50 ~ 60 nm. The effective trap concentration, Dt = Nt / Wdep, in the channel is thus estimated to be 1.48 × 10^{18} cm^{-3} for electrons and 1.9 × 10^{18} cm^{-3} for holes. Significant lowering in subthreshold swing as channel width is smaller than 120 nm is due to the reduction of effective trap densities in the channel. This phenomenon is more significant for p-mode operation, which well explains why p-mode operation exhibits larger improvement in on-state current as channel width is scaled into the nanometer regime shown in Fig. 5.3.

Figure 5.9 shows the threshold voltage as a function of fin width (channel width). The channel length is fixed at 470nm, and V_{TH} is defined as the $|V_{G,main}|$ at which a |10| nA/um drain current flows at $|V_D|$=0.1Volt. Interestingly, $|V_{TH}|$ decreases as the fin width decreases, which is contrary to the SS trend. The explanation is that when the fin width is thin enough, a smaller amount of defects, which influence V_{TH}, exists in the active region, so it is easier to turn on the nano-scale poly-silicon film device. This, together with the tri-gate control, accounts for the observed sharp SS.

Figure 5.10 shows the sub-gate bias effect on threshold voltage roll-off characteristics. It can be seen that V_{TH} roll-off is more pronounced with higher $|V_{G,sub}|$. The aggravation in V_{TH} roll-off curves is believed to be due to the sub-gate induced barrier lowering. This is similar to the drain-induced barrier lowering (DIBL phenomenon), except that the penetration of electric field now originates from the sub-gate bias. A small amount of potential edges toward the channel and can modulate the channel length when a high $|V_{G,sub}|$ is applied [10]. To further illustrate the influence of FID, we compare the short channel effect for devices with different offset channel lengths, for example X_D = 0.1 um and self-aligned spacer, in Fig.5.11. Apparently, the short channel effect is more severe for the device with self-aligned spacer, due to the stronger drain-side electric field. Figure 5.12 shows the subthreshold slope as a function of fin width, for FinFET devices with either 0.1um offset length or self-aligned spacer. It can be found that the swing degrades more seriously for self-aligned device, because of drain-side electric field mentioned above.

5.4 Summary

In this work, a novel nano-scale SB poly-Si TFT device which features metallic silicide Schottky barrier source/drain and field-induced S/D extension was fabricated and characterized. The fabrication of the new device is simple, and does not require implantation and associated annealing steps. Low overall processing temperature makes the new device suitable for applications using large-area glass substrates. With the unique field-induced S/D extension scheme, extremely low off-state leakage current and high on/off current ratio ($>10^8$) could be achieved. Besides, excellent p- and n-channel device performances could be realized on a single device.

The fabricated devices exhibit higher current drive for n-channel operation mode, which is different from that observed on SOI FinFET, and can not be explained by the relatively lower barrier height for holes at the Schottky junction. Nevertheless, our results also indicate that, despite the high trap density in poly-Si films, high on/off current ratio and small subthreshold swing can be achieved. It appears therefore possible to achieve SOI-like device characteristics if poly-Si film improvement methods, such as excimer laser annealing and metal-induced crystallization scheme, are adopted.

References :

[1] D.Hisamoto, W.C. Lee, and J.Kedzier et al., “A Folded-channel MOSFET for Deep-sub-tenth Micron Era”, IEDM Tech. Dig., pp. 1032-1034, 1998.

[2] D. Hisamoto, W.C. Lee, J. Kedzierski, H. Takezuhci, K. Asano, c. Kuo, E. Anderson, T.J. King, J. Boker, and C. Hu, “FinFET-A self-aligned Double-Gate MOSFET Scalable to 20 nm,” IEEE Trans Electron Device, vol.47, p.2320, 2000.

[3] X. Huang, et al., “Sub-50 nm P-Channel FinFET,” IEEE Trans. Electron Device, vol.48, p.880, 2001.

[4] Y.K. Choi, T.J. King, and C. Hu, “A Spacer Patterning Techonology for Nanoscale CMOS,” IEEE Electron Device Lett., vol.49, p.436, 2002.

[5] J.Kedzierski, P. Xuan and E. H. Anderson et al., “Complementary silicon source/drain thin-body MOSFETs for the 20nm gate length regime”, IEDM Tech. Dig., pp.57-60, 2000.

[6] C.Wang, J.P.Snyder and J.R.Tucker, “Sub-40nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistor”, Applied Physics Letters, Vol.74,pp.1174-1176,Feb.1999.

[7] J. R. Tucker, “Schottky barrier MOSFETs for silicon nanoelectronics,” *WOFE’97 Proceedings.*, *Frontiers in electronics*, p.97, 1997.

[8] S.-I. Takagi, J.Koga and A. Toriumi. “Subband Structure Engineering for Performance Enhancement of Si MOSFETs”, IEDM Tech. Dig., pp. 219-222, 1997.

[9] H.-S.P.Wong, D.J.Frank, and P.M.Ssolmon, “Device Design Considerations for Double-Gate, Ground-Plane,and Single-Gate Ultra-Thin SOI MOSFET’s at the 25nm Channel Length Generation”, IEDM Tech. Dig., pp.407-410,1998.

[10] L.Chang, S.Tang and T.-J.King et al.,”Gate Length Scaling and Threshold Voltage Control of Double-Gate MOSFETs”, IEDM Tech. Dig., pp.719-722, 2000.

[11] B.Majkusiak, T.Janik and J.Walczak, “Semiconductor Thickness Effects in the Double-Gate SOI

MOSFET”, IEEE Trans. Electron Devices, Vol. 45, pp.1127-1134, May1998.

[12] L.Chang, K.J.Yang and Y.-C Yeo et al., “Reduction of Direct-Tunneling Gate Leakage Current in Double-Gate and Ultra-Thin Body MOSFETs”, IEDM Tech. Dig.,2001.

[13] R. Chau, SSDM Tech. Dig. (2001) p.68

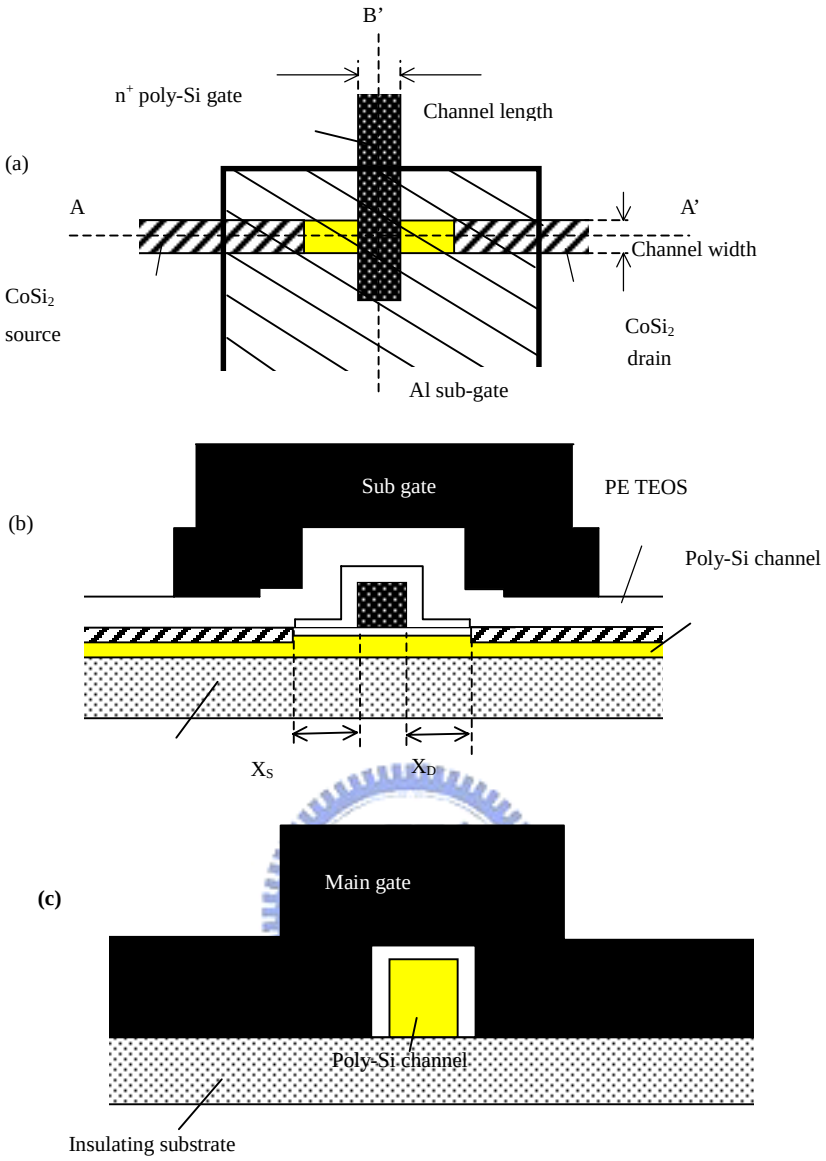


Fig. 5.1 (a) Top view of the SB poly-Si TFT, (b) Cross-sectional view of the SB poly-Si TFT along A - A' direction in (a), and (c) Cross-sectional view of the SB poly-Si TFT along B - B' direction in (a). Note that the sub-gate is not shown in (c).

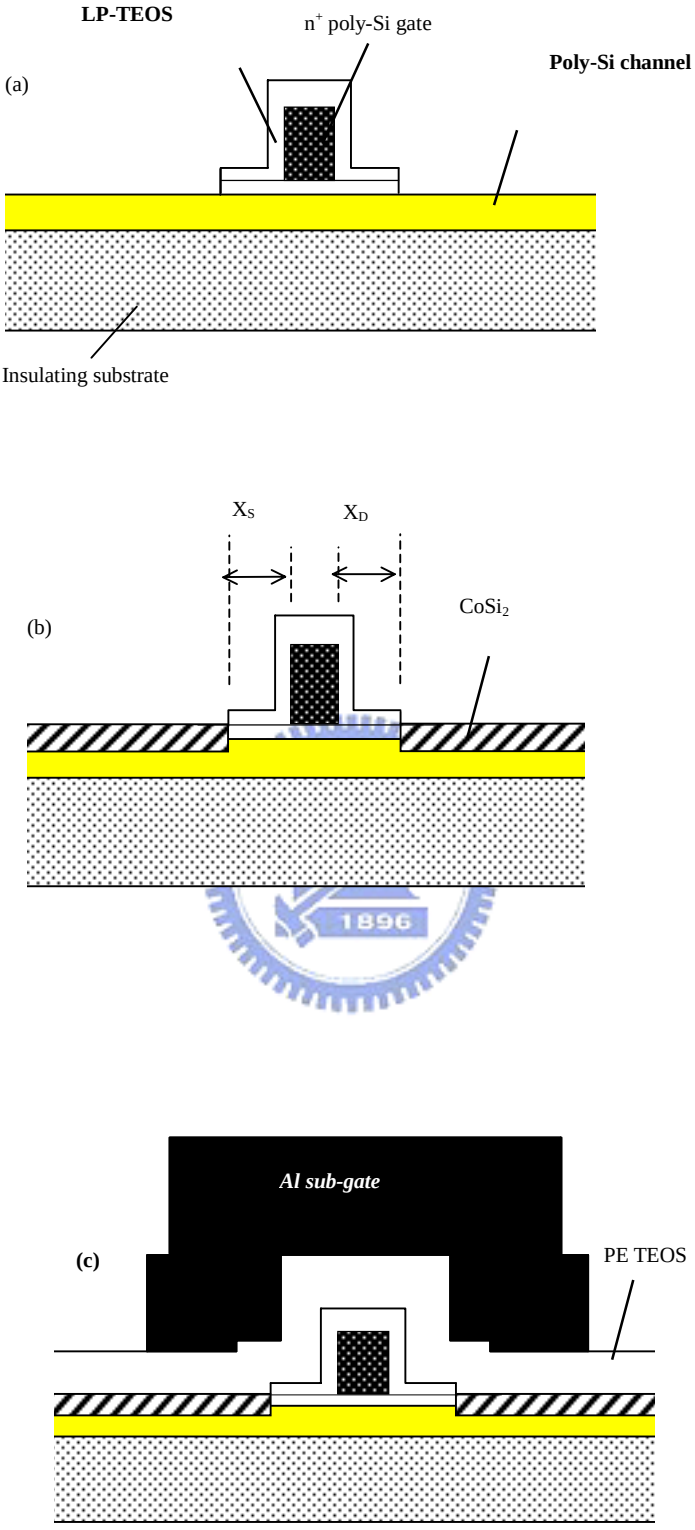
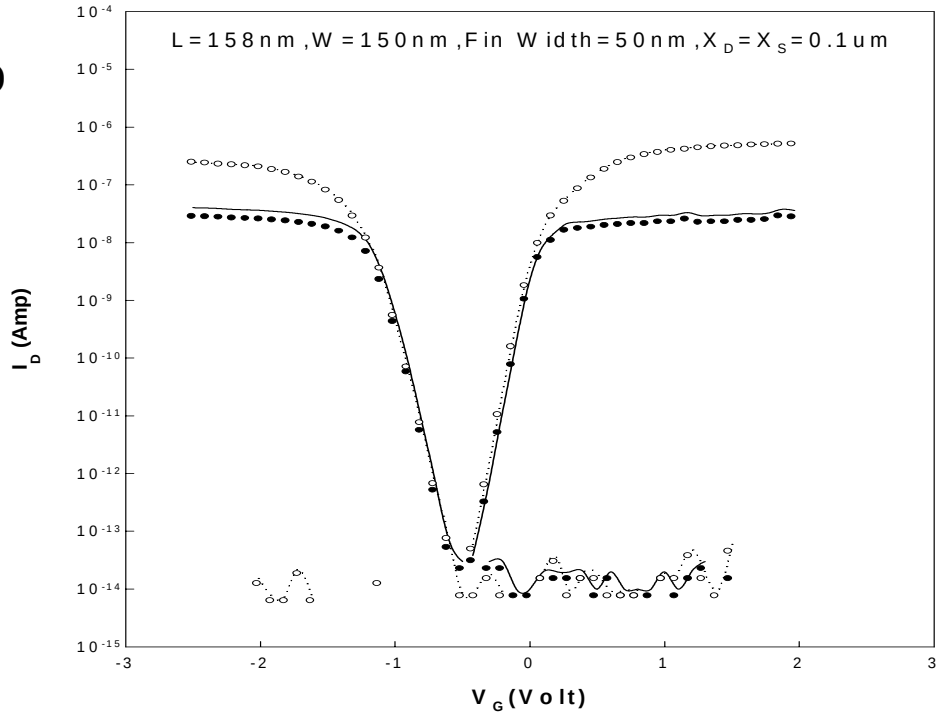
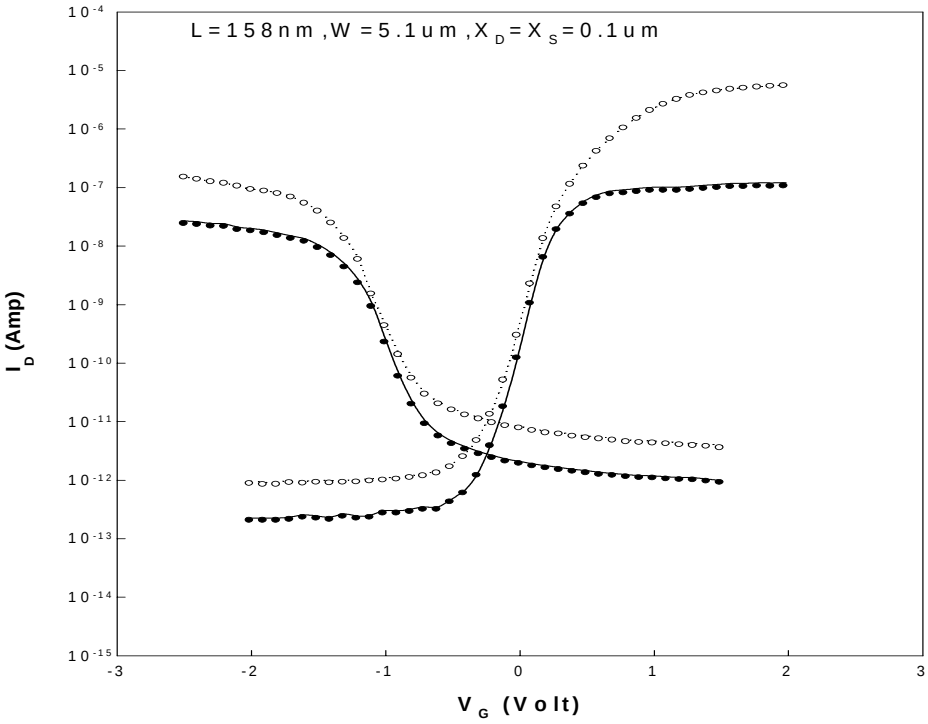


Fig. 5.2 **Key device fabrication flow.**

(a)


L=158nm,W=150nm,Fin Width=50nm,X_D=X_S=0.1um
I_D (Amp)
V_G (Volt)


L=158nm,W=5.1um,X_D=X_S=0.1um
I_D (Amp)
V_G (Volt)

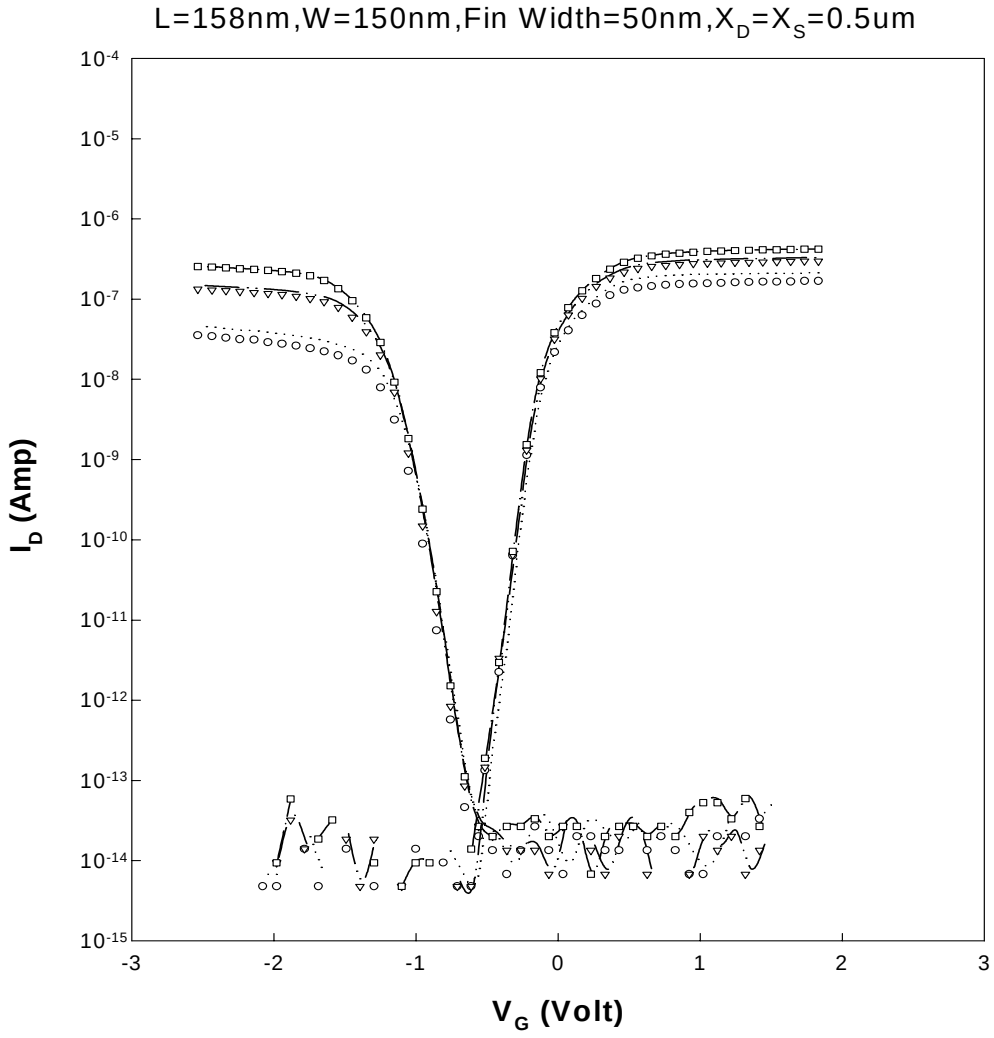


Fig. 5.4 The effect of sub-gate bias. $|V_D| = 1$ Volt.

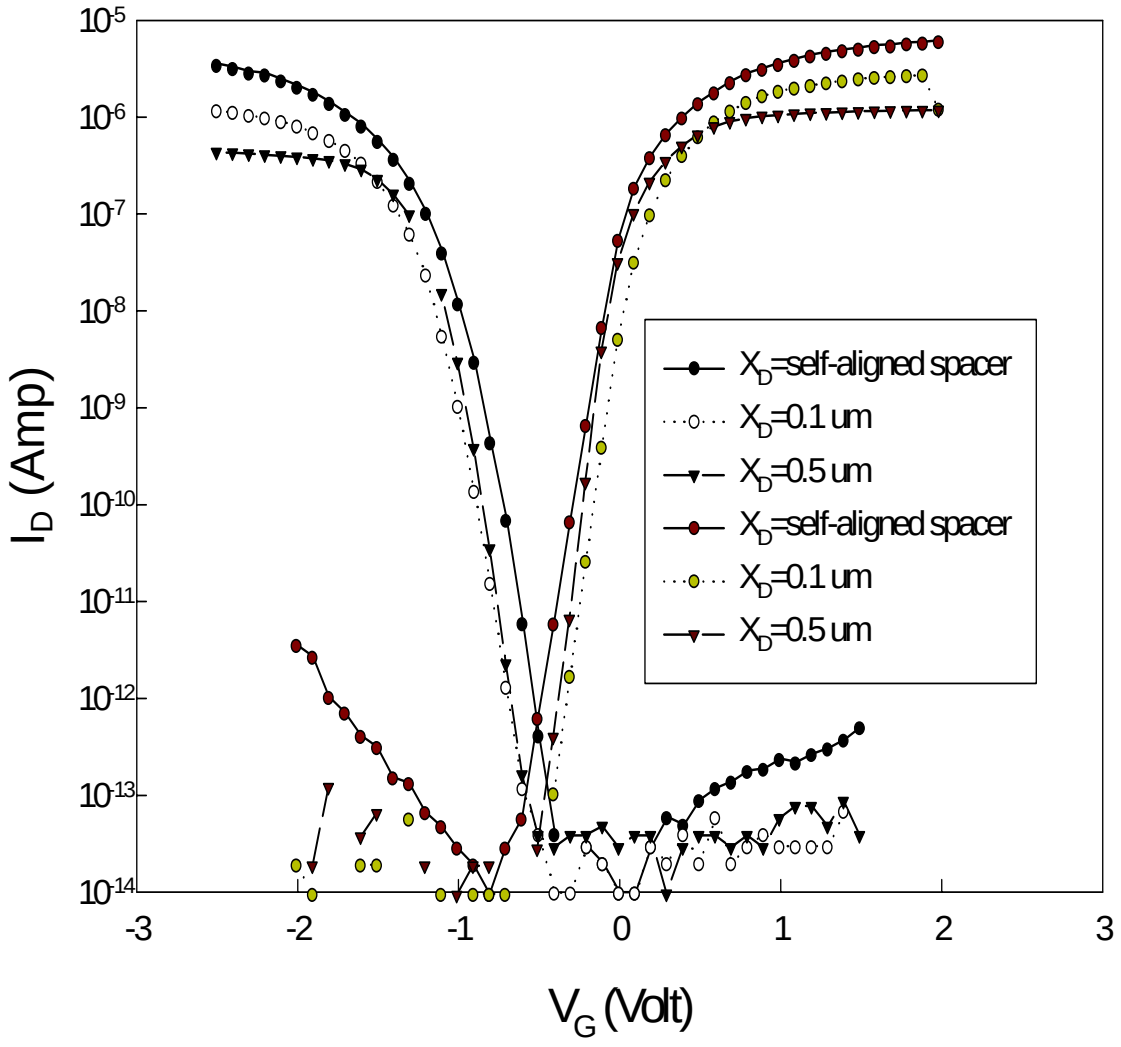


Fig. 5.5 The effect of FID length.

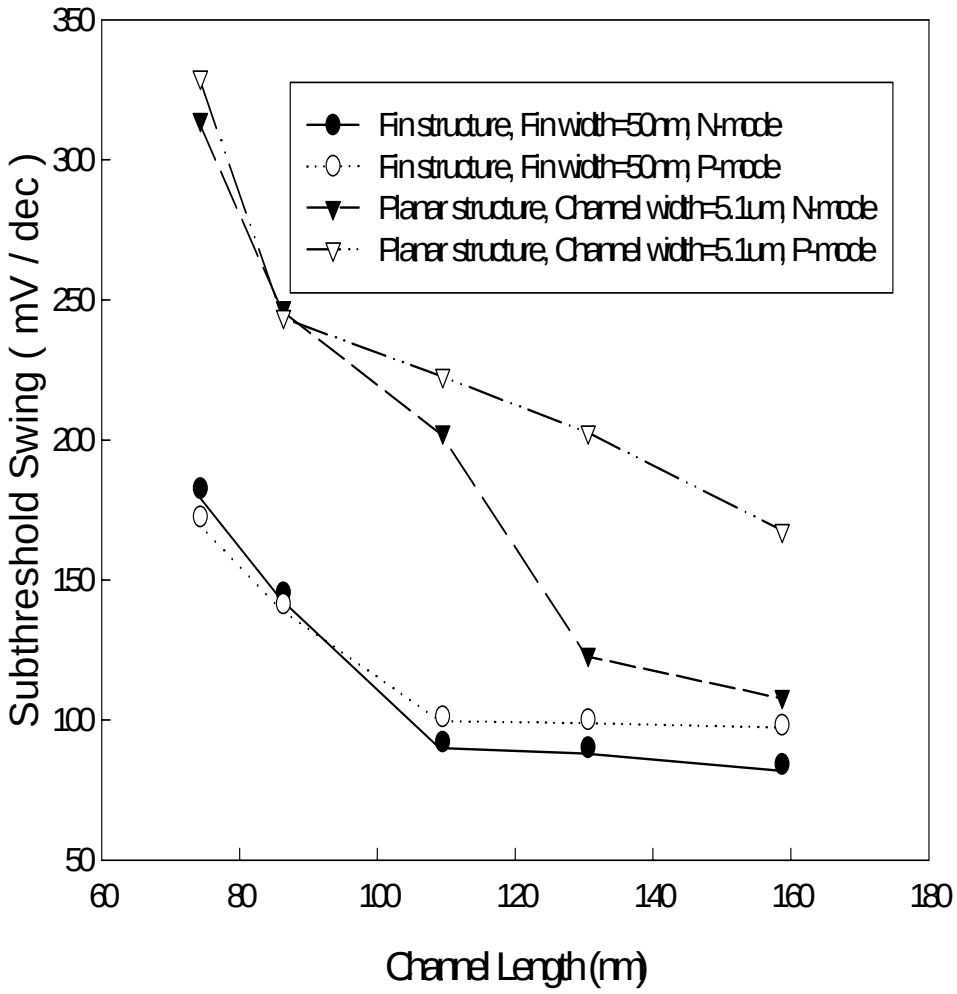


Fig. 5.6 Suthreshold swing degradation for both structures.

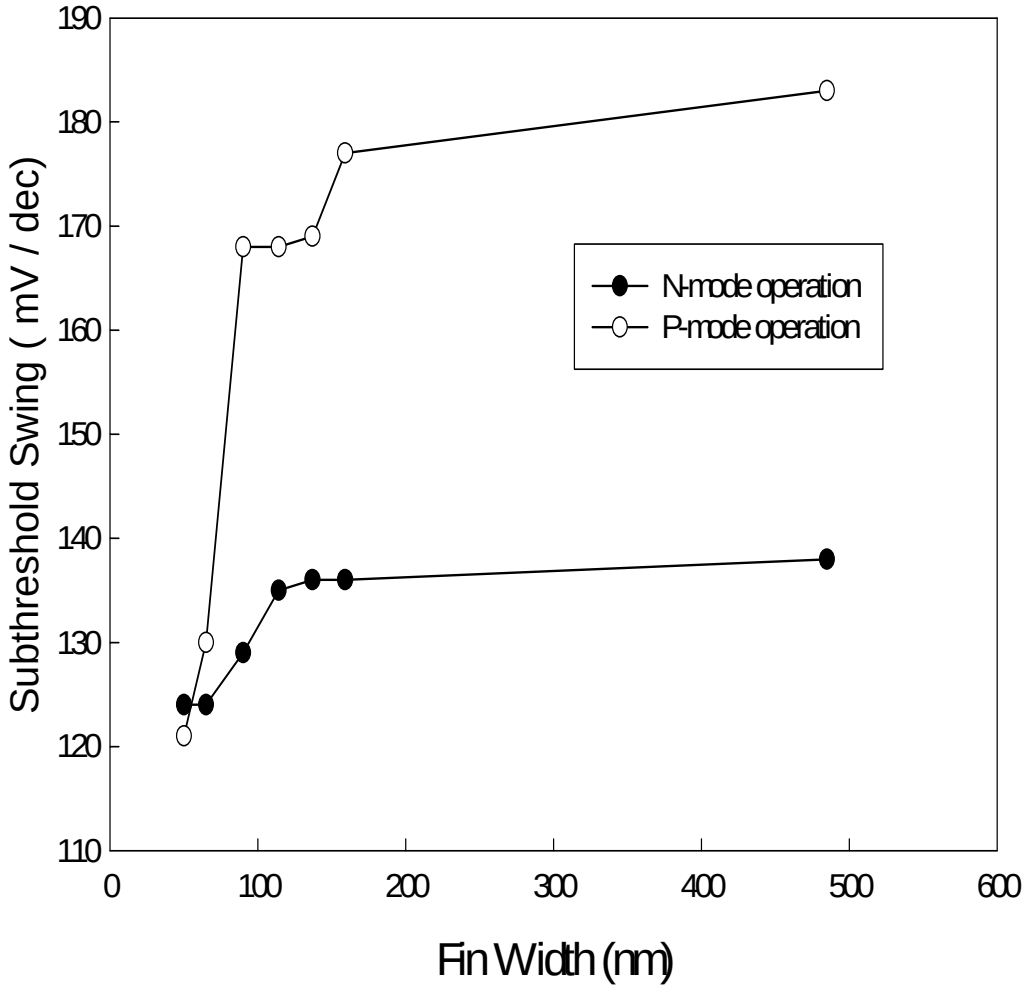


Fig.5.7 The effect of fin width on suthreshold swing. Channel length = 158 nm.

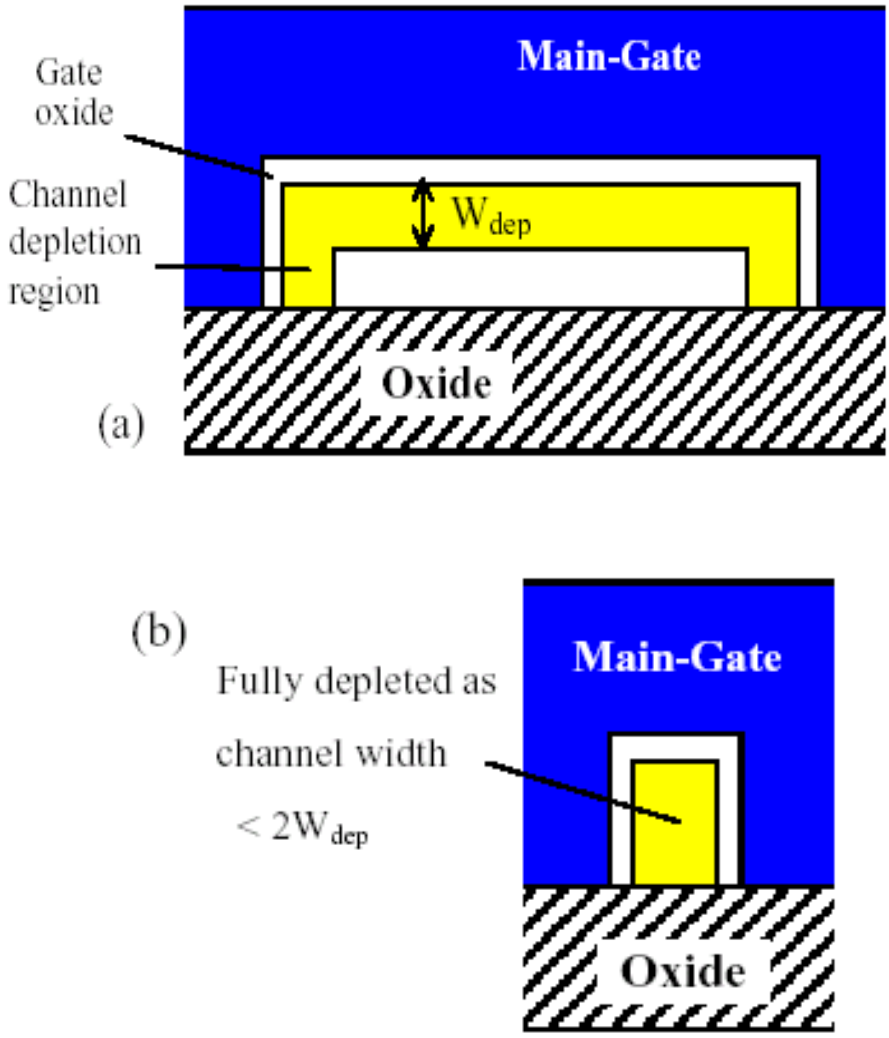


Fig. 5.8 **Illustration of channel depletion layer in devices with (a) wide, and (b) narrow channels.**

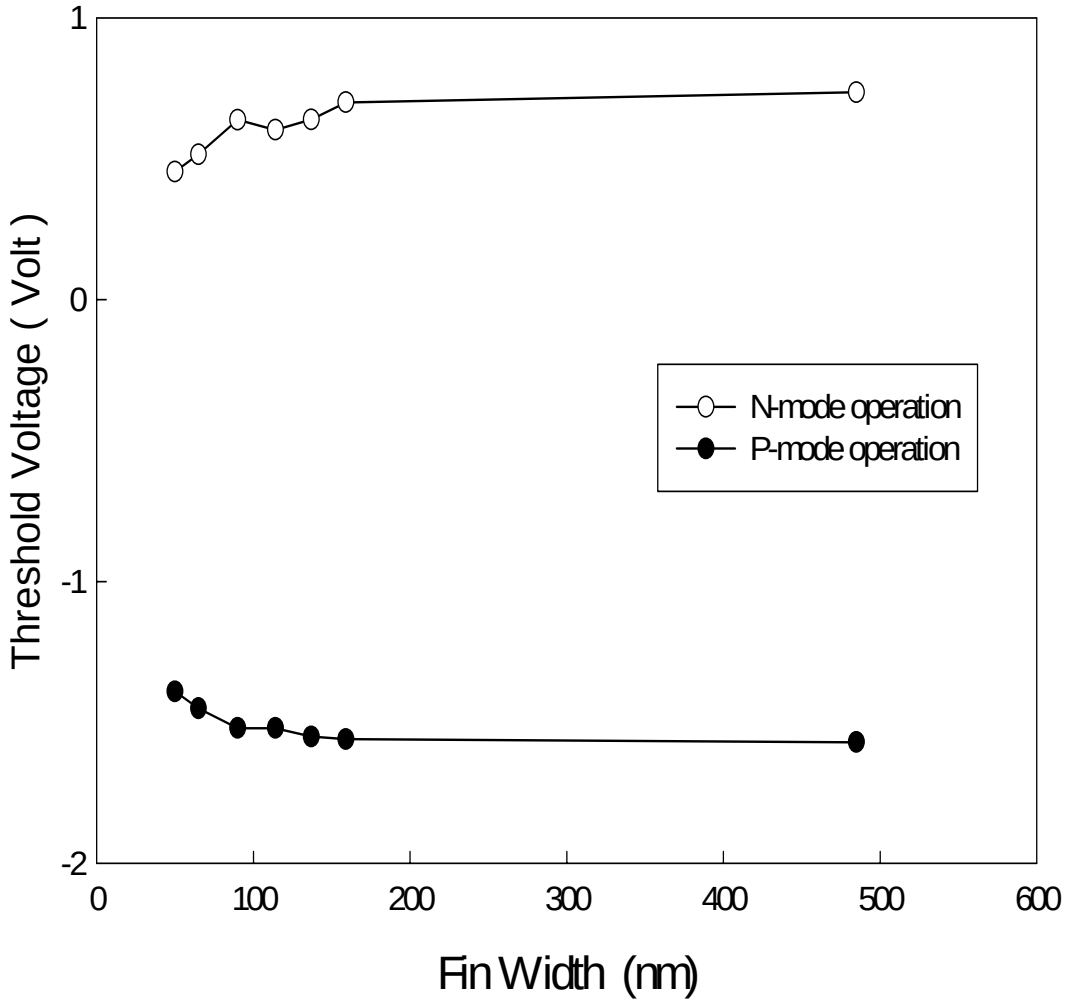


Fig. 5.9 **The effect of fin width on threshold voltage. Channel length = 158 nm.**

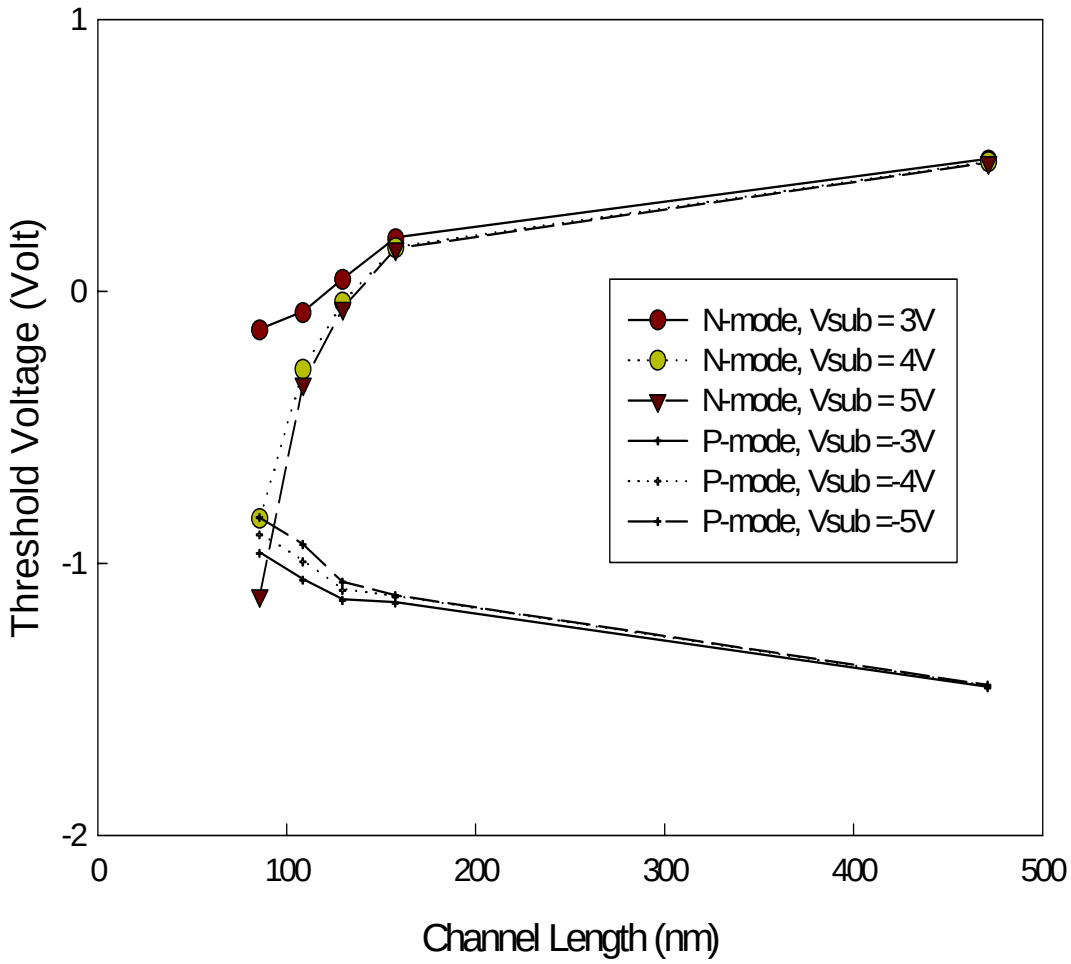


Fig. 5.10 **The effect of sub-gate bias on threshold voltage roll-off. Fin width = 50 nm.**

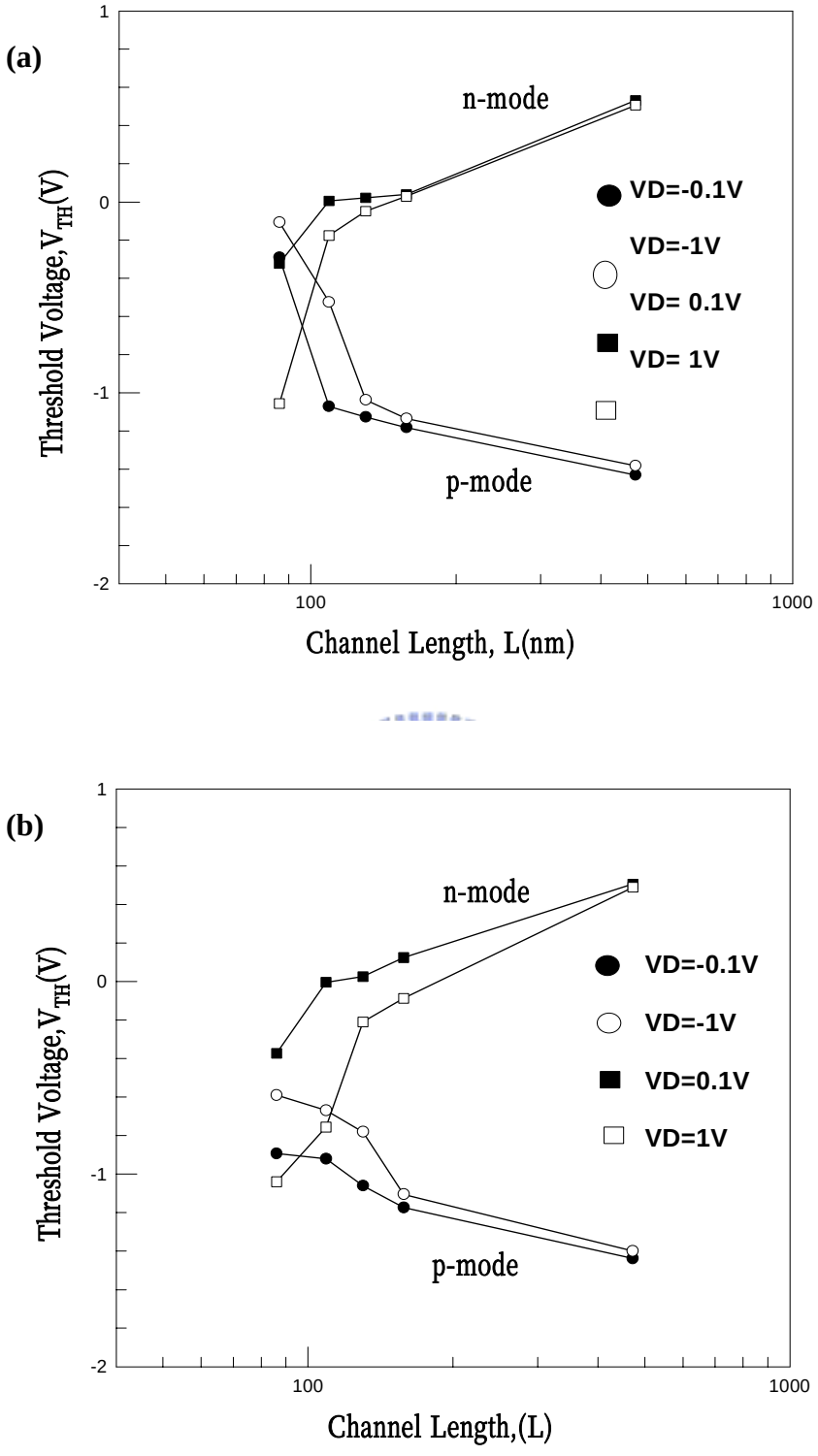


Fig. 5.11 Threshold voltage of FinFET device as a function of channel length for (a) with 0.1um offset length, and (b) with self-aligned spacer. Fin width is 50nm, and fin number=1. | VG,sub | =5V.

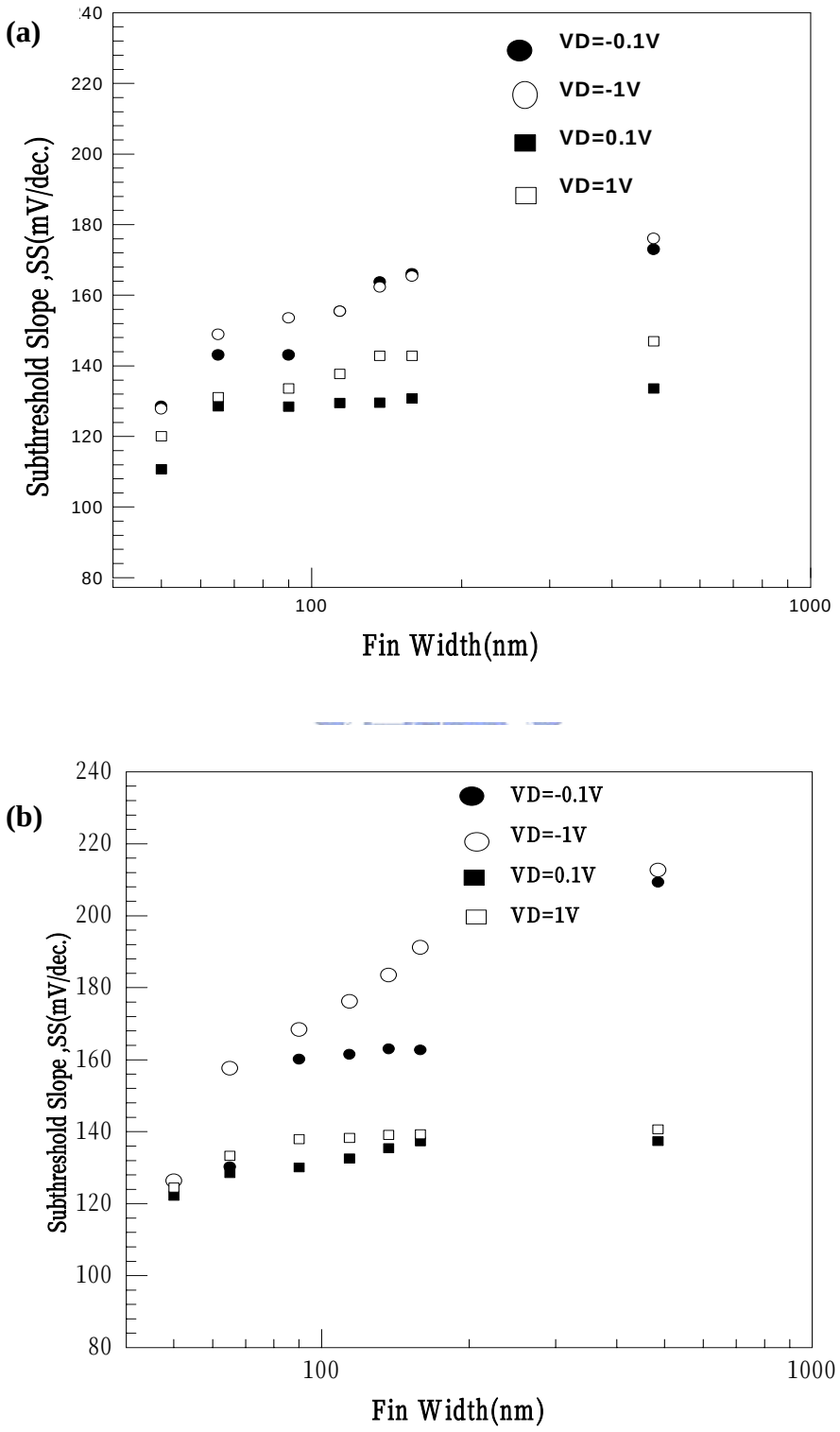


Fig. 5.12 Subthreshold slope as a function of fin width for FinFET device (a) with 0.1um offset length, and (b) with self-aligned spacer ｜VG,sub｜=5V.

Chapter 6

A Novel Method to Analyze Full Band-Gap Density of States Distribution in Thin Film Transistors

6.1 Introduction

The electrical properties of polycrystalline semiconductor devices are strongly affected by defects such as dangling bonds and strained bonds located at the grain boundaries [1-3] as mentioned in the previous chapters. An understanding of the nature, energy distribution, density, and behavior of these defects is important for the development of polycrystalline TFTs. Several approaches have been developed to determine the density of gap states (DOS) in polycrystalline devices, such as capacitance-voltage method [4], the doping dependence of conductivity [5], and the field effect conductance (FEC) method [6-7]. Among them, only the field effect conductance method is compatible with modern poly-Si TFT samples. A theoretical interpretation of the field effect conductance method was given by Suziki et al. [8] to calculate the DOS of amorphous Si TFTs [9]. The technique has been extensively applied to a-Si:H devices and provides adequate information on the DOS in spite of some interpretation difficulties, such as the differentiation between bulk and interface states. In the case of poly-Si TFTs, the method has also been proven to be sensitive enough to account for the effect of film morphology and differences in device processing [10]-[11], thereby providing an essential tool for the analysis of poly-Si thin film transistors.

However, there are also several issues associated with the field-effect conductance method. In particular, the distributions of gap states in upper (Ei ~ Ec) and lower (Ei ~ Ev) half of band-gap are obtained using n- and p- channel devices, respectively. This limitation necessitates the use of at least two separate devices with different channel types to obtain full band-gap density of state analysis. Moreover, measurements need to be performed at various temperatures in order to determine the flat-band voltage (for details, please refer to the method description session later in this chapter).

In this work, we propose a novel method to determine the full band-gap density of states of poly-Si channel using only a single device. The new method is successfully demonstrated on the novel Schottky barrier (SB) TFT device with field-induced drain (FID) described in previous chapters [12]-[16]. The SB-TFT device exhibits an ambipolar operation capability, i.e., both n- and p- channel operation modes could be achieved in a single device. By exploiting this unique characteristic, we can perform the field effect conductance method to acquire the full-band gap state density distribution using only a single device. Experimentally, we also found that the flat-band voltage could be acquired by simply characterizing the ambipolar current-voltage (I-V) characteristics, without resorting to various temperature measurements. The extracted value is very close to that obtained by the temperature method, while the measurement scheme is greatly simplified.

6.2 Realization of Full Band-Gap DOS Analysis Using a Single Device

6.2.1 Field Effect Conductance Method

As mentioned in the last chapter, the performance of poly-Si TFTs is strongly affected by defects in the poly-Si channel. Characterization and analysis of DOS is thus essential for understanding the device characteristics and their dependence on the processing conditions. Moreover, accurate DOS is required for the modeling of poly-Si TFT characteristics. It has been shown that field effect conductance (FEC) method can serve this purpose. In this chapter, we will first briefly review its theoretical background.

FEC method was original proposed for characterizing the DOS in a-Si TFTs. When applied to poly-Si TFTs, the presence of grain boundaries in the channel could be of great concern. Fortunately, it has been proven that, when the grain size is small enough (compared to the channel length), the poly-Si channel film can be modeled using the “effective-medium” approach [6], in which the existence of grain boundary defects and intragranular defects are assumed to be uniformly distributed throughout the material. Under this assumption, the band bending is a solution of the one-dimensional Poisson’s equation.

$$\frac{d^2\psi}{dx^2}|_{x=0} = -\frac{\rho(\chi)}{\varepsilon_{Si}} \tag{6-1}$$

The meanings of the symbols could be found in the List of Symbols (page [xxi]).

ρ (x), charge density per unit volume, can be expressed by

$$\rho(\psi) = -q\int_{Ev}^{Ec} Ng(E)f(E-E_F-q\psi)dE + q\int_{Ev}^{Ec} Ng(E)f(E-E_F)dE \tag{6-2}$$

The first term denotes acceptor-like states, which are neutral when empty and negatively charged when filled with electrons. The second term denotes donor-like states, which are positively charged when empty and neutral when filled with electrons. For sufficiently low temperatures, all states below the Fermi level are filled and all states above the Fermi level are empty. Eqn. (6-2) can be written (zero-temperature approximation)：

$$\rho(\psi) = -q\int_{E_F}^{E_F+q\psi} Ng(E)dE \tag{6-3}$$

where *Ng(E)* is the gap-state density (per unit volume). Multiplying by $2\cdot\partial\psi/\partial x$ and integrating from x=0 (oxide-semiconductor interface) to x=Xo (un-modulated bulk, see Fig. 6.1)：

$$\left(\frac{d\psi}{dx}|_{x=0}\right)^2 = \frac{2q}{\varepsilon_{Si}}\int_0^{\psi_s} d\phi \int_{E_F}^{E_F+q\psi} Ng(E)dE \tag{6-4}$$

where ψ_s is the band bending at x=0 (surface potential), and $\left(\frac{d\psi}{dx}|_{x=0}\right)$ is the electric field at the surface. The gap-state density is then given by

$$Ng(E_F+\psi_s) = \frac{\varepsilon_{Si}}{2q}\frac{\partial^2}{\partial\psi_s^2}\left(\frac{d\psi}{dx}|_{x=0}\right)^2 \tag{6-5}$$

The electric field at the semiconductor surface is given, in the absence of surface states,

$$\frac{d\psi}{dx}|_{x=0} = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\frac{V_{ox}}{t_{ox}} = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\frac{V_G - V_{FB} - \psi_S}{t_{ox}} \tag{6-6}$$

From Eqns. (6-5) and (6-6), the gap-state density can be determined if the relationship between V_G and ψ_s and bulk Fermi energy is known. The relationship between V_G and ψ_s can be determined

by the following two methods.

The incremental method

By assuming that the transport is by electrons, the field conductance is defined as [8]

$$G = G_0 - \frac{G_0}{d}\int_0^{\psi_s} \frac{\exp(q\psi / KT) - 1}{d\psi / dx} d\psi \tag{6-7}$$

where d is the poly-Si film thickness and G_o is the conductance for the flat band condition. The conductance is defined as the derivative of drain current with respect to the gate voltage at a fixed drain voltage. Differentiating Eqn. (6-7) with respect to the surface potential gives

$$\frac{dG}{d\psi_s} = -\frac{G_0}{d} \cdot \frac{\exp(q\psi / KT) - 1}{d\psi / dx\,|_{x=0}} \tag{6-8}$$

By substituting Eqn. (6-6) into Eqn. (6-8), the following approximation expression is obtained:

$$\frac{d\psi_s}{dG} = \frac{1}{G_0} \cdot \frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{d}{t_{0x}} \cdot \frac{V_G - V_{FB} - \psi_s}{\exp(q\psi_s / KT) - 1} \tag{6-9}$$

Actually, Eqn. (6-9) can be expressed by the differential form:

$$\psi_{s,i+1} = \psi_{s,i} + \frac{G_{i+1} - G_i}{G_0} \cdot \frac{d}{t_{0x}} \cdot \frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{V_{G,i} - V_{FB} - \psi_{S,i}}{\exp(q\psi_{S,i} / KT) - 1} \tag{6-10}$$

which can be used to construct the ψ_s against V_G relationship.

The temperature method

This method is based on the temperature dependence of dG/dV_G. From Eqns. (6-8) and (2-6), and $dG/dV_G=(dG/d\psi_S)(d\psi_S/dV_G)$, one can obtain the following expression:

$$dG/dV_G = G_0 \frac{\varepsilon_{0x}}{d_{Si} \cdot t_{0x}} \cdot \frac{\exp[(E_F - E_C + q\psi) / KT]}{\rho(\psi_s)} \equiv k \cdot e^{(-\Delta E / KT)} \tag{6-11}$$

Both E_F and ψ_s in the above equation are expected to be temperature dependent. This dependence is due to the variation of Eg with T and to the so-called statistical shift. The latter is due to the fact that the total density of electrons (trapped plus free electrons) is a constant, so Eg must shift with T in order to compensate for the temperature dependence of the Fermi function. Since all terms

on the right-hand side, with the exception of exp($q\psi_s$/kT), have a weak temperature dependence, ψ_s can be determined from log(dG/dV_G) versus 1/T plot. The temperature analysis also allows the determination of an important parameter, namely, the flat band voltage. Following the method proposed by Weisfield and Anderson [17], the following expression is obtained for small ψ_s.

$$\frac{d\log G}{dV_G} \cong \frac{\varepsilon_{0x}}{t_{0x}} \cdot \frac{1}{qkTN_0}\left[1+\frac{1}{2}\left(\frac{q\psi_s}{KT}\right)+O\left(\frac{q\psi_s}{KT}\right)^2 ...\right] \qquad (6\text{-}12)$$

where N_o is the DOS at the Fermi level under flat band condition. V_{FB} is then determined as the gate voltage where T($dlogG/dV_G$) is temperature independent. Fig. 6.2 summarizes the flow chart using conventional FEC scheme to determine the DOS. It should be noted here that both p- and n-channel devices are needed for full band-gap DOS characterization.

6.2.2 Operation of Ambipolar TFT

In this study we propose a new approach that utilizes only a single FID SB-TFT to achieve the full band-gap DOS characterization. The device operation and fabrication are described in previous chapters. In this work, most samples use $CoSi_2$ as the source and drain material to exploit its near-mid-gap work function. With near-mid-gap work function, the barrier height between electrons and holes is comparable (Note: barrier height for electron is slightly higher than for hole in this case), resulting in near symmetrical I-V characteristics. Issues regarding the barrier height of silicde on the DOS measurement will be addressed in next section.

During device operation, a proper fixed voltage is applied to the field-plate to form an electrical drain extension under the field-plate region. The device can be set for n- and p-channel operations with positive and negative biases, respectively. With appropriate bias and polarity applied on other electrodes (i.e., main gate, source, and drain), excellent ambipolar transfer characteristics could be achieved. The unique ambipolar characteristics are exploited in our approach to extract full band gap DOS using only a single device.

6.3 Analysis of Full Band-Gap DOS in FID-SB TFT Structure

6.3.1 Determination of DOS Using Temperature and Incremental Methods

Figure 6.2 shows the flow chart for the determination of DOS used in field effect conduction method. First of all, we have to obtain the flat-band voltage of the device. The flat band voltage can be determined by the temperature (i.e., activation energy) method with Equation (6-12)

$$\frac{d\log G}{dV_G} \cong \frac{\varepsilon_{0x}}{t_{0x}} \cdot \frac{1}{qkTN_0}\left[1+\frac{1}{2}\left(\frac{q\psi_s}{KT}\right)+O\left(\frac{q\psi_s}{KT}\right)^2 ...\right] \tag{6-12}$$

From the above equation, the flat-band voltage can be determined by the V_G when the product T x ($d$logG/dV_G) is temperature independent (because surface potential is zero). Figures 6.3 (a) and (b) show the characteristics of T x ($d$logG/dV_G) against 1000/T performed on a FID SBTFT under n- and p-channel operation modes, respectively. From the two figures, the flat-band voltage is determined to be around -2.1V that is almost independent of the temperature in either p- or n-channel operation.

Once the flat-band voltage is obtained, the relationship between the gate voltage V_G and surface potential Φ_s could be established by either incremental method or the temperature method mentioned in Section 6.2. Next, we first use the incremental method to obtain this relationship, as shown below:

$$\psi_{s,i+1} = \psi_{s,i} + \frac{G_{i+1}-G_i}{G_0} \cdot \frac{d}{t_{0x}} \cdot \frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{V_{G,i}-V_{FB}-\psi_{S,i}}{\exp(q\psi_{S,i}/KT)-1} \tag{6-10}$$

Here we use the Visual Basic Language to obtain the solution of this equation. After the flat-band voltage and the relationship between gate voltage and the surface potential are determined, Matlab language is adopted to obtain the gap-state density. Fig. 6.4 shows an example of the DOS versus energy level in the gap. In this case the channel is made up of solid phase crystallization (SPC) poly-Si film. The channel width is 20um, and the channel length is 2um. The upper- and lower-half gap density is obtained by biasing the device into n- and p-channel operation modes, respectively.

Next, we show how the temperature method is performed to obtain the relationship between the gate voltage and surface potential. This method is based on the temperature dependence of

conductance at different gate voltages. Figure 6.5 shows the characteristics of drain current versus gate voltage measured at different temperatures. It can be seen that the on-current becomes larger as the temperature gets higher, simply due to a higher thermionic emission. Figure 6.6 shows the Arrhenius plot of dG/dV_G against 1000/T at different applied gate voltages. The slope of each straight line defines the activation energy, Ea. Figure 6.7 shows the characteristics of activation energy against gate voltage. As the gate voltage is increased, activation energy falls due to increasing carrier density (and thus lower barrier height). From the equation $Ea= E_{cb}-E_{F0}-q\psi_s$ stated in Section 6.2 and the results obtained in Fig. 6.7, we can obtain the relationship between the gate voltage and surface potential. As a result, the gap-state density distribution could be obtained. Figure 6.8 shows and compares the DOS versus energy level in the gap obtained by the temperature method and incremental method. The results are in reasonable agreement with each other. Nevertheless, in most cases it is observed that the data obtained from the temperature method show more fluctuation in the mid-gap region. This is ascribed to the dramatically lowering in measured current as temperature is reduced. In some instances the current is close to or even below the limit of the measurement system. Thus, it is preferable to use the incremental method, rather than the temperature method, to determine the relationship between the surface potential and gate voltage.

6.3.2 Effects of Applied Drain Bias

Here we address the effect of drain bias on the measurement results. The measurements were carried out for n-channel operation by sweeping gate voltages from –3 to +6V, and for p-channel operation by sweeping gate voltages from –1 to –10 V, with drain voltages $|V_{DS}|$= 0.1V or 5V, and sub-gate voltage |Vsub|=50V. Figure 6.9 shows I_D-V_G characteristics for the FID SB-TFT with $CoSi_2$ S/D material. The channel film is SPC poly-Si film. As can be seen in the figure, the on-current in n-channel operation is more sensitive to V_{DS} than p-channel operation, owing to the higher barrier height of electrons than holes at the $CoSi_2$/Si contact. The extracted DOS results are shown in Fig. 6.10. It is observed that the DOS remains unaffected in the mid-gap regime, but increases significantly near the band edge when $|V_{DS}|$ is set at 0.1V, especially for the conduction band edge. It was shown in

previous chapters that the increase in $|V_{DS}|$ could decrease the source-side carrier tunneling distance [12]-[14], and thus the parasitic resistance. As the Fermi level moves toward the band edge, the operation is near threshold and becomes more sensitive to the contact resistance. As a result, the DOS is overestimated when $|V_{DS}|$ is not sufficiently high.

6.3.3 Effects of Channel Length

Figures 6.11~6.14 show the ambipolar transfer characteristics and corresponding extracted DOS for four devices with self-aligned spacer and channel length ranging from 0.8 to 5 μm. The on-current measured at $|V_{DS}|$ = 0.1 V as a function of channel length for these devices is shown in Fig. 6.15. The on-current becomes larger as the channel length becomes shorter due to reduced channel resistance. However, the n-mode current is almost independent of channel length when channel length is lager than 1 μm, indicating the significance of contact resistance due to larger electron barrier height. In these measurements, the mid-gap DOS is almost the same (about $1.2x10^{18}$ $eV^{-1}cm^{-3}$), while the tail DOS is strongly dependent of the applied bias conditions. Figures 6.16 (a) & (b) compare the DOS results among devices with different channel lengths and $|V_{DS}|$ of 5 V. It can be seen that reasonable agreement is achieved among these devices, indicating that $|V_{DS}|$ of 5 V is sufficiently large so the effects of parasitic resistance is insignificant.

6.3.4 Effects of Drain-side Extension Length

Figure 6.17 (a) shows ambipolar transfer characteristics of devices with either self-aligned or non-self-aligned (X_D = 3 μm) FID length under $|V_{DS}|$ of 0.1V. The extracted DOS results are shown in Fig.6.17 (b). It can be seen that the on-state current is significantly lower for the device with X_D of 3 μm. This is apparently due to the larger parasitic resistance in the FID region and thus leads to an overestimation of tail DOS, as shown in Fig.6.17 (b). Such disparity can, again, be removed by increasing $|V_{DS}|$ to 5 V, as shown in Fig. 6.18.

6.3.5 Effects of Measurement Temperature

Figure 6.19 shows the ambipolar transfer characteristics of a device characterized at 25°C and 55°C. The on-state current is larger at 55°C than 25°C, owing to the enhanced conduction of

thermionic emission at higher temperature. The extracted DOS results are shown in Fig. 6.20. We can see that the results are in reasonable agreement with each other, indicating that the zero-temperature approximation mentioned in Section 6.2 holds in the characterized temperature range.

6.3.6 Results Comparison with Conventional Approach

Figure 6.21 shows and compares the DOS results extracted by performing the characterization process on a FID SB-TFT and two conventional TFTs (i.e., p- and n-channel TFTs with degenerately doped S/D) with same channel material, which is as-deposited poly-Si films. It can be seen that the results are similar which validates the DOS data deduced from the FID SB-TFT structure, even though only a single device is used in our proposed methodology.

6.3.7 Effects of Channel Crystallization Treatment

The electrical performance of poly-Si TFTs strongly depends on the quality of the polysilicon film. Methods such as direct deposition of polysilicon film by low-pressure chemical vapor deposition (as-deposited poly-Si), low-temperature solid phase crystallization (SPC) of amorphous silicon, and excimer laser annealing (ELA) crystallization methods, have been carried out in this work to examine their crystallinity and its consequence on the DOS characteristics. Fig. 6.22 shows the DOS extracted from samples with SPC and as-deposited poly-Si channels. Both samples received 1-hour NH_3 plasma treatment. It is seen that the SPC channel shows less DOS than the as-deposited poly-Si counterparts. This is primary due to the larger grain size of SPC sample than that of as-deposited poly-Si, as characterized by the transmission electron microscopy (TEM) results shown in Fig. 6.23. Both electrical and physical characterizations confirm that the SPC film indeed has larger grain size and better quality than the as-deposited poly-Si film.

Figure 6.24 shows the DOS comparison between the ELA and SPC samples The results indicate that the ELA treatment could further reduce the DOS. Figures 6.25(a) and (b) show the TEM micrographs of the SPC and ELA samples, respectively. We can clearly see that the grain size of ELA film is much larger than that of SPC film, and resulting in the reduced DOS shown in Fig. 6.25.

6.3.8 Effects of Plasma Hydrogenation

It was shown previously that deep trap states located near the mid gap mainly arise from dangling bond defects (predominantly located in grain boundary regions) whereas tail states may arise from distorted bond defects (predominantly existed inside the grains) [18]. These traps could be effectively reduced after performing hydrogenation treatment on the fabricated devices. Moreover, the relative passivation efficiencies on different types of defects can be determined and compared by comparing the DOS before and after hydrogenation. Fig. 6.26 shows and compares the ambipolar transfer characteristics of the SPC samples before and after 1 hour NH_3 plasma treatment. After plasma treatment, the on-current and the subthreshold swing are improved. The corresponding DOS results are shown in Fig. 6.27. As can be seen in the figure, a hump appears near mid-gap before hydrogenation, presumably caused by the dangling bonds situated in grain boundaries. Hydrogenation reduces the mid-gap state density by one order of magnitude (from 10^{19} to 10^{18} $eV^{-1}cm^{-3}$). This results in improved subthreshold swing and on-current. It can also be seen that, although the mid-gap state density is reduced dramatically after plasma hydrogenation, the tail state density near both valence and conduction band edges are only affected slightly. This indicates that the plasma treatment passivates the dangling bond more effectively. It may need more time to reduce the tail state density, as pointed out in Ref. 18.

Figure 6.28 shows and compares the DOS of devices with as-deposited poly-Si channel before and after plasma hydrogenation. Similarly, the DOS is reduced, though the improvement on tail states seems to be more significant, as comparing to the SPC case shown in Fig. 6.27. This phenomenon is not fully understood at this stage and may presumably be related to the column grain texture with the smaller grain size. Table 6.1 lists DOS of the devices before and after plasma hydrogenation.

6.3.9 Effects of Silicide Material

Figure 6.29 shows the ambipolar transfer characteristics of FID SB-TFT device with PtSi Source/Drain. We can see that the on-current is larger in p-channel operation than in n-channel operation. This is due to the lower barrier height for holes (~0.24eV) than for electrons (~0.88eV) in the case of PtSi/Si contact. As a result the contact resistance will be significant for n-channel

operation. The extracted DOS is shown in Fig. 6.30, together with that obtained from the device with $CoSi_2$ S/D. We can see that the upper-band DOS is obviously overestimated for the device with PtSi S/D, owing to the high parasitic resistance presenting at the silicide junction. Thus, for full-band gap DOS analysis, it is essential to choose a proper mid-gap silicide material to obtain accurate gap state density distribution.

6.3.10 Analysis of Full band-gap DOS in SB Poly-Si FinFET

In the previously chapter, we proposed poly-Si SB-TFT with nano-scale channel width featuring silicided Schottky barrier source/drain with field-induced source/drain extension. This device is also called poly-Si SB FinFET. The process flow of fabricating these nano-scale devices is similar to that of fabricating conventional structures with three notable differences: First, e-beam lithography is employed for device patterning throughout the fabrication. Second, the etching selectivity of poly-Si to SiO_2 must be high enough to ensure that the poly-Si channel is not damaged during the process. The etching selectivity in both main etch and over etch steps are larger than 100, which is suitable for nano-scale gate patterning with ultra-thin gate dielectric layer. Third, 10nm-thick sacrificial oxide is needed to remove the damage created by dry-etching processes on the sidewall surface of the poly-Si fin.

In this section we characterize and examine the DOS of the poly-Si SB FinFET. Two splits of samples, denoted as SA- and NSA-series, are characterized. The top view of the SA-series devices with 15nm offset length is shown in Fig. 6.31(a). This device employs a self-aligned sidewall spacer to define the offset region. The top and side views of the NSA-series devices with 1 μm offset length in both drain and source sides (X_D and X_S) are shown in Figs. 6.31(b) ~ (d). An extra mask is employed to define the 1 μm offset channel region. It is worth noting that these devices actually have a triple-gate structure, as can be seen in Fig. 6.31(d) which shows the cross-sectional view along the B---B' direction in Fig 6.31(b). As a result, the effective channel width should be the sum of the Si Fin width (50nm) plus twice of the Si thickness (50nm).

Figure 6.32 shows the ambipolar transfer characteristics of FinFET structure at sub-gate

voltage Vsub=2V and 5V. The on-state current increases as the sub-gate voltage increases. To explain this trend, Fig. 6.33 shows the band diagram near source side, which was also illustrated in Section 4.3. As the sub-gate bias increases, the source-side field emission current is enhanced by the narrowed tunneling width and therefore higher on-current. Fig.6.34 and Fig.6.35 show the ambipolar transfer characteristics of different channel widths. The device with a wide (i.e., 5 μm) channel width serves as the "de facto" planar structure. While the other nanoscale device with three fins, each fin having a width of 50 nm and height of 50 nm, represents an effective channel width of 450 nm. We can see that the poly-Si SB FinFET exhibits much steeper subthreshold swing comparing with the device with planar with. Fig. 6.36 shows the ambipolar transfer characteristics and Tx(d(logG)/dV_G) against 1000/T, from which we can deduce that the flat band is around –0.4V. Fig. 6.37 shows the extracted DOS of the planar structure (W=5um) and FinFET (W=0.45um) structure. It can be seen the DOS is smaller in the FinFET structure than in the planar structure. This is because the FinFET has a channel thickness that is narrower than the depletion length and thus the effective DOS within the channel is lowered. In other words, the controllability of gate bias on adjusting the channel potential is promoted when a nano-scale fin channel is employed, and thus the subthreshold swing is improved.

6.3.11 A New & Simpler Methodology to Determine Flat-band Voltage

Precise determination of the flat-band voltage is essential for building the relationship between DOS and the energy level inside the gap. As mentioned above, in order to achieve this purpose, a number of conductance measurements needs to be performed at various temperatures. Moreover, in conventional approach, the process needs to be conducted separately on p- and n-channel devices. It is thus very tedious and time-consuming. In this work, we experimentally found that the flat-band voltage obtained using the above method is actually in close proximity with the gate voltage at the intersection point of p- and n-mode I-V curves measured at room temperature. An example is provided by the results shown in Figs. 6.3 and 6.5. We can see that the p- and n-mode I-V curves at 25 ^oC intersected at V_G ~ -2V, which is very close to the result obtained in Fig. 6.3 (V_{FB} ~ -2.1 V). We thus propose a simpler methodology to determine the flat-band voltage by simply measuring the gate

voltage at the intersection point of p- and n-mode I-V curves measured at room temperature using a single SB TFT. To validate this method, a number of samples were characterized and the results are summarized in Fig. 6.38. We can see that the difference between the conventional method and our method is indeed quite small. To take advantage of this simpler method, we modify the flow chart for analysis of full band-gap DOS using the SB TFT in Fig. 6.39. This scheme greatly simplify the process of conventional approach shown in Fig. 6.2, since only two I-V measurements performed on a single device at room temperature is required for the analysis.

6.4 Summary

In this chapter, we have proposed and successfully demonstrated a novel approach to extract the full band-gap DOS of the TFT channel. In this approach, the field-effect conductance method is performed on an SB poly-Si TFT which has the capability of ambipolar operation. Both incremental and temperature methods are adopted on the SB and conventional devices to construct the relationship between DOS and the energy level in the gap. For devices with the same channel material, the results are in good agreement among the different measurement schemes, indicating that the novel approach is very reliable.

We have also characterized the dependence of both electrical and structural parameters on the measurement results in order to set suitable test conditions. Our results indicate that the parasitic resistance presenting in the channel would result in an overestimation of tail state density. Accurate DOS extraction can be obtained by employing sufficiently high drain and sub-gate biases and short electrical junction. In addition, near-mid-gap silicide material such as $CoSi_2$ is desirable for reliable full band-gap DOS analysis.

We have also characterized the effect of process treatments including re-crystallization and plasma hydrogenation steps on the DOS characteristics. Their impacts could be clearly identified using the new approach. Benefits of using a nano-scale fin channel for promotion of the controllability of gate voltage over the channel potential is also clearly demonstrated.

Finally, we show that the flat-band voltage can be approximated by simply measuring the gate voltage at the intersection point of p- and n-mode I-V curves. The overall process is thus greatly simplified with cost-s aving compared with the conventional approach, since only two I-V measurements performed on a single device at room temperature are all that needed. We strongly believe that the novel method is extremely useful for practical applications.

References :

[1] Ichio Yudasaka, et al., “Ploysilicon thin-Film Transistors”, Mat Res. Soc. Symp. Proc., pp.162, vol.182, 1990.

[2] Byung-Seong Bae and Choochon Lee, “Effect of interface state distribution on field effect conductance activation energy in hydrogenated amorphous silicon thin film transistors”, J. Appl. Phys., vol.88, pp.3439-3442, 1990

[3] M. J. Powell, J. Pritchard, “The effect of surface states and fixed charge on the field effect conductance of amorphous silicon”, J. Appl. Phys., vol.54, pp. 3244-3248, 1983

[4] S.Hirae , M.Hirose , and Y. Osaka , “Energy distribution of trapping states in polycrystalline silicon”, J. Appl. Phys., vol.51, pp.1403, 1980

[5] Werner. J, and Peisl. M, “Exponential band tails in polycrystalline semiconductor films”, Phys.Rev. B, vol.31, pp.6881, 1985

[6] G. Fortunato, P. Migliorato, “Field-effect analysis for the determination of gap-state density and Fermi-level temperature dependence in polycrystalline silicon”, Phil. Mag. B., vol.57, pp.573-586, 1988

[7] Philips Research Laboratories, Redhill, Surrey, “Analysis of field-effect conductance measurements on amorphous semiconductors”, Phil. Mag. B., vol.43, pp.93-103, 1981

[8] Tohru Suzuki, Masataka Hirose, Yukio Osaka, “Theoretical inpretations of the gap state density determined from the field effect and capacitance-voltage characteristics of amorphous semiconductors”, Jap. J. Appl. Phys., vol.21, pp.L159-161, 1982

[9] Nancy B. Goodman and H. Fritzsche, “Analysis of field-effect and capacitance-voltage measurements in amorphous semiconductors”, Phil. Mag. B., 1980, vol. 42, pp.149-165, 1980

[10] G. Fortunato, and P. Migliorato, “Determination of gap state density in polycrystalline silicon by field-effect conductance”, Appl. Phys. Lett., vol.49, pp.1025, 1986

[11] Tsu-Jae King, Michael G. Hack, and I-Wie. Wu, “Effective density-of-states distributions for

accurate modeling of polycrystalline-silicon thin-film transistors ”, J. Appl. Phys., vol.75,pp. 908-913, 1994

[12] H. C. Lin, C. Y. Lin, K.L. Yeh, R.G. Huang, M.F. Wang, C.M. Yu, T. Y. Huang, and S. M. Sze, “A novel implantless MOS thin-film transistor with simple processing, excellent performance and ambipolar operation capability”, IEDM Tech. Dig., vol.10, pp. 857-859 , 2000

[13] H. C. Lin, K.L. Yeh, R.G. Huang, and T. Y. Huang, “Schottky barrier thin-film transistor (SBTFT) with silicided source/drain and field-induced drain extension”, IEEE Electron Device Lett., vol. 22, pp. 179-181, 2001.

[14] H. C. Lin, K.L. Yeh, R.G. Huang, T. Y. Huang, and S. M. Sze, “Ambipolar Schottky barrier thin-film transistor (SBTFT),” IEEE Trans. Electron Devices., vol. 49, pp. 264-270, 2002.

[15] K.L. Yeh, H. C. Lin, R.G. Huang, R. W. Tsai, and T. Y. Huang, “Reduction of off-state leakage current in Schottky barrier thin-film transistors (SBTFT) by a field-induced drain,” Jpn. J. Appl. Phys., vol.15, pp.315-329, 2002.

[16] H. C. Lin, Kuan-Lin Yeh, R.G. Huang, and T. Y. Huang, “Impacts of field-induced drain (FID) on the ambipolar operation of poly-Si Schottky barrier thin-film transistors (SBTFT’s)”, Proc. Active–Matrix Liquid-Crystal Display (AM-LCD)., vol. 1, 2001, pp. 247-250.

[17] Weisfield, R.L, and Anderson,D.A, “Analysis of field effect conductance measurements on amorphous semiconductor ”, Phil. Mag. B., vol.33, pp.935, 1981

[18] I-Wei Wu, Tiao-Yuan Huang, Warren B. Jackson, “passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation ”, IEEE Electron Device. Lett., vol12, pp.181-183, 1991

Gap state density \channel film		Solid Phase Crystallization (SPC)	As-deposited	ELA
Mid-gap state density	Before Hydrogenation	~$8x10^{18}$	$2.2x10^{19}$	$5.4x10^{17}$
	After Hydrogenation	~$2x10^{18}$	$7.8x10^{18}$	
Tail-state density	Before Hydrogenation	$5.6x10^{20}$	$3.5x10^{21}$	$6.8x10^{19}$
	After Hydrogenation	~$2.1x10^{20}$	$7.3x10^{20}$	

Table 6.1 Gap state density of different channel films.

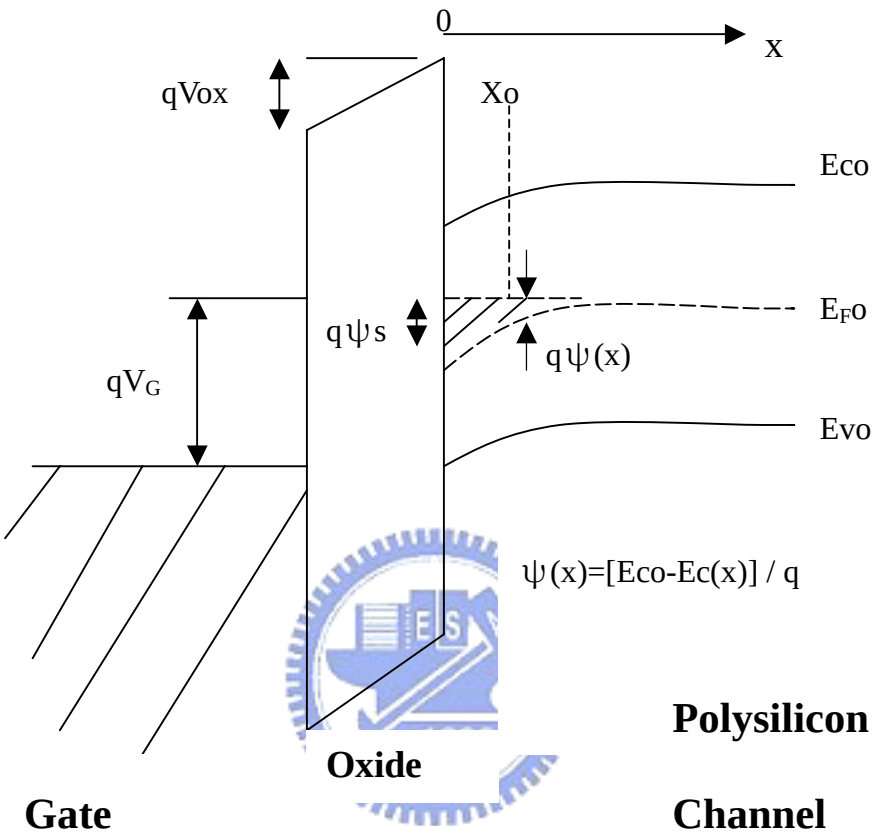


Fig. 6.1 1-D Band diagram of a gate-oxide-poly-Si channel structure. x is 0 at the oxide/poly-Si interface.

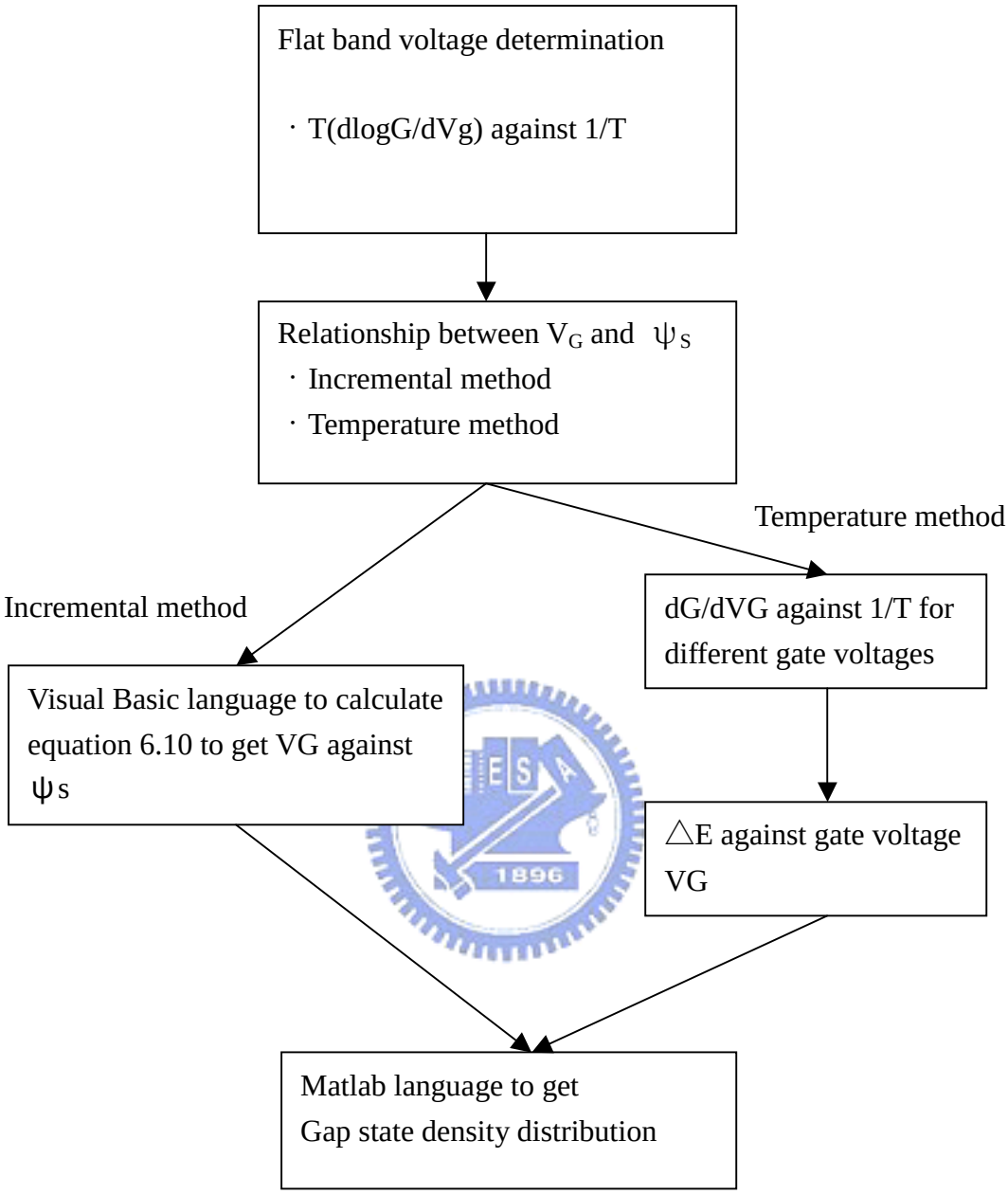


Fig. 6.2 Flow chart for determination of DOS using conventional approach.

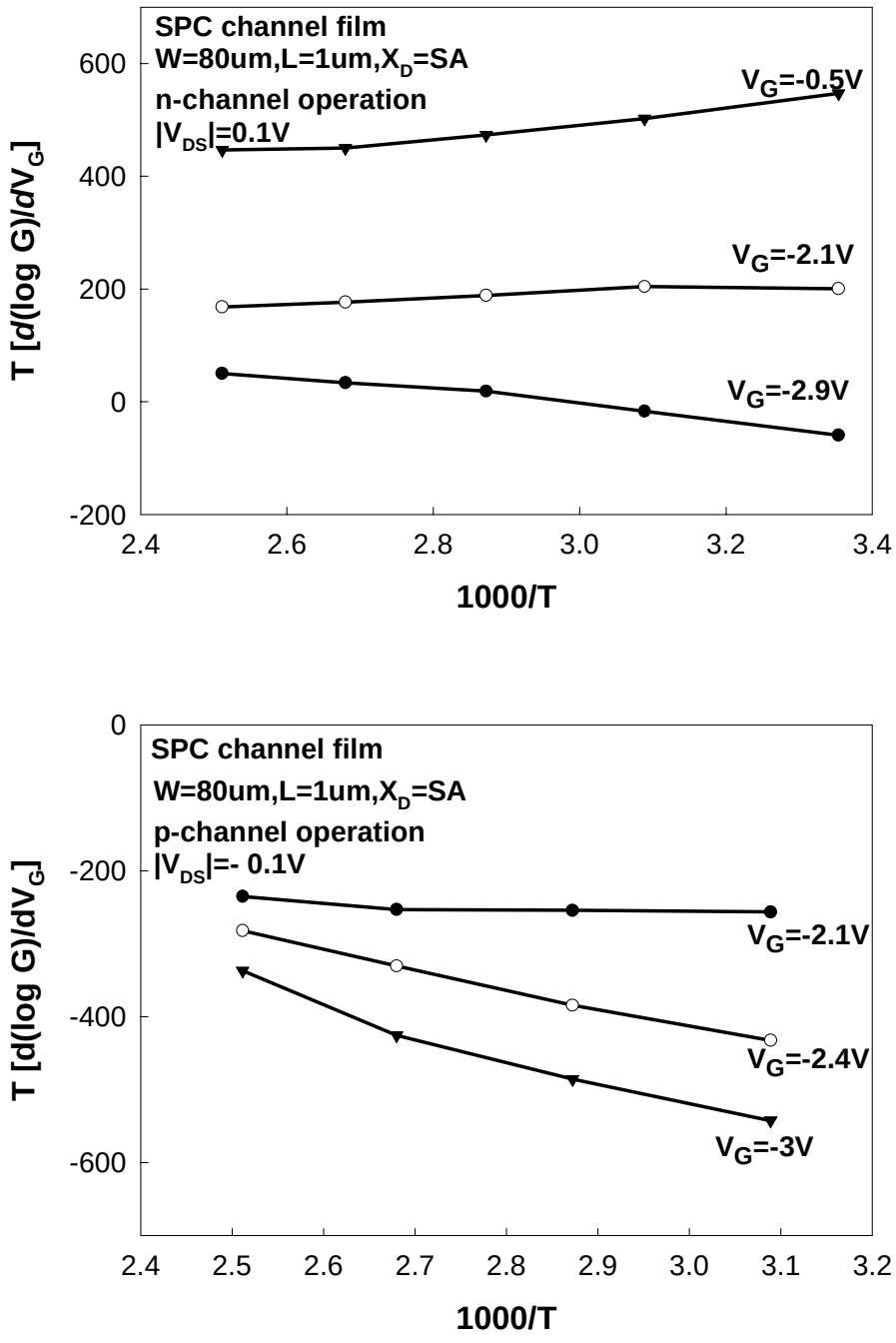


Fig. 6.3 Flat-band voltage determination of FID SB-TFT using Tx($d$logG/dV$_G$) vs. 1/T plots: (a) n-channel operation; (b) p-channel operation.

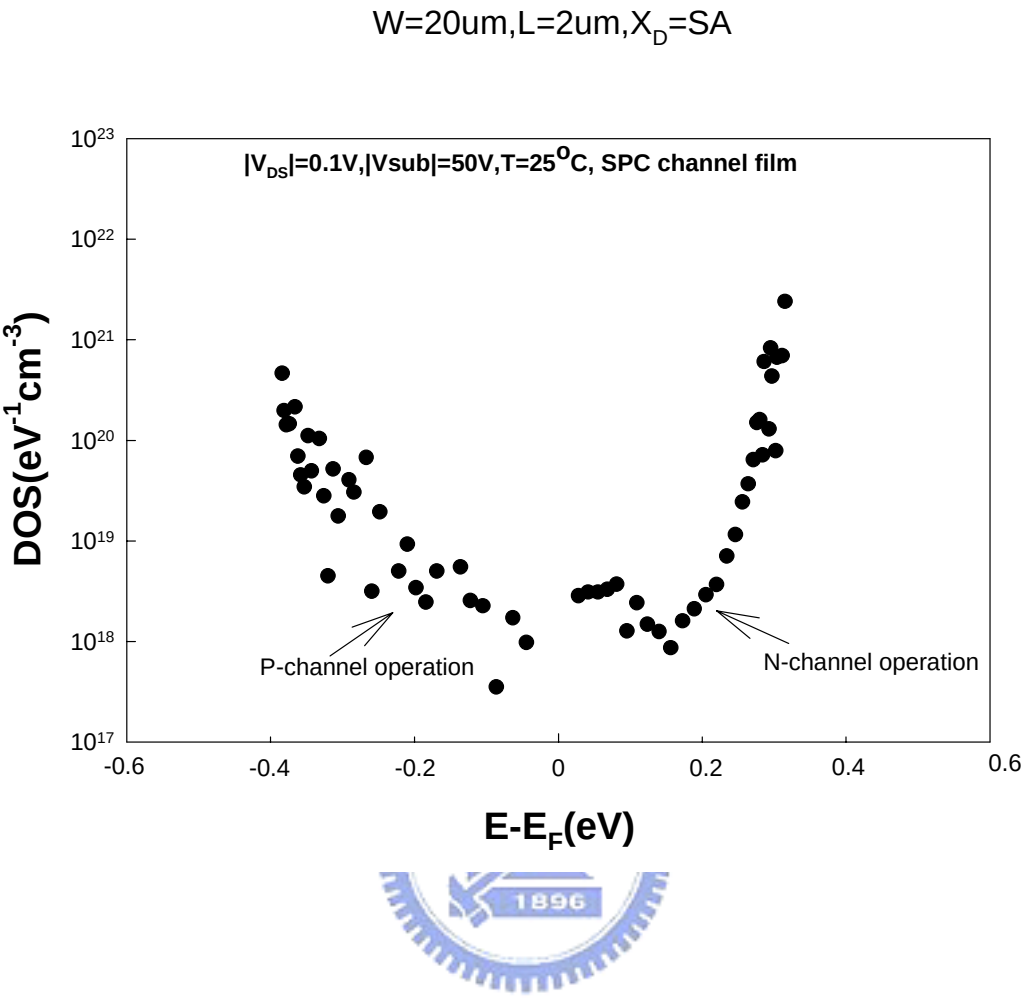


Fig. 6.4 Full-band DOS distribution extracted using FID SB-TFT.

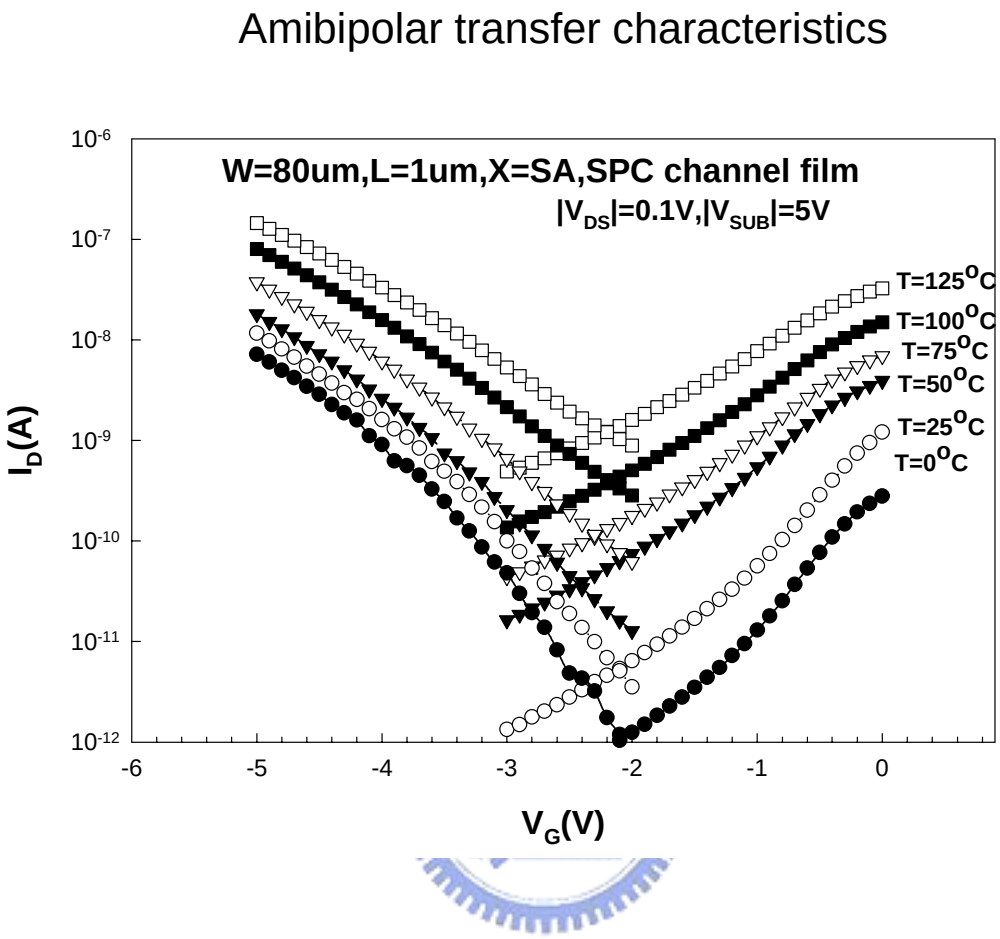


Fig. 6.5 Drain current versus gate voltage characteristics.

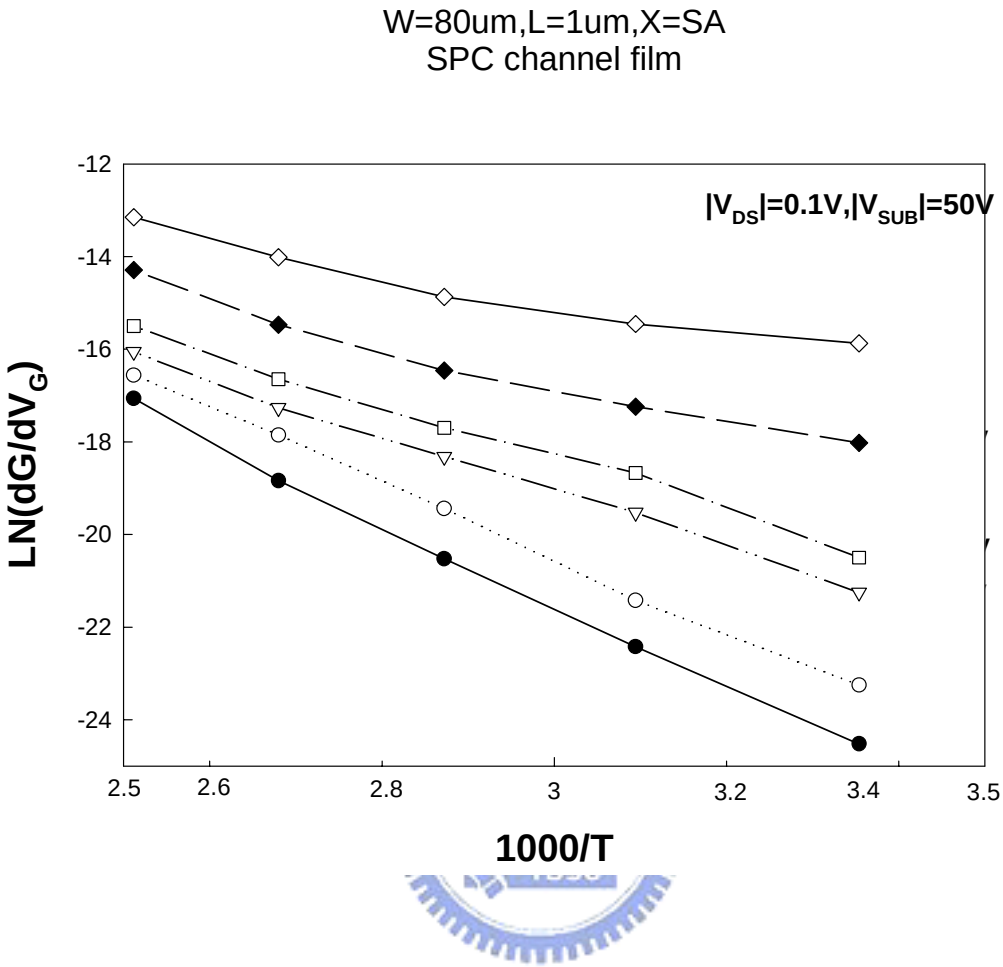


Fig. 6.6 **Arrhenius plots of Ln (dG/dV_G) extracted from Fig. 6.5.**

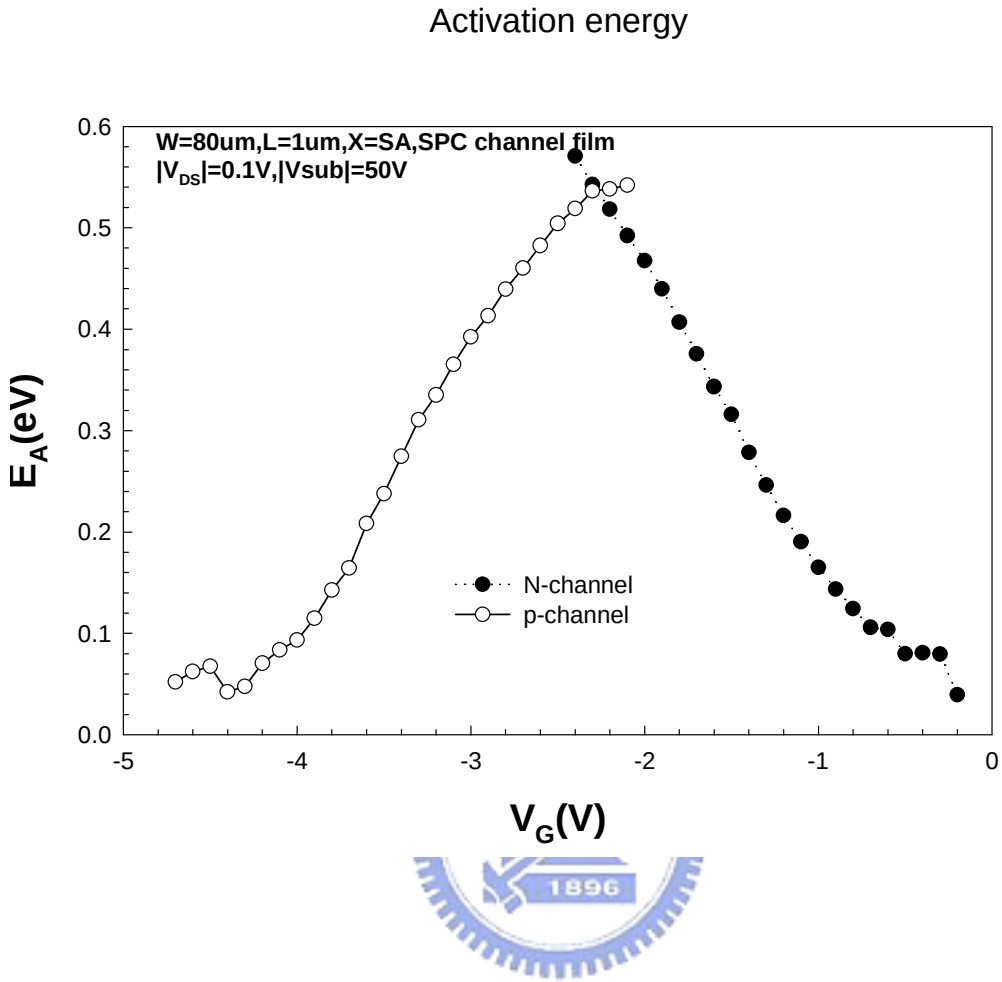


Fig. 6.7 Activation energy versus gate voltage characteristics.

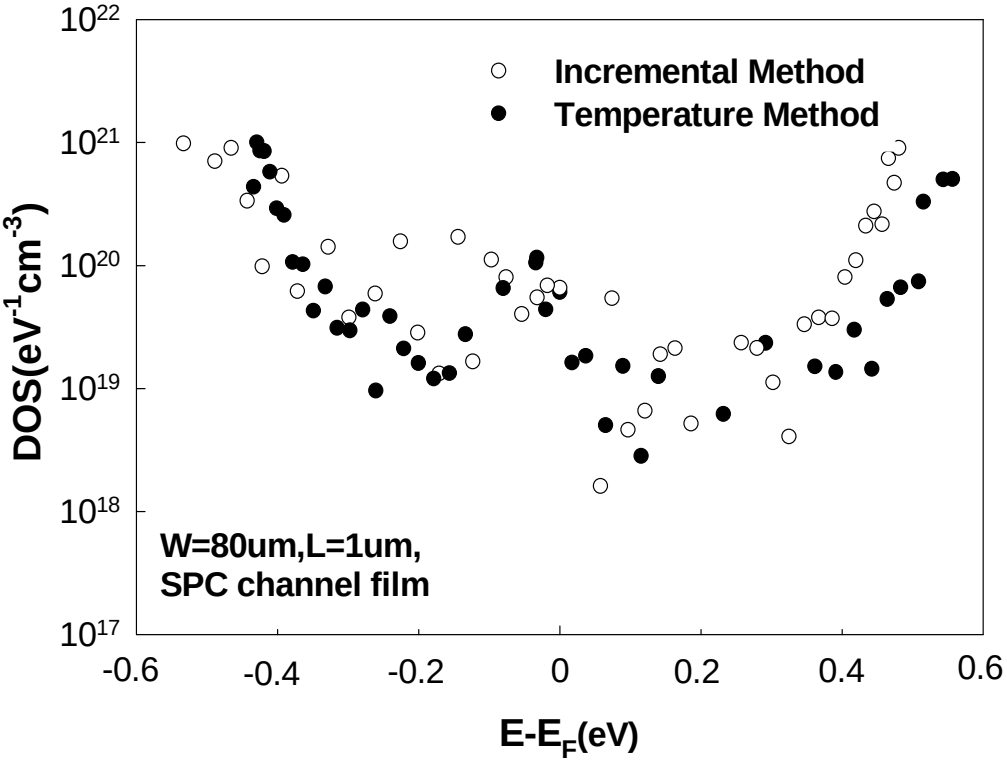


Fig. 6.8 Full-band Gap state density distribution deduced by the incremental method and the temperature method.

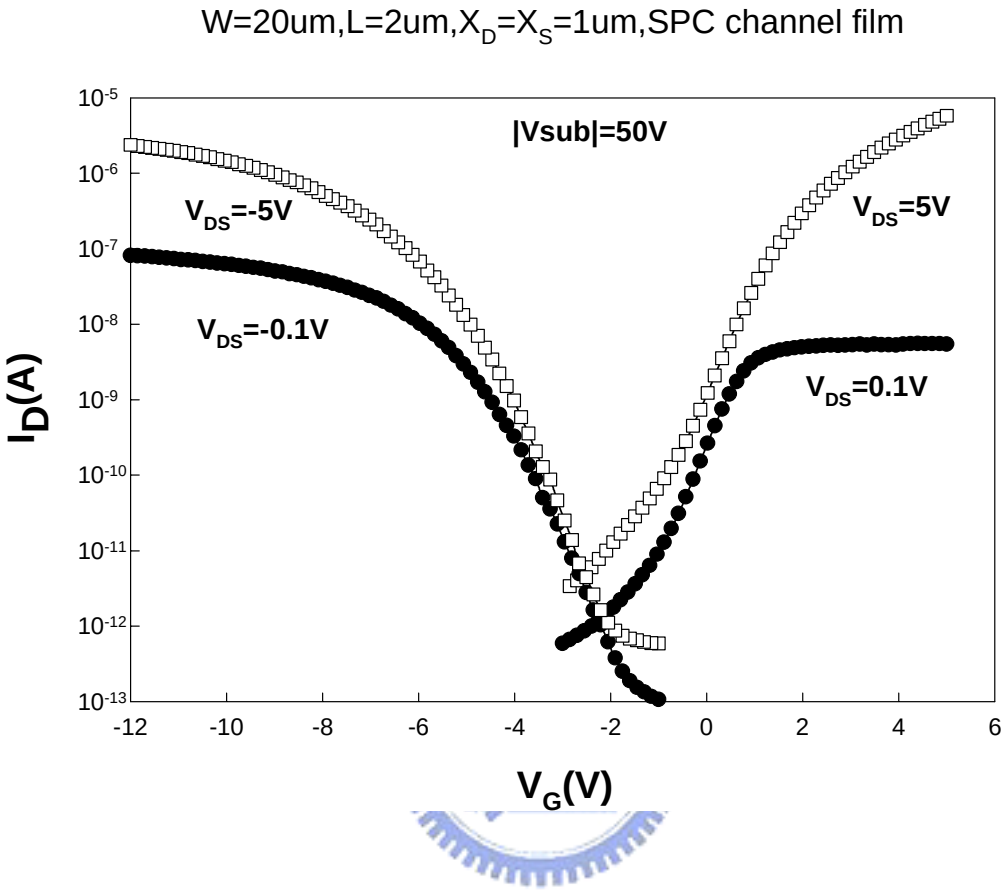


Fig. 6.9 Ambipolar transfer characteristics under both low and high drain bias.

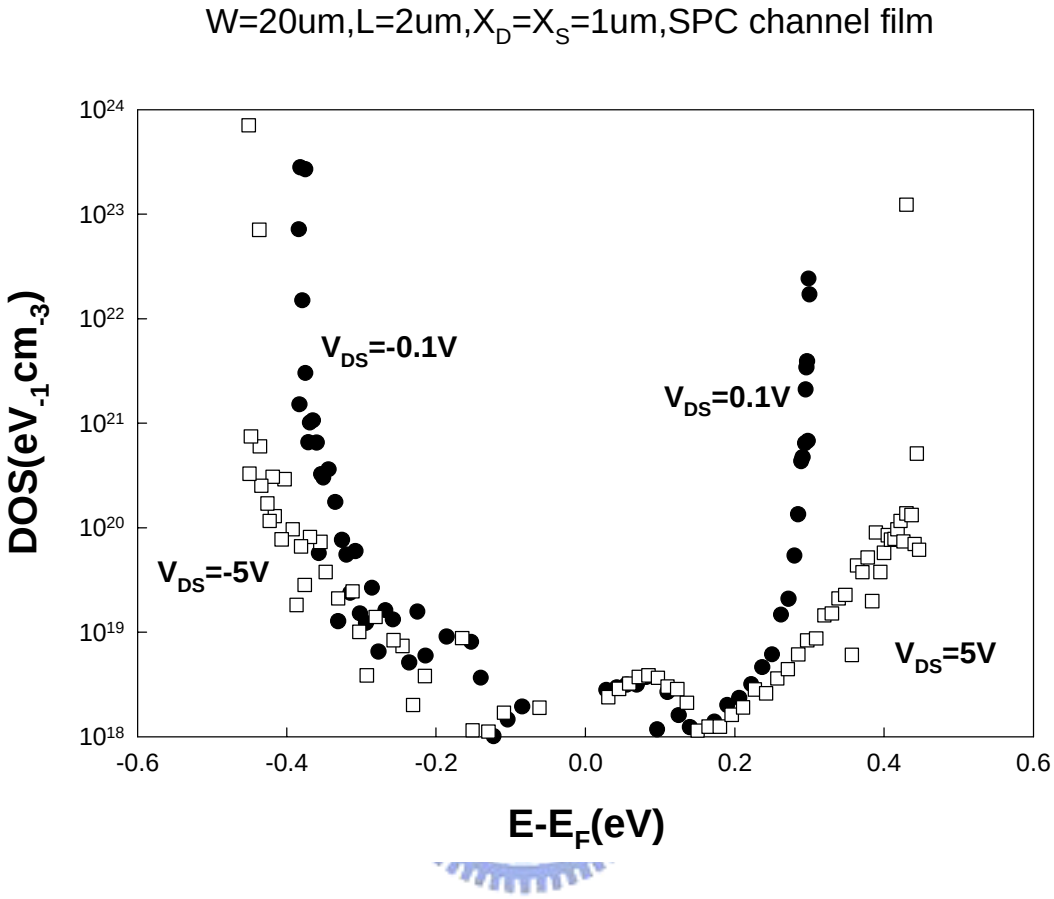
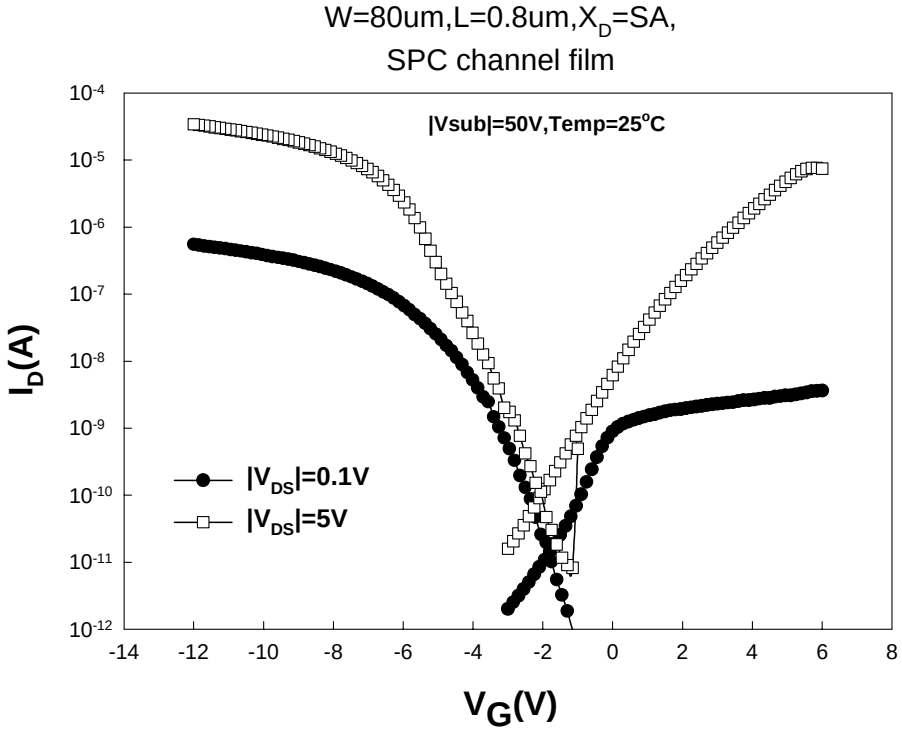
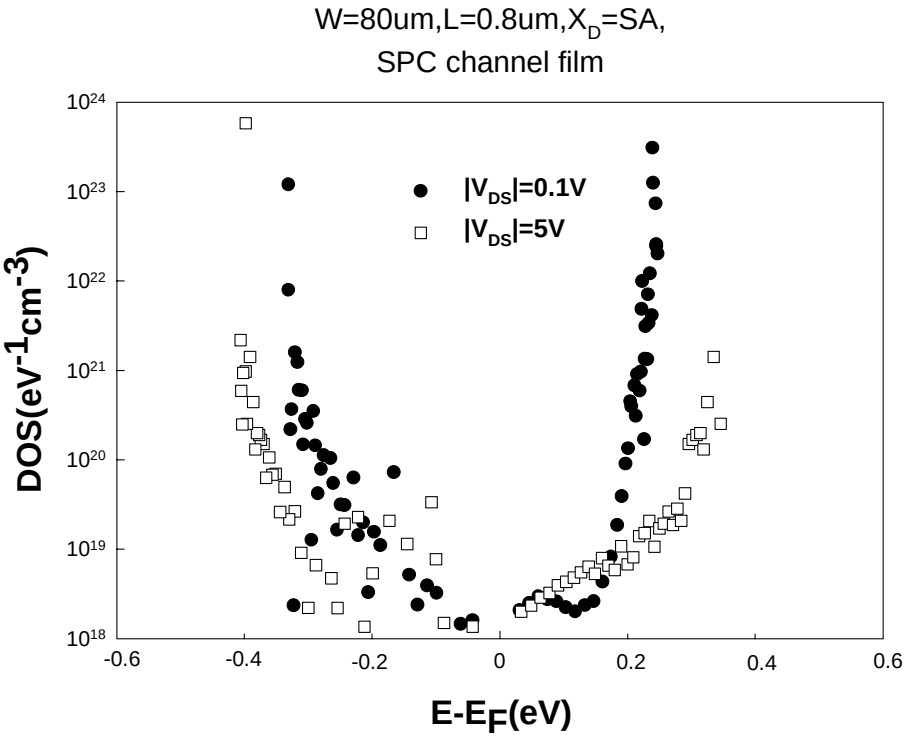


Fig. 6.10 Full-band gap DOS extracted at $|V_{DS}|$ of 0.1 and 5 V.

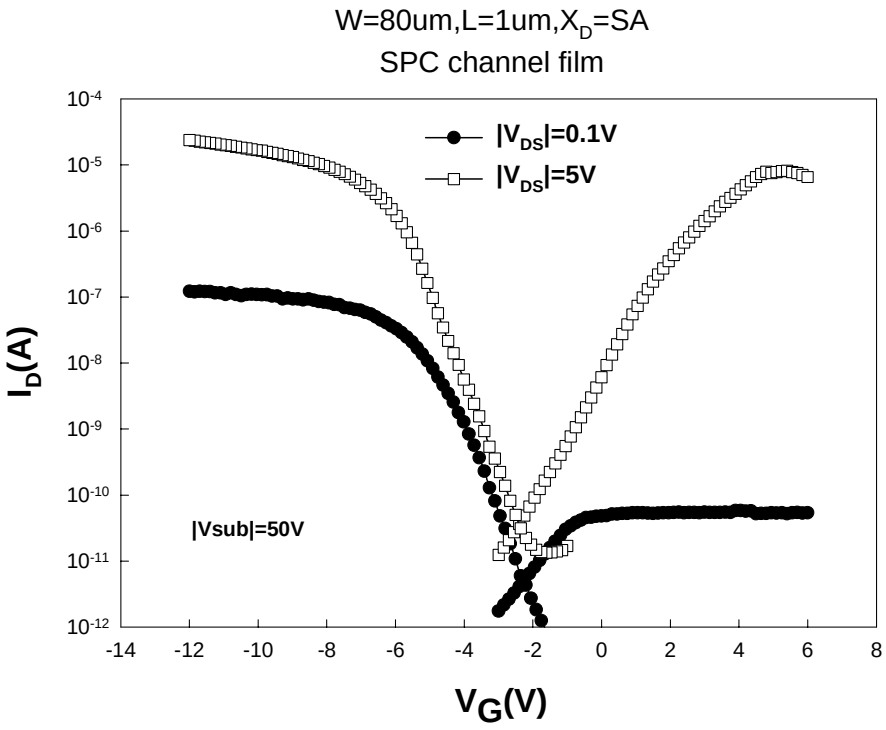


(a)

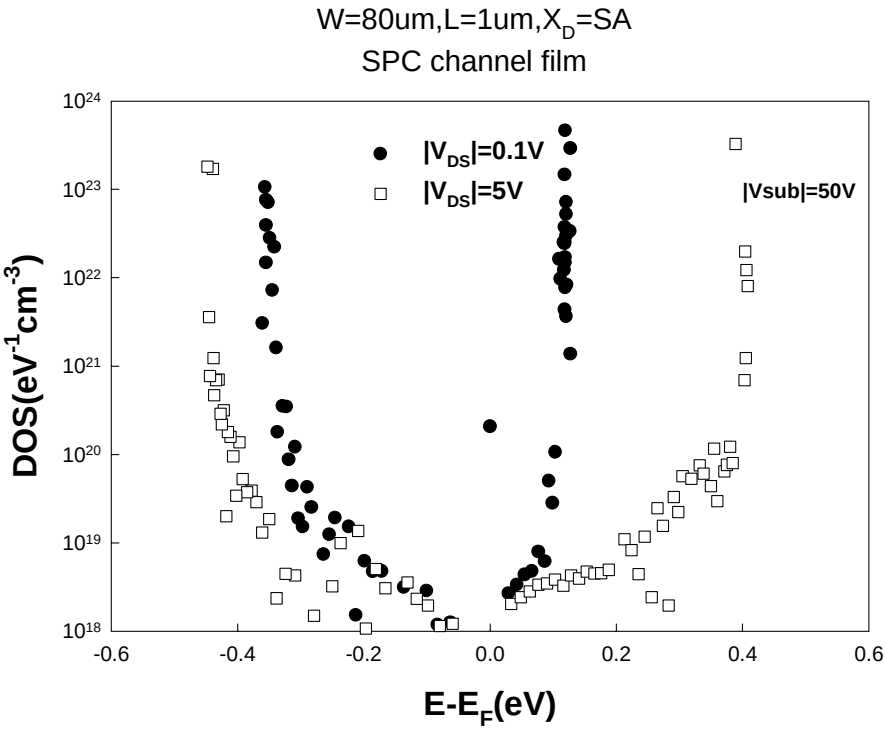


(b)

Fig. 6.11 (a) Ambipolar transfer characteristics, and (b) the extracted DOS results in a device with channel length of 0.8um.

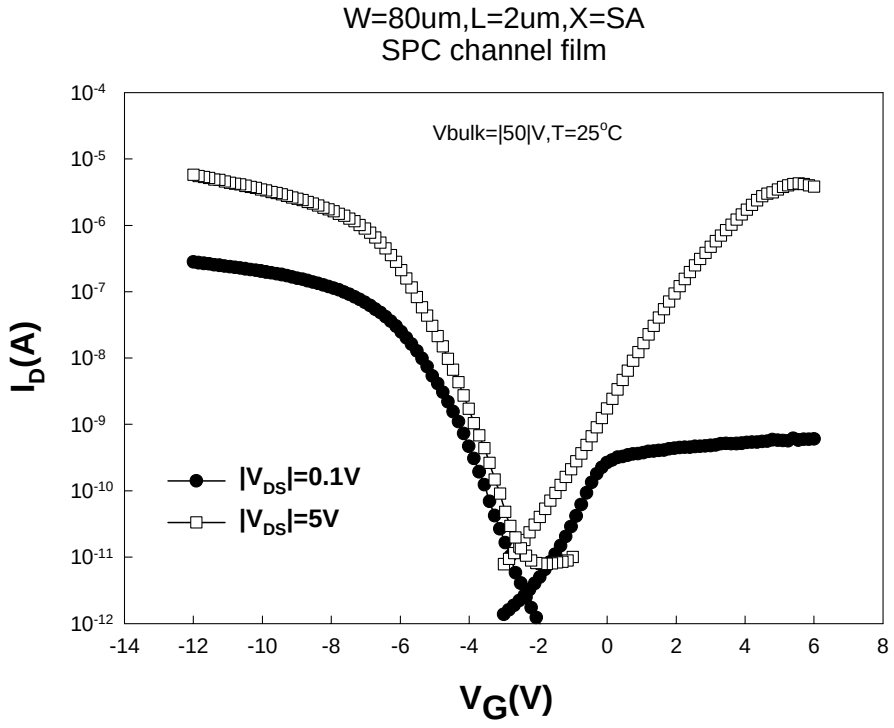


(a)

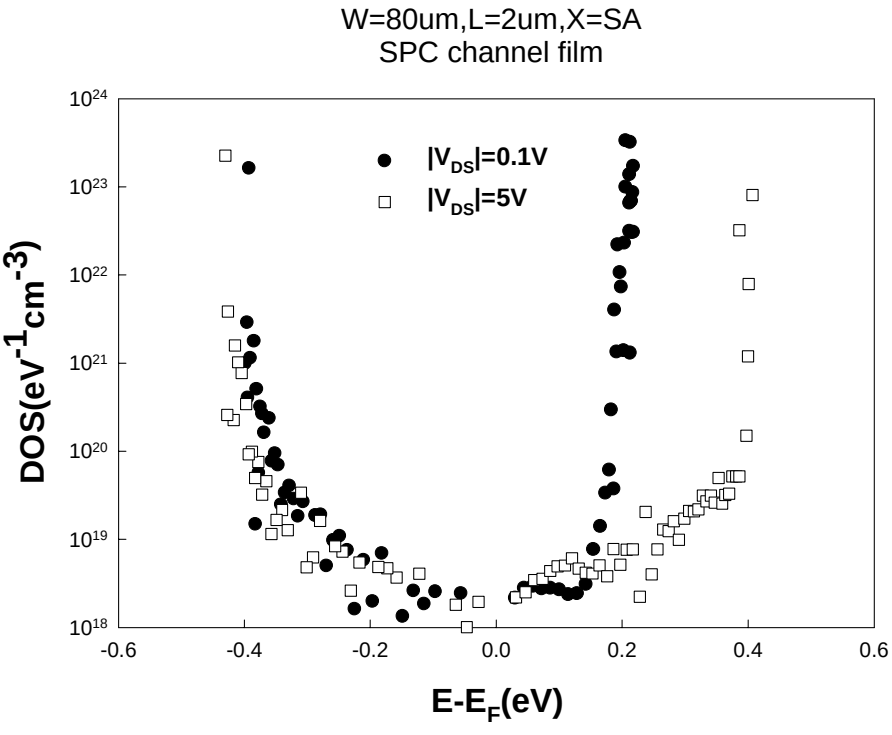


(b)

Fig. 6.12 (a) Ambipolar transfer characteristics, and (b) the extracted DOS results in a device with channel length of 1um.

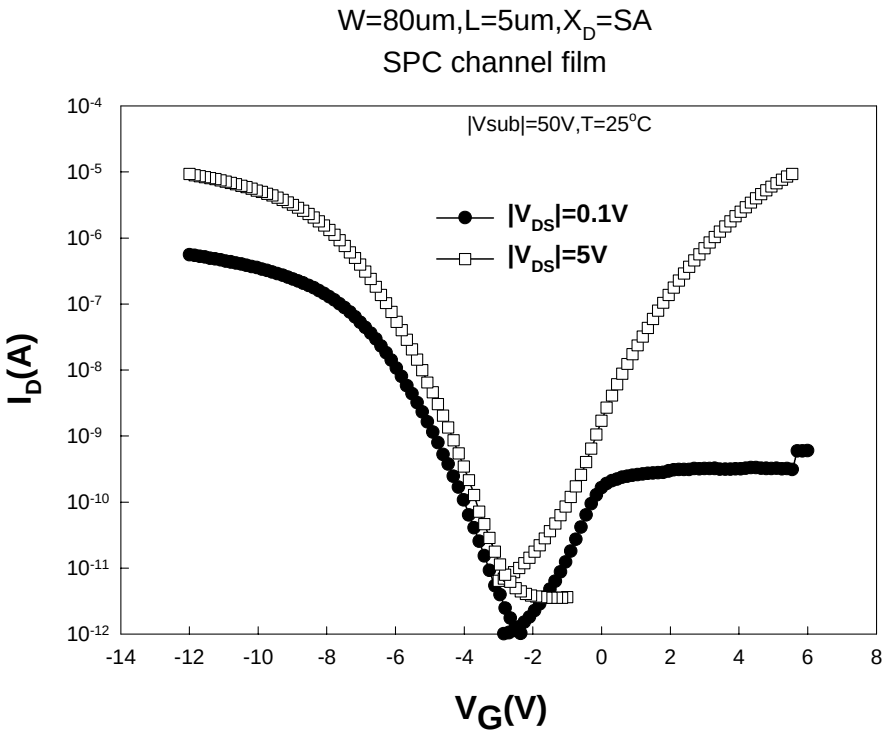


(a)

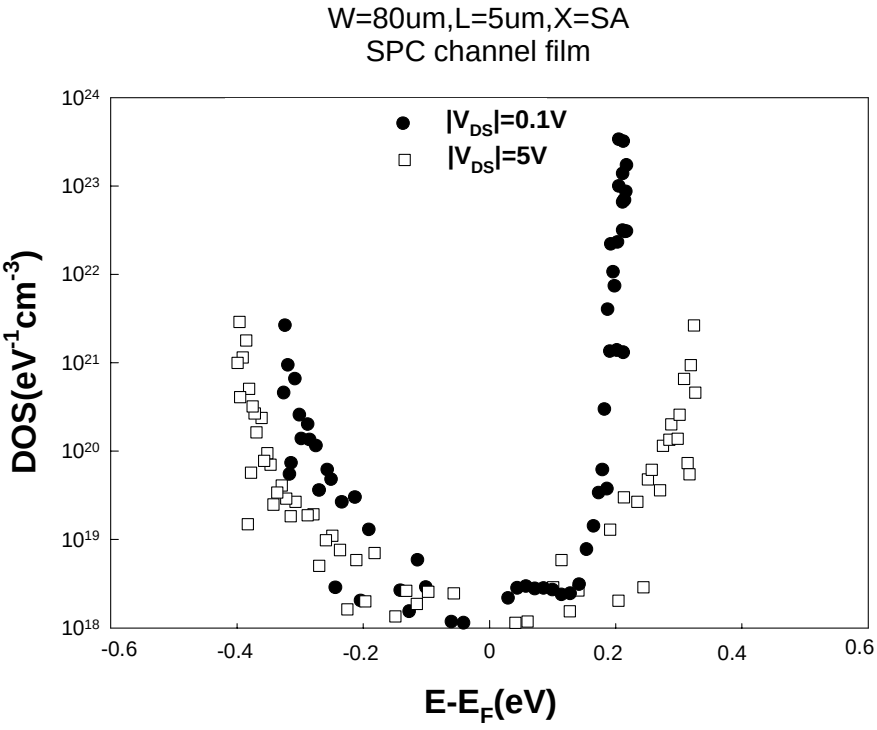


(b)

Fig. 6.13 (a) Ambipolar transfer characteristics, and (b) the extracted DOS results in a device with channel length of 2um.



(a)



(b)

Fig. 6.14 (a) Ambipolar transfer characteristics, and (b) the extracted DOS results in a device with channel length of 5um.

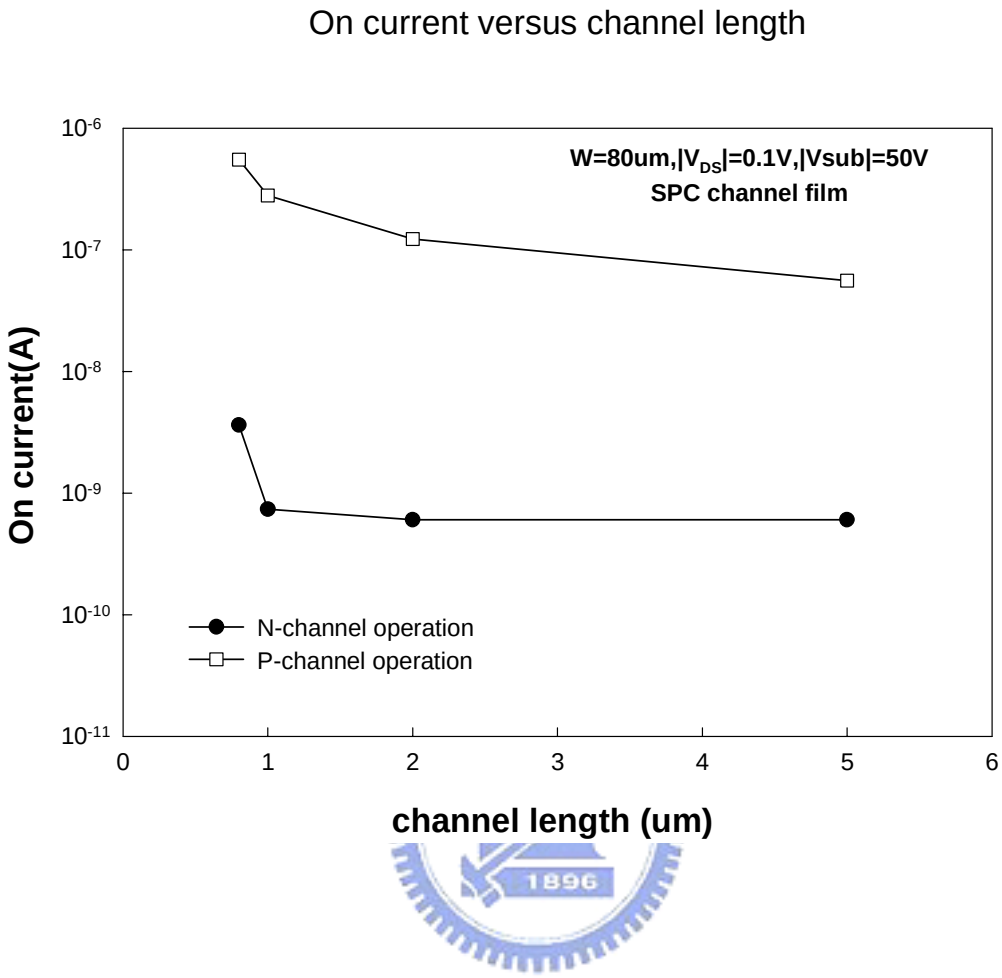
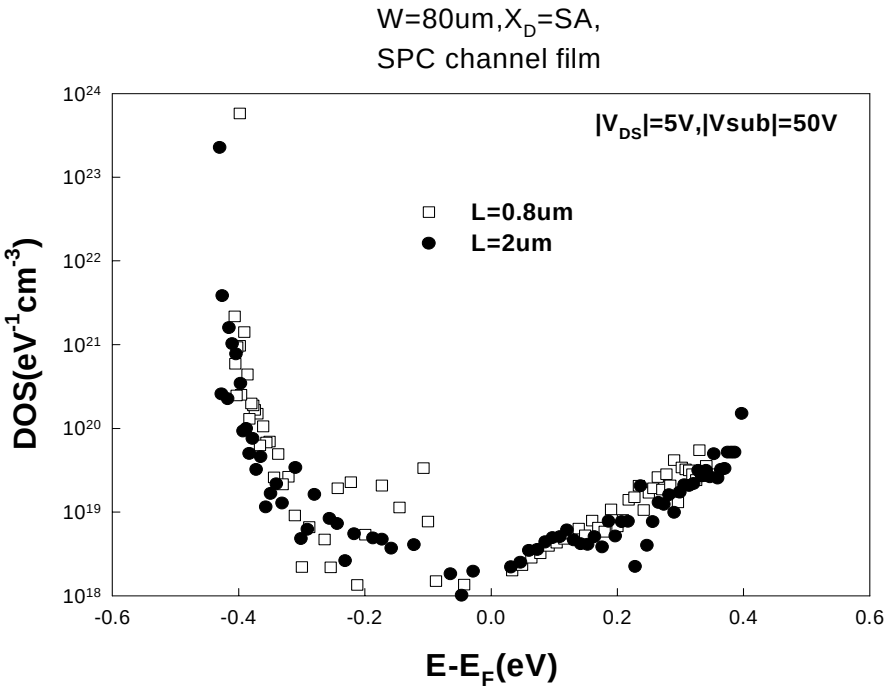
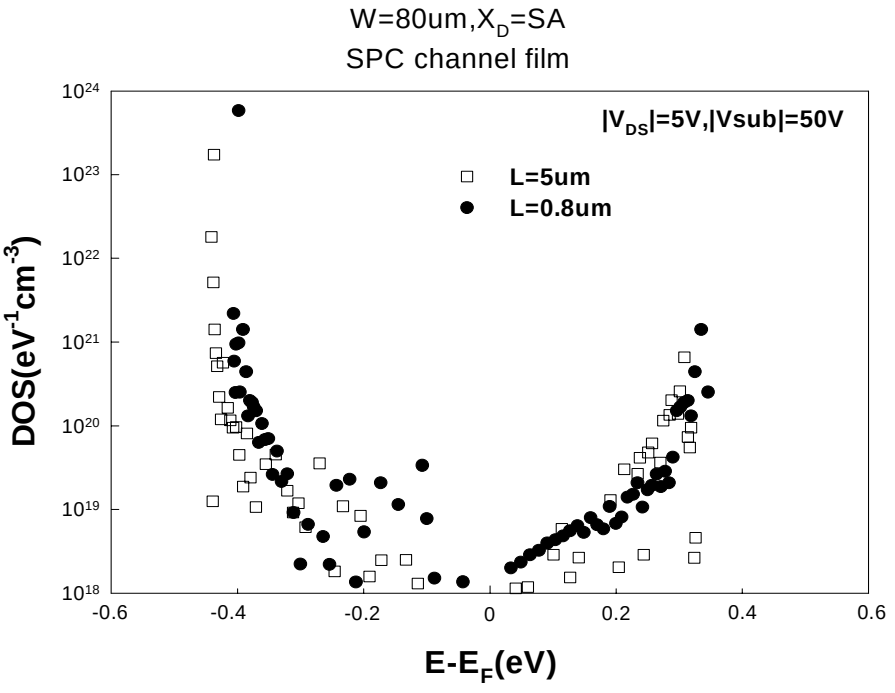


Fig.6.15 **On-current vs. channel length.**

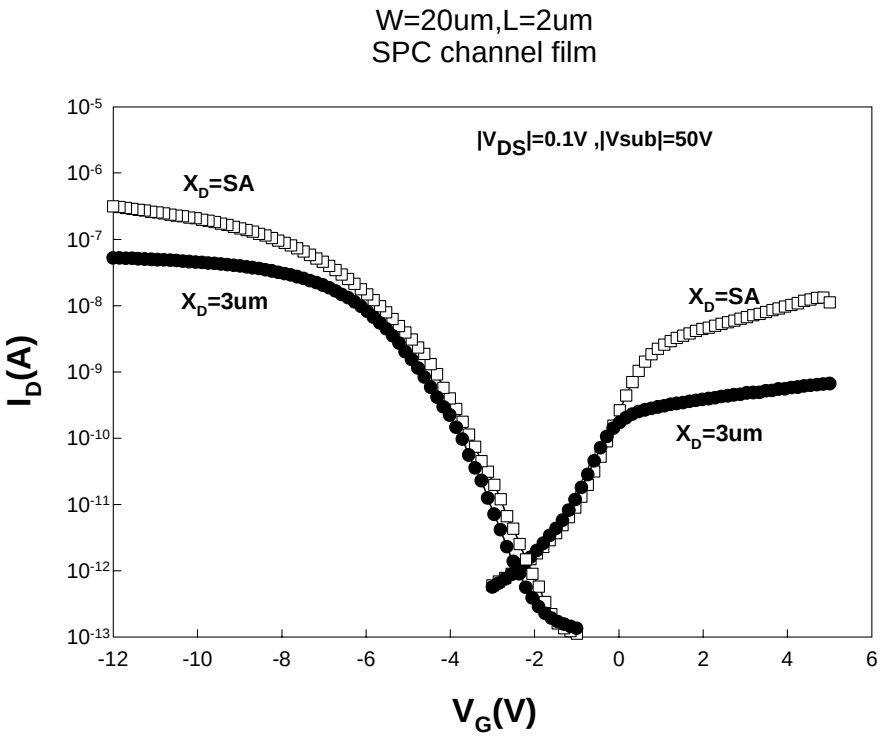


(a)

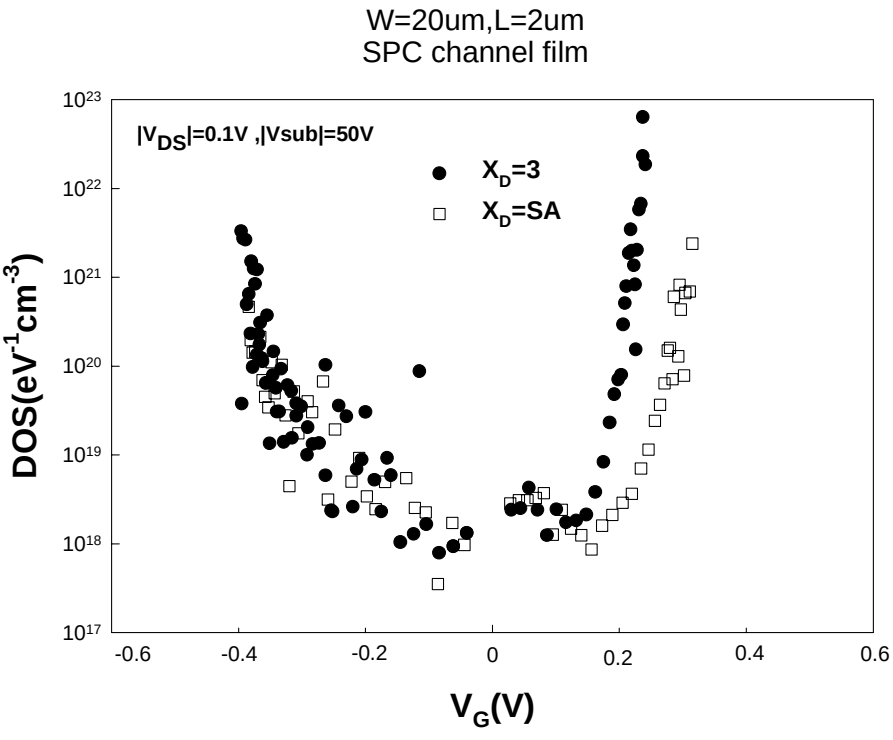


(b)

Fig. 6.16 (a), (b) Comparison of DOS extracted in devices with various channel lengths.reasonable agreement is achieved among these devices, indicating that $|V_{DS}|$ of 5 V is sufficient large so the effects of parasitic resistance is insignificant.

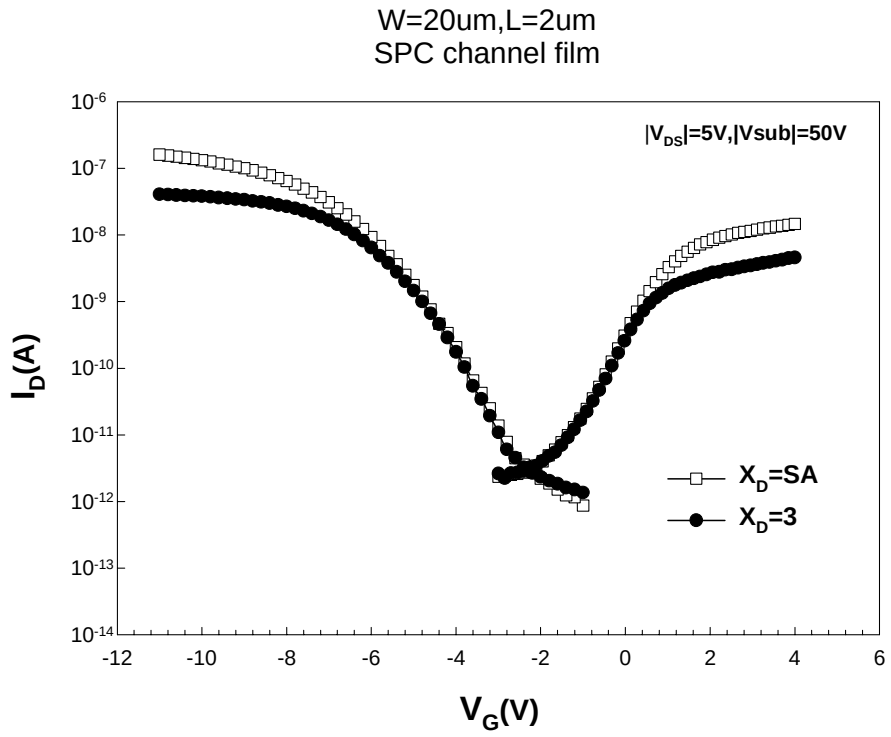


(a)

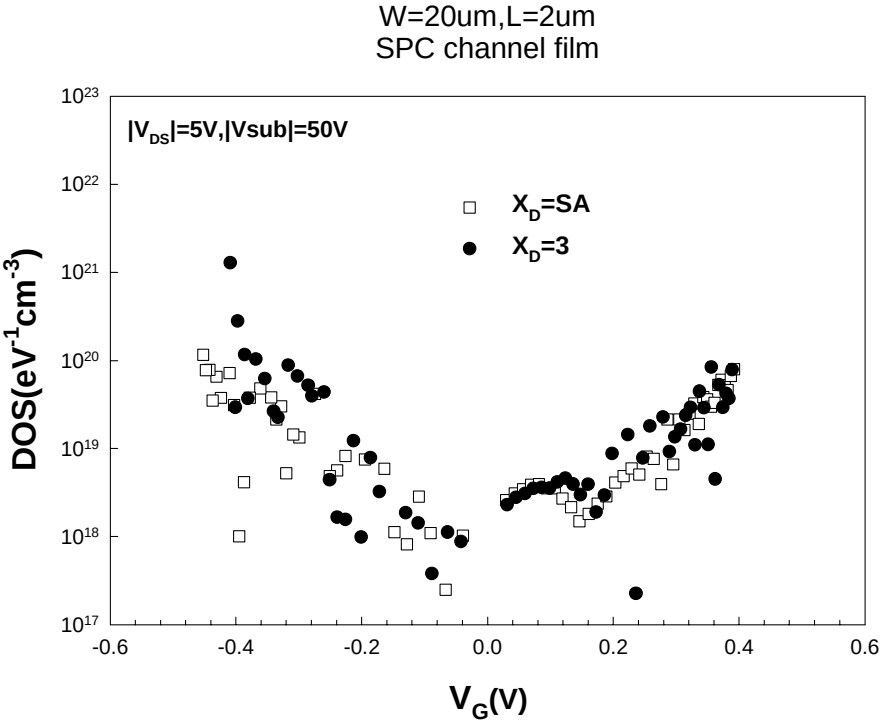


(b)

Fig. 6.17 (a) Ambipolar transfer characteristics, and (b) extracted full-band gap DOS of devices with various drain-side offset lengths at $|V_{DS}|$ of 0.1 V.



(a)



(b)

Fig. 6.18 (a) Ambipolar transfer characteristics, and (b) extracted full-band gap DOS of devices with various drain-side offset lengths at $|V_{DS}|$ of 5 V.

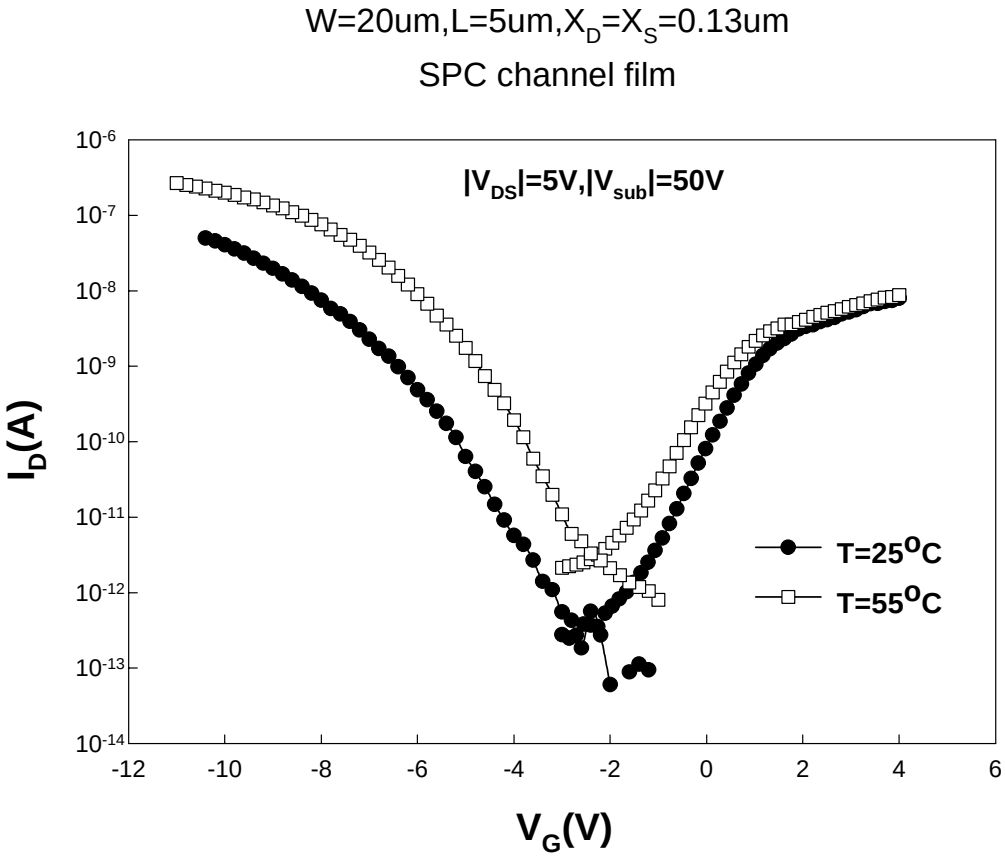


Fig. 6.19 Ambipolar transfer characteristics measured at 25 and 55 °C.

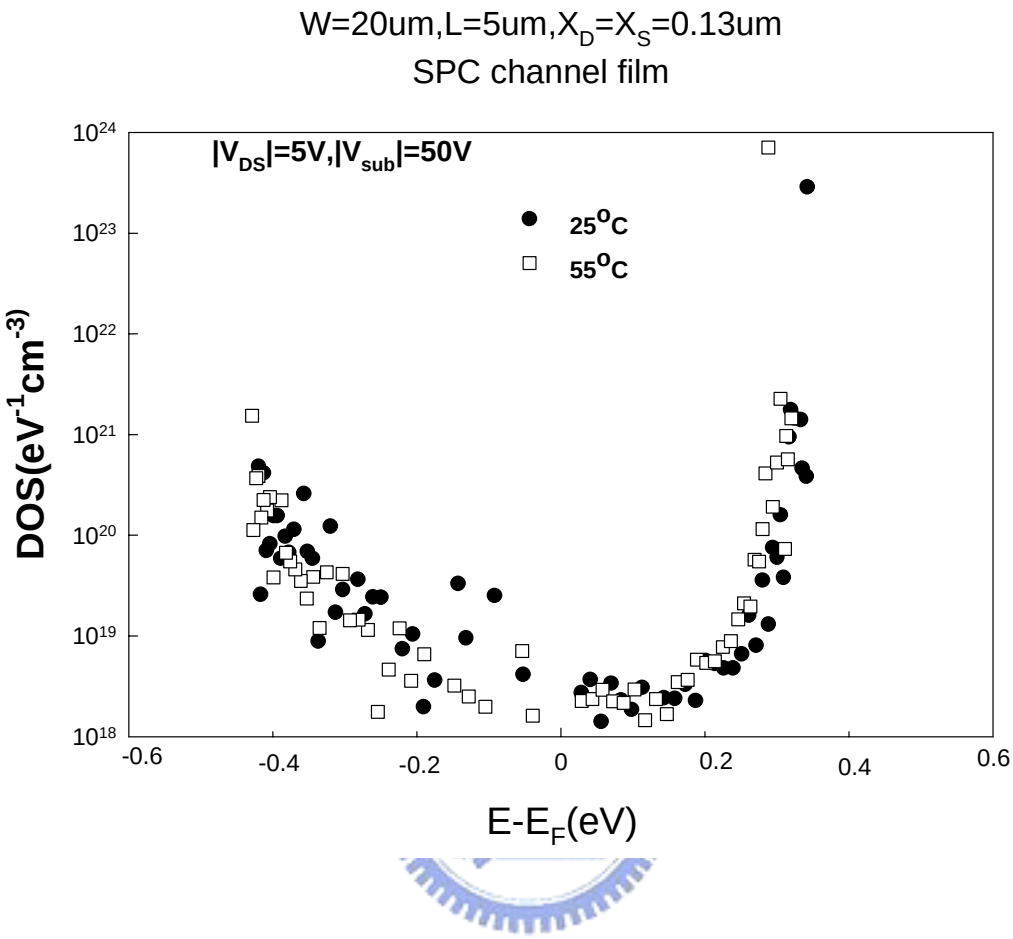


Fig. 6.20 **DOS extracted at 25 and 55 °C.**

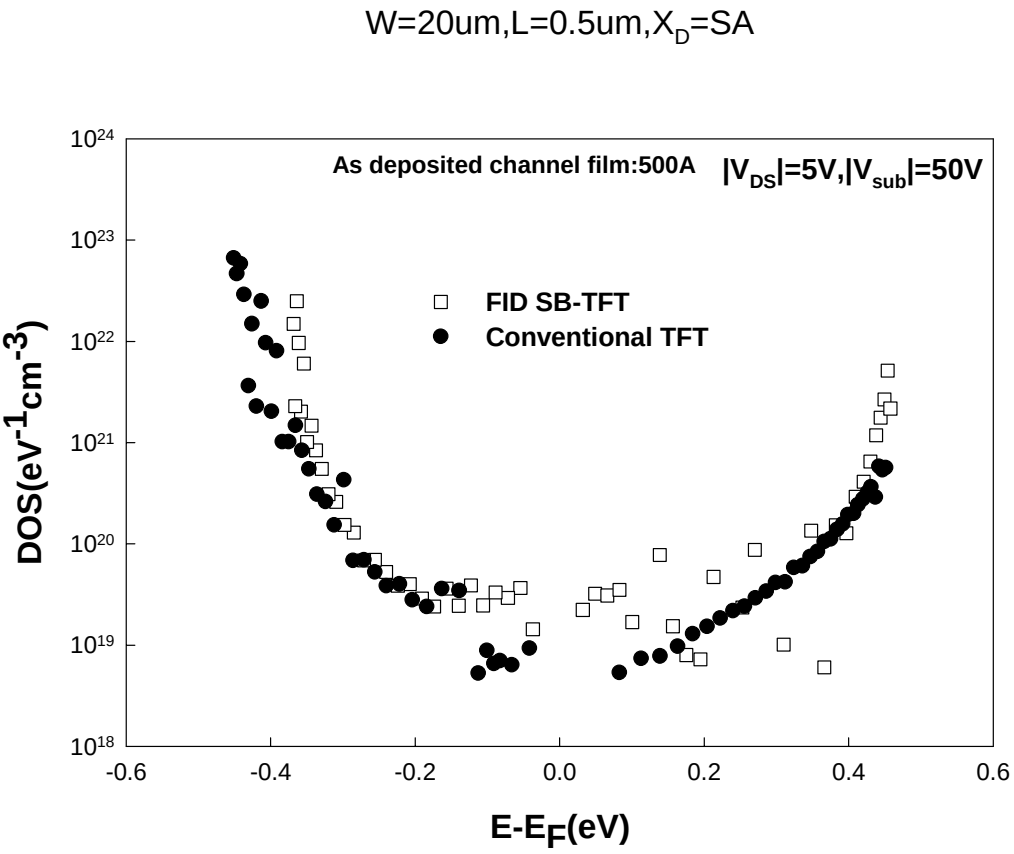


Fig. 6.21 Comparisons of DOS extracted from FID SB-TFT and Conventional TFTs.

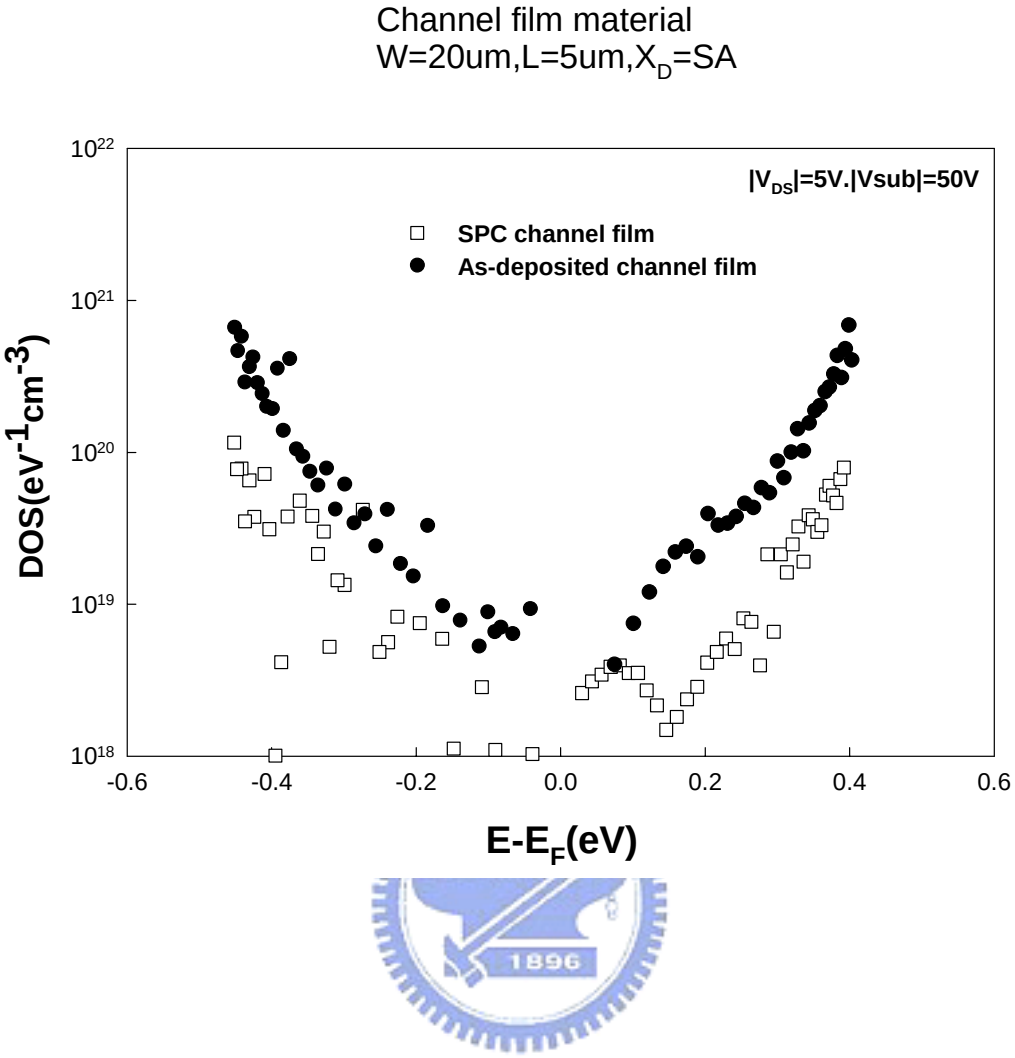
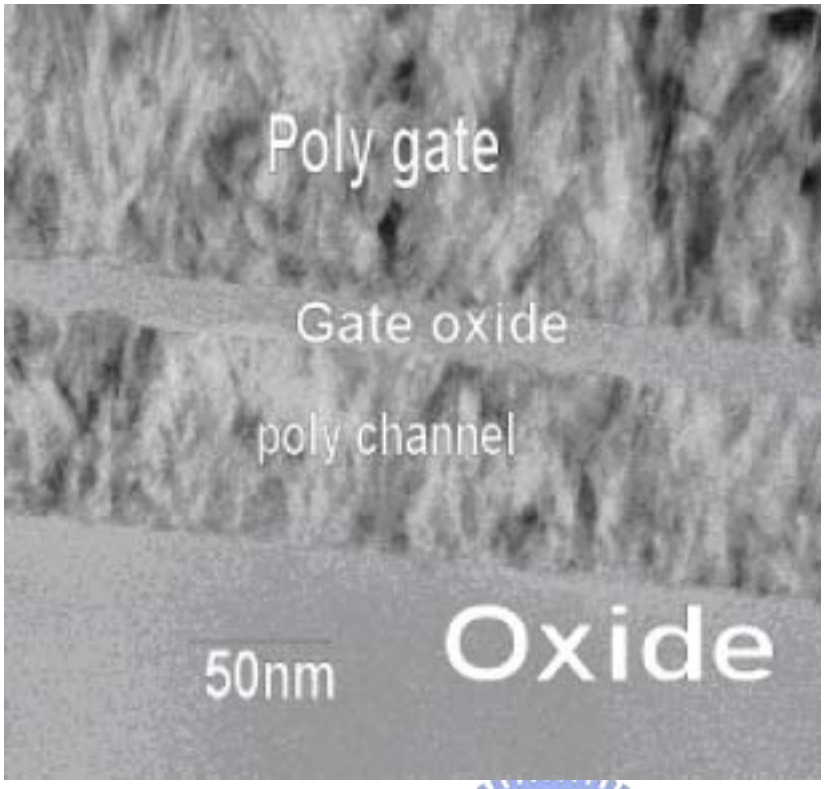
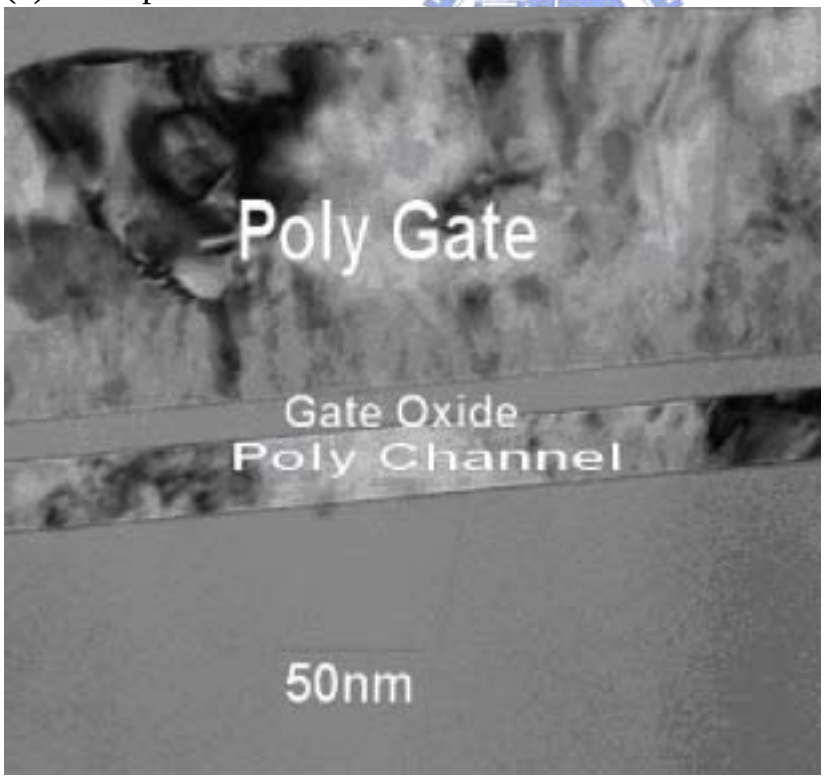


Fig. 6.22 Full-band gap DOS of devices with SPC and as-deposited poly-Si channels.



(a) As-deposited channel film



(b) SPC channel film

Fig. 6.23 TEM micrographs of devices with (a) as-deposited poly-Si, and (b) SPC channel films.

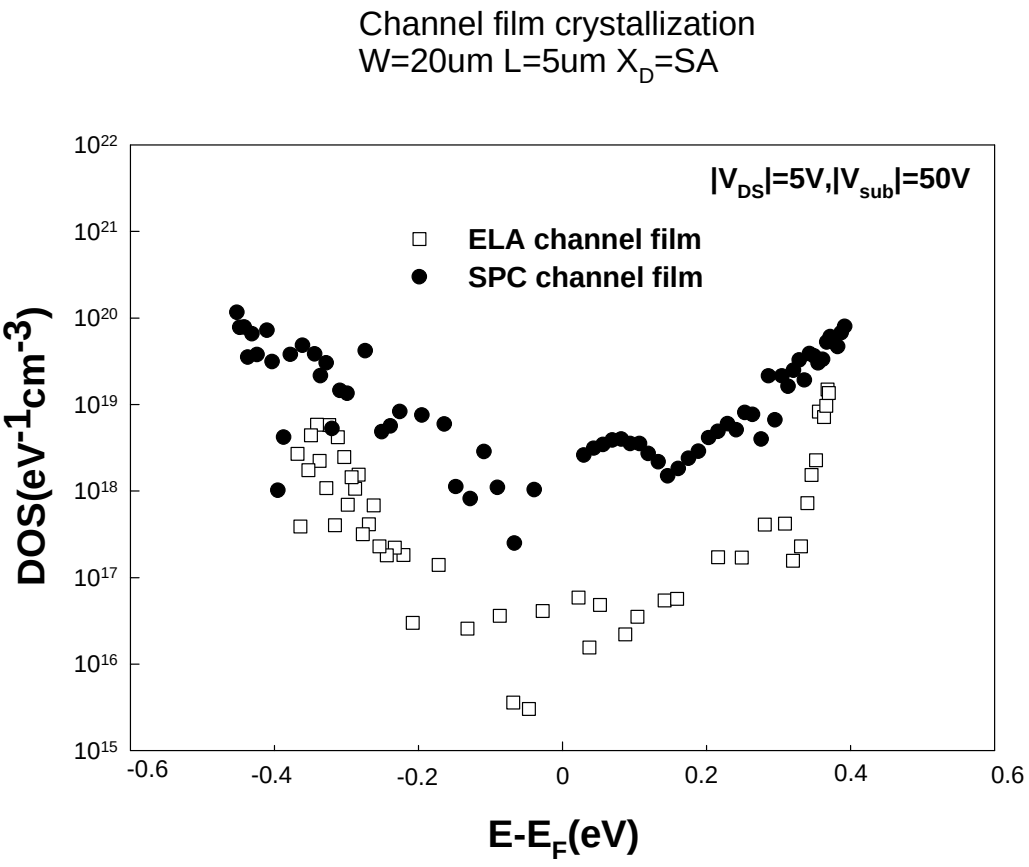


Fig. 6.24 Full-band gap DOS of devices with SPC and ELA poly-Si channels.

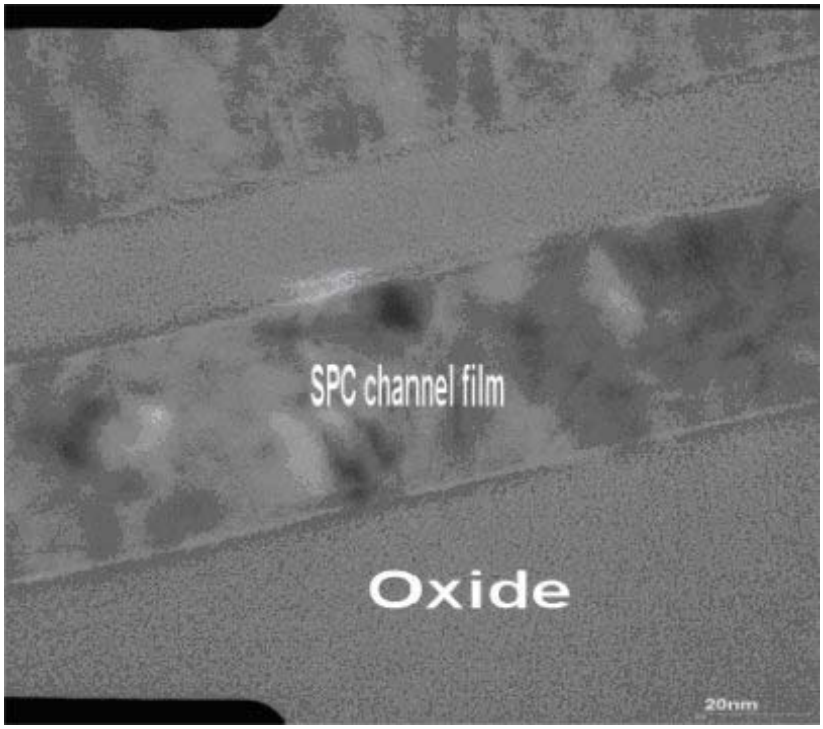
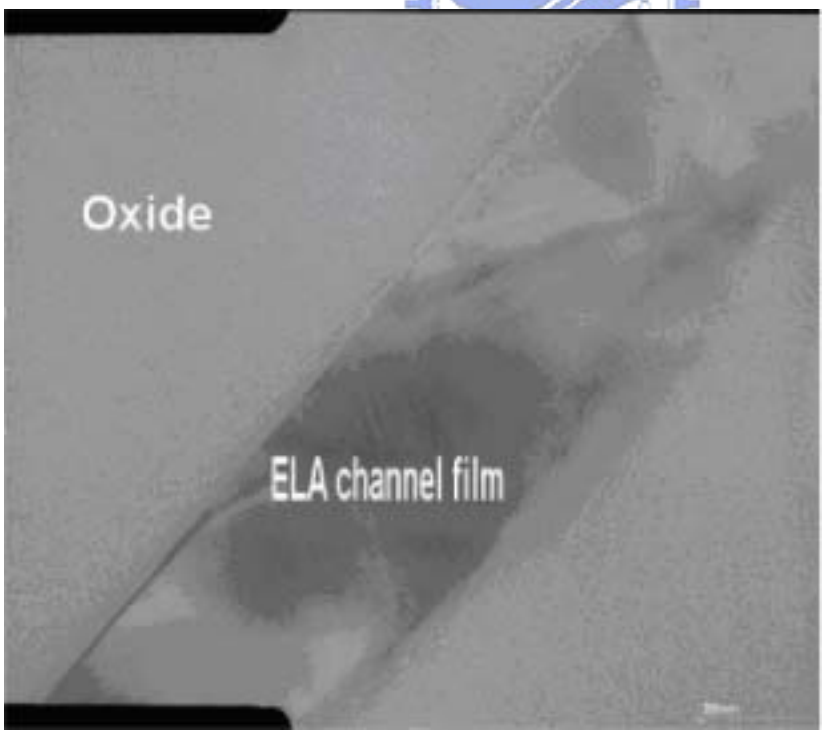


Fig. 6.25 **(a) TEM micrograph of SPC channel film.**



(b)

Fig. 6.25 **(b) TEM micrographs of ELA channel film.**

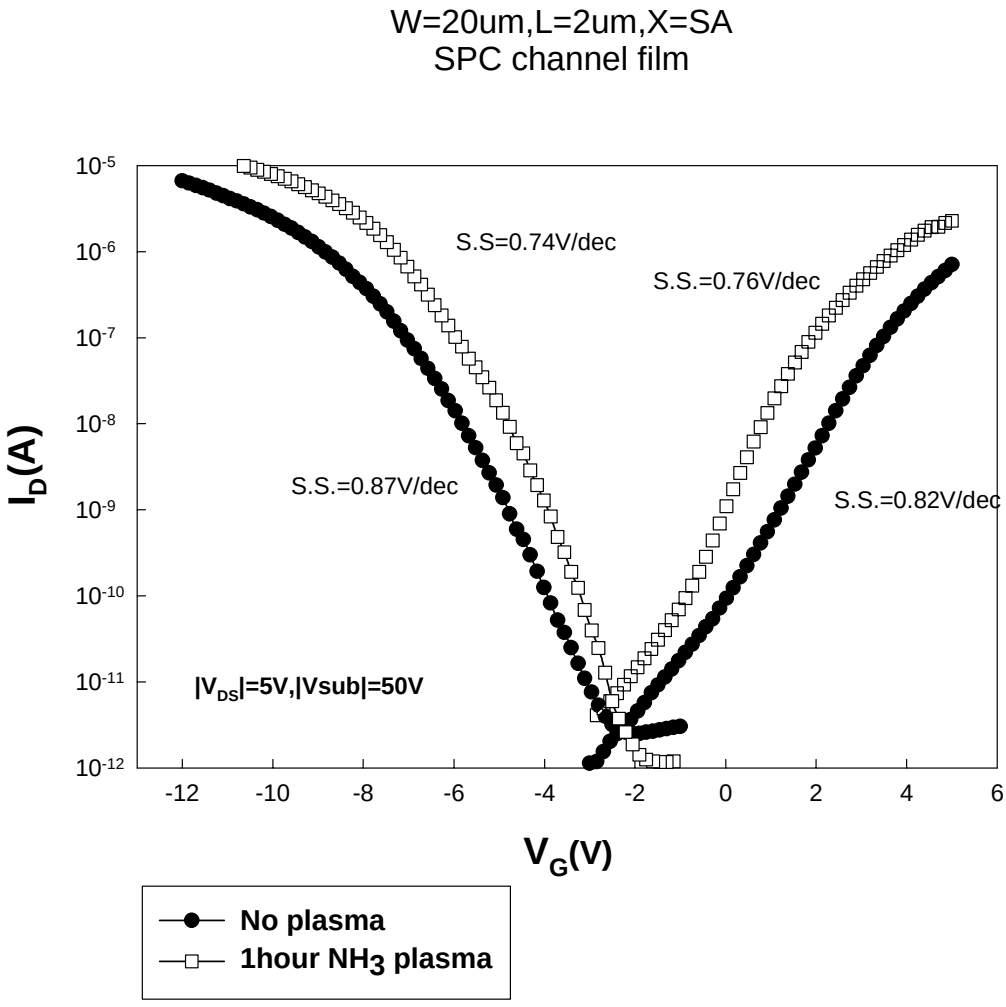


Fig. 6.26 Ambipolar transfer characteristics of devices with and without plasma treatment.

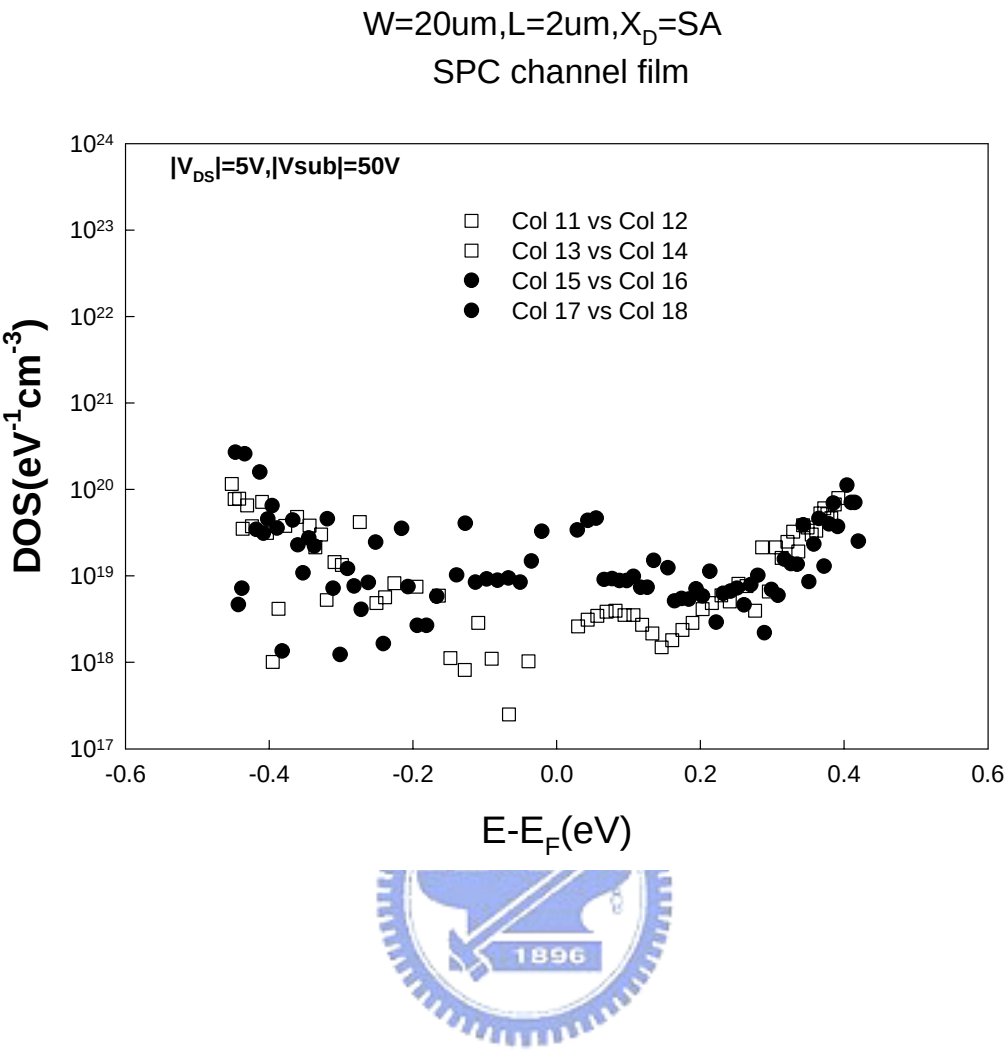


Fig. 6.27 Full-band gap DOS before and after hydrogenation in devices with SPC channel.

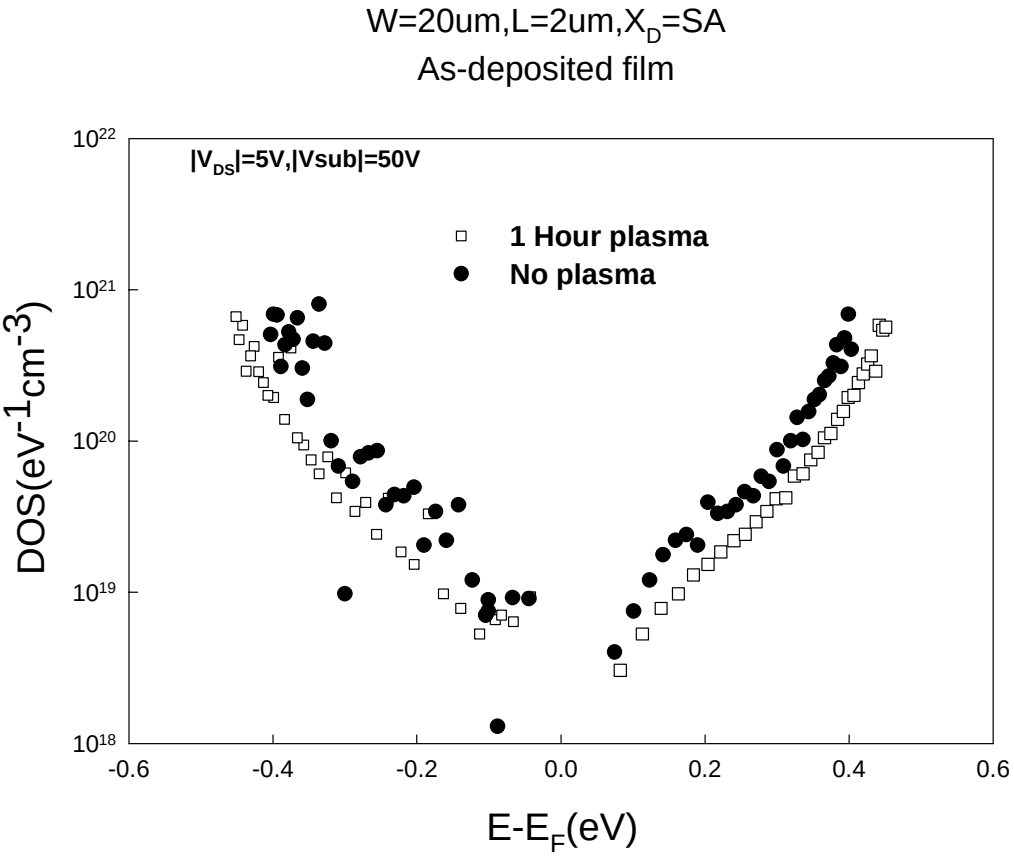


Fig. 6.28 Full-band DOS before and after hydrogenation in devices with as-deposited poly-Si channel.

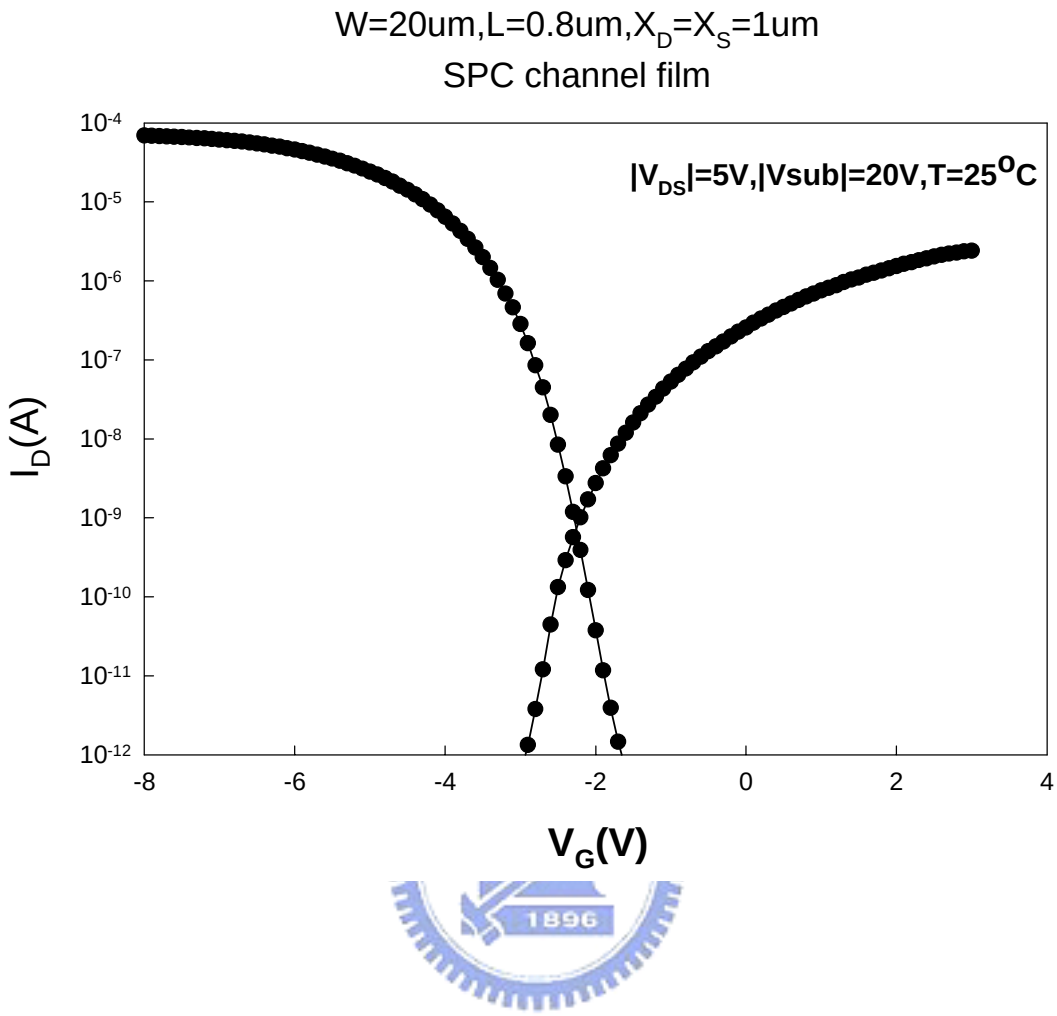


Fig. 6.29 **Ambipolar transfer characteristics of a device with PtSi S/D.**

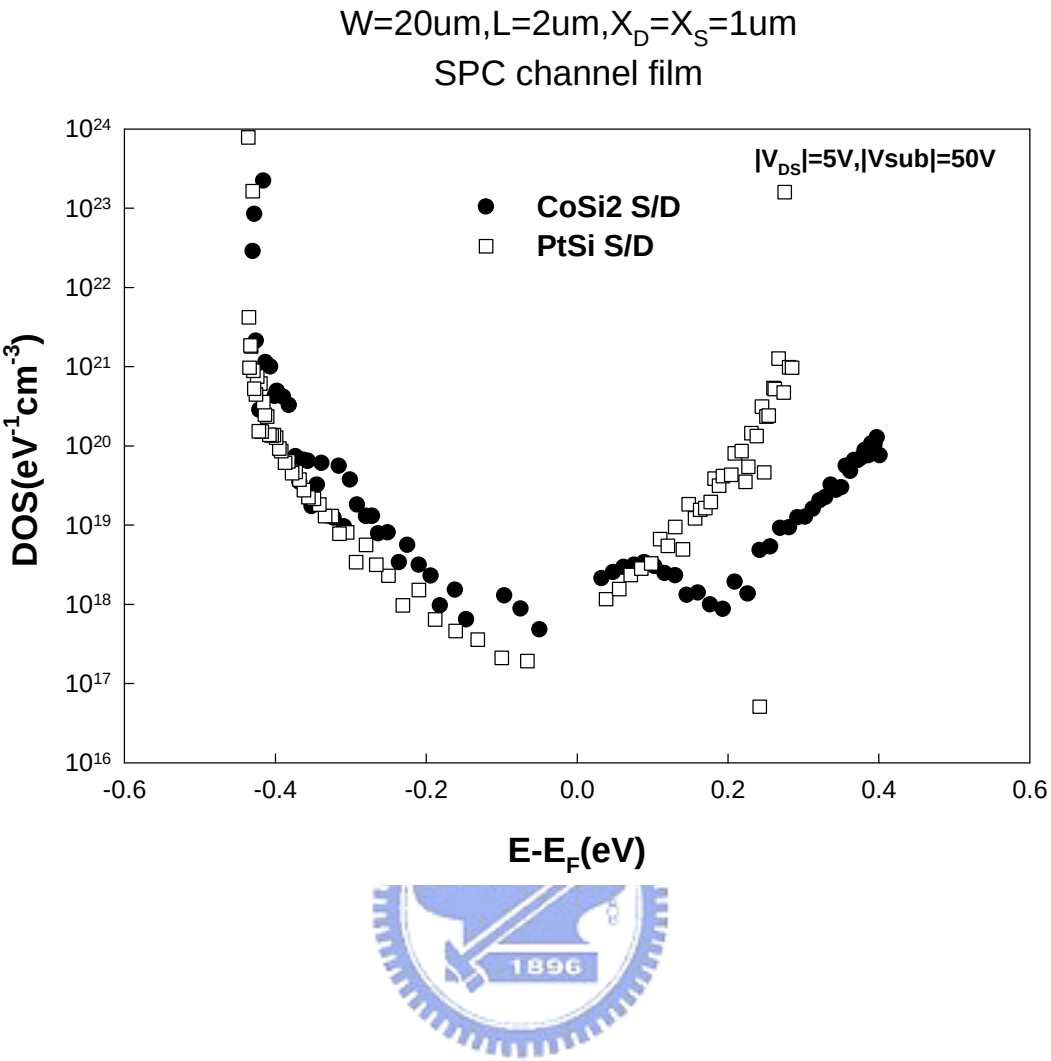


Fig. 6.30 Full band-gap DOS of devices with CoSi2 and PtSi S/D.

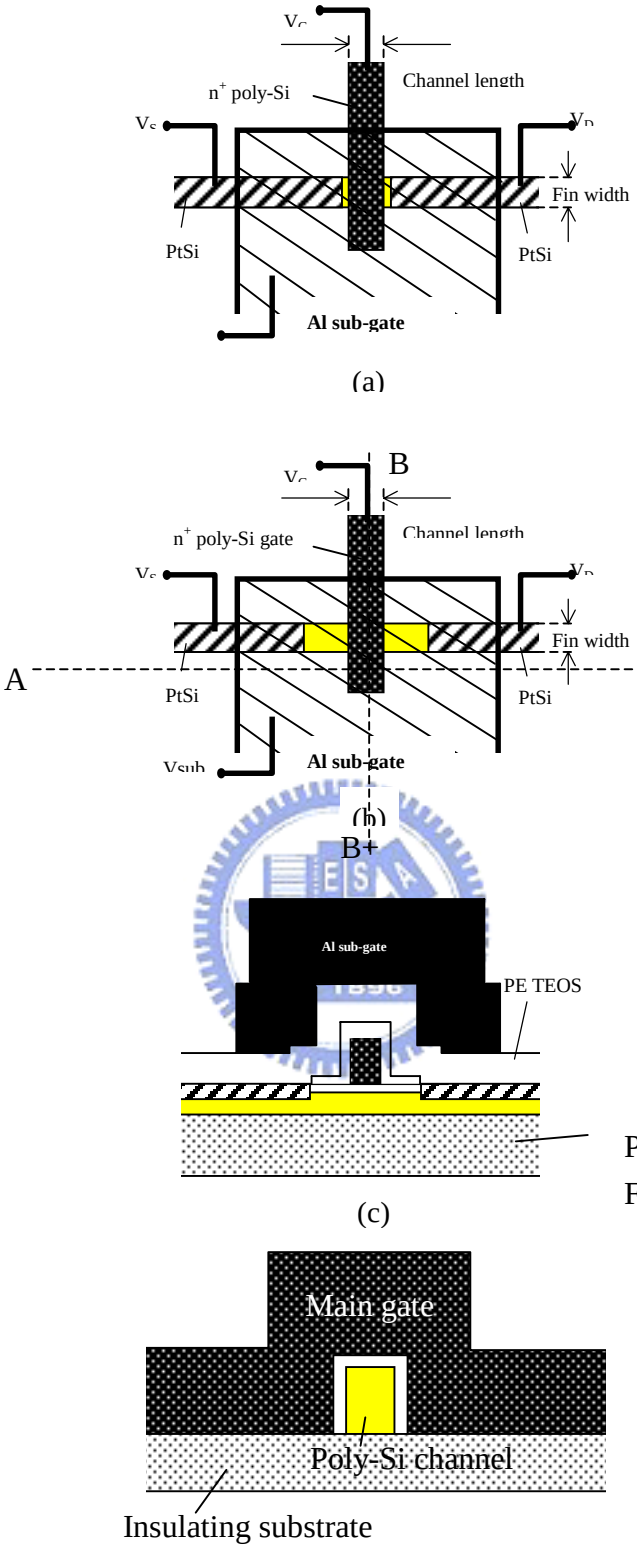


Fig. 6.31 (a) Top view of poly-Si SB FinFET with self-aligned spacer; (b) Top view of poly-Si SB FinFET with offset region X_D and X_S. (c) Cross-sectional view along A-A+ direction in (b); (d) Cross-sectional view along B-B+ direction in (b).

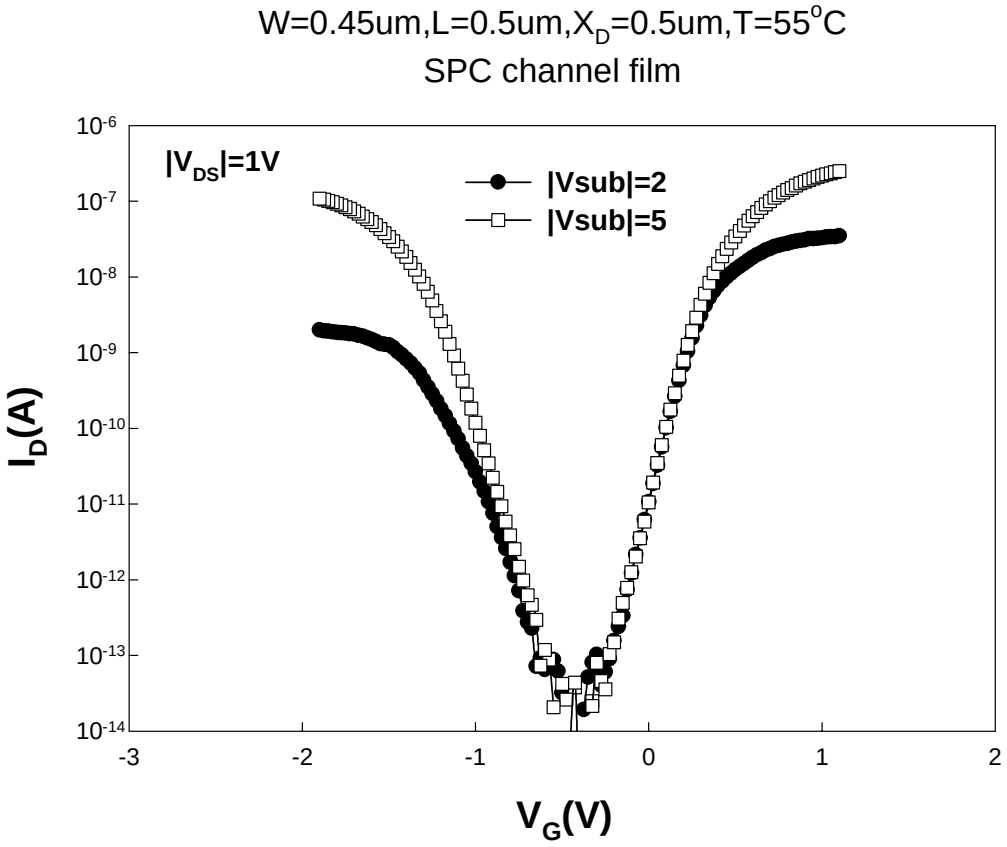


Fig. 6.32 Ambipolar transfer characteristics of SB poly-Si FinFET.

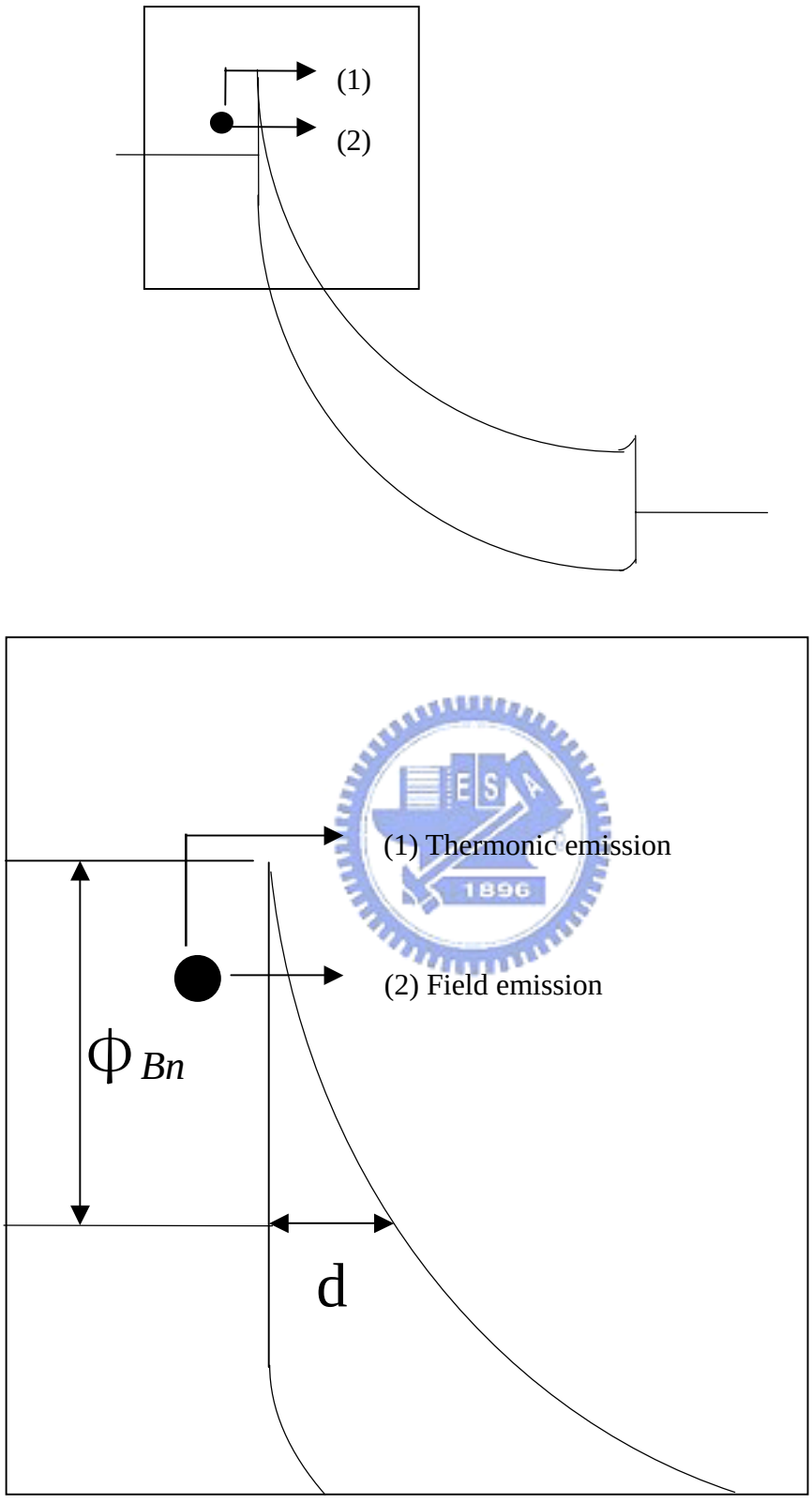


Fig. 6.33 Schematic showing that higher sub-gate bias enhances source-side field emission.

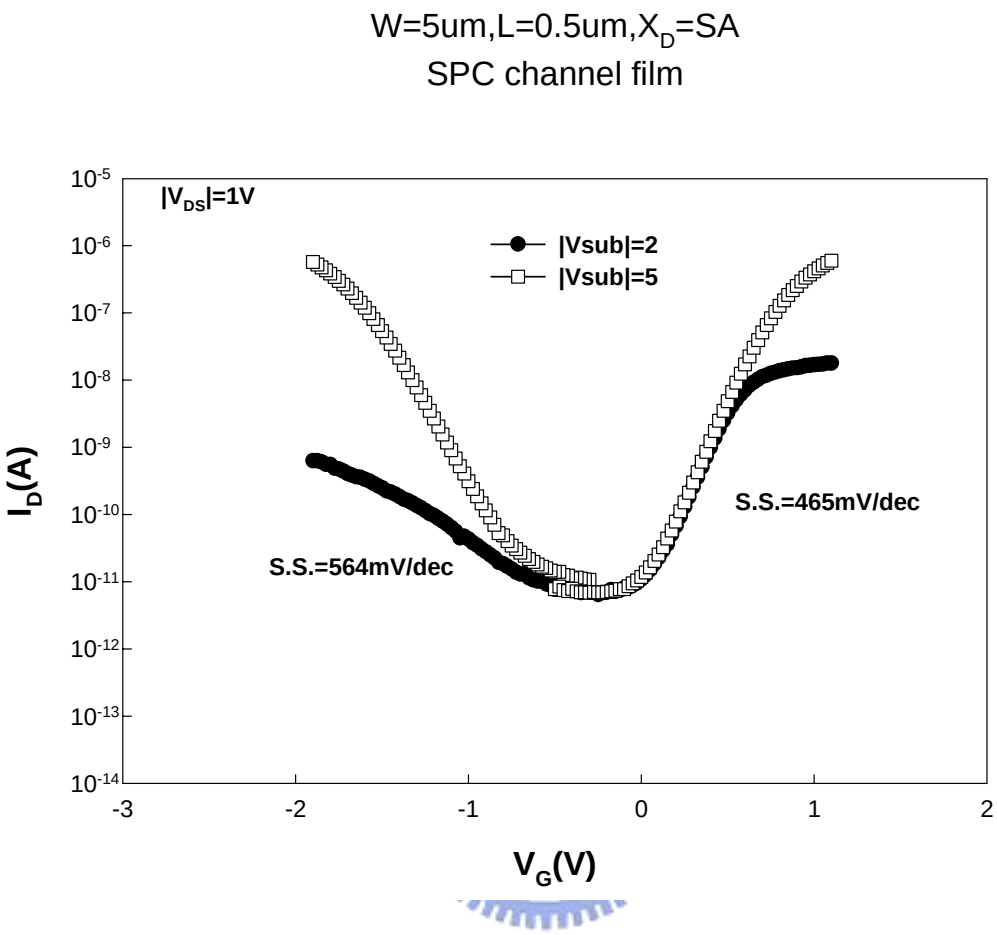


Fig. 6.34 Ambipolar transfer characteristics of SB poly-Si TFT with planar structure.

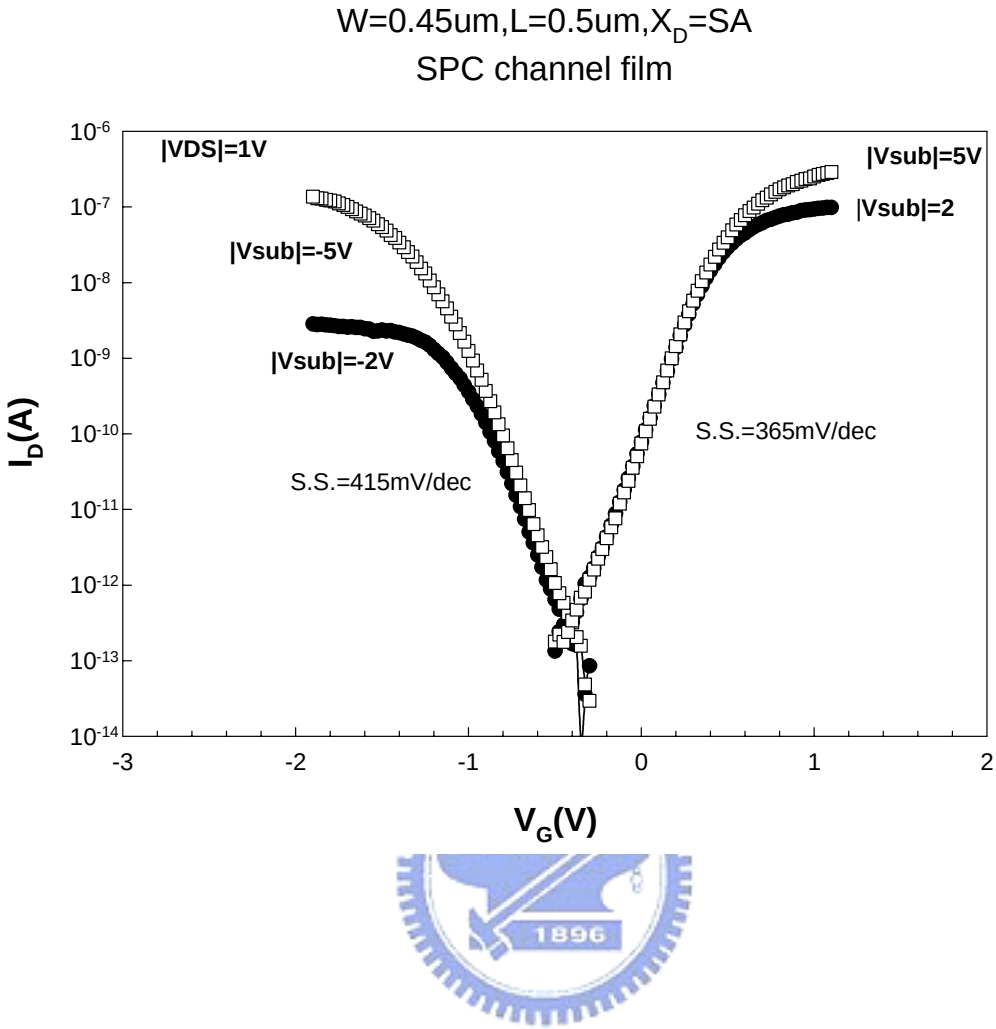
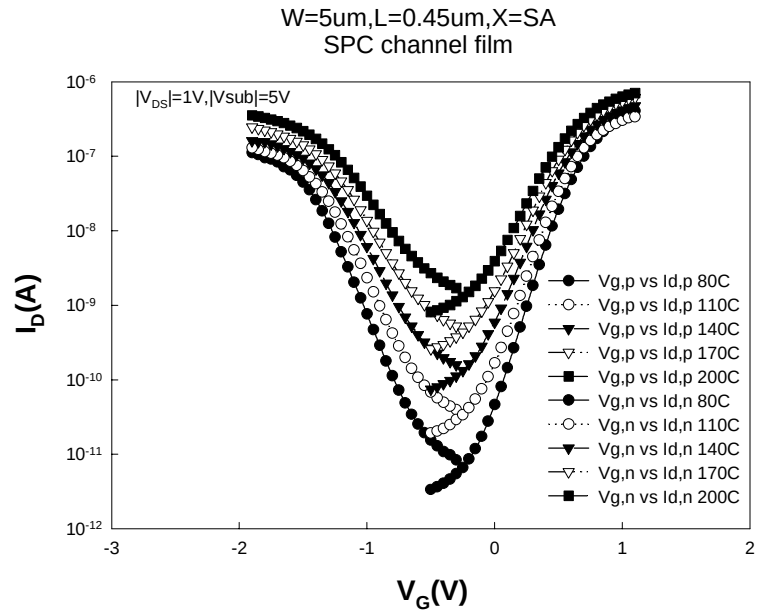
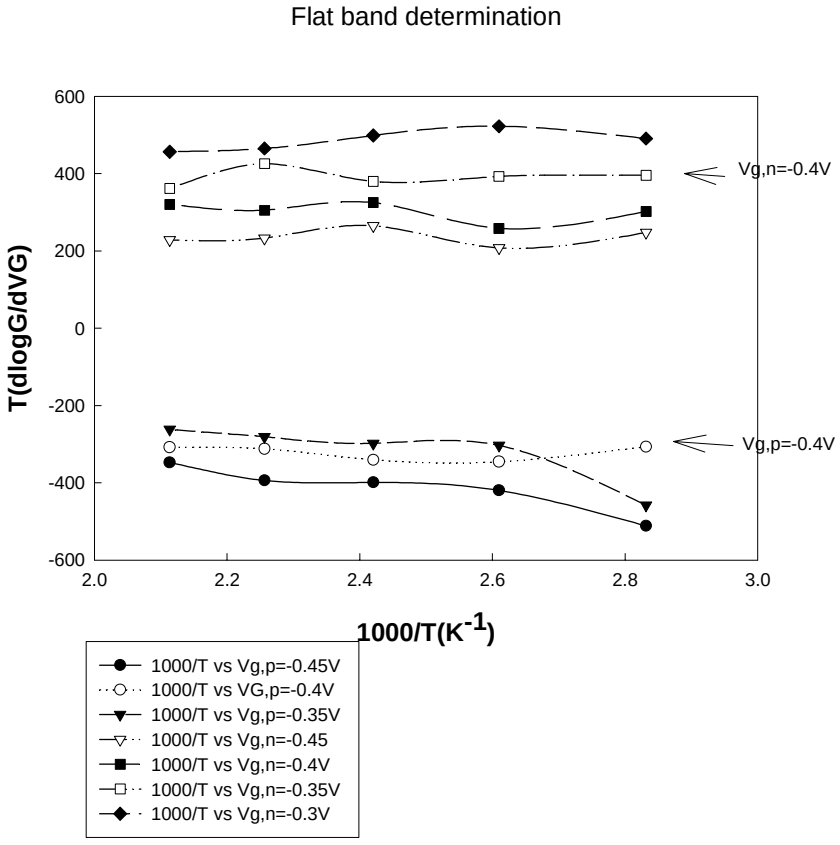


Fig. 6.35 Ambipolar transfer characteristics of SB poly-Si FinFET.



(a)



(b)

Fig. 6.36 (a) Ambipolar transfer characteristics of a SB poly-Si FinFET measured at varying temperature, (b) Flat band voltage determination.

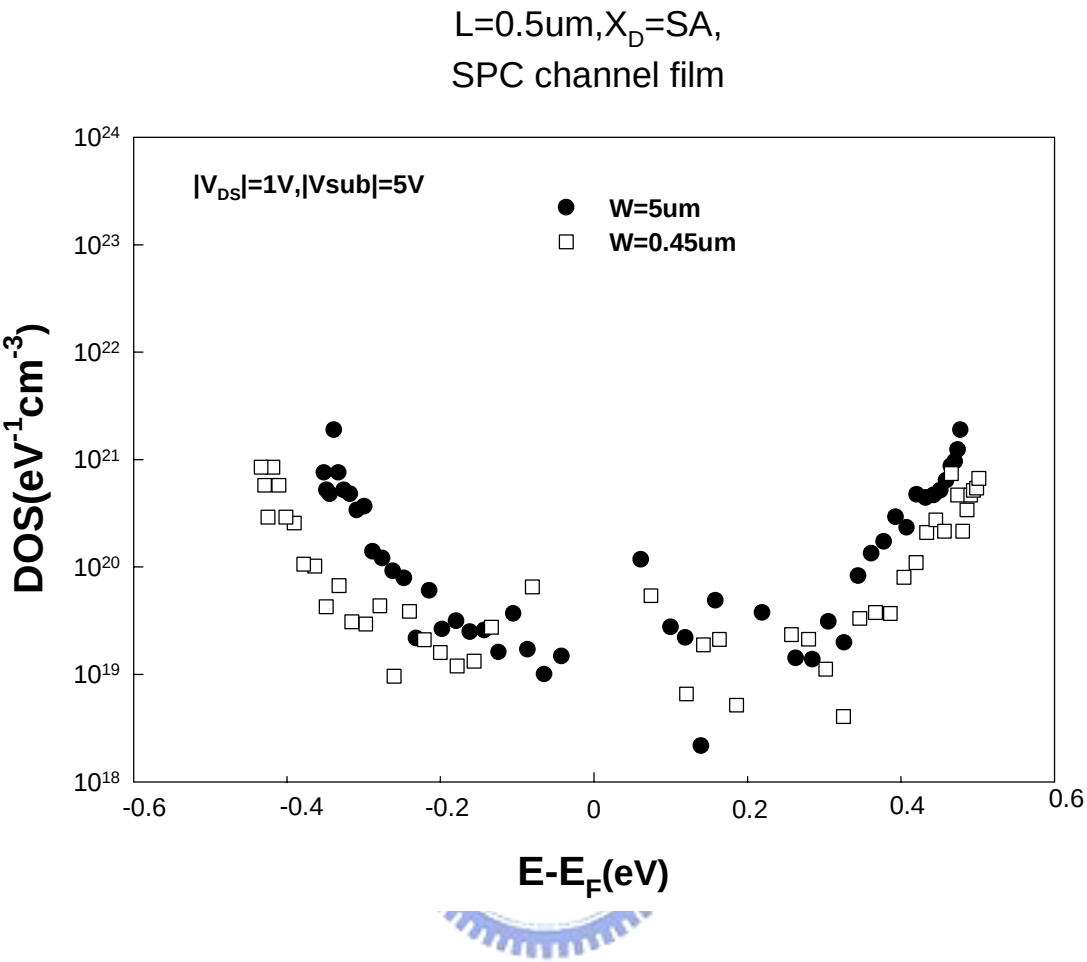


Fig. 6.37 Full-band gap DOS of planar SB -TFT and SB FinFET.

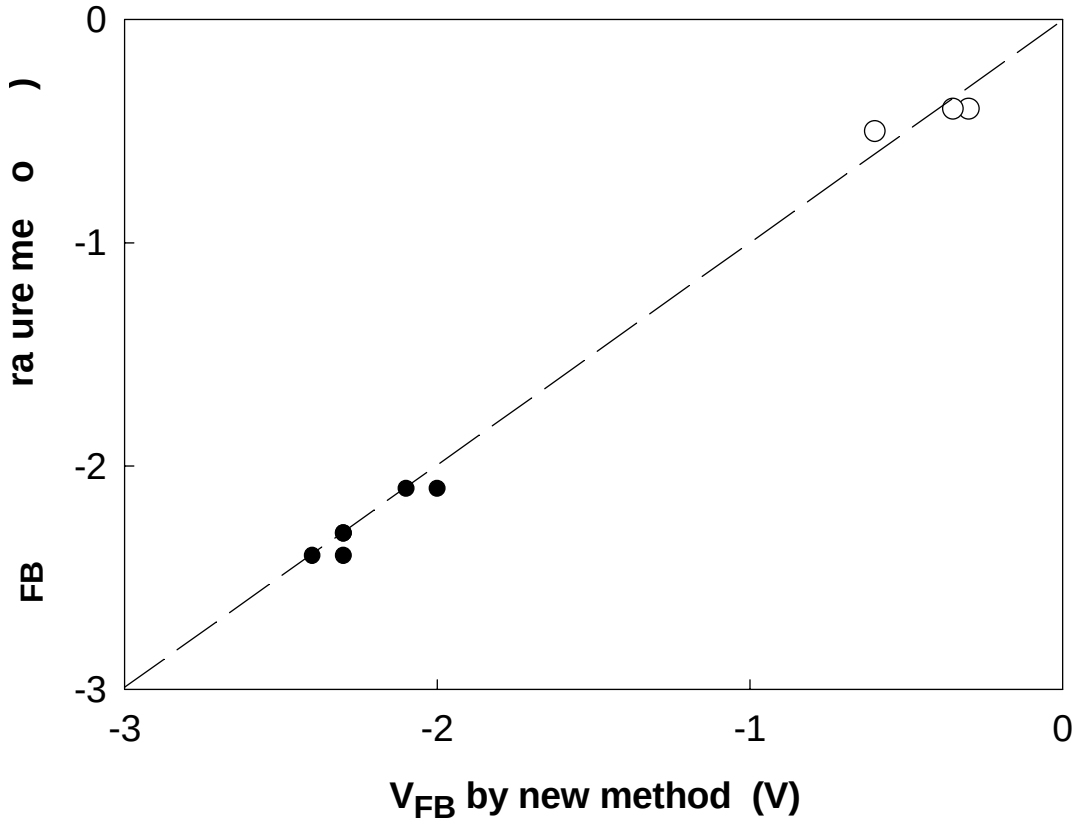


Fig. 6.38 **Comparison of V_{FB} values determined using conventional *temperature method* and the new methodology performed on two groups of devices with various parameters.**

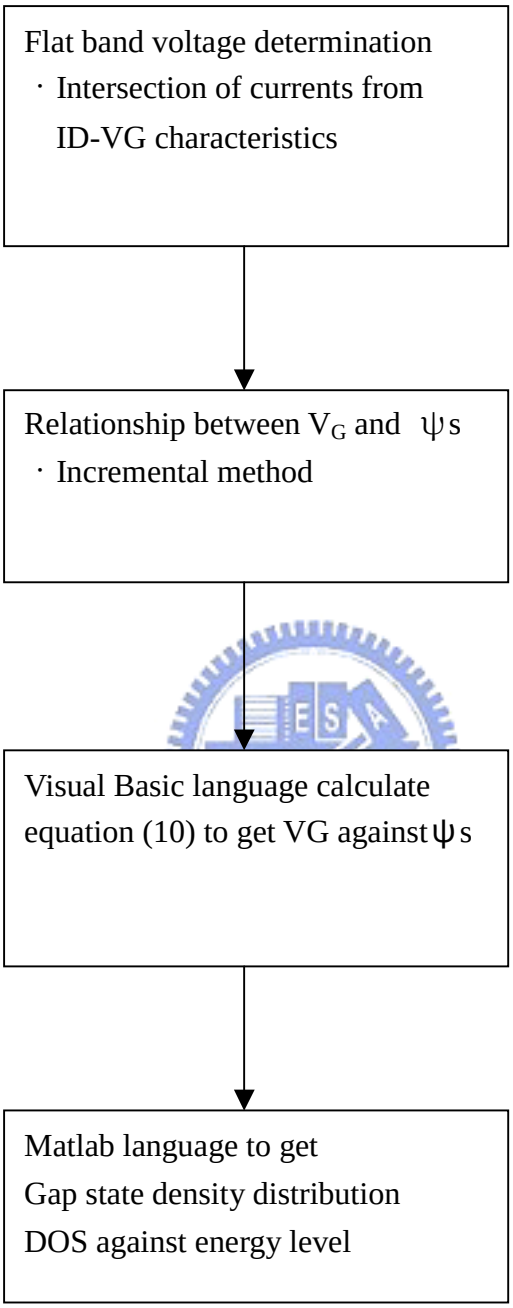


Fig. 6.39 Modified Flow chart for determination of DOS density distribution.

Chapter 7

Conclusions and Future Works

7.1 Conclusions

In this dissertation, we have fabricated and systematically studied Schottky Barrier poly-Si Thin-Film Transistors with FID. Device fabrication and ambipolar operation were first demonstrated. Then leakage conduction mechanisms were analyzed and identified. Our study was then extended to ELA channel preparation and nano width FinFET. Finally, we exploited the ambipolar characteristics of our FID SBTFT to analyze full band-gap density of states distribution in poly-channel films. Several important results were obtained and summarized as follows:

1. A novel Schottky barrier thin-film transistor (SBTFT) with silicided source/drain and field-induced drain (FID) extension was proposed and demonstrated. In the new device configuration, a metal field-plate (or sub-gate) lying on the passivation oxide is employed to induce a sheet of carriers in a channel offset region located between the silicided drain and the active channel region underneath the main-gate. The new device thus allows ambipolar device operation by simply switching the polarity of the bias applied to the field plate. In contrast to the conventional SBTFT that suffers from high GIDL (gate-induced drain leakage)-like off-state leakage current, the new SBTFT with FID is essentially free from the GIDL-like leakage current. In addition, unlike the conventional SBTFT that suffers from the low on/off current ratio, the new device exhibits high on/off current ratio of up to 10^6 for both *n*- and *p*-channel modes of operation. Moreover, the implantless feature and the ambipolar capability of the new device also result in extra low mask count for CMOS processes integration. These excellent device characteristics, coupled with its simple processing, make the new device very promising for future large-area electronic applications. We also found that the

channel region underneath the sub-gate has a lower Vth value and depicts much more severe short-channel effects for *n*-channel operation. These trends are ascribed to the positive fixed charges at the oxide/channel interface and the *n*-type background channel doping, the latter could be explained by the prior furnace history used in the SPC step of the device fabrication.

2. We have experimentally investigated the conduction mechanisms of the off-state leakage current for Schottky Barrier TFTs with FID and conventional structure. The results show that the activation energy of the off-state leakage decreases significantly with increasing $|V_{GD}|$ for SBTFT with conventional structure. This indicates that field-emission conduction plays a major role as the field strength in the drain junction becomes high, and results in the strong GIDL-like phenomenon. In contrast, the activation energy of the off-state leakage shows only minor dependence on V_{GD} for SBTFT with FID. This is ascribed to the fact that the high-field region could be pulled away from the silicided drain for the FID structure. As a result, the field-emission conduction will be eliminated, and thus the GIDL-like leakage current can be effectively suppressed.

3. SBTFT devices with ELA poly-Si active channel were successfully fabricated in this work. Excellent device performance in terms of steep subthreshold slope and high on/off current higher than 10^8 for both p- and n-channel operations are demonstrated, for the first time, on a single poly-Si TFT device. Source-side tunneling process is found to be important for device operation, especially for the n-channel operation that has a larger barrier height. The stellar performance with on/off current ratio larger than 10^8 for both n- and p-channel modes of operation, together with its inherent ambipolar capability, implantless process, silicided source/drain, low thermal budget, and simplified CMOS integration scheme, makes this kind of device a promising candidate for future AMLCDs and SOP applications.

4. We have shown that the ambipolar performance of SB poly-Si TFTs can be improved by scaling the channel width into the nano-scale regime. Our results indicate that, despite the high trap density in poly-Si films, high on/off current ratio and small subthrehold swing can be achieved. It appears therefore possible to achieve SOI-like device characteristics if poly-Si film improvement methods, such as excimer laser annealing and metal-induced crystallization scheme, are adopted.

5. We have proposed and successfully demonstrated a novel approach to obtain the full band-gap DOS in the channel of TFT devices. In this approach, the field-effect conductance method is performed on an SB poily-Si TFT which has the capability of ambipolar operation. Both incremental and temperature methods are adopted on the SB and conventional devices to construct the relationship between DOS and the energy level in the gap. For devices with the same channel material, the results are in good agreement among the different extraction schemes, indicating the novel approach is very reliable.

We have also characterized the dependence of both electrical and structural parameters on the measurement results in order to set suitable test conditions. Our results indicate that the parasitic resistance presenting in the channel would result in overestimation of tail state density. A sufficiently high drain and sub-gate biases and short electrical junction length are thus needed. In addition, for reliable full band-gap DOS analysis, near-mid-gap silicide material like $CoSi_2$ is desirable.

We have also characterized the effect of process treatment like the re-crystallization and plasma hydrogenation steps on the DOS characteristics. Their impacts could be clearly identified using the new approach. Benefits of using a nano-scale fin channel for promotion of the controllability of gate voltage over the channel potential is also clearly demonstrated.

Finally, we show that the flat-band voltage could be obtained by simply measuring the gate voltage at the intersection point of p- and n-mode I-V curves. The overall process is thus greatly simplified and cost-saving comparing to conventional approach, since only one device and two I-V measurements performed at room temperature are needed. We strongly believe that the novel method is extremely useful for practical applications.

7.2 Future Works

There are some interesting and important topics that are valuable for the future research about the Schottky Barrier Thin Film Transistors:

1. In Chapter 2, future research is suggested on building a current transport model of Schottky Barrier Thin Film Transistor with FID. It is also suggested to study other metal siliside materials with low barrier (e.g. ErSi and PtSi used for n- and p-channel operations, respectively) to improve the output performance. The optimization of fabrication should also be studied.

2. In Chapter 3, we should further investigate the leakage current model, and computer simulation is need.

3. The on-state and off-state conduction mechanisms for FID SBTFT with ELA poly-Si channel have been identified in this thesis, future research is suggested on study of the interface defects distribution between channel and metallic silicide.

The results shown in Sec. 4.3 indicated that the devices with shorter offset channel exhibit better performance. Nevertheless, the shortest offset channel explored in this work is 1 μm. More investigation on devices with offset length shorter than 1 μm is thus needed in ordre to optimize the device performance.

It is also possible to realize fully implantless CMOSFET circuits by employing the metal gate process in the fabrication of the FID SBTFT. The use of metal gate process would further reduce the processing temperature. By choosing gate material with appropriate metal work function, symmetric threshold voltages for p- and n-channel operations could be obtained, and thus makes the devices more suitable for CMOS applications

4. In Chapter 5, it is important to focus on the topics of improved FinFET layout and material change. Continuous scaling of the fin width and gate oxide thickness is essential to enhance the SCE immunity, and should be an interesting future research topic. However, the integrity of thin gate oxide is an important issue of reliability. Special care must be taken when the under layer is poly-silicon, for the surface roughness may degrade the long time reliability. In addition, decreasing the S/D series resistance by shortening the S/D contact distance is helpful to increase the on-current, and should be investigated. Finally, it is interesting to fabricate SiGe channel FinFET with Pt-silicided S/D to further reduce the Schottky barrier of the p-channel device, to see if the output performance of such Schottky FinFET could match that of the conventional implanted S/D poly-Si devices.

5. In Chapter 6, since our method provides a simple and efficient way to map the full band-gap density of states of the channel material, it will be a very powerful tool in the development and production of thin film transistors. We believe our method could be applied to TFT technologies using poly-SiGe or organic channel materials. The method would provide an efficient and powerful tool in understanding the impact of process treatment on the device characteristics and on addressing some material issues such as the impurity contamination and segregation in the channel. With specially designed test structures, the method may also be useful to characterizing the reliability issues of TFT devices such as the hot-carrier induced damage effect.