Short Papers

Efficient Physical Timing Models for CMOS AND-OR-Inverter and OR-AND-Inverter Gates and Their Applications

CHUNG-YU WU AND MING-CHUEN SHIAU

Abstract—**Efficient physical timing models for complex CMOS AND-OR-Inverter (AOI) and OR-AND-Inverter (OAI) gates have been successfully developed. Through extensive comparisons with SPICE simulation results, the developed models have shown a maximum error of 30% for long-channel and small-geometry CMOS AOI/OAI gates with wide ranges of channel dimensions, capacitive loads, logic input patterns, circuit configurations, device parameter variations, and noncharacteristic waveform input excitations. The error can be further reduced to 16% with commonly used device dimensions. The developed timing models are successfully applied to the autosizing of CMOS AOI/OAI gates. The results show a good accuracy and a reasonable CPU time consumption.**

NOMENCLATURE

B	Mobility correction factor (SPICE device parameter).
$C_{bdn(p)}$	Bulk-drain p-n junction capacitance of an n-channel (p-channel) MOSFET.
$C_{bsn(p)}$	Bulk-source p-n junction capacitance of an n-channel (p-channel) MOSFET.
$C_{gbn(p)}$	Gate-bulk capacitance of an n-channel (p-channel) MOSFET.
$C_{gdn(p)}$	Gate-drain capacitance of an n-channel (p-channel) MOSFET.
$C_{gsn(p)}$	Gate-source capacitance of an n-channel (p-channel) MOSFET.
DELTA	Narrow-channel width factor (SPICE device parameter).
GAMMA	Bulk threshold parameter in SPICE, which represents the proportionality factor relating the change in threshold voltage to backgate bias.
$I_{dn(p)}$	Linearized drain current of an n-channel (p-channel) MOSFET in the large-signal equivalent circuit.
I_{DS}	DC drain current of a MOSFET.
L	Effective channel length of a MOSFET.
L_{mask}	Mask channel length of a MOSFET.
N	Fan-out number of a gate.
NSUB	Substrate doping concentration (SPICE device parameter).
T_{OX}	Oxide thickness (SPICE device parameter).
UCRIT	Critical field for mobility degradation due to normal field (SPICE device parameter).
UEXP	Critical field exponent for mobility degradation due to normal field (SPICE device parameter).
UO	Surface mobility at low gate voltage and large device size (SPICE device parameters).
UTRA	Mobility degradation factor due to lateral field (SPICE device parameter).
V_{oj}	Large-signal voltage at the internal node j of a logic gate.
$V_{BS(D)}$	Bulk-source (drain) voltage of a MOSFET.
V_{DD}	Power supply voltage.
$V_{DS(GS)}$	Drain-source (gate-source) voltage of a MOSFET.
V_T	Threshold voltage of a MOSFET under substrate bias.
V_{TO}	Zero-bias threshold voltage of a MOSFET.
W	Effective channel width of a MOSFET.
XJ	Metallurgical junction depth (SPICE device parameter).
$\epsilon_{SI(SIO_2)}$	Permittivity of S_i semiconductor (silicon dioxide).
$\mu_{n(p)}$	Electron (hole) surface mobility.
ϕ_F	Fermi potential.

Manuscript received February 13, 1987; revised September 4, 1987, February 15, 1988, and August 17, 1989. This paper was recommended by Editor M. R. Lightner.

The authors are with the Institute of Electronics and the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, China.

IEEE Log Number 9035468.

I. INTRODUCTION

Efficient timing models or macromodels of MOS logic gates [1]–[22] have shown many advantageous features in the design of MOS digital IC's. They can be applied to timing analysis and verification of MOS circuits [4]–[11], [18]–[20] as well as circuit optimization and autosizing [12]–[17], [21], [22]. Furthermore, all these models have reasonable accuracy and consume little computer memory and CPU time. They can also provide a deep insight into the speed nature of digital MOS IC's.

Although CMOS has become a dominant technology in digital VLSI/ULSI [23], only a few timing models have so far been proposed [5]–[7], [14]–[17], [19]–[22]. Among them, the use of the step-response models [14] does not guarantee the required accuracy due to the neglect of the strong influence of input signals on delay times [16].

There are two approaches to cope with the input waveshape effects [17]. One is table driven techniques like Crystal [5]. Crystal is a timing simulator in which transistor resistances can be adjusted according to the input waveforms and device operating regions to obtain a higher accuracy. This approach, however, has been proven to have some limitations [17]. These limitations are, for example, the accuracy problem due to resistance extractions for the gates with different beta ratios, sizes, etc., the problem due to the table interpolations, and the difficulties in optimizations. The other approach is entirely based on device equations. In this approach, the resistance extractions are not required and the table interpolation problem can be avoided. Moreover, this approach is quite suitable for optimization and autosizing. For efficient design automation and optimization, good analytical delay macromodels [6], [7], [16]–[22] entirely based on device equations are required [17].

Generally, accurate and efficient timing models entirely based on device equations are very useful in various CAD applications in VLSI, such as timing verification, optimization, logic simulation, and autosizing [17].

So far, the timing models for inverters, NAND and NOR gates [5]–[7], [14]–[16], [19]–[22] have been developed. However, the timing models for AND-OR-Inverter (AOI) and OR-AND-Inverter (OAI) gates, which are commonly used in the design of CMOS digital IC's, have not yet been reported. Due to their complicated structures, the computer time consumed in the simulation of the circuits containing those gates is very long. The efficient timing models of those CMOS gates, therefore, are more urgently required than those of other simple combinational logic gates.

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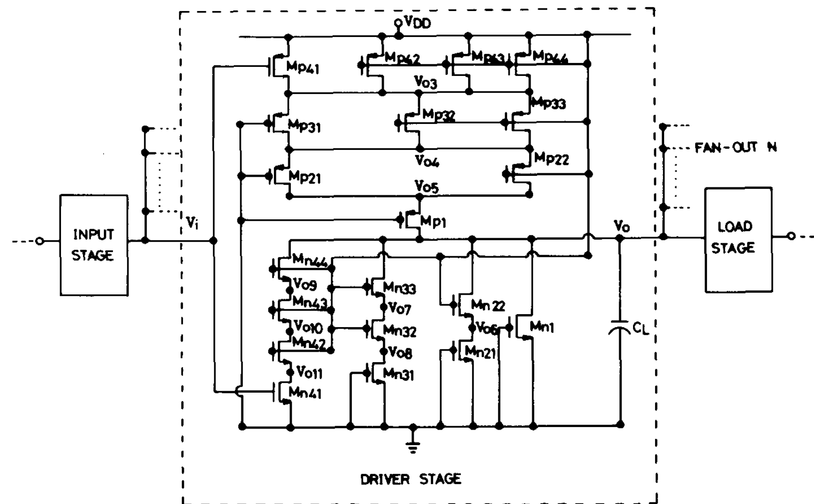

Fig. 1. A chain of identical CMOS 4-3-2-1-input AOI gates under the worst-case timing condition.

It is the aim of this paper to develop efficient physical timing models for CMOS AOI/OAI gates with wide ranges of channel dimensions, capacitive loads, circuit configurations, input excitations, and device parameters. As compared to the SPICE [24] simulation results, the maximum error of model calculation results is 30% within a large applicable range. Fine tuning within a special range can reduce the error to 16%. By using the developed models, the signal timing of the commonly used CMOS AOI/OAI gates with less than 4 PMOSFET's or 4 NMOSFET's in series can be quickly computed. Moreover, autosizing of CMOS AOI/OAI gates can be performed through the use of the timing models.

The model formulations are described in Section II. Comparisons between model calculations and SPICE simulations are given in Section III. An application example of the developed models in autosizing is given in Section IV. Finally, conclusions are made.

II. Timing Models

As an illustrative example for model formulations, a 3.5-μm CMOS 4-3-2-1-input AOI gate under a worst-case timing condition is considered. The AOI gate circuit is shown in Fig. 1 where the input voltage V_i drives the MOSFET's M_{p41} and M_{n41}. It is known that after the signal passes through several stages, the rising or the falling waveforms at the output node of a stage gradually become the same, being independent of input excitations. Such waveforms are named characteristic waveforms [16]. The typical characteristic waveforms obtained from the SPICE simulations for the falling input voltage V_i are plotted in Fig. 2. As the name of characteristic waveforms implies [16], the waveforms of the AOI gate in 1.5-μm CMOS technology are very similar to those of Fig. 2. As shown in the figure, the output voltage V_o has a rising waveform with the characteristic rise time T_R defined as the time interval between $V_o = 0.1V_{DD}$ and $V_o = 0.9V_{DD}$. The rise delay time T_{PLH} for the output voltage V_o and the initial delay time t_{drj} for any output voltage V_{oj} are also indicated in Fig. 2.

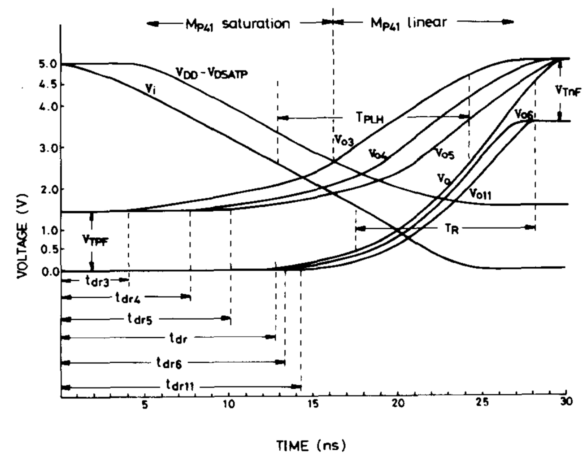

Fig. 2. Typical rise characteristic waveforms of a CMOS 4-3-2-1-input AOI gate.

During the rise time period T_R, the operating region of each MOSFET can be determined from its drain-source voltage V_{DS} and drain-source saturation voltage V_{DSAT} generated from its corresponding gate-source voltage V_{GS} and drain-source voltage V_{DS}. From the simulated curves in Fig. 2, it is found that the MOSFET's M_{p31}, M_{p21}, M_{p1}, M_{n44}, M_{n43}, M_{n42}, M_{n33}, M_{n32}, and M_{n22} in the series branches of the driver stage are mostly operated in the linear region during T_R. This is because they all have a smaller V_{DS} during T_R. The driven PMOSFET M_{p41} has a gate-source voltage $V_i - V_{DD}$ and a drain-source voltage $V_{o3} - V_{DD}$. The trajectory of $V_{DD} - V_{DSATP}$ has an intersection point with the curve of V_{o3} as shown in Fig. 2. According to our observations, this intersection point is located outside the rise time region for typical AOI gates even when the device channel length is down to 1.5 μm. This means that during T_R the drain-source voltage $|V_{DD} - V_{o3}| = |V_{DS}|$ is always smaller than V_{DSATP} in the PMOSFET M_{p41}. Thus it is operated in the linear region during T_R and in those complex AOI gates only the linear-region current is involved in deriving the formula of T_R. This is true for AOI/OAI gates with long-channel and small-geometry MOSFET's.

Under the similar considerations, the PMOSFET M_{p41} of the load stage is mostly in the linear region during T_R whereas the NMOSFET M_{n41} of the load stage is mostly in the saturation region. Both devices in the load stage are treated as a capacitive load and their capacitances are calculated according to their operating regions.

From the determined operating region and the large-signal equivalent circuit of each MOSFET, the overall large-signal equivalent circuit of the 4-3-2-1-input AOI gate during the characteristic rise time T_R can be built as shown in Fig. 3 where the load stage

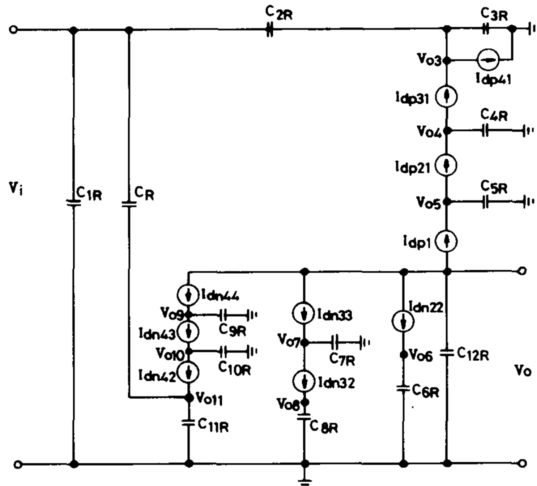

Fig. 3. Large-signal equivalent circuit of a CMOS 4-3-2-1-input AOI gate during the rise time period.

is effectively represented by a capacitive load to the driver stage. Both the capacitive load and the fixed capacitor C_L are included in the capacitance C_{12R}.

The expressions of all the capacitances in the equivalent circuit are listed in Table I where the device capacitances C_{gd}, C_{gs}, and C_{gb} can be approximated by appropriate constant values [25] according to the operating region of the associated MOSFET. The voltage-dependent p-n junction reverse-bias capacitances C_{bd} and C_{bs} can also be approximated by their constant values calculated from the same formulas in SPICE [24] at the linearization point. The linearization point in this case is optimally determined at the center point with $t = t_e$ where $V_o(t_e) = V_{DD}/2$. All the other node voltages at the point can be found from the characteristic waveforms. After the above cited linearization procedure, all the capacitances listed in Table I become linear and have fixed values. Since the p-n junction reverse-bias capacitance is not a strong function (e.g., exponential function) of voltage, the linearization leads to a limited error.

The linear-region drain current used in the modified SPICE program is expressed in Table II. By applying the same technique [6], the voltage-dependent mobility and the nonlinear terms in the current expression can be linearized. The resultant expressions of the linearized drain currents in the equivalent circuit of Fig. 3 are listed in Table III. Note that the drain currents in the equivalent circuit are those of the linear region, the linearization thus does not lead to an unbearable error. With the linearized capacitances and drain currents, the equivalent circuit of Fig. 3 becomes a linear circuit.

Since the internal characteristic waveform in a digital circuit strongly depends upon the circuit structure rather than the input excitation, it can be well characterized by the poles and zeros of the corresponding equivalent circuit. In complicated circuits like CMOS AOI/OAI gates, they tend to have a dominant pole. Thus the signal timing can be analytically modeled from the dominant pole only. Dominant-pole calculation in the S domain, however, is too tedious in a complex logic gate. In this paper, the zero value time constant method [26] will be applied to simplify the dominant-pole calculation while obtaining a satisfactory result.

To compute the dominant pole of the equivalent circuit in Fig. 3, the input port is short circuited. Thus the output resistance looking into each capacitor with all others taken away can be found. The expressions of all the output resistances are given in Table IV. From these expressions, it can be seen that the effective resistances of each MOSFET, for example, M_{p31}, in the associated output resistance expressions, for example, R_{4R}, R_{5R}, and R_{12R}, are different.

TABLE I
THE EXPRESSIONS OF THE CAPACITANCES IN THE EQUIVALENT CIRCUIT USED FOR THE CHARACTERISTIC RISE TIME CALCULATION OF A CMOS 4-3-2-1-INPUT AOI GATE

$C_{1R} = C_{gsp41} + C_{gsn41} + C_{gbn41}$

$C_{2R} = C_{gdp41}$

$C_{3R} = C_{gdp42} + C_{bdp42} + C_{gdp43} + C_{bdp43} + C_{gdp44} + C_{bdp44} + C_{bdp41} + C_{gsp31} + C_{bsp31} + C_{gsp32} + C_{bsp32} + C_{gsp33} + C_{bsp33}$

$C_{4R} = C_{gdp31} + C_{bdp31} + C_{gdp32} + C_{bdp32} + C_{gdp33} + C_{bdp33} + C_{gsp21} + C_{bsp21} + C_{gsp22} + C_{bsp22}$

$C_{5R} = C_{gdp21} + C_{bdp21} + C_{gdp22} + C_{bdp22} + C_{gsp1} + C_{bsp1}$

$C_{12R} = C_{gdp1} + C_{bdp1} + C_{gdn44} + C_{bdn44} + C_{gdn33} + C_{bdn33} + C_{gdn22} + C_{bdn22} + C_{gdn1} + C_{bdn1} + N \cdot NSL_R + C_L$

$NSL_R = C_{gsp41} + C_{gdp41} + C_{gdn41} + C_{gsn41}$

$C_{6R} = C_{gdn21} + C_{bdn21} + C_{gsn22} + C_{bsn22}$

$C_{7R} = C_{gdn32} + C_{bdn32} + C_{gsn33} + C_{bsn33}$

$C_{8R} = C_{gdn31} + C_{bdn31} + C_{gsn32} + C_{bsn32}$

$C_{9R} = C_{gdn43} + C_{bdn43} + C_{gsn44} + C_{bsn44}$

$C_{10R} = C_{gdn42} + C_{bdn42} + C_{gsn43} + C_{bsn43}$

$C_{11R} = C_{bdn41} + C_{gsn42} + C_{bsn42}$

$C_R = C_{gdn41}$.

TABLE II
DRAIN CURRENT EQUATION USED IN THE MODIFIED SPICE PROGRAM FOR A MOSFET IN THE LINEAR REGION

$$I_{DS} = \beta\{(V_{GS} - V_{BIN} - \frac{\eta}{2} V_{DS}) \cdot V_{DS} - \frac{2}{3}\gamma_s[(2\phi_F + V_{DS} - V_{BS})^{3/2} - (2\phi_F - V_{BS})^{3/2}]\}$$

where

$$\beta = \frac{W}{L} \cdot \mu_s \cdot C_{ox}$$

$$C_{ox} = \frac{\epsilon_{SIO_2}}{T_{OX}}$$

$$\mu_s = UO\left(\frac{UCRIT \cdot \epsilon_{SI}}{C_{ox}[V_{GS} - V_{TH} - UTRA \cdot \min(V_{DS}, 2\phi_F)]}\right)^{UEXP}$$

$$V_{TH} = V_{BIN} + \gamma_s \cdot (2\phi_F - V_{BS})^{1/2}$$

$$V_{BIN} = V_{BI} + (\eta - 1) \cdot (2\phi_F - V_{BS})$$

$$V_{BI} = V_{TO} - GAMMA \cdot (2\phi_F)^{1/2}$$

$$\eta = 1 + \frac{\pi \cdot DELTA \cdot \epsilon_{SI}}{4 \cdot C_{ox} \cdot W}$$

$$\gamma_s = GAMMA \cdot (1 - \alpha_S - \alpha_D)$$

$$\alpha_S = \frac{1}{2} \frac{XJ}{L} \cdot [(1 + \frac{2 \cdot W_S}{XJ})^{1/2} - 1]$$

$$\alpha_D = \frac{1}{2} \frac{XJ}{L} \cdot [(1 + \frac{2 \cdot W_D}{XJ})^{1/2} - 1]$$

$$W_S = XD \cdot (2\phi_F - V_{BS})^{1/2}$$

$$W_D = XD \cdot (2\phi_F - V_{BS} + V_{DS})^{1/2}$$

$$XD = \left(\frac{2 \cdot \epsilon_{SI}}{q \cdot NSUB}\right)^{1/2}$$

It is not adequate, therefore, to use a fixed resistance to represent an MOSFET in a logic gate.

According to the zero value time constant method, the characteristic rise pole P_r can be expressed as

$$P_r = [R_{23R}(C_{2R} + C_{3R}) + R_{4R}C_{4R} + R_{5R}C_{5R} + R_{6R}C_{6R} + R_{7R}C_{7R} + R_{8R}C_{8R} + R_{9R}C_{9R} + R_{10R}C_{10R} + R_{11R}(C_{11R} + C_R) + R_{12R}C_{12R}]^{-1}. \quad (1)$$

TABLE III
THE EXPRESSIONS OF THE LINEARIZED DRAIN CURRENTS IN THE EQUIVALENT CIRCUIT USED FOR THE CHARACTERISTIC RISE TIME CALCULATION OF A CMOS 4-3-2-1-INPUT AOI GATE

$$X_{kS} = [-V_{Gk}+V_{BINk} - \frac{2}{3}\gamma_{Sk}(|2\phi_{Fk}|+V_{Bk}-V_{Sk})^{1/2} + \frac{\eta_k}{2}\gamma_{Sk}]|_{t=te}$$

$j = n44, n43, n42, n33, n32, n22.$

$k = p31, p21, p1.$ $\quad t_e = (1/p_r)\ln 2.$

$$\gamma_{Dp41} = \gamma_{Sp31} = 2V_{DD} - [(V_{DD}-V_{Tpf})\exp(-0.375)]/2$$

$$\gamma_{Dp31} = \gamma_{Sp21} = 2V_{DD} - [(V_{DD}-V_{Tpf})\exp(-0.25)]/2$$

$$\gamma_{Dp21} = \gamma_{Sp1} = 2V_{DD} - [(V_{DD}-V_{Tpf})\exp(-0.125)]/2$$

$$\gamma_{Dn44} = \gamma_{Dn33} = \gamma_{Dn22} = \gamma_{Dp1} = 3V_{DD}/2$$

$$\gamma_{Sn22} = 2(V_{DD}-V_{Tnf}) - [(V_{DD}-V_{Tnf})\exp(0.0025)]/2$$

$$\gamma_{Sn33} = \gamma_{Dn32} = 2(V_{DD}-V_{Tnf}) - [(V_{DD}-V_{Tnf})\exp(0.004)]/2$$

$$\gamma_{Sn32} = 2(V_{DD}-V_{Tnf}) - [(V_{DD}-V_{Tnf})\exp(0.0075)]/2$$

$$\gamma_{Sn44} = \gamma_{Dn43} = 2(V_{DD}-V_{Tnf}) - [(V_{DD}-V_{Tnf})\exp(0.01)]/2$$

$$\gamma_{Sn43} = \gamma_{Dn42} = 2(V_{DD}-V_{Tnf}) - [(V_{DD}-V_{Tnf})\exp(0.02)]/2$$

$$\gamma_{Sn42} = 2(V_{DD}-V_{Tnf}) - [(V_{DD}-V_{Tnf})\exp(0.04)]/2$$

$$V_{Tpf} = -\{2[\gamma_{Spte}(2\phi_{Fn})^{1/2} - V_{Tp}] + \gamma_{Spte}^2\}/2 + \{[2\gamma_{Spte}(2\phi_{Fn})^{1/2} - 2V_{TP} + \gamma_{Spte}^2]^2 + 4[2\gamma_{Spte}V_{Tp}(2\phi_{Fn})^{1/2} + \gamma_{Spte}^2 V_{DD} - V_{Tp}^2]\}^{1/2}/2$$

$$V_{Tnf} = -\{2[\gamma_{Snte}(2\phi_{Fp})^{1/2} - V_{Tn} + \gamma_{Snte}^2]/2 + \{[2\gamma_{Snte}(2\phi_{Fp})^{1/2} - 2V_{Tn} + \gamma_{Snte}^2]^2 + 4[2\gamma_{Snte}V_{Tn}(2\phi_{Fn})^{1/2} + \gamma_{Snte}^2 V_{DD} - V_{Tn}^2]\}^{1/2}/2$$

$$V_{Tp} = V_{BINpte} + \gamma_{Spte}(2\phi_{Fn})^{1/2}$$

$$V_{Tn} = V_{BINnte} + \gamma_{Snte}(2\phi_{Fp})^{1/2}$$

$$\gamma_{Spte}(\gamma_{Snte}) = \gamma_{Sp}(\gamma_{Sn})|_{t=te}$$

$$V_{BINnte}(V_{BINpte}) = V_{BINn}(V_{BINp})|_{t=te}$$

$$I_{dp41} = \beta_{p41}X_{p41D}V_{03}$$

$$I_{dp31} = \beta_{p31}(X_{p31D}V_{04} - X_{p31S}V_{03})$$

$$I_{dp21} = \beta_{p21}(X_{p21D}V_{05} - X_{p21S}V_{04})$$

$$I_{dp1} = \beta_{p1}(X_{p1D}V_0 - X_{p1S}V_{05})$$

$$I_{dn44} = \beta_{n44}(X_{n44D}V_0 - X_{n44s}V_{09})$$

$$I_{dn43} = \beta_{n43}(X_{n43D}V_{09} - X_{n43S}V_{010})$$

$$I_{dn42} = \beta_{n42}(X_{n42D}V_{010} - X_{n42S}V_{011})$$

$$I_{dn33} = \beta_{n33}(X_{n33D}V_0 - X_{n33S}V_{07})$$

$$I_{dn32} = \beta_{n32}(X_{n32D}V_{07} - X_{n32S}V_{08})$$

$$I_{dn22} = \beta_{n22}(X_{n22D}V_0 - X_{n22S}V_{06})$$

where

$$\beta_i = W_i\mu_{Stei}C_{ox}/L_i$$

$$\mu_{Stei} = \mu_{Si}|_{t=te}$$

$i = p41, p31, p21, p1, n44, n43, n42, n33, n32, n22.$

$$X_{p41D} = -V_{DD}\cdot\exp(-0.375)\cdot 2^{-P_f/P_r} + [V_{BINp41} - \frac{2}{3}\gamma_{sp41}(2\phi_{FP41} + V_{BP41} - V_{DP41})^{1/2} + \frac{\eta_{P41}}{2}\gamma_{DP41}]|_{t=te}$$

$$X_{jD} = [V_{Gj} - V_{BINj} - \frac{2}{3}\gamma_{Sj}(2\phi_{Fj} + V_{Dj} - V_{Bj})^{1/2} - \frac{\eta_j}{2}\gamma_{Dj}]|_{t=te}$$

$$X_{jS} = [V_{Gj} - V_{BINj} - \frac{2}{3}\gamma_{Sj}(2\phi_{Fj} + V_{Sj} - V_{Bj})^{1/2} - \frac{\eta_j}{2}\gamma_{Sj}]|_{t=te}$$

$$X_{kD} = [-V_{Gk} + V_{BINk} - \frac{2}{3}\gamma_{Sk}(|2\phi_{Fk}| + V_{Bk} - V_{Dk})^{1/2} + \frac{\eta_k}{2}\gamma_{Dk}]|_{t=te}$$

TABLE IV
THE EXPRESSIONS OF THE OUTPUT RESISTANCES LOOKING INTO THE CAPACITOR PORTS IN THE EQUIVALENT CIRCUIT OF A CMOS 4-3-2-1-INPUT AOI GATE

$$R_{23R} = \frac{1}{\beta_{p41}X_{p41D}}$$

$$R_{4R} = \frac{1}{\beta_{p31}X_{p31D}} + \frac{X_{p31S}}{X_{p31D}}\frac{1}{\beta_{p41}X_{p41D}}$$

$$R_{5R} = \frac{1}{\beta_{p21}X_{p21D}} + \frac{X_{p21S}}{X_{p21D}}\frac{1}{\beta_{p31}X_{p31D}} + \frac{X_{p21S}X_{p31S}}{X_{p21D}X_{p31D}}\frac{1}{\beta_{p41}X_{p41D}}$$

$$R_{12R} = \frac{1}{\beta_{p1}X_{p1D}} + \frac{X_{p1S}}{X_{p1D}}\frac{1}{\beta_{p21}X_{p21D}} + \frac{X_{p1S}X_{p21S}}{X_{p1D}X_{p21D}}\frac{1}{\beta_{p31}X_{p31D}} + \frac{X_{p1S}X_{p21S}X_{p31S}}{X_{p1D}X_{p21D}X_{p31D}}\frac{1}{\beta_{p41}X_{p41D}}$$

$$R_{6R} = \frac{1}{\beta_{n22}X_{n22S}} + \frac{X_{n22D}}{X_{n22S}}R_{12R}$$

$$R_{7R} = \frac{1}{\beta_{n33}X_{n33S}} + \frac{X_{n33D}}{X_{n33S}}R_{12R}$$

$$R_{8R} = \frac{1}{\beta_{n32}X_{n32S}} + \frac{X_{n32D}}{X_{n32S}}\frac{1}{\beta_{n33}X_{n33S}} + \frac{X_{n32D}X_{n33D}}{X_{n32S}X_{n33S}}R_{12R}$$

$$R_{9R} = \frac{1}{\beta_{n44}X_{n44S}} + \frac{X_{n44D}}{X_{n44S}}R_{12R}$$

$$R_{10R} = \frac{1}{\beta_{n43}X_{n43S}} + \frac{X_{n43D}}{X_{n43S}}\frac{1}{\beta_{n44}X_{n44S}} + \frac{X_{n43D}X_{n44D}}{X_{n43S}X_{n44S}}R_{12R}$$

$$R_{11R} = \frac{1}{\beta_{n42}X_{n42S}} + \frac{X_{n42D}}{X_{n42S}}\frac{1}{\beta_{n43}X_{n43S}} + \frac{X_{n42D}X_{n43D}}{X_{n42S}X_{n43S}}\frac{1}{\beta_{n44}X_{n44S}} + \frac{X_{n42D}X_{n43D}X_{n44D}}{X_{n42S}X_{n43S}X_{n44S}}R_{12R}$$

Because the output voltage is assumed to have a single-pole response, the characteristic rise time T_R can be written as

$$T_R = \ln 9/P_r. \tag{2}$$

Similarly, the large-signal equivalent circuit for the characteristic fall time calculation can be obtained as shown in Fig. 4. The characteristic fall pole P_f and fall time T_F can be written as

$$P_f = [R_{23F}(C_{2F} + C_{3F}) + R_{4F}C_{4F} + R_{5F}C_{5F} + R_{6F}C_{6F} + R_{7F}C_{7F} + R_{8F}C_{8F} + R_{9F}C_{9F} + R_{10F}C_{10F} + R_{11F}(C_{11F} + C_F) + R_{12F}C_{12R}]^{-1} \tag{3}$$

$$T_f = \ln 9/P_f. \tag{4}$$

Both P_r and P_f are nonlinear equations of P_r/P_f. However, they can be easily solved by using numerical iterations.

The rise propagation delay T_{PLH} as defined in Fig. 2 can be expressed as

$$T_{PLH} = t_{dr} + \frac{\ln 2}{\ln 9}T_R - \frac{\ln 2}{\ln 9}T_F. \tag{5}$$

For simplicity, empirical laws for the initial delay times t_{dr} and t_{df} were found. As a result, the rise propagation delay T_{PLH} and the pair delay T_P can be reformulated by the simple relations

$$T_{PLH} = 0.8T_R - 0.15T_F \tag{6}$$

$$T_P = T_{PLH} + T_{PHL} = 0.3T_R + 0.7T_F. \tag{7}$$

Note that the above equations are universal and can be used to calculate the delay times for various AOI gates with satisfactory

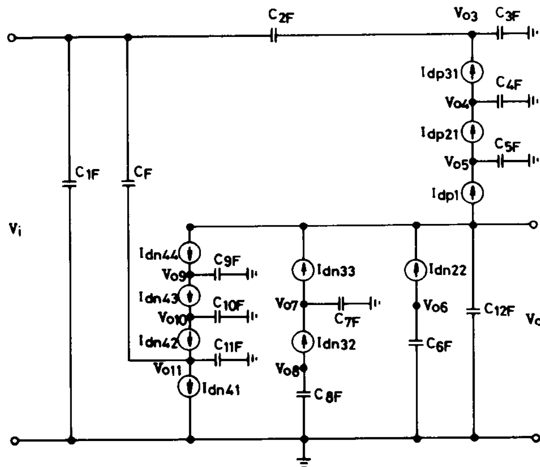

Fig. 4. Large-signal equivalent circuit of a CMOS 4-3-2-1-input AOI gate during the fall time period.

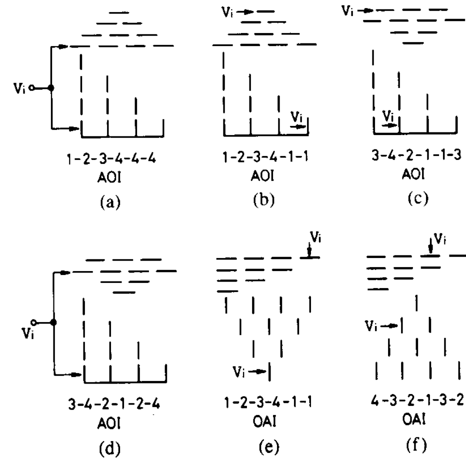

Fig. 5. Symbolic diagrams and six-digit codes of some CMOS AOI/OAI gates.

accuracy, as will be verified in the following section. It can be realized that the delay equations (6) and (7) are universal only when T_R and T_F are calculated from the derived formulas.

For the 4-3-2-1-input AOI gate under nonworst-case timing condition, the input voltage V_i drives an NMOSFET and a PMOSFET other than M_{n41} and M_{p41}, respectively. The delay times can be similarly modeled but with different capacitances and currents.

In the PMOSFET part of the 4-3-2-1-input AOI gate, there are four different branches each with 1, 2, 3, or 4 PMOSFET's in parallel. The four branches can be connected in series to form 24 different configurations. The delay times of these different AOI gates can be characterized by using the developed modeling technique. Besides the 4-3-2-1-input AOI gate with 24 different configurations, the modeling technique can also be applied to other AOI gates with less than 4 NMOSFET's or 4 PMOSFET's in series. The timing models for all these AOI gates have been built with the delay time equations of (6) and (7).

A six-digit code is designed to represent various AOI gates for easy identification. Each of the first four most significant digits (MSD's) represents the number of parallel PMOSFET's in a branch. The branch farthest to the output node corresponds to the first MSD and so on. The fifth digit is used to denote the position of the PMOSFET branch driven by the input voltage. The driven PMOSFET branch farthest to the output node is denoted as 1 whereas that nearest to the output node as 4. The sixth digit denotes the position of the driven NMOSFET in a series NMOSFET branch. Starting with 1 for the top MOSFET, each of the lower MOSFET's is assigned to a successively larger number. According to the above description, the AOI gate in Fig. 1 can be represented by 4-3-2-1-1-4. More examples are given in Fig. 5(a)–(d) where the AOI gates are shown by the symbolic diagrams. A similar code system is used to represent OAI gates. Two examples are given in Fig. 5(e) and (f).

A 4-3-2-1-input OAI gate under the worst-case timing condition is shown in Fig. 6 where the input voltage drives the MOSFET's M_{n41} and M_{p41}. Similar to the AOI gates, the NMOSFET branches in series can be arranged to form 24 different configurations. For all these different configurations of OAI gates and other simpler OAI gates with less than 4 PMOSFET's or 4 NMOSFET's in series, the worst-case and the nonworst-case timing can be characterized by applying the same modeling technique. The timing models for all these OAI gates have been built. The universal delay time equations for the OAI gates are

$$T_{PLH} = 0.8T_R - 0.25T_F \quad (8)$$

$$T_P = 0.4T_R + 0.6T_F \quad (9)$$

where T_R and T_F are the calculated characteristic rise and fall times of OAI gates, respectively.

Note that the developed timing modes can be applied to CMOS AOI/OAI gates with both long-channel and small-geometry devices, because a small-geometry AOI/OAI gate has an inherent output voltage waveform nearly independent of the device channel lengths and its timing can be characterized similarly as in the long-channel case. However, this similarity does not exist in simple CMOS inverters, and NAND/NOR gates [6], [22].

III. Comparisons With SPICE Simulations

To verify the accuracy of the developed analytical timing models, extensive comparisons between theoretical calculations and SPICE simulations were made for the AOI/OAI gates with different configurations, device sizes, device parameters, capacitive loads, and input excitations. Fig. 7(a) shows the 3.5-μm CMOS 3-2-1-0-1-3 AOI gates with $C_L = 5.0$ pF and normal device parameters, whereas Fig. 7(b) shows the 4-3-2-1-1-4 OAI gates with $C_L = 0$ pF and V_{TON} reduced to 0.3 V. It is found that the maximum error is 30% in the calculated delay times for the AOI/OAI gates with fixed load capacitors.

The input waveform effect on the output signal timing is incorporated into our model through the term $V_{GS} \cdot V_{DS}$ in the drain-current expression of the driven MOSFET's. For example, the rise time calculation of the AOI gate as shown in Fig. 1, the drain current I_{dp41} of the driven PMOSFET M_{p41} has a term $V_{GS} \cdot V_{DS}$ which is related to $V_i \cdot V_{o3}$ and then is linearized as $V_i(t_e) \cdot V_{o3}(t)$. Since t_e is related to the output rise pole P_r and V_i to the input fall pole P_f, the term $V_i(t_e)$ in X_{p41D} of the resultant linearized drain current I_{p41} and all the resistances is a function of P_f/P_r as may be seen from Tables III and IV. Finally, the output rise pole P_r becomes a function of the input fall pole P_f and the input waveform effect is included. Thus the developed model can predict the output responses under noncharacteristic input waveform excitations.

Table V shows the 3.5-μm CMOS 1-2-3-4-4-2 AOI gates driven by the step input and the input waveforms with rise and fall times two times as large as those in the characteristic waveform case. The ability to calculate the noncharacteristic waveform timing makes the developed models more practical and versatile in computing the timing of CMOS AOI/OAI gates.

There is a compromise between the model accuracy and the applicable ranges of the models. Thus the maximum error of 30% can be reduced if the model applicable range is slightly confined to those gates with commonly used device dimensions. For example, the maximum error of delay times for the CMOS AOI gates with

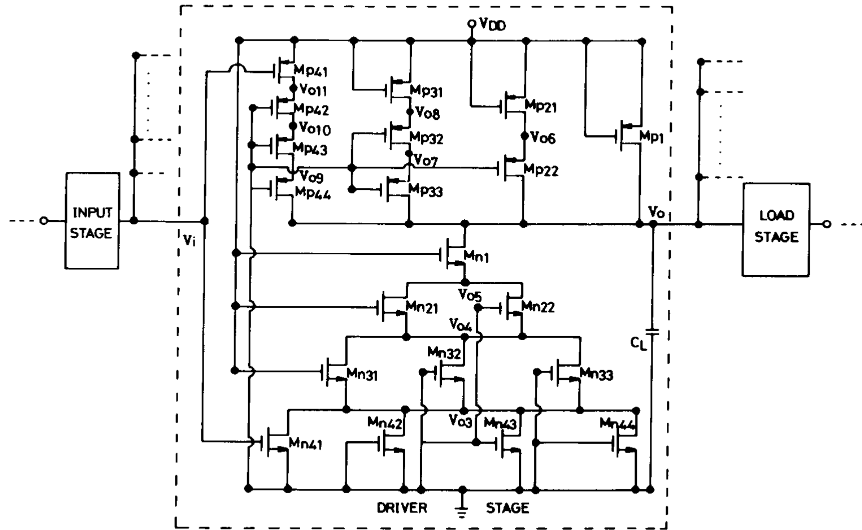

Fig. 6. A chain of identical CMOS 4-3-2-1-input OAI gates under the worst-case timing condition.

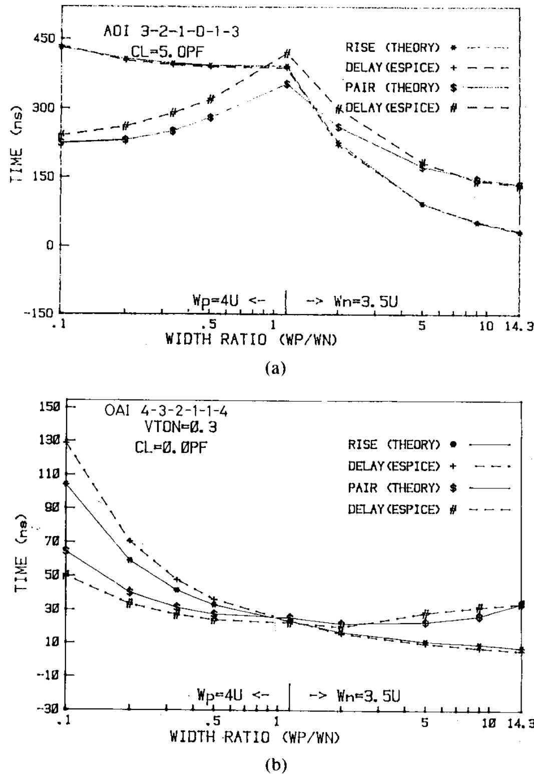

Fig. 7. Calculated and simulated rise/pair delay of (a) the 3.5-μm CMOS 3-2-1-0-1-3 AOI gates with normal parameters; (b) the 3.5-μm CMOS 4-3-2-1-1-4 OAI gates with a reduced V_{TON} to 0.3 V.

commonly used device dimensions can be reduced to 16% by properly tuning the universal constants in (6) and (7). The tuned results are

$$T_{PLH} = 0.9T_R - 0.11T_F \tag{10}$$

TABLE V
CALCULATED AND SIMULATED TIMING DATA OF CMOS 1-2-3-4-4-2 AOI GATES WITH $W_P/W_N = 4\ \mu m/3.5\ \mu m$ AND $L_{mask} = 3.5\ \mu m$

Input Excitation	C_L (pF)	Data Type	T_R	T_{PLH}	T_F	T_{PHL}
Step	0	THEORY(ns)	26,28	21.02	4.86	4.13
		SPICE (ns)	28.80	25.30	6.45	4.52
		ERROR (%)	-8.75	-16.90	-24.60	-8.63
	5	THEORY(ns)	666	532.8	141	133.95
		SPICE (ns)	830	581	198	138.6
		ERROR (%)	-19.7	-8.30	-28.80	-3.35
Rise Time =56.3 ns Fall Time =25.32ns	0	THEORY(ns)	30.35	20.88	22.80	-8.80
		SPICE (ns)	28.10	29.40	18	-7.20
		ERROR (%)	+8.00	-29	+26.60	-22
Rise Time =1660ns Fall Time =736 ns	5	THEORY(ns)	856.6	575	602	-318.3
		SPICE (ns)	855	640.5	465	-248
		ERROR (%)	+0.19	-10.2	+29.4	-29.7

$$T_P = 0.46T_R + 0.66T_F. \tag{11}$$

Similarly, the tuned equations for the CMOS OAI gates are

$$T_{PLH} = 0.67T_R - 0.33T_F \tag{12}$$

$$T_P = 0.45T_R + 0.72T_F. \tag{13}$$

As expected, the developed timing models can also be applied to complex small-geometry CMOS AOI/OAI gates. It is found that the maximum error is still 16% for various 1.5-μm CMOS AOI/OAI gates with commonly used device dimensions. Part of comparisons are shown in Fig. 8(a) and (b) for 1.5-μm CMOS AOI and OAI gates with $C_L = 0.0$ pF, respectively.

IV. Applications of the Timing Models in Autosizing

To demonstrate the application of the developed timing models in autosizing, the timing models are implemented in an experimental autosizing program called the TIming Synthesis and Analysis

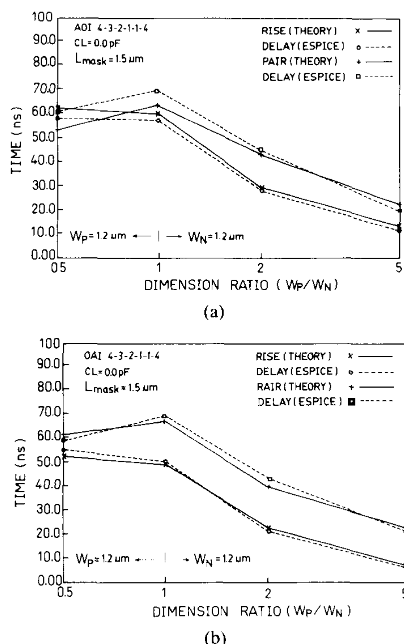

Fig. 8. Calculated and simulated rise/pair delay of (a) the 3.5-μm CMOS 4-3-2-1-1-4 AOI gates; (b) the 1.5-μm CMOS 4-3-2-1-1-4 OAI gates.

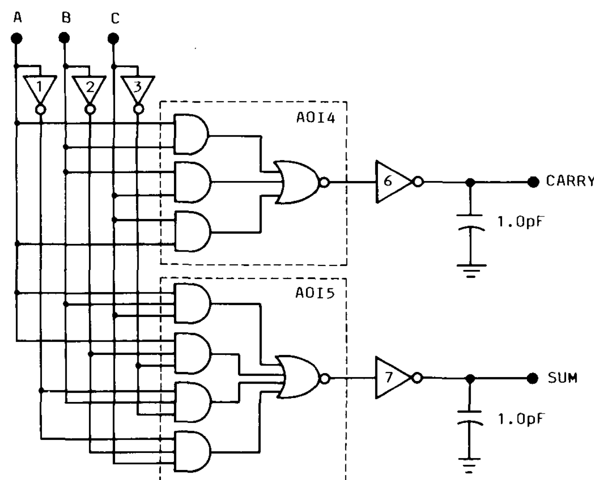

Fig. 9. A 1-b full adder to be sized.

(TISA) Program [6]. In the TISA, two popular CMOS design strategies are adopted in synthesizing the device sizes. One strategy is that all the same type of MOSFET's in series in a logic gate are designed with equal channel widths and so are all MOSFET's in parallel [10]. The other is that only the input excitation pattern which leads to the worst-case timing of a logic gate is considered in sizing. This results in a save design so that the actual chip delay is always smaller than that synthesized. Under these two strategies, the optimal device sizes which lead to the minimum total delay time can be obtained by solving the developed timing equations through the numerical optimization algorithm [27].

As shown in Fig. 9, a 1-b full adder is designed. The synthesized device sizes are listed in Table VI. Table VII lists the comparisons between SPICE simulations and model calculations under the consideration that the input pattern ABC changes from 100 to 110. It is found that the error is 10.8 and 7.2% for the outputs CARRY and SUM.

TABLE VI
THE DEVICE SIZES OF THE FULL ADDER IN FIG. 9 SYNTHESIZED BY USING THE TISA PROGRAM WITH THE MINIMUM TOTAL DELAY TIME

Gates	Dimension	
	W_P (μm)	W_N (μm)
INV1	10.5	3.5
INV2	10.5	3.5
INV3	10.5	3.5
AOI4	11.5	3.5
AOI5	100	35
INV6	19.5	6.0
INV7	268	84

TABLE VII
COMPARISONS OF TIMING DATA FOR THE FULL ADDER IN FIG. 9 WITH THE DEVICE SIZES IN TABLE VI

Total Delay Time (ns)					
CARRY			SUM		
THEORY	SPICE	ERROR(%)	THEORY	SPICE	ERROR(%)
4.60	4.15	10.8	6.22	5.80	7.2

V. CONCLUSION

Efficient physical timing models for complex 1.5- and 3.5-μm CMOS AOI/OAI gates have been successfully developed to calculate the signal timing without performing troublesome SPICE transient simulations. Under the characteristic waveform consideration, the rise time and fall time equations in the developed models are first derived from the dominant pole of the linearized large signal equivalent circuit of the gate. To efficiently find the dominant pole, the zero value time constant method [26] is adopted. Universal laws are then found to calculate the delay times from the calculated rise and fall times.

Extensive comparisons between theoretical computations and SPICE simulations were made. It is found that the developed timing models have a maximum error of 30% in calculating the signal timing of the CMOS AOI/OAI gates with wide ranges of device dimensions, capacitive loads, device parameter variations, logic input patterns, and input excitation waveforms not deviating much from the characteristic. The same maximum error is found in the timing calculations of all different configurations of the CMOS AOI/OAI gates with less than 4 NMOSFET's or 4 PMOSFET's in series. However, the model error can be further tuned to 16% for 1.5 and 3.5-μm CMOS AOI/OAI gates with commonly used device dimensions.

The application of the developed timing models in autosizing has also been demonstrated successfully. With the aid of the developed timing models, the sized gates can have a much less deviation in delay times from the simulated values. This gives a more correct design than the case of using a rough timing model. The consumed CPU time is still in the reasonable range.

ACKNOWLEDGMENT

The authors would like to thank reviewers for their critical reading of the manuscript and helpful suggestions.

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Detection of Multiple Faults in MOS Circuits

F. JOEL FERGUSON

***Abstract*—This paper characterizes test sets that detect multiple faults in MOS circuits guided by the observation that such circuits are implemented as networks of switches. This leads to a conceptually simple technique for generating multiple fault test sets. Sufficient conditions for the detection of all multiple faults are given for switch networks, and it is shown that a test set exists meeting these conditions for any irredundant circuit with certain restrictions on fan out. In the cases where these conditions cannot be met, a class of "robust" test sets is presented. Test sets are presented that generate complete multiple fault test sets with fewer vectors for many MOS complex gates than is possible using a gate-level description of the circuit.**

I. INTRODUCTION

Recently, there has been much interest in modeling faults in MOS circuits at the circuit level due to the inability of logic-level fault models to adequately characterize their faulty behavior [1]-[3]. Wadsack [1] showed that transistor-stuck faults in MOS, especially CMOS, circuits can cause sequential behavior in a combinational circuit. Galiay *et al.* [2] showed that many faults in MOS circuits cannot be modeled by the gate-level single-line stuck-at-0/1 fault (SSF) model, implying that many actual faults may not be detected by SSF test sets.

Multiple faults are possible and probable due to a single fabrication defect [3]-[5]. Three percent of all single defects that were simulated in [5] caused multiple faults. The distribution of defect sizes in that study was inversely proportional to the cube of the defect radius and only defects of a radius less than 4 μm were considered. Since defects often appear in clusters [6] and are often more than 4 μm in radius, the likelihood of multiple faults in physical circuits is even greater than indicated in [5].

There has been considerable research in detecting multiple-line stuck-at faults (MSFS) in gate-level circuits. Gault *et al.* [7] detailed several circuit structures in which any complete SSF test set is a complete MSF test set, characterized conditions that one component of a multiple fault can mask another, and set limits on the number of tests necessary for a complete MSF test set for some classes of circuits. Schertz and Metze [8] developed equivalence classes to determine possible masking relationships among faults. Agarwal and Fung [9] set bounds on the percentage of multiple faults detected by SSF test sets, and Hughes [10] presented experimental data concerning the percentage of multiple faults detected by SSF test sets. Other gate-level research focused on algebraic techniques for generating MSF test sets [11], [12].

El-ziq and Su [13] developed test procedures for the detection of all multiple transistor stuck faults for a specific class of complex gates with fan-out free inputs. Jha developed a procedure based

Manuscript received September 12, 1988; revised May 8, 1989 and September 6, 1989. This work was supported in part by the Semiconductor Research Corporation under Contracts SRC-83-01-022 and 89-DJ-141. This paper was recommended by Associate Editor V. K. Agarwal.

The author is with the Computer Engineering Department, University of California at Santa Cruz, Santa Cruz, CA 95064.

IEEE Log Number 9036171.

0278-0070/90/0900-1009$01.00 © 1990 IEEE