國立交通大學

電子工程學系電子研究所

博士論文

高速電流引導式數位類比轉換器

High-Speed Current-Steering Digital-to-Analog Converters

研究生 ： 曾偉信

指導教授 ： 吳介琮

中華民國一佰年六月

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博士論文

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中華民國一佰年六月

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摘要

通訊系統裡大多數的資訊是在數位形態做處理，但是這些資訊要發射到介質中時，需要轉到類比的形態再由載波傳送出去。可知，數位類比轉換器及類比數位轉換器是系統中必須要的區塊。而這些轉換器是連接品質好壞的關鍵，經常限制了通訊系統的速度與精準度，因此高頻寬與高動態範圍的轉換器是有強烈需求的。

本論文將著重在數位類比轉換器 (Digital-to-Analog Converters, DACs) 上，要達高速操作電流引導式架構是被廣泛採用的，因其速度限制是來自於輸出端而非電路內部，因此有利於高速操作。然而，非理想的電流切換限制了無雜散動態範圍 (spurious-free dynamic range, SFDR) 的頻寬，當輸入之數位信號達高頻時無雜散動態範圍也急速下降。為了保持良好的高頻無雜散動態範圍，此論文提出「數位式亂數歸零法 (Digital Random Return-to-Zero, DRRZ) 」。

為了實驗本論文提出的「數位式亂數歸零法」，吾人實現一個八位元、每秒十六億個取樣之數位類比轉換器，使用九十奈米之互補式金氧半場效電晶體，此數位類比轉換器給定弦波輸入時，其無雜散動態範圍優於六十分貝，直至輸入頻頻高達四點六億赫茲，且優於五十五分貝直到輸入頻率為八億赫茲，功率消耗量為

九十毫瓦。

當高解析度的電流引導式數位類比轉換器是必須時，電流源就得高度滿足匹配特性，其付出的代價即為大面積，由面積引起的本質電容、雜散電容也變大因而導致頻寬下降，改善此現象的途徑為使用較小面積的電流源。然而，小面積電流源將引起嚴重的不匹配，本論文提出一個背景校正技術來保確高精準度。

為驗証本論文提出的背景校正理論，吾人實現一個十二位元數位類比轉換器，使用九十奈米金氧半場效電晶體，且電流源面積只有理論值的四百分之一。此數位類比轉換器功率消耗為一百二十八毫瓦，有效面積為一仟一百乘七百五十微米。操作速度可達每秒十二點五億個取樣。當頻率高達五億赫茲時，此數位類比轉換器有優於七十分貝之無雜散動態範圍。

High-Speed Current-Steering Digital-to-Analog Converters

Student : Wei-Hsin Tseng Advisor : Jieh-Tsorng Wu

Department of Electronics Engineering
and Institute of Electronics
National Chiao-Tung University

Abstract

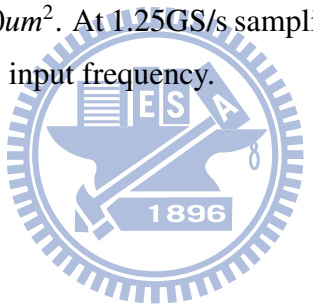
In communication systems, most of the information processing is performed in the digital domain, but the signal carrying the information must be transmitted using analog signals. Therefore, the use of digital-to-analog(DA) and analog-to-digital(AD) converters are unavoidable. Data converters are critical for connecting signals to the real world, often limiting the accuracy and speed of the overall system. As a result, wide-band high-dynamic-range converters are in high demand.

This thesis focuses on the Digital-to-Analog Converters (DACs). The current-steering structure has been widely used in high-speed DACs, since in this structure the main speed limitation comes from the output node, and high sampling speed is thus easily achieved. However, the non-ideal switching limits the bandwidth of spurious-free dynamic range(SFDR). The SFDR decreases rapidly with increasing input frequency. Therefore, Digital Random Return-to-Zero(DRRZ) is proposed for the high sampling rate current-steering DAC to maintain high SFDR at high frequency.

To demonstrate the proposed Digital Random Return-to-Zero technique, a CMOS 8-bit 1.6-GS/s DAC was fabricated in a 90 nm CMOS technology. The DAC achieves a SFDR better than 60 dB for a sinewave input up to 460 MHz, and better than 55 dB up to 800 MHz. The DAC consumes 90 mW of power.

In the design of high-accuracy current-steering DACs, current sources with high matching property are required and the penalty is large area. Intrinsic and parasitic capacitor loading also degrade the signal bandwidth. The way to reduce loading is using compact current cells. In this thesis, background calibration is proposed to correct the mismatch current caused by small dimension.

To verify the proposed background calibration algorithm, a 12-bit DAC was fabricated in 90nm CMOS technology and using compact current cells. The area of current sources are 1/400 of the required area which is designed for 12-bit resolution. The chip consumes 128mW. Active area is 1100x750um^2. At 1.25GS/s sampling rate, the DAC achieves better SFDR than 70dB up to 500MHz input frequency.



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曾偉信

國立交通大學

中華民國一佰年六月

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Chapter 1

Introduction

1.1 Motivation

In communication systems, most of the information processing is performed in the digital domain, but the signal carrying the information must be transmitted using analog signals. Therefore, the use of digital-to-analog(DA) and analog-to-digital(AD) converters are unavoidable. Data converters are critical for connecting signals to the real world, often limiting the accuracy and speed of the overall system and this work focuses on the DACs. Wide-band high-dynamic-range DACs are in high demand, especially for multicarrier radio applications [1, 2]. A simplified architecture of a cable modem head end transmitter is shown in Figure 1.1. The cable modem system consists of multiple channels, where each channel contains a digital modulator and a DAC. When multiple channels are combined simultaneously, as shown in Figure 1.2, the SFDR of the DAC should meet a minimum SFDR. If the SFDR is worse than the requirement,signals in one channel will be corrupted by spurious components from other channels. Therefore, the major challenge for designing DAC of frequency domain applications is to obtain a wide-band SFDR. Moreover, if the DAC can provide a high sampling rate and large SFDR bandwidth, the multiple channel signal can be combined in digital domain. Then, the digital code can be delivered by one DAC. Figure 1.3 [3] shows another example, a signal transmission over radio frequency (RF) involves a complex system design. A baseband message, typically digital, is converted to an analog signal through a DAC at the beginning of the transmission system

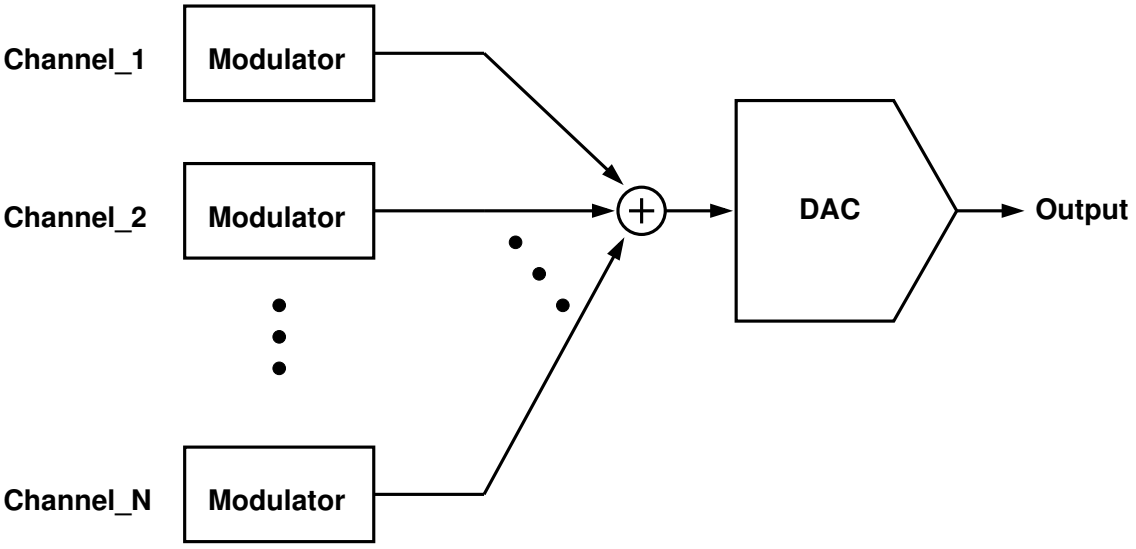

Figure 1.1: Block diagram of multi channel transmitter for cable modem.

and a series of analog processing which filtering the signal suitable for RF transmission. If the DACs are designed with good high frequency SFDR, the requirement of filter can be relaxed [4].

In recent years, many arts have been published on high-speed DAC design [1, 5, 6, 7, 8, 4, 9, 10, 11, 12]. Most of these designs concentrate on obtaining good low-frequency performance, but they do not perform well at higher frequencies. In [9], the spectrum shows that spurs, almost harmonic distortions, can be improved because they are higher than the noise floor. Therefore, the goal of this work is to reduce the harmonic distortions at high and low frequency. We should know the key points that cause harmonic distortions. At low frequency, the performance is limited by static linearity, DNL and INL, the nonlinearity source is from mismatch of current cells. To design a DAC, designers take care of matching by matching properties of MOSFET [13] or use techniques such as calibration [14, 15, 16, 17, 5, 18, 19, 20, 21, 22, 23], dynamic element matching [24, 25, 26, 27, 28], and random walks [29, 30]. That is, several ways can be used to have a good static linearity.

In [17], the measured DNL and INL are good, but SFDR still drops at high frequencies. The reason is that the DACs cause more switching transients. Switching transient is the non-ideal temporary waveform at output node when switching occurs. Each cur-

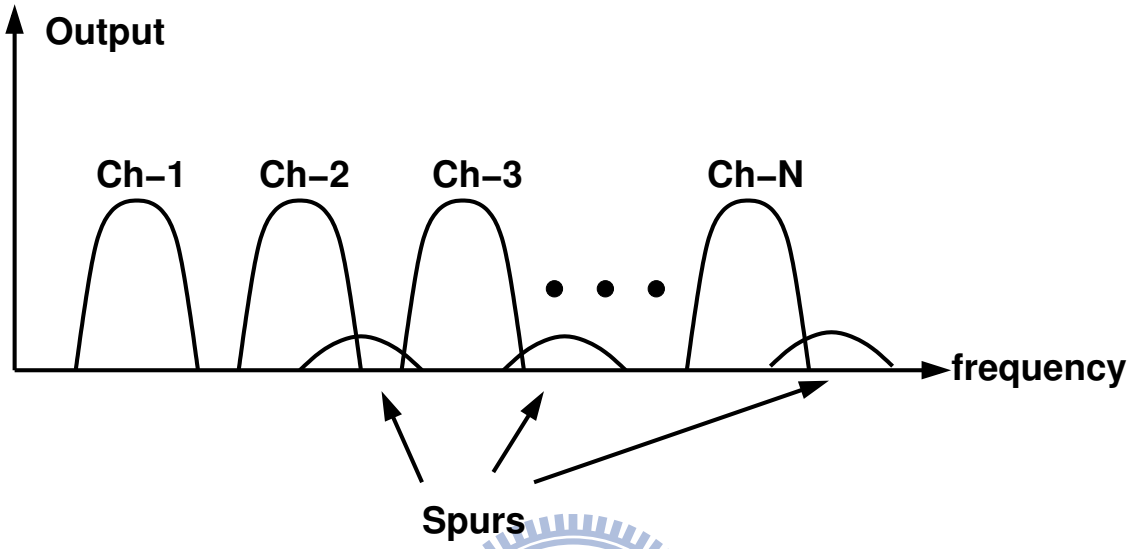

Figure 1.2: Harmonic distortions will interference adjacent channel.

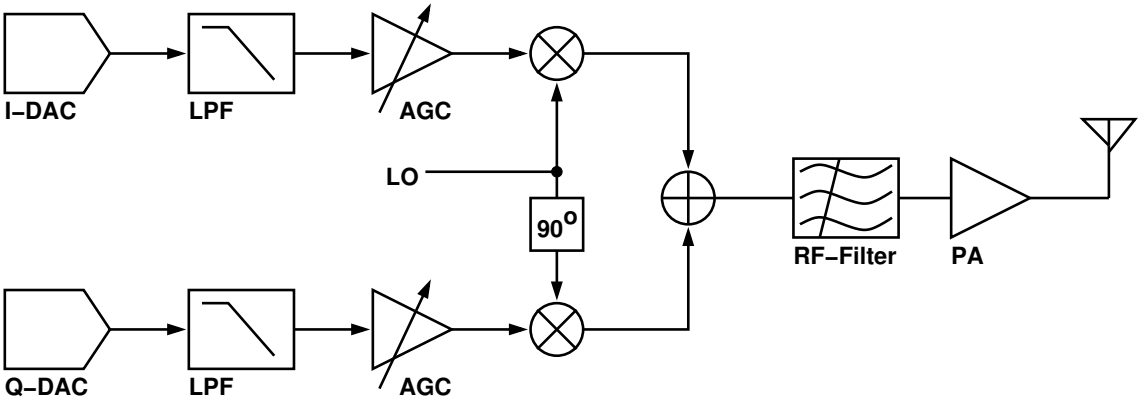

Figure 1.3: Application of DAC in Transmitter chain.

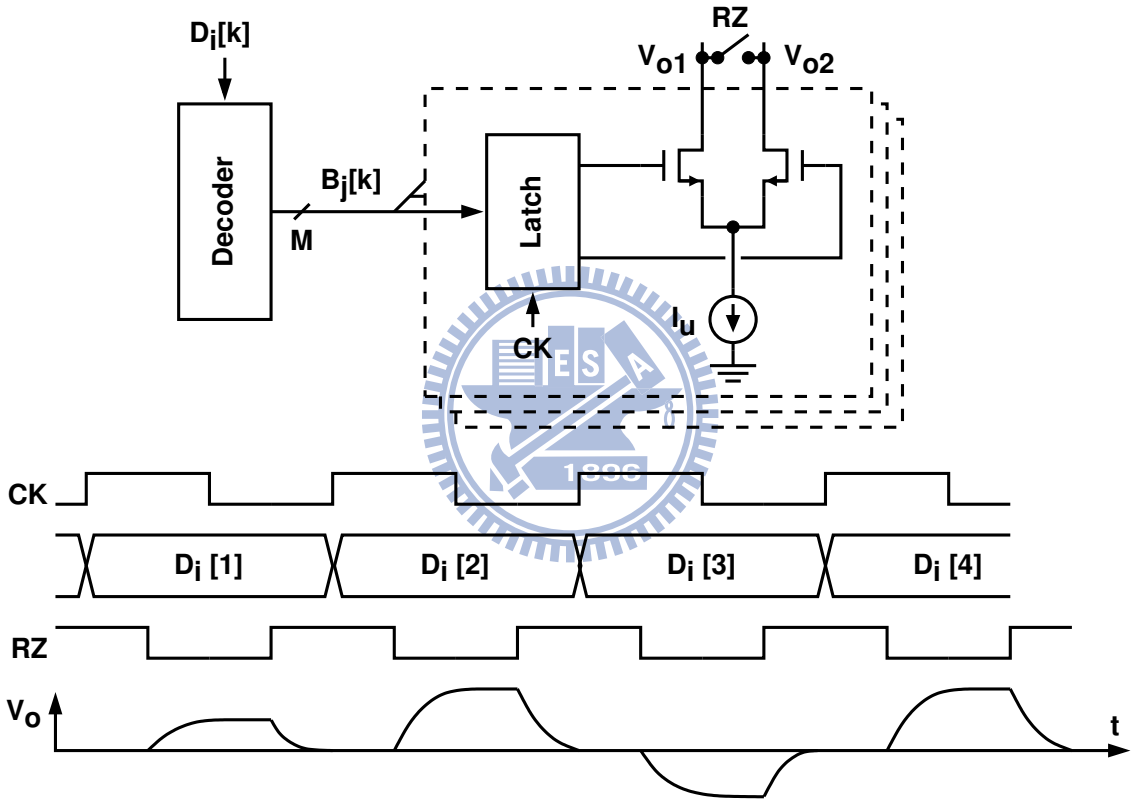

Figure 1.4: The ARZ can be expressed as an equivalent switch at output node.

rent cell has different switching transients due to clock skew, drivers mismatch, signal feed-through, and internal node fluctuation. In other words, they are cell dependant, also called code-dependant, and will result in harmonic distortions. This is why the prior arts perform well at low frequencies but not well at high frequencies. In [31], analog return-to-zero(ARZ) was proposed to mitigate this effect. As shown in Figure 1.4, ARZ can be expressed as an equivalent switch at output node and controlled by the signal RZ. The RZ signal has a phase delay with clock. When RZ is low, the switch will short the output and force the differential current to zero. If switching transient occurs at this state, they would be hidden by the switch. However, the switch is on the signal path, the turn-on resistor must be small for good linearity. Most of high speed DACs output 16 mA of current. It means that the switch will pass 8mA, the area cost of this switch is very high and induce parasitic capacitor, which is a serious disadvantage for high sampling rate.

In this thesis, we proposed a digital return-to-zero (DRZ). It can be realized by only replacing the latch architecture and digital input sequence. Moreover, random sequence is inserted into the digital return-to-zero. Then, the switch transients are randomized into noise floor, and SFDR will be improved. This new technique is digital random return-to-zero, called DRRZ. A lower resolution, 8-bit, DACs was fabricated in 90nm COMS to verify the DRRZ [32], and the sampling rate is 1.6GS/s.

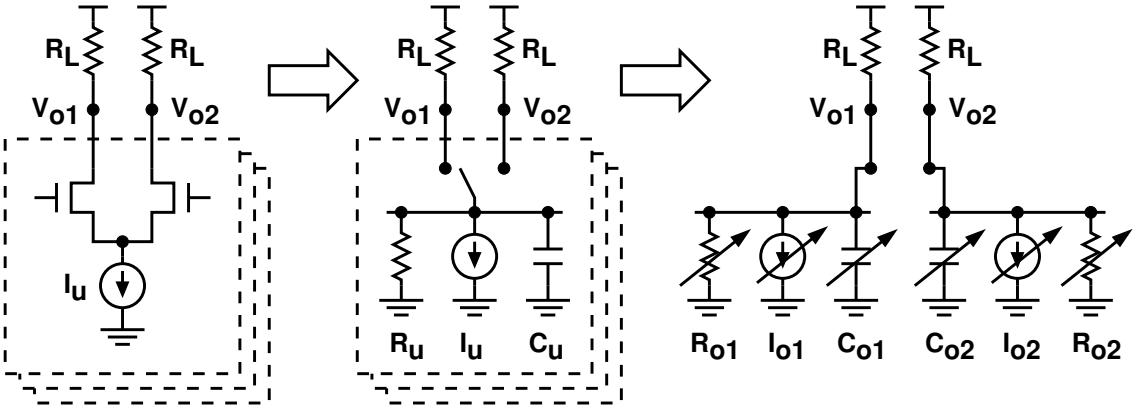

Figure 1.5: Code-dependent loading variation (CDLV).

Figure 1.5 shows another source of harmonic distortion. Each current cell is modeled as an ideal switch on top of an ideal current source I_u in parallel with a resistor R_u and a capacitor C_u. The resistor R_u represents the output resistance of the current source.

The capacitor C_u represents the capacitance associated with the output node of the current source, including the gate capacitance of the current switch. Both R_u and C_u are connected to either the V_{o1} node or the V_{o2} node, depending on the state of the switch. As a result, the total loadings for output nodes V_{o1} and V_{o2} vary with digital input $D_i[k]$. This code-dependent loading variation (CDLV) effect introduces harmonic distortion in the differential output $V_o = V_{o1} - V_{o2}$. Increasing R_u and reducing C_u can mitigate the CDLV effect. Adding cascode stage to a current source can increase R_u. In most designs, the CDLV effect at high frequencies is dominated by C_u. The C_u capacitance is determined by the device dimensions of the current switch and the current source, while the device dimensions are governed by the matching requirements. The CDLV effect can be mitigated by adding an additional cascode stage following the current switch in each current cell [33, 7, 34]. The MOSFETs in those cascode stages need to have large transconductances to achieve good high-frequency performance [34, 12].

For this work, instead of adding additional cascode stages, we simply use smaller devices for both the current sources and the current switches to reduce C_u. Smaller devices lead to larger mismatches. However, due to the use of DRRZ, the matching requirement for the current switches is relaxed. We also propose a new calibration algorithm for the using of smaller current cells which will reduce parasitic capacitor; therefore, the DACs would be operated in higher sampling rate. A 12-bit 1.25GS/s DAC[35] is implemented as a design example.

1.2 Organization

The organization of the thesis is described as follows:

Chapter 2 discusses the highlight to design a high speed high performance current-steering DACs. Including transient effect, finite output impedance effect and static linearity. And introduce the techniques to improve the static and dynamic performances.

Chapter 3 describes a 8-bit and with a high sampling rate of 1.6GS/s DAC. This DAC is designed to demonstrate the digital random return-to-zero(DRRZ) can improve the high output frequency SFDR.

In Chapter 4, base on the DRRZ technique, we develop a background calibration

technique to overcome the mismatch due to small size. Since small size is used for high speed and wide SFDR bandwidth.

Finally, conclusions and recommendations for future works will be given in Chapter 5.


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Chapter 2

Design Considerations for DACs

2.1 Introduction

This chapter lists three sections for designing a high performance of current-steering DAC. The first is basic resolution requirement or static linearity. In general design, the matching is guaranteed by large size and gate over-drive voltage. The second and the third are code-dependant switching transient (CDST) and code-dependant loading variation(CDLV) respectively. The static linearity impacts the both signal to noise ratio (SNR) and SFDR. The effects of CDST and CDLV will result in the degradation of SFDR.

2.2 Static Linearity

The DAC static linearity is specified as differential nonlinearity (DNL) and integral nonlinearity (INL). In the design of high-accuracy current steering DACs, the matching properties are the first issue that should be concerned. For example, the DNL and INL of a DAC are shown in Figure 2.1. While the INL is as large as 10LSBs, the spectrum shown in Figure 2.2 is spurious with odd and even order harmonic distortions. As a result, the dynamic performance of a current-steering DAC is limited by not only frequency but also static linearity. This section will discuss the technique for good static linearity.

I. Matching property

In a simple design, we can choose proper device sizes for the matching of transistors

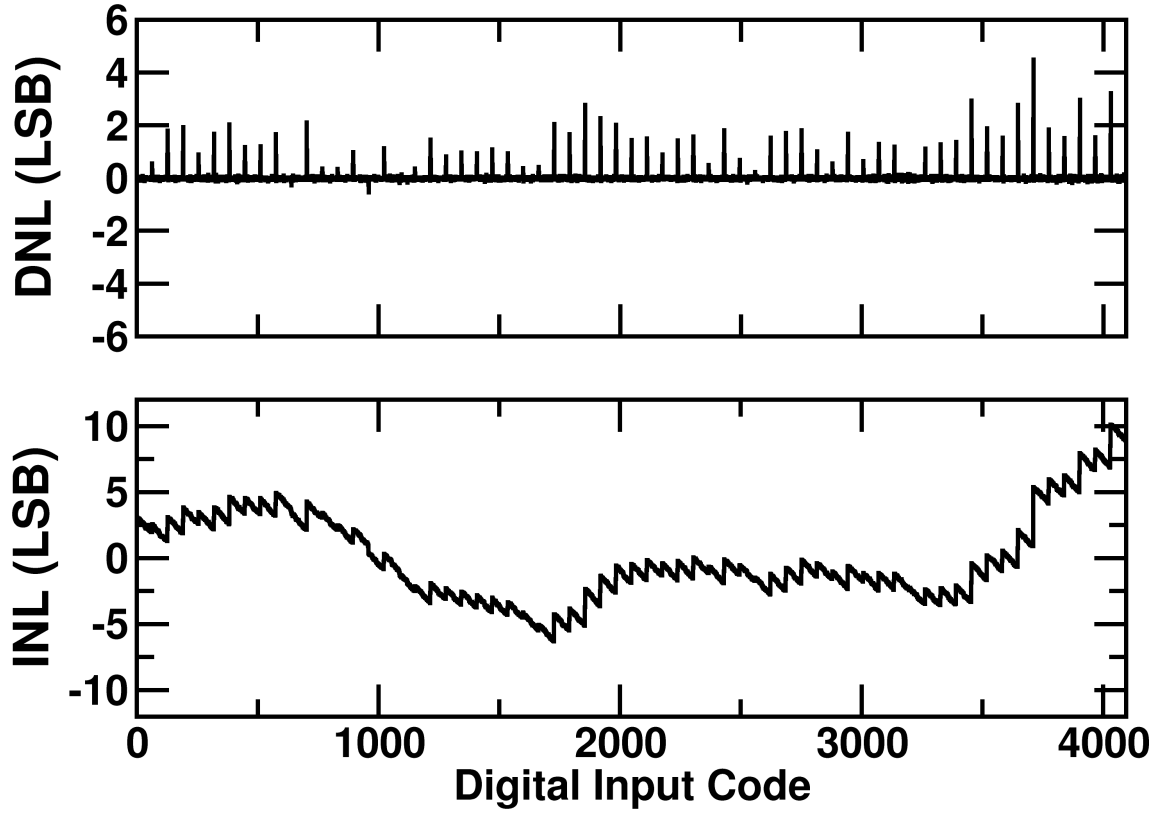


Figure 2.1: A DAC with worse DNL and INL

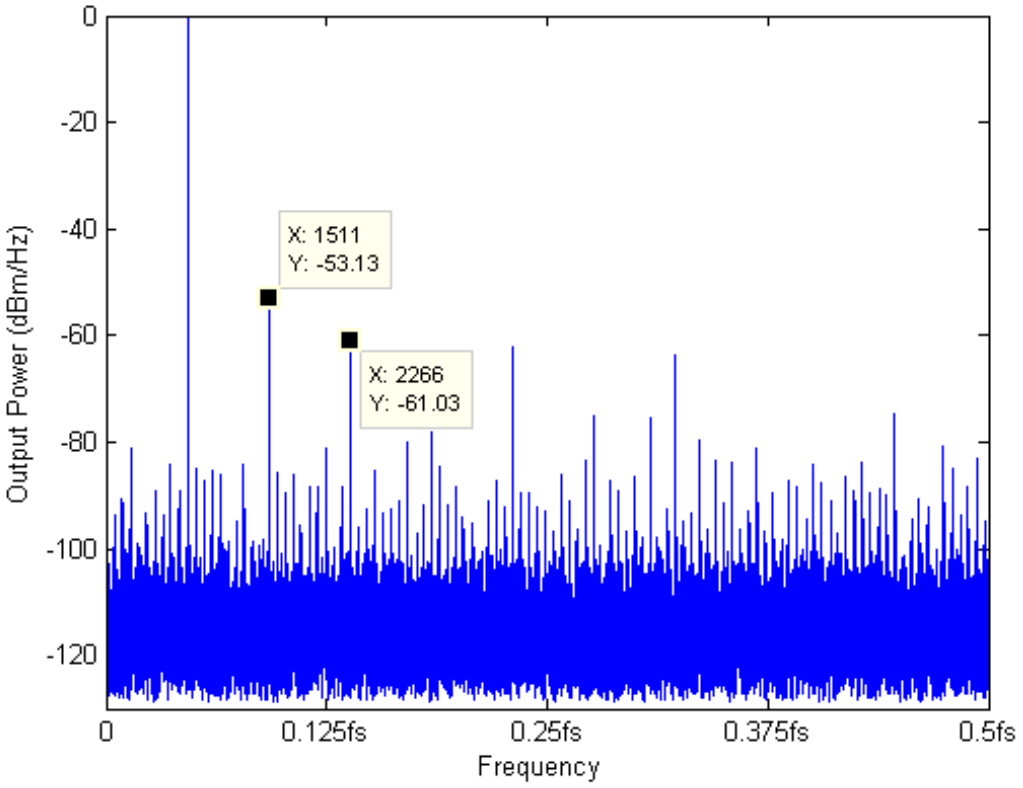


Figure 2.2: When the INL is as large as 10LSB in Figure 2.1, the spectrum is spurious with odd and even order harmonic distortions.

Table 2.1: Maximum INL of a 8-bit 5-3 segment DAC

INL (max)	$\sqrt{256}\sigma$	$\leq 0.5LSB$
DNL(max)	$\sqrt{16}\sigma$	$\leq 0.5LSB$

Table 2.2: The required area versus different gate overdrive

V_{ov} (mV)	100	150	200	250	300	350
WL_{unit} $(um^2)(1\sigma)$	14.1/2	6.4	3.7	2.5	1.8	1.1
WL_{unit} $(um^2)(3\sigma)$	127/2	57.6	33.3	22.5	16.2	9.9

[13]. The current mismatch between two transistors can be calculated by matching data and the equation.

$$\sigma^2_{\frac{\Delta I}{I}} = \frac{1}{W \cdot L} \cdot (\frac{4A^2_{VT}}{V_{ov}} + A^2_{\beta}), \tag{2.1}$$

where σ is the standard deviation of mismatch current, W is the MOSFET width and L is the Length, and A_{VT} and A_{β} are the matching parameters from foundry.

For 8-bit with 5-3 segmentation, LSB = 1I, 2I, 4I and MSB = 8I 8I 8I ... Then, the maximum INL and DNL are listed in Table 2.1 and the requirement is less than 0.5 LSB. Then, the σ and the area are expressed as

$$1 \times \sqrt{256}\sigma \leq 0.5$$

$$\sigma \leq 3.125 \times 10^{-2}$$

$$2 \times (3.125 \times 10^{-2})^2 \times WL_{unit} \geq 4 \cdot \frac{5.81^2}{V^2_{ov}} + 0.0162^2$$

The required area versus different gate overdrives, V_{ov}, are listed in Table 2.2. Generally, we use three sigma for the yield up to 99.7%, and Table 2.3 is the relation of yield and sigma.

II. Dynamic Element Matching

In the technique of dynamic element matching, the DAC is made of several unit DAC elements which inevitably are subject to random mismatches incurred during IC fabrica-

Table 2.3: The relationship between yield and sigma

σ	×1.0	×1.4	×1.6	×1.8	×2	×2.2	×2.4	×2.6	×2.8	×3.0
yield	68.3	77.0	83.8	89.0	92.8	95.4	97.2	98.4	99.1	99.7

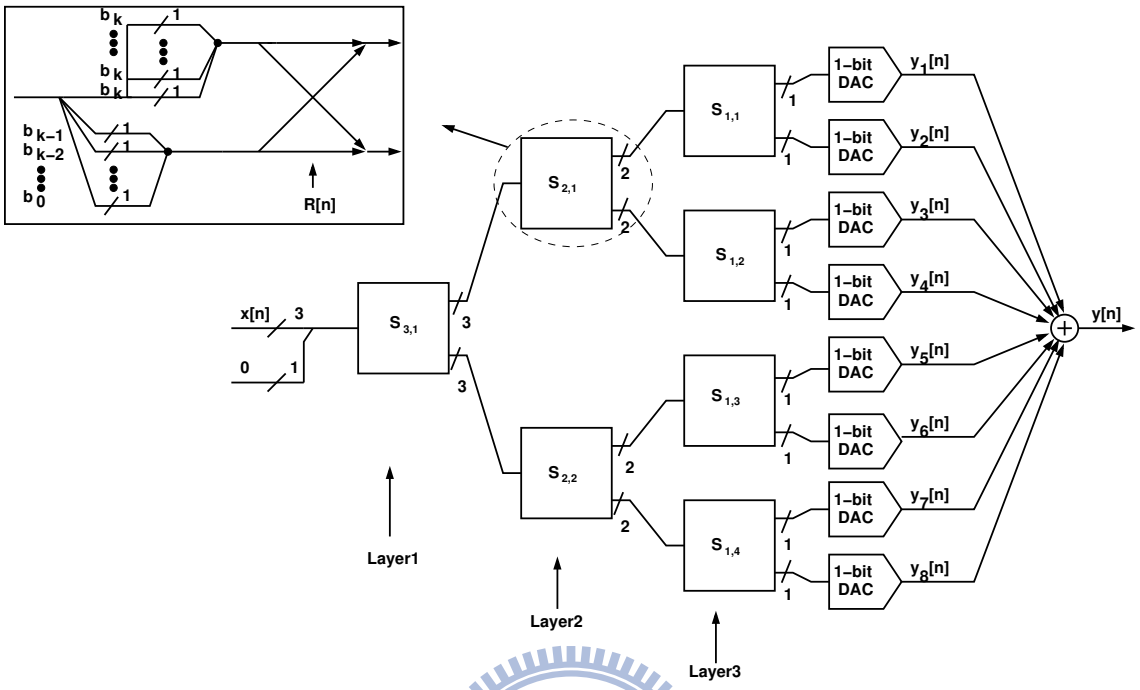


Figure 2.3: A 3-bit 3-layer DEM DAC

tion as well as possible systematic circuit and layout mismatches. DAC output signals which usually introduce nonlinear distortion in the overall DAC output signal, often limiting the linearity of the overall DAC. In [25, 27, 36, 37, 24], dynamic element matching (DEM) was proposed for high-resolution DACs. They spread the mismatching into noise by selecting unit DAC elements randomly. A 3-bit 3-layer DEM DAC was shown in Figure 2.3, and each layer was controlled by random numbers. The first layer input $x[n]$ is decoded by switch box $S3,1$. The $x[n]$ will be randomly distributed into $y_1[n]$ *to* $y_8[n]$, so the mismatch of each 1-bit DAC will not be code-dependant. That is, DEM spreads the mismatch into noise floor. In [29, 30], random walk was proposed to reduce the systematic and graded errors. The random walk is a scheme for the layout placement, and they have good performance on the INL.

III. Calibration and Trimming

Calibration and trimming techniques are the schemes to against the random mismatch, allowing to use small current source transistors. In [17], the authors proposed an foreground self-trimming. The off-chin CAL-ADC, shown in Figure 2.4, digitizes the mis-

match of each MSB current cells at star-up step. Then, the mismatch are stored in memory and a CAL-DAC is used to compensate the total mismatch of the MSB current cells. And in [5], the authors also proposed an off-line self-trimming technique which is based on the trimmable floating gate. The gate can be charged and discharged, and then the current is changed. However, the foreground self-trimming techniques lack of tracking ability of supply and temperature variation. There would be a 0.7 LSB drift over temperature variation form -40 to 85 degrees [20]. As a result, the author proposed background calibration technique which can work under the normal operation. The floating current sources [15] provide the current from the tail node, so the current calibration does not interrupt the normal operation. In [18], the floating source and an analog calibration loop are shown in Figure 2.5. The current comparator locates at right-half side, and the total current of the current source injects into comparator at node A. The cell current and I_B are summed to be compared with I_R. If I_R is larger than the total current, the C_{store} will be discharged. During the guard time between two consecutive calibration phases when MSB cells are switched, the parasitic capacitance at node B may discharge due to the temporary current imbalance. To prevent subsequent charge-sharing from causing glitches, the latter is sampled by a common tracking capacitor Chold during the phase before the particular MSB be calibrated. This pre-sampled voltage VHi is then used to hold the voltage on node B through a buffer during the guard time to make the transition seamless.

2.3 Code-Dependant Switching Transients(CDSTs)

At the beginning of this section, we define and introduce what code-dependant switching transient is.

Figure 2.6 shows the operation of a single current cell. The current cell contains a current source I_u and a MOSFET current switch M1-M2. Upon the rising edge of clock CK, the binary input $B_j[k]$ is loaded into the latch. Its two complementary outputs, V_{s1} and V_{s2}, drive the current switch, directing the I_u current to either output node V_{o1} or output node V_{o2}. Figure 2.6 also shows the transient response of the differential output current $I_o = I_{o1} - I_{o2}$. The output current I_o is a combination of an ideal transient response and switching transients. Switching transients occur only when $B_j[k]$ varies. There are

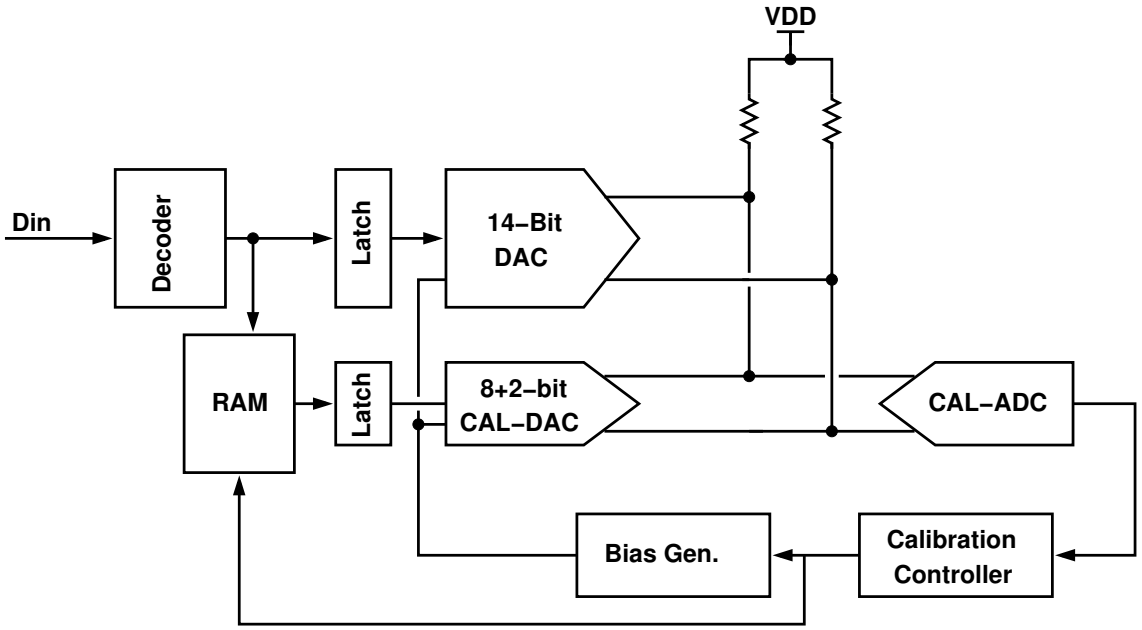


Figure 2.4: Calibrated DAC architecture proposed by Cong

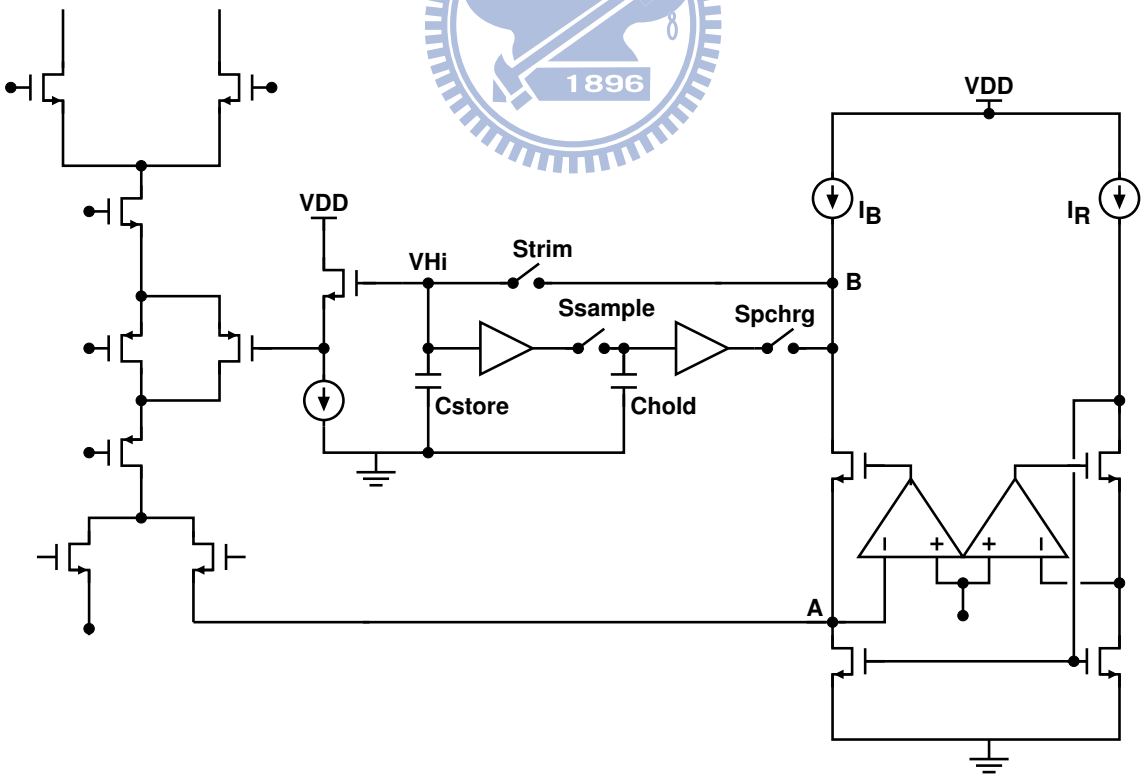


Figure 2.5: Calibrated DAC architecture proposed by Q. Huang

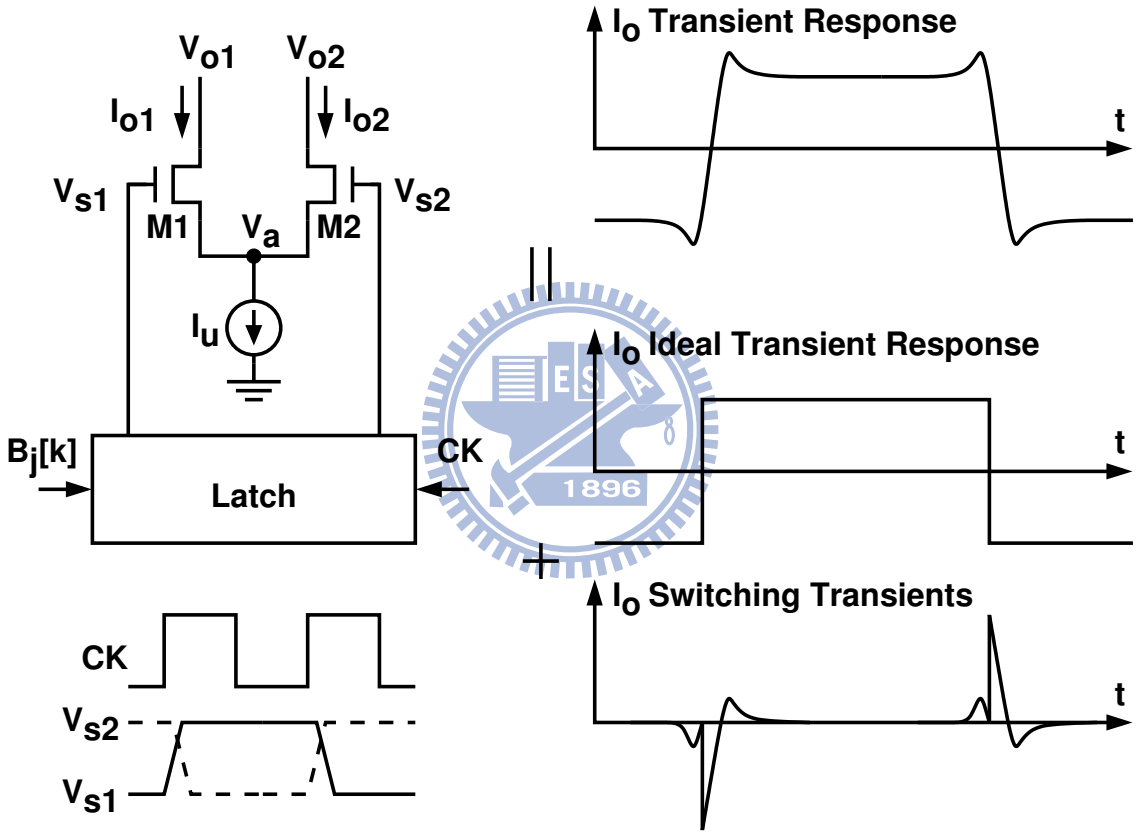


Figure 2.6: Code-dependent switching transient (CDST).

several sources for switching transients [31], including switch feedthrough through the current switch, timing skew of CK or cell-delay differences [38], finite rise/fall time of V_{s1} and V_{s2}, and voltage fluctuation at the common-source node V_a.

The I_o switching transients from all current cells are summed up at the DAC V_o port. Assume the switching transients are invariant and identical among all current cells, and the switching transients at the rising edges of I_o are the inverse of the switching transients at the falling edges of I_o. Then total switching transients appear at V_o are proportional to $D_i[k] - D_i[k-1]$. These identical switching transients do not cause harmonic distortion. However, there are device variations in both the current switch and the latch, and there are different CK timing skew for different current cells. Thus, different current cells exhibit different switching transients. Depending on the $D_i[k]$ sequence, the sequence of the switching transient summation becomes a nonlinear term, resulting in harmonic distortions. This is called the code-dependent switching transient (CDST) effect. If the input $D_i[k]$ is a single-tone sinewave and its frequency is increased, the CDST effect is intensified due to the increase of $|D_i[k] - D_i[k-1]|$. Thus, the DAC SFDR decreases with increasing input frequency.

To reduce variation in switching transients, the V_{s1} and V_{s2} waveforms must be carefully designed. Matching among current switches, latches, and CK routes must be considered in the design. Adding a cascode stage to the current switch is also a common practice to reduce feedthrough of V_{s1} and V_{s2} into the outputs.

Control signal feed-through

The control signal of one current cell is decoded from input signal D_i; in other words, all controls are a function of input D_i. And if the function is ideal, the control signals contribute a signal gain into output without distortion. Unfortunately, the feed through paths are different due to the binary architecture and device mismatch. In most of DACs, the size of switches are changed according to the current weighting, so that the junction capacitors are different. As a result, the signal feed through will contribute to harmonic distortion. We use a 12-bit DAC with 6-6 segmentation to simluate the impact of switch size. Figure 2.7 is the unit cell to run this simulation, and only the switch MOSFETs are with transistor model. The resistors, current source, decoder and switch driver are ideal components. As shown in Figure 2.8 and Figure 2.9, the large switch size DAC is more

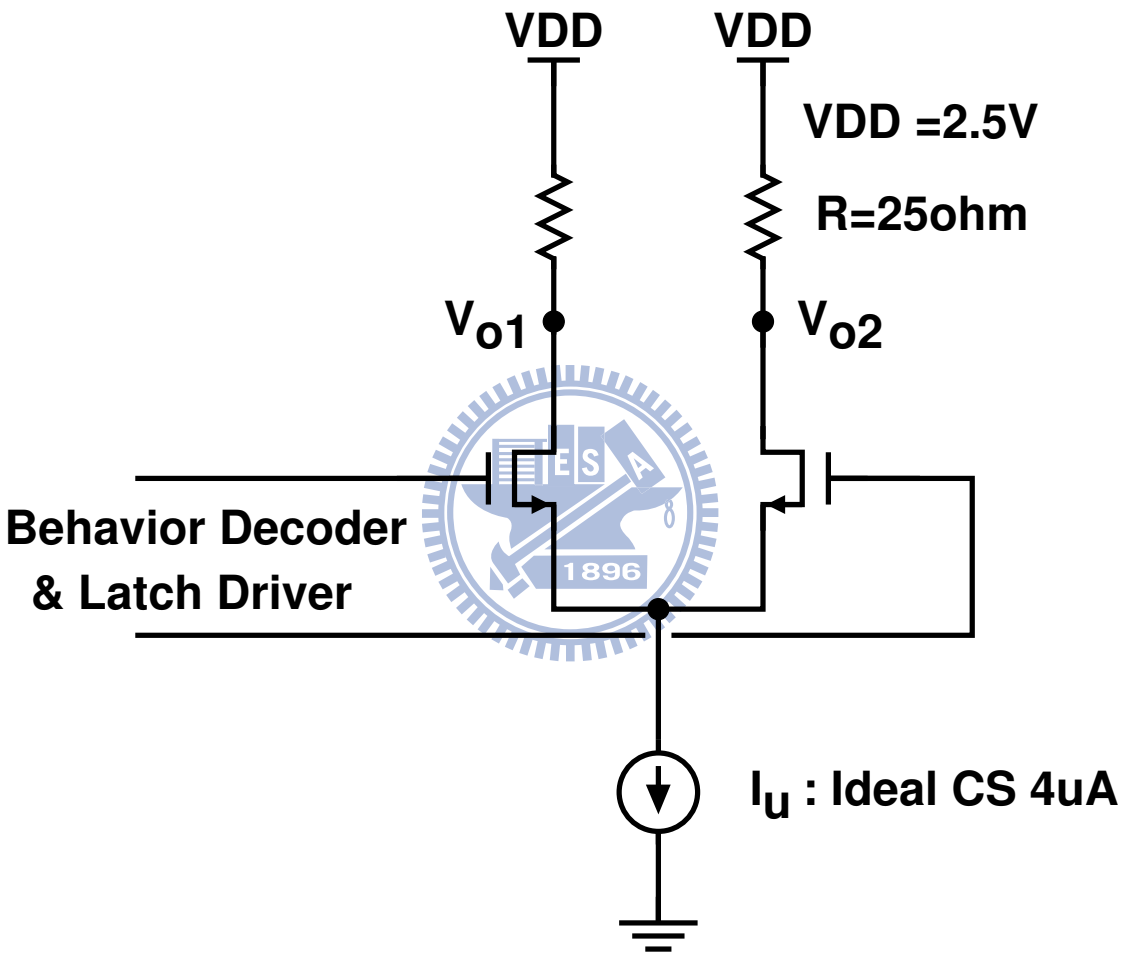


Figure 2.7: Unit current cell with ideal current source, resistor and latch driver. The current switches are thick oxide device.

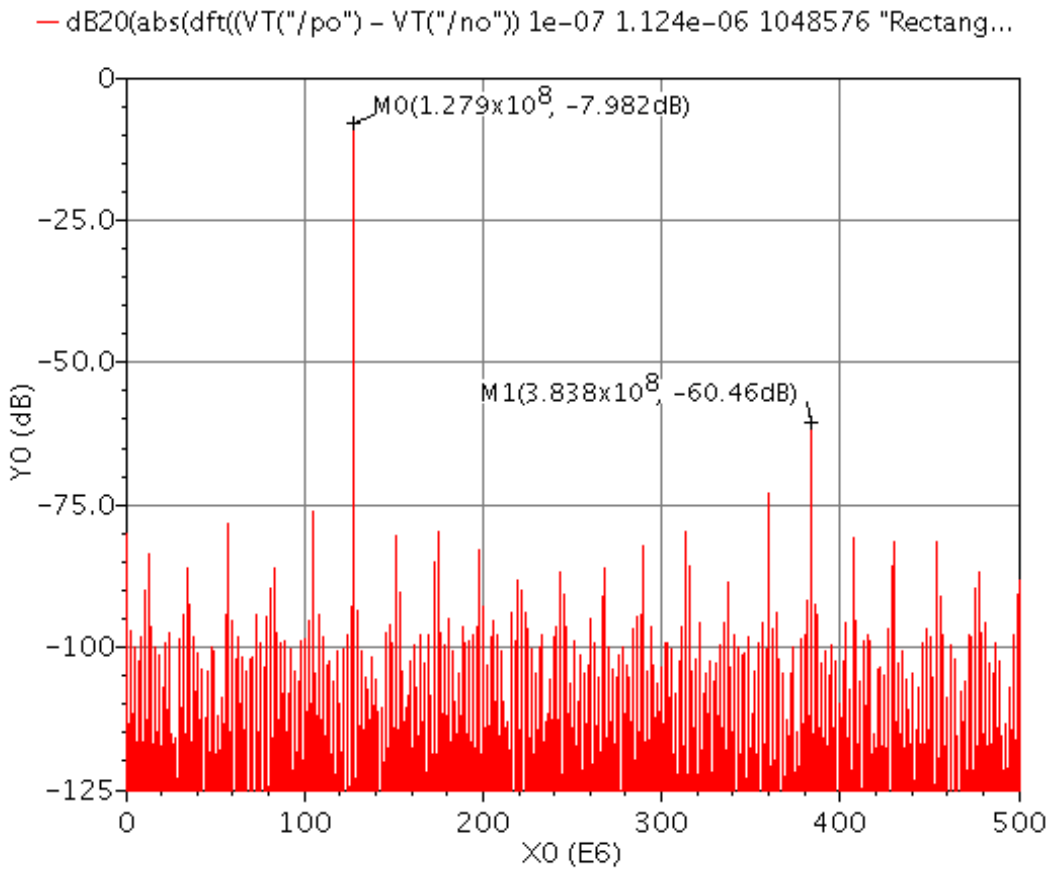


Figure 2.8: Simulated Spectrum with sample rate 1GS/s switches size W=2.44um L=0.24um and SFDR 52.5dB.

spurious at sampling rate of 1 GS/s. The SFDRs are 52.5dB and 55.3dB respectively. The feed-through of control signals are passing by the capacitor; therefore, when the sampling clock is down to 200 MS/s, the SFDR shown in Figure 2.10 is higher than 1 GS/s. The simulation results are summarized in Figure 2.11. The SFDR with sample rate 1GS/s of switch size W=1.44um L=0.24um is better than the SFDR of switches size W=2.44um L=0.24um. And the switch size W=2.44um L=0.24um, the SFDR at 200 MS/s of sampling rate is better than at 1 GS/s.

Clock skew between current sources

For high resolution DAC, the area of current source must be large enough to fit the

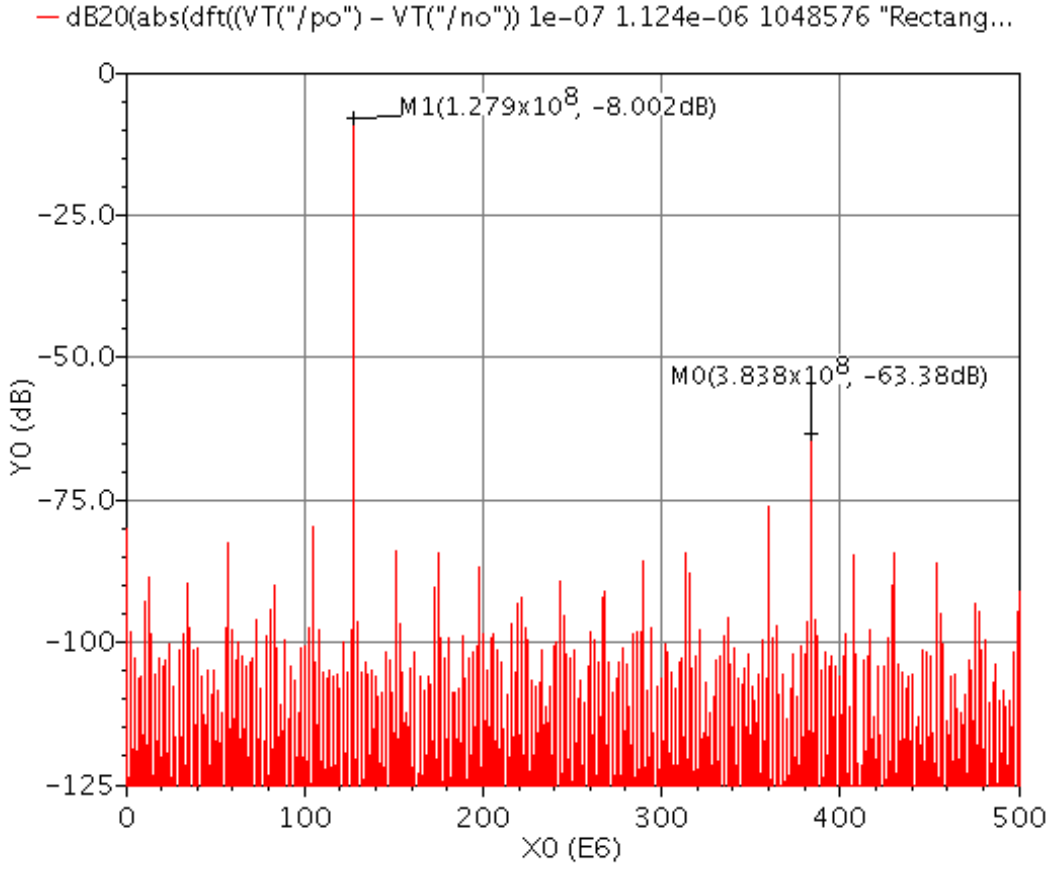


Figure 2.9: Simulated Spectrum with sample rate 1GS/s switches size W=1.44um L=0.24um and SFDR 55.3dB.

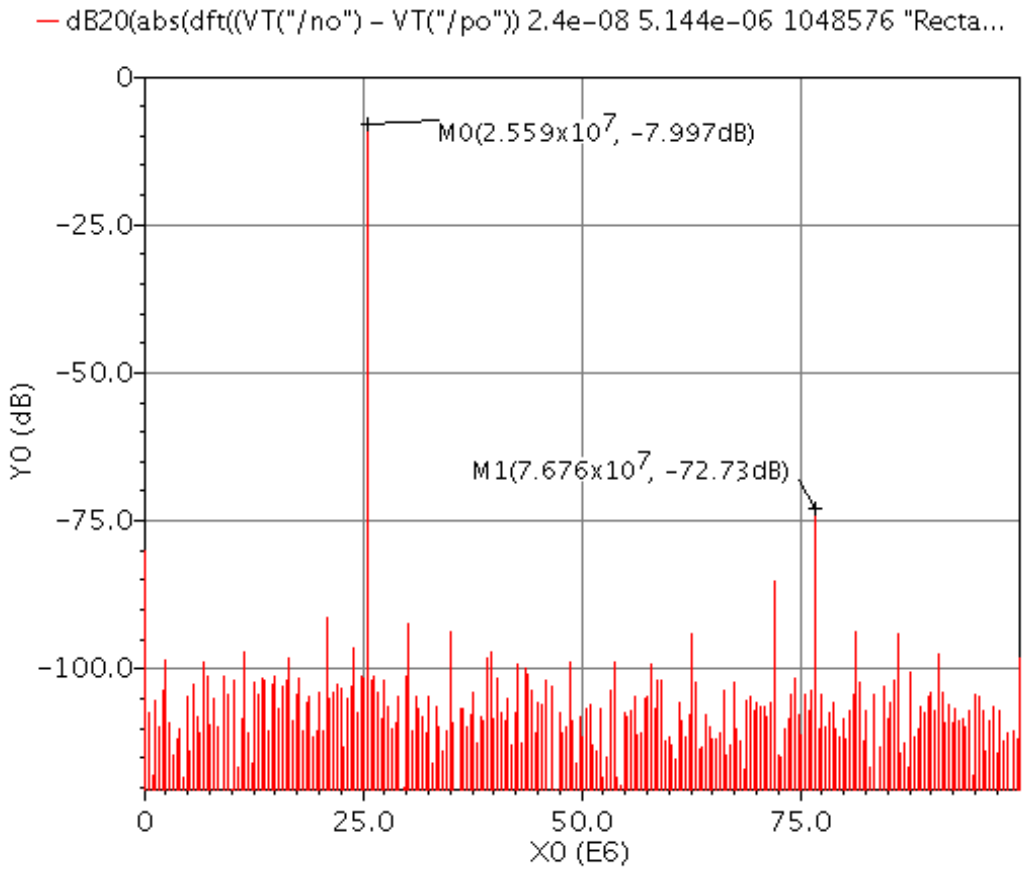


Figure 2.10: Simulated Spectrum with sample rate 200MS/s switches size W=2.44um L=0.24um and SFDR 64.7dB.

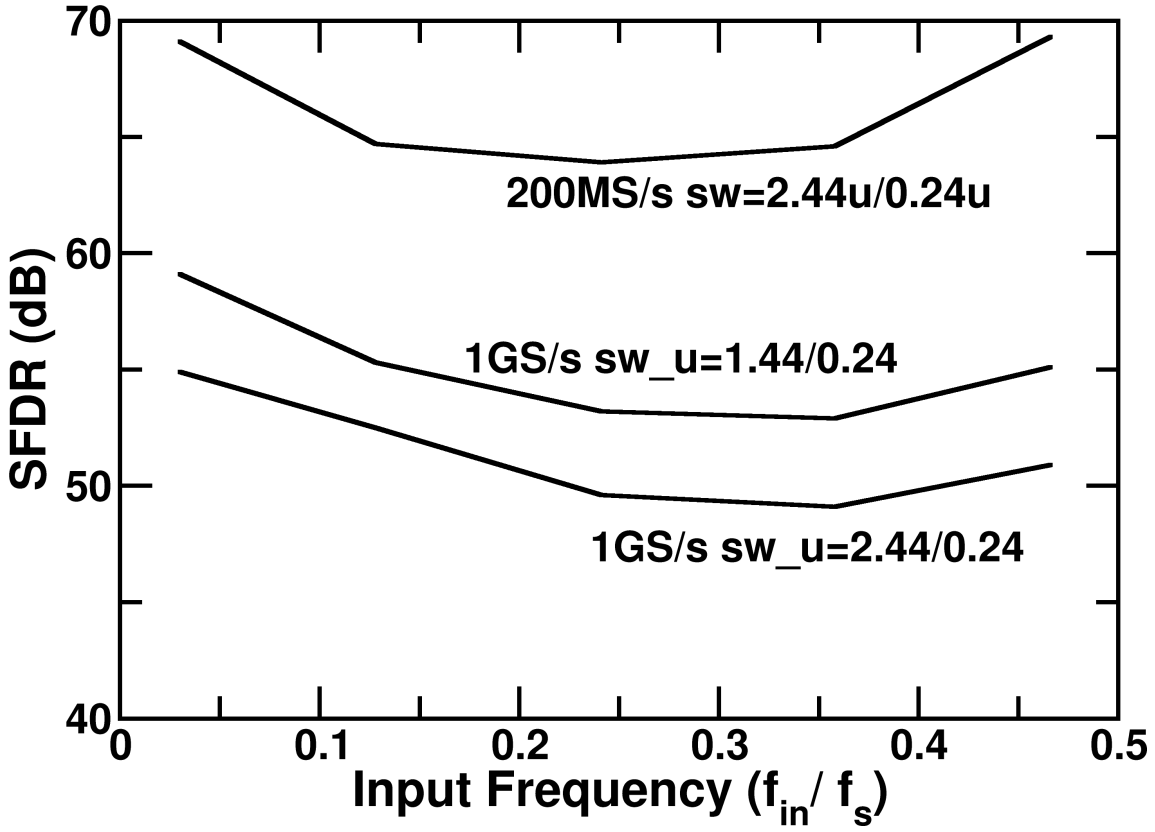


Figure 2.11: SFDR summary of different switch sizes and sampling rates.

matching property if the DAC is designed with calibration. The matching property equation Equation (2.2), where $\sigma^2_{\frac{\Delta I}{I}}$ is the standard deviation of mismatch current of two current cells, A_{VT} is the foundry parameter to model the variation of threshold voltage and A^2_β is for the size dimension.

$$\sigma^2_{\frac{\Delta I}{I}} = \frac{1}{W \cdot L} \cdot (\frac{4A^2_{VT}}{V_{ov}} + A^2_\beta) \tag{2.2}$$

From the equation, we can know that the increasing 1 bit resolution the area is 4 times larger. That is, the core area of the DAC is growing. Therefore, the imbalance of the clock line becomes serious. The layout of clock line must be tree shaped for timing synchronization. However, buffer in the clock tree may be with variation and wire loading may be different, resulting in clock skew. The clock delay for each current cells are invariant. In other words, the clock skew is cell-dependant, also called code-dependant, and will result in harmonic distortion. We run simulation based on the 12-bit DAC with 6-6 segmentation to examine the impact of clock skew. Assume that, 3 out of the 63 equally weighted MSB cells are suffered with clock skew of 10psec. And the DAC current cells are all ideal devices including switches, resistors and current sources. Figure 2.12 shows that the black line is the spectrum of DAC output without clock skew, and the yellow color one is the spectrum of DAC output with clock skew. It's clearly, that the clock skew induces harmonic distortions. In Figure 2.13, x axis is sampling frequency and y axis is SFDR. The upper line is the SFDR of DAC with lower output frequency. When the sampling clock, Fs, is 250 MHz, the lower output frequency of 0.03Fs is with a 90dBc of SFDR and the higher one of 0.36Fs is 82dBc. Because the clock skew is cell-dependant, the high frequency input will have more switching switches. As the sampling frequency increased, the SFDR of the both line drops dramatically due to the shorter clock period.

Switch driver mismatch

Switch driver mismatch may result in different rising time and falling time or asymmetry rising/falling time [39, 28]. Then, the glitch area or glitch energy becomes cell-dependant. This phenomenon is severe for the high-speed DAC since the glitch area of one sampling period increases with the sampling frequency. Next, we run a simulation by a 12-bit DAC with 6-6 segmentation. The simulation condition is with ideal current sources and behavioral switch drivers. By setting different driving strength of the switch

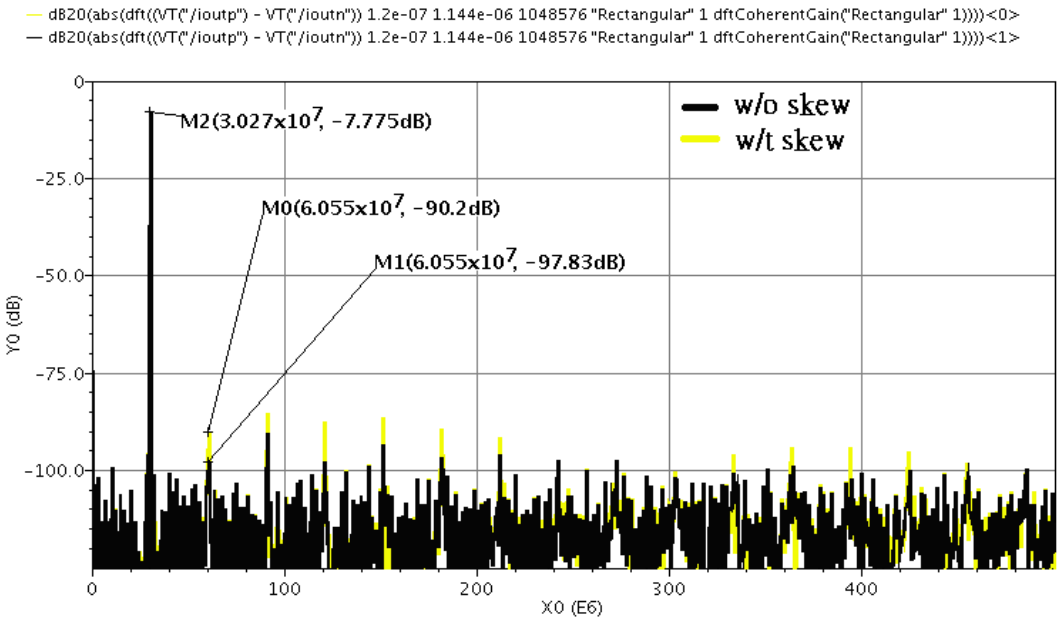


Figure 2.12: 3 cells out of 63 with 10ps clk skew.

drivers, we can see the spectra shown in Figure 2.14. There is one driver with a weak driving strength of 80ps and others are with driving strength of 50ps. The resulting spectra show that the switch driver mismatch also causes harmonic distortion since they are cell-dependant.

Current Switch mismatch

Device mismatch is usually considered in discussions of static linearity [31] mentioned that device mismatch also contributes to dynamic nonlinearity because switching behavior is dependent on switch transistor parameters such as threshold voltage and oxide thickness. These differences of devices introduce code dependencies in the switching transients. The effect of threshold voltage mismatch would be like the current cells with clock skew, and the skews will cause harmonic distortions. Moreover, the current switch mismatch causes different code-dependent settling time constants.

Voltage fluctuation at internal switch node

The internal source coupled node of the current switch should be carefully designed since the fluctuation at the internal node directly impacts the output current. During the

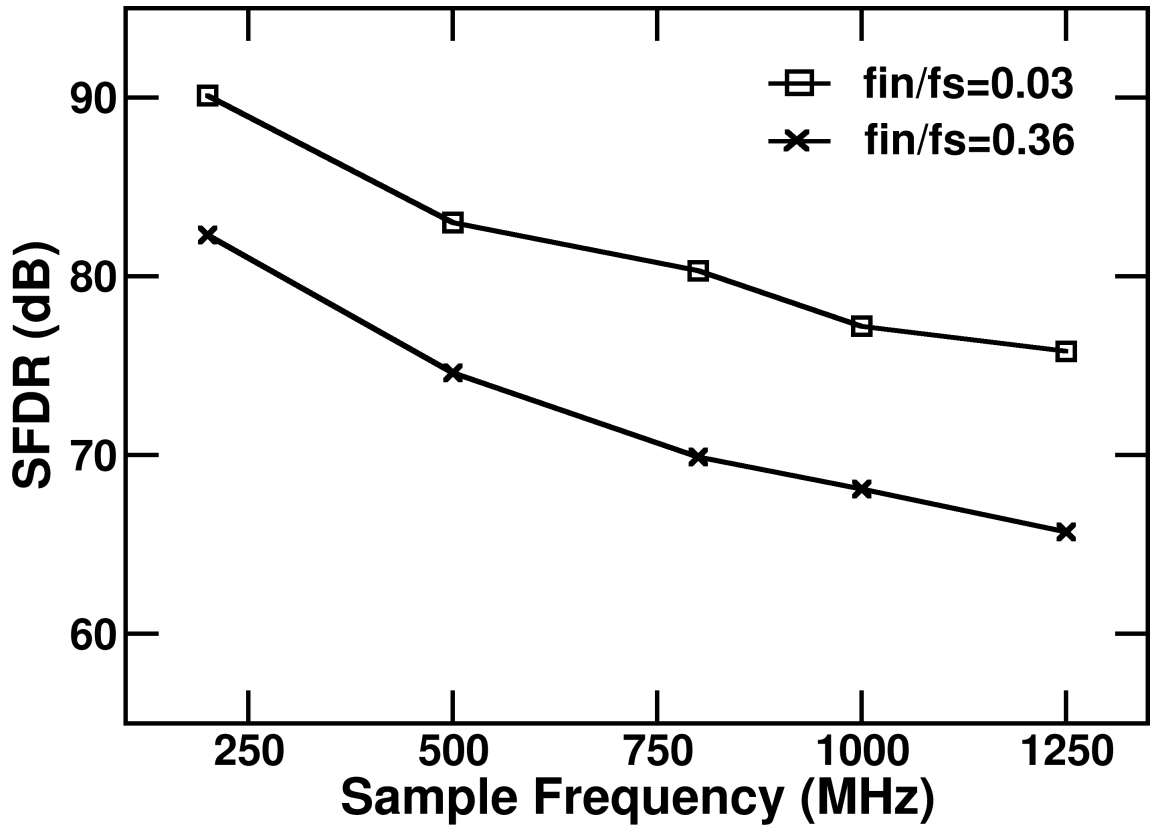


Figure 2.13: 3 cells out of 63 with 10ps clk skew.

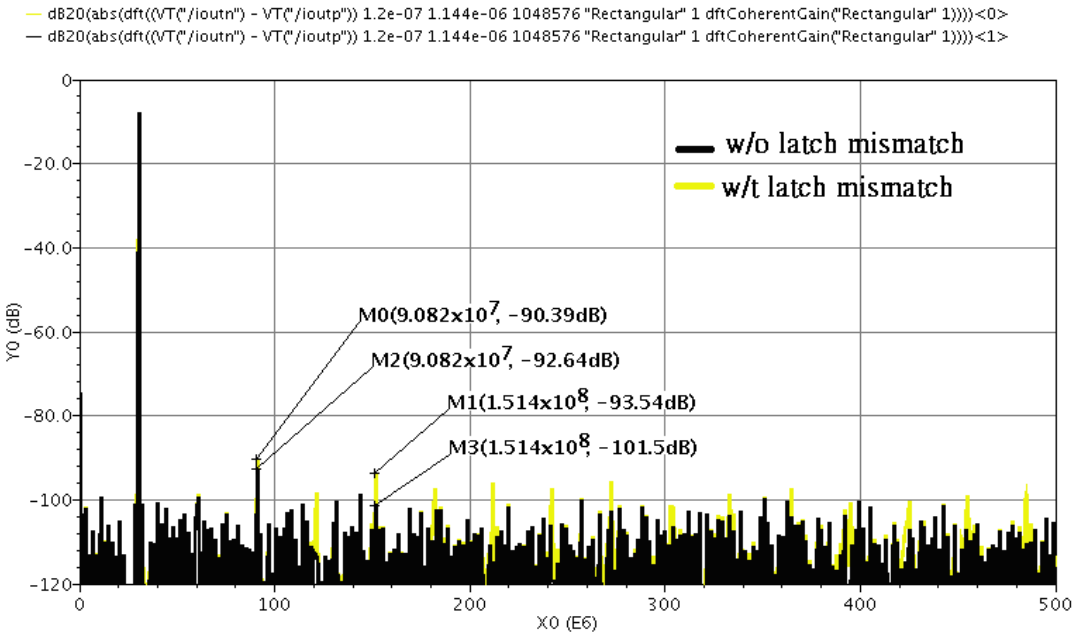


Figure 2.14: Spectra of the DAC's output signal. 6-6 segmentation only one latch with weak driving strength of 80ps of rising/falling time and others with 50ps.

switching transient, the internal node voltage fluctuation depends on the cross point of control signal [1, 40, 30, 41]. If the MOSFETs of switch pair are all off simultaneously, the current source will enter triode region and a large voltage fluctuation at internal node until one of the switch MOSFET is turn on. As shown in Figure 2.15, in a NMOS current sources of DAC shown in Figure 2.7, the latch's differential output cross-point dominate the voltage fluctuation of the internal node. This phenomenon will induce both harmonic distortions and noise. Since the amplitude of the voltage fluctuation is direct proportion to switching current cells and the number of switch cells is $D_i[n] - D_i[n-1]$, it's the digital input filtered by a high pass filter. And this fluctuation becomes serious at high output frequency.

Major carry glitch

The advantage of such binary-weighted DAC is its simplicity and no decoding logic is required, but it's suffered by large major carry glitch at the mid-code transition [2]. The most significant bit (MSB) current source needs to be matched to the sum of all the other

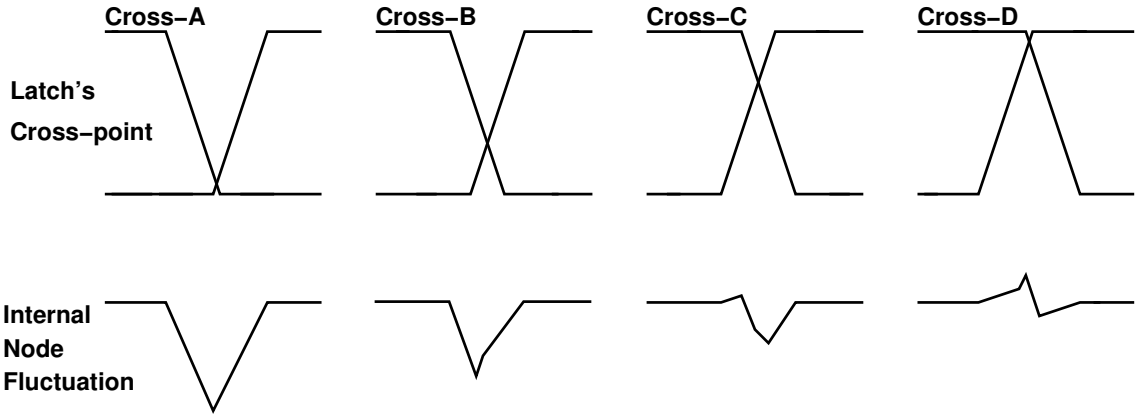


Figure 2.15: The latch's differential output cross-point dominate the voltage fluctuation of the internal node.

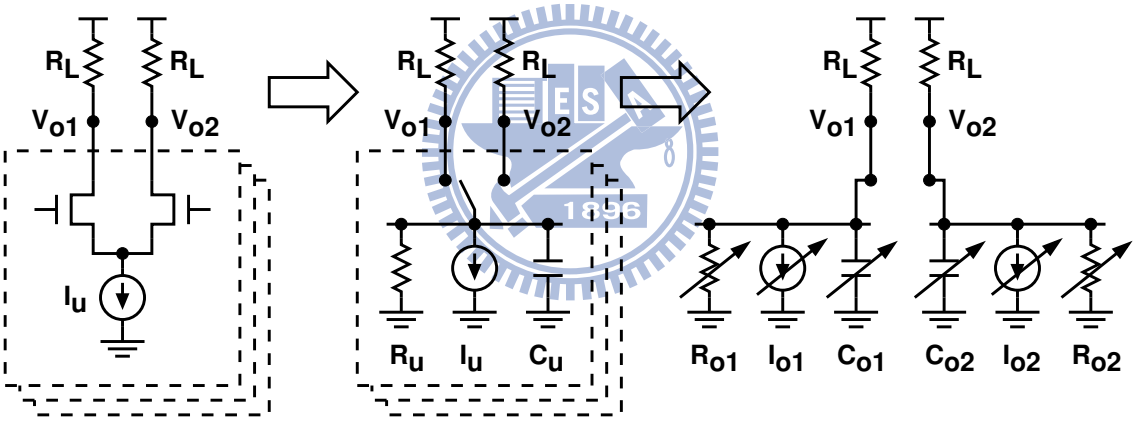


Figure 2.16: Code-dependent loading variation (CDLV).

current sources to within 0.5 LSB's (least significant bits). That is, the maximum DNL locates at the mid-code transition. The miscode glitch contains highly nonlinear signal components and will manifest itself as spurs in the frequency domain. Thermometer weighted DAC can avoid this major carry glitch, but the cost is unacceptable for high resolution DACs. The DACs are designed with less major carry glitch and lower cost than thermometer weighted by segmentation. The degree of segmentation influence on both the structure of the converter and on its performance.

2.4 Code-dependant Loading Variation (CDLV)

Figure 2.16 shows another source of harmonic distortion. Each current cell is modeled as an ideal switch on top of an ideal current source I_u in parallel with a resistor R_u and a capacitor C_u. The resistor R_u represents the output resistance of the current source. The capacitor C_u represents the capacitance associated with the output node of the current source, including the gate capacitance of the current switch. Both R_u and C_u are connected to either the V_{o1} node or the V_{o2} node, depending on the state of the switch. As a result, the total loadings for output nodes V_{o1} and V_{o2} vary with digital input $D_i[k]$. This code-dependent loading variation (CDLV) effect introduces harmonic distortion in the differential output $V_o = V_{o1} - V_{o2}$. When $D_i[k]$ is a sinewave, the 3rd-order harmonic distortion caused by the CDLV effect is [42, 43, 34, 12]

$$\text{HD3} = \left[\frac{M}{4} \cdot \frac{R_{L,d}}{|Z_u|}\right]^2 \tag{2.3}$$

where M is the total number of current cells, $R_{L,d} = 2R_L$ is the differential resistance of the DAC output loads, and Z_u is the output impedance of a single current cell, where

$$\frac{1}{Z_u} = \frac{1}{R_u + j\omega C_u}. \tag{2.4}$$

In single-ended application, the CDLV would cause second harmonic distortion

$$HD2 = -20log\left[\left(\frac{MR_L}{4Z_u + 2MR_L}\right)\right] \tag{2.5}$$

For NMOS DAC shown in Figure 2.17, the Z_u in Equation (2.4) is the output impendence look into the current cell. The simulated results of Z_u is drawn in Figure 2.18. The Z_o is dominated by R_u at low frequency, as the frequency is increased then Z_u is dominated by C_u. The slope of Z_o versus frequencies in log scale is -1. If the DAC is 12-bit with 6-6 segmentation, there are 63 MSB's current cells and 6 LSB's current cells which can be treated as one MSB cell. In other words, M is 64 in Equation (4.1). Assume that $R_{L.d}$ is 50 Ω. The -70 dB HD3 requirement is that Z_u must larger than 45 $k\Omega$. Refer to the Figure 2.18, the Z_u is 45 $k\Omega$ at output frequency equal to 84 MHz. The -70dB HD3 bandwidth is limited by the large C_u. For the 12-bit, 6-6 segmentation DAC, Figure 2.19 shows the required output impedance versus specified SFDR. If the target SFDR is higher,

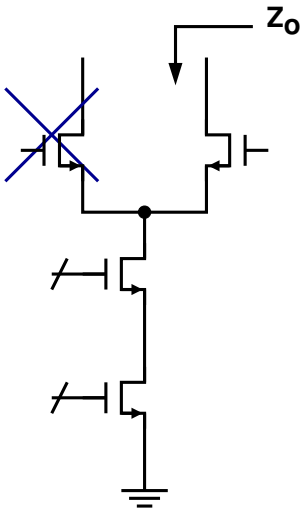


Figure 2.17: Z_u is the simulated output impedance of one current cell when one switch is off.

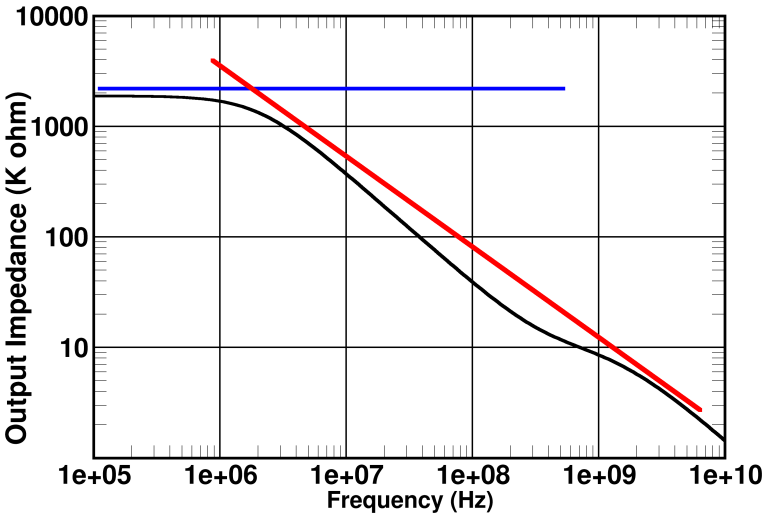


Figure 2.18: The frequency response of Z_u

output impedance requirement is more strict. In Figure 2.21, we also plot the limitation of HD2 and HD3 which are described in Equation (2.5) and Equation (4.1).

The equation describes the maximum single-end INL at middle code [44].

$$INL = \frac{I_{unit} R_L^2 M^2}{4 R_{out}} \tag{2.6}$$

This is the CDLV effect in static performance. If the INL of DAC is specified to 0.5 LSB, the required output impedance can be obtained from the equation Equation (2.6). The required impedance of different resolutions are plotted in Figure 2.21 [42, 43]; nevertheless, the required impedance challenge is not for static linearity since the impedance is easy to be reached.

As shown in Table 2.4, segmentation does not impact the output impedance requirement. For example, a 12-bit DAC with 7-5 segmentation needs 90 $K\Omega$, and the unit current cell needs 2.88 $M\Omega$. However, 12-bit DAC with 4-8 segmentation has the same impedance requirement for the unit current cell.

Increasing R_u and reducing C_u can mitigate the CDLV effect. Adding cascode stage to a current source can increase R_u. In most designs, the CDLV effect at high frequencies

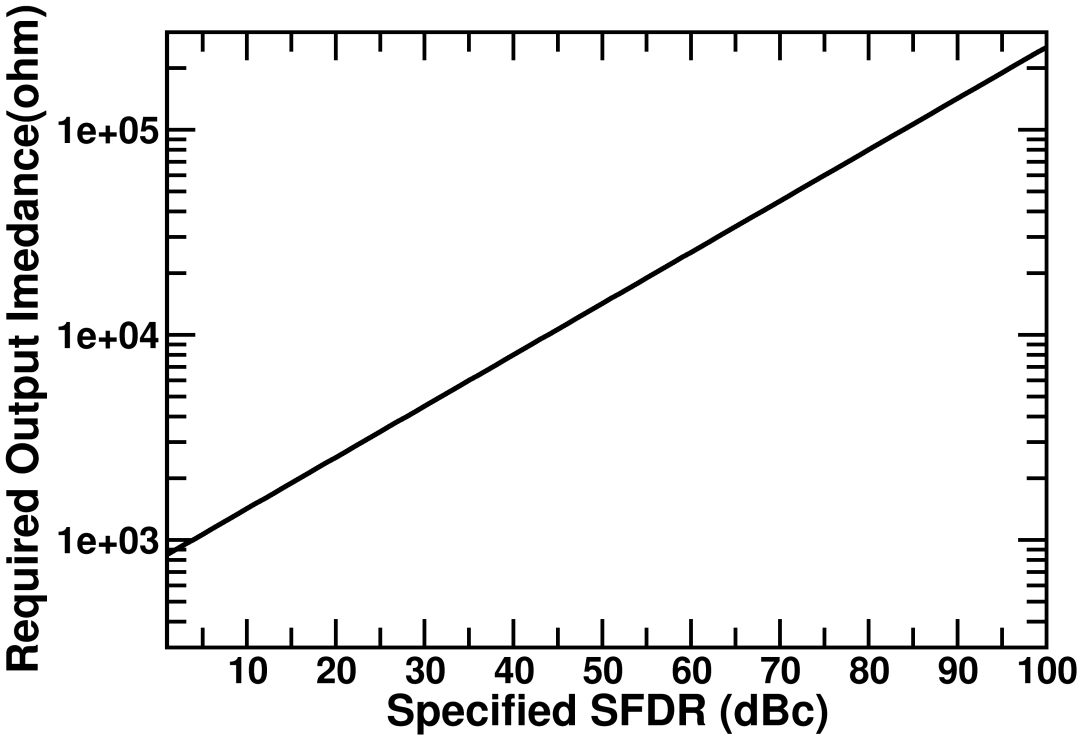


Figure 2.19: The required output impedance versus specified SFDR for 12-bit DAC. The degree of segmentation does not influence the output impedance requirement.

Table 2.4: Different segmentations for —HD3—=70dB

Seg.	M	$R_{out,MSB}$	I_{MSB}	INL	DNL	λ	V_{ov}	MSBsize	$R_{out,unit}$
7-5	128	90KΩ	$I_f/128$	64σ	8σ	λ	V_{ov}	$32\frac{W}{L}$	$2.88M\Omega$
6-6	64	45KΩ	$I_f/64$	64σ	$8\sqrt{2}\sigma$	λ	V_{ov}	$64\frac{W}{L}$	$2.88M\Omega$
5-7	32	22.5KΩ	$I_f/32$	64σ	16σ	λ	V_{ov}	$128\frac{W}{L}$	$2.88M\Omega$
4-8	16	11.25KΩ	$I_f/16$	64σ	$16\sqrt{2}\sigma$	λ	V_{ov}	$256\frac{W}{L}$	$2.88M\Omega$

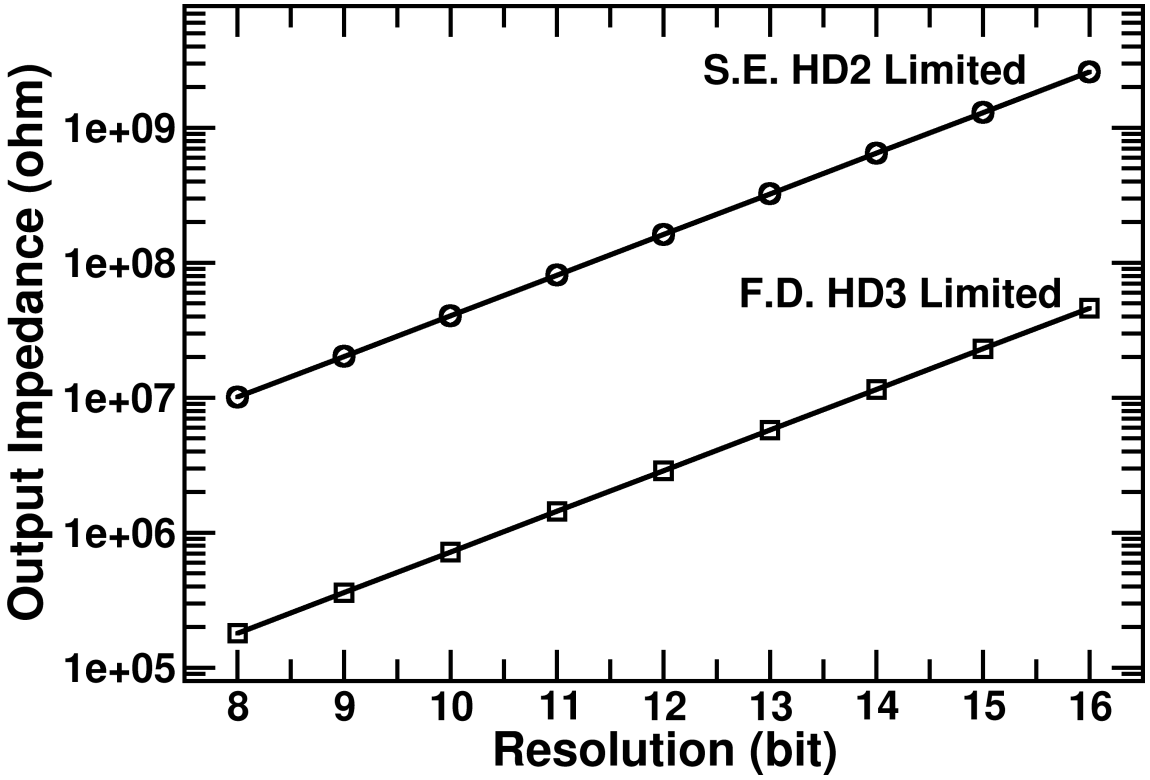


Figure 2.20: Output impedance requirement of unit current cell vs. bit number of DAC. The CDLV caused HD2, HD3 must larger than 70dB and R_L is 50ohm.

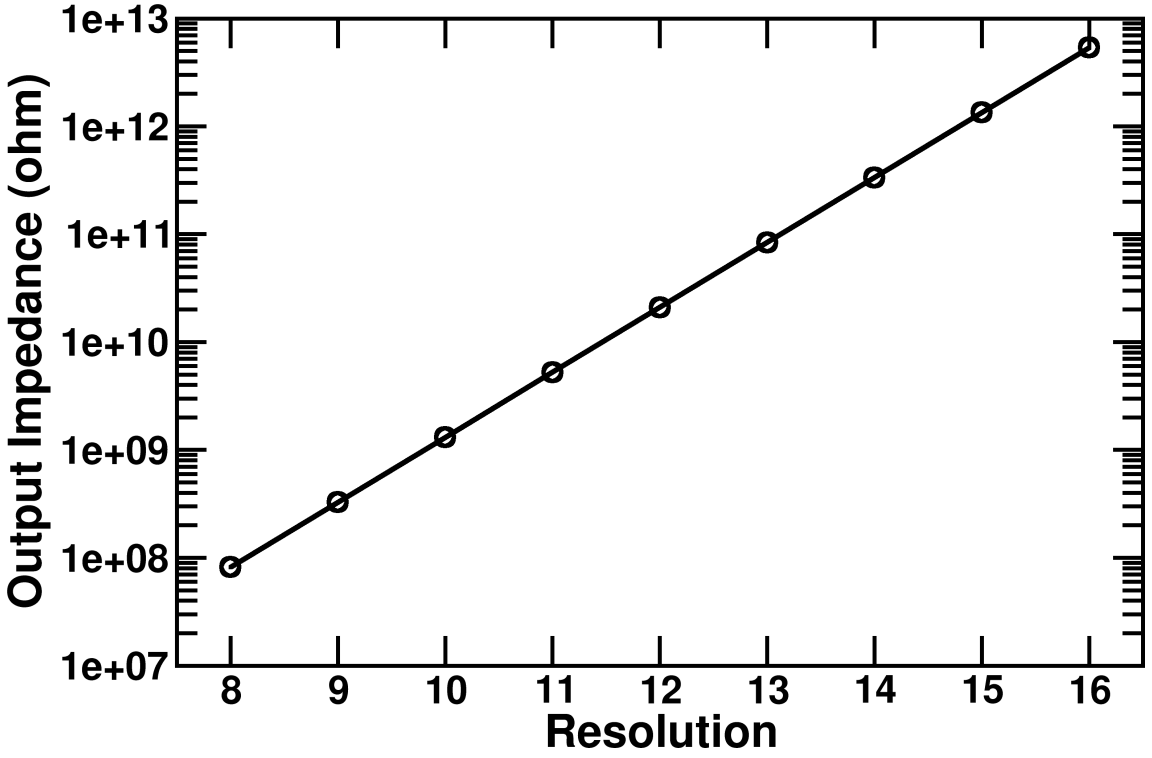


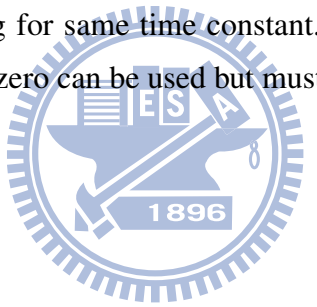
Figure 2.21: Output impedance requirement of unit current cell vs. bit number of DAC. The single ended INL caused by CDLV must small than 0.5LSB and R_L is 50ohm.

is dominated by C_u. The C_u capacitance is determined by the device dimensions of the current switch and the current source, while the device dimensions are governed by the matching requirements.

The CDLV effect can be mitigated by adding an additional cascode stage following the current switch in each current cell [33, 7, 34]. The MOSFETs in those cascode stages need to have large transconductances to achieve good high-frequency performance [34, 12].

2.5 Summary

In this section, we discuss most of the design considerations for high speed current-steering DACs. The key point is to reduce the parasitic loading on the signal path for high signal bandwidth. And carefully chose the size of switch, cross point the switches, layout matching and tree-shape routing for same time constant. Moreover, techniques such as calibration, DEM and return-to-zero can be used but must evaluate the extra penalty.

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Chapter 3

A 8-Bit 1.6 GS/s 90 nm CMOS DAC

3.1 Introduction

The current-steering digital-to-analog converts (DACs) can achieve high sampling rate, and thus are commonly used in generating high-frequency signals [6, 1, 7, 10, 34]. Figure 3.1 shows a generic current-steering DAC. It consists of M equally-weighted current cells. Each current cell contains a current source of I_u output current, a p-channel MOSFET pair functioning as a current switch, and a digital latch controlled by a clock CK. The complementary outputs of the latch control the current switch, directing the I_u current to either the R_L load at V_{o1} or the one at V_{o2}. A decoder converts the DAC digital input $D_i[k]$ into M thermometer-code signals $B_j[k]$, where $1 \leq j \leq M$, such that $D_i[k] = \sum_{j=1}^{M} B_j[k]$. The $B_j[k]$ signal has a binary value of either $+1$ or -1. Figure 3.2 illustrates the DAC differential non-return-to-zero (NRZ) output waveform $V_o = V_{o1} - V_{o2}$. The V_o has a voltage range between $+MI_uR_L$ and $-MI_uR_L$, and a step size of $2I_uR_L$.

The DAC static linearity, specified as differential nonlinearity (DNL) and integral nonlinearity (INL), is mainly determined by the matching of I_u among different current cells and the output resistances of the I_u current sources. There are techniques to improve the static linearity, which will not be covered in this section. However, even with ideal I_u current sources, dynamic nonlinearity still occurs. It is manifested as spurious-free dynamic range (SFDR) degradation shown in the V_o output spectrum when the $D_i[k]$ input is a single-tone sinewave. The SFDR decreases rapidly with increasing input fre-

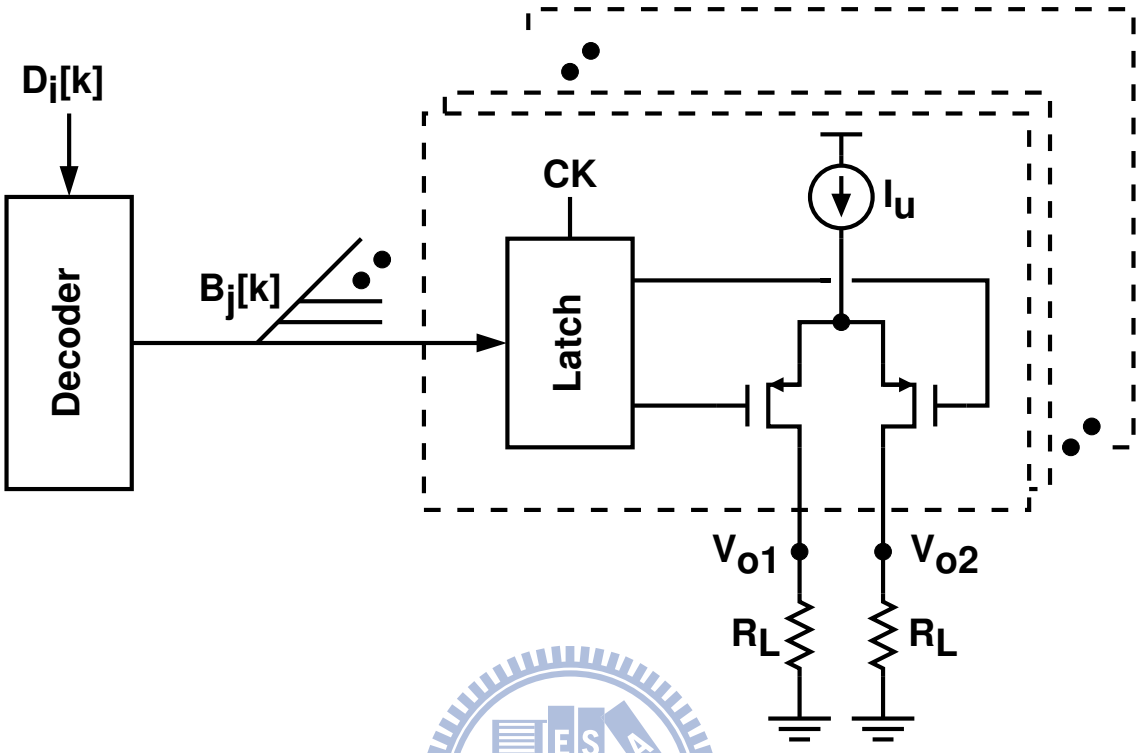

Figure 3.1: A current-steering DAC.

quency. The sources of dynamic nonlinearity are numerous and complex, including code-dependent switching transients [31, 38] and capacitive output impedance of the current cells [42, 34, 43].

The return-to-zero (RZ) technique has been proposed to improve the DAC dynamic performance [31, 15, 18]. The technique adds an output buffer to isolate the output loads from the current switches and executes current switching operation during the zero phase. The DAC dynamic performance can also be improved by modifying the current switching operation to make the switching transients uncorrelated with the input sequence [45, 1, 24].

In this section, we propose a digital random return-to-zero (DRRZ) technique to mitigate the effect of switching transients on the DAC dynamic performance. A 8-bit 1.6-GS/s current-steering DAC chip was designed to demonstrate the proposed technique.

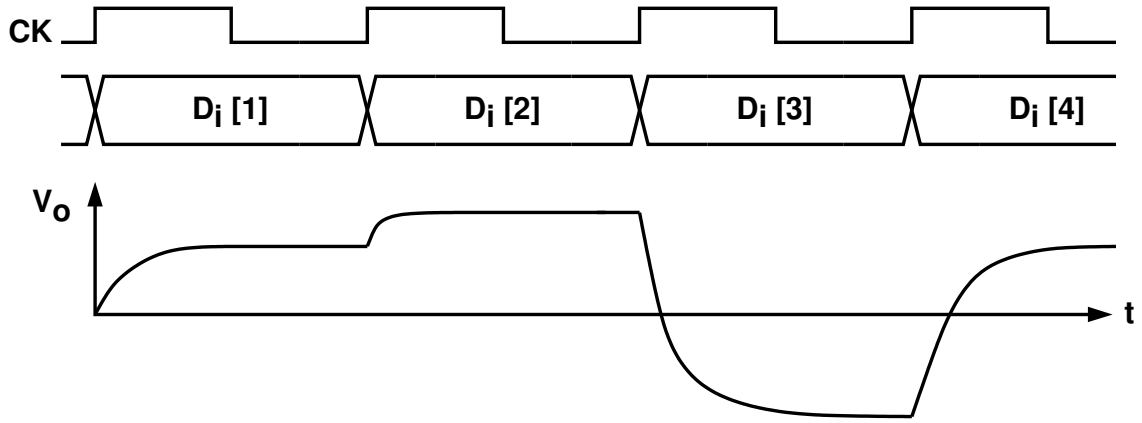

Figure 3.2: Non-return-to-zero (NRZ) output waveform of a current-steering DAC.

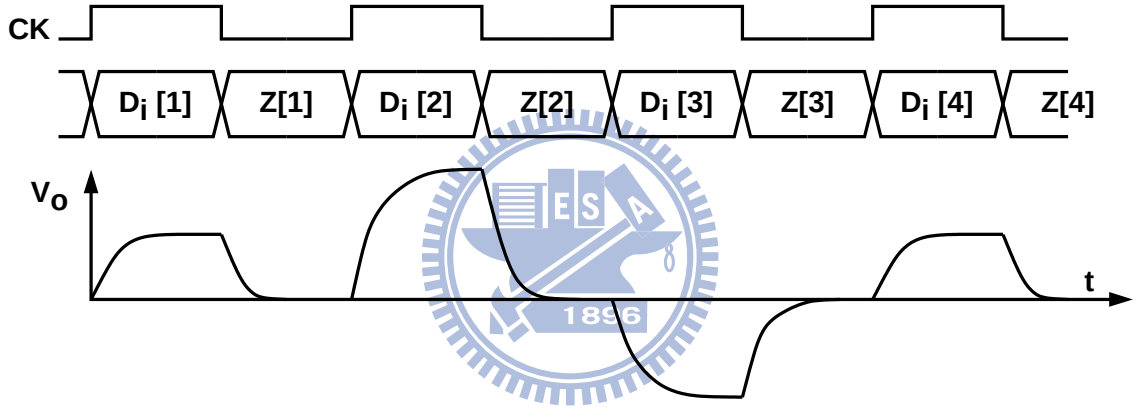

Figure 3.3: Waveforms of a return-to-zero (RZ) DAC.

3.2 Digital Random Return-to-Zero (DRRZ)

Consider the j-th current cell of the DAC shown in Figure 3.1. Its current switch is driven by $B_j[k] \in \{-1, +1\}$. When CK changes from low to high, the current switch may remain unchanged or undergo a (-1)-to-$(+1)$ switching or a $(+1)$-to-(-1) switching. When the current switch makes a switching, the DAC output V_o experiences a transient disturbance called switching transient. The (-1)-to-$(+1)$ switching transient and $(+1)$-to-(-1) switching transient have opposite polarities. For the NRZ DAC, the switching of the current cells is determined by the input $D_i[k]$. Thus, the switching transients are input-dependent and will result in DAC dynamic distortion.

Analog return-to-zero (ARZ) has been used to hide the switching transients from the

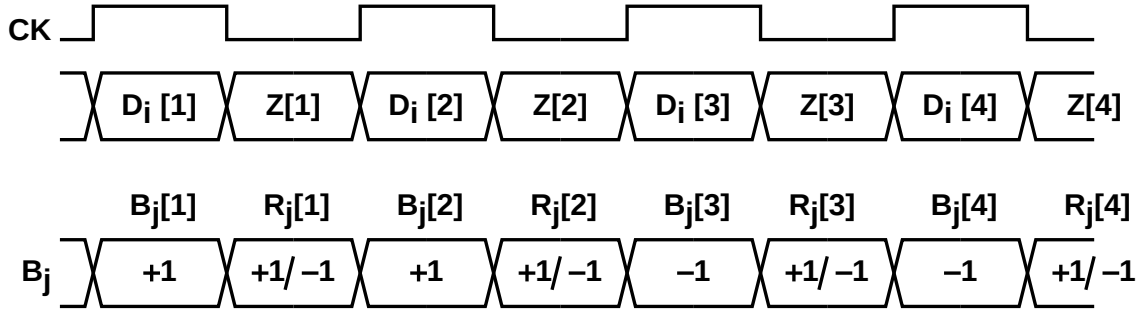

Figure 3.4: Switching behavior of a current cell in a digital return-to-zero (DRZ) DAC or a digital random return-to-zero (DRRZ) DAC.

output [31, 15, 18]. The CK and V_o waveforms of Figure 3.3 show the ARZ operation. When CK is high, the DAC is in the data phase. It decodes the digital input $D_i[k]$, sets up its internal current switches, and generates an analog output V_o corresponding to $D_i[k]$. When CK is low, the DAC is in the zero phase. The DAC output V_o is forced to zero by analog switches added at output nodes V_{o1} and V_{o2}. The current switches in the DAC are switched to reflect the next input $D_i[k+1]$ during the zero phase. Thus, the switching transients do not appear in V_o to contribute dynamic distortion. The analog switches at the output nodes must be large enough to eliminate switching transients.

We can generate the RZ V_o waveform without using the analog switches at the output nodes. As shown in Figure 3.3, when CK is low, the DAC is in a zero phase, $Z[k]$, in which the DAC arranges its internal current switches in such a way that output $V_o = 0$. In the $Z[k]$ state, the switch controls, $B_j[k]$, are reset to pre-defined values such that $\sum_{j=1}^{M} B_j[k] = 0$, assuming M is an even number. However, in this digital return-to-zero (DRZ) setup, switching transients appear in V_o. Consider the j-th current cell. The sequence of its switching control, B_j, is shown in Figure 3.4. When CK is high, $B_j = B_j[k]$ is determined by the input $D_i[k]$. When CK is low, $B_j = R_j[k]$ is a fixed value of either $+1$ or -1. In Figure 3.4, $B_j[1] = +1$ and $B_j[2] = +1$ have the same value. If $R_j[1] = +1$, there will be no switching during the $Z[1]$ period. If $R_j[1] = -1$, there will be a $(+1)$-to-(-1) and a (-1)-to-$(+1)$ transients on both edges of the $Z[1]$ period. Also shown in Figure 3.4, $B_j[2] = +1$ and $B_j[2] = -1$ have different values. If $R_j[2] = +1$, a $(+1)$-to-(-1) transient occurs at the right edge of the $Z[2]$ period. If $R_j[2] = -1$, a $(+1)$-to-(-1) transient occurs at the left edge of the $Z[2]$ period. In summary, the DRZ assigns

a constant to $R_j[k]$, i.e., $R_j[k] = +1$ for all k or $R_j[k] = -1$ for all k. The current switch transitions are determined by the $B_j[k]$ sequence alone. Their strong correlation with the input $D_i[k]$ yields distortion in V_o. The DRZ in fact introduces more input-dependent switching transients than the NRZ.

We propose the digital random return-to-zero (DRRZ) technique to randomize the switching transients appearing in DRZ. In this scheme, the switch controls $B_j[k]$ in the $Z[k]$ phase are dictated by a pseudo random number generator (PRNG), such that $\sum_{j=1}^{M} B_j[k] = 0$. Consider the j-th current cell and the operation sequence shown in Figure 3.4. When CK is high, $B_j = B_j[k]$ is determined by the input $D_i[k]$. When CK is low, $B_j = R_j[k]$ becomes a binary random variable which has a value of either $+1$ or -1. In Figure 3.4, $B_j[1] = +1$ and $B_j[2] = +1$ have the same value. Switch transitions occur only if $R_j[1] = -1$. Also shown in Figure 3.4, $B_j[2] = +1$ and $B_j[2] = -1$ have different values. A switch transition occurs at the right edge of the $Z[2]$ period if $R_j[2] = +1$. On the other hand, a switch transition occurs at the left edge of the $Z[2]$ period if $R_j[2] = -1$. In summary, the DRRZ makes $R_j[k]$ a random sequence, which randomizes the current switch transitions. When the switching transients are not correlated with the input $D_i[k]$, they appear as noises in V_o and will not cause distortion.

3.3 Circuit Descriptions

Figure 3.5 shows the block diagram of the 8-bit DAC. It is segmented into a 5-bit equally-weighted MSB DAC (M-DAC) and a 3-bit binary-weighted LSB DAC (L-DAC). The M-DAC comprises 31 identical current cells. Each current cell can output an current of $8I$, where I is the DAC unit current. The L-DAC comprises 4 current cells which output an current of $1I$, $1I$, $2I$, and $4I$ respectively. There are two $1I$ current cells in the L-DAC so that a differential output of zero can be realized. The node I_{o1} and node I_{o2} of all current cells are tied together respectively to form the two differential DAC output terminals. The two output terminals are connected to two R_L resistors to generate the differential V_o as illustrated in Figure 3.1. When CK is high, the decoder controls both the M-DAC and the L-DAC. The current of the extra 1I current cell in the L-DAC is always directed to the I_{o1} node. The DAC output is expressed as $V_o[k] = (D_i[k] - 127) \times 2IR_L$, where $D_i[k]$

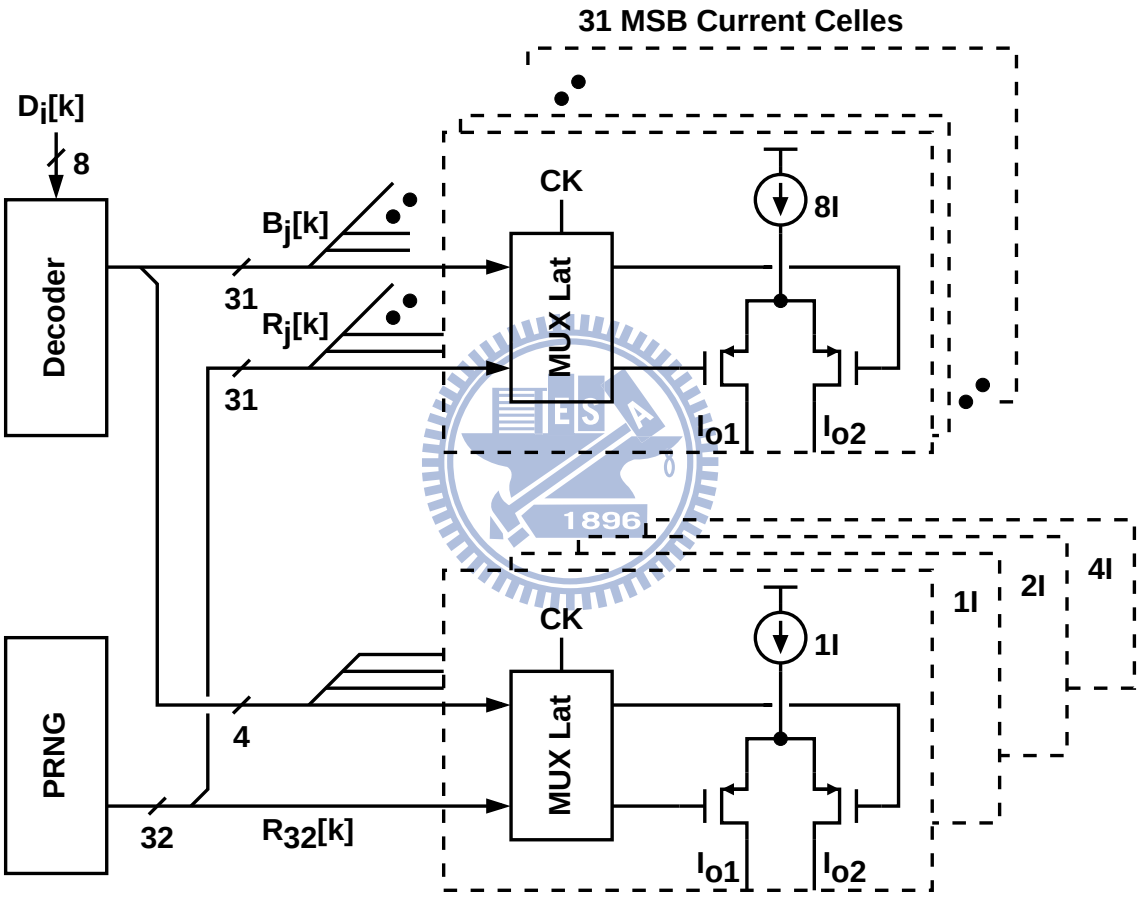

Figure 3.5: DAC block diagram.

is an integer from 0 to 255. In our design, $I = 80\ \mu$A and $R_L = 25\ \Omega$ yield a V_o with a differential signal range of 1 V_{pp}.

In this work the devices were sized to fit the 8-bit linearity by matching equation Equation (3.1).

$$\sigma^2_{\frac{\Delta I}{I}} = \frac{1}{2} \times \frac{1}{W \cdot L} \cdot (\frac{4A^2_{VT}}{V_{ov}} + A^2_{\beta}) \tag{3.1}$$

For 8-bit with 5-3 segmentation, LSB = 1 2 4, MSB = 8 8 8 ...

INL (max)	$\sqrt{256}\sigma$	$\leq 0.5LSB$
DNL(max)	$\sqrt{16}\sigma$	$\leq 0.5LSB$

$$1 \times \sqrt{256}\sigma \leq 0.5$$

$$\sigma \leq 3.125 \times 10^{-2}$$

$$2 \times (3.125 \times 10^{-2})^2 \times WL_{unit} \geq 4 \cdot \frac{5.81^2}{V_{ov}^2} + 0.0162^2$$

V_{ov} (mV)	100	150	200	250	300	350
WL_{unit} $(um^2)(1\sigma)$	14.1/2	6.4	3.7	2.5	1.8	1.1
WL_{unit} $(um^2)(3\sigma)$	127/2	57.6	33.3	22.5	16.2	9.9

σ	×1.0	×1.4	×1.6	×1.8	×2	×2.2	×2.4	×2.6	×2.8	×3.0
yield	68.3	77.0	83.8	89.0	92.8	95.4	97.2	98.4	99.1	99.7

As shown in Figure 3.5, each current cell contains a multiplexing latch. When CK is high, the latch selects the $B_j[k]$ control from the $D_i[k]$ decoder for normal DAC output. When CK is low, the latch selects the $R_j[k]$ control from a PRNG. The PRNG is a 16-bit linear feedback shift register. Its 16 outputs and their complements form the 32 $R_j[k]$ zero-phase controls. This arrangement ensures that $\sum_{j=1}^{32} R_j[k] = 0$. During the zero

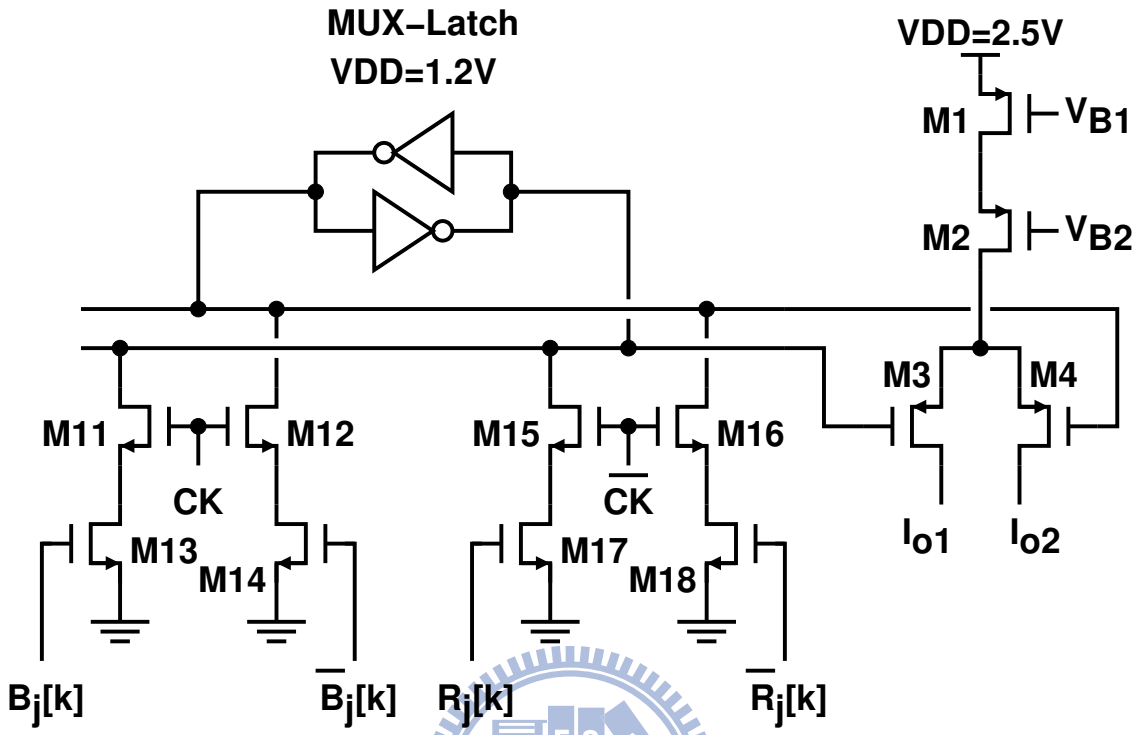

Figure 3.6: Current cell schematic.

phase, the entire L-DAC is treated as a single MSB current cell controlled by a single $R_{32}[k]$ signal.

Figure 3.6 shows the circuit schematic of a current cell. MOSFETs M1 and M2 form a cascode current source. M3 and M4 together function as a current switch. The current source is operated under a 2.5 V supply. M1–M4 are MOSFETs with thick gate oxide. MOSFETs M11–M18 and the two inverters form a level-sensitive MUX-latch. When CK is high, the $B_j[k]$ signal is loaded into the latch. When CK is low, the $R_j[k]$ signal is loaded into the latch. The MUX-latch is operated under a 1.2 V supply.

As shown in Figure 3.7 sine-wave was translated to fully differential by off-chip transformer, and a internal differential to single ended amplifier was used before flip-flop which divided the clock by two. With the division function, duty cycle of clock is near to fifty percentages to avoid timing error between digital and analog interface. The digital circuit dealt with data phase signal at rising edge of digital clock and zero phase signal at the falling edge. The analog clock was above 180 degree differ from digital clock; therefore, level-sensitive MUX-Latch could catch the proper digital signal. For measurement,

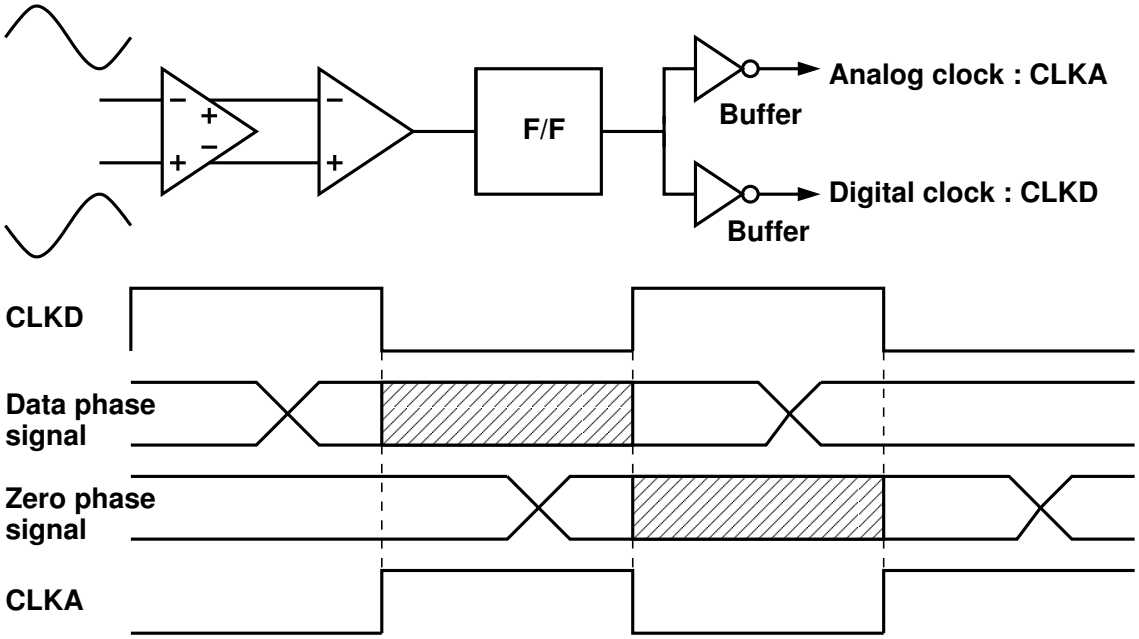

Figure 3.7: Clock buffer and interface timing between digital and analog

a direct digital frequency synthesizer (DDFS) was imbedded. All the digital part were implemented by synthesis and auto place and route.

3.4 Experimental Results

The DAC was fabricated in a standard 90 nm CMOS technology. Figure 3.8 shows the chip photograph. The DAC core area is 400×400 μm^2. The chip also includes a direct digital frequency synthesizer (DDFS) to generate digital inputs for DAC testing. Figure 3.9 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the DAC. The DNL is $+0.04/-0.03$ LSB and the INL is $+0/-0.2$ LSB.

Figure 3.10 and Figure 3.11 show the output spectra of the DAC operating at 1.6 GS/s sampling rate, and the input frequency is 107 MHz. For Figure 3.10, the DRRZ function is turned off, and the DAC output waveform is similar to the NRZ V_o waveform shown in Figure 3.2. For Figure 3.11, the DRRZ function is turned on, and the DAC output waveform is similar to the RZ V_o waveform shown in Figure 3.3. There are no significant harmonic tones in both figures. The measured SFDR is 65.4 dB for the NRZ DAC and

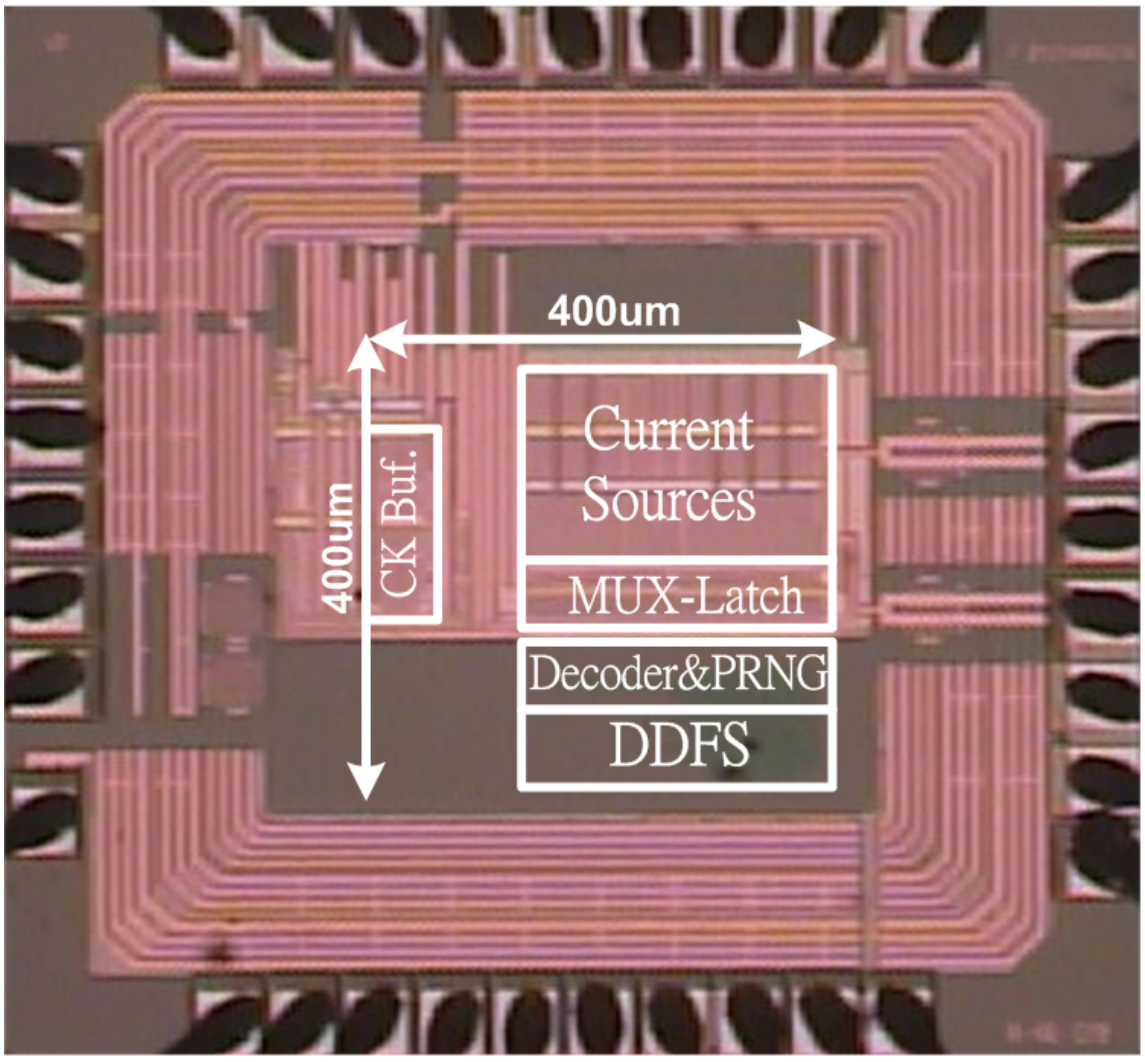

Figure 3.8: Microphotograph of the DRRZ DAC

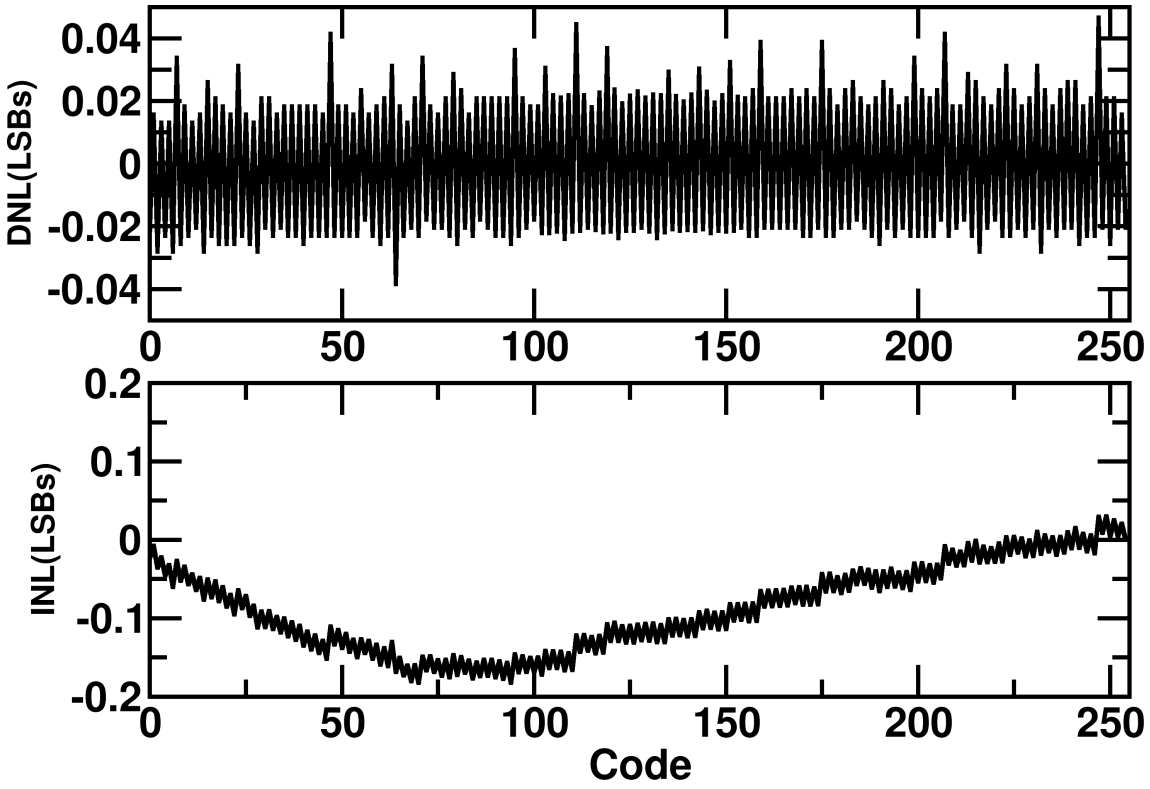

Figure 3.9: Measured differential nonlinearity (DNL) and integral nonlinearity (INL).

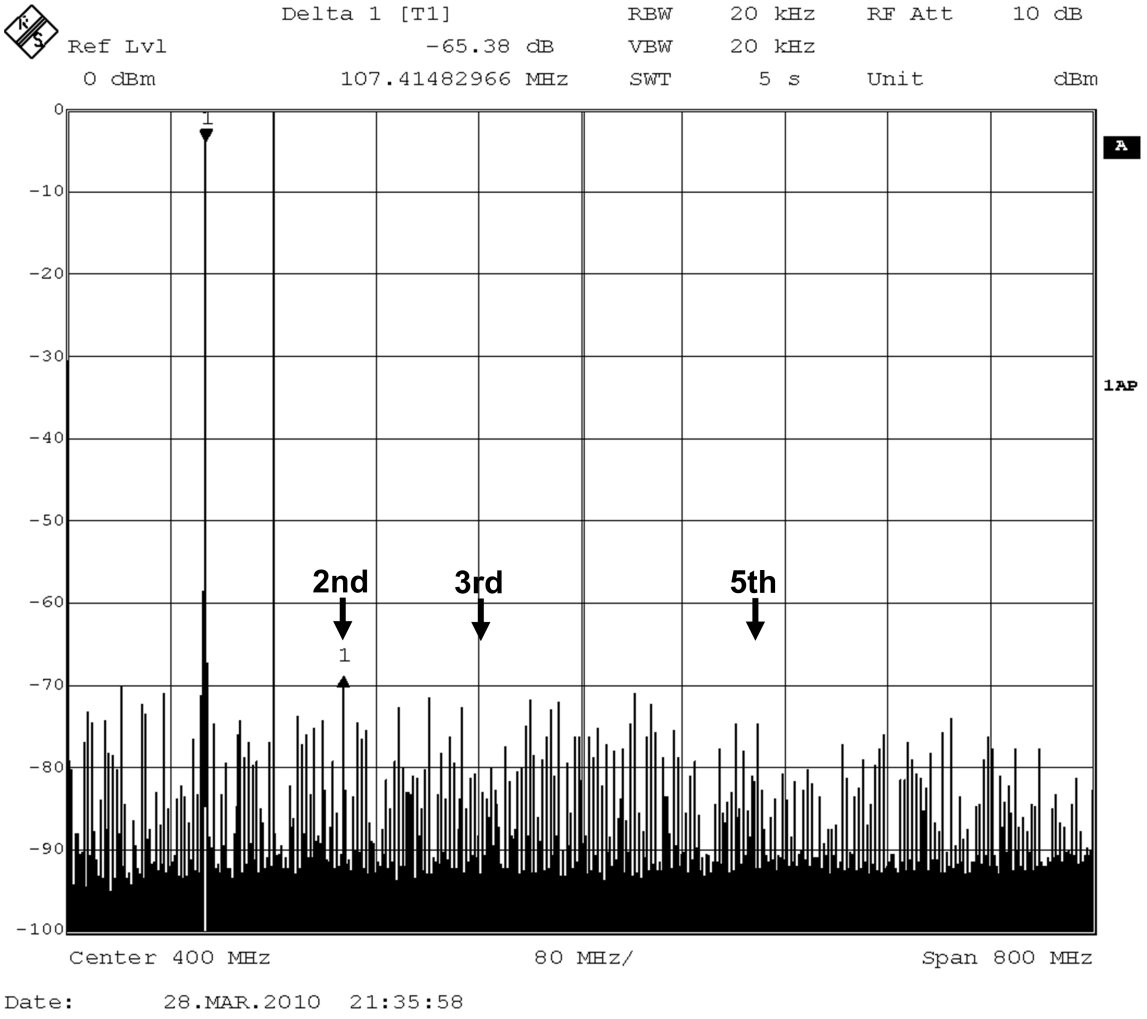

Figure 3.10: Output spectrum of the DAC with NRZ. Sampling rate is 1.6 GS/s, input frequency is 107 MHz.

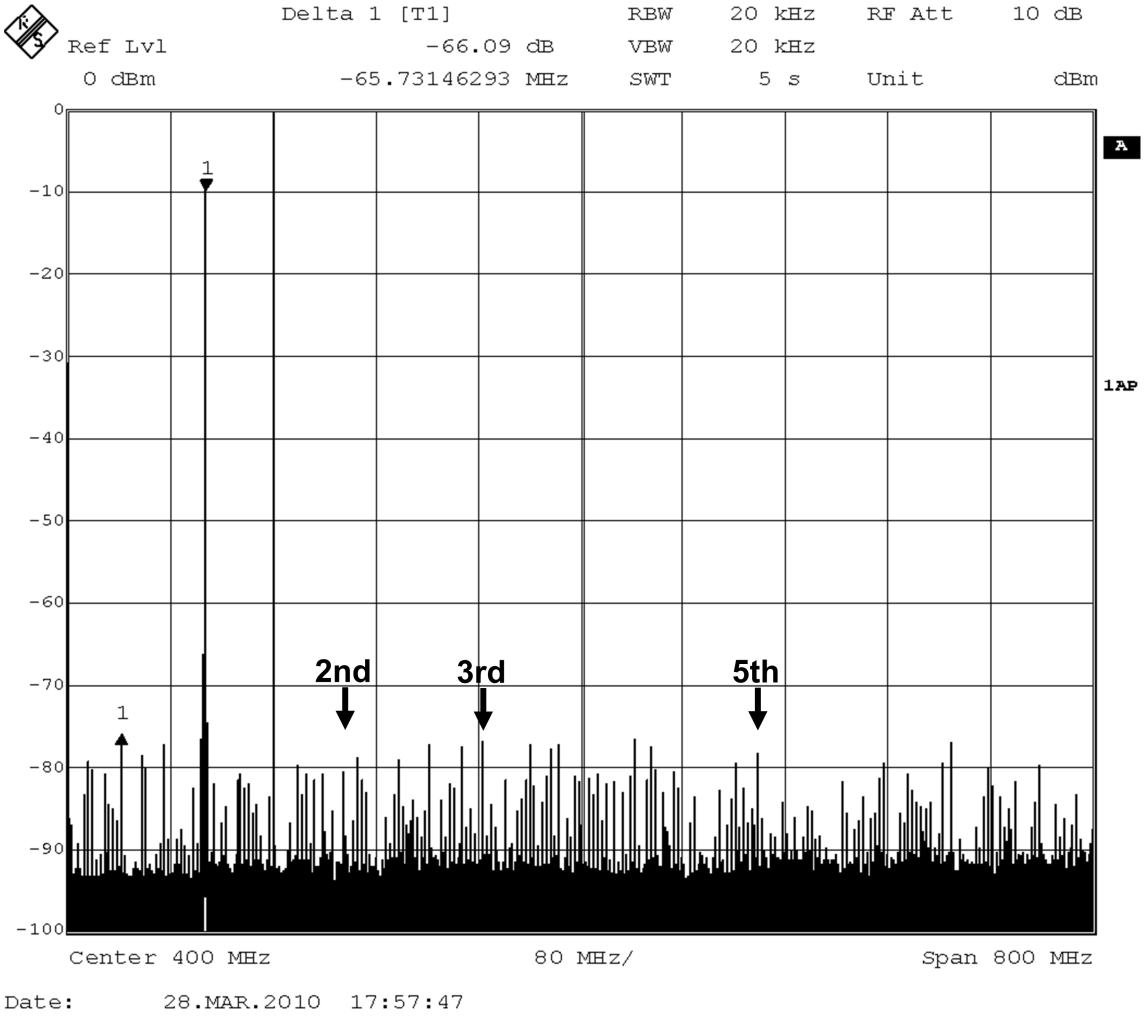

Figure 3.11: Output spectrum of the DAC with DRRZ. Sampling rate is 1.6 GS/s, input frequency is 107 MHz.

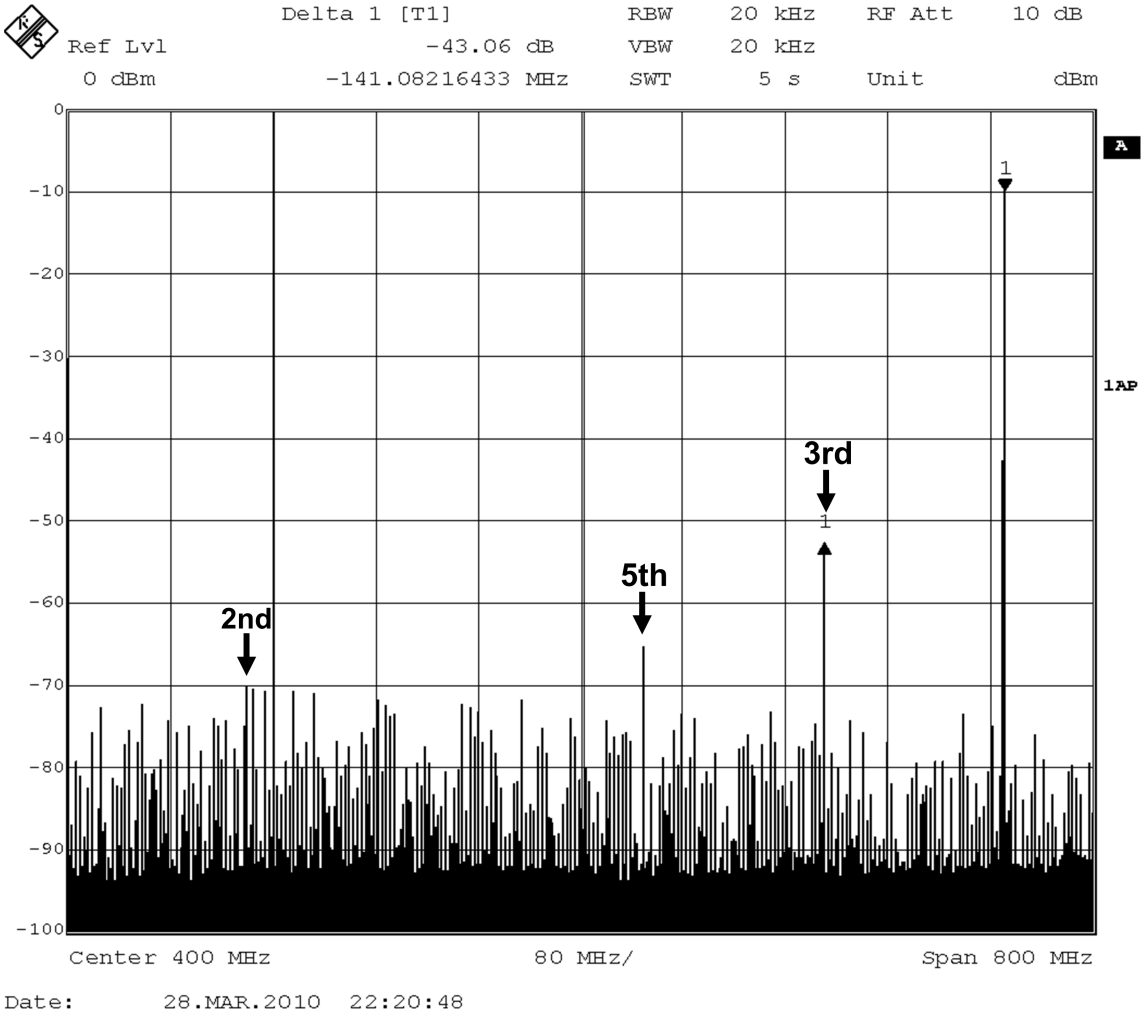

Figure 3.12: Output spectrum of the DAC with NRZ. Sampling rate is 1.6 GS/s, input frequency is 731 MHz.

66 dB for the DRRZ DAC. When the input frequency of the DAC is low, the total number of current switches forced to switch is low in each clock cycle. The overall switching transients have little effect on the harmonic distortion of the DAC. Thus, the DRRZ function shows little improvement in SFDR.

Figure 3.12 and Figure 3.13 are DAC output spectra under similar conditions except the input frequency is raised to 731 MHz. When the input frequency of the DAC is high, the total number of current switches forced to switch is high in each clock cycle. The effect of switching transients becomes large and is revealed as the harmonic tones in Figure 3.12. The SFDR is 43 dB and is dominated by the third harmonic. The harmonic

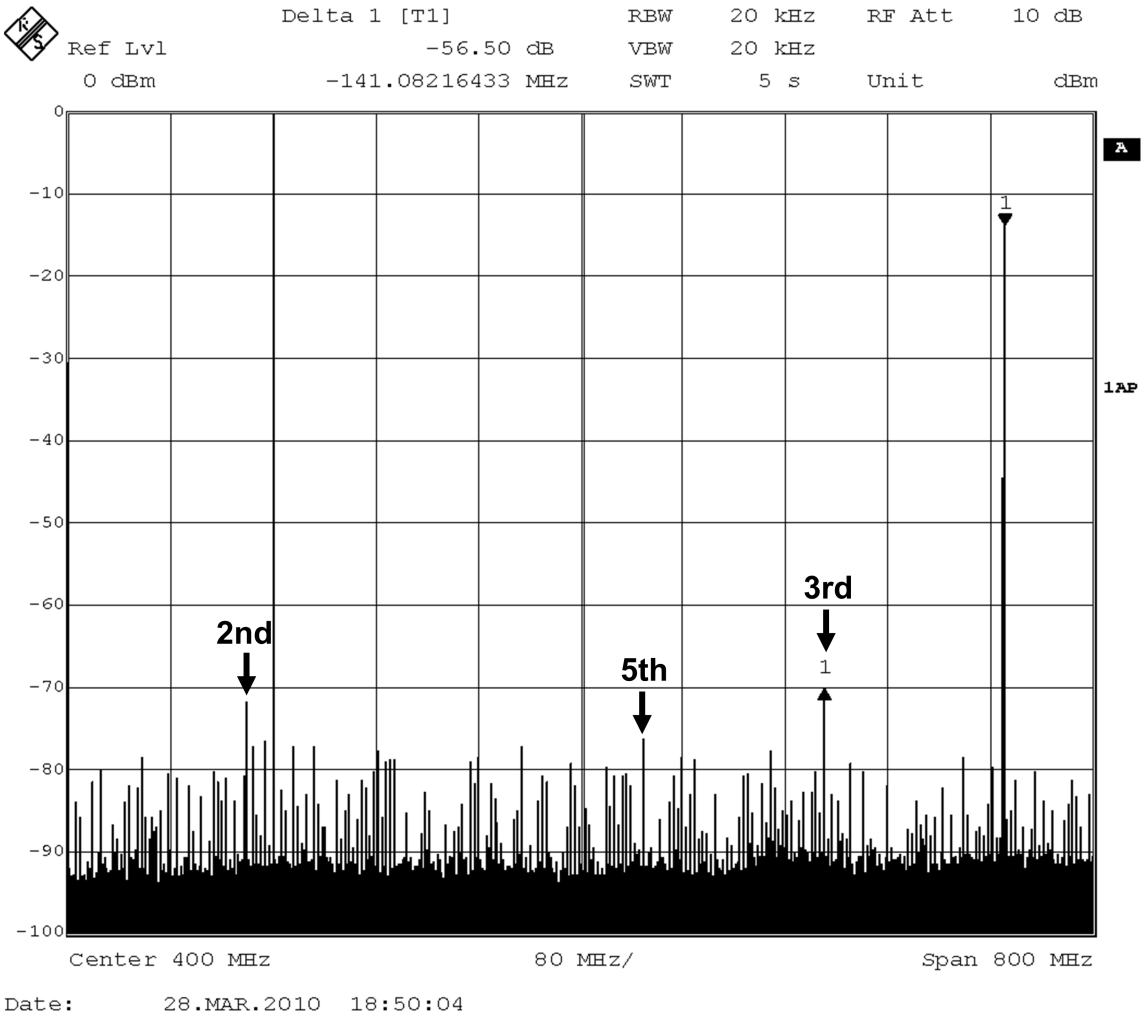

Figure 3.13: Output spectrum of the DAC with DRRZ. Sampling rate is 1.6 GS/s, input frequency is 731 MHz.

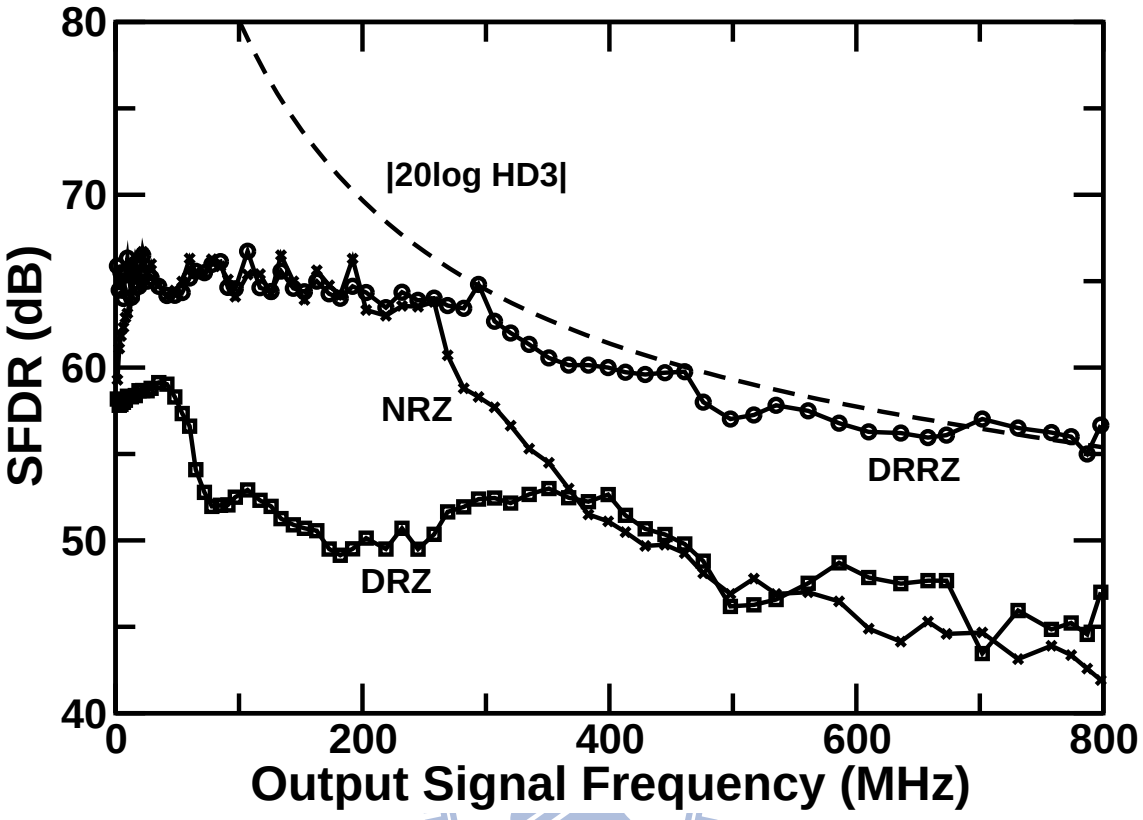

Figure 3.14: Measured SFDR at different signal frequencies.

tones are suppressed by the DRRZ operation as illustrated in Figure 3.13. The SFDR is improved to 56.5 dB.

Figure 3.14 shows the measured SFDR of the DAC operated at 1.6 GS/s sampling rate and with different input frequencies. The DAC has three different configurations, which are NRZ, DRZ, and DRRZ. For the NRZ DAC, the measured SFDR is degraded from 65 dB to 42 dB as input frequency increases toward 800 MHz. Employing the DRRZ operation, the DAC can maintain a SFDR larger than 60 dB up to 460 MHz and a SFDR larger than 55 dB up to 800 MHz. Figure 3.14 also shows the measured SFDR of the DRZ DAC. The DRZ setup cannot improve SFDR at all. At low frequencies, the DRZ DAC exhibits a SFDR even worse than the NRZ DAC. This is because, at low frequencies, DRZ introduces more switching transients than NRZ.

Also shown in Figure 3.14 is a theoretical HD3 calculation by considering only the

Table 3.1: DAC Performance Summary

Technology	CMOS 90 nm
Resolution	8 Bits
Sampling Rate f_s	1.6 GS/s
DNL	+0.04 / −0.03 LSB
INL	+0.0 / −0.2 LSB
SFDR @ f_{in} = 100 MHz	64.5 dB
SFDR @ f_{in} = 700 MHz	57.0 dB
Load Current	20 mA
Output Swing	1 V_{pp}
Supply Voltage (Analog/Digital)	2.5 V / 1.2 V
Power Consumption	90 mW
Core Area	0.16 mm^2

output impedance of current cells [42, 34, 43]. It is expressed as

$$\text{HD3} = \left[\frac{M}{4} \cdot \frac{R_{L,d}}{|Z_o|}\right]^2 \tag{3.2}$$

where $R_{L,d} = 50\ \Omega$ is the differential resistance of the DAC output loads, $M = 32$ is the total number of M-DAC current cells, and Z_o is the output impedance of a M-DAC current cell. The L-DAC is treated as a single M-DAC current cell. Referring to Figure **??**, Z_o is the output impedance looking into the I_{o1} terminal when M3 is turned on and M4 is off. The Z_o in our design can be modeled as a resistor $R_o = 1.9\ \text{M}\Omega$ in parallel with a capacitor $C_o = 10.8$ fF. Figure 3.14 indicates that the HD3 of Equation (3.2) is the major distortion source for the DRRZ DAC with input frequencies higher than 300 MHz. This type of distortion cannot be removed by DRRZ.

The DAC specifications are summarized in Table 4.2. Figure 3.15 compares the dynamic performance of this DAC against other published DAC works. In order to compare DACs of different sampling rates, the dynamic performance is defined as SFDR × f_s, where SFDR is expressed in power ratio and f_s is sampling rate in Hz. Note the reported DAC is only an 8-bit design. But its dynamic performance is competitive at high signal frequencies.

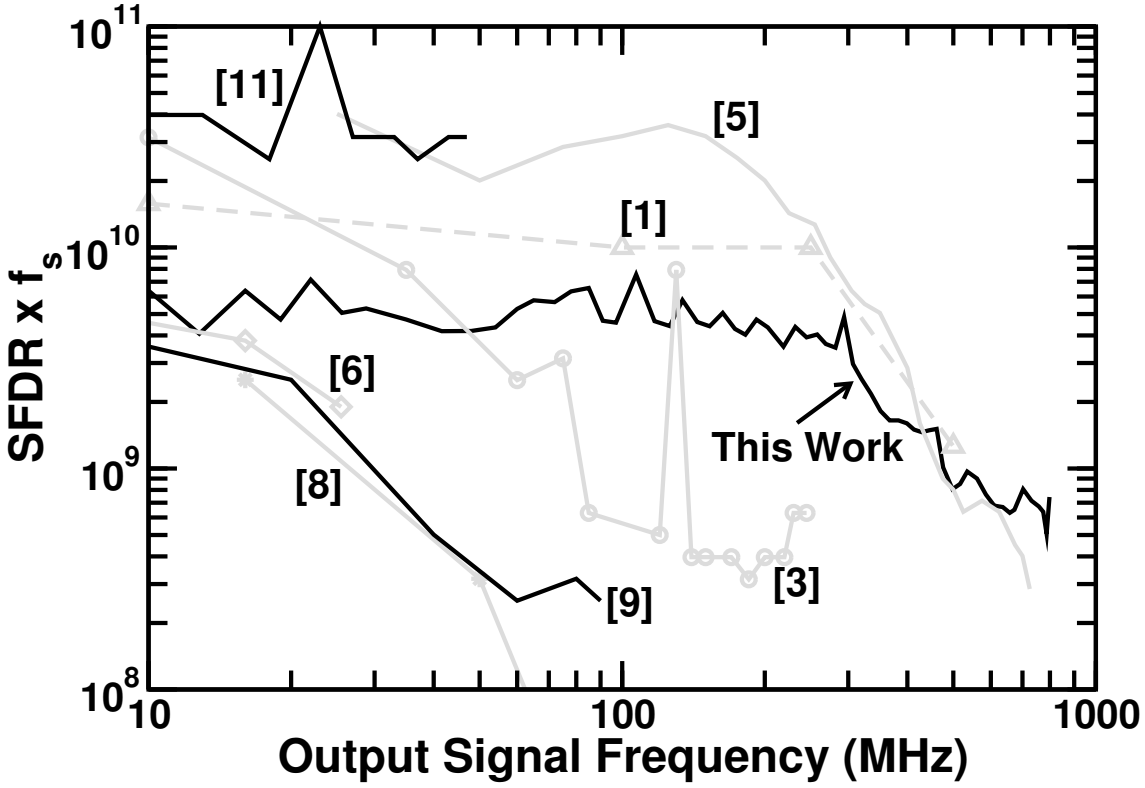

Figure 3.15: Dynamic performance comparison of published DACs.

3.5 Summary

A CMOS 8-bit 1.6-GS/s current-steering DAC was presented to demonstrate the proposed digital random return-to-zero (DRRZ) technique. The technique requires only a small overhead in digital circuits. The improvement in SFDR of the DAC is 14 dB when the input frequency is 800 MHz.


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Chapter 4

A 12-Bit 1.25-GS/s Background Calibrated DAC

4.1 Introduction

The current-steering digital-to-analog converts (DACs) can achieve high sampling rate, and thus are commonly used in generating high-frequency signals [6, 1, 7, 8, 4, 10, 34, 12]. Figure 4.1 shows a generic current-steering DAC. It consists of M equally-weighted current cells. Each current cell contains a current source of I_u output current, a MOSFET pair functioning as a current switch, and a digital latch controlled by a clock CK. The complementary outputs of the latch control the current switch, directing the I_u current to either the R_L load at V_{o1} or the one at V_{o2}. A decoder converts the DAC digital input $D_i[k]$ into M thermometer-code signals $B_j[k]$, where $1 \leq j \leq M$. We define the $B_j[k]$ signal has a binary value of either $+1$ or -1. Figure 4.1 illustrates the DAC differential non-return-to-zero (NRZ) output waveform $V_o = V_{o1} - V_{o2}$. The V_o has a voltage range between $+M I_u R_L$ and $-M I_u R_L$, and a step size of $2 I_u R_L$.

The DAC static linearity, specified as differential nonlinearity (DNL) and integral nonlinearity (INL), is mainly determined by the matching of I_u among different current cells and the output resistances of the I_u current sources. Cascode technique is usually used to increase the output resistance of a current source. The dimension of the transistors in the current sources must be large enough to ensure good I_u matching [13]. There

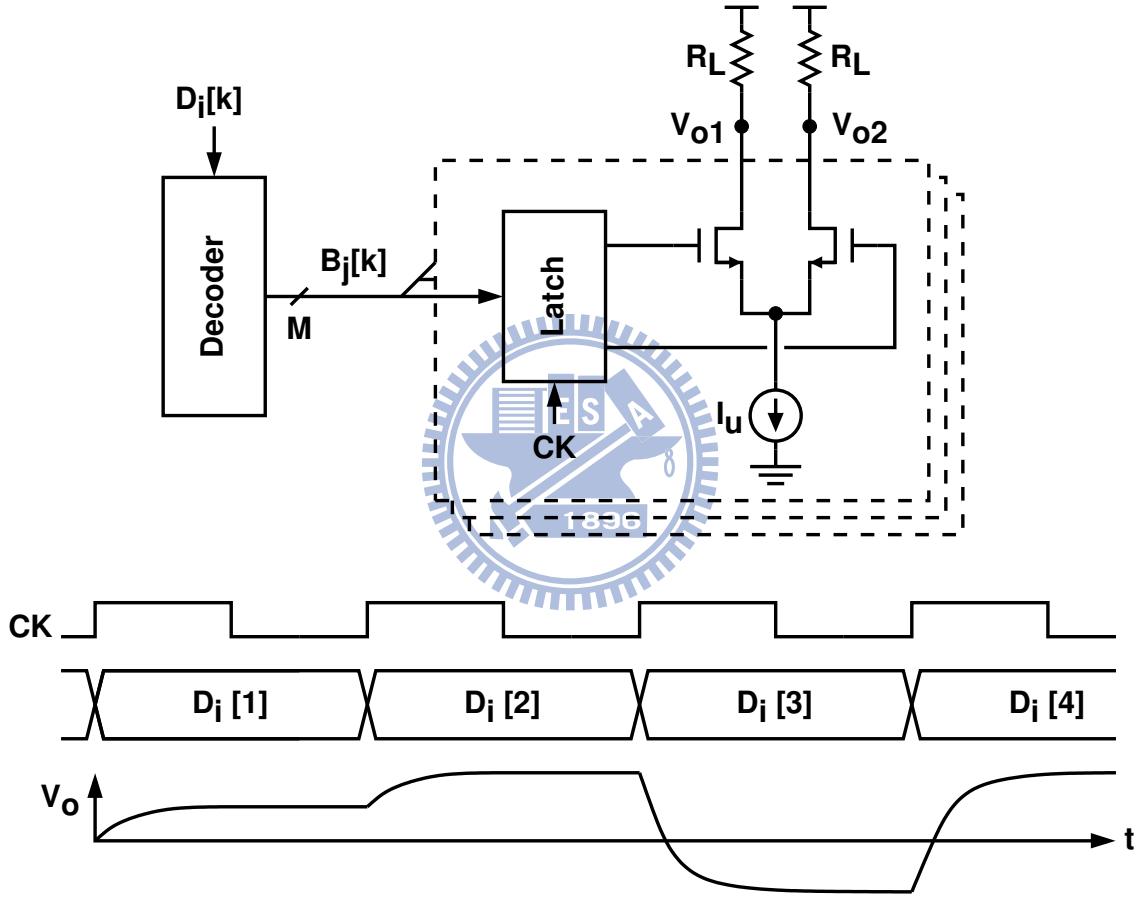

Figure 4.1: A current-steering DAC.

are techniques that can relax the device matching requirements, including calibrations [14, 15, 17, 18, 20] and dynamic element matching [24].

Besides static linearity, dynamic performance is also crucial for a high-speed DAC. The DAC dynamic performance is manifested as spurious-free dynamic range (SFDR) degradation shown in the output spectrum of V_o when the $D_i[k]$ input is a single-tone sinewave. As for a DAC with poor dynamic performance, its SFDR decreases rapidly with increasing input frequency. The DAC dynamic performance is related to the switching operation of the internal current switches. It induces the code-dependent switch transient (CDST) effect [31, 38, 28] and the code-dependent loading variation (CDLV) effect [42, 34, 43, 12].

This section describes a 12-bit 1.25-GS/s current-steering DAC [35]. We employ the digital random return-to-zero (DRRZ) technique [32] to mitigate the CDST effect and relax matching requirement for current switches. The DRRZ operation also enables a current-cell background calibration. The calibration relaxes the device matching requirements for the I_u current sources, allowing a more compact design of the current cells. The compact current cell design directly reduces the CDLV effect. The DAC was fabricated using a standard 90 nm CMOS technology. At 1.25 GS/s sampling rate, this DAC chip achieves a SFDR better than 70 dB up to 500 MHz input frequency.

4.2 Design for High Signal Bandwidth

Figure 4.2 shows the operation of a single current cell. The current cell contains a current source I_u and a MOSFET current switch M1-M2. Upon the rising edge of clock CK, the binary input $B_j[k]$ is loaded into the latch. Its two complementary outputs, V_{s1} and V_{s2}, drive the current switch, directing the I_u current to either output node V_{o1} or output node V_{o2}. Figure 4.2 also shows the transient response of the differential output current $I_o = I_{o1} - I_{o2}$. The output current I_o is a combination of an ideal transient response and switching transients. Switching transients occur only when $B_j[k]$ varies. There are several sources for switching transients [31], including switch feedthrough through the current switch, timing skew of CK, finite rise/fall time of V_{s1} and V_{s2}, and voltage fluctuation at the common-source node V_a.

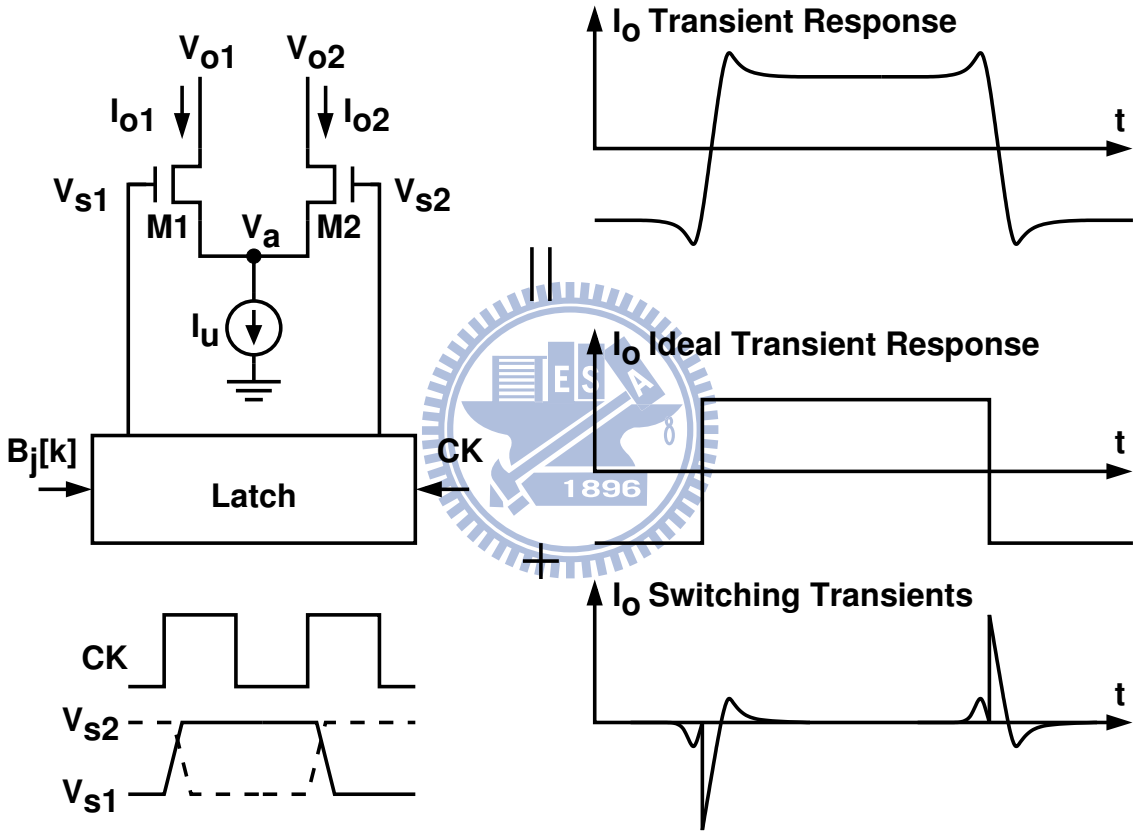

Figure 4.2: Code-dependent switching transient (CDST).

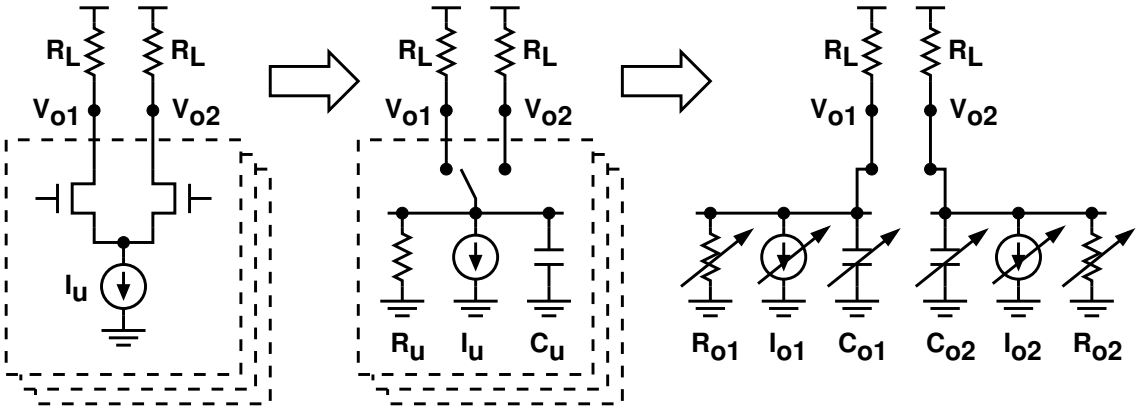

Figure 4.3: Code-dependent loading variation (CDLV).

The I_o switching transients from all current cells are summed up at the DAC V_o port. Assume the switching transients are invariant and identical among all current cells, and the switching transients at the rising edges of I_o are the inverse of the switching transients at the falling edges of I_o. Then total switching transients appearing at V_o are proportional to $D_i[k] - D_i[k-1]$. These identical switching transients do not cause harmonic distortion. However, there are device variations in both the current switch and the latch, and there are different CK timing skew for different current cells. Thus, different current cells exhibits different switching transients. Depending on the $D_i[k]$ sequence, the sequence of the switching transient summation becomes a nonlinear term, resulting in harmonic distortions. This is called the CDST effect. If the input $D_i[k]$ is a single-tone sinewave and its frequency is increased, the CDST effect is intensified due to the increase of $|D_i[k] - D_i[k-1]|$. Thus, the DAC SFDR decreases with increasing input frequency.

To reduce variation in switching transients, the V_{s1} and V_{s2} waveforms must be carefully designed. Matching among current switches, latches, and CK routes must be considered in the design. Adding a cascode stage to the current switch is also a common practice to reduce feedthrough of V_{s1} and V_{s2} to the outputs.

Figure 4.3 shows another source of harmonic distortion. Each current cell is modeled as an ideal switch on top of an ideal current source I_u in parallel with a resistor R_u and a capacitor C_u. The resistor R_u represents the output resistance of the current source. The capacitor C_u represents the capacitance associated with the output node of the current source, including the gate capacitance of the current switch. Both R_u and C_u are

connected to either the V_{o1} node or the V_{o2} node, depending on the state of the switch. As a result, the total loadings for output nodes V_{o1} and V_{o2} vary with digital input $D_i[k]$. This code-dependent loading variation (CDLV) effect introduces harmonic distortion in the differential output $V_o = V_{o1} - V_{o2}$. When $D_i[k]$ is a sinewave, the 3rd-order harmonic distortion caused by the CDLV effect is [42, 43, 34, 12]

$$\text{HD3} = \left[\frac{M}{4} \cdot \frac{R_{L,d}}{|Z_u|}\right]^2 \tag{4.1}$$

where M is the total number of current cells, $R_{L,d} = 2R_L$ is the differential resistance of the DAC output loads, and Z_u is the output impedance of a single current cell, where $1/Z_u = 1/R_u + j\omega C_u$.

Increasing R_u and reducing C_u can mitigate the CDLV effect. Adding cascode stage to a current source can increase R_u. In most designs, the CDLV effect at high frequencies is dominated by C_u. The C_u capacitance is determined by the device dimensions of the current switch and the current source, while the device dimensions are governed by the matching requirements. The CDLV effect can be mitigated by adding an additional cascode stage following the current switch in each current cell [33, 7, 34]. The MOSFETs in those cascode stages need to have large transconductances to achieve good high-frequency performance [34, 12].

For this work, instead of adding additional cascode stages, we simply use smaller devices for both the current sources and the current switches to reduce C_u. Smaller devices lead to larger mismatches. However, due to the use of DRRZ, the matching requirement for the current switches is relaxed. The mismatches among the current sources are corrected by the current-cell background calibration described in Section 4.4.

4.3 DAC Architecture

Figure 4.4 shows the 12-bit DAC architecture. The DAC is segmented into a 6-bit equally-weighted MSB DAC (M-DAC) and a 6-bit binary-weighted LSB DAC (L-DAC). The differential output currents from both the M-DAC and the L-DAC are tied together and connected to two external resistive loads R_{L1} and R_{L2} to produce the differential output voltage $V_o = V_{o1} - V_{o2}$. The M-DAC comprises 63 identical current cells. Each current

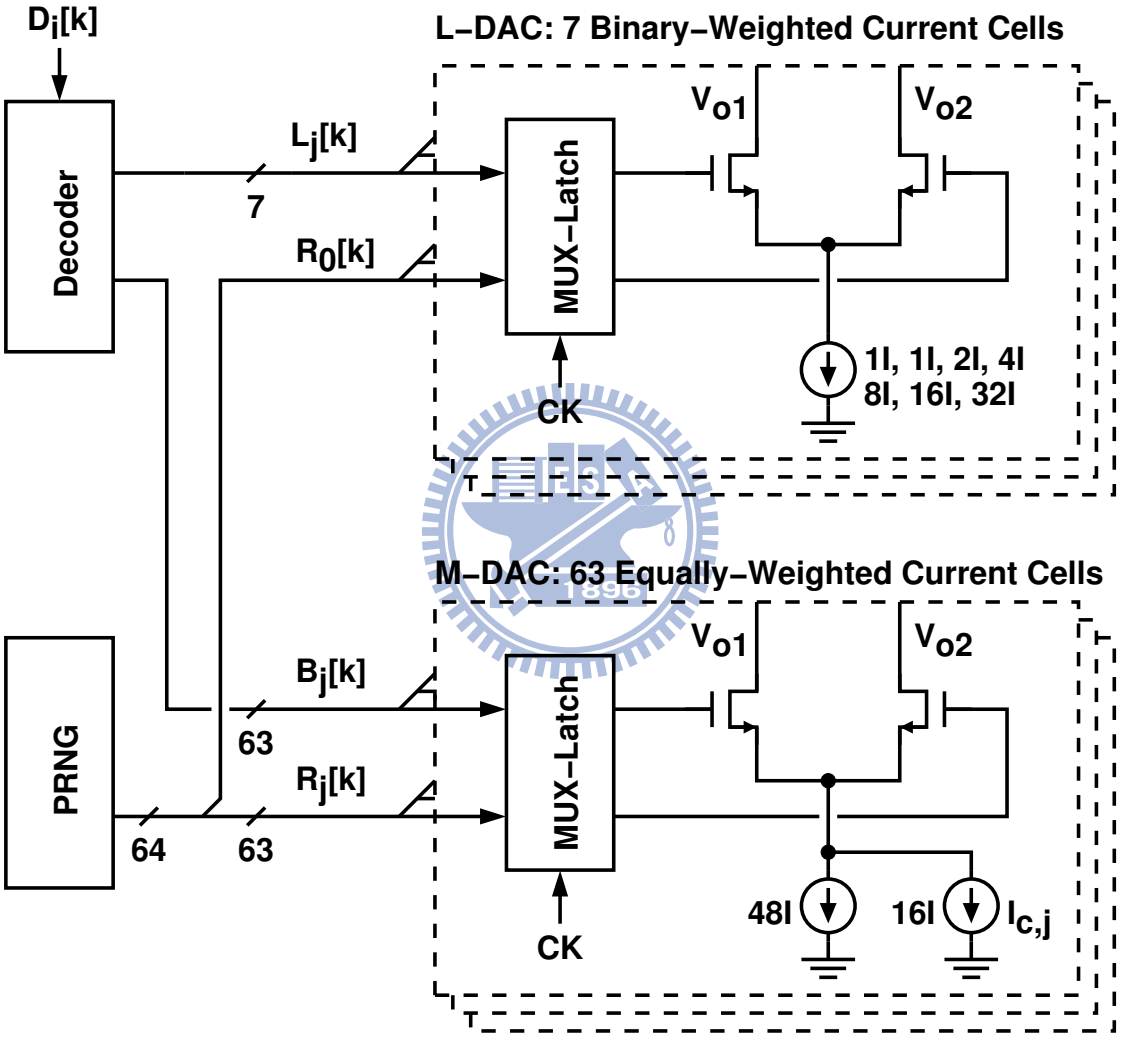

Figure 4.4: A segmented 12-bit DAC.

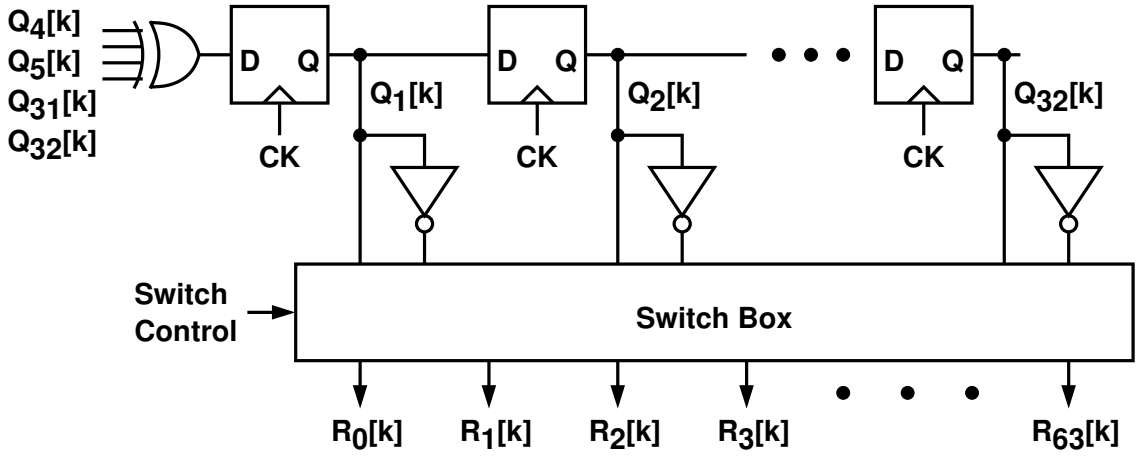

Figure 4.5: Pseudo random number generator (PRNG).

cell is designed to output a nominal current of $64I$, where I is the DAC unit current. The L-DAC comprises 7 current cells which output an current of $1I$, $1I$, $2I$, $4I$, $8I$, $16I$, and $32I$ respectively. There are two $1I$ current cells in the L-DAC so that a differential output of zero can be realized. In our design, $I = 4\ \mu$A and $R_{L1} = R_{L2} = R_L = 25\ \Omega$ yield a V_o signal range of 0.8 V_{pp}.

The DAC employs the DRRZ operation described in Section 4.2. As shown in Figure 4.4, each current cell contains a multiplexing latch (MUX-Latch). When CK is high, the DAC is in the data phase. The j-th M-DAC current cell selects the $B_j[k] \in \{-1, +1\}$ control signal from the D_i decoder, and the j-th L-DAC current cell selects the $L_j[k] \in \{-1, +1\}$ control signal. The combination of the equally-weighted $B_j[k]$ and binary-weighted $L_j[k]$ reflects the value of $D_i[k]$. When CK is low, the DAC is in the $Z[k]$ zero phase. The j-th M-DAC current cell selects the $R_j[k] \in \{-1, +1\}$ control signal from a pseudo-random number generator (PRNG). The entire L-DAC is treated as a single MSB current cell. Its current cells select the same $R_0[k]$ control signal. Since $\sum_{j=0}^{63} R_j[k] = 0$, the DAC differential output current is zero during the zero phase.

Figure 4.5 shows the PRNG schematic. It is a 32-bit linear feedback shift register. The 32 outputs from the register, $Q_j[k]$ where $j = 1, \cdots, 32$, and their complementary outputs, $\overline{Q}_j[k]$, form the 64 $R_j[k]$ control signals, such that $\sum_{j=0}^{63} R_j[k] = 0$. The switch box shown in Figure 4.5 is used to rearrange the connections from $Q_j[k]$ and $\overline{Q}_j[k]$ to $R_j[k]$. The rearrangement is required by the background calibration described in Section 4.4.

Table 4.1: Dimensions of MOSFETs in the M-DAC

	M1	M2	M3	M4	M5	M6
W (μm)	48	16	38.4	12.8	12	12
L (μm)	1	1	0.4	0.4	0.34	0.34

As shown in Figure 4.4, there are two separate current sources in each M-DAC current cell. One current source provides an output current of $48I$. The current may vary due to mismatch of devices. The other current source provides an output current of $I_{c,j}$. The calibration described in Section 4.4 adjusts $I_{c,j}$ so that the total output current of a M-DAC current cell is $64I$.

For 12-bit with 6-6 segmentation, LSB = 1 2 4 8 16 32, MSB = 64 64 64 ...

INL (max)	$64 \times \frac{1}{2}$TLSB	$\leq ---LSB$
DNL(max)	$\sqrt{64}\sigma$	$\leq 0.125LSB$

TLSB: Trimmer DAC resolution

$$1 \times \sqrt{64}\sigma \leq 0.125$$

$$\sigma \leq 1.5625 \times 10^{-2}$$

$$2 \times (1.5625 \times 10^{-2})^2 \times WL_{unit} \geq 4 \cdot \frac{5.81^2}{V_{ov}^2} + 0.0162^2$$

V_{ov} (mV)	100	150	200	250	300	350
WL_{unit} $(um^2)(1\sigma)$	56.5/2	25.6	14.9	9.9	7.2	4.5
WL_{unit} $(um^2)(3\sigma)$	508/2	230	134	90	65	40

Figure 4.6 shows the circuit schematic of the j-th current cell in the M-DAC. MOSFETs M11–M18 and four inverters form a level-sensitive MUX-Latch. When CK is high, the $B_j[k]$ input is loaded into the latch. When CK is low, the $R_j[k]$ input is loaded into the latch. The MUX-Latch is operated under a 1.2 V supply. MOSFETs M5 and M6 together function as a current switch. MOSFETs M1 and M3 form a cascode current source with a fixed current of $48I$. MOSFETs M2 and M4 form another cascode current source whose output current is mirrored from the $I_{c,j}$ current input. Both current sources are operated under a 2.5 V supply. M1–M6 are MOSFETs with thick gate oxide. Device dimensions are listed in Table 4.1. Current mirrors MC1–MC6 are also thick-gate MOSFETs. The level converter shown in Figure 4.6 converts the MUX-Latch complementary outputs of

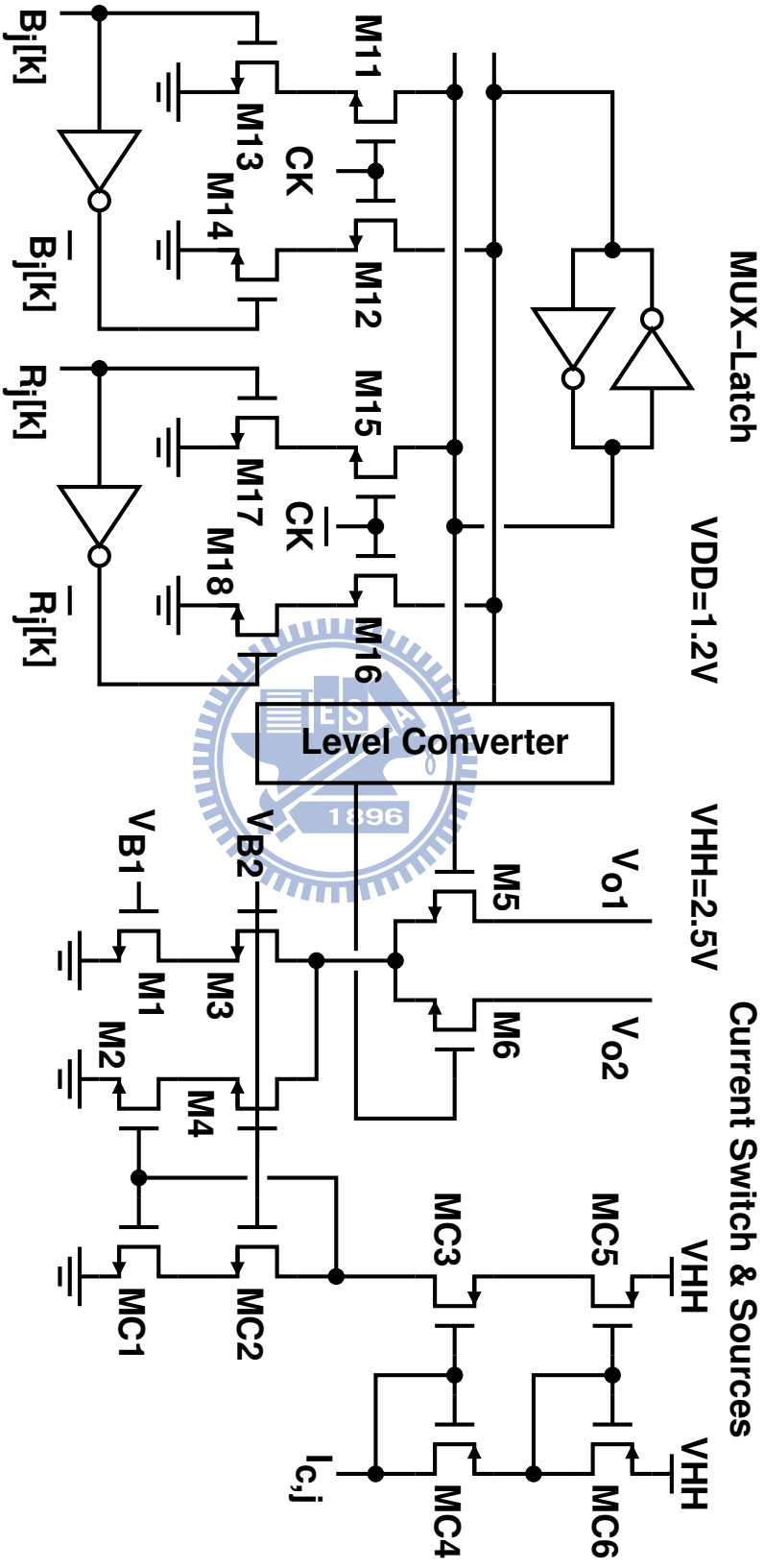

Figure 4.6: Schematic of the j-th M-DAC current cell.

1.2 V swing into signals of 2.5 V swing to drive the M5-M6 current switch. Each signal path in the level converter is a cascade of 3 inverters. The supply voltage for the last inverter is 2.5 V.

From post-layout simulation result shown in Figure 4.7, we obtain $R_u = 19$ MΩ and $C_u = 6.3$ fF. From Equation (4.1) with $M = 64$ and $R_{L,d} = 50$ Ω, the HD3 due to the CDLV effect is less than -70 dB if the input frequency is lower than 560 MHz.

Consider only the M1 and M2 current sources of the current cell shown in Figure 4.6. Its total output current I_u exhibits a standard deviation of $\sigma(I_u) = 2.56I$ due to device variation, where I is the LSB current of the DAC. To achieve 12-bit resolution and an INL less than 0.5, $\sigma(I_u) < 0.125I$ is required. Calibration described in the next section is used to meet the requirement.

4.4 Current-Cell Background Calibration

For the M-DAC current cell shown in Figure 4.6 with the device dimensions listed in Table 4.1, its output current variation does not meet the resolution requirement due to the device variation. In this work, we use background calibration to correct the current variation.

Figure 4.8 shows the proposed calibration principle. The total L-DAC current is I_L. There are 63 M-DAC current cells whose currents are $I_{M,1}$ to $I_{M,63}$ respectively. The calibration choose I_L as a reference and adjusts $I_{M,j}$ to make $I_{M,j} = I_L$, where $j = 1, \cdots, 63$. The M-DAC and the L-DAC execute the regular DRRZ operation described in Section 4.2. During the $Z[k]$ zero phase, all M-DAC current cells and the L-DAC are controlled by $R_j[k]$ from the PRNG. The output current of the entire L-DAC is $R_0[k] \times I_L$. The output current of the j-th M-DAC current cell is $R_j[k] \times I_{M,j}$. When the j-th M-DAC current cell is under calibration, the switch box shown in Figure 4.5 rearranges its zero-phase control such that

$$R_j[k] = \overline{R}_0[k] \tag{4.2}$$

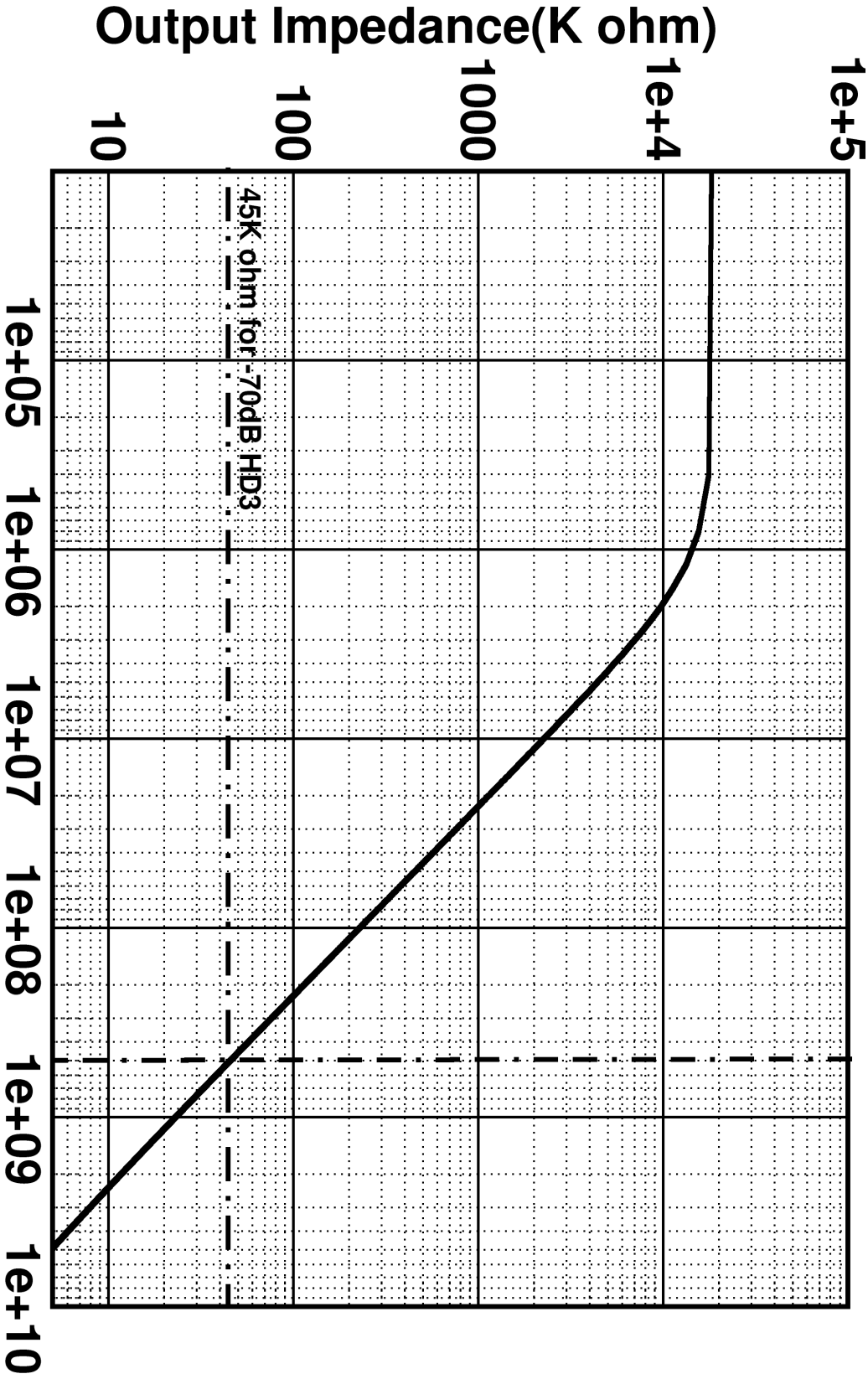

Figure 4.7: Zero-phase current-mismatch modulation

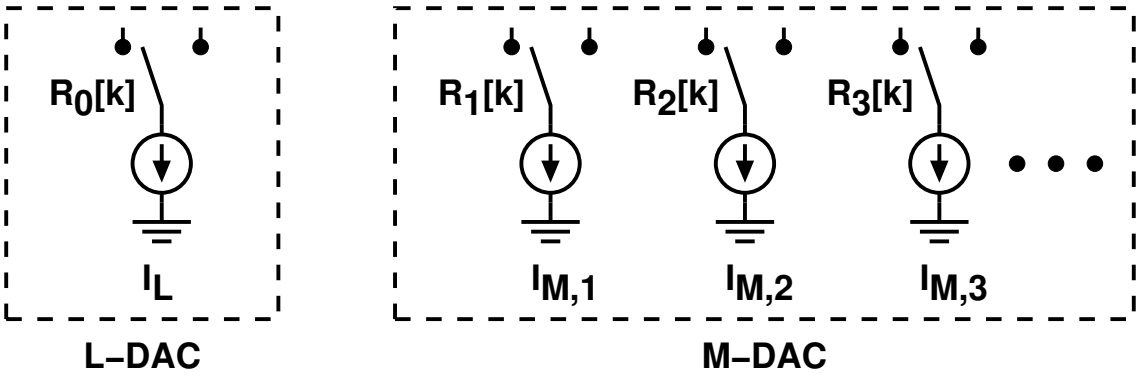

Figure 4.8: Zero-phase current-mismatch modulation

The DAC total output current in the $Z[k]$ zero phase can be expressed as

$$I_o[k] = R_0[k] \times \left(I_L - I_{M,j}\right) + \sum_{i=1, i\neq j}^{63} R_i[k] \times I_{M,i} \tag{4.3}$$

The current mismatch $\Delta I_j = I_L - I_{M,j}$ is modulated by $R_0[k]$. The calibration can extract ΔI_j from $I_o[k]$ by using $R_0[k]$ correlation. Once ΔI_j is acquired, it is used to correct $I_{M,j}$. The goal is to make ΔI_j approach zero. The calibration proceeds sequentially. It calibrates all 63 M-DAC, but only one at a given time.

Figure 4.9 shows the block diagram of the entire DAC, including its calibration signal path. The differential output currents from both M-DAC and L-DAC are tied together and connected to R_{L1} and R_{L2} to generate the differential output voltage $V_o = V_{o1} - V_{o2}$. When the j-th M-DAC current cell is under calibration, the modulated current mismatch $R_0[k] \times \Delta I_j$ is embedded in V_o during the $Z[k]$ zero phase. The DAC output V_o is sampled and processed by a chopper followed by a low-pass filter (LPF) to extract ΔI_j, yielding $V_m = V_{m1} - V_{m2}$. The V_m voltage is digitalized by a delta-sigma modulator (DSM). The resulting digital code is used to adjust the j-th calibration DAC (C-DAC). It's output current $I_{c,j}$ adjusts the the j-th current cell in the M-DAC, $I_{M,j}$, to make ΔI_j approach zero. The 63 C-DACs are controlled by a same BUS Master as shown in Figure 4.11 and the transfer function of one C-DAC is shown in Figure 4.12.

Figure 4.10 illustrates various signal waveforms in the calibration signal path. When CK is low, the DAC output voltage V_o during the zero phase is sampled, yielding $V_z = V_{z1} - V_{z2}$. And when CK is high, $V_z = 0$. Voltage V_z is correlated with $R_0[k]$ by a

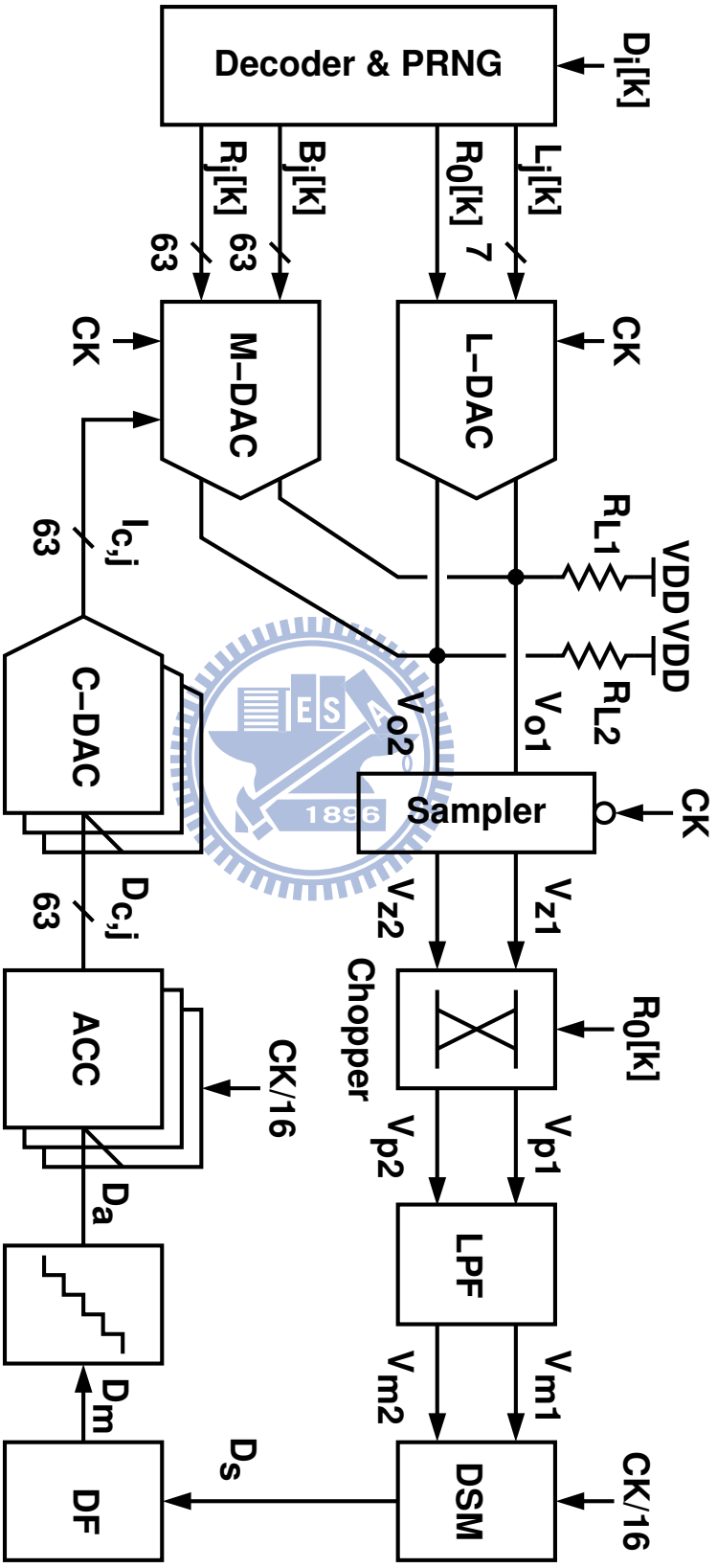

Figure 4.9: DAC block diagram.

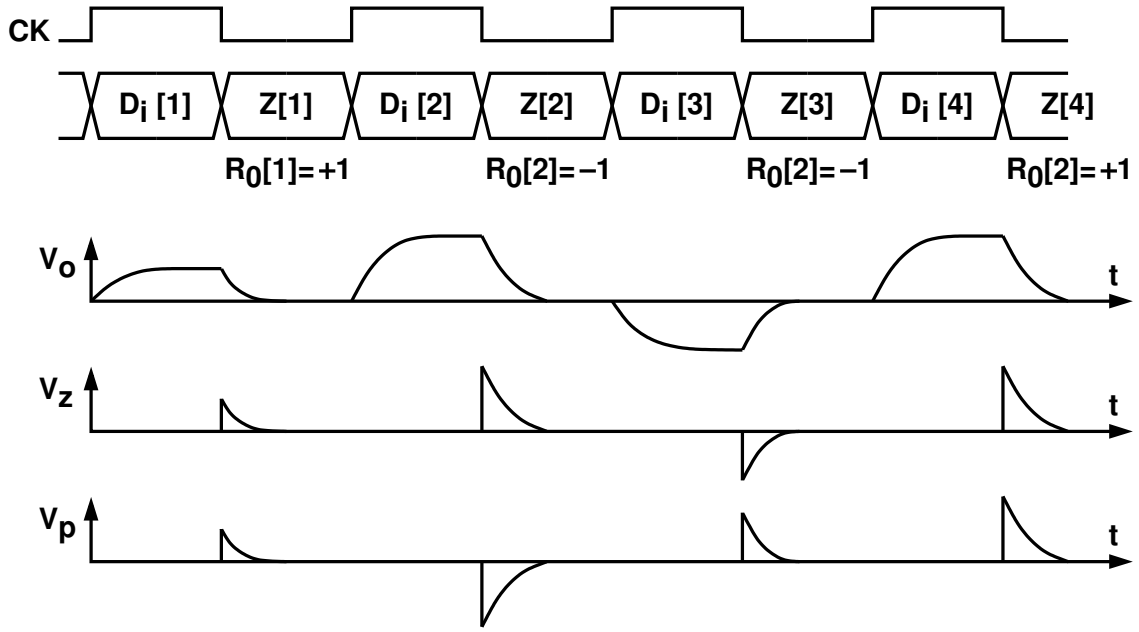

Figure 4.10: Various waveforms in calibration signal path.

chopper. The output of the chopper can be expressed as $V_p = V_z \times R_0[k]$. A LPF produces the averaged value of V_p, yielding $V_m = 0.5\Delta I_j \times R_L$. A continuous-time DSM is used to digitize V_m. The DSM operates at 1/16 of the CK frequency. It produces an one-bit digital stream $D_s \in \{-1, +1\}$. The decimation filter (DF) following the DSM is an accumulator that dumps its content every 2^{18} D_s samples. The DF output D_m is a digital representation of V_m. The digital code D_m is then scaled into D_a. The value of D_a is $\{0, \pm1, \pm2, \pm4\}$. Figure 4.13 shows the D_m-to-D_a mapping function. The D_a is added to the content of the j-th accumulator (ACC). There are 63 ACCs. Their outputs, $D_{c,j}$, control 63 calibration DACs (C-DACs) respectively. Each C-DAC is a 7-bit current-steering DAC with a resolution of $I/8$. For the j-th C-DAC, its output is $I_{c,j} = D_{c,j} \times I/8$. The current $I_{c,j}$ adjusts the output of the j-th M-DAC current cell, $I_{M,j}$.

Figure 4.14 shows the schematic of the calibration analog signal path. MOSFETs M1–M4 form the V_o sampler. When CK is high, the V_{z1} and V_{z2} nodes are connected to a common-mode voltage, V_{CM}. MOSFETs M5–M8 form the V_z chopper. The RC pairs, R_{F1}-C_{F1} and R_{F2}-C_{F2}, are the LPFs with a bandwidth of 26.5 kHz. The LPF output, V_m, is converted to current by a transconductor $G_m = 825$ μA/V, and then integrated

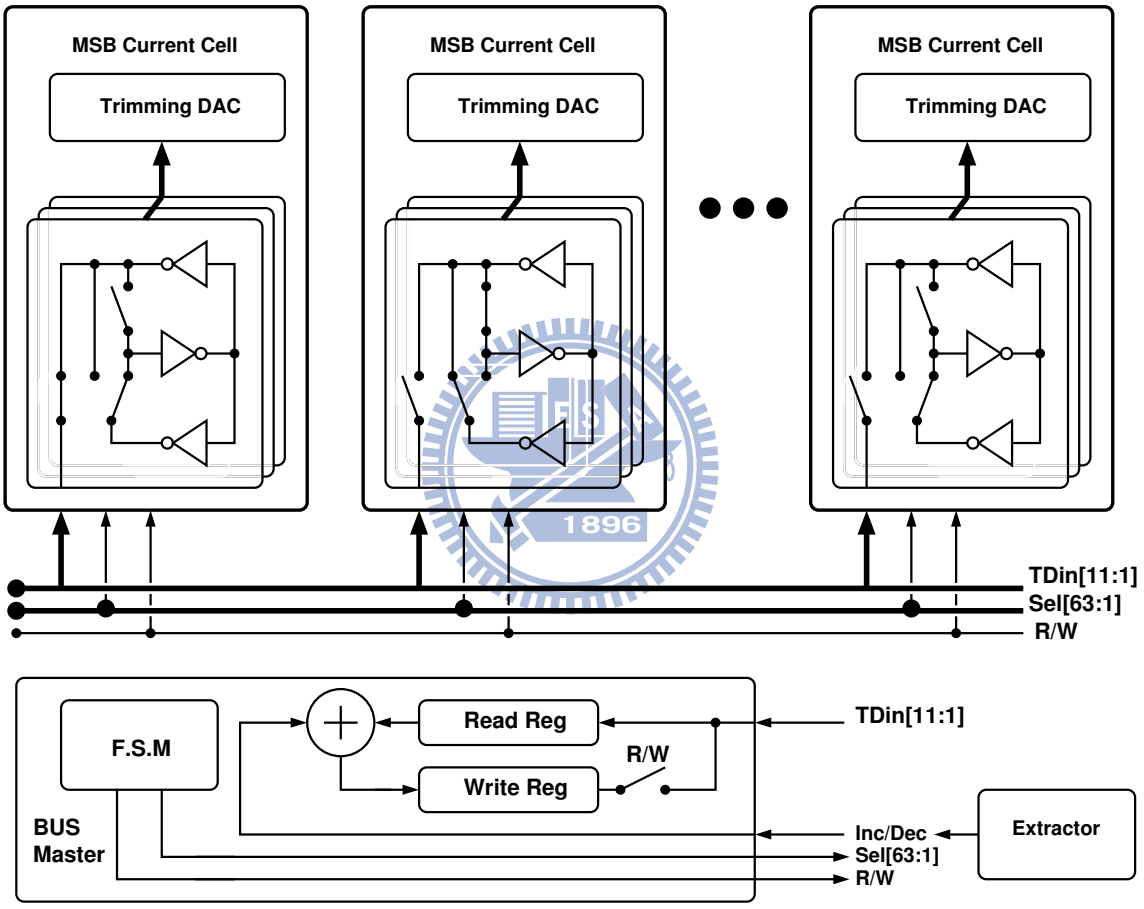

Figure 4.11: The C-DAC and BUS master.

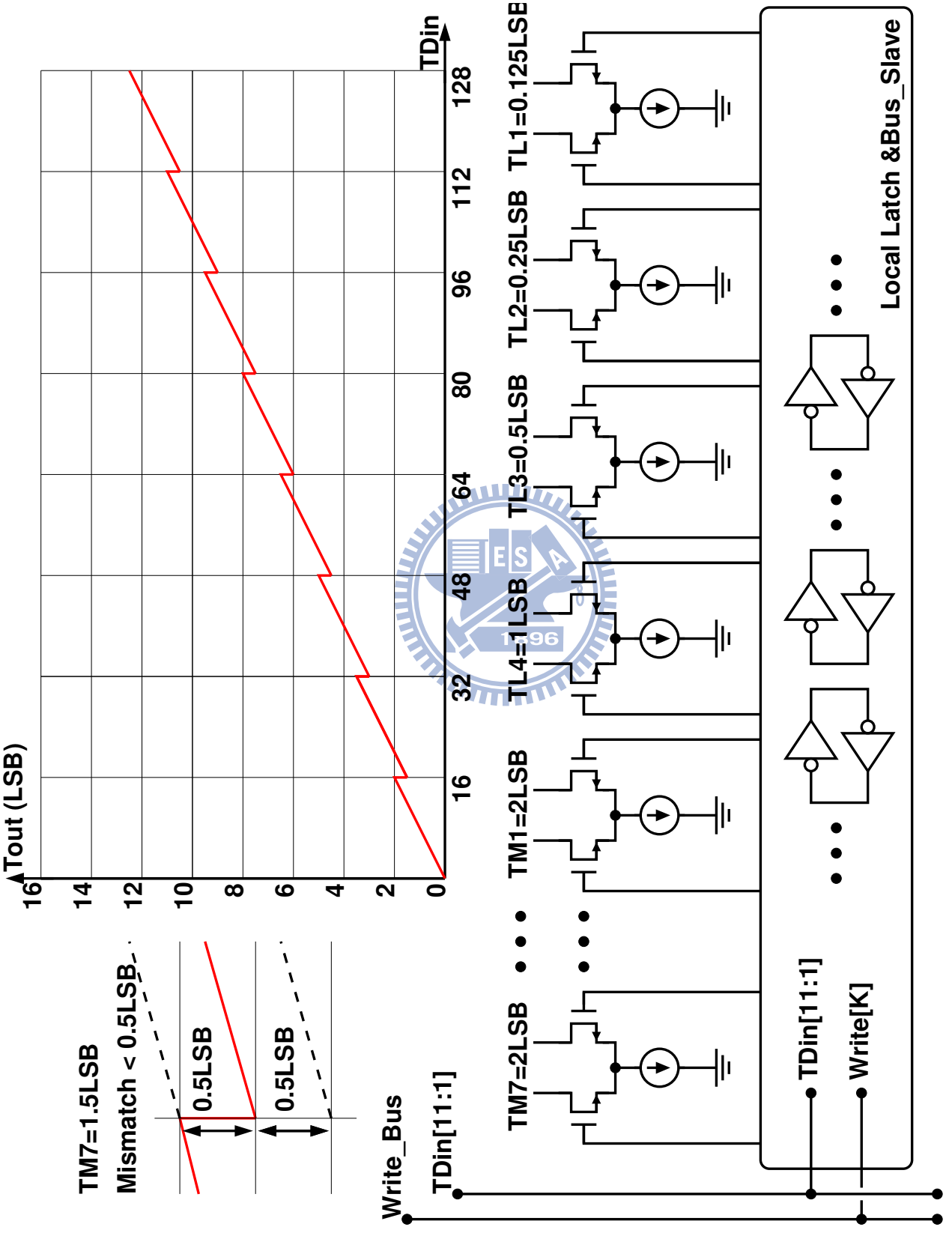

Figure 4.12: The C-DAC and transfer function.

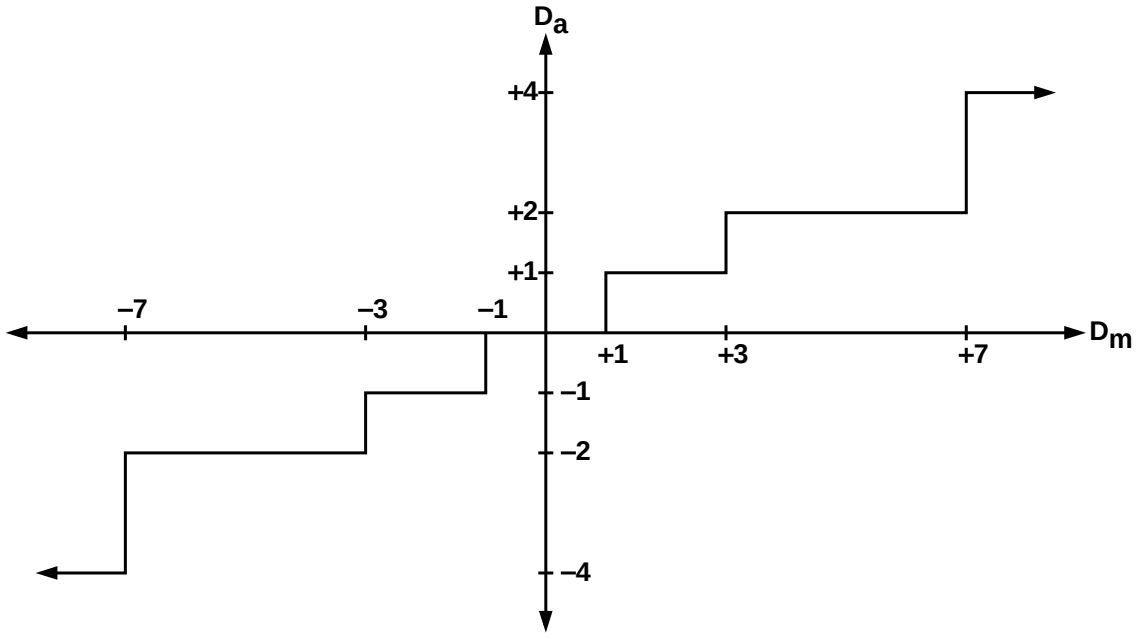

Figure 4.13: D_m-to-D_a mapping function.

by the following DSM. Both the transconductor and the opamp are simple folded-cascode opamps. The DSM is operated at a clock frequency of 78.125 MHz. The internal feedback in the DSM is a one-bit current-steering DAC with an output current of $I_s = 40\ \mu$A. The DSM can resolve a current mismatch ΔI_j as large as $\pm I_s/(R_L G_m) = \pm 242I$. A ΔI_j of $1I$ corresponds to a $D_m = 15$.

The calibration path shown in Figure 4.14 includes a transconductor G_m and an opamp. They exhibit offsets due to device mismatches. The offsets introduce errors in the DSM measurements. Assume the 1st M-DAC current cell is under calibration. During the $Z[k]$ zero phase, I_L is modulated by $R_0[k]$ and $I_{M,1}$ is modulated by $\overline{R}_0[k]$. Neglecting the DSM conversion gain, the corresponding digital output D_m can be expressed as

$$D_{m1} = +I_L - I_{M,1} + \text{Offset} \tag{4.4}$$

The offset must be removed from the measurement data. To find the offset, an additional calibration measurement is performed at the beginning of each calibration cycle. During the $Z[k]$ zero phase of this measurement, I_L is modulated by $\overline{R}_0[k]$ and $I_{M,1}$ is modulated

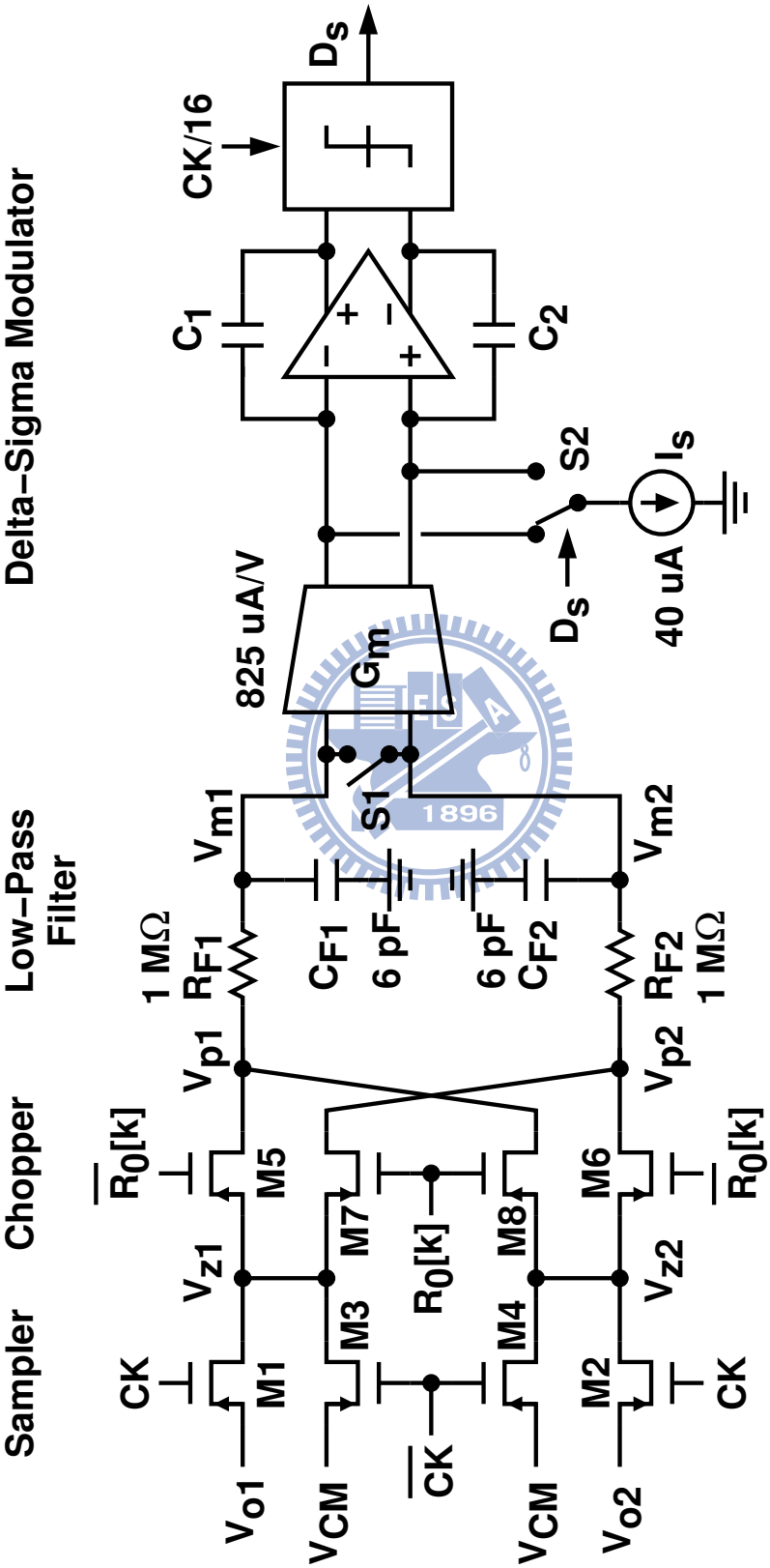

Figure 4.14: Schematic of the calibration analog signal path.

by $R_0[k]$. The resulting digital output D_m can be expressed as

$$D_{m2} = -I_L + I_{M,1} + \text{Offset} \tag{4.5}$$

Thus, the offset is obtained by applying $(D_{m1} + D_{m2})/2$. This acquired offset is subtracted from the subsequent measurement data. Every calibration cycle includes one offset measurement and 63 mismatch measurements. The acquired offset is updated in every calibration cycle.

As shown in Figure 4.10, due to the finite bandwidth of the V_o port, the sampled signal V_z contains the return-to-zero tails of V_o. They are scrambled by $R_0[k]$ and reduced by the following LPF and DF. The remaining residues cause calibration errors. The residues can be reduced by increasing the DF down-sampling ratio. For this design, 2^{18} consecutive D_s data are accumulated for every D_m. This DF down-sampling ratio allows the worst-case V_z, in which the sampled V_o holds its last data-phase value throughout the zero phase and never decays.

With a DF down-sampling ratio of 2^{18}, one calibration measurement takes 3.34 msec. Since one calibration cycle requires 64 measurements, it takes 214 msec to complete one calibration cycle. During power up, it takes 9 calibration cycles or 1.93 sec for the calibration to converge if the initial M-DAC current cell mismatches are as large as $4.5I$. After that, the calibration only need to track the environmental variations, such as supply voltage and temperature variations. Although not implemented in this design, the calibration time for the initial power up can be reduced by setting input $D_i[k] = 0$ and then reducing the DF down-sampling ratio.

The calibration technique collects mismatch from output signal, and the output waveform is not in a square shape due to the finite output port bandwidth. As shown in Figure 4.10, V_z is the sampled residue during zero phase. After the chopper, the residue is moved to high frequency and mismatch information back to DC. In Figure 4.15, the high frequency residue is the calibration noise should be eliminated by LPF and DF, and the output port also cuts the shape of mismatch information. We define η_e as the collected gain ratio of mismatch information in one clock period. Assume that the output port is single pole dominated and η_e can be expressed in Equation (4.6).

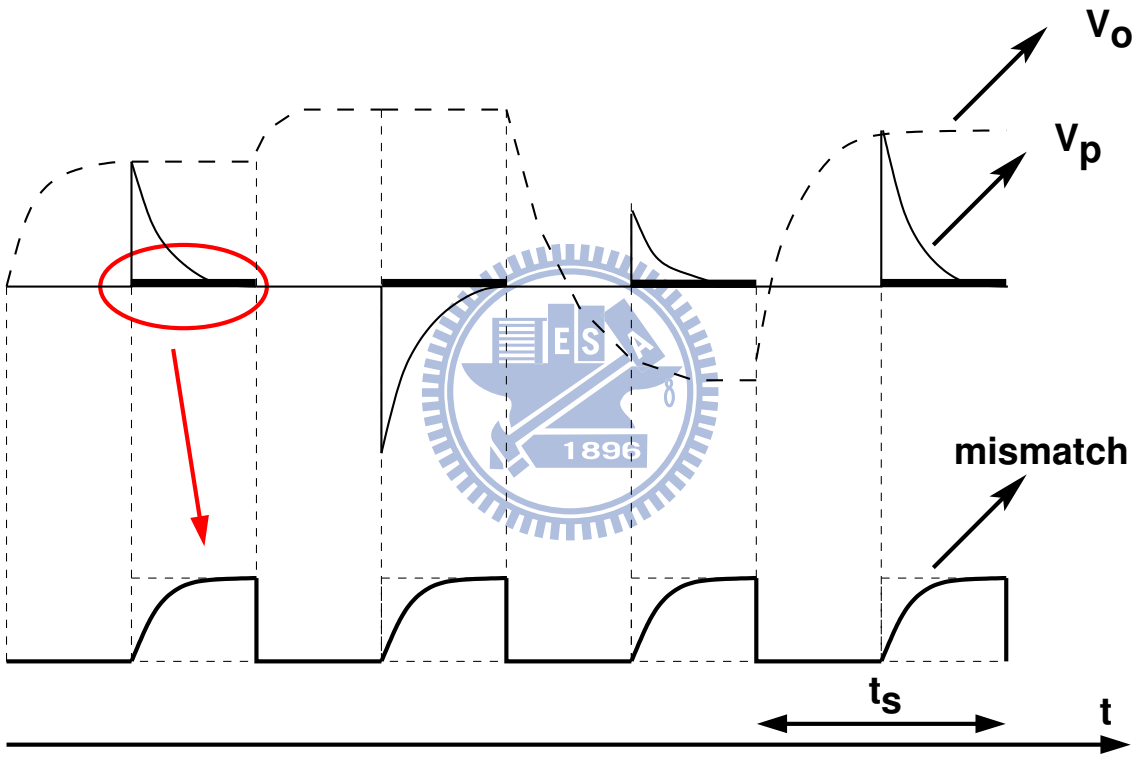

Figure 4.15: Mismatch information loss due to the finite output port bandwidth

$$\eta_e = \frac{\int_0^{t_s/2} R_L(I_L - I_{M,j})(1 - e^{\frac{-t}{\tau}})dt}{R_L(I_L - I_{M,j}) \cdot t_s} = \frac{\frac{t_s}{2} + \tau e^{\frac{-t_s}{2\tau}} - \tau}{t_s} \tag{4.6}$$

where t_s is the sampling clock and τ is the time constant of output pole. The calibration noise is the zero phase residue which can be treated as RC discharging and the initial voltage is the data phase signal, then the residue power ratio η in one clock period is expressed as

$$\eta = \frac{\int_0^{t_s/2} \left(V_o(t) \cdot e^{\frac{-t}{\tau}}\right)^2 dt}{V_o^2(t) \cdot t_s/2} = \frac{\tau}{t_s}(1 - e^{\frac{-t_s}{\tau}}) \tag{4.7}$$

These two factors, η_e and η, are calculated in time domain; moreover, they can be used in frequency domain. Assume that the output signal power spectrum density (PSD) is $S_o(f)$, and the PSD of V_z is $S_z(f)$, the node shown in Figure 4.14. V_z is the V_o with return-to-zero function and given by

$$S_z(f) = S_o(f) \cdot \frac{1}{2} sinc(\frac{f}{2f_s}) \cdot \eta. \tag{4.8}$$

The PSD of V_p is given by

$$S_p(f) = S_z(f) * S_c(f) \tag{4.9}$$

where $S_c(f)$ is PSD of chopper signal which is a random binary sequence and given by

$$S_c(f) = \frac{1}{L_c^2}\delta(f) + \frac{1 + L_c}{L_c^2} \sum_{n=-\infty, n\neq 0}^{\infty} sinc^2(\frac{n}{L_c})\delta(f - \frac{n}{L_c}f_s). \tag{4.10}$$

In Equation (4.10), L_c is the period of the random sequence. Then, the high frequency residue will be filtered by LPF and anti-alias filter of the DSM. Mismatch information is moved back to DC, thus it's mean can pass these two filters. The DSM and DF will accumulate the power of filtered residue and the mean amplitude of mismatch information. The in-band residue power denote as σ_n^2 which is easy to find in frequency domain. The decision equation is derived as

$$3 \cdot \sqrt{M_c} \cdot \sigma_n < M_c \cdot \frac{1}{2} \cdot (\frac{I}{8} \cdot R_L \cdot \eta_e) \tag{4.11}$$

where M_c is the accumulation periods refer to DSM clock, 1/16 of the system clock, the last term is the unit step of the calibration DAC through the calibration path. When output signal V_o is low frequency, we need longer M_c to extract the mismatch.

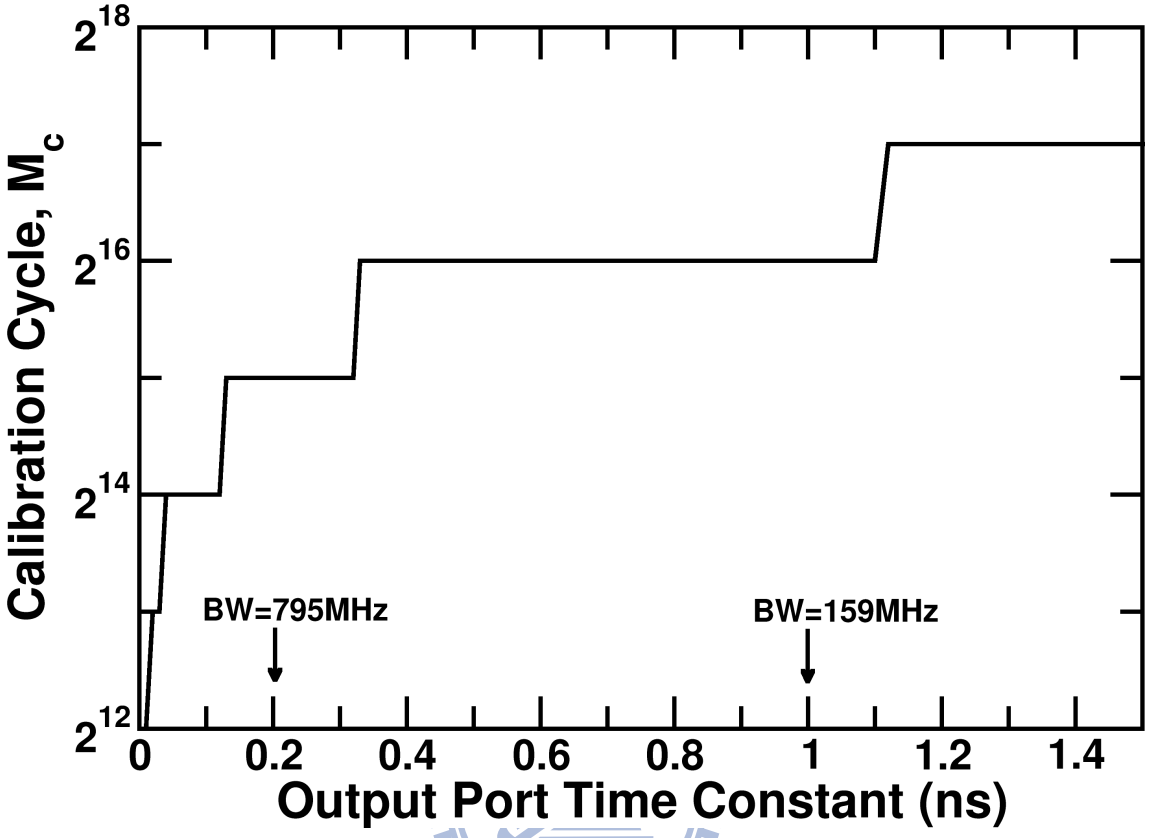

Figure 4.16: Calibration cycle vs. output port bandwidth

Output port bandwidth effects both the value of η_e and η. Figure 4.16 shows that the different output port time constant versus the length of calibration cycle M_c. The figure is calculated by MATLAB and assume that the output signal is a very low frequency sinewave since the worst case occur. If τ is 0.32 nsec., $M_c = 2^{15}$ is required and $L_c = 16 \times M_c = 2^{19}$ periods. Because the off-chip output loading is hard to estimate, we use $M_c = 2^{18}$. At this condition, one M-DAC cell takes 3.3 msec of calibration time and once the M-DAC requires 214msec.

4.5 Experimental Results

The DAC was fabricated using a standard 90 nm CMOS technology. All functional blocks shown in Figure 4.9 are integrated, except the V_o resistive loads R_{L1} and R_{L2}. Figure 4.17 shows the chip photograph. The DAC core area is 1100 × 750 μm^2. The area of a single

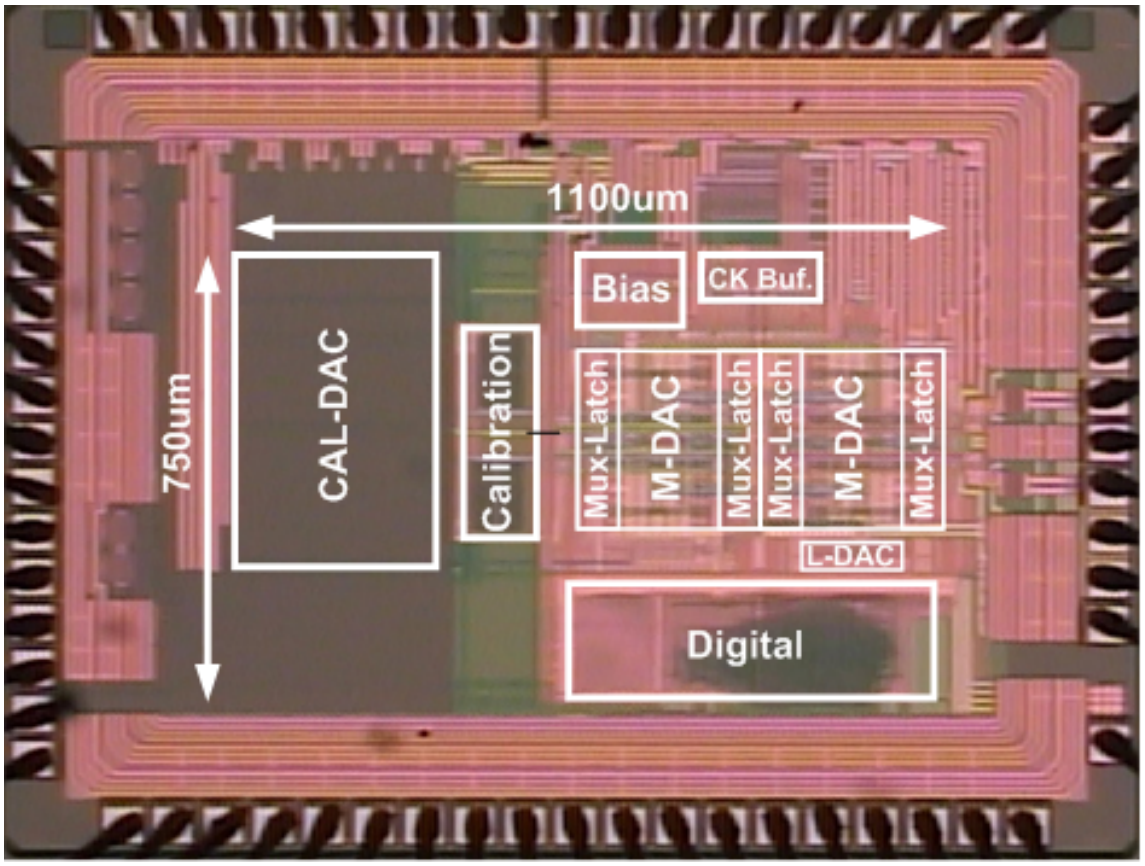

Figure 4.17: Microphotograph of the DAC.

M-DAC current cell is 90 × 12 μm^2. The chip also includes a direct digital frequency synthesizer (DDFS) to generate digital inputs for DAC dynamic testing. The synthesizer can also generates ramp waveforms for DNL and INL measurements.

The measured DNL and INL before calibration is shown in Figure 4.18. In our design, the device dimensions and bias conditions for the L-DAC current cells are different from those for the M-DAC current cells. In addition, this DAC floor plan does not employ common-centroid scheme to reduce the gradient effects. As a result, the raw DNL and INL are poor. The DNL is $+4.5/-0.5$ LSB and the INL is $+10.2/-7.1$ LSB. Figure 4.18 shows the measured DNL and INL after current-cell calibration. The DNL is improved up to $+0.47/-0.51$ LSB and the INL is improved up to $+1.0/-1.2$ LSB.

Figure 4.20 shows the measured DAC full-scale transient response. The 10%-to-90% rising time is 0.5 nsec, which corresponds to an output-port bandwidth of 700 MHz. For this DAC, the DRRZ operation is applied to its differential output current I_o. Its differential output voltage V_o may not return to zero due to the finite output-port bandwidth. Both the DRRZ and the current-cell background calibration can operate and be effective under any output-port bandwidth. They put no restriction on choosing output-port bandwidth.

The DAC output spectra are measured during the single-tone tests. The DAC is operated at 1.25 GS/s sampling rate. shows the output spectrum of the DAC without calibration and DRRZ. The spectrum is spurious with the 2nd, 3rd and 5th order distortions which are cause by the static linearity. We measured the output voltage of each digital input and then use MATLAB to run a FFT test shown in Figure 4.25. This the first step to check if the measurement environment for dynamic test is ready. Figure 4.22 shows the output spectrum when the input frequency is 40 MHz. The DAC is calibrated and the DRRZ is turned off. The SFDR is 73.3 dB. At low input frequencies, the CDST effect is low. The SFDR is dictated by the DAC static linearity. In this design, the static linearity is achieved by calibration. Figure 4.23 shows the DAC output spectrum with the input frequency increased to 477 MHz. The SFDR is degraded to 58.8 dB by the CDST effect. Figure 4.24 shows the DAC output spectrum with the DRRZ enabled. The SFDR recovers to 73.6 dB. The DRRZ mitigates the CDST effect.

Several sources contribute the random noises at DAC output. They are estimated as follows. (1) The total quantization noise power is $\overline{I_{n1}^2} = I^2/12$. Assume the signal band-

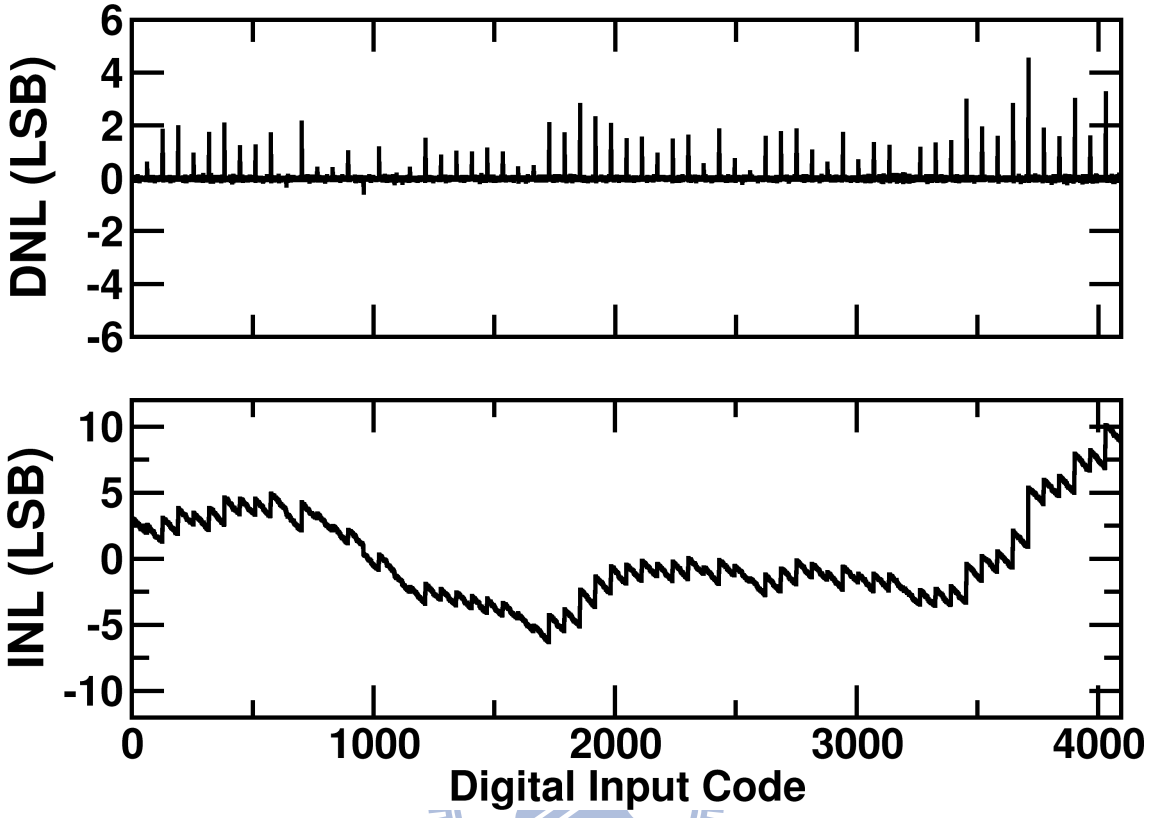

Figure 4.18: Measured DNL and INL before current-cell calibration.

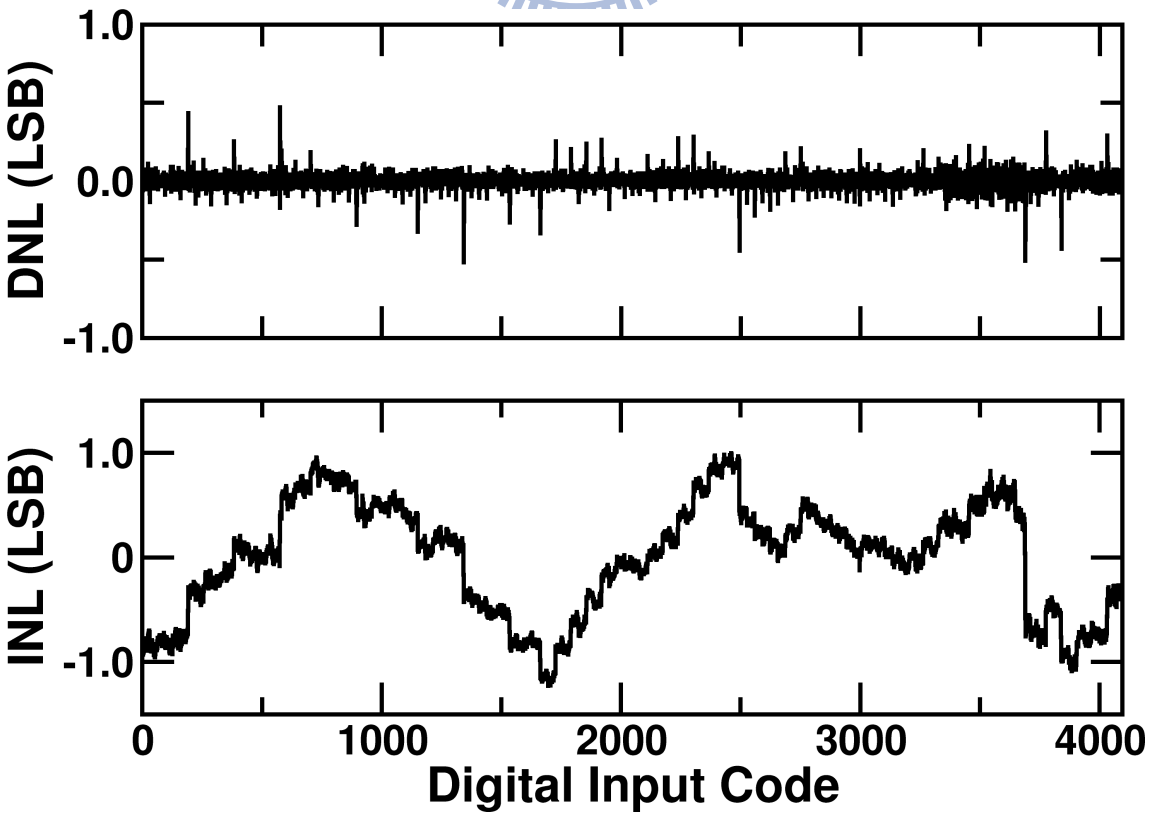

Figure 4.19: Measured DNL and INL after current-cell calibration.

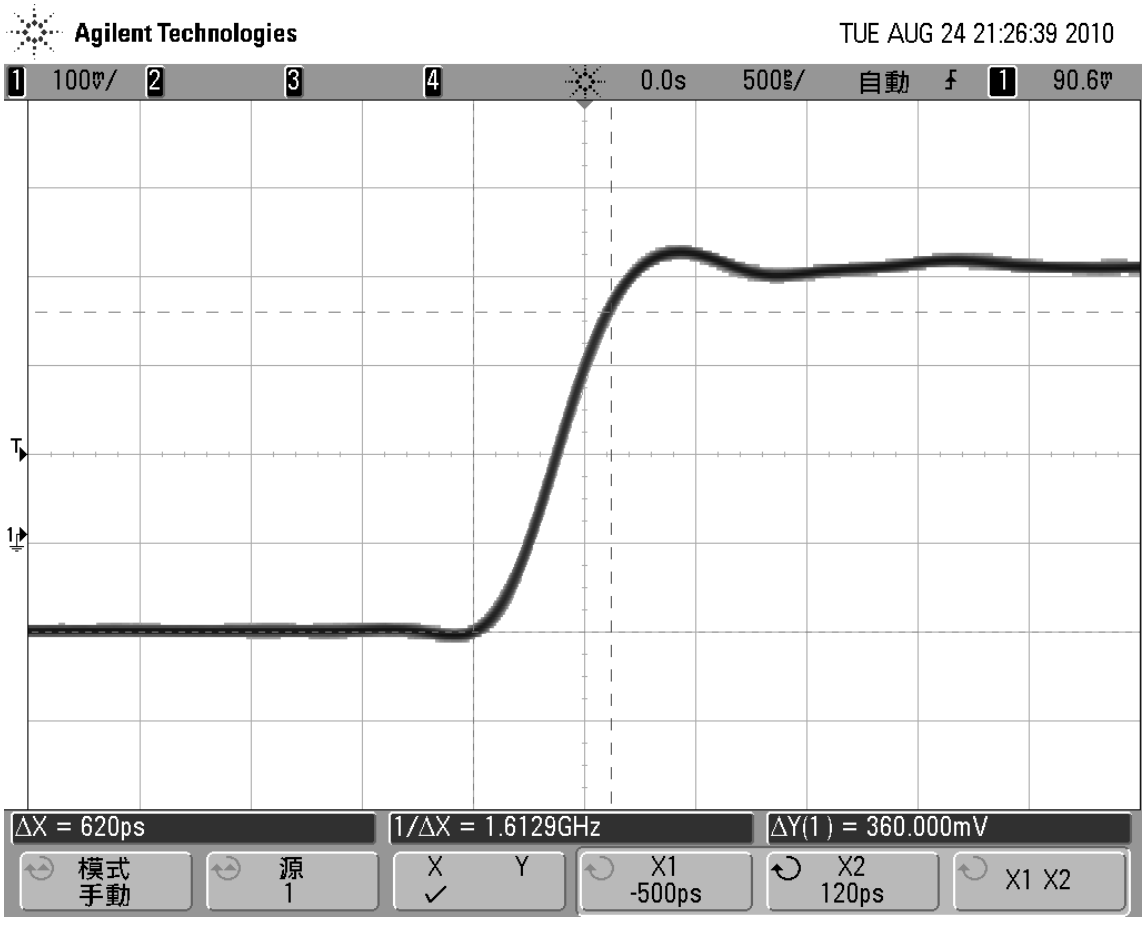

Figure 4.20: Measured DAC full-scale transient response.

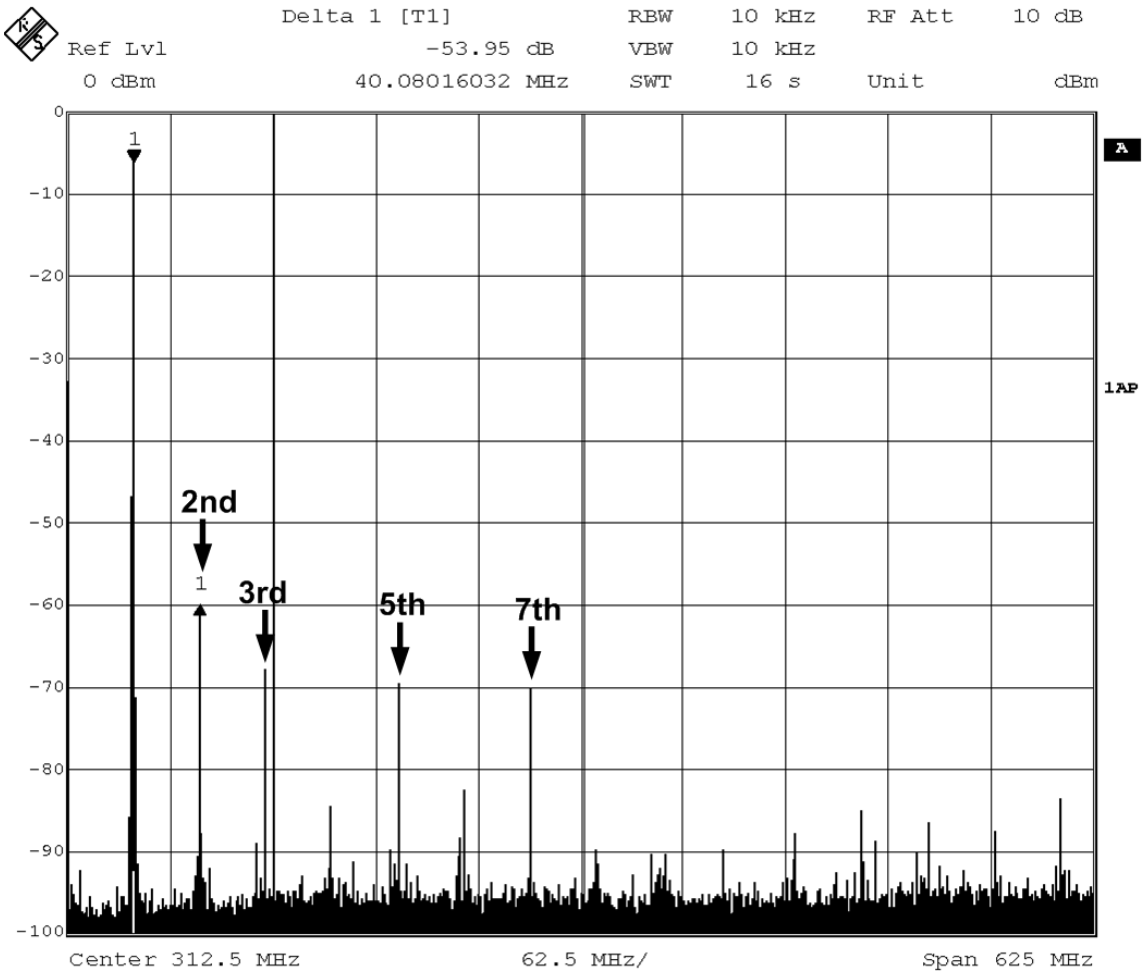

Figure 4.21: Measured DAC output spectrum without calibration and DRRZ. Sampling rate is 1.25 GS/s. Input frequency is 40 MHz.

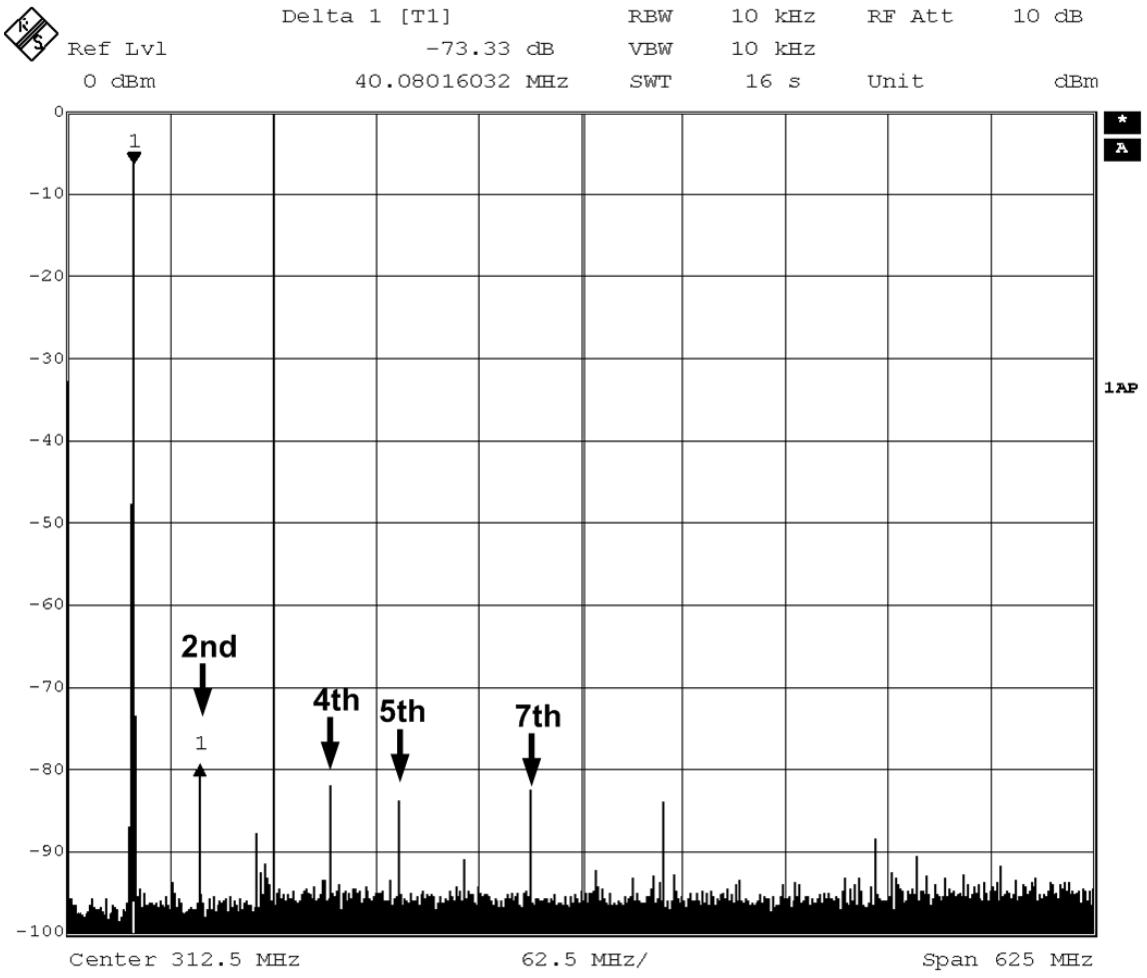

Figure 4.22: Measured DAC output spectrum after calibration but without DRRZ. Sampling rate is 1.25 GS/s. Input frequency is 40 MHz.

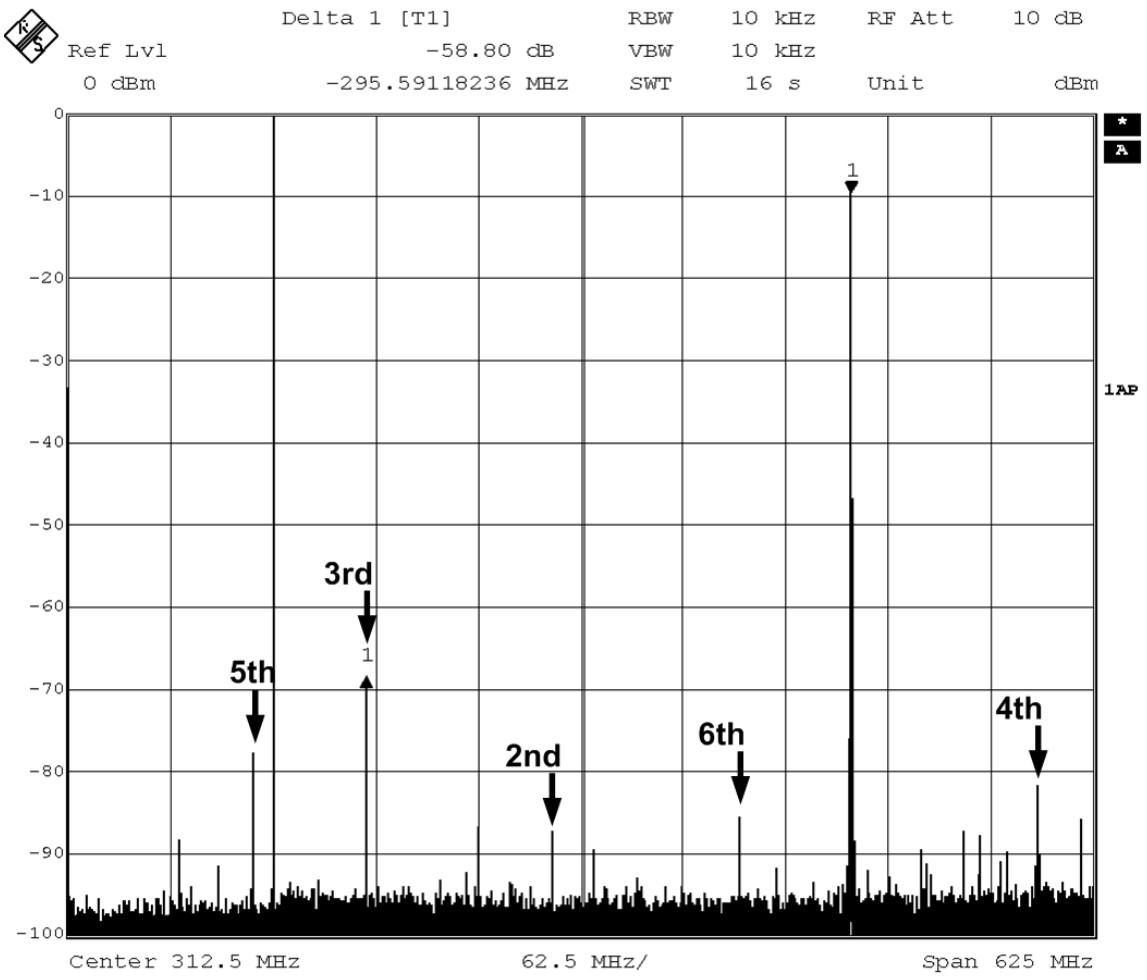

Figure 4.23: Measured DAC output spectrum after calibration but without DRRZ. Sampling rate is 1.25 GS/s. Input frequency is 477 MHz.

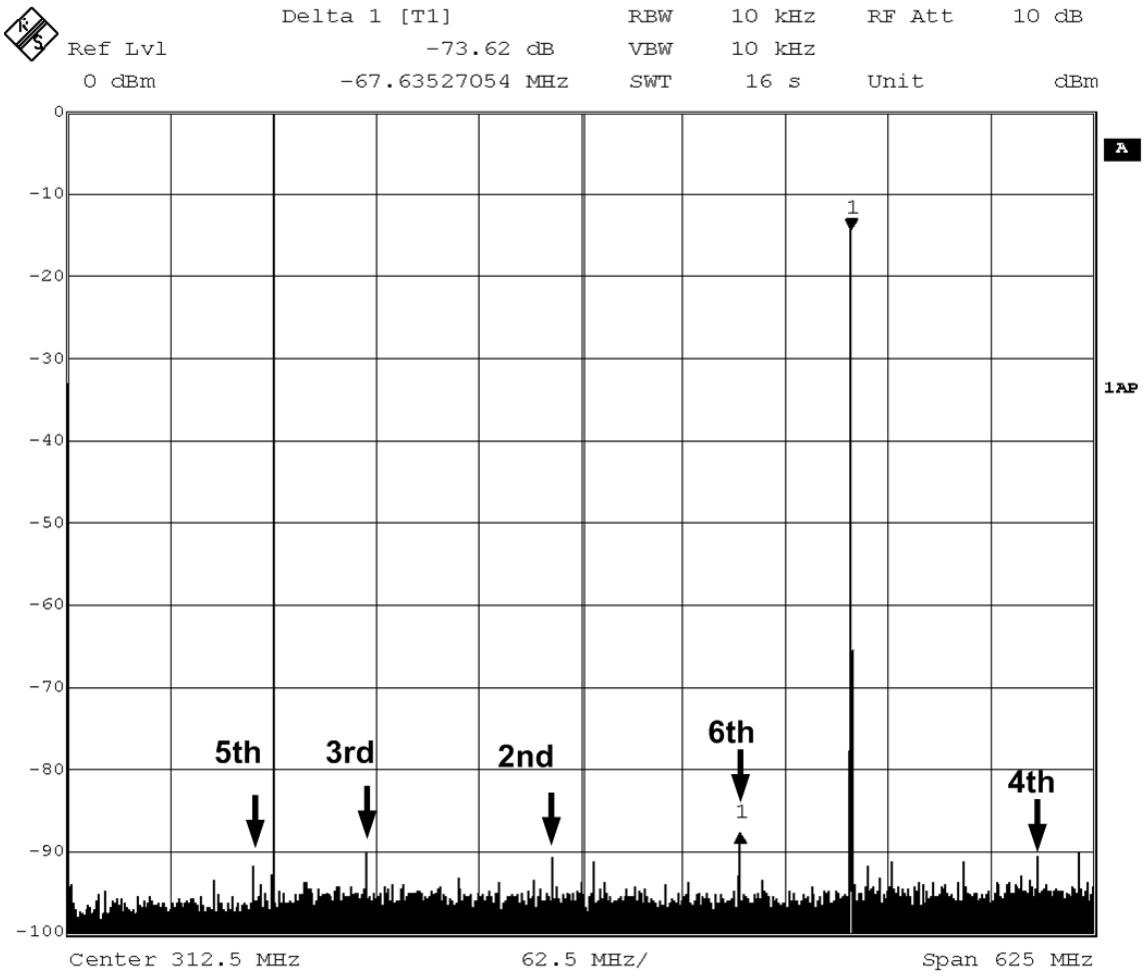

Figure 4.24: Measured DAC output spectrum after calibration and with DRRZ. Sampling rate is 1.25 GS/s. Input frequency is 477 MHz.

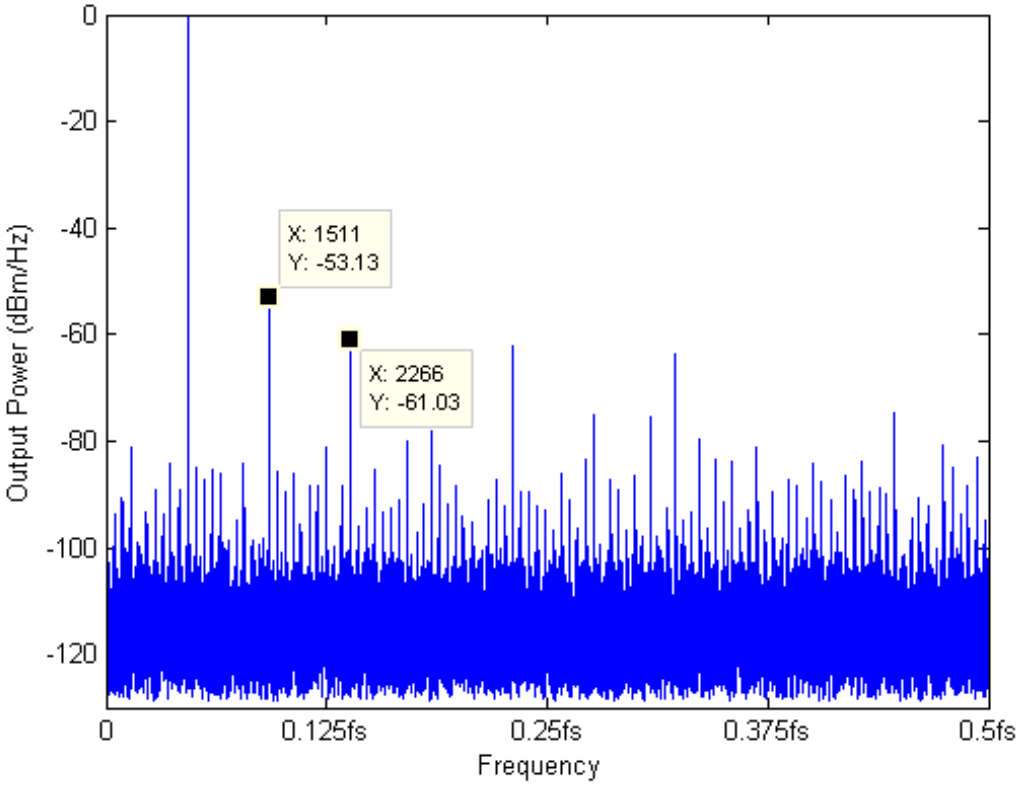
0
-20
-40
-60
-80
-100
-120
Output Power (dBm/Hz)
X: 1511
Y: -53.13
X: 2266
Y: -61.03
0
0.125fs
0.25fs
0.375fs
0.5fs
Frequency

Figure 4.25

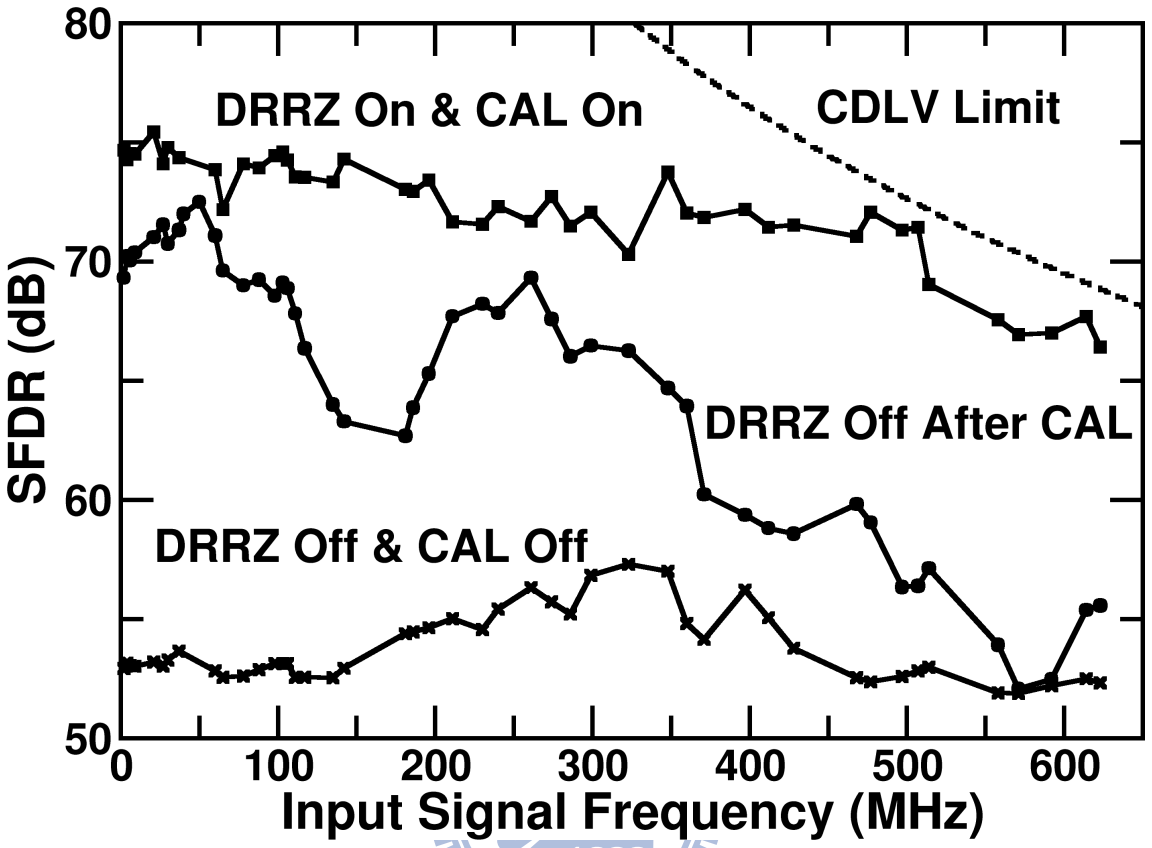

Figure 4.26: Measured SFDR versus input frequencies

width is 625 MHz. The current power density is $\overline{I_{n1}^2}/\Delta f = 2.13\times10^{-21}$ A^2/Hz. The corresponding noise spectral density (NSD) received by the SA is NSD$_1 = -165.74$ dBm/Hz. (2) The current sources in the DAC contain device thermal noises. From simulation, the total DAC output current density due to these thermal noises is $\overline{I_{n2}^2}/\Delta f = 2.05 \times 10^{-21}$ A^2/Hz. The corresponding NSD received by the SA is NPD$_2 = -171.93$ dBm/Hz. (3) Comparing Figure 4.23 to Figure 4.22, the power increase in the harmonics is $\Delta P_{st} = 10^{-7}$ mW as input frequency is increased. Assume ΔP_{st} is induced entirely by the CDST effect, and it is spread from 0 Hz to $f_s/2$ by the DRRZ. The resulting NSD is NSD$_3 = \Delta P_{st}/(f_s/2) = -158$ dBm/Hz. The SA in our measurement setup has a noise floor of -140 dBm/Hz by itself. It is too high for the SA to measure the DAC output noises directly.

Figure 4.26 shows the measured SFDR versus input frequencies. If the DAC is not

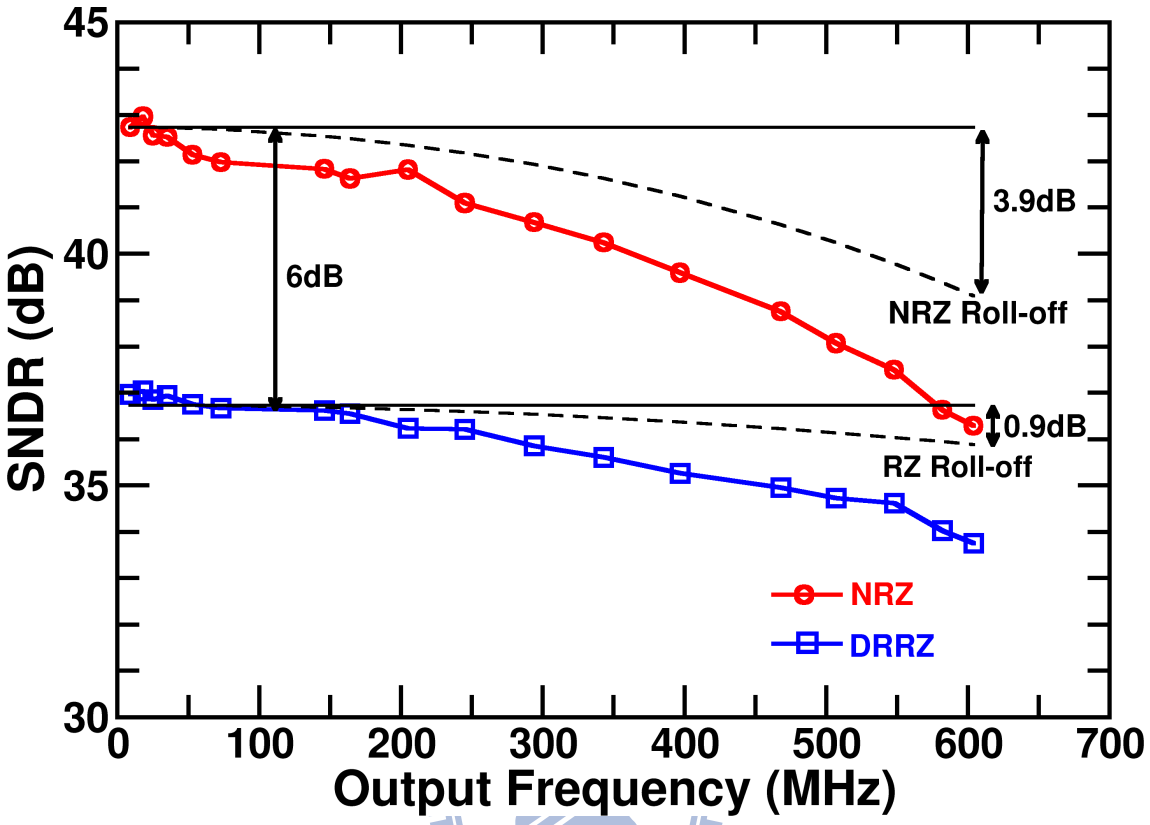

Figure 4.27: Measured SNDR versus input frequencies. The SNDR of the DAC is limited by the Signal Analyzer

calibrated, the SFDR exhibits no significant change by varying input frequency. The DAC static linearity dominates the SFDR performance. Once the DAC is calibrated, and if the DRRZ is turned off, the CDST effect is the main source of SFDR degradation. When the DAC is calibrated and the DRRZ is turned on, the SFDR is better than 70 dB for input frequencies up to 500 MHz. Also shown in Figure 4.26 is the CDLV effect calculated with Equation (4.1). In this design, the CDLV effect becomes relevant only when the input frequency is higher than 550 MHz.

Table 4.2 summarizes the DAC specifications. Figure 4.28 compares the SFDR performances of several high-speed DAC published in recent years. Our design has the best dynamic performance.

Figure 4.28 compares the SFDR performance of several high-speed DAC of which the sampling rate is higher than 0.5 GS/s and the resolution is better than 12 bits. Table 4.3

Table 4.2: DAC specifications

Technology	CMOS 90 nm
Resolution	12 bits
Update Rate f_s	1.25 GS/s
DNL	+0.47/−0.51 LSB
INL	+1.0/−1.2 LSB
SFDR @ f_{sig} = 30 MHz SFDR @ f_{sig} = 500 MHz	75.5 dB 71.7 dB
70 dB SFDR Bandwidth	510 MHz
Load Current	16 mA
Output Voltage Swing	0.8 Vpp
Power Supply (Analog/Digital)	2.5/1.2 V
Power Consumption	128 mW
Core Area	1100 × 750 μm^2

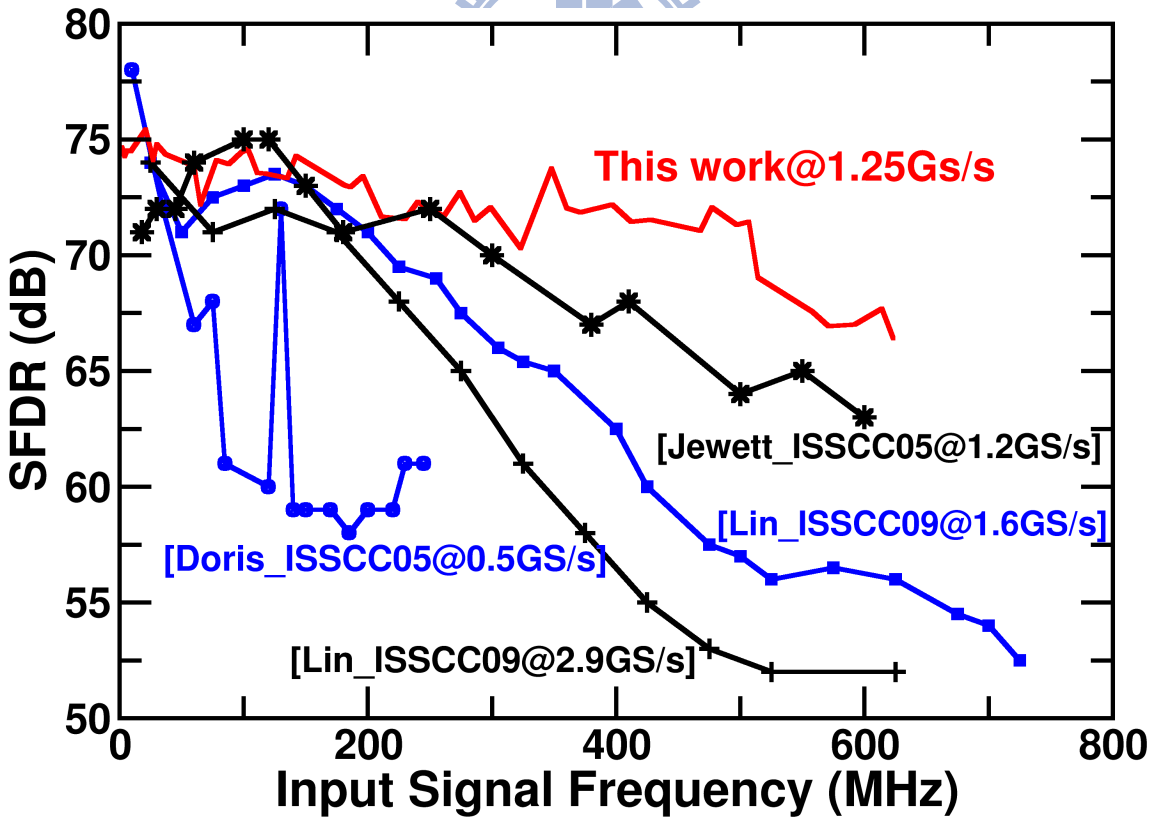

Figure 4.28: SFDR performance comparison.

Table 4.3: Comparison of Published High-Speed DACs.

	This Work	[7]	[8]	[34]
Technology (nm)	90	180	350	65
Core Area (mm^2)	0.825	1.13	30.6	0.31
Supply (V)	1.2/2.5	1.8	3.3	1.0/2.5
P_{Total} (mW)	128	216	6000	188
Resolution (Bits)	12	12	15	12
f_s (GS/s)	1.25	0.5	1.2	2.9
I_L (mA)	16	15	N/A	50
P_{Load} (dBm)	−7	+1.5	0	+9
SFDR_{LF} (dB)	75	78	75	74
$\text{SFDR}_{f_s/2}$ (dB)	66	62	63	52
FOM ($10^4 \times$ GHz/mW)	7.36	1.55	0.11	2.24

The technology used in [8] is BiCMOS.

lists their specifications. In Table 4.3, f_s is the sampling rate, I_L is the maximum output current, P_{Load} is the low-frequency sinewave power delivered to the DAC output load, SFDR_{LF} is the SFDR at low input frequency, and $\text{SFDR}_{f_s/2}$ is the SFDR at $f_s/2$ input frequency. The figure of merit (FOM) is defined as

$$\text{FOM} = \frac{2^{\text{ENOB}_{\text{LF}}} \times 2^{\text{ENOB}_{f_s/2}} \times f_s}{P_{\text{Total}} - P_{\text{Load}}} \tag{4.12}$$

where $\text{ENOB}_{\text{LF}} = (\text{SFDR}_{\text{LF}} - 1.76)/6.02$ and $\text{ENOB}_{f_s/2} = (\text{SFDR}_{f_s/2} - 1.76)/6.02$. There are various FOM definitions for DAC comparison [12]. None of the existing definitions is universally endorsed. The FOM of Equation (4.12), first defined in [21], includes the DAC dynamic performance at high input frequency.

4.6 Summary

The static linearity of a current-steering DAC is governed by the matching of its internal current sources. Its dynamic performance is degraded by both the code-dependent switching transient (CDST) effect and the code-dependent loading variation (CDLV) effect. The random return-to-zero (DRRZ) operation can eliminate the CDST effect. Adopting a compact current cell design can mitigate the CDLV effect. The DRRZ also facilitates a current-cell background calibration scheme that can correct the mismatches among DAC

internal current sources due to device variations. We designed a CMOS 12-bit 1.25-GS/s current-steering DAC to demonstrate the above design techniques. As a result, the DAC achieves a SFDR better than 70 dB up to 500 MHz input frequency.


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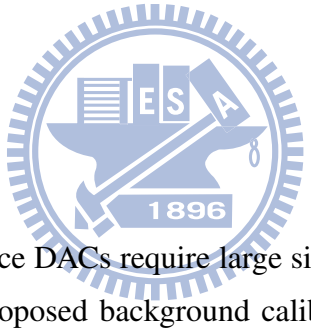
Chapter 5

Conclusions and Future Works

5.1 Conclusions



High-speed and high-performance DACs require large signal bandwidth and low switching noise. In this thesis, we proposed background calibration which allows the use of small size current cells. Then, the signal bandwidth can extend. The DAC is insensitive to the PVT variations and slow time-variant error. We also proposed a Digital Random Return-to-Zero to randomize the code-dependant switching transients rather than elimate the transients. The switching transients contribute to harmonic distortions and would damage the adjcent channel. The DRRZ technique relax the spur-expression requirement of reconstruction filter. Moreover, the induced noise power is spread into all the Nyquist band, and only a portion of noise into the channel power.

Finally, all the experimental Results were verified by these two high-speed DACs. The results show the theory was truth and can be implemented in silicon. The 8-bit 1.6-GS/s current-steering DAC shows an 14 dB improvement in SFDR when the input frequency is 800 MHz. The 12-bit 1.25-GS/s current-steering DAC achieves a SFDR better than 70 dB up to 500 MHz input frequency.

5.2 Recommendations for Future Investigation

This section presents several suggestions for future investigations for these high-speed and high-resolution DACs.

- To develop technique to improve the output power efficiency. The RZ output loss 6 dB signal power; however, anti-droop filter can be avoided in RZ DACs.
- To analysis the additional noise power caused by DRRZ.
- The CAL-DAC design optimization is needed. The mismatch information of the M-DAC cells are saved in local latch which occupied large area. Also the CAL-DAC can be implemented in more low cost way.

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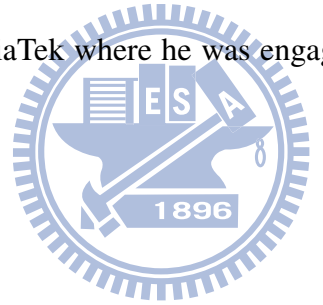
自傳

Wei-Hsin received the B.S. degree from the department of electrical engineering, National Cheng Kung University(NCKU), Tainan, Taiwan, R.O.C., in 2002. From 2002 to 2011, he worked toward the M.S. and Ph.D. degree in electronics engineering with the National Chiao-Tung University, Hsinchu. His current research interest is high-speed high- resolution data converters design.

In 2010, he joined the MediaTek where he was engaged in the design of analog and mixed-signal ICs.



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- Journal Paper:
  - **W.-H. Tseng**, J.-T. Wu, and Y.-C. Chu, “A CMOS 8-bit 1.6-GS/s DAC with digital random return-to-zero,” IEEE Trans. Circuits Syst. II, vol. 58, no. 1, pp. 1 - 5, Jan. 2011.
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