國　立　交　通　大　學
電　控　工　程　研　究　所

博　士　論　文

單級並聯型升壓返馳式轉換器

Single-Stage Parallel Boost-Flyback Converter

研　究　生：李恆毅

指導教授：張隆國　博士

陳鴻祺　博士

中華民國九十九年五月

單級並聯型升壓返馳式轉換器

Single-Stage Parallel Boost-Flyback Converter

研 究 生 ： 李 恆 毅　　Student: Heng-Yi Li

指 導 教 授 ： 張 隆 國 博 士　　Advisor: Dr. Lon-Kou Chang

陳 鴻 祺 博 士　　Dr. Hung-Chi Chen

國 立 交 通 大 學

電 控 工 程 研 究 所

博 士 論 文

A Dissertation

Submitted to Institute of Electrical Control Engineering

College of Electrical Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

in

Electrical Engineering

May 2010

Hsinchu, Taiwan, Republic of China.

中華民國九十九年五月

單級並聯型升壓返馳式轉換器

研究生：李恆毅　　指導教授：張隆國 博士/ 陳鴻祺 博士

國立交通大學電控工程研究所

摘要

無論單級式或兩級式交直流轉換器，均有部份電能會重覆處理或循環。因此，本論文應用了並聯式功因校正的概念，提出了一種嶄新的單級並聯式功率因數校正設計。此設計係利用升壓-返馳半級（包括升壓單元和返馳單元）產生兩條並聯電能處理路徑。主要的輸入功率經反馳單元轉換後即輸出至負載，而剩餘的功率經升壓單元處理，再儲入大型電容，然後被直流-直流半級取出作為輸出功率調節。理論分析證實，只要升壓單元和反馳單元運轉於非連續模式，且工作週期和切換頻率維持固定，減少升壓電感可提昇功率因數。因大部份功率僅經一次處理，故轉換效率提高和開關電流應力降低。在此架構中，可將返馳單元和直流-直流半級作不同電路的替換，而衍生其它不同的轉換電路。

本論文以單級並聯式升壓-反馳-反馳轉換器為對象，分析電路的運轉模式和各元件的平均切換週期信號，提出功率分配和大型電容電壓之影響參數、設計方程式和設計程序。藉著遵循設計程序，一個 80 瓦泛用電壓的原型被建置。實驗結果顯示，在使用範圍的最壞條件下，測得的諧波電流仍符合 IEC61000-3-2 class D 限制，最高大型電容電壓為 415.4 伏特，最大轉換效率達 85.8%。

從上述電路分析得知，轉換器在半個線週期也會有兩個操作模式，其中之一模式，工作週期需隨著線電壓相位改變而改變以維持輸出恆定。這種工作週期可變之轉換器的小信號轉移函數無法以傳統頻率響應量測證實。因此，藉著建立各模式的小信號模型和提出模式分界點補償器的設計方法，使轉換器的動態響應在操作範圍內具有較小的穩態誤差、快速上升時間和大量阻尼。最後，並聯式轉換器的動態模型和所設計的補償器，以模擬和實驗在時域內得以證實。

關鍵字：交直流轉換器，並聯式功因校正、返馳式轉換器。

Single-Stage Parallel Boost-Flyback Converter

Student: Heng-Yi Li Advisor: Dr. Lon-Kou Chang/ Dr. Hung-Chi Chen

Institute of Electrical Control Engineering
National Chaio Tung University

Abstract

It is known that part of the power is repeatedly processed or recycled in the conventional single-stage (S^2) and two-stage AC/DC converters. Therefore, a novel S^2 scheme is presented based on the parallel power factor correction (PPFC). In the scheme, the boost-flyback semi-stage containing boost cell and flyback cell is used to generate two energy processing path. The main input power flow stream is processed only by flyback cell and output to load directly. And the remaining input power stream is stored in bulk capacitor by boost cell and then transferred by DC/DC semi-stage to output for regulating output power. Theoretical analysis shows that as the boost cell and flyback cell operate in DCM and duty ratio and switching frequency are kept constant, using smaller boost inductor can result in higher power factor. Since most power is processed only once, the power conversion efficiency is improved and the current stress of control switch is reduced. The scheme can also be applied to other conversion circuits by replacing flyback cell and DC/DC semi-stage with other topology.

Taking the parallel boost-flyback-flyback converter as an example, the operation modes and average switching period signals are analyzed, the key parameters of power distribution and bulk capacitor voltage, design equations, and design procedure are also presented. By following the procedure, an 80 W universal prototype has been built and tested. The experimental results show that at the worst condition of operation range the measured line harmonic current complies with the IEC61000-3-2 class D limits, the maximum bulk capacitor voltage is about 415.4 V, and the maximum efficiency is about 85.8%.

It can be seen from the converter analysis, there are two operation modes in half line cycle and the duty ratio varied with line phase to keep output constant in one mode. The small signal transfer function of the converter with variable duty ratio cannot be validated with conventional frequency response measurement. Hence, the small-signal models of operation modes are built and the compensator design at the boundary of modes is presented, the dynamic response has small steady state error, fast rise time, and heavily damping within operation range. Finally, the dynamic model and designed compensator of parallel converter are verified in time domain by simulation and experiment.

Keywords: AC to DC converter, parallel power factor correction, flyback converter.

誌　謝

本論文完成，使我有『黑夜將盡，黎明破曉』的感覺。感謝神在黑夜中的引導，以及師長和同學的幫助。首先，要感謝我的指導教授張隆國博士，在前六年的研究生涯裡，由於他的啟蒙和教導，並在邏輯思考與論文寫作方面下了不少苦心，使我能完成論文，在此謹致最深忱的謝意與敬意。然後，還要感謝另一位指導教授陳鴻祺教授，在最後兩年給予後續的指正及幫助，使我能順利畢業。另外，要感謝廖德誠教授的經驗傳授和精神鼓勵，他的系統系性思考原則，幫助我化繁為簡，快速找到問題關鍵。感謝林君明教授的鼓勵，他的引導式的發問，使我能澄清重要的基本觀念。感謝潘晴財教授和廖聰明教授，也是令我景仰的學者，他們發表電源控制方面的著作對本研究極有幫助，而後續的指正以及寶貴的建議，也使得本論文更加地完整。

在這八年的博士生涯裡，要特別感謝晏銘，在我研究初期，給予許多資料、建議和協助，使我得以快速地步上研究軌道。感謝基漳所提供的實務經驗與協助。感謝 815 實驗室的歷屆學長、同學及學弟，以及阿暉，在研究上所提供的建議與協助，還有許多生活上的幫忙。感謝如璇，與我一同奮戰，從 815 實驗室經 740 室到 613A 室，並給我許多寶貴的訊息。感謝 613A 室的廖振宇和其他同學。感謝世澤，常常幫我下載資料及提供信息。感謝田叔叔、寶珠阿姨、板橋市召會的治平、俊宏等，感謝你們在精神上的鼓勵。感謝推薦我來進修的核研所曾錦清博士和關心我的同事。

最後要感謝我的家人，尤其是我所敬愛的雙親，平常幫忙照顧小孩，由於他們的支持與鼓勵，使我能全心全意的專注於功課與研究工作上。特別要感謝內人明珠對欣安、欣柔和興仁的照顧，讓我無後顧之憂地在交大完成博士學位。謹將此研究成果與榮耀獻給我的家人以及所有關心我的親朋好友！

李恆毅　2010 年初春

于新竹交大

Contents

List of Tables

List of Figures

Notation

The follow notations are adopted throughout this work.

AC/DC: ac-to-dc

BIFRED: boost integrated/flyback rectifier/energy storage/dc-to-dc converter

DC/DC: dc-to-dc

ICS: input current shaper

K_{DP}: direct power ratio

K_{IDP}: indirect power ratio

K_{M1}: inductance ratio

M_{CB}: voltage gain of boost cell

M_O: voltage gain of flyback cell

PF: power factor

PFC: power factor correction

PPFC: parallel power factor correction

SSTO: single-switch two-output

S^2: single-stage

S^4: single-stage-single-switch

TIBuck: two-input-buck

$\boldsymbol{T_{HL}}$: half line period

$\boldsymbol{T_L}$: line period

$\boldsymbol{T_S}$: switching period

$\langle \boldsymbol{x}(\boldsymbol{t}) \rangle$: moving average of $\boldsymbol{x}(\boldsymbol{t})$ over $\boldsymbol{T_S}$

$\boldsymbol{X}(\boldsymbol{t})$: the dc part of $\langle \boldsymbol{x}(\boldsymbol{t}) \rangle$ or $\boldsymbol{x}(\boldsymbol{t})$

$\tilde{x}(t)$: the ac part of $\langle \boldsymbol{x}(\boldsymbol{t}) \rangle$ or $\boldsymbol{x}(\boldsymbol{t})$

CHAPTER 1

INTRODUCTION

1.1 Background

Most electronic equipment is supplied by 60 Hz utility power by using the ac-to-dc (AC/DC) converter which is a diode rectifier followed by a bulk capacitor. Since these power converters absorb energy from the AC line only when the line voltage is higher than the DC bus voltage, the input line current contains rich harmonics, which pollute the power system and interfere with other electric equipment.

Hence, the power factor correction (PFC) has been widely employed for improving the power quality of the power converters. In conventional converters design, a two-stage structure as shown in Fig. 1.1 was usually employed for performing PFC and output regulation simultaneously, where the bulk capacitor C_B is in the power transfer path between the PFC stage and dc-to-dc (DC/DC) stage. This structure can give high power factor and high regulation simultaneously by using two independent controllers and power stages, but the cost of switching devices and the control circuitry is not easy to cut down especially in low power application. Although unity power factor is the ideal objective, it is no longer an essential requirement. According to the regulation IEC61000-3-2 [1], the power supplies of low power products such as computers, PC monitors and television sets have to comply with Class D limits as shown in Table 1.1. This fact promotes the development of the single-stage (S^2) AC/DC converter as shown in Fig. 1.2, such as boost integrated/flyback rectifier/energy storage/dc-to-dc converter (BIFRED) [2] and boost input current shaper (ICS) [3]-[8], which comply with the regulations without achieving unity power factor. In those designs two power stages were integrated into one stage by using only one controller and sharing the control switch so that the component count and cost could be reduced. However, these converters have the problems of high bulk capacitor voltage at high line and light load when PFC

semi-stage is operated in DCM and DC/DC semi-stage in CCM. Some alternative designs [5]-[8] using additional coupled feedback windings could reduce the bulk capacitor voltage, but they also result in dead angle in the input current so the input current distortion is increasing. Furthermore, it can be seen that part of the power is repeatedly processed or recycled in both the conventional two-stage and single-stage AC/DC converters.

To improve the power processing, the parallel power factor correction (PPFC) scheme as shown in Fig. 1.3 has been proposed in [9] and [10]. In those schemes, two parallel power flow paths are used and part of the input power is processed only once. Therefore, the converters could transfer power with higher efficiency. Since each path only transmits part of the whole conversion power, the components can be replaced with smaller ones. However, the PPFC design has complex circuit with special control scheme as mentioned in [11]. Another scheme of parallel power processing approach was presented on the base of two-output pre-regulator cascaded with two-input post-regulator [12]. Although the output capacitor is smaller and the power conversion efficiency is high, some extra implementation prices exist, such as, multiple switching devices and floating MOSFET driver. In addition, the output voltage range of the post-regulator is limited so it is not suitable for universal input, and it is a two-stage structure so it needs two controllers. The universal boost/forward converter presented in [14]-[15] makes use of an auxiliary transformer to reduce link voltage stress without inducing the dead angle of the line current. Hence, it inspires the parallel idea for the universal S^2 converter in this dissertation.

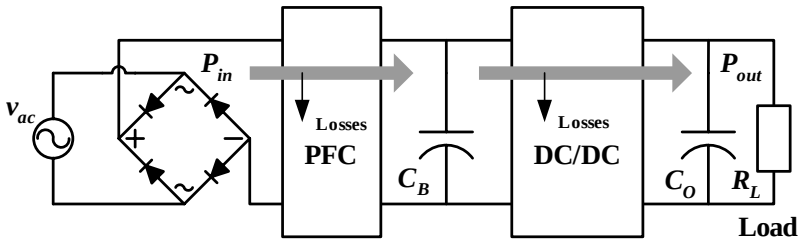


Fig. 1.1 Two-stage AC/DC converter scheme.

Table 1.1 Limits for class D equipment in standard IEC 61000-3-2

Harmonic wave Order n	Maximum permissible harmonic current per watt (mA/W)	Maximum permissible harmonic current (A)
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13	3.85/n	0.21
15≦n≦39		0.15×(15/n)

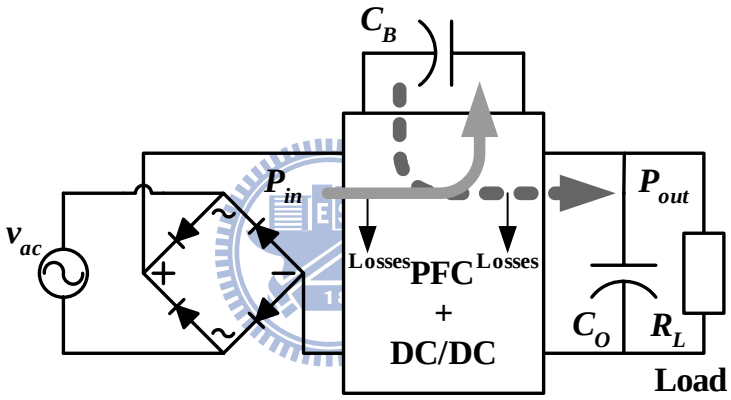


Fig. 1.2 Typical single-stage AC/DC converter scheme.

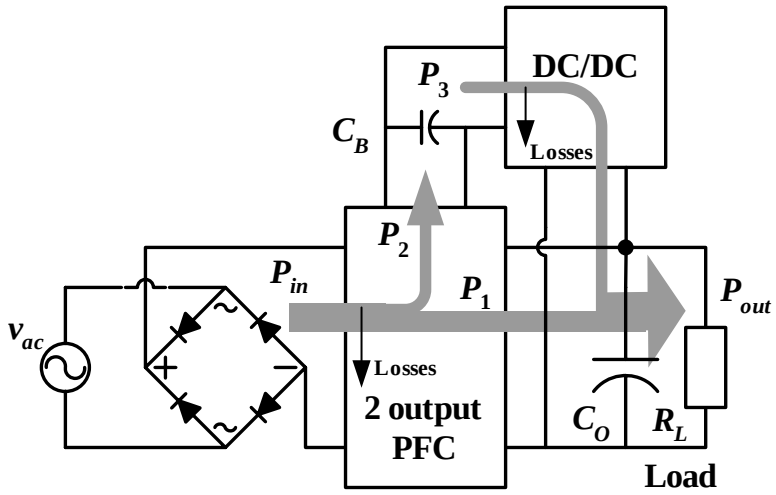


Fig. 1.3 Parallel power factor correction converter scheme.

1.2 Motivation

For the power relationship of an ideal PFC AC/DC converter as shown in Fig. 1.4, the ac input power (P_{in}) is a sine square function biased by constant output power (P_{out}). It is clear that 68% of line average input power (P_1) can be transferred to output directly through PFC stage, which is called the direct power. Only the remaining 32% of line average input power (P_2/ P_3) needs to be stored in C_B temporarily through PFC stage and taken off from the C_B through DC/DC stage. Since the processed powers are not directly transferred from ac input to dc output, they are called indirect powers. However, for conventional scheme, no matter whether it is a two-stage or a single-stage configuration as shown in Fig. 1.1 and 1.2, P_{in} is first transferred into somewhat pulsating dc power stored on C_B by the PFC stage. The power stored on C_B is processed again by the DC/DC stage to reach final P_{out} for load (C_O and R_L). The conversion efficiency of the double power processing is low, which is the product of the efficiency of each power conversion. In addition, these two processing stages are in cascade, they both have to handle whole input power. Fortunately the parallel scheme can transfer partial input power to output directly without going through DC/DC stage as shown in Fig. 1.3. Therefore, based on the aforementioned concept, a new family of S^2 parallel AC/DC converter is proposed in this dissertation to increase the direct power content percentage on the input power. The parallel converters are expected to have advantages of high efficiency and small rating components.

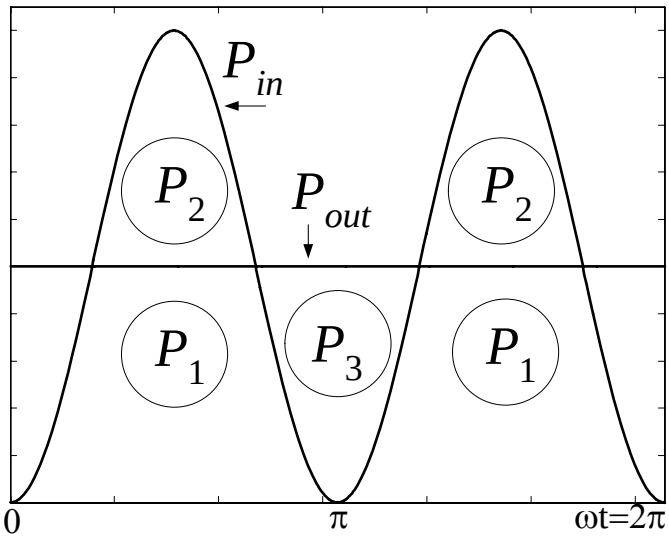


Fig. 1.4 Power relationship of ideal PFC converter.

1.3 Contributions of the Dissertation

This study proposes a new family of S^2 parallel AC/DC converter. In the circuits, the front semi-stage is of single-switch two-output (SSTO) boost-flyback configuration that works as a power factor corrector. Part of input power is processed only with the front flyback cell, and the remainder of input power is processed through the path along boost cell-C_B-DC/DC semi-stage. To illustrate the circuit and control of the proposed converter, several recently published low-power single-stage approaches are tabulated in Table 1.2. Only the proposed converter and those in [20-21] are implemented with single switch and single-loop controller. However, the efficiency of [20] is significantly lower than the proposed one and the component count of [21] is more than the proposed one. It can be seen from Table 1.2 that the circuits in [20], [21], and [13] have relatively small capacitor voltages. However, the circuit of [20] has the shortcoming of low efficiency. The circuit of [21] employs two bulk capacitors and multi-winding transformer to get low voltage. The circuit in [13] puts bulk capacitor on the secondary side of flyback transformer, which results in the low capacitor voltage. However, it also has the shortcomings of extra control switch and that the efficiency would decrease when universal voltage is applied. Though the bulk capacitor voltage in proposed con-

verter is higher than those in [13], [20], and [21], it is not higher than 450 V, the voltage limitation of commercial capacitors. Additionally, the use of single switch with small current stress, two parallel power streams with small components, and single-loop controller is a competitive advantage in the low-power universal applications. The modeling and control of the parallel converter is also presented. The technique can solve the model uncertainty problem and be generalized to other parallel converter.

Table 1.2 Recently published S^2 approaches

	Diode	Control switch	Magnetic components	Control	V_{CB} (V)	Switching frequency (kHz)	Input voltage (V_{rms})	Output voltage (V)	Output power (W)	Maximum efficiency (%)	PF (%) or compliance
[20] 2004	4	1	1 T with 3 windings + 1 L	Single controller	<375	96	90-264	5	60	73.2	IEC 1000-3-2 Class D
[21] 2005	7	1	1 T with 3 windings + 1 T + 1 L	Single controller UC3844	<260	100	85-265	28	150	83.2	>0.97
[13] 2007	2	2	1 T + 1 L	Single controller	<35	?	187-265	56	100	85.4	IEC 61000-3-2 Class D
[22] 2008	4	2	1 T + 1 L	Two controllers and logic	400	50	100-240	24	100	87	0.93-0.96 IEC 61000-3-2 Class D
[23] 2008	2	2	1 T with 6 windings	Single controller and logic	?	140	110-120	?	150	92	IEC 1000-3-2 Class D
Proposed	5	1	2 T + 1 L	Single controller UC3844	<415.4	100	85-265	54	80	85.8	0.91-0.99 IEC 61000-3-2 Class D

Letter T denotes transformer, letter L denotes inductor, V_{CB} denotes bulk capacitor voltage, mark '?' denotes that the item was not mentioned in the literature.

1.4 Dissertation Outline

This dissertation is composed of five chapters. The content of each chapter is briefly described as follows:

Chapter 1 introduces the background regarding the present power factor correction techniques and parallel converter concept. It then lists the research motivations and contributions.

Chapter 2 offers a review of conventional parallel AC/DC converters and introduces proposed parallel boost-flyback converter.

Chapter 3 analyzes the parallel boost-flyback-flyback converter by averaging method at first. Then, the power distribution and bulk capacitor voltage of the converter are studied. The design equations and procedure for universal application are also derived. In addition, the experiment results of 80 W prototype are presented.

Chapter 4 depicts the modeling and control of the parallel boost-flyback-flyback converter. The text contains the large signal model, small signal model, compensator design, simulation and experimental results.

Chapter 5 summarizes the conclusions of this work and presents suggestions for further work in related research directions.

CHAPTER 2

SYNTHESIS OF SINGLE-STAGE PARALLEL CONVERTERS

In the last decade, many efforts were made to implement the PPFC scheme for reducing power processing. However, besides efficiency, there are several aspects must be considered from the viewpoint of AC/DC converter, such as component count, circuit complexity, component voltage and current stresses, input current quality, etc. Thus, the main objective of this chapter is to present a topological study of the representative parallel converters and then propose a new family of parallel boost-flyback converters.

2.1 Review of Conventional Parallel AC-to-DC Converters

The concept and scheme of PPFC are first proposed by Y. Jiang *et al*. [9-10] and implemented with full bridge boost PPFC circuit as shown in Fig. 2.1. The circuit operates in two cases. For the case $P_{in} > P_{out}$, all switches act so that the partial input energy is transferred to load through T_1 directly and excess energy is put into C_B. Whereas, for the case $P_{in} < P_{out}$, all switches act so that the input energy is transferred to C_B and the stored energy in C_B is transferred to load through T_2.

The PPFC circuit shown in Fig. 2.1 clearly demonstrates that the power is through two parallel processing paths and partial input power is processed only once. However, the circuit contains two isolation transformers, fives switches and multi-loop control together with logic circuits. Complicated circuit structure may cause practical issues such as sophisticated operation mechanism, complex control, and thus difficult design and poor reliability. Thus, this converter would be good for those applications where the power level is high. For below a certain power level, it seems too complex and expensive.

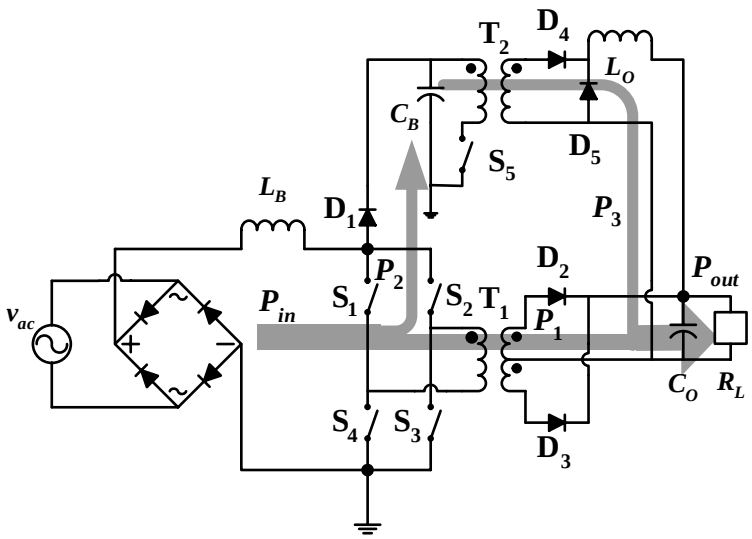
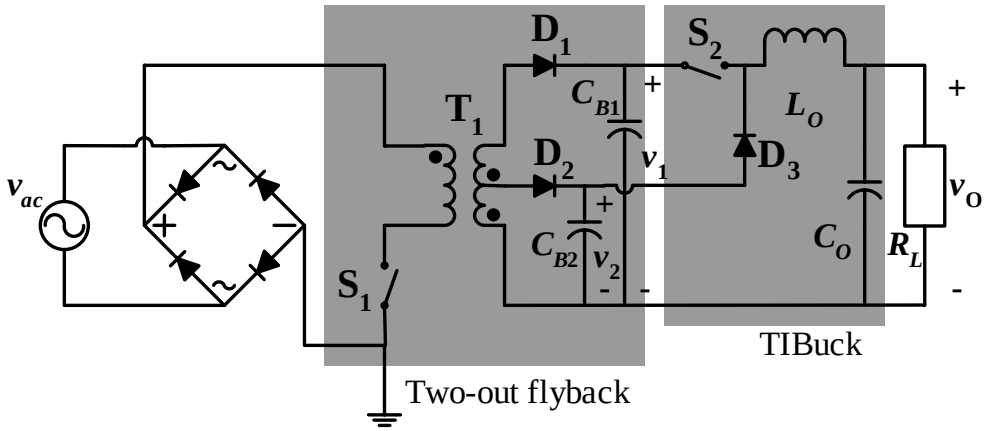


Fig. 2.1 Full bridge boost PPFC circuit [9-10].

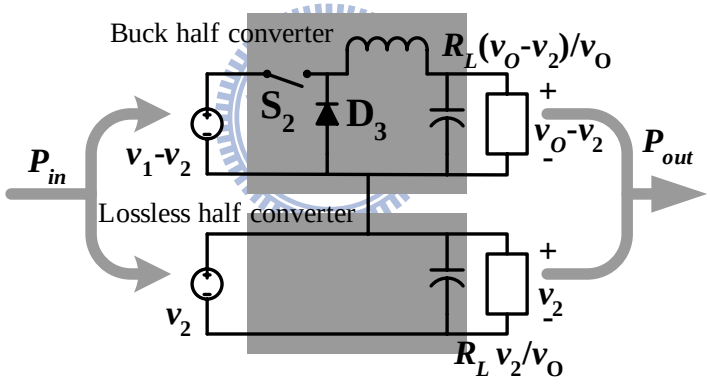
To simplify the circuit, another parallel method [12] that could improve the dynamic response of PFC stage with almost no efficiency penalty is shown in Fig. 2.2(a). In the circuit, the first stage is a two-output flyback converter, which supplies two “poorly regulated” (from the dynamic point of view) outputs instead of one, both at relatively close voltages. The second stage is a Two-Input-Buck (TIBuck) postregulator, which is highly efficient. From the static characteristic of view, the TIBuck postregulator is equivalent to two half converters in series as shown in Fig. 2.2(b). For the half converter at the top, it is a standard buck converter, whose input and output voltages are v_1-v_2 and v_O-v_2, respectively, and whose output load is R_L (v_O-v_2)/v_O. Besides, for the converter at the bottom, it works as a lossless converter, whose input and output voltages are v_2, and the load is R_L v_2/v_O. Therefore, the total output power comes up to the load following two different paths. A considerable fraction of the input power (typically 85%–90%) comes up to the load with no power processing, whereas the remaining power undergoes a power processing based on a buck topology, therefore, with a typical efficiency of 80%–95%.

Although the parallel method with TIBuck converter has the advantages of small output capacitor and high power conversion efficiency, some extra implementation prices exist, such as, multiple switching devices and floating MOSFET driver. In addition, the output voltage range

of the post-regulator is limited so as not suitable for universal input, and each stage needs individual controller.



(a)



(b)

Fig. 2.2 The parallel method with TIBuck converter: (a) Two-output flyback converter with TIBuck postregulator [12] and (b) equivalent circuit of TIBuck postregulator.

To realize the PPFC concept with a single stage topology, a single-switch PPFC AC/DC converter with flyback converter [20] is proposed as shown in Fig. 2.3. The concept is to create a voltage source that is parallel to the rectified input voltage source. When the line voltage is near the zero crossing area, the paralleled voltage source that is approximate to $V_{CB} \cdot N_1/(N_1 + N_2)$ provides the output power as P_3. When the line voltage is near the peak area, it is the rectified input voltage source that provides main power P_1 to the output directly and

also stores some extra power P_2 in the bulk capacitor. Furthermore, during peak line voltage both L_B and T_1 operate in CCM, and the boost inductor current is strongly dependent on the reflected load current. This inherent load current feedback mechanism can reduce the input power at light load without reducing the duty ratio. All the current processed by the switch is the primary side current of the feedback converter. Hence, the load current feedback can effectively reduce both the voltage stress of the bulk capacitor and the current stress of the active stress. The proposed converters combine the advantages of simple topology, low bulk capacitor voltage and low switch current stress. However, the efficiency and power factor are not better compared to other methods as can be seen in Table 1.2.

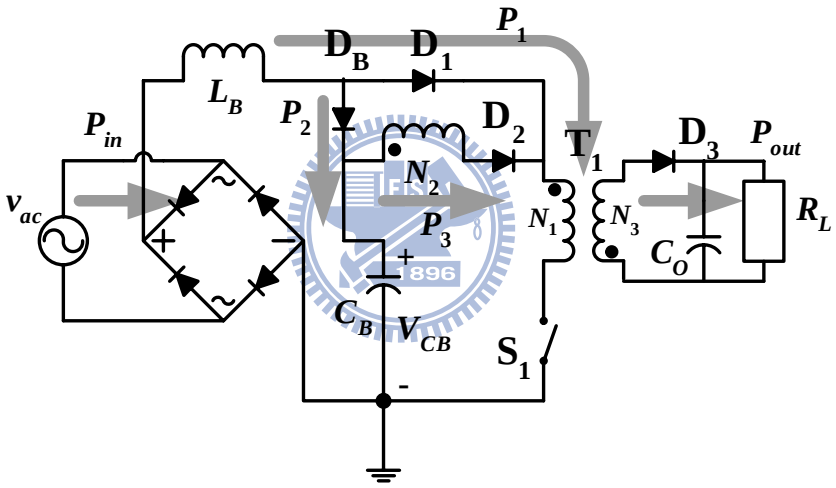


Fig. 2.3 Single switch parallel power factor correction AC/DC converter with inherent load current feedback.

To improve the efficiency and power factor, an alternative method based on a novel PFC cell called “flyboost” to reduce redundant power processing is presented [21]. The method contains a new family of S^2 converters derived from the direct power transfer concept and is intended for use in low to medium power level AC/DC converters such as adapters of personal computers.

The representative flyboost circuit shown in Fig. 2.4 has two operation modes. When recti-

fied line voltage $|v_{ac}(t)|$ is less than $2V_{CB}$-n_1V_O (n_1: the turn ratio of T_1; V_O: output voltage), Transformer T_1 works like a flyback transformer to discharge all stored input power directly to the load. The portion of power is processed by active switch S_1 only once. Meanwhile, DC/DC cell will deliver some power from bus capacitors to the load to keep tight output voltage regulation. When instantaneous input voltage goes higher, and $| v_{ac}(t)|$ is higher than $2V_{CB}$-n_1V_O, the voltage across transformer T_1 primary winding is clamped to $2V_{CB}$–$| v_{ac}(t)|$ during S_1 OFF interval, which will be less than n_1V_O. It means that diode D_1 in T_1 secondary discharging path will not conduct. T_1 works like a boost inductor and discharges its magnetizing energy to both bus capacitors via D_2. And DC/DC cell will deliver all output power from bus capacitors to the load. Under this mode, the input power is stored in bus capacitors, and then transferred to the load by DC/DC cell, resulting in this portion of power being processed twice by switch S_1.

It can be seen that the derived S^2 flyboost converters are of simplified circuit configuration and control, and typically, only one simple voltage control and one power switch are needed in circuit implementation. Experimental results demonstrate that the flyboost cell significantly improves the efficiency over the conventional converter. Moreover, experiments also verify that a newly derived S^2 converter can operate in discontinuous current mode + continuous current mode (DCM+CCM) operation due to the clamped bulk capacitor voltage characteristic of flyboost PFC cell. However, the components of the circuit of seem excessive because two bulk capacitors and multi-winding transformer are employed to get low voltage.

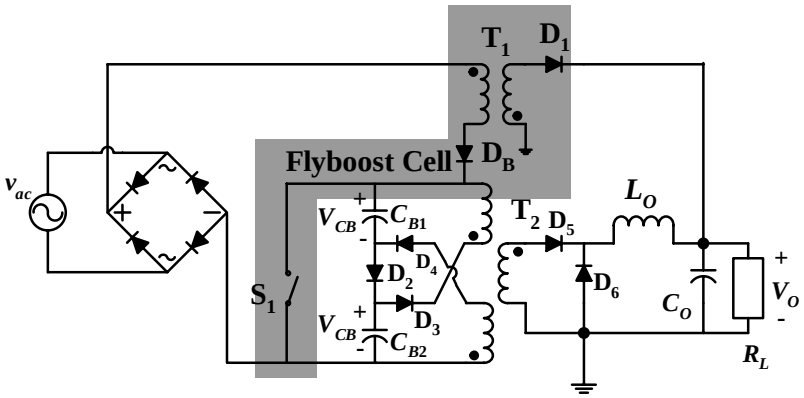


Fig. 2.4 Single-stage AC/DC converters with flyboost cell.

2.2 S^2 Parallel Boost-Flyback Converter

2.2.1 Principle

The new design power flow scheme of a single-stage (S^2) PPFC is shown in Fig. 2.5. In Fig. 2.5, the line power, p_{in} is fed to SSTO boost-flyback semi-stage and split to two power flow streams, p_1 and p_2. The power flow stream p_1 is processed only by flyback cell and transferred to output directly, and hence it is direct power. Since the instantaneous p_{in} is always different from output power P_{out}, the remaining input power, p_2, is buffered to bulk capacitor C_B through the boost function of boost cell to regulate power flow. To fulfill a better output power regulation, a DC/DC semi-stage is employed to transfer the power, denoted by p_3, from C_B to the output when p_{in} is low, especially smaller than P_{out}. The power series p_2 and p_3 are processed twice from ac input to dc output, and hence they are indirect powers. Furthermore, to obtain high power factor, the boost and flyback cells both had better operate in discontinuous conduction mode (DCM), whereas the DC/DC semi-stage can be implemented with forward or flyback configuration and operate either in continuous conduction mode (CCM) or DCM. A S^2 implemented circuit of Fig. 2.5 is shown in Fig. 2.6(a). The circuit has been simplified so as to use only one common power control switch for SSTO boost-flyback and DC/DC semi-stages as shown in Fig. 2.6(b). In Fig. 2.6(b), PFC and output regulation are

performed with one feedback controller as shown in Fig. 2.6(c). The practical realization circuit in Fig. 2.6(b) is composed of a SSTO boost-flyback semi-stage, which is constructed by L_B, D_B, T_1, D_{O1}, D_{I1}, S, D_b, and a bulk capacitor C_B, and a DC/DC semi-stage, which is implemented by a flyback circuit and constructed by T_2, D_{O2}, D_{I2}, S, and D_b. In Fig. 2.6(a) and (b), the two transformers T_1 and T_2 share the load current, so their size could be small. Furthermore, the boost inductor L_B and transformers T_1 process the input power together when switch S is on, so the size of L_B could be of smaller one. Therefore, the sizes of L_B, T_1 and T_2, can be chosen smaller ones in this design.

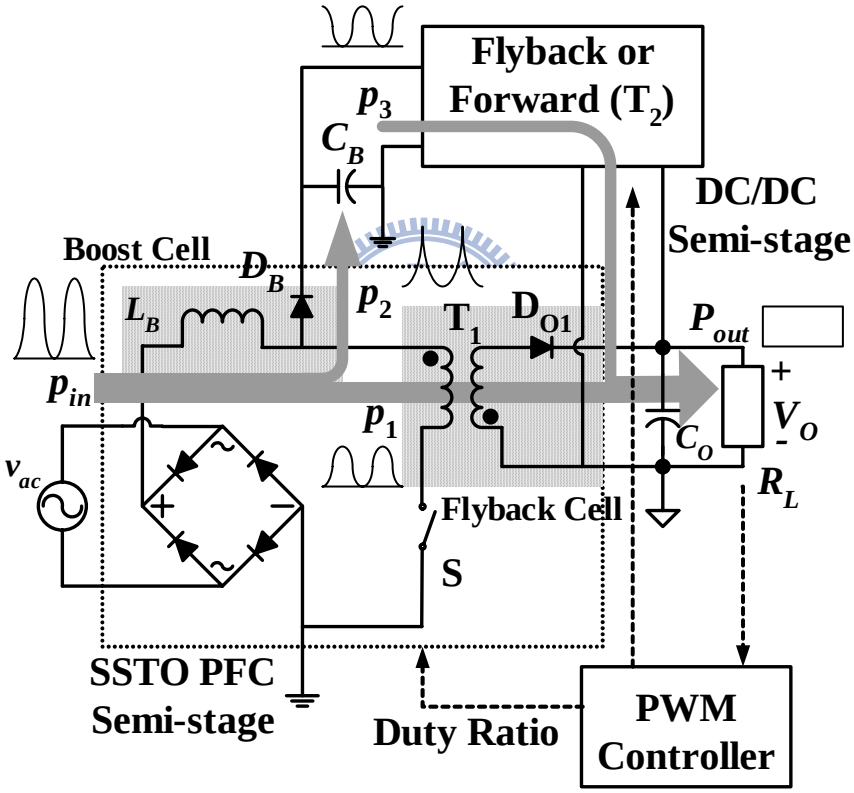
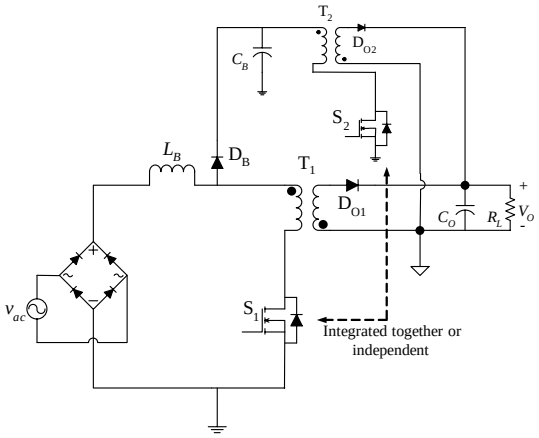
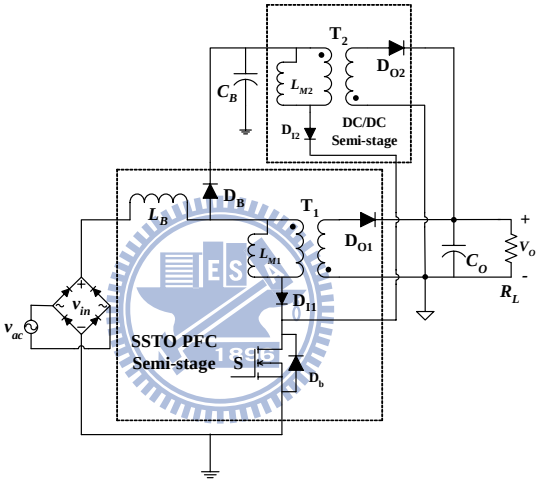


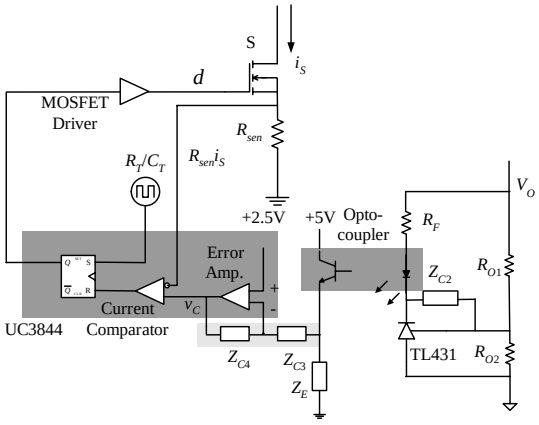
Fig. 2.5 Proposed S^2 PPFC scheme.



(a)



(b)



(c)

Fig. 2.6 S^2 Implementation circuit of parallel boost-flyback-flyback converter: (a) two-switch circuit, (b) single-switch circuit, and (c) feedback controller circuit.

2.2.2 SSTO Boost-Flyback Circuit

In order to clearly build the primary operation concepts and theories of the proposed S^2 parallel AC/DC converter depicted in Fig. 2.5 and 2.6, the operation of a SSTO boost-flyback converter depicted in Fig. 2.7(a) will be introduced in advance. In SSTO boost-flyback converter, T_1-D_{O1}-D_{I1}-C_O-R_O-S is the flyback cell and L_B-D_B-C_B-R_B-S is the boost cell. This converter has power factor correction function that will be demonstrated later. In the converter, the boost inductance L_B and the flyback transformer T_1 both operate in DCM. When control switch S is turned on, T_1 and L_B are charged serially. When S is turned off, T_1 and L_B are discharged to R_O-C_O and R_B-C_B respectively. The main current waveforms of SSTO boost-flyback converter operating in one switching period are shown in Fig. 2.7(b). To demonstrate the operation theory of the converter, the moving average notation $\langle x(t) \rangle$ of a waveform $x(t)$ over a switching period T_S is employed and defined as follows [16],

$$\langle x(t) \rangle \equiv \langle x(t) \rangle_{T_S} = \frac{1}{T_S} \int_{t}^{t+T_S} x(\tau) d\tau \,. \tag{2.1}$$

To focus on the primary analyses, some assumptions are made as follows:

1) All components are ideal.
2) Since switching frequency f_S is far greater than line frequency f_L=1/T_L, where T_L is line period. The input voltage $v_{in}(t)$, regarded as the rectified line voltage $V_{inpk}\left|\sin(\omega_L \cdot t)\right|$, is approximated to a constant over one switching period, where V_{inpk} is the ac voltage amplitude, and $\omega_L = 2 \cdot \pi / T_L$.
3) Since bulk capacitor C_B and output capacitor C_O are sufficiently large, flyback output voltage V_O and boost output voltage V_{CB} are regarded as constants within one half line cycle.

From Fig. 2.7(a), it can be seen that the average input current $\langle i_{in}(t)\rangle$ is equal to the sum of average flyback input diode current $\langle i_{DI1}(t)\rangle$ and average boost output diode current $\langle i_{DB}(t)\rangle$. Therefore, by summing the current waveforms of $\langle i_{DI1}(t)\rangle$ and $\langle i_{DB}(t)\rangle$ shown in Fig. 2.7(b), $\langle i_{in}(t)\rangle$ can be obtained as

$$\langle i_{in}(t)\rangle = \langle i_{DI1}(t)\rangle + \langle i_{DB}(t)\rangle = \frac{i_{pk1}\times(d+d_2)}{2}, \tag{2.2}$$

where d is the duty ratio of S, d_2 is the boost cell diode conduction time ratio, and the current peak value can be obtained from

$$i_{pk1} = \frac{d\cdot v_{in}(t)}{f_S(L_B+L_{M1})} = \frac{d_2\cdot(V_{CB}-v_{in}(t))}{f_S L_B} = \frac{d_1\cdot n_1\cdot V_O}{f_S L_{M1}}, \tag{2.3}$$

where L_{M1} is the primary magnetizing inductance of T_1, n_1 is the primary turns ratio of T_1, and d_1 is the flyback cell output diode conduction time ratio. From (2.3), d_2 can be obtained as

$$d_2 = \frac{d\cdot v_{in}(t)}{(V_{CB}-v_{in}(t))}\left(\frac{L_B}{L_B+L_{M1}}\right). \tag{2.4}$$

With substituting (2.3) and (2.4) into (2.2), $\langle i_{in}(t)\rangle$ can be found as

$$\langle i_{in}(t)\rangle = \frac{d^2 v_{in}(t)}{2f_S(L_B+L_{M1})}\left(1+\frac{v_{in}(t)}{(V_{CB}-v_{in}(t))}\left(\frac{L_B}{L_B+L_{M1}}\right)\right). \tag{2.5}$$

Since the average current of C_O over a half line cycle is zero at steady state, the half line average current of i_{DO1} is equal to the average output current. Thus,

$$\frac{2}{T_L}\int_0^{\frac{\pi}{\omega_L}}\langle i_{DO1}(t)\rangle dt = \frac{V_O}{R_O}. \tag{2.6}$$

From Fig. 2.7(b), average current over one switching period $\langle i_{DO1}(t)\rangle$ in (2.6) can be obtained as follows

$$\langle i_{DO1}(t)\rangle = \frac{n_1\cdot i_{pk1}\cdot d_1}{2}, \tag{2.7}$$

where the magnetism discharging time ratio of T_1 transformer, d_1, can be found from (2.3) as

$$d_1 = \frac{d\cdot v_{in}(t)}{n_1\cdot V_O}\left(\frac{L_{M1}}{L_B+L_{M1}}\right). \tag{2.8}$$

With substituting (2.3) and (2.8) into (2.7), $\langle i_{DO1}(t)\rangle$ can be obtained as

$$\langle i_{DO1}(t)\rangle = \frac{L_{M1} d^2 v_{in}^2(t)}{2 f_S (L_B + L_{M1})^2 V_O}. \tag{2.9}$$

Substituting (2.9) into (2.6), the voltage gain of flyback cell M_O can be obtained as

$$M_O = \frac{V_O}{V_{inpk}} = d \cdot \sqrt{\frac{L_{M1} \cdot R_O}{4 f_S (L_B + L_{M1})^2}}, \tag{2.10}$$

where R_O is the load resistance of flyback cell.

Similarly, since C_B has zero average current over a half line cycle in steady state, the average current relation can be obtained as

$$\frac{2}{T_L}\int_0^{\frac{\pi}{\omega_L}} \langle i_{DB}(t)\rangle dt = \frac{V_{CB}}{R_B}, \tag{2.11}$$

where $\langle i_{DB}(t)\rangle$ can be obtained from Fig. 2.7(b) as

$$\langle i_{DB}(t)\rangle = \frac{i_{pk1} \cdot d_2}{2} = \frac{L_B d^2 v_{in}^2(t)}{2 f_S (L_B + L_{M1})^2 (V_{CB} - v_{in}(t))}. \tag{2.12}$$

The voltage gain of boost cell M_{CB} is defined and obtained with substituting (2.12) into (2.11) as

$$M_{CB} = \frac{V_{CB}}{V_{inpk}} = \frac{d^2 \cdot R_B \cdot L_B}{2\pi \cdot f_S (L_B + L_{M1})^2} \int_0^{\pi} \frac{\sin^2\theta}{M_{CB} - |\sin\theta|} d\theta, \tag{2.13}$$

where R_B is the load resistance of boost semi-stage.

It can be seen from (2.5) that while d and f_S are regarded as constants, the arrangement of smaller ratio of $L_B/(L_B + L_{M1})$ can result in higher linear relation between $\langle i_{in}(t)\rangle$ and $v_{in}(t)$, in other words, lower input harmonic distortion. Furthermore, (2.10) and (2.13) show that voltage gain rises as load resistance increases. In particular, V_{CB} in (2.13) can be very high at light load and high line. Therefore, the method to keep it under commonly accepted limit would be presented in Chapter 3.

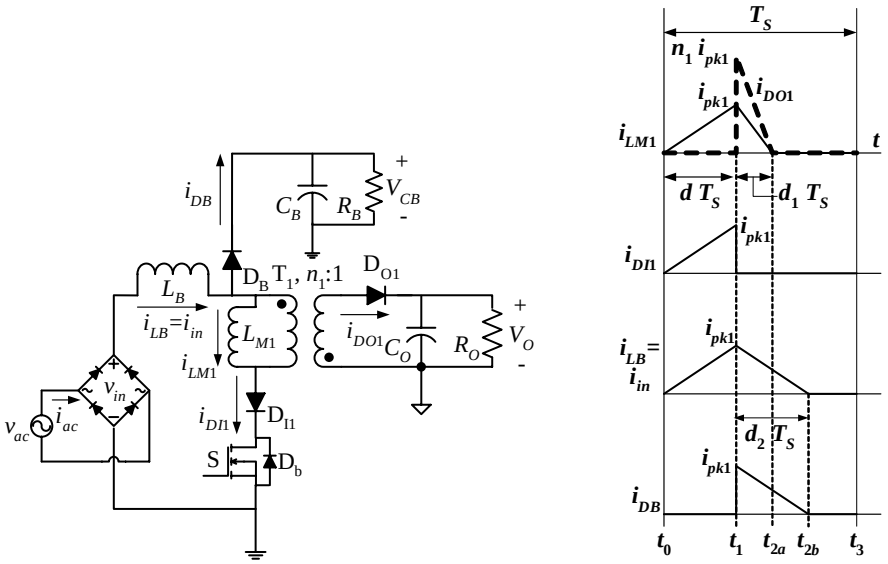
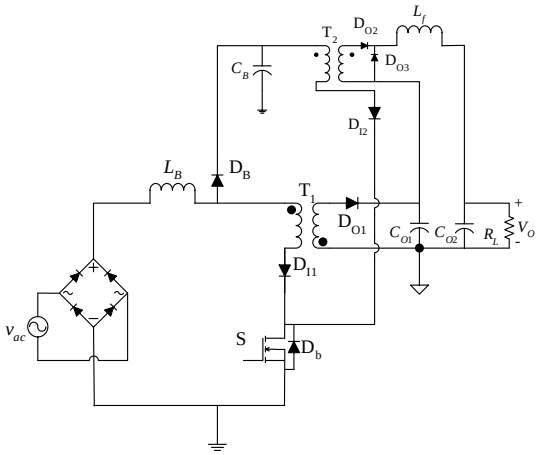


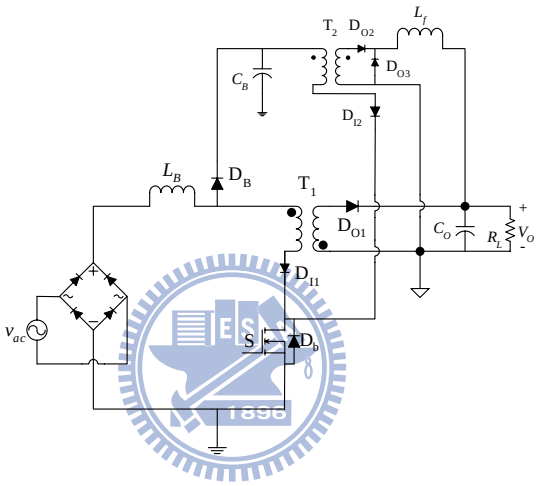
Fig. 2.7 SSTO boost-flyback converter: (a) circuit and (b) main waveforms.

2.3 New Family of Parallel Boost-Flyback Converter

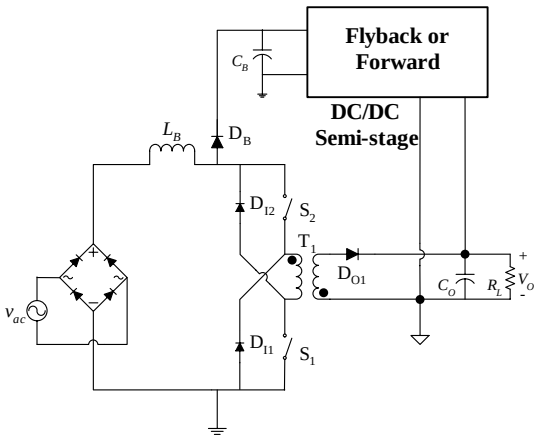
Based on the proposed S^2 PPFC scheme shown in Fig. 2.5, more circuits of the proposed S^4 boost-flyback converters can be formed by modifying the DC/DC semi-stage or flyback cell. By replacing the flyback DC/DC semi-stage in Fig. 2.6 with another DC/DC circuit such as forward circuit, a new single-stage-single-switch parallel AC/DC converter is obtained in Fig. 2.8(a). Moreover, the SSTO boost-flyback converter can be incorporated with the two-input Buck (TIBuck) post-regulator [12] to form another new single stage single switch parallel AC/DC converter as shown in Fig. 2.8(b). This converter can decrease the size of the bulk capacitor and improve the dynamic response with almost no efficiency penalty in either. Alternatively, the flyback cell of SSTO boost-flyback semi-stage can be replaced with a two-switch-flyback circuit to form another parallel scheme shown in Fig. 2.8(c), which has the merits of low switch voltage stress and leakage inductance clamping.



(a)



(b)



(c)

Fig. 2.8 Derived topologies from proposed parallel scheme: (a) with forward semi-stage, (b) with TIBuck semi-stage, (c) S^2 boost-two-switch-flyback parallel converter scheme.

CHAPTER 3

Analysis and Design of a Single-Stage-Single-Switch Parallel Boost-Flyback-Flyback Converter

The practical realization circuit of proposed S^2 PPFC scheme is composed of a SSTO boost-flyback semi-stage, C_B, and a DC/DC semi-stage. The SSTO boost-flyback semi-stage splits input power into two power flow streams including direct power stream and indirect stream. The direct power stream is processed only by flyback cell and transferred to output directly. The indirect power stream is buffered to C_B through the boost function of boost cell to regulate power flow through DC/DC semi-stage. As the boost cell and flyback cell operate in DCM, and duty ratio and switching frequency are constants, the arrangement of smaller ratio of boost inductor can result in higher power factor. The V_{CB} can be very high at light load and high line. Therefore, the method to keep input current harmonics and V_{CB} under commonly accepted limit would be presented later.

3.1 Analysis of the Proposed Converter

The proposed S^2 boost-flyback-flyback PPFC that has two semi-stages is shown in Fig. 2.5 and Fig. 2.6. The S^2 implementation circuit in Fig. 2.6(b) is redrawn as Fig. 3.1(a). The boost-flyback semi-stage has power factor correction function and simultaneously gives two energy-processing paths. Being the remaining semi-stage, the flyback DC/DC converter circuit has fast output regulation ability. The proposed circuit has three magnetic elements, and each element has two operation modes (i.e. CCM and DCM). Hence, there are eight modes may happen in the circuit as shown Table 3.1. In order to obtain good power factor, the boost and flyback cells are designed to operate in DCM, whereas the flyback DC/DC semi-stage operates in either CCM or DCM in a line cycle. Thus, the converter has two operating states.

The operation state while the flyback DC/DC semi-stage operates in CCM is defined as the M_1 state. Contrarily, the operation state while the flyback DC/DC semi-stage operates in DCM is defined as the M_2 state. However, making L_B operate in DCM in universal application is not easy, and CCM offers higher efficiency and lower current stress than DCM. M_3 and M_4 modes are allowed under harmonic limitation of IEC 61000-3-2 Class D, and not discussed in this dissertation. With properly selected n_1, it is easy to control T_1 in DCM, so M_5-M_8 modes would not happen. The main current waveforms of the boost-flyback semi-stage in a switching period are the same as Fig. 2.7(b), and the waveforms of flyback DC/DC semi-stage in both two modes are shown in Fig. 3.1 (b) and (c). The circuit operations of the single-switch implemented circuit shown in Fig. 2.6(b) are demonstrated as follows:

In $t_0 \le t \le t_1$ control switch S is switched on, flyback input diode D_{I1} conducts, and D_B, D_{O1} and D_{O2} are cut-off. Because the boost inductor L_B and the flyback transformer primary inductance L_{M1} both are connected in series, they are charged by the input power at the same time. The current i_{LB}, which is equal to i_{DI1} and also the magnetizing current of T_1, i_{LM1}, increases linearly from zero. Meanwhile, the currents i_{DI2}, which is equal to the magnetizing current of T_2, i_{LM2}, also increases linearly from its initial value while in M_1 mode and from zero while in M_2 mode. At the moment t_1, S is turned off. The currents i_{LB}, i_{DI1}, and i_{LM1} reach the same peak value i_{pk1} and the currents, i_{DI2} and i_{LM2} reach another peak value i_{pk2}.

In $t_1 \le t \le t_3$, the main switch S is off, the diode D_{I1} and D_{I2} are off, and D_B, D_{O1} and D_{O2} are on. The magnetic energy of inductor L_B is transferred to C_B and the magnetic energies of the transformers T_1 and T_2 are transferred to the same output load R_L simultaneously. Consequently, the energy discharging in T_1 produces the result that i_{LM1} and i_{DO1} ($= n_1 \cdot i_{LM1}$) both decrease linearly to zero at t_{2a} and keep zero until t_3, and i_{LB} and i_{DB} decrease linearly to zero at t_{2b}. The energy discharging in T_2 gives the result that both i_{LM2} and i_{DO2} ($= n_2 \cdot i_{LM2}$) decrease linearly to none zero final values at t_3 for M_1 mode and to zero at t_{2c} for M_2 mode.

Since M_1 and M_2 modes are to be discussed, three kinds of the combination of operation modes may be yielded within a half line cycle as shown in Table 3.2. The major currents waveforms and the corresponding duty ratios waveforms are depicted and shown in Fig. 3.2. Case I normally happens in low input voltage and high output power condition, whereas Case III normally happens at high input voltage and low output power.

For transient current balance of C_O, the transient load current can be expressed as

$$i_O(t) = i_{DO1}(t) + i_{DO2}(t) - i_{CO}(t), \tag{3.1a}$$

where $i_{DO1}(t)$, $i_{DO2}(t)$, and $i_{CO}(t)$ represent the transient current of D_{O1}, D_{O2}, and C_O. By an ideal output voltage feedback control, the duty-cycle of control switch is varied in order to set output voltage on reference value. As shown in Fig. 3.1, the input current ($i_{DO1}(t)+i_{DO2}(t)$) of C_O is regulated to balance with output current (i_O) in T_S so that $\langle i_O(t)\rangle = I_O$, $\langle i_{CO}(t)\rangle = 0$, $\langle v_O(t)\rangle = V_O$, and (3.1a) can be expressed as

$$I_O = \frac{V_O}{R_L} = \frac{P_{out}}{V_O} = \langle i_{DO1}(t)\rangle + \langle i_{DO2}(t)\rangle, \tag{3.1b}$$

where V_O is the average output voltage, R_L is the load resistance, $<i_{DO1}(t)>$ represents the averaging current of D_{O1} as expressed in (2.9), and $<i_{DO2}(t)>$ represents the averaging current of D_{O2}. Although the input voltage varies in a half line cycle, the output power will be kept constant through the output feedback control. To make (3.1b) come true, the ideal output voltage feedback controller should have superior transient response and robust stability. The structure of controller is implemented with current mode controller with optically isolated feedback as shown in Fig. 2.6(c). In the circuit of Fig. 2.6(c), output voltage signal V_O is transferred to UC3844 via TL431 and opt-coupler, the switch current i_S is sensed and fed back to comparator, then the duty ratio d of control switch S is well controlled.

For the M_1 mode, consider the bulk capacitance is a large one. Then the duty ratio d in M_1 mode will be kept nearly constant D_{m1} and yield a high regulation output, which is given by

$$V_O = \left.\frac{V_{CB} \cdot d}{n_2(1-d)}\right|_{d=D_{m1}}, \tag{3.2}$$

where n_2 is the turns ratio of T_2. From (3.2), D_{m1} can be found as

$$d = D_{m1} = \frac{n_2 V_O}{n_2 V_O + V_{CB}}. \tag{3.3}$$

From (3.1b), $\langle i_{DO2}(t)\rangle$ can be obtained as

$$\langle i_{DO2}(t)\rangle = I_O - \langle i_{DO1}(t)\rangle\big|_{d=D_{m1}}. \tag{3.4}$$

While in M_2 mode, T_2 operates in DCM. From Fig. 3.1(b) by following the similar deriving procedure of (2.9), $\langle i_{DO2}(t)\rangle$ can be obtained as

$$\langle i_{DO2}(t)\rangle = \frac{n_2 \cdot i_{pk2} \cdot d_3}{2} = \left.\frac{d^2 \cdot V_{CB}^2}{2 f_S L_{M2} V_O}\right|_{d=d_{m2}}, \tag{3.5}$$

where d_{m2} is the instant duty ratio in M_2 mode. Substituting (2.9) and (3.5) into (3.1b), it can be obtained as

$$d = d_{m2}(\theta) = \sqrt{\frac{2 f_S P_{out}}{\left(\frac{L_{M1} V_{inpk}^2 \sin^2\theta}{(L_B + L_{M1})^2} + \frac{V_{CB}^2}{L_{M2}}\right)}}, \tag{3.6}$$

where $\theta = \omega_L \cdot t$ is the phase of sinusoidal line voltage, and P_{out} is the output power. In order to generate the complex duty d_{m2}, the compensator in the current mode control had been optimized to possess superior transient responses such as small rising time, low overshoot, and zero steady state error. Addition, the compensator also can generate the correct duty d_{m2} with different operation modes due to its superior performances.

From (2.9) and (3.1b), $\langle i_{DO1}(t)\rangle$ reaches maximum and $\langle i_{DO2}(t)\rangle$ reaches minimum at $\theta = \pi/2$. For case I, the converter operates only in M_1 mode (T_2 operates in CCM), I_O must be greater than the boundary value $I_{DO1PK} + I_{DO2B}$,

$$I_O \geq I_{DO1PK} + I_{DO2B}, \tag{3.7}$$

where I_{DO1PK} is the peak value of $\langle i_{DO1}(t)\rangle$ and I_{DO2B} is the boundary value of i_{DO2} between

CCM and DCM. The former can be obtained by replacing d with D_{m1} and $v_{in}(t)$ with $V_{inpk}\sin(\pi/2)$ in (2.9), and expressed as

$$I_{DO1PK} = \frac{L_{M1}D_{m1}^2V_{inpk}^2}{2f_S(L_B + L_{M1})^2V_O}, \tag{3.8}$$

and the latter can be obtained by replacing d with D_{m1} in (3.5) and expressed as

$$I_{DO2B} = \frac{D_{m1}^2 \cdot V_{CB}^2}{2f_S L_{M2}V_O}. \tag{3.9}$$

Furthermore, as I_O is smaller than the boundary value in (3.7), M_2 mode shows in the operation of the proposed converter as plotted in Fig. 3.2(b). From the equality $I_{DO2} = I_{DO2B}$ and (3.1b), the transition angle θ_T from M_1 to M_2 mode can be expressed as

$$\theta_T = \omega_L \cdot t_T = \sin^{-1}\left[\sqrt{\frac{2f_S(L_B + L_{M1})^2V_O}{L_{M1}D_{m1}^2V_{inpk}^2}(I_O - I_{DO2B})}\right]. \tag{3.10}$$

As I_O gets smaller, the interval of M_2 becomes wider and M_1 becomes narrower. It can also be seen from (2.9) that $<i_{DO1}(t)>$ reaches zero at line voltage phase being 0 and π and from (3.1b) that $<i_{DO2}(t)>$ reaches maximum at the same time. Thus, as I_O gets smaller than the boundary value of (3.9), the converter would work in M_2 mode only during a half line cycle. Consequently, for case II operation that the converter works in both M_1 and M_2 modes in a half line cycle, I_O will be in the range of

$$I_{DO1PK} + I_{DO2B} \geq I_O \geq I_{DO2B}. \tag{3.11}$$

Besides, for case III operation that the converter works only in M_2 mode in a half of a line cycle, I_O is smaller than the boundary value

$$I_{DO2B} \geq I_O. \tag{3.12}$$

Based on above discussion, the theoretical currents and voltages waveforms for the cases I to III examples are illustrated in Fig. 3.2(a)-(c) and the corresponding parameters used are shown in Table 3.3. For the case I operation, the value of L_{M2} in (3.9) is intentionally selected a large one so that (3.7) can be satisfied and case I operation can present. For the other parameters, L_B, L_{M1}, n_1, and n_2, they are selected according to the procedure described in Section

3.4 so that cases II and III can be activated.

From Fig. 2.6 and Fig. 3.2(a)-(c), it can be seen that the average input current $<i_{in}(t)>$ is divided into $<i_{DI1}(t)>$ and $<i_{DB}(t)>$ through the operation of boost-flyback semi-stage. Among these two currents, $<i_{DI1}(t)>$ is transformed to $<i_{DO1}(t)>$ by the flyback cell, and then transferred to R_L directly. Alternatively, $<i_{DB}(t)>$ is mainly buffered in C_B during v_{in} peak, then transformed to $<i_{DO2}(t)>$ by the flyback DC/DC semi-stage, and then transferred to R_L for output regulation. The output current I_O is primarily supplied by $<i_{DO2}(t)>$ in low line voltage duration.

The switch current of conventional cascade S^4 converter like [3] mainly composed of inductor current of the boost-ICS semi-stage and the transformer primary current of the flyback semi-stage. Both semi-stages have to handle the whole input power. Hence, the peak switch current is doubled and reaches peak value when input power is the maximum and occurs at $\theta = \omega_L \cdot t = \pi/2$. In Fig. 2.6, the average switch current $<i_S(t)>$ of the proposed converter is the sum of $<i_{DI1}(t)>$ and $<i_{DI2}(t)>$, and can be expressed as

$$\langle i_S(t)\rangle = \langle i_{DI1}(t)\rangle + \langle i_{DI2}(t)\rangle, \tag{3.13}$$

where both $<i_{DI1}(t)>$ and $<i_{DI2}(t)>$ represent the charged current of the first semi-stage from line input and the transformer primary current of second semi-stage from bulk capacitor, and can be obtained from Fig. 2.7(b) as

$$\langle i_{DI1}(t)\rangle = \langle i_{LB}(t)\rangle - \langle i_{DB}(t)\rangle, \tag{3.14}$$

and

$$\langle i_{DI2}(t)\rangle = \frac{V_O}{V_{CB}}\langle i_{DO2}(t)\rangle = \frac{V_O}{V_{CB}}\left(I_O - \langle i_{DO1}(t)\rangle\right). \tag{3.15}$$

It can be seen from (3.13) and (3.15) that if $<i_{DO1}(t)>$ increases, more output current will be provided by flyback cell, and $<i_S(t)>$ will be reduced. Contrarily, if flyback cell is absent (i.e. $<i_{DO1}(t)>=0$), the circuit in Fig. 2.6(b) will be reduced to a conventional S^2 converter [3]. Furthermore, from Fig. 2.7(b), $<i_{DI1}(t)>$ can be further obtained as

$$\langle i_{DI1}(t)\rangle = \frac{i_{pk1}\cdot d}{2} = \frac{d^2 V_{inpk}\sin(\omega_L \cdot t)}{2 f_S (L_B + L_{M1})}. \tag{3.16}$$

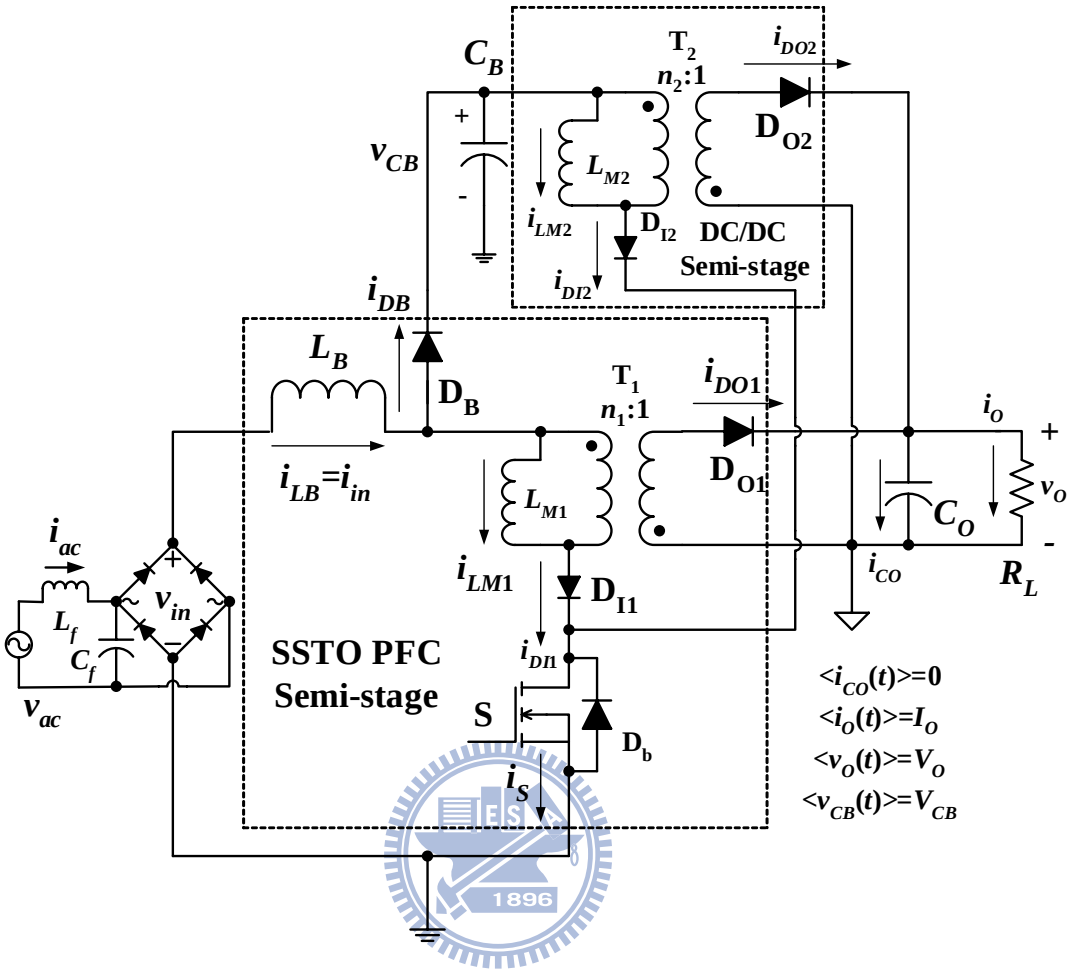
Substituting (2.9) into (3.4) and the result is substituted into (3.15), $<i_{DI2}(t)>$ for M_1 mode can be further expressed as

$$\langle i_{DI2}(t)\rangle = \frac{V_O}{V_{CB}}\left(I_O - \frac{L_{M1}D_{m1}^2 V_{inpk}^2 \sin^2(\omega_L \cdot t)}{2 f_S (L_B + L_{M1})^2 V_O}\right). \tag{3.17}$$

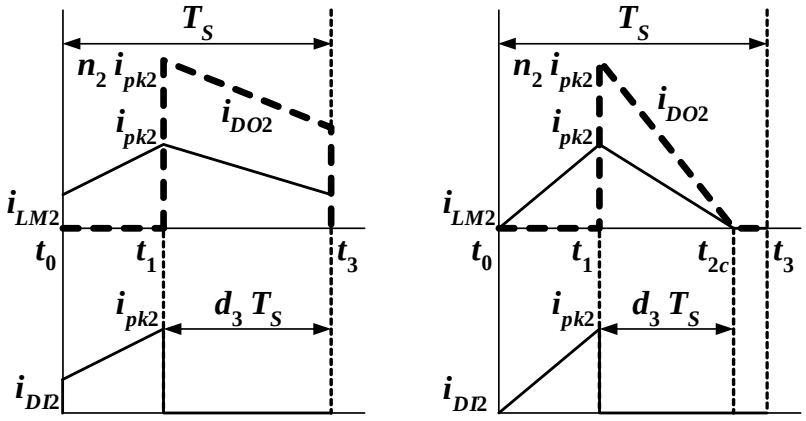
Substituting (3.5) into (3.15), $<i_{DI2}(t)>$ for M_2 mode can be further obtained as

$$\langle i_{DI2}(t)\rangle = \frac{d^2 \cdot V_{CB}}{2 f_S L_{M2}}\bigg|_{d=d_{m2}}, \tag{3.18}$$

where d_{m2} can be obtained from (3.6). It can be seen from (3.16)-(3.18) and Fig. 3.3 that $<i_{DI1}(t)>$ reaches local maximum at $\theta = \omega_L \cdot t = \pi/2$ while $<i_{DI2}(t)>$ is minimum, and $<i_{DI2}(t)>$ reaches local maximum at $\theta = \omega_L \cdot t = 0$ or π while $<i_{DI1}(t)>$ is zero. Therefore, the power processed by flyback cell is transferred to load directly and would not be processed by the switch again, the local maximum current stresses due to direct and indirect power do not appear at the same time during half line cycle, so the overall current stress of main switch compared small with that of conventional S^4 converter.



(a)



(b) (c)

Fig. 3.1 Parallel boost-flyback-flyback converter: (a) Implementation circuit, (b) DC/DC semi-stage waveform in M_1 mode, and (c) DC/DC semi-stage waveform in M_2 mode.

Table 3.1 Various operation modes in the proposed circuit

Mode	M_1	M_2	M_3	M_4	M_5…M_8
L_B	DCM	DCM	CCM	CCM	CCM/DCM
T_1	DCM	DCM	DCM	DCM	CCM
T_2	CCM	DCM	CCM	DCM	CCM/DCM
	Self PFC	Self PFC	Allowed under CL. D	Allowed under CL. D	Not happen

Table 3.2 Various cases in the proposed circuit

Case	Mode	V_{ac}	P_{out}
I	M_1	Low	High
II	M_1+ M_2	Medium	Medium
III	M_2	High	Low

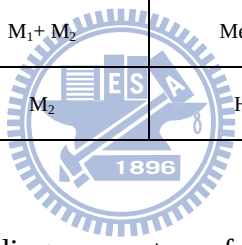
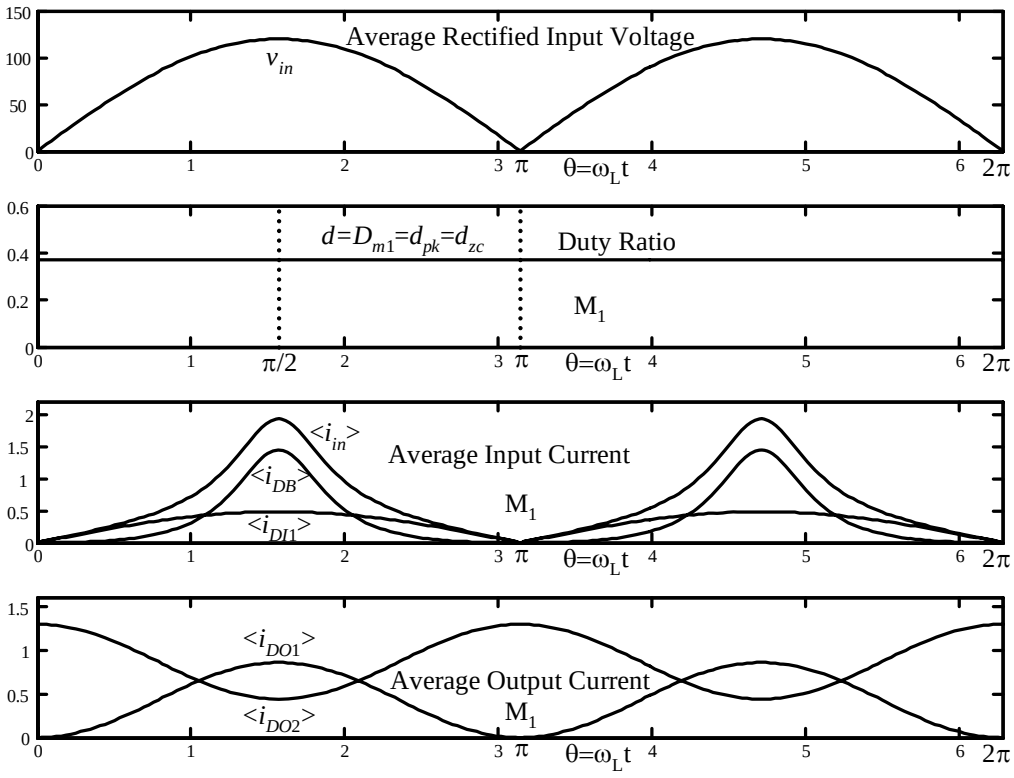
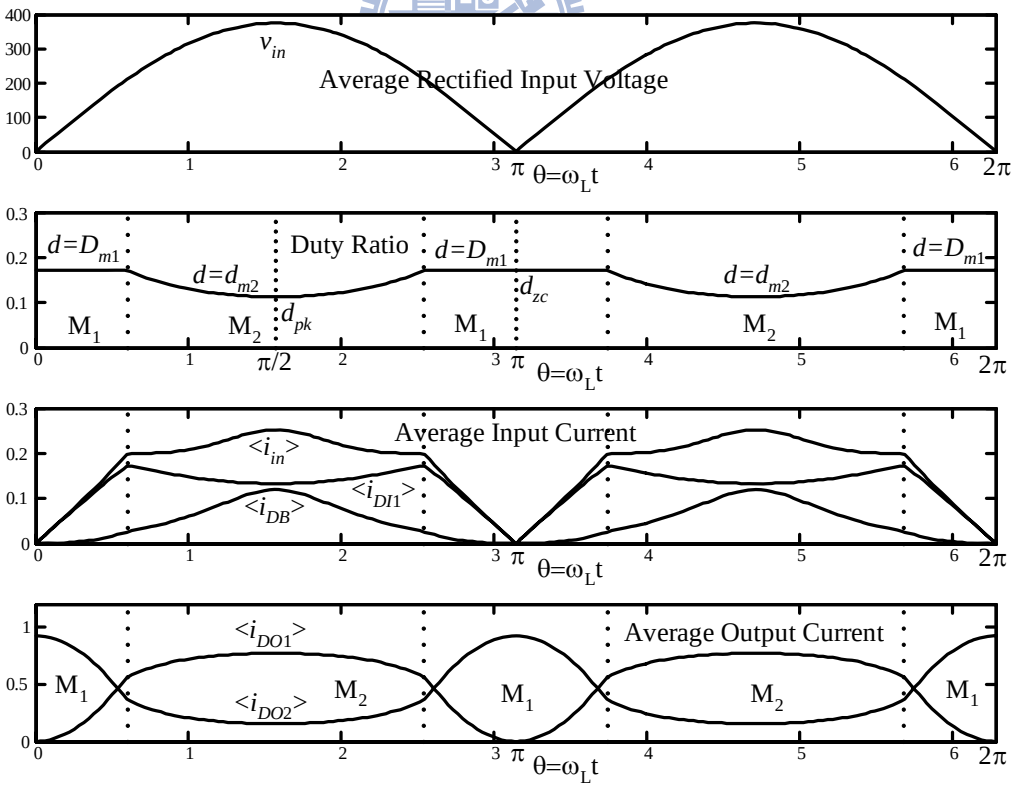


Table 3.3 The corresponding parameters of cases I-III illustration example

Case	L_B	L_{M1}	n_1	L_{M2}	n_2	V_{ac}	V_O	P_{out}	f_S	f_L	V_{CB}
I	35 μ H	135 μ H	1.2	4 mH	1.4	85 V_{rms}	54 V	70 W	100 kHz	60 Hz	128.5 V
II	30 μ H	150 μ H	1.6	1.5 mH	1.9	265 V_{rms}	54 V	50 W	100 kHz	60 Hz	444.5 V
III	30 μ H	150 μ H	1.6	1.5 mH	1.9	265 V_{rms}	54 V	20 W	100 kHz	60 Hz	449.9 V

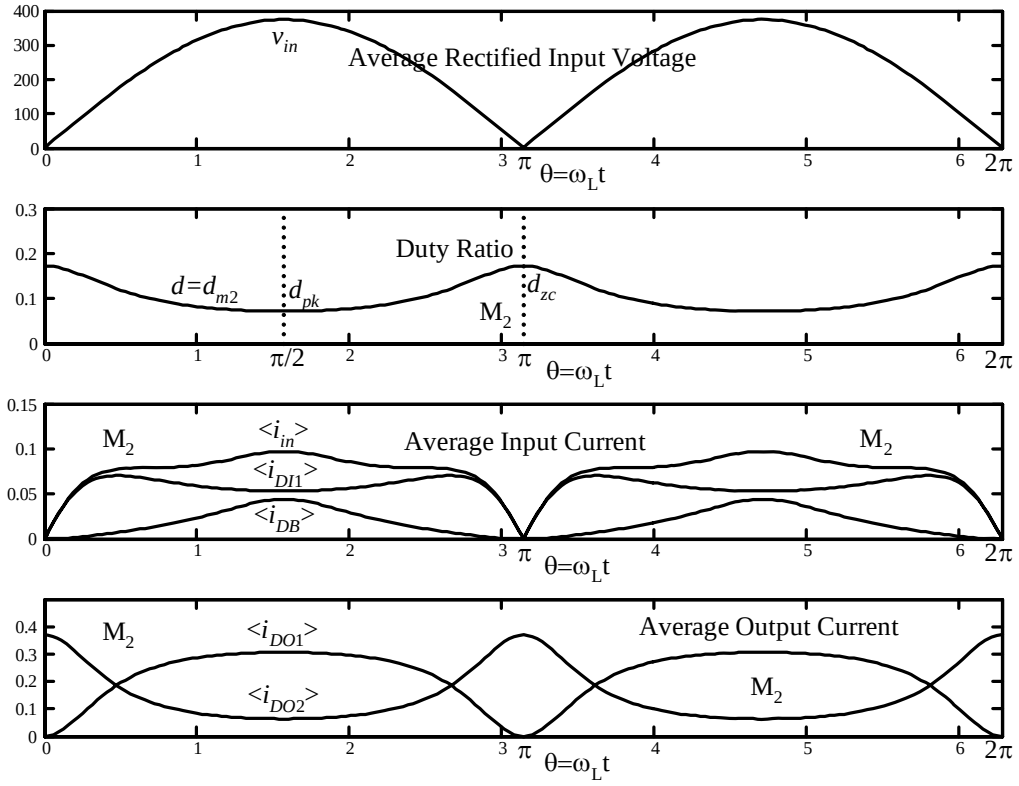


(a)



(b)

(Continued on next page)



(c)

Fig. 3.2 Main waveforms of parallel boost-flyback-flyback converter in a line cycle: (a) case I (M_1 mode only), (b) case II (both M_1 and M_2 modes), and (c) case III (M_2 mode only).

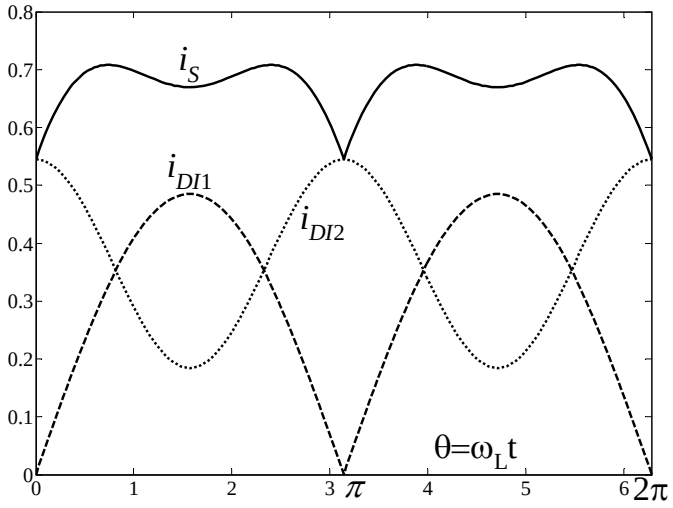


Fig. 3.3 Average switch current for case I.

3.2 Power Distribution and Bulk Capacitor Voltage

In the proposed S^2 PPFC scheme shown in Fig. 2.5, the power distribution between the direct (p_1) and indirect power (p_2 or p_3) processing paths is one of the important design considerations since it affects not only the converter efficiency but also the power ratings required to the components in each processing power path. Besides, in the indirect power path, the energy balance between the power flow into (p_2) and out (p_3) of bulk capacitor determines the bulk capacitor voltage, which can be very high if not properly design. Based on the above design considerations, the power distribution will be analyzed according to the implementation circuit shown in Fig. 2.6(b), and hence the formula related to power distribution and bulk capacitance voltage can be derived. They are formulated as follows:

The input power p_{in} is composed of p_1 and p_2,

$$p_{in}(\theta) = v_{in}(t)\langle i_{LB}(t)\rangle = p_1(\theta) + p_2(\theta). \tag{3.19}$$

The direct power processed by flyback semi-stage is given by

$$p_1(\theta) = v_{in}(t)\frac{L_{M1}}{L_B + L_{M1}}\langle i_{DI1}(t)\rangle = V_O\langle i_{DO1}(t)\rangle. \tag{3.20a}$$

Substitution of $\langle i_{DO1}(t)\rangle$ given by (2.9) to (3.20a) gives

$$p_1(\theta) = 2k_p P_{out}\sin^2\theta, \tag{3.20b}$$

where

$$k_p \equiv \frac{P_{1,pk}(d)}{P_{out}} = \frac{L_{M1}d^2V_{inpk}^2}{4f_S(L_B + L_{M1})^2 P_{out}}, \tag{3.21}$$

and

$$P_{1,pk}(d) = \frac{L_{M1}d^2V_{inpk}^2}{4f_S(L_B + L_{M1})^2}. \tag{3.22}$$

In M_1 mode, k_p is a constant and can be found by

$$k_p = k_p\big|_{d=D_{m1}} = K_{P1}. \tag{3.23}$$

In M_2 mode, k_p is a function of θ and obtained by

$$k_p = k_p\Big|_{d=d_{m2}(\theta)} = k_{p2}(\theta) = \frac{L_{M1}\cdot V_{inpk}^2}{2\left[L_{M1}V_{inpk}^2\sin^2\theta + \frac{V_{CB}^2}{L_{M2}}\left(L_B + L_{M1}\right)^2\right]}. \tag{3.24}$$

It can be seen from (3.24) that k_{p2} is independent of P_{out}. The values of D_{m1} and d_{m2} can be obtained from (3.3) and (3.6).

The indirect power processed by boost semi-stage from L_B to C_B is given by:

$$p_2(\theta) = V_{CB}\langle i_{DB}(t)\rangle. \tag{3.25a}$$

Substitution of $\langle i_{DB}(t)\rangle$ given by (2.12) into (3.25a) gives

$$p_2(\theta) = \frac{M_{CB}\sin^2\theta}{M_{CB} - |\sin\theta|}\frac{2k_pP_{out}}{K_{M1}}, \tag{3.25b}$$

where K_{M1} is called inductance ratio and expressed as

$$K_{M1} = \frac{L_{M1}}{L_B}. \tag{3.26}$$

The dimensionless variable M_{CB} in (2.13) in (3.25b) can be regarded as the normalized V_{CB} with respect to V_{inpk}. In practice, the true value of V_{CB} is lower than the theoretical value because of presence of the equivalent series resistance (ESR) of inductance and capacitor. Thus, in order to avoid the bulk capacitor voltage V_{CB} from exceeding the limitation voltage, 450 V, of the commercial capacitor, it is suggested that M_{CB} had better been controlled below or just equal to 1.2 for V_{ac}=265 V_{rms}. Furthermore, the indirect power processed by flyback DC/DC semi-stage from C_B can be expressed as

$$p_3(\theta) = V_O\langle i_{DO2}(t)\rangle = P_{out} - p_1(\theta) = P_{out}\left(1 - 2k_p\sin^2\theta\right). \tag{3.27a}$$

Substituting (3.5) into (3.27a), p_3 for M_2 mode can be expressed as

$$p_3(\theta) = \frac{d^2\cdot V_{CB}^2}{2f_SL_{M2}}\Big|_{d=d_{m2}} = \frac{d^2\cdot\left(M_{CB}\cdot V_{inpk}\right)^2}{2f_SL_{M2}}\Big|_{d=d_{m2}}. \tag{3.27b}$$

Since p_1 and p_2 (or p_3) vary with $\theta = \omega_L\cdot t$, they would be expressed as

$$P_{x,ave}\big|_{x=1,2,3} = \frac{1}{\pi}\int_0^{\pi}p_x(\theta)d\theta\Big|_{x=1,2,3}. \tag{3.28}$$

Therefore, direct power ratio K_{DP} is defined as

$$K_{DP} = \frac{P_{1,ave}}{P_{out}}. \tag{3.29}$$

In this equation, high K_{DP} implies high efficiency and large utilization performance of T_1. Because the average power sent to and out from C_B are equal for a half line cycle, the indirect power ratio K_{IDP} can be defined as

$$K_{IDP} = \frac{P_{2,ave}}{P_{out}} = \frac{P_{3,ave}}{P_{out}} = 1 - K_{DP} . \tag{3.30}$$

The more detailed indirect power ratio expressions defined in (3.30) for three cases can be derived as shown in Table 3.4 by substituting (3.25b) and (3.27a) into (3.28) and normalizing with P_{out}. By using iterative approaching methodology for obtaining accurate M_{CB}, the detailed expressions in Table 3.4 are calculated repeatedly until (3.30) is satisfied, and K_{DP}, K_{IDP}, and M_{CB} can be solved consequently. Following the iterative calculation process, the curves of direct power ratio K_{DP} versus output power P_{out} for different line input voltage V_{ac} and operation cases are obtained and shown in Fig. 3.4, and the curves are obtained by taking the converter parameters in Table 3.3-case I as an example. It can be seen from Fig. 3.4 that the relation between K_{DP} and case is $(K_{DP})_{III} > (K_{DP})_{II} > (K_{DP})_{I}$. K_{DP} increases as P_{out} is low or V_{ac} is high.

The curves of K_{DP} and M_{CB} versus P_{out} for different K_{M1} and L_{M2} at the assigned conditions of the converter, L_{M1}=150 μH, n_2=1.7, V_{ac}=265 V_{rms}, and V_O=54 V, are shown in Fig. 3.5. Substituting (3.19) into case III of Table 3.4, M_{CB} obtained from (3.30) is independent of P_{out}. Hence, each M_{CB} curve in Fig. 3.5(b) is horizontal when converter operates in case III. From Fig. 3.5(a), it can be seen that K_{DP} is greater at low output power. That is to say, K_{IDP} rises as output power increases. This implies that the direct power is the main portion providing the load and the indirect power is regarded as energy reservoir used for regulating the power flow to load. Besides, it can be seen from Fig. 3.5(b) that M_{CB} increases as P_{out} decreases, and approaches and holds to the maximum value at lighter load. This phenomenon shows that high bulk capacitor voltage will be resulted at high line and case III. However, from Fig. 3.5, it also can be seen that K_{DP} goes up and M_{CB} slides down as K_{M1} increases. This is because more in-

put power goes through flyback cell without being buffered by C_B. Hence, for the purpose of obtaining high efficiency and low V_{CB} it is better to select K_{M1} as large as possible. Furthermore, the decrease of L_{M2} can lower both K_{DP} and M_{CB} since it can be seen from (3.5) that low L_{M2} will result in large current i_{DO2} for M_2 mode, or equivalently to say that the output power ratio provided by C_B will be increased. In other words, more output power comes from buffered energy and less input power passes through flyback cell, so this will result in lower efficiency. However, it is good for reducing the maximum value of M_{CB} since more power is continuously sent out from C_B. Therefore, M_{CB} has to be lower to achieve half line cycle average indirect power balance in (3.30) as can be seen from (3.25b) and (3.27b). Besides, decreasing L_{M2} would cause flyback DC/DC semi-stage closer to DCM but make worse output voltage regulation. A compromise is suggested for selecting proper value of L_{M2} in considering of the proper values of V_{CB}, K_{DP}, and output voltage regulation. It can be seen from Fig. 3.5 that curves (1) and (2) have high K_{DP} and the maximum values of M_{CB} are below or close to 1.2 among all curves. Thus, with the consideration of obtaining high efficiency and low V_{CB}, curves (1) and (2) are better choices.

Table 3.4 K_{IDP} indirect power ratio

Case	$P_{2,ave}/P_{out}$	$P_{3,ave}/P_{out}$
I	$\frac{2K_{P1}}{\pi \cdot K_{M1}} \int_0^{\pi} \frac{M_{CB} \sin^2 \theta}{M_{CB} - \lvert \sin\theta \rvert} d\theta$	$1 - K_{P1}$
II	$\frac{4}{\pi \cdot K_{M1}} \left[\int_0^{\theta_T} \frac{M_{CB} \sin^2 \theta \cdot K_{P1}}{\left(M_{CB} - \lvert \sin\theta \rvert\right)} d\theta + \int_{\theta_T}^{\frac{\pi}{2}} \frac{M_{CB} \sin^2 \theta \cdot k_{p2}(\theta)}{\left(M_{CB} - \lvert \sin\theta \rvert\right)} d\theta \right]$	$\frac{2}{\pi} \left[\int_0^{\theta_T} \left(1 - 2K_{P1} \sin^2 \theta\right) d\theta + \int_{\theta_T}^{\frac{\pi}{2}} \left(1 - 2k_{p2}(\theta) \sin^2 \theta\right) d\theta \right]$
III	$\frac{2}{\pi \cdot K_{M1}} \int_0^{\pi} \frac{M_{CB} \sin^2 \theta \cdot k_{p2}(\theta)}{\left(M_{CB} - \lvert \sin\theta \rvert\right)} d\theta$	$\frac{1}{\pi} \int_0^{\pi} \left(1 - 2k_{p2}(\theta) \sin^2 \theta\right) d\theta$

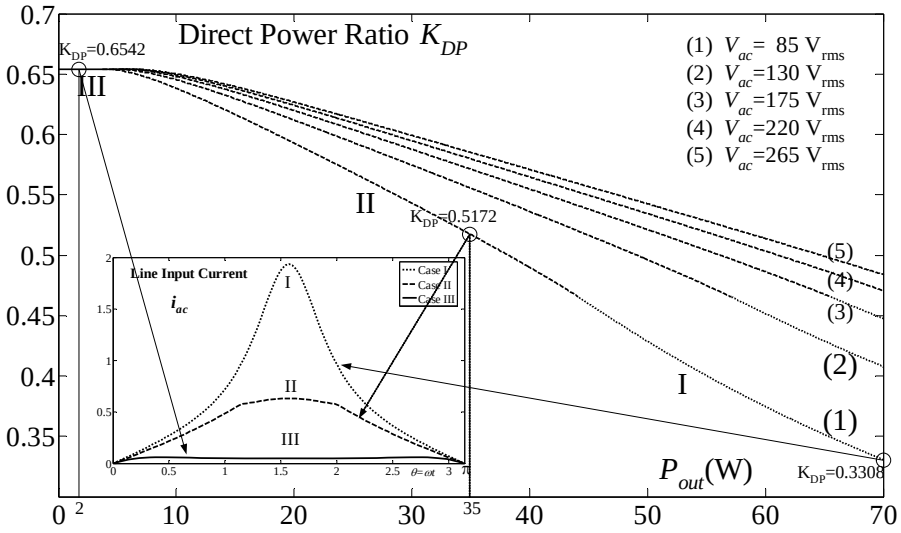


Fig. 3.4 K_{DP} versus output power for different V_{ac} and cases at the condition of Table 3.3-case I.

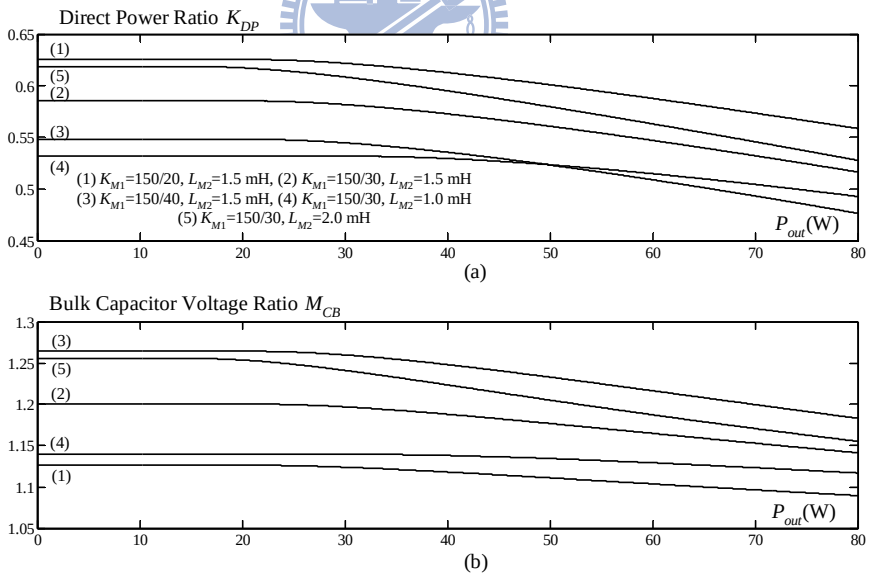


Fig. 3.5 (a) K_{DP} and (b) M_{CB} versus output power for different K_{M1} and L_{M2} , at L_{M1}=150 μH, n_2=1.7, V_{ac}=265 V_{rms}, V_O=54 V.

3.3 Design equations

The design equations are going to be derived for the objectives of obtaining proper power factor correction and output voltage regulation. The DCM operation design of boost-flyback semi-stage is essential for obtaining good power factor correction. It can be seen from i_{LM1} waveform in Fig. 2.7(b) that to guarantee T_1 operating in DCM, d_1T_S should be smaller than (1-d) T_S. Thus, n_1 should be designed to satisfy the following equation derived from (2.8)

$$n_1 \geq \frac{K_{M1}}{(K_{M1}+1)} \frac{V_{inpk}}{V_O} \frac{d_{pk}}{(1-d_{pk})}, \tag{3.31a}$$

where d_{pk} is the duty ratio occurring at $\theta = \pi/2$ as shown in Fig. 3.2. From (3.31a), the minimum turns ratio for T_1 to operate in DCM is obtained as

$$n_1 \geq n_{1,\min} = \frac{K_{M1}}{(K_{M1}+1)} \frac{V_{inpk,\min}}{V_O} \frac{d_{pk,\max}}{(1-d_{pk},\max)}, \tag{3.31b}$$

where $d_{pk,\max}$ is the maximum of d_{pk} and occurs at the lowest rectified line input voltage $v_{in}(t) = V_{inpk.\min}|\sin(\pi/2)|$ and the largest output power. With conservative design, $d_{pk,\max}$ can be replaced with the acceptable maximum value.

Similarly, to guarantee L_B operating in DCM, d_2T_S should be smaller than (1-d) T_S. Thus, L_B and L_{M1} should be designed to satisfy the following equation derived from (2.4):

$$(1-d_{pk}) \geq \frac{L_B}{(L_B+L_{M1})} \frac{d_{pk}}{(M_{CB}-1)}, \tag{3.32a}$$

where M_{CB} can be solved from (3.30) and Table 3.4. From previous section, it can be known that M_{CB} will slide down and d_{pk} thus rises as output power is increasing. Thus, the worst DCM condition occurs at the low input voltage and the large output power for universal application. From (3.32a), the minimum time ratio needed for i_{LB} to decay to zero before the end of switch off time duration can be obtained as

$$D_{dz} = \frac{L_B}{(L_B+L_{M1})} \frac{d_{pk,\max}}{(M_{CB,\min}-1)}, \tag{3.32b}$$

where $M_{CB,\min} = V_{CB,\min}/V_{inpk,\min}$, and $V_{CB,\min}$ is the minimum bulk capacitor voltage occurring at

the lowest rectified line input voltage and the largest output power. However, the converter needs sufficient secondary open voltage of DC/DC semi-stage transformer T_2, V_{CB}/n_2, to guarantee the output regulation operation all the time even at $v_{in}(t)=0$. Hence, for flyblack DC/DC semi-stage, the following relation must be satisfied

$$\frac{V_{CB}}{n_2}\frac{d_{zc}}{(1-d_{zc})}=V_O\,, \tag{3.33a}$$

where d_{zc} is the duty ratio at $v_{in}(t)=0$ as denoted in Fig. 3.2. It can be seen from (3.33a) that V_O is decreasing as n_2 increases. Thus, after rearranging (3.33a), the turns ratio limitation of T_2 is obtained as:

$$n_2<\frac{V_{CB,\min}}{V_O}\frac{d_{zc,\max}}{(1-d_{zc,\max})}=n_{2,\max}\,, \tag{3.33b}$$

where $d_{zc,\max}$ is the maximum d_{zc} while occurring at the lowest rectified line input voltage and the largest output power, and $n_{2,\max}$ is the upper bound of n_2 to satisfy output voltage requirement shown in (3.33a).

3.4 Example and Design Procedure

To verify the proposed boost-flyback-flyback converter, a prototype converter with the following specifications was designed:

- AC input voltage (V_{ac}): 85-265 V_{rms};
- Output voltage (V_O): 54 V;
- Maximum output power ($P_{out,\max}$): 80 W;
- Switching frequency (f_S): 100 kHz;
- Maximum duty ratio ($D_{\max}$) at v_{ac} =85 V_{rms}: 0.44.

As the suggested criterion [17] for universal input voltage single stage converter, the main design objective is to comply with the line current harmonic standards such as IEC 61000-3-2 Class D, to keep bulk capacitor voltage below 450 V, and to filter output ripple as small as

possible.

From the previous section, it can be known that L_B tends to operate in CCM as input voltage decreases and load increases, thus at this condition the harmonic current will get large. Furthermore, the bulk capacitor voltage will be high and may increase over 450 V at high line and light load. While considering the object of input current, the DCM operation gives a better PF in comparing with that given by the CCM operation. However, the CCM operation offers higher conversion efficiency and lower switch current stress than those given by the DCM operation. For the regular design, it is not easy to be realized in practice that L_B operates in DCM under the lowest line and the fullest load condition. Hence, it is not necessary for L_B to operate in DCM during the whole half cycle, and the worst DCM condition for L_B in this example is set at V_{ac}=85 V_{rms}, and P_{out}=60 W. It is permissible that L_B operates in CCM during a small interval within a half line cycle, that is also called semi-continuous conduction mode (SCM) [17] while V_{ac}=85 V_{rms} and P_{out}>60 W, as long as the IEC regulation can be satisfied. With the substitution of the above specifications to (3.31b), DCM condition for T_1 could be reached as long as n_1 and K_{M1} were properly selected. However, L_{M1} and L_B cannot be determined by (3.32b) directly since L_{M2} must be assigned in advance, and further, $M_{CB,\min}$ and $d_{pk,\max}$ have to be calculated. For the object of low bulk capacitor voltage, M_{CB} had better no more than 1.2 at high line and light load condition in order to guarantee V_{CB} below 450 V by properly selecting K_{M1} and L_{M2}. The critical parameters L_B, L_{M1}, n_1, L_{M2}, and n_2 are interrelated and designed from the following procedure:

1) Assign L_{M2} at first, and calculate $M_{CB,\min}$ and $d_{pk,\max}$ by following the iterative calculating process in Section 3.2 at the preset worst DCM condition of L_B, V_{ac}=85 V_{rms}, and P_{out}=60 W;
2) Generate the curves of (1-$d_{pk,\max}$) and D_{dz} versus L_{M1} for different L_B by using equation (31b) with the calculated $M_{CB,\min}$ and $d_{pk,\max}$ in step 1;
3) Generate the curves of $n_{2,\max}$ versus L_{M1} for different L_B with substituting $M_{CB,\min}$ and

$d_{zc,\max}$ in (3.28b), and set $d_{zc,\max}$ to 0.42 while P_{out}=60 W to prevent from over 0.44 when P_{out}=80 W;

4) Select L_{M1} and L_B from the curves of (1-$d_{pk,\max}$) and D_{dz} provided from step 2 such that L_B can operate in DCM at the preset worst DCM condition, and hence K_{M1}=L_{M1}/L_B is determined;

5) Select n_2 with selected L_{M1} and L_B from $n_{2,\max}$ curves given by step 3 such that flyback DC/DC semi-stage can correctly fulfill output regulation;

6) Select n_1 with the selected K_{M1} from step 4 substituted to (3.31b) such that T_1 can operate in DCM;

7) Calculate M_{CB} at high line and light load with the selected L_B, L_{M1}, n_1, L_{M2}, and n_2 by following the iterative calculating process in Section 3.2;

8) Check M_{CB} whether it is below 1.2 at high line and light load or not. If not, reduce L_{M2} and repeat steps 1-7 until M_{CB} is equal to or smaller than 1.2 at high line and light load.

Following the above procedure, the final curves of (1-$d_{pk,\max}$) and D_{dz} is shown in Fig. 3.6, the curves of $n_{2,\max}$ is shown in Fig. 3.7, and the designed parameters of key components are obtained as: L_B=30 μH, L_{M1}=150 μH, n_1=1.6, L_{M2}=1.5 mH, n_2=1.7.

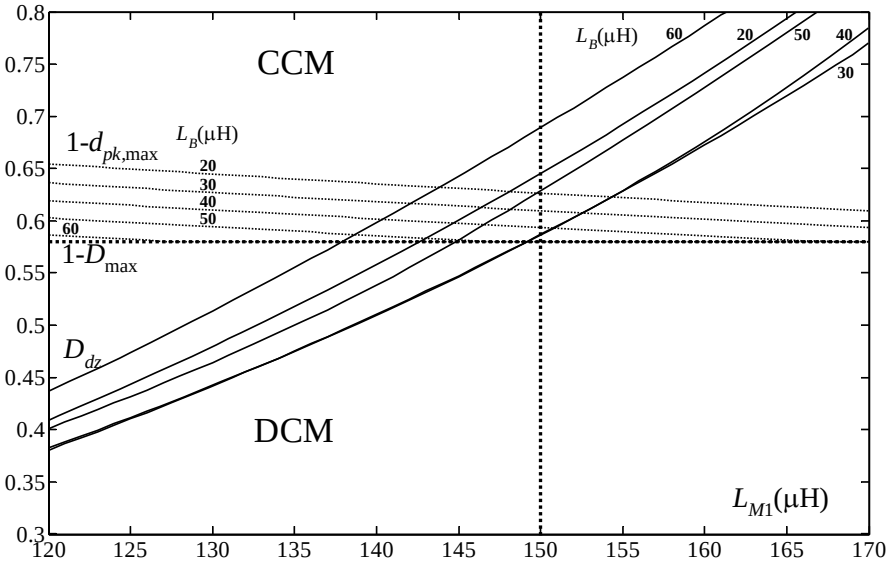


Fig. 3.6 D_{dz} and (1-$d_{pk,\max}$) versus L_{M1} for different L_B, L_{M2} =1.5 mH, at $D_{\max}$= 0.42, V_{ac}= 85 V_{rms}, V_O= 54 V, and P_{out}= 60 W.

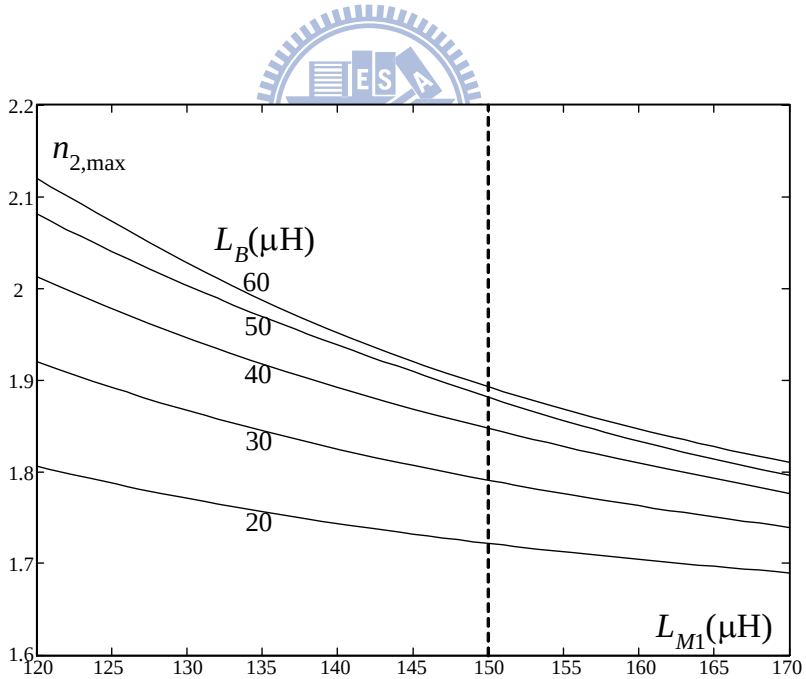


Fig. 3.7 $M_{CB,\min}$ and $n_{2,\max}$ versus L_{M1} for different L_B, L_{M2} =1.5 mH, at $D_{\max}$= 0.42, V_{ac}= 85 V_{rms}, V_O= 54 V, and P_{out}= 60 W.

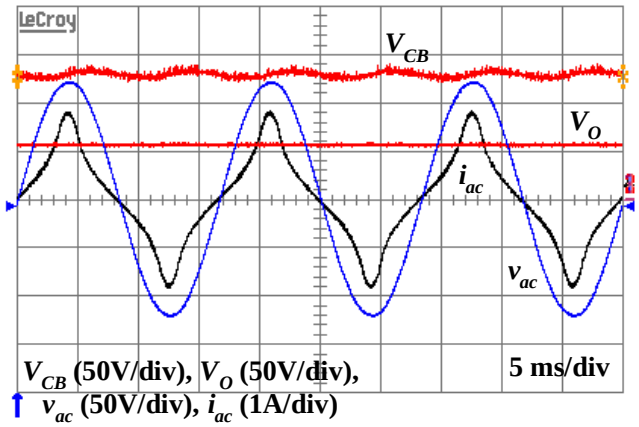
3.5 Experimental Results

For presenting the performance of the prototype based on the proposed topology, the circuit of Fig. 2.6(b) and (c) has been built and tested in the specifications described in Section 3.4. The parameters of the critical components are given in Table 3.5. Because the input current i_{in}= i_{LB} of the proposed converter is pulsating when L_B operates in DCM, the EMI level would be above the limits of standard such as FCC or CISPR. Hence, an input filter which low input displacement angle between input voltage and current, minimum interaction with the converter and system stability is designed to attenuate EMI to meet regulatory specifications and get smooth waveform of line input current i_{ac} in Fig. 3.8 and 10(a). The detailed design and analysis about input filter could be referred to [18] and [19]. The key waveforms at V_{ac}=85 V_{rms}/P_{out}=60 W, V_{ac}=265 V_{rms}/P_{out}=60 W, and V_{ac}=265 V_{rms}/P_{out}=20 W are presented in Fig. 3.8, and the switching current waveforms for M_1 mode and M_2 mode at V_{ac}=130 V_{rms}/R_L=60.24Ω are presented in Fig. 3.9. As can be seen, the shapes of line input current i_{ac} are approaching to the average input currents shown in Fig. 3.2. The measured key waveforms at the worst condition (V_{ac}=85 V_{rms} and P_{out}=80 W) are shown in Fig. 3.10(a) and the power factor is 0.91. Although the line input current is distorted due to the SCM operation of L_B, its harmonic contents still comply with the class D limits as shown in Fig. 3.10(b) and the total harmonic distortion is 45.5%. Fig. 3.11 shows the measured bulk capacitor voltage versus load under line variations. The maximum bulk capacitor voltage is 415.4 V, which is below the commercial size 450 V and occurs at V_{ac}=265 V_{rms} with P_{out}=20 W. Fig. 3.12 shows measured power factor versus load under line variations. It can be seen that the lowest power factor is 0.91 and occurs at the worst condition. The power factors at most conditions are above 0.95 and some even reach 0.99. As described in Section 3.3 and C, L_B tends to operate in CCM as input voltage decreases and load increases, and the worst DCM condition for L_B is set at V_{ac}=85 V_{rms}, and P_{out}=60 W. Hence, L_B begins to operate in semi-continuous conduction

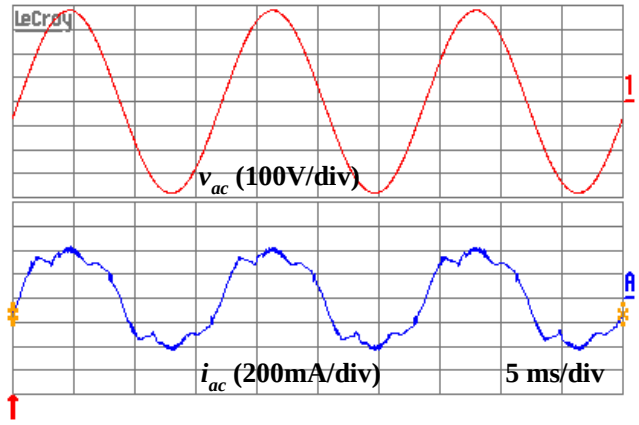
mode (SCM) when P_{out} is greater or equal to 60 W. Consequently, i_{ac} is distorted and PF degrades as can be seen V_{ac}=85 V_{rms} curve in Fig. 3.12. Fig. 3.13 shows efficiency versus load under line variations. The efficiency is greater than 80% in most operating range, and the maximum value is 85.8% at V_{ac}=130 V_{rms} with P_{out}=60 W.

Table 3.5 Parameters of critical components

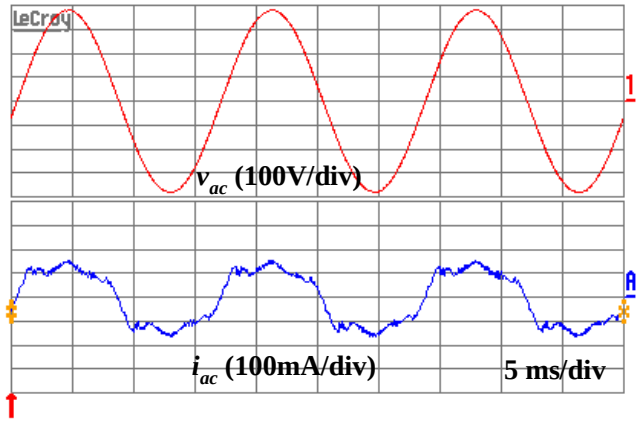
L_B	35 μ H
T_1	L_{M1}=145 μ H; n_1=1.6
T_2	L_{M2}=1.4 mH; n_2=1.8
S	K2968
C_B	470 μ F/450 V
C_O	220 μ F/100 V



(a)

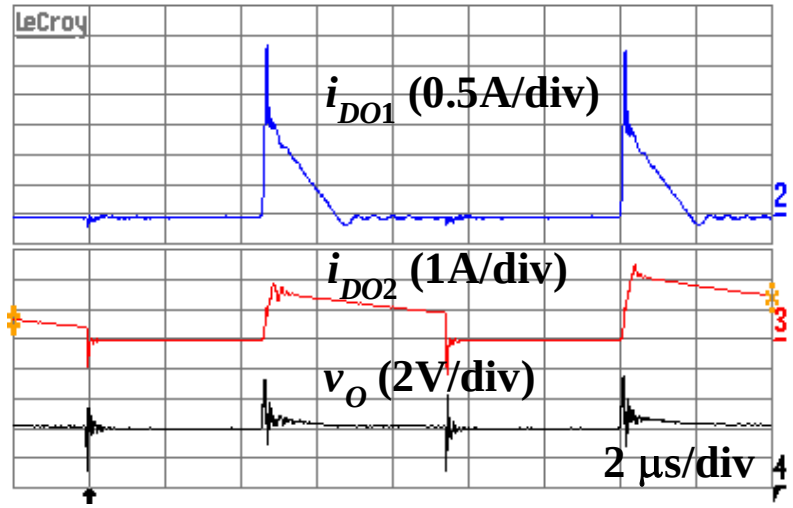


(b)

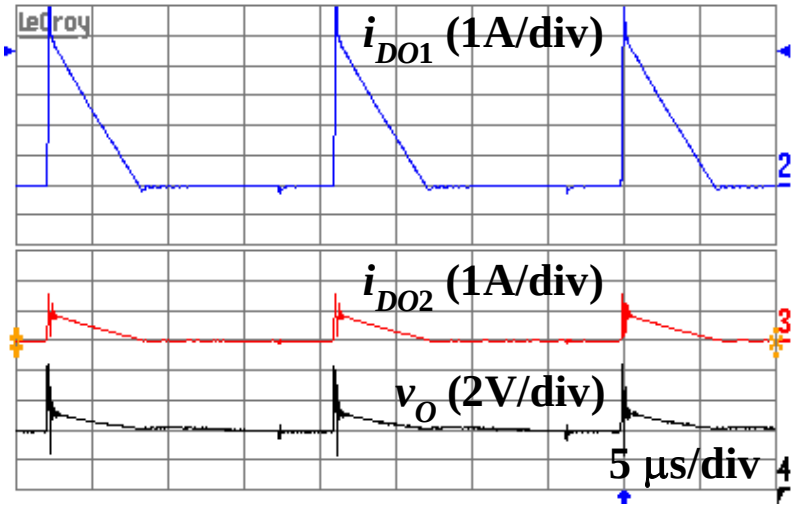


(c)

Fig. 3.8 Measured line voltage, bulk capacitor voltage, line current, output voltage: (a) V_{ac}=85 V_{rms}, P_{out}=60 W, (b) V_{ac}=265 V_{rms}, P_{out}=60 W, and (c) V_{ac}=265 V_{rms}, P_{out}=20 W.

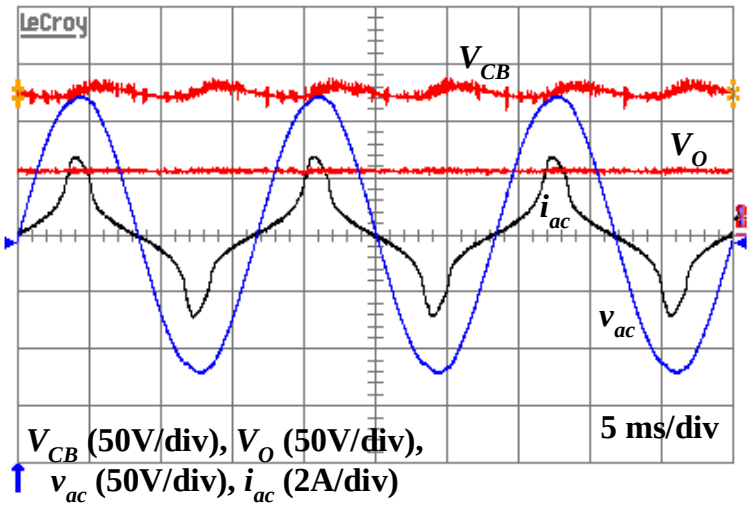


(a)

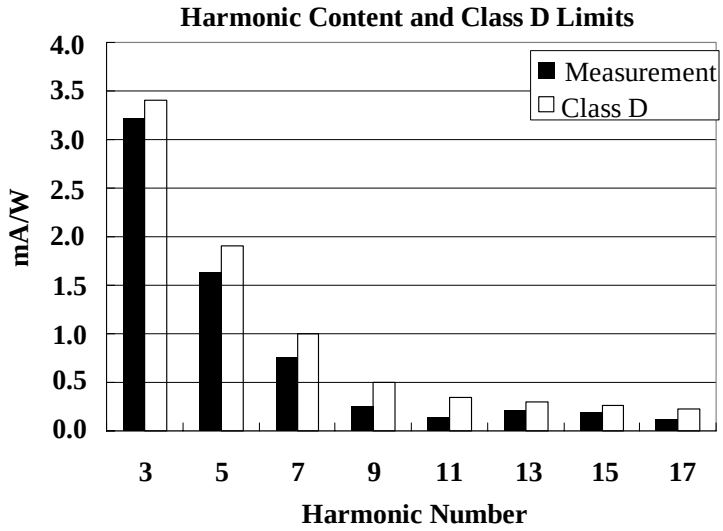


(b)

Fig. 3.9 Measured switching current waveforms: (a) M_1 mode and (b) M_2 mode at V_{ac}=130 V_{rms}, R_L=60.24Ω .



(a)



(b)

Fig. 3.10 (a) Line voltage and line current measured at the worst condition (V_{ac}=85 V_{rms} and P_{out}=80 W) and (b) harmonic content and class D limits.

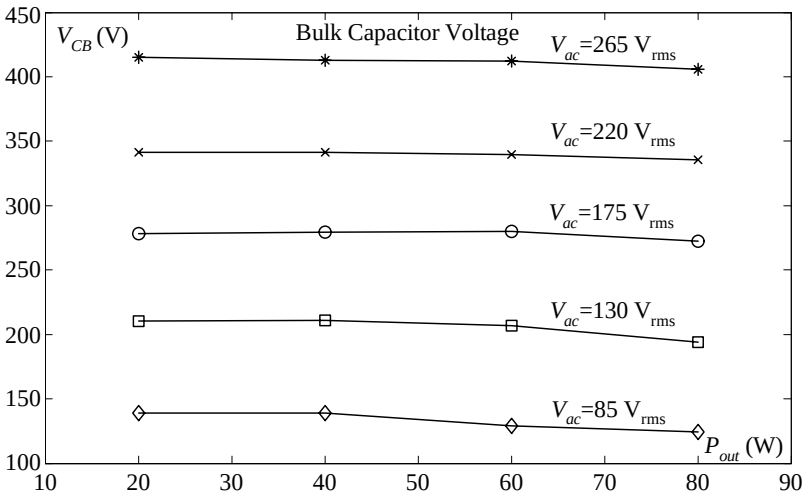


Fig. 3.11 Measured bulk capacitor voltage versus load under line variations.

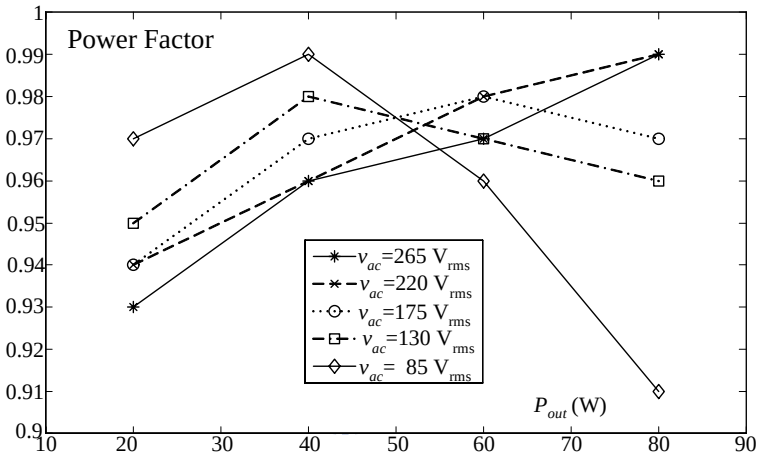


Fig. 3.12 Measured power factor versus load under line variations.

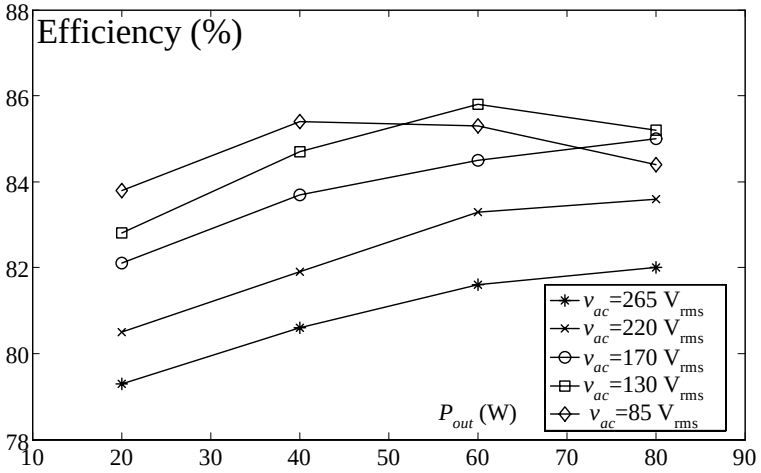


Fig. 3.13 Measured efficiency versus load under line variations.

CHAPTER 4

CONTROLLER DESIGN FOR A SINGLE-SWITCH PARALLEL BOOST-FLYBACK-FLYBACK CONVERTER

The electronic dc loads are wide spread interfacing on the utility system via AC/DC converters. Conventional two-stage AC/DC converter uses the power factor stage to obtain sinusoidal input current and a DC/DC stage to regulate output voltage. The DC/DC stage needs a fast voltage control loop, and the power factor correction (PFC) stage requires three interconnected control loops [24]: a wide bandwidth loop for shaping the input current, a slower loop for output voltage regulation, and a low-pass-filtered line-voltage RMS loop to ensure input-output power balance. This approach can get nearly unity power factor, yet has the drawback of complex circuit and high cost. For the purpose of simplicity and cost down, the two processing stages are integrated to the single stage (S^2) AC/DC converters, such as boost integrated/flyback rectifier/energy storage/dc-to-dc converter (BIFRED) [25], boost input current shaper [4, 26], parallel converter [13, 21, 27] were also presented. In those designs, only one output feedback controller is needed and the input current shaping is automatically achieved. Usually, small signal transfer function and bode plots were employed for compensator design [28]. Unlike traditional dc-to-dc converters, variations in the line voltage and duty ratio cannot be ignored in the AC/DC power factor correction converters modeling. For the S^2 converters [4, 25-26] that integrate a DCM boost inductor with a dc-to-dc stage, the duty ratio has to be held relatively constant to regulate output voltage and improve power factor. The small signal model of such converter with constant duty can be built with double averaging method [29] or Fourier series substitution [10], and verified by frequency response measurement technique [31]. However, for parallel converter, which allows partial power to be processed only once or transfers partial power directly. They have duty ratio varied with line phase to keep output constant [13, 21, 27] or more than one operation modes in half line

cycle [13, 21]. Hence, as described in [32] the small signal transfer function of the converter with variable duty ratio cannot be validated with frequency response instrument, because the operating points are not constant. Fortunately, the problems of operating point changing and different operation modes can be solved by large signal method [32] or switched transformer average model [33]. Nevertheless, the controller design for parallel converter operating under universal voltage and load variation is seldom to see in publishing literatures. If the control loop features are poor, not only additional distortion might appear in the input current but also higher output voltage ripple would be induced.

The single-stage-single-switch (S^4) parallel boost-flyback-flyback converter mentioned in chapter 2 and 3 had been presented by [34] and is of parallel structure for universal usage with high efficiency. The parallel converter operates as other parallel converters have variable duty ratio and two operation modes. Therefore, this dissertation proposes the small signal modeling and the controller design for S^4 parallel boost-flyback-flyback converter. First, the nonlinear large signal models of two operation modes are described according to the operation principle. By linearizing the large signal models, the small-signal models are developed as the state space equations. From the equations, the uncertainty of transfer function caused by the changing of operation points is investigated. To overcome the uncertainty problem, an optically isolated feedback compensator for current mode control is proposed. The compensator is designed according to the transfer function at the boundary of modes and assures small steady state error, fast rise time, and heavily damping within operation range. The dynamic model and designed controller of parallel boost-flyback converter are demonstrated by simulation and experiment.

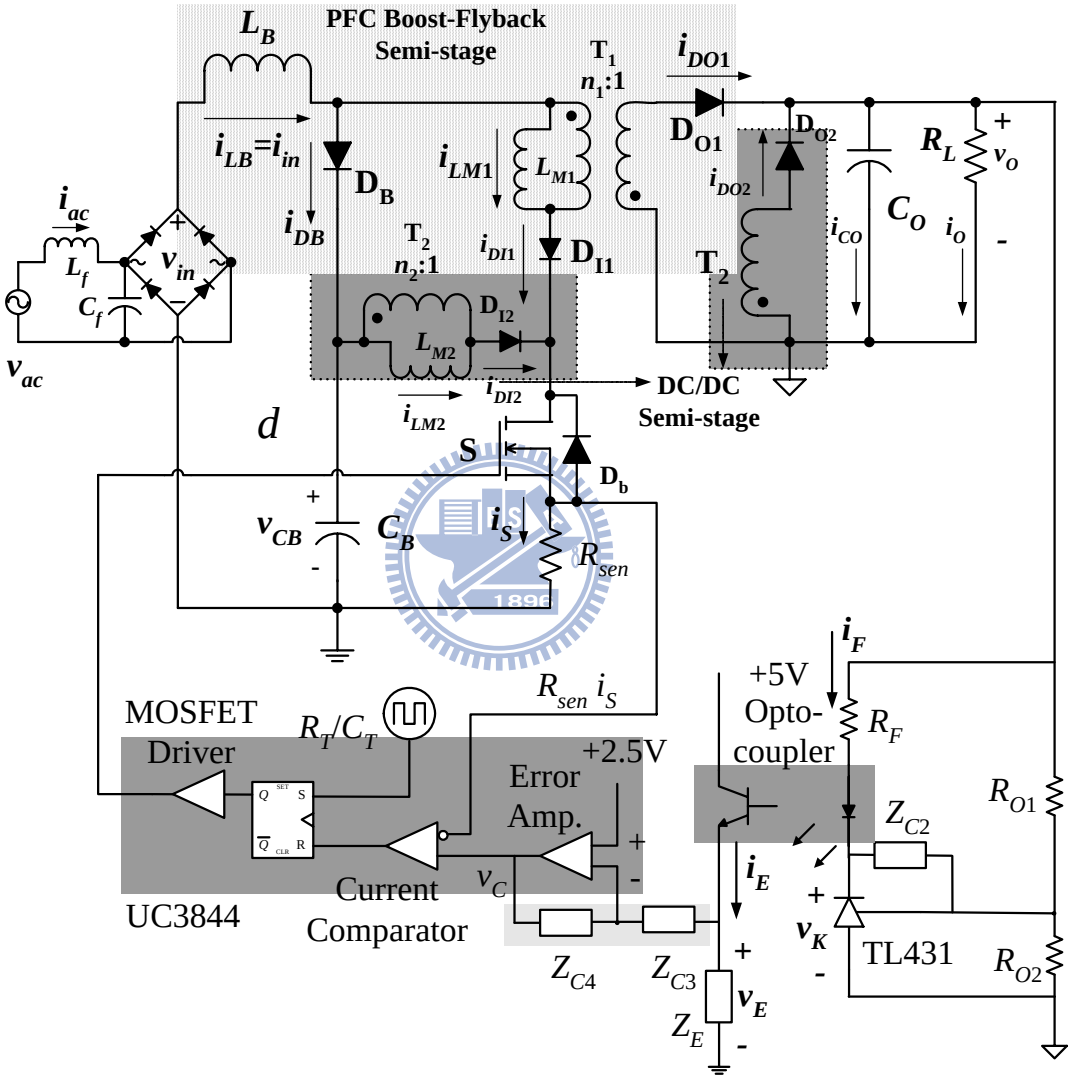


Fig 4.1 Schematic diagram of S^4 parallel boost-flyback-flyback converter with optocoupler feedback current mode controller.

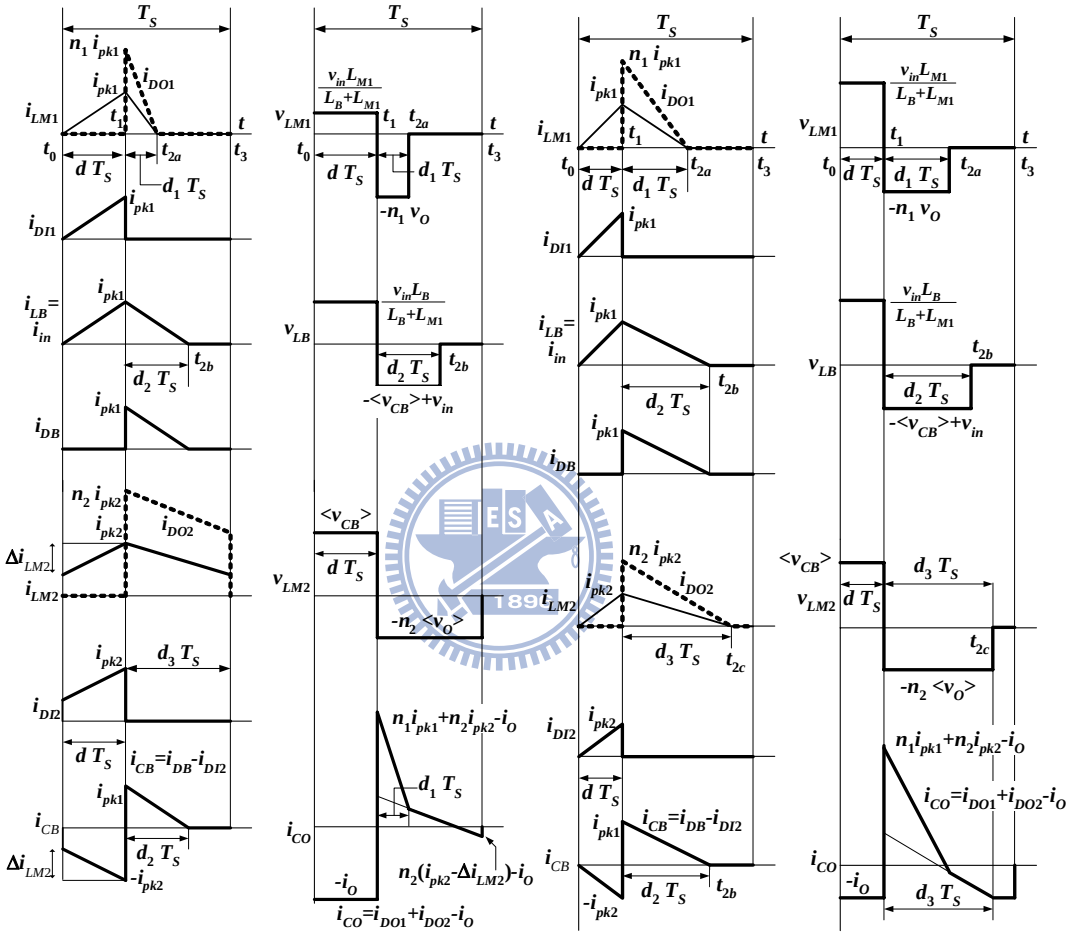
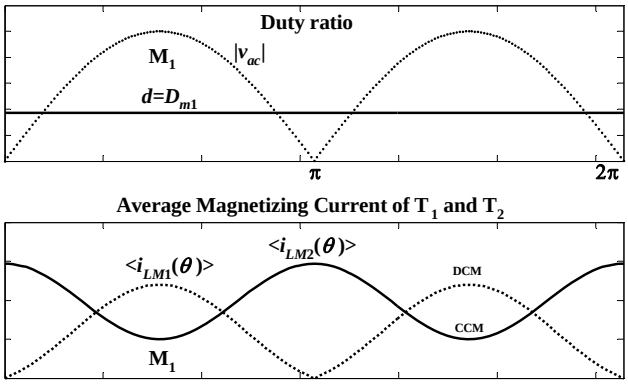
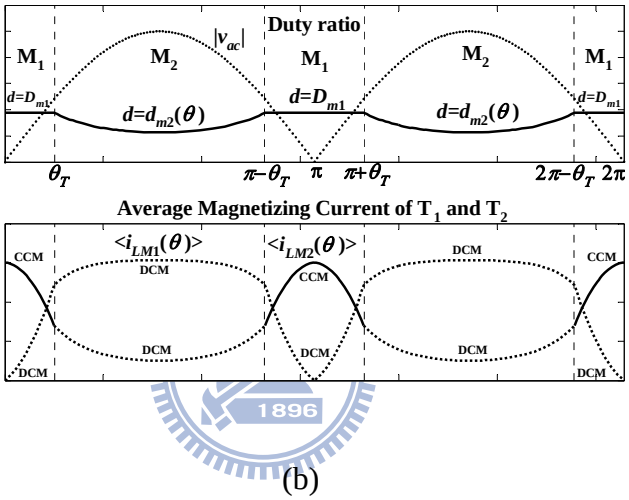


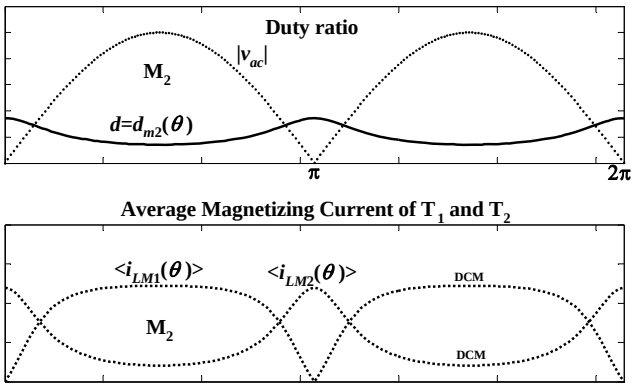
Fig. 4.2 Illustrated waveforms within one switching period: (a) for DCM-DCM boost-flyback semi-stage + CCM flyback DC/DC semi-stage (M_1 mode); (b) for DCM-DCM boost-flyback semi-stage + DCM flyback DC/DC semi-stage DCM (M_2 mode)



(a)



(b)



(c)

Fig. 4.3 Operation waveforms in a line cycle: (a) case I (M_1 mode only), (b) case II (both M_1 and M_2 modes), and (c) case III (M_2 mode only).

4.1 Small Signal Modeling

In this section, both the small-signal modeling for S^4 parallel boost-flyback-flyback converter and current mode control with optocoupler feedback are developed for controller design. The boost-flyback-flyback converter with optocoupler feedback current mode controller is plotted in Fig. 4.1. The waveforms within a switching period for the waveforms for M_1 and M_2 modes are shown in Fig. 4.2(a) and (b), respectively. The major current waveforms and the corresponding duty ratio waveforms of three combination cases are depicted and shown in Fig. 4.3.

4.1.1 M_1 Mode

It can be seen from Fig. 4.1 that there are five energy storage elements L_B, L_{M1}, L_{M2}, C_B and C_O in the converter. For M_1 mode, both L_B and L_{M1} operate in DCM, and their initial and final inductor currents vanish in each switching period T_S. Thus, these inductor currents should not be selected as state variables. Whereas L_{M2} operates in CCM, and thus, only v_{CB}, v_{CO}, and flyback DC/DC transformer magnetizing current i_{LM2} are chosen as the state variables in the following small-signal modeling.

Based on the definition (2.1), the average state variable description of the converter is

$$C_B \frac{d\langle v_{CB}(t)\rangle}{dt} = \langle i_{CB}(t)\rangle \tag{4.1a}$$

$$C_O \frac{d\langle v_{CO}(t)\rangle}{dt} = \langle i_{CO}(t)\rangle \tag{4.1b}$$

$$L_{M2} \frac{d\langle i_{LM2}(t)\rangle}{dt} = \langle v_{LM2}(t)\rangle . \tag{4.1c}$$

Moreover, in DCM, the inductor voltage averaged over a switching period is zero and independent of duty ratio. Hence, two constraints are given by

$$L_{M1} \frac{d\langle i_{LM1}(t)\rangle}{dt} = \langle v_{LM1}(t)\rangle = 0 \tag{4.2a}$$

$$L_B \frac{d\langle i_{LB}(t)\rangle}{dt} = \langle v_{LB}(t)\rangle = 0 \tag{4.2b}$$

and the output equation is expressed as

$$\langle v_O(t)\rangle = \langle v_{CO}(t)\rangle \tag{4.3}$$

From the waveforms in Fig. 4.3, the averaged variables in (4.1a)-(4.2b) can be written as

$$\langle i_{CB}(t)\rangle = \frac{1}{2} i_{pk1} d_2 - \frac{1}{2}\left(i_{pk2} + i_{pk2} - \Delta i_{LM2}\right) d \tag{4.4a}$$

$$\langle i_{CO}(t)\rangle = \frac{1}{2} n_1 i_{pk1} d_1 + \frac{1}{2} n_2 \left(i_{pk2} + i_{pk2} - \Delta i_{LM2}\right)(1-d) - i_O \tag{4.4b}$$

$$\langle v_{LM2}(t)\rangle = \langle v_{CB}(t)\rangle d - n_2 \langle v_{CO}(t)\rangle (1-d) \tag{4.4c}$$

$$\langle v_{LM1}(t)\rangle = \frac{L_{M1}}{(L_B + L_{M1})} v_{in}(t) d - n_1 \langle v_{CO}(t)\rangle d_1 \tag{4.4d}$$

$$\langle v_{LB}(t)\rangle = \frac{L_B}{(L_B + L_{M1})} v_{in}(t) d - \left(\langle v_{CB}(t)\rangle - v_{in}(t)\right) d_2 \tag{4.4e}$$

where

$$i_{pk1} = \frac{v_{in}(t)}{L_B + L_{M1}} d \cdot T_S \tag{4.5a}$$

$$i_{pk2} = \langle i_{LM2}(t)\rangle + \frac{1}{2}\Delta i_{LM2} \tag{4.5b}$$

$$\Delta i_{LM2} = \frac{\langle v_{CB}(t)\rangle}{L_{M2}} d \cdot T_S \tag{4.5c}$$

$$i_O = \frac{\langle v_{CO}(t)\rangle}{R_L} \tag{4.5d}$$

Substituting (4.4d) and (4.4e) into constraint (4.2a) and (4.2b) yields

$$d_1 = \frac{L_{M1}}{(L_B + L_{M1})} \frac{v_{in}(t)}{n_1 \langle v_{CO}(t)\rangle} d \tag{4.6a}$$

$$d_2 = \frac{L_B}{(L_B + L_{M1})} \frac{v_{in}(t)}{\left(\langle v_{CB}(t)\rangle - v_{in}(t)\right)} d \tag{4.6b}$$

Substituting (4.5a)-(4.5c) and (4.6a)-(4.6b) into (4.4a) and (4.4b) yields

$$\langle i_{CB}(t)\rangle = \frac{\alpha \cdot d^2 \cdot v_{in}^2(t)}{\left(\langle v_{CB}(t)\rangle - v_{in}(t)\right)} - \langle i_{LM2}(t)\rangle d \tag{4.7a}$$

$$\langle i_{CO}(t)\rangle = \frac{\beta \cdot d^2 \cdot v_{in}^2(t)}{\langle v_{CO}(t)\rangle} + n_2 \langle i_{LM2}(t)\rangle (1-d) - i_O\,, \tag{4.7b}$$

where

$$\alpha = \frac{L_B}{2 f_S (L_B + L_{M1})^2} \tag{4.8a}$$

$$\beta = \frac{L_{M1}}{2 f_S \left(L_B + L_{M1}\right)^2} \tag{4.8b}$$

Substituting (4.4c) and (4.7a)-(4.8b) into (4.1a)-(4.1c) yields

$$C_B \frac{d\langle v_{CB}(t)\rangle}{dt} = \frac{\alpha \cdot d^2 \cdot v_{in}^2(t)}{\left(\langle v_{CB}(t)\rangle - v_{in}(t)\right)} - \langle i_{LM2}(t)\rangle d \tag{4.9a}$$

$$C_O \frac{d\langle v_{CO}(t)\rangle}{dt} = \frac{\beta \cdot d^2 \cdot v_{in}^2(t)}{\langle v_{CO}(t)\rangle} + n_2 \langle i_{LM2}(t)\rangle (1-d) - i_O \tag{4.9b}$$

$$L_{M2} \frac{d\langle i_{LM2}(t)\rangle}{dt} = \langle v_{CB}(t)\rangle d - n_2 \langle v_{CO}(t)\rangle (1-d) \tag{4.9c}$$

In (4.9a) and (4.9c) C_B is sufficiently large, $\langle v_{CB}\rangle$ can be considered as constant V_{CB}. Besides, a dynamic equation linearized around the operating point is derived as follows. Small perturbations: $\langle v_{CO}\rangle = V_{CO} + \tilde{v}_{CO}$, $\langle i_{LM2}\rangle = I_{LM2} + \tilde{i}_{LM2}$, $v_{in} = V_{in} + \tilde{v}_{in}$, $i_O = I_O + \tilde{i}_O$, and $d = D + \tilde{d}$ are introduced into (4.9a)-(4.9c). Thus, the linearized small-signal model is given by

$$\begin{aligned} [\dot{\tilde{x}}] &= [A]\cdot[\tilde{x}] + [B_1]\tilde{v}_{in} + [B_2]\tilde{i}_O + [B_3]\tilde{d} \\ \tilde{y} &= [C]\cdot[\tilde{x}] \end{aligned} \tag{4.10}$$

where the parameters are expressed as

$$\{\tilde{x}\} = \begin{bmatrix} \tilde{i}_{LM2} & \tilde{v}_{CO} \end{bmatrix}^T,$$

$$[A] = \begin{bmatrix} \frac{a_{11}}{L_{M2}} & \frac{a_{12}}{L_{M2}} \\ \frac{a_{21}}{C_O} & \frac{a_{22}}{C_O} \end{bmatrix},\ [B_1] = \begin{bmatrix} \frac{b_{111}}{L_{M2}} \\ \frac{b_{121}}{C_O} \end{bmatrix},\ [B_2] = \begin{bmatrix} \frac{b_{211}}{L_{M2}} \\ \frac{b_{221}}{C_O} \end{bmatrix},\ [B_3] = \begin{bmatrix} \frac{b_{311}}{L_{M2}} \\ \frac{b_{321}}{C_O} \end{bmatrix},\ [C] = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

$$a_{11} = 0\,,\ a_{12} = -n_2(1-D)$$

$$a_{21} = n_2(1-D),\ \ a_{22} = -\frac{\beta D^2 V_{in}^2}{V_{CO}^2} - \frac{1}{R_L},$$

$$b_{111} = 0,\ \ b_{211} = 0\,,\ b_{311} = V_{CB} + n_2 V_{CO}$$

$$b_{121} = \frac{2\beta D^2 V_{in}}{V_{CO}},\ \ b_{221} = -1\,,\ b_{321} = \frac{2\beta D V_{in}^2}{V_{CO}} - n_2 I_{LM2}$$

(4.11)

In (4.10), $[\tilde{x}]$ is the vector of state variables, $\tilde{d}$ is system input, which is manipulated by the controller, $\tilde{v}_{in}$ and $\tilde{i}_O$ stand for the exogenous disturbances, which are not manipulated by the

controller, and $\tilde{y}$ is the sensed or measured output. Hence, the following five transfer functions for M_1 mode can be derived from (4.10) and (4.11) by Laplace transformation: the open loop audio susceptibility $G_{VV} = \tilde{v}_O(s)/\tilde{v}_{in}(s)$, the line-to-inductor current transfer function $G_{IV} = \tilde{i}_{LM2}(s)/\tilde{v}_{in}(s)$, the duty ratio-to-output transfer function $G_{VD} = \tilde{v}_O(s)/\tilde{d}(s)$, the duty ratio-to-inductor current transfer function $G_{ID} = \tilde{i}_{LM2}(s)/\tilde{d}(s)$, the open loop output impedance $Z_O = \tilde{v}_O(s)/\tilde{i}_O(s)$, where s is a complex variable.

4.1.2 M_2 Mode

For M_2 mode L_{M2} operates in DCM, (4.4a)-(4.4c) are given by

$$\langle i_{CB}(t)\rangle = \frac{1}{2} i_{pk1} d_2 - \frac{1}{2} i_{pk2} d \tag{4.12a}$$

$$\langle i_{CO}(t)\rangle = \frac{1}{2} n_1 i_{pk1} d_1 + \frac{1}{2} n_2 i_{pk2} d_3 - i_O \tag{4.12b}$$

$$\langle v_{LM2}(t)\rangle = \langle v_{CB}(t)\rangle d - n_2 \langle v_{CO}(t)\rangle d_3 = 0 \tag{4.12c}$$

where

$$i_{pk2} = \frac{v_{CB}}{L_{M2}} d \cdot T_S \tag{4.13}$$

With substituting (4.12a)-(4.12b) and (4.13) into (4.1a)-(4.1c), (4.9a)-(4.9c) can be expressed as

$$C_B \frac{d\langle v_{CB}(t)\rangle}{dt} = \frac{\alpha \cdot d^2 \cdot v_{in}^2(t)}{\left(\langle v_{CB}(t)\rangle - v_{in}(t)\right)} - \frac{d^2 \langle v_{CB}(t)\rangle}{2 f_S L_{M2}} \tag{4.14a}$$

$$C_O \frac{d\langle v_{CO}(t)\rangle}{dt} = \frac{\beta \cdot d^2 \cdot v_{in}^2(t)}{\langle v_{CO}(t)\rangle} + \frac{d^2 \langle v_{CB}(t)\rangle^2}{2 f_S L_{M2} \langle v_{CO}(t)\rangle} - i_O \tag{4.14b}$$

$$L_{M2} \frac{d\langle i_{LM2}(t)\rangle}{dt} = 0 \tag{4.14c}$$

With (4.13), (4.14a)-(4.14c), parameters in (4.11) can be reduced to

$$\{\tilde{x}\} = [\tilde{v}_{CB} \quad \tilde{v}_{CO}]^T,$$

$$[A] = \begin{bmatrix} \frac{a_{11}}{C_B} & \frac{a_{12}}{C_B} \\ \frac{a_{21}}{C_O} & \frac{a_{22}}{C_O} \end{bmatrix}, \quad [B_1] = \begin{bmatrix} \frac{b_{111}}{C_B} \\ \frac{b_{121}}{C_O} \end{bmatrix}, \quad [B_2] = \begin{bmatrix} \frac{b_{211}}{C_B} \\ \frac{b_{221}}{C_O} \end{bmatrix}, [B_3] = \begin{bmatrix} \frac{b_{311}}{C_B} \\ \frac{b_{321}}{C_O} \end{bmatrix}, [C] = [0 \quad 1]$$

$$a_{11} = -\frac{\alpha D^2 V_{in}^2}{(V_{CB} - V_{in})^2} - \frac{D^2}{2 f_S L_{M2}}, \quad a_{12} = 0$$

$$a_{21}=\frac{D^2V_{CB}}{f_S L_{M2} V_{CO}},\quad a_{22}=-\frac{\beta D^2 V_{in}^2}{V_{CO}^2}-\frac{D^2V_{CB}^2}{2f_S L_{M2} V_{CO}^2}-\frac{1}{R_L}$$

$$b_{111}=\frac{\alpha D^2 V_{in}\left(2V_{CB}-V_{in}\right)}{\left(V_{CB}-V_{in}\right)^2},\quad b_{211}=0\,,\, b_{311}=\frac{2\alpha D V_{in}^2}{V_{CB}-V_{in}}-\frac{DV_{CB}}{f_S L_{M2}}$$

$$b_{121}=\frac{2\beta D^2 V_{in}}{V_{CO}},\quad b_{221}=-1\,,\, b_{321}=\frac{2\beta D V_{in}^2}{V_{CO}}+\frac{DV_{CB}^2}{f_S L_{M2} V_{CO}}$$

(4.15)

It can be seen that G_{VV}(s), G_{VD}(s), and Z_O(s) for M_2 mode can be derived from (4.10) and (4.15). Furthermore, it can be seen from (4.11) and (4.15) that, the input voltage $V_{in}=V_{pk}\left|\sin\left(\omega_L\cdot t\right)\right|$ in the model is time-dependent, R_L is varied within required range, and D is not fixed in M_2 mode. Furthermore, the small-signal modeling of M_1 is quite different from that of M_2 mode. These modeling uncertainties would be a challenge to design a compensator with robustness.

4.1.3 Current Mode Controller and Optocoupler Feedback

As mentioned in [35], the current-mode controlled converter possesses the advantages of input voltage feed forward characteristic and easy of making current limiting, and optocoupler is the most popular and widely used for necessary isolation of analog error signal. Hence, the commercially available IC UC3844 associated with TL431 based optically feedback circuit is employed to implement the switching control of parallel boost-flyback-flyback converter as shown in Fig. 4.1.The output voltage signal v_O is transferred to UC3844 via TL431 and opto-coupler, the switch current i_S is sensed and fed back to the comparator, then the duty ratio d of control switch S is well controlled.

Its necessary components include TL431, the output voltage error calculation circuit G_{EA} (R_{O1}, Z_{C2}), the optocoupler, and the compensator of current mode control. The TL431, which consists of voltage reference, amplifier and driver, is designed as a shunt regulator for modulating the LED current in response to the feedback voltage error. Then an error voltage is yielded from the optocoupler output, and the current command is further generated from the

compensator A_{OC}, which is implemented using the compensating network (Z_{C3}, Z_{C4}) connected externally. Through properly choosing the low pass filter Z_E and the current compensation network according to the power stage dynamic behavior, the excellent current mode control is yielded. The small signal model of the optocoupler feedback circuit is derived with Laplace transformation as follows:

For M_1 mode, the flyback DC/DC semi-stage operates in CCM. With the CCM current mode control model proposed by Ridley [36], and the control voltage is expressed as $\langle v_C \rangle = V_C + \tilde{v}_C$, duty ratio perturbation $\tilde{d}$ is related to its control perturbation $\tilde{v}_C$ and inductor current perturbation $\tilde{i}_{LM2}$ by the relation of

$$\tilde{d} = F_M \left(\tilde{v}_C - H_e(s) R_{sen} \tilde{i}_{LM2} \right), \tag{4.16a}$$

where

$$F_M = \frac{1}{(S_n + S_e) T_S}, S_n = \frac{V_{CB} \cdot R_{sen}}{L_{M2}}. \tag{4.16b}$$

In (4.16a) and (4.16b), the sampling gain $H_e(s) \approx 1$, the slope of saw-tooth ramp S_e can be ignored and current mode control modulator gain F_M is equal to the on-time slope of the current-sense waveform S_n, as duty ratio is smaller than 0.5 for UC3844. The small signal block diagram of parallel boost-flyback-flyback converter with optocoupler feedback current mode controller for M_1 mode is shown in Fig. 4.4(a), and the control-to-output transfer function is given as

$$G_{VC}(s) = \frac{\tilde{v}_O(s)}{\tilde{v}_C(s)} = \frac{F_M G_{VD}(s)}{1 + F_M R_{sen} G_{ID}(s)} \tag{4.17}$$

For M_2 mode, the flyback DC/DC semi-stage operates in DCM. According to the DCM current mode control model [37], $\tilde{d}$ is given by

$$\tilde{d} = F_M \tilde{v}_C. \tag{4.18}$$

The small signal block diagram of parallel boost-flyback-flyback converter with optocoupler feedback current mode controller for M_2 mode is shown in Fig. 4.4(b), and the control-to-output transfer function is given as

$$G_{VC}(s) = F_M G_{VD}(s). \tag{4.19}$$

The output sensing feedback transfer function is given by

$$-G_{EA}(s) = \frac{\tilde{v}_K(s)}{\tilde{v}_O(s)} = -\frac{Z_{C2}(s)}{R_{O1}}. \tag{4.20}$$

The transfer function of compensator and optocoupler is given by

$$-A_{OC}(s) = \frac{\tilde{v}_C(s)}{\tilde{v}_{RF}(s)} = -\frac{Z_{C4}(s)\cdot Z_E(s)\cdot CTR}{Z_{C3}(s)\cdot R_F}, \tag{4.21}$$

where $\tilde{v}_{RF}(s) = \tilde{v}_O(s) - \tilde{v}_K(s)$ and *CTR* is current transfer ratio.

The output-to-control transfer function can be expressed as

$$\frac{\tilde{v}_C(s)}{\tilde{v}_O(s)} = -A_{OC}(s)(1 + G_{EA}(s)). \tag{4.22}$$

The loop gain is derived as

$$T = G_{VC}(s)A_{OC}(s)(1 + G_{EA}(s)) \tag{4.23}$$

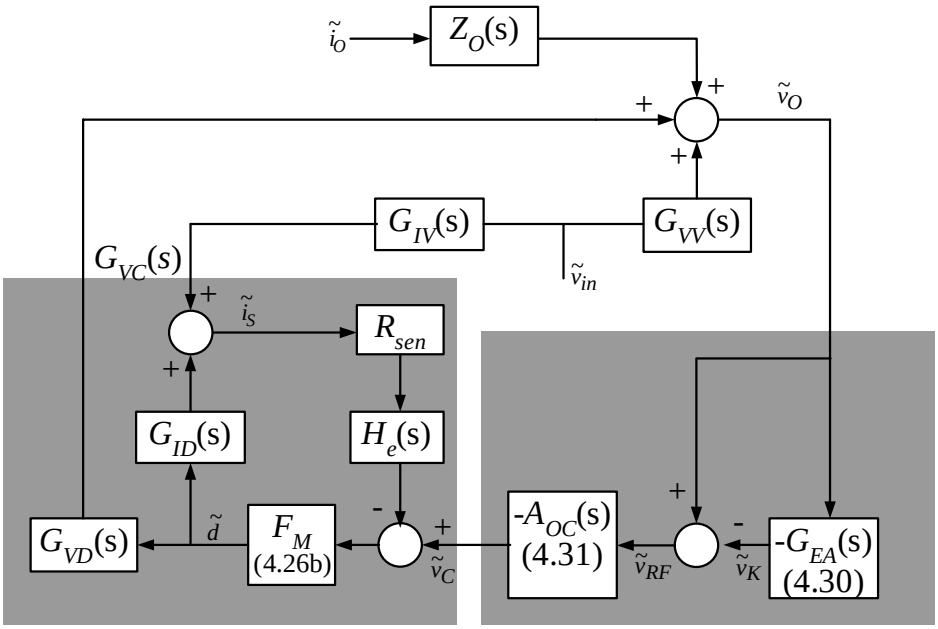
For the case of $G_{EA}(s) >> 1$, (4.23) can be obtained as

$$T \approx G_{VC}(s)G_C(s), \tag{4.24}$$

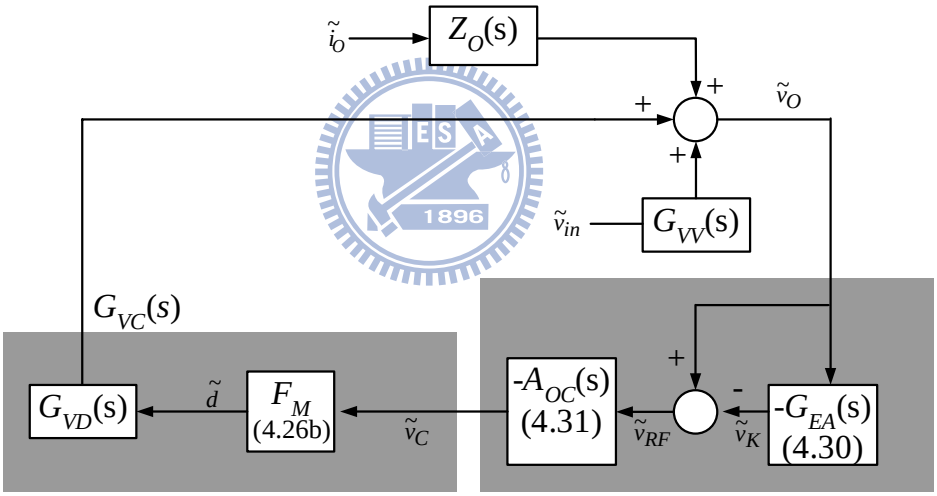
where $G_C(s)$ is the compensation transfer function.

$$G_C(s) = A_{OC}(s)\cdot G_{EA}(s). \tag{4.25}$$

As mentioned in [28], it is desirable to maximize loop gain *T* in order to achieve the best rejection of line and load disturbances.



(a)



(b)

Fig. 4.4 Small signal block diagram: (a) M_1 mode and (b) M_2 mode.

4.2 Controller Design

4.2.1 Model Uncertainty

To investigate the characteristic of the model obtained in preceding section the parallel converter of the design specifications and component values listed in Table 4.1 are taken as an

example. With substituting the parameters in Table 4.1 into equation (4.10), (4.11), and (4.15), it can be seen that the coefficient matrices would vary as the operating point changes, and is so called model uncertainty. The open loop poles and zero of various line phases ($\omega_L \cdot t$ =0 to $\pi/2$) at a certain condition (V_{ac}=85 V_{rms} and P_{out}=30 W) listed in Table 4.2. The effect of the second pole and zero are ignored, because they are both far away from origin and on the left real axis. It can be seen that the dominant pole moves toward origin when phase is near transition angle, which is between $(\pi/20)3$ and $(\pi/20)4$. In addition, the locations of poles and zeros on both sides of the transition angle violently change when line phase cross the transition angle, because the dynamic equations of M_1 and M_2 modes are quit different. Hence, the closed loop system with designed compensator should be stable over the operation range, especially at the transition angle.

Table 4.1 Converter specifications and parameters of components

v_{in}	85-265 V_{rms}
V_O	54 V
P_{out}	60 W
f_S	100 kHz
L_B	35 μ H
T_1	L_{M1}=145 μ H; n_1=1.6
T_2	L_{M2}=1.4 mH; n_2=1.8
S	K2968
C_B	470 μ F/450 V
C_O	1000 μ F/63 V

Table 4.2 Open loop poles and zero for various phases

NO	$\omega_L \cdot t$	Mode	Pole	Pole	Zero
1	0	M_1	-88.16	$-1.6685*10^5$	$2.015*10^5$
2	$(\pi/20)1$	M_1	-86.97	$-1.6685*10^5$	$2.425*10^5$
3	$(\pi/20)2$	M_1	-83.52	$-1.6686*10^5$	$5.9211*10^5$
4	$(\pi/20)3$	M_1	-78.14	$-1.6688*10^5$	$-4.7536*10^5$
5	$(\pi/20)4$	M_2	-2.8688	-93.5279	-2.5704
6	$(\pi/20)5$	M_2	-3.8504	-93.5279	-4.0014
7	$(\pi/20)6$	M_2	-5.7128	-93.5279	-6.1503
8	$(\pi/20)7$	M_2	-8.8468	-93.5279	-9.5094
9	$(\pi/20)8$	M_2	-13.3798	-93.5279	-14.2412
10	$(\pi/20)9$	M_2	-18.1843	-93.5279	-19.2016
11	$\pi/2$	M_2	-20.4032	-93.5279	-21.4826

* Operation conditions is at v_{ac}=85 V_{rms} and P_{out}=30 W.

4.2.2 Controller design

In order to generate the complex duty d_{m2} in (4.9), the controlled system had to possess small rising time, low overshoot, and zero steady state error. In addition, the compensator also can generate the correct duty d in (3.3) and (3.6) with different operation modes and points. Since the coefficient matrices in (4.11) and (4.15) varies as the operating point changes, especially the open loop poles and zero of the system move as the line phase increases and violently change at transition angle. Hence, the compensator is designed so that the loop gain has desired dc gain, gain crossover frequency, and phase margin at the transition angle over the operation range. The feedback control loop shown in Fig. 4.1 is implemented with $Z_{C2}=R_{C2}+\frac{1}{C_{C2}\cdot s}$, $Z_{C3}=R_{C3}\|\frac{1}{C_{C3}\cdot s}$, and $Z_{C4}=R_{C4}\|\frac{1}{C_{C4}\cdot s}$. Consequently, the transfer functions

of error amplifier and compensator can be obtained as

$$G_{EA}(s)=\frac{g_1\left(\frac{s}{\omega_2}+1\right)}{s} \tag{4.26a}$$

and

$$A_{OC}(s)=\frac{g_2\left(\frac{s}{\omega_3}+1\right)}{\left(\frac{s}{\omega_4}+1\right)} \tag{4.26b}$$

where

$$g_1=\frac{1}{R_{O1}\cdot C_{C2}},\ g_2=\frac{R_{C4}\cdot R_E\cdot CTR}{R_{C3}\cdot R_F},\ \omega_2=\frac{1}{R_{C2}\cdot C_{C2}},\ \omega_3=\frac{1}{R_{C3}\cdot C_{C3}},\ \omega_4=\frac{1}{R_{C4}\cdot C_{C4}}. \tag{4.26c}$$

In (4.26a), there is a pole at zero frequency so that the gain could be kept high at dc level. The design criteria of the parameters in (4.26c) are shaping the loop frequency response by placing pole ω_4 near the crossover frequency ω_C, setting the zeros ω_2 and ω_3 below ω_C and near the pole of plant. The good output regulation accuracy can be achieve by increasing dc gain, which can be expressed as

$$g_{dc}=G_{VC}(0)\cdot A_{OC}(0) \tag{4.27}$$

Consequently, the designed corresponding circuit parameters are listed in Table 4.3. The dc gain g_{dc}, the gain crossover frequencies ω_{gc}, and phase margins P_m of loop gain for various conditions are listed in Table 4.4. It can be seen that the compensated system has dc gain of 58.4818 dB, crossover frequency of $1.3349\cdot10^5$ rad/s and phase margin of 67.5056 degrees at least.

Table 4.3 Parameters of controller and optocoupler circuit

R_{O1}	22kΩ	R_E	2.4kΩ
R_{O2}	1.05kΩ	R_F	18kΩ
R_{C2}	4.4kΩ	CTR	1
R_{C3}	510Ω	C_{C2}	22nF
R_{C4}	33kΩ	C_{C3}	100nF
R_{sen}	0.22Ω‖1Ω	C_{C4}	470pF

Table 4.4 Gain crossover frequency and phase margin for various conditions

NO	v_{ac} (V_{rms})	P_{out} (W)	θ_T (rad)	Mode	Open Loop system			Compensated loop		
					Pole	Pole	Zero	g_{dc} (dB)	ω_{gc} (rad/s)	P_m (deg)
1	85	30	0.6271	M_1	-71.43	$-1.669\cdot10^5$	$-1.4615\cdot10^5$	70.3268	$1.5334\cdot10^5$	105.4899
2	85	30	0.6271	M_2	-2.8638	-93.5279	-2.5607	74.8905	$3.7717\cdot10^5$	95.1699
3	175	30	0.3721	M_1	-91.37	$-1.319\cdot10^5$	$-3.401\cdot10^5$	70.2323	$1.3430\cdot10^5$	79.0114
4	175	30	0.3721	M_2	-0.5638	-93.5279	-0.09642	58.4818	$2.9587\cdot10^5$	96.5204
5	265	30	0.2743	M_1	-105.3	$-1.2099\cdot10^5$	$-6.1354\cdot10^5$	69.7509	$1.3349\cdot10^5$	67.5056
6	265	30	0.2743	M_2	-0.257	-93.5279	0.06242	60.7801	$2.7037\cdot10^5$	97.0965
7	85	60	1.1972	M_1	-109.2	$-1.7128\cdot10^5$	$-4.4395\cdot10^4$	66.4146	$5.5232\cdot10^5$	106.1982
8	85	60	1.1972	M_2	-42.5721	-187.0557	-44.9171	76.5502	$7.8111\cdot10^5$	92.5365
9	175	60	0.7706	M_1	-113.4	$-1.3303\cdot10^5$	$-6.7166\cdot10^4$	68.2781	$3.6071\cdot10^5$	105.0967
10	175	60	0.7706	M_2	-1.874	-187.0557	-1.9477	74.2250	$6.0540\cdot10^5$	93.2640
11	265	60	0.6609	M_1	-121	$-1.2156\cdot10^5$	$-8.0031\cdot10^4$	68.5006	$3.0272\cdot10^5$	103.4549
12	265	60	0.6609	M_2	-0.6273	-187.0557	-0.591	72.5892	$5.5262\cdot10^5$	93.5710

4.3 Simulation and Experimental Results

Since the small-signal behavior predicted by means of the average model cannot be measured with frequency instrument directly, the validation of the proposed model together with designed feedback control loop will be verified in the time domain. The specification of the prototype is shown in Table 4.1, and the parameters of control circuits are shown in Table 4.3.

For comparison purpose, the theoretical model, PSPICE simulation and experimentally measured waveforms of the boost-flyback-flyback at V_{ac} = 265V_{rms} and P_{out}=60W are put to-

gether and shown in Fig. 4.5-4.7 From the waveforms in Fig. 4.5 and 4.6, it is clear that the theoretical model and PSPICE simulation waveforms correspond very well in $<i_{LB}>$, $<i_{DB}>$, $<i_{DI1}>$, $<i_{DO1}>$, and $<i_{DO2}>$. The waveforms correspond well in d for M_2 mode, but PSPICE d waveform for M_1 mode varies because of the feedback effect of v_O ripple. Furthermore, the PSPICE simulation and experimentally measured waveforms are similar in i_{ac} shape and steadily stable in v_O in Fig. 4.6 and 4.7. It can be seen in Fig. 4.7 that i_{ac} is slightly distorted form $<i_{LB}>$ because of the characteristics of line filter and snubber. This doesn't affect discerning the modes of M_1 and M_2. Hence the theoretical model can be verified.

To show the input current shape and output voltage regulation, the measured power factor, output voltage, and output ripple with different line inputs and output loads are given in Table 4.5. The maximum output ripple is 170.573 mV, and occurs at 265 V_{rms} and 60 W. The data tabulation shows that the converter with properly designed controller has high power factor and small steady state error over the entire operation range.

The PSPICE dynamic waveforms for positive load changing from 97.2 Ω to 48.6 Ω are shown in Fig. 4.8(a), and waveforms for negative load changing from 48.6 Ω to 97.2 Ω are shown in Fig. 4.8(b), both Fig 4.8(a) and (b) are at V_{ac} = 85 V_{rms}. The output ripple voltages are 0.21 V at 97.2 Ω and 0.26 V at 48.6 Ω, the steady state error is smaller than 0.5%, and the settling time is small than 1.111 ms. The measured dynamic waveforms for positive load stepping from 0.555 A to 1.110 A are shown in Fig. 4.9(a), and waveforms for negative load changing from 1.110 A to 0.555 A are shown in Fig. 4.9(b), both Fig 4.9(a) and (b) are at V_{ac} = 85 V_{rms}. The overshoot or dropped voltages are small than 0.1 V, the settling time is small than 2 ms, and the output ripple voltage is very small. Accordingly, the simulation and experiment results in Fig. 4.8 and Fig. 4.9 match well in the superior dynamic response. Moreover, the duty cycle and the line current are adjusted to the new load conditions instantaneously. Hence, the converter does not require several line cycles to reach the new steady state conditions. Because the controlled system possesses fast dynamic response and tightly regu-

lated output voltage, the $<i_{ac}>$ can have low harmonics and high power factor as shown in Table 4.5.

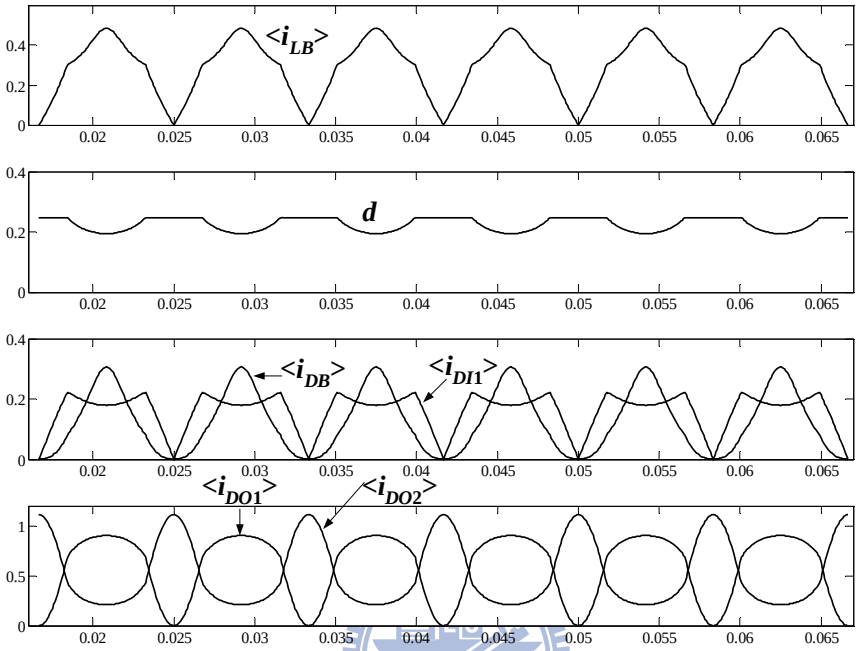


Fig. 4.5 Theoretical waveforms of the parallel boost-flyback-flyback converter at V_{ac} = 265 V_{rms} and P_{out}=60 W.

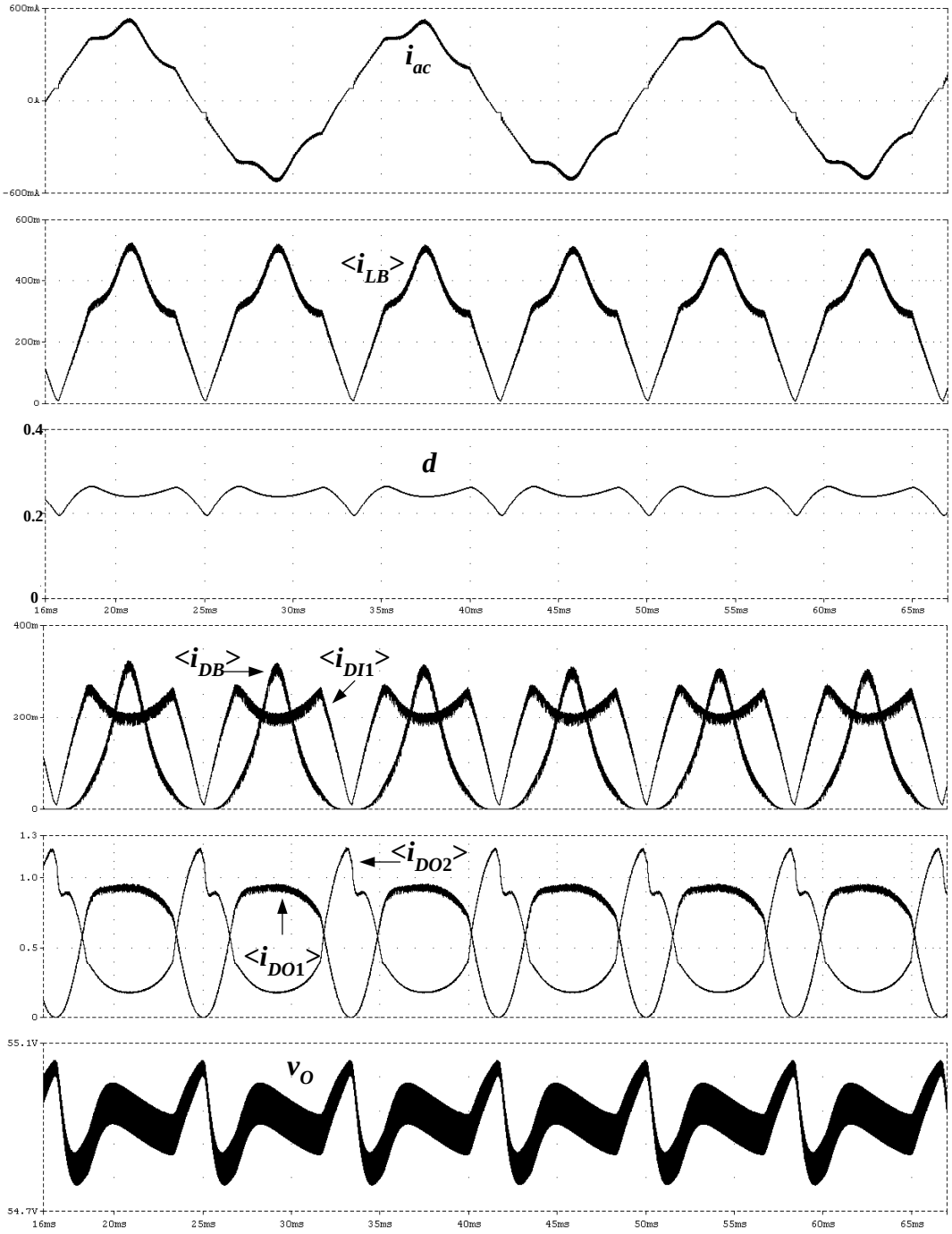
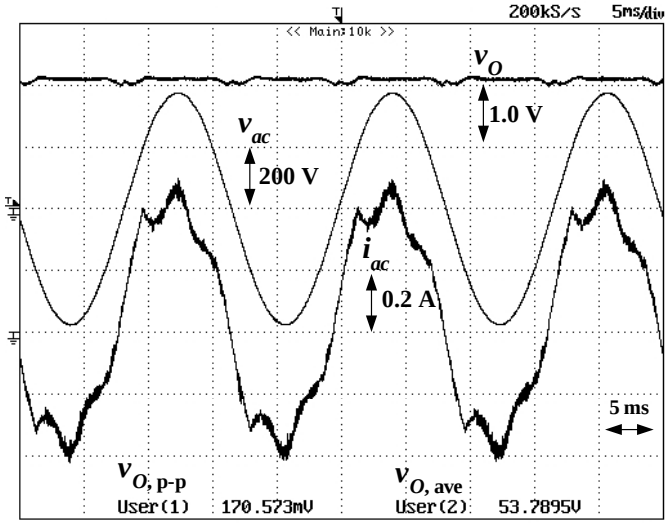


Fig. 4.6 PSPICE simulation waveforms of the parallel boost-flyback-flyback converter at V_{ac} = 265 V_{rms} and P_{out}=60 W.

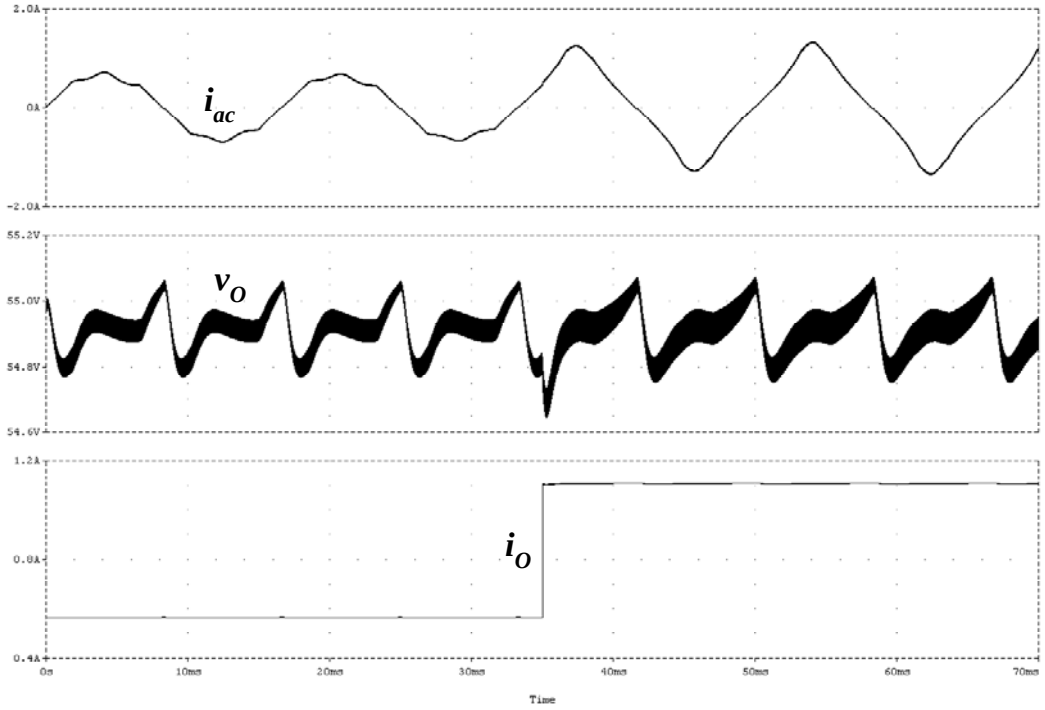


v_{ac}: 200 V/div, i_{ac}: 0.2 A/div, v_O: 1.0 V/div

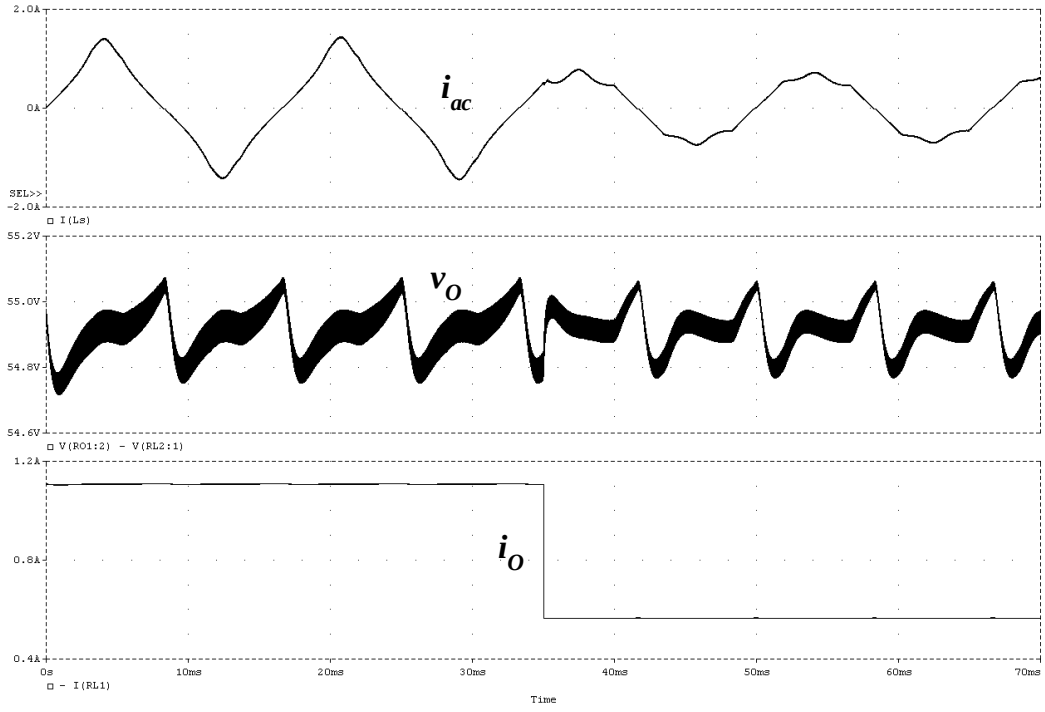
Fig. 4.7 Experimental waveforms of the parallel boost-flyback-flyback converter at V_{ac} = 265 V_{rms} and P_{out}=60 W.

Table 4.5 Measured power factor, load regulation, and ripple voltage

V_{ac} (V_{rms})	R_L (Ω)/P_{out} (W)	PF	$v_{O,ave}$ (V)	$v_{O,pp}$ (mV)
85	98.03/30	0.98	53.8341	83.3333
175	98.03/30	0.95	53.8341	85.9375
265	98.03/30	0.93	53.8306	105.469
85	49.01/60	0.97	53.8074	175.781
175	49.01/60	0.99	53.8011	147.135
265	49.01/60	0.95	53.7895	170.573

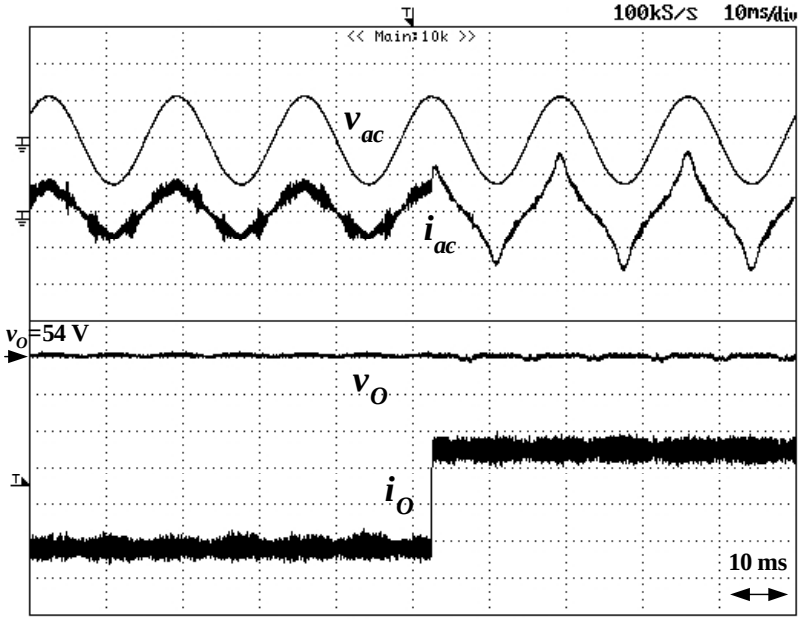


(a)



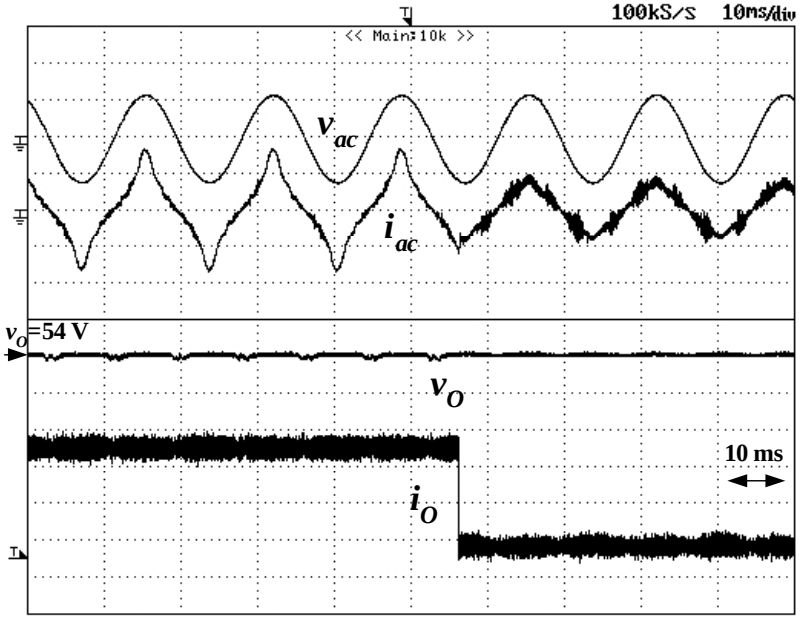
(b)

Fig. 4.8 PSPICE simulation dynamic response of the parallel boost-flyback-flyback converter at V_{ac} = 85 V_{rms}: (a) positive load step and (b) negative load step.



v_{ac}: 100 V/div, i_{ac}: 1.0 A/div, v_O: 1.0 V/div, i_O: 0.2 A/div

(a)



v_{ac}: 100 V/div, i_{ac}: 1.0 A/div, v_O: 1.0 V/div, i_O: 0.2 A/div

(b)

Fig. 4.9 Experimental dynamic response of the parallel boost-flyback-flyback converter at V_{ac} = 85 V_{rms}: (a) positive load step and (b) negative load step.

CHAPTER 5

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

5.1 Conclusions

In conventional AC/DC converters design, a two-stage structure was usually employed for performing PFC and output regulation simultaneously. However, it is preferred to employed S^2 converter for low power products because of reduced component count and low cost. No matter in the conventional two-stage converter or S^2 AC/DC converter, it can be seen that part of the power is repeatedly processed or recycled. To improve the power processing and achieve the cost-effective objective simultaneously, this dissertation explores advanced techniques for S^2 parallel AC/DC converters.

Conventional parallel AC/DC converters have high efficiency because of reduced power processing. However, they either suffer from complex circuit or not good efficiency. To upgrade the performance of the conventional parallel converters, a novel S^2 PPFC scheme are presented. In the PPFC scheme, the line power is fed to SSTO boost-flyback semi-stage that contains boost cell and flyback cell, and split to two power flow streams. The main power flow stream is processed only by flyback cell, and the remaining input power stream is stored in bulk capacitor by boost cell and taken off by DC/DC semi-stage for regulating output power. Theoretical analysis of SSTO boost-flyback circuit shows that as the boost cell and flyback cell operate in DCM, and duty ratio and switching frequency are constants, the arrangement of smaller ratio of boost inductor can result in higher power factor. With the scheme, a family of S^2 parallel converters is generalized.

After analyzing one of the S^2 parallel families, S^4 parallel boost-flyback-flyback converter, it can be seen that there are two modes with self-PFC property and hence three cases may happen. And power flow analysis shows that the direct power ratio is dependent on the operation conditions and inductance. Furthermore, the voltage gain of the boost cell could be con-

trolled with adjusting the inductance ratio and the inductance of T_2. To keep boost cell and flyback cell in DCM and allow flyback DC/DC semi-stage regulating output, the design equations are derived. By the design equations, the design procedure for satisfying the harmonic regulation and keeping the bulk capacitor voltage below commercial limit under universal range are also presented. With this procedure, an 80 W prototype was built and tested. The experimental results show that the voltage across bulk capacitor is kept under 415.4 V for full range operation (85-265 V_{rms}) and load (20-80 W). The maximum power factor is 0.99 and the measured line current harmonic contents at the worst condition comply with the IEC61000-3-2 class D limits. The maximum efficiency is 85.8%. This new circuit structure also can be extended to more alternative parallel combinations. Therefore, the proposed parallel converter presents an overall good performance in the main aspects of universal single-stage PFC converters.

The S^4 parallel boost-flyback-flyback converter operates as other parallel converters have two operation modes in a half line cycle and duty cycle varied with line phase in one mode. After linearizing the large signal models of M_1 and M_2 modes, the small-signal models of the two modes are developed as the dynamic equations, which involve input voltage and load current as disturbances. From the equations, the small-signal transfer functions could be derived. It can be shown that the dynamic characteristic varies as the operation point changes, and violently changes at the transition angle. To solve the problem of model uncertainty, an optically isolated compensator is proposed. By properly design the zeros and poles of compensator, the loop gain could have enough dc gain, crossover frequency, and phase margin at all conditions. Hence, the controlled converter possesses small steady state error, fast rise time, and heavily damped within operation range. The theoretical model, PSPICE simulation, and experimentally measured waveforms match well in steady state and dynamic response. Hence, the model and dynamic of parallel boost-flyback converter with the designed compensator are verified over wide operation range by the results of simulation and

experiment.

In conclusion, the dissertation provides a practical solution to implement simple, reliable, efficient, cost-effective, and well-controlled parallel AC/DC converters.

5.2 Suggestions for Further Work

The dissertation employs SSTO boost-flyback semi-stage to generate two power flow streams, and one of the streams is for direct power transferring. However, there are one inductor and two transformers in the circuit. Hence, the suggested further work is to realize magnetic integration circuits by integrating the boost inductor and two transformers with single magnetic core. This implementation will result in smaller size, lighter weight and lower cost as well as more attraction for low power applications.

To further promote the conversion efficiency and power rating of the proposed converters, several topics could be the potential further work for this objective. Since DCM boost-flyback semi-stage results rich EMI in ac source and high current stress of control switch, the suggested further work is to push boost-flyback semi-stage in CCM with soft-switching technique, such as active clamp circuit or zero-voltage-transition (ZCT) circuit, etc. These techniques can effectively achieve soft-switching and voltage spike suppression at turn-off of the power switch. Moreover, although this dissertation focuses on single stage AC/DC converter, there still exists potential for S^2 PPFC inverter. The inverter would be applicable to ballast of fluorescent and high intensity discharge (HID) lamp.

REFERENCES

[1] *Electromagnetic Compatibility (EMC)*, Part 3, International Standard IEC61000-3-2, 2001.

[2] M. J. Willers, M. G. Egan, J. M. D. Murphy, and S. Daly, "A BIFRED converter with a wide load range," in *Proc. IEEE IECON'94*, Bologna, Italy, 1994, pp 226-231.

[3] R. Redl, L. Balogh, and N. O. Sokal, "A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage," in *Proc. PESC'94*, Taipei, Taiwan, 1994, pp.1137-1144.

[4] L. Huber, J. Zhang, M. M. Jovanovic, and F. C. Lee, "Generalized topologies of single-stage input-current-shaping circuits," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 508-513, Jul. 2001.

[5] F. Tsai, P. Markowski, and E. Whitcomb, "Off-line flyback converter with input harmonic correction," in *Proc. IEEE INTELEC'96, Annu. Meeting*, 1996, pp. 120-124.

[6] J. Zhang, L. Huber, M. M. Jovanovic, and F. C. Lee, "Single-stage input-current-shaping technique with voltage doubler-rectifier front end," *IEEE Trans. Power Electron.*, vol. 16, no. 1, pp. 55-63, Jan. 2001.

[7] L. Huber and M. M. Jovanovic, "Single-stage, single-switch, isolated power supply technique with input-current-shaping and fast output-voltage regulation for universal input-voltage-range applications," in *Proc. IEEE APEC'97*, 1997, pp. 272-280.

[8] J. Qian, Q. Zhao, and F. C. Lee, "Single-stage single-switch power factor correction (S^4-PFC) ac/dc converters with dc bus voltage feedback," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1079-1088, Nov. 1998.

[9] Y. Jiang, F. C. Lee, G. Hua, and W. Tang, "A novel single-phase power factor correction scheme," in *Proc. IEEE APEC'93*, San Diego, CA, 1993, pp. 287-292.

[10] Y. Jiang and F. C. Lee, “Single-stage single-phase parallel power factor correction scheme,” in *Proc. IEEE PESC’94*, Taipei, Taiwan, 1994, pp. 1145-1151.

[11] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, “Single phase power factor correction: a survey,” *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 749-755, May. 2003.

[12] J. Sebastian, P. J, Villegas, F. Nuno, O. Garcia, and J. Arau, “Improving dynamic response of power-factor pre-regulators by using two-input high-efficient post-regulators,” *IEEE Trans. Power Electron.* , vol. 12, no. 6, pp. 1007-1016, Nov. 1997.

[13] A. Lazaro, A. Barrado, M. Sanz, V. Salas, and E. Olias, “New power factor correction ac-dc converter with reduced storage capacitor voltage,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 384-397, Feb. 2007.

[14] J. Y. Lee and M. J. Youn, “A single-stage power-factor-correction converter with simple link voltage suppressing circuit (LVSC),” *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 572-584, Jun. 2001.

[15] H. Y. Li and L. K. Chang, “A single stage single switch parallel ac/dc converter based on two-output boost-flyback converter,” in *Proc. PESC’06*, Jeju, Korea, 2006, pp. 2501-2507.

[16] R. W. Erickson, Fundamentals of Power Electronics, New York: Chapman & Hall, 1997.

[17] G. Moschopoulos and P. Jain, “Single-phase single-stage power-factor-corrected converter topologies,” *IEEE Trans. Ind. Electron.* , vol. 52, no. 1, pp. 23-35, Feb. 2005.

[18] V. Vlatkovic, D. Borojevic, and F. C. Lee, “Input filter design for power factor correction circuits,” *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 199–205, Jan. 1996.

[19] J. Sun, “Input impedance analysis of single-phase PFC converters,” *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 308–314, Mar. 2005.

[20] Q. Zhao, M. Xu, F. C. Lee, and J. Qian, “Single-switch parallel power factor correction ac-dc converters with inherent load current feedback,” *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 928–936, Jul. 2004.

[21] S. Luo, W. Qui, W. Wu, and I. Batarseh, “Flyboost power factor correction cell and a new family of single-stage ac/dc converters,” *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 25–34, Jan. 2005.

[22] D. D. C. Lu, H. H. C. Iu, and V. Pjevalica, “A single-stage ac/dc converter with high power factor, regulated bus voltage, and output voltage,” *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 218–228, Jan. 2008.

[23] R. T. Chen, Y. Y. Chen, and Y. R. Yang, “Single-stage asymmetrical half-bridge regulator with ripple reduction technique,” *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1358–1369, May 2008.

[24] L. H. Dixon, Jr., “High power factor preregulator for off-line power supplies,” in *Unitrode Switching Regulated Power Supply Design Manual*. Merrimack, NH: Unitrode Corp., 1990.

[25] M. J. Willers, M. G. Egan, J. M. D. Murphy, and S. Daly, “A BIFRED converter with a wide load range,” in *Proc. IEEE IECON’94*, Bologna, Italy, 1994, pp. 226-231.

[26] C. Qian and K. M. Smedley, “A topology survey of single-stage power factor corrector with a boost type input-current shaper,” *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 360-368, May 2001.

[27] O. Garcia, P. Alou, J.A. Oliver, J.A. Cobos, J. Uceda, and S. Ollero, “AC/DC converters with tight output voltage regulation and with a single control loop,” in *Proc. APEC’99*, Dallas, Texas, 1999, pp. 1098 -1104.

[28] Y. Panov and M. M. Jovanovic, “Small signal analysis and control design of isolated power supplies with optocoupler feedback,” *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 823-832, Jul. 2005.

[29] V. J. Thottuvelil, D. Chin, and G. Verghese, “Hierarchical approaches to modeling high-power-factor AC-DC converters,” *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 179–187, Apr. 1991.

[30] J. Y. Choi and B. H. Cho, “Small-signal modeling of single-phase power-factor correcting AC/DC converters: a unified approach,” in *Proc. PESC’98*, 1998, pp. 1351-1357.

[31] R. B. Ridley, “Frequency response measurements for switching power supplies,” Unitrode Power Supply Design Seminar, pp. A1-A12, 1999.

[32] A. Lazaro, A. Barrado, J. Pleite, J. Vazquez and E. Olias, “New approach of average modeling and control for AC/DC power supplies which operates with variable duty cycle,” in *Proc. PESC’04*, 2004, pp. 652-658.

[33] K. Rustom, W. Qiu, C. Iannello, and I. Batarseh, “Five-terminal switched transformer average modeling and AC analysis of PFC converters,” *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2352-2362, Nov. 2007.

[34] H. Y. Li, H. C. Chen and L. K. Chang, “Analysis and design of a single stage parallel AC-to-DC converter,” *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 2989-3002, Dec. 2009.

[35] T. H. Chen, W. L. Lin and C. M. Liaw, “Dynamic modeling and controller design of flyback converter,” *IEEE Trans. Aerospace and Electronic Systems*, vol. 35, no. 4, pp. 1230–1239, Oct. 1999.

[36] R. B. Ridley, “A new continuous-time model for current-mode control,” *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271-280, Apr. 1991.

[37] R. B. Ridley, “A new continuous-time model for current-mode control with constant frequency, constant on-time, and constant off-time, in CCM and DCM,” in *Proc. PESC’90*, San Antonio, TX, 1990, pp. 382-389.