國立交通大學

電子工程學系電子研究所

博士論文

鎳矽化物應用在奈米金氧半導體元件技術之研究

Investigation of Nickel Silicide Application toward Nano-Scale MOS Device Technology

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摘要

在先進互補式金氧半導體元件裡，當接觸尺寸縮小至奈米等級，源極及汲極的接觸電阻也會隨之增加。因此，金屬矽化物的技術應用在源極及汲極已經被開發用來同時降低接觸電阻及接面寄生電阻。在奈米金氧半場效電晶體的製造中，矽化製程是必須的，為了抑制源極及汲極的超淺接面形成所產生的短通道效應。所以，是否具有與矽基材完好介面特性的金屬矽化物，是在製造奈米尺寸的元件時重要的製程考量。除此之外，當閘極氧化層隨著元件尺寸縮小而縮小時，閘極金屬矽化的製程，是否會對閘極氧化層可靠度造成影響也是一個需要考量的因素。

在本論文中，主要研究的方向是，鎳矽化物與超淺接面製程、完全閘極金屬矽化製程整合的可靠度研究。首先，我們對鋯覆蓋在鎳上後形成的金屬矽化物的熱穩定性作一系列的研究。藉由鋯在金屬矽化過程中，抑制氧摻雜的能力，鎳矽化物的熱穩定性將能大大的改善。並且由穿隧式電子顯微鏡的觀測，這種方法能獲得一個平緩的矽化物與矽的介面。

然後，我們將蓋有鋯的鎳堆疊在二極體接面後形成鎳矽化物，研究用鋯覆蓋的方法對鎳矽化接面特性的影響，並與傳統用鈦覆蓋的方法作一個比較。由於熱穩定性上的改善，經由金屬矽化過程所造成的接面漏電增加，果然如預期的被抑

制。並由於矽化物深度良好控制的優點，鎳矽化物形成在 30 奈米深的超淺接面上也如預期般的被實現了。

再者，我們對利用 PH$_3$ 電漿摻雜方式所形成的超淺接面，作一個探討。雖然表面雜質濃度低的缺點，能藉由一個覆蓋層來改善，但同時也造成了接面深度的增加。在我們的實驗中，我們發現，在 PH3 電漿摻雜後，透過短時間的退火的方式，能形成一個較少缺陷的超淺接面。

最後，我們去觀察在鎳矽化物形成在不同閘極結構上的特性。經於磷的摻雜，能增加閘極氧化層的可靠度。因此，我們相信，對於應用在未來元件製作上，完全鎳矽化閘極仍具有潛力。

Investigation of Nickel Silicide Application toward Nano-Scale MOS Device Technology

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Abstract

In advanced CMOS devices, as contact dimensions scale down to nanometer range, contact resistance of source and drain is increased correspondingly. As a result, the technique of metal silicides for poly gate and source/drain has been developed to reduce the contact resistance and the parasitic junction resistance as well. In nanometer MOSFET fabrication, this silicidation process requires considering to suppress short channel effect (SCE) when forming the ultra shallow source and drain junction. Therefore, metal silicides owning a perfect interfacial property with Si above an ultra-shallow junction is considered as a critical module toward the realization of nano-scale CMOS. Besides, as the oxide thickness scaling down with the device dimensions, the gate oxide reliability will also be a concern for the silicided gate process.

The objective of this dissertation is to investigate the feasibility of nickel silicide integration into the formation process of the ultra shallow junction and full silicide

gate. First of all, we have investigated the thermal stability of nickel silicide with Zr capping. To employ its good capability for the suppression of oxygen incorporation during silicidation process, a siginificantly improvement on the thermal stability of nickel silicide can be obtained. And a smooth interface between silicide and silicon also can be demonstrated by TEM images.

Then, we combined the Zr capped on nickel silicide with the p^+/n junction, and investigated the influence on junction charateristics by this capping layer compared with a conventional Ti-capped method. Due to the advantages of improvement on thermal stability, the increase of leakage current resulted from the silicidation process can be suppressed as expected. By the advantage of well-controlled silicide depth, an 30nm ultra shallow junction with nickel silicide was also accomplished as expected.

Third, the formation of ultra shallow junction by PH_3 plasma doped method was investigated. Its low surface concentration can be improved by a cap layer but meanwhile it will result in the increase of junction depth. In our experimental, a defect less ultra shallow junction formation by PH_3 plasma doped can be achieved by short activation time.

Finally, we have observed the behavior of nickel silicide gate based on different gate structures. By phosphorus incorporation, the gate oxide reliability can be enhanced. Thus, we believed that full nickel silicide gate still possesses potential for the application on future device fabrication.

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願將此論文獻給所有關心我的人。

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Chapter 1

Introduction

1.1 General Background

Silicon technology has been main basis of microelectronics and electronics systems for more than thirty years [1]. The performance and density of MOSFET integrated circuits are improved due to not only the progress in lithography but also the innovation in device fabrication technology. However, as device dimensions continue to be scaled down following the "Moore's law", the resistance of the polycrystal-line increases with the scaling factor. In addition, the increase of contact resistance is by the square of the factor. Those degradation due to the increase of parasitic resistance will give rise to excessive RC time delay and undesired voltage drop which may offset the advantages coming from the scaling technology or even deteriorate the performance of devices [2].

Over the years, many efforts have been made for reducing the parasitic resistance resulting from the device shrinking. Since 1966, metal silicides have been considerated for its advantages of low resistance and schottky contacts [3]. In 1979, the idea of metal silicides on the doped polysilicon for high-conductivity interconnect was proposed and adopted at once in industry [4]. Presently, this concept was extended into the diffusion region by the development of self-aligned silicide technology at both poly-gate and source/drain diffusion region [5]. Now, the silicide-related technologies become integral module for the realization of nano-scale MOS devices.

The major advantages of metal silicides can be grouped as follows : (1) their low resistivity for gate and interconnect applications, (2) easy formation by self-aligned technology without any extra mask and compatible with conventional CMOS process, (3) silicides on S/D region can somewhat ease the problem of Al spiking. However, the main issue induced by silicides is the degradation on device reliability including the increase of junction leakage and the descent of oxide breakdown field [6, 7]. Thus, study on metal silicides process is essential for integration into the device fabrication processes.

For titanium silicide ($TiSi_2$), it has been widely used in the IC industry due to its low sheet resistance (13-15$\Omega/\square$) and high thermal stability. However, it has been found that the sheet resistance of $TiSi_2$ applied on poly-Si line will increase significantly as the line width scaled to the deep-submicron range (~0.2μm), i.e. the narrow line width effects. The increase in sheet resistance of narrow $TiSi_2$ poly-Si line has been explained [8,9] in terms of the difficulty of the phase transformation from the high-resistance phase (C49-$TiSi_2$ ~ 60-80$\Omega/\square$) to the low-resistance phase (C54- $TiSi_2$). Because the C54 structure features a large grain size (~0.2μm) compared with C49 structure [8-10]. Besides, the Ti diffusion will degrade the oxide reliability by trap generation even the silicidation temperature as low as 400^{o}C [11].

Recently, $CoSi_2$ is mostly used to be the alternative to $TiSi_2$ due to its line-width independence characteristics [8]. In addition, th cobalt silicide has other advantages such as the less film stress by its better lattice match than $TiSi_2$, better stability in presence of dopants and better resistance against plasma-etch [12]. However, its rough interface of silicide/Si and the relatively large Si consumption will restrict its application on poly-gate and on shallow junction due to the degradation on oxide reliability and the increase of junction leakage [13, 14].

Toward nano-scale device fabrication, NiSi is regarded as a potential candidate to replace TiSi2 and CoSi2. First, The sheet resistance of NiSi is comparable with that of $TiSi_2$ and $CoSi_2$. Another advantage of NiSi is its much more insensitive to the narrow line-width than $TiSi_2$ and $CoSi_2$. Besides, nickel silicide possesses the merits of lower formation temperature, less silicon consumption, only one annealing step, and relatively small film-stress compared with the other two silicides [15]. However, the major shortage for NiSi is its poor thermal stability. The appropriate improvement on thermal stability of NiSi will contribute to the integration into nano MOS device fabrication processes.

1.2Motivation

Although NiSi has many advantages as mentioned, its poor thermal stability due to the formation of precipitates and NiSi2 will result in the degradation on device performance and reliability such as the increase of junction leakage. Thus, several efforts have been made for the improvement of its thermal charateristics.

Nitrogen ion implantation into the Si Substract prior to the deposition of Ni was reported to minimize the agglomeration of silicide and to widen the window of silicide processing temperature. By the incorporation of nitrogen in Ni films, the roughness of the silicide/Si interface can be retarded [16] which leads to the improvement on the thermal stability of NiSi [16, 17]. However, it will sacrifice the sheet resistance for better thermal stability of NiSi.

Ti and TiN capping layer were introduced to reduce the junction leakage and enhance the thermal stability of NiSi by gettering oxygen and preventing the diffusion of oxygen, respectively [16, 18]. However, Ti may interdiffuse through Ni and form the $TiSi_2$ or Ti_xN_ySi. That will result in the increase of sheet resistance [19].

Furthermore, the insertion of a thin Pt layer and the addition of some amount of Pt was proposed to improve the thermal stability of NiSi due to the change in intrinsic quality [20].

In our experimental, we proposed a Zr cap on the Ni film to getter oxygen, which originated from the annealing ambient, the Ni-deposition chamber or interfacial oxide at metal/silion interface, because of the lower binding energy of Zr and O than that of Ti and O, and the better thermal stability of ZrSi. In order to integrate NiSi into the nano-scale device fabrication, NiSi is formed on 30nm ultra shallow junction, and is investigated for junction characteristics. Finally, full nickel silicide gate was accomplished and studied for future nano-device technology application.

1.3 Organization of the Thesis

There are seven chapters in this dissertation. Chapter 1 shows the overview of the metal silicides. Motivation for the thesis is also described.

In chapter 2, the thermal stability of nickel silicide with a Zr cap layer are investigated. The improvement on thermal stability of NiSi by Zr capping compared with conventional Ti capping was proved in terms of Rs(sheet resistance), TEM and XRD.

In chapter 3, the nickel silicided junction with/with capping was studied for its basic IV characteristics and the temperature effects. Not only the thermal stability improvement but also the suppression of junction leakage can be attributed to the Zr cap layer.

In chapter 4, the charateristics and feasibility of nickel silicide applied on 30nm ultra-shallow junction were investigated. And the reverse junction leakage current density vs. periphery to area ratio (P/A ration) is also dicussed.

In chapter 5, PH_3 plasma doped method for ultra shallow junction formation was studied. Different dopant activation methods and conditions were performed included excimer laser annealing. Finally, a few defect ultra-shallow junction below 30nm can be achieved by short time annealing.

In chapter 6, full nickel silicide gate based on different gate structures is studied. The influence by nickel silicide on gate oxide is also examined in terms of J_g, V_{FB} , E_{bd} and electron barrier height. The Zr cap layer is also integrated with full nickel silicide gate to enhance the oxide reliability.

Finally, in chapter 7, the conclusions are made and the recommendation describes the topics which could be further researched.

Chapter 2

Characteristics of Nickel Silicide Combined with a Zirconium Cap Layer

2.1 Introduction

The silicide and self-aligned silicide (salicide) process have been widely applied to VLSI MOS devices for lowering their gate and source/drain resistances and increasing their driving current [1], [2]. Currently, the most commonly used silicides (salicides) are TiSi_2, CoSi_2, and NiSi. For TiSi_2, the transformation from the metastable high resistivity C49 phase to the thermodynamically stable low resistivity C54 phase is nucleation limited, causing linewidth dependence of the sheet resistance for lines narrower than 0.35μm [3], [4]. Although CoSi_2 was used without the disadvantage, its high Si consumption and junction spiking limited its applications to deep submicron devices [2]. However, NiSi, without the above drawbacks, has been shown to be a suitable silicide material for the future ultra-shallow junction devices since it has the advantages of the lowest resistivity (~15μΩ-cm), near zero resistivity degradation on narrow lines/gates, and it only needs one single annealing step [5]. However, for NiSi it was reported that agglomeration takes place at a temperature as low as 600˚C and its phase transformation from NiSi to NiSi_2 occurs at a temperature above 750˚C [2], [6]. That will degrade the performance of devices and give rise to some reliability issues. Recently, much study had shown that, during silicidation, NiSi is extremely sensitive to oxygen contamination which could be suppressed by adding a capping layer [4]. In this letter, Zr is proposed to be the capping layer as a barrier to oxygen during formation of the NiSi and it is demonstrated that the occurrence of agglomeration is delayed and a high quality single phase NiSi, which can sustain annealing at a temperature as high as 850˚C, is obtained.

2.2 Experimental

Samples were fabricated on both n-type and p-type (100) oriented Si wafers. After a standard RCA cleaning process, the samples were loaded into a dual electron-gun evaporation system. A 10-nm and 30-nm-thick Ni film was first deposited on the silicon substrate as two groups. Following, a 5-nm and 10-nm-thick Zr was then deposited onto the Ni layer at a base pressure of 1×10^{-6} torr with a deposition rate of 1 Å/s. For comparison, Ti was deposited in the same condition to prepare the Ti-capped samples for comparison. After that, all samples were annealed in a RTA system from 500-850ºC in N_2 ambient to form the silicide. After the RTA treatment, the un-reacted metal was removed by wet etching (SC1 for the Zr cap layer reacted with oxygen and $H_2SO_4+H_2O_2$ for unremoved Ni). Samples were examined for sheet resistance with a four-point probe, microstructure with a TEM and phase formation with a X-ray diffratometry (XRD) at an incident angle of 0.5º.

2.3 Results and Discussion

2.3.1 Sheet Rsistance of Nickel Silicide on n-type Si/p-type Si

In Table 2.1, three different groups of samples were designated as group1: Ni/Si, group2: Ti/Ni/Si, and group3: Zr/Ni/Si, where the first two groups are for comparison. Phase formation of NiSi was studied for the temperature of RTA ranging from 500ºC to 850ºC. Fig. 2.1s shows sheet resistance values of samples of group1, 2, and 3 with different nickel thickness and different Si-substract type in various silicidation temperature, respectively. In these figures, the degradation of the sheet resistances of group1 was due to agglomeration and phase transformation of NiSi at the high annealing temperature as reported in Ref. 7. However, comparing with group1, groups 2 and 3 exhibited a significant improvement in sheet resistance due to a capping layer, which suppressed the oxidation of silicide films [4], [8]. Especially, for group 3 samples, sheet resistances still remained low even after the annealing temperature reached 850ºC. This indicates that Zr has a stronger capping ability in NiSi. It may not only be more effective in preventing oxidation of NiSi from the ambient, but also in suppressing the agglomeration phenomenon and interfacial oxide formation at the NiSi/Si interface [4]. The another possible reason for the improvement on thermal stability is that Zr will react with Ni to form an amorphorus-like barrier layer for suppression the excess Ni diffusion, which may result in the formation of agglomeration or precipitates.

2.3.2 TEM Images for Zr capped on Nickel Silicide

Fig. 2.2 is the Transmission electron microscopy (TEM) image for as-deposited nickel film. In this figure, an uniform nickel film can be obtained by dual electron gun system, and the as-deposited nickel film exhibits a bambo structure. However, an undesired native oxide at interface between as-deposited nickel and Si is found even though the surrounding of deposition system is about 1×10^{-6} torr. It would result in the degradation of nickel silicide on its thermal properties. The cross-section views of samples without and with capping after silicidation at 650°C and 850°C are shown in fig. 2.3s. It is seen that no agglomeration and $NiSi_2$ precipitates exist in without capping Ni sample and with Ti capping or Zr capping Ni samples which were annealed at 650ºC (Fig. 2.3(a), (c) and (e)). However, for the samples annealed at 850°C (Fig. 2.3(b), (d) and (f)), the sample without capping and the sample with Ti capping had agglomeration and $NiSi_2$ precipitates appeared at the silicide region while the samples which had a Zr capping did not show any formation of agglomeration or precipitates and had a smooth interface and well-controlled silicide region of uniform depth. This indicates that the Zr film has a better capping ability for NiSi. It can not only prevent nickel silicide from oxidizing in the annealing system, but also suppress the agglomeration and retard the formation of $NiSi_2$ precipitates [10].

2.3.3 XRD Analysis for Zr capped on Nickel Silicide

Fig. 2.4(a) and (b) show the XRD spectra of group2 and group3 samples annealed at 650ºC and 850ºC, respectively. For both groups of samples, NiSi was the dominant phase at the annealing temperature of 650ºC. However, for the high annealing temperature of 850ºC, $NiSi_2$ that is located of about 28º [9] occurred in the group 2 samples, but for the group 3 samples in Fig. 3(b), only the NiSi phase is identified. This further strengthens the results of Fig. 2.1 and 2.3, that is, Zr capping in the Ni silicide system is more effective in preventing oxidation from the ambient, and in retarding agglomeration and $NiSi_2$ formation, resulting in a more stable low contact resistance system.

2.4 Summary

In summary, in this chapter, we have proposed and demonstrated a new nickel silicide process by using Zr, instead of the conventional Ti, as the capping layer to obtain a nickel silicide of an excellent thermal stability which can sustain a heat treatment as high to 850ºC. Experimental results has shown that, even after such a high temperature treatment, the nickel silicide obtained by this process still retained its NiSi phase, thus maintaining an excellent interface between silicide and silicon. This is achieved mainly by the good capping capability of thin Zr layer in retarding oxygen during the high temperature silicidation process.

Due to the well-controlled metallurgical structure of the formed silicide, the formation of low-leak shallow junction for the deep sub-micron MOSFET devices can be achieved.

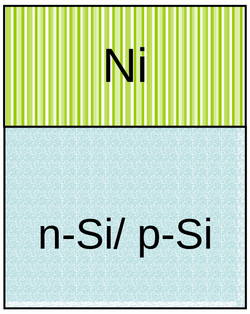
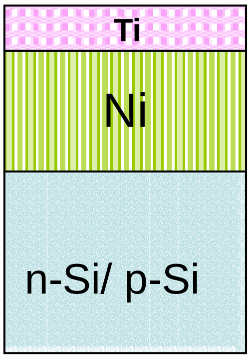
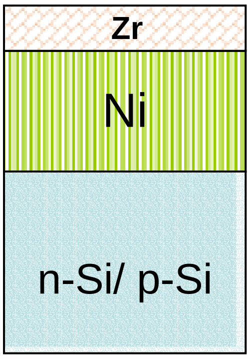
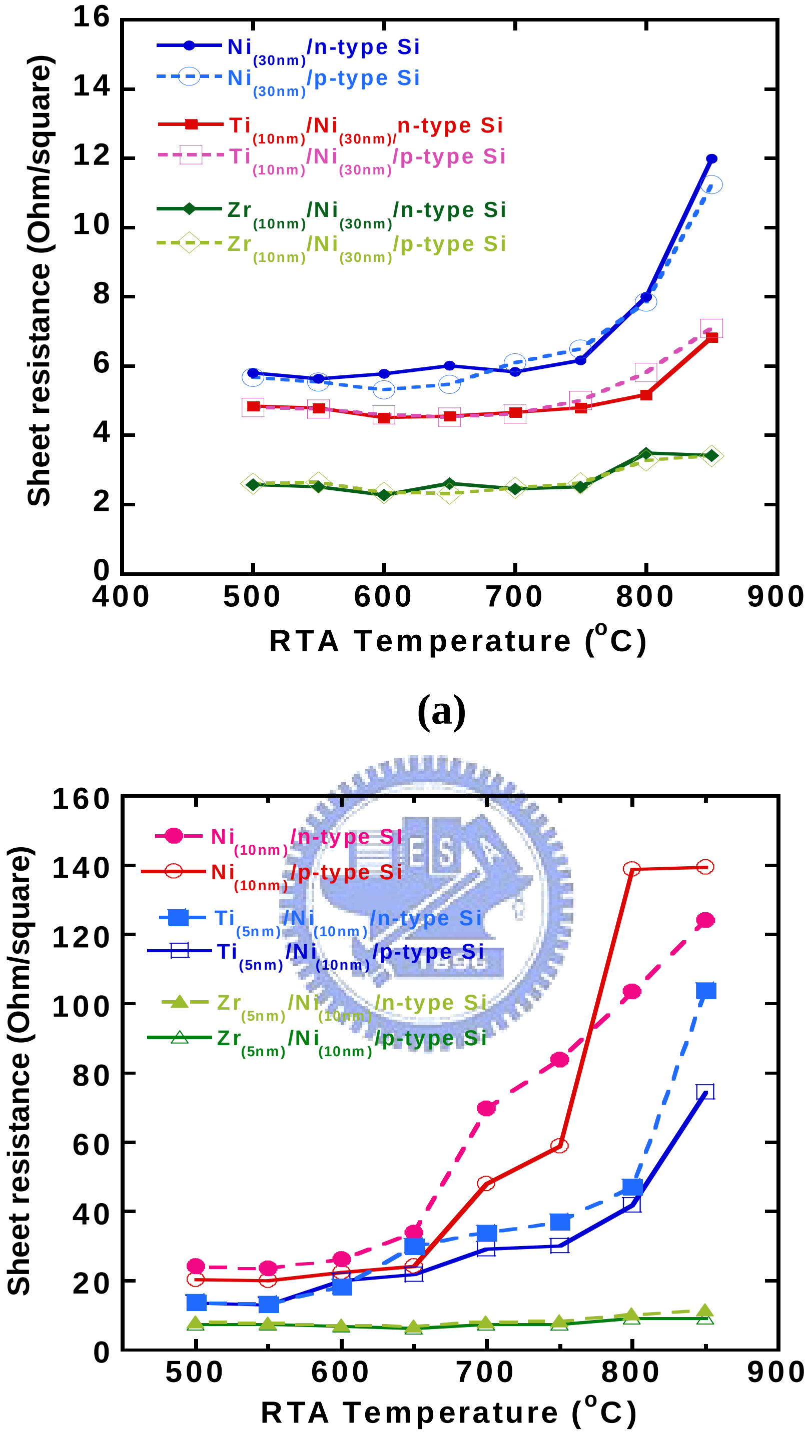
Sample	Group I	Group II	Group III
Structure	Nickel : 10nm / 30nm	Titanium : 5nm / 10nm Nickel : 10nm / 30nm	Zirconium : 5nm / 10nm Nickel : 10nm / 30nm
			

Table 2.1 Three different groups of samples were designed as : groupI : Ni/Si、groupII : Ti/Ni/Si、groupIII : Zr/Ni/Si. Ni film is 10nm and 30nm, respectively and the capping layer is 5nm and 10nm, respectively on both n-type and p-type Si.



(a)

(b)

Fig. 2.1 Sheet resistance of nickel silicide with and without capping. (a) nickel thickness is 30nm and the capping layer is 10nm. (b) nickel thickness is 10nm and the capping layer is 5nm.

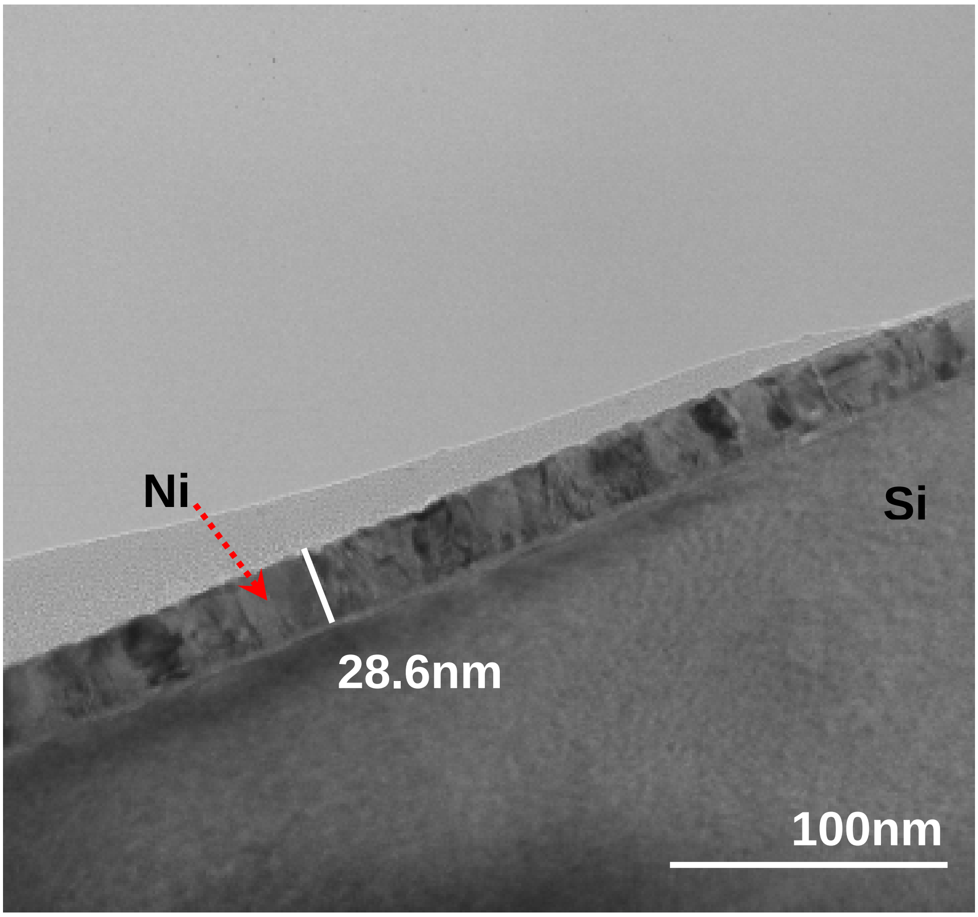
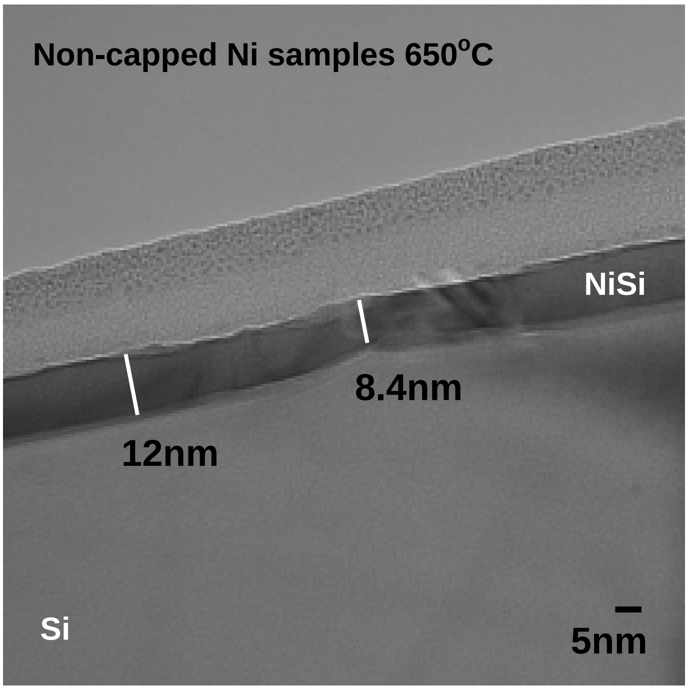
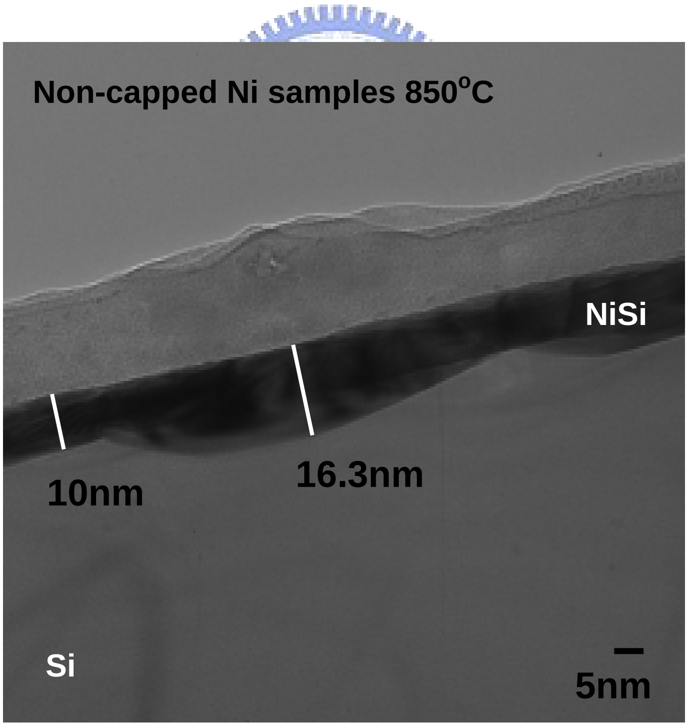


Fig. 2.2 Transmission electron microscopy (TEM) image of the as-deposited nickel film.

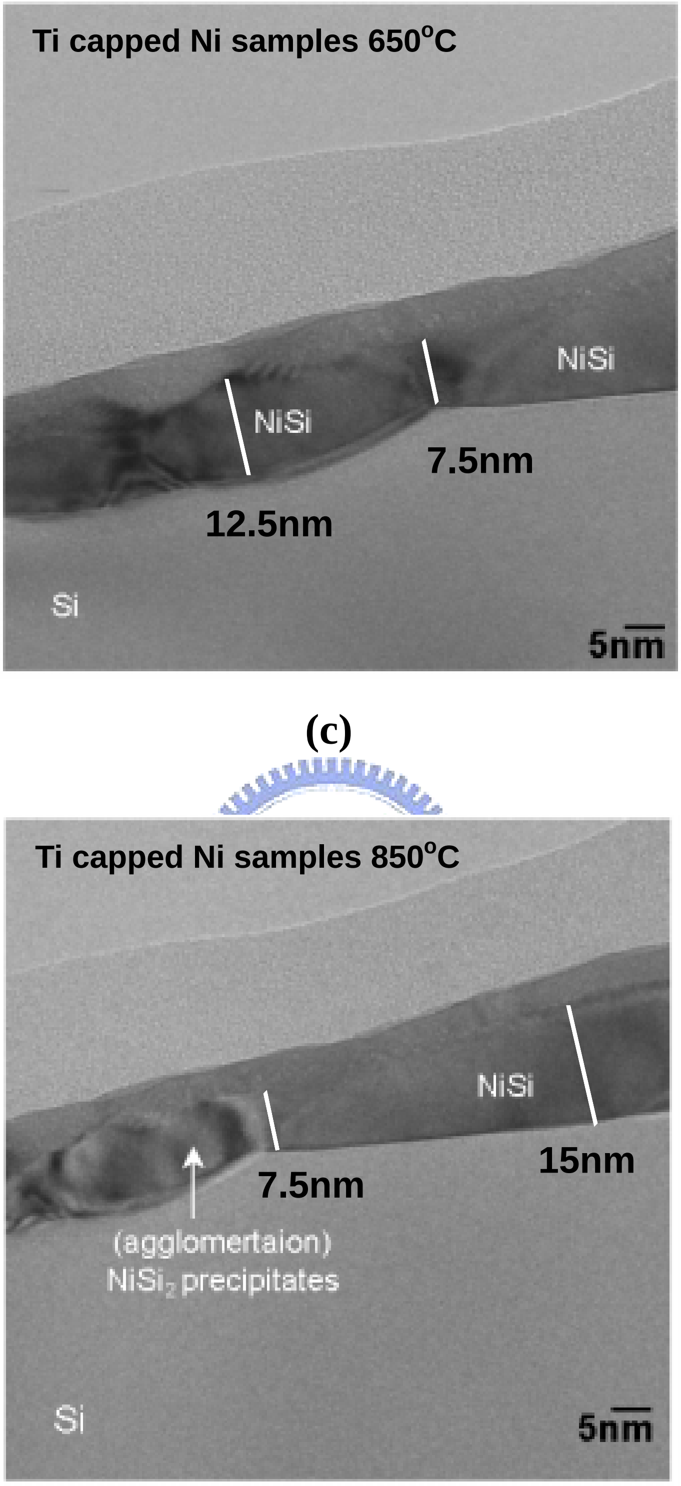


(a)



(b)

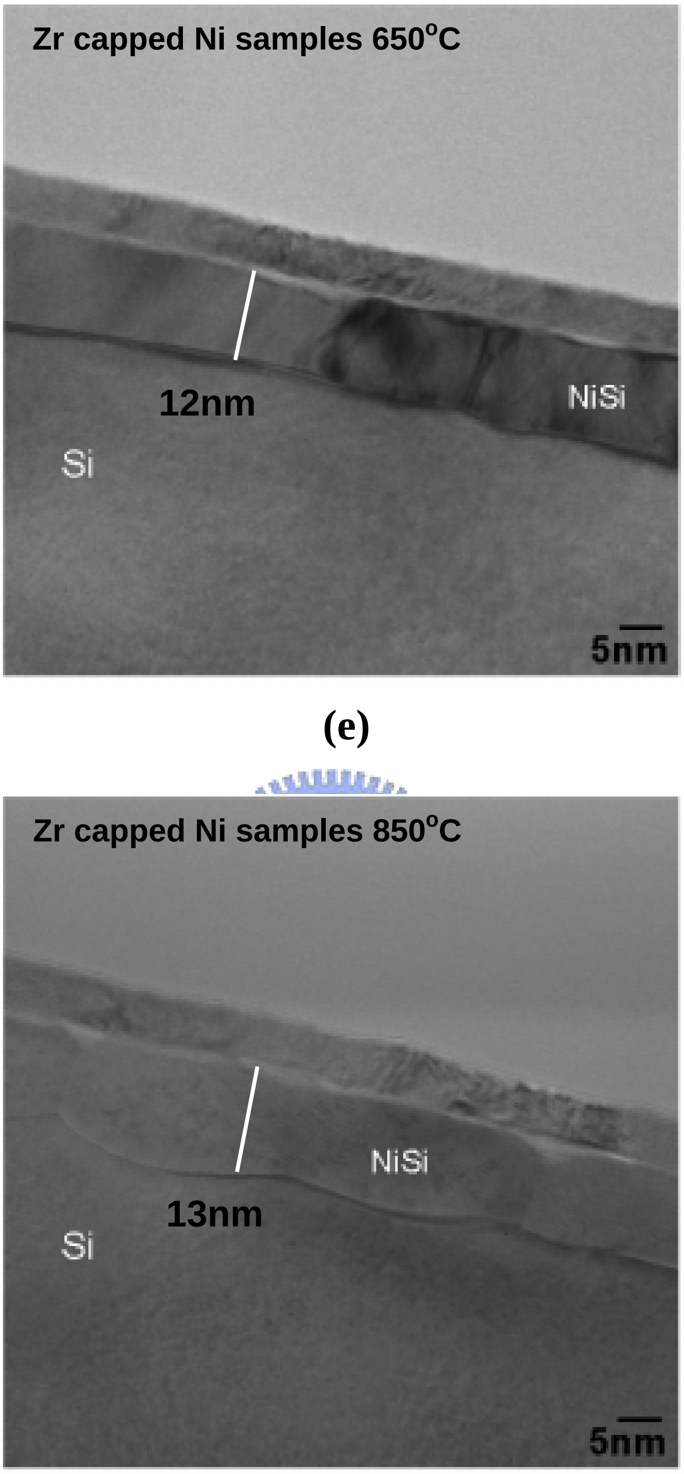
Fig.2.3 Transmission electron microscopy (TEM) images of nickel silicide. (a) non-capped Ni samples after RTA at 650ºC. (b) non-capped Ni samples after RTA at 850ºC.



(c)

(d)

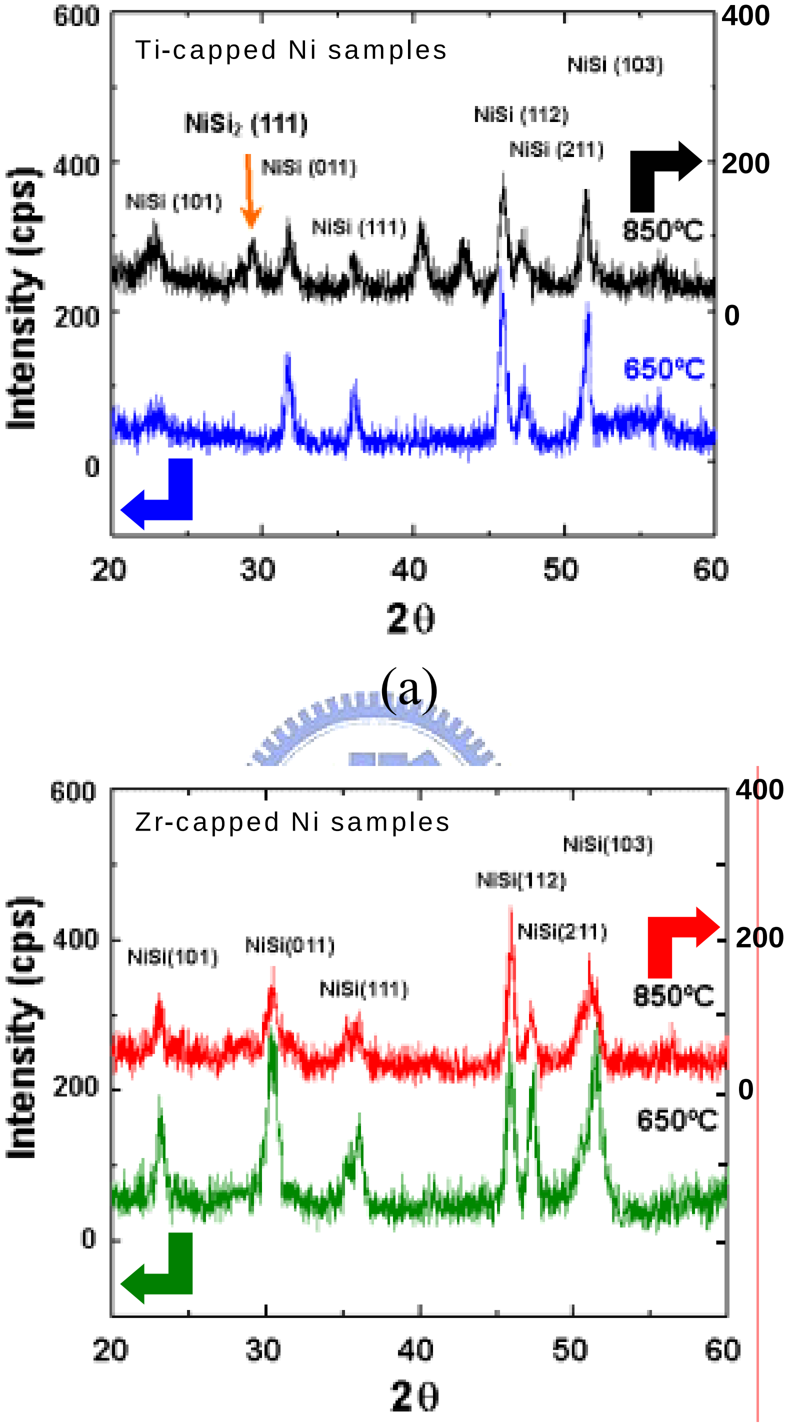
Fig.2.3 Transmission electron microscopy (TEM) images of nickel silicide. (c) Ti capped Ni samples after RTA at 650ºC. (d) Ti capped Ni samples after RTA at 850ºC.



(e)

(f)

Fig.2.3 Transmission electron microscopy (TEM) images of nickel silicide. (e) Zr capped Ni samples after RTA at 650ºC. (f) Zr capped Ni samples after RTA at 850ºC.



(a)

(b)

Fig. 2.4 X-ray diffraction spectra (XRD) of (a) Ti/Ni/Si and (b) Zr/Ni/Si contact systems after annealing at 650ºC and 850ºC respectively.

Chapter 3

Characteristics of Nickel Silicide on P^+/N Junction Combined with a Zirconium Cap Layer

3.1 Introduction

Si integrated circuit (IC) industry has followed a steady path of constantly shrinking device dimensions to achieve a dense and higher-speed chip. In advanced CMOS devices, as contact dimensions scale down to nanometer range, contact resistance of source and drain is increased correspondingly. Moreover, such resistance deterioration is mainly encountered in local interconnect through poly-line connection. As a result, the technique of simultaneous metal silicides for poly gate and source/drain has been developed to reduce the contact resistance and the parasitic junction resistance as well [1]. In nanometer MOSFET fabrication, this silicidation process requires considering to suppress short channel effect (SCE) when forming the ultra shallow source and drain junction. Therefore, metal silicides owning a perfect interfacial property with Si above an ultra-shallow junction is considered as a critical module toward the realization of nano-scale CMOS.

Currently, the most widely used metal silicides include $TiSi_2$, $CoSi_2$, and NiSi. For $TiSi_2$, athough it possesses good thermal stability, extremely high silicidation temperature is still required for its phase transformation (from a high-resistivity C49 phase to a low-resistivity C54 phase). This limits its application for the ultra-shallow junction formation [2-7]. Furthermore, its restricted grain size results in a poor series-resistance for the line-width below 350nm [8], [9]. For this reason, Ti is replaced by Co since the cobalt silicide has a negligible line-width effect for 0.1um CMOS technology [7], [22-24]. However, for cobalt silicide, non-uniform $CoSi_2$/Si interface or Co spike will lead to the increase of junction leakage [10], [11], [24]. Hence, for ultra-shallow junction, nickel silicide is considered since it consumes less silicon atoms than does cobalt silicide. Furthermore, an additional benefit of nickel silicide is that it has a relatively small film-stress [12] and requires only one annealing step. Although nickel silicide possesses so many advantages, its poor thermal stability must be improved in CMOS process application [13], [14]. Also recent studies of nickel silicide have shown that the formation of NiSi is extremely sensitive to interfacial native oxide on the silicon surface or oxygen contamination during the silicidation process [9], [15-18].

In this chapter, we propose a Zr capping process for forming nickel silicide. This Zr cap layer can effectively reduce the oxygen contamination during formation of nickel silicide and improve its thermal stability, hence making its application to nano-meter CMOS VLSI more practicable.

3.2 Experimental

Fig.3.1 shows the process flow for samples fabricated for our experiments. Firstly, after the standard RCA cleaning process, a 500nm-thick field oxide was formed on the surface of the n-type (100) oriented, 3-5 Ω-cm, Si wafer at 1050°C. Next, active regions were defined by photolithography and wet etching. Then a 20nm-thick sacrificial oxide was deposited by PECVD to avoid the damage from the implantation followed by a 5×10^{15} cm^{-2}, 40keV BF_2 implant. After that, rapid thermal annealing (RTA) at 950°C for 30s was performed to activate the implanted dopants. Then, samples were loaded into a dual electron-beam evaporation system after a dilute HF dip. A 10nm-thick nickel thin film was first deposited onto the p^+/n junction at a base pressure of 1×10^{-6} torr at a deposition rate of 1Å/s. Immediately, a titanium or zirconium film of about 5nm was sputtered onto the nickel layer respectively as the capping layer. After this step of metal deposition, the silicidation procedure was carried out by the rapid thermal annealing process at various temperatures from 500°C to 850°C in N_2 ambient. Then wafers were wet etched to remove the un-reacted metal. A thin TiN of about 25nm was then deposited as a barrier layer and, finally aluminum was deposited on both the front and backside to serve as contact electrodes.

Table 3.1 shows the four different groups of samples that were fabricated in the above process for this experiment. In the table, samples in group I, which were for reference, were just the simple p^+/n junction. The other samles are nickel silicided junctions. Among those nickel silicided samples, the first group of samples was without any capping layer, the second group of samples was with Ti capping layer, and the third group of samples was with the Zr capping layer.

3.3 Results and Discussion

3.3.1 SIMS Analysis for Nickel Silicided Junction with / without a Cap Layer

Fig. 3.2a shows the SIMS boron profiles before and after the silicidation process of 850ºC. Boron redistribution in the bulk region at this silicidation temperature is small. Nevertheless, boron atoms are pushed out from the silicide region [21], [22]. Fig. 3.2b shows the SIMS nickel profiles of Ni without cap samples, Ti capped Ni samples, and Zr capped Ni samples respectively. It can be seen that, for Ti and Zr capped Ni samples, which had a capping layer, diffusion of nickel atoms were retarded and stayed to form a shallower silicided region by the capping layer and this is especially evident for the samples which used Zr as the capping layer. Recent studies [16] [19] showed that oxygen contamination in silicides generate oxygen-related defects which enhance the nucleation or $NiSi_2$ precipitate formation [16]. Fig 3.2c shows the oxygen profiles of the same groups I, II, and IV samples. These profiles also indicate that the capping layers indeed prevented oxygen from diffusing into the samples since the un-capped sample had the highest oxygen concentration both at the surface and in the silicon and the Zr capping layer had the strongest capping capability.

3.3.2 Basic IV Charateristics of P^+/N Nickel-Silicided Junction

The reverse leakage current of the silicided junction of samples were measured to further study the capping effect on retarding the nickel penetrating the junction region. Fig. 3.3 shows the J-V characteristic of the un-silicided and nickel silicided p^+/n junctions with and without a capping layer and Fig. 3.4a, b and c exhibit the Weibull plots of the samples without capping, with Ti capped and Zr capped, respectively for different silicidation conditions. According to the above two figures, the sample with the Zr-cap layer had the smallest leakage current. In all groups, samples had the smallest leakage level at RTA condition of 650ºC. Fig. 3.5a and b are Weibull plots of the reverse currents measured at –3 V for three groups at RTA 650ºC and 850ºC, respectively. From these plots, we find that the samples with the Zr capping layer had the best and most uniform reverse junction leakage, less than 1 x 10^{-8} A/cm^2 even at the annealed temperature up to 850 ^{o}C.

It is known that the leakage current (J_r) in p-n junction is composed of two components, i.e., the junction area leakage (J_{ra}) and junction periphery leakage (J_{rp}). Fig. 3.6a, b and c are plots of the leakage current density versus the ratio of junction periphery and area for the Ni without cap samples, Ti capped Ni samples and Zr capped Ni samples. The smallest periphery and area leakage can be observed at the annealing temperature of 650ºC in all samples. Effects of capping conditions on junction leakage from periphery and area are also shown in Fig. 3.7. The leakage level by junction area for Zr capped Ni samples is almost independent on RTA temperature, but the leakage level in the other groups shows strong silicidation-temperature dependence (Fig. 3.7a). From Fig. 3.7b, it should be emphasized that junction periphery leakage is almost independent on RTA temperature by using a capping layer, particularly for samples with a Zr thin film.

3.3.3 Temperature Effects of P^+/N Nickel-Silicided Junction

Fig. 3.8-3.10 show the reverse current voltage characteristics of nickel-silicided junction without capping and with Ti capping or Zr capping, respectively at various temperature. The reverse current is constructed from the generation current (I_{gen}) and diffusion current (I_{diff}). The current equations of these two components are as follows :

$$I_{gen} = \frac{1}{2} qA \frac{n_i}{\tau} W \propto T^{\frac{2}{3}} e^{\frac{-Eg}{2kT}} \text{---}(1)$$

$$I_{diff} = qAD \frac{n_i^{\,2}}{N_b \times L_d} \propto T^3 e^{\frac{-Eg}{kT}} \text{---}(2)$$

(I_{gen} is voltage dependent and I_{diff} is voltage independent.)

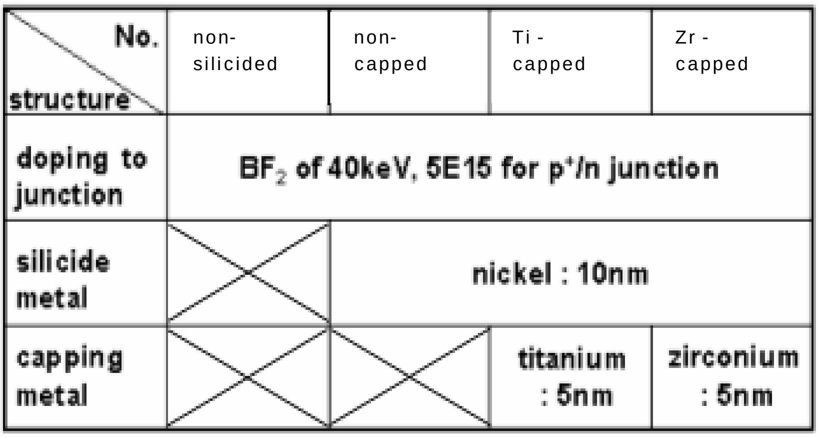
Fig. 3.11a, b and c are Arrhenius plots for reverse leakage of nickel silicided junction measured at various voltages. The Arrhenius plot for leakage current exhibits activation energy (Ea) of 1.12eV (Eg) when diffusion current is the dominant component of leakage current. Fig. 3.11a, b and c indicated the Ea of non-capped, Ti capped and Zr capped Ni samples, respectively. It can be found that Ea of all nickel silicided junction with RTA condition at 650°C approximates 1.12eV. However, Ea of the samples without capping with silicidation temperature at 850°C will decrease and the Zr cap layer can suppress the degradation of Ea more effectively than the Ti cap layer. Hence, with the results of all the above both physical and electrical analyses, it can be concluded that the Zr capping layer exhibited the most effective capping capability in maintaining the metallurgical as well as electrical properties of the Ni silicide system.

3.4 Summary

In conclusion, in this chapter, we have proposed and demonstrated a new nickel silicide process with junction formation by using Zr, instead of the conventional Ti, as the capping layer to obtain low leakage current, less voltage and temperature dependence by effectively retarding oxygen during the high temperature silicidation process. Combined with the advantages of Zr capped nickel silicide from Chapter 2, such as NiSi phase conservation, an excellent interface between silicide and silicon after a high treatment temperature, the ultra shallow junction can be preserved to obtain a low reverse junction leakage for the deep sub-micron MOSFET devices.

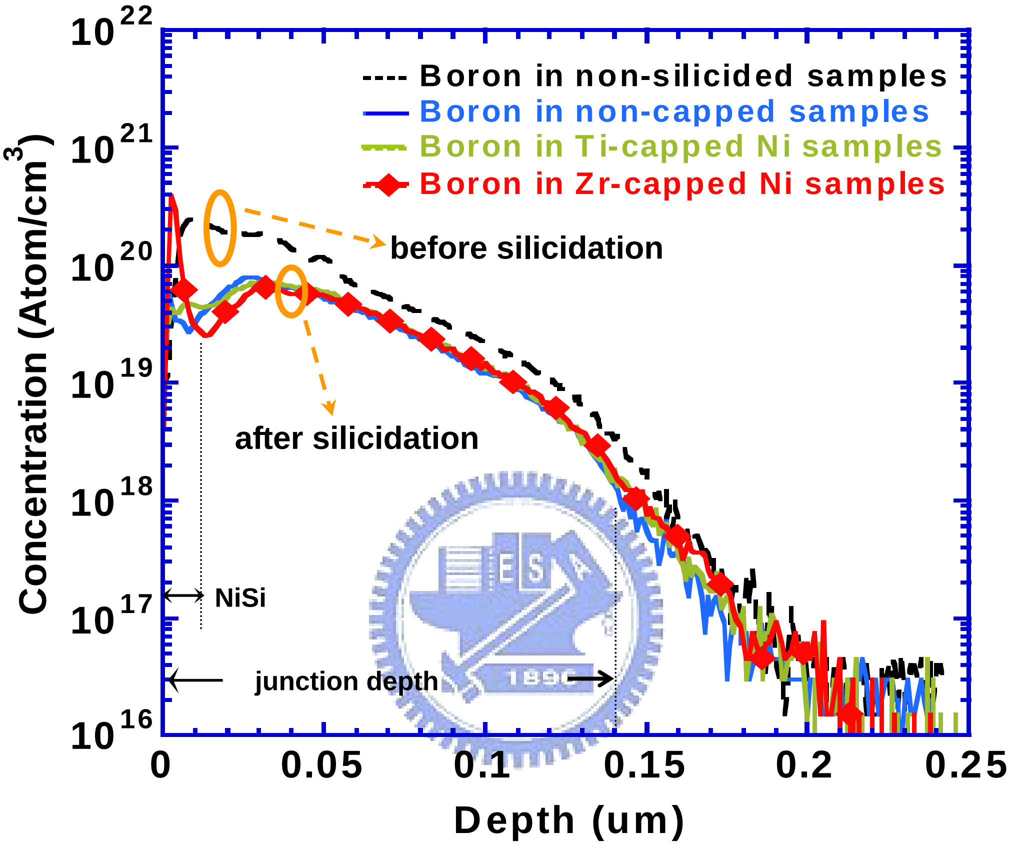
- field oxide isolation : 500nm
- junction formation : BF_2 , 40keV, 5E15
- dopants activation : RTA 950°C, 30s
- metal layer deposition : Ni (10nm) / the capping metal (5nm)
- silicidation : 550°C ~ 850°C
- stripping off unreacted metal
- metalization : **TiN (25nm) / Al (500nm)**

Fig. 3.1 Process flow of the nickel silicided junction



No. structure	non-silicided	non-capped	Ti -capped	Zr -capped
doping to junction	BF_2 of 40keV, 5E15 for p^+/n junction			
silicide metal	☒	nickel : 10nm		
capping metal	☒	☒	titanium : 5nm	zirconium : 5nm

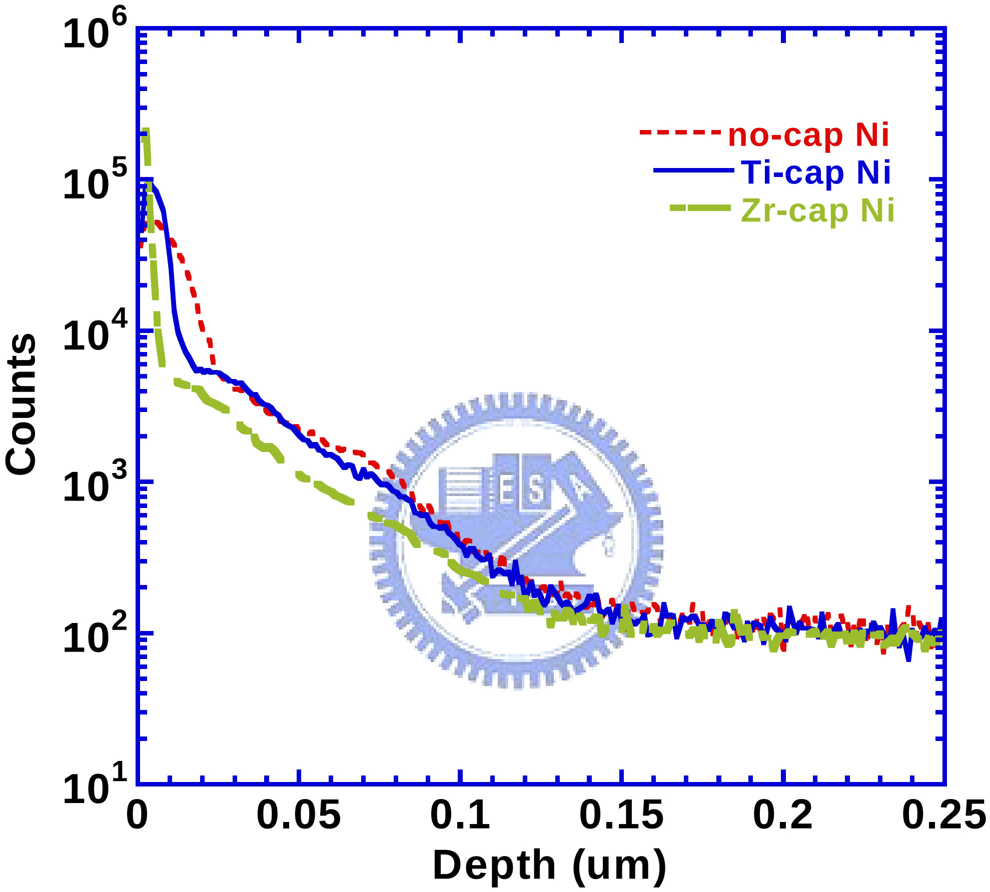
Table 3.1 P^+/n junctions implanted by BF_2 with and without nickel silicide in different capping conditions. The nickel film and the capping layer are about 10nm and 5nm respectively.



(a)

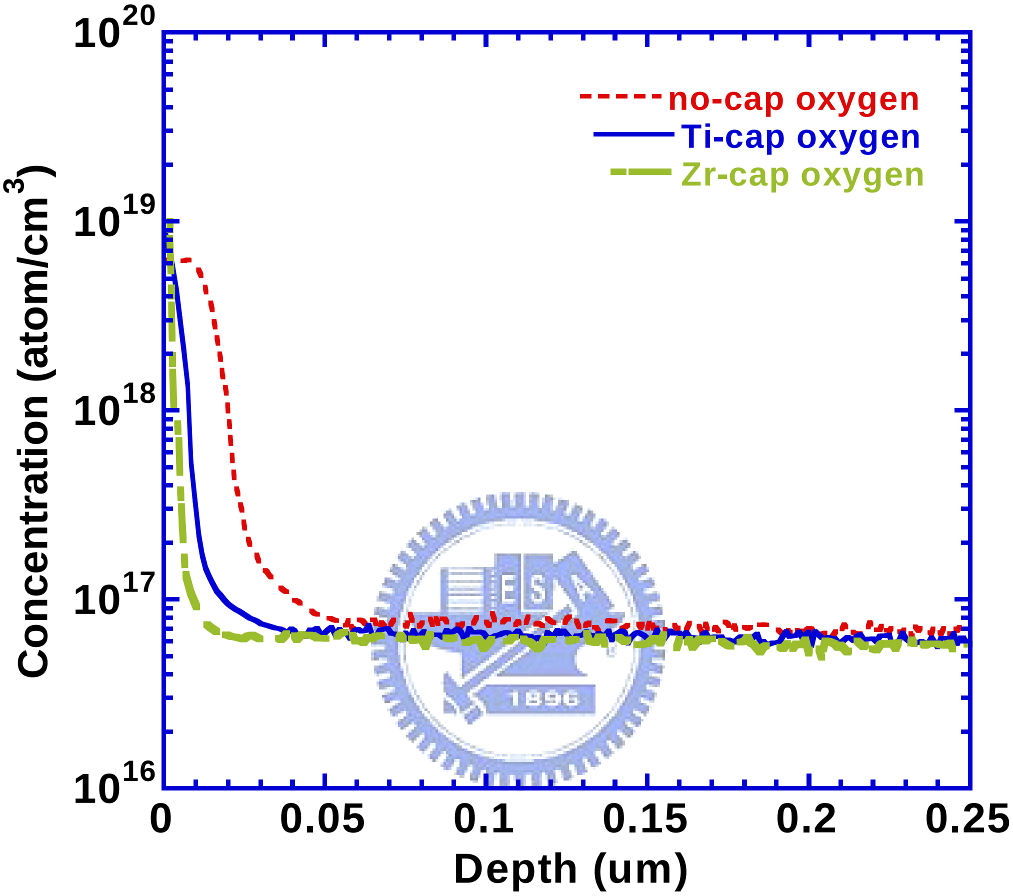
Fig. 3.2a SIMS profiles of impurities. The dopant activation and silicidation condition are 950ºC and 850ºC.

(a) Boron redistribution before and after silicidation. Silicide depth is about 10nm, which is consistentwith observation of TEM, and the junction depth is about 0.12μm.



(b)

Fig. 3.2b (b) The diffusion of nickel after silicidation at 850ºC with different capping layers. Zr-capping shows a good capability in suppressing penetration of nickel.



(c)

Fig. 3.2c (c) Oxygen contamination in nickel silicide in different capping conditions. This contamination can be eliminated by a novel Zr-cap layer.

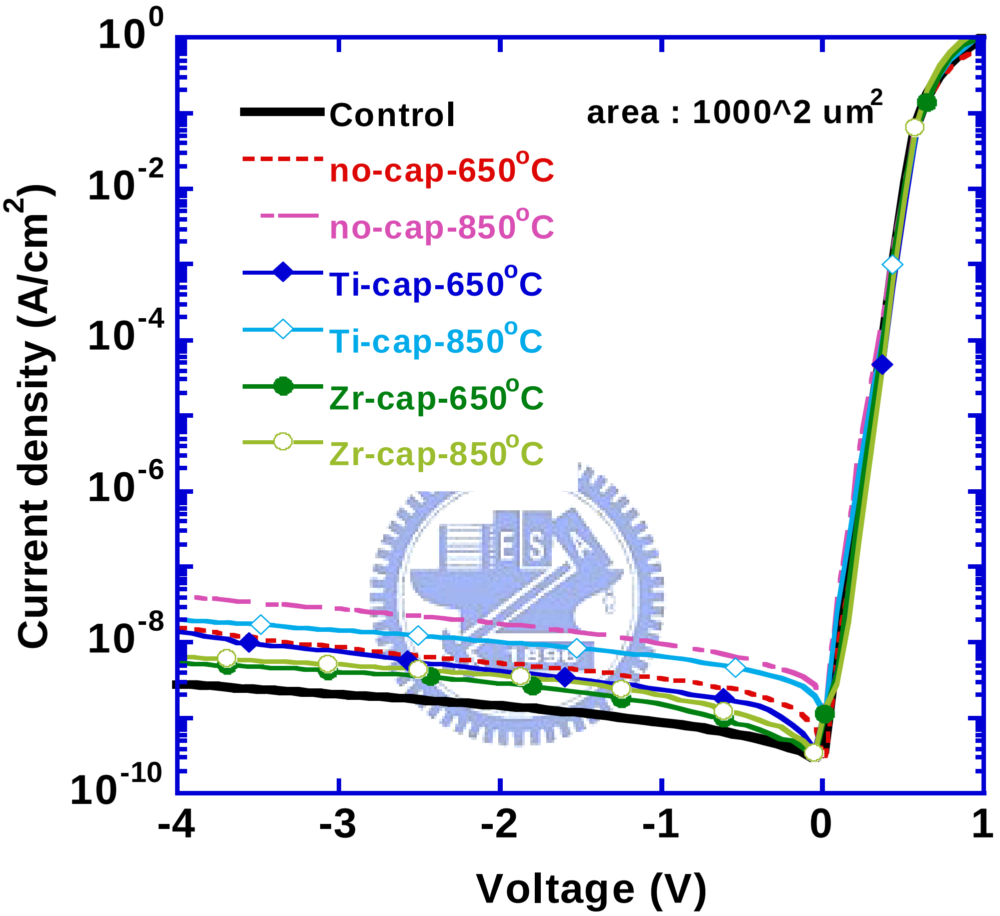
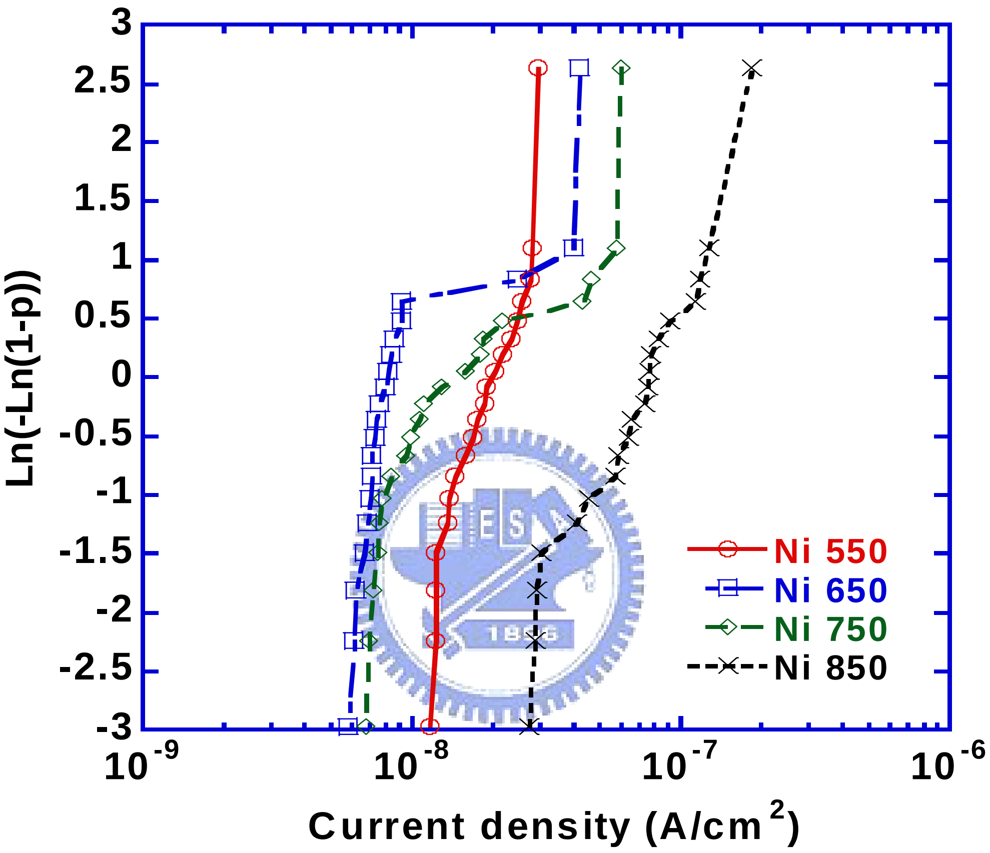
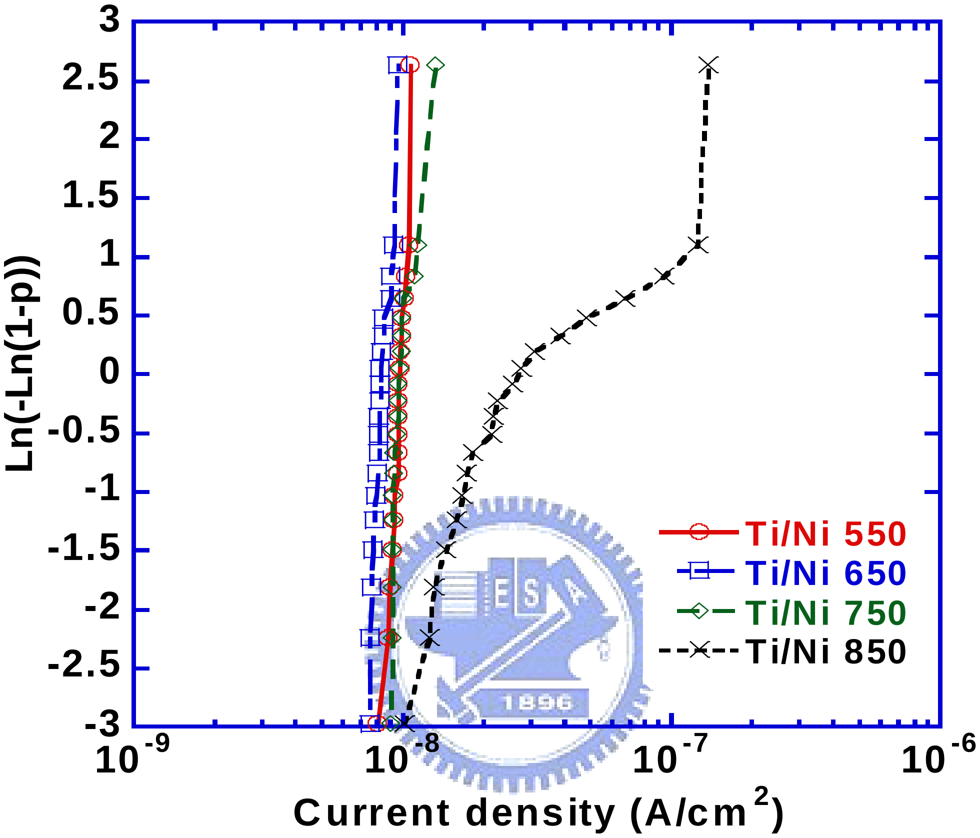


Fig. 3.3 Reverse current-voltage characteristics of all groups at silicidation temperature of 650ºC and 850ºC. The size of the junction area is 1000×1000 μm^2.



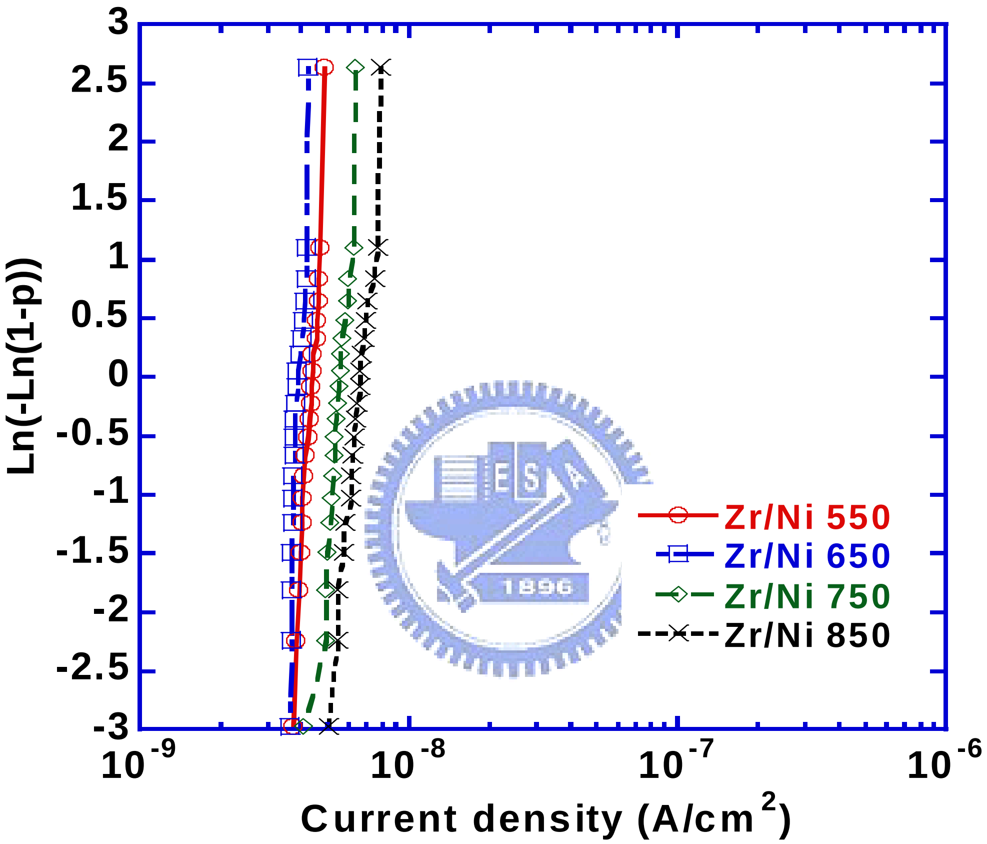
(a)

Fig. 3.4a Weibull plots of leakage current density measured at -3V for non-capped Ni samples at different RTA conditions.



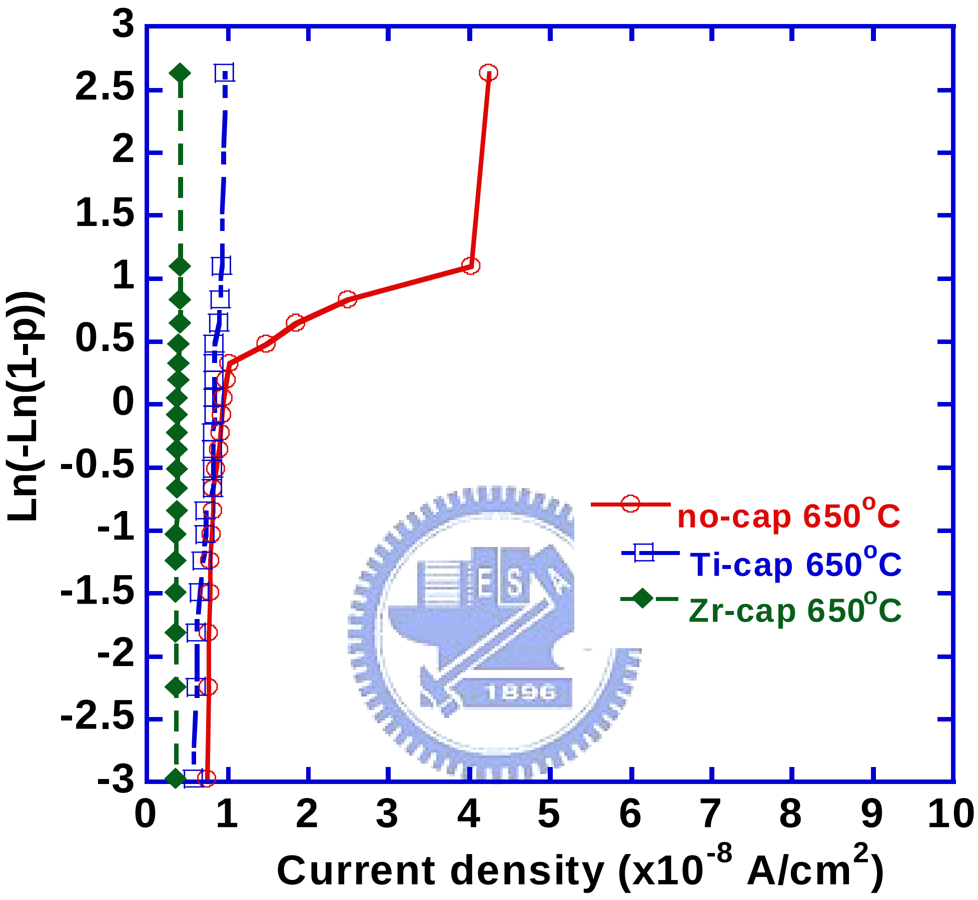
(b)

Fig. 3.4a Weibull plots of leakage current density measured at -3V for Ti capped Ni samples at different RTA conditions.



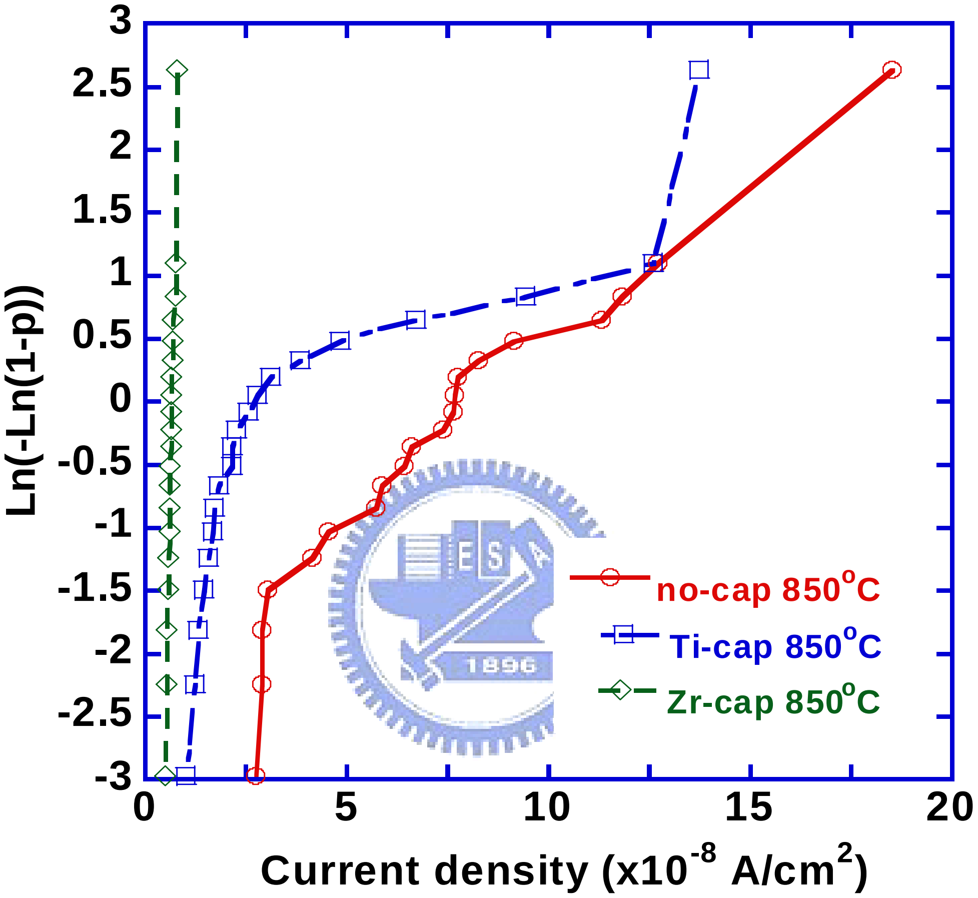
(c)

Fig. 3.4c Weibull plots of leakage current density measured at -3V for Zr capped Ni samples at different RTA conditions.



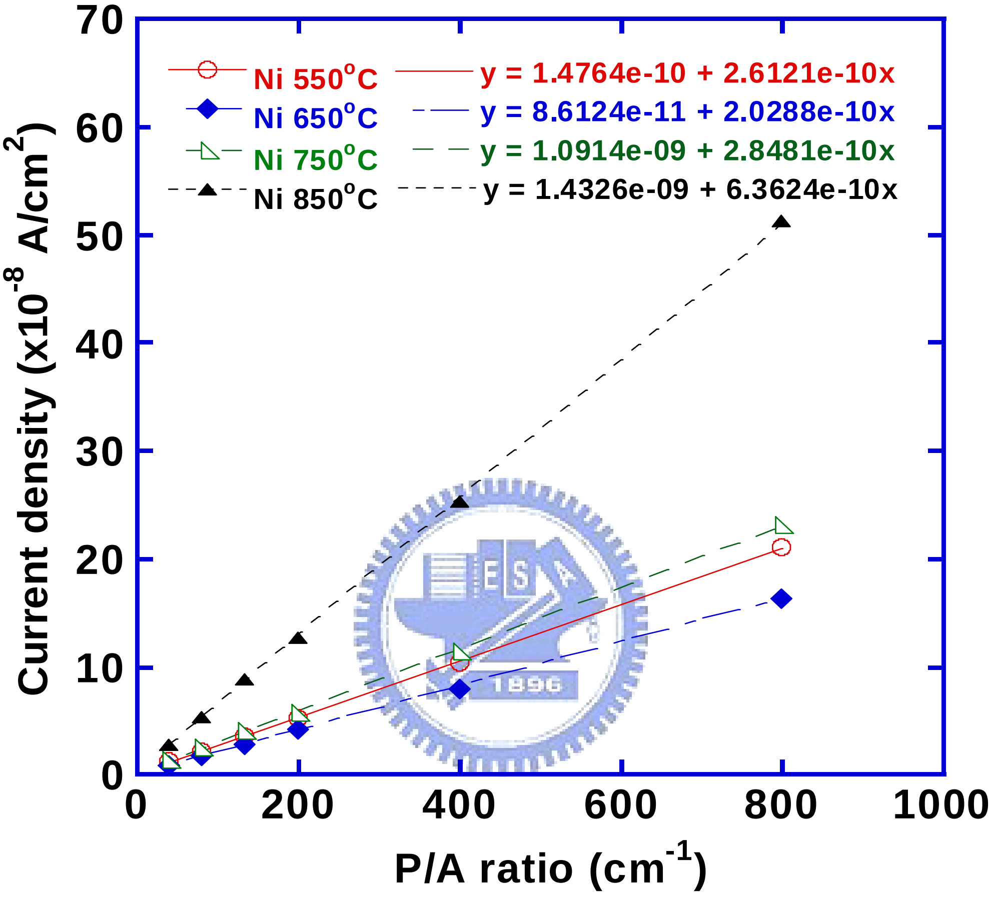
(a)

Fig. 3.5a Weibull plots of leakage current density measured at -3V for all silicided samples. (a) at RTA condition of 650ºC.



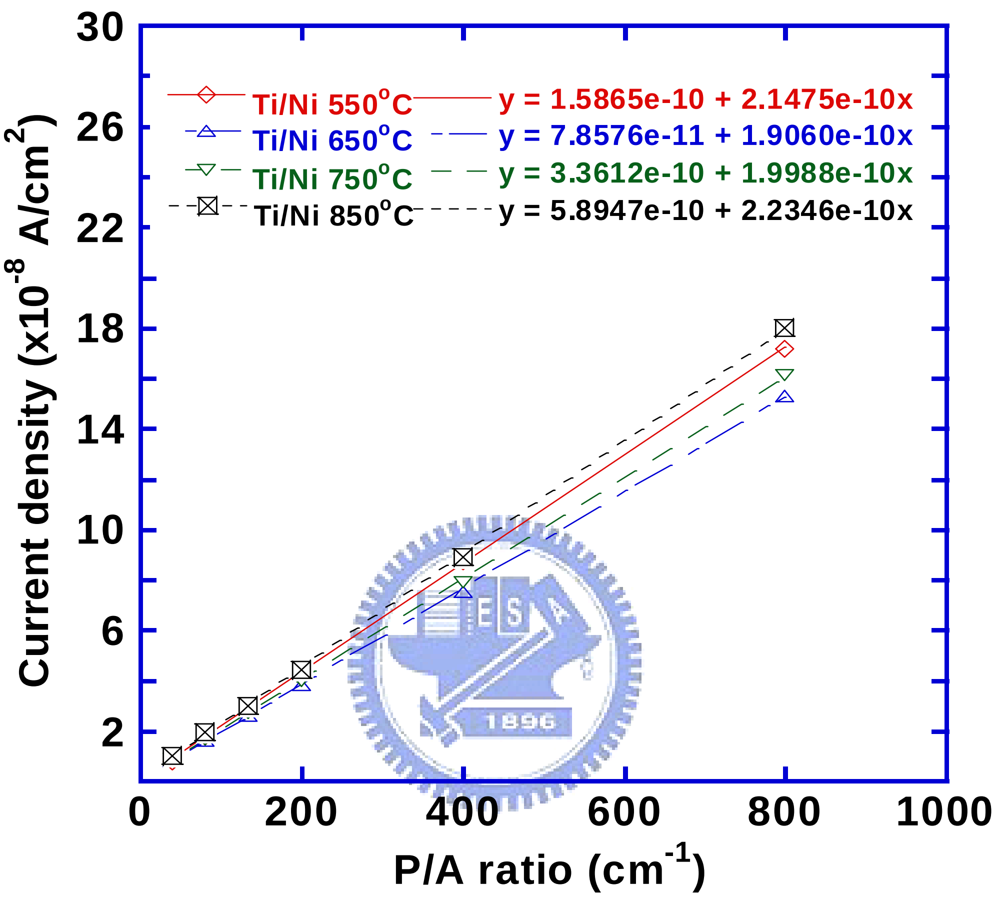
(b)

Fig. 3.5b Weibull plots of leakage current density measured at -3V for all silicided samples. (b) at RTA condition of 850ºC.



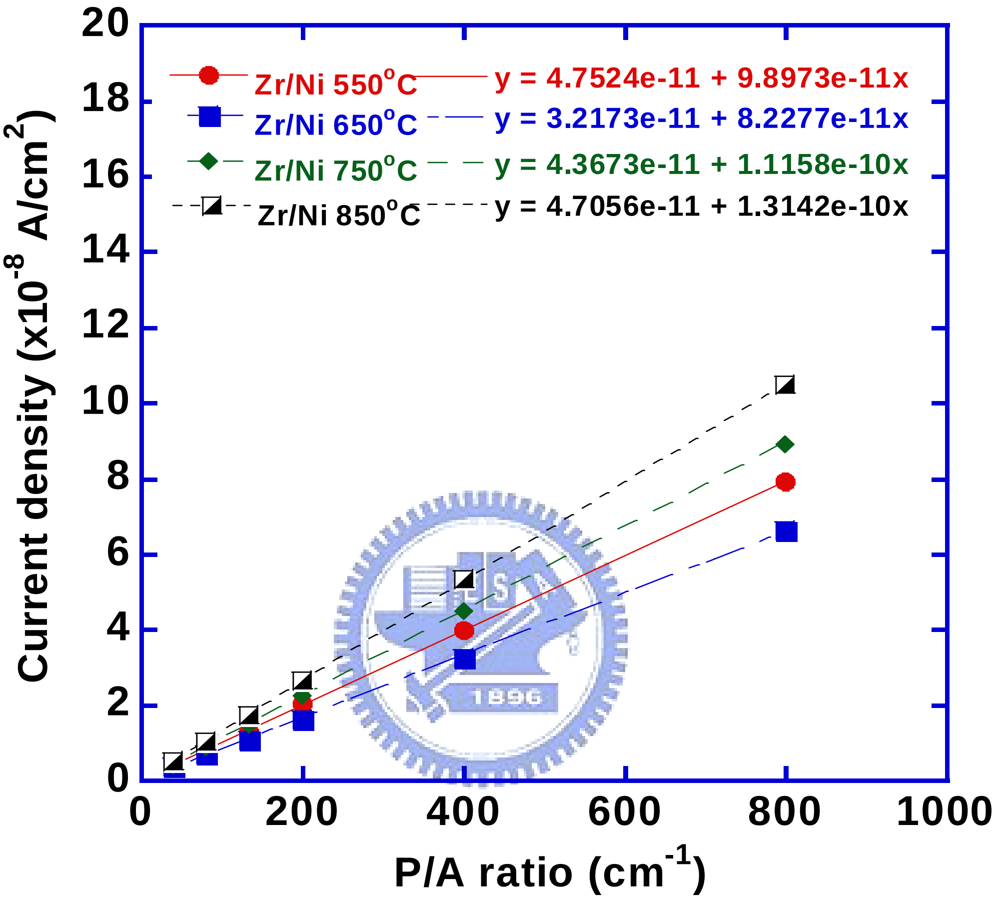
(a)

Fig. 3.6a Comparison of the reverse junction leakage current density vs. the periphery to area ratio (P/A ratio) for (a) nickel silicide.



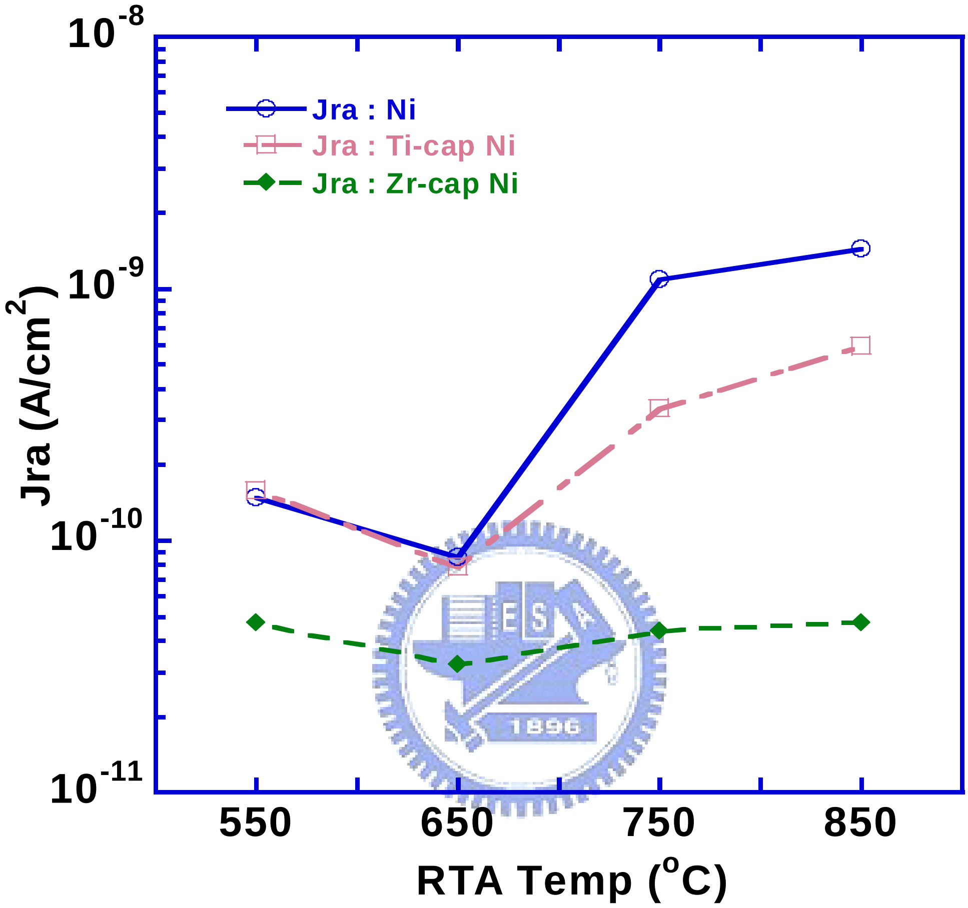
(b)

Fig. 3.6b Comparison of the reverse junction leakage current density vs. the periphery to area ratio (P/A ratio) for (b) Ti-capped nickel silicide.



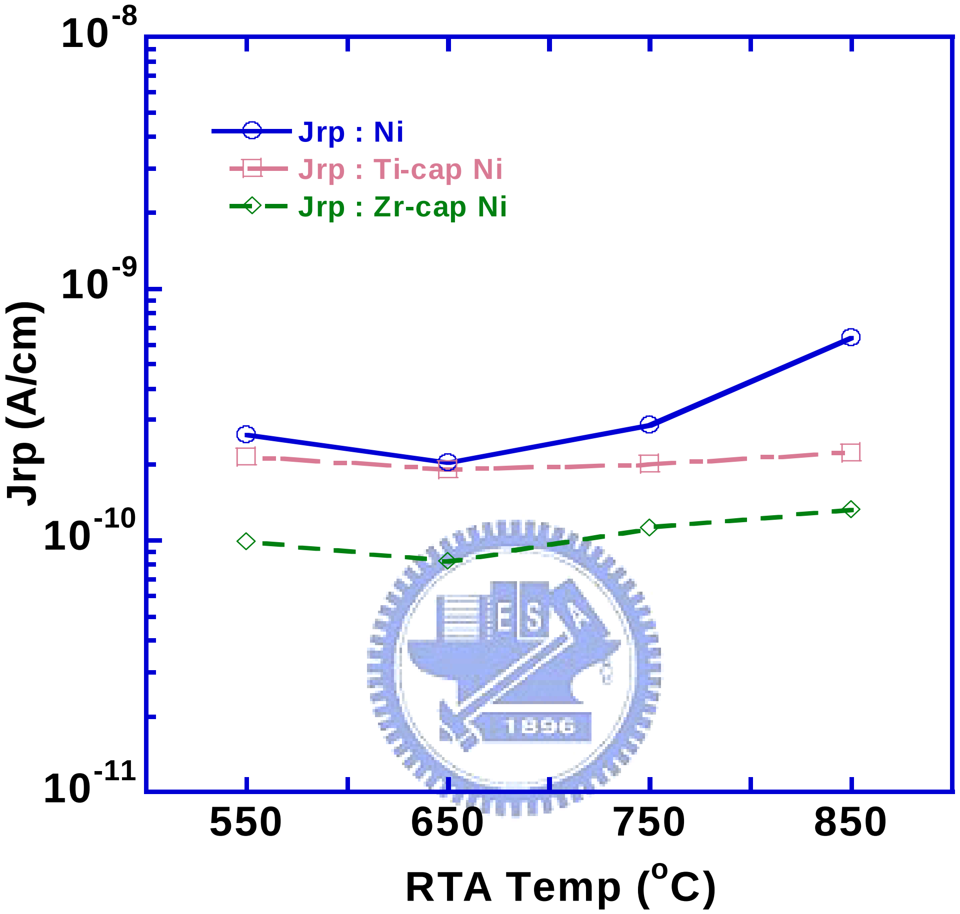
(c)

Fig. 3.6c Comparison of the reverse junction leakage current density vs. the periphery to area ratio (P/A ratio) for (c) Zr-capped nickel silicide.



(a)

Fig. 3.7a (a) Reverse junction area leakage versus the RTA temperature for all nickdel silicided junctions in different capping conditions.



(b)

Fig. 3.7b (b) Reverse junction periphery leakage versus the RTA temperature for all nickdel silicided junctions in different capping conditions.

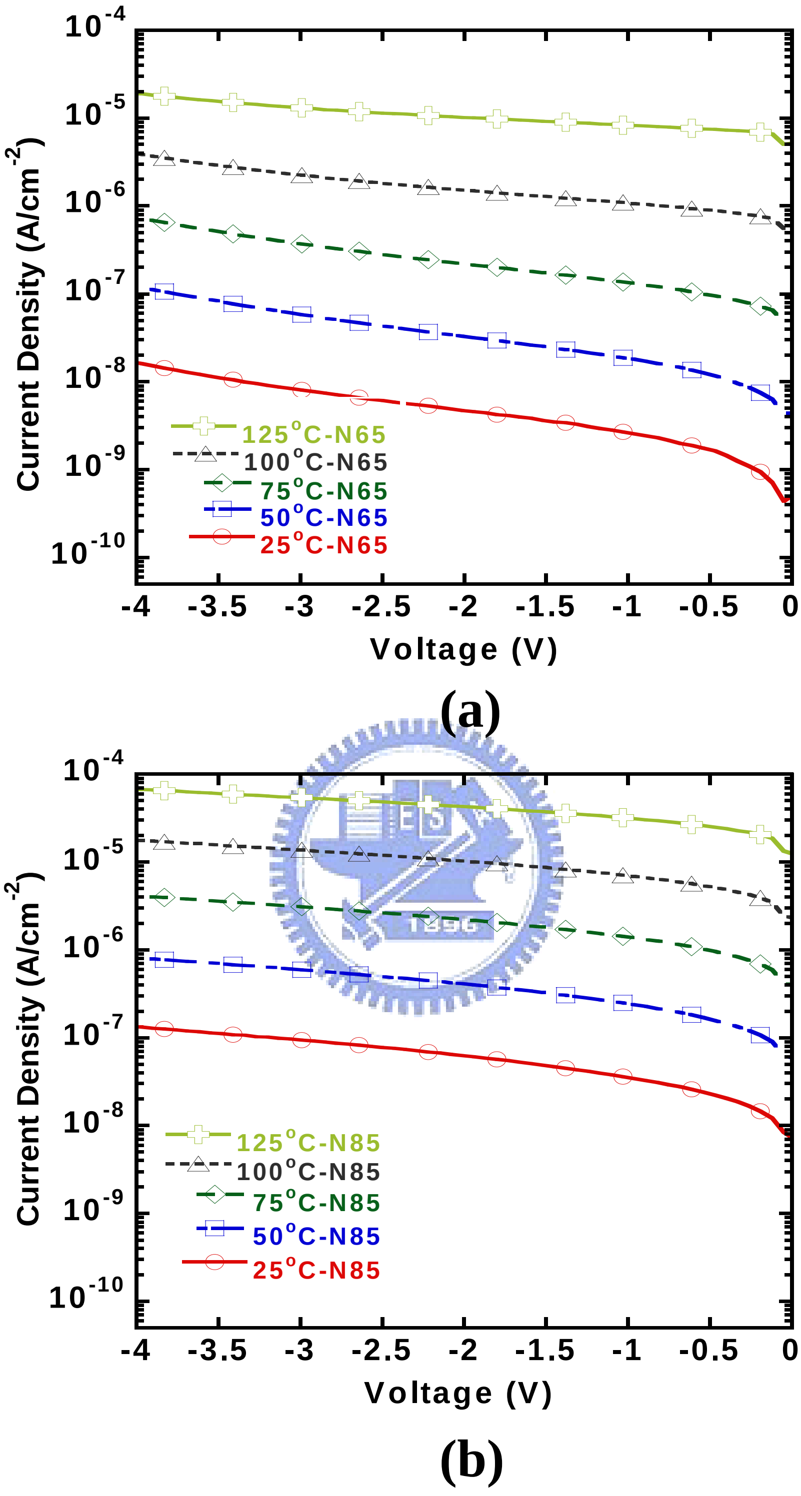
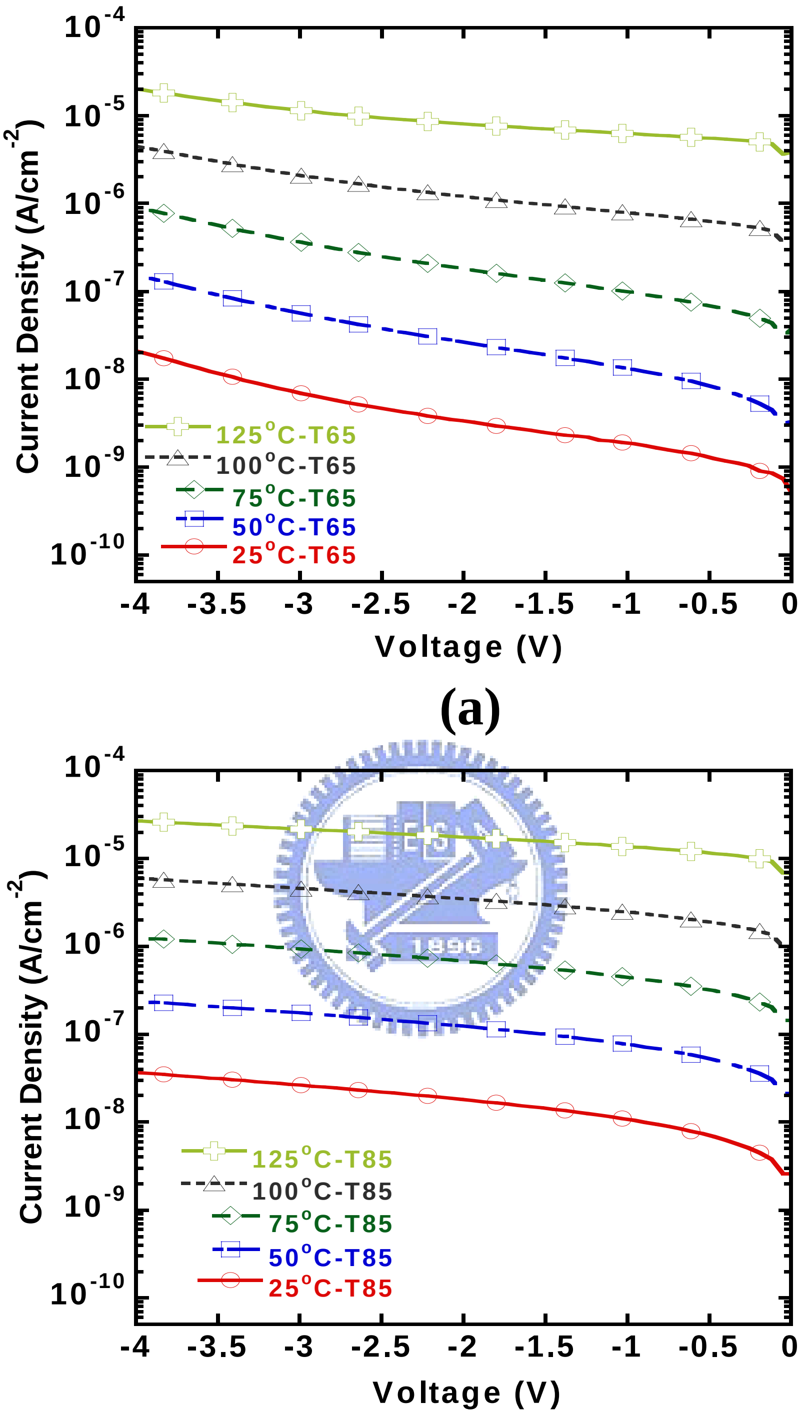


Fig. 3.8 Reverse currrent voltage characteristics of non-capped Ni samples measured at various temperatures. (a) samples with RTA 650°C (b) samples with RTA 850°C



(a)

(b)

Fig. 3.9 Reverse currrent voltage characteristics of Ti capped Ni samples measured at various temperatures. (a) samples with RTA 650°C (b) samples with RTA 850°C

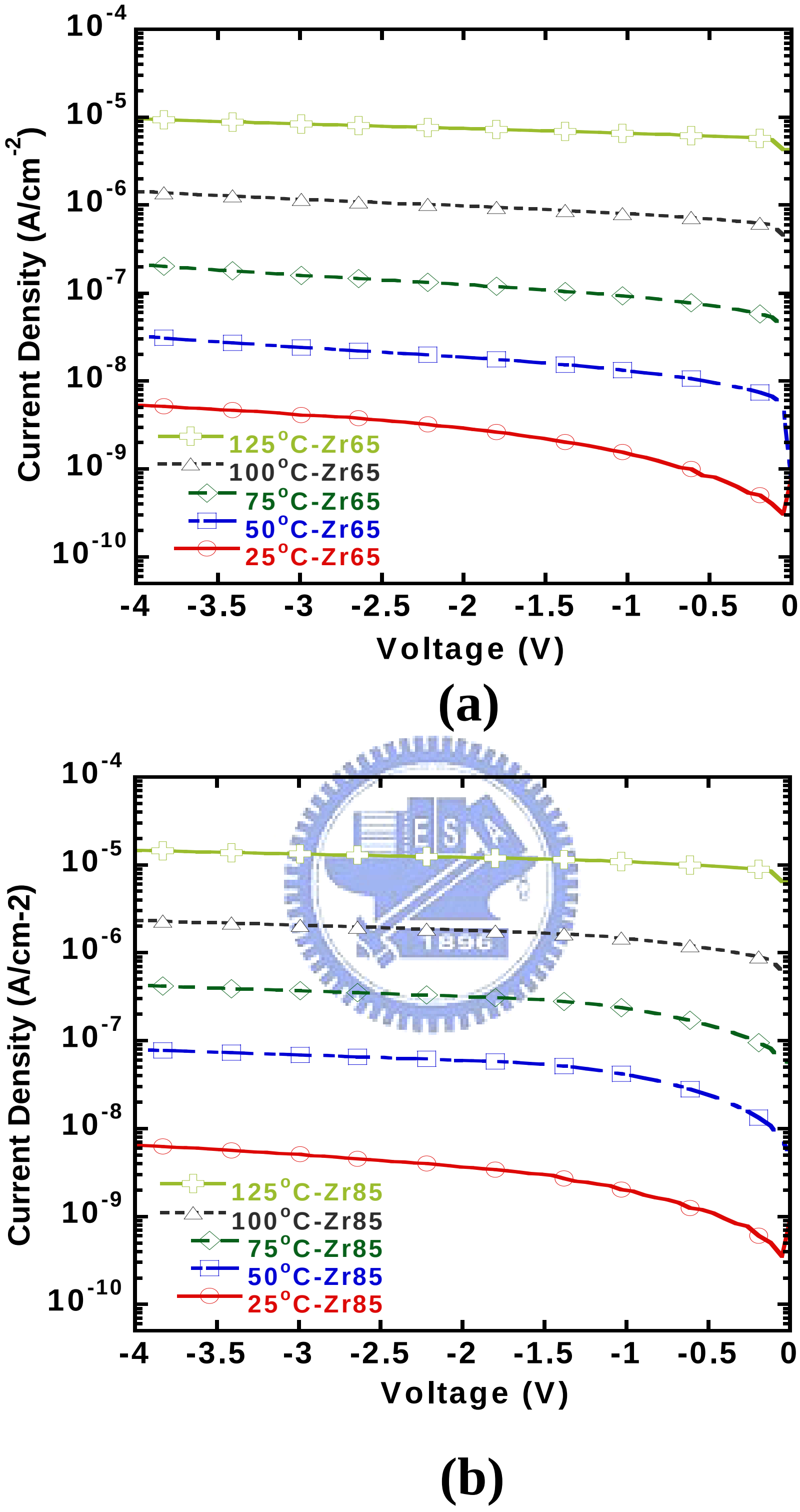
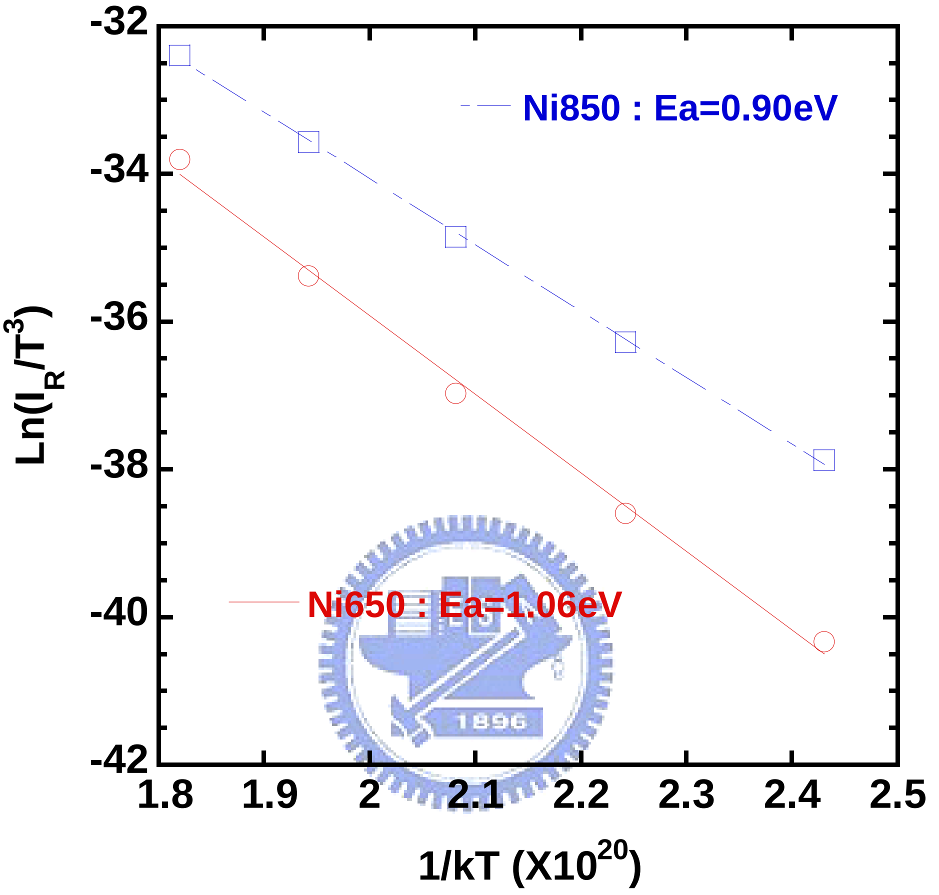
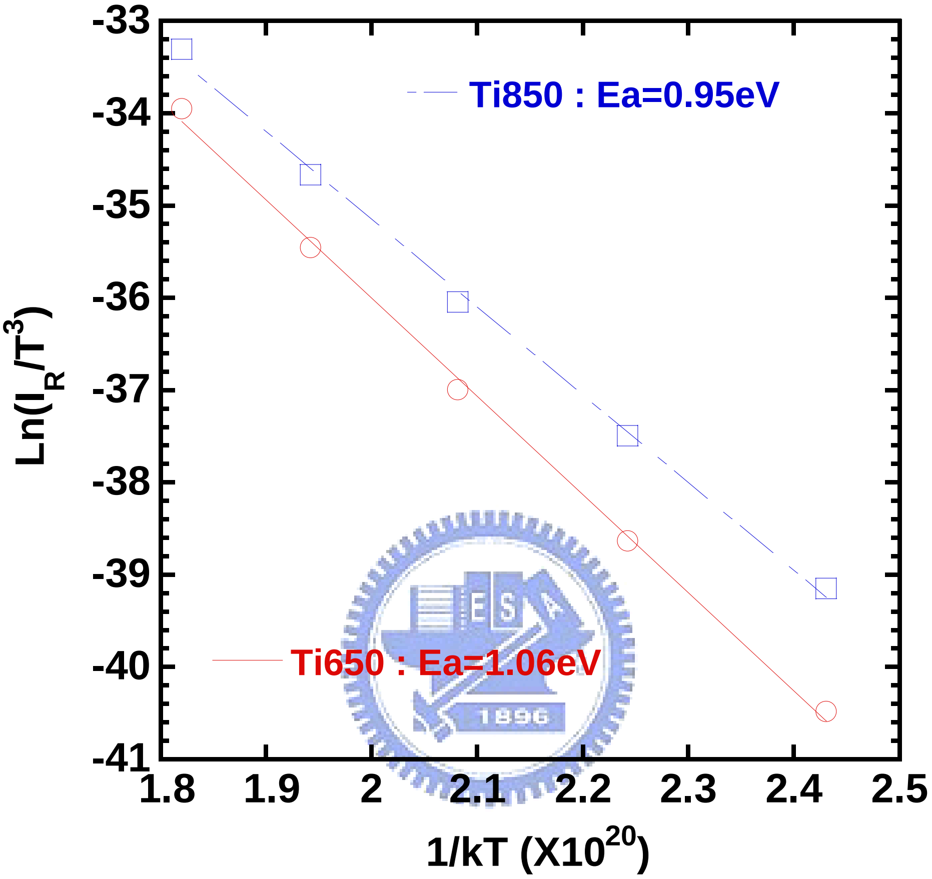


Fig. 3.10 Reverse currrent voltage characteristics of Zr capped Ni samples measured at various temperatures. (a) samples with RTA 650°C (b) samples with RTA 850°C



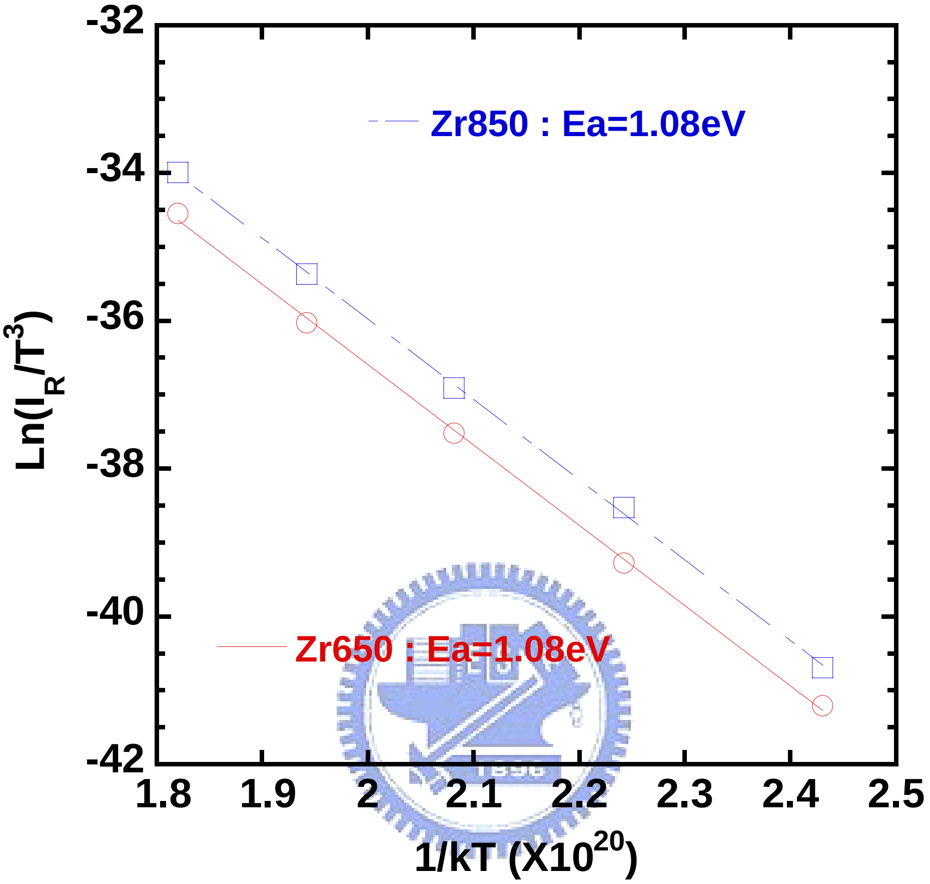
(a)

Fig. 3.11a Arrhenius plot (Ln I_R/T^3 versus 1/kT) for non-capped nickel silicide schottky junction after RTA at 650°C and 850°C, respectively measured at -3V.



(b)

Fig. 3.11b Arrhenius plot (Ln I_R/T^3 versus 1/kT) for Ti capped nickel silicide schottky junction after RTA at 650°C and 850°C, respectively measured at -3V.



(c)

Fig. 3.11c Arrhenius plot (Ln I_R/T^3 versus 1/kT) for Zr capped nickel silicide schottky junction after RTA at 650°C and 850°C, respectively measured at -3V.

Chapter 4

Ultra-Shallow Junction Formation by PH_3 Plasma Immersion Method

4.1 Introduction

For complementary metal-oxide-semiconductor (CMOS) technology to meet the demanding scaling requirements, ultra shallow and low resistance junctions are required to suppress short channel effect (SCE) and to obtain high current drivability [1]. For the formation of ultra-shallow junction, the transient enhanced diffusion (TED) effect and channeling effect are the major problems. Numerous solutions have been proposed such as solid phase diffusion (SPD), pre-amorphizing ion implantation (PAI), low energy ion implantation (LII), plasma doping (PD) and laser annealing (LA) [2-8]. For SPD method, It has the advantage of not demonstrating transient enhanced diffusion effects. However, it is very difficult to control the thickness of screen oxide and the ion implantation energy which can remain the implanted dopants and the damages within screen oxide. In the view of PAI way, it is a good way to form a shallow junction by the channeling effect suppression. Nevertheless, the major problem for Si pre-amorphizing ion implantation is much more defects induce larger leakage ~ 10^{-8}A/cm^{-2} and a large spread of leakage current. New annealing processes should be developed to minimize density of defects. Table 4.1 shows the trend of source and drain extension junction depth and sheet resistance in 1999 ITRS [9]. To meet these needs, surface reaction doping was first introduced [9]. By this method, the defects result from ion implantation can be avoided. However, the plasma damage will be produced in the meantime.

In this chapter, we compared LA and PD method for ultra shallow junction formation and focus our investigation on the plasma doping without vertical bias method to eliminate the defects result from doping process.

4.2 Experimental

Fig. 4.1 shows the process flow and schematics for the fabrication of n$^+$/p junction by PH_3 plasma immersion. Following a standard Radio Corporation of America (RCA) cleaning process, a 500nm-thick field oxide was thermally grown on the p-type (100) oriented Si wafer with 3-5 Ω-cm at 1050°C for one hour. After isolation oxide formation, the active regions were defined by photolithography and etched by BOE (Buffer oxide etcher) solution. Subsequently, RCA clean was performed for eliminating the contamination. Then, the PH_3 plasma immersion was used to form an n$^+$/p junction with RF power 50W for 1, 5, and 10minutes, respectively. Parts of samples were capped with oxide layers before dopant activation. After plasma immersion, rapid thermal annealing (RTA) was carried out to formed n$^+$/p junctions at 850℃, 900℃, 950℃, and 1000℃ for 10sec and 30sec, respectively, in nitrogen ambient. At final metallization process, a thin TiN of about 25nm was deposited as a barrier layer and aluminum was deposited immedately for both the front and backside electrode. Table 4.2 is the split table of different annealing conditions for ultra shallow junction formation by PH_3 plasma immersion.

4.3 Results and Discussion

4.3.1 Sheet Resistance and SIMS Analysis of PH_3-Plasma Immersion Junction

Sheet resistances of all samples were examined with a four-point probe. Fig. 4.2a, shows the sheet resistance of PH_3 plasma immersion junction activated by excimer laser with different energy. Fig. 4.2b exhibits the sheet resistance of the junction annealed by different laser energy and then with RTA 950^{o}C for 30s. In Fig. 4.2c, the sheet resistance versus different laser energy of plasma doped junction with cap-oxide is extracted. It seems that dopant at the surface can't be activated even the laser energy up to 300mJ/cm^2. Fig 4.3 is the plot of sheet resistance vs. different RTA conditions of plasma doped junction with and without cap-oxide by 50W RF power for 5 minutes. And Fig. 4.4a, b and c show the sheet resistance of n^+/p junction doped by PH_3 plasma with 50W RF power for 1, 5 and 10 minutes, respectively. The sheet resistance of the junction with a oxide cap is much lower than that without capping. And the higher activation temperature is used, the lower sheet resistance is obtained. Fig. 4.5 a and b show the SIMS results of the phosphorus profile for PH_3 plasma doping junction with and without cap-oxide at different activation conditions, respectively. From Fig. 4.5b, a shallower junction depth about 30nm-depth can be achieved by plasma RF power of 50W for 5mins even with 950°C RTA for 30s. However, its lower surface dopant concentration results in a higher resistance pn junction. In order to keep the surface dopant from diffusing out, an oxide cap of 100nm was deposited immediately after PH_3 plasma doped by the PECVD system. Although ions of P produced by PH_3 plasma are retained at the surface and the dopant concentration at surface is rised due to this cap-oxide, the excessive junction depth can not be avoid (Fig. 4.5a). The deeper junction depth may be due to the plasma damages from the plasma treatment or due to the excessive phosphorus concentration at surface. About 40nm-deep junction is formed by activation temperature at 950°C for 5s. However, dopant activation with such a short time is not easy to control.

4.3.2 Basic IV Charateristics of PH_3 Plasma Doped Junction

The reverse leakage current-voltage characteristics of PH_3 plasma doped junction without capping is shown in Fig. 4.6a and the plasma RF power is 50W for 5minutes. In this figure, it compares the I-V characteristics of PH3 plasma junction with different RTA conditions. Fig. 4.6b shows the Weibull plots of reverse leakage current for PH_3 plasma junction measured at 3V. From these two plots, all samples with RTA for 30s have the larger leakage current except the sample with RTA at 850°C. Thus, the excessive annealing time will induce junction defects and increase the junction leakage. It is known that the leakage current (J_r) in p-n junction is composed of two components, i.e., the junction area leakage (J_{ra}) and junction periphery leakage (J_{rp}). Fig. 4.7a, and b are plots of the leakage current density versus the ratio of junction periphery and area of PH_3 plasma junction with RTA for 10s and 30s, respectively. The slope stands for the junction periphery leakage density, while the intersection with Y-axis represents the junction area leakage density. The excessive annealing time will result in the increase of J_{ra} and J_{rp} except the samples with RTA at 850^{o}C.

4.3.3 Temperature Effects of PH_3 Plasma Doped Junction

Fig. 4.8a and b are the Mechanism of generation current at low reverse bias and high reverse bias, respectively. At low bias, thermal emission is the major mechanium for generation current. But, at high bias, tunneling distance obviously is shorten ($d_2<d_1$). Furthermore, the reverse current is constructed from the generation current (I_{gen}) and diffusion current (I_{diff}). The current equations of these two components are as follows :

$$I_{gen} = \frac{1}{2} qA \frac{n_i}{\tau} W \propto T^{\frac{2}{3}} e^{\frac{-Eg}{2kT}} \text{ --(1)}$$

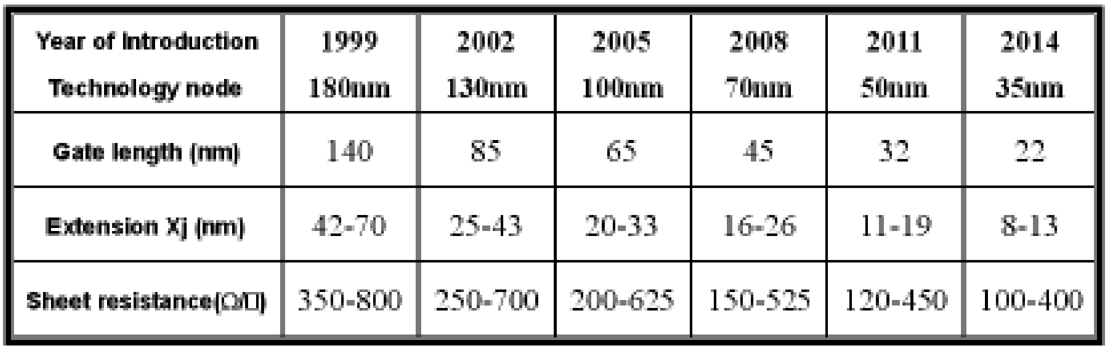
$$I_{diff} = qAD \frac{n_i^{\,2}}{N_b \times L_d} \propto T^3 e^{\frac{-Eg}{kT}} \text{ --(2)}$$

(I_{gen} is voltage dependent and I_{diff} is voltage independent.)

Fig. 4.9~4.14 show the reverse IV charateristics and activation energy (Ea) of PH_3 plasma junction with different activation conditions. For those reverse current-voltage plots, the diffusion current can be regarded as the dominant component of the leakage source due to its voltage independence (in plot-a of Fig. 4.9~4.14). However, junctions with dopant activation time of 30s, will obviously reduce the activation energy of thermal emission, especially at high annealing temperature except the samples with RTA at 850°C for 30s.

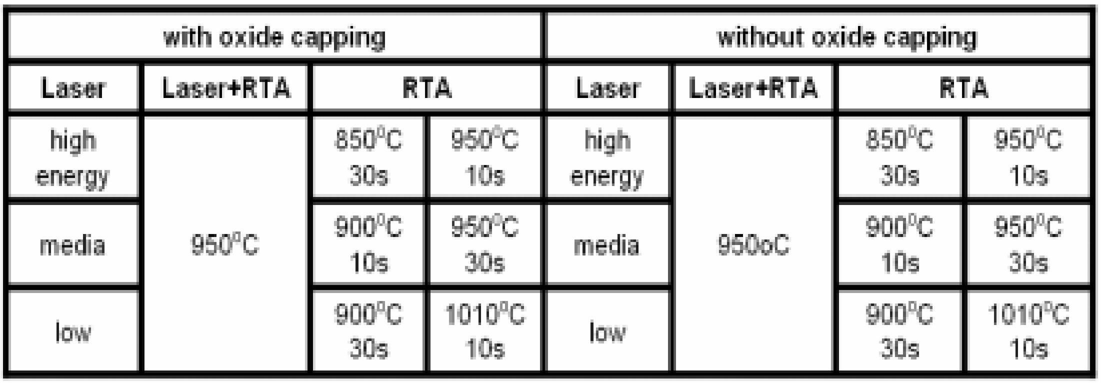
4.4 Summary

In summary, in this chapter, 30nm-deep ultra shallow junction can be achieved by PH_3 plasma doped method. However, preservation of surface concentration by a oxide cap will increase the junction depth which may result from oxide enhanced dopant diffusion, plasma damages during doping treatment or excessive phosphorus concentration at junction surface. The diffusion current will be the dominant component of leakge in a short dopant activation time. But the excessive annealing time will enhance the defect generation and result in the increase of leakage. Furthermore, it will lower the activation energy for junction leakage. In conclusion, by PH_3 plasma doped method with short activation time, the formation of a defect-less ultra-shallow junction below 30nm can be achieved for nano-scale MOS device application.



Year of Introduction Technology node	1999 180nm	2002 130nm	2005 100nm	2008 70nm	2011 50nm	2014 35nm
Gate length (nm)	140	85	65	45	32	22
Extension Xj (nm)	42-70	25-43	20-33	16-26	11-19	8-13
Sheet resistance(Ω/□)	350-800	250-700	200-625	150-525	120-450	100-400

Table 4.1 the trend of S/D extension from ITRS99



with oxide capping				without oxide capping			
Laser	Laser+RTA	RTA		Laser	Laser+RTA	RTA	
high energy	950^{0}C	850^{0}C 30s	950^{0}C 10s	high energy	950oC	850^{0}C 30s	950^{0}C 10s
media		900^{0}C 10s	950^{0}C 30s	media		900^{0}C 10s	950^{0}C 30s
low		900^{0}C 30s	1010^{0}C 10s	low		900^{0}C 30s	1010^{0}C 10s

Table 4.2 the split of different annealing conditions for ultra shallow junction formation by PH_3 plasma immersion method

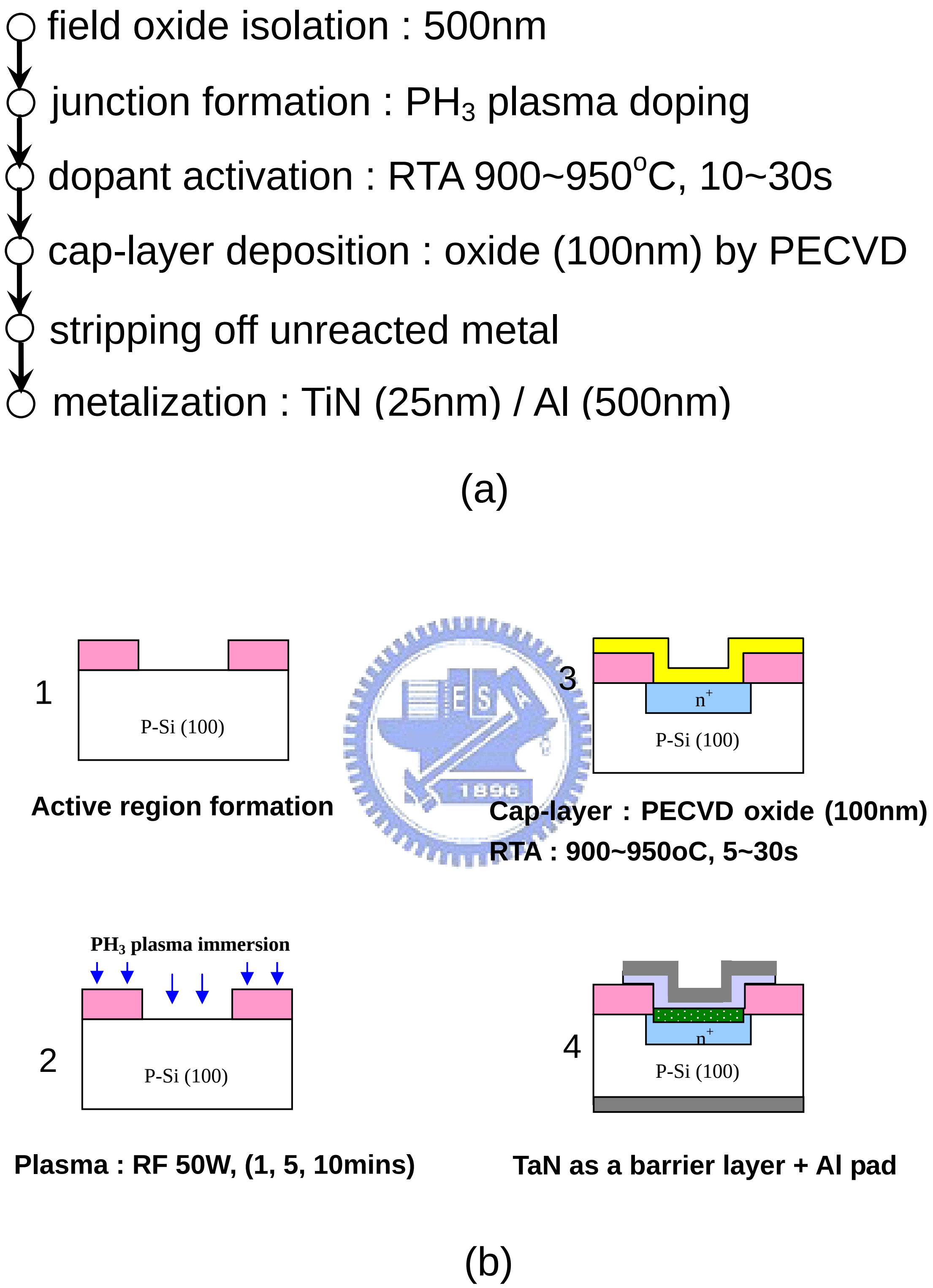
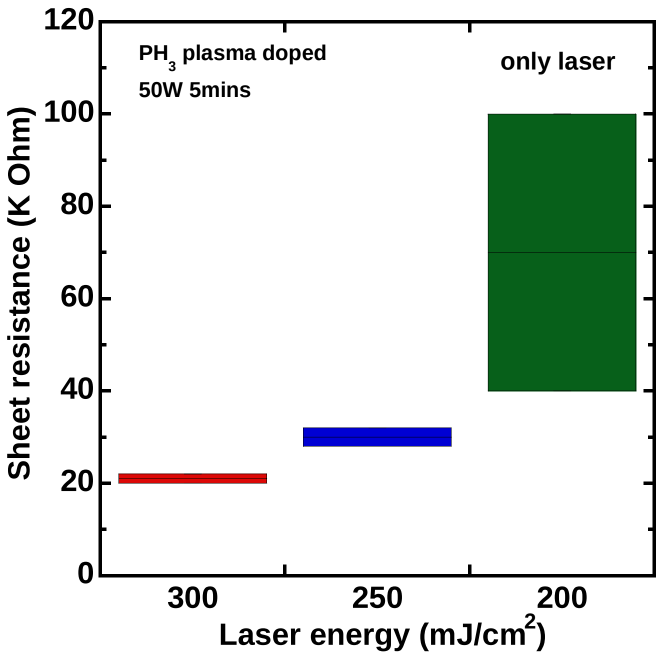
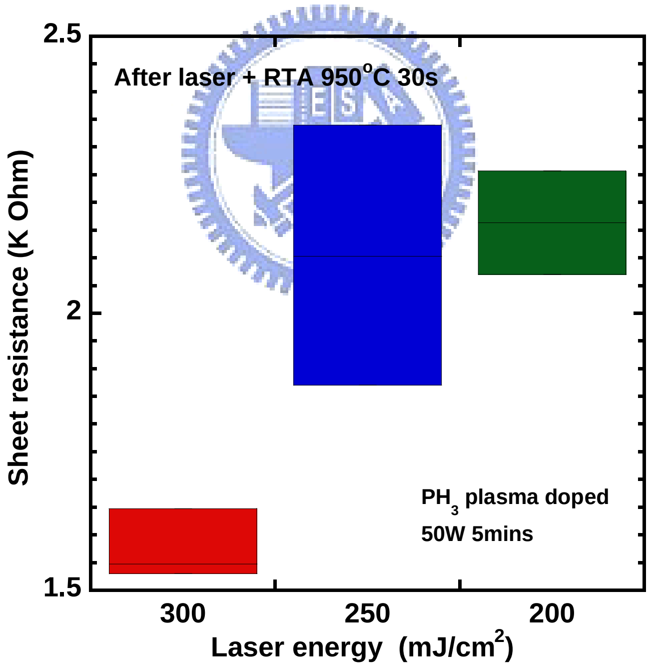


Fig. 4.1 (a) Key processes of n^+/p junction formation. (b) The schematics of n^+/p junction fabrication.

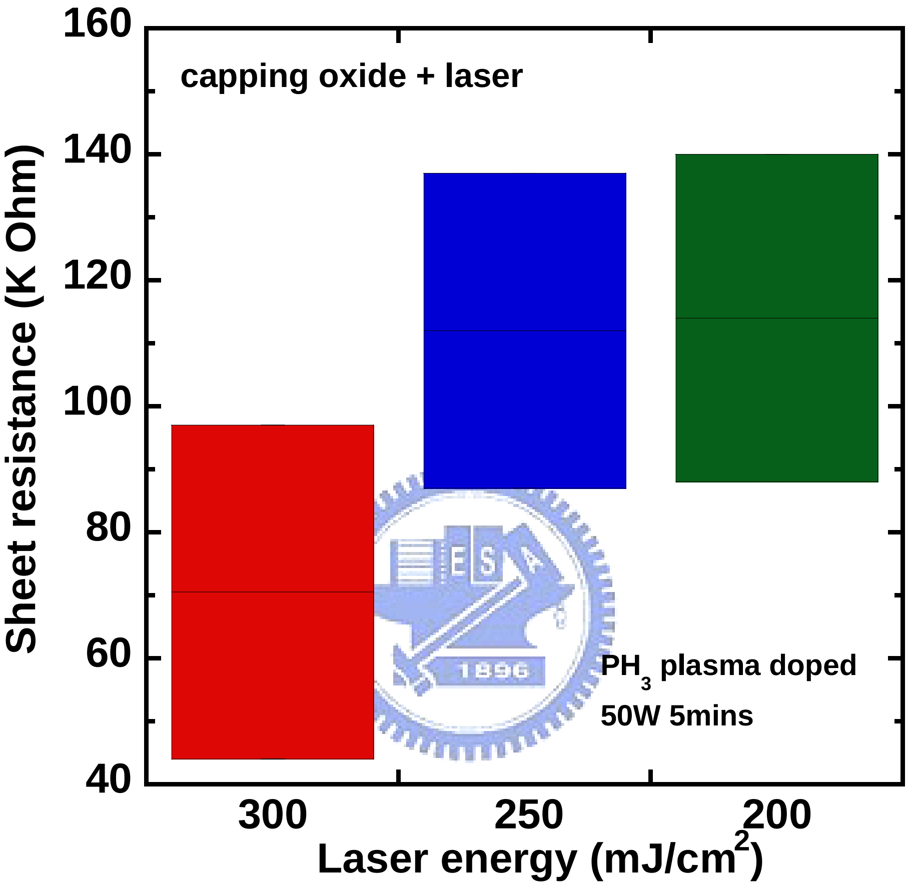


(a)



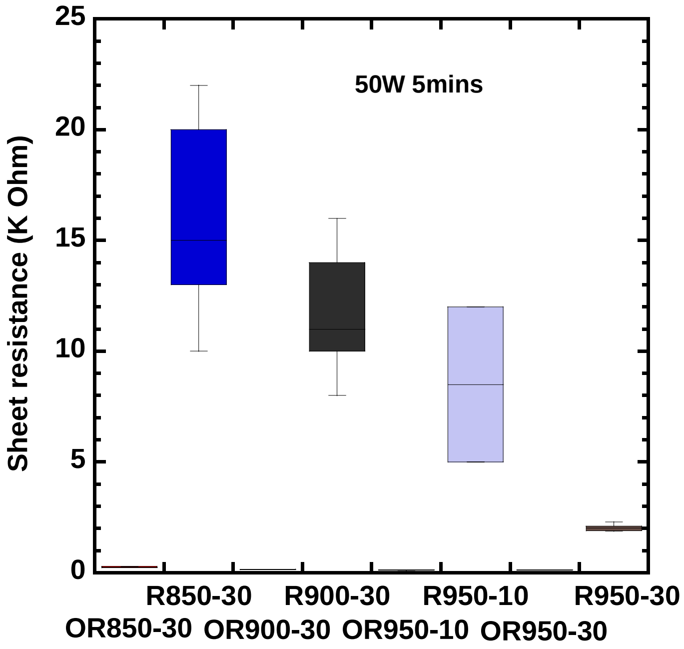
(b)

Fig. 4.2 sheet resistance plot (a) with different Laser annealing energy. (b) with different Laser annealing engery and RTA at 950^{o}C for 30s.

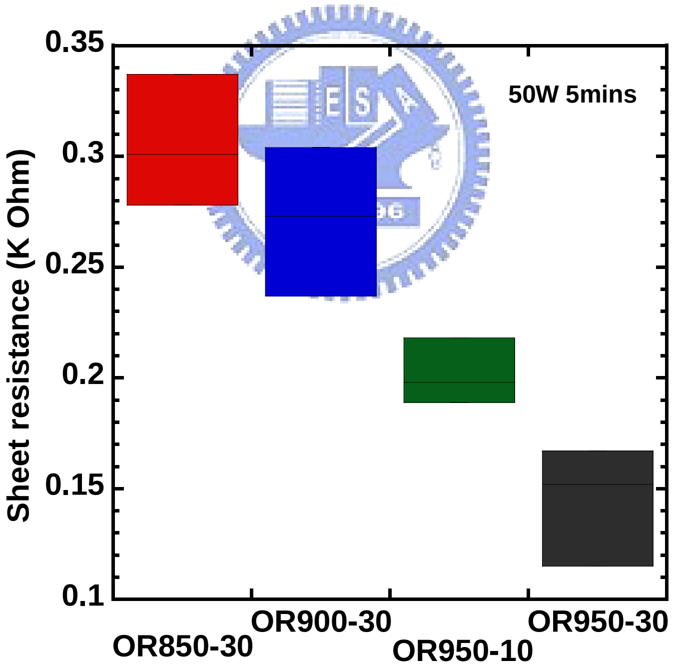


(c)

Fig. 4.2 sheet resistance plot of the n$^+$/p junction by PH3 plasma immersion with 100nm oxide capping (c) for different Laser energy

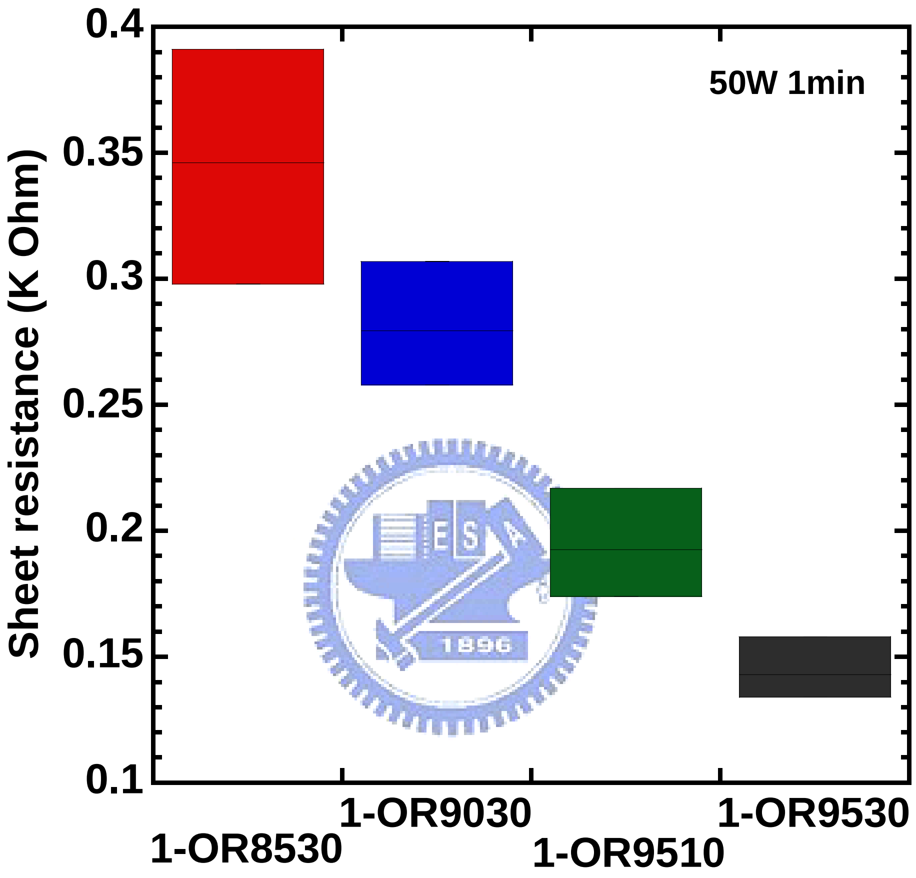


(a)



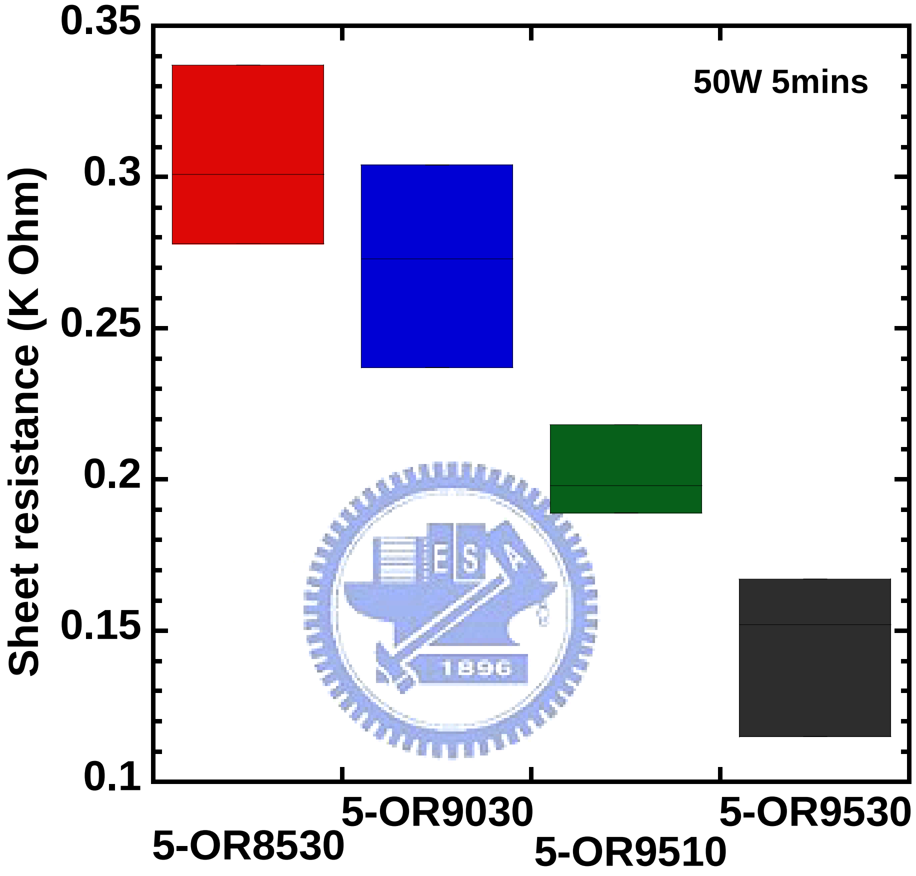
(b)

Fig. 4.3 sheet resistance versus different RTA conditions. (a) both n^+/p junction with and without oxide capping. (b) n^+/p junction with oxide capping.



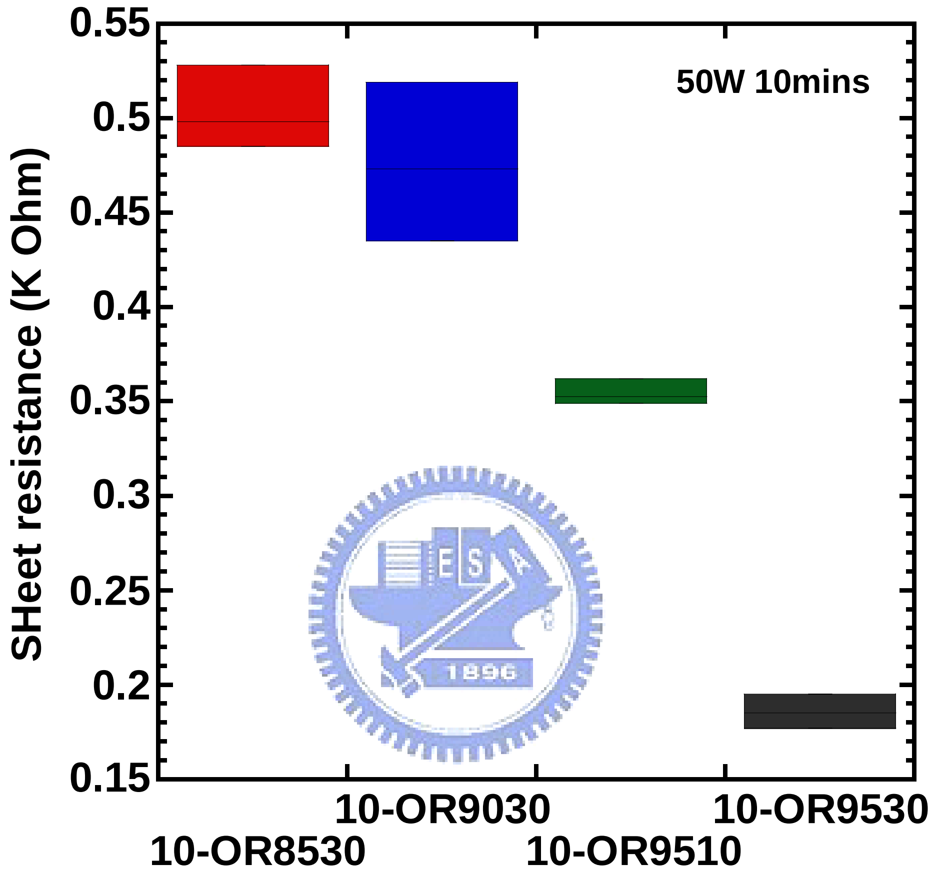
(a)

Fig. 4.4 (a) sheet resistance versus different RTA conditions of n^+/p junction with oxide capping by 50W plasma power for 1 minute.



(b)

Fig. 4.4 (b) sheet resistance versus different RTA conditions of n^+/p junction with oxide capping by 50W plasma power for 5 minutes.



(c)

Fig. 4.4 (c) sheet resistance versus different RTA conditions of n^+/p junction with oxide capping by 50W plasma power for 10 minutes.

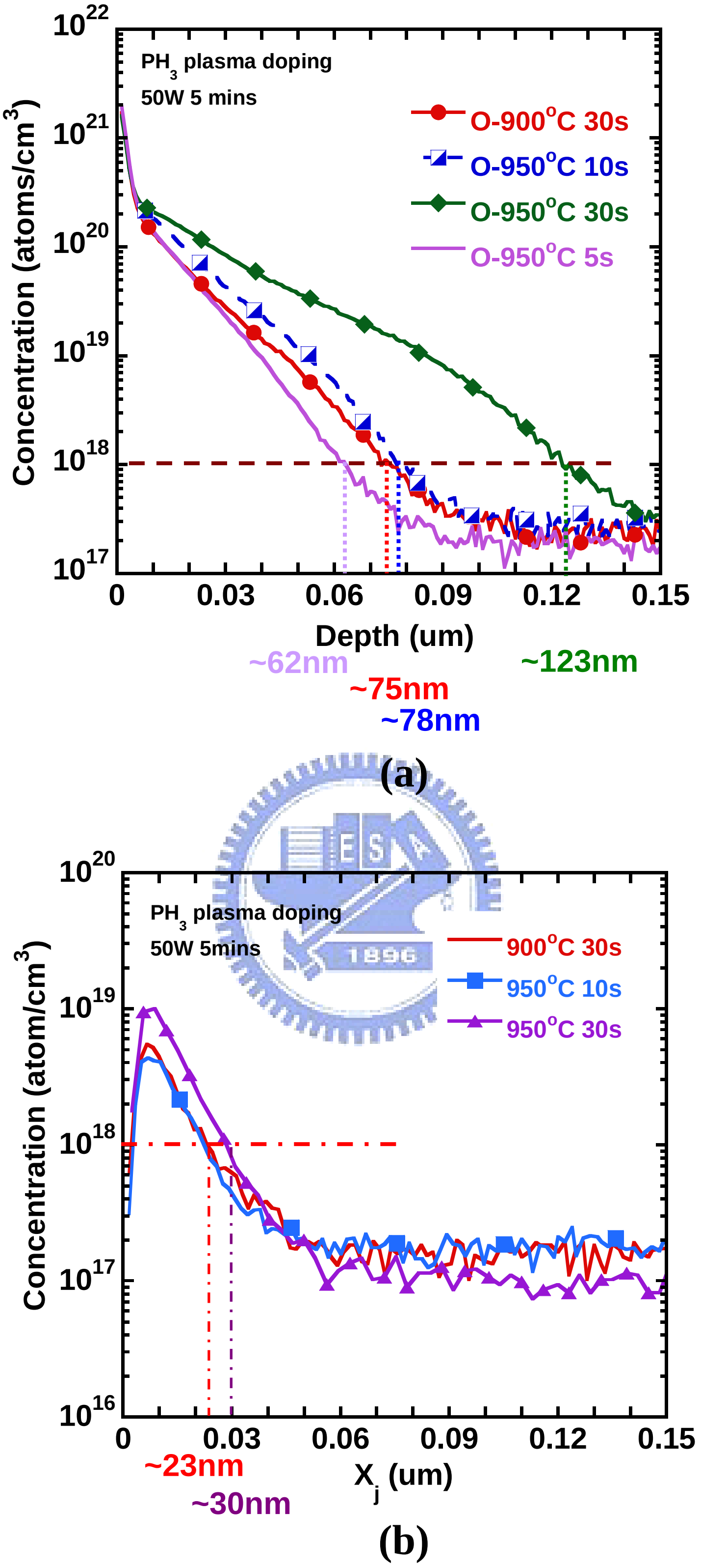
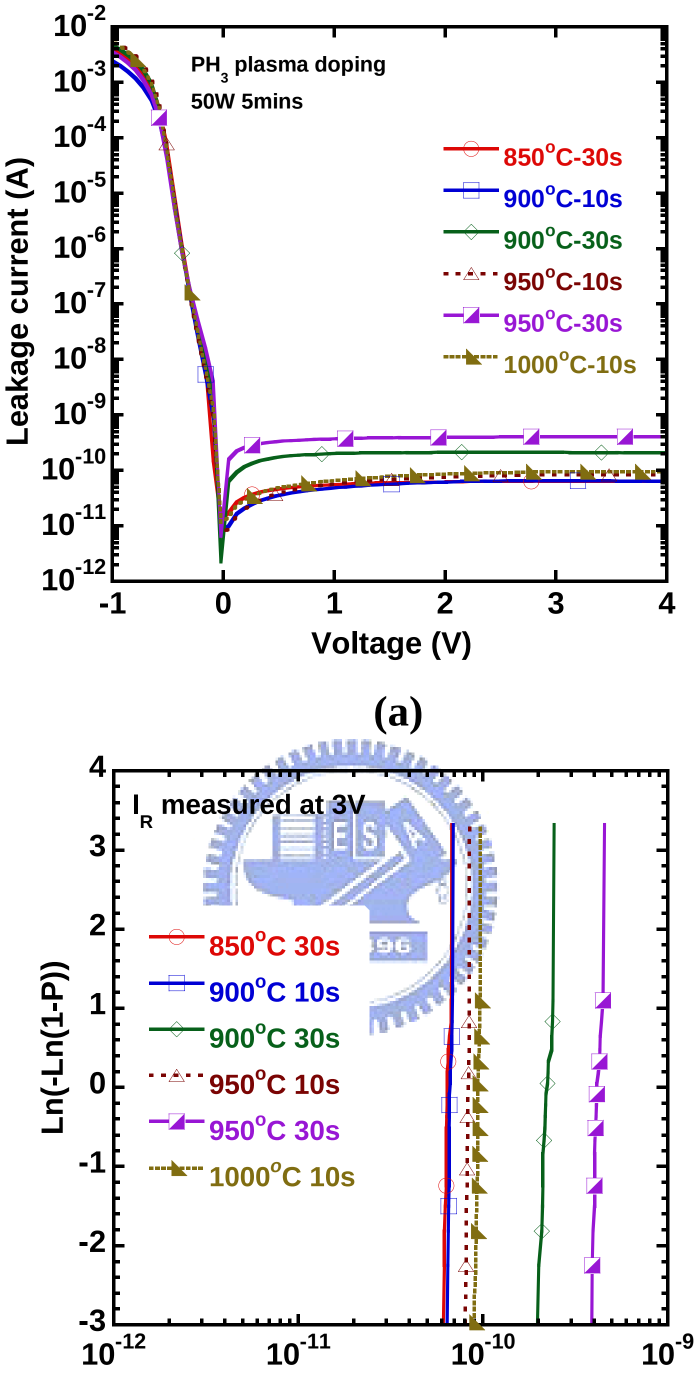


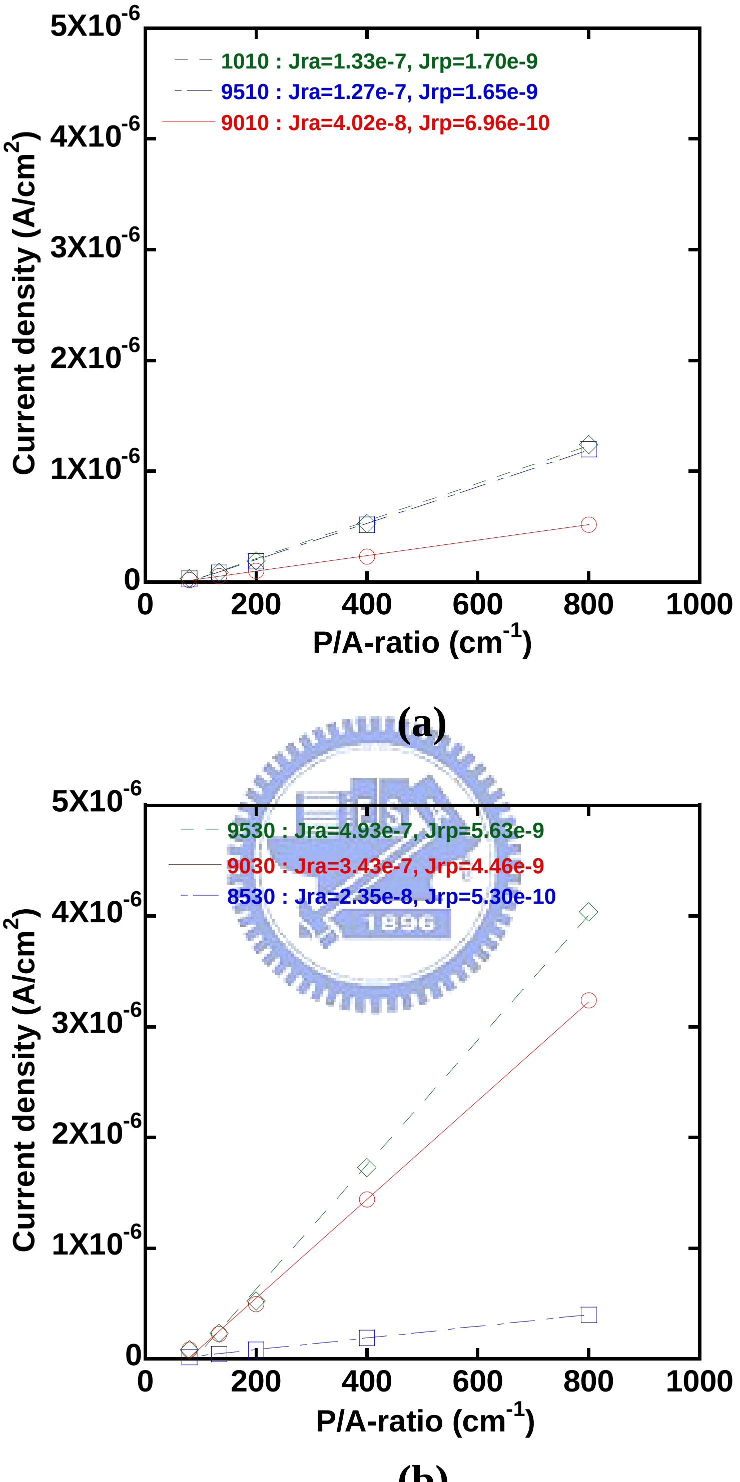
Fig. 4. 5 SIMS profile of n^+/p junction by PH_3 plasma doping at various RTA temperatures (a) with (b) without oxide capping.



(a)

(b)

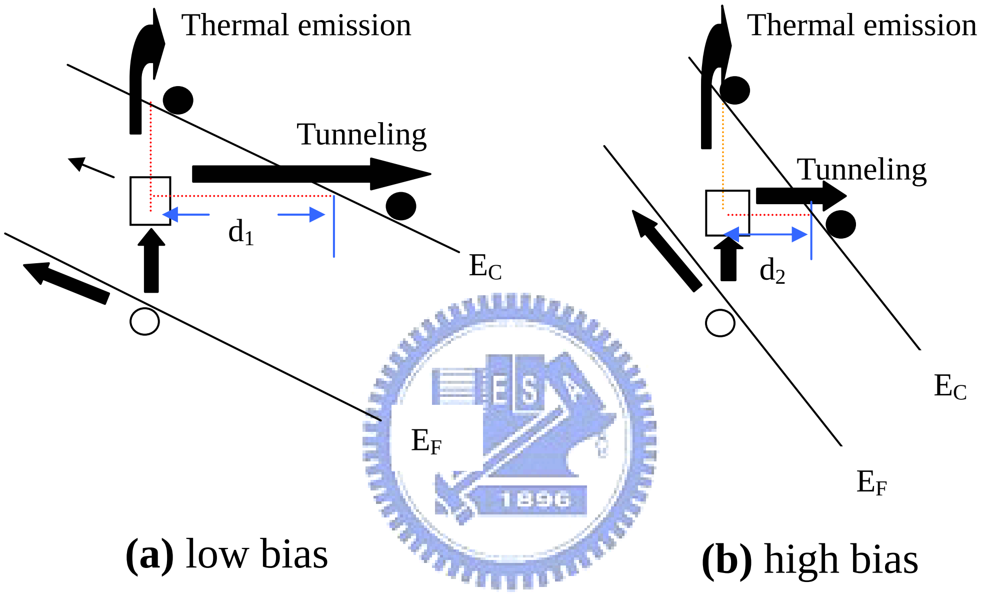
Fig. 4. 6 (a) Reverse current-voltage characteristics of PH_3 plasma junctions with different annealing conditions. (b) Weibull plots of reverse leakage current measured at 3V with different RTA conditions.



(a)

(b)

Fig. 4.7 Reverse junction leakage current density vs. periphery to area ratio (P/A ratio) with different annealing temperature for (a) 10s (b) 30s



(a) low bias **(b)** high bias

Fig. 4.8 Mechanism of generation current (a) is at low reverse bias and (b) is at high reverse bias.

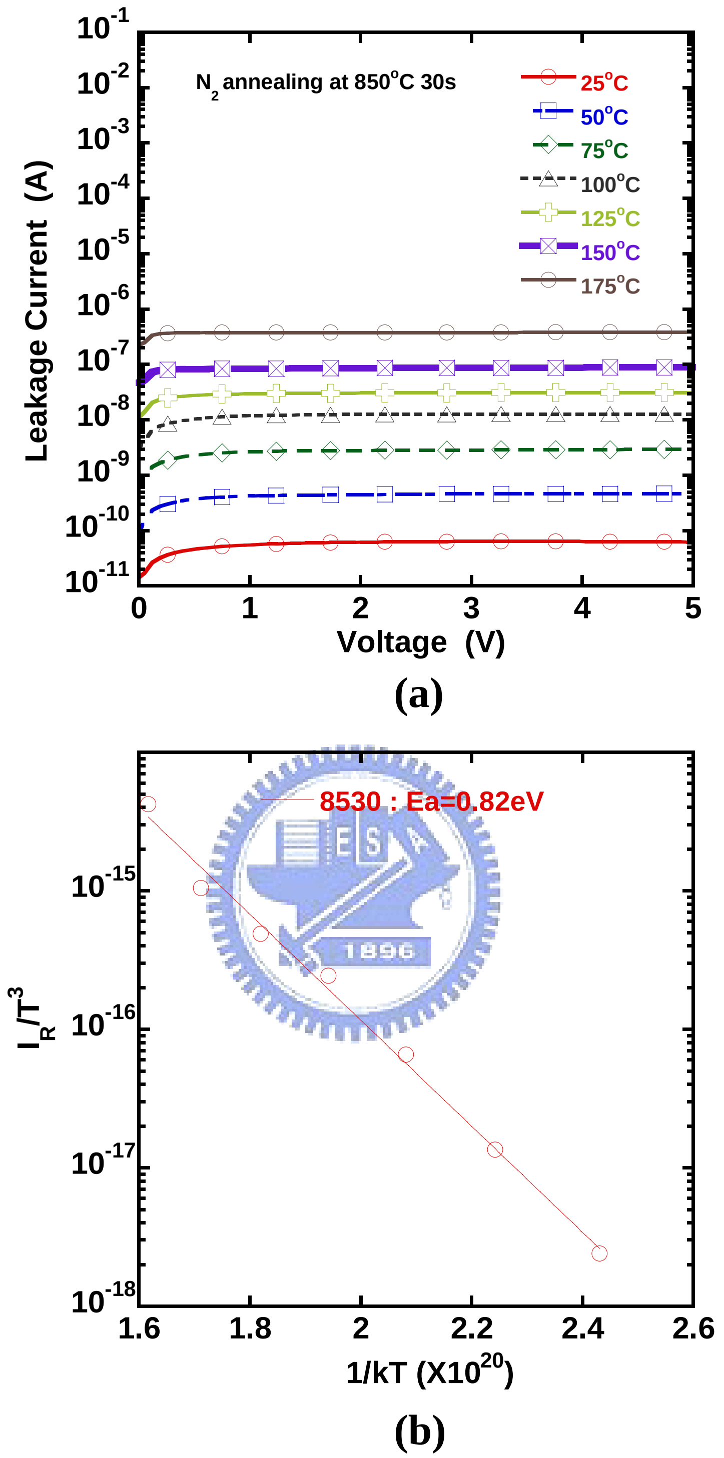
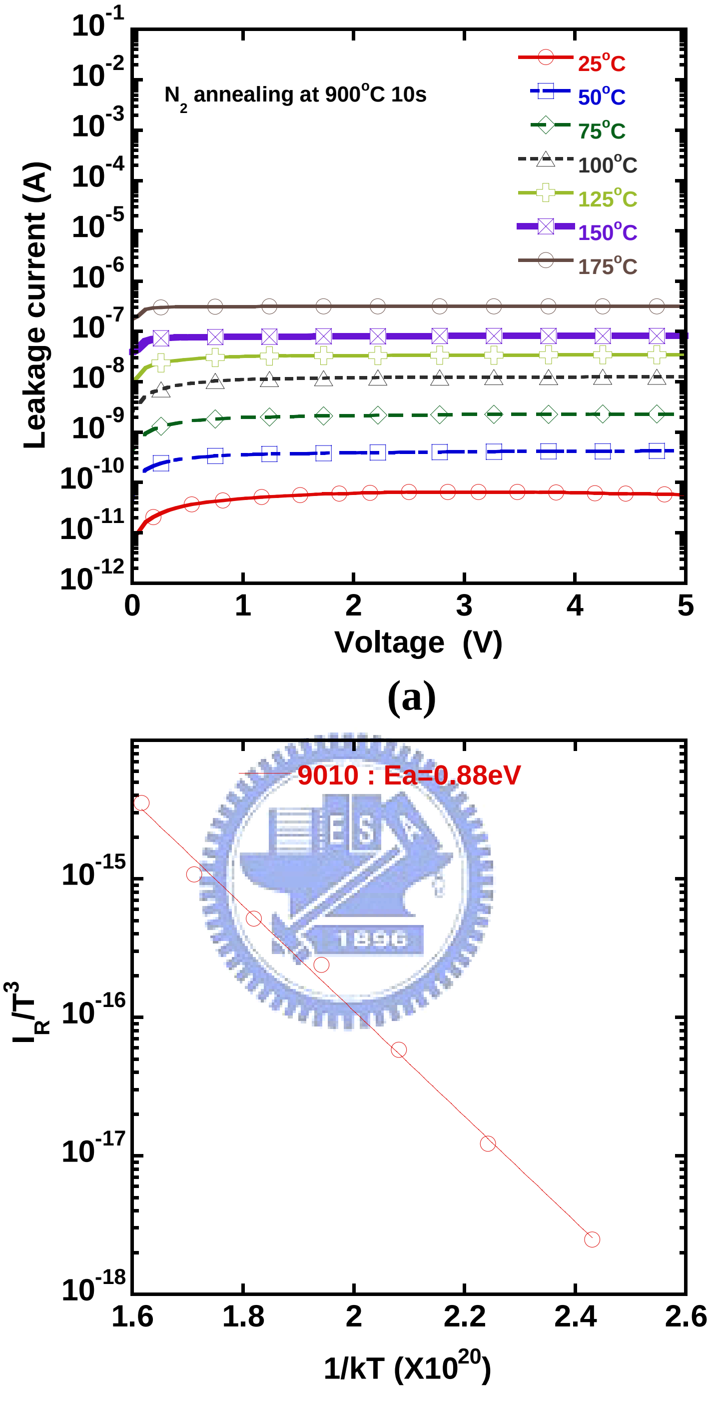


Fig. 4.9 (a) Reverse currrent voltage characteristics measured at various temperatures of the junction with RTA 850°C for 30s. (b) Arrhenius plot (Ln I_R/T^3 versus 1/kT) of junction after RTA at 850°C, 30s measured at -3V.



(a)

(b)

Fig. 4.10 (a) Reverse currrent voltage characteristics measured at various temperatures of the junction with RTA 900°C for 10s. (b) Arrhenius plot (Ln I_R/T^3 versus 1/kT) of junction after RTA at 900°C, 10s measured at -3V.

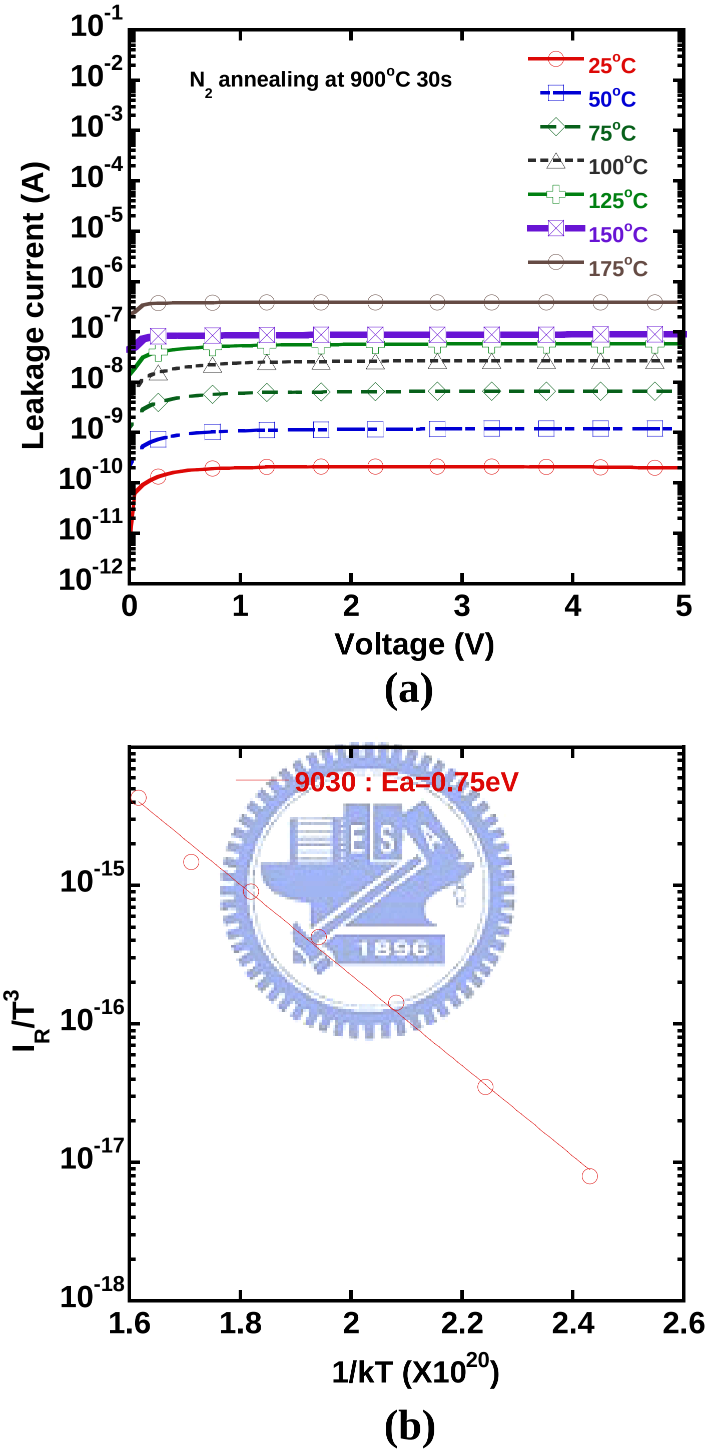
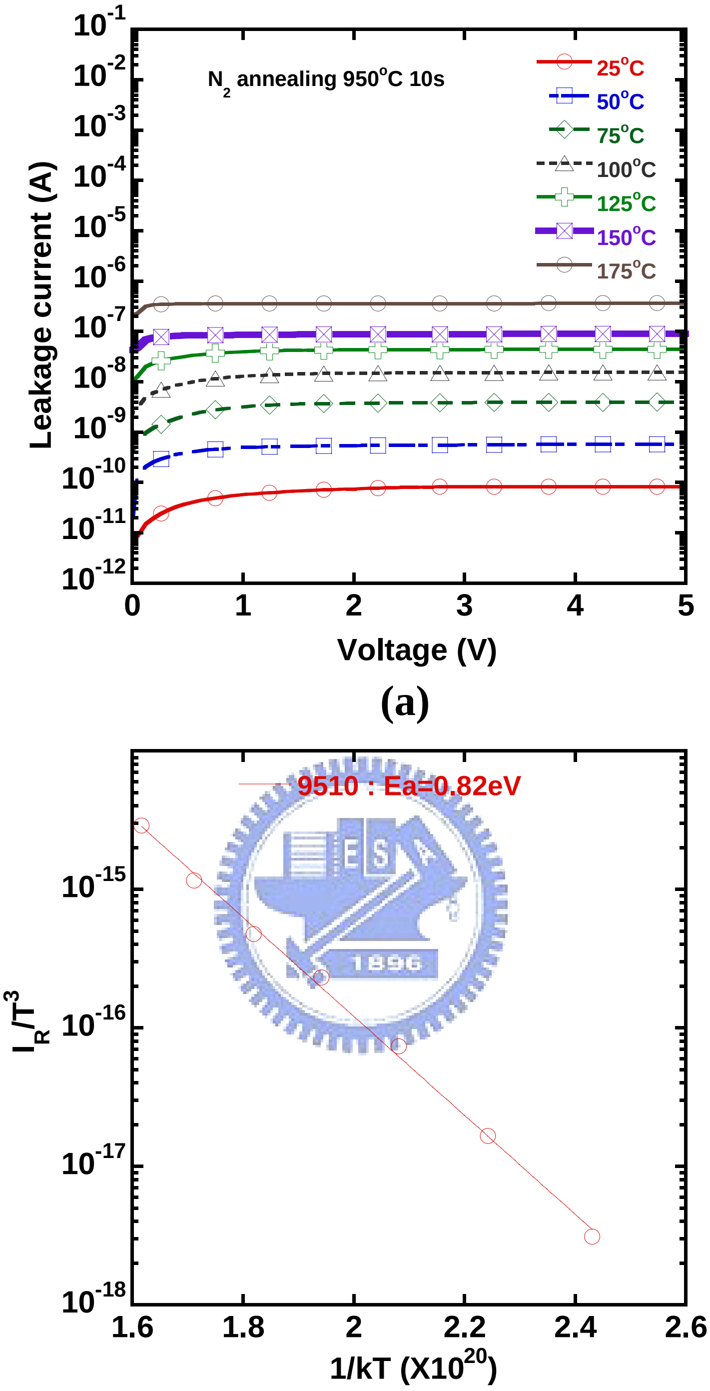


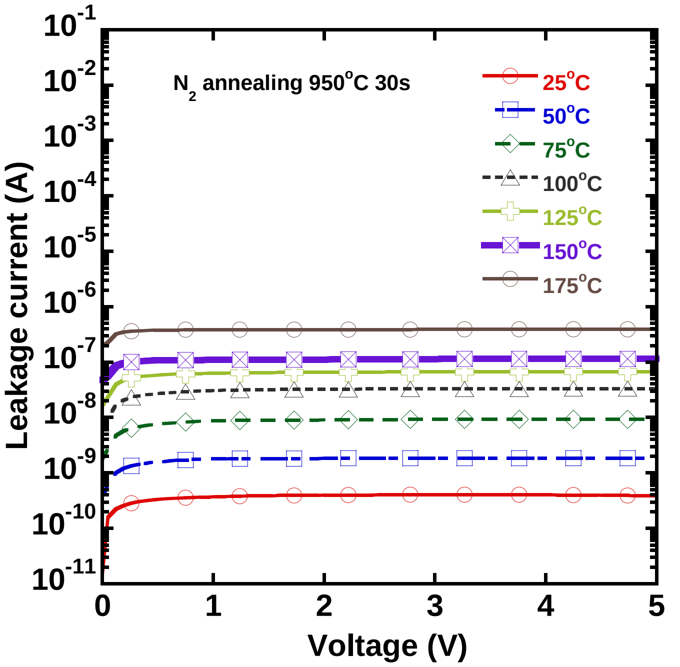
Fig. 4.11 (a) Reverse currrent voltage characteristics measured at various temperatures of the junction with RTA 900°C for 30s. (b) Arrhenius plot (Ln I_R/T^3 versus 1/kT) of junction after RTA at 900°C, 30s measured at -3V.



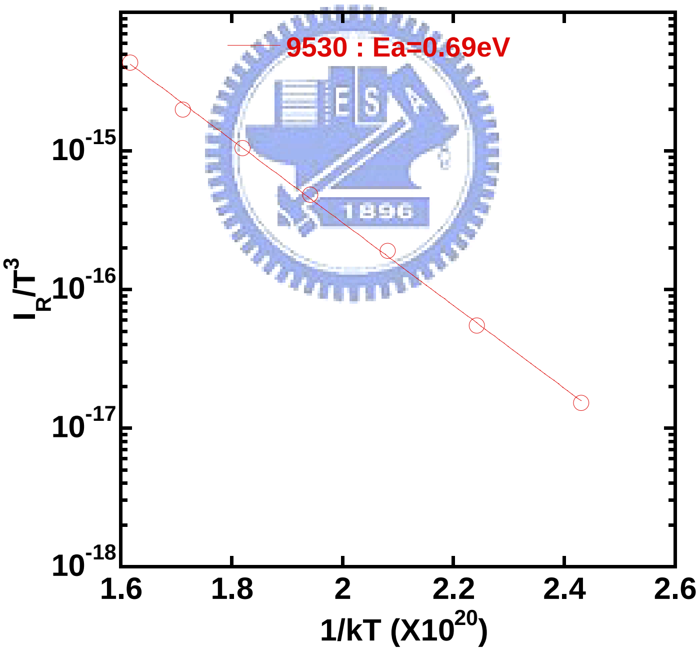
(a)

(b)

Fig. 4.12 (a) Reverse currrent voltage characteristics measured at various temperatures of the junction with RTA 950°C for 10s. (b) Arrhenius plot (Ln I_R/T^3 versus 1/kT) of junction after RTA at 950°C, 10s measured at -3V.

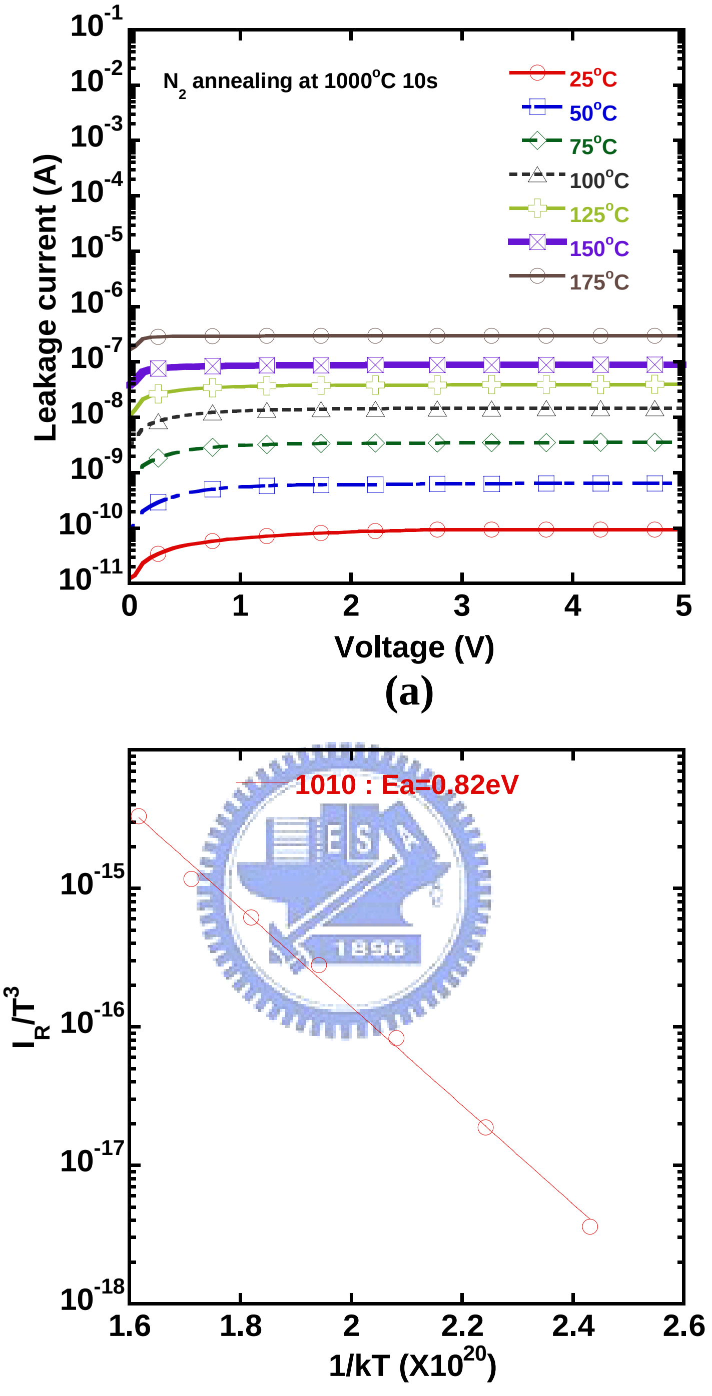


(a)



(b)

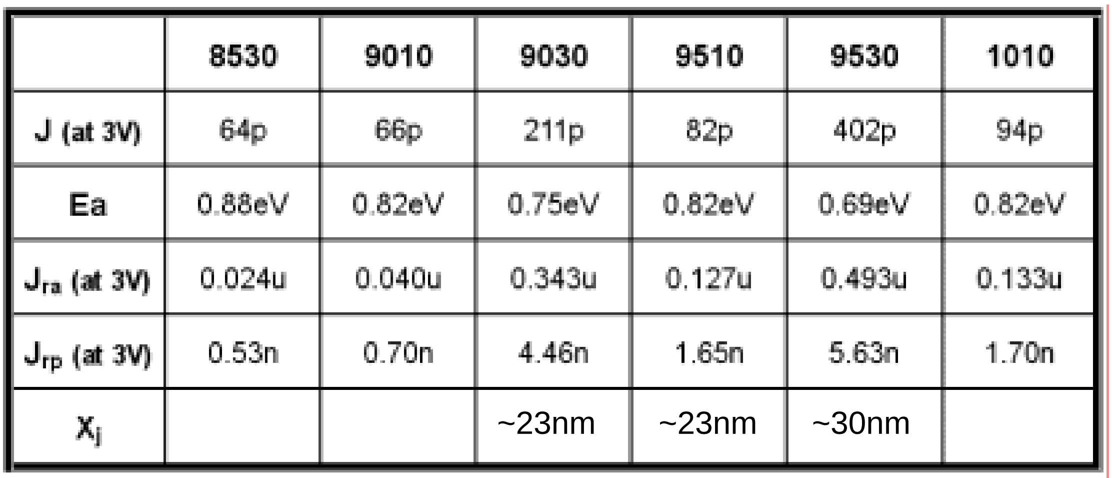
Fig. 4.13 (a) Reverse currrent voltage characteristics measured at various temperatures of the junction with RTA 950°C for 30s. (b) Arrhenius plot (Ln I_R/T^3 versus 1/kT) of junction after RTA at 950°C, 30s measured at -3V.



(a)

(b)

Fig. 4.14 (a) Reverse currrent voltage characteristics measured at various temperatures of the junction with RTA 1000^{o}C for 10s. (b) Arrhenius plot (Ln I_R/T^3 versus 1/kT) of junction after RTA at 1000^{o}C, 10s measured at -3V.



	8530	9010	9030	9510	9530	1010
J (at 3V)	64p	66p	211p	82p	402p	94p
Ea	0.88eV	0.82eV	0.75eV	0.82eV	0.69eV	0.82eV
J_{ra} (at 3V)	0.024u	0.040u	0.343u	0.127u	0.493u	0.133u
J_{rp} (at 3V)	0.53n	0.70n	4.46n	1.65n	5.63n	1.70n
X_j			~23nm	~23nm	~30nm	

Table 4.3 the electrical characteristics of PH_3 plasma doped junction at 50W RF power for 5 minutes with different activation conditions.

Chapter 5

Ultra shallow Junction Combined with Zirconium Capped Nickel Silicide

5.1 Introduction

As MOSFET scaling continues to achieve a dense and high speed integrated circuit, formation an ultra shallow junction is essential for device performance and suppression of short channel effects (SCE) [1], [2]. Along with the device dimensions shrinking, the contact resistance of source and drain is increased correspondingly. Moreover, such resistance deterioration is also encountered in local interconnect. As a result, the technique of metal silicides for poly gate and source/drain has been developed to reduce their contact resistance and the parasitic junction resistance as well [3]. In nanometer MOSFET fabrication, a silicidation process incorporation compatible with the presence of shallow is indispensable. Therefore, how to form a shallow silicided junction without increasing junction leakage is considered as a critical module for the nano-scale CMOS.

Currently, the most widely used metal silicides include $TiSi_2$, $CoSi_2$, and NiSi. For $TiSi_2$, even though it possesses good thermal stability, high silicidation temperature is still required for the phase transformation (from a high-resistivity C49 phase to a low-resistivity C54 phase), thus limiting its use with ultra-shallow junction [4-9]. However, as the line-width below 350nm, the phase transformation from C49 to C54 phase becomes harder because the enlarged silicide grain size is restricted [10], [12]. Beyond the 0.35um technology node, titanium is replaced by cobalt due to its less line-width effect. However, large amount of silicon consumption, rough CoSi2/Si interface, and local spiking of junction will lead to the increase of junction leakage [11], [12], [13]. For ultra-shallow junction, nickel silicide consumes less silicon atoms than cobalt silicide and is believed as a potential candidate for future silicide technologies. In addition, its relatively small film-stress is another merit [14]. Although nickel silicide possesses lower resistivity, lower silicon consumption, only one annealing step, and negligible degradation on narrow line-width, its poor thermal stability must be improved in CMOS process application [15], [16], [24]. Recent studies of nickel silicide have shown that the formation of NiSi is extremely sensitive to interfacial native oxide on silicon surface or oxygen contamination during the silicidation process [10], [17-20]. In last chapter, it was found that the silicide depth can be well controlled by a Zr capping layer upon nickel silicides, and at the same time a smooth interface between silicides and silicon substrate can be maintained [21]. Moreover, thermal stability is dramatically improved by Zr capping. In this chapter, we compare the effect of this Zr cap to the behaviour of a conventional Ti cap layer in terms of the leakage characteristics of ultra-shallow nickel-slilicide junction.

5.2 Experimental

Fig. 5.1 shows the process flow and schematics for the fabrication of n^+/p silicided junction in our experiment. Following a standard Radio Corporation of America (RCA) cleaning process, a 500nm-thick field oxide was thermally grown on the p-type (100) oriented Si wafer with 3-5 Ω-cm at 1050°C for one hour. After isolation oxide formation, the active regions were defined by photolithography and etched by BOE (Buffer oxide etcher) solution. Subsequently, RCA clean was performed for eliminating the contamination. Then, the PH_3 plasma immersion was used to form an n^+/p junction with RF power 50W for 5 minutes. After plasma immersion, rapid thermal annealing (RTA) was carried out to formed n^+/p junctions for 10sec at 950℃ in nitrogen ambient. Then, the samples were loaded into a dual electron-beam evaporation system following a dilute HF dip. A 10nm-thick nickel film was first deposited onto n^+/p junctions at a base pressure of 1×10^{-6} torr with a deposition rate of 1Å/s, and immediately a titanium and zirconium film of about 5nm were sputtered as a capping layer onto the nickel layer respectively. After metal deposition, the silicidation procedure was carried out by the rapid thermal process and the annealing temperature was varied from 550°C to 850°C in N_2 ambient. In order to integrate into the ultra-shallow-junction formation, the silicidation time is shortened to be 10 seconds. Hence, the un-reacted metal was removed by wet etching. Before final metallization, a thin TiN of about 25nm was deposited as a barrier layer. Eventually, aluminum was used for both the front and backside electrode.

Table 5. 1 shows four different groups of samples that were fabricated in this experiment. As reference, non-silicide samples are simple n^+/p

junctions only. The other samples are nickel silicide junction. Among those silicide samples, non-capped NiSi samples and Ti capped on NiSi samples are designed for comparison. And the experimental samples are capped by Zr.

5.3 Results and Discussion

5.3.1 Sheet resistance and SIMS profile of Nickel Silicided Ultra Shallow Junction

Sheet resistances of all samples were examined with a four-point probe. Fig. 5.2 shows the sheet resistance of PH_3 plasma immersion junction with different activation conditions. In order to form low-resistivity junctions, the control sample was activated with RTA condition at 950^{o}C for 10s. Fig. 5.3 shows the SIMS result of the phosphorus profile of PH_3 plasma doping junction after the activation condition of 950ºC for 10s. From this plot, a shallow n^+/p junction formation about 30nm-depth can be demonstrated.

The sheet resistances of those nickel silicided junction are displayed in Fig. 5.4. From Fig. 5.4, the degradation in sheet resistance of non-capped nickel silicide samples may be due to agglomeration and phase transformation from NiSi to $NiSi_2$ at the high annealing temperature as reported in [9], [23]. However, Ti capped and Zr capped on NiSi samples are improved in sheet resistance due to a capping layer, which can suppress the oxidation of silicide films during the RTA process

[10], [16-20]. Especially for Zr capped on NiSi samples, its sheet resistance degradation can be obviously suppressed compared with other cases even after the annealing temperature reached 850ºC.

5.3.2 Characteristics of Ultra Shallow Junction Combined with Nickel Silicide

In addition, the current-voltage characteristics of the PH_3 plasma doped junction is shown in Fig. 5.5 and the junction area size is about 1000╳1000um^2. The reverse leakage current of the silicided junctions were measured using a Hewlett-Packard 4156 semiconductor parameter analyzer. In this figure, it compares the I-V characteristics of nickel silicide and non-silicide n^+/p junctions. Fig. 5.6 shows the cumulative leakage current distribution of all junction samples. From these two plots, the samples with a Zr-cap layer with silicidation condition of 650^{o}C have the smallest leakage current in all silicided n^+/p junctions. Fig. 5.7 is a group of Weibull plots illustrated with the leakage current at reverse bias of 3V for different capping conditions. In Fig. 5.7(a), (b), and (c), all nickel silicide samples exhibit the lowest leakage level at the RTA condition of 650ºC. We have indeed concluded that using a cap layer can avoid the increase of junction leakage and also confine the cumulative leakage distribution within a narrow window of values. These effects are more pronounced for the samples with Zr , that was attributed to the presence of a smooth interface between silicide and substrate [21].

It is well known the leakage current (I_r) in pn junction is composed of two major components including junction area leakage (I_{ra}) and junction periphery leakage (I_{rp}). That is :

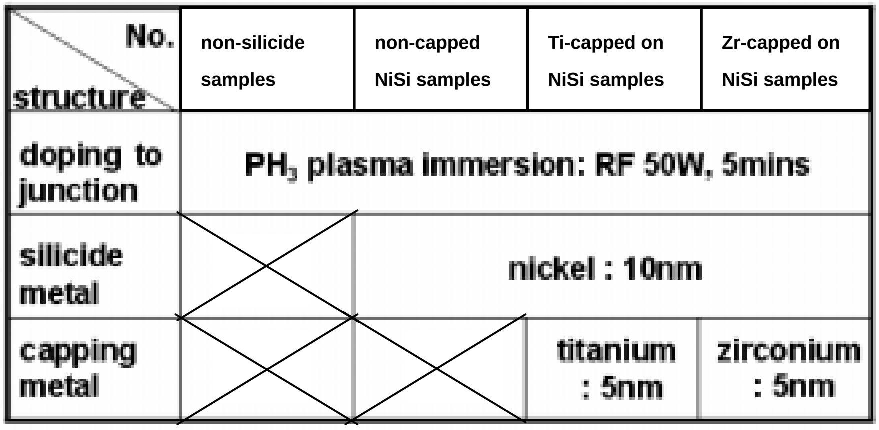
$$I_r = I_{ra} + I_{rp} = J_r(A) = J_{ra}(A) + J_{rp}(P) \qquad (1)$$

$$J_r = J_{ra} + J_{rp}(P/A) \qquad (2)$$

Those two components of leakage current can be separated by the equation (2) [22]. Fig. 5.8(a), (b), and (c) are plots of the leakage current density versus the ratio of junction periphery and area for all silicided samples. The slope stands for the junction periphery leakage density, while the intersection with Y-axis represents the junction area leakage density. The smallest periphery and area leakage could be observed at the annealing temperature of 650ºC in all three groups. Effects of capping conditions on junction leakage from periphery and area are also shown in Fig. 5.9. The samples with a capping structure can remain the leakage level low even after a high RTA temperature. The values of J_{ra} and J_{rp} have been shown in figure 9a and b as a function of T and the cap type to illustrate that junction leakage from area and periphery can be reduced by using a Zr cap.

5.4 Summary

In summery, nickel silicide with a cap layer can achieve better thermal stability and can improve junction leakage characteristics as well. Especially for the Zr cap layer, it can effectively suppress the enormous degradation of NiSi sheet resistance due to the phase transformation after a high annealing temperature (~850^{o}C) and significantly reduce the increase of reverse junction leakage. With this Zr cap layer, low-resistance and smooth-interface nickel silicide can be obtained and integrated into the 30nm ultra-shallow-junction formation.



No. structure	non-silicide samples	non-capped NiSi samples	Ti-capped on NiSi samples	Zr-capped on NiSi samples
doping to junction	PH_3 plasma immersion: RF 50W, 5mins			
silicide metal		nickel : 10nm		
capping metal			titanium : 5nm	zirconium : 5nm

Table 5.1 n^+/p junction formation by PH_3 plasma immersion with and without nickel silicide in different capping conditions. The nickel and the capping layer are about 10nm and 5nm respectively.

○ field oxide isolation : 500nm

○ junction formation : PH_3 plasma doping

○ dopant activation : RTA 950°C, 10s

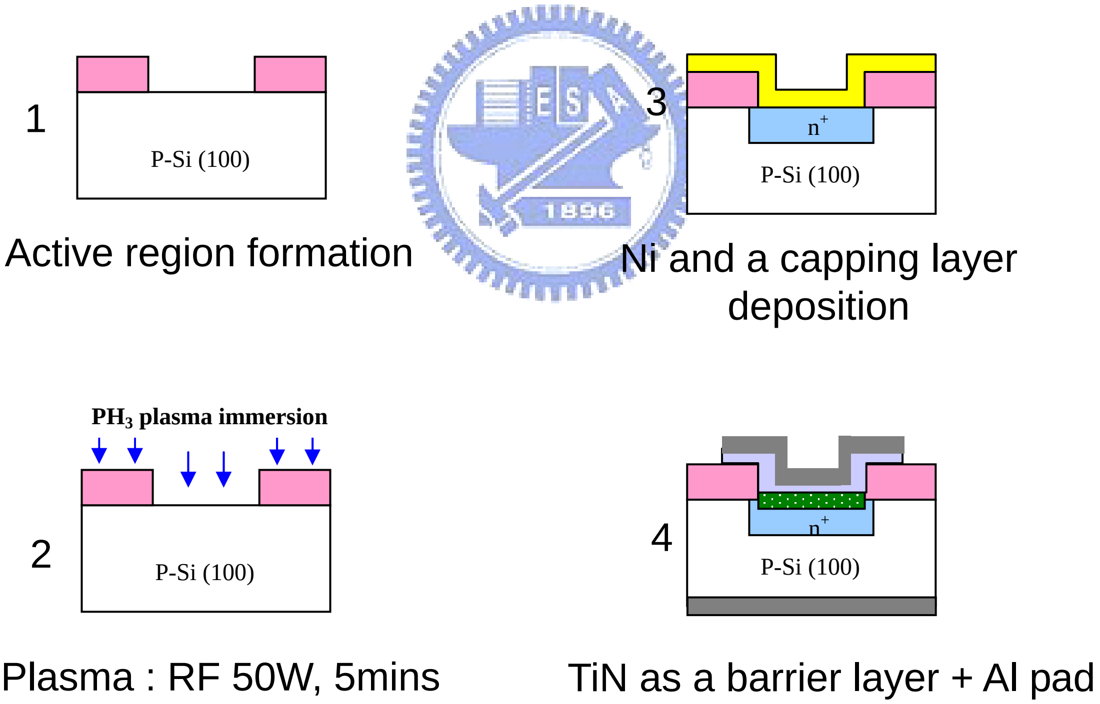
○ metal layer deposition : Ni (10nm)/a cap layer(5nm)

○ silicidation : 550°C~ 850°C

○ stripping off unreacted metal

○ metalization : TiN (25nm) / Al (500nm)

(a)



Active region formation

Ni and a capping layer deposition

Plasma : RF 50W, 5mins

TiN as a barrier layer + Al pad

(b)

Fig. 5. 1 (a) The simple process flow of n^+/p silicided junction formation. (b) The schematics of n^+/p silicided junction fabrication.

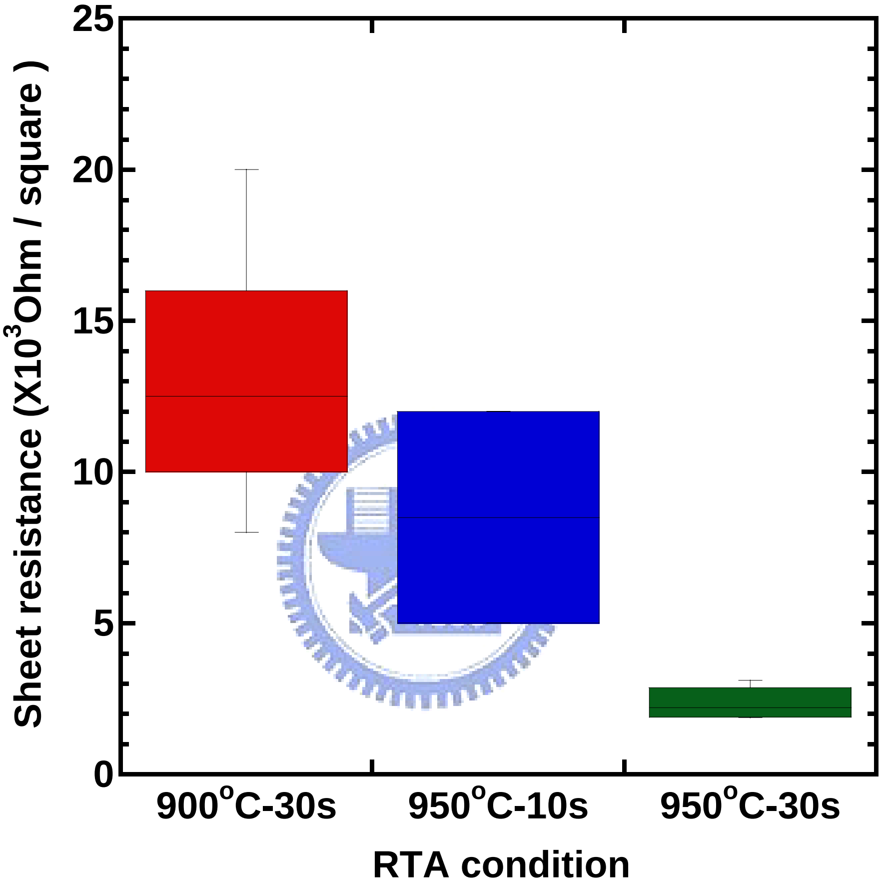


Fig. 5. 2 Sheet resistance versus the annealing temperature for PH_3 plasma junction.

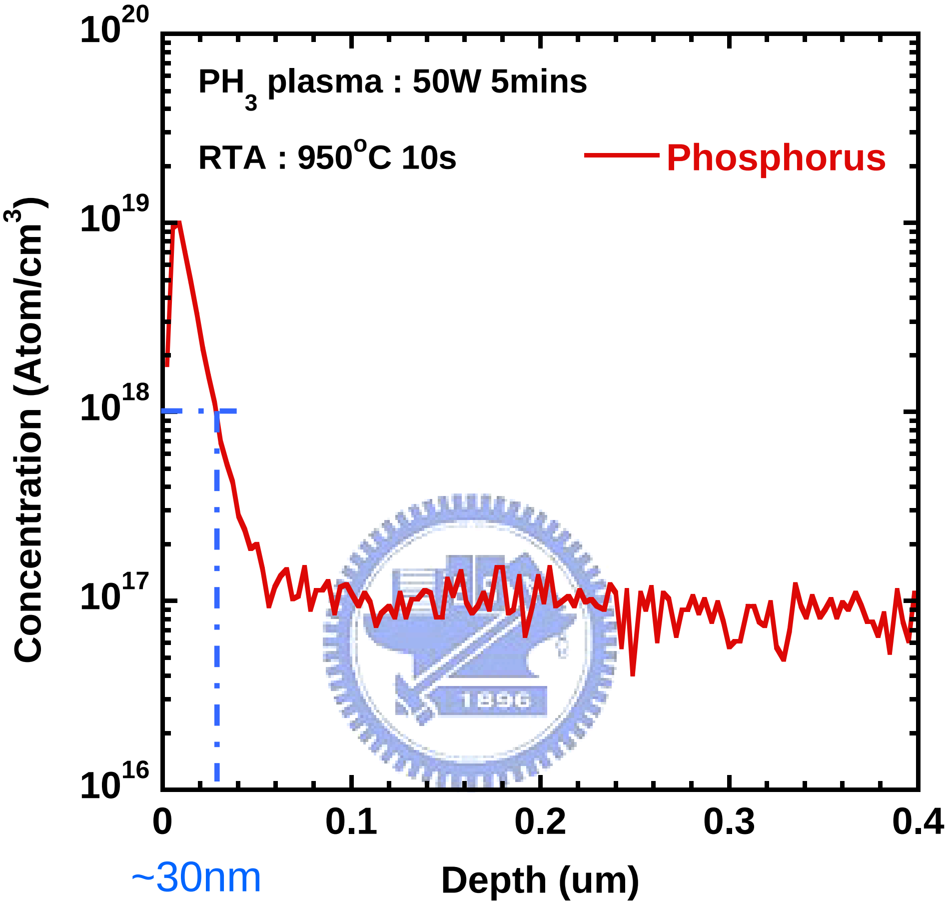


Fig. 5. 3 SIMS profile of n^+/p junction by PH_3 plasma doping. The dopant activation condition is 950°C for 10seconds.

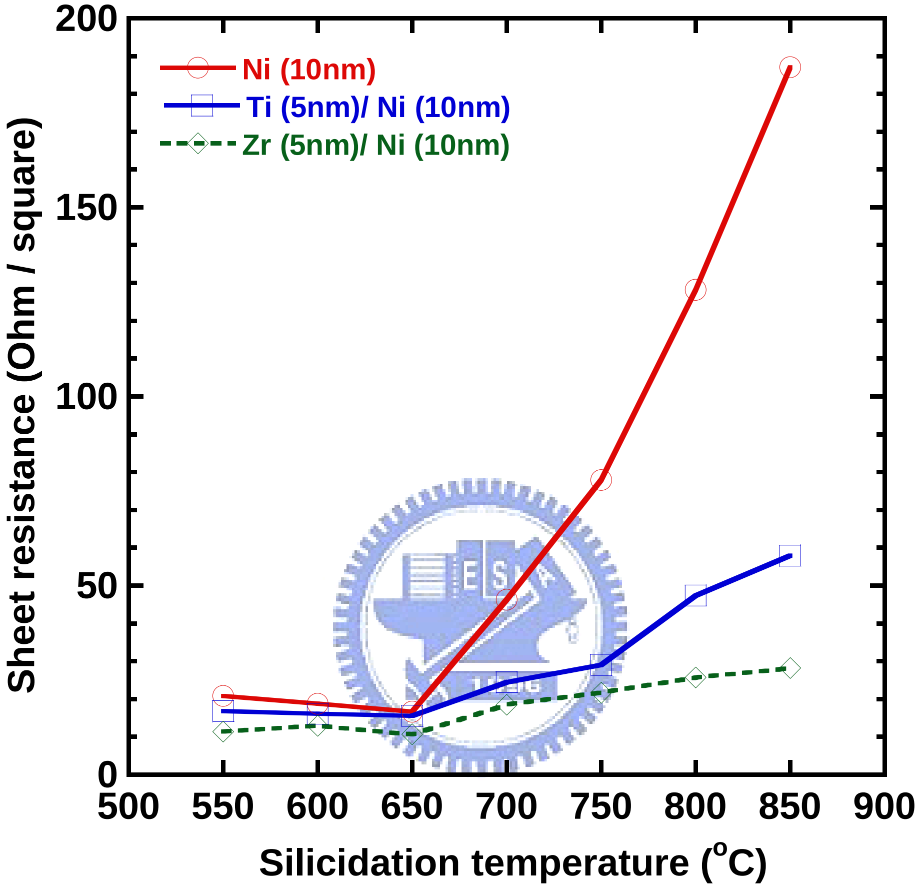


Fig. 5. 4 Sheet resistance versus the silicidation condition for (1) Ni/Si (2) Ti/Ni/Si and (3) Zr/Ni/Si nickel silicide systems.

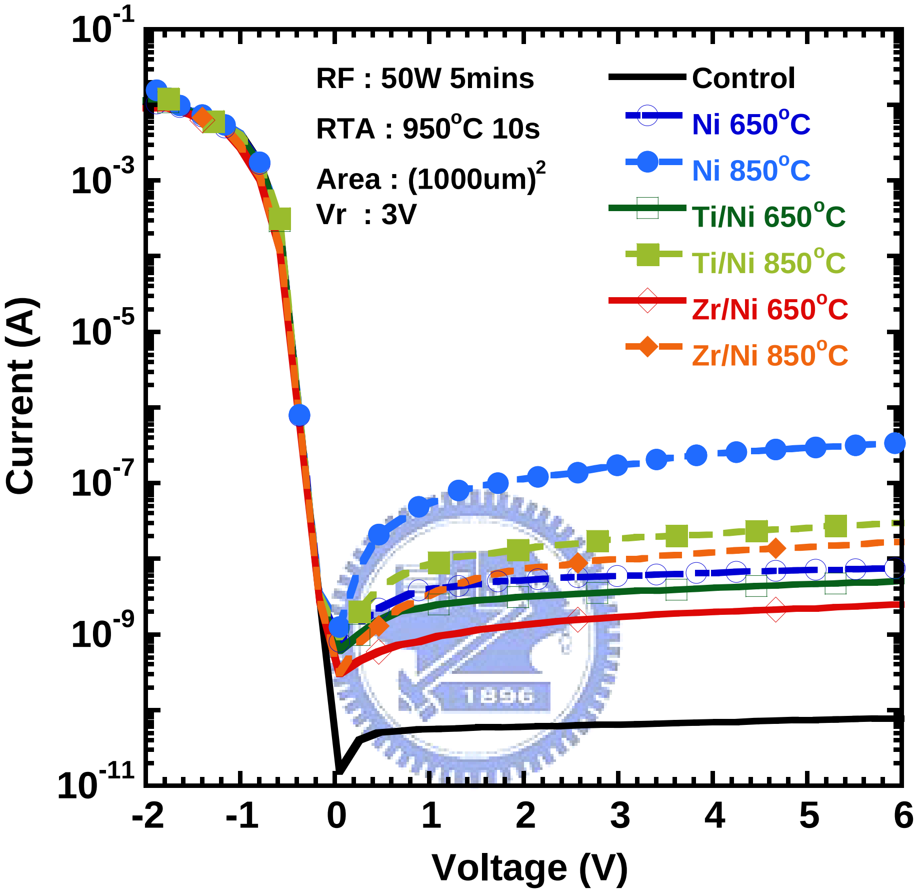


Fig. 5. 5 Reverse current-voltage characteristics of PH_3 plasma junctions with and without nickel silicide.

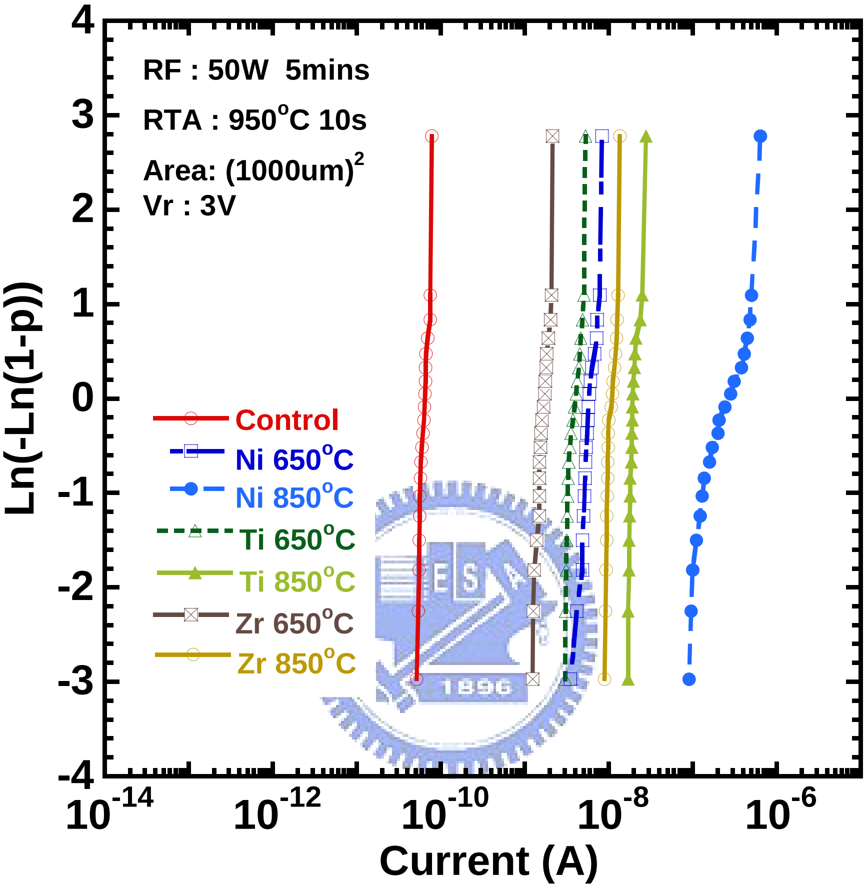
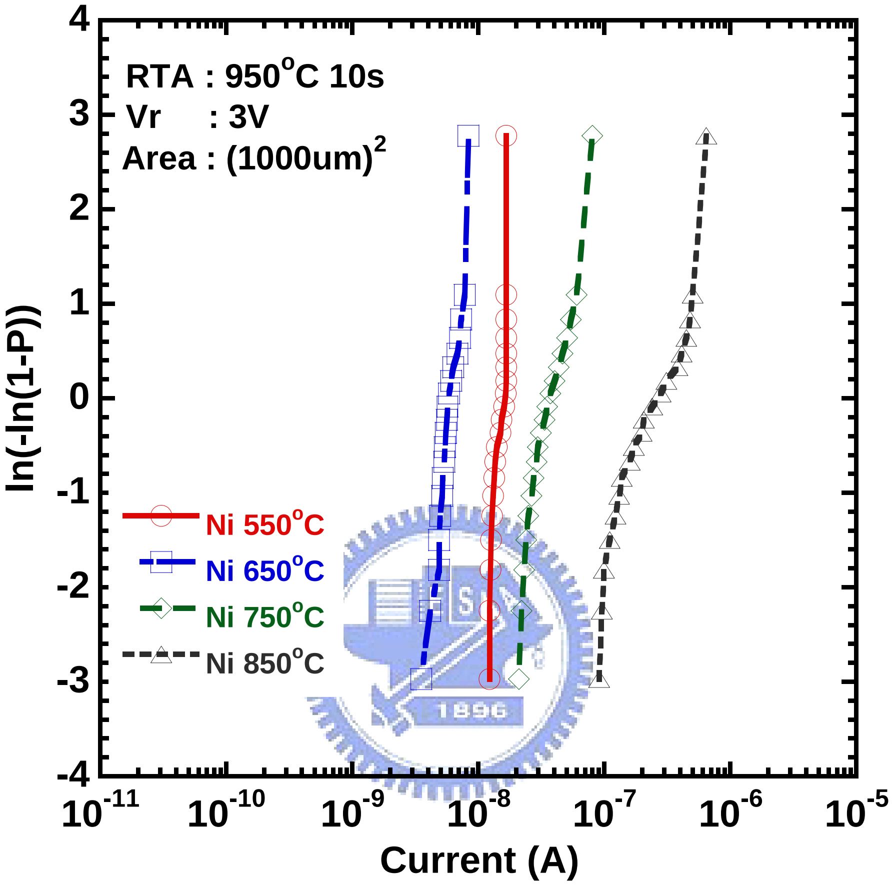
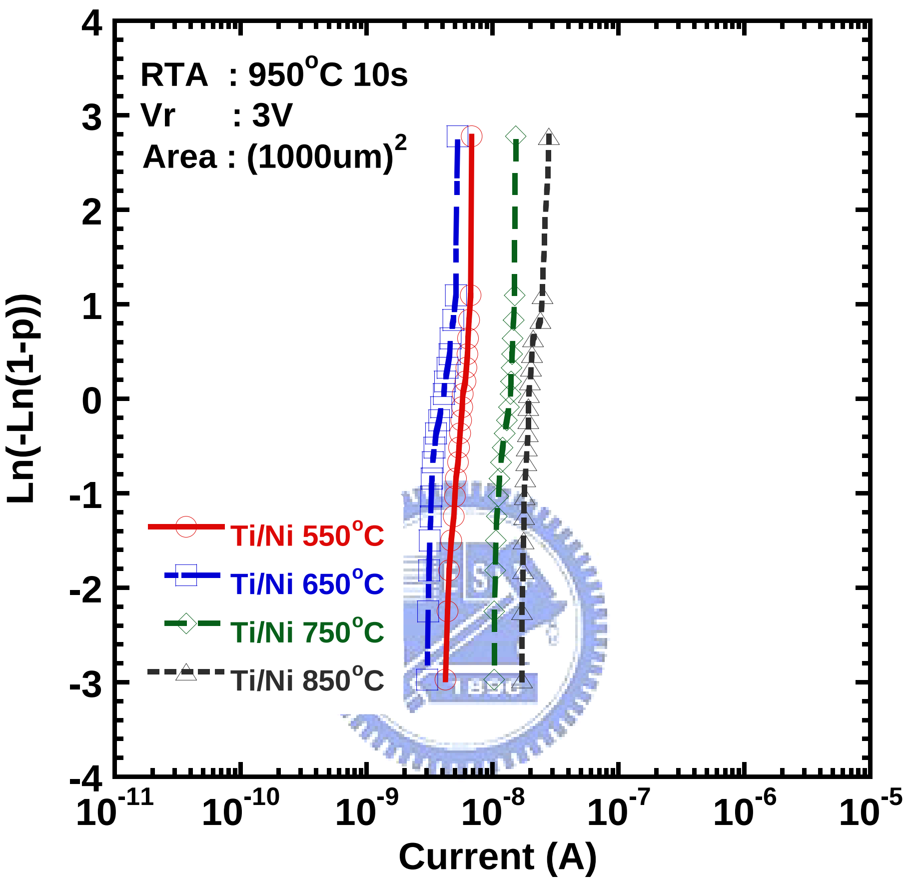


Fig. 5. 6 Weibull plots of the leakage current of all nickel silicide samples at silicidation temperature of 650°C and 850°C respectively. And the size of junction area is 1000×1000μm^2.



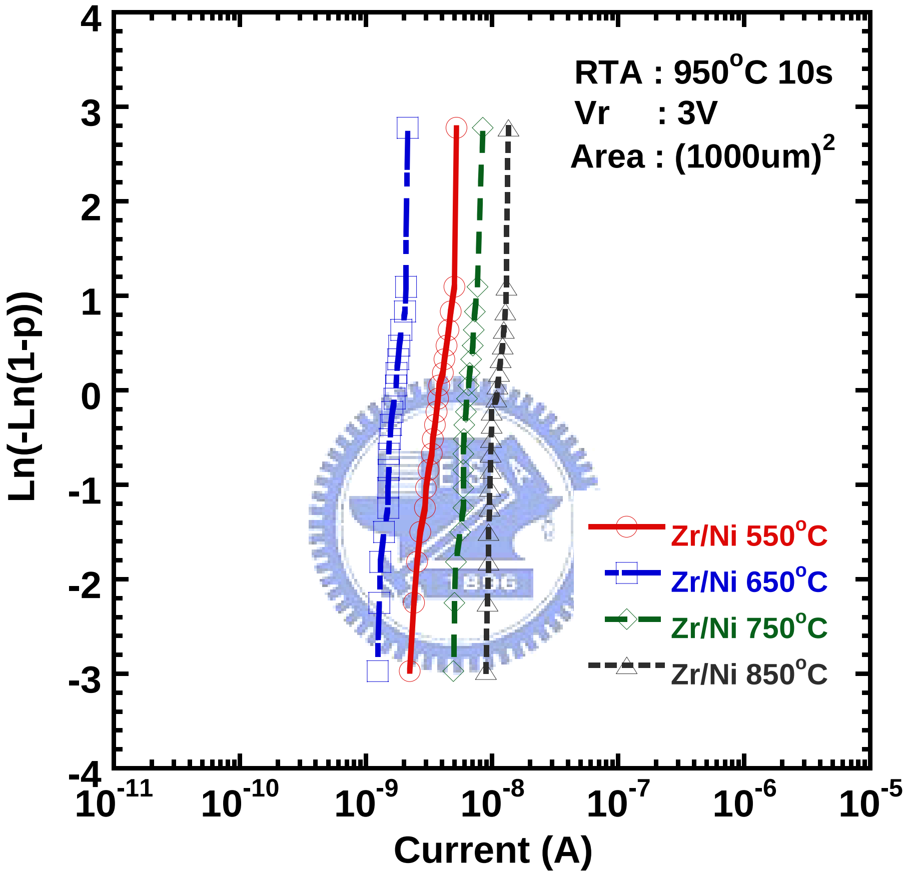
(a)

Fig. 5. 7a (a) Cumulative leakage distribution for simple nickel silicided junction with the annealing temperature various from 550ºC to 850ºC.



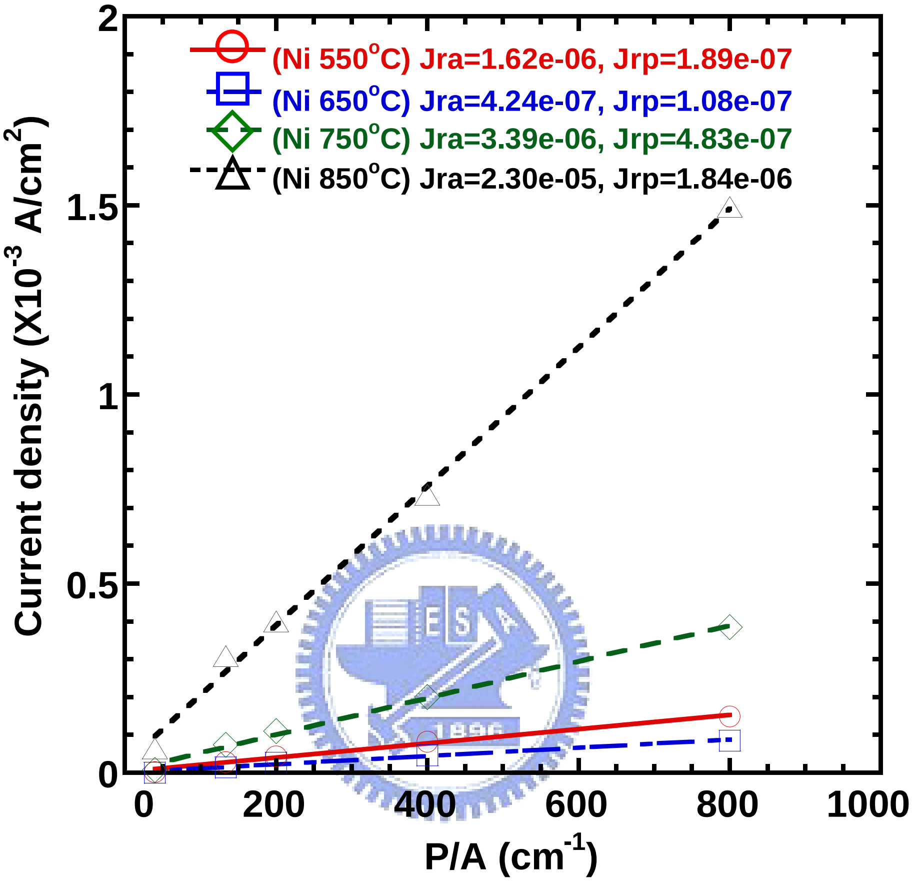
(b)

Fig. 5. 7b (b) The weibull plot of leakage current density for nickel silicided junction with Ti capping after being annealed from 550ºC to 850ºC.



(c)

Fig. 5. 7c (c) Cumulative leakage distribution for Zr capped nickel silicided junction with the annealing temperature various from 550ºC to 850ºC.



(a)

Fig. 5. 8a Comparison of reverse junction leakage current density vs. periphery to area ratio (P/A ratio) for (a) non-capped NiSi samples

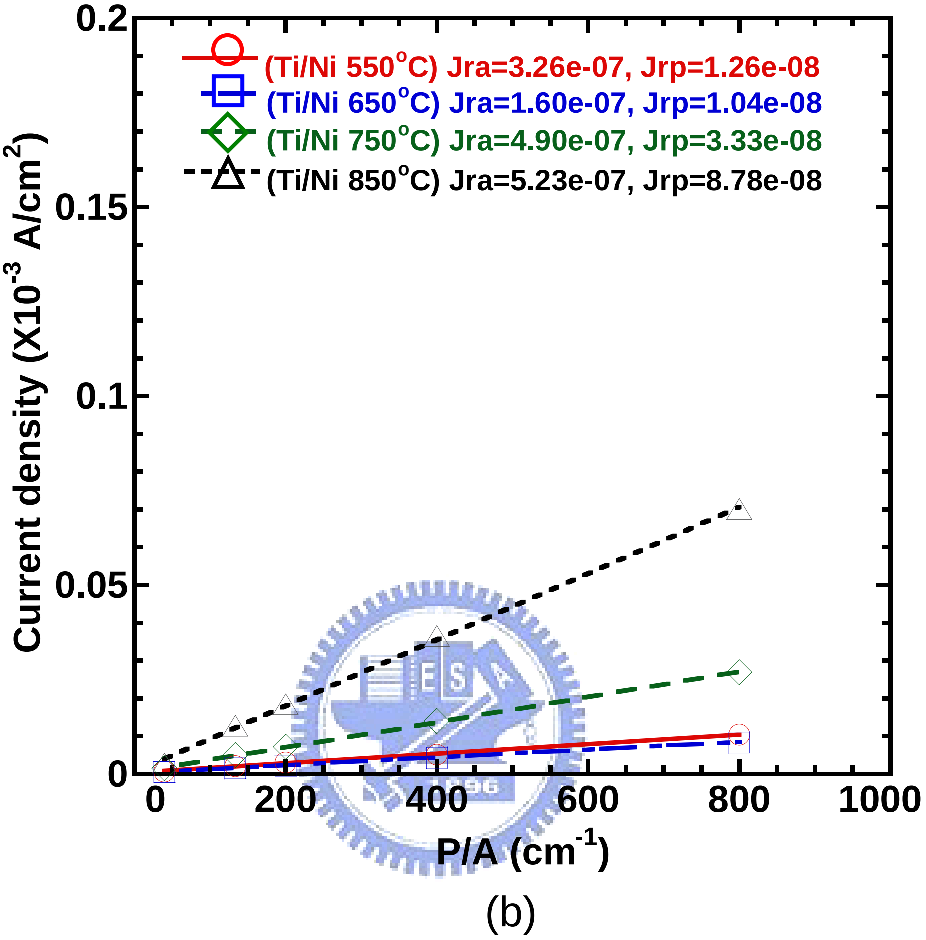
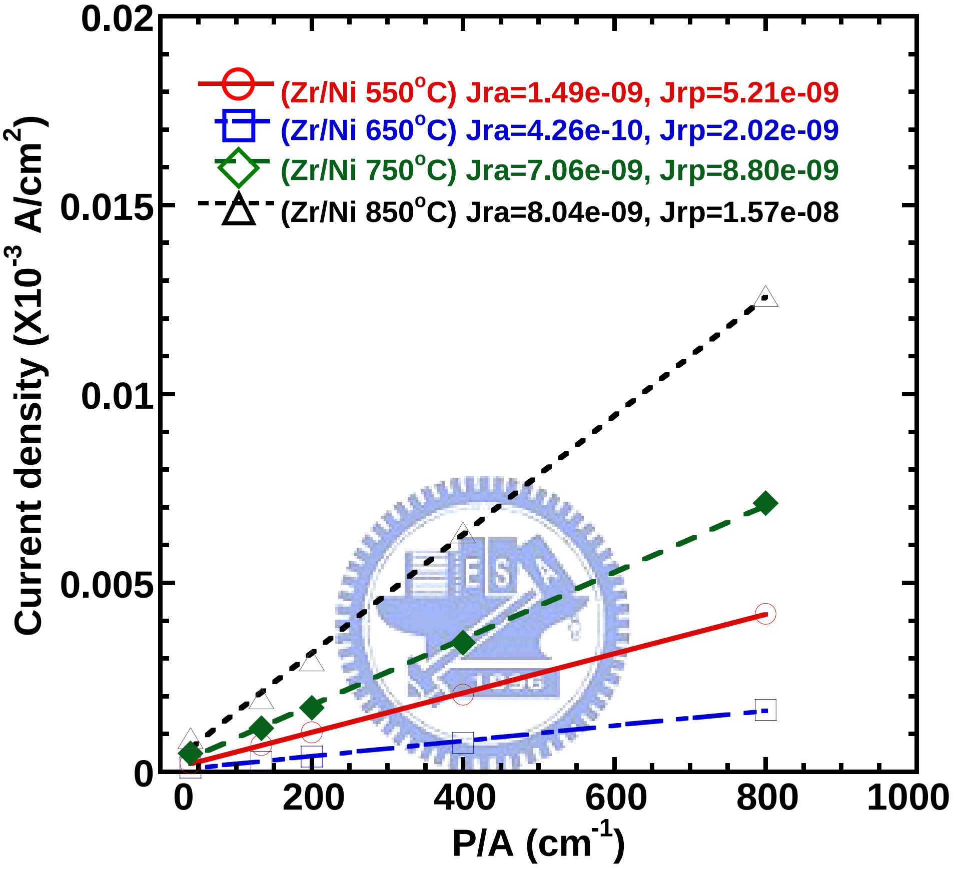
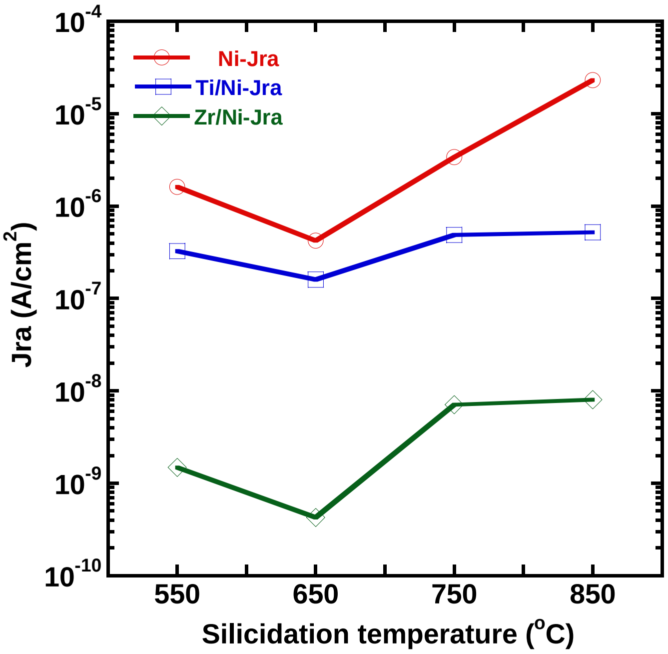


Fig. 5. 8b Comparison of reverse junction leakage current density vs. periphery to area ratio (P/A ratio) for (b) Ti capped on NiSi samples.

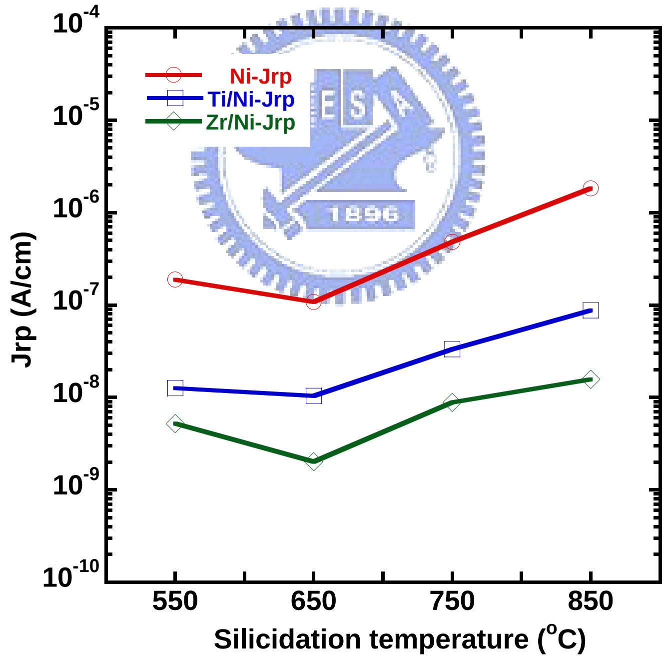


(c)

Fig. 5. 8c Comparison of reverse junction leakage current density vs. periphery to area ratio (P/A ratio) for (c) Zr capped on NiSi samples.



(a)



(b)

Fig. 5. 9 Reverse junction (a) area leakage (b) periphery leakage versus the RTA temperature for all nickel silicide samples in different capping conditions.

Chapter 6

Characteristics of Full Nickel Silicide Gate Based on In-Situ Doped Amorphorus-Si and Amorphorus-Si/Poly-Si Stack Structure

6.1 Introduction

In order to realize high performance sub-quarter-micrometer complementary metal-oxide-semiconductor (CMOS) devices, the reduction of the parasitic resistance of the source/drain and gate is essentially. The self-aligned silicide process has been widely used to satisfy this requirement. On the other hand, the silicide gate which is used to replace poly-silicon gate is investigated extensively such as $TiSi_2$, $CoSi_2$, HfSi, and NiSi have been studied intensively [1-5]. Besides the merit of small sheet resistance, full silicide gate can effectively eliminate the poly-depletion-effect (PDE). Moreover, when high-κ dielectrics are implemented to suppress the gate leakage, poly-silicon loses its thermal stability advantage over metals [6]. In addition, the metal silicide gate provides extra advantages over the metal gate. The damage from metal etching can be avoided due to the self-align silicide process [7].

However, the reliability of the gate oxide with silicide process is needed to take into consideration. In order to form a low-resistance silicide gate, high annealing temperature can't be avoided. This high temperature during silicidation may result in the degradation on the device performance and reliability. Therefore, a suitable material for low thermal-buget silicidation must be taken into account.

NiSi is a potential candidate for the future salicide application because of its low resistivity, one-step annealing, less silicon consumption and non-linewidth effects [8-10]. Furthermore, some reseaches indicated that oxide is a good barrier for nickel diffusion at low temperature [11, 12]. Hence, the characteristics of full nickel-silicide gate capacitors accomplished with a high silicidation temperature were studied. In this chapter, full NiSi gated-MOS capacitors based on different gate structure were fabricated and investigated.

6.2 Experimental

6.2.1 Full Nickel Silicide Gate Based on In-Situ Doped and Undoped a-Si

Full nickel silicide MOS capacitors were fabricated on the <100> p-type silicon wafer. Following the standard RCA clean, silicon wafers were thermally oxidized in diluted dry O_2 ambinet at 800^{o}C to form the gate dielectrics of 35, 50and 75Å by Vertical Furnace system. And 600Å-thick in-situ doped amorphous silicon was deposited immediately in SiH_4+PH_3 ambient at 550^{o}C by the same system. Then, dopant activation was carried out at 900^{o}C for 30 seconds by Heatpulse 610i rapid thermal processing system. Before the deposition of nickel film, all wafers were dipped in a diluted HF solution ($HF/H_2O = 1/100$) to remove the native oxide from the silicon surface and were loaded presently into the Metal PVD system. A 450Å-thick nickel film was deposited on the in-situ doped gate surface at a pressure of $5x10^{-9}$ torr. During the silicidation procedure, all samples were treated at various temperature ranged from 500°C to 800°C in N_2 ambient for 20 seconds by Heatpulse 610 rapid thermal processing system. After that, the unreacted nickel was removed by wet etching ($H_2SO_4/H_2O_2 = 3/1$) and 5000Å-thick aluminum was deposited on the silicide surface of all samples by sputter system. After the front gate electrode was patterned and defined by wet etching (H_3PO_4: HNO_3: CH_3COOH:H_2O = 50:2:10:9 for aluminum etching; HNO_3:NH_4F:H_2O=64:3:33 for silicide etching), 5000Å-thick aluminum was also deposited on the backside of the wafer to form the backside electrode. For comparison, the control sample was fabricated with the same procedure except the nickel deposition and the silicidation process. The other control sample was fabricated based on undoped a-Si. The gate area is $7.85x10^{-5}cm^2$. Key fabrication procedure and schematics of this experimental were shown in Fig. 6.1.

6.2.2 Full Nickel Silicide Gate Based on Stack Structure

Full nickel silicide MOS capacitors were fabricated on the <100> p-type silicon wafer. Following the standard RCA clean, silicon wafers were thermally oxidized in diluted dry O_2 ambinet at 800°C to form the gate dielectrics of 35, 50and 75Å by Vertical Furnace system. Immediately, the stack gate structure were performed in the same system:

(1) 300Å n^+ amorphous silicon / 300 Å undoped polysilicon / SiO_2

(2) 300Å undoped poly silicon /300 Å n^+ amorphous silicon / SiO_2

Dopant activation was accomplished by Heatpulse 610i rapid thermal processing system for 30 seconds in N_2 ambient at 900°C. Before the deposition of nickel film, all wafers were dipped in a diluted HF solution ($HF/H_2O = 1/100$) to remove the native oxide from the silicon surface and were loaded presently into the Metal PVD system. 450Å-thick nickel was deposited on the stack gate surface at a pressure of $5x10^{-9}$ torr. During the silicidation procedure, all samples were treated at various temperature ranged from 500°C to 800°C in N_2 ambient for 20 seconds by Heatpulse 610 rapid thermal processing system. After that, the unreacted nickel was removed by wet etching ($H_2SO_4/H_2O_2 = 3/1$) and 5000Å-thick aluminum was deposited on the silicide surface of all samples by sputter system. After the front gate electrode was patterned and defined by wet etching (H_3PO_4: HNO_3: CH_3COOH:H_2O = 50:2:10:9 for aluminum etching; HNO_3:NH_4F:H_2O=64:3:33 for silicide etching), 5000Å-thick aluminum was also deposited on the backside of the wafer to form the backside electrode. The gate area is $7.85x10^{-5}cm^2$. Key fabrication procedure and schematics of this experimental were shown in Fig. 6.12.

6.2.3 Full Nickel Silicide Gate Based on In-Situ Doped a-Si with Zr Capping

Full nickel silicide MOS capacitors were fabricated on the <100> p-type silicon wafer. Following the standard RCA clean, silicon wafers were thermally oxidized in diluted dry O_2 ambinet at 800^{o}C to form the gate dielectrics of 35, 50and 75Å by Vertical Furnace system. And 600Å-thick in-situ doped amorphous silicon was deposited immediately in SiH_4+PH_3 ambient at 550^{o}C by the same system. Then, dopant activation was carried out at 900^{o}C for 30 seconds by Heatpulse 610i rapid thermal processing system. Before the deposition of nickel film, all wafers were dipped in a diluted HF solution (HF/H_2O = 1/100) to remove the native oxide from the silicon surface and were loaded presently into dual electron gun system. 450Å-thick nickel and 100Å-thick Zirconium were deposited before and after on the in-situ doped gate surface at a pressure of 1x10^{-6} torr. During the silicidation procedure, all samples were treated at various temperature ranged from 500^{o}C to 800^{o}C in N_2 ambient for 20 seconds by Heatpulse 610 rapid thermal processing system. After that, the unreacted nickel was removed by wet etching (H_2SO_4/H_2O_2 = 3/1) and 5000Å-thick aluminum was deposited on the silicide surface of all samples by sputter system. After the front gate electrode was patterned and defined by wet etching (H_3PO_4: HNO_3: CH_3COOH:H_2O = 50:2:10:9 for aluminum etching; HNO_3:NH_4F:H_2O=64:3:33 for silicide etching), 5000Å-thick aluminum was also deposited on the backside of the wafer to form the backside electrode. The gate area is $5.024 \times 10^{-3} cm^2$. Key fabrication procedure and schematics of this experimental were shown in Fig. 6.19.

The physical thicknesses of oxide and the thickness of all MOS capacitors were measured by N&K analyzer. The Sheet resistance (R_s) of nickel silicide was obtained by four-point-probe analyzer. Electrical characteristics of all MOS capacitors were measured by using Hewlett-Packard 4156B (HP-4156B) semiconductor parameter analyzer. HP4284 LCR meter was used the measurement of the CV characteristics at 100K Hz.

6.3 Results and Discussion

6.3.1 Characteristics of Full Nickel Silicide Gate Based on In-Situ Doped and Undoped a-Si

The sheet resistance of the undoped-NiSi (A) and in-situ doped NiSi (IA) samples with different silicidation temperature is shown in Fig. 6.2. In this figure, the sheet resistance of all samples remains low even after high temperature annealing (<5Ω/□). And the sheet resistance of the in-situ doped a-Si without silicide is about~140 Ω/□ which is very larger than the sheet resistance of in-situ doped a-Si with nickel silicide.

Fig. 6.3a and b show the transmission electron microscopy (TEM) images of full nickel silicide gate capacitor based on undoped a-Si with silicidation temperature at 500°C and 800°C, respectively. The oxide thickness is about 38Å and the thickness of NiSi on undoped a-Si film increases with the silicidation temperature. Besides, the nickel silicide on undoped a-Si becomes more uniform as the RTA condition reached 800^{o}C. Fig. 6.4a shows the TEM image of in-situ doped a-Si (IA) gate capacitor without silicidation, and the thickness of a-Si and silicon dioxide are about 595Å and 38.1Å. Fig. 6.4b and c are the TEM images of full nickel silicide n^{+} a-Si (IA) with RTA 500^{o}C and 800^{o}C, respectively. In Fig. 6.4b, the thickness of NiSi is about 726Å and some residues of silicon without reaction with nickel near the interface of can be observed. However, Fig. 6.4c reveals no silicon residues near the n^{+} a-Si and SiO$_2$ interface after RTA 800^{o}C and proves a nuiform NiSi film formation (750Å).

Fig. 6.5a shows the SIMS profile of nickel silicide gate capacitors on undoped a-Si with RTA 800^{o}C. From this figure, the ratio of Si and nickel in the whole gate region is about 1:1, it also can be concluded that there is no silicon residues near the n^{+} a-Si and SiO$_2$ interface. Fig. 6.5b is the SIMS profile of the in-situ doped a-Si gate capacitors without nickel silicide. The uniform distribution of dopant (P) in n^{+} a-Si region can be obtained after dopant activation at RTA 900^{o}C for 30s. And Fig. 6.5c and d are the SIMS profiles of n^{+} a-Si gate capacitors with silicidation temperature of 500^{o}C and 800^{o}C, respectively. A large amount of dopant (p) is accumulated near the SiO$_2$, in the meanwhile, diffusion of nickel will be retarded slightly (Fig. 6.5c). However, after the RTA temperature is reached 800^{o}C, the phenomenon of the dopant accumulation near the SiO$_2$ will be suppressed and most of dopant will be piled up to the surface of nickel silicide gate. The uniform distribution of nickel in the whole a-Si region can be observed at this RTA condition.

Fig. 6.6a and b are the high frequence CV plot and gate leakage versus gate voltage plot of undoped a-Si gate capacitors with 50Å-thick oxide. Table 6.1a, b and c exhibit some parameters (EOT, V_{FB}, E_{BD}, and $\Phi_{B.}$) of undoped a-Si gate samples with 35, 50 and 75Å-thick oxide, respectively.

The effective barrier height could be deduced from the Fowler-Nordheim tunneling equation. We use the J-E curve in the accumulation region to extract the electron barrier height from nickel silicide to the oxide and use the J-E curve in the inversion region by the illumination of light to extract the electron barrier height from the silicon substrate to the oxide. Based on the F-N tunneling model:

$$J=AE_{OX}^{2}\exp(-B/E_{OX}) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 1$$

$$\ln(J/E_{OX}^{2})=\ln A-B/E_{OX} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 2$$

where J = gate current density (A/cm^2)

E = electric field of oxide (MV/cm)

$A = m_0 q^3/(16\pi^2 \hbar m^* \Phi_B) \sim 3.471\times10^{-6}\Phi_B^{-1}$ (for $m^* = 0.47m_0$)

$B = 4(2m^*)^{1/2}(q\Phi_B)^{3/2}/(3q\hbar) \sim 46.8\Phi_B^{3/2}$ (for $m^* = 0.47m_0$)

From the plot of J/E_{OX}^2 versus $1/E_{OX}$ plot, the slope (B) gives the tunneling barrier height (Φ_B).

Fig. 6.7 is the X-ray diffraction sepctra (XRD) of the nickel silicide gate capacitors based on in-situ doped a-Si with silicidation temperature ranged from 500^{o}C to 800^{o}C. From this figure, there is no obvious phase transformation of nickel silicide with vaious RTA conditions. This result can explain why no obvious sheet resistance degradation of NiSi after high temperature annealing occurred in Fig. 6.2.

Fig. 6.8a, c and e are the CV plots of nickel silicide n^+ a-Si gate samples of 35, 50 and 75Å-thick oxide. And Fig. 6.8b, d and e are the IV characteristics of nickel silicide n^+ a-Si gate samples with 35, 50 and 75Å-thick oxide, respectively. In these CV plots, the V_{FB} shift from 500 to 800^{o}C might result from a) the residues of silicon without reacting with nickel near the interface of gate and SiO_2 (the results of TEM images). b) dopant (p) reaction with nickel near the interface of gate and SiO_2 (the results from SIMS analysis). In summary, most of the electrical characteristics (EOT, V_{FB}, E_{BD}, and $\Phi_{B.}$) are extracted and listed in Table. 6.2.

6.3.2 Characteristics of Full Nickel Silicide Gate Based on Stack Structure

The sheet resistance of in-situ doped a-Si / undoped p-Si stack (AP) and undoped p-Si / in-situ doped a-Si stack (PA) samples with different silicidation temperature are shown in Fig. 6.10a and b, respectively. In these two figures, the sheet resistance of all samples remains low even after high temperature annealing (<5Ω/□). And the sheet resistance of AP and PA structure without silicide are about~780 Ω/□ and 540Ω/□, respectively. Fig. 6.11a, shows the transmission electron microscopy (TEM) image of n^+ a-Si/p-Si stack (AP) gate capacitors without silicidation and the thickness of nickel film, n^+ a-Si, p-Si and silicon dioxide are about 447Å, 282Å, 353Å and 39Å, respectively. In Fig. 6.11b, most of the silicon has reacted with nickel to form NiSi but there were silicon residues near the poly-Si/SiO_2 interface. However, after the 800°C silicidation, nickel has consumed all silicon as shown in Fig. 6.11c, and the NiSi film is more uniform than that treated by 500°C annealing. For p-Si/n^+ a-Si (PA) stack structure, the thickness of nickel film, p-Si, n^+ a-Si and silicon dioxide are about 450Å, 270Å, 360Å and 41.5Å, respectively (Fig. 6.12a). As shown in Fig. 6.12b, some residual silicon also can be observed near the interface of gate and SiO_2, but samples treated with 800°C annealing possesses a uniform NiSi film on the oxide surface (Fig. 6.12c). The higher annealing temperature is treated, the more uniform NiSi film is formed.

Fig. 6.13a and b show the SIMS profiles of AP stack gate capacitors with RTA 500°C and 800°C, respectively, and the SIMS profiles of PA stack gate samples are displayed in Fig. 6.13c and d. A amount of dopant (p) is accumulated at the interface of n^+ a-Si/p-Si and interface of gate/SiO_2 in both AP and PA structures with RTA 500°C, in the meanwhile, diffusion of nickel will be retarded slightly (Fig. 6.13a and c). However, after the RTA temperature is reached 800°C, the phenomenon of the dopant accumulation near the SiO_2 will be suppressed and most of dopant will be piled up to the surface of nickel silicide gate. The uniform distribution of nickel in the whole a-Si region can be observed at this RTA condition (Fig. 6.13b and d).

Fig. 6.14a, c and e are the CV plots of nickel silicide n^+ a-Si/p-Si gate samples of 35, 50 and 75Å-thick oxide. And Fig. 6.14b, d and f are the IV characteristics of nickel silicide n^+ a-Si/p-Si gate samples with 35, 50 and 75Å-thick oxide, respectively. Fig. 6.15a, c and e are the CV plots of nickel silicide p-Si/n^+ a-Si gate samples of 35, 50 and 75Å-thick oxide. Fig. 6.15b, d and f are the IV characteristics of nickel silicide p-Si/n^+ a-Si gate samples with 35, 50 and 75Å-thick oxide, respectively. Compared with AP and PA stack gate structure, it should be a relative large amount of p exists near the interface of gate and SiO_2 and to be a barrier against the nickel diffusion in PA stack structure, that may be the reason why PA stack structure is possessed of better electrical characteristics than AP stack structure. The electrical characteristics (EOT, V_{FB}, E_{BD}, and $\Phi_{B.}$) of AP and PA stack structure are extracted and listed in Table 6.3 and Table 6.4, respectively.

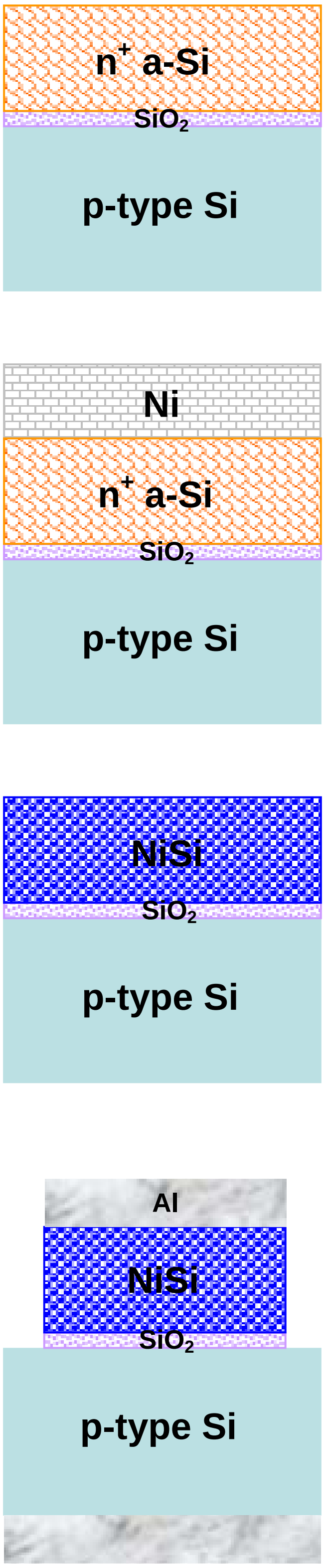
6.3.3 Characteristics of Full Nickel Silicide Gate Based on In-Situ Doped a-Si with Zr Capping

The sheet resistance of nickel silicide gate capacitors on in-situ doped a-Si with and without Zr capping (IA-Z) at different silicidation temperature is shown in Fig. 6.17. The variance in sheet resistance for two different structure samples is the same.

Fig. 6.18a, c and e are the CV plots of nickel silicide n^+ a-Si gate samples with Zr capping of 35, 50 and 75Å-thick oxide. And Fig. 6.18b, d and e are the IV characteristics of nickel silicide n^+ a-Si gate samples with Zr capping of 35, 50 and 75Å-thick oxide, respectively. Table 6.5 lists the electrical characteristics (EOT, V_{FB}, E_{BD}, and $\Phi_{B.}$) for nickel silicide n^+ a-Si gate samples with Zr capping of different oxide thickness. Table 6.6 compares IA, IA-Z, AP and PA samples with RTA at 500°C and 800°C. The small V_{FB} can be obtained by Zr capping and with a higher silicidation temperature. And samples with Zr capping can obtain a low leakage level compared with other structures. That may be due to its higher electron barrier height and a smoother interface between gate and oxide as-mentioned in chapter 2. We believed that the Zr cap layer will enhance the gate oxide reliability.

6.4 Summary

In this chaper, we investigated full nickel silicide gate capacitor with different gate structure. After 800°C silicidation, the degradation on gate leakage and oxide breakdown is apparent. By in-situ doped method, in low annealing temperature, dopant accumulates near the interface of gate/SiO_2 and retards the excess nickel diffusion. After high temperature silicidation, phosphorus may react with nickel and Si, and then enhances the reliability of full nickel silicide devices. The stack structure can't effectively suppress the excess nickel diffusion by extra grain boundary at the n^+ a-Si / p-Si interface as expected. However, phosphorus in stack gate structure still plays a role as in n^+ a-Si gate structure, and restrains the degradation of gate oxide by a high silicidation process. Besides, a slight degradation on device reliability will be observed owing to the less phosphorus concentration in stack gate structure compared with n^+ a-Si gate structure. Adding a Zr cap, the gate leakage can be supressed by retarding the excess nickel diffusion and the oxide reliability also can be enhanced owing to above mentioned advantages of Zr capping on NiSi. In conclusion, by phosphorus incorporation ,the gate oxide reliability can be enhanced. Combined it with Zr capping method, the full nickel silicide gate structure will become feasible for nano-scale MOS device application.



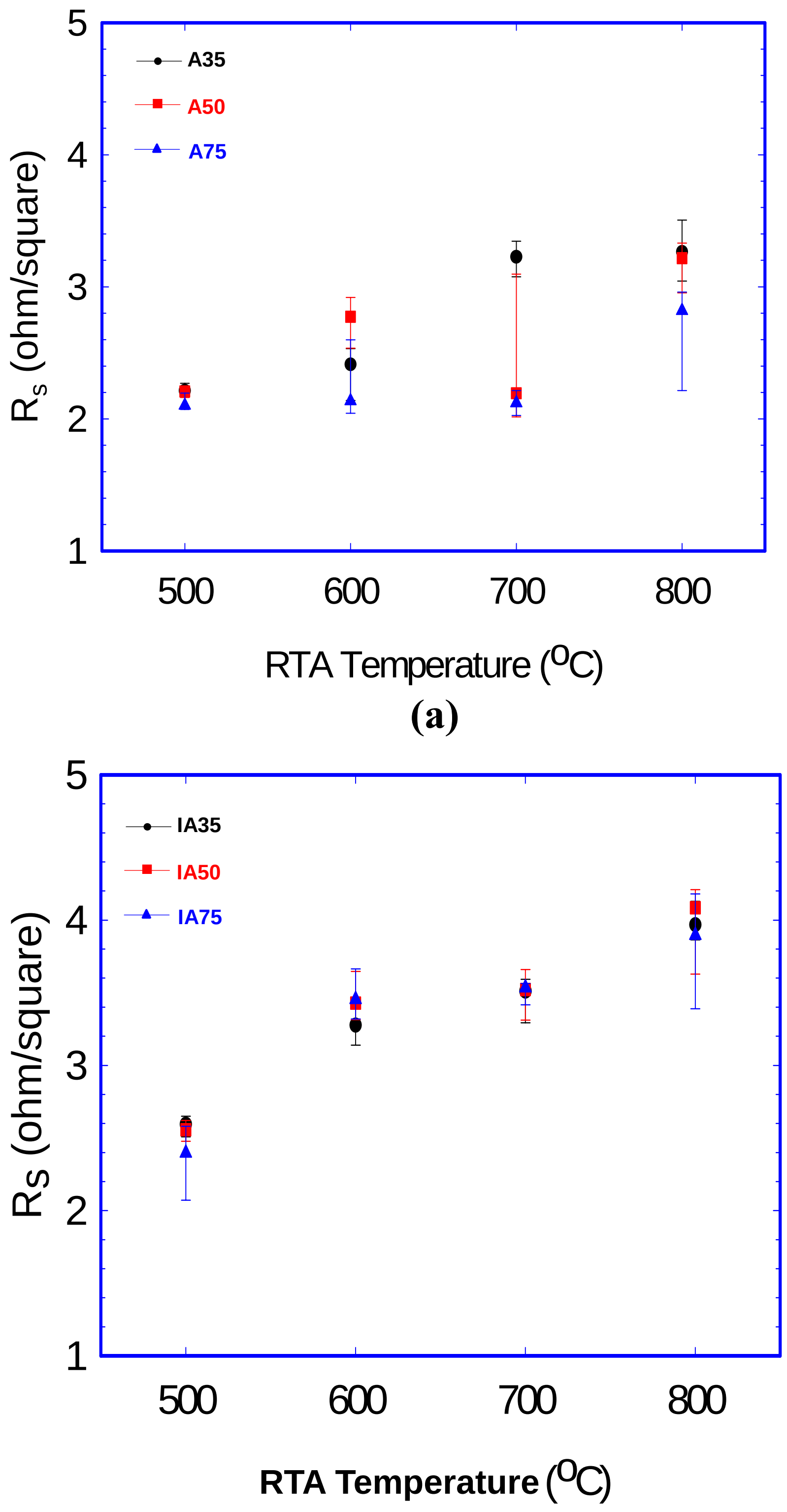
3. RCA clean
4. dilute O2 dry oxidation : 35, 50 and 75Å
5. PH_3 in-situ doped a-Si : 600Å (IA)
   (undoped a-Si also was fabricated as control)

1. dopant activation : RTA 900°C, 30s
2. PVD nickel film : 450Å

6. silicidation : RTA 500-800°C, 20s
7. unreacted Ni removement : (H_2SO_4+H_2O_2)

8. Sputter Al : 5000Å (Top electrode)
9. Wet etching for gate region
10. Sputter Al : 5000Å (Back electrode)

Fig. 6.1 Key process flow and schematics of the full nickel silicide MOS capacitor formation.



(a)

(b)

Fig. 6.2 Sheet resistance vs. RTA temperature for full nickel silicide gate with various gate oxide thickness (a) based on undoped a-Si (b) based on in-situ doped a-Si

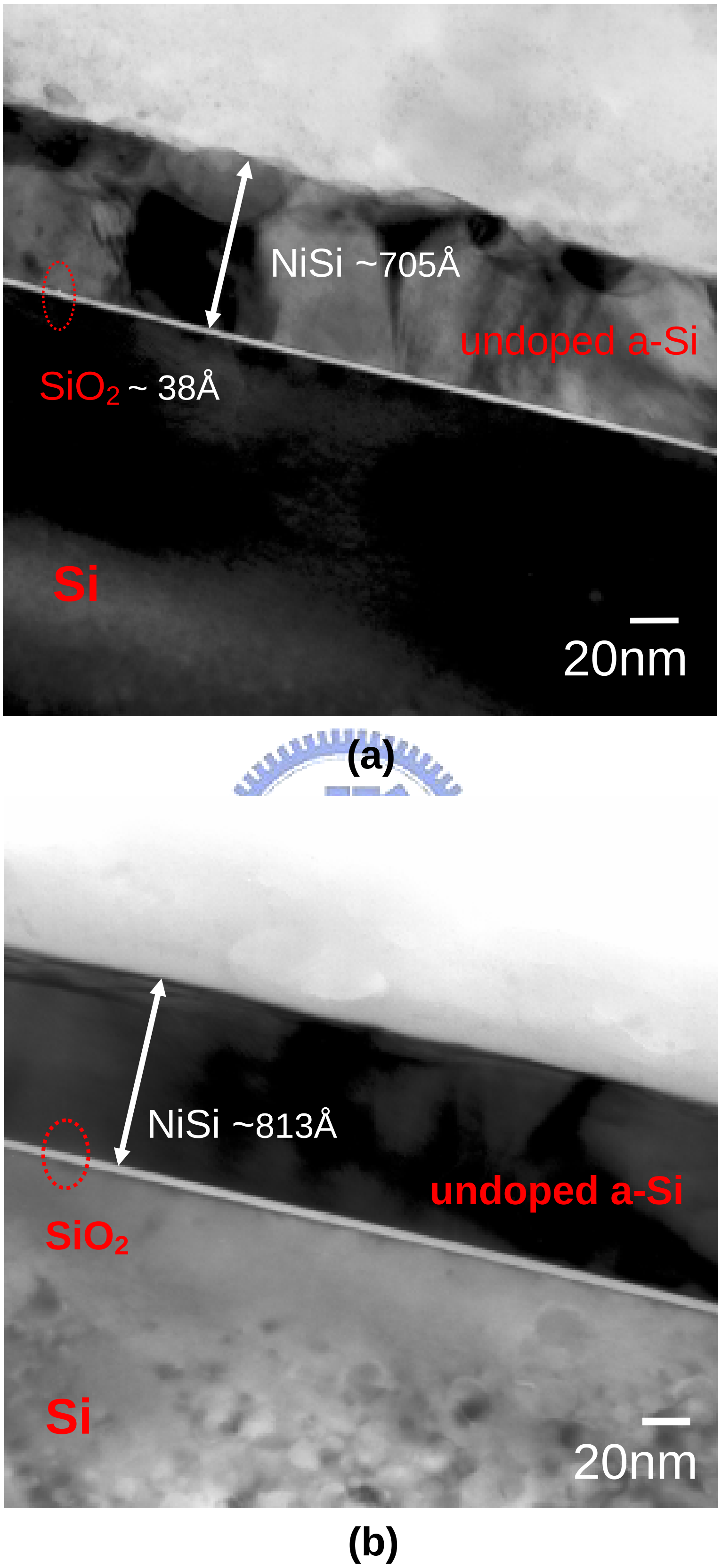
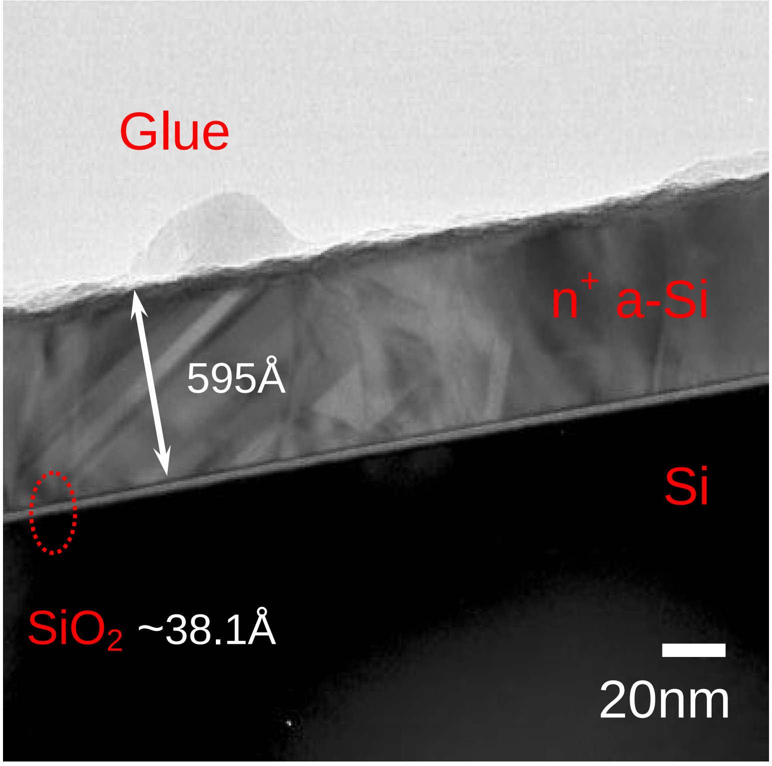
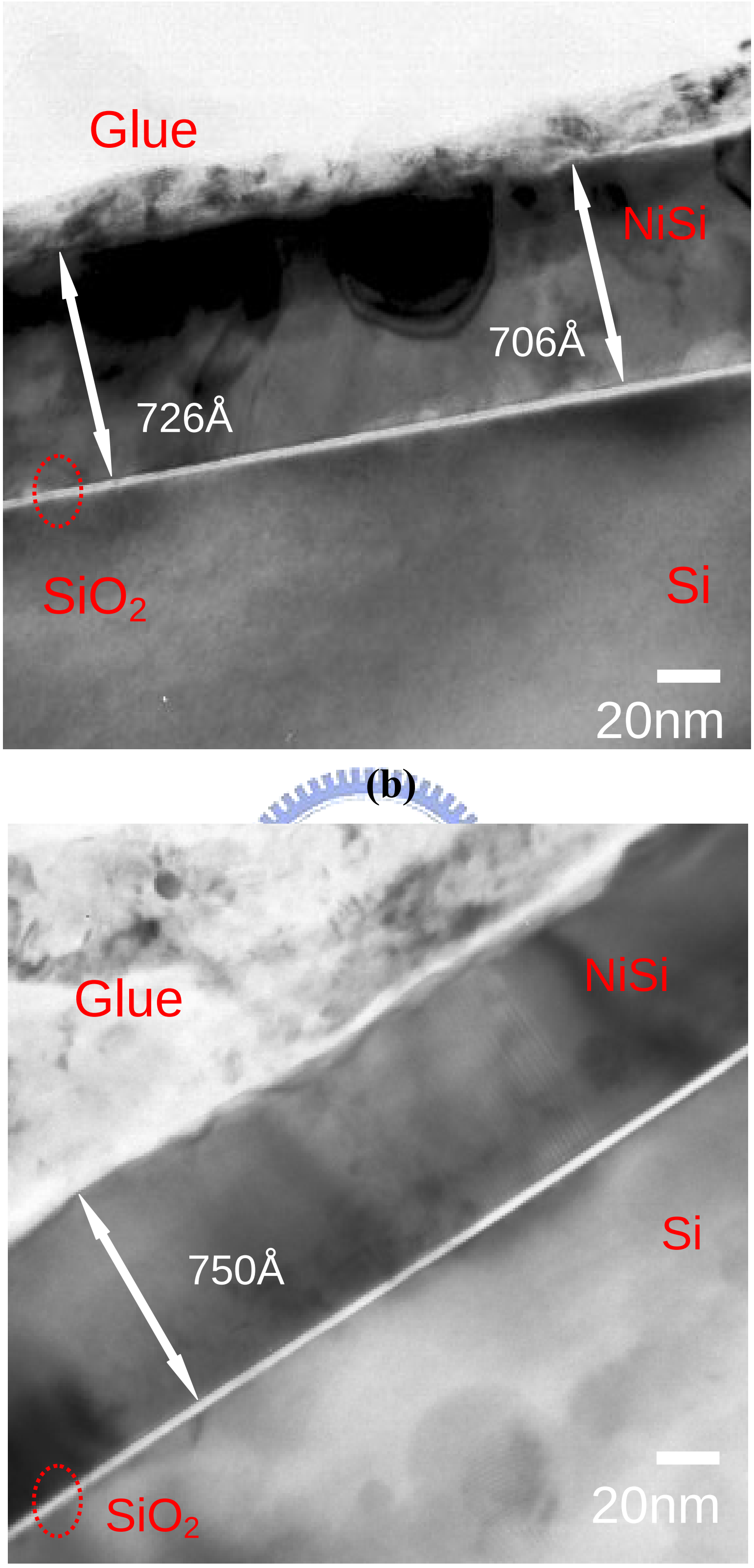


Fig. 6.3 TEM images for full nickel silicide gate capacitors based on undoped a-Si (a) at RTA 500°C (b) at RTA 800°C.



(a)

Fig. 6.4 (a) TEM image of in-situ doped a-Si gate capacitor.



(b)

(c)

Fig. 6.4 TEM images of full nickel silicide gate capacitors based on in-situ doped a-Si (b) at RTA 500°C (c) at RTA 800°C.

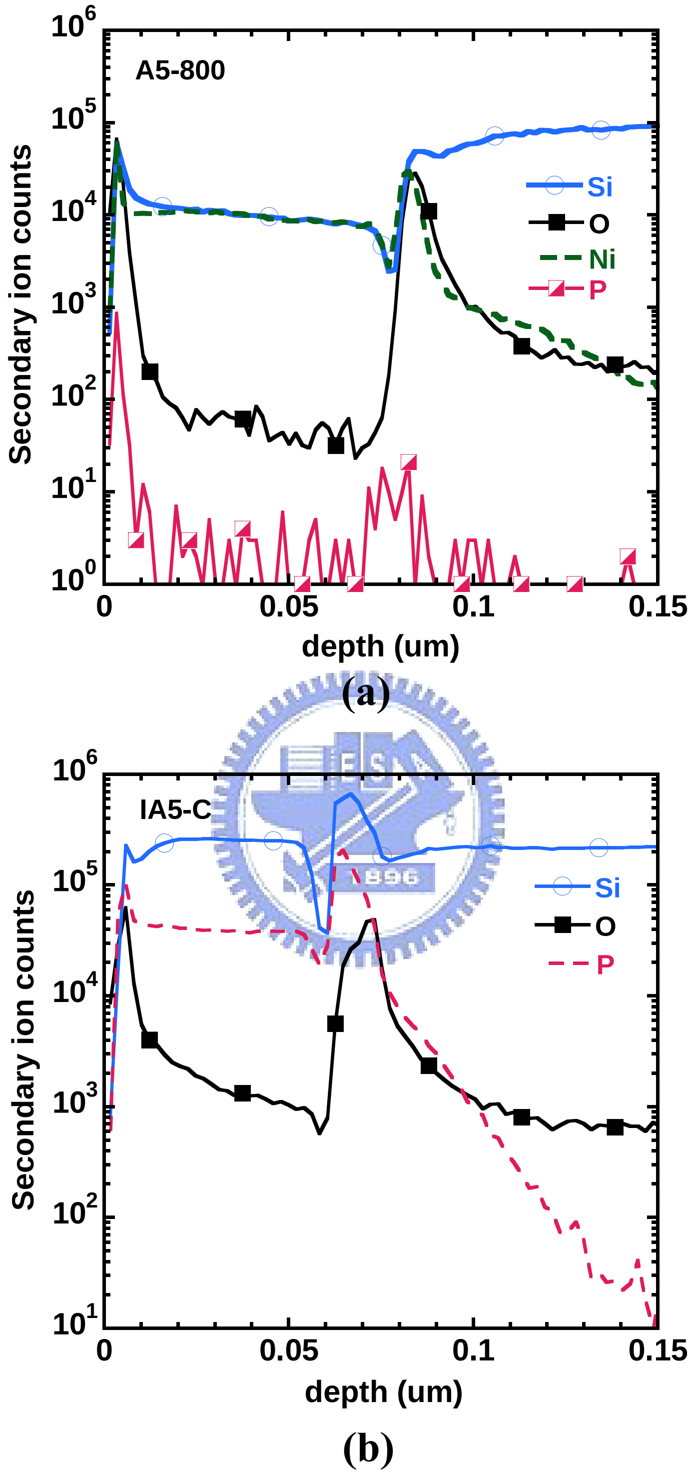
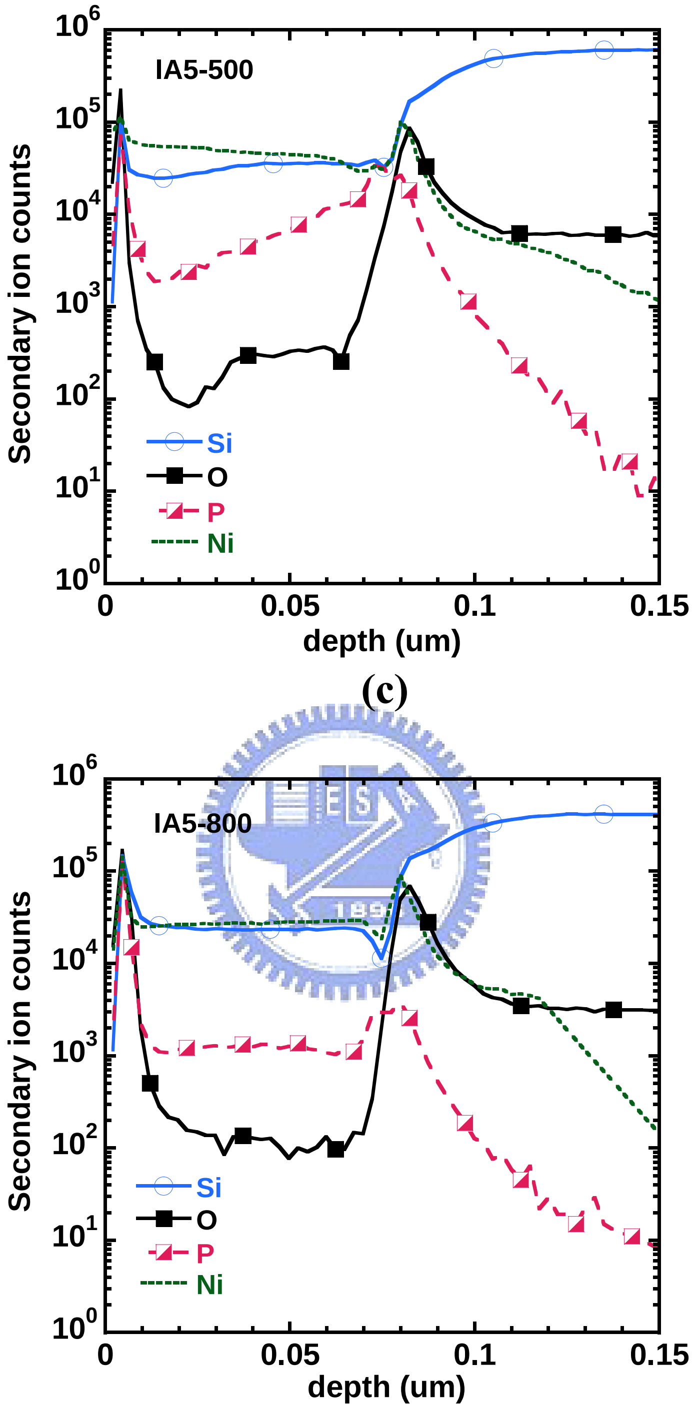


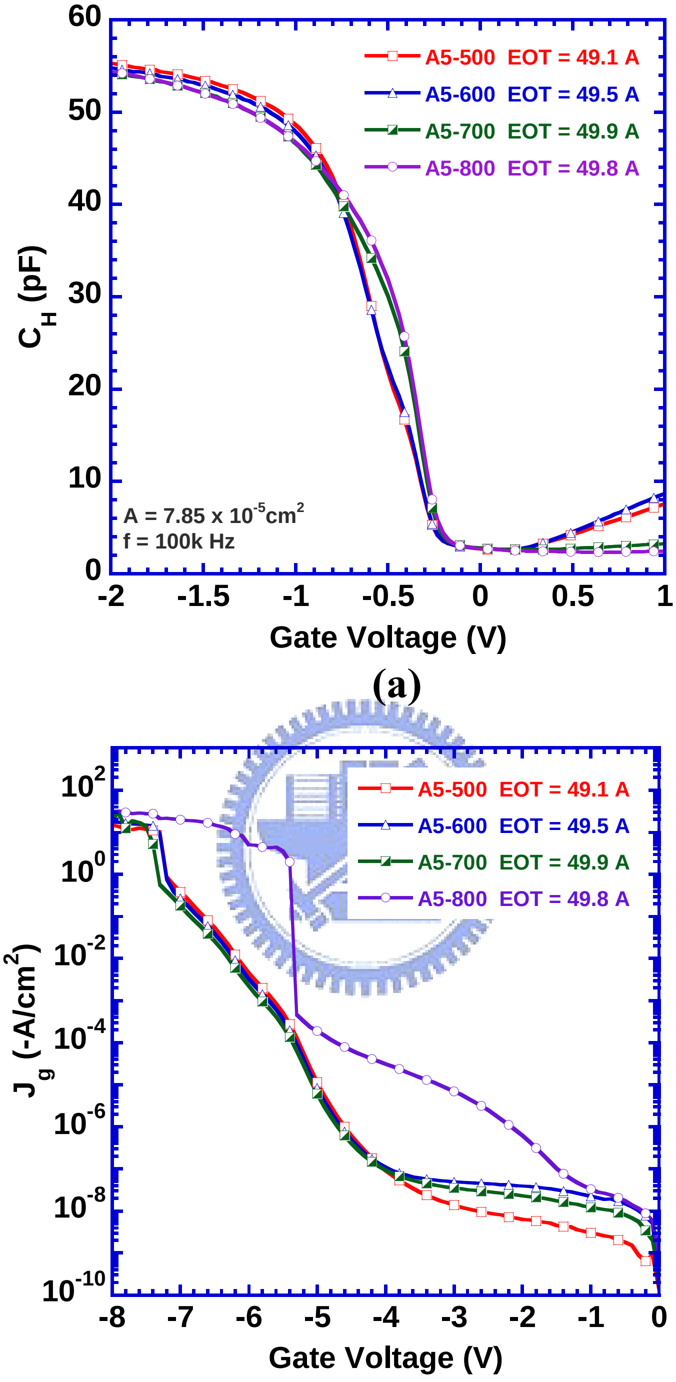
Fig. 6.5 SIMS profiles for (a) full nickel silicide gate capacitor on undoped a-Si at RTA 850°C. (b) in-situ doped a-Si gate capacitor without NiSi.



(c)

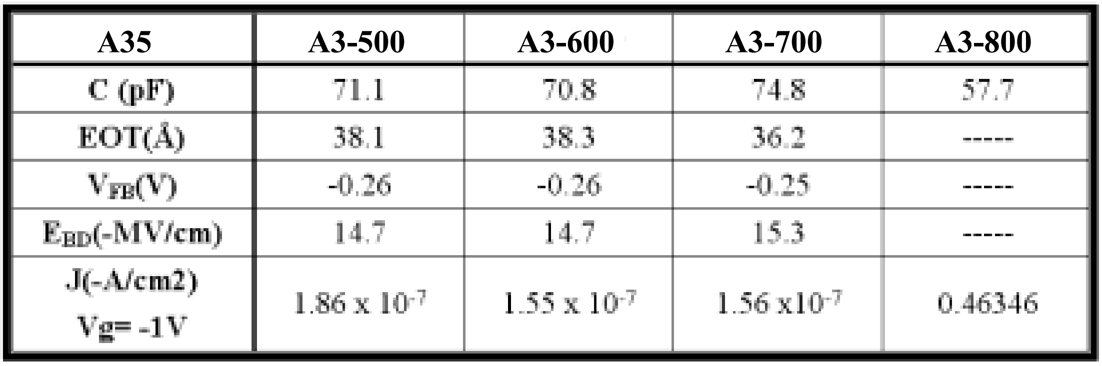
(d)

Fig. 6.5 SIMS profiles for full nickel silicide gate capacitor based on in-situ doped a-Si (c) at RTA 500°C. (d) at RTA 800°C.



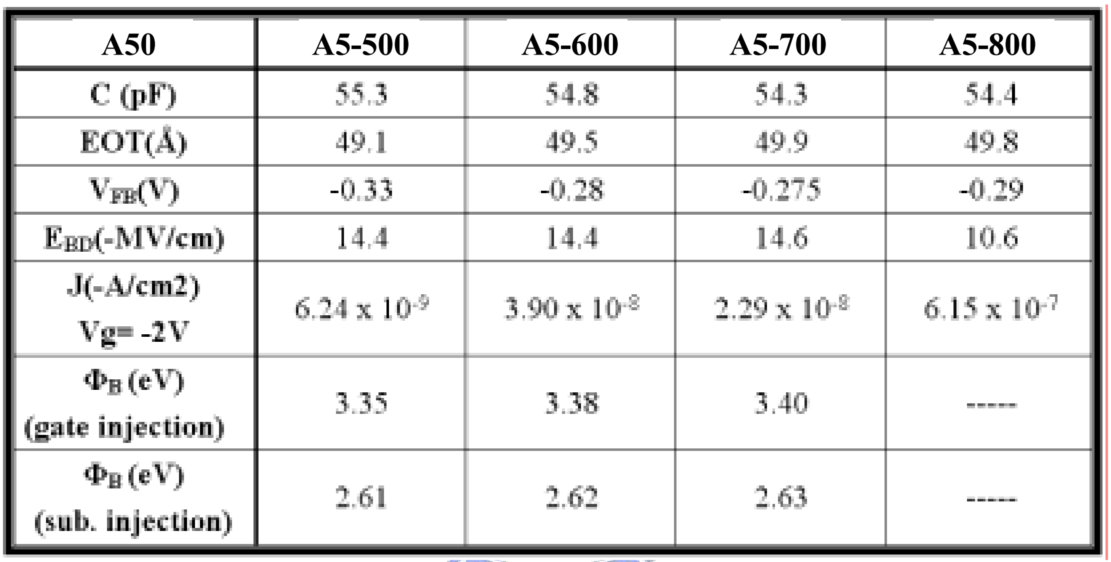
(b)

Fig. 6.6 (a) High frequency capacitance versus gate voltage plot (b) Gate leakage current density versus gate voltage of the a-Si/SiO$_2$(50Å) structure with 500~800^{o}C RTA.



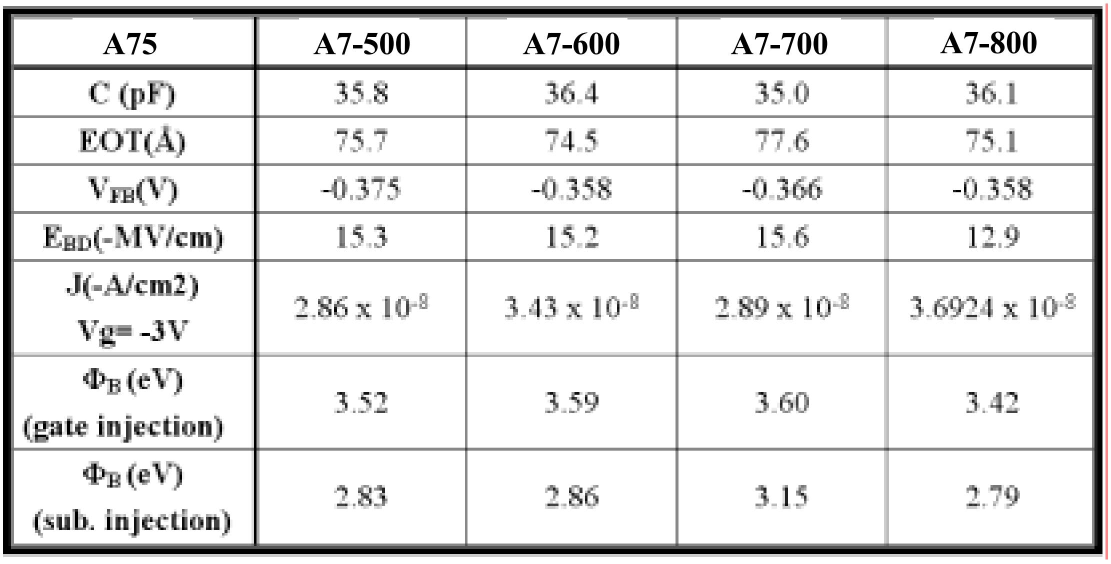
A35	A3-500	A3-600	A3-700	A3-800
C (pF)	71.1	70.8	74.8	57.7
EOT(Å)	38.1	38.3	36.2	-----
V_{FB}(V)	-0.26	-0.26	-0.25	-----
E_{BD}(-MV/cm)	14.7	14.7	15.3	-----
J(-A/cm2) Vg= -1V	1.86×10^{-7}	1.55×10^{-7}	1.56×10^{-7}	0.46346

(a)



A50	A5-500	A5-600	A5-700	A5-800
C (pF)	55.3	54.8	54.3	54.4
EOT(Å)	49.1	49.5	49.9	49.8
V_{FB}(V)	-0.33	-0.28	-0.275	-0.29
E_{BD}(-MV/cm)	14.4	14.4	14.6	10.6
J(-A/cm2) Vg= -2V	6.24×10^{-9}	3.90×10^{-8}	2.29×10^{-8}	6.15×10^{-7}
Φ_B (eV) (gate injection)	3.35	3.38	3.40	-----
Φ_B (eV) (sub. injection)	2.61	2.62	2.63	-----

(b)



A75	A7-500	A7-600	A7-700	A7-800
C (pF)	35.8	36.4	35.0	36.1
EOT(Å)	75.7	74.5	77.6	75.1
V_{FB}(V)	-0.375	-0.358	-0.366	-0.358
E_{BD}(-MV/cm)	15.3	15.2	15.6	12.9
J(-A/cm2) Vg= -3V	2.86×10^{-8}	3.43×10^{-8}	2.89×10^{-8}	3.6924×10^{-8}
Φ_B (eV) (gate injection)	3.52	3.59	3.60	3.42
Φ_B (eV) (sub. injection)	2.83	2.86	3.15	2.79

(c)

Table 6.1 characteristics of full nickel silicide gate capacitors based on undoped a-Si by various RTA conditions of (a) 35Å (b) 50Å (c) 75Å-thick SiO_2

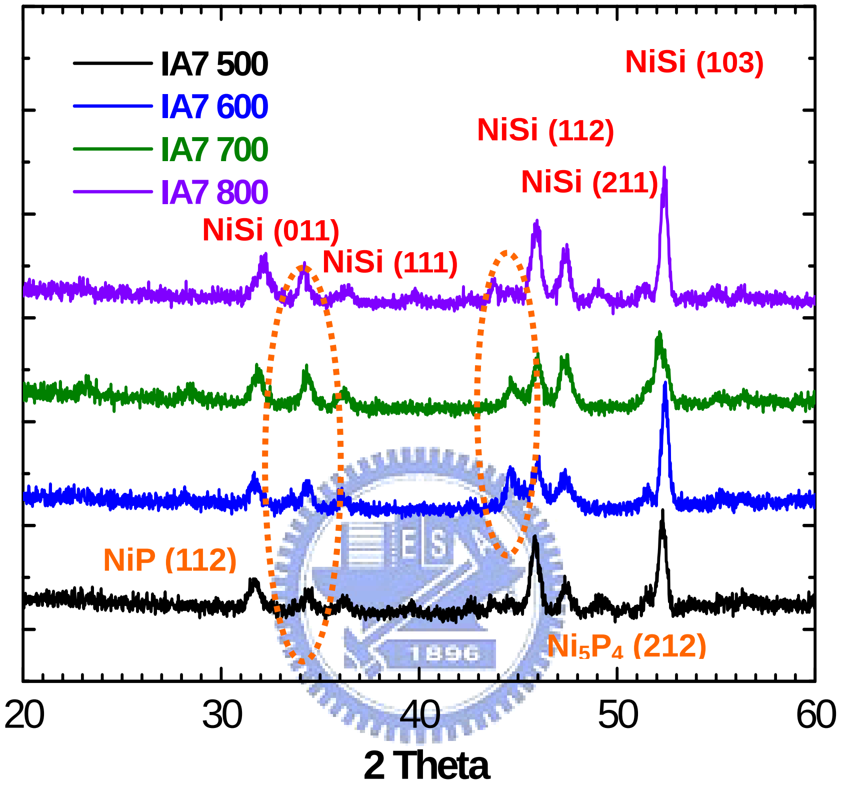
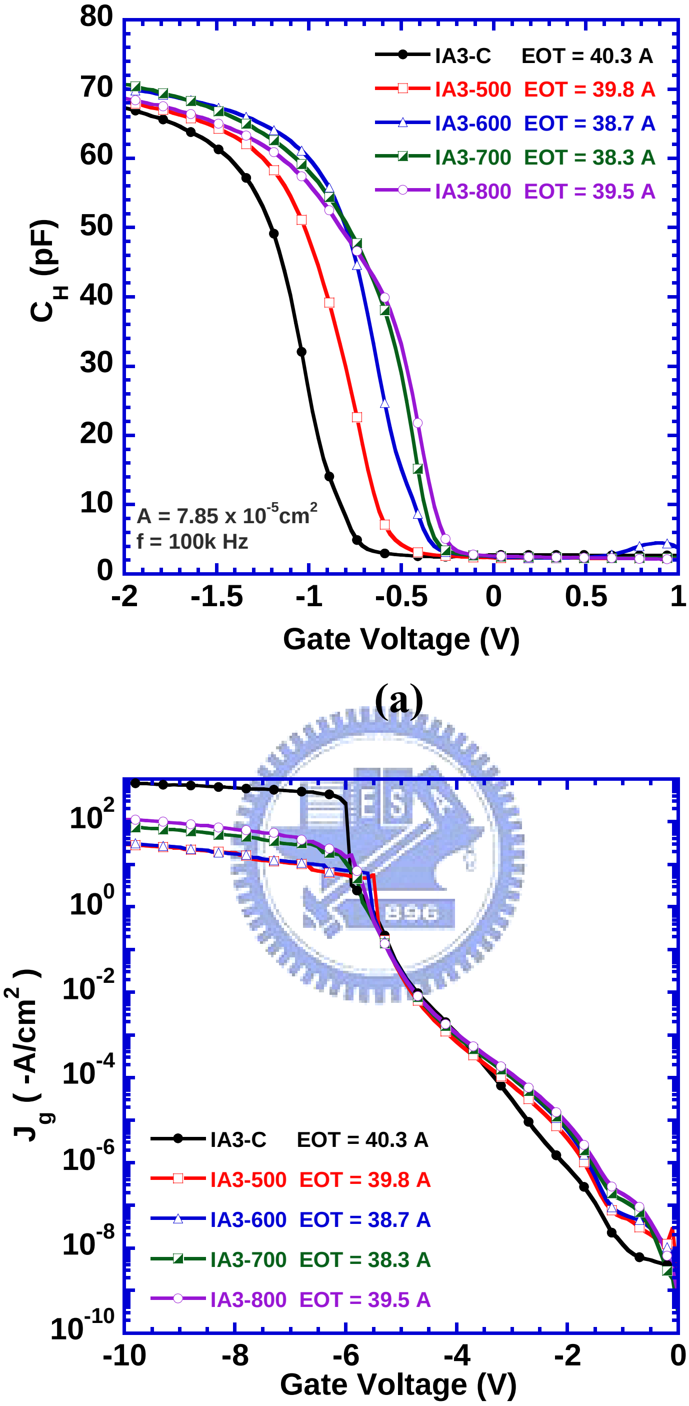


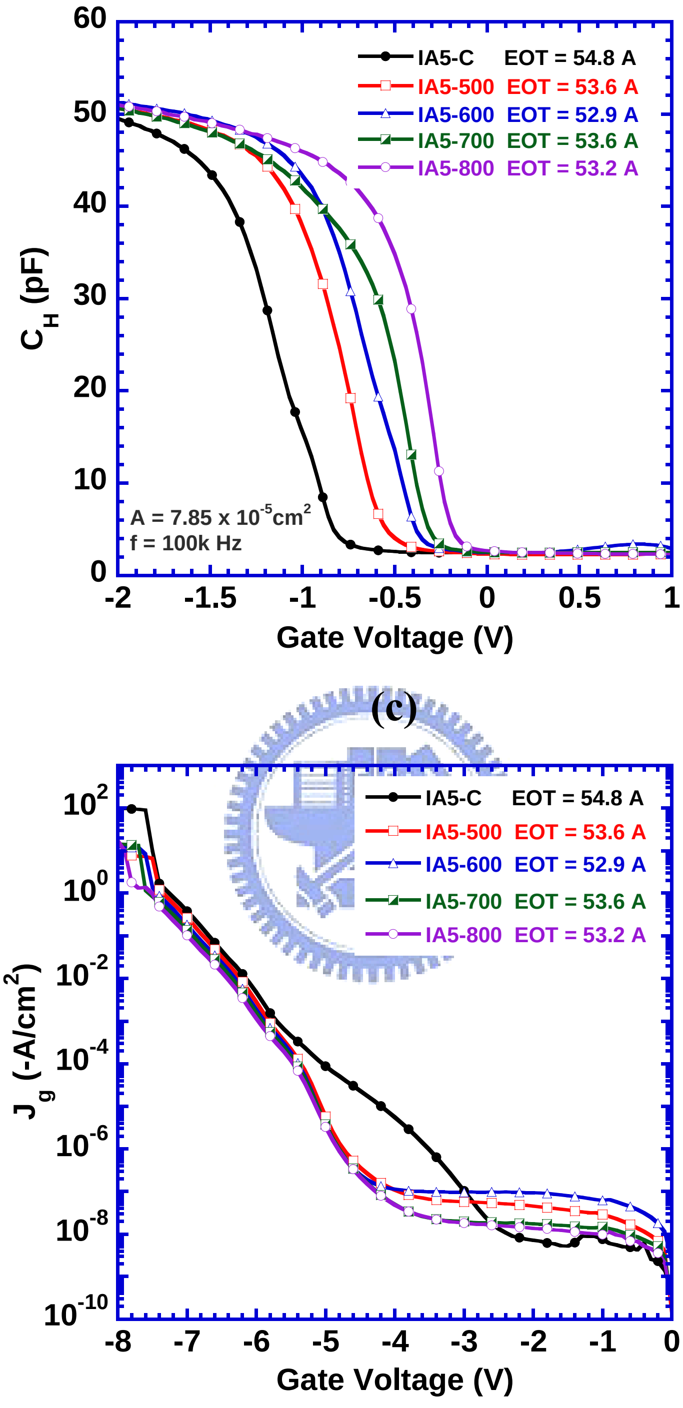
Fig. 6.7 X-ray diffraction spectra (XRD) of full nickel silicide gate capacitors based on in-situ doped a-Si with the various RTA conditions.



(a)

(b)

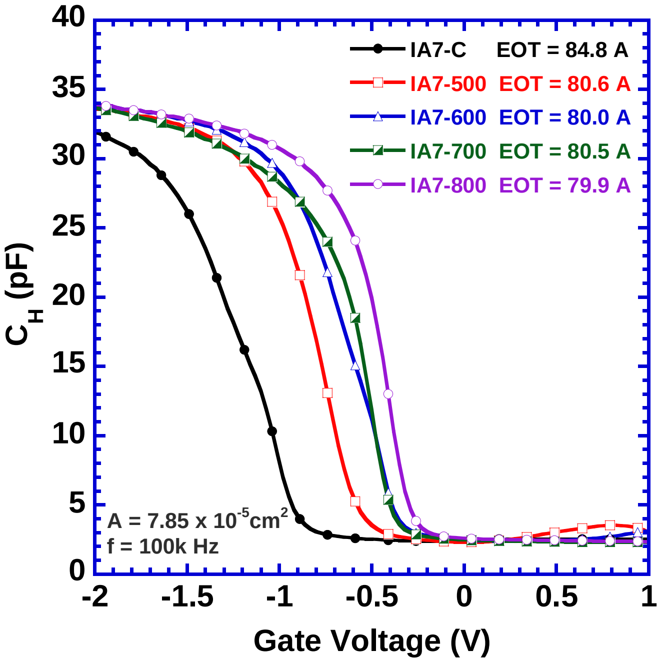
Fig. 6.8 (a) High frequency capacitance versus gate voltage plot (b) Gate leakage current density versus gate voltage of the full nickel silicide n^+ a-Si/SiO$_2$ (35Å) structure (IA3) with 500~800°C RTA.



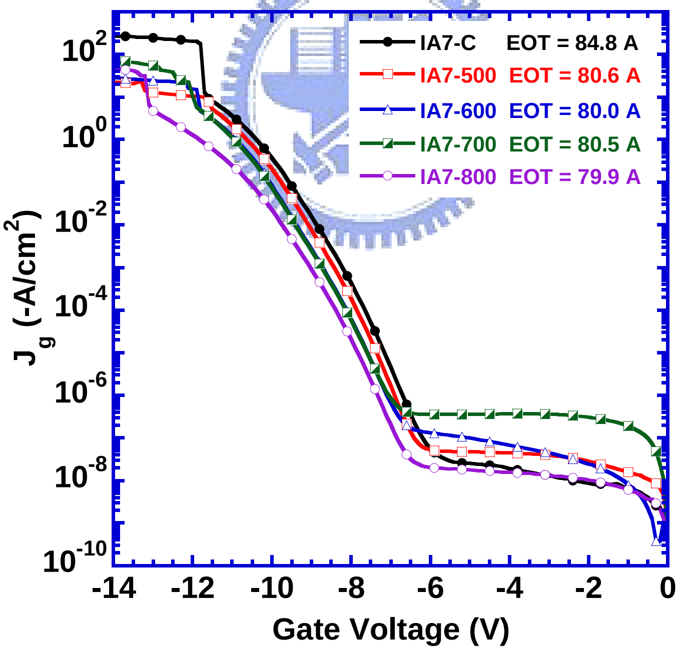
(c)

(d)

Fig. 6.8 (c) High frequency capacitance versus gate voltage plot (d) Gate leakage current density versus gate voltage of the full nickel silicide n^+ a-Si/SiO_2 (50Å) structure (IA5) with 500~800°C RTA.



(e)



(f)

Fig. 6.8 (e) High frequency capacitance versus gate voltage plot (f) Gate leakage current density versus gate voltage of the full nickel silicide n^+ a-Si/SiO$_2$ (75Å) structure (IA7) with 500~800°C RTA.

IA3	IA3-C	IA3-500	IA3-600	IA3-700	IA3-800
C (pF)	67.3	68.1	70.1	70.7	68.7
EOT(Å)	40.3	39.8	38.7	38.3	39.5
V_{FB}(V)	-0.925	-0.7	-0.5416	-0.3916	-0.383
E_{BD}(-MV/cm)	15.5	14.2	14.5	15.0	14.5
J(-A/cm2) Vg= -1V	1.20×10^{-8}	5.08×10^{-8}	6.16×10^{-8}	1.31×10^{-7}	1.81×10^{-7}

(a)

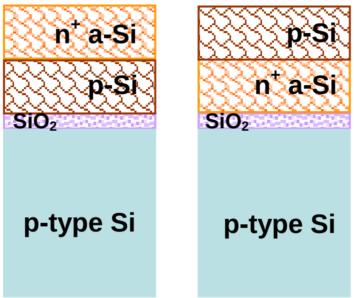
IA5	IA5-C	IA5-500	IA5-600	IA5-700	IA5-800
C (pF)	49.5	50.6	51.2	50.6	51.0
EOT(Å)	54.8	53.6	52.9	53.6	53.2
V_{FB}(V)	-0.941	-0.716	-0.5416	-0.4	-0.29
E_{BD}(-MV/cm)	14.2	14.0	14.2	14.3	14.7
J(-A/cm2) Vg= -2V	7.13×10^{-9}	4.53×10^{-8}	9.31×10^{-8}	1.74×10^{-8}	1.36×10^{-8}
Φ_B (eV) (gate injection)	2.93	3.08	3.15	3.25	3.30
Φ_B (eV) (sub. injection)	1.94	2.27	2.33	2.44	2.57

(b)

IA7	IA7-C	IA7-500	IA7-600	IA7-700	IA7-800
C (pF)	31.9	33.6	33.9	33.7	33.9
EOT(Å)	84.8	80.6	80.0	80.5	79.9
V_{FB}(V)	-1.05	-0.74	-0.55	-0.516	-0.408
E_{BD}(-MV/cm)	14.6	14.4	14.8	14.9	16.3
J(-A/cm2) Vg= -3V	1.29×10^{-8}	3.92×10^{-8}	4.39×10^{-8}	3.59×10^{-7}	1.35×10^{-8}
Φ_B (gate injection)	2.92	3.15	3.29	3.37	3.35
Φ_B (sub. injection)	2.47	2.54	2.75	2.79	2.79

(c)

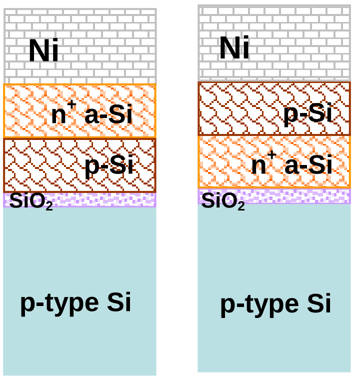
Table 6.2 characteristics of full nickel silicide gate capacitors based on in-situ doped a-Si by various RTA conditions of (a) 35Å (b) 50Å (c) 75Å-thick SiO_2



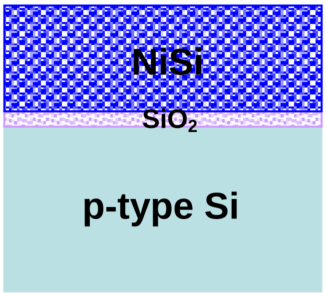
1. RCA clean
2. dilute O2 dry oxidation : 35, 50 and 75Å
3. Stack gate formation :

   (AP) : n^+ a-Si / undoped poly-Si / SiO_2 (600Å)

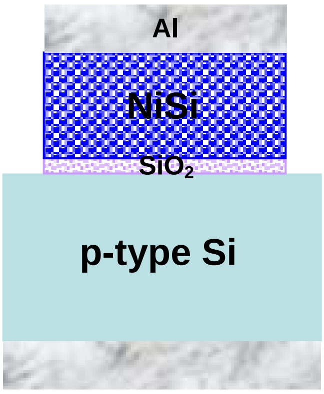
   (PA) : undoped poly-Si / n^+ a-Si / SiO_2 (600Å)



4. dopant activation : RTA 900°C, 30s
5. PVD nickel film : 450Å

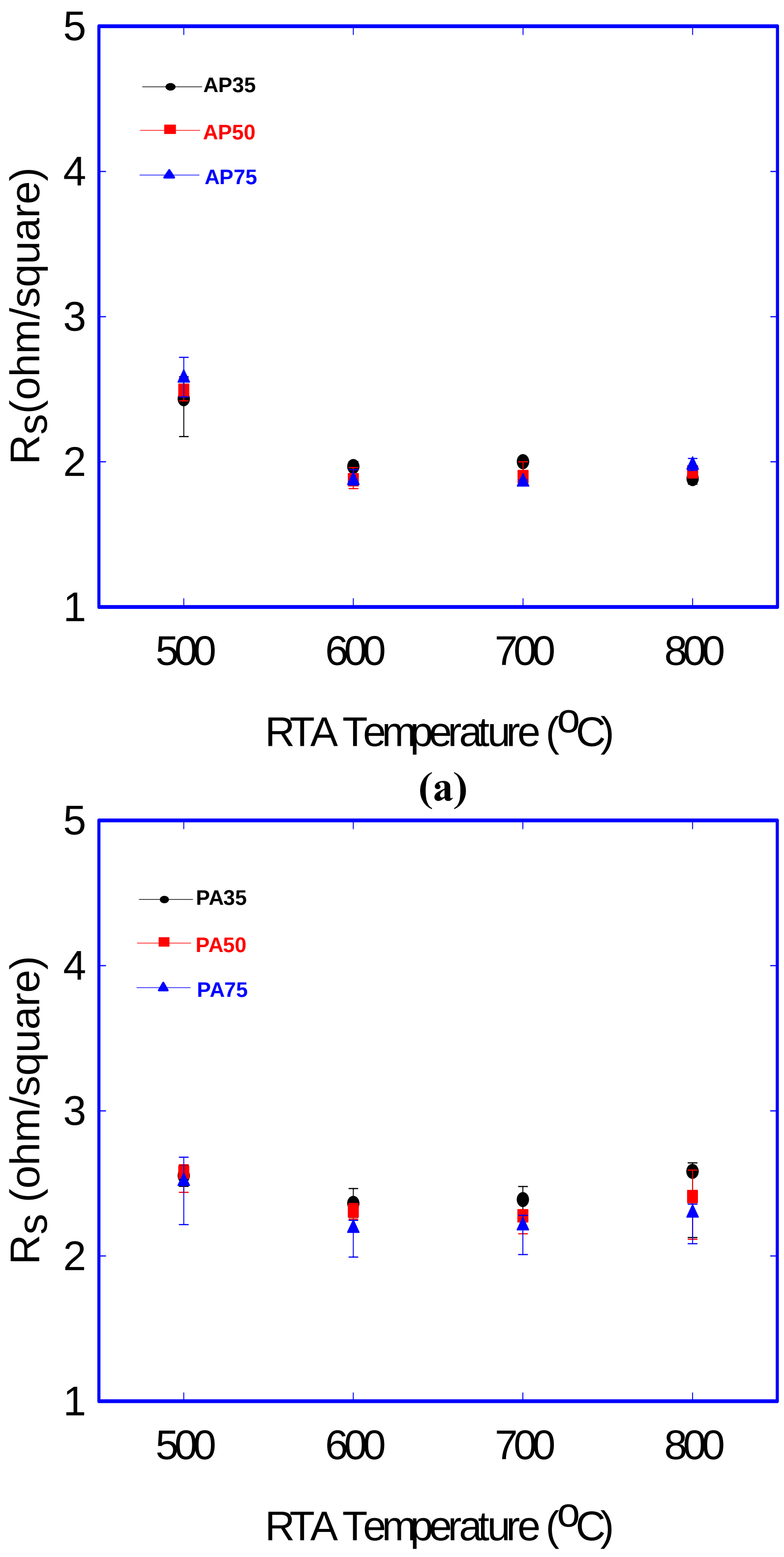


6. silicidation : RTA 500-800°C, 20s
7. unreacted Ni removement : (H_2SO_4+H_2O_2)



8. Sputter Al : 5000Å (Top electrode)
9. Wet etching for gate region
10. Sputter Al : 5000Å (Back electrode)

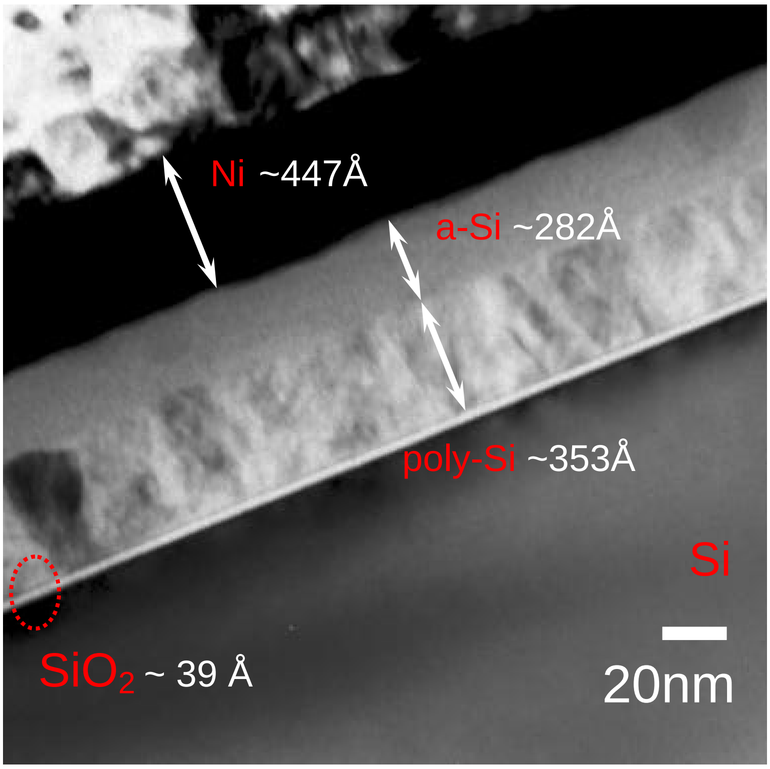
Fig. 6.9 Key process flow and schematics of the full nickel silicide MOS capacitor formation based on stack structure.



(a)

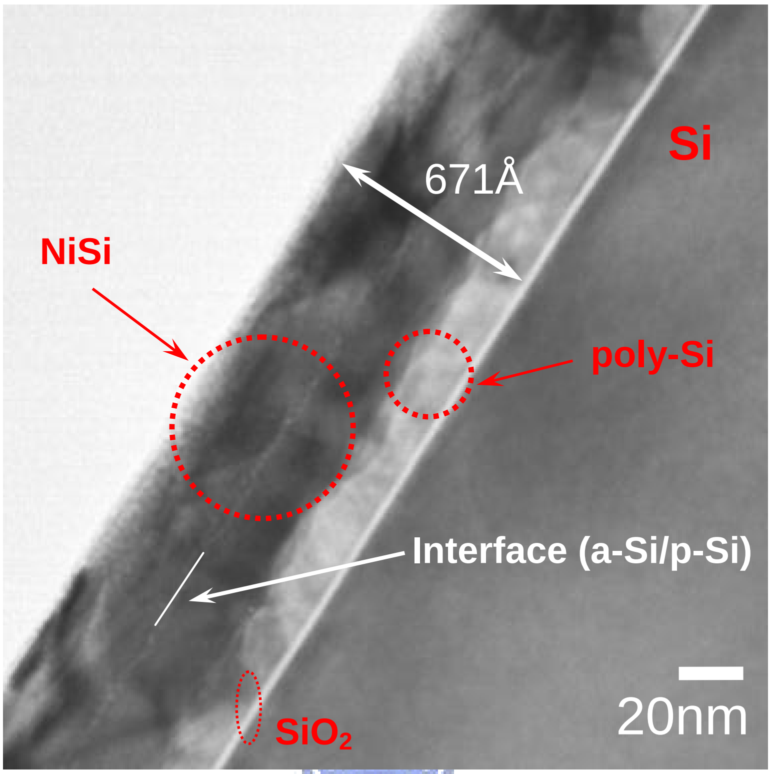
(b)

Fig. 6.10 Sheet resistance vs. RTA temperature for full nickel silicide gate based on stack structure (a) n^+ a-Si/p-Si (b) p-Si/n^+ a-Si with various gate oxide thickness.

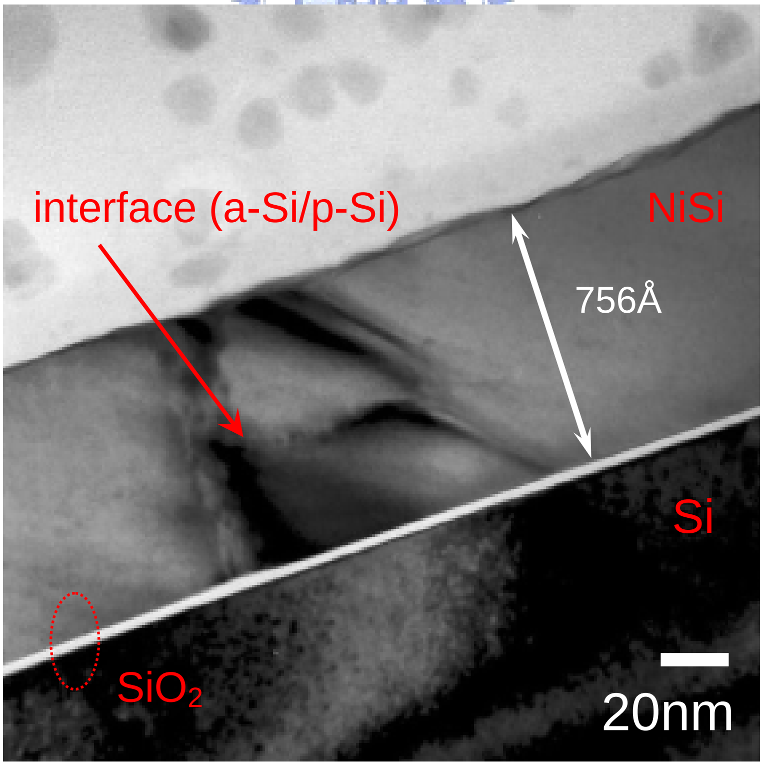


(a)

Fig. 6.11 (a) TEM image of in-situ doped a-Si/ undoped p-Si gate structure.

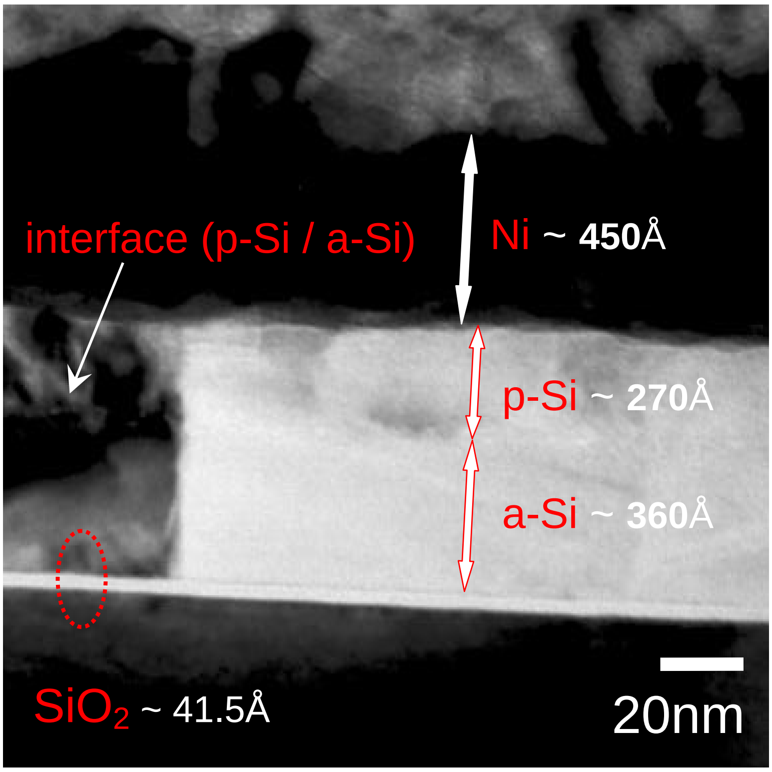


(b)



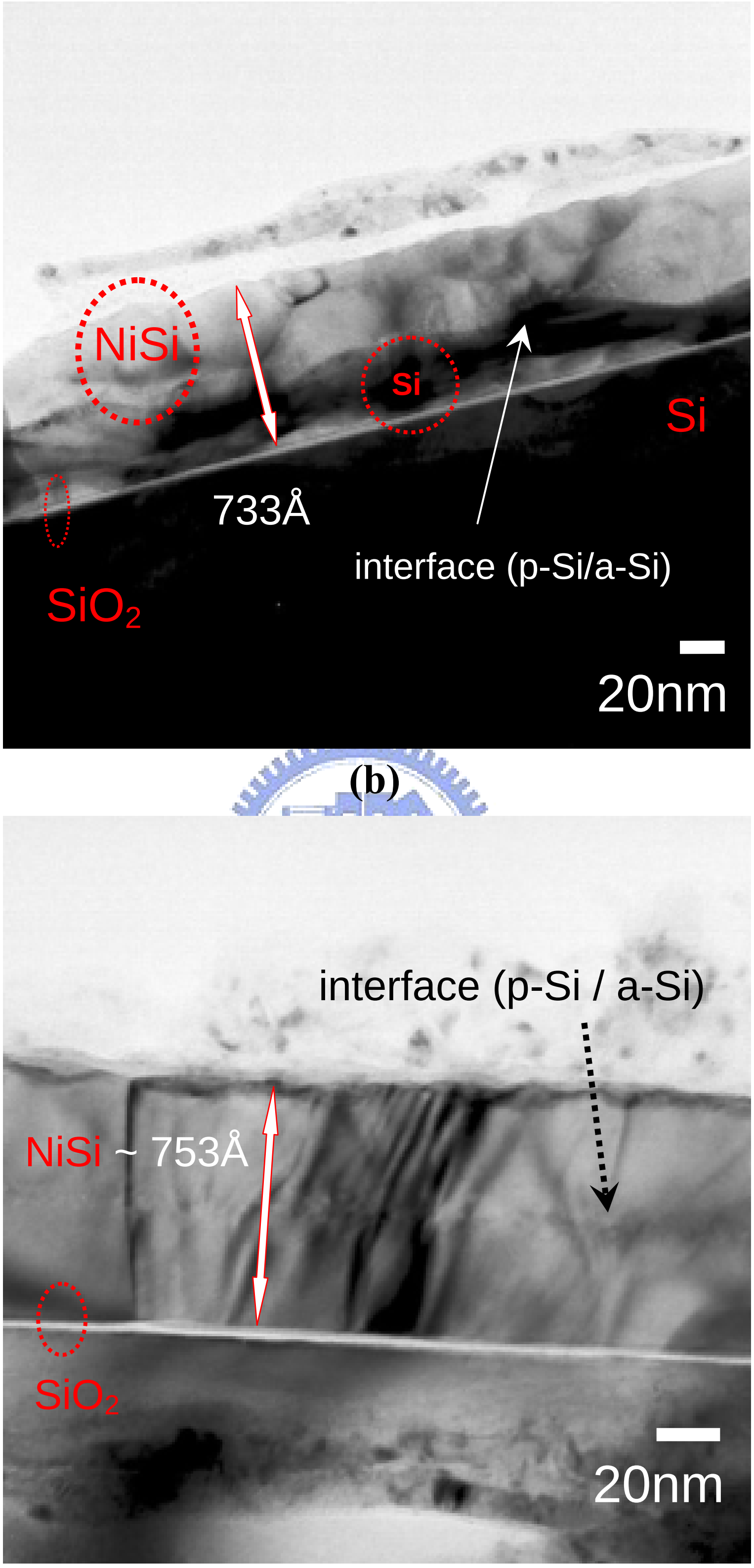
(c)

Fig. 6.11 TEM images of n$^+$ a-Si/p-Si stack gate capacitors after silicidation at (b) 500°C (c) 800°C.



(a)

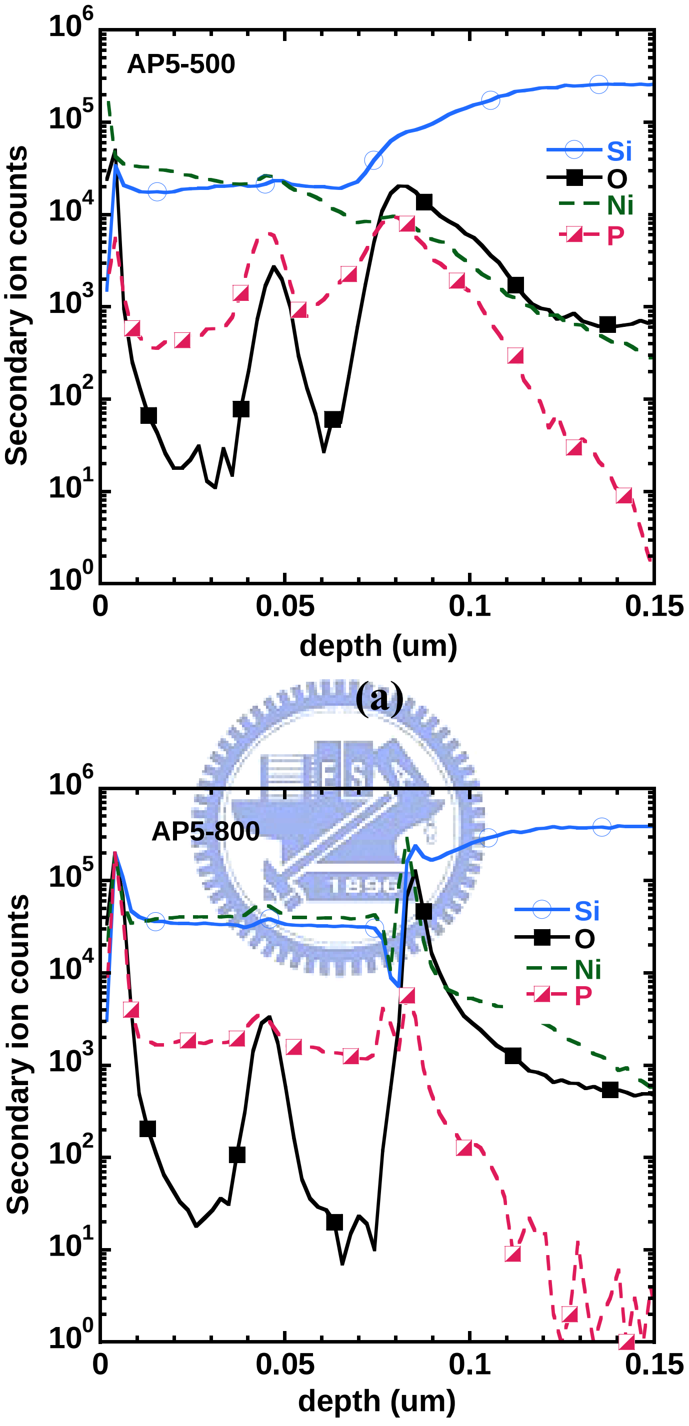
Fig. 6.12 (a) TEM image of undoped p-Si/in-situ doped a-Si gate structure.



(b)

(c)

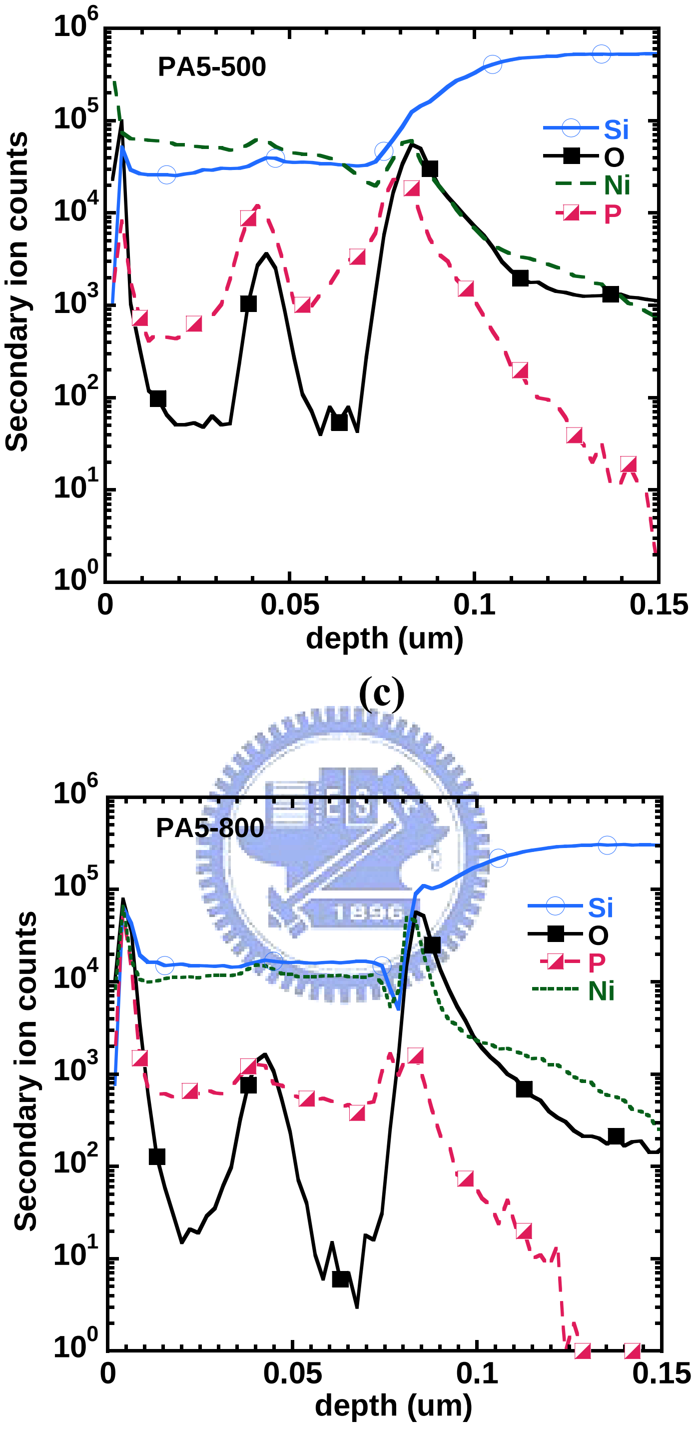
Fig. 6.12 TEM images of p-Si/ n^+ a-Si stack gate capacitors after silicidation at (b) 500°C (c) 800°C.



(a)

(b)

Fig. 6.13 SIMS profiles of full nickel silicide gate capacitor based on n^+ a-Si/p-Si structure (a) at RTA 500^{o}C. (b) at RTA 800^{o}C.



(c)

(d)

Fig. 6.13 SIMS profiles of full nickel silicide gate capacitor based on p-Si/n$^+$ a-Si structure (c) at RTA 500^{o}C. (d) at RTA 800^{o}C.

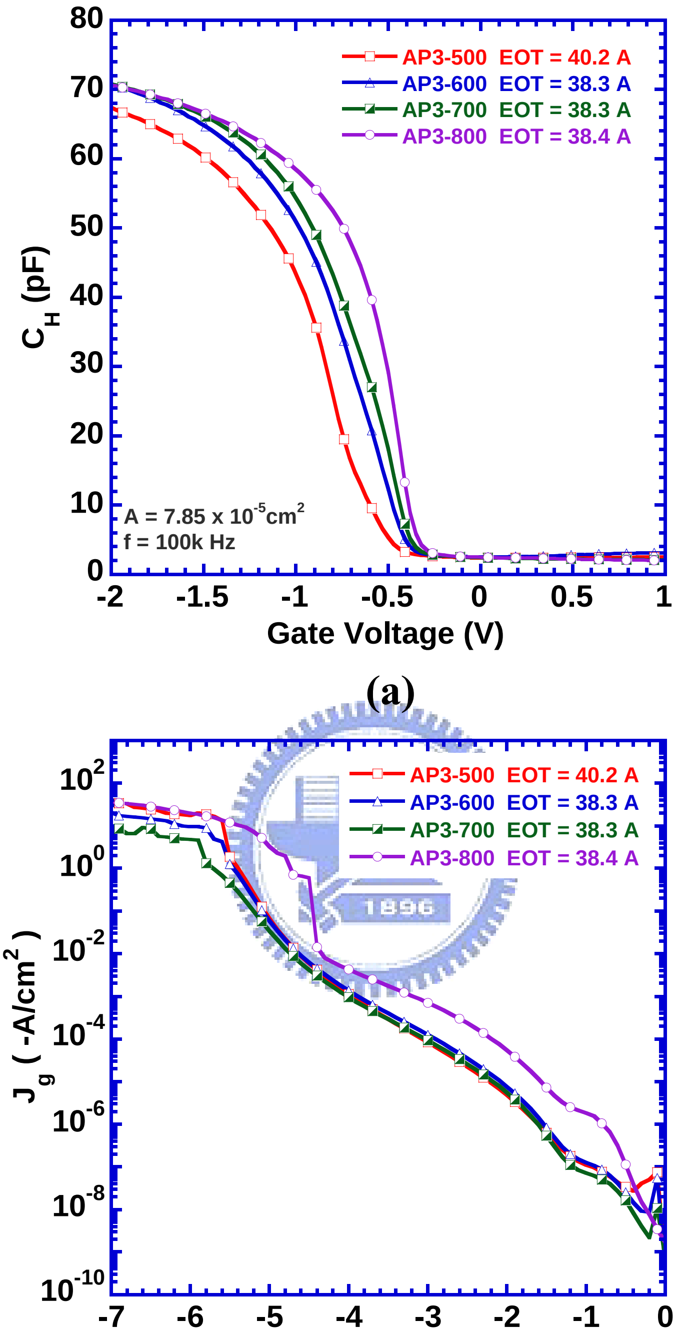
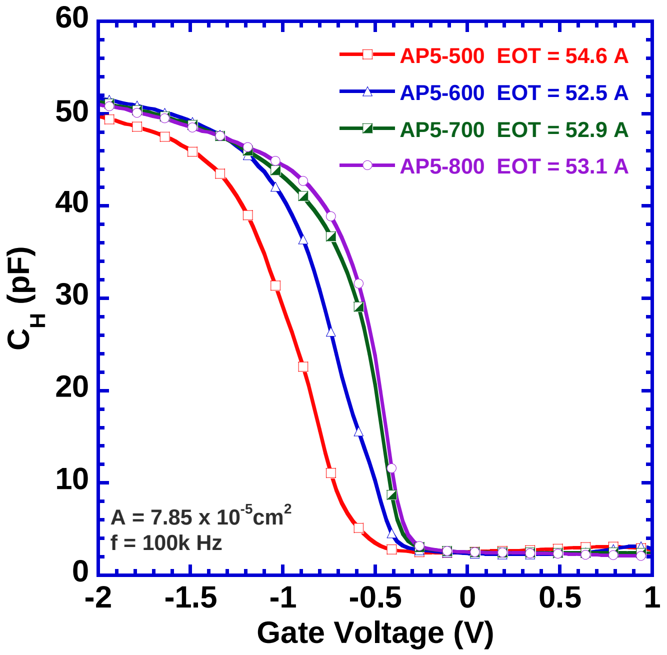
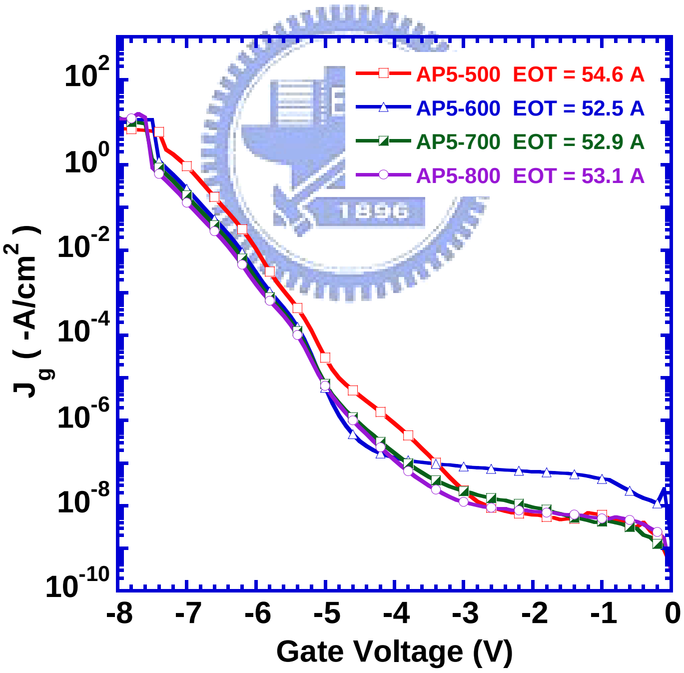


Fig. 6.14 (a) High frequency capacitance versus gate voltage plot (b) Gate leakage current density versus gate voltage of n^+ a-Si/p-Si/SiO_2 (35Å) structure (AP3) with 500~800°C RTA.

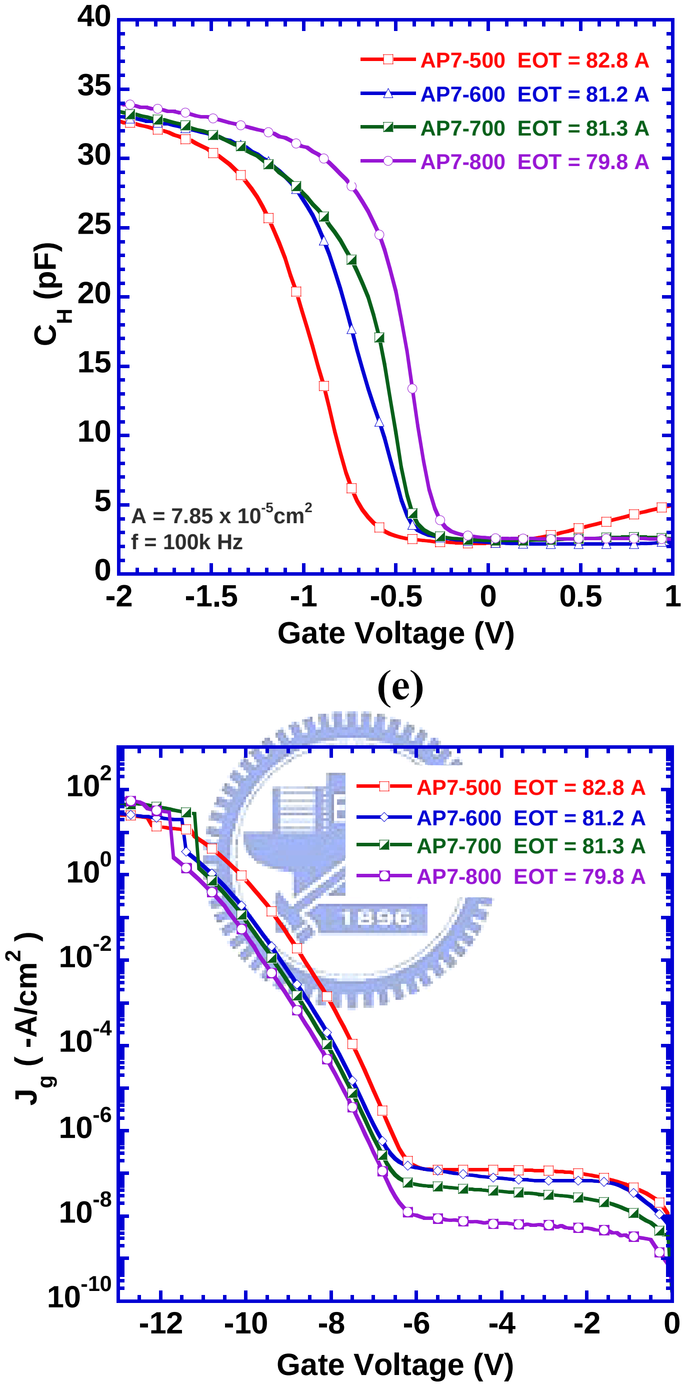


(c)



(d)

Fig. 6.14 (c) High frequency capacitance versus gate voltage plot (d) Gate leakage current density versus gate voltage of n^+ a-Si/p-Si/SiO_2 (50Å) structure (AP5) with 500~800°C RTA.



(e)

(f)

Fig. 6.14 (e) High frequency capacitance versus gate voltage plot (f) Gate leakage current density versus gate voltage of n^+ a-Si/p-Si/SiO_2 (75Å) structure (AP7) with 500~800°C RTA.

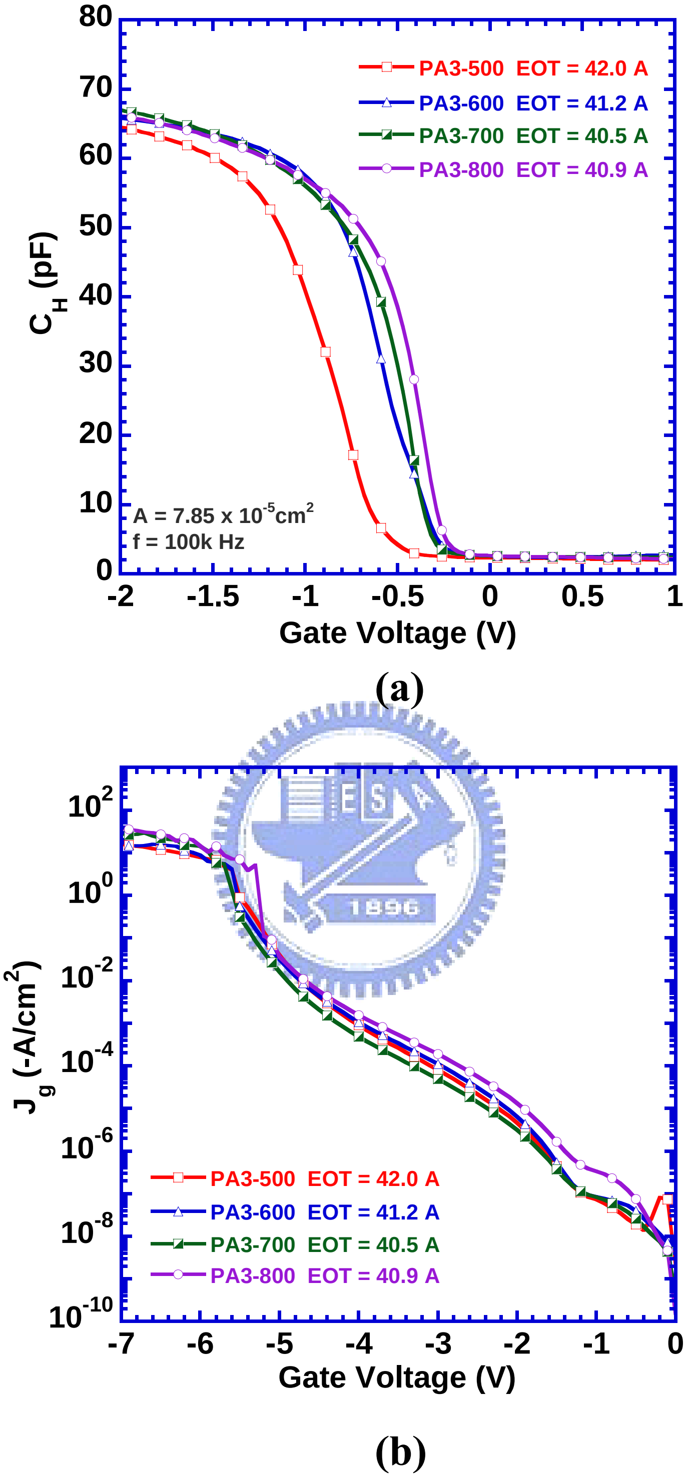
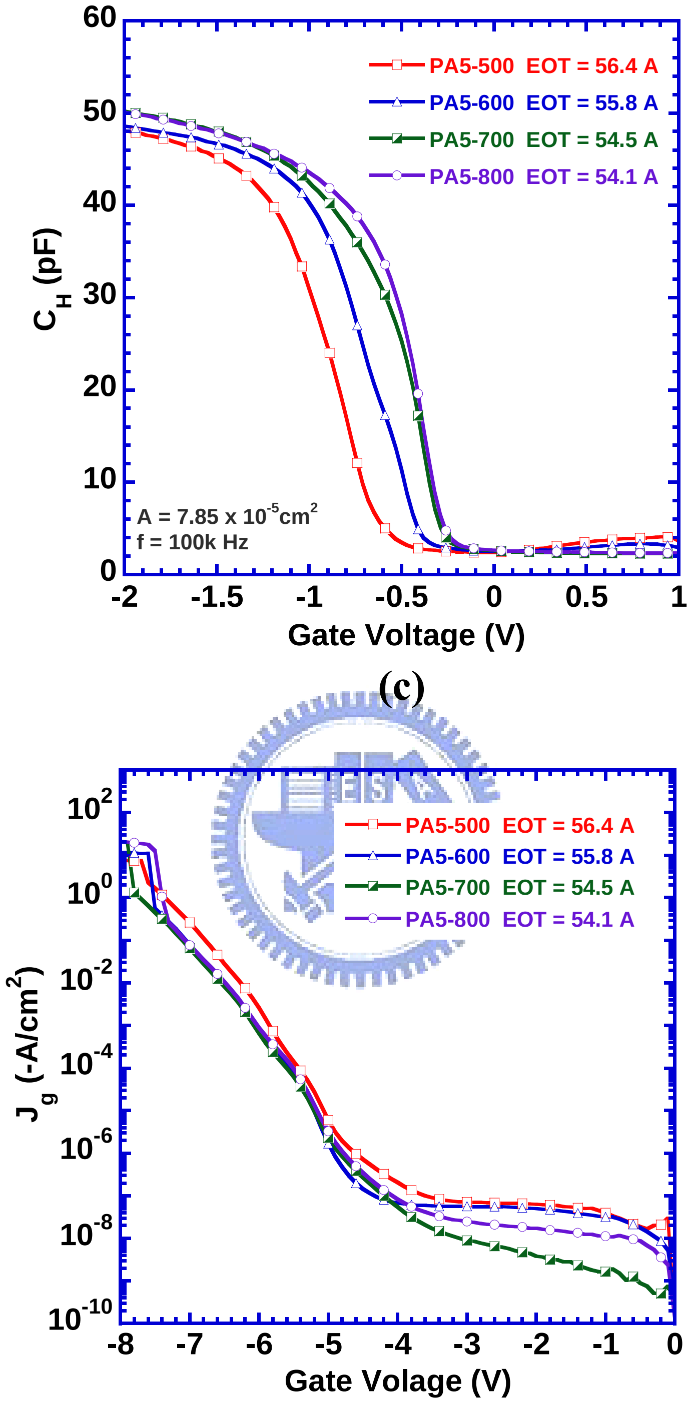


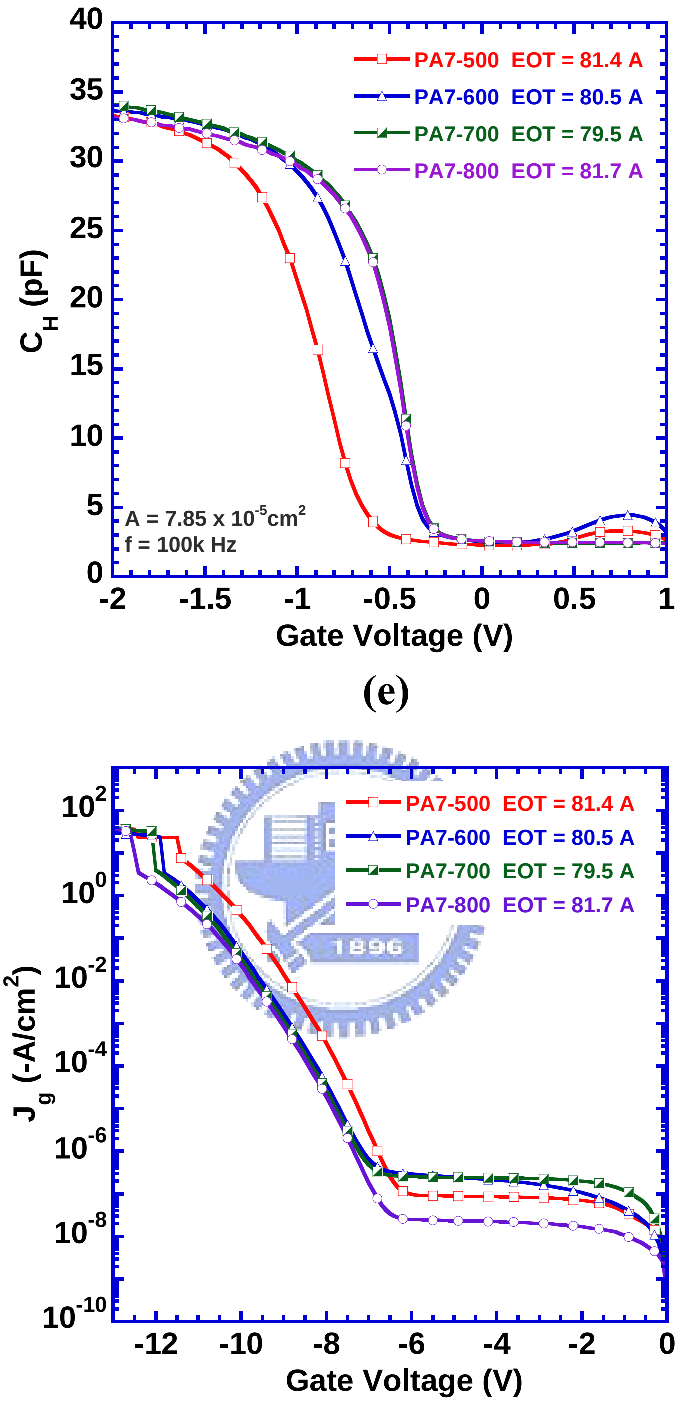
Fig. 6.15 (a) High frequency capacitance versus gate voltage plot (b) Gate leakage current density versus gate voltage of p-Si/n$^+$ a-Si/SiO$_2$ (35Å) structure (PA3) with 500~800°C RTA.



(c)

(d)

Fig. 6.15 (c) High frequency capacitance versus gate voltage plot (d) Gate leakage current density versus gate voltage of p-Si/n$^+$ a-Si/SiO$_2$ (50Å) structure (PA5) with 500~800^{o}C RTA.



(e)

(f)

Fig. 6.15 (e) High frequency capacitance versus gate voltage plot (f) Gate leakage current density versus gate voltage of p-Si/n$^+$ a-Si/SiO$_2$ (75Å) structure (PA7) with 500~800°C RTA.

AP3	AP3-500	AP3-600	AP3-700	AP3-800
C (pF)	67.4	70.8	70.8	73.1
EOT(Å)	40.2	38.3	38.3	3.71
V_{FB}(V)	-0.7	-0.508	-0.5	-0.408
E_{BD}(-MV/cm)	14.5	14.5	15.3	11.6
J(-A/cm2) Vg= -1V	1.10×10^{-7}	1.26×10^{-7}	7.19×10^{-8}	1.85×10^{-6}

(a)

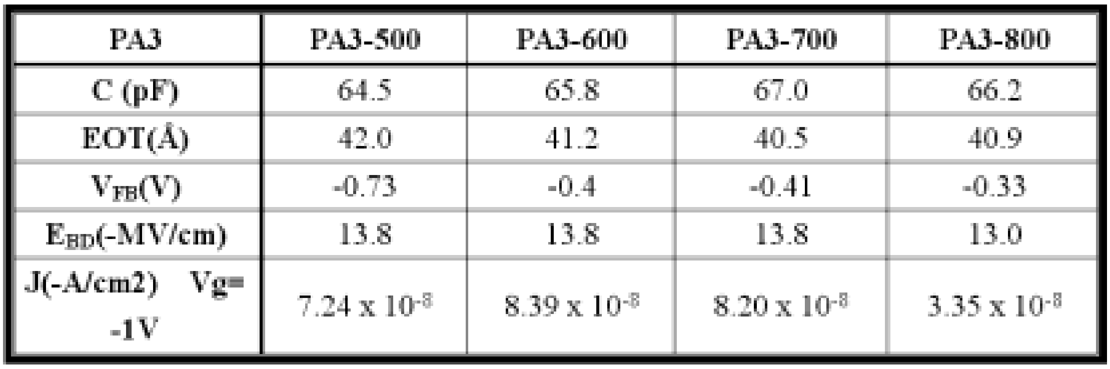
AP5	AP5-500	AP5-600	AP5-700	AP5-800
C (pF)	49.7	51.7	51.3	51.0
EOT(Å)	54.6	52.5	52.9	53.1
V_{FB}(V)	-0.75	-0.59	-0.46	-0.44
E_{BD}(-MV/cm)	13.8	14.0	14.2	14.2
J(-A/cm2) Vg= -2V	5.98×10^{-9}	6.25×10^{-8}	9.17×10^{-9}	7.26×10^{-9}
Φ_B (eV) (gate injection)	2.91	3.09	3.10	3.05
Φ_B (eV) (sub. injection)	2.09	2.45	2.34	2.41

(b)

AP7	AP7-500	AP7-600	AP7-700	AP7-800
C (pF)	32.7	33.3	33.4	34.0
EOT(Å)	82.8	81.2	81.3	79.8
V_{FB}(V)	-0.83	-0.64	-0.541	-0.383
E_{BD}(-MV/cm)	13.7	14.1	13.7	14.4
J(-A/cm2) Vg= -3V	1.15×10^{-7}	6.70×10^{-8}	3.21×10^{-8}	5.86×10^{-9}
Φ_B (gate injection)	2.96	3.17	3.26	3.34
Φ_B (sub. injection)	2.58	2.71	2.70	2.63

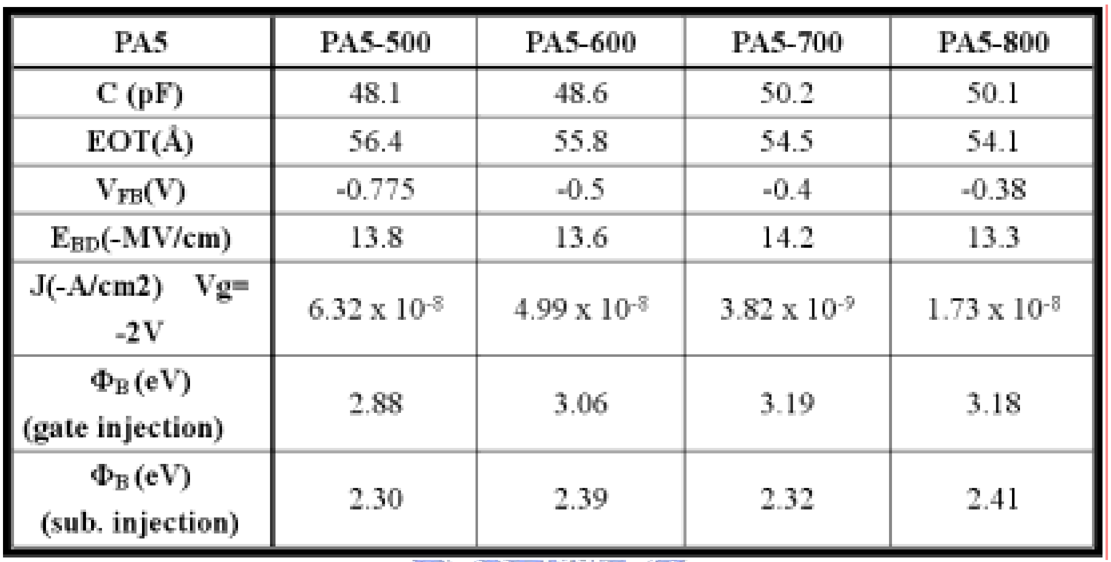
(c)

Table 6.3 characteristics of full nickel silicide gate capacitors based on n^+ a-Si/p-Si by various RTA conditions of (a) 35Å (b) 50Å (c) 75Å-thick SiO_2



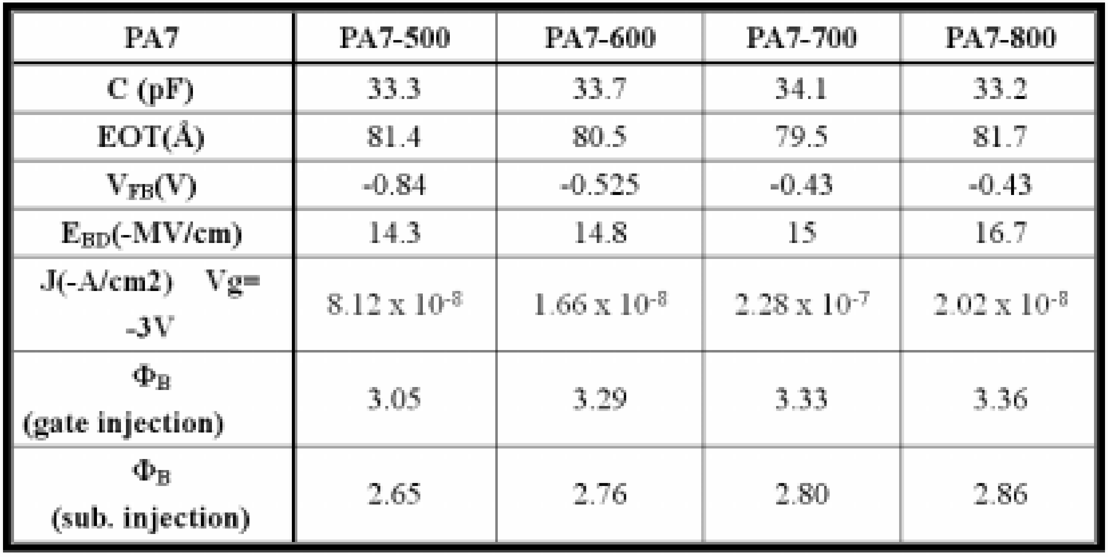
PA3	PA3-500	PA3-600	PA3-700	PA3-800
C (pF)	64.5	65.8	67.0	66.2
EOT(Å)	42.0	41.2	40.5	40.9
V_{FB}(V)	-0.73	-0.4	-0.41	-0.33
E_{BD}(-MV/cm)	13.8	13.8	13.8	13.0
J(-A/cm2) Vg= -1V	7.24×10^{-8}	8.39×10^{-8}	8.20×10^{-8}	3.35×10^{-8}

(a)



PA5	PA5-500	PA5-600	PA5-700	PA5-800
C (pF)	48.1	48.6	50.2	50.1
EOT(Å)	56.4	55.8	54.5	54.1
V_{FB}(V)	-0.775	-0.5	-0.4	-0.38
E_{BD}(-MV/cm)	13.8	13.6	14.2	13.3
J(-A/cm2) Vg= -2V	6.32×10^{-8}	4.99×10^{-8}	3.82×10^{-9}	1.73×10^{-8}
Φ_B (eV) (gate injection)	2.88	3.06	3.19	3.18
Φ_B (eV) (sub. injection)	2.30	2.39	2.32	2.41

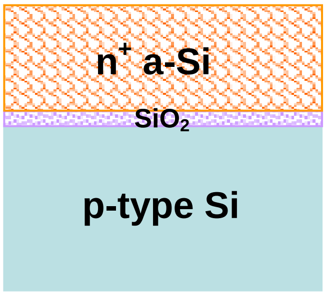
(b)



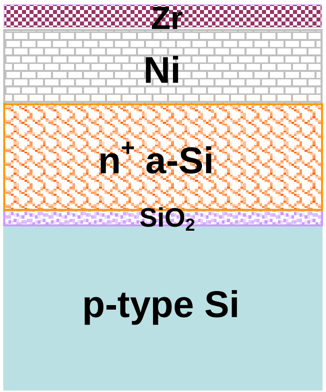
PA7	PA7-500	PA7-600	PA7-700	PA7-800
C (pF)	33.3	33.7	34.1	33.2
EOT(Å)	81.4	80.5	79.5	81.7
V_{FB}(V)	-0.84	-0.525	-0.43	-0.43
E_{BD}(-MV/cm)	14.3	14.8	15	16.7
J(-A/cm2) Vg= -3V	8.12×10^{-8}	1.66×10^{-8}	2.28×10^{-7}	2.02×10^{-8}
Φ_B (gate injection)	3.05	3.29	3.33	3.36
Φ_B (sub. injection)	2.65	2.76	2.80	2.86

(c)

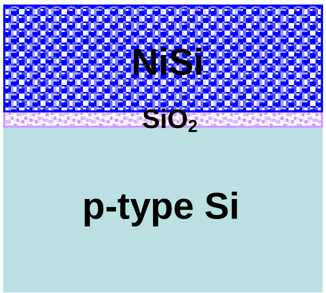
Table 6.4 characteristics of full nickel silicide gate capacitors based on p-Si/n^+ a-Si by various RTA conditions of (a) 35Å (b) 50Å (c) 75Å-thick SiO_2



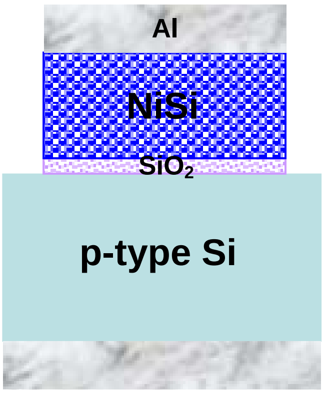
3. RCA clean
4. dilute O2 dry oxidation : 35, 50 and 75Å
5. PH_3 in-situ doped a-Si : 600Å (IA)



1. dopant activation : RTA 900°C, 30s
2. deposition by Dual E-gun : Ni(450Å) and Zr(100Å)



6. silicidation : RTA 500-800°C, 20s
7. unreacted Ni removement : (H_2SO_4+H_2O_2)



8. Sputter Al : 5000Å (Top electrode)
9. Wet etching for gate region
10. Sputter Al : 5000Å (Back electrode)

Fig. 6.16 Key process flow and schematics of the full nickel silicide MOS capacitor formation with Zr capping.

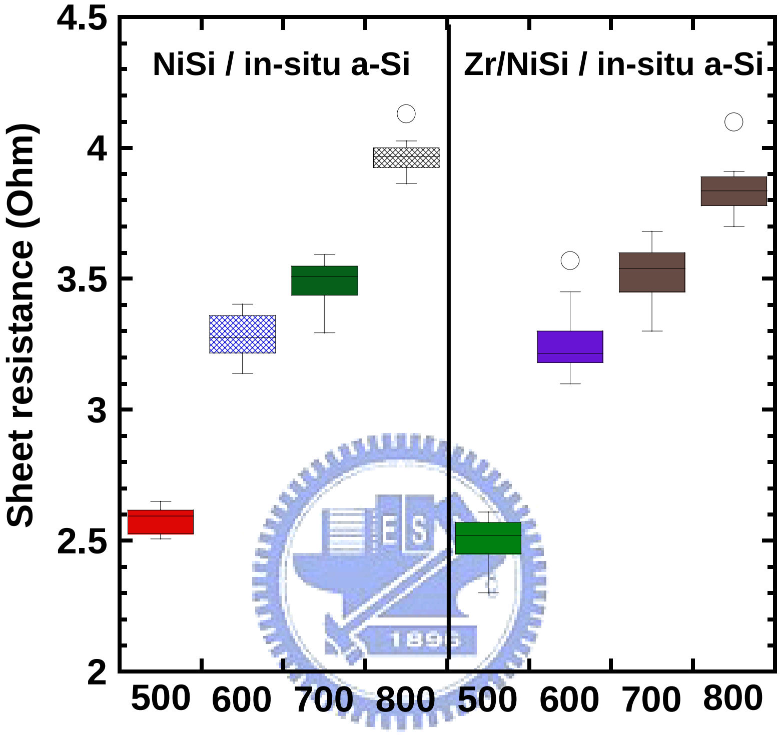


Fig. 6.17 Sheet resistance vs. RTA temperature for full nickel silicide gate capacitor and thoes with Zr capping.

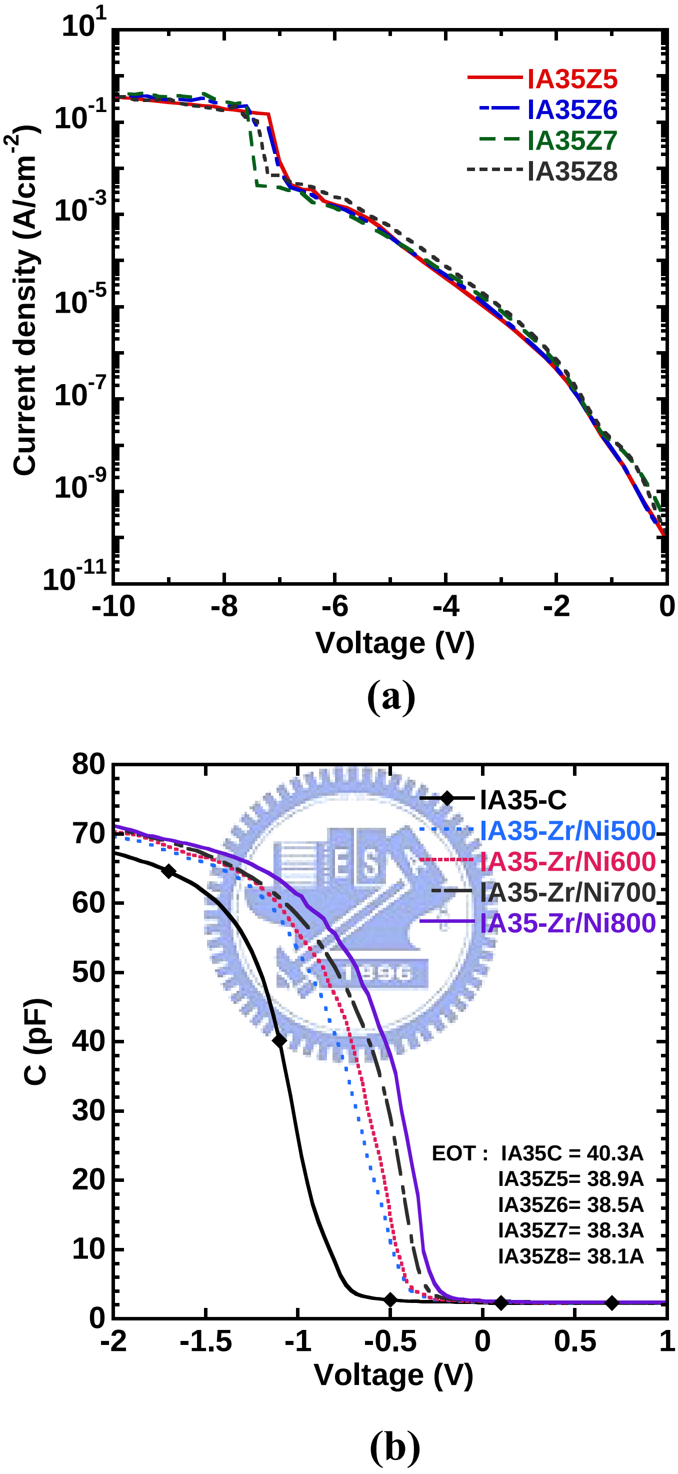
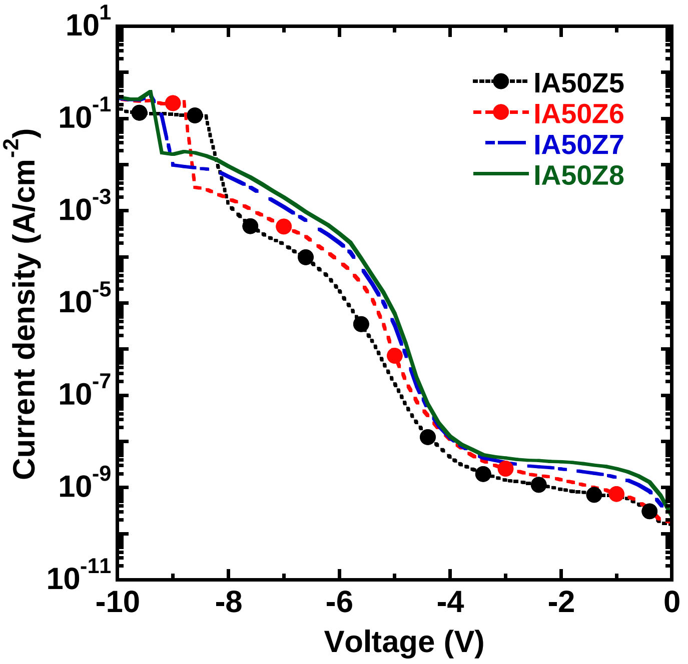
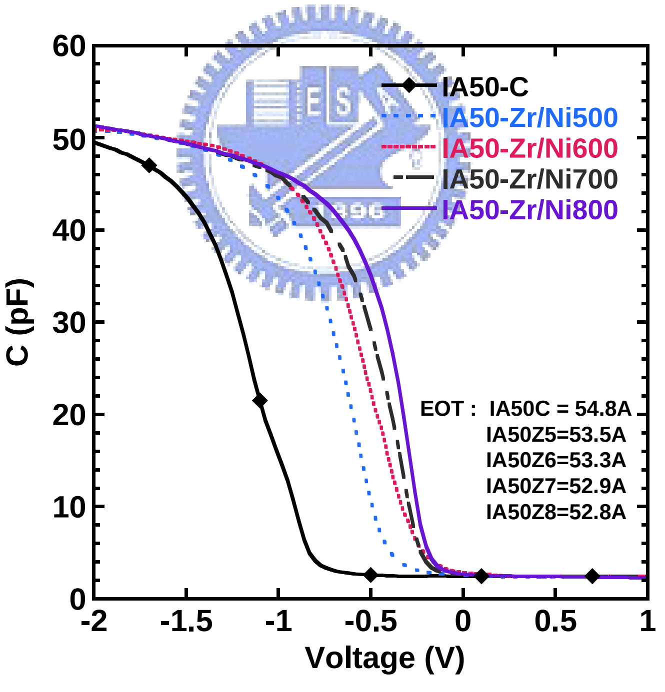


Fig. 6.18 (a) High frequency capacitance versus gate voltage plot (b) Gate leakage current density versus gate voltage of the full nickel silicide n^+ a-Si/SiO$_2$ (35Å) structure with Zr capping by different silicidation conditions.



(c)



(d)

Fig. 6.18 (c) High frequency capacitance versus gate voltage plot (d) Gate leakage current density versus gate voltage of the full nickel silicide n^+ a-Si/SiO$_2$ (50Å) structure with Zr capping by different silicidation conditions.

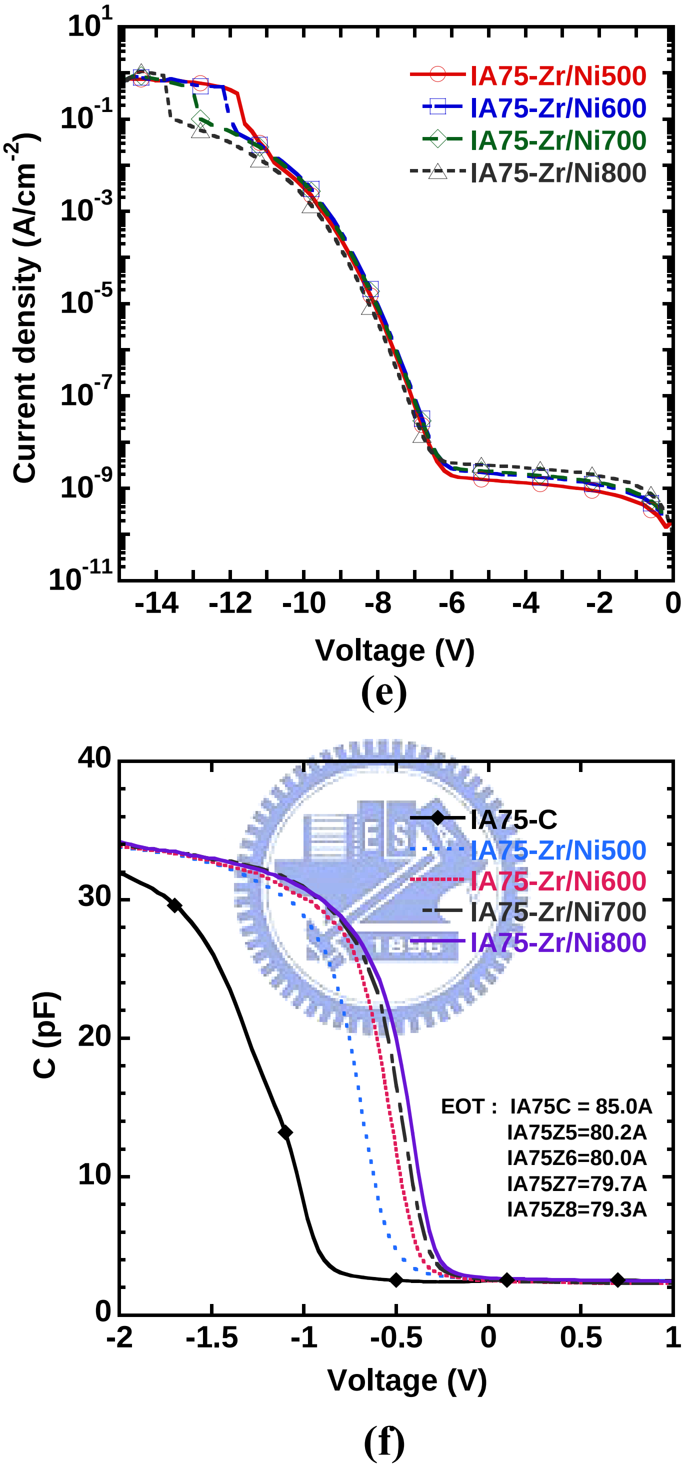
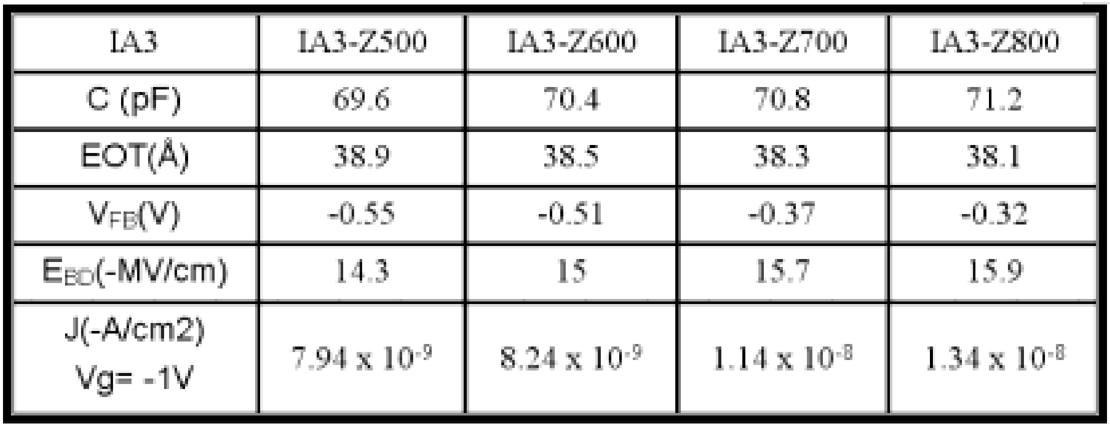
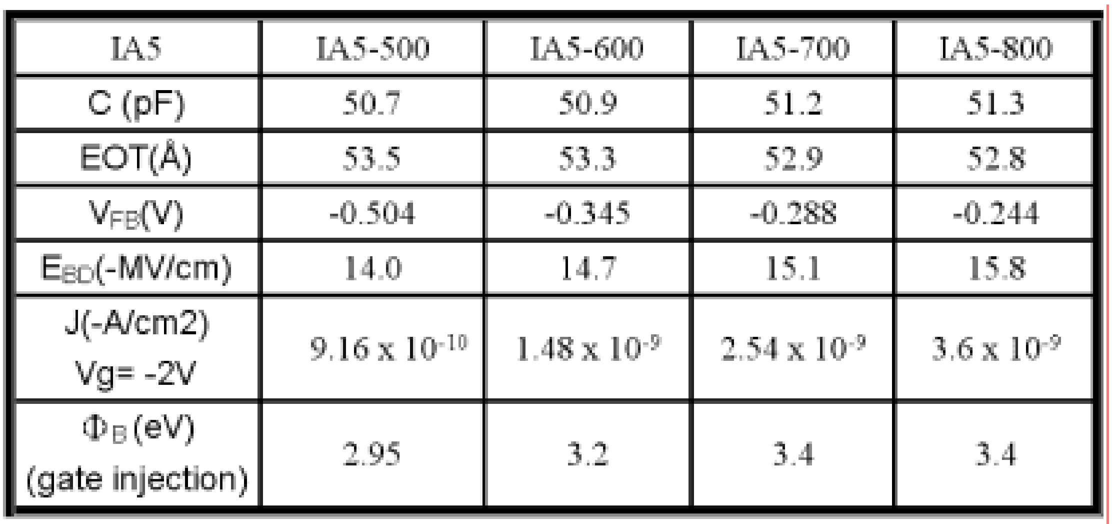


Fig. 6.18 (e) High frequency capacitance versus gate voltage plot (f) Gate leakage current density versus gate voltage of the full nickel silicide n^{+} a-Si/SiO$_2$ (50Å) structure with Zr capping by different silicidation conditions.



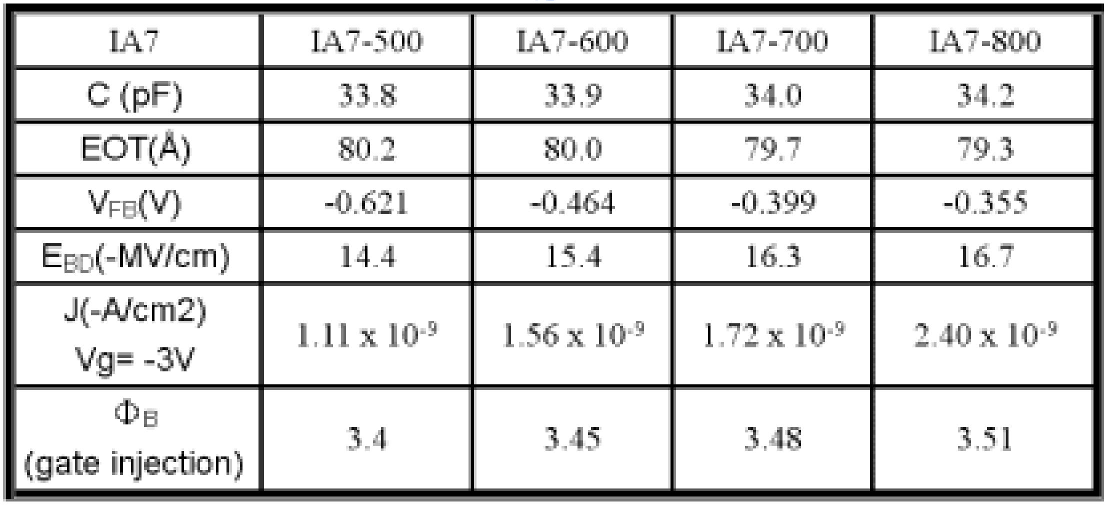
IA3	IA3-Z500	IA3-Z600	IA3-Z700	IA3-Z800
C (pF)	69.6	70.4	70.8	71.2
EOT(Å)	38.9	38.5	38.3	38.1
V_{FB}(V)	-0.55	-0.51	-0.37	-0.32
E_{BD}(-MV/cm)	14.3	15	15.7	15.9
J(-A/cm2) Vg= -1V	$7.94 x 10^{-9}$	$8.24 x 10^{-9}$	$1.14 x 10^{-8}$	$1.34 x 10^{-8}$

(a)



IA5	IA5-500	IA5-600	IA5-700	IA5-800
C (pF)	50.7	50.9	51.2	51.3
EOT(Å)	53.5	53.3	52.9	52.8
V_{FB}(V)	-0.504	-0.345	-0.288	-0.244
E_{BD}(-MV/cm)	14.0	14.7	15.1	15.8
J(-A/cm2) Vg= -2V	$9.16 x 10^{-10}$	$1.48 x 10^{-9}$	$2.54 x 10^{-9}$	$3.6 x 10^{-9}$
Φ_B (eV) (gate injection)	2.95	3.2	3.4	3.4

(b)



IA7	IA7-500	IA7-600	IA7-700	IA7-800
C (pF)	33.8	33.9	34.0	34.2
EOT(Å)	80.2	80.0	79.7	79.3
V_{FB}(V)	-0.621	-0.464	-0.399	-0.355
E_{BD}(-MV/cm)	14.4	15.4	16.3	16.7
J(-A/cm2) Vg= -3V	$1.11 x 10^{-9}$	$1.56 x 10^{-9}$	$1.72 x 10^{-9}$	$2.40 x 10^{-9}$
Φ_B (gate injection)	3.4	3.45	3.48	3.51

(c)

Table 6.5 characteristics of full nickel silicide gate capacitors based on in-situ doped a-Si with Zr capping by various RTA conditions of (a) 35Å (b) 50Å (c) 75Å-thick SiO_2

Structure		V_{FB}(V)	$\lvert E_{BD} \rvert$ (MV/cm)	J(-A/cm2) Vg= -1,2,3V	Φ_B (gate injection)
RTA (500°C)	**IA3**	-0.7	14.2	5.08×10^{-8}	--
	IA3-Z	-0.55	14.3	7.94×10^{-9}	--
	AP3	-0.7	14.5	1.10×10^{-7}	--
	PA3	-0.73	13.8	7.24×10^{-8}	
RTA (800°C)	**IA3**	-0.383	14.5	1.81×10^{-7}	--
	IA3-Z	-0.32	15.9	1.34×10^{-8}	--
	AP3	-0.408	11.6	1.85×10^{-6}	--
	PA3	-0.33	13.0	3.35×10^{-8}	--
RTA (500°C)	**IA5**	-0.716	14.0	4.53×10^{-8}	3.08
	IA5-Z	-0.504	14.0	9.16×10^{-10}	2.95
	AP5	-0.75	13.8	5.98×10^{-9}	2.91
	PA5	-0.775	13.8	6.32×10^{-8}	2.88
RTA (800°C)	**IA5**	-0.29	14.7	1.36×10^{-8}	3.30
	IA5-Z	-0.244	15.8	3.6×10^{-9}	3.4
	AP5	-0.44	14.2	7.26×10^{-9}	3.05
	PA5	-0.38	13.3	1.73×10^{-8}	3.18
RTA (500°C)	**IA7**	-0.74	14.4	3.92×10^{-8}	3.15
	IA7-Z	-0.62	14.4	1.11×10^{-9}	3.4
	AP7	-0.83	13.7	1.15×10^{-7}	2.96
	PA7	-0.84	14.3	8.12×10^{-8}	3.05
RTA (800°C)	**IA7**	-0.408	16.3	1.35×10^{-8}	3.35
	IA7-Z	-0.355	16.7	2.40×10^{-9}	3.51
	AP7	-0.38	13.7	5.86×10^{-9}	3.34
	PA7	-0.43	16.7	2.02×10^{-8}	3.36

Table 6.6 Comparison of electrical characteristics with different gate structures and various oxide thickness at RTA 500°C and 800°C.

Chapter 7

Conclusions and Recommendations for Future Works

7.1 Conclusions

In a word, this dissertation is the feasibility study of nickel silicide integration into the formation process of an ultra shallow junction and a full silicide gate. Major contributions of each subject in this work are summarized as follows.

First, we have investigated the thermal stability of nickel silicide with a Zr cap layer, and compared with conventional Ti capped nickel silicide. An improved thermal stability of nickel silicide can be obtained without the degradation on sheet resistance even after the silicidation treatment as high to 850ºC. Through this Zr cap method, the temperature of phase transformation from NiSi to $NiSi_2$ will be shifted which is proven by XRD spectra. And a smooth interface of silicide/Si can be obtained even after high silicidation temperature which is demonstrated by TEM images. Those benefits are attributed to the suppression of oxygen incorporation during the high temperauter silicidation process.

Next, combined our proposed nickel silicide with the p^+/n junction, a diffusion current dominated junction with high activation energy can be obtained due to the good capability of Zr thin film. One of the major causes for thoes benefits should be attributed to the suppression of oxygen contamination by adding a Zr cap which can be proved by SIMS analysis. Consequently, the generation of oxygen-related defects can be effectively retarded and a defect-less junction can be achieved.

Third, due to the advantage of well-controlled silicide depth by introducing a Zr cap, an 30nm ultra shallow junction with nickel silicide was carried out. As expected, owing to above mentioned advantages by adding a Zr cap, nickel silicide applied to the formation of ultra shallow junction to reduce the parasitic resistance can be realized for nano-scale device technology.

Third, in order to eliminate the damages from implantation and avoid transient enhanced diffusion (TED) or channeling effect (CE), PH_3 plasma doped method was performed for the formation of damage-less ultra shallow junction. Due to the theory of PH_3 plasma doped method, the low surface concentration is the major issue to overcome. Although the introduced oxide cap can effectively raise the surface dopant concentration, the junction depth will be increased which may be due to the effect of oxygen enhanced diffusion (OED). Besides, the excessive annealing time will enhance the defect generation and result in the increase of leakage current. Thus, a defect less ultra shallow junction formation by PH_3 plasma doped can be achieved by short activation time.

Finally, we have observed the behavior of nickel silicide gate based on different gate structures. Full nickel silicide gate structure on undoped a-Si shows a poor thermal stability which may be due to the excess nickel at the interface of gate/SiO_2. For nickel silicide gate capacitor based on in-situ doped a-Si, phosphorus in the gate region will be accumulated at the interface of gate/SiO_2 and be a barrier for the diffusion of nickel which will result in the improvement on oxide reliability. But the stack structure can't effectively suppress the excess nickel diffusion by extra grain boundary at the n^+ a-Si / p-Si interface as expected. Besides, a slight degradation on device reliability will be observed owing to the less phosphorus concentration in stack gate structure compared with n^+ a-Si gate structure. Thus, full nickel silicide gate combined with phosphorus incorporation and Zr capped on NiSi still possesses potential for future device application.

In conclusion, nickel silicide with appropriate improvement on its thermal stability is still the major candidate for nano-scale device application.

7.2 Recommendations for Future Works

There are some topics that are suggested for future work.

(1) Study the contact resistance of Zr capped on NiSi system.

(2) Use B_2H_6 gas for p_+/n shallow junction formation and combine with NiSi.

(3) Study the interaction of boron and Ni, and investigate its impact on V_{FB}, Φ_m, and gate oxide reliability.

(4) Integrate the nickel silicide process into the MOSFET fabrication procedures and investigate its influence on device performance and reliability.

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Investigation of Nickel Silicide Application toward Nano-scale MOS Device Technology

Publication List

I. International Journal:

[1] **T. L. Lee**, M. Z. Lee, T. F. Lei and C. L. Lee, "Improvement of Junction Leakage by Using a Zr Cap Layer on 30nm Ultra-Shallow Nickel-Silicide Junction," *Journal of the Electrochemical Society (JES)* accepted at 28 July, 2004

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[3] **T. L. Lee**, C. Y. Chen, J. W. Lee, T. F. Lei and C. L. Lee, "Improvement of Thin Gate Dielectrics Reliability by High Temperature Oxidation using N_2O and O_2 Ambient," *WSEAS Transactions on Electronics (WTE)*, vol. 1, pp. 145-149, January 2004.

II. International Letter:

[1] **T. L. Lee**, J. W. Lee, M. C. Lee, T. F. Lei and C. L. Lee, "Highly reliable nickel silicide formation with a Zr capping layer," *Electrochemical and Solid-State Letters (ESSL)*, vol. 6, no. 5, pp. G66-G68, May 2003.

III. International Conference:

[1] **T. L. Lee**, T. F. Lei and C. L. Lee, "Improvement of Junction Leakage of Nickel Silicided Junction by a Novel Zr Capping Layer," *11th Canadian Semiconductor Technology Conference (CSTC)***,** *Ottawa*, *Canada*, 18-22 Aug. 2003.

[2] **T. L. Lee**, C. Y. Chen, J. W. Lee, T. F. Lei and C. L. Lee, "Improvement of Thin Gate Dielectrics Reliability by High Temperature Oxidation using N_2O and O_2 Ambient," 4th WSEAS International Conference *(WSEAS)*, April 2004**.**

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