國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

具多閘極之修正蕭基位障電晶體及氮化鈦奈米晶粒記憶體之研究

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摘要

隨著製程技術的蓬勃發展，互補式金氧半電晶體和非揮發性記憶體不斷地成功微縮。然而，若持續在這些元件上使用傳統式的平坦結構設計，一些不可避免的問題將會愈來愈嚴重。因此，不僅在邏輯元件或是記憶體元件上，多閘極結構都已經被提出來用以改善元件的表現。在多閘極金氧半電晶體上，一種在源汲極接面設計上進行改良的修正蕭基位障源汲極接面電晶體已被提出來改善電晶體特性，除了可以提高驅動電流、降低外部阻抗，並可以保有原先蕭基位障電晶體所具備的優點，例如：增加短通道效應的免疫力及降低汲極引發能帶降低效應(drain-induced barrier lowing)。但是，到目前為止，對於修正蕭基位障電晶體來說，仍有許多富有價值性的深入分析需要被探討。在非揮發性記憶體上，浮動閘的設計已經被預測將會改良至電荷侷限儲存(charge trapping)的結構設計，例如改用金屬奈米晶粒。因此，如何將多閘極結構與金屬奈米晶粒的儲存結構設計整合在一起，亦是非常有價值性的探討。在本論文中，吾人對於多閘極修正蕭基位障

電晶體之分析和多閘極氮化鈦金屬奈米晶粒記憶體之製備與特性做了深入的探討。

首先，利用測量元件的溫度效應，蕭基位障與修正蕭基位障電晶體的電流傳導機制被探討，並發現傳導機制主要受到蕭基位障的高度與長度來決定，而這些參數都會受到製程及外加電場的影響。在蕭基位障電晶體上，電流傳導在小閘極偏壓下會是由熱放射(thermionic emission)或穿透(tunneling)機制來主宰，而當在足夠大閘極偏壓下，將轉變由漂移擴散(drift-diffusion)機制主導。而在修正蕭基位障電晶體上，因為在源汲極延伸區域(SDE)有非常薄且高濃度的接面來有效地壓抑蕭基位障，因此，隨著閘極電壓增加，電流傳導機制會由熱放射至穿透轉變再轉變成漂移擴散方式來變化，而這些傳導機制的轉換點亦可以有效地用來評估修正蕭基位障接面形成的好壞。另外，這些轉換點通常發生在大於臨限電壓 1 V 左右的位置，代表在小閘極偏壓下，修正蕭基位障仍然存在並影響著電流傳導。

吾人並且提出了改良式外部負載方法用以萃取在修正蕭基位障電晶體上具有電壓相依性的源極端入射電阻(source injection resistance)。利用此方法分析觀察得到，在小偏壓下，此入射電阻隨(V_{GS}-V_{th}-$0.5V_{DS}$)增加，呈現指數等級下降，但在大偏壓下，將會停止下降並飽和在其外部串聯阻抗之值。這表示了源極端的修正蕭基位障會主宰著電流直到外加偏壓足夠大到完全壓抑此蕭基位障為止。而且，不同的熱預算的影響亦可用此方法觀察，若元件具有不足的後離子植入矽化物之(post-ITS)退火，在小偏壓下會有明顯較大的串聯阻抗。並且，此種方法亦可有效地用來判定修正蕭基位障的效率。

並且，我們亦成功製作出使用了 P^+高功函數多晶矽閘極和氧化鋁高介電常數阻擋層之奈米尺度的三閘極氮化鈦奈米晶粒非揮發記憶體，並探討不同的電荷

侷限捕捉層設計之影響。首先，此元件具有大記憶窗口達到 5.2 伏特且具有很好的耐久度表現。並且，對於不同厚度的氮化鈦沾濕層(wetting layer)、後續沉積退火(post deposition annealing)的時間和不同的阻擋層厚度對於記憶特性的影響亦有研究。此次製作出的氮化鈦奈米晶粒直徑皆小於三奈米，如此會導致強烈的庫倫阻斷效應(Coulomb blockage effect)並影響寫入/抹除速度和保存能力(retention)。並且，經過 10^3 秒的偏壓後，很小的閘極電壓擾動(gate disturbance)與讀取偏壓擾動(read disturbance)亦可以達成。

最後，在此奈米尺度三閘極氮化鈦奈米晶粒非揮發記憶體測量中，吾人在關閉反向讀取(reverse read)狀態下的源極電流上發現到一種不尋常但有趣的電流調變現象。經過不同的偏壓條件操作後，這個電流調變的現象可以回覆到原先的電流等級，並可來回操縱，表現出含有兩種狀態的可再現電阻調變現象。另外，此現象可與操作在開啟狀態下的非揮發記憶體特性合併展現出具有兩位元(dual-bit)操作方式的可能性。而且，藉由更進一步地分析其電流組成、儲存能力表現、溫度效應、元件尺寸效應(area effect)和閘極疊層設計的影響後，吾人推測出一個可能在局部電荷侷限捕捉層產生或阻斷導電細絲(conducting filaments)而引發此電流調變現象的操作模型。

總而言之，利用變溫測量和我們提出的改良式外部負載方法，在修正蕭基源汲極電晶體上與閘極偏壓相關的電流傳導機制與源極端入射電阻分別被探討分析。多閘極氮化鈦奈米晶粒非揮發記憶體亦被實現並具有良好的特性可做為微縮之參考，並且發現了一個可重複操作的關閉電流調變現象，以及討論了其可能發生的原因。

A Study on the Modified Schottky Barrier (MSB) FETs and TiN Nanocrystal Memories with Multi-Gate Structure

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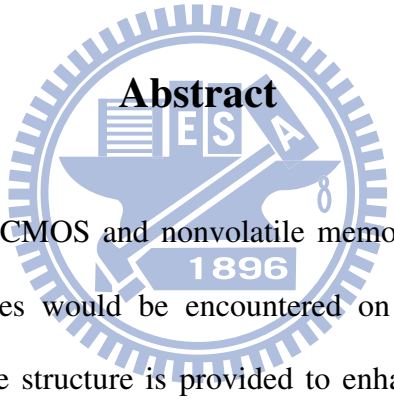

Abstract

As the technology of CMOS and nonvolatile memory continuously scale down, several unpreventable issues would be encountered on the classical planar device structure. Hence, multi-gate structure is provided to enhance the device performance either on the logic device or on the flash memory. For the multi-gate MOSFETs, modified Schottky barrier (MSB) source/drain junction are proposed to apply on the MOSFETs to improve the driving current and reserve the advantages of SB MOSFETs, such as the immunity of short channel effect and less drain-induced barrier lowing effect. However, some further analyses on the MSB MOSFETs are still required. For nonvolatile memory, the floating gate structure is projected to migrate to the charge trapping devices, such as the metal nanocrystal. Hence, the integration of metal nanocrystals and multi-gate structure is worthy to investigate. In this dissertation,

multi-gate modified Schottky barrier MOSFETs and multi-gate metal TiN nanocrystal memory are investigated.

The current transportation mechanisms of the SB and MSB source/drain MOSFETs are investigated firstly. By measuring the temperature effect, it reveals that the current transportation mechanism is mainly dominated by the length and height of SB, which depends on the processes and the external supplying electric-field. For SB MOSFETs, the current transportation mechanisms start from the tunneling or thermionic emission at low gate bias and eventually become to the drift-diffusion at sufficient high gate bias. For MSB MOSFETs, since the source-side SB is suppressed by the ultra-thin and highly doped SDE, the current transportation mechanism changes from the thermionic emission to tunneling and then to drift diffusion as the gate voltage increases. Moreover, the changing point of mechanism is a good indicator to evaluate the efficiency of MSB junction. In addition, the changing point of mechanism is around at V_G-V_{TH} = 1 V, indicating the MSB still exists at low gate bias condition.

Then, the modified external loading method is proposed to extract the bias-dependent source injection resistance of the MSB source/drain MOSFETs. The injection resistance is observed to exponential proportion to the (V_{GS}-V_{th}-$0.5V_{DS}$) at low electric field but saturates to the source/drain resistance of conventional MOSFET at sufficient high electric field, suggesting the source-side MSB would dominate the current flow until the external bias large enough to suppress the barrier. The effect of the thermal budget of MSB process on the source injection resistance can observe. Sample without sufficient post-ITS annealing exhibits much higher R_{SD} at low bias region. Moreover, this method also provides a good method to evaluate the efficiency of MSB junction.

The charge trapping layer engineered nano-scale tri-gate TiN nanocrystal memories with high-k Al_2O_3 blocking layer and high work function P^+ gate electrode are successfully fabricated and investigated. Large memory window equals to 5.2 V and good endurance performance are achieved. Memory characteristics of various samples with different TiN wetting layer thickness, post deposition annealing time, and blocking oxide thickness are also investigated. The TiN nanocrystals are smaller than 3 nm, which induces strong Coulomb blockade effect to influence the P/E speed and retention property. Furthermore, the gate disturbance and read disturbance are also measured with very small charge migrations after 10^3 sec. stressing bias.

Finally, an abnormal but interesting current modulation is observed in the off-state source current at reverse read on the nano-scale tri-gate TiN nanocrystal memory. By different pulse bias conditions, this current modulation can switch back and forth, showing a reproducible resistive switching behavior with two different states. Possible dual-bit operation is demonstrated. From the further analyses on the current components, the retention properties, the temperature effect, the area effect, and the engineering of gate stacks, a possible switching model is supposed due to the generation and rupture of the conducting filaments in the local charge trapping layer.

To summarize, the current transportation mechanism and the bias dependent source injection resistance of the MSB MOSFETs are investigated by measuring the temperature effect and our provided modified external loading method, respectively. The multi-gate SAMOS-type TiN nanocrystal nonvolatile memories are realized and an interesting repeatable current modulation is demonstrated and the possible reason is discussed.

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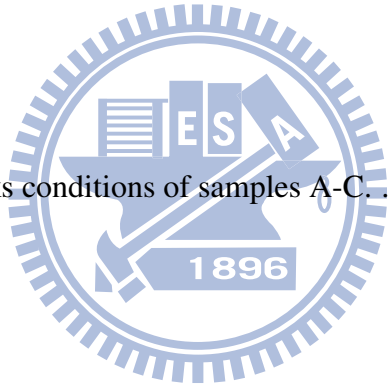

Figure Captions

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Chapter 1

Introduction

1.1 Scaling of CMOS Technology

In the past four decades, the rapid growth in electronics industry mainly bases on the successful scaling of each technology generation, providing better device performance, faster circuit operation speed, lower power consumption, and lower production cost. This scaling trend mostly follows the Moore's law, which is an empirical observation by Gordon Moore in 1965 that the transistor density of integrated circuit doubles and the feature size of device are scaled by a factor of 0.7 every eighteen months [1]. Nowadays, the 32 nm generation node has been achieved. However, from the recently prediction of International Technology Roadmap for Semiconductor (ITRS), to obtain higher driving current and lower leakage current in the conventional planar bulk CMOS, some critical challenges would be encountered in the further downscaling. These challenges mainly originate from the gate leakage, source-drain leakage, and junction leakage. Figure 1-1(a) presents the schematic cross-sectional view of the typical planar MOSFET. To get good gate controllability and suppress the short-channel effect (SCE), the gate-to-channel capacitance (C_{gc}) must be maximized. It can be achieved by thinning the thickness of SiO_2 gate dielectric. However, the extremely large gate leakage current due to the direct tunneling would stop the SiO_2 scaling. This problem can be solved by using the high

dielectric constant (high-k) material as the gate dielectric layer to replace the SiO_2 thin film, since thicker film can be utilized to achieve the same C_{gc}. Today, the equivalent oxide thickness (EOT) is around 0.95 nm for high-performance (HP) logic applications [2]. Additionally, high channel doping and shallow junction are also required to suppress source-drain leakage current to maintain tolerable short-channel effect. However, the doping concentration is too high (~10^{19} cm^{-3}) for the continued scaling device, resulting in degraded carrier mobility, low driving current, high junction leakage current induced by band-to-band tunneling, and severe gate-induced drain leakage (GIDL) [1-3]. Therefore, from the forecast in ITRS 2009, non-classical CMOS structures with better electrostatic controllability will be implemented in the future, such as ultra-thin body (UTB) MOSFET [4-5] and multi-gate FET (MuGFET) [6-8].

Comparing to the structure of the planar bulk CMOS, UTB MOSFET, the silicon-on-insulator (SOI) substrate has an extremely thin silicon layer for the channel and a buried SiO_2 layer for isolation. It can effectively control the potential through the whole channel and suppress source-drain leakage current and short-channel effect without requiring the highly dosed punch-through implantation. Hence, UTB MOSFET with low-doped channel obtains larger carrier mobility, enhanced current drive, and better immunity to short channel effect. It has been predicted that the UTB structure would be applied as the technology node below than 27 nm for high performance logic applications [2]. The schematic structure of the UTB SOI MOSFET is shown in Figure 1-1(b). To suppress the issues originate from the SCE and to achieve better turn-off characteristic, thinner Si layer is required as scaling of the gate length. However, some critical challenges will be encountered for the further scaling. Normally, from the experimental observation, the Si thickness is demanded

approximately one third of the gate length for the UTB SOI MOSFET, indicating the required Si thickness thinner than 10nm as the gate length shorter than 30 nm [9]. However, as the Si thickness thinner than 10nm, quantum confinement effect arises and it causes an increasing of threshold voltage as compare to a thick-body device [10]. Moreover, the variation in the body thickness is another concern. Hence, controllability of the threshold voltage and the thickness of ultra-thin body are the most critical issues for the UTB SOI MOSFET. Hence, owing to the aforementioned reasons, the limitation of UTB structure is forecasted around 22 nm node for the CMOS applications. Then, multi-gate FETs (MuGFET) have been thought as a possible solution for the further scaling as the technology node beyond 22 nm [2].

1.2 Multi-gate structure

MuGFETs such as FinFET [6-7,10-11], gate-all-around (GAA) FET [12-14] include two or more than two gates, exhibiting better gate controllability to fully deplete Si channel and show significant reduction of short channel effect as compare to the UTB SOI MOSFET. Therefore, multi-gate structure is expected to replace the UTB structure in the future and become the most possible solution for the further scaling. Moreover, high channel doping is not required to suppress S/D leakage current and hence higher mobility can be obtained. Additionally, the FinFETs include a double-gate or tri-gate structure with relative similar processes and structure, except the hard-mask layer on the top of Si fin. When the hard-mask layer stays on the top of Si fin, double-gate FinFET is realized, implying two sidewall channel will turn-on in the on-state; when the hard-mask layer is removed on the top of Si fin, tri-gate FinFET is accomplished, indicating two sidewall channel and one top channel will

turn-on in the on-state. Figures 1-2(a) and 1-2(b) present the schematic structures of the double-gate and the tri-gate FinFETs. Moreover, FinFETs have better driving current and lower off-current with compatible processes and similar layout design to that of the classical bulk CMOS. Furthermore, the effective channel width is increased by the double-gate structure or tri-gate structure. For example, the effective width in the double-gate FinFET is double of the fin-height. Then, the effective width in the tri-gate FinFET is double of the fin-height plus the fin-width. Hence, the effective driving current can be enhanced by using this three-dimensional structure.

1.3 Modified Schottky Barrier (MSB) Multi-gate FETs

Following the future scaling steps, as the multi-gate structure employing in the device, the fin width gets much narrower, thus much higher series resistance would exist outside of the channel since lacking of deep source/drain (S/D) regions to achieve lower enough resistance by forming metal silicide [15]. Hence, to effectively minimize parasitic source/drain resistance (R_{SD}) and increase the driving current, some techniques have been presented, such as the raised source/drain [16] and low barrier silicide S/D [17-20]. The raised S/D realizes by the selective epitaxial growth (SEG) on the Si channel can effective thicken the Si fin and obtain lower R_{SD}. However, applying this technique on the MuGFETs has high complexity and it may induce some failures during the process, such as agglomeration, facet, or bridging effect [11]. The low resistive S/D silicide is fabricated by the thermal reaction of the metal and the Si layers at S/D regions, which would produce Schottky barriers (SB) at the interface of the silicide and the Si-channel and lower the external R_{SD}. Moreover,

SB MOSFETs have been proposed with highly suitable for future nano-scale devices because it offers benefits such as easy processing, low thermal budget, and small external resistance of S/D [17-20]. Hence, devices with low Schottky barrier height silicides, such as PtSi for p-MOSFET [17, 18], and $ErSi_{2-x}$ [17, 19], $YbSi_{2-x}$ [20], and $DySi_{2-x}$ [18] for n-MOSFET have already been demonstrated. However, the SB MOSFETs still have some drawbacks. First, using complementary S/D silicides for nFET and pFET requires a dual-silicide process, inducing much more complexity and large modification for mass production. Furthermore, owing to the existence of the SB in the turn-on state, smaller on-state driving current (I_{on}) is exhibited than that of the conventional pn junction MOSFETs. The existed SB not only affects the driving capability but also degrades the performance of the sub-threshold swing [21]. Moreover, the problem of high turn-off current (I_{off}) of SB MOSFETs comes from the carrier injection at the drain side is the other drawback [22]. Furthermore, in all of the present silicides, the extracted SB height are around 0.15 eV – 0.25 eV, which is not low enough to outperform the performance of the convention CMOS with highly doped S/D junction because the requirement of the SB height is smaller than 0.1 eV [23]. Therefore, by using the metal S/D to lower external S/D series resistance in the MuGFET needs another solution to overcome the aforementioned issues.

Recently, modified Schottky barrier (MSB) MOSFETs have been proposed to improve the driving current and reserve the advantages of SB MOSFETs such as better short channel effect and less drain-induced-barrier-lowering [10, 11]. The MSB junction is a Schottky junction with a very thin but high doping concentration layer located at silicide/Si-channel interface which not only drastically improves the driving capability by reducing and thinning the SB at source junction but also can significantly suppress the off-state leakage current due to the thick SB at drain

junction. Hence, am-bipolar current-voltage characteristics can be significantly improved by using the MSB technology.

The MSB junction can be accomplished by either implantation-to-silicide (ITS) method or dopant segregation (DS) method [10, 11]. For the ITS method, dopants are implanted to the pre-formed S/D silicide regions follows a low temperature annealing to migrate the dopants to the silicide/Si interface to form the ultrathin and steep MSB junction. As contrary, for the DS method, the dopants are implanted before silicidation. During silicidation, the dopants are segregated at the silicide/Si interface and construct the MSB junction. Hence, the formation of MSB junction only requires low temperature process which is suitable for the integration of high-k/metal gate stacks. Moreover, the carrier injection velocity enhancement associated with the velocity overshoot is observed in the dopant-segregated MOSFETs [24]. Besides, several literatures have been devoted to evaluate the efficiency of the MSB junction. Recently, M. Zhang et al. reported that the effective Schottky barrier height can be reduced to about 0.1 eV at high gate bias [25]. However, the gate bias dependence of the series resistance in the MSB MOSFETs and the current transport mechanisms of the MSB MOSFETs have not been reported.

1.4 Multi-Gate nanocrystal memories (NCM)

As the scaling trend of the CMOS logic device has been forecasted that the planar structure may be replaced by the three-dimensional structure, i.e. multi-gate. The nonvolatile memory has been considered to modify its planar structure to the three-dimensional architecture since some challenges would be encountered. Moreover, because the multi-gate structure offers some advantages such as better gate

controllability and higher gate coupling ratio, multi-gate structure seems to be a candidate for the future application of nonvolatile memory. However, some inevitable issues would rise as scaling, which is mainly originated from the storage material and it is suspected to change another applicable material as the new storage node. Hence, firstly, we should focus on what happened in the past of the nonvolatile memory and what it is predicted to change.

1.4.1 Evolution of the planar nonvolatile memory

In the past years, the market of the nonvolatile memory has huge growth and it makes the Flash memories as one of the fastest growing semiconductor products. Lots of commercial products need the Flash memory, mostly relating to the mobile digital consumer application, such as MP3, PDA, digital cameras and so on. The current state-of-the-art for the flash memory is based on the floating gate (FG) technology which has nearly 100% market share [26]. The FG flash stands out owing to its highly compatibility with the CMOS technology and good scalability to achieve extremely high density. In 1967, D. Kahng and S. M Sze invented the first floating gate non-volatile memory (NVM) at Bell Lab [27]. Till today, various kinds of floating gate memories have been proposed and the process technology progressed rapidly. Figure 1-3(a) shows the schematic cross-section structure of the basic floating gate flash memory. The device structure is mainly based on the MOSFET with a modified gate stacks, including a control gate (CG) and a floating gate separated by a dielectric layer. The storage node is the isolated floating gate. Floating gate NVM has the advantages of large memory window, high program/erase (P/E) speed, and good reliability. Moreover, for the commercial applications, the FG NVM can satisfy the requirements of high density, low power consumption, smaller form factor, and lower system cost

[26]. Hence, flash memory becomes one of the fastest growing semiconductor technologies and provides hundreds of portable electronic products in last decade. However, the International Technology Roadmap for Semiconductors (ITRS) forecasts that the scaling limitation of the conventional floating gate memories is around 25 nm node [28] and some challenges would encounter in the near future. The main issue is un-scalable tunneling oxide thickness. For allowing charge transfer to the FG at reasonable voltage, the tunneling oxide layer must be thin enough but for maintaining acceptable retention performance in read-mode or off-state, the tunneling oxide layer have to be thick enough to avoid charge loss. Therefore, higher operation voltages are needed for present FG technology and the thickness of tunneling oxide layer is predicted to keep at 6-7 nm and it is very hard to decrease [28]. Moreover, since the floating gate is a conductive material, the stored charges will leak easily if the tunneling oxide is damaged during operations. The gate coupling ratio (GCR) is required to larger than 0.6. It can be enlarged by thinning the thickness of inter-poly dielectric (IPD) layer, however, for the data retention requirement, the thickness of IPD decreases slowly as scaling. Moreover, the short channel effect becomes more critical as scaling. The increasing floating gate to floating gate coupling effect is another urgent issue for the continually closing floating gate memory cell. Therefore, the FG technology is projected to migrate to the charge trapping devices with discrete traps for charge storage, such as SONOS (Silicon/ Oxide/ Nitride/ Oxide/ Silicon) and nanocrystal (NC) structures [28].

Since the cross-talk between thin charge-trapping layers is negligible, the largest advantage of the charge-trapping devices is the immune of the floating gate to floating gate cross-talk effect. Moreover, the charge-trapping devices also enable to utilize thinner gate stacks to enhance gate controllability and suppress short channel effect

[29]. Figure 1-3(b) shows the schematic cross-section structure of the SONOS-type flash memory. The storage node is the silicon nitride layer. Theoretically, when the CG is biased positively, electrons would tunnel through the tunneling oxide layer and be trapped by the deep level in the silicon nitride layer. As contrary, when the CG is biased negatively, the trapped electrons would be ejected from the nitride layer and back into the channel. Therefore, the SONOS-type memory which stores charges in the discrete trap node of silicon nitride layer exhibits improved retention performance so that the tunneling oxide thickness can be reduced to increase the P/E speed and to decrease the operation voltage [30-31]. Besides, some advanced SONOS memories such as bandgap engineered SONOS (BE-SONOS) and TANOS (TaN/ Al_2O_3/ Nitride/ Oxide/ Silicon) have demonstrated high P/E speed and attracted much attention for applying in the future NVM [32, 33]. BE-SONOS use triple ultra-thin layers of ONO as the tunnel dielectric layer. Each ultra-thin layer is around 1-2 nm thick. Because the smaller energy barrier of Si_3N_4 layer to hole, the injection efficiency of hole in the erasing-mode can be enhanced. Moreover, the effective thickness of the tunneling dielectric layer still thick enough to prevent the escaping of the trapped electrons in the read-mode or off-state. The retention performance still performs well. TANOS uses metal gate electrode and high-k blocking dielectric layer to prevent back-side gate injection when erasing and obtained fast erasing speed. Additionally, the usage of high-k dielectric can enhance the electric field at tunneling oxide layer and improve the GCR to enhance the programming efficiency. Unfortunately, the erase saturation [34] and unwanted migration of stored charges in the nitride layer [35] are the major drawbacks and can be observed in all SONOS-type memories. Therefore, nanocrystal memories have been thought as promising candidates for the future NVM application.

Nanocrystal memory which uses various materials as the storage node such as Si, Ge, HfO_2, Pt, Ag, Au, Ni and TiN has been proposed and became another possible solution for the future NVM applications [36-44]. Figure 1-3(c) shows the schematic cross-section structure of the nanocrystal flash memory. Owing to each nanocrystal is theoretically isolated by surrounding dielectric, nanocrystal memory have better charge storage ability than SONOS-type memory. The lateral migration of storage charges can be theoretically removed and the crosstalk behavior between the bits of source-side and drain-side would not be observed. Therefore, it may show better performance of the multi-bit operation [36]. Moreover, thinner tunneling oxide can be used to improve P/E speed and reduced P/E operation voltage without degrading the retention performance. In 2002, Liu et al. proposed the design principle and fabrication process of metal nanocrystal memories [36-37]. The self-assembled nanocrystal can be formed easily by deposition a thin metal layer followed by a rapid thermal annealing (RTA). Besides, metal nanocrystals have more work function engineering ability, higher density of state around Fermi-level, stronger coupling to the Si-channel, and better size scalability than the semiconductor nanocrystals have. Although lots of literatures were proposed to provide various techniques to form nanocrystals, one of the main challenges of nanocrystal memory is the storage node property which means the nanocrystal quality. She et al. has proposed in 2003 that the optimized size of Ge nanocrystal is 5 nm with concerning about the effect of Coulomb blockade and quantum confinement [38]. Therefore, how to formation nanocrystals with high density, constant size, and uniform distribution [39-41] is required to be concerned, especially when the device getting smaller and smaller. Some variation of the nanocrystal's property in different device would induce unstable storage data in these nanocrystal memories.

1.4.2 Multi-gate charge trapping Flash memory

The multi-gate structure is not only a possible solution for the CMOS logic device but also very attractive for the future application of memory devices, especially for the nonvolatile memory. For the non-volatile memory (NVM), it has thicker gate dielectric, implying worse channel controllability. Hence, multi-gate structure, such as FinFET structure, can be utilized to suppress the short channel effect and improve the gate coupling ratio by wrapping sidewall FG. In 2003, Xuan et al. have proposed the first FinFET SONOS flash memories with excellent program/erase characteristics and good reliability performance [45]. Recently, multi-gate field effect transistors (MuGFETs) were predicted as one of the most potential solution for the NAND Flash beyond the 25 nm node, and various SONOS-type and nanocrystal memories have been fabricated with multi-gate structure [28]. It has been reported that the multi-gate memory cell can achieve excellent short-channel effect controllability, high driving current, low leakage current, good programming inhibition, and large numbers of nanocrystals in one cell of nanocrystal memory [42-50]. Furthermore, the potential of a floating fin-type body is modulated in the multi-gate structure, differently from that in the single gate structure, exhibiting a longer charge retention time [43]. Additionally, multi-level operation [46] and dual-bit operation [47] in the FinFET SONOS-type flash memories are also achieved. Moreover, some technologies which utilized in the planar flash memory to improve the property are also applicable on the multi-gate FinFET Flash memories. Cho et al. has proposed that using high-k inter-poly dielectric layer as blocking layer can enlarge gate coupling ratio and then enhance programming/erasing efficiency [48]. In 2007, Hsu et al. presented the FinFET bandgap engineered BE-SONOS flash memory with better retention and

erase speed than that of FinFET SONOS [49]. The FinFET WN nanocrystals flash memory with Al_2O_3 high-k blocking layer and trapping layer engineering by adding extra nitride layer has been investigated. Owing to the additional trap sites in Si_3N_4, the memory window and the retention performance are improved [42]. Hence, multi-gate structure provides a selection to reduce the scaling limitation and it is an important candidate for further scaling of NVM. Therefore, both in the CMOS and NVM, this kind of three-dimensional structure displays extremely large possibility and scaling capability for the future applied technology.

1.5 Thesis Organization

In this dissertation, we mainly focus on the some possible solutions for the multi-gate MOSFET and multi-gate flash memory. In the first part, the influence by the existed Schottky barriers on a multi-gate MOSFET and a novel extraction method of the series resistance in MSB S/D MOSFET are also described. In the second part, a nano-scale multi-gate nanocrystal memory has been demonstrated as a promising candidate for the NAND flash memory application.

In the first chapter of this dissertation, some overviews of the CMOS revolution and its challenges will be mentioned. Non-planar device structure, such as multi-gate structure, is highly considered for the future application on the logic CMOS transistors and the Flash memory. The advantage and the shortcoming for using multi-gate are also described. For CMOS devices, multi-gate structure and metal S/D are forecasted for the further scaling. Modified Schottky barrier S/D junction is one possible solution for the future S/D engineering. For flash memory, multi-gate

structure is also a candidate. Moreover, the possible enhancement of the charge storage element and its revolution are also reviewed.

In chapter 2, current transport mechanisms of SB S/D MOSFETs and MSB S/D MOSFETs are investigated by measuring the temperature effect on current-voltage characteristics. The current transport mechanism varied while different gate voltage was biased. Moreover, the SB height would impact the transport mechanism largely in different gate bias conditions.

In chapter 3, we provide a novel method for extracting gate voltage dependent source injection resistance of MSB MOSFETs. The relationship between the injection resistance and the gate bias will be discussed. Furthermore, this method provides a good indicator to evaluate the efficiency of the MSB junction directly.

In chapter 4, the fabrication and the electrical characteristics of a nano-scale n-channel tri-gate TiN nanocrystal non-volatile memory has been demonstrated. The Al_2O_3 high-k blocking layer and the P^+ high work function gate electrode were used to obtain low operation voltage and suppress the back-side injection effect, respectively. TiN nanocrystals were formed by annealing the TiN/Al_2O_3 nano-laminates which were deposited by an atomic layer deposition system. Moreover, the charge-trapping layer has engineered with different TiN wetting layer thickness, post deposition annealing time, and blocking oxide thickness. The size of the nanocrystal affects the performance largely. Moreover, the memory characteristics and the reliability performance of these samples have been demonstrated.

In chapter 5, we demonstrate an interesting resistive switching phenomenon in the turn-off state in the naon-scale multi-gate TiN nanocrystal memory. This electric-bias-induced reproducible change of reverse read current are observed after pulsing at the conditions of CHE and BTBHH, normally utilizing for the NOR flash operations.

This abnormal leakage current will be investigated and possible mechanism will be discussed.

Finally, in chapter 6, we will give some important conclusions. Moreover, some further works which are worthy for further study will be suggested.

References

[1] L. Risch, "Pushing CMOS beyond the roadmap," *Solid-state Electron.*, vol. 50, no. 4, pp. 527-535, 2006.

[2] Process Integration, Devices and Structures in International Technology Roadmap for Semiconductors 2009 edition, pp. 1-10, 2009.

[3] L. Chang, Y.-K. Choi, J. Kedzierski, N. Lindert, P. Xuan, J. Bokor, C. Hu, and T.-J. King, "Moore's Law Lives on," *IEEE Circuits and Devices Mag.*, vol. 19, no. 1, pp. 35-42, 2003.

[4] Y.-K. Choi, K. Asano, N. Lindert, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Ultrathin-Body SOI MOSFET for Deep-Sub-Tenth Micron Era," *IEEE Electron Devices Lett.*, vol. 21, no. 5, pp. 254-255, 2000.

[5] K. Uchida, J. Koga, R. Ohba, T. Numata, and S. Takagi, "Experimental Evidences of Quantum-Mechanical Effects on Low-field Mobility, Gate-channel Capacitance, and Threshold Voltage of Ultrathin Body SO1 MOSFETs," in *IEDM Tech. Dig.*, 2001, pp. 633-636.

[6] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King, J. Bokor, C. Hu, M.-R. Lin, and D. Kyser, "FinFET scaling to 10 nm gate length," in *IEDM Tech. Dig.*, 2002, pp. 251-254.

[7] N. Lindert, L. Chang, Y.-K. Choi, E. H. Anderson, W.-C. Lee, T.-J. King, J. Bokor, and C. Hu,"Sub-60-nm Quasi-Planar FinFETs Fabricated Using a Simplified Process," *IEEE Electron Devices Lett.,* vol. 22, no. 10, pp. 487-489, 2001.

[8] R. H. Yuan, A. Ourmazd, and K. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," *IEEE Trans. Electron Devices,* vol. 39, no. 7, pp. 1704-1710, 1992.

[9] J. Chen, R. Solomon, T.-Y. Chan, P. K. KO, and C. Hu, "Threshold Voltage and C-V Characteristics of SO1 MOSFET's Related to Si Film Thickness Variation on SIMOX Wafers," *IEEE Trans. Electron Devices,* vol. 39, no. 10, pp. 2346-2353, 1992.

[10] B.-Y. Tsui, C.-P. Lin, "A novel 25-nm modified schottky-barrier FinFET with high performance," *IEEE Electron Device Lett.,* vol. 25, no. 6, pp. 430-432, 2004.

[11] A. Kaneko, A. Yagishita, K. Yahashi, T. Kubota, M. Omura, K. Matsuo, I. Mizushima, K. Okano, H. Kawasaki, T. Izumida, T. Kanemura, N. Aoki, A. Kinoshita, J. Koga, S. Inaba, K. Ishimaru, Y. Toyoshima, H. Ishiuchi, K. Suguro, K. Eguchi, Y. Tsunashima, "High-Performance FinFET with Dopant-Segregated Schottky Source/Drain," in *IEDM Tech. Dig.*, 2006, pp. 893-896.

[12] K. H. Yeo, S. D. Suk, M. Li, Y. Yeoh, K. H. Cho, K.-H. Hong, S. Yun, M. S. Lee, N. Cho, K. Lee, D. Hwang, B. Park, D.-W. Kim, D. Park, and B.-I. Ryu, "Gate-All-Around (GAA) Twin Silicon Nanowire MOSFET (TSNWFET) with 15 nm Length Gate and 4 nm Radius Nanowires," in *IEDM Tech. Dig.*, 2006, pp. 539-542.

[13] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D.-L. Kwong, "High-Performance Fully Depleted Silicon Nanowire (Diameter ≤ 5 nm) Gate-All-Around CMOS Devices," *IEEE Electron Device Lett.,* vol. 27, no. 5, pp. 383-386, 2006.

[14] J. W. Peng, S. J. Lee, G. C. A. Liang, N. Singh, S. Y. Zhu, G. Q. Lo, and D. L. Kwong, "Improved carrier injection in gate-all-around Schottky barrier silicon nanowire field-effect transistors," *App. Phys. Lett.,* vol. 93, no. 7, p. 073503, 2008.

[15] A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak, and K. De Meyer, "Analysis of the parasitic S/D Resistance in Multiple-Gate FETs," *IEEE Trans. Electron Devices,* vol. 52, no. 6, pp. 1132-1140, 2005.

[16] J. Kedzierski, M. Ieong, E. Nowak, T. S. Kanarsky, Y. Zhang, R. Roy, D. Boyd, D. Fried, and H.-S. P. Wong, "Extension and source/drain design for high-performance FinFET devices," *IEEE Trans. Electron Devices,* vol. 50, no. 4, pp. 952-958, 2003.

[17] J. Kedziersk, P. Xuan, E. H. Andersonf, J. Bokor, T.-J. King, C. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime," in *IEDM Tech. Dig.*, 2000, pp. 57-60.

[18] S. Zhu, H. Y. Yu, S. J. Whang, J. H. Chen, C. Shen, C. Zhu, S. J. Lee, M. F. Li, D. S. H. Chan, W. J. Yoo, A. Du, C. H. Tung, J. Singh, A. Chin, and D. L. Kwong, "Schottky-Barrier S/D MOSFETs With High-K Gate Dielectrics and Metal-Gate Electrode," *IEEE Electron Device Lett.,* vol. 25, no. 5, pp. 268-270, 2004.

[19] M. Jang, Y.Kim, J. Shin, S. Lee, and K. Park, " A 50-nm-gate-length erbium-silicided n-type Schottky barrier metal-oxide-semiconductor field-effect transistor," *App. Phys. Lett.,* vol. 84, no. 5, pp. 741-743, 2004.

[20] R. T. P. Lee, A. E.-J. Lim, K.-M. Tan, T.-Y. Liow, G.-Q. Lo, G. S. Samudra, D. Z. Chi, and Y.-C. Yeo, "N-channel FinFETs With 25-nm Gate Length and Schottky-Barrier Source and Drain Featuring Ytterbium Silicide." *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 164-167, 2004.

[21] J. Knoch, M. Zhang, Q. T. Zhao, St. Lenk, S. Mantl, and J. Appenzeller, "Effective Schottky barrier lowering in silicon-on-insulator Schottky-barrier metal-oxide-semiconductor field-effect transistors using dopant segregation,"

App. Phys. Lett., vol. 87, no. 26, p. 263505, 2005.

[22] J. Knoch and J. Appenzeller, "Impact of the channel thickness on the performance of Schottky barrier metal–oxide–semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 81, no. 16, pp. 3082-3084, 2002.

[23] S. Xiong, T.-J. King, and J. Bokor, "A Comparison Study of Symmetric Ultrathin-Body Double-Gate Devices With Metal Source/Drain and Doped Source/Drain," *IEEE Trans. Electron Devices,* vol. 52, no. 8, pp. 1859-1867, 2005.

[24] A. Kinoshita, T. Kinoshita, Y. Nishi, K. Uchida, S. Toriyama, R. Hasumi, and J. Koga, "Comprehensive Study on Injection Velocity Enhancement in Dopant-Segregated Schottky MOSFETs," in *IEDM Tech. Dig.*, 2006, pp. 79-82.

[25] M. Zhang, J. Knoch, Q.T. Zhao, A. Fox, St. Lenk, and S. Mantl, "Low temperature measurements of Schottky-barrier SOI-MOSFETs with dopant segregation," *Electronics Letters,* vol. 41, no. 19, pp. 1085-1086, 2005.

[26] R. Bez, and A. Pirovano, "Non-volatile memory technologies: emerging concepts and new materials," *Materials Science in Semiconductor Processing,* vol. 7, no. 4-6, pp. 349-355, 2004.

[27] D. Kahng and S. M Sze, "A floating gate and its application to memory devices," *IEEE Trans. Electron Devices*, vol. 14, no. 9, p. 629, 1967.

[28] Process Integration, Devices and Structures in International Technology Roadmap for Semiconductors 2009 edition, pp. 13-20, 2009.

[29] J. Fu, N. Singh, K. D. Buddharaju, S. H. G. Teo, C. Shen, Y. Jiang, C. X. Zhu, M. B. Yu, G. Q. Lo, N. Balasubramanian, D. L. Kwong, E. Gnani, and G. Baccarani, "Si-Nanowire Based Gate-All-Around Nonvolatile SONOS Memory Cell," *IEEE Electron Device Lett.,* vol. 29, no. 5, pp. 518-521, 2008.

[30] M. H. White, D. A. Adams, and J. Bu, "On the go with SONOS," *IEEE Circuits and Devices Magazine*, vol. 16, no. 4, pp. 22-31, 2000.

[31] J. Bu, and M. H. White, "Effects of Two-step High Temperature Deuterium Anneals on SONOS Non-volatile Memory Devices," *IEEE Electron Device Lett.*, vol. 22, no. 1, pp. 17-19, 2001.

[32] H. T. Luo, S. Y. Wang, E. K. Lai, Y. H. Shih, S. C. Lai, L. W. Yang, K. C. Chen, J. Ku, K. Y. Hsieh, R. Liu, and C. Y. Lu, "BE-SONOS: A Bandgap Engineered SONOS with Excellent Performance and Reliability," in *IEDM Tech. Dig.*, 2005, pp. 547-550.

[33] C.-H. Lee, J. Choi, C. Kang, Y. Shin, J.-S. Lee, J. Sel, J. Sim, S. Jeon, B.-I. Choe, D. Bae, K. Park, and K. Kim, "Multi-Level NAND Flash Memory with 63 nm-node TANOS (Si-Oxide-SiN-Al2O3-TaN) Cell Structure," in *VLSI Symp. Tech. Dig.*, 2006, pp. 21-22.

[34] Gowrishankar L. Chindalore, *Member, IEEE*, Craig T. Swift, and David Burnett, *Member, IEEE,* "A New Combination–Erase Technique for Erasing Nitride Based (SONOS) Nonvolatile Memories," *IEEE Electron Device Lett.,* vol. 24, no. 4, pp. 257-259, 2003.

[35] T. Sugizaki, M. Kohayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka, "Novel Multi-bit SONOS Type Flash Memory Using a Highk Charge Trapping Layer," in *VLSI Symp. Tech. Dig.*, 2003, pp. 27-28.

[36] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal Nanocrystal Memories—Part I: Device Design and Fabrication," *IEEE Trans. Electron Devices,* vol. 49, no. 9, pp. 1606-1613, 2002.

[37] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal Nanocrystal

Memories—Part II: electrical characteristics," *IEEE Trans. Electron Devices,* vol. 49, no. 9, pp. 1614-1622, 2002.

[38] M. She, and T.-J. King, "Impact of Crystal Size and Tunnel Dielectric on Semiconductor Nanocrystal Memory Performance," *IEEE Trans. Electron Devices,* vol. 50, no. 9, pp. 1934-1940, 2003.

[39] J. J. Lee, and D. -L. Kwong, "Metal Nanocrystal Memory With High-k Tunneling Barrier for Improved Data Retention," *IEEE Trans. Electron Devices,* vol.52, no. 4, pp. 507-511, 2005.

[40] S. Maikap, P. J. Tzeng, H. Y. Lee, C. C. Wang, T. C. Tien, L. S. Lee, and M. -J. Tsai, "Physical and electrical characteristics of atomic layer deposited TiN nanocrystal memory capacitors," *Appl. Phys. Lett.,* vol. 91, no. 4, p. 043114, 2007.

[41] S. Choi, S. S. Kim, M. Chang, H. Hwang, S. Jeon, C Kim, "Highly thermally stable TiN nanocrystals as charge trapping sites for nonvolatile memory device applications," *Appl. Phys. Lett.,* vol. 86, no.12, p. 123110, 2005.

[42] Y. J. Ahn, J. -D. Choe, J. J. Lee, D. Choi, E. S. Cho, B. Y. Choi, S. -H. Lee, S. K. Sung, C. -H. Lee, S. H. Cheong, D. K. Lee, S. B. Kim, D. Park and B. I. Ryu, "Trap Layer Engineered FinFET NAND Flash with Enhanced Memory Window," in *VLSI Symp. Tech. Dig.*, 2006, pp. 88-89.

[43] K. Yanagidaira, M. Saitoh, and T. Hiramoto, "Enhancement of Charge Storage Performance in Double-Gate Silicon Nanocrystal Memories With Ultrathin Body Structure," *IEEE Electron Devices Lett.,* vol. 26, no. 7, pp. 473-475, 2005.

[44] C.-P. Lu, C.-K. Luo, B.-Y. Tsui, C.-H. Lin, P.-J. Tzeng, C.-C. Wang, and M.-J. Tsai, "Nanoscale Multigate TiN Metal Nanocrystal Memory Using High-*k* Blocking Dielectric and High-Work-Function Gate Electrode Integrated on

Silcon-on-Insulator Substrate," *Jap. J. Appl. Phys.,* vol. 48, p. 04C059, 2009.

[45] P. Xuan, M. She, B. Harteneck, A. Liddle, J. Bokor, and T.-J. King, "FinFET SONOS Flash Memory for Embedded Applications," in *IEDM Tech. Dig.*, 2003, pp. 609-612.

[46] M. Specht, U. Dorda, L. Dreeskornfeld, J. Kretz, F. Hofmann, M. Städele, R. J. Luyken, W. Rösner, H. Reisinger, E. Landgraf, T. Schulz, J. Hartwich, R. Kömmling, and L. Risch, "20 nm tri-gate SONOS memory cells with multi-level operation," in *IEDM Tech. Dig.*, 2004, pp. 1083-1085.

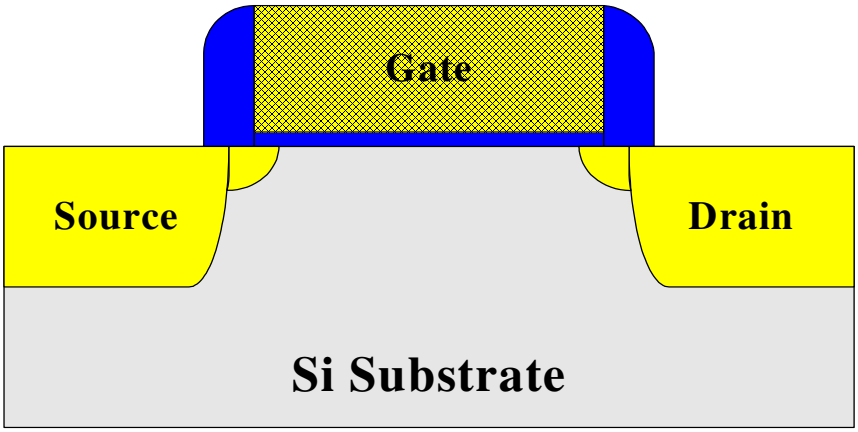
[47] M. Specht, R. Kömmling, F. Hofmann, V. Klandzievski, L. Dreeskornfeld, W. Weber, J. Kretz, E. Landgraf, T. Schulz, J. Hartwich, W. Rösner, M. Städele, R. J. Luyken, H. Reisinger, A. Graham, E. Hartmann, and L. Risch, "Novel Dual Bit Tri-Gate Charge Trapping Memory Devices," *IEEE Electron Devices Lett.,* vol. 25, no. 12, pp. 810-812, 2004.

[48] E. S. Cho, C.-H. Lee, T.-Y. Kim, S.-K. Sung, B. K. Cho, C. Lee, H. J. Cho, Y. Roh, D. Park, K. Kim and B.-I. Ryu, "Hf-silicate Inter-Poly Dielectric Technology for sub 70nm Body Tied FinFET Flash Memory," in *VLSI Symp. Tech. Dig.*, 2005, pp.208-209.

[49] T.-H. Hsu, H. T. Lue, Y.-C. King, J.-Y. Hsieh, E.-K. Lai, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, "A High-Performance Body-Tied FinFET Bandgap Engineered SONOS (BE-SONOS) for NAND-Type Flash Memory," *IEEE Electron Devices Lett.,* vol. 28, no. 5, pp. 443-445, 2007.

[50] F. Hofmann, M. Specht, U. Dorda, R. Kömmling, L. Dreskorndeld, J. Kretz, M. Städele, W. Rösner, and L. Risch, "NVM based on FinFET device structures," *Solid-State Electron.,* vol. 49, no. 11, pp. 1799-1804, 2005.

(a)



(b)

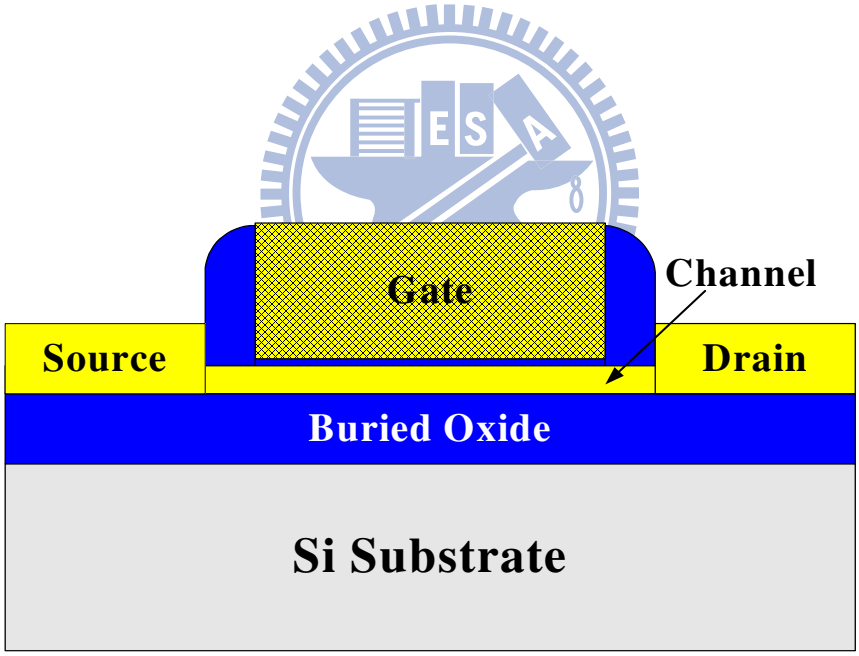
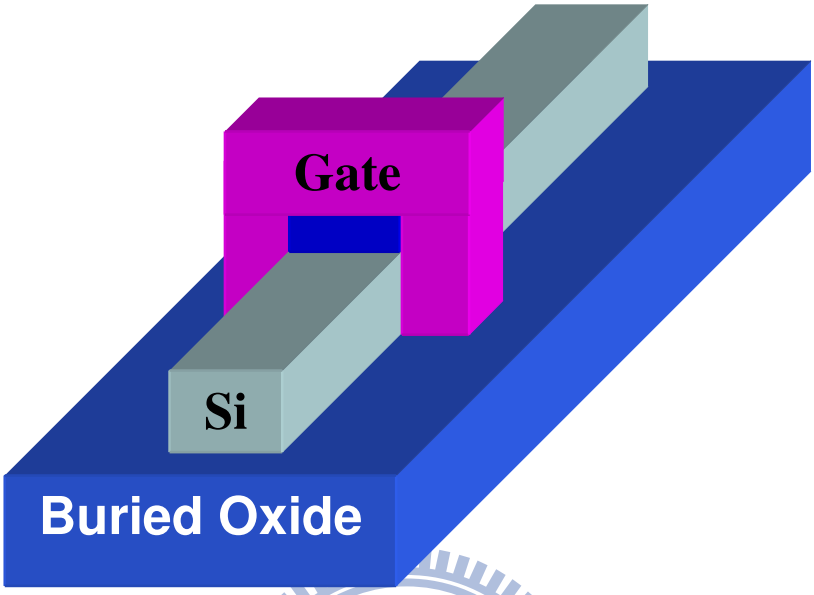


Fig. 1-1 Schematic cross-section views of (a) planar MOSFET, and (b) planar UTB SOI FET.

(a)



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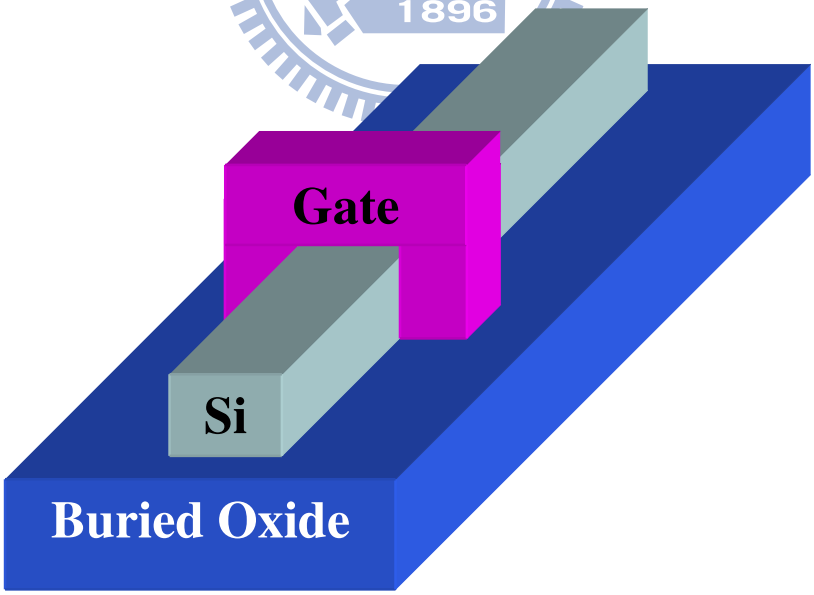
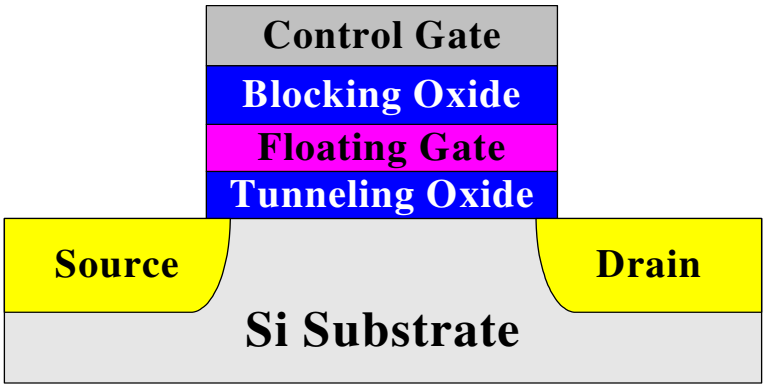
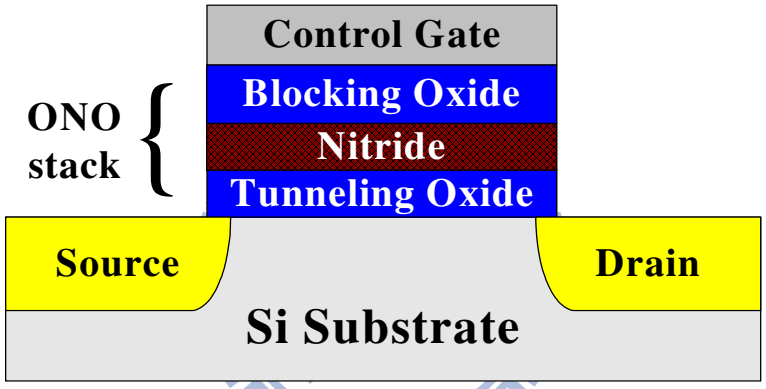


Fig. 1-2 Schematic structures of the FinFETs on SOI substrate, (a) double-gate FinFETs, and (b) tri-gate FinFETs.

(a)



(b)



(c)

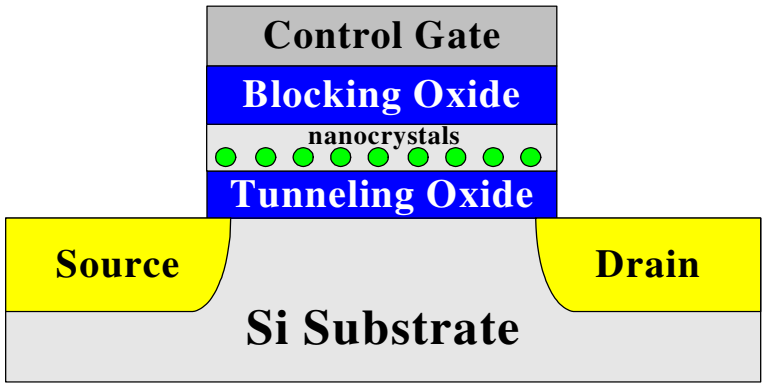


Fig. 1-3 Basic structure of (a) FG flash memory device, (b) SONOS flash memory device, and (c) nanocrystal flash memory device.

Chapter 2

Current Transportation Mechanisms of Schottky Barrier (SB) MOSFETs and Modified Schottky Barrier (MSB) MOSFETs

2.1 Introduction

From the prediction of ITRS Roadmap, it mentions that the metal gate electrode, high dielectric constant gate dielectric layer, and metal source/drain would be utilized to enhance the device performance and promote further scaling. The metal source/drain is normally achieved by using metal silicide which is easily formed by the thermal reaction of the metal and the Si layers at source/drain regions and thus the Schottky barriers (SB) were created at the interface between silicide and Si-channel. Hence, metal source/drain MOSFETs are usually called SB source/drain MOSFETs. Recently, SB source/drain MOSFETs have been proposed for future nano-scale devices because of easy processing, low thermal budget, small external resistance of source/drain, good drain-induced barrier lowing and better short channel effect. [1-4]. However, the SB MOSFETs still have some drawbacks. The first drawback of the SB MOSFETs is the smaller on-state driving current (I_{on}) than that of the conventional pn junction MOSFETs due to the existed SB between the silicide and the inverted channel. The existed SB not only affects the driving capability but also degrades the

performance of the sub-threshold swing [5]. Hence, low Schottky barrier height silicides, such as PtSi for p-MOSFET [1, 2], and $ErSi_{2-x}$ [1, 3], $YbSi_{2-x}$ [4], and $DySi_{2-x}$ [2] for n-MOSFET have been proposed to improve the driving capability. However, the complementary silicides for n-type and p-type MOSFETs suffers from the complex fabrication processes. In addition, the high I_{off} of SB MOSFETs comes from the carrier injection at the drain side is another drawback [6]. Kedzierski et al. introduced the FinFET architecture on silicon-on-insulator (SOI) and demonstrated low I_{off} ~ 1nA/μm for 20x25 nm^2 devices [1]. Moreover, adding a metal field-plate over the MOSFETs has been shown to be effective in reducing the I_{off} by suppressing back-injection from the drain contact, but it requires an additional voltage supply and sacrifices device density [8]. Therefore, the on/off characteristics of SB MOSFETs are both inferior to that of conventional pn junction MOSFETs.

Recently, modified Schottky barrier (MSB) MOSFETs has been proposed to overcome the drawbacks of SB MOSFETs [9-11]. The MSB junction is a Schottky junction with a very thin but high concentration layer located at the metal/Si interface. This high concentration layer could be accomplished by several methods, for example, implantation-to-silicide (ITS) method [9] and dopant segregation (DS) method [10-11]. Using these methods, the dopants can segregate to the silicide and silicon interface and form an ultra-thin but highly doped silicon layer which can not only lower the Schottky barrier height effectively in on-state to improve the Schottky limit for I_{on} but also can thicken the SB at the drain-side during off-state to reduce the I_{off}. Additionally, nickel monosilicide (NiSi) is a promising candidate as a contact metal. It exhibits low formation temperature, smaller Si consumption, and low silicide/Si contact resistance [12, 13], showing strong potential and suitable for the application of MSB MOSFETs. Tsui et al. has proposed high performance nano-scale MSB multi-

gate MOSFET with NiSi source/drain [9]. Furthermore, although the carrier injection velocity of the MSB MOSFETs fabricated by the DS method has been studied [14], the current transportation mechanism of MSB MOSFETs has not been reported. In this chapter, current transportation mechanisms of SB and MSB MOSFETs are investigated by measuring the temperature effect on the current-voltage characteristics. Current transportation mechanisms at different bias conditions are clarified.

2.2 Devices Fabrication

Various kinds of multi-gate MOSFETs have been fabricated with different source/drain engineering. They are (1) double gate SOI MOSFETs with SB source/drain were built and can operate as n-channel or p-channel devices depends on the bias conditions, (2) n-channel double-gate SOI MOSFETs with n^+ MSB source/drain junctions, and (3) p-channel tri-gate SOI MOSFETs with p^+ MSB source/drain. The detailed process steps would be mentioned in the following subsections.

2.2.1 Double-Gate MOSFETs with SB and n-MSB Source/Drain

Figure 2-1 shows the main process steps of the double-gate n-channel MSB MOSFET fabrication. The starting material is 6-inch SIMOX silicon-on-insulator (SOI) wafer with the nominal 50-nm-thick SOI layer and a 150-nm-thick buried oxide layer. The SOI layer is lightly boron doped and the doping concentration is around $1x10^{15}$ cm^{-3}. First, the Si layer was thinned down to 40 nm by thermal oxidation. A 50-nm-thick TEOS oxide was deposited in a low pressure chemical vapor deposition

system as hard-mask on the Si layer before active area definition so that only sidewall channel could be conducted. Then, Si fins in <110> direction were patterned by e-beam lithography and plasma dry etching. After removing the residue photo-resist, a 3-nm-thick SiO_2 layer was thermally grown as the gate dielectric. Poly-Si film of 150 nm thickness was deposited and doped by P_{31}^+ ion implantation at 40 keV to a dose of $5x10^{15}$ cm^{-2} followed by a rapid thermal activation at 1025°C for 10 sec. By employing the e-beam lithography and plasma dry etching again, the gate pattern was defined. Then, a 10-nm-thick SiO_2 and a 30-nm-thick Si_3N_4 composite spacer were formed and the device structure is shown in the Fig. 2-1(a). Following by the spacer formation, self-aligned nickel silicide process was then performed. A 22-nm-thick Ni film was deposited by the physical vapor deposition system followed by a two-step Ni-silicidation process to control the lateral growth length of Ni-silicide and prevent excess silicidation induced source/drain short circuit. The first step is performed in the vacuum chamber at 300°C for 60 min. and the Ni_2Si was formed at source/drain and the poly-Si gate regions. Then, after removing the residual un-reacted Ni film by hot H_2SO_4/H_2O_2 mixed solution, the second annealing step was performed in the rapid thermal annealing system at 600°C for 30 sec in N_2 ambient. During this step, since there is no excess Ni covers on the Si fin, the issue of excess silicidation would not occur and the source/drain region was converted into NiSi completely and the gate electrode became Ni-polycide structure, as shown in Fig. 2-1(b).

To form the n^+ MSB junction, P_{31}^+ ions were implanted to silicide at 20 keV to a dose of $5x10^{15}$ cm^{-2}, followed by a post-ITS furnace annealing at 600 °C for 30 min in N_2 ambient. During the post-ITS annealing step, phosphors atoms diffuse out of the silicide and pile up at the interface of silicide/Si-channel. Then, a very thin source-drain-extension (SDE) layer was formed after the post-ITS annealing step to modify

the SB property. Additionally, the thermal budget is largely reduced by utilizing the ITS method. Therefore, the device structure of the n-channel MSB MOSFETs is displayed in Fig. 2-1(c). Figure 2-1(d) shows the double-gate structure along the gate direction, implying only two sidewall channel would be conducted as device turns on. Moreover, the simple SB MOSFETs were fabricated by neglecting the ITS process step. The schematic structure is shown in Fig. 2-1(b). According to the applied bias conditions, n-channel or p-channel SB MOSFETs can be achieved.

2.2.2 Tri-Gate MOSFETs with p-MSB Source/Drain

For the fabrication of tri-gate p-channel MSB MOSFET, the process flow is quite similar to that of double-gate n-channel MSB MOSFET which is mentioned above, excluding different type of implanted dopants and no hard-mask layer. Figure 2-2 illustrates the main process steps of tri-gate p-channel MSB MOSFETs. After active layer definition, a 4-nm-thick SiO_2 was thermally grown as the gate dielectric followed by the deposition of Poly-Si film of 50 nm thickness. Then, after Gate patterning, a 10-nm-thick SiO_2 and a 30-nm-thick Si_3N_4 composite spacer was formed, as shown in Fig. 2-2(a). Two-step Ni-salicide process was performed to convert the source/drain into the NiSi completely. Since the thickness of poly-Si gate is similar to that of the source/drain Si layer, Ni fully-silicided (FUSI) gate structure was obtained, as shown in Fig. 2-2(b).

To form the MSB junction, BF_2^+ ions were implanted to silicide at 15 KeV to a dose of $1x10^{15}$ cm^{-2} followed by a post-ITS furnace annealing at 600 °C for 30 min. Therefore, the p-channel MSB MOSFETs was built and a very thin SDE layer was formed after the post-ITS annealing step to modify the SB property, as shown in Fig.

2-2(c). Figure 2-2(d) shows the tri-gate structure alone the gate direction, indicating two sidewall channel and one top channel would be conducted as device turns on.

2.3 Results and Discussion

2.3.1 Basic Current-Voltage Characteristics

Figure 2-3(a) and (b) present the typical transfer characteristics of n-channel SB MOSFET and p-channel SB MOSFET with gate length equals to 5 μm and fin width equals to 80 nm, respectively. Clearly, the ambipolar property and the extremely high leakage current in the off-state were observed. Additionally, smaller on-state current, poor sub-threshold swing, and larger threshold voltage are also obtained. In Fig. 2-4(a) and (b) which show the typical output characteristics of n-channel SB MOSFET and p-channel SB MOSFET, respectively. The obvious sub-linear curves indicate large SB height at the source-side. These on/off behaviors can be easily explained by the schematic energy band diagram of n-channel SB MOSFET in Fig. 2-5 and p-channel SB MOSFET in Fig. 2-6. While operating in the on-state, owing to the thick SB existed at the source-side to block carriers flow, the electrons (n-channel) and holes (p-channel) are required to pass through the SB by the thermionic-emission and tunneling mechanisms. The SB at source-side dominates the carrier transportation, as shown in Fig. 2-5(a) and Fig. 2-6(a). Moreover, the existed SB not only affects the driving capability but also degrades the performance of the sub-threshold swing [5]. Therefore, comparing to the conventional pn junction MOSFETs, lower on-state current and poor subthreshold swing are expected. On the other hand, when biasing in the off-state, large number holes (n-channel) and electrons (p-channel) will tunnel

through the drain junction and induce abnormal high leakage current, as shown in Fig. 2-5(b) and Fig. 2-6(b). Hence, large off-state current and ambipolar behavior are obtained in SB MOSFETs.

For n-channel MSB MOSFET, since an ultra-thin n^+ SDE exists in the interface of NiSi/Si channel, the SB at source-side is thinned and the effective SB height is reduced to let the electrons tunnel through the SB more easily and enhance driving ability in the on-state. Furthermore, while biasing in the off-state, the SB at drain-side is thicken and the effective SB height is increased to effectively block holes tunneling and suppresses the leakage current. Figure 2-7(a) and (b) show the schematic energy band diagrams of the n-channel MSB MOSFET in the on-state and off-state, respectively. Figure 2-8(a) and (b) show the transfer characteristics and output characteristics of the n-channel double-gate MSB MOSFET with gate length equals to 5 μm and fin width equals to 80 nm. The properties of the on-state and off-state are clearly enhanced. Higher driving current, better subtheshold swing, lower leakage current, and vanished sub-linear phenomenon are observed. Therefore, the MSB MOSFET can overcome the drawbacks and keep the advantages of SB MOSFET. Similarly, for the p-channel MSB MOSFET, the ultra-thin p^+ SDE not only lowers the effective SB height at source-side to enhance hole tunneling in the on-state but also broads the SB at drain-side to block electron tunneling in the off-state. The schematic energy band diagrams of the p-MSB MOSFET are displayed in Fig. 2-9. Figure 2-10(a) and (b) show the transfer characteristics and output characteristics of the p-channel tri-gate MSB MOSFETs with the gate length equals to 0.5 μm and the fin width equals to 0.3 μm. No sub-linear phenomenon and ambipolar behavior can be observed.

2.3.2 Fundamental Theory

The current transportation of the conventional pn junction MOSFETs has been described by drift-diffusion model successfully. The driving current decreases as temperature increases due to the phonon scattering induced mobility degradation. At the same time, the threshold voltage reduction and the subthreshold swing degradation occur. For the SB junction, the total current is composed of thermionic emission component ($J_{thermionic}$) and tunneling component ($J_{tunneling}$) [15], that is,

$$J = J_{thermionic} + J_{tunneling} \tag{1}$$

$$J_{thermionic} = \frac{A^{*}T}{k}\exp(\frac{-q\phi_b}{kT})\int_0^{\infty} Q(\zeta)\exp(\frac{-\zeta}{kT})d\zeta \tag{2}$$

$$J_{tunneling} = \frac{A^{*}T}{k}\int_0^{q(V_b-\Delta\phi)} F_m Q(\eta)(1-F_s)d\eta \tag{3}$$

, where A* is the Richardson constant, T is the temperature, k is the Boltzman constant, q is the unit charge, ϕ_b is the Schottky barrier height, $\Delta\phi$ is the image force lowering, ζ is the energy measured upward from the potential maximum, and η is the energy measured downward from the potential maximum. F_m and F_s are the Fermi-Dirac distribution functions of the metal and the semiconductor, respectively. $Q(\zeta)$ and $Q(\eta)$ are the transmission coefficients above and below the potential maximum, respectively.

Equations (2) and (3) show that both the thermionic emission component and the tunneling component exhibit positive temperature dependence. Moreover, the thermionic emission component has stronger temperature dependence than the tunneling component. Therefore, the temperature dependence of the SB MOSFET should be in reverse trend of the conventional pn junction MOSFETs, that is, the higher temperature is, the higher current can be obtained. The dominant component

depends on the barrier height and barrier thickness. These barrier properties could be affected by doping concentration and electrical field. Moreover, for MSB junctions, the carrier transportation mechanism is similar to the SB junction since it still can be fundamentally considered as a SB junction with varied SB height and thickness. Hence, the current transportation of MSB MOSFETs would be expected to consist of the drife-diffusion, thermionic emission, and tunneling. Therefore, we can use the temperature dependence of these mechanisms to identify the current transportation mechanism in different bias conditions by measuring the temperature effect of device.

2.3.3 SB MOSFETs

Figure 2-11 shows the typical transfer characteristics of the SB MOSFET with gate length equals to 5 μm and fin width equals to 80 nm, which is biased as an n-channel device. In this case, the electrons from the source-side are dominated in the on-state and the holes from the drain-side are dominated in the off-state. The expected ambipolar phenomenon is clearly observed at each chuck temperature from 300 K to 400 K. These transfer characteristics of the SB MOSFET shown in Fig. 2-11 is redrawn in linear scale at V_{DS}=0.05 V in Fig. 2-12(a). In the both on-state and off-state, the current increases as the temperature increases. It should be noted that the temperature dependence in the off-state is much stronger than that in the on-state. It implies that electron-injection from the source to the inverted channel tends to be dominated by the tunneling mechanism in the on-state while the hole-injection from drain to the p-type body in the off-state tends to be dominated by the thermionic emission mechanism. This inference is consistent with the fact that the barrier for electron is higher than the barrier for hole at the NiSi/Si SB junction [16]. Figure 2-12(b) shows the transfer characteristics of the SB MOSFET shown in Fig. 2-11 in

linear scale at V_{DS}=1 V. The on-state current is still dominated by the tunneling mechanism. However, in the off-state, the positive temperature dependence changes to negative temperature dependence as the V_G decreases to be lower than -2 V. This phenomenon implies that the current transportation mechanism changes from thermionic emission or tunneling to drift-diffusion as increasing the gate bias. In addition, when the drain bias varies from +0.05 V to +1 V, the increasing electric field induces more band bending and the SB at drain-side is getting much thinner. Hence, the holes at drain electrode can more easily tunnel through the SB and inject into the p-type body by the tunneling mechanism and so the smaller positive temperature dependence is observed. Moreover, it is believed that the strong negative gate voltage and positive drain voltage induce more barrier thickness thinning and barrier height lowering. Therefore, while the gate bias increases, the injection resistance of the SB at drain-side decreases. As the hole-injection resistance from drain contact becomes low enough, the current flow becomes controlled by the drift-diffusion mechanism.

Similarly, Fig. 2-13 shows the typical transfer characteristics of the SB MOSFET with gate length equals to 5 μm and fin width equals to 80 nm and the device is biased as a p-channel device. In this case, holes are injected from source to the inverted channel in the on-state while electrons are injected from drain to body in the off-state. Fig. 2-14(a) shows the transfer characteristics of the SB MOSFET shown in Fig. 2-13 in linear scale at V_{DS}=-0.05 V. The on-state current (negative V_G region) increases with the increase of temperature apparently. Similar to the discussion on Fig. 2-12(a), the hole current is dominated by the thermionic emission current while the electron current is dominated by the tunneling current. Fig. 2-14(b) shows the transfer characteristics of the SB MOSFET shown in Fig. 2-13 in linear scale at V_{DS}=-1 V. The on-state current becomes dominated by tunneling current due to the strong drain

field. Additionally, the positive temperature dependence decreases as the negative gate bias increases, indicating that the source-side injection resistance is reduced. This hole-injection resistance would become low enough at further high negative gate bias and thus the reverse temperature dependence is expected to be observed at that condition. In the off-state, the strong positive gate voltage and negative drain voltage reduce the electron-injection resistance at drain contact greatly so that the current becomes dominated by the drift-diffusion mechanism.

2.3.4 n-MSB MOSFETs

Figure 2-15 presents the typical transfer characteristics of the n-channel MSB MOSFET with gate length equals to 5 μm and fin width equals to 80 nm. As indicate in Fig. 2-7, due to the thin thickness and high concentration SDE layer, the modified SB at drain contact is wider and higher than the conventional SB and can block hole-tunneling effectively in the off-state. Moreover, the modified SB at source contact is thinner and lower than the conventional SB and thus can improve the electron-tunneling drastically. Therefore, the properties in the on and off-states are enhanced and the ambipolar phenomenon is suppressed effectively. The transfer characteristics of the n-channel MSB MOSFET shown in Fig. 2-15 in linear scale at V_{DS}=0.05 V is redrawn in Fig. 2-16(a). At low V_G, current increases with the increase of temperature while at high V_G, the temperature dependence is reversed. The intersecting occurs at about V_G=1.2 V. This phenomenon indicates that the current transportation mechanism changes from thermionic emission to tunneling and then to drift-diffusion. It is believed that at low V_G, the SB at source contact is still thick and high enough to dominate current flow. As V_G increases, the barrier thickness and height are reduced. Once the source injection resistance becomes lower than the channel resistance,

current transportation becomes dominated by the drift-diffusion mechanism and thus the negative temperature dependence is observed. In addition, the gate bias dependent source injection resistance on the MSB MOSFET would be discussed in the next chapter. A novel modified external method is proposed to extract the bias dependent series resistance. Furthermore, Fig. 2-16(b) shows the transfer characteristics of the n-channel MSB MOSFET shown in Fig. 2-15 in linear scale with V_{DS}=1 V. Similar to that observed in Fig. 2-16(a), positive temperature dependence is obtained at low V_G but it reverses at high gate bias and the current transportation mechanism changes to drift-diffusion mechanism. Comparing with the SB MOSFET, the stronger negative temperature dependence of the on-state current confirms the effect of the MSB junction, indicating the ITS method and the low-temperature post-ITS annealing at 600 °C for 30 min can form the thin and highly doped SDE regions successfully. To evaluate the process effect, Fig. 2-17 shows the linear scale transfer characteristics of the n-channel MSB MOSFET fabricated with a post-ITS annealing at 600 ºC for 30 sec or 30 min and at V_{DS}=0.05 V. The changing point from tunneling mechanism to drift-diffusion mechanism moves from 1.2 V to 1.8 V as the post-ITS annealing time decrease from 30 min to 30 sec. This result indicates that the insufficient post-ITS thermal budget (600 ºC, 30 sec) results in higher source injection resistance so that the current transportation is more likely to be controlled by the tunneling mechanism. Figure 2-18 compares the transfer characteristics of the n-channel MSB MOSFETs fabricated with two different post-ITS thermal budget. It is observed that the MOSFET with higher thermal budget exhibits higher driving capability, better subthreshold swing, and lower off-state current.

2.3.5 p-MSB MOSFETs

For the p-MSB MOSFETs, the observation is similar to that of the n-MSB MOSFETs, i.e., the highly doped p^+ SDE regions are successfully formed in the interface of the Ni-silicide/Si-channel to improve the on/off states properties. Figure 2-19 shows the typical transfer characteristics of the p-channel MSB MOSFET with gate length equals to 0.5 μm and fin width equals to 0.3μm. The ambipolar phenomenon is suppressed effectively owing to the MSB junctions. The transfer characteristics of the p-channel MSB MOSFET shown in Fig. 2-19 in linear scale at V_{DS} =-0.05 V and -1 V are redrawn in Fig. 2-20(a) and (b), respectively. The trend of the temperature dependence is quiet alike to that of the n-channel MSB MOSFET, as shown in Fig. 2-16. Hence, the same tendency of temperature dependence and dominated current transportation mechanism are obtained. At low negative V_G, due to the thick source-side SB, current is controlled by thermionic emission. Then, as the negative V_G increases, the SB is thinner and lower and then the current transportation mechanism changes from tunneling and then to drift-diffusion. The intersection occurs at about V_G=-1.6 V. Comparing with the SB MOSFET, the stronger negative temperature dependence of the on-state current confirms the effect of the MSB junction.

2.4 Conclusions

Ultra-thin and highly doped SDE regions are successfully formed in the NiSi SB source/drain SOI MOSFETs by implantation-to-silicide (ITS) method and low temperature post-ITS annealing processes. Owing to the engineering of energy band near at the Ni-silicide/Si-channel interface, the modified Schottky barrier (MSB) source/drain can effectively improve both the on-state and the off-state current-

voltage properties. Moreover, current transportation mechanisms of n/p-channel Schottky barrier (SB) and n/p-channel Modified Schottky barrier (MSB) MOSFETs are identified by measuring the temperature effect on current-voltage characteristics. For the SB MOSFETs, current transportation could be dominated by thermionic emission or tunneling mechanism depends on the Schottky barrier height and the applied electric field, i.e. the gate and drain voltages. Drift-diffusion current could occur at sufficient high electric field. The current transportation of the n/p-channel MSB MOSFETs changes from tunneling mechanism to drift-diffusion mechanism as the gate voltage increases since the SDE region can effectively reduce the effective SB height and reduced the source-side injection resistance. Once the source-side injection resistance is smaller than the channel resistance, the current transportation mechanism would be dominated by the drift-diffusion model. Furthermore, the changing point is a good indicator to evaluate the efficiency of the MSB junction. Sufficient post-ITS thermal budget is required to obtain high performance MSB MOSFET. Since the current transport mechanism depends on bias condition, the extraction of mobility should be treated carefully, especially at low gate voltage. In addition, the bias condition would affect the SB properties and modify the series resistance of MSB MOSFETs. In next chapter, a novel modified external method will be proposed to extract the bias dependent series resistance.

References

[1] J. Kedziersk, P. Xuan, E. H. Andersonf, J. Bokor, T.-J. King, C. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime," in *IEDM Tech. Dig.*, 2000, pp.57-60.

[2] S. Zhu, H. Y. Yu, S. J. Whang, J. H. Chen, C. Shen, C. Zhu, S. J. Lee, M. F. Li, D. S. H. Chan, W. J. Yoo, A. Du, C. H. Tung, J. Singh, A. Chin, and D. L. Kwong, "Schottky-Barrier S/D MOSFETs With High-K Gate Dielectrics and Metal-Gate Electrode," *IEEE Electron Device Lett.,* vol. 25, no. 5, pp. 268-270, 2004.

[3] M. Jang, Y.Kim, J. Shin, S. Lee, and K. Park, " A 50-nm-gate-length erbium-silicided n-type Schottky barrier metal-oxide-semiconductor field-effect transistor," *App. Phys. Lett.,* vol. 84, no. 5, pp. 741-743, 2004.

[4] R. T. P. Lee, A. E.-J. Lim, K.-M. Tan, T.-Y. Liow, G.-Q. Lo, G. S. Samudra, D. Z. Chi, and Y.-C. Yeo, "N-channel FinFETs With 25-nm Gate Length and Schottky-Barrier Source and Drain Featuring Ytterbium Silicide." *IEEE Electron Device Lett.,* vol. 28, no. 2, pp. 164-167, 2004.

[5] J. Knoch, M. Zhang, Q. T. Zhao, St. Lenk, S. Mantl, and J. Appenzeller, "Effective Schottky barrier lowering in silicon-on-insulator Schottky-barrier metal-oxide-semiconductor field-effect transistors using dopant segregation," *App. Phys. Lett.,* vol. 87, no. 26, p. 263505, 2005.

[6] J. Knoch and J. Appenzeller, "Impact of the channel thickness on the performance of Schottky barrier metal–oxide–semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 81, no. 16, pp. 3082-3084, 2002.

[7] H. C. Lin, M. F. Wang, F. J. Ho, J. T. Liu, Y. Li, T. Y. Huang, and S. M. Sze,

"Effects of sub-gate bias on the operation of Schottky-barrier SOI MOSFETs having nano-scale channel," in *IEEE Conf. Nanotechnology (NANO)*, 2002, pp. 205–208.

[8] S. Xiong, T.-J. King, and J. Bokor, "A Comparison Study of Symmetric Ultrathin-Body Double-Gate Devices With Metal Source/Drain and Doped Source/Drain," *IEEE Trans. Electron Devices,* vol. 52, no. 8, pp. 1859-1867, 2005.

[9] Bing-Yue Tsui and Chia-Pin Lin, "A novel 25 nm modified-Schottky-barrier FinFET with high performance," *IEEE Electron Device Lett.,* vol. 25, no.6, pp. 430-432, 2004.

[10] A. Kinoshita, Y. Tsuchiya, A. Yagishita, K. Uchida and J. Koga, "Solution for High-Performance Schottky-Source/Drain MOSFETs: Schottky Barrier Height Engineering with Dopant Segregation Technique," in *VLSI Symp. Tech. Dig.*, 2004, pp. 168-169.

[11] M. Zhang, J. Knoch, Q.T. Zhao, A. Fox, St. Lenk, and S. Mantl, "Low temperature measurements of Schottky-barrier SOI-MOSFETs with dopant segregation," *Electronics Letters,* vol. 41, no. 19, pp. 1085-1086, 2005.

[12] S. P. Murarka, Silicides for VLSI application, New work: Academic, 1983, p. 130.

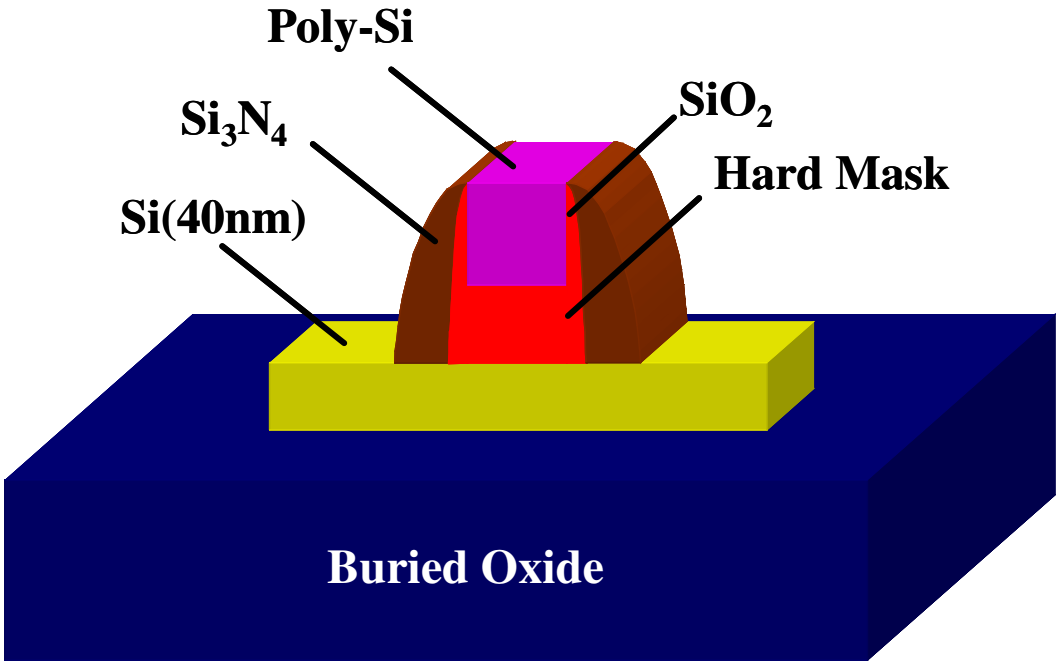
[13] J. P. Lu, D. Miles, J. Zhao, A. Gurba, Y. Xu, C. Lin, M. Hewson, J. Ruan, L. Tsung, R. Kuan, T. Grider, D. Mercer, C. Montgomery, "A novel nickel salicide process technology for CMOS devices with sub-40 nm physical gate length," in *IEDM Tech. Dig.*, 2002, pp. 371-374.

[14] A. Kinoshita, T. Kinoshita, Y. Nishi, K. Uchida, S. Toriyama, R. Hasumi, and J. Koga, "Comprehensive Study on Injection Velocity Enhancement in Dopant-

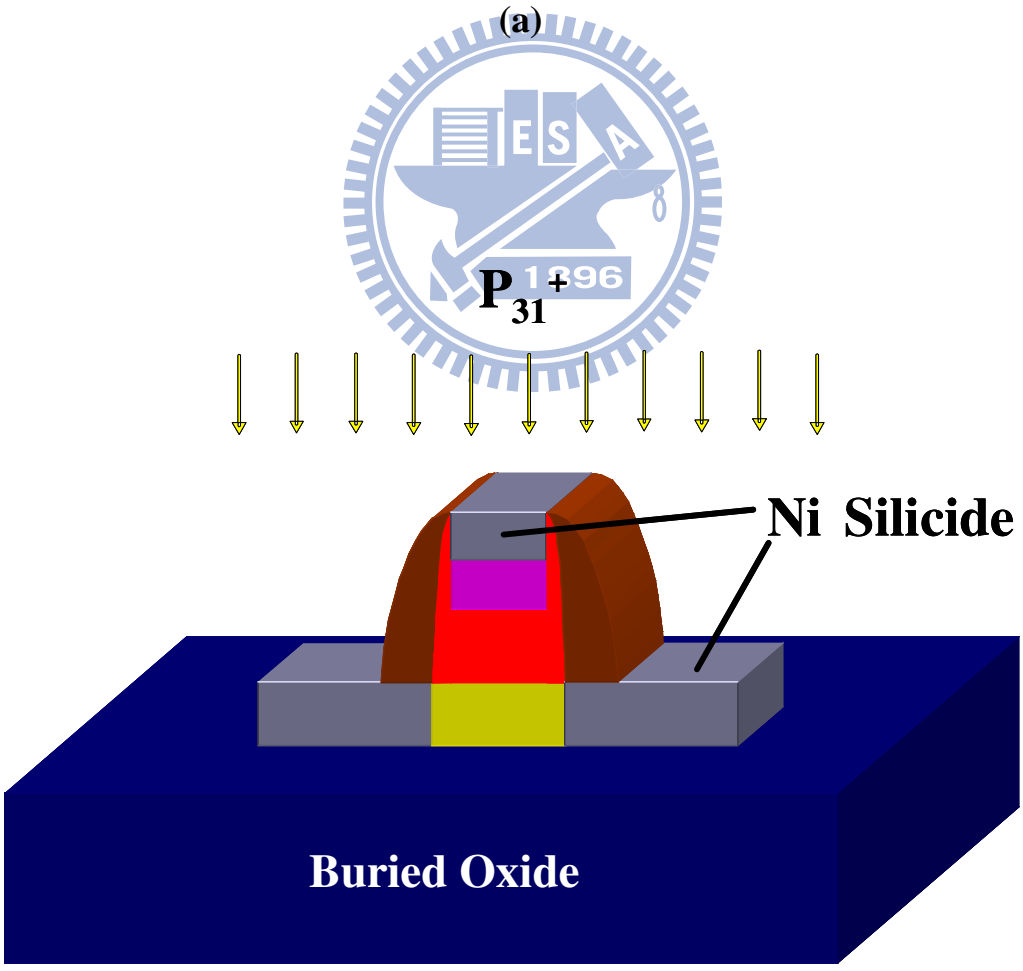
Segregated Schottky MOSFETs," in *IEDM Tech. Dig.*, 2006,, pp. 79-82.

[15] S. M. Sze, Physics of Semiconductor Devices, 2 ed., John Wiley & Sons, 1981, pp. 263-264.

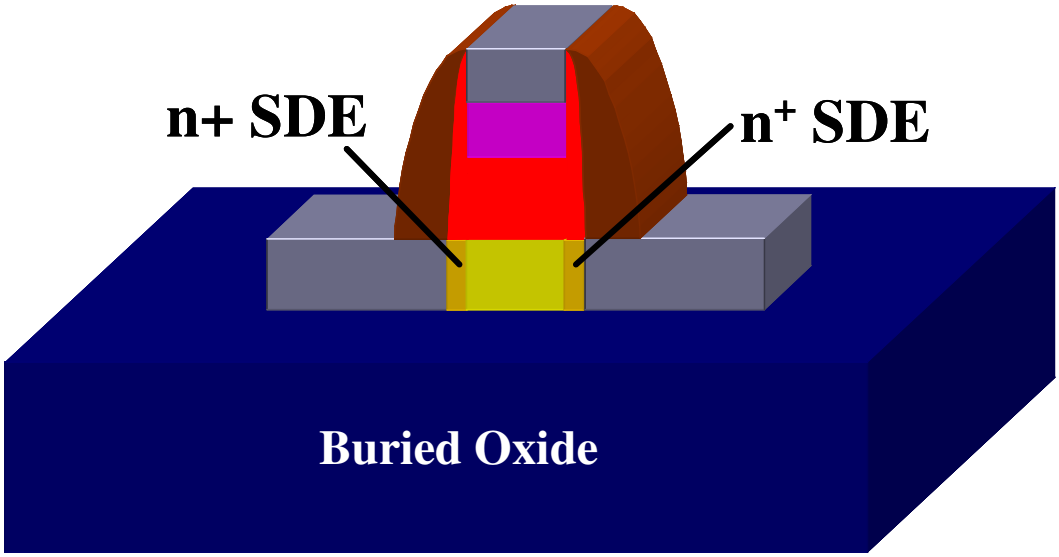
[16] S. M. Sze, Physics of Semiconductor Devices, 2 ed., John Wiley & Sons, 1981, p. 292.


Poly-Si
Si_3N_4
SiO_2
Hard Mask
Si(40nm)
Buried Oxide

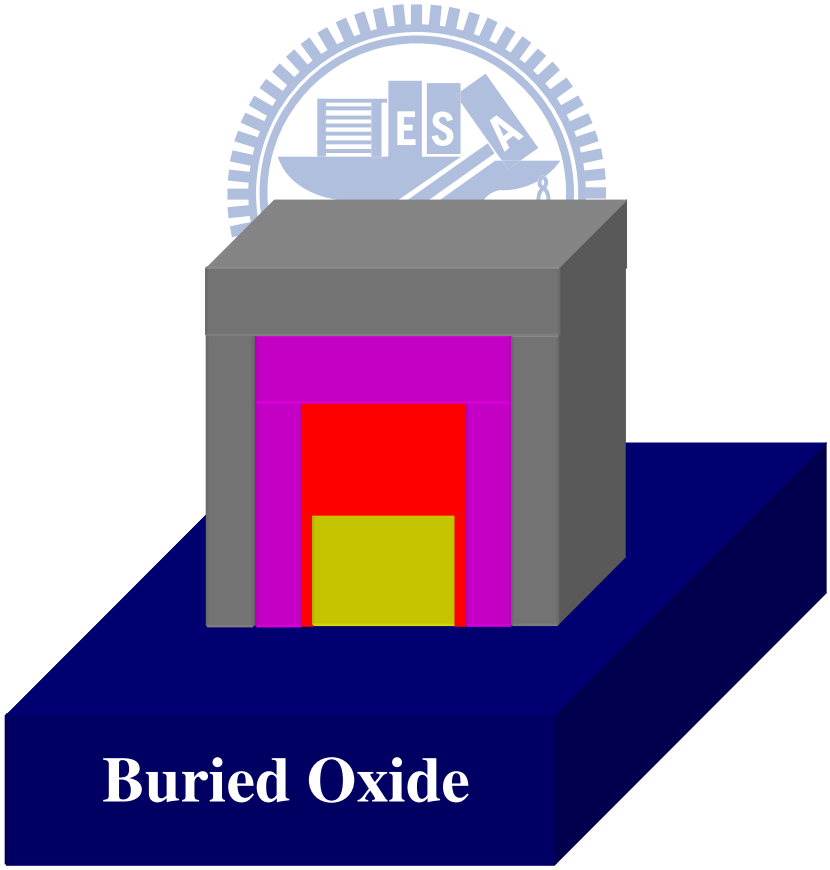
(a)


P_{31}^{+}
Ni Silicide
Buried Oxide

(b)

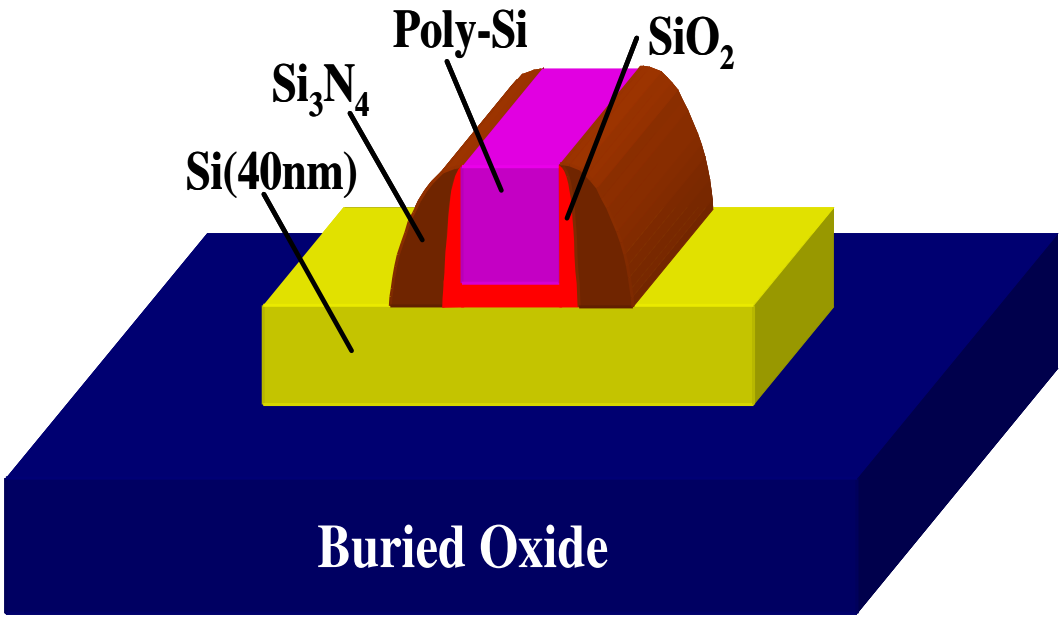


(c)

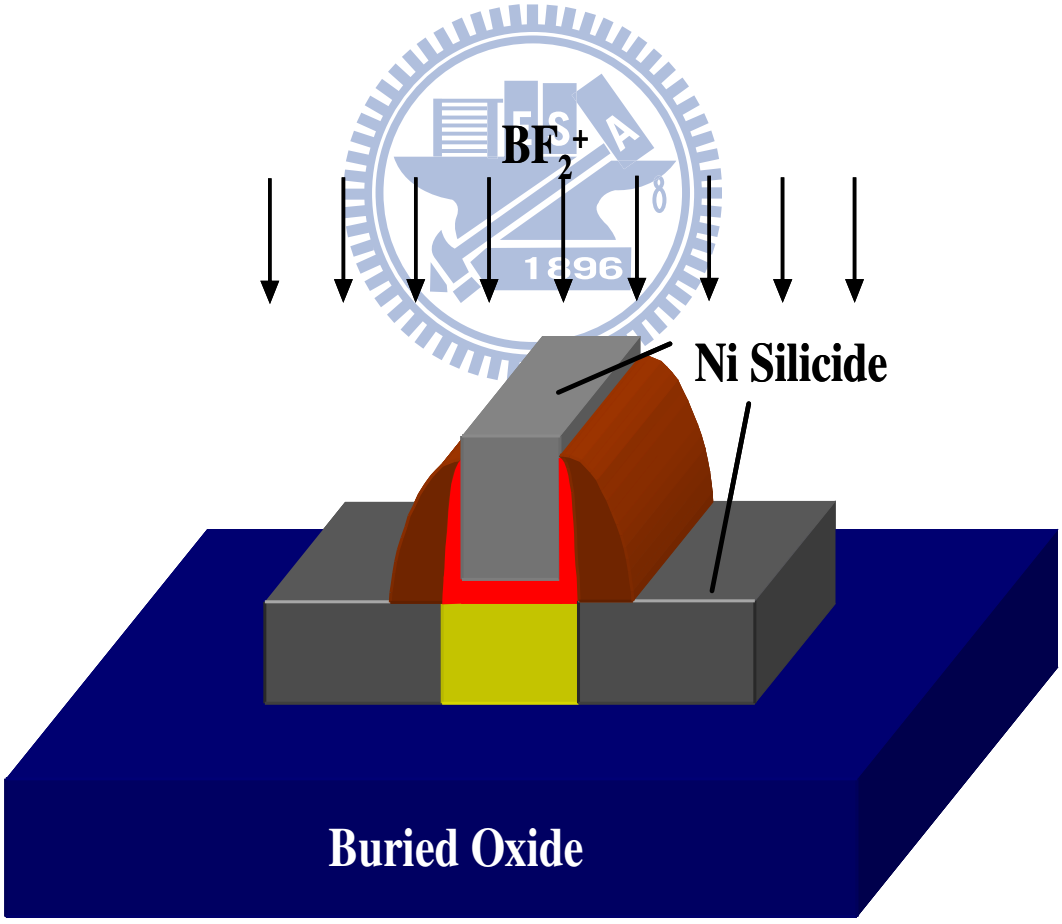


(d)

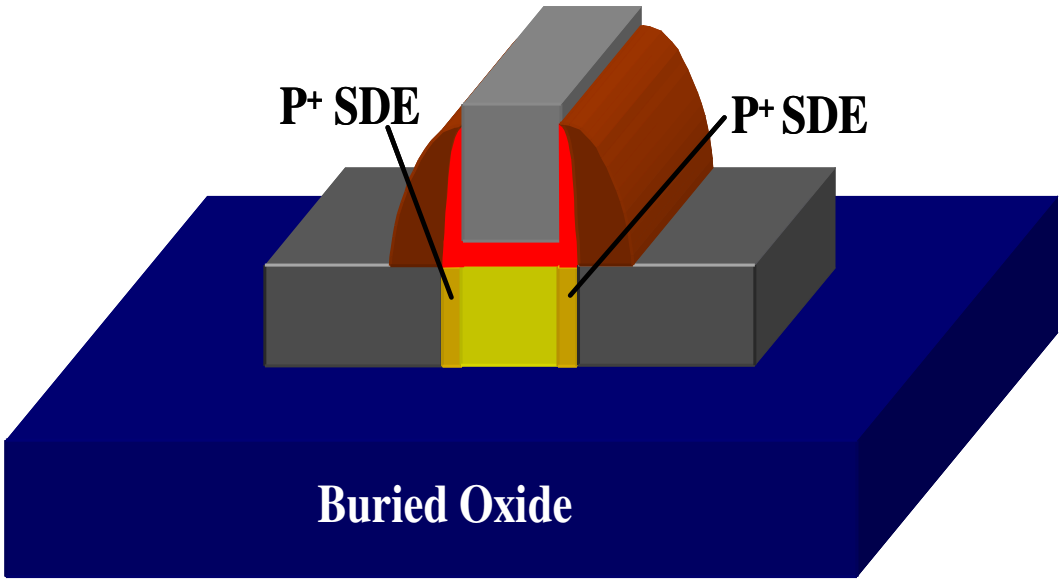
Fig. 2-1 Process flow of the double-gate n-channel MSB MOSFETs.


Poly-Si
SiO_2
Si_3N_4
Si(40nm)
Buried Oxide

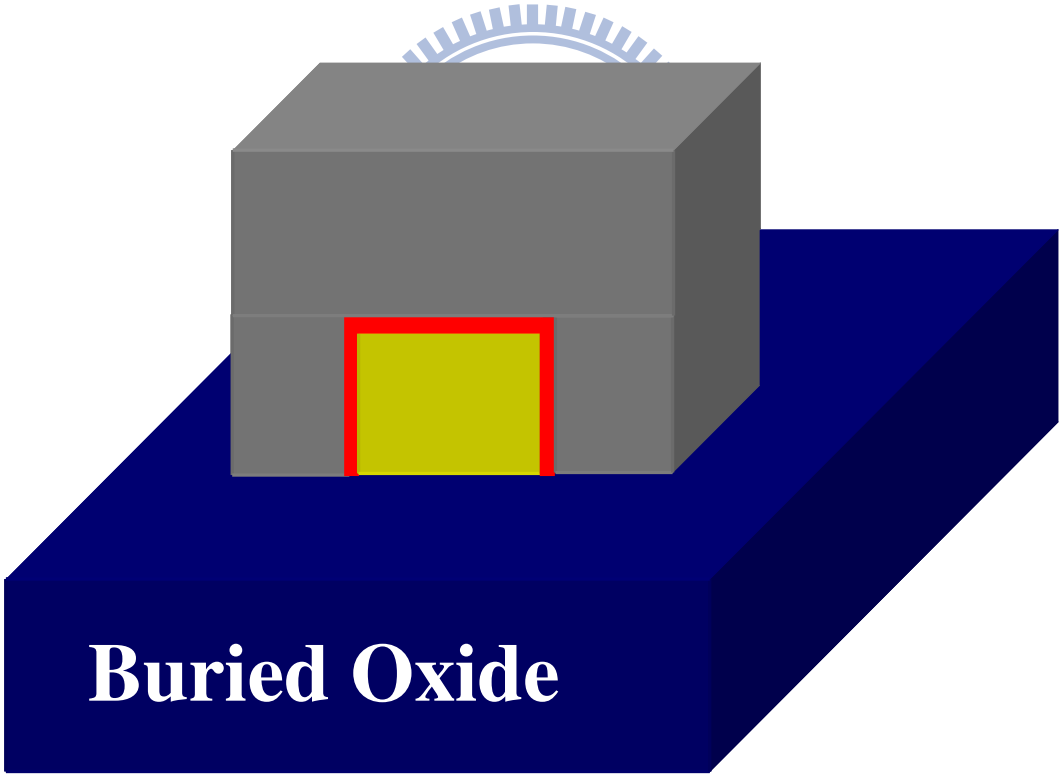
(a)


BF_2^+
Ni Silicide
Buried Oxide

(b)



(c)



(d)

Fig. 2-2 Process flow of the tri-gate p-channel MSB MOSFETs.

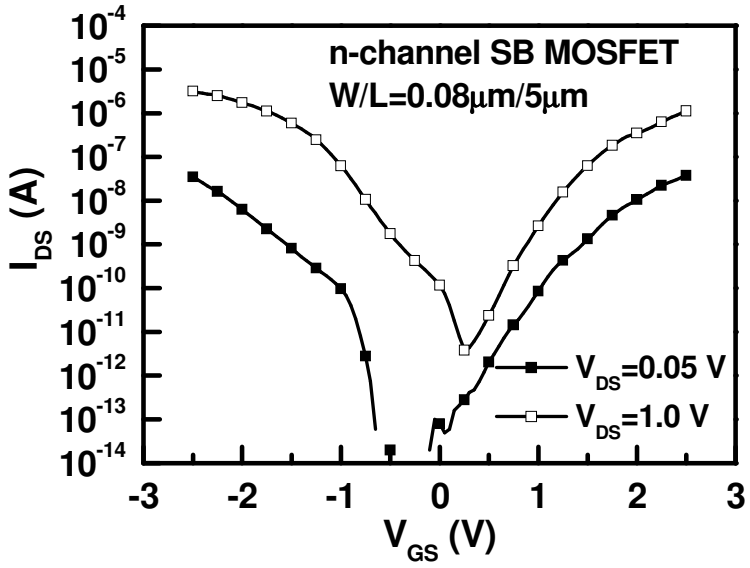


Fig. 2-3(a) Transfer characteristics of n-channel double-gate SB MOSFET with L_G=5 μm, and W_{Fin}=0.08 μm.

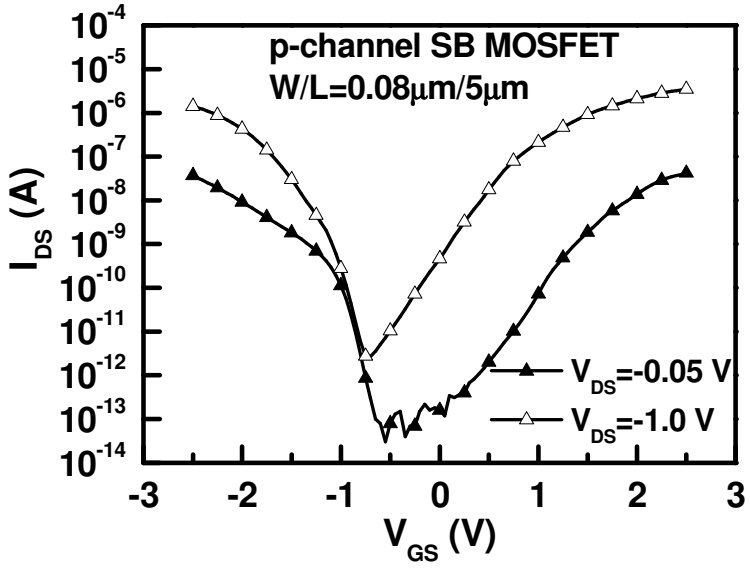


Fig. 2-3(b) Transfer characteristics of p-channel double-gate SB MOSFET with L_G=5 μm, and W_{Fin}=0.08 μm.

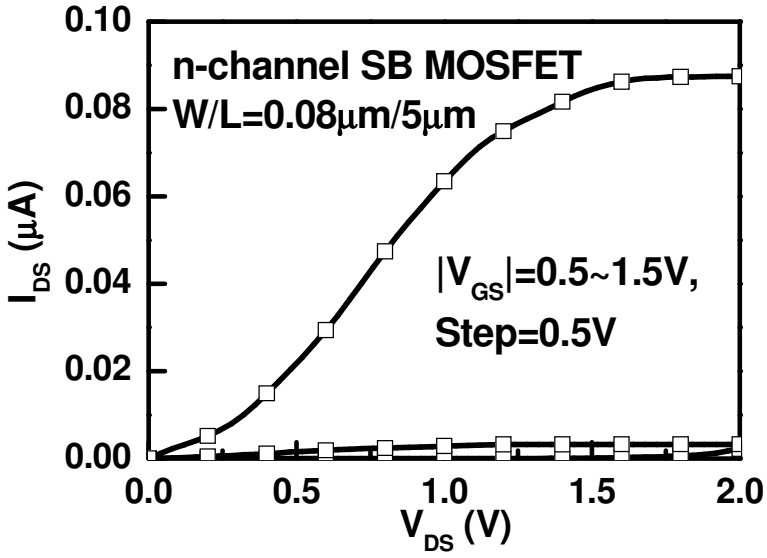


Fig. 2-4(a) Output characteristics of n-channel double-gate SB MOSFET with L_G=5 μm, and W_{Fin}=0.08 μm.

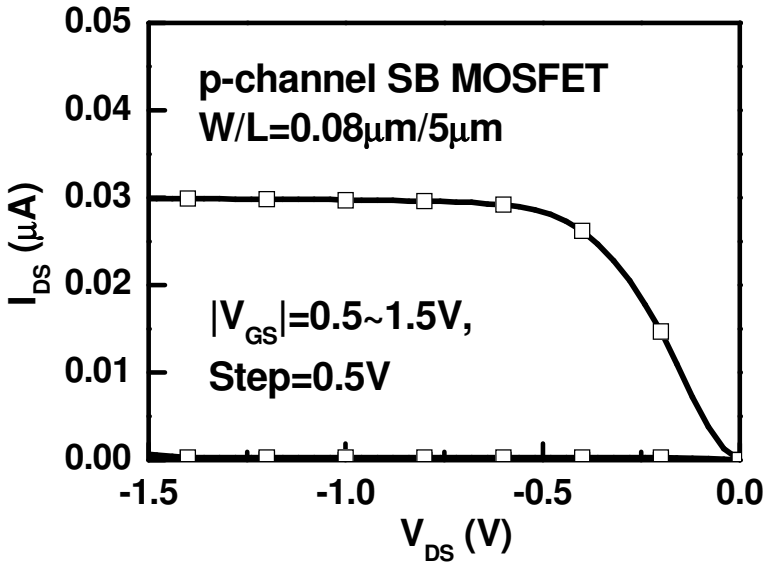


Fig. 2-4(b) Output characteristics of p-channel double-gate SB MOSFET with L_G=5 μm and W_{Fin}=0.08 μm.

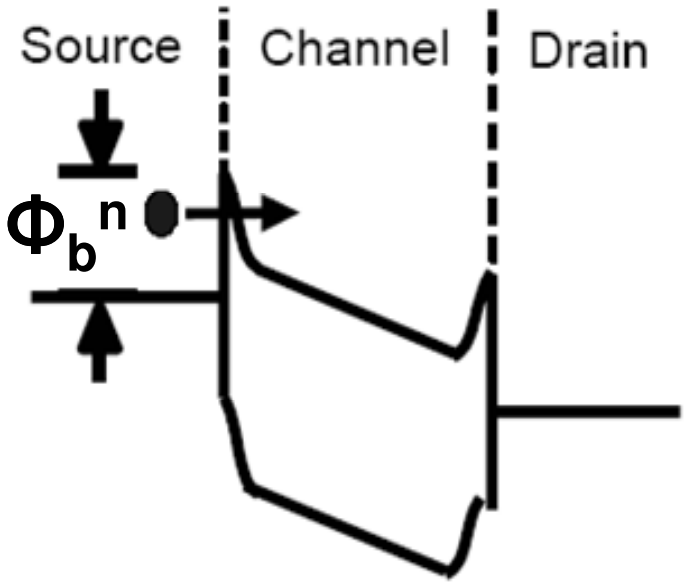


Fig. 2-5(a) Schematic energy band diagram of the n-channel SB MOSFETs operates at the on-state.

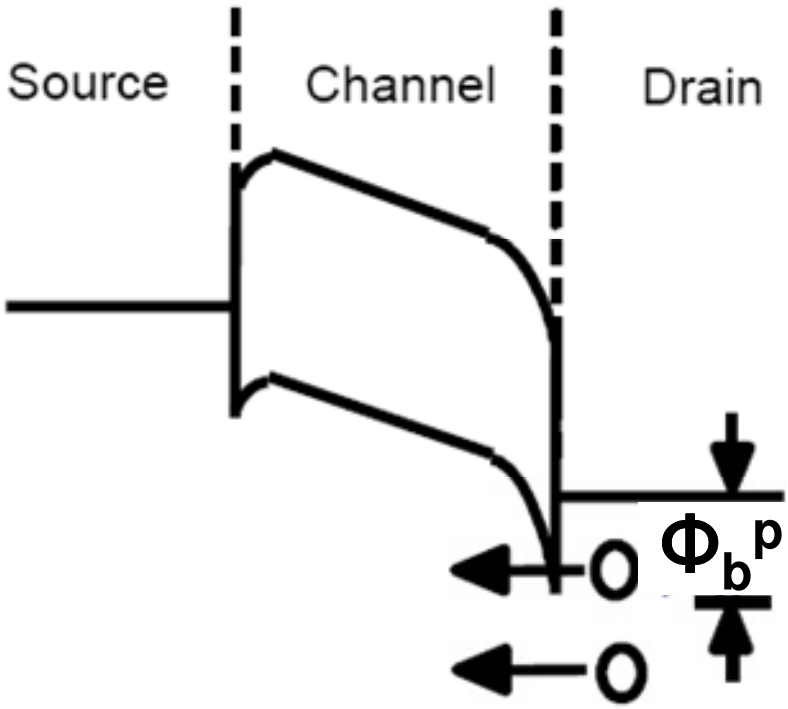


Fig. 2-5(b) Schematic energy band diagram of the n-channel SB MOSFETs operates at the off-state.

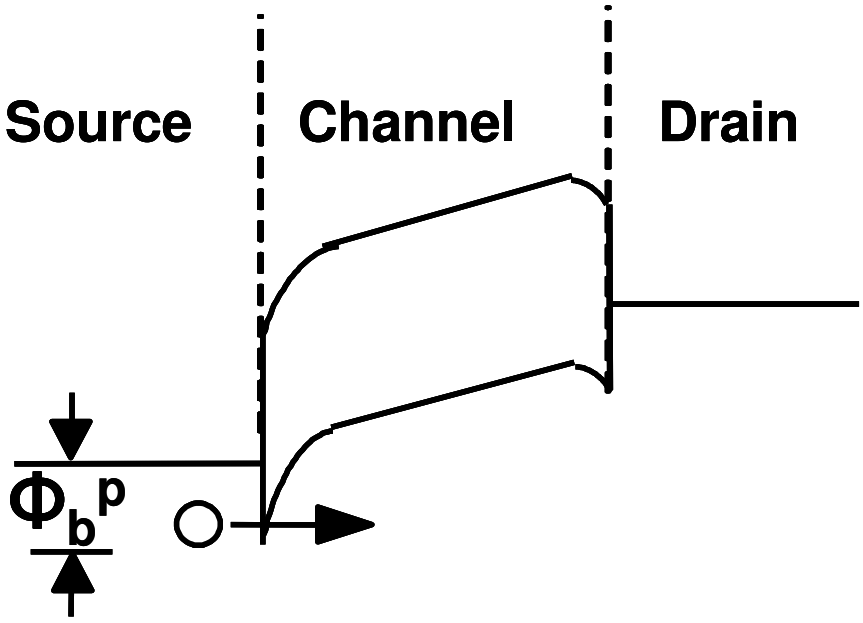


Fig. 2-6(a) Schematic energy band diagram of the p-channel SB MOSFETs operates at the on-state.

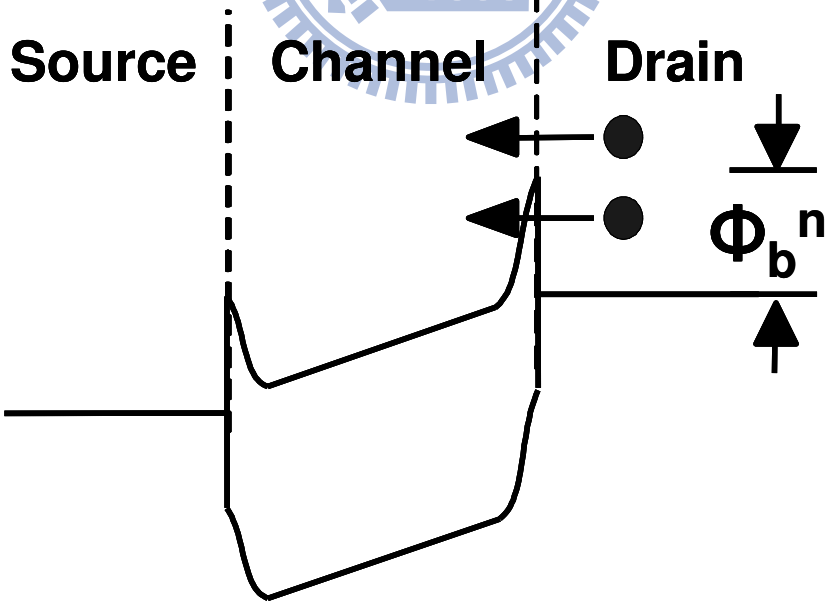


Fig. 2-6(b) Schematic energy band diagram of the p-channel SB MOSFETs operates at the off-state.

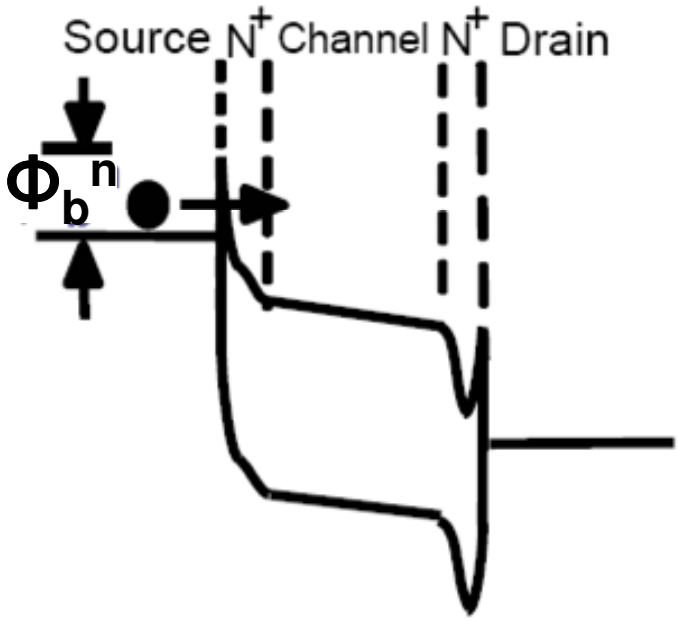


Fig. 2-7(a) Schematic energy band diagrams of the n-MSB MOSFET at on-state.

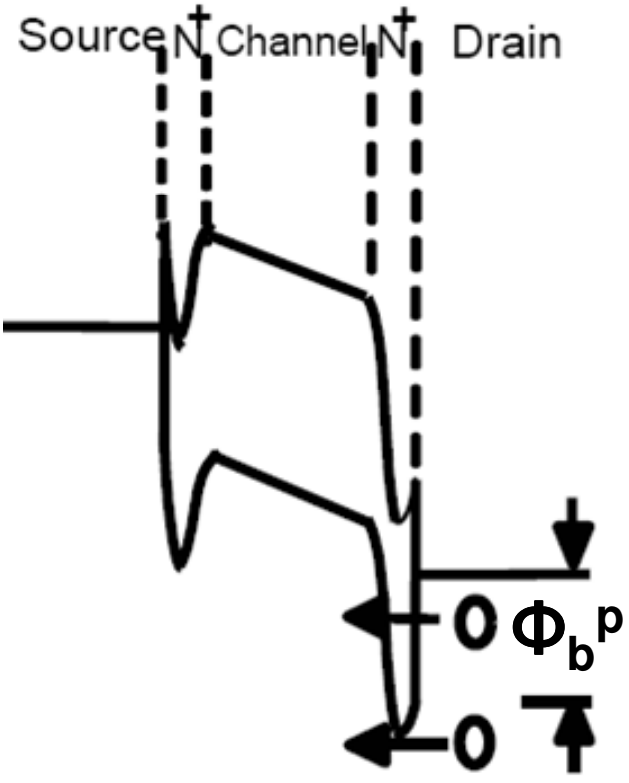


Fig. 2-7(b) Schematic energy band diagrams of the n-MSB MOSFET at off-state.

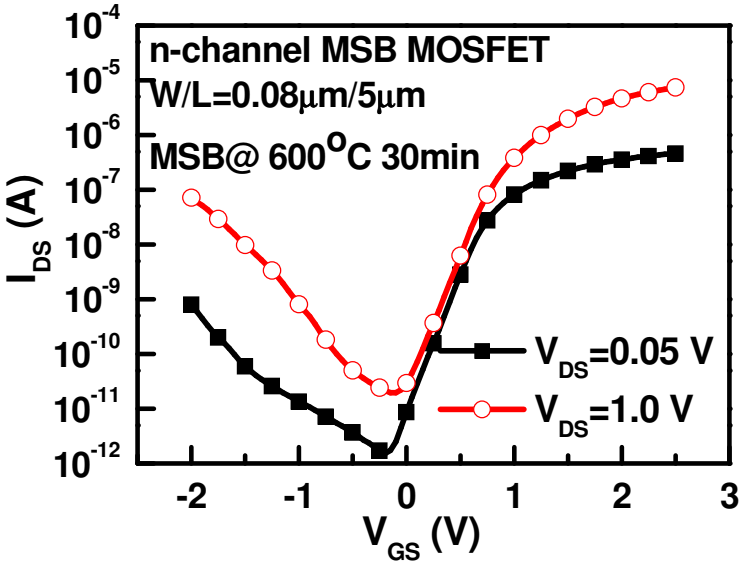


Fig. 2-8(a) Transfer characteristics of the n-channel double-gate MSB MOSFET with L_G=5 μm, and W_{Fin}=0.08 μm.

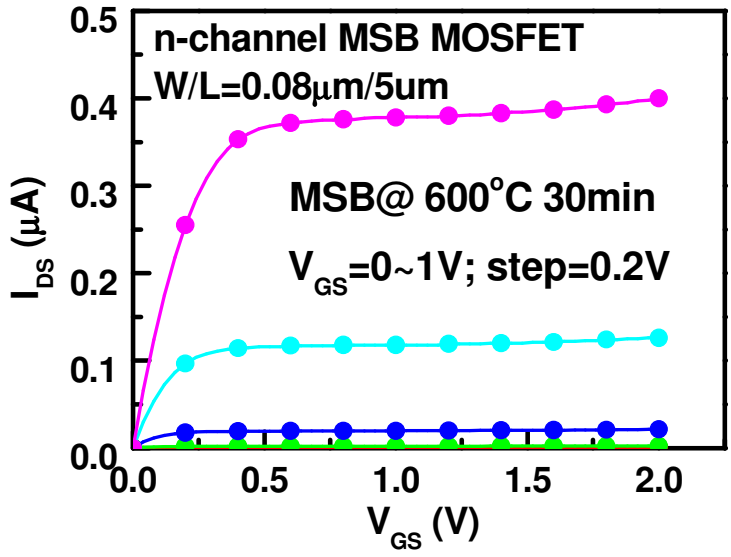


Fig. 2-8(b) Output characteristics of the n-channel double-gate MSB MOSFET with L_G=5 μm, and W_{Fin}=0.08 μm.

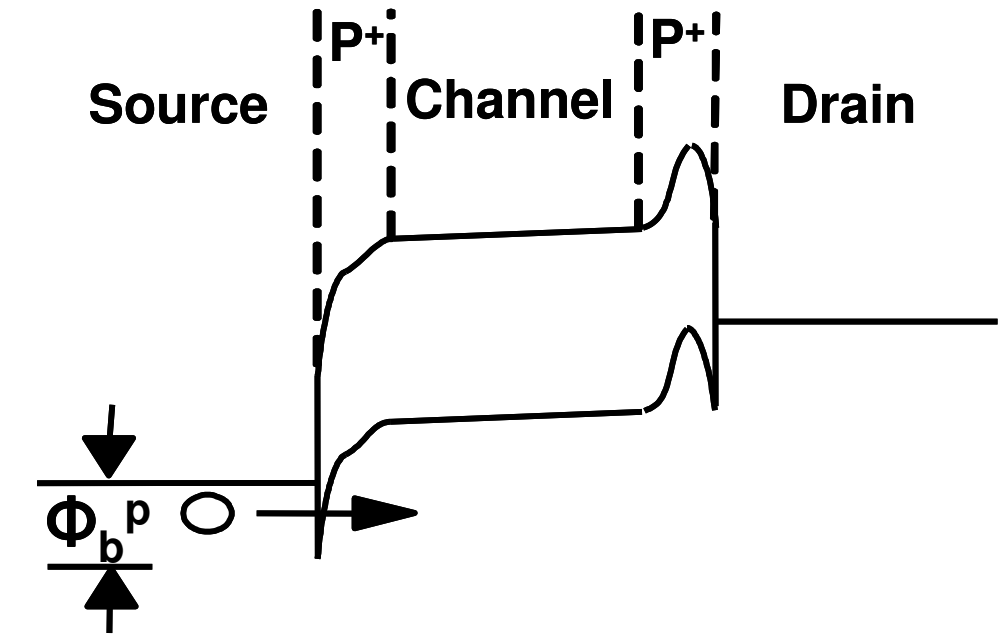


Fig. 2-9(a) Schematic energy band diagrams of the p-MSB MOSFET at on-state.

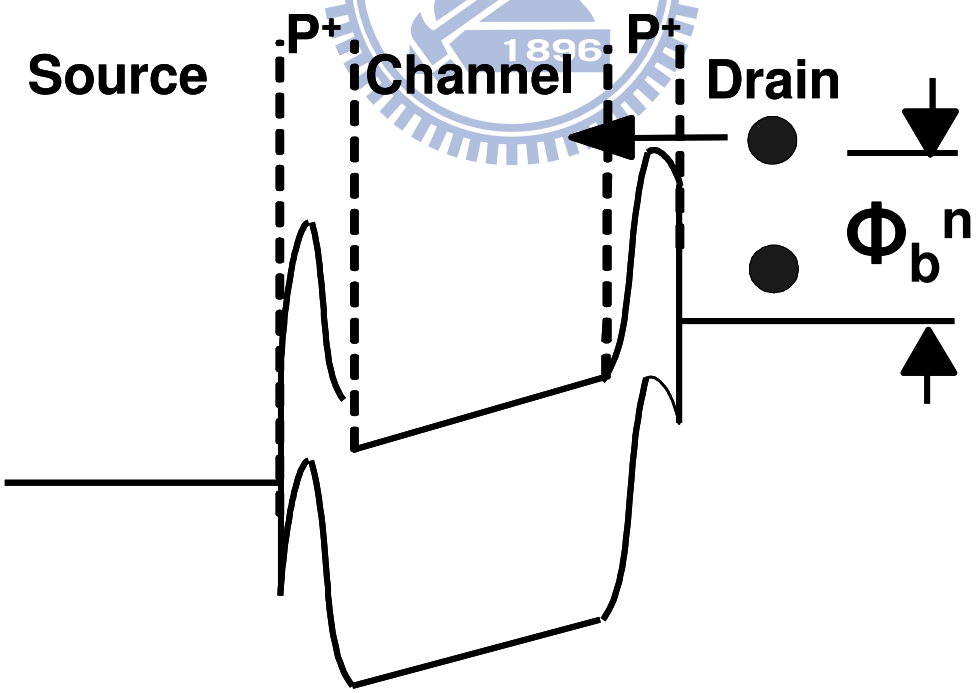


Fig. 2-9(b) Schematic energy band diagrams of the p-MSB MOSFET at off-state.

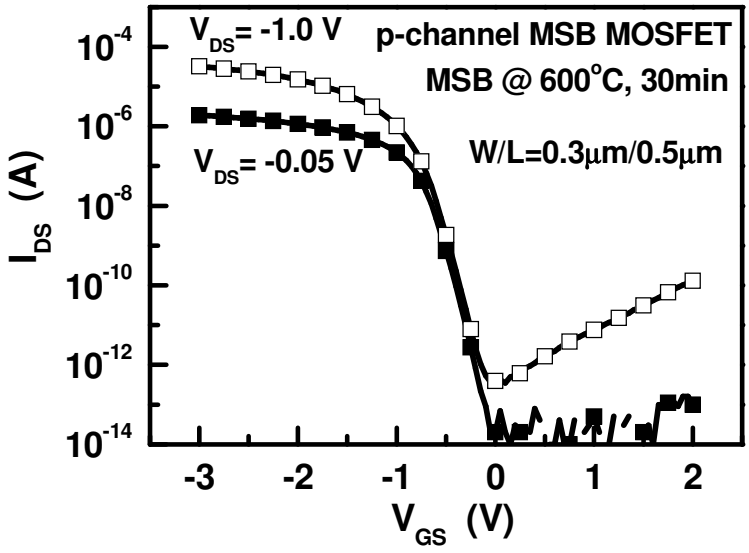


Fig. 2-10(a) Transfer characteristics of the p-channel tri-gate MSB MOSFET with gate length equals to 0.5 μm and fin width equals to 0.3 μm.

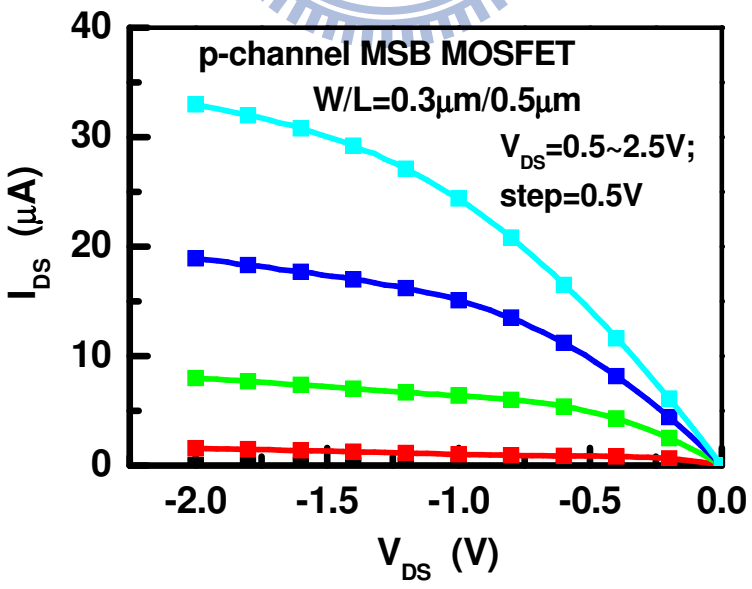


Fig. 2-10(b) Output characteristics of the p-channel tri-gate MSB MOSFET with gate length equals to 0.5 μm and fin width equals to 0.3 μm.

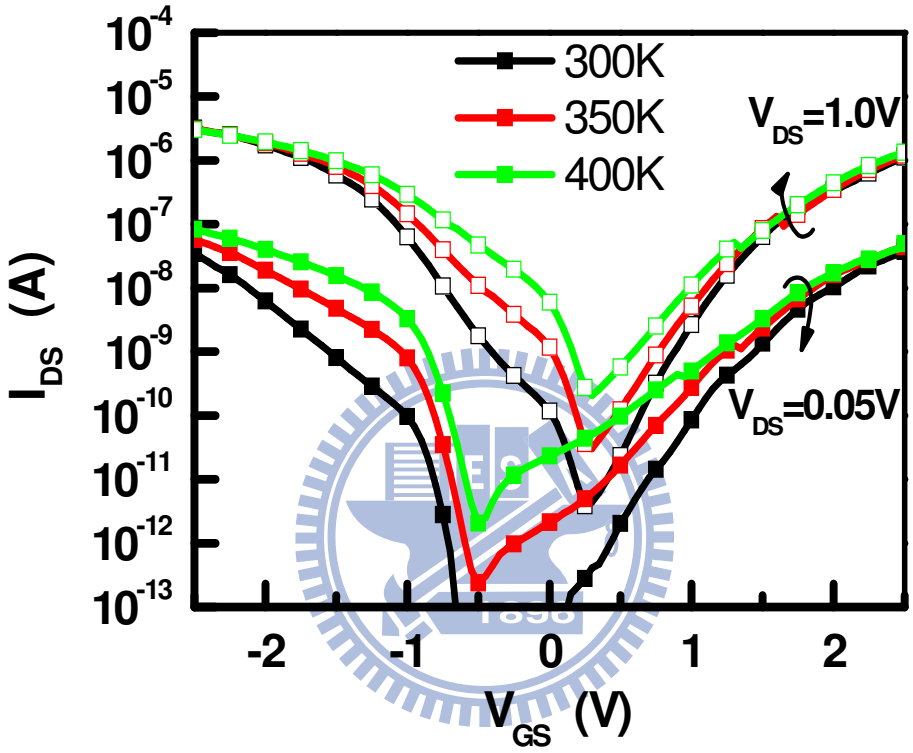


Fig. 2-11 Transfer characteristics of the n-channel SB MOSFET with gate length equals to 5 μm and fin width equals to 80 nm.

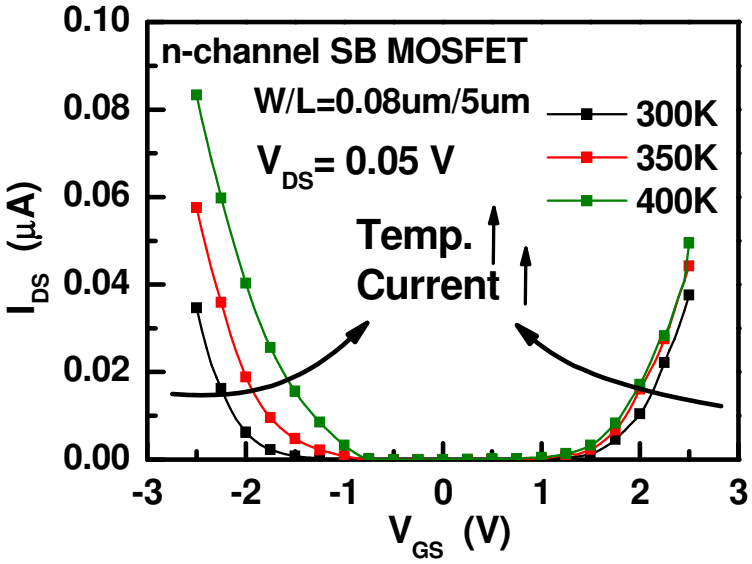


Fig. 2-12(a) Transfer characteristics of the n-channel SB MOSFET shown in Fig. 11 in linear scale with V_{DS}=0.05 V.

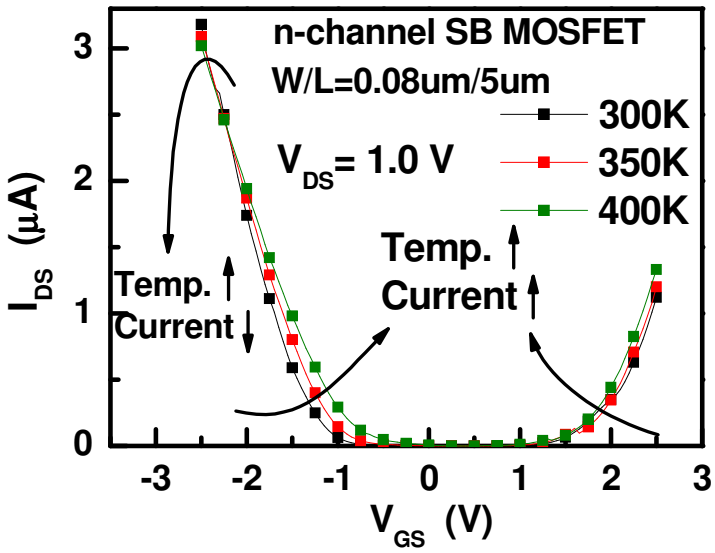


Fig. 2-12(b) Transfer characteristics of the n-channel SB MOSFET shown in Fig. 11 in linear scale with V_{DS}=1.0 V.

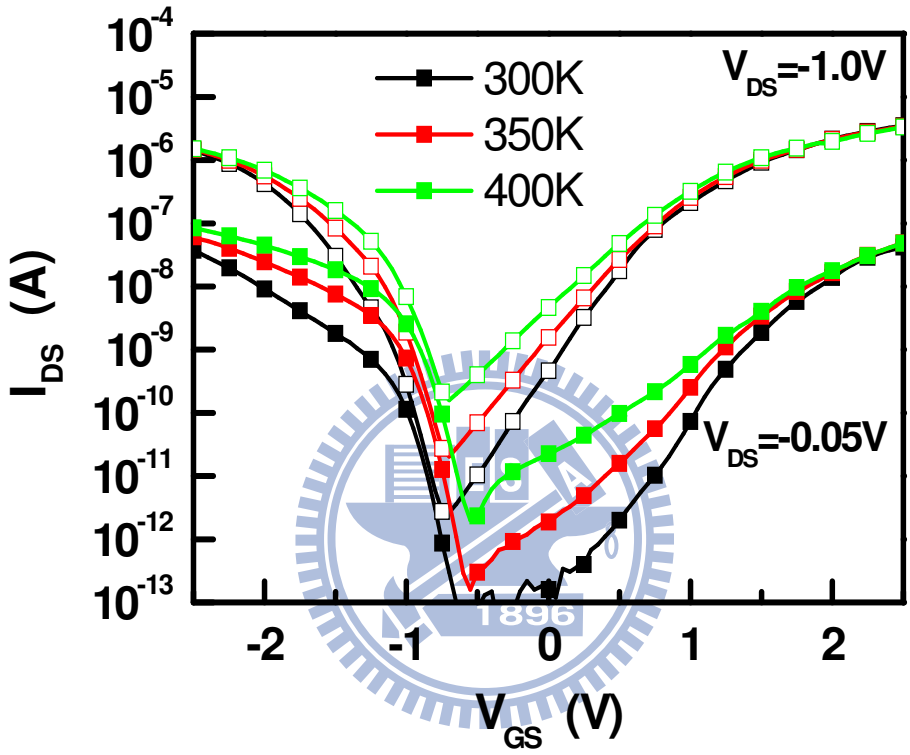


Fig. 2-13 Transfer characteristics of the p-channel SB MOSFET with gate length equals to 5 μm and fin width equals to 80 nm.

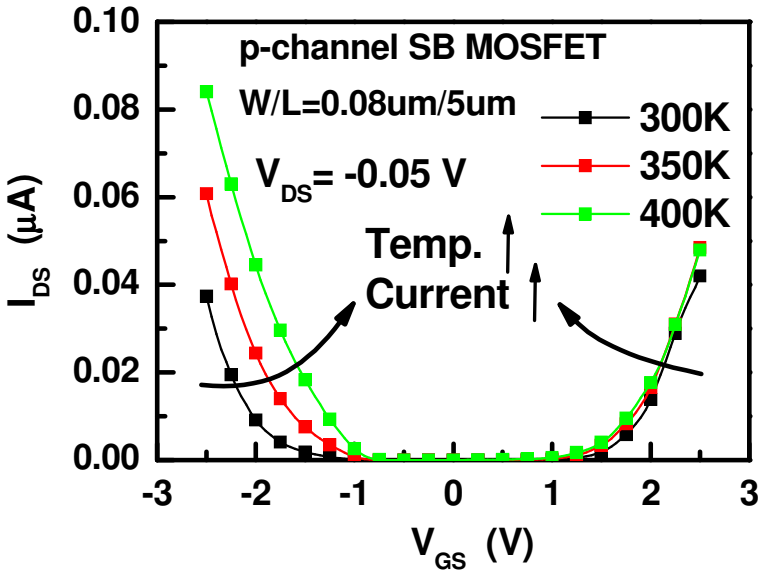


Fig. 2-14(a) Transfer characteristics of the p-channel SB MOSFET shown in Fig. 13 in linear scale with V_{DS}= -0.05 V.

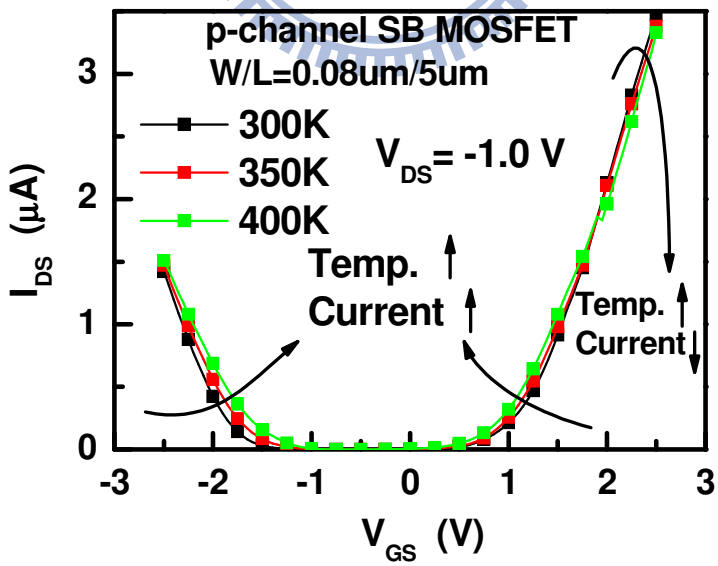


Fig. 2-14(b) Transfer characteristics of the p-channel SB MOSFET shown in Fig. 13 in linear scale with V_{DS}= -1.0 V.

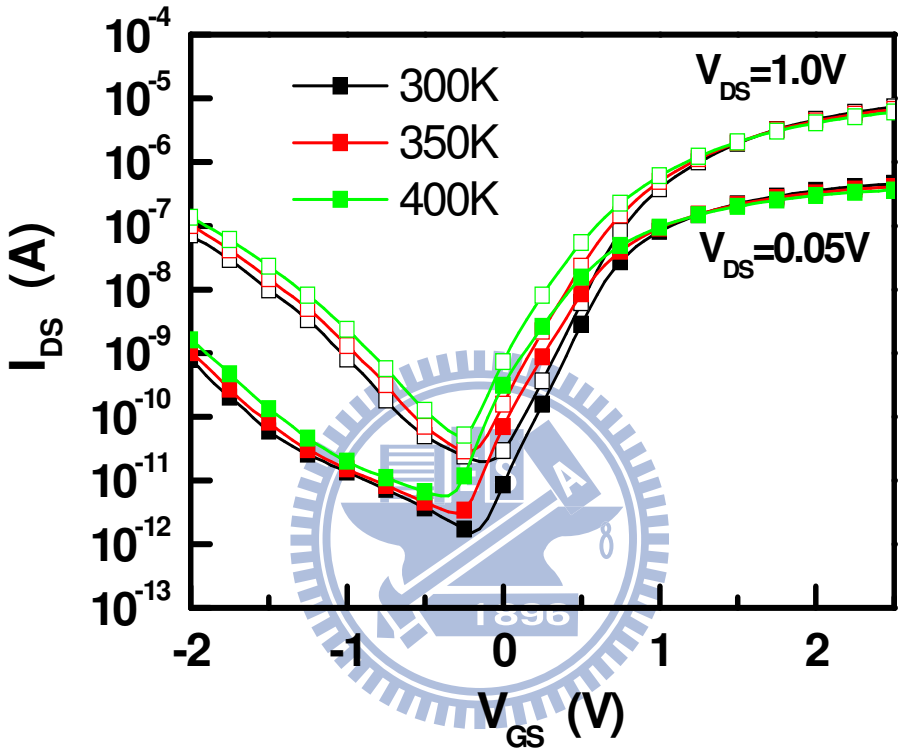


Fig. 2-15 Transfer characteristics of the n-channel MSB MOSFET with gate length equals to 5 μm and fin width equals to 80 nm.

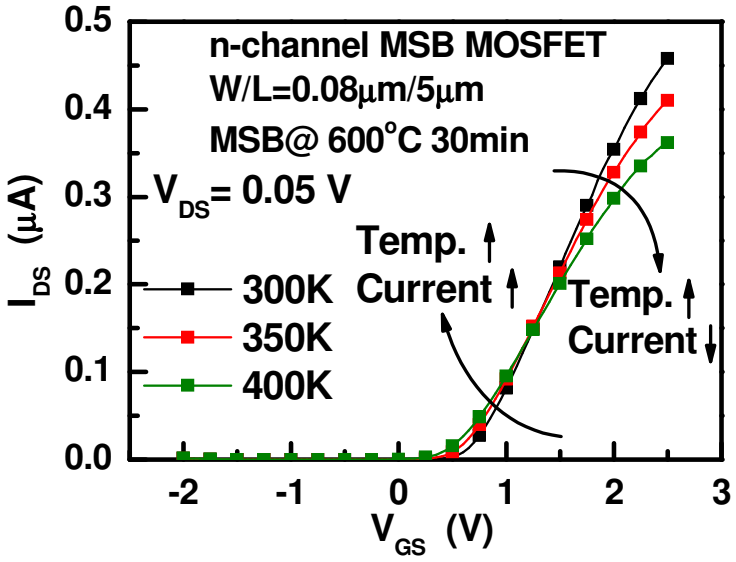


Fig. 2-16(a) Transfer characteristics of the n-channel MSB MOSFET shown in Fig. 15 in linear scale with V_{DS}= 0.05 V.

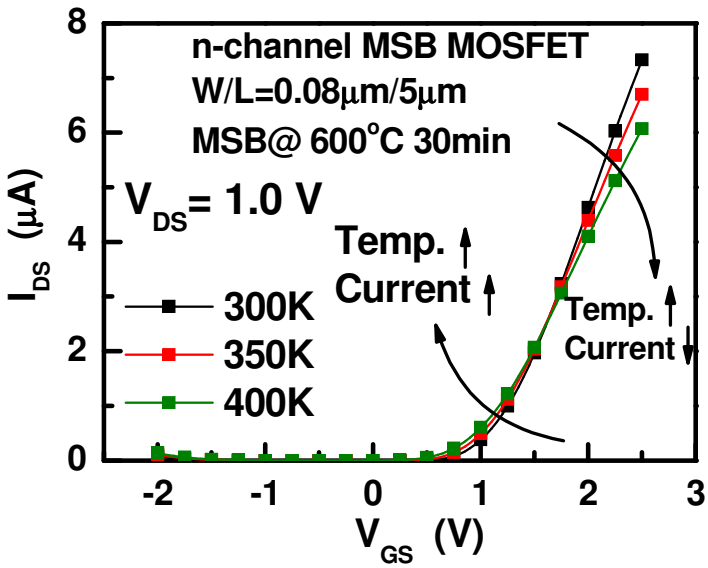


Fig. 2-16(b) Transfer characteristics of the n-channel MSB MOSFET shown in Fig. 15 in linear scale with V_{DS}= 1.0 V.

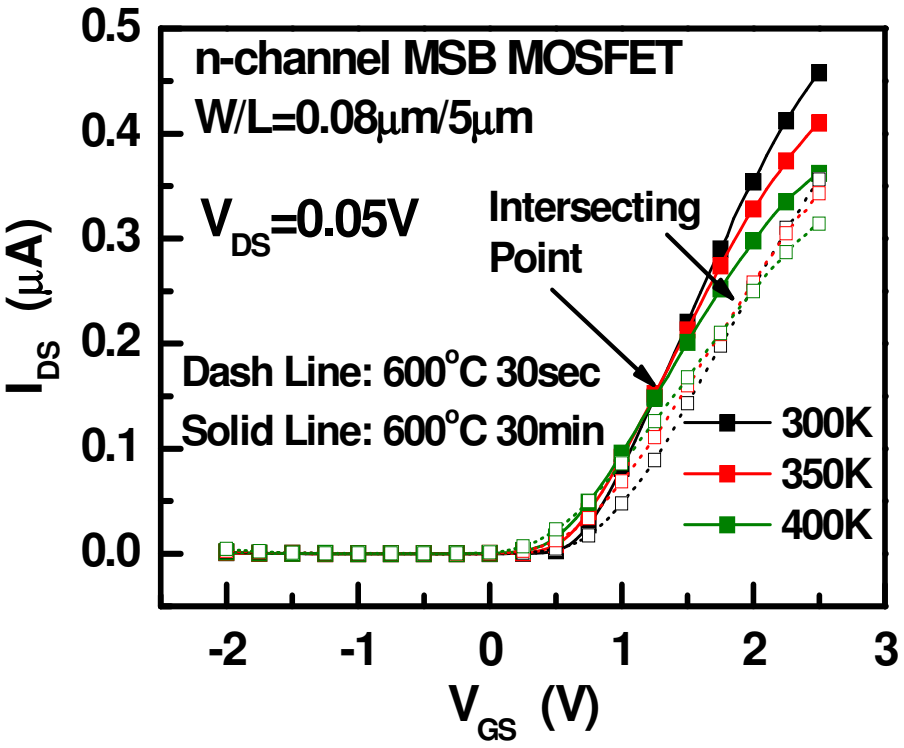


Fig. 2-17 Transfer characteristics of the n-channel MSB MOSFET in linear scale with V_{DS}=0.05 V and the post-ITS annealing at 600 ℃ for 30 sec or for 30 min.

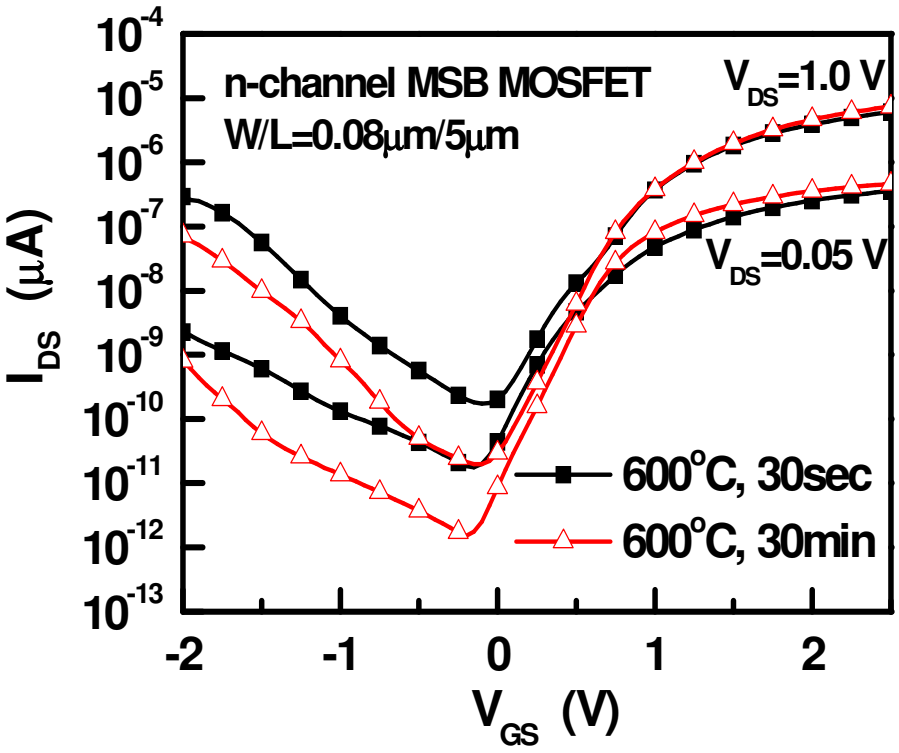


Fig. 2-18 Transfer characteristics of the n-channel MSB MOSFET with the post-ITS annealing at 600 ℃ for 30 sec or for 30 min.

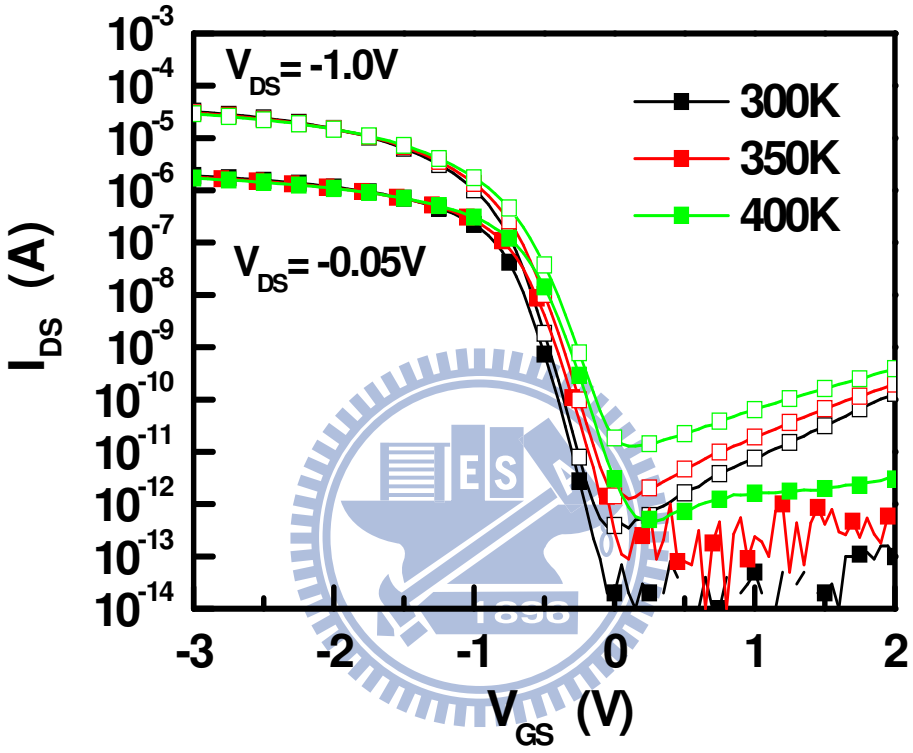


Fig. 2-19 Transfer characteristics of the p-channel MSB MOSFET with gate length equals to 0.5 μm and fin width equals to 0.3 μm.

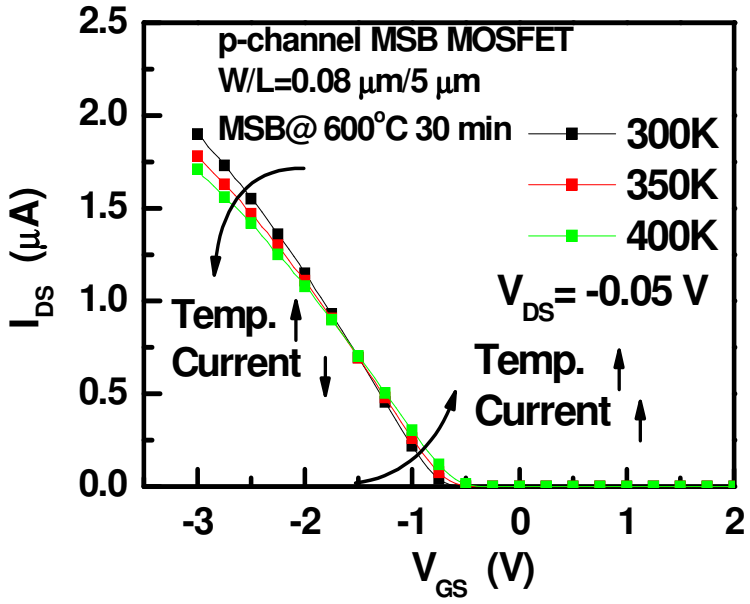


Fig. 2-20(a) Transfer characteristics of the p-channel MSB MOSFET shown in Fig. 19 in linear scale with V_{DS}= -0.05 V.

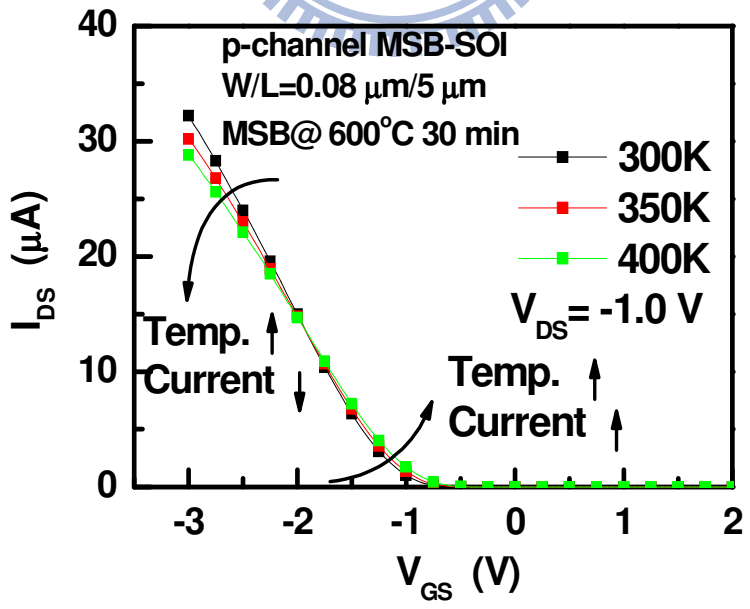


Fig. 2-20(b) Transfer characteristics of the p-channel MSB MOSFET shown in Fig. 19 in linear scale with V_{DS}= -1.0 V.

Chapter 3

Extraction of Bias-Dependent Source Injection Resistance of Modified Schottky Barrier MOSFET

3.1 Introduction

As the CMOS device scales down, multi-gate structure has been reported as a promising candidate to replace the present planar CMOS since it exhibits significant reduction of the short channel effect and extremely well gate controllability [1-4]. Additionally, multi-gate structure, such as FinFET, not only utilizes the top channel but also uses the side-wall channel to conduct source and drain in the on-state, which can enhance current driving capability by increasing the effective channel width. However, as scaling the device, the channel width shrinks and the series resistance outside the channel region gets much larger. The parasitic source/drain resistance (R_{SD}) would become a critical issue for CMOS scaling to nanometer regime [5]. Therefore, metal-silicde source/drain or the so-called Schottky barrier (SB) source/drain MOSFETs are proposed to minimize the R_{SD}, especially for the sheet resistance of source/drain electrodes. Moreover, SB MOSFET also shows some advantages, such as easy processing, low thermal budget, good drain-induced barrier lowing, and better short channel effect. It has been considered as one of the candidates for future nano-

scale devices [6-10]. Nevertheless, poor on/off-state properties and ambipolar characteristic are the drawbacks of SB MOSFETs due to the SB at source/drain junction.

Recently, by using implantation-to-silicide (ITS) method or dopant segregation method to place an highly-doped interfacial layer between the silicided source/drain and Si-channel region, the modified Schottky barrier (MSB) MOSFETs are realized and have been proposed to improve the driving current and reserve the advantages of SB MOSFETs such as better short channel effect and less drain-induced-barrier-lowering [3-4, 11-12]. Although the effective SB height is reduced by the MSB technology to enhance the carrier injected efficiency at source-side, some topics on the MSB junction and MSB MOSFETs are worthy for understanding. Several literatures have been devoted to evaluate the efficiency of the MSB junction. M. Zhang et al. reported that the effective Schottky barrier height can be reduced to about 0.1 eV at high gate bias [13]. A. Kinoshita et al. reported the carrier injection velocity enhancement associated with the velocity overshoot [12]. In chapter 2, it has been also reported that the current transportation mechanism of SB and MSB MOSFETs would change from the thermionic emission to the tunneling and then to the drift-diffusion as the gate bias increases. While the source-side injection resistance is smaller than the channel resistance, the current transportation mechanism is changed from the thermionic emission or tunneling to drift diffusion. The gate bias of the changing point decreases with increasing the thermal budget of MSB junction formation. However, the source injection resistance and its gate bias dependence have not been reported. In this chapter, a modified external loading method is proposed to successfully extract the bias dependent source/drain resistance of MSB MOSFETs. The gate-bias dependent source injection resistance of MSB MOSFETs can be

observed no matter the integrated material of gate dielectric layer. This observation provides a good indicator to evaluate the efficiency of the MSB junction and would be useful for device and circuit simulation.

3.2 Devices Fabrication

Various n-channel multi-gate MSB MOSFETs were fabricated with different gate dielectrics layers, including HfAlO high-k dielectric and SiO_2 dielectric. The n^+ MSB source/drain junction was formed by the ITS technique. The detail process flow of MSB MOSFET has been described in the previous chapter. Therefore, we only list some important processes and structure parameters here.

For the n-channel double-gate MSB MOSFET with HfAlO gate dielectric layer, the starting material was boron-doped 6 inch's SOI wafer with a doping concentration of around $1x10^{15}$ cm^{-3}. The thickness of the Si layer was thinned down to 40 nm and the buried oxide layer was 150-nm-thick. Then, a thick SiO_2 hard mask layer was deposited on the active layer so that only sidewall channel could be conducted. Before the 3-nm-thick HfAlO high-k layer was deposited by an atomic layer deposition (ALD) system, the chemical SiO_2 was formed with around 1-nm-thick. Hence, the high-k gate stacks were formed. Then, 40-nm-thick poly-Si layer was deposited followed by gate pattern definition by e-beam lithography and plasma dry etching, as shown in Fig. 3-1(a). Then, a SiO_2 (10nm)/Si_3N_4 (20nm) composite spacer was formed, as shown in Fig. 3-1(b). The source/drain region was converted into NiSi completely by a 2-step annealing silicide process. Additionally, since the thickness of poly-Si gate is similar to that of the source/drain Si layer, Ni fully-silicided (FUSI) gate structure was obtained, as shown in Fig. 3-1(c). To form the MSB source/drain

junction, P_{31}^{+} ions were implanted into the nickel silicide (ITS) at 20 keV to a dose $5x10^{15}$ cm^{-2} followed by a post-ITS annealing step at 600 ˚C for 30 min. (sample A) or 30 sec. (sample B). During this annealing step, phosphorus atoms diffused out of the silicide and piled up at the Si/silicide interface to form the MSB junction, as shown in Fig. 3-1(d) [14].

For the n-channel double-gate MSB MOSFET with SiO_2 gate dielectric layer, a 3-nm-thick SiO_2 was thermally grown as the gate dielectric followed by a 150-nm-thick poly-Si film deposition. The poly-Si gate was doped by P_{31}^{+} ion implantation at 40 keV to a dose $5x10^{15}$ cm^{-2} followed by a rapid thermal activation at 1025 ˚C for 10 sec. Then, after the same aforementioned process flow for the spacer formation and Ni-salicide process, the source/drain region was converted to NiSi completely. Additionally, polycide gate electrode was built, simultaneously. Then, n^{+} MSB junction were formed by the ITS method and followed by post-ITS annealing step at 600 ˚C for 30 min. (sample C) or 30 sec. (sample D). For the reference devices with 3-nm-thick SiO_2 gate dielectric layer and conventional pn source/drain junction, phosphorus ions were implanted into the source/drain region at 10 keV to a dose $5x10^{15}$ cm^{-2} followed by a rapid thermal activation at 1025 ˚C for 20 sec. The silicide thickness is about 25 nm. Table 1 lists the important structure parameters of these five samples.

Figure 3-2(a) and Fig. 3-2(b) show the typical transfer characteristics and output characteristics of the n-channel MSB MOSFET with HfAlO gate dielectric layer and different thermal budget of post-ITS annealing, i.e. sample A and sample B. Gate length (L_G) equals to 0.2 μm and fin width (W_{Fin}) equals to 5 μm. Due to the successful work from the thin and high concentration source/drain extension layer, the features of the SB MOSFET such as ambipolar and sub-linear current-voltage

characteristics are completely annihilated. Sample A with larger thermal budget of the post-ITS annealing shows better on/off current ratio and larger driving current, indicating more dopants pile-up at the silicide/si interface and modified the SB more strongly. Moreover, Fig. 3-3(a) and Fig. 3-3(b) show the typical transfer characteristics and output characteristics of the n-channel MSB MOSFET with SiO_2 gate dielectric layer and different thermal budget of post-ITS annealing, i.e. sample C and sample D. Gate length (L_G) and fin width (W_{Fin}) equal to 0.08 μm and 5 μm, respectively.

3.3 Modified External Loading Method (ELM)

3.3.1 The ELM on Conventional pn junction MOSFETs

Since the parasitic source/drain resistance (R_{SD}) would largely affect the characteristics of scaled MOSFET. How to extract the reasonable R_{SD} in a simple procedure becomes an important issue. In 1983, the external loading method was proposed to extract the source/drain resistance of MOSFET by S. T. Hsu [15]. The benefit of this method is that only one device is measured and the extracted result is exactly the source/drain resistance of the measured device. Firstly, the MOSFET was biased at moderate gate voltage and operated in the linear region. Thus, assuming the substrate is doped uniformly, the carrier mobility is independent to gate bias, and no R_{SD}, the drain current (I_{DS}) of the conventional pn MOSFETs is given by:

$$I_{DS} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_{TH} - \frac{1}{2}V_{DS})V_{DS}] \qquad \text{for } V_{DS} << (V_{GS}\text{-}V_{TH}) \qquad (1)$$

, where $K = \frac{W}{L}\mu C_{ox}$, W is channel width, L is channel length, μ is carrier mobility, and C_{ox} is gate capacitance.

But, considering the series resistance effect inside the MOSFET, and thus there have some voltage drops in the source resistance (R_S) and drain resistance (R_D). These parasitic resistances can significantly degrade the property of device. The external loading method inserts various external load resistors at source side and the effective circuit diagram of this method is sketched in the Fig. 3-4. The total resistance of the circuit is composed of external load resistance (R_L), source resistance (R_S), drain resistance (R_D), and intrinsic channel resistance (R_{Ch}), where the R_S and R_D are independent to the bias condition on the device with conventional heavily doped pn source/drain junction. The channel current (I_{DS}) of the MOSFET operating at linear region is given by:

$$I_{DS} = \frac{W}{L}\mu C_{ox}(V'_{GS} - V_{TH} - \frac{1}{2}V'_{DS})V'_{DS}$$
$$= K\{[V_{GS} - I_{DS}(R_S + R_L) - V_{TH}] - \frac{1}{2}[V_{DS} - I_{DS}(R_S + R_D + R_L)]\}[V_{DS} - I_{DS}(R_S + R_D + R_L)], \quad (2)$$

This equation models the intrinsic channel property and it is independent of the source/drain junction. Furthermore, by choosing suitable external loads to satisfy the following condition,

$$V_{GS} - V_{TH} - \frac{1}{2}V_{DS} >> \frac{I_{DS}}{2}|R_D - R_S - R_L| \quad (3)$$

, eq. (2) can be simplified to:

$$I_{DS} = K\{[V_{GS} - V_{TH} - \frac{1}{2}V_{DS}][V_{DS} - I_{DS}(R_T + R_L)], \quad (4)$$

After some manipulations, this equation becomes

$$\frac{1}{I_{DS}} = \frac{R_T + R_L}{V_{DS}} + \frac{1}{K(V_{GS} - V_{TH} - \frac{1}{2}V_{DS})V_{DS}} \quad (5)$$

, where $R_T = R_S + R_D$ and R_T represents the total external resistance of this MOSFET. Then, by plotting $1/I_{DS}$ versus R_L with V_{GS} as a parameter, the x-axis intersection R_{L0} could be expressed as

$$-R_{L0}(V_{GS}) = R_T + K^{-1}(V_{GS} - V_{TH} - \frac{1}{2}V_{DS})^{-1} \quad (6)$$

By plotting $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$, the y-axis intersection gives the R_T.

Figure 3-5 presents the $1/I_{DS}$ versus R_L plot of the MOSFET with the conventional pn source/drain junction (sample E). Good linearity and the x-axis intersections give the R_{L0} to provide further extraction of R_T. Then, the $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot of the MOSFET with conventional source/drain junction (sample E) is shown in Fig. 3-6. The good linearity as predicted by eq. (6) confirms that the external loading method can be applied well on the SOI devices. The extracted series resistance equals to 1.13k Ω-μm. The inset shows the schematic device structure.

3.3.2 The Modify ELM on MSB MOSFETs

By using this method to the MSB MOSFET with SiO_2 gate dielectric layer and post-ITS annealing at 600 ˚C for 30 min., i.e. sample C, good linearity can also be observed in the $1/I_{DS}$ versus R_L plot and various R_{L0} are extracted, as shown in Fig. 3-7. However, for the MSB MOSFET, the good linearity behavior can not be observed in the $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot at similar gate bias range. Fig. 3-8 shows the $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot of the sample C. This non-linear $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot deviates from eq. (5). This confliction arises from that the R_T

of MSB MOSFET is dependent on bias condition, which conflicts with the basic assumption of the external loading method. Hence, the above observation indicates that the resistance of the MSB junction varies at different bias condition since the height and the thickness of the modified SB change as the gate voltage changes. Therefore, to solve this problem, we assume that R_T can be treated as a constant in a small ΔV_G range ($V_{GX} \pm \Delta V_G/2$). The x-axis intersection of the $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot extracted at $V_{GS}=V_{GX}-\Delta V_G/2$, V_{GX}, and $V_{GX}+\Delta V_G/2$ could be explained as the R_T at V_{GX}. Consequently, the bias dependence of R_T can be obtained with repeating this procedure [16].

Figure 3-9 shows the extracted R_T of samples C and D as a function of $(V_{GS}-V_{TH}-0.5V_{DS})$. It is observed that the R_T is exponentially proportional to the bias condition of $(V_{GS}-V_{TH}-0.5V_{DS})$. This is reasonable because the source/drain resistance is dominated by the effective SB height at source side and the effective SB height is linearly proportional to V_{GS} in the measured V_{GS} range [13]. The R_T of device with MSB annealing for 30 min is much lower than that with MSB annealing for 30 sec because the insufficient post-ITS thermal budget (600 ºC, 30 sec) results in higher source injection resistance. Similarly, for the MSB MOSFET with HfAlO gate dielectric layer with post-ITS annealing at 600 ˚C for 30 min. and 30sec., i.e. samples A and B, due to the bias dependent resistance of the MSB junction, non-linear behavior is also observed in the $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot, as shown in Fig. 3-10(a) and (b). Then, by utilizing the modified ELM to extract the series resistance, the extracted R_T of sample A as a function of $(V_{GS}-V_{TH}-0.5V_{DS})$ is shown in Fig. 3-11. The R_T is also exponentially proportional to the gate bias because carrier injection resistance is exponentially proportional to the effective SB height. In addition, the higher thermal budget results in low R_T. Therefore, the proposed modified ELM can both

successfully extracted the series resistance of the MSB MOSFETs with conventional SiO_2 or high-k HfAlO gate dielectric layers. Additionally, extrapolating R_T to (V_{GS}-V_{TH}-$0.5V_{DS}$) = 0.5 V in Fig. 3-9 and Fig. 3-11, the R_T would be very close to that of the conventional MOSFET. It should be noted that as device is biased in the on-state, the effect of MSB at drain side is much smaller than the MSB at source side. Therefore, the decreasing of R_T is mainly attributed to the decrease of source injection resistance.

3.3.3 Selection of R_{Load} on Modify ELM

From the equation (3) of the external loading method, since the symmetry of the source and drain, the R_S and the R_D can be considered to have the same value. Hence, the upper limitation of R_L is obtained:

$$R_L << \frac{(2V_{GS} - 2V_{TH} - V_{DS})}{I_{DS}} \tag{7}$$

Because too large R_L adds to the circuit will dominate the measured total resistance and then it is hardly to extract the relatively small series resistance. This relationship (eq.(7)) provides a good guideline for extracting the series resistance at moderate large (V_{GS}-V_{TH}-$0.5V_{DS}$) bias condition.

For the MSB MOSFET, since the extracted series resistance exhibits gate bias dependency, the R_T at small (V_{GS}-V_{TH}-$0.5V_{DS}$) bias condition is also required to be extracted. However, while biasing at smaller gate voltage, the channel resistance is increased. Hence, if too smaller R_L are selected to connect to the source-side of device, the influences of drain current by these loads are barely to observe. Therefore, the slope in the $1/I_{DS}$ versus R_L plot will near to zero and it may induce errors in the further steps for extracting the R_T of MSB MOSFET. For example, Fig. 3-12 shows

the $1/I_{DS}$ versus R_L plot of the sample A connected to the smaller resistance of external load. The resistance of these selected loads is from 805 Ω to 9.67k Ω. Clearly, since the channel resistance is much higher than the selected resistance, the slope of $1/I_{DS}$ is nearly zero, indicating the influences of I_{DS} are quiet small.

Nevertheless, by selecting suitable loads which have similar magnitude to the measured resistance, i.e. $R_{DS}= V_{DS}/ I_{DS}$, the effect by connecting these loads can be obviously measured. Figure 3-13 shows the $1/I_{DS}$ versus R_L plot of the sample A connected to the larger resistance of external load. The resistance of these selected loads is from 21.8k Ω to 91.8k Ω. Good linearity and positive slope of these lines can be observed. Therefore, appropriate $-R_{L0}$ and thus reasonable R_T can be obtained by the modified ELM. In short, for obtaining the series resistance at smaller gate bias condition, moderate larger R_L must be used but these R_L need to obey the inequality as shown in eq. (7).

3.3.4 Bias-Dependent Source Injection Resistance of MSB MOSFETs

According to the above observations, the complete bias-dependent source injection of MSB MOSFET can be obtained from the small gate bias, i.e. slightly larger than V_{TH}, to the high gate bias by applying modified ELM and choosing suitable external loads. Figure 3-14 presents the $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot of sample C at V_{DS} = 0.05 V to 0.3 V. These curves imply that the resistance of MSB junction varies as the gate voltage increases to reduce the effective SB height. Figures 3-15 (a) and (b) display the extracted series resistance of sample C as a function of $1/(V_{GS}-V_{TH}-0.5V_{DS})$ in linear scale and log scale, respectively. When biasing at $(V_{GS}-V_{TH}-0.5V_{DS})$ = 0.035 V and V_{DS} = 0.05 V, the R_T is 79k Ω. Then, as the $(V_{GS}-V_{TH}-0.5V_{DS})$ increases, the R_T reduces dramatically and decays exponentially till to $(V_{GS}-$

V_{TH}-$0.5V_{DS}$) around 0.5 V. Moreover, this resistance reduction saturates at higher (V_{GS}-V_{TH}-$0.5V_{DS}$) bias and the R_T is close to that of the conventional MOSFET. Similar behaviors are also observed in the sample D which has less thermal budget. Figure 3-16 (a) and (b) display the extracted series resistance of sample D as a function of $1/(V_{GS}$-V_{TH}-$0.5V_{DS})$ in linear scale and log scale, respectively. Although some fluctuations due to the non-ideal probe contact with the NiSi pads, clear trend of the resistance reduction can be obtained. Therefore, from the aforecited observations, the modified SB still not low and thin enough while the gate bias is only slightly larger than the threshold voltage and the extracted series resistance is mainly came from the source-side modified SB, indicating that the carrier transportation mechanisms would be affected by these modified SB in this situation. As the gate bias increases, the source-side SB gets thinner and lower. Moreover, while the gate bias is large enough, the modified SB at source-side can be seen as transparent for the carrier transportation. Hence, the extracted series resistance is constant and mainly comes from the resistance outside the MSB source/drain junction, which is similar to that of the conventional MOSFET.

3.4 Conclusions

In this chapter, a modified external load resistance method was proposed to extract the bias dependent source injection resistance of the MSB MOSFET no matter what dielectrics are used as the gate dielectric layer. To use this method to extract source injection resistance at small gate bias condition, which is slightly larger than the threshold voltage, moderate larger R_L must be selected. The bias dependent source injection resistance is observed. The source injection resistance is exponentially

proportional to (V_{GS}-V_{TH}-$0.5V_{DS}$) and saturates at moderate high gate voltage, which the source/drain resistance of MSB MOSFET would be close to that of the conventional MOSFET at that gate bias. This observation indicates that the modified SB still dominate the carrier transportation at small gate bias but it would be vanished and became transparent for the current flow at moderate high gate bias condition. Additionally, without sufficient post-ITS thermal budget, the source injection resistance can not be suppressed effectively at reasonable V_{GS}. Moreover, the proposed modified external loading method provides a good method to evaluate the efficiency of the MSB junction directly.

References

[1] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King, J. Bokor, C. Hu, M.-R. Lin, and D. Kyser, "FinFET scaling to 10 nm gate length," in *IEDM Tech. Dig.*, 2002, pp. 251-254.

[2] N. Lindert, L. Chang, Y.-K. Choi, E. H. Anderson, W.-C. Lee, T.-J. King, J. Bokor, and C. Hu,"Sub-60-nm Quasi-Planar FinFETs Fabricated Using a Simplified Process," *IEEE Electron Devices Lett.,* vol. 22, no. 10, pp. 487-489, 2001.

[3] B.-Y. Tsui, C.-P. Lin, "A novel 25-nm modified schottky-barrier FinFET with high performance," *IEEE Electron Device Lett.,* vol. 25, no. 6, pp. 430-432, 2004.

[4] A. Kaneko, A. Yagishita, K. Yahashi, T. Kubota, M. Omura, K. Matsuo, I. Mizushima, K. Okano, H. Kawasaki, T. Izumida, T. Kanemura, N. Aoki, A. Kinoshita, J. Koga, S. Inaba, K. Ishimaru, Y. Toyoshima, H. Ishiuchi, K. Suguro, K. Eguchi, Y. Tsunashima, "High-Performance FinFET with Dopant-Segregated Schottky Source/Drain," in *IEDM Tech. Dig.*, 2006, pp. 893-896.

[5] S. D. Kim, C. M. Park, and J. C. S. Woo, "Advanced Model and Analysis of Series Resistance for CMOS Scaling Into Nanometer Regime-Part : Quantitative Analysis," *IEEE Trans. Electron Devices,* vol. 49, no. 3, pp. 467-472, 2002.

[6] J. P. Synder, C. R. Helms, and Y. Nishi, "Experimental investigation of a PtSi source and drain field emission transistor," *Appl. Phys. Lett.,* vol. 67, no. 10, p. 1420, 1995.

[7] J. R. Tucker, "Schottky barrier MOSFETs for Silicon nanoelectronics," in *Advanced Workshop on Frontiers in Electronics,* 1997, pp. 97-100.

[8] M. Nishisaka and T. Asano, "Reduction of the Floating Body Effect in SOI

MOSFETs by Using Schottky Source/Drain Contacts," *Jpn. J. Appl. Phys.*, vol. 37, pp. 1295-1299, 1998.

[9] C. Wang, J. P. Synder, and J. R. Tucker, " Sub-40 nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol.74, no. 8, pp. 1174-1176, 1999.

[10] W. Saitoh, S. Yamagami, A. Itoh, and M. Asada, " 35 nm metal gate p-type metal-oxide- semiconductor field-effect-transistor with PtSi Schottky source/drain on separation by implanted oxygen substrate," *Jpn. J. Appl. Phys.*, vol.38, pp. 629-631, 1999.

[11] A. Kinoshita, Y. Tsuchiya, A. Yagishita*, K. Uchida and J. Koga, "Solution for High-Performance Schottky-Source/Drain MOSFETs: Schottky Barrier Height Engineering with Dopant Segregation Technique," in *VLSI Symp. Tech. Dig.*, 2004, pp. 168-169.

[12] A. Kinoshita, T. Kinoshita, Y. Nishi, K. Uchida, S. Toriyama, R. Hasumi, and J. Koga, "Comprehensive Study on Injection Velocity Enhancement in Dopant-Segregated Schottky MOSFETs," in *IEDM Tech. Dig.*, 2006, pp. 79-82.

[13] M. Zhang, J. Knoch, Q.T. Zhao, A. Fox, St. Lenk, and S. Mantl, "Low temperature measurements of Schottky-barrier SOI-MOSFETs with dopant segregation," *Electronics Letters,* vol. 41, no. 19, pp. 1085-1086, 2005.

[14] Bing-Yue Tsui and Chia-Pin Lin, "Process and Characteristics of Modified-Schottky-Barrier (MSB) p-Channel FinFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 11, pp. 2455-2462, 2005.

[15] S. T. Hsu, "A simple method to determine series resistance and. K. factor of an MOS field effect transistor," *RCA Review*, vol. 44, pp. 424-429, 1983.

[16] G. J. Hu, C. Chang, and Y. T. Chia, "Gate-Voltage-Dependent Effective Channel

Length and Series Resistance of LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. 34, no.12, pp. 2469-2475, 2005.

Table 3.1: The important structure parameters of samples A-E.

	Gate Electrode	Gate Dielectric Layer	Source/Drain junction type	S/D Activation Condition
A	FUSI	$HfAlO/SiO_x$ = 3 nm/1 nm	n^+ MSB	600^oC, 30 min.
B	FUSI	$HfAlO/SiO_x$ = 3 nm/1 nm	n^+ MSB	600^oC, 30 sec.
C	Polycide	SiO_2 = 3 nm	n^+ MSB	600^oC, 30 min.
D	Polycide	SiO_2 = 3 nm	n^+ MSB	600^oC, 30 sec.
E	Polycide	SiO_2 = 3 nm	Conventional	1025^oC, 20 sec.

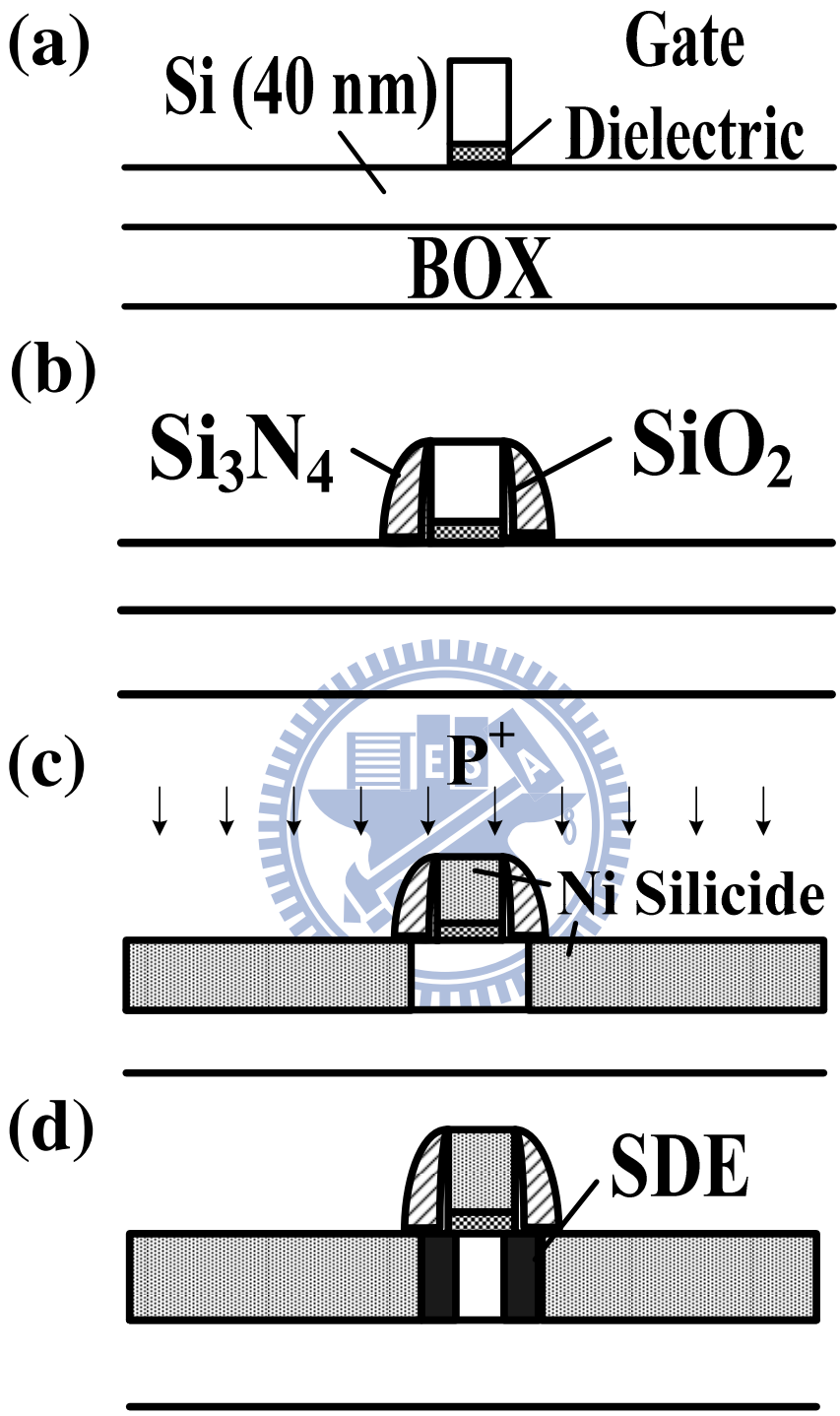


Fig. 3-1 Main Process flow of n-channel double-gate MSB MOSFET with HfAlO gate dielectric layer.

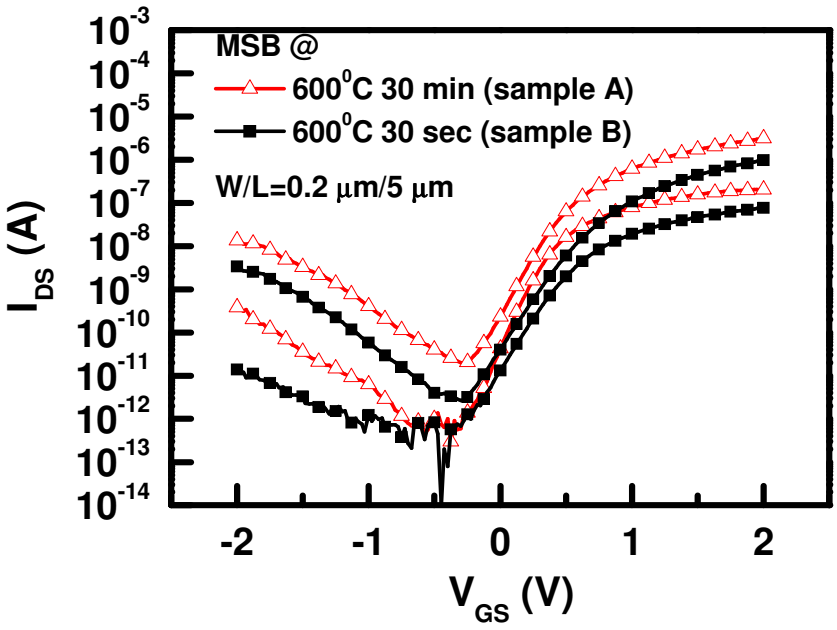


Fig. 3-2(a) Transfer characteristics of the n-channel MSB MOSFET with HfAlO gate dielectric layer and two different post-ITS annealing.

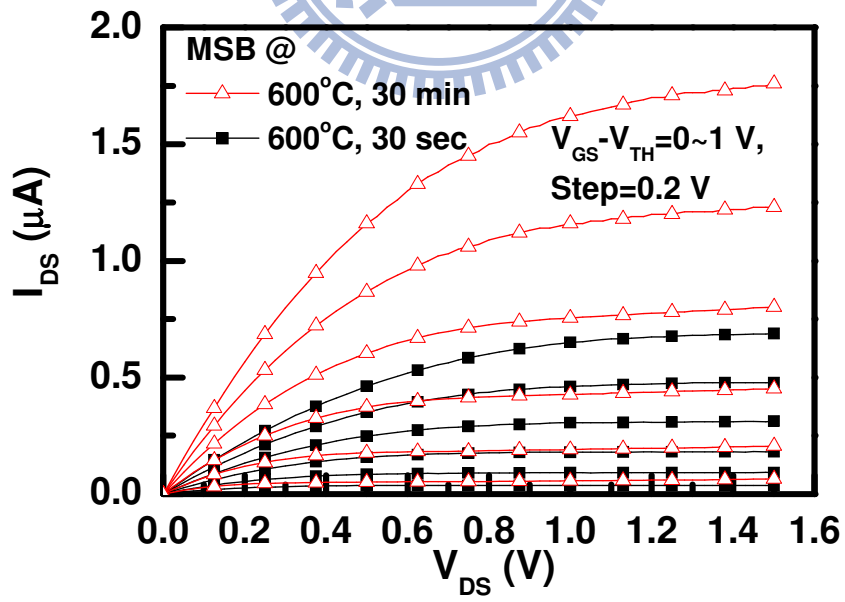


Fig. 3-2(b) Output characteristics of the n-channel MSB MOSFET with HfAlO gate dielectric layer and two different post-ITS annealing.

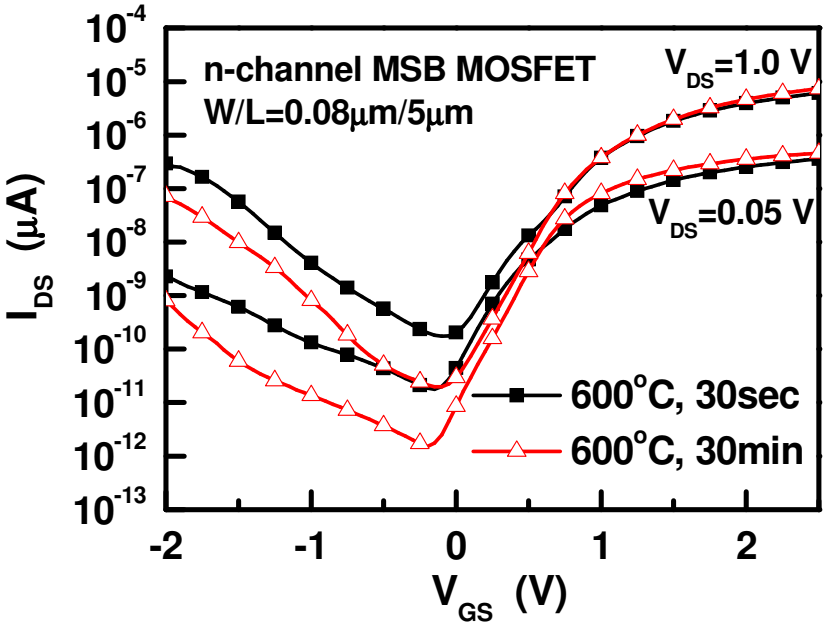


Fig. 3-3(a) Transfer characteristics of the n-channel MSB MOSFET with SiO_2 gate dielectric layer and two different post-ITS annealing.

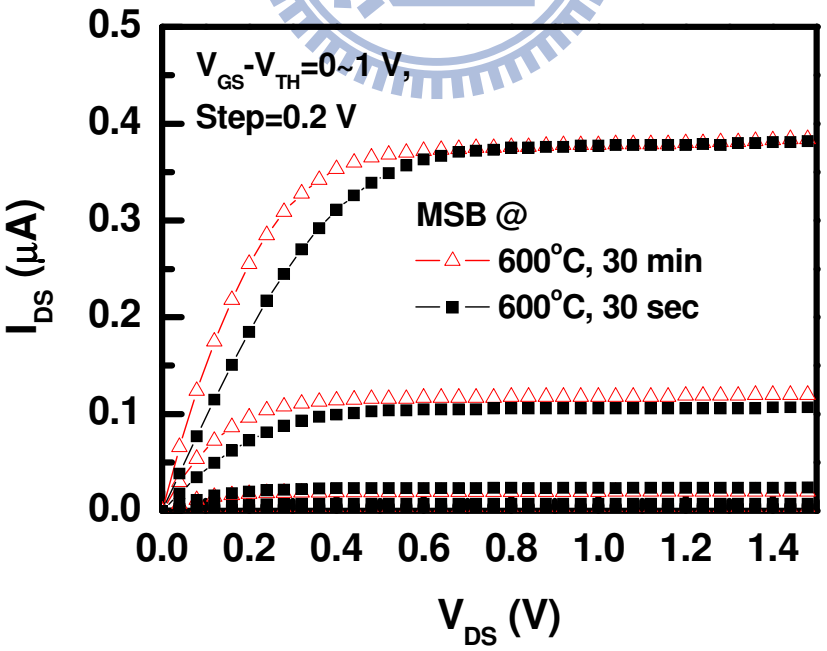


Fig. 3-3(b) Output characteristics of the n-channel MSB MOSFET with SiO_2 gate dielectric layer and two different post-ITS annealing.

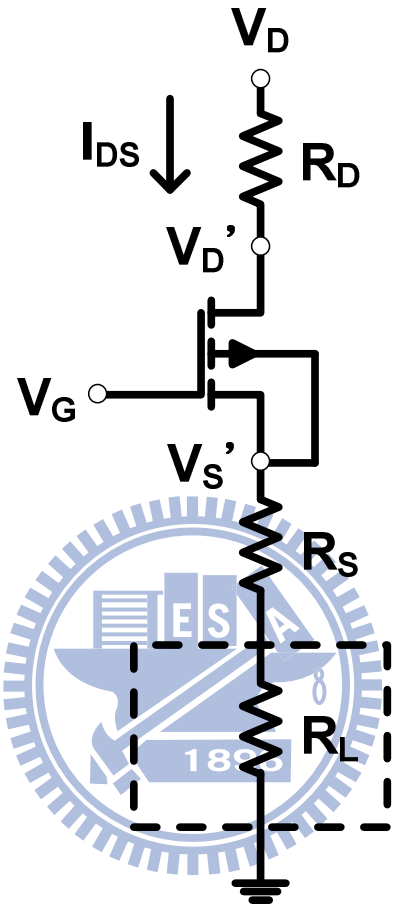


Fig. 3-4 The Effective circuit diagram of the external loading method. An external load resistor with suitable range of impendence is connected to the source terminal.

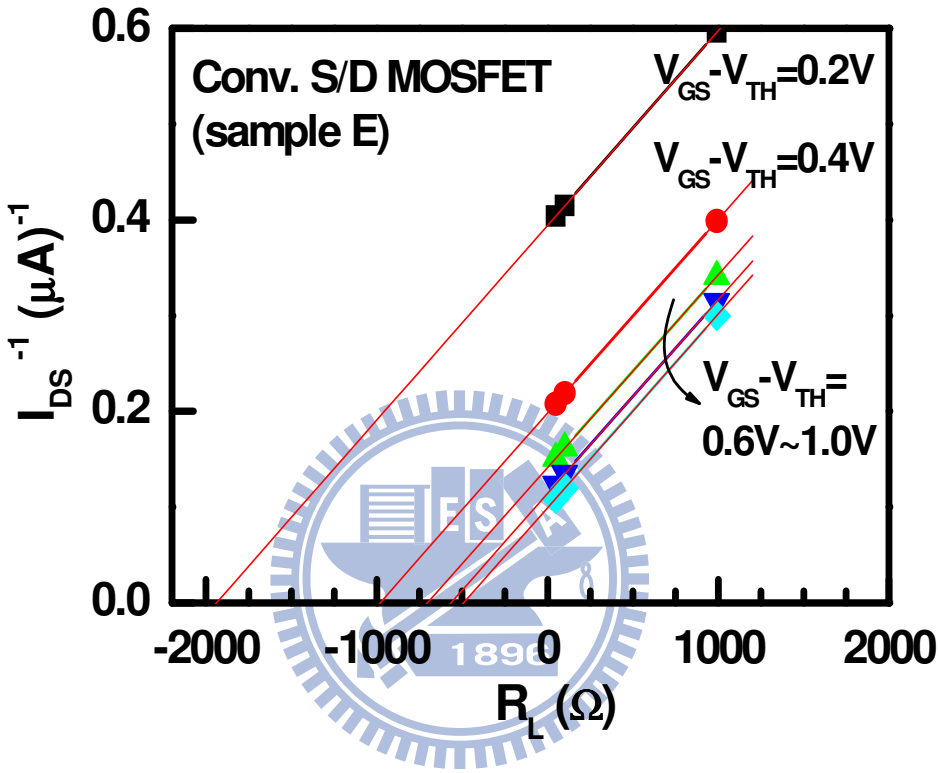


Fig. 3-5 The $1/I_{DS}$ versus R_L plot of the conventional pn source/drain MOSFET with SiO_2 gate dielectric layer (sample E).

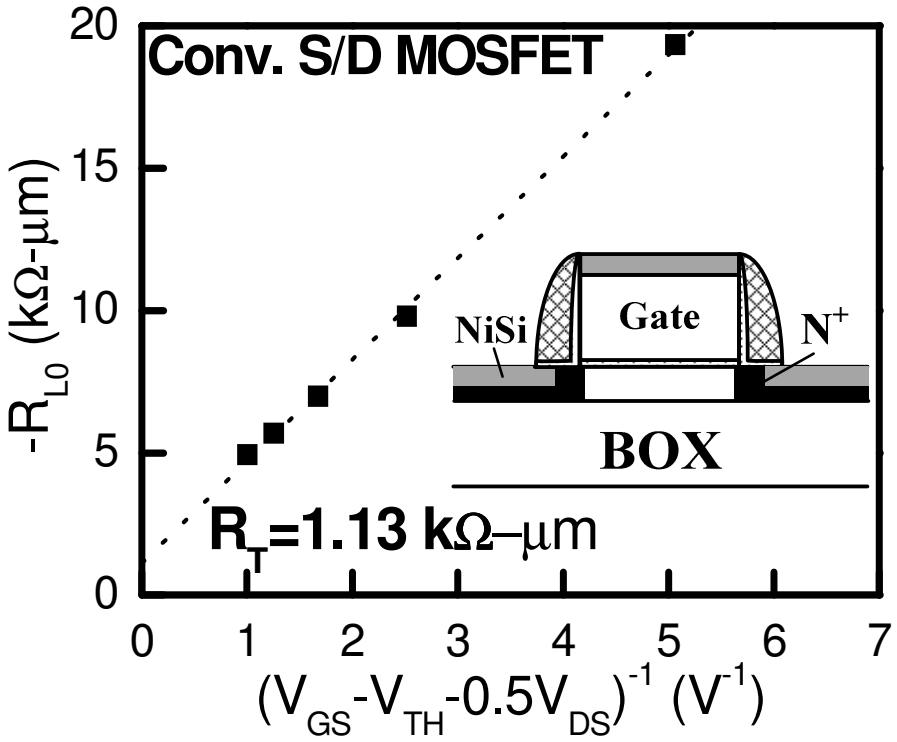


Fig. 3-6 The $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot of sample E. The inset displays the illustration of device structure.

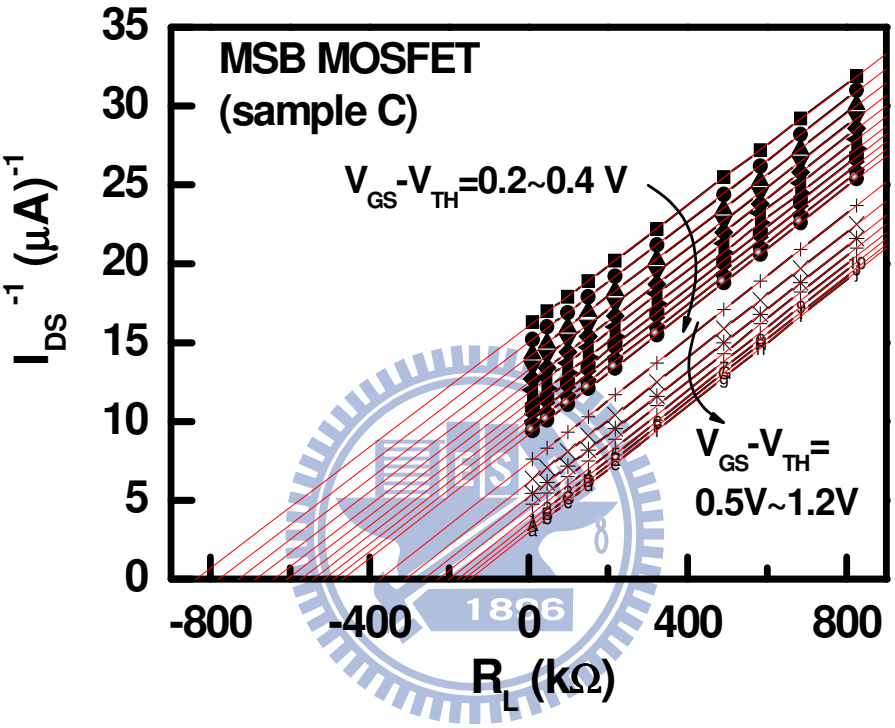


Fig. 3-7 The $1/I_{DS}$ versus R_L plot of MSB source/drain MOSFET with SiO_2 gate dielectric layer (sample C).

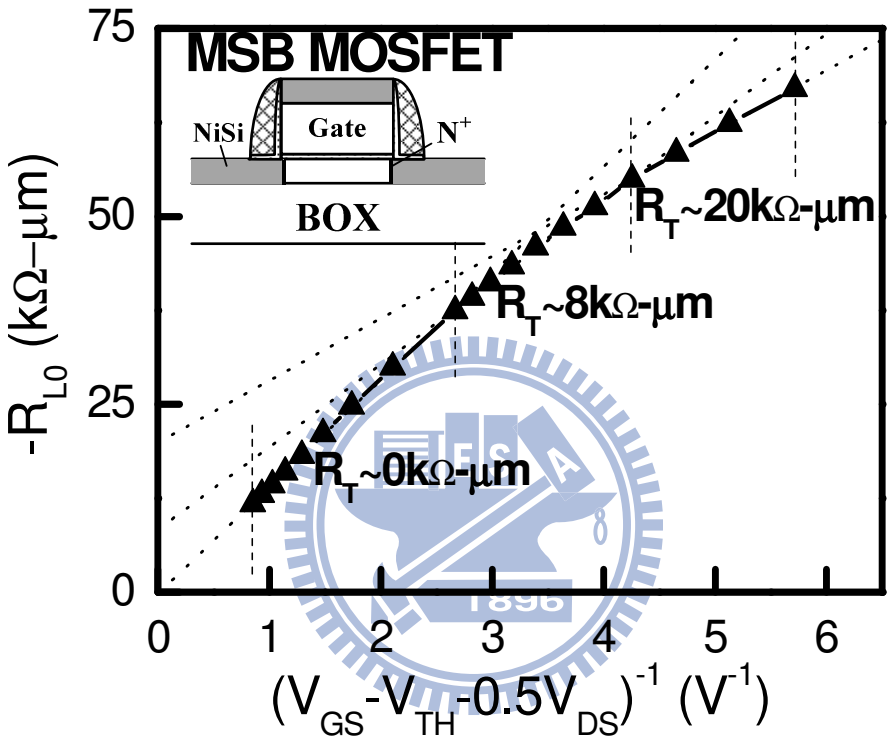


Fig. 3-8 The $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot of sample C. The inset displays the illustration of device structure.

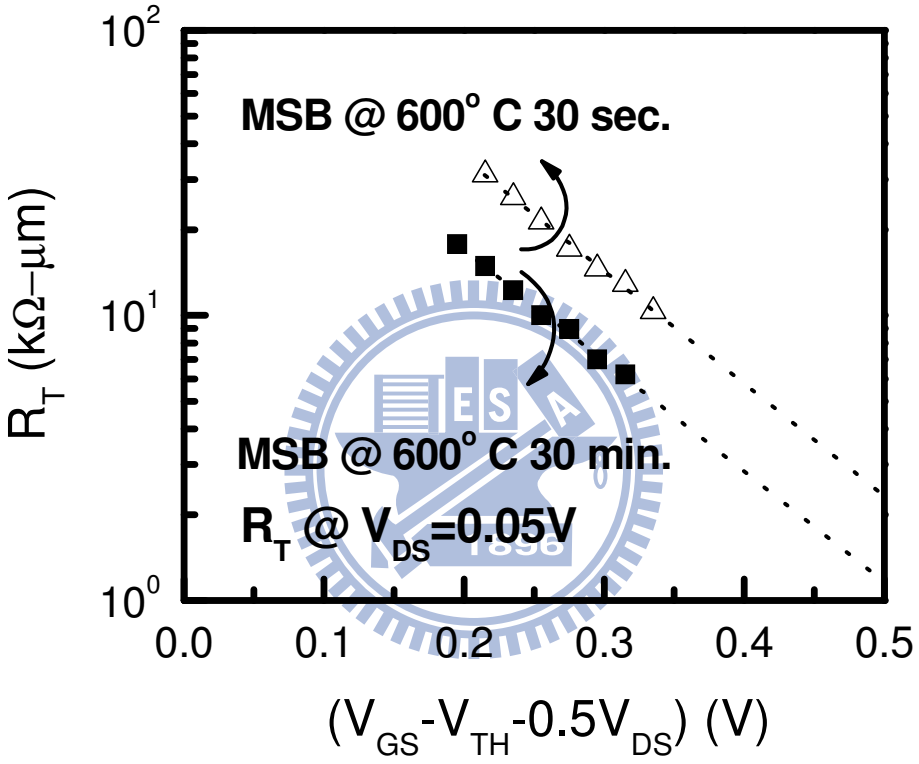


Fig. 3-9 Extracted R_T as a function of $(V_{GS}\text{-}V_{TH}\text{-}0.5V_{DS})$ of the MSB MOSFET SiO_2 gate dielectric layer and two different post-ITS annealing (sample C and sample D).

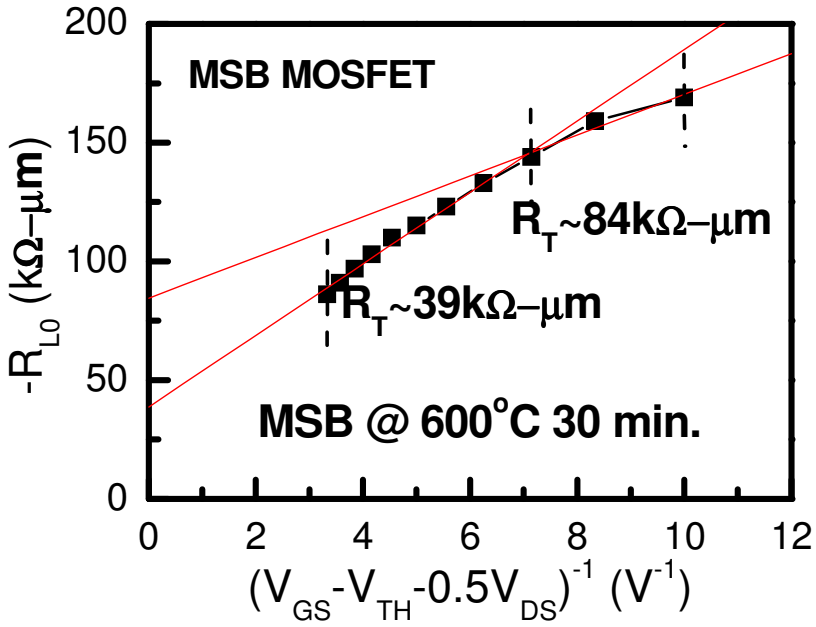


Fig. 3-10(a) The $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot of MSB MOSFET with HfAlO gate dielectric layer (sample A).

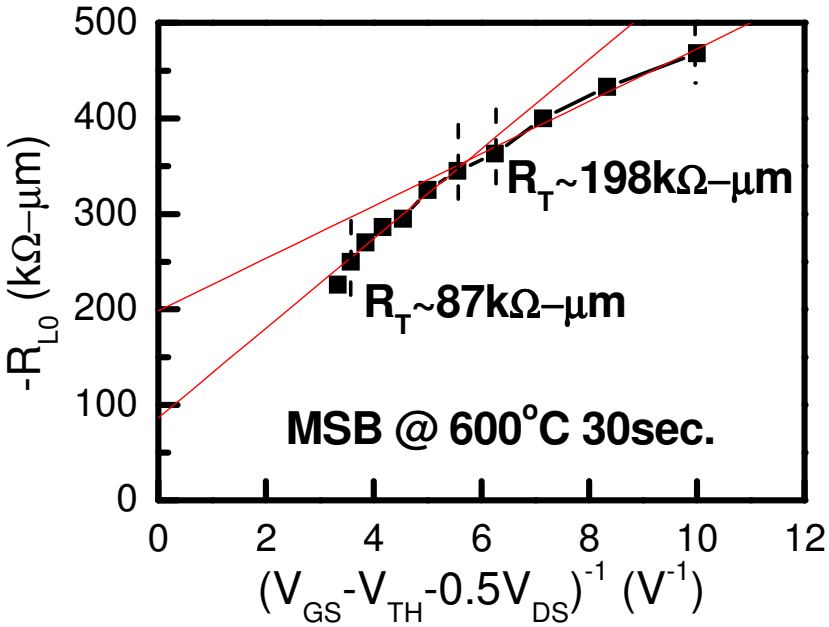


Fig. 3-10(b) The $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot of MSB MOSFET with HfAlO gate dielectric layer (sample A).

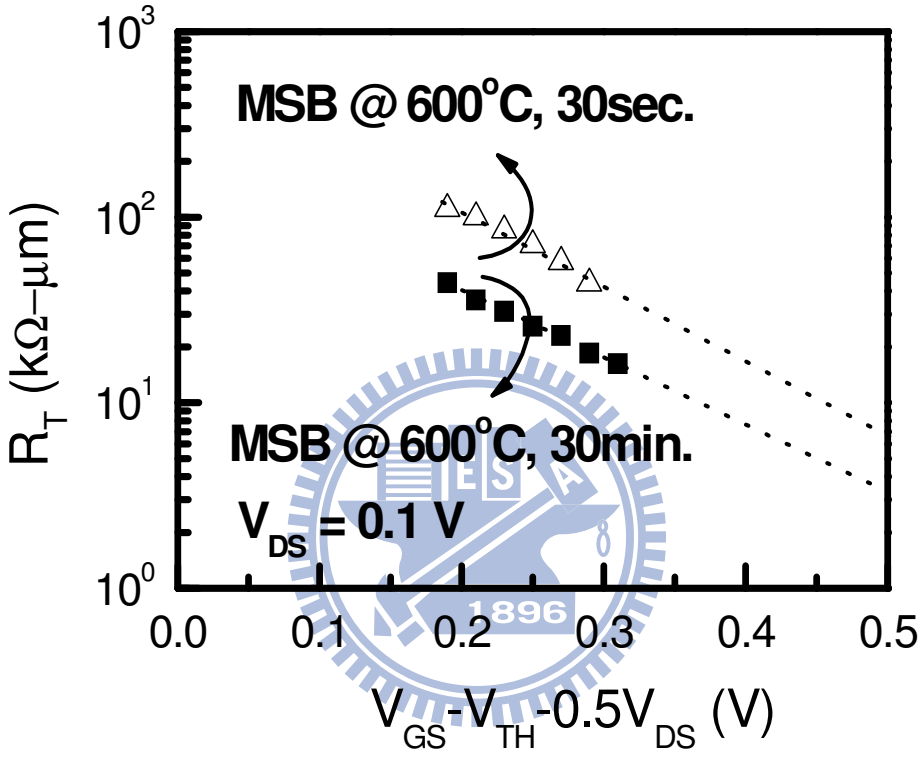


Fig. 3-11 Extracted R_T as a function of $(V_{GS}\text{-}V_{TH}\text{-}0.5V_{DS})$ of the MSB MOSFET with HfAlO gate dielectric layer and two different post-ITS annealing (sample A and sample B).

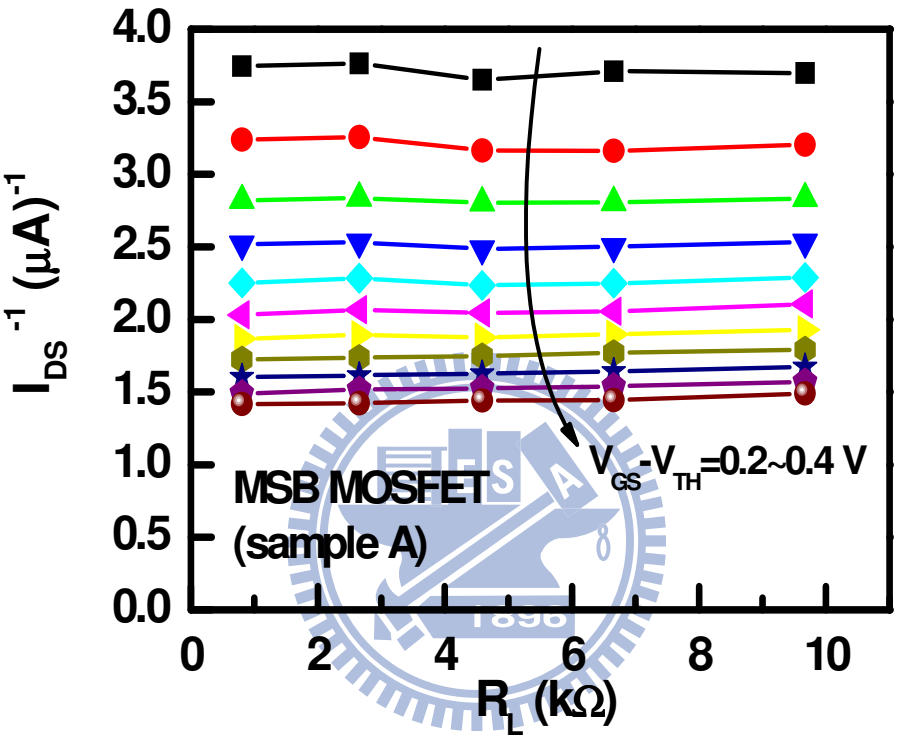


Fig. 3-12 The $1/I_{DS}$ versus R_L plot of MSB source/drain MOSFET with HfAlO gate dielectric layer (sample A). Smaller loads are used to extract the R_T.

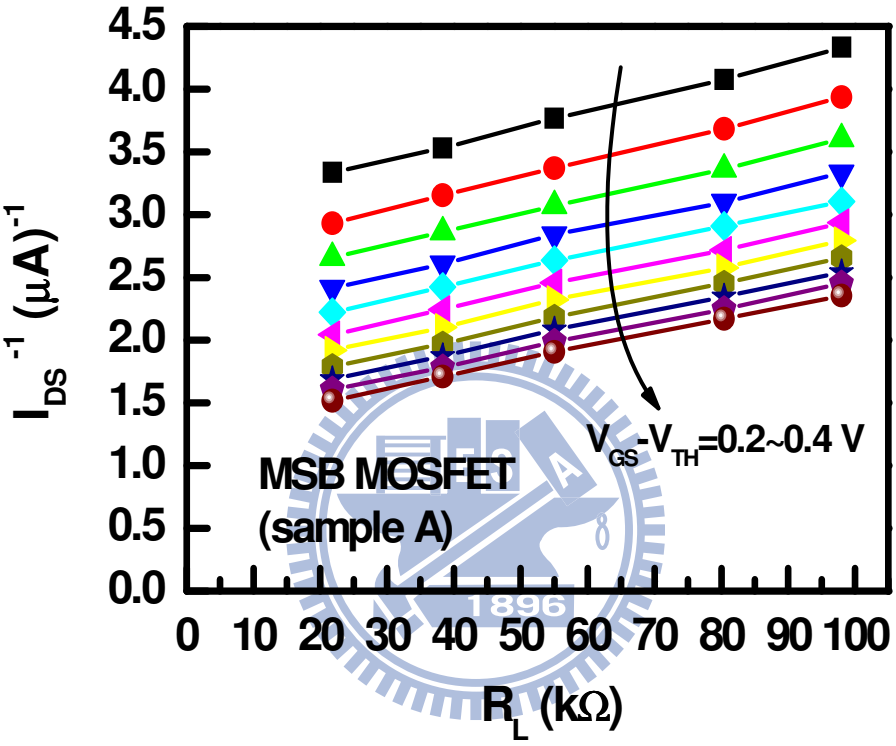


Fig. 3-13 The $1/I_{DS}$ versus R_L plot of MSB source/drain MOSFET with HfAlO gate dielectric layer (sample A). Larger loads are used to extract the R_T.

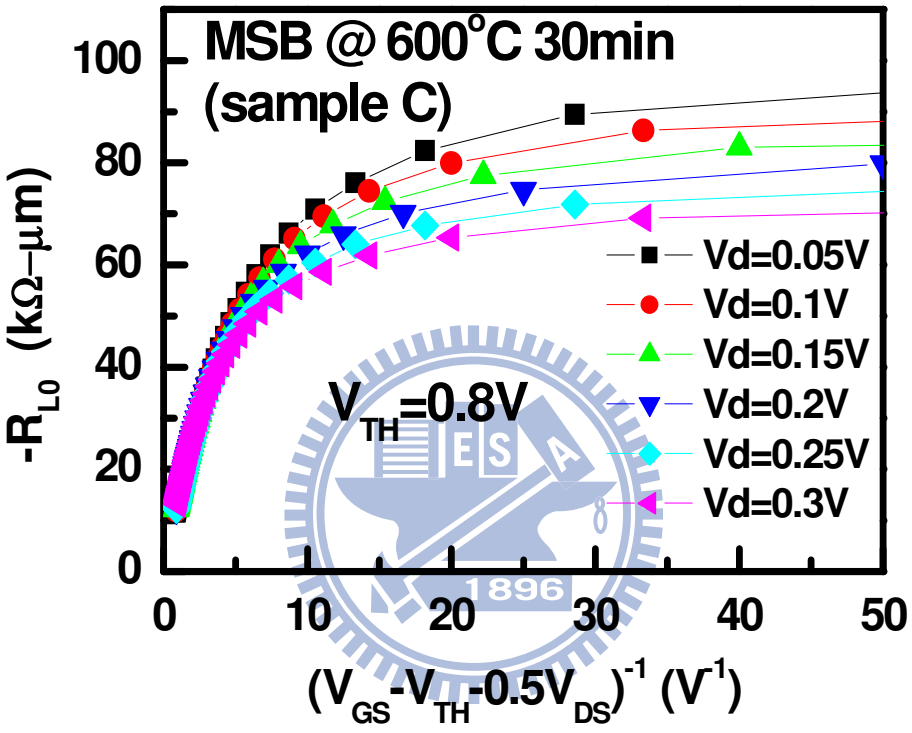


Fig. 3-14 The $-R_{L0}$ versus $1/(V_{GS}-V_{TH}-0.5V_{DS})$ plot of MSB MOSFET with SiO_2 gate dielectric layer (sample C) at V_{DS} = 0.05 V to 0.3 V.

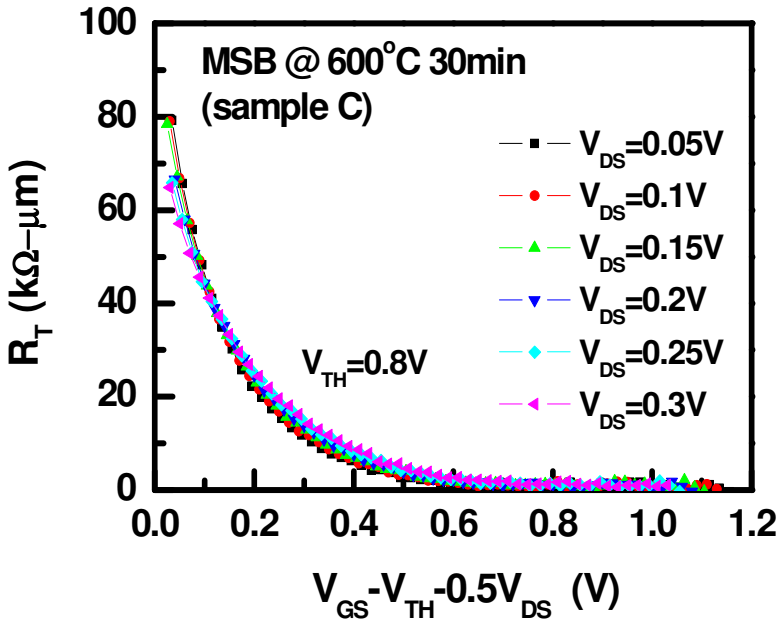


Fig. 3-15(a) Extracted series resistance of sample C as a function of $(V_{GS}-V_{TH}-0.5V_{DS})$ in the linear scale.

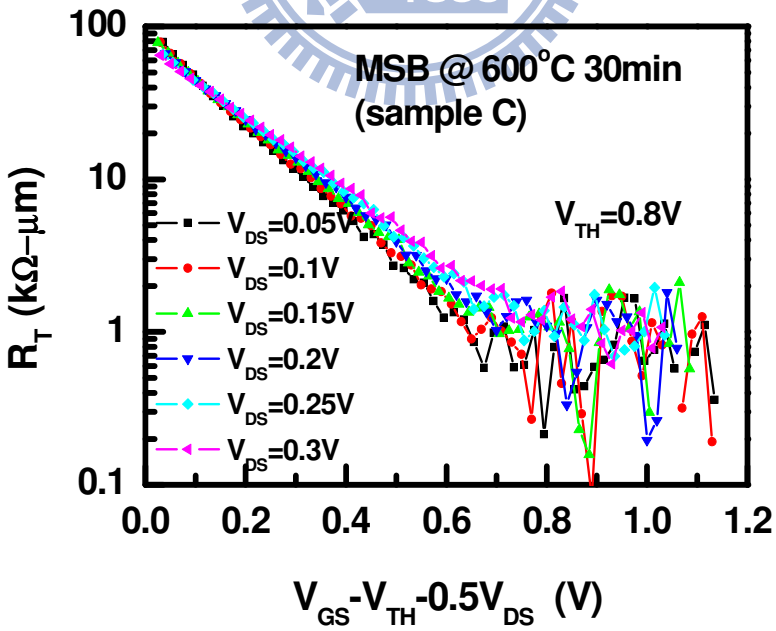


Fig. 3-15(b) Extracted series resistance of sample C as a function of $(V_{GS}-V_{TH}-0.5V_{DS})$ in the log scale.

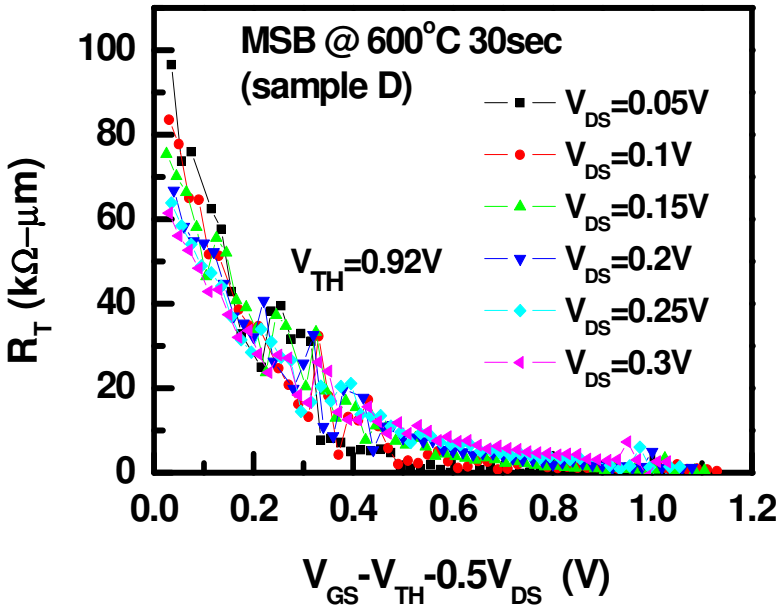


Fig. 3-16(a) Extracted series resistance of sample D as a function of $(V_{GS}-V_{TH}-0.5V_{DS})$ in the linear scale.

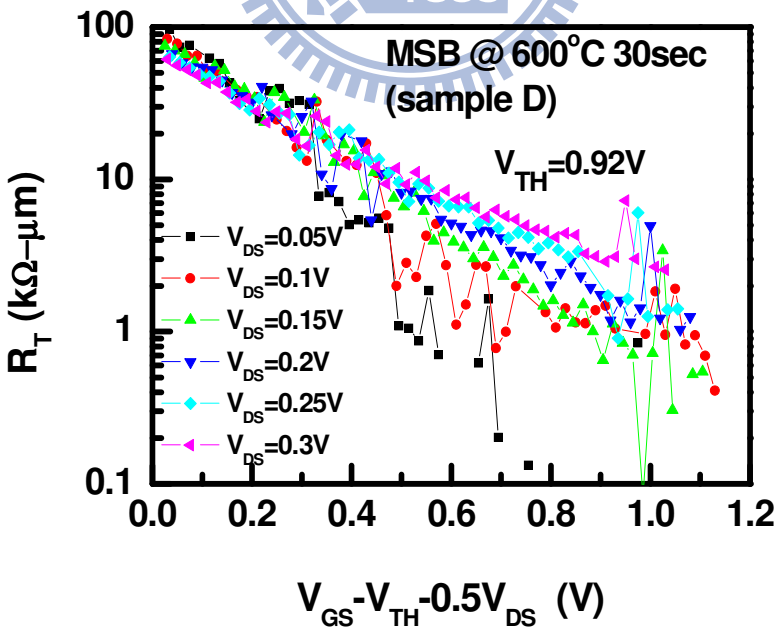


Fig. 3-16(b) Extracted series resistance of sample D as a function of $(V_{GS}-V_{TH}-0.5V_{DS})$ in the log scale.

Chapter 4

Nano-scale Multi-gate TiN Metal Nanocrystal Memory

4.1 Introduction

Integrating multi-gate structure into the CMOS device provides lots of advantages and helps for the further scaling of CMOS technology. In the previous two chapters, we focus on the modified Schottky barrier MOSFET with multi-gate structure. In fact, the nonvolatile memory has also been considered to change its planar structure to the three-dimensional structure. In addition, some inevitable issues would rise as scaling nonvolatile memory, which is mainly originated from the storage material and it is suspected to use another applicable material as the new storage node. In this chapter, we propose a novel flash memory which integrates with the multi-gate structure.

Since 1967, D. Kahng and S. M Sze has invented the first floating gate nonvolatile memory (NVM) at Bell Lab [1], the industry of nonvolatile memory developed extremely fast in the past four decades and the floating gate (FG) devices are widely applied in present NVM for data storage. Floating gate NVM has the following advantages: large memory window, high program/erase (P/E) speed, and good reliability for commercial applications. In recent years, flash memory becomes

one of the fastest growing semiconductor technologies and provides hundreds of portable electronic products. However, the International Technology Roadmap for Semiconductors (ITRS) forecasts that several critical challenges would limit the conventional FG memory scaling around 25 nm node [2]. The main issue is un-scalable tunneling oxide thickness for maintaining acceptable retention performance. Therefore, a high operation voltage is required and the thickness of tunneling oxide layer is predicted to keep at 6-7 nm [2]. Additionally, an increased floating gate coupling effect is another issue for the continually closing floating gate memory cells. Therefore, NAND technology is projected to migrate to the charge trapping devices with discrete traps for charge storage, such as silicon/ oxide/ nitride/ oxide/ silicon (SONOS) and nanocrystal structures [2].

SONOS-type memories which store charges in the discrete trap node of theirs silicon nitride layer exhibit improved retention performance so that the tunneling oxide thickness can be reduced to increase the P/E speed and decrease operation voltage [3-8]. Besides, some advanced SONOS memories such as bandgap engineered SONOS (BE-SONOS) and TaN/ Al_2O_3/ nitride/ oxide/ silicon (TANOS) have demonstrated high P/E speed and have attracted much attention for applying in the future NVM [9-10]. Unfortunately, all SONOS-type memories exhibit erase saturation phenomenon [11] and unwanted migration of stored charges in the nitride layer [12]. Some storage electrons still leak to control gate or channel if they are trapped at the shallow levels in the silicon nitride layer. Hence, nanocrystal memories which use various materials as the storage node such as Si, Ge, HfO_2, Pt, Ag, Au, Ni and TiN have been proposed and have become another possible solution for the future NVM applications [13-26]. Nanocrystal memories may have better charge storage ability than SONOS-type memory since each nanocrystal is theoretically isolated by the

surrounding dielectric. Therefore, a thinner tunneling oxide can be used to improve P/E speed and reduced P/E operation voltage without degrading retention performance. In addition, metal nanocrystals have better work function engineering ability and higher density of state around the Fermi level than semiconductor nanocrystals [17-24]. However, nanocrystal memories still have some challenges, such as how to formation nanocrystals with high density, constant size and uniform distribution [23-26].

Recently, multi-gate field effect transistors (MuGFETs) were predicted as one of the most potential solution for the NAND Flash beyond 22 nm node, and various SONOS-type and nanocrystal memories have been fabricated with multi-gate structure [2]. It has been reported that the multi-gate memory cell can achieve excellent short channel effect controllability, higher driving current, lower leakage current, better gate coupling ratio, better programming inhibition, and more numbers of nanocrystals in one cell [3-6, 13, 19]. Furthermore, the potential of floating fin-type body is modulated in the multi-gate structure which is different than that in the single gate structure and exhibits longer charge retention time [13, 30]. Moreover, TiN nanocrystal memories with a high density of TiN nanocrystals can be formed in the surrounding Al_2O_3 dielectric and these memories can exhibit larger hysteresis memory window which has potential to be used in the multilevel operation [21, 23]. In this chapter, n-channel multi-gate metal nanocrystal memory using TiN nanocrystals, an Al_2O_3 high-k blocking dielectric layer, and a P^+ poly-Si gate electrode was fabricated on a silicon-on-insulator (SOI) wafer. The work function of TiN is extracted around 4.6 eV [21, 27]; it is expected to provide a level 0.6 eV deeper than that of Si nanocrystal to improve the retention performance. The high-k dielectric, Al_2O_3, has an energy bandgap similar to SiO_2 but has higher gate to

channel coupling efficiency. Therefore, using Al_2O_3 as blocking dielectric layer can lower P/E operation voltage. In addition, using high work function gate electrode can enhance the erase characteristic by suppressing the unwanted back-side injection effect [6]. Moreover, the nanocrystal size effects on memory window, P/E speed, and retention property would also been discussed.

4.2 Devices Fabrication

Figure 4-1 shows the main process flow of the n-channel multi-gate TiN nanocrystal memory cell. The starting material is a 6 inches separation-by-implanted-oxygen (SIMOX) SOI wafer with 40-nm-thick SOI layer and a 150-nm-thick buried oxide layer. The SOI layer is lightly boron-doped and the doping concentration is around $1x10^{15}$ cm^{-3}. The Si fins in the <110> direction were patterned by e-beam lithography and plasma dry etching. Next, a very thin 3.6-nm-thick tunneling oxide layer was thermally grown using a furnace system at 800 °C. Then, in order to provide a material for forming nanocrystals and its surrounding material, a TiN wetting layer with thickness equals to 0.5 or 0.7 nm and an Al_2O_3 layer with thickness equals to 1 nm were sequentially deposited with seven periods in a plasma enhanced atomic layer deposition/ atomic layer deposition (PEALD/ALD) clustered system and a 15- or 20-nm-thick Al_2O_3 layer was deposited consecutively as the blocking dielectric layer in the same ALD system followed by a 150-nm-thick amorphous Si deposition at 545 °C as the gate electrode. The TiN layers were deposited with $TiCl_4$ as a precursor at 350 °C in N_2/H_2 gas ambient and the Al_2O_3 layers were deposited with trimethylamine (TMA) and H_2O as precursors at 300 °C. Next, post deposition annealing (PDA) was performed at 900 °C for 10 sec or 40 sec in nitrogen gas

ambient to provide sufficient surface mobility to transform the TiN wetting layer into nanocrystals [17-18].

In order to estimate the effect of charge trapping layer engineering, a set of devices with various TiN wetting layer thicknesses, blocking dielectric thicknesses, and PDA times were fabricated. The sample ID and process parameters are listed in Table 4-1. The TiN wetting layer thickness of sample A (0.7 nm) is thicker than that of the other samples (0.5 nm). Sample B has the longest PDA time (40 sec) among all the samples. Moreover, sample D has the thinnest blocking dielectric thickness (15 nm). The poly-Si gate was doped by BF_2^+ ion implantation at 40 keV to a dose of $5x10^{15}$ cm^{-3} followed by activation at 900 °C for 20 sec in nitrogen gas ambient. Before gate definition by e-beam lithography and dry etching, a thick TEOS oxide layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 695 °C as a hard mask to avoid the anti-doping of poly-Si gate during the n^+ source/drain (S/D) dopants implantation. The device structure in this process step is shown in Fig. 4-1(a).

Next, a SiO_x (10 nm)/SiN_x (40 nm) stack layers were deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C and dry-etched to form a composite spacer as shown in Fig. 4-1(b). Then, P_{31}^+ ions were implanted in S/D areas at 20 keV to a dose of $5x10^{15}$ cm^{-3} and rapid thermal annealing (RTA) at 900 °C for 20 sec was performed to activate the S/D dopants. Then, a TEOS hard mask and a native oxide were selectively etched using HF solution and a 25-nm-thick Ni layer was deposited by e-gun evaporation followed by a two-step self-aligned Ni-silicide process to obtained better controllability of Ni silicide lateral formation. The first silicidation step was vacuum annealing at 300 °C for 45 min and the Ni silicide was formed in the Ni_2Si phase. After removing the unreacted Ni film by H_2SO_4:H_2O_2 (3:1)

solution at 75 °C, the second silicidation step was performed at 600 °C for 30 sec to transform the $NiSi_2$ phase to the NiSi phase. The S/D region was converted into a full NiSi structure, as shown in Fig.4-1(c). The gate electrode became a polycide structure after the silicidation.

All the measured cells have the same device dimensions with gate length equals to 80 nm and fin width equals to 50 nm, as shown in Fig. 4-2. The cross-sectional transmission electron microscopy (TEM) images of the fabricated tri-gate nanocrystal memory (sample B) with a gate length of 80 nm and a fin width of 50 nm are shown in the Figs. 4-2(a) and (b), respectively. Moreover, Ni silicides are formed in the S/D region and the top of the gate electrode. Figure 4-3(a) and (b) show high resolution TEM images of samples A and B to magnify the charge trapping layer. The tunneling oxide thickness is around 3.6 nm and TiN nanocrystals embedded in Al_2O_3 are observed. Note that the diameter of TiN nanocrystal in sample A is around 3 nm, which is larger than that in sample B of about 1-2 nm because sample A has a thicker TiN wetting layer which provides more source material to form larger TiN nanocrystals than that of sample B. In the next section, we will show that nanocrystal size has a marked effect on memory performance as previously reported in literature [20, 28].

4.3 Results and Discussion

4.3.1 Program/Erase Efficiency and Memory Window

Figure 4-4 shows the transfer characteristics of sample A with various programming/erasing (P/E) biases for 0.1 sec. For the fresh device, the threshold

voltage (V_{TH}) is 1 V, the subthreshold swing is about 100 mV/decade, the driving current capability is 236 μA/μm at $|V_{GS}-V_{TH}|=V_{DS}=1$ V, and on/off current ratio is larger than 10^7. Moreover, sample A exhibits an impressive memory window as large as 5.2 V after P/E at ±10 V for 0.1 sec and it also presents symmetry threshold voltage shift with increasing bias condition, indicating that this sample has the potential of multilevel operation by choosing P/E bias carefully.

Figure 4-5(a) and (b) shows the programming and erasing speeds of samples A-D with the same pulse bias at ±10 V and different pulse widths. All the devices utilized Fowler-Nordheim (FN) tunneling for P/E operations and both source and drain terminals were grounded during the biasing pulse. After operation at positive pulse bias, the V_{TH} were shifted toward positive V_G direction and this V_{TH} was defined as the V_{TH} of program state. Therefore, prior to the erase pulse bias conditions, the initial V_{TH} is the V_{TH} after operation at 10 V for 0.1 sec for samples A-D. In either the programming properties shown in Fig. 4-5(a) or the erasing properties shown in Fig. 4-5(b), sample A has the largest V_{TH} shift at the same P/E time. It is because sample A utilized a thicker TiN wetting layer (0.7 nm) than the other samples (0.5 nm), inducing the larger TiN nanocrystals were formed, as shown in Fig. 4-3, and enhancing the storage capability. Moreover, this enhancement confirms that charges are clearly stored in the TiN nanocrystals but not in Al_2O_3 dielectric. As device dimension continually shrinks, small nanocrystals provide more trapping sites and this is beneficial for three-dimensional integration. However, some reports proposed that the diameter of nanocrystals has a marked effect on the programming and retention characteristics and the optimal nanocrystal diameter is around 5 nm [20, 28]. In our samples, the nanocrystal size of samples A (~3 nm) and B (1-2 nm) are rather smaller than the proposed nanocrystal size, that pronounced critical quantum confinement and

coulomb blockade effects occur to degrade the charge trapping efficiency, which may decrease the program speed.

Figure 4-6 shows the memory windows of samples A-D after various P/E biases for 0.1 sec. As aforementioned, sample A has the largest memory window under all biases among the other samples owing to the large nanocrystal size. On the other hand, because sample B has the longest PDA time (40 sec), a slightly larger memory window is obtained in sample B than in samples C-D. This implies that a moderately longer annealing time helps the formation of TiN nanocrystals. However, total TiN mass has much more significant effects on TiN nanocrystal size. Moreover, the device with a thinner blocking dielectric of 15 nm thickness (sample D) has almost the same memory window as the device with thicker blocking dielectric of 20 nm thickness (sample C), which indicates that the back-side electron injection is quite negligible under these FN bias conditions.

Furthermore, the memory windows of samples B-D increased monotonically with increasing FN bias. However, the memory window of sample A increases to its largest value at ±10 V and then turns down as P/E bias increases further. The degradation of the memory window in the strong P/E electrical field is usually attributed to the back-side electron injection effect. Figure 4-7(a) and (b) shows the programming and erasing speeds of sample A under various bias conditions. The V_{TH} values in the both programmed and erased states were affected at a high P/E voltage. Because of the larger hole/electron injection rate from the gate electrode to nanocrystals during higher P/E bias operations, these injected carriers from the gate would recombine with the electrons/holes injected from the Si channel [29]. Therefore, smaller V_{TH} shifts or the so-called saturation phenomenon of the V_{TH} shift is observed in both the program and erase states at P/E biases higher than ±10 V for larger pulse

width. In Fig. 4-7(a) and (b), the V_{TH} shift increases with increasing of pulse bias when the pulse width is shorter than 0.1 sec. However, as the pulse width increases to 1 sec, the V_{TH} shift decreases in both the programmed and erased states with increasing FN bias and the maximum memory window is obtained at the cell P/E at ±8 V. This phenomenon indicates again that as the amount of stored carriers increases to a certain value in the nanocrystals, the degradation of the memory window occurs. Hence, memory window degradation should also occur in samples B-D after a much larger P/E bias or pulse width is achieved.

4.3.2 Retention Performance

Figure 4-8 show the retention characteristics of samples A and B at temperatures equal to 25 °C and 85 °C. In order to compare charge loss rate, sample A, which was programmed and erased at ±10 V for 0.01 s to reach a similar programmed state and the erased state of sample B, which has the maximum memory window, was programmed and erased at ±12 V for 0.1 s. In this case, the memory window for both samples is about 1.95 V, which is close to the maximum memory window of sample B. It is observed that sample A has a lower charge loss rate than sample B either at temperatures equal to 25 °C and 85 °C because the nanocrystal size of sample A (~3 nm) is larger than that of sample B (~1-2 nm). The 3 nm nanocrystal is still too small to be affected by the Coulomb repulsive force and quantum confinement effect. The Coulomb repulsive force would discharge trapped carriers more quickly in the nanocrystals and increase the charge loss rate [28]. Moreover, the quantum confinement effect in nanocrystals would split the energy level and raise trap energy so that stored charges can escape more easily. At a similar initial memory window of around 2 V, charges stored in the nanocrystals of sample A have not reach its

saturation status and thus more carriers can be stored in sample A with a lower Coulomb repulsive force and a smaller quantum confinement effect. On the other hand, there exist stronger Coulomb repulsive force and quantum confinement effect for degrading the retention performance more critically in sample B. At room temperature, only a 6 % charge loss after 10^4 sec in sample A and an 18 % charge loss after 10^4 sec in sample B were observed. Moreover, a mere 12 % charge loss up to 10 years in sample A at room temperature was observed. Both the charge losses of samples A and B are more serious at higher temperature than at room temperature owing to the more energetic trapped carriers can escape easily from TiN nanocrystals.

In order to compare the retention performance of samples A and B at the maximum initial memory window, the retention property of sample A with a full memory window is also measured. The initial memory window is around 5 V and has a 21% charge loss after 10^4 s, which is about the same charge loss in sample B, indicating that although the quantum confinement effect is one of reasons for the enhancement of charge loss, Coulomb repulsive force is the main reason for the degradation of the retention performance at various initial memory windows in the TiN metal nanocrystals with diameters in the 1-3 nm range. However, the quantum confinement effect has an important role in the retention performance of semiconductor nanocrystal memories [28]. Moreover, although a very thin 3.6-nm-thick tunneling oxide layer was utilized in both samples, the acceptable retention performance can still be obtained. This confirms again that by using the small nanocrystal to replace the FG as the storage node can help to shrink the thickness of tunneling oxide and reduce the P/E bias voltage. In addition, the multi-gate structure can also help to enhance the retention performance since the multi-gate structure can

fully depletes the channel and the lifted channel potential reduces the electric field and the retention performance is improved by suppressing the trap-assisted leakage [30].

4.3.3 Retention Performance in Different P/E Conditions

For our TiN nanocrystal memory, since holes inject into the nanocrystals to compensate the stored electrons while erase state, the threshold voltage can shift negatively more than the fresh threshold voltage and no erase saturation phenomenon would exhibit. Hence, the retention performance is largely affect by the selected initial P/E states. The influence of the P/E conditions on the retention performance are presented in Fig. 4-9, which shows the retention properties of sample C with similar initial memory window but two different P/E conditions were chosen. One condition is operated with moderate P/E biases, as shown in red triangular. By applying the fresh V_{TH} as a reference, good symmetry of the V_{TH} shift in the programmed state and erased state are obtained. Another condition is operated with moderate programming bias but larger erasing bias, as shown in black squares. Because the stronger erasing field was supplied, smaller V_{TH} in both P/E states are observed. After 10^3 sec, although both conditions have similar initial memory window, the condition with stronger erasing bias has a higher charge loss of about 38 % than the condition with moderate erasing bias (20 %). It can be easily explained by the energy band diagram between the nanocrystal and Si body, as shown in Fig. 4-10. Device with stronger erasing bias would store more holes that induce higher electric field between nanocrystals and Si body. Thus, holes have higher probability to tunnel to the Si body and hence worse retention performance is obtained. Therefore, to obtain better retention performance, the suitable initial P/E states have to be selected carefully.

4.3.4 Endurance and Disturbance Performance

Figure 4-11 shows the endurance characteristics of samples A and B with P/E at ± 8 V, 0.1 sec and P/E at ± 12 V, 0.1 sec, respectively. Because the FN tunneling mechanism was used for P/E operations, the injected electrons and holes have a uniform distribution. The distribution mismatch is negligible and neither electrons nor holes would be hard to erase after the P/E cycles [9, 31-32]. Therefore, an invisible shift in the programmed and erased states can be observed and the memory window is kept at about 93% for sample A and at 97% for sample B after 10^4 P/E cycles. Good endurance performance can also be observed. Figure 4-11(a) and (b) shows the transfer characteristics of sample A and B after the first and 10^4 P/E cycle operations. In Fig. 4-11(a), a small deterioration of the subthreshold swing and driving current after 10^4 P/E cycles means that a small amount of interface state was generated during the P/E cycles. For the multi-gate device structure, charges stored in each nanocrystal may not be identical. For example, for the nanocrystals located near the top corner of the active layer, more charges can be injected owing to a stronger electric field. This phenomenon may also result in the deterioration of the subthreshold swing. In Fig. 4-11(b), no apparent degradation after 10^4 P/E cycles can be observed.

Gate disturbance occurs when the neighboring cells, which share the same word line, are biased by programming or erasing pulses. Therefore, the gate disturbance characteristics of sample A under four situations for 10^3 sec are shown in Fig. 4-12. It can be observed that after stressing at V_G= ±10 V for 10^3 sec, the device in the erase state has a negligible V_{TH} shift, which is due to the decreased electric field in the multi-gate structure on the SOI wafer. In the multi-gate structure, the body, source and drain terminal potentials are all floating. Therefore, we suspect that the electric field between the trapping nodes and the Si body is reduced to suppress unwanted

carrier migration or charge loss. However, after V_G= ±10 V for 10^3 s stressing in the programmed state, the device with an erased bias has a more pronounced V_{TH} shift than that with a programmed bias because the repulsive force and the floating body can block the extra injected electrons in the programmed state but some stored electrons are de-trapped by higher negative erased voltage. Note these disturbance properties both saturate after 10-20 sec and are not critical issue. Figure 4-13 shows the read disturbance of sample A in the erase state for 10^3 sec stressing bias. A very small variation can be observed, indicating insignificant carrier migrations, injection or de-trapping during read operations.

4.4 Conclusions

As the NAND technology continually scales down, the combination of discrete traps storage and MuGFETs structure is one of the most potential candidates for the future application. In this chapter, we successfully combine multi-gate as the non-planar cell structure and the metal nanocrystal as the storage node together. An n-channel tri-gate metal nanocrystal memory using TiN nanocrystals, a high-k blocking dielectric layer and a p^+ poly-Si gate was fabricated. The effects of charge trapping layer thickness and post deposition annealing time have been investigated. It is observed that the memory window is determined by the size of nanocrystals. Although a longer annealing time could help the growth of TiN nanocrystals and slightly enhance the memory window, an adequate mass of the source material is the key factor for forming larger TiN nanocrystals and obtaining larger memory window. The device with thicker TiN nano-laminates (0.7 nm) has much larger memory window, 5.2 V than the devices with thinner TiN nano-laminates (0.5 nm). Moreover,

phenomenon of the turn-down memory window as FN bias increases is observed and explained by the back-side injection effect.

In addition, the charge loss rates of samples with different nanocrystal sizes are similar when the devices are programmed and erased at the maximum initial memory window. Retention performance was mainly affected by the coulomb repulsive force but not by the quantum confinement effect. This observation implies that the quantum confinement effect in the metal nanocrystal is not as critical as that in the semiconductor nanocrystal. Furthermore, in these TiN nanocrystal memories, holes can inject into nanocrystals to shift the threshold voltage more negative than fresh threshold voltage during erase operation. Hence, by selecting the suitable initial P/E states, better retention performance would achieve. Finally, the FN tunneling mechanism has a uniform injection profile to avoid unwanted charge migration, and the multi-gate structure on an SOI wafer with a floating body can reduce inner electric field to suppress trapped charge migration. Therefore, good endurance and disturbance performance can be obtained in these nano scale multi-gate nanocrystal memories.

References

[1] D. Kahng and S. M Sze, "A floating gate and its application to memory devices," *IEEE Trans. Electron Devices,* vol. 14, no. 9, p. 629, 1967.

[2] Process Integration, Devices and Structures in International Technology Roadmap for Semiconductors 2009 edition, pp. 13-20, 2009.

[3] M. Specht, U. Dorda, L. Dreeskornfeld, J. Kretz, F. Hofmann, M. Städele, R. J. Luyken, W. Rösner, H. Reisinger, E. Landgraf, T. Schulz, J. Hartwich, R. Kömmling, and L. Risch, "20 nm tri-gate SONOS memory cells with multi-level operation," in *IEDM Tech. Dig.*, 2004, pp. 1083-1085.

[4] P. Xuan, M. She, B. Harteneck, A. Liddle, J. Bokor, and T.-J. King, "FinFET SONOS Flash Memory for Embedded Applications," in *IEDM Tech. Dig.*, 2003, pp. 609-612.

[5] F. Hofmann, M. Specht, U. Dorda, R. Kömmling, L. Dreskorndeld, J. Kretz, M. Städele, W. Rösner, and L. Risch, "NVM based on FinFET device structures," *Solid-State Electron.,* vol. 49, no. 11, pp. 1799-1804, 2005.

[6] C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, "A Novel SONOS Structure of $SiO_2/SiN/Al_2O_3$ with TaN Metal Gate for Multi-giga Bit Flash Memories," in *IEDM Tech. Dig.*, 2003, pp. 613-617.

[7] M. H. White, D. A. Adams, and J. Bu, "On the Go with SONOS", *IEEE Circuits and Devices*, vol. 16, no. 4, pp. 22-31, 2000.

[8] J. Bu, and M. H. White, "Effects of Two-step High Temperature Deuterium Anneals on SONOS Non-volatile Memory Devices," *IEEE Electron Device Lett.,* vol. 22, no. 1, pp. 17-19, 2001.

[9] H. T. Luo, S. Y. Wang, E. K. Lai, Y. H. Shih, S. C. Lai, L. W. Yang, K. C. Chen,

J. Ku, K. Y. Hsieh, R. Liu, and C. Y. Lu, "BE-SONOS: A Bandgap Engineered SONOS with Excellent Performance and Reliability," in *IEDM Tech. Dig.*, 2005, pp. 547-550.

[10] C.-H. Lee, J. Choi, C. Kang, Y. Shin, J.-S. Lee, J. Sel, J. Sim, S. Jeon, B.-I. Choe, D. Bae, K. Park, and K. Kim, "Multi-Level NAND Flash Memory with 63 nm-node TANOS (Si-Oxide-SiN-Al2O3-TaN) Cell Structure," in *VLSI Symp. Tech. Dig.*, 2006, pp. 21-22.

[11] Gowrishankar L. Chindalore*, Member, IEEE*, Craig T. Swift, and David Burnett*, Member, IEEE,* "A New Combination–Erase Technique for Erasing Nitride Based (SONOS) Nonvolatile Memories," *IEEE Electron Device Lett.,* vol. 24, no. 4, pp. 257-259, 2003.

[12] T. Sugizaki, M. Kohayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka, "Novel Multi-bit SONOS Type Flash Memory Using a Highk Charge Trapping Layer," in *VLSI Symp. Tech. Dig.*, 2003, pp. 27-28.

[13] K. Yanagidaira, M. Saitoh, and T. Hiramoto, "Enhancement of Charge Storage Performance in Double-Gate Silicon Nanocrystal Memories with Ultray thin Body Structure," *IEEE Electron Devices Lett.*, vol. 26, no. 7, pp. 473-475, 2005.

[14] T. Osabe, T. Ishii, T. Mine, T. Sano, T. Arigane, T. Fukumura, H. Kurata, S. Saeki, Y. Ikeda, and K. Yano, "Charge-injection Length in silicon nanocrystal memory cells," in *VLSI Symp. Tech. Dig.*, 2004, pp. 242-243.

[15] M. L. Ostraat, J. W. De Blauwe, M. L. Green, L. D. Bell, M. L. Brongersma, J. Casperson, R. C. Flagan, and H. A. Atwater, "Synthesis and characterization of aerosol silicon nanocrystal nonvolatile floating-gate memory devices," *App;. Phys. Lett.,* vol. 79, no. 3, pp. 433-435, 2001.

[16] Y. H. Lin, C.H. Chien, C.T. Lin, C. Y. Chang, and T. F. Lei, "Novel two-bit HfO_2 nanocrystal nonvolatile flash memory," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 782-789, 2006.

[17] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal Nanocrystal Memories- Part I: Device Design and Fabrication," *IEEE Trans. Electron Devices*, vol. 49, no.9, pp. 1606-1613, 2002.

[18] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal Nanocrystal Memories—Part II: electrical characteristics," *IEEE Trans. Electron Devices,* vol. 49, no. 9, pp. 1614-1622, 2002.

[19] Y. J. Ahn, J. -D. Choe, J. J. Lee, D. Choi, E. S. Cho, B. Y. Choi, S. -H. Lee, S. K. Sung, C. -H. Lee, S. H. Cheong, D. K. Lee, S. B. Kim, D. Park and B. I. Ryu, "Trap Layer Engineered FinFET NAND Flash with Enhanced Memory Window," in *VLSI Symp. Tech. Dig.*, 2006, pp. 88-89.

[20] T.-H. Hou, C. Lee, V. Narayanan, U. Ganguly, and E. C. Kan, "Design Optimization of Metal Nanocrystal Memory- Part I: Nanocrystal Array Engineering," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 3095-3102, 2006.

[21] S. Maikap, P. J. Tzeng, H. Y. Lee, C. C. Wang, T. C. Tien, L. S. Lee, and M. -J. Tsai, "Physical and Electrical Characteristics of Atomic Layer Deposited TiN Nanocrystal Memory Capacitors," *Appl. Phys. Lett.*, vol. 91, no. 4, p. 043114, 2007.

[22] J. J. Lee, and D. -L. Kwong, "Metal Nanocrystal Memory With High-k Tunneling Barrier for Improved Data Retention," *IEEE Trans. Electron Devices,* vol. 52, no. 4, pp. 507-511, 2005.

[23] S. Choi, S. S. Kim, M. Chang, H. Hwang, S. Jeon, C Kim, "Highly thermally

stable TiN nanocrystals as charge trapping sites for nonvolatile memory device applications," *Appl. Phys. Lett.,* vol. 86, no. 12, p. 123110, 2005.

[24] C. P. Lu, C. K. Luo, B. Y. Tsui, C. H. Lin P. J. Tzeng, C. C. Wang, H. Y. Lee, D. Y. Wu, and M. -J. Tsai "High Endurance Multi-gate TiN Nanocrystal Memory Devices with High-k Blocking Dielectric and High Work Function Gate Electrode," in *VLSI Symp. Tech. Dig.*, 2007, pp. 62-63.

[25] A. K. Dutta, "Visible photoluminescence from Ge nanocrystal embedded into a SiO_2 matrix fabricated by atmospheric pressure chemical vapor deposition," *Appl. Phys. Lett.*, vol. 68, no. 9, pp.1189-1191, 2007.

[26] Y. Liu, T. P. Chen, C. Y. Ng, L. Ding, M. S. Tse, S. Fung, and A. A. Tseng, "Influence of Si-Nanocrystal Distribution in the Oxide on the Charging Behavior of MOS Structures," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 914-917, 2006.

[27] A. Yagishita, T. Saito, K. Nakajima, S. Inumiya, K. Matsuo, T. Shibata, Y. Tsunashima, K. Suguro, and T. Arikado, "Improvement of threshold voltage deviation in damascene metal gate transistors," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1604-1611, 2001.

[28] M. She, and T.-J. King, "Impact of Crystal Size and Tunnel Dielectric on Semiconductor Nanocrystal Memory Performance," *IEEE Trans. Electron Devices,* vol. 50, no. 9, pp. 1934-1940, 2003.

[29] R. van Schaijk, M. van Duuren, P. Goarin, W. Y. Mei, and K. van der Jeugd, "Reliability of embedded SONOS memories," in *Euro. Solid-State Devi. Res. Conf.,* 2004, pp. 277-280.

[30] S.-K. Sung, S.-H. Lee, B. Y. Choi, J. J. Lee, J.-D. Choe, E. S. Cho, Y. J. Ahn, D. Choi, C.-H. Lee, D. H. Kim, Y.-S. Lee, S. B. Kim, D. Park, and B.-I. Ryu,

"SONOS-type FinFET Device Using P+ Poly-Si Gate and High-k Blocking Dielectric Integrated on Cell Array and GSL/SSL for Multi-Gigabit NAND Flash Memory," in *VLSI Symp. Tech. Dig.*, 2006, pp. 86-87.

[31] Y. H. Shih, H. T. Lue, K. Y. Hsieh, R Liu, and C. Y. Lu, "A Novel 2-bitkeII Nitride Storage Flash Memory with Greater than 1M PE-cycle Endurance," in *IEDM Tech. Dig.*, 2004, pp. 881-884.

[32] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash memory cells—An overview" *Proc. IEEE*, vol. 85, no.8, pp. 1248–1271, 1997

Table 4-1: Gate stacks conditions of sample A-D.

Sample	Tunneling Layer	Trapping Layer	Blocking Layer	PDA @ 900°C (sec)
	SiO_2 (nm)	TiN/ Al_2O_3 x 7 periods (nm/nm)	Al_2O_3 (nm)	
A	3.6	0.7 /1	20	10
B	3.6	0.5 /1	20	40
C	3.6	0.5 /1	20	10
D	3.6	0.5 /1	15	10

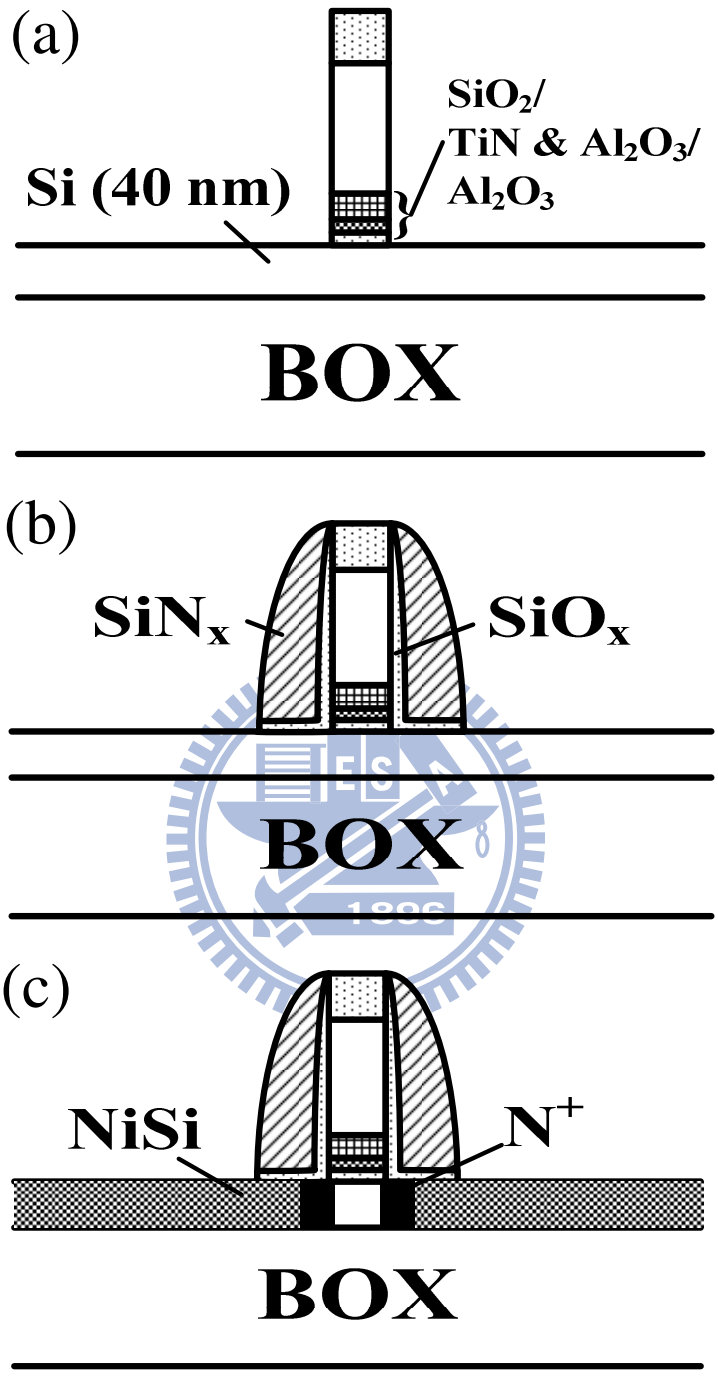


Fig. 4-1 Process flow of n-channel MuGFET TiN nanocrystal NVM on SOI substrate.

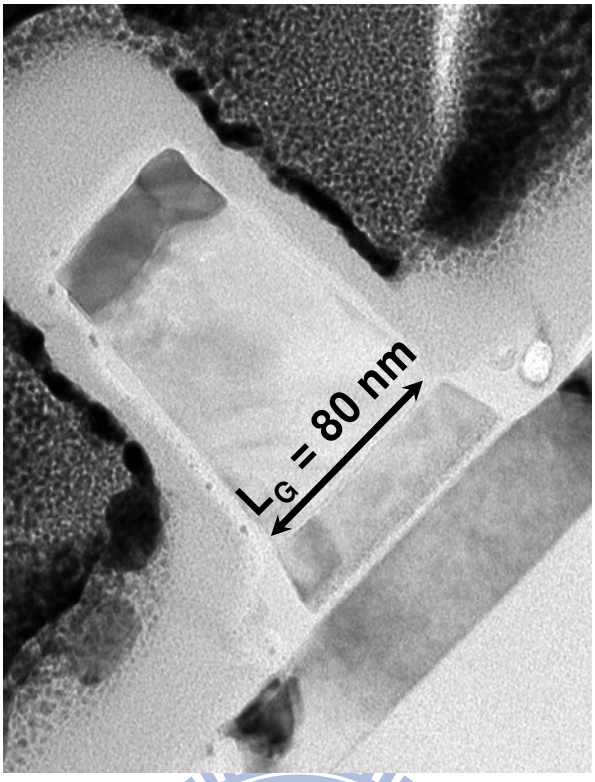


Fig. 4-2(a) High-resolution X-TEM images of the fabricated MuGFET TiN nanocrystal memory with gate length of 80 nm.

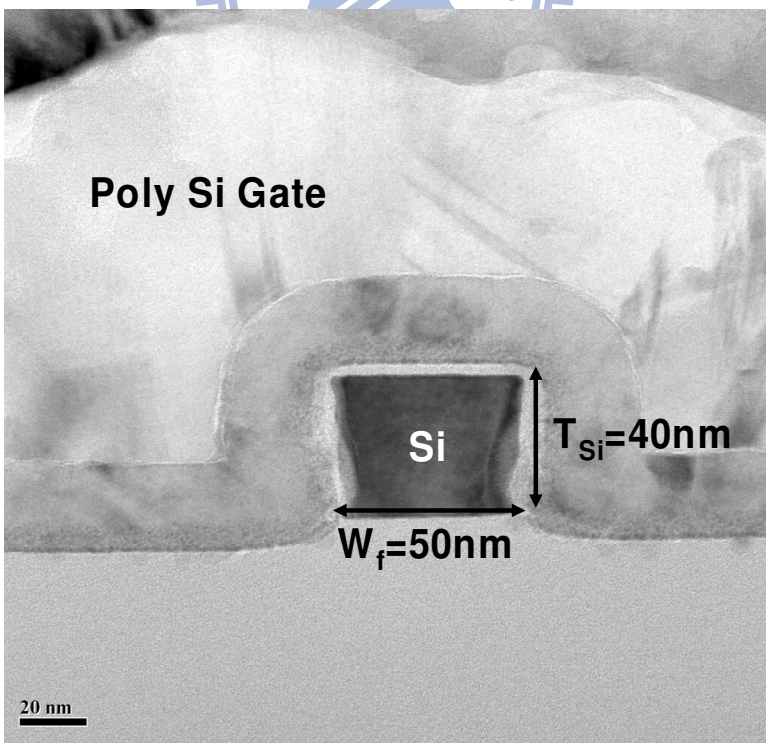


Fig. 4-2(b) High-resolution X-TEM images of the fabricated MuGFET TiN nanocrystal memory with fin width of 50 nm.

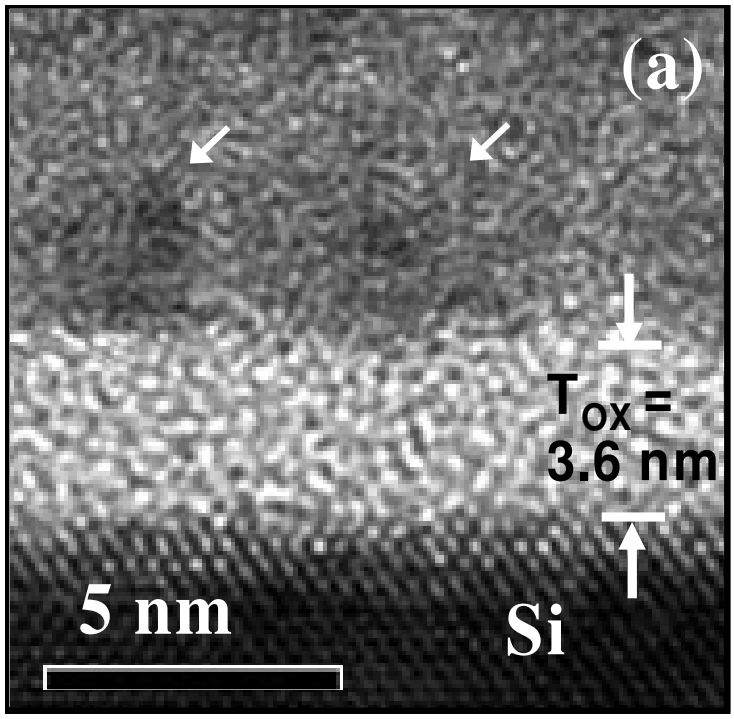


Fig. 4-3(a) High-resolution X-TEM images of sample A. Nanocrystals with diameter around 3 nm were embedded by Al_2O_3.

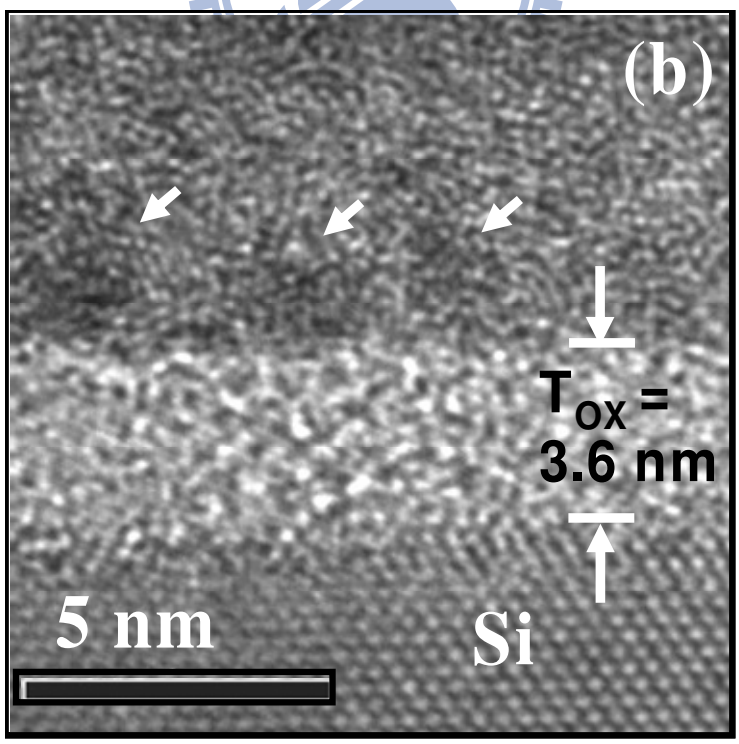


Fig. 4-3(b) High-resolution X-TEM images of sample B. Nanocrystals with diameter around 1-2 nm were embedded by Al_2O_3.

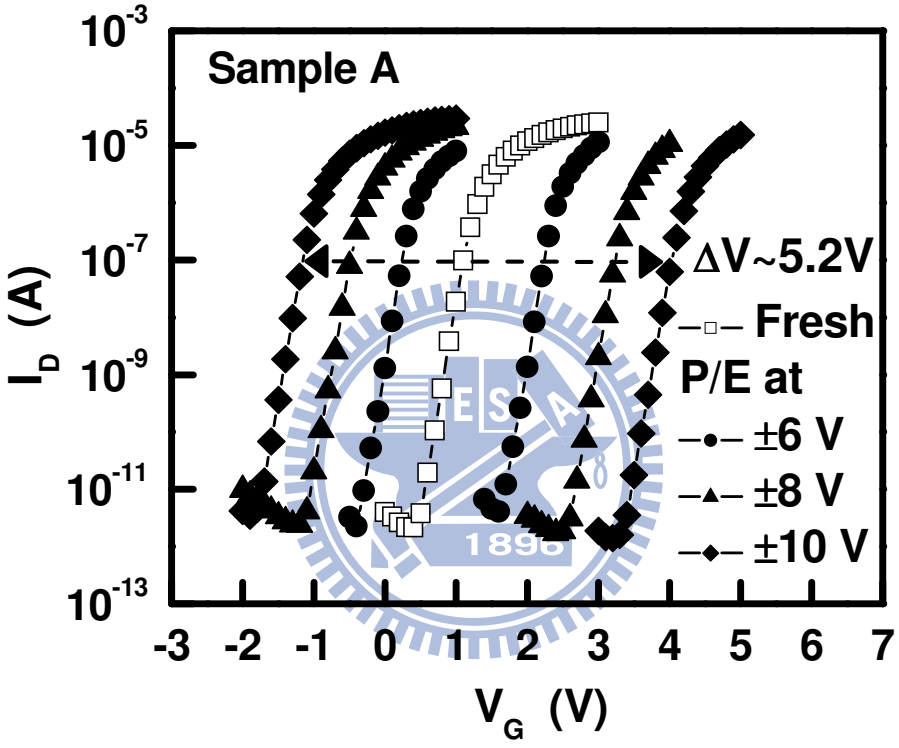


Fig. 4-4 Transfer characteristics of sample A after various P/E bias for 0.1 sec.

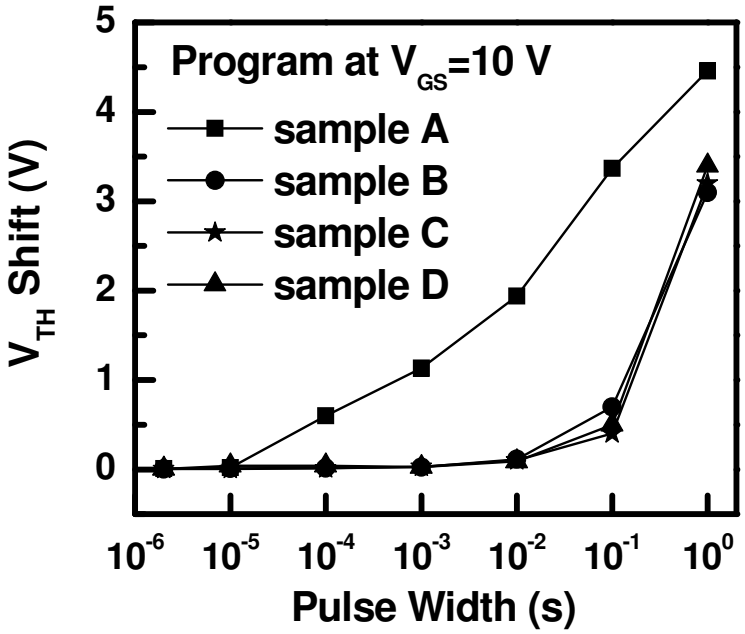


Fig. 4-5(a) Programming speeds of samples A-D with same pulse bias at +10 V and different pulse width.

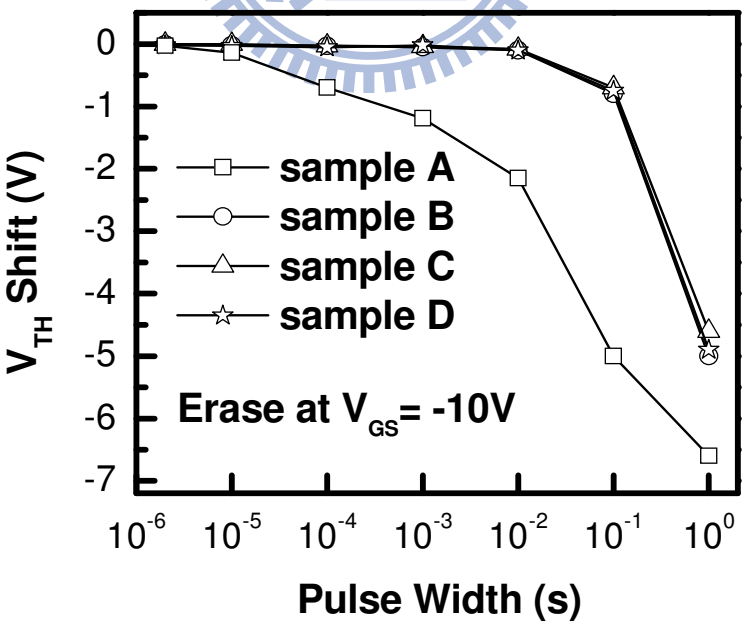


Fig. 4-5(b) Erasing speeds of samples A-D with same pulse bias at -10 V and different pulse width.

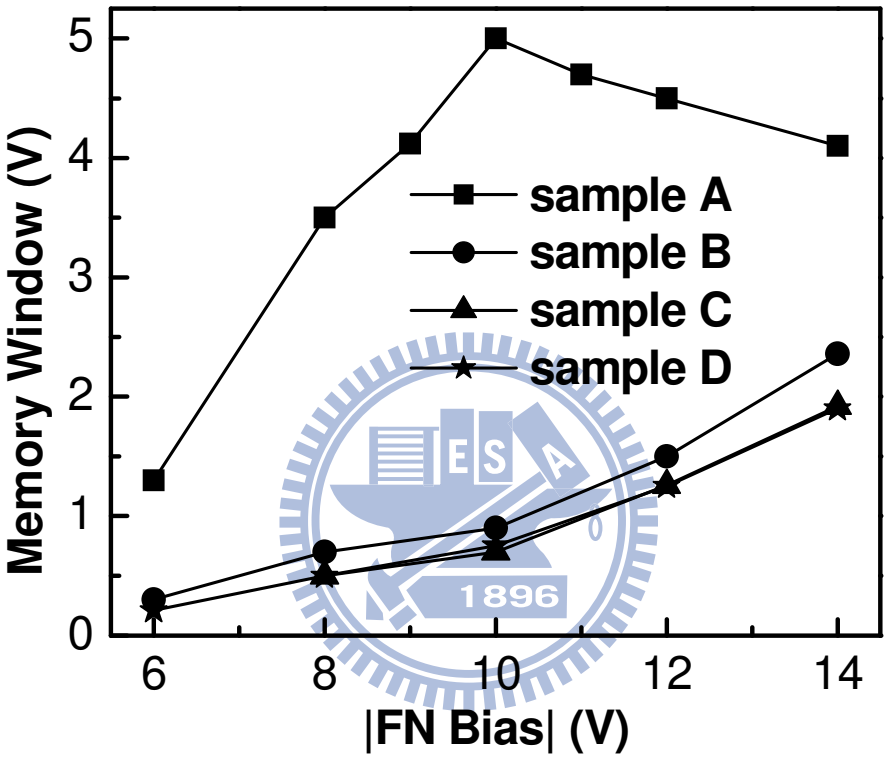


Fig. 4-6 The memory window of sample A-D after various P/E bias for 0.1 sec. The P/E operations utilized Fowler-Nordheim tunneling, and both source and drain terminals were grounded during the biasing pulse.

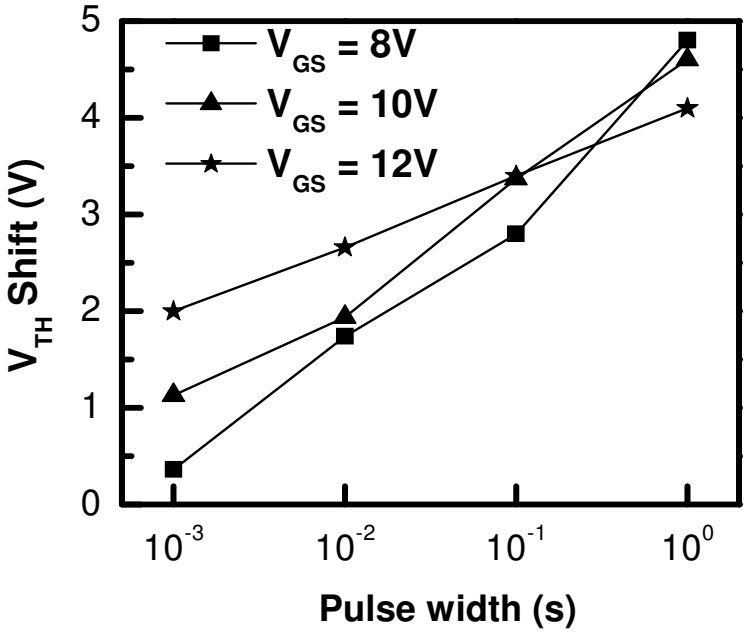


Fig. 4-7(a) Programming speeds of sample A with various pulse biases and pulse widths.

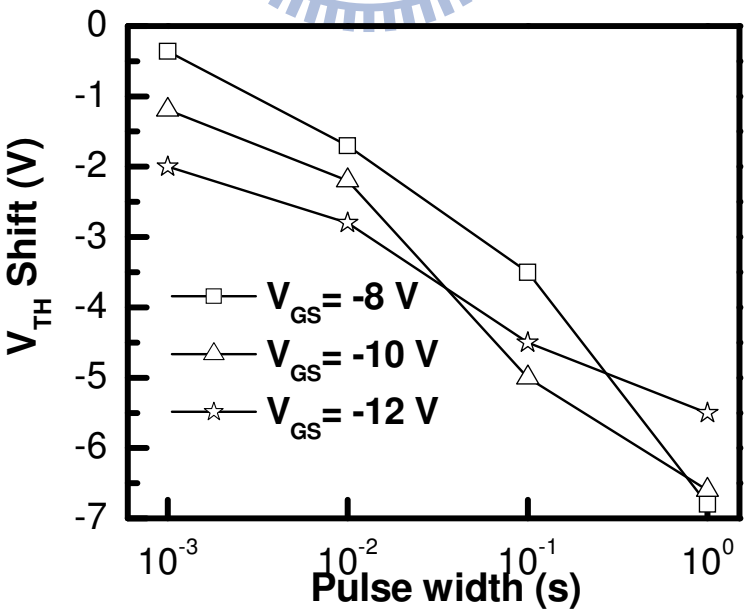


Fig. 4-7(b) Erasing speeds of sample A with various pulse biases and pulse widths.

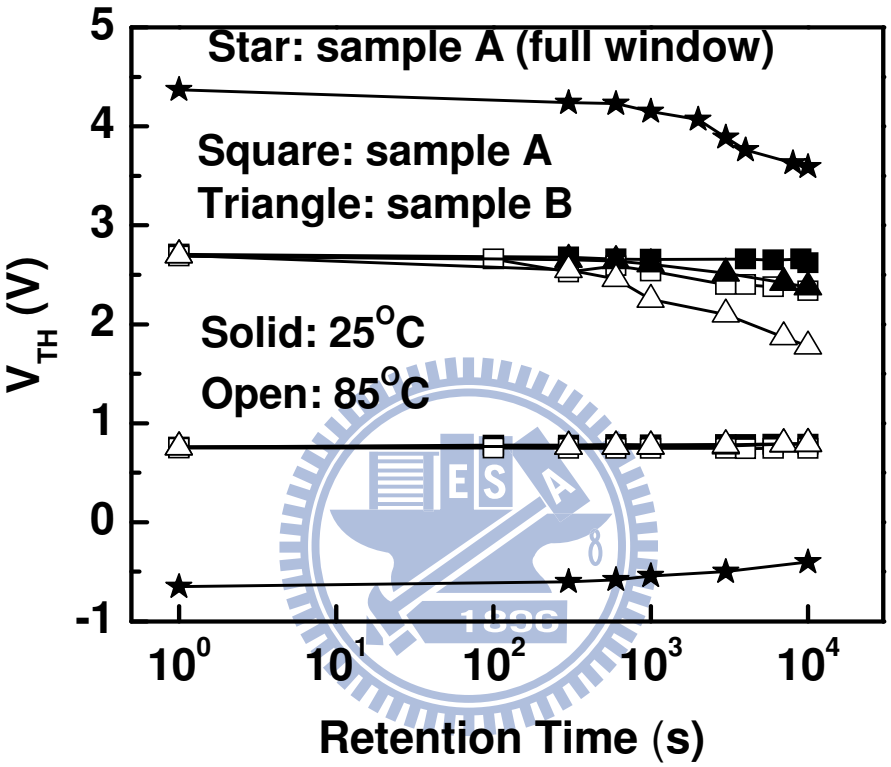


Fig. 4-8 Retention characteristics of trigate TiN nanocrystal memory devices of samples A-B at room temperature (T = *25 °C*) and high temperature (T = *85 °C*).

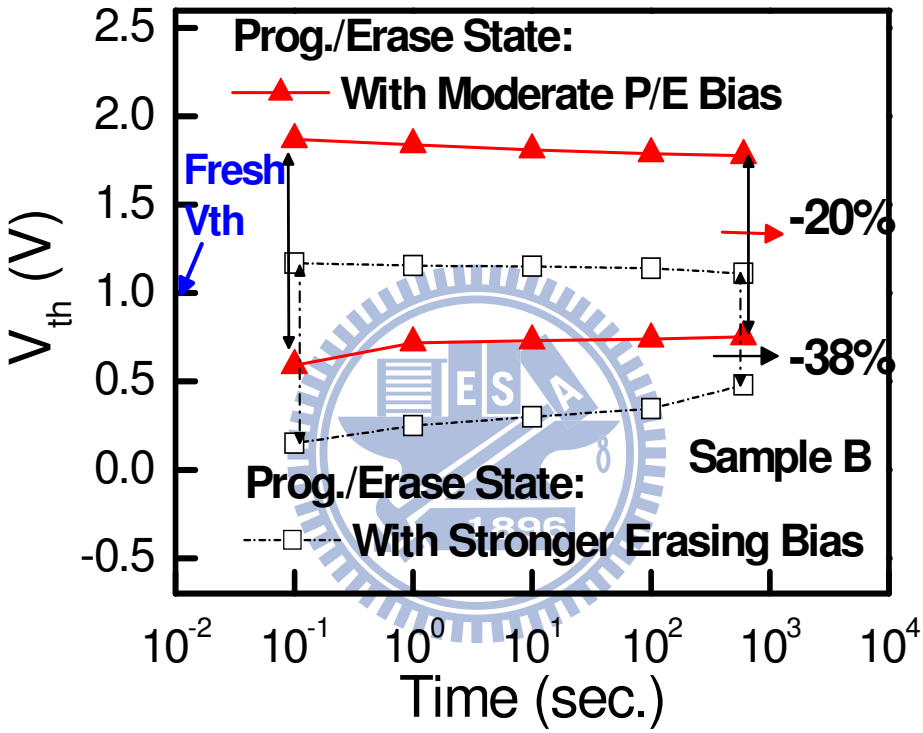


Fig. 4-9 Retention properties of sample C in two different P/E conditions but similar initial memory window.

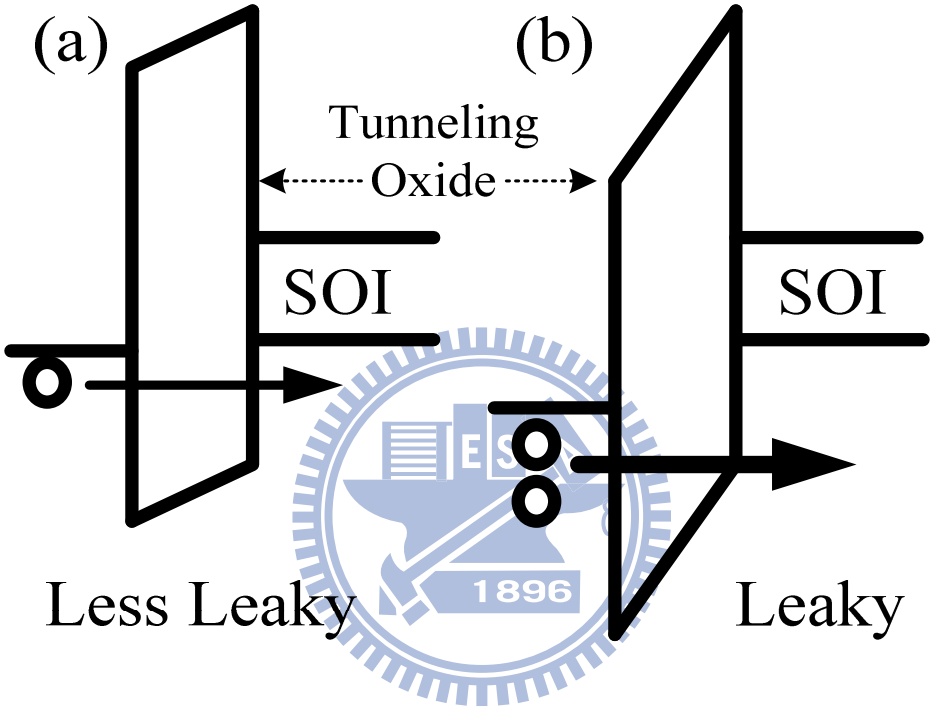


Fig. 4-10 Simple energy band diagrams in the retention condition after (a) moderate erasing bias or (b) stronger erasing bias.

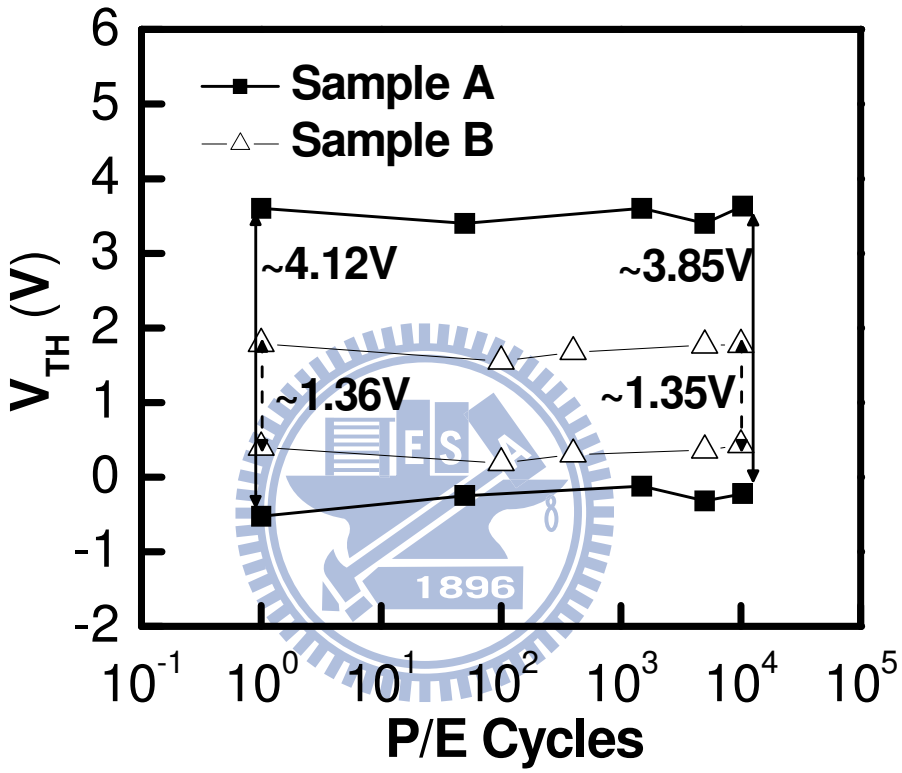


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Fig. 4-11 Endurance characteristics of samples A and B. The P/E bias conditions are ±9 V, 0.1 sec for sample A and ±12 V, 0.1 sec for sample B.

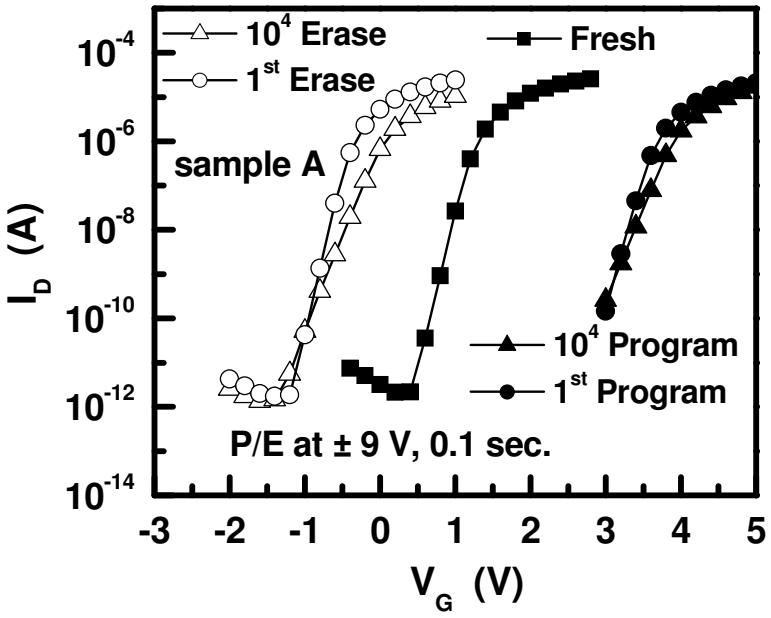

Fig. 4-12(a) Transfer characteristics after the first and the 10^{4th} P/E cycle operations of sample A.

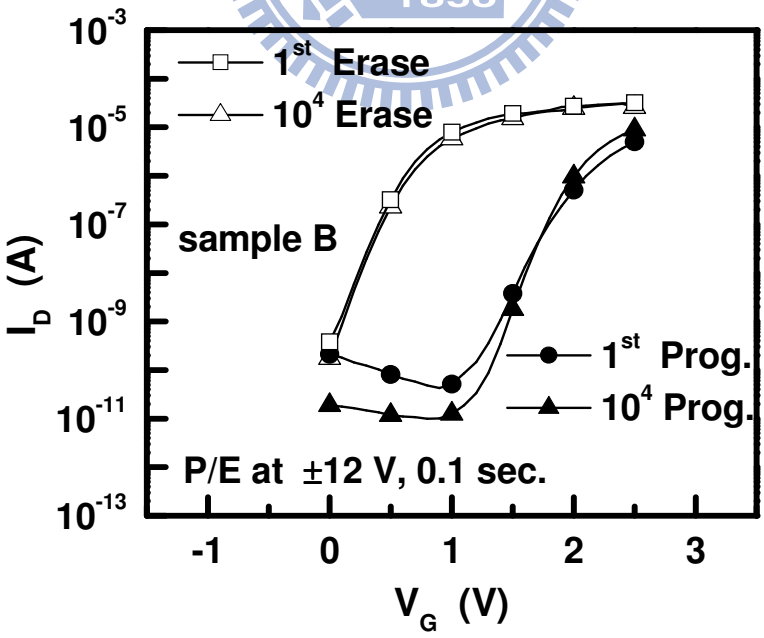

Fig. 4-12(b) Transfer characteristics after the first and the 10^{4th} P/E cycle operations of sample B.

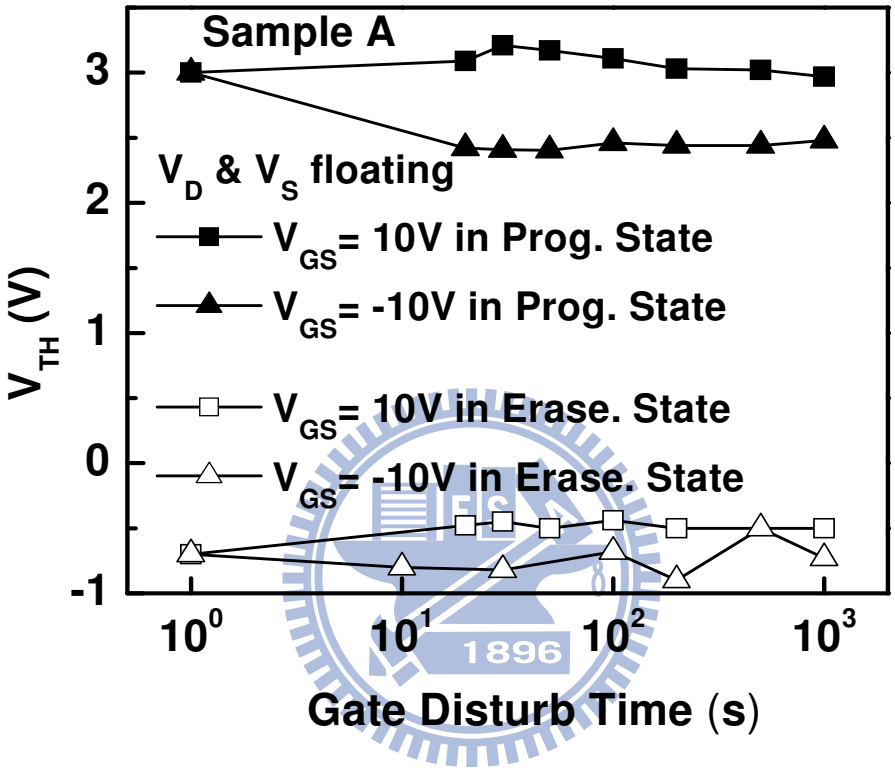

Fig. 4-13 Gate disturbance characteristics of sample A in four different states.

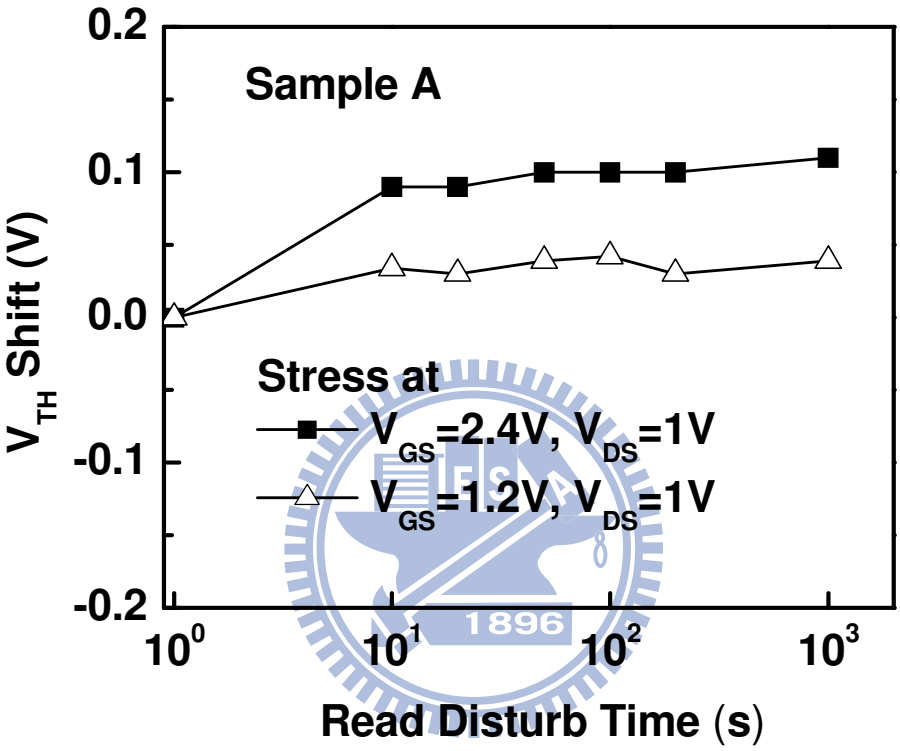

Fig. 4-14 Read disturbance of sample A in erase state for 10^3 sec stressing bias.

Chapter 5

Abnormal Current Modulation in the Turn-off State of 1-T Nano-Scale Multi-Gate Nanocrystal Memory

5.1 Introduction

The international technology roadmap for semiconductors (ITRS) recently forecasted that the scaling of conventional floating gate non-volatile memory is becoming increasingly difficult. For floating gate (FG) flash memories, no scalability of tunnel dielectric or inter-poly dielectric in the 22 nm node was predicted [1]. Nanocrystal memories, which utilize a thinner tunneling layer to improve memory characteristics without degrading retention performance because each nanocrystal is theoretically isolated by the surrounding dielectric is one possible replacement for the floating gate memories [2-4]. Meanwhile, several non-volatile memory architectures, such as magnetoresistive memories (MRAM) [5], phase change memories (PCM) [6], and resistance random access memories (RRAM) [7-13] have been widely investigated with a view to their future application in the non-volatile memory. On the other hand, to increase data storage density, both multi-bit operation and hybrid memory scheme are both possible strategies for the further scaling. It is well known that the flash memory can be manipulated by the injections of channel hot electrons

(CHE) and band-to-band hot holes (BTBHH) for programming and erasing, respectively. Moreover, for SONOS-type memory, since discrete charges are stored in the local nitride region near to the drain-side, dual-bit operation is proposed by utilizing the injections of CHE and BTBHH with selectable bit at read status [14]. Furthermore, dual bit operation is also presented by sensing the off-state gate induced drain leakage (GIDL) current and the on-state current in a SONOS-type memory [15]. In addition, BTBHHs are utilized to passivate the trapped electrons and suppress the off-state GIDL current to avoid mis-idenfication [16]. In the previous chapter, by using the Fowler-Nordheim (FN) tunneling for P/E operations, the memory characteristics in the turn-on state of a one-transistor (1-T) nano-scale silicon-Al_2O_3-metal TiN nanocrystal-SiO_2-silicon (SAMOS)-type multi-gate nanocrystal memory have been investigated. The charge trapping layer is composed of many TiN nanocrystals and the surrounding Al_2O_3 dielectric. In this chapter, this nanocrystal memory is attempted to operate by the injections of CHE and BTBHH first. However, no significant effect in the on-state is observed but an abnormal current modulation in the off-state at reverse read status is exhibited after biasing at the status of BTBHH. Moreover, this current modulation can be recovered by the bias at the status of CHE. This resistively switchable behavior and their off-state current in such a device are observed with excellent retention performance. Detail analyses indicate the conductance of the charge trapping layer close to drain-side would induce the current modulation. Possible mechanism will be proposed and discussed. Furthermore, this switchable behavior can be operated individually without affecting the memory state in the on-state. Therefore, possible dual-bit operation is demonstrated. However, some critical issues let this dual-bit operation is hard for practical application.

5.2 Devices Fabrication and Experiment

Multi-gate TiN metal nanocrystal memories with a channel width of 50 nm and a gate length of 80 nm were fabricated on a silicon-on-insulator (SOI) substrate. The details of the process procedures and the device structure can be found in the previous chapter. Samples A-C have different gate stacks. First, a 3.6-nm-thick thermally silicon dioxide layer was grown as a tunneling layer in all samples. Then, by the sequential deposition of the TiN and Al_2O_3 nano-laminates with seven periods in a clustered plasma enhanced atomic layer deposition/atomic layer deposition (PEALD/ALD) system and an annealing process after poly-gate deposition, an 8-nm-thick charge-trapping layer was formed, including TiN nanocrystals surrounded by Al_2O_3 dielectric. The diameters of the nanocrystal in these samples are about 3 nm in sample A and 1-2 nm in samples B and C. Finally, a 20-nm (samples A and B) or a 15-nm (sample C) -thick Al_2O_3 layer was deposited as the blocking dielectric layer. Table 5-1 lists the detail components of the gate stack in samples A-C. The current-voltage properties in the forward read (FR) mode and the reverse read (RR) mode are measured using an HP 4156C semiconductor parameter analyzer. In FR, the drain and source electrodes are biased at 1 V and 0 V, respectively. In RR, the biases of source and drain are exchanged, that is V_D=0 V and V_S=1 V.

5.3 Results and Discussion

5.3.1 Current Modulation and Switching Behavior in the Off-State

Figures 5-1(a)-(c) present the abnormal current modulation in the off-state of sample A. Figure 5-1(a) plots the transfer characteristics of fresh device after the application of first pulsing bias at V_G/V_D= +6/+6 V for 0.1 sec. Clearly, the short pulse does not affect the characteristics in FR and RR. The current-voltage characteristics are quiet similar in the on-state and off-state. The insets present the bias conditions of gate, source, and drain electrodes in FR and RR. However, in Fig. 5-1(b), when the second short pulse at V_G/V_D= -6/+6 V is applied for 0.1 sec, interesting transfer characteristics in the turn-off state are observed. The off-state current in FR and RR differs markedly; the off-state current is lower in RR, being around 1 pA, while the off-state current remains around 0.1 nA in FR. Furthermore, when another short pulse is subsequently applied at V_G/V_D= +6/+6 V for 0.1 sec as displayed in Fig. 5-1(c), the off-state current in RR recovers to around 0.1 nA and the transfer characteristic in RR is similar again to that in FR. Therefore, monitoring the current in RR at V_G = -3 V reveals that this current modulation would switch back and forth. Moreover, this reproducible resistive switching phenomenon includes the low resistive state (LRS) and the high resistive state (HRS) with a current ratio approximately 100 on sample A. Besides, in Fig. 5-1(a)-(c), no significant shift of threshold voltage can be observed after applying different biases. However, the biases of CHE at V_G/V_D= +6/+6 V and BTBHH at V_G/V_D= -6/+6 V are normally considered to generate and inject electrons and holes into the gate stack close to drain junction, respectively, and then alter the threshold voltage in the cell. Hence, hot carriers injection can not be utilized to manipulate our nanocrystal memories. Furthermore, it also indicates that the observed off-state current modulation and the reproducible switching behavior may be not induced by the locally trapped charges.

5.3.2 Further Analyses on the Off-State Current Modulation

Figure 5-2 depicts the retention performance in FR and RR of sample A following the application of pulsing bias at V_G/V_D= -6/+6 V. Initially, in the turn off-state, the drain current in FR differs from the source current in RR, as displayed in Fig. 5-1(b). Moreover, these off-currents remain constant for at least 10^6 s without visible degradation. The retention performance is excellent and no crosstalk occurs between FR and RR. If this switching phenomenon is caused by local charge trapping, then the magnitude of the off-state current in FR and RR should tend to converge as charges escape or are trapped. Hence, it confirms again that the current modulation is not induced by the charge trapping. Figure 5-3 plots the retention performance in the LRS and HRS at 25 °C and 85 °C. The source currents in RR in both states keep unchanged and the retention performance is good. This result reconfirms that the resistive switching mechanism does not involve locally trapped charges and another mechanism needs to be considered.

To elucidate the current flow in the off-state, Fig. 5-4 displays the components of current in that state after biasing at (a) V_G/V_D= -6/+6 V and (b) V_G/V_D= +6/+6 V. Only gate, source, and drain currents are detected because the body is floating. Notably, in both FR and RR, the gate current (green curves) always equals the sum of the drain current (black curves) and the source current (red curves) under biasing in the off-state, i.e. $|I_G|=|I_S|+|I_D|$. Accordingly, the current flows from the source/drain to the gate electrode and composes the mainly off-state current. Therefore, the off-state current is not responsible by the GIDL current since the GIDL current normally flows from the drain to the bulk but not flows into the gate electrode. Moreover, although Padilla et al. and Chen et al. presented the modulation of off-state GIDL current by the injection of BTBHH at drain-side, the GIDL current is modulated only in FR but

not in RR [15-16]. Therefore, the modulation of GIDL current is clearly not responsible for the resistive switching in Fig. 5-1. In addition, Fig. 5-5 shows the temperature dependence of the off-state current. It is clear that no temperature dependence of the off-state current can be observed at higher negative gate bias, which reconfirms the current is not dominated by the GIDL current. Furthermore, since gate current are quiet similar in both states at high negative gate voltage, it implies that a quiet large resistance exists in the gate stacks to determine the whole gate current.

In Fig. 5-4(a), for the current components of cell after biasing at V_G/V_D= -6/+6 V, the drain current comprises mostly the off-state current in FR and RR and the magnitude of drain currents are quiet similar to that of gate current, indicating that most of the gate leakage current arises from the drain-side. However, in Fig. 5-4(b), after biasing at V_G/V_D= +6/+6 V, most of the gate current comes from the drain current in FR (closed black squares) or the source current in RR (closed red circles), implying that the higher potential difference produces higher off-state current. Therefore, by focusing on the source current in RR, two different magnitudes of current are observed, i.e. HRS and LRS. Hence, it can be considered as the conductance of the gate dielectric stacks near at drain-side is switched back and forth by applying different biases, which induces the abnormal current modulation in the off-state.

To fully understand the possible mechanism for current flowing into gate stacks, another device which also shows the resistive switching phenomenon is measured. The gate, source, and drain currents have been sensed with connecting the source and drain electrodes to ground. Figure 5-6(a)-(b) show the current components after biasing at (a) V_G/V_D= -6/+6 V and (b) V_G/V_D= +6/+6 V, respectively. Firstly, the

magnitude of gate current are similar in both states, which means some layer inside the gate stacks act as a current limiter to determine the gate current at high negative bias. Moreover, in Fig. 5-6(a), the most gate leakage current is composed of the drain current in both FR and RR, which exhibits the same property as that of Fig. 5-4(a), indicating again that the conductance at parts of gate stacks near at drain junction is varied after the V_G/V_D= -6/+6 V stress. In addition, in Fig. 5-6(b), the magnitudes of source current and drain current are almost the same, which both provide the leakage current to the gate electrode equally, confirming that the locally modified conductance near drain junction is recovered and the major difference of the sensed currents at drain and source in FR and RR, respectively, are principally owing to the bias potential difference. Therefore, by the observation in the Fig. 5-6, it reconfirms the inference from Fig. 5-4 that the abnormal current modulation is induced by the switchable conductance at parts of gate stacks near at drain-side.

This switching phenomenon is also observed on the other samples, as shown in Fig. 5-7. The sample B has smaller TiN nanocrystals (diameter= 1-2 nm) but the same blocking oxide thickness, 20 nm, as sample A. The sample C has smaller TiN nanocrystals (diameter= 1-2 nm) but a thinner blocking oxide, 15 nm. In HRS, the sensed currents increase from around 1 pA in sample A to about 10 pA in samples B and C, as shown in Fig. 5-7, suggesting that the aforementioned locally switchable conductance occurs in the charge trapping layer. Hence, the conductance of the charge trapping layer is altered by the presence of smaller TiN nanocrystal, and that the charge trapping layer controls the HRS current after biasing at V_G/V_D= -6/+6 V. Moreover, in the LRS, the current increases only in sample C, as shown in Fig 5-7, indicating that the thickness of blocking layer determines the magnitude of the current after biasing at V_G/V_D= +6/+6 V. Additionally, since the source current in the LRS

contributes the main gate current and the current in the LRS can be manipulated by the thickness of the blocking layer, the aforesaid layer in the gate stacks with huge resistance is considered as the blocking layer and it acts as a current limiter at high negative gate voltage, i.e. V_G = -2 V to -4 V.

To simulate the cell status under the switching biases, the output characteristics of sample A is measured and shown in Fig.5-8(a). As the V_G/V_D = +6/+6 V, the cell is operated in the strong turn-on state and the drain bias reduces the conductivity of channel near at drain-side and thus increases the potential drop to accelerate the electrons. By the enhancement of vertical field, these hot electrons would inject into gate dielectric near at drain region, which is the so-called hot electron injection. Moreover, as the gate voltage bias at -6 V, the cell is normally manipulated at off-state and no carriers can be conducted. However, as the drain voltage increases to around +5.5 V, the channel is suddenly conducted and large current is sensed. Furthermore, large gate current is also measured at V_G/V_D = -6/+6 V, as shown in Fig. 5-8(b), indicating a large amount of hot holes are generated and injected into the gate stacks. This abrupt increase of drain current can be explained by the punchthrough and impact ionization effect [17-18]. This particular behavior only occurs on the short channel device with lightly doped channel as the gate voltage is smaller than the threshold voltage and large drain voltage is applied. At high drain voltage, impact ionization takes place and since the saddle point of the electrostatic potential is created in the channel, part of holes would accumulate at this potential pocket, locating at the oxide/channel interface close to the middle point from the source to drain and thus redistributes the potential in the channel. Finally, the followed punchthrough effect would be triggered and thus an abrupt increasing of drain current is observed. Moreover, an outstanding subthreshold slope of transfer characteristic

can also be achieved. In our cell, a similar behavior in the transfer characteristic which the subthreshold slope equals to 2.5 mV/decade is observed, as shown in Fig. 5-9. Therefore, during biasing at V_G/V_D= -6/+6 V in our cell, both punchthrough and impact ionization effects were happened to induce large current flow from source to drain. Moreover, at this bias condition, the band-to-band hot holes are also supposed to occur. Therefore, large amount of accumulated holes are expect to inject from the potential pocket close to the middle of channel and near at drain-side.

Since the creation of hot holes is related to the punchthrough effect, the observed abnormal current modulation should have some relation with the channel length. Figure 5-10 shows the area effect of the current modulation. Both currents in the LRS and HRS are displayed as a function of gate length. It can be observed that the effectiveness of current modulation, i.e. current of HRS, is getting lower as the gate length increases. No clear difference of LRS and HRS are shown as the gate length is longer than 0.16 μm. Hence, the off-state current modulation only happens on the short channel devices.

5.3.3 Possible Switching Mechanism

Material that contains the Ti element is an effective extractor of oxygen, inducing an interface reaction and forming many oxygen vacancies in the thin dielectric film [10-11]. Hence, the TiN nanocrystals are suspected to generate oxygen vacancies in the surrounding Al_2O_3 charge trapping layer. Moreover, the resistive switching mechanism of the Al_2O_3 thin film is commonly described as the formation of conducting filaments owing to the oxygen-related defects [9-10]. Additionally, binary oxide thin films with various embedded metal nanocrystals have been presented to exhibit better resistive switching property [12-13]. Therefore, we suppose the current

modulation and its resistive switching phenomenon can be considered as the formation and rupture of the conducting filaments in the charge trapping layer close to the drain region, as shown in Fig. 5-11. Moreover, the abovementioned observations indicate that the V_G/V_D pulse changes the property of the charge trapping layer near the drain-side. The thick blocking layer act as a current limiter and has a much higher resistance than that of charge trapping layer to limit the leakage current at high $|V_G|$. Hence, the repeated alteration of the conductance of the charge trapping layer near at drain-side results in the current modulation and the resistance switching phenomenon.

Under biasing at V_G/V_D = -6/+6 V, as mentioned above, a high-field promotes the injection of hot holes into the gate stack from the middle of channel and near the G/D overlap region, potentially inducing the formation of conductive filaments between the TiN nanocrystals in charge trapping layer, as depicted in the Fig. 5-11(a). The resistance of the drain side charge trapping layer is thus greatly reduced, while the resistance of the source side charge trapping layer remains high. Therefore, as shown in Fig. 5-4(a) and Fig. 5-6(a), a large drain current is detected no matter in FR or in RR, even at low $|V_G|$. In this status, most of the gate current comes from the drain-side. Additionally, since the blocking layer limits the magnitude of the total gate current, the gate current equals to the sum of the drain current and the source current in the off-state. Due to the above reason, a low source current is detected in both FR and RR due to the higher resistance source-side charge trapping layer. Therefore, small source current in RR are sensed and thus the off-state current modulation occurs.

In contrast, pulsing at V_G/V_D = +6/+6 V ruptures the conducting filaments in the charge trapping layer close to the drain region but the conducting filaments locate in the middle region still remain, as shown in Fig. 5-11(b). The resistance near at the drain-side is recovered to a value similar to that in the source-side. Hence, equal

source and drain currents are sensed as shown in Fig. 5-6(b). In addition, the higher sensed current depends on the larger difference between the biases of the gate/source in RR and the gate/drain electrodes in FR, so that the LRS is detected from the source side in RR, as shown in Fig. 5-4(b). Furthermore, in Fig. 5-7, according to this proposed model, the currents of samples B and C in HRS increase as the size of nanocrystals decrease and thus the space of the near nanocrystals are increased, lowering the possibility of formation of a conducting path. Higher LRS current of sample C is observed because it has a thinner integrated blocking layer. It should be noted that since the mechanism of the current modulation is the RRAM-like mechanism occurs in the gate stack, it should be careful for using novel dielectrics in the gate stacks of nanocrystal memories, especially the dielectrics which exhibit RRAM characteristics.

5.3.4 Potential of Dual-Bit Operation

Since the current modulation is not due to charge trapping so that the cell can be simultaneously operated as an NCM in the turn-on state, multi-bit operation can be successfully achieved. Figure 5-12 demonstrates the potential of dual-bit operation in this nano-scale multi-gate memory cell. When the device is operated as a nanocrystal memory, Fowler-Nordheim tunneling is employed to inject electrons or holes into the TiN nanocrystals, causing a clear shift of threshold voltage. Moreover, off-state current modulation and resistance switching are realized after different biases are simultaneously applied at the gate/drain. Each bit can be individually operated without influencing the sensed memory state of another bit. However, some critical issues would cause this dual-bit operation hard for practical application. Firstly, two reading biases are required, which increases the complexity of the design of the output

control circuit. Second, the read currents are too small in the off-state. The typical sensing circuit needs the magnitude of several μA. Therefore, although this current modulation reveals some possibility for memory application, the difficulty may retard to carry out.

5.4 Conclusions

In this chapter, an abnormal off-state current modulation in reverse read mode on a nano-scale nanocrystal memory cell is observed and characterized, which also exhibits an interesting reproducible resistive switching phenomenon. By applying different biases on the gate and drain electrodes, two reproducible resistance states with a resistance ratio of approximately 100 and excellent retention properties are observed. Moreover, the gate current is composed of the drain current and the source current, indicating that the modulation of GIDL current is not responsible for this interesting behavior. Furthermore, the thickness of the blocking dielectric has a large resistance to limit the gate current and the magnitude of current in the LRS. The size of the TiN nanocrystal influences the magnitude of currents in HRS, indicating that the current modulation to HRS is controlled by the property of the charge trapping layer near at drain-side. The switching mechanism is supposed due to the formation and rupture of conducting filaments in the local charge trapping layer. In addition, dual-bit operation can be achieved by resistance switching in the turn-off state and the threshold shift in the turn-on state. However, several peripheral circuit design issues would retard this dual-bit behavior for practical application.

References

[1] Process Integration, Devices and Structures in International Technology Roadmap for Semiconductors 2009 edition, pp. 13-20, 2009.

[2] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal Nanocrystal Memories—Part I: Device Design and Fabrication," *IEEE Trans. Electron Devices,* vol. 49, no. 9, pp. 1606-1613, 2002.

[3] T.-H. Hou, C. Lee, V. Narayanan, U. Ganguly, and E. C. Kan, "Design Optimization of Metal Nanocrystal Memory- Part I: Nanocrystal Array Engineering," *IEEE Trans. Electron Devices*, vol.53, no.12, pp. 3095-3102, 2006.

[4] C.-P. Lu, C.-K. Luo, B.-Y. Tsui, C.-H. Lin, P.-J. Tzeng, C.-C. Wang, and M.-J. Tsai, "Nanoscale Multigate TiN Metal Nanocrystal Memory Using High-*k* Blocking Dielectric and High-Work-Function Gate Electrode Integrated on Silcon-on-Insulator Substrate," *Jap. J. Appl. Phys.*, vol. 48, p. 04C059, 2009.

[5] S. Tehrani, J. M. Slaughter, E. Chen, M. Durlam, J. Shi, and M. DeHerrera, "Progress and Outlook for MRAM Technology," *IEEE Trans. Magnetics*, vol. 35, no. 5, pp. 2814-2819, 1999

[6] M. H. R. Lankhorst, B. W. S. M. M. Ketelaars, and R. A. M. Wolters, "Low-cost and nanoscale non-volatile memory concept for future silicon chips," *Nature Materials*, vol. 4, pp. 347-352, 2005

[7] G. Dearnaley, A. M. Stoneham, and D. V. Morgan, "Electrical phenomena in amorphous oxide films," *Rep. Prog. Phys.*, vol. 33, pp. 1129-1189, 1970

[8] K. M. Kim, B. J. Choi, B. W. Koo, S. Choi, D. S. Jeong, and C. S. Hwang, "Resistive Switching in Pt/Al_2O_3/TiO_2/Ru Stacked Structures," *Electrochem. Solid-State Lett.*, vol. 9, no. 12, pp. G343-G346, 2006

[9] S. Kim, and Y.-K. Choi, "Resistive switching of aluminum oxide for flexible memory," *Appl. Phys. Lett.*, vol. 92, no. 22, p. 223508, 2008.

[10] C.-Y. Lin, C.-Y. Wu, C.-Y. Wu, C. Hu, and T.-Y. Tseng, "Bistable Resistive Switching in Al_2O_3 Memory Thin Films," *J. Electrochem. Soc.*, vol. 154, no. 9, pp. G189-G192, 2007

[11] A. Sawa, T. Fujii, M. Kawasaki, and Y. Tokura, "Hysteretic current–voltage characteristics and resistance switching at a rectifying $Ti/Pr_{0.7}Ca_{0.3}MnO_3$ interface," *Appl. Phys. Lett.* vol. 85, no. 18, pp. 4073-4075, 2004

[12] W-Y. Chang, K.-J. Cheng, J.-M. Tsai, H.-J. Chen, F. Chen, M.–J. Tsai, and T.-B. Wu, "Improvement of resistive switching characteristics in TiO_2 thin films with embedded Pt nanocrystals," *Appl. Phys. Lett.* vol. 95, no. 4, p. 042104, 2009

[13] Q. Zuo, S. Long, Q. Liu, S. Zhang, Q. Wang, Y. Li, Y. Wang, and M. Liu, "Self-rectifying effect in gold nanocrystal-embedded zirconium oxide resistive memory," *J. Appl. Phys.* vol. 106, no. 7, p. 073724, 2009

[14] M. Specht, R. Kömmling, F. Hofmann, V. Klandzievski, L. Dreeskornfeld, W. Weber, J. Kretz, E. Landgraf, T. Schulz, J. Hartwich, W. Rösner, M. Städele, R. J. Luyken, H. Reisinger, A. Graham, E. Hartmann, and L. Risch, " Novel Dual Bit Tri-Gate Charge Trapping Memory Devices," *IEEE Electron Devices Lett*, vol. 25, no. 12, pp. 810-812, 2004

[15] A. Padilla, K. Shin, T.-J. King Liu, J. W. Hyun, I. Yoo, and Y. Park, "Dual-Bit Gate-Sidewall Storage FinFET NVM and New Method of Charge Detection," *IEEE Electron Devices Lett*, vol. 28, no. 6, pp. 502-505, 2007

[16] T.-C. Chen, T.-C. Chang, F.-Y. Jian, S.-C. Chen, C.-S. Lin, M.-H. Lee, J.-S. Chen, and C.-C. Shih, "Improvement of Memory State Misidentification Caused by Trap-Assisted GIDL Current in a SONOS-TFT Memory Device," *IEEE*

Electron Devices Lett, vol. 30, no. 8, pp. 834-836, 2009

[17] A. Boudou, and B. S. Doyle, "Hysteresis I-V Effects in Short-Channel Silicon MOSFET's," *IEEE Electron Devices Lett*, vol. EDL-8, no. 7, pp. 300-302, 1987

[18] K. E. Moselund, D. Bouvet, V. Pott, C. Meinen, M. Kayal, and A.M. Ionescu, "Punch-through impact ionization MOSFET (PIMOS): From device principle to applications," *Solid-State Electronics*, vol. 52, no. 9, pp. 1336-1344, 2008

Table 5-1: Gate stack conditions of samples A-C.

Sample	Tunneling Layer	Trapping Layer	Blocking Layer
	SiO_2 (nm)	TiN NC Diameter (nm)	Al_2O_3 (nm)
A	3.6	3	20
B	3.6	1-2	20
C	3.6	1-2	15

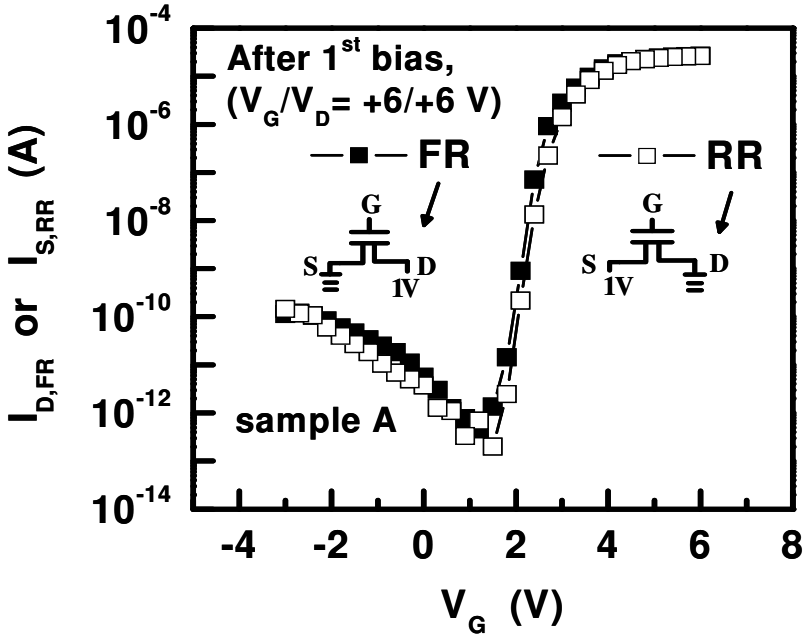

Fig. 5-1(a) Transfer characteristics after applying for the first pulsing at V_G/V_D = +6/+6 V.

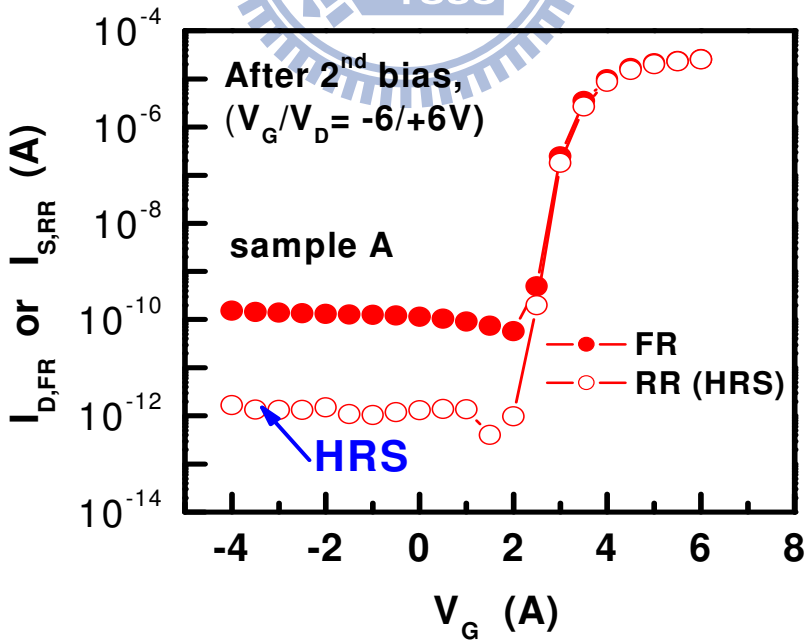

Fig. 5-1(b) Transfer characteristics after applying for the second pulsing at V_G/V_D= -6/+6 V. The off-state current modulation shows in the RR mode.

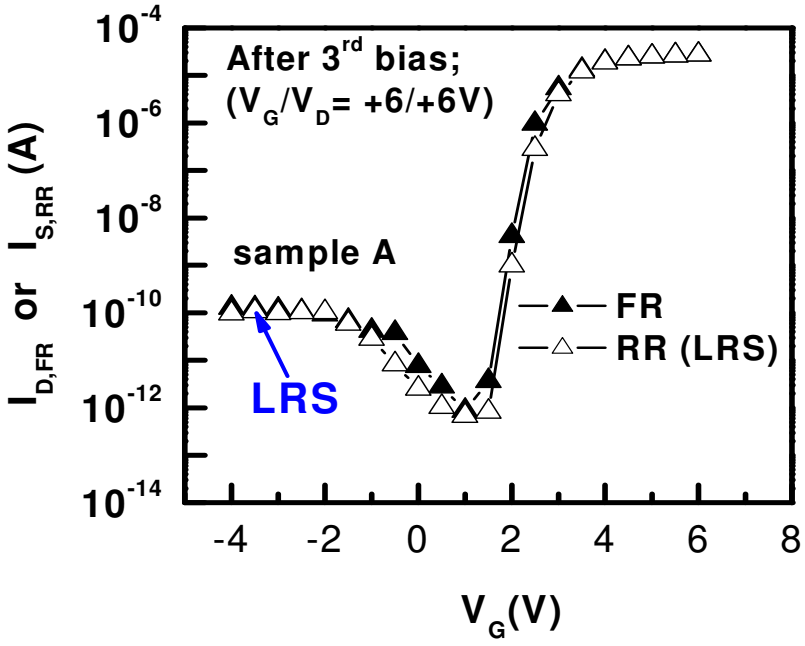

Fig. 5-1(c) Transfer characteristics after applying for the third pulsing at V_G/V_D= +6/+6 V. Reproducible switching phenomenon shows in the turn-off state.

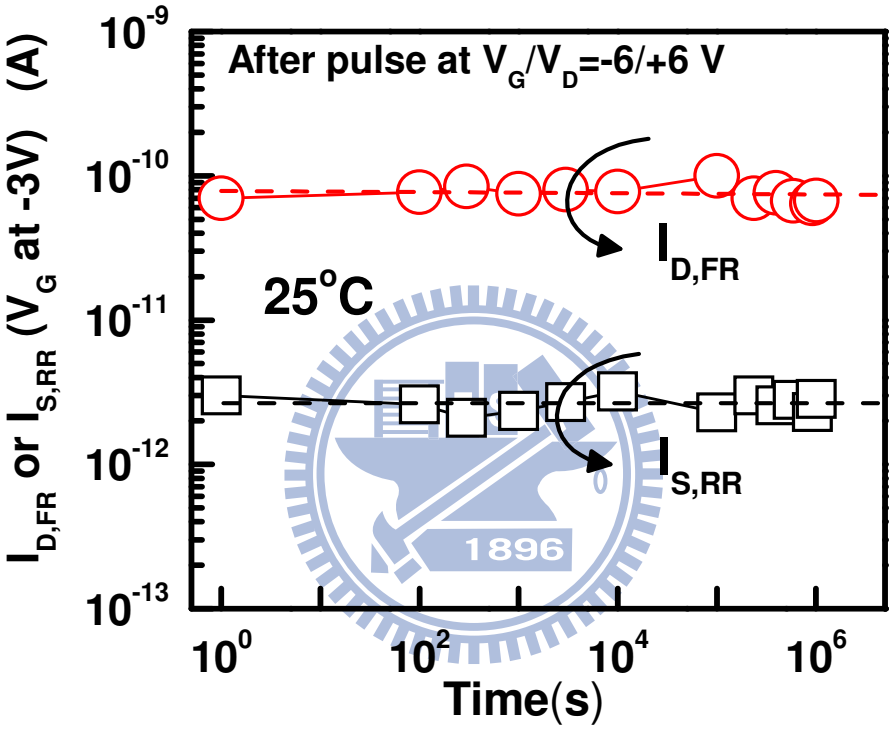

Fig. 5-2 Retention performance in FR and RR of sample A after pulsing bias at V_G/V_D= -6/+6 V and 25 °C.

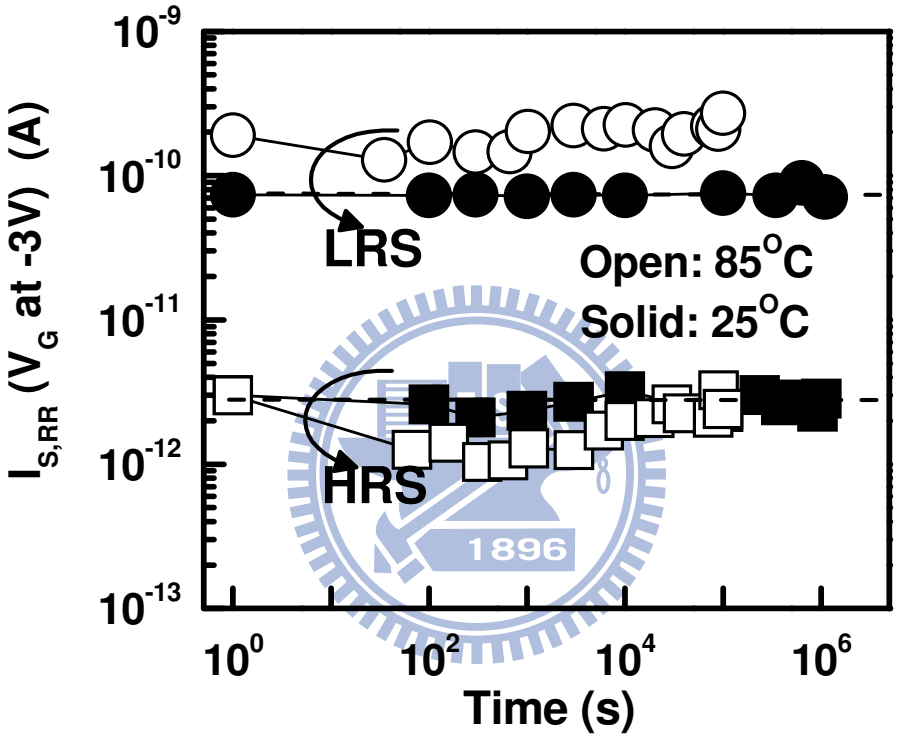

Fig. 5-3 Retention performance at HRS and LRS of sample A at 25 °C and 85 °C.

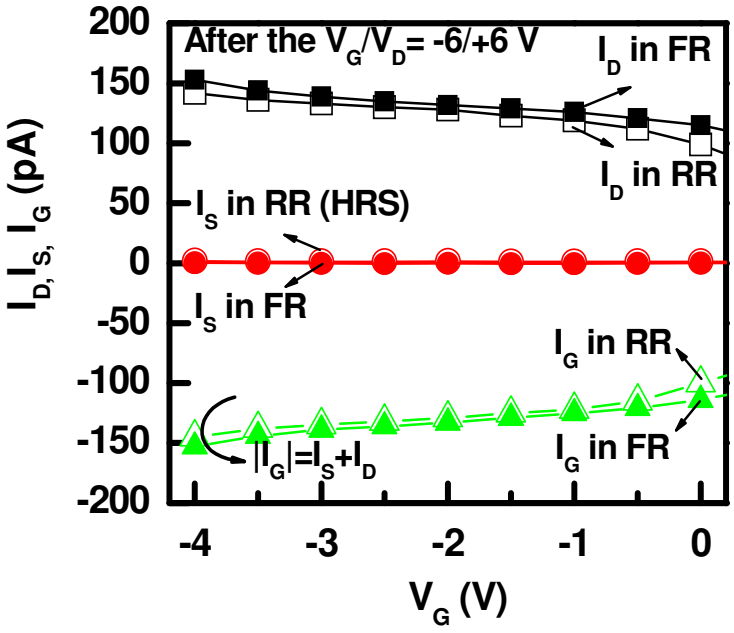

Fig. 5-4(a) Current components of sample A after pulsing at V_G/V_D= -6/+6 V. Main gate leakage current comes from the drain electrode.

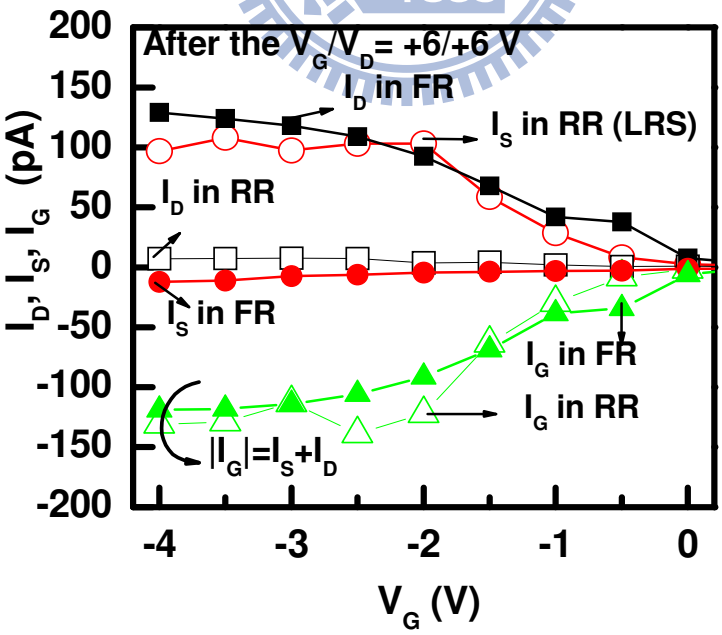

Fig. 5-4(b) Current components of sample A after pulsing at V_G/V_D= +6/+6 V. Gate leakage current mainly depends on the potential difference.

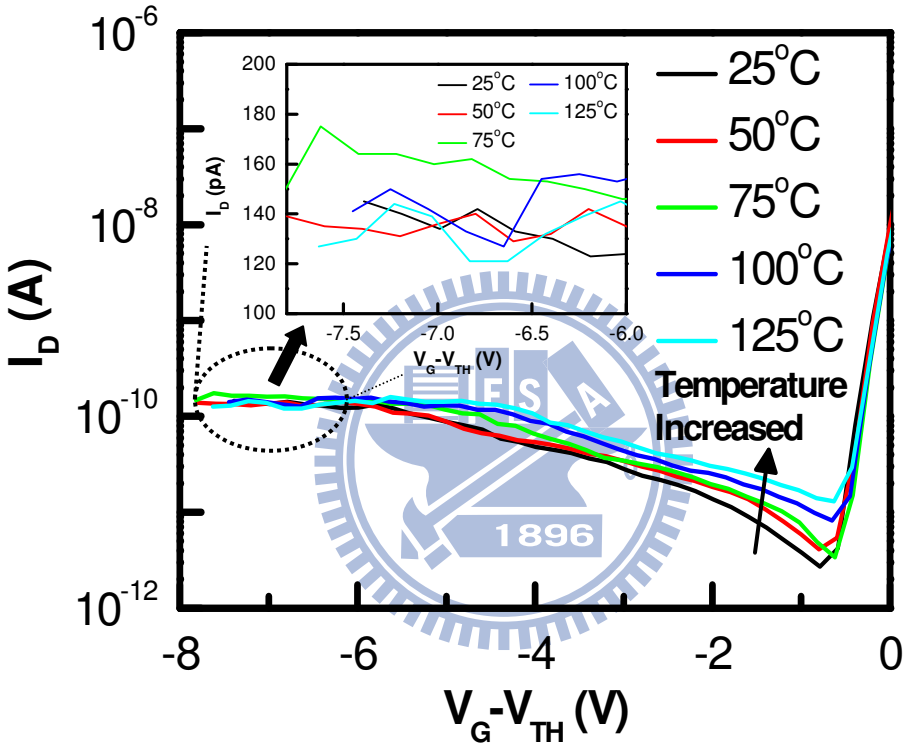

Fig. 5-5 The off-state current in sample A with different chuck temperature. No temperature dependence of the off-state current is observed at higher negative gate bias.

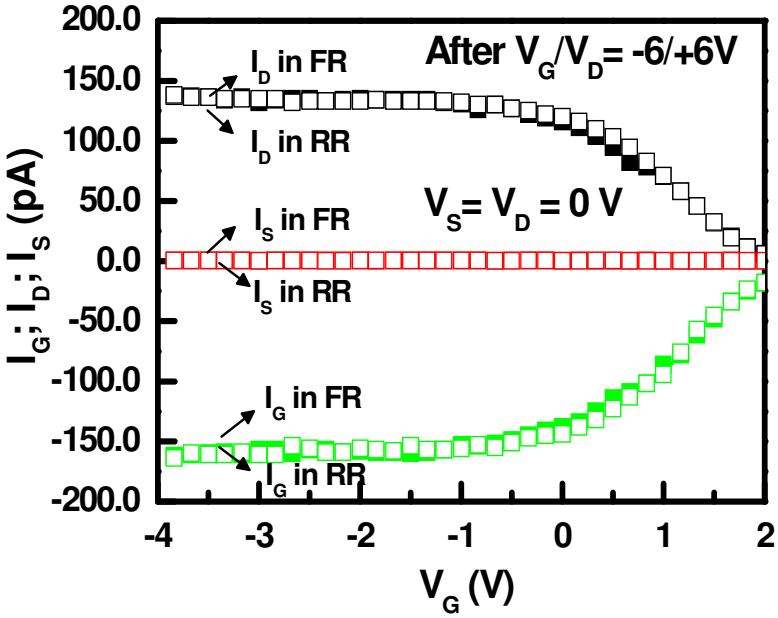

Fig. 5-6(a) Current components of sample A after pulsing at V_G/V_D= -6/+6 V with grounding the source and drain electrodes.

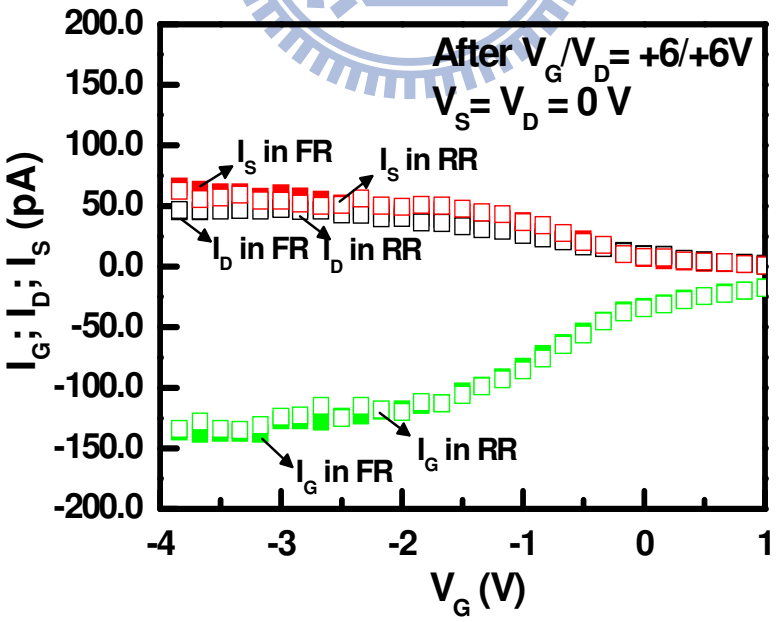

Fig. 5-6(b) Current components of sample A after pulsing at V_G/V_D= +6/+6 V with grounding the source and drain electrodes.

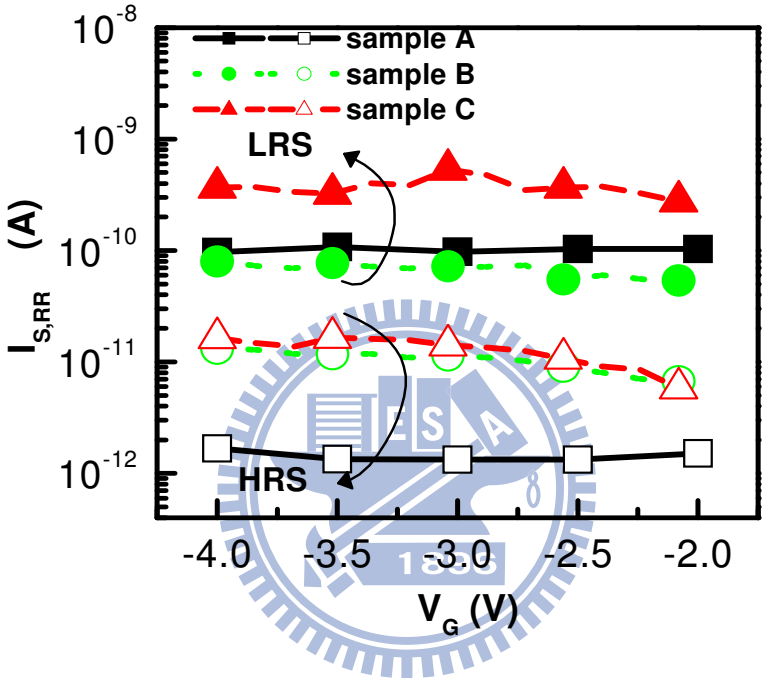

Fig. 5-7 The electrical-bias-induced resistive switching phenomenon in sample A-C. The property of the charge trapping layer controls the HRS current and the thickness of the blocking layer dominates the magnitude of the LRS current.

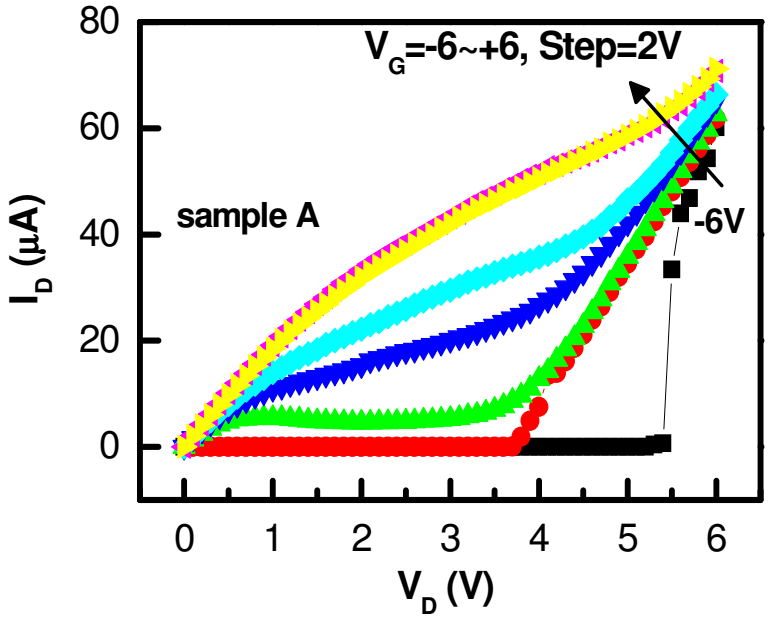

Fig. 5-8(a) Output characteristics of sample A with the V_G biases from -6 V to +6 V. Impact ionization and punchthrough effects induce abrupt current.

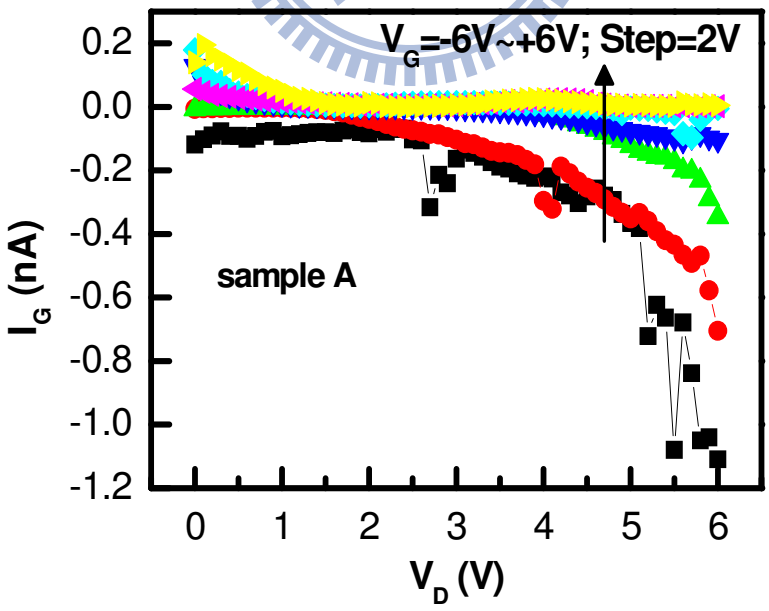

Fig. 5-8(b) Gate leakage current of sample A with the V_G biases from -6 V to +6 V. Large gate current is sensed as the V_G/V_D = -6/+6 V.

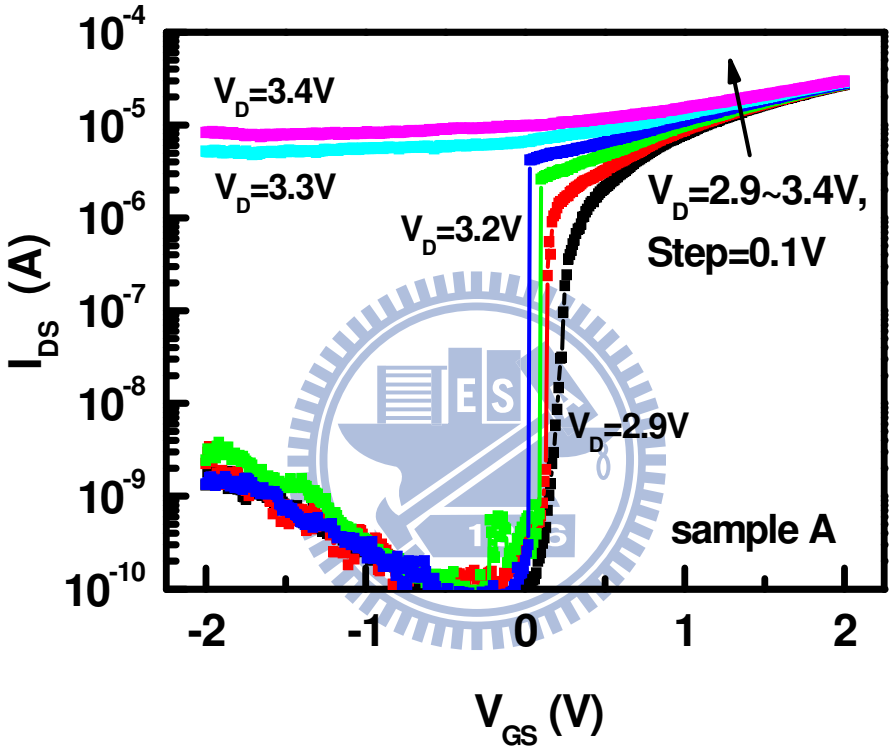

Fig. 5-9 Transfer characteristics of sample A with the V_D bias from 2.9 V to 3.4 V. When the V_D=3.2 V, outstanding subthreshold swing equals to 2.5 mV/decade is obtained owing to the impact ionization and punchthrough effects induced abrupt current.

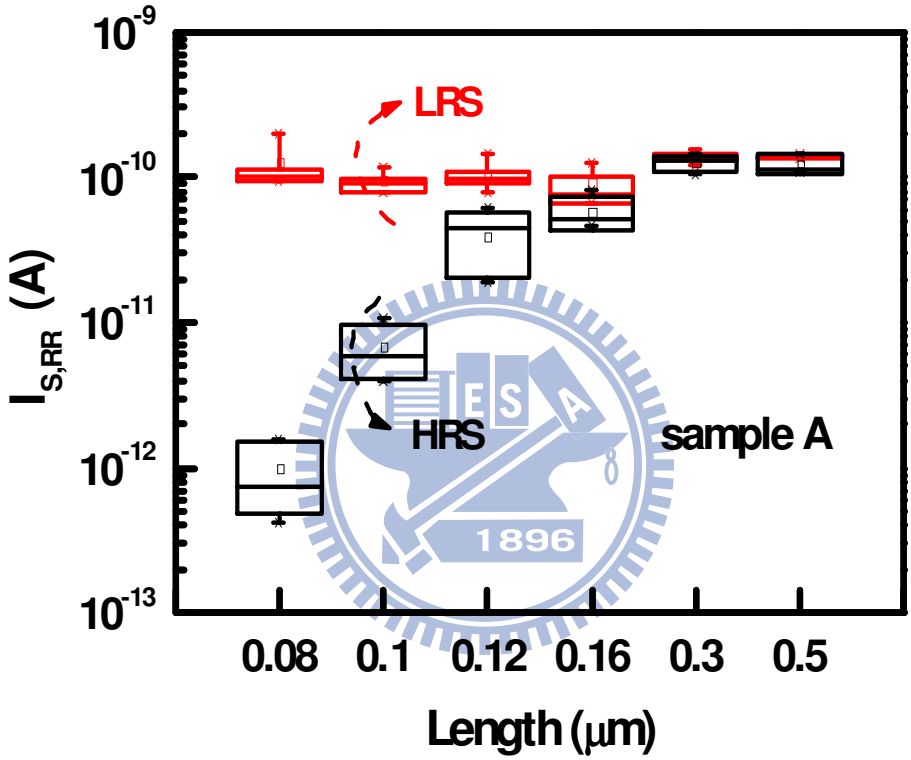

Fig. 5-10 The area dependence of the current modulation in sample A. Currents of HRS and LRS with different gate length are shown. No clear difference between the HRS and LRS as the gate length larger than 0.16 μm.

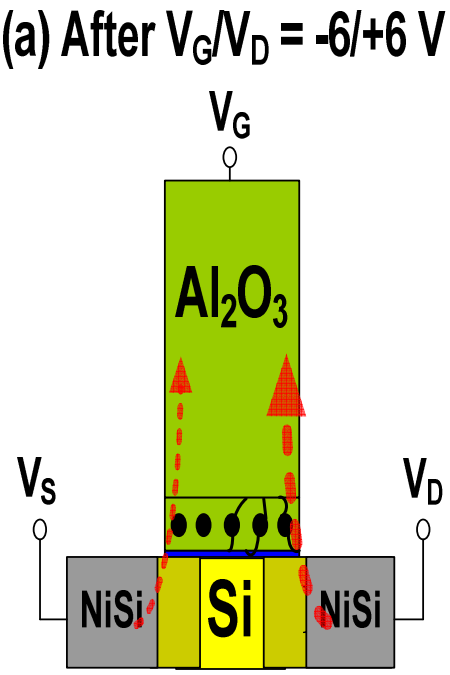

Fig. 5-11(a) The schematic illustrations of the possible switching mechanism after V_G/V_D = -6/+6 V (HRS). Smaller source current is sensed.

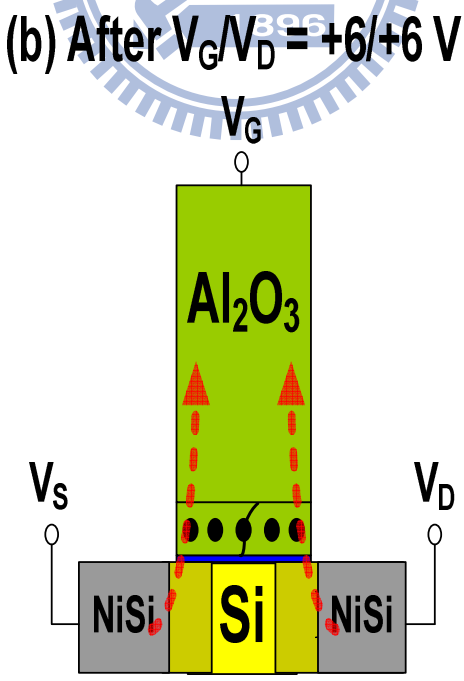

Fig. 5-11(b) The schematic illustrations of the possible switching mechanism after V_G/V_D = +6/+6 V (LRS). Larger source current is sensed.

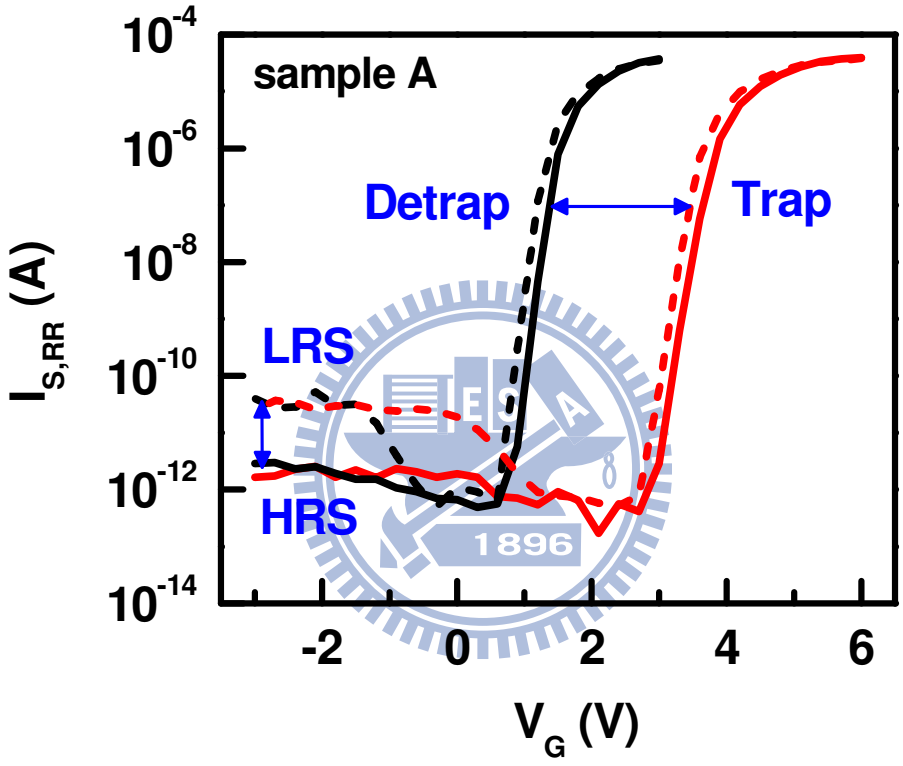

Fig. 5-12 Potential of dual-bit operation in the nanoscale multi-gate nanocrystal memory cell. It is achieved by resistive switching in the off-state and NCM operation in the on-state.

Chapter 6

Conclusions and Further Recommendations

6.1 Conclusions

In this dissertation, multi-gate devices with the modified Schottky barrier (MSB) junction for CMOS logic application and with the TiN metal nanocrystal for nonvolatile memory application are studied. For the MOSFET' applications, the bias-dependent influence of the existed MSB on the current transportation mechanisms and on the extracted series resistance are demonstrated. A novel extraction method for the bias-dependent source injection resistance is provided. For the flash memory' applications, the gate stacks engineering of nano-scale TiN metal nanocrystal memory with Al_2O_3 high-k blocking dielectric layer and P^+ high work function gate electrode are demonstrated. An abnormal current modulation in the off-state and the possible induced mechanism are discussed. The important results and observation are summarized as follows:

Since different temperature dependence of the drift-diffusion model, thermionic emission and tunneling, the current transportation mechanisms of the n/p-channel MSB MOSFET or SB MOSFET are identified by measuring the temperature effect in chapter 2. The dominated mechanism is major depended on the height and thickness of SB which is also deformed by the gate/drain biases. Hence, as the gate bias increases, the current transportation mechanism of SB MOSFET is firstly controlled

by the tunneling or thermionic emission during at low electric field, depending on the thickness and height of SB. Then, at sufficient high gate bias, the drift-diffusion model is dominated. Moreover, MSB junctions are successfully fabricated by the implantation-to-silicide (ITS) technology and the low temperature post-ITS annealing, which effectively suppresses the height and thickness of SB. Therefore, the current transportation mechanism of n/p-channel MSB MOSFET changes from the thermionic emission to tunneling and then to drift diffusion as increasing the performed gate voltage. In addition, the intersect point of transfer characteristics at different temperature is observed, indicating the changes of current transportation. Moreover, device with non-sufficient thermal budget for MSB junction formation exhibits much larger gate voltage of the changing point. Therefore, this changing point is a good indicator to evaluate the efficiency of the MSB junction.

In chapter 3, a novel modified external load resistance method is proposed to extract the bias dependent source injection resistance of the MSB MOSFET. In order to obtain the extracted R_{SD} in the small gate bias region which is slightly lager than the threshold voltage, moderate large resistance of the external loads are required to be selected. By utilizing this method, the bias dependent source injection resistance is observed on the devices which used SiO_2 or HfAlO layer as gate dielectric. The extracted R_{SD} displays exponentially proportional to $(V_{GS}\text{-}V_{TH}\text{-}0.5V_{DS})$ at low bias region but saturates at sufficient large gate voltage bias, indicating that the source-side barrier of MSB junction dominates and affects the current flow at low electric field but becomes transparent for the carriers at sufficient large electric field. Moreover, device with non-sufficient thermal budget for MSB junction formation exhibits much larger R_{SD} and can not be suppressed effectively at reasonable V_{GS}. Therefore, the

proposed external loading method is another good indicator to evaluate the efficiency of the MSB junction.

In chapter 4, n-channel tri-gate SAMOS-type metal nanocrystal memories using TiN nanocrystals as discrete storage nodes, Al_2O_3 high-k blocking dielectric layer and p^+ poly-Si gate were successfully fabricated with gate length equals to 80 nm and fin width equals to 50 nm. Memory window as higher as 5.2 V is achieved after P/E operation at ± 10V for 0.1sec. High endurance performance around 93 % after 10^4 P/E cycles and small disturbance are obtained. Moreover, from engineering on the charge trapping layer, the nanocrystal size will extremely affect the memory characteristic. The TiN nanocrystals are formed by the post annealing which is followed the cyclic deposition of TiN/Al_2O_3 nano-laminates. Diameters of TiN nanocrystal are around 3 nm and 1-2 nm in different samples. It is found that the thicker TiN nano-laminate is used, the larger TiN nanocrystals are formed and hence the larger memory window is obtained. The strong Coulomb blockade effect would limit the trapping efficiency and slow the P/E speeds. In addition, retention performance is also dominated by the Coulomb blockade effect. Furthermore, to get better retention performance, suitable initial P/E states should be carefully selected. Finally, good endurance and disturbance performance can be obtained since the multi-gate structure on an SOI wafer with a floating body can reduce inner electric field to suppress trapped charge migration.

In chapter 5, an interesting electric-bias-induced reproducible change of reverse-read current in the turn-off state is observed in the nano-scale tri-gate TiN nanocrystal memories which are built in chapter 4. Two repeatably switchable states, i.e. HRS and LRS, are revealed with a moderate current ratio of approximately 100, and excellent retention performance in both states. The current components indicate that the gate leakage current is arisen from the source and drain. And the conductance of the local

gate stacks close to drain junction is changed back and forth as operating between the HRS and LRS. Moreover, current modulation of the other samples reveal that the magnitude of LRS current is dominated by the thickness of blocking layer and the magnitude of HRS current is controlled by the size of TiN nanocrystal, indicating that the blocking layer acts as a current limiter at moderate high negative gate bias and dominates the gate leakage at both LRS and HRS. Then, the property of the charge trapping layer near at drain-side dominates the current modulation at HRS. Furthermore, a supposed switching mechanism is provided owing to the conducting filament formation and rupture in the charge trapping layer near to the drain-side. In addition, since the abnormal current modulation is considered as the conducting filaments related effect occurs in the gate stacks, it should be noted that if using some novel materials in the nanocrystal memory which have RRAM-like property may also induce similar behavior in the off-state current.

6.2 Further Recommendations

There have several topics and suggestions which are worthy for the further research and mention below,

1. For the MOSFETs with surrounding gate structure, in order to further increase the gate controllability, the nano-wire structure is suggested to apply. In this structure, the Si channel is fully surrounded by the gate oxide and gate electrode, which is the extreme case for the achievement of multi-gate structure. Moreover, MSB source/drain junction and high-k gate dielectric layer are both recommended to integrate into this structure for obtaining higher driving capability and better immunity of the short channel effect.

2. In chapter 2 and chapter 3, while applying the MSB S/D junction on the multi-gate SOI devices, since different magnitude of the fringe field from gate electrode, the location of the interface of Ni-silicide/Si channel is a critical parameter to influence the current-voltage performance, current transportation mechanism, and the extracted R_T. Therefore, in order to achieve the optimization of MSB junction, it is quiet important to optimize the two step Ni-silicidation process and further well control the concentration and length of source/drain extension regions.
3. In chapter 2 and chapter 3, to observe the simple influence of the MSB junction on the current transportation mechanisms and source-injection resistance, we extract these effects and parameter on the long channel devices with MSB junction but the short channel device, since velocity enhancement effect would be incorporated in the carrier transportation. However, till now, the carrier injection velocity enhancement effect on the short channel device with the MSB junction which is fabricated by the ITS method is still lack. Therefore, it is also worthy to investigate the transportation mechanism and the temperature effect on the nano-scale MSB MOSFETs.
4. In chapter 2 and chapter 3, although we proposed that the temperature effect and the extraction of the bias-dependent source injection resistance are both good indicators to evaluate the efficiency of the MSB junction, the real doping concentration of the MSB junction is still lack. Moreover, each of the spacer length, the dose of ITS, the lateral encroachment length of silicide, and the post-ITS thermal budget would affect the modulation of SB height and thickness. Hence, it will very helpful to obtain the length and doping concentration of MSB junction. Nevertheless, until now, it is still short of the analysis technology or

equipment to directly measure this ultra-thin and highly doped SDE. Therefore, new technology is required.

5. In chapter 4, the NCM uses the tiny TiN nanorcrystal as the storage node, indicating the main degradation of the memory characteristics is considered as the Coulomb blockage effect. However, there still have some factors to influence the capture and escape of carriers. Different bias conditions and variant structure parameters are required to be considered to affect the property at program, erasing, or read state. Hence, further detail analysis on the carrier behavior at P/E, read states can be achieved by the help of the TCAD simulation.
6. In chapter 4, since too small TiN nanocrystals would degrade the memory performance, some modification would enhance the properties. Therefore, it is suspected that thicker TiN nano-laminated can be used for forming larger TiN nanocrystals, which may help for increasing the P/E speeds, enlarging memory window and enhancing the retention performance. Moreover, the Al_2O_3 blocking layer is crystallized to induce the degradation of retention property, which is required to be avoided or replaced by the new high-k material with higher crystallization temperature and moderate large energy band gap. Moreover, since the thickness of gate stacks are too thick, the gate electrode does not fully cover the sidewall of Si-fin, especially in the bottom corner, as shown in Fig. 4-2(b). Hence, by inserting a process to recessing the buried oxide can effective improve and modify the structure of cell. Furthermore, other materials which exhibit higher work function may be used to enhance the retention performance since TiN is a kind of material which has mid-gap work function around 4.5 ~ 4.6 eV.
7. In chapter 5, the supposed switching model is mainly attributed by the formation and rupture of the conducting filaments in the local charge trapping layer. This

hypothesis is based on the RRAM-like switching mechanism. However, although lots amount of specialists are devoted to the research and development of the RRAM, the real cause of the conducting filament is required to further understanding. Therefore, it is waiting for the new method to actual observe the supposed conducting filaments in the NCM.

Publication List

Journal Paper:

1. B.-Y. Tsui and **C.-P. Lu**, "Method for Extracting Gate-Voltage- Dependent Source Injection Resistance of Modified Schottky Barrier (MSB) MOSFETs," *IEEE Electron Device Lett.,* vol. 29, no. 9, pp.1053-1055, 2008.
2. **C.-P. Lu**, B.-Y. Tsui, C.-K. Luo, C.-H. Lin, P.-J. Tzeng, C.-C. Wang, and M.–J. Tsai, "Tri-gate TiN Nanocrystal Memory with High-k Blocking Dielectric Layer and High Work Function Gate Electrode," *Electrochemical and Solid-state Letter,* vol. 12, H70, 2009.
3. **C.-P. Lu**, C.-K. Luo, B.-Y. Tsui, C.-H. Lin, P.-J. Tzeng, C.-C. Wang, and M.–J. Tsai, "Nano-scale Multi-gate TiN Metal Nano-crystal Memory using High-k Blocking Dielectric and the High Work Function Gate Electrode Integrated on SOI Substrate," *Japanese Journal of Applied Physics*, vol. 48, 04C059, 2009.

Conference Paper

1. B.-Y. Tsui and **C.-P. Lu**, "Current Transport Mechanisms of Schottky Barrier and Modified Schottky Barrier MOSFETs," in *Proc. of the 37th European Solid State Device Research Conference*, pp.307-310, 2007.
2. **C.-P. Lu**, B.-Y. Tsui, C.-P. Lin and Y.-J. Lee, "Current Transport Mechanisms of p-channel Schottky Barrier and Modified Schottky Barrier MOSFETs," in *15th Symposium on Nano Device Technology*, 2007.
3. B.-Y. Tsui and **C.-P. Lu**, and Hsiao-Han Liu, "Bias-Dependent Source Injection Resistance of Modified Schottky Barrier MOSFET," in Proc. of the 2008 IEEE *Silicon Nanoelectronics Workshop,* pp. p1_1-2, 2008.
4. **C.-P. Lu**, C. K. Luo, B. Y. Tsui, C. H. Lin P. J. Tzeng, C. C. Wang, H. Y. Lee, D. Y. Wu, and M. -J. Tasi, "High Endurance Multi-gate TiN Nanocrystal Memory Devices with High-k Blocking Dielectric and high Work Function Gate Electrode," in *IEEE VLSI-TSA 2008*, pp.62-63. 2008
5. **C.-P. Lu**, C.-K. Luo, B.-Y. Tsui, C.-H. Lin, P.-J. Tzeng, C.-C. Wang, and M.–J. Tsai, "Multi-Gate Metal Nano-crystal Memories with TiN Nano-crystals, High-k Blocking Dielectric and High Work Function Gate Electrode," in the *2008 Int. Conf. on Solid State Devices and Material*, pp.824-825, 2008.
6. B.-Y. Tsui, S.-H. Liu, and **C.-P. Lu**, "Evolution of Schottky Barrier MOSFETs," in Proc. of the 16th Symposium on Nano Device Technology, 2009.

7. M. Schimidt, **C.-P. Lu,** H. D. B. Gottlob, and H. Kurz, “Metal gate electrode for rare earth oxide high-k dielectrics,” in *2009 IEEE International Conf. on Signals, Circuits and Systems (SCS’09)*, pp.1-5, 2009.
8. B.-Y. Tsui, C.-C. Yen, P.-H. Li, **C.-P. Lu**, J.-Y. Lai, “Extreme Ultra-Violate Exposure Induced Damages on Non-Volatile Memories,” in *the Proc. of the 2010 IEEE Silicon Nanoelectronics Workshop*, pp.143-144, 2010.
9. **C.-P. Lu,** H. D. B. Gottlob, M. Schimidt, and H. Kurz, “Integration of ALD AlN Work Function Tunning Layers,” in IEEE *VLSI-TSA 2010*, pp.92-93, 2010.

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國立交通大學電子研究所碩士班　　92 年 9 月-93 年 7 月

國立交通大學電子研究所博士班　　93 年 8 月-99 年 8 月

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榮譽：

第一屆聯華電子(UMC)學生獎

98 年行政院國科會與德國學術交流總署三明治計畫獎學金

博士論文題目:

具多閘極之修正蕭基位障電晶體及氮化鈦奈米晶粒記憶體之研究

A Study on the Modified Schottky Barrier (MSB) FETs and TiN Nanocrystal Memories with Multi-Gate Structure