國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

運用於射頻系統封裝應用之異質整合技術開發

Development of Heterogeneous Integration Technology for RF System-on-Package Applications

研 究 生：趙子元

指導教授：鄭裕庭 教授

中華民國 一〇一 年 二 月

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研究生：趙子元　　Student：Tzu-Yuan Chao
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電子工程學系　電子研究所
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摘　　要

在不久後的將來，由於材料特性與元件結構的自然限制，矽基互補式金屬氧化物半導體(CMOS)技術的持續微小化將不再遵守摩爾定律(Moore’s Law)之預測而達到其終點。例如，當通道長度低於9奈米時，金氧半場效電晶體(MOSFET)將表現出較大的漏電流從而導致功率消耗之增加。相較於CMOS技術的微小化，在微電子系統的發展中，一個新興的技術趨勢在於實現超越摩爾定律(More than Moore)之目標，對於未來微電子系統的效能提升，主要將集中於系統整合之技術發展而非電晶體密度之增加來創造高附加價值與功能多樣化之微電子系統。因此，系統封裝(SOP)將成為一個非常重要的技術發展方向來整合CMOS與non-CMOS元件，例如無線被動元件、感測器與制動器、微流道…等，於一個單一封裝體之中。此篇博士論文之目標即為開發應用於下一世代高效能、低成本智慧型系統製造的射頻系統封裝(RF SOP)之關鍵技術發展。憑藉著系統封裝的優點可進一步將現有組裝了大量元件的龐大電路板縮小在一個微型封裝基板中，此優點伴隨著一個技術挑戰，其技術難度在於如何整合所有的CMOS晶片於封裝基板之上並且具有低損耗與低寄生效應的連接特性，特別是在射頻系統整合方面，為了克服這個困境，在此論文中首先提出用於異質晶片整合(Heterogeneous chip integration)之金-金熱壓接合(Au-Au thermocompressive bonding)技術，此技術可以提供一個低損耗的連接而不需要在電性轉接結構上採用複雜的結構設計或額外的阻抗匹配，從DC到50GHz頻率範圍可具有低於-15dB的返回損失及-1.8dB的插入損失。為了展現此連接技術在射頻微機電異質晶片整合的可行性，一個低功率射頻低雜訊放大器(Low noise amplifier)藉由

整合 TSMC 0.18-μm RF CMOS 晶片與製作有高品質因子微機電式電感(high-*Q* MEMS Inductor)的矽載具(Si carrier)被提出來，此連接技術與矽載具系統封裝應用方案也可以使用在其他微電子封裝應用，例如：軟性電子，光電，微機電系統…等。

在此論文中，軟性電子應用(Flexible electronics)是另一個研究主題之概念展示。以軟性微電子整合為例，首先提出了先進 SU-8 微加工製程來展現嵌入元件在軟性基板的可行性，利用此製程可使製作微機電串聯式切換器(MEMS serial switch)之製程溫度低於 135°C。提出之 SU-8 微機電切換器為靜電力驅動之兩端固定 SU-8 樑結構，高頻特性方面在 12GHz 可提供-28.2dB 之高隔離度，若製作於 100Ω·cm 之矽晶圓之上由於降低了基板損失則預期具有低於-0.75dB 之插入損失。此外，與先前矽基射頻系統封裝概念相同，吾人發展並提出一個低成本晶圓級軟性微系統整合技術來實現軟性射頻系統封裝，此技術合併先前開發之無凸塊射頻系統封裝連接方案與特殊的表面清潔製程來達成接合溫度低於 200°C 之 CMOS 晶片組裝於 SU-8/PDMS 有機基板之上。射頻轉接結構在有機基板上同樣展現低損耗的特性，在 40GHz 有大約-15dB 返回損失與-0.8dB 插入損失。此外，相同的整合製程被利用來整合生醫矽探針與 SU-8 軟性帶狀排線以提供可靠的信號傳輸至人體外部之讀取設備。同時，利用金化學惰性的優點，晶圓級犧牲層釋放製程也被提出來實現未來低成本批次製造之軟性微系統。

除了組裝晶片於封裝基材之上，在射頻系統封裝的進展上，發展高效能嵌入式被動元件是非常關鍵的，因此，在論文的最後部分，吾人研究並提出整合鐵磁性鐵芯之晶片式螺旋電感，晶片式電感被大量使用於射頻積體電路(RFIC)的設計上，然而，電感通常佔據大部分矽晶片之面積且無法隨著 CMOS 技術的進步而縮小，同時，電感的性能會受到如導體結構的電阻損耗(resistive loss)與矽基板損耗(substrate loss)等自然限制，因此吾人提出合併磁性奈米複合材料，包括鎳-磷-陽極氧化鋁(Ni-P-AAO)與鎳鐵-陽極氧化鋁(NiFe-AAO)材料，來作為晶片式電感之感應鐵芯以提升電感值，使用 NiFe-AAO 奈米複合磁性鐵芯之螺旋電感在 GHz 頻率可提升約 25%之電感值並且沒有大幅的品質因子降低，本論文將提出相關磁性奈米複合薄膜之詳細實驗流程與奈米複合電感之整合製程與量測討論。

Development of Heterogeneous Integration Technology for RF System-on-Package Applications

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ABSTRACT

In the near future, the continuous downscaling of Si-based CMOS technology will not follow the Moore's Law and would reach its endpoint owing to the nature limitation of the material property and device structure. For instance, MOSFET channel lengths below 9 nm will exhibit higher leakage currents leading to increased power consumption. Instead of the CMOS scaling, an emerging technology trend in the development of microelectronics system is aimed to realize the goal of "More than Moore", indicating the future performance improvement of an microelectronic system would mainly focus on the technology of system integration rather than transistor density increase for creating high value and functional diversification of microelectronics systems. Thus, the integration of CMOS and non-CMOS based components, such as wireless passive components, sensors and actuators and microfluidic channel and so on, within a single package, i.e. system-on-package (SOP), would

become an important technology development direction. The objective of the dissertation is to develop the key technologies of radio frequency SOP for the next generation high performance and low cost smart system fabrication. The virtue of SOP is aimed to further shrink a bulky circuit board assembled with components into a miniature packaging substrate. The virtue would come with a technical challenge which is the difficulty in the integration of a packaging substrate with all CMOS chips with low loss and low parasitic of interconnections, especially in RF system integration. To overcome this predicament, an interconnecting technology using an Au–Au thermocompressive bond is presented first in the dissertation for the heterogeneous chip integration. This technology can provide a low loss interconnection which is less than -15 dB return loss and -1.8 dB insertion loss up to 50 GHz without implementing complex structure designs and extra impedance matching networks in the electrical transition. A low-power RF low-noise amplifier by integrating a TSMC 0.18-μm RF CMOS chip with a silicon carrier substrate, where high *Q* MEMS inductors are fabricated, is proposed to demonstrate the feasibility of the interconnecting technology for RF MEMS heterogeneous chip integration. Such an interconnecting and the Si carrier SOP application schemes can be also applied to the other microsystem packaging applications like flexible electronics, optoelectronics, MEMS and so on. In the dissertation, flexible electronic application is another subject for the concept demonstration. For the case of flexible microsystem integration, a novel SU-8 micromachining process for MEMS series switch fabrication with processing temperature lower than 135°C is presented first to show the feasibility to embed devices in a flexible substrate. The proposed SU-8 MEMS switch is designed with a clamped–clamped SU-8 beam structure driven by electrostatic force. The switch can exhibit better than −28.2 dB isolation up to 12 GHz and expect to have −0.75 dB insertion loss as long as the substrate resistivity is increased up to 100 Ω·cm resulting in lower substrate loss. Then, a low-cost wafer-level flexible microsystem integration technology is developed and presented for the ultimate realization of flexible RF SOP same concept as the prior Si-based RF SOP. The technology combines the previously developed bumpless RFSOP interconnection scheme with a special surface cleaning process to assemble a CMOS chip with an organic substrate (SU-8/PDMS) that the bonding temperature less than 200°C. The RF transition on the organic substrate also provides a low loss performance about -15dB return loss and -0.8dB insertion loss at 40GHz. In addition, the same integration process is utilized to integrate the biomedical Si probe with an SU-8 flexible ribbon cable for providing a reliable signal transmission to the instrument reader outside human body. Meanwhile, by taking advantage of chemical inertia of Au, a wafer-level sacrificial release process is also proposed and performed for future low-cost batch fabrication of flexible microsystem. In addition to the assembly of chips onto a packaging substrate, developing high performance embedded passive components is very critical in the advancement of RF SOP technology. Thus, in the last part of the dissertation, on-chip spiral inductor with ferromagnetic core is developed, investigated, and presented. On-chip inductors have been extensively used in the design of Radio Frequency Integrated Circuits (RFICs). It, however, occupies a large silicon chip area which cannot be scaled with the advancement of CMOS technology. Meanwhile, the performance of the inductor suffers with its nature limitation owing to resistive loss of its conducting structure and silicon substrate loss. An inductance enhancement scheme is then proposed to incorporate magnetic nanocomposite materials including Ni-P-AAO and NiFe-AAO with on-chip inductors as the inductive cores. The spiral inductor using a NiFe-AAO nanocomposite magnetic core can have more than 25% inductance enhancement without tremendous *Q* degradation to GHz range. The detail experimental procedures of synthesis and characterization of magnetic nanocomposite films, the integration process of nanocomposite inductors, and the related measurements and discussions are all presented in this dissertation.

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Chapter 1 Introduction

1.1 Overview

Nowadays, there has been an emerging technology trend in integrating computing, communicating, sensing, biomedical detecting functionality and so on into a portable consumer electronic device. Based on the virtue of consumer products, such an electronic device should come with the characteristics of low cost, low power consumption, small form factor, and high system performance. Therefore, from the integrated circuit (IC) fabrication point of view, it has become an emergent technology challenge to integrate various electronic components including digital, analog, memory, radio frequency (RF), microelectromechanical system (MEMS), and optical circuits…etc. in a compact chip system. Since late 90's, there have been two major technologies, system-on-chip (SOC) [1] and system-on-package (SOP) [2], which have been developed and proposed to pave the way to realize the ultimate goal. According to the Moore's law, recent technology development in semiconductor manufacture has disclosed that the number of transistors that can be integrated on a single chip continues to double every 18 to 24 months. The integration capability has enables an entire system with multifunctional components in a single chip, i.e. SOC, as shown in Figure 1.1 [3]. SOC can not only provides the best performance electronic product owing to the shortest interconnection length between circuit blocks but also the lowest manufacture cost resulted by batch processing. However, truly accomplishing a full SOC product is still underway today since the integration of the distinct circuitries is usually accompanied with different fabrication process and transistor design, and interconnect and layout methodology which would drastically affect the yield of chip manufacture resulted by a dozen of masks. Meanwhile, in terms of the consideration of chip cost and transistor performance, the rationale to fabricate all kinds of circuitries in the most advanced process technology seems debatable. Therefore, it is more practical to integrate the subsystem components based on the scheme of SOP rather than to build an entire SOC, while developing a multifunctional microsystem. Figure 1.2 shows the illustration of the SOP [4], instead of building everything on a single chip, modules of RF transceiver, analog/digital IC, MEMS devices, and optical interconnect…etc. can be fully integrated onto a substrate, or called carrier, to become an integrated system. Various modules or devices can be either individually optimized and fabricated in separate chips without the limitation of material and fabrication process and then directly assembled on or embedded to a single carrier. For that reason, the SOP approach exhibits the characteristics of design flexibility, high performance, short time to market and low manufacture cost so as to become the most effective method to provide a realistic integration solution.

In the recent years, wireless technologies have gained prominence for interfacing the computational devices to the remote host servers owing to the great demand of personal portable devices, such as smart phone and tablet computer [5]. RF front-end module is the foundation of these devices but system integration of the module with the computational components poses a great technical challenge. Previously, much effort has been devoted to the realization of RF SOC using advanced Si CMOS technology since the speed of CMOS transistor has gradually increased with the decrease of transistor size and the chip cost is much lower in comparison with that of GaAs-based monolithic microwave integrated circuit (MMIC). Nevertheless, the performance of RF CMOS circuit is usually limited by low quality factor of on-chip passive components due to substrate loss in low resistivity Si. Meanwhile, RF transceiver also needs lots of discrete passive components on bulky system printed circuit board (PCB), such as surface acoustic wave (SAW) filter, surface mount inductors, capacitors, and resistors, for matching, tuning, filtering and biasing circuitry. For SOC implementation, part of these off-chip discrete components would be integrated onto a RF CMOS chip where these components usually occupy up to 80% of the total transceiver area accounted for ~70% of the cost [2]. Therefore, the concept of SOP can then be applied for the optimization and miniaturization of the RF systems by replacing the on-chip passives and discrete components with high-*Q* integrated passive devices (IPD) in the package carrier. In addition, the RF SOP module can further integrate several RF MEMS devices, such as MEMS switches, inductors and resonators, onto the carrier to replace the conventional passive components owing to its superior RF characteristic applications [6]. Therefore, a miniaturized RF system can be truly realized with more design flexibility and better circuit performance. In this dissertation, several heterogeneous integration technologies have been developed and presented for advancing the RF-SOP applications. The technologies include a broadband low loss interconnection scheme for the chip integration onto a Si carrier [7,8], a sacrificial release process with low temperature flip-chip assembly scheme (<200°C) for organic substrate-based flexible RF microsystem fabrication [9-12], and synthesis and design of magnetic nanocomposite materials for the area reduction of on-chip inductor [13,14].

Digital content-on-demand, such as high-definition videos or 3D movies, has become a must feature of the present handheld products which require a high speed wireless communication technology for data transportation. Therefore, the development of RF system with a higher operating frequency up to millimeter-wave range is required to have a wider bandwidth for enough channel capacity. As aforementioned, RF SOP can provide the most effective approach for high performance module integration. Nevertheless, to realize a high frequency SOP scheme, the design and fabrication of the interconnection between chips and packaging carrier is a critical research topic. A good interconnection should exhibit good return loss and low insertion loss in a wide-frequency range; so that it won't degrade CMOS chip performance. For high frequency interconnection application, flip chip assembly has been widely utilized for chip integration with interconnect lines [15]. However, inevitable structure discontinuity in the conventional flip chip joint can still result in the increase of return loss while the RF frequency is larger than 10GHz or even higher [16]. Si-based System-on-Package (SOP) scheme has been proposed for microsystem fabrication in recent years [17]. Discrete components are designed and fabricated in separate chips then fully integrated onto a silicon substrate to form a microsystem. Using silicon instead of ceramic or printed circuit board (PCB) as packaging substrate can ensure the SOP scheme suitable for high density interconnect application due to perfect coefficient of thermal expansion (CTE) match which will not induce thermal stress to cause reliability problems in chip assembly. The contact size of chip to silicon substrate can be as small as possible [18]. A bumpless interconnecting technology based on the Si-Based SOP scheme is, therefore, developed and presented in the dissertation to provide a broadband low loss interconnecting by minimizing the parasitic effect to conquer the aforementioned large return loss. Based on this technology, an ultra-wideband low noise amplifier (UWB LNA) is demonstrated by integrating RF CMOS chip onto Si carrier with high-*Q* MEMS inductors to exhibit its capability for RF-SOP integration.

In addition to the handheld products, flexible electronics in the applications of wireless body sensing networks (WBSN) and smart sensor tag has revealed another potential market including point of care healthmonitoring, environmental monitoring and homeland surveillance and security…etc. The RF-SOP concept can be also implemented for the miniaturization of high performance flexible sensor tags. Therefore, in the thesis work, several fabrication techniques have been developed and proposed based on the RF SOP scheme for flexible microsystem applications.

One of the technical challenges in the fabrication of flexible microsystem is the requirement of low the processing temperature which should be less than ~200°C due to the low glass transition temperature of organic substrate. Meanwhile, as aforementioned, integrating several RF MEMS devices in a RFIC system can boost system performance. An SU-8 based MEMS switch using organic sacrificial layer is therefore developed first in the dissertation for demonstration of low-temperature fabrication of the MEMS device for flexible wireless microsystem applications. On the other hand, several developed technologies in the realization of a flexible microsystem are usually accompanied with several drawbacks including poor active device performance, low process flexibility, or high manufacturing cost and complexity. To resolve the problem, a wafer-level sacrificial release process based on the SU-8 is then proposed in this dissertation. The process can assemble high performance CMOS chips onto a patterned organic substrates (SU-8) by combining the prior bumpless interconnecting technology with a low-cost surface cleaning process. Thus, various flexible microsystems can be fabricated at one time after metal sacrificial layer removal. In addition, this technology can be also applied for the biomedical applications by providing a mechanical and electrical interconnection between the biomedical Si probe with a flexible SU-8 ribbon cable. Related application will also be included in the dissertation.

As discussed previously, passive components are indispensable in the RF front-end module. Among the passive components, on-chip inductor has been widely used in impedance matching and LC tank circuits…etc. The inductor usually occupies more than 50% area of an RFIC chip. Therefore, numerous researches have been conducted to fabricate area-effective CMOS-compatible magnetic inductors over the past decade because the area reduction of on-chip inductors is the most effective way in comparison with the reduction of the CMOS transistor size in the development of RF microsystems with low cost and small form factors. Inductance represents the ability of an inductor to store energy in a magnetic field. Via the incorporation of ferromagnetic materials, the magnetic flux density, $\vec{B}$, generated by the current source flowing through the inductor, can further be enhanced due to high magnetic permeability, μ, of the magnetic core which can store more magnetic energy. In other words, the stored magnetic energy and also inductance of the inductor with the core is then larger than that of the inductor without the core but the same structure. It is noted that the magnetic materials for the inductance enhancement in such a RF inductor require not only large μ but also high ferromagnetic resonance (FMR) frequency which determines the maximum usable frequency. Thus, in this dissertation, two kinds of magnetic nanocomposite materials with high FMR frequency synthesized with CMOS compatible processes has been characterized and verified for performance enhancement of on-chip inductors and the proposed process can be utilized either for RF SOC or RF SOP applications.

1.2 Organization of the Dissertation

In Chapter 2, a novel bumpless interconnecting scheme using an Au-Au thermocompressive bond is presented for Si-based RF SOP chip integration. The bumpless interconnecting provides a broadband low return loss transition without adapting the complex compensation structure by minimizing the structure discontinuity in the transition. Two testing structures, the DC Daisy chain and RF transition structures are both designed and fabricated for the electrical characterization of the interconnect scheme. Related fabrication process regarding Si carrier fabrication and bonding metallization will be also described in detail. The feasibility of the proposed scheme is finally demonstrated by the promise performance of a low-power RF SOP low-noise amplifier by integrating a TSMC 0.18-μm RF CMOS chip with a silicon carrier, where high *Q* MEMS inductors are fabricated and utilized for good circuit performance.

In Chapter 3, an SU-8-based wafer-level sacrificial release process is presented for flexible microsystem fabrication. The process includes three basic techniques which are SU-8 MEMS fabrication, bonding interface cleaning technique for low temperature flip chip bonding and a wafer-level metal sacrificial release process for SOP-based flexible microsystem fabrication, respectively. The manufacture of flexible microsystem requires to keep the whole process temperature well below the glass transition temperature of organic substrate. Thus, a SU-8 MEMS switch with clamped-clamped SU-8 beam and organic sacrificial layer is first designed and fabricated to demonstrate the integration feasibility of RF MEMS for flexible RF SOP application. The usage of SU-8 instead of PECVD SiO_2 or Si_3N_4 as beam material can keep process temperature below 135°C. Meanwhile, based on the previously develop bumpless Au-Au thermocompressive bond, a surface cleaning treatment on Au surface is then developed to lower the bonding temperature than 200°C with acceptable electrical and mechanical performance for the integration of conventional CMOS chips with the flexible SU-8 substrate. The element composition of Au surface before and after surface cleaning is analyzed. At final, with the cleaning technique, a wafer-level metal sacrificial release process is present to assemble a CMOS chip with an SU-8 flexible substrate. The proposed fabrication scheme can also be used to interconnect MEMS biomedical device with external circuit chips for biomedical application.

A performance enhancement scheme of on-chip spiral inductor using nanocomposite magnetic materials is presented in Chapter 4. Via the integration of magnetic nanocomposite material with the spiral inductor, inductance enhancement can be expected due to the enlargement of stored magnetic energy. Two magnetic nanocomposite materials, Ni-P-AAO and NiFe-AAO, with different synthesis procedure and integration process for fabricating the nanocomposite inductor are developed with a criterion of CMOS process compatible, respectively. The magnetic properties of nanocomposites are characterized by measured hysteresis loop. The influences of magnetic nanocomposites on the inductors performance are discussed from measurement data.

Finally, the conclusions of the developed heterogeneous technologies and the suggestion of future research direction are summarized in Chapter 5. This is belief that the proposed technologies have great potential for next generation RF SOP product manufacture.

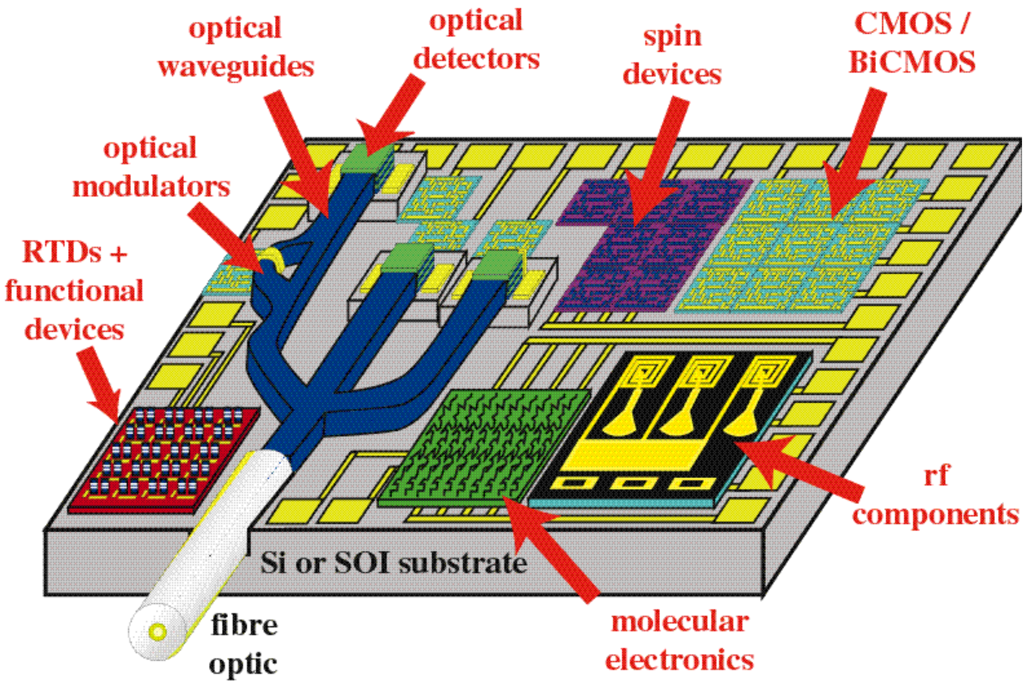


Figure 1.1 The illustration of System-on-Chip (SOC) [3]

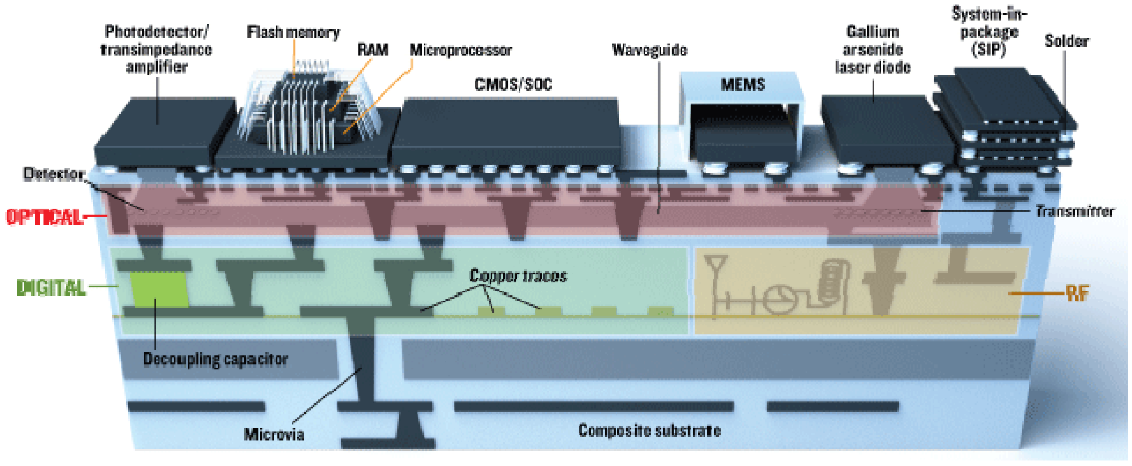


Figure 1.2 The illustration of System-on-Package (SOP) [4]

Chapter 2 An Interconnecting Technology for RF MEMS Heterogeneous Chip Integration

2.1 Introduction

Process integration is a critical research topic in the development of micromechanical circuitry for wireless communication applications [19–22]. From surface, bulk, to CMOS-microelectromechanical system (CMOS-MEMS) micromachining processes, the tradeoff among device performance, material selection, process compatibility, and manufacture cost is required in design consideration while the machining techniques are employed for MEMS fabrication. For example, Nguyen and Howe [19] presented the first integrated high Q MEMS CMOS oscillator showing the potential of RF MEMS for low-power wireless communication applications. The work must utilize all tungsten interconnects for surviving in a post-CMOS poly-Si surface micromachining process with a processing temperature up to 835°C. The nonstandard CMOS interconnect material with high electrical resistivity makes the approach not practical for the technology continuation of CMOS scaling. Weigold *et al.* [20] developed a merged process to integrate thick single-crystal Si resonators with a bipolar CMOS (BiCMOS) circuit for having high intrinsic Q factor performance. Deep silicon doping, i.e., 15 μm in depth, which is not an economical BiCMOS process, is required for etching stop in the ethylenediamine pyrocatechol (EDP) release process. Although Lakdawala *et al.* [21] and Oz and Fedder [22] demonstrated a series of monolithic RF integrated circuits using MEMS-type passives fabricated by a standard CMOS process, only the backend aluminum and aluminum-oxide layers can be utilized as structural materials of RF MEMS components. Inevitable stress compensation and material property limitation would complicate the device design. In comparison with the integration approaches, post-CMOS electroforming techniques [23,24] might be an ultimate integration solution of RF CMOS-MEMS with several process advantages, including flexible material choice, low process temperature, and high manufacturing throughput. Mechanical deficiencies of metal-based materials, such as fatigue, aging, and low stiffness, still need to be resolved as the structural material of MEMS devices [25–27]. Therefore, it is critical to develop an integration scheme with the least tradeoff design for RF CMOS-MEMS fabrication.

Meanwhile, Si-based system-on-package (SOP) schemes have been proposed for microsystem fabrication in recent years [17,18,28,29]. Instead of building everything on a single chip, discrete components are designed and fabricated on separate chips and then fully integrated onto a silicon substrate to form a microsystem. A compact microsystem can be realized with the design flexibility without having any material and process limits for better performance. In addition, using silicon instead of ceramic or a printed-circuit-board (PCB) material as the packaging substrate can ensure the SOP scheme to be suitable for high-density interconnects due to a perfect coefficient-of-thermal-expansion match, which will not induce thermal stress to cause reliability problems in chip assembly. The contact size of the chip-to-silicon substrate can be reduced to several tens of micrometers in diameter [18]. Thus, a heterogeneous chip integration scheme, as shown in Figure 2.1, is presented by adapting the SOP concept to integrate a CMOS circuit chip with a micromachined silicon carrier, where high-performance RF MEMS components are fabricated.

Previously, Carchon *et al.* [29] successfully demonstrated a similar silicon-based multi chip module-deposited (MCM-D) technology for the integration of 0/1-level packaged RF-MEMS devices at millimeter-wave frequencies. Although this paper had shown excellent RF characteristics in the integration of a silicon substrate with an RF MEMS chip, most of research works were merely concentrated in the performance study of connected RF passive components without involving in any active CMOS circuit, which is, however, the most critical component in the development of RF MEMS for wireless transceiving system applications. In comparison with the MCM-D technology using Au-stub interconnects, better system performance with more design flexibility can be further expected in the realization of RF CMOS-MEMS since the scheme proposed here for multiple chip integration is aimed at a system structure with the interconnect configuration similar to that of a system-on-chip (SOC). Nevertheless, in the heterogeneous chip integration scheme, a flip-chip (FC) bonding technique is the key to achieve chip assembly with better interconnect performance. The conventional FC technology like Carchon *et al.*'s approach has been widely utilized for microelectronic packaging applications because it can enable the electrical interconnects between chips to have high-density and low parasitic reactance characteristics. However, large solder bumps for the interconnects still exhibit no negligible parasitic effects. While the device size continues to shrink, the parasitic effect can cause large sensitivity reduction of devices. While the frequency of the electrical signal transmitted within chips is greater than 10 GHz or even higher, the parasitic effect will result in the drastic increase in return loss in the interconnecting transition. Therefore, a bumpless bonding technique must be developed and implemented in the proposed integration scheme to further reduce the bump size effects for having an interconnection with low loss, wide bandwidth, high speed, and ultrafine pitch characteristics [15,30,33].

Previously, several bumpless interconnecting and microbumping concepts have been developed and implemented in the FC technology [15,30–33]. Saito et al. [32] utilized the surface activated bonding (SAB) [30,31] to realize high-density bumpless interconnection from a Si chip to a polyimide substrate in which a pad loss at 20 GHz will be about 1/20 of that of wire bonding. In 2006, the same group also demonstrated Si-to-Si bumpless ultrafine pitch interconnects using the Cu SAB technique in which about 0.1-μm bump height and less than 10-μm pitch can be achieved [33]. The mechanism of SAB is based on the adhesive force formed by two atomically clean surfaces with intimate contact. The clean surfaces must be formed by a chemical–mechanical planarization process combined with the Ar fast atom beam (Ar-FAB) or Ar plasma irradiation treatment in an ultrahigh vacuum environment. Since the SAB has the characteristics of low process uniformity tolerance, long activation time (~30 min), and special customized tool requirement, it is difficult to be implemented for mass production. IBM Research demonstrated a controlled collapse chip connection (C4) microbump interconnect technique, which can provide conventional Pb and Pb-free solder bumps with ~10 μm bump height, 25 μm in diameter, and 50 μm pitch size at the wafer level (200 mm) by an electroplating method [15]. The contact resistance can be achieved as low as several milliohms depending on the type of the solder material used for the microjoint. However, the microsolder bumping process requiring electroplating is generally the last process step that could raise the process integration problem for most of MEMS chips.

In this chapter, a bumpless interconnecting technique is presented based on a self-interlocking design with a Au–Au thermocompressive bond for realizing the proposed heterogeneous chip integration scheme. A low-power RF low-noise amplifier (LNA) is designed, fabricated, and utilized to demonstrate the technology feasibility by integrating a TSMC 0.18-µm RF CMOS chip with a silicon carrier where high Q MEMS inductors are designed and fabricated in-house. In comparison with the aforementioned interconnecting technologies, a near-zero bump height and a post-CMOS compatible process without solder bumping on the CMOS chip can provide a total solution not only to the characteristic impedance matching problem raised in electromagnetic (EM) signal transmission between RF circuits but also to the heterogeneous chip integration of RF MEMS fabricated by different fabrication processes.

2.2 Bumpless Interconnecting Scheme

Figure 2.2 shows a typical FC transition from one interconnect line on a chip to another on a PCB and the corresponding equivalent circuit model, respectively [16,34,35]. The lump elements L_S, R_S, C_M, C_C, G_M, and G_C are the bump inductance, the radiation loss resistance in bump [34], the discontinuity capacitance at the PCB and the one at the chip, and the substrate loss conductance of the PCB and that of the chip, respectively. In general, series resistance R_S and shunt conductance G_M (G_C) are small enough to be neglected; the effective bump impedance can be calculated as follows:

$$Z_{bump} = \sqrt{\frac{L_S}{C_M + C_C}} \tag{2.1}$$

In the FC transition, the structure geometry and parasitic discontinuity capacitance C_M and C_C would lead the transition with a capacitive dominant characteristic, which results in a low bump impedance smaller than the system characteristic impedance of 50 Ω. Wang and Wu [16] estimated that the effective bump impedance of a typical FC structure with 127 μm in bump height, 160 μm in bump diameter, and 200 μm in pad size is about 32 Ω, where series inductance L_S and shunt capacitance C_M (C_C) are 68.67 pH and 34.91 fF, respectively. To solve the 50 Ω matching problem resulted by the FC transition, several compensation structures like the staggered structure [36], high impedance line [37], and ground retreat [16] have been applied to reduce excessive capacitance of the transition and to make the FC transition with a 50 Ω impedance for lowering return loss. On the other hand, bumpless interconnecting is an alternative approach enabling the FC transition to have almost zero bump height and tiny bump pad size that can be reduced down to several micrometers. L_S and C_M (C_C) can be further neglected by the reduction of inductance and fringing capacitance, and the impedance of the FC transition will become negligible in the two connected 50 Ω transmission lines at a low frequency. To minimize the transition impact to the two connected transmission lines, the bumpless interconnecting can also simply reduce the return loss of the transition without adapting the complex compensation structure requiring customized design.

Figure 2.3 shows the scheme of the proposed self-interlocking bumpless interconnecting technology. As aforementioned, the silicon carrier can be fabricated using either the same as or different from standard CMOS processes for having good process design flexibility in terms of the performance consideration of MEMS devices. For a standard CMOS chip, Si_3N_4 or polyimide will be deposited last on the top of CMOS circuitry as a passivation layer to prevent possible contamination, damage, and corrosion. For example, a TSMC 0.18-μm mixed signal CMOS chip has a 1 μm altitude difference between the top surfaces of the Al contact pad and the passivation, as shown in Figure 2.4. Concave pad structures with the same step height generally form on the top of the chip, and solder balls are, conventionally, put inside the pads and utilized as metallurgical and electrical connection for chip assembly. This dissertation presents an alternative joint scheme, as shown in Figure 2.3, where one end of the concave pad structures is removed first (chip A), the signal line, i.e., the electrical interconnect line, on the other chip (chip B) is opened, and then the electrical joint is achieved by mechanically interlocking and bonding the pads with the lines using a Au–Au thermocompressive bond to make two chips become a "single" chip. The interlocking mechanism can effectively prevent the metal interconnect line from the horizontal shift to be blocked by the edge of the concave pad, particularly when two chips are bonded on an unleveled bonder stage. Thus, the design rule for the interconnect line in a silicon carrier and the contact pad on a CMOS chip is determined based on the alignment accuracy provided by an FC bonder. For instance, the width of the contact pad is larger than the width of the interconnect line by 2 μm, which is two times larger than the maximum misalignment distance of the bonder used in this work. Because the metal lines on a chip can be directly connected with the contact pads, the characteristics of almost zero bump height and similar signal line width between chips can allow a high-frequency EM signal to directly pass through the metal joint with the lowest power loss due to diminutive characteristic impedance mismatch and parasitic effects resulted by the minute structure discontinuity.

Several issues need to be addressed in the proposed bumpless interconnecting technology. First, all contact pads of the CMOS chip should be designed and located on the periphery of the chip. Second, either a blade or laser dicing process must be employed to remove the edge of the chip, so that one end of the contact pads can be opened. Third, because the contact pad and the metal line of a CMOS chip are either made of Cu or Al determined by the process node chosen for the CMOS chip fabrication, a metallization process and related electrical characterization must be developed for the chip assembly. At last, a Au–Au thermocompressive bond and related metallization processes must be developed and utilized as the last processing step to realize the proposed interconnecting technology.

2.3 Test Structure Design

2.3.1 DC Contact and RF Transition Structure

Firstly, the DC electrical contact resistance of the Au–Au thermocompressive bonding is characterized using the test structure, i.e., the Daisy chain, as shown in Figure 2.5. The Daisy chain is fabricated using the Cu plating and metallization processes. Ten corresponding bonding pads with complementary conducting lines are both designed on two separate chips [Figure 2.5(a) and (b)]. Thus, the total contact resistance can be obtained by subtracting the resistance of the line pattern [Figure 2.5(c)] from the resistance measured from two contact pads, A and A′, once the two chips are bonded. The contact resistance for each bonding pad can be derived by dividing the total contact resistance by the total number of bonding pads.

For most of the RF SOP schemes, it is a common feature to bond a circuit chip with a substrate carrier in which high-performance passives, including capacitors, inductors, and filters, are fabricated [38–40]. To electrically bridge the two chips, a transition structure from a CPW to a microstrip line and related RF characteristics are critical to the design of the RF SOP. Therefore, as shown in Figure 2.6, an electrical transition from CPWs to microstrip lines, which are designed and fabricated on a silicon carrier substrate and a TSMC 0.18 μm RFCMOS chip, respectively, is utilized to verify the effectiveness of the proposed bumpless interconnecting technology.

The microstrip line on CMOS chip consists of the top metal layer (M_6) as the signal line and the bottom metal layer (M_1) as the ground plane. Based on the standard layer structure of 0.18 μm 1P6M CMOS technology, the width of signal line which is only adjustable parameter is set as 10.5 μm to obtain 50 Ω characteristic impedance. In order to connect ground references on the chip with that on Si carrier as the chip is flipped, vias are therefore required to connect the M_6 ground pads to the M_1 ground layer in the microstrip line on the CMOS chip. Regarding the substrate carrier part, probing pads and CPWs are designed and fabricated on a silicon substrate using the Cu electroplating technique for RF characterization. Here, the characteristic impedance and signal line width of CPWs are designed the same with microstrip line for smooth transition, which are 50 Ω and 10.5 μm, respectively. The gap size of the CPW line is set as 7.2 μm based on the assumption of 10 S/m substrate conductivity. The shape of CPW grounds is tapered near the interface to have better smooth current and continuous filed distributions in order to reduce signal power loss.

2.3.2 Ultrawideband Low-Noise Amplifier (UWB LNA) and Si Carrier Design

In the present RF receiver architecture, an LNA is usually the first signal processing circuit right after an antenna receives an RF signal. The implementation of high Q inductors in the LNA can greatly improve the circuit performance like low power, low noise, high gain, and high tuning range [41,42]. Previous investigations have shown that MEMS inductors can also exhibit high Q characteristics on a silicon substrate using a silicon micromachining technique to effectively reduce ohmic and eddy current losses [43,44]. Thus, a low-power RF LNA is designed, fabricated, and utilized to demonstrate the heterogeneous chip integration technology by integrating a TSMC 0.18 μm RF CMOS chip with a silicon carrier, where high Q MEMS inductors are designed and fabricated in-house. Figure 2.7 shows the scheme of the LNA circuit where four high Q MEMS inductors, i.e., L_1, L_2, L_g, and L_{d1}, are employed to improve the circuit performance. On the input side, a three-section bandpass Chebyshev filter configuration consisting of L_1, L_2, L_g, L_s, C_1, C_2, C_{ex} and C_{gs} of M_1 is adopted for broadband input impedance matching. The three MEMS inductors L_1, L_2, and L_g are used to decrease the thermal noise due to small parasitic resistance. At tunable load, another inductor L_{d1} at the tunable LC resonator is used to provide high power gain and to maintain good gain flatness as a result of the wideband performance in terms of a high Q factor. Circuit simulation by Advanced Design System (ADS) shows that the LNA can have about 50% power savings and 50% tuning range enhancement in comparison with the LNA circuit using the conventional CMOS inductors [45]. The layout of the silicon carrier is shown in Figure 2.8. The silicon carrier is designed with high Q MEMS inductors [43], reference ground, signal pads, and bypass capacitors. All the ground pads are connected together to have the same reference plan for the chip die and the carrier. The I/O probing pads, including two GSG pads and two PGP pads, are fabricated on carrier for measurement. By the way, the metal multi-finger capacitor offers larger bypass capacitance between V_{tune} and ground. It should be noted that the V_{gs} pad was augmented in scale to raise the by-pass capacitance. In order to minimize the unwanted transmission line effect at high frequencies, the multi-finger capacitor was not applied between V_{gs} and reference ground and was replaced with a large parallel capacitor.

2.4 Fabrication Process

2.4.1 Bonding Metallization

The process for the metallization of contact pads is described as shown in Figure 2.9. The metallization for the bonding is a maskless process. First, double-zincating processes on the Al pads of the CMOS chip are performed in a 5% diluted zincating-based solution for 30 and 60 s, respectively, at room temperature. Before starting the secondary zincating process, the Al pads should be put into a 10% diluted nitric acid for 30 s to remove the first Zn layer formed on the top of the pads. The purpose of double zincating is to deposit a uniform Zn layer on the Al pad for being a catalytic and adhesion layer for following electroless Ni deposition [46]. After the zincating process, serial electroless plating processes of 0.2 μm Ni and 0.4 μm Au are performed at 80°C and 88°C, respectively. Finally, blade dicing is performed on the CMOS chip to remove the edge of bonding pads. Once the contact pads are opened, the chip is ready for following Au–Au thermocompressive bonding. It is noted that because several advanced CMOS processes have used Cu instead of Al as the material of metal interconnects and contact pads, the metallization will be slightly different from the previous one. Instead of double zincating, the chip is firstly put into a Pd catalyst solution for 30 s to activate the surface of Cu pads. In the process step, Pd is deposited on Cu pads as the catalyst seed for following electroless Ni plating. After seeding, the Ni and Au electroless deposition processes, same as the aforementioned one, are performed for having a layer of 0.2 µm Ni/0.4 µm Au on the Cu pads for the following bonding process. Figure 2.10 shows the enlarged view of contact pads on the CMOS chip right after Ni/Au metallization and blade dicing. The SEM picture shows that the contact pads are uniformly coated with a Ni/Au layer and have smooth surface morphology for following bonding.

2.4.2 Si Carrier Fabrication

Figure 2.11 illustrates the fabrication processes of the silicon carrier. The fabrication begins with 0.7 µm wet oxidation on a p-type Si wafer, followed by 0.7 µm low-pressure chemical vapor deposition (CVD) Si_3N_4 and 0.7 µm plasma-enhanced CVD tetraethoxysilane SiO_2 deposition as an electrical insulation layer. A layer of Ti (10 nm)/Cu (90 nm) is then sputtered onto the silicon substrate as a seeding layer for Cu electroplating, as shown in Figure 2.11(a). Figure 2.11(b) shows that a 6 µm thick AZ-4620 photoresist is coated and patterned on the top of the electrical insulation layer as a mold structure for 5 µm thick electroplated Cu to make the coil part of the spiral inductor. After the first layer of Cu plating, a 10 µm AZ-4620 is coated, patterned, and sputtered with another 120 nm Cu seeding layer, as shown in Figure 2.11(c), for the air-bridge Cu via filling. Figure 2.11(d) shows that another 10 µm AZ-4620 is then utilized to be the mold for 5 µm Cu plating for the air-bridge fabrication of the inductor. The fabrication of the spiral inductor is done after stripping the photoresist and the seeding layer by acetone, CR-7T, and buffered oxide etchant, respectively, as shown in Figure 2.11(e). Once the inductor is fabricated, the bonding pads will be metallized by serial electroplating processes of 1 μm Ni and 0.4 μm Au as described in the previous Cu pad metallization for bonding. For high *Q* performance, the Si under the inductors is removed to reduce eddy current loss. Figure 2.11(f) shows that the $SiO_2/Si_3N_4/SiO_2$ membrane in the center of inductors is reactive ion etched to expose Si for following XeF_2 isotropic etching. Finally, the photoresist mask is stripped by acetone, as shown in Figure 2.11(g).

2.5 Results and Discussions

2.5.1 Bumpless Interconnect Bonding

Figure 2.12 shows the micrographs of the CMOS chip before and after being diced and the as-fabricated silicon carrier, respectively. The dashed lines in Figure 2.12(a) indicate the dicing traces that are cut for bonding, as shown in Figure 2.12(b). The reference plane is defined at the edge of contact pads using thru-reflect-line (TRL) calibration [47] for RF characterization, as shown in Figure 2.12(c). The air bridge between two grounds is used to inhibit odd-mode excitation in the CPW. The CMOS chip and the Si carrier, which contain microstrip lines and CPWs, respectively, are bonded together under the conditions of 300°C at the carrier, 180°C at the chip, and 50 MPa applied pressure for 3min.

Figure 2.13 shows the SEM photographs of the chip-to-carrier assembly. An enlarged view of the SEM picture on the bonding interface shows that there is about 2 μm misalignment. The misalignment is caused by the malfunction of interlocking resulted by the overplating of Zn/Ni/Au layers on the Al pad. Such a malfunction can be further resolved by a better process control. After forcefully pulling the bonded CMOS chip away from the Si carrier, it is found that a cross-alignment mark on the carrier is totally transferred and attached onto the CMOS chip [Figure 2.14(a)], or the Cu line deposited on the carrier can be lifted [Figure 2.14(b)]. The results indicate that the Au–Au thermocompressive bond is strong enough to break the interface between Ti and SiO_2, which is about 100 MPa [48].

2.5.2 Electrical Characterizations of the DC Contact and the RF Transition Structure

The DC contact resistance is measured using DC probe station and Keithley 2000 multimeter. The contact resistance is calculated as aforementioned which is about 14±5 mΩ for each circular bonding pad of 0.4 μm Au/1 μm Ni with a radius of 20 μm. Since the contact resistance is about two orders smaller than equivalent series resistance of inductor, it doesn’t have to take into account of DC ohmic loss at interconnection joint in RF SOP integration design.

Two-port S-parameters of the transition structure are measured using Agilent E8364B PNA and Cascade Infinity GSG probe in the frequency range from 10 to 50 GHz, as shown in Figure 2.15. The measured S-parameters have excluded the parasitic effect from measurement pads and have a reference plane to the edge of the bonding pad via TRL calibration. The assembly technique provides about −1.7 dB insertion loss and −15 dB return loss at 40 GHz, including the transmission loss of the microstrip line. After detail investigations, the discrepancy from the simulation results and the measurement results might be due to underestimate of substrate conductivity in the carrier. From the measurement results of the CPW, the conductivity of the Si substrate is extracted as 75 S/m, much higher than the initial assumption of 10 S/m. This higher silicon conductivity will cause CPW become lower characteristic impedance and more dispersive, but Z_0 of the microstrip line is still kept around 50Ω. High substrate conductivity also contribute more signal loss to flip-chip interconnect due to propagate of EM fields in the lossy substrate. The revised high-frequency structural simulation at 75 S/m silicon conductivity shows comparable S_{11} and S_{21} values as compared with the measurement result. Nevertheless, the measurement result has revealed that the low loss and wide bandwidth characteristics of the bumpless interconnecting technology have the potential for RF chip integration.

2.5.3 UWB LNA with MEMS Inductors

Figure 2.16 shows the SEM picture of the as-fabricated LNA circuit using the proposed bumpless chip assembly technique. Figure 2.17 shows the comparison between simulated [Figure 2.17(a)] and measured [Figure 2.17(b)] S_{11} and S_{21} with a different tuning voltage in the LNA circuit. There are discrepancies in S_{11} and gain degradation. The bandwidth of measured S_{11} is narrower than that of the simulation one and varied with the tuning voltage. The discrepancy could be caused by EM field coupling within inductors, which would result in input mismatch. The proximity and interconnect trace of inductor can cause the coupling between coils. In terms of LNA circuit design, the four MEMS inductors on Si carrier are individually designed in HFSS at the beginning, so the proximity effect is not considered in the initial design. After made effort to debug, the measurement result can be verified by full-layout simulation as shown in Figure 2.17(c). The effect, in fact, can be resolved by adding guard rings around the inductors for the enhancement of EM signal isolation and by removing more Si underneath the inductors for *Q* enhancement to realize higher gain performance.

2.5.4 Discussions

Although the function of self-interlocking was not fully demonstrated in this experiment due to the overplating of the Zn/Ni/Au layer on the CMOS chip, it can be resolved by process optimization. Nevertheless, it is noted that Ni, in the bonding scheme, not only plays a role as a seeding layer for following Au plating but also acts as a diffusion barrier to Au. In this work, the Au–Au thermocompressive bond is chosen to realize bumpless interconnecting unlike the under-bump metal (UBM) of the packaging, where the Au layer is only used as a wetting layer to the solder for FC bonding. Thus, to effectively prevent Au from diffusing into a CMOS chip, to have a strong Au–Au bond, and to maintain self-interlocking mechanism, further process characterizations, including the thickness control of the Ni/Au metallization and related bonding quality and reliability investigation, are required for having an optimal process condition for manufacture applications. In fact, in comparison with the other two kinds of Au–Au thermocompressive bonding techniques proposed for FC applications, i.e., the Au bump and the Au stud bump, as listed in Table 2.1 [49,50], the presented Ni/Au bumpless metallization for Au–Au thermocompressive bonding has shown a great potential in chip integration with the characteristics of high throughput, flexible bump geometry and pitch size, low cost without a lithography process, and almost zero bump height for high-frequency signal transition. In addition, the previous study has shown that the electromigration of a typical Pb-free solder using Ni-P/Au UBM is mainly caused by the movements of Sn atoms against the electron flow [51]. Since there is no Sn solder required in the bonding scheme, a better electromigration characteristic can be expected.

The bumpless interconnecting technology can provide low parasitic capacitance and small contact resistance for chip assembly and make the electrical joint behave like a simple interconnect line, which can reduce IC design complexity, provide process flexibility, and make the whole system perform like the SOC. Thus, in addition to MEMS inductors, RF MEMS components, such as switches, tunable capacitors, inductors, antennas, and BAW resonators, can be easily implemented for RF microsystem fabrication based on the heterogeneous chip integration scheme with the bumpless interconnecting technology. Although this work only demonstrated an integration of a CMOS chip to a silicon carrier, the scheme can be utilized for a CMOS chip to a CMOS chip, a MEMS chip, or a III–V chip integration, and to provide an alternative technique for heterogeneous integration applications without modifying the existed chip design. Owing to the intrinsic characteristic of heterogeneous chip integration, the scheme can further ensure a cost-effective CMOS-MEMS fabrication process without sacrificing system performance as the scaling of CMOS technology is down to 90 nm or even further.

2.6 Summary

In this chapter, a bumpless interconnecting scheme has been presented for MEMS heterogeneous chip integration based on the developed Au–Au thermocompressive bonding. The scheme can fully integrate a CMOS chip with another chip, which can be another CMOS, MEMS, III-V, or silicon carrier chip. The dc and RF electrical behaviors of the bumpless interconnect have been characterized and have shown good broadband transition performance. A low-power broadband LNA circuit has been realized using the bumpless interconnecting technology to fully integrate a TSMC 0.18 μm RF CMOS chip with a silicon carrier where high *Q* MEMS inductors and CPWs are fabricated in-house. With a better layout design and process optimization, the technology has shown its great potential for RF MEMS heterogeneous chip integration applications.

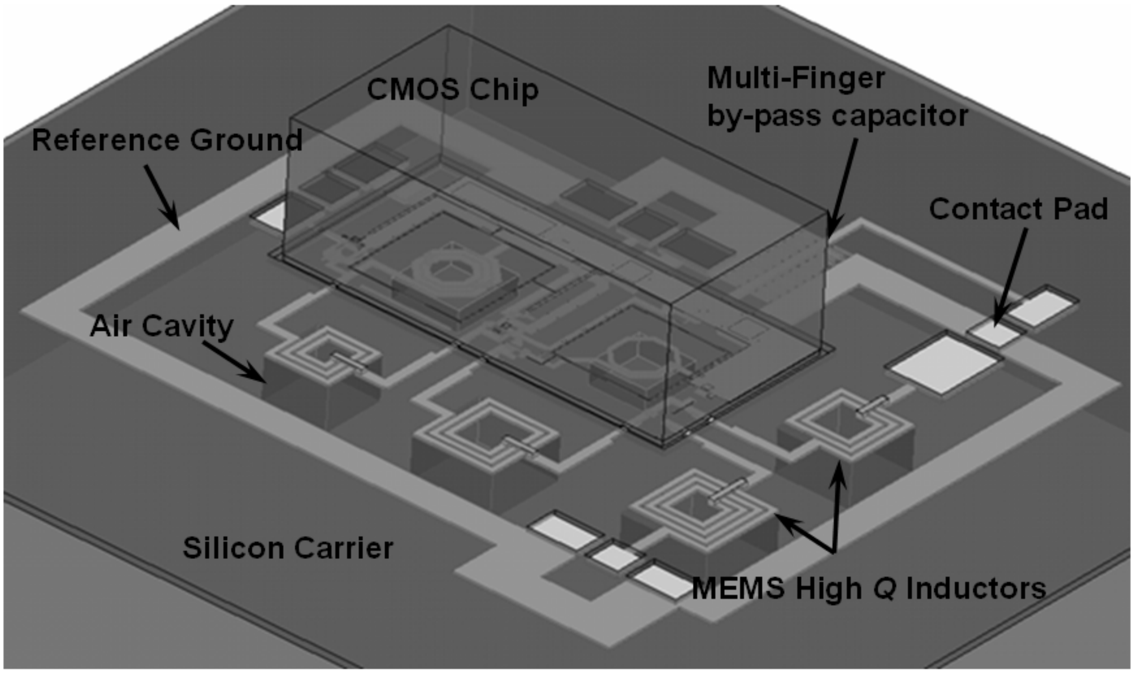
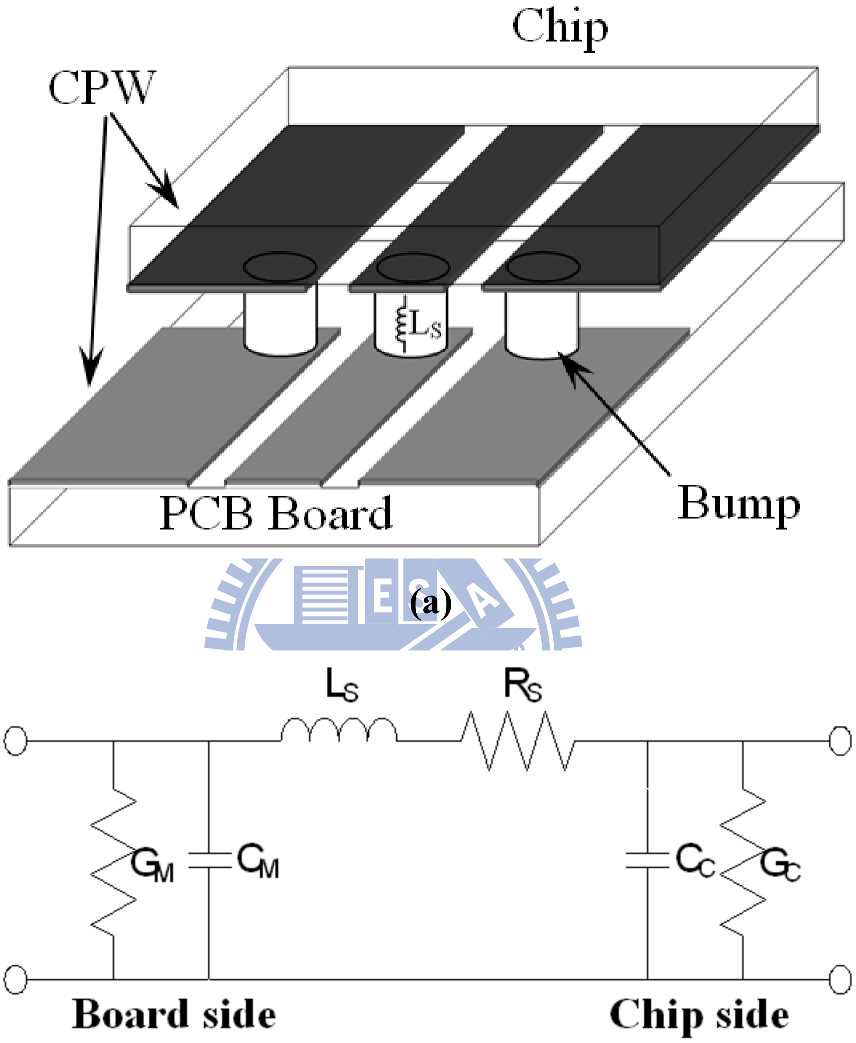


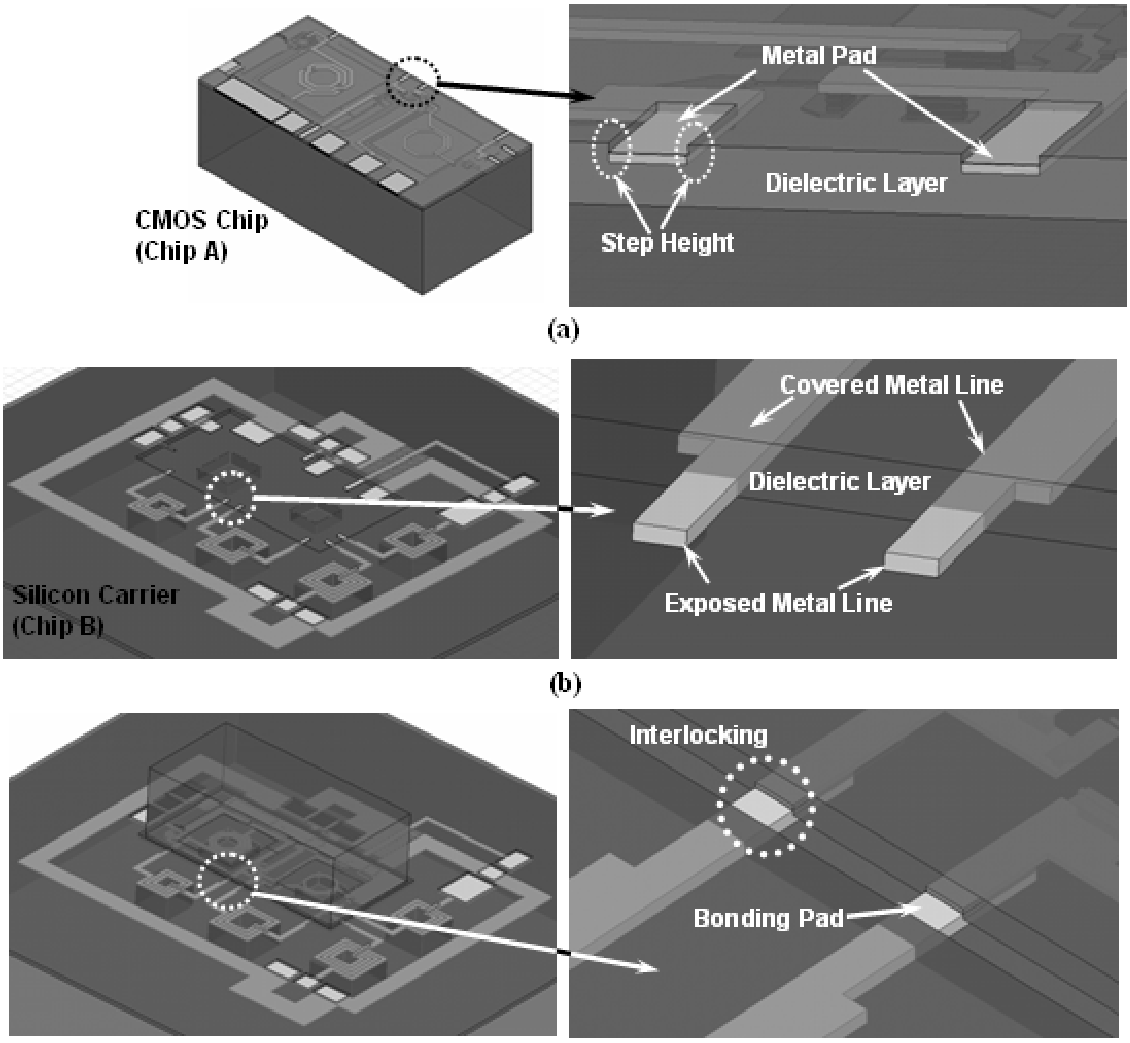
Figure 2.1 MEMS heterogeneous chip integration.



(a)

(b)

Figure 2.2 (a) Typical FC transition structure and (b) corresponding equivalent circuit model.



(a)

(b)

(c)

Figure 2.3 Self-interlocking bumpless interconnecting technology proposed for heterogeneous chip integration. (a) CMOS chip after blade dicing. The enlarged view of a diced CMOS chip near bonding pads shows a step height between the top surface of the bonding pad and the passivation. (b) Silicon carrier is fabricated using a standard CMOS backend process and a MEMS process. The backend process is utilized to fabricate interconnect lines and bonding pads for the CMOS chip assembly, and a MEMS process is utilized to etch silicon, which is underneath the inductors for the purpose of substrate loss reduction. The thickness of the exposed metal line should be thicker than the step height on the CMOS chip. (c) CMOS chip is integrated with the carrier using the bumpless interconnecting technology. The inset shows that the concave pad on the chip will be self-interlocked with the metal line on the carrier during the chip integration.

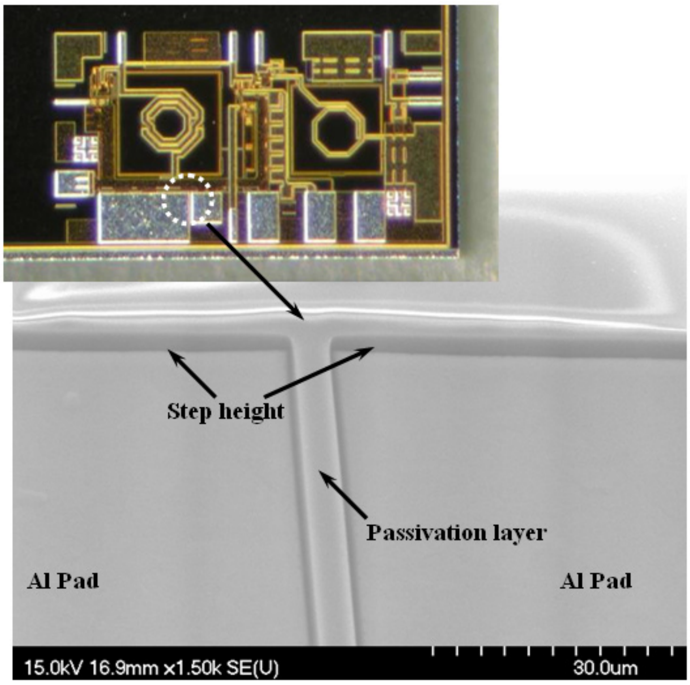


Figure 2.4 SEM photograph of the enlarged view on the corner of an Al pad shows a step height between the top surfaces of the Al contact pad and the passivation in a standard CMOS chip. (Inset) Optical micrograph of the TSMC 0.18 μm mixed signal CMOS chip.

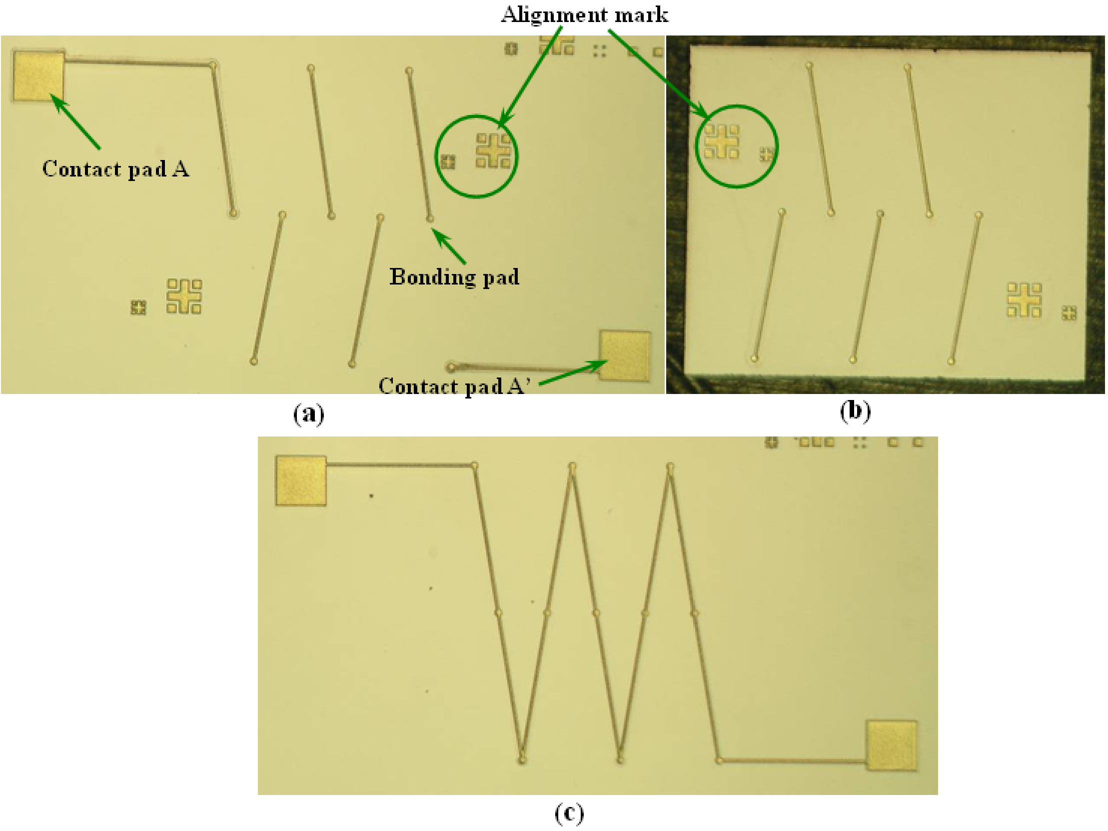


Figure 2.5 Optical micrographs of dc contact resistance test structures, i.e., the Daisy chain, including two separate chips (a, b), and a line pattern (c) for de-embedding.

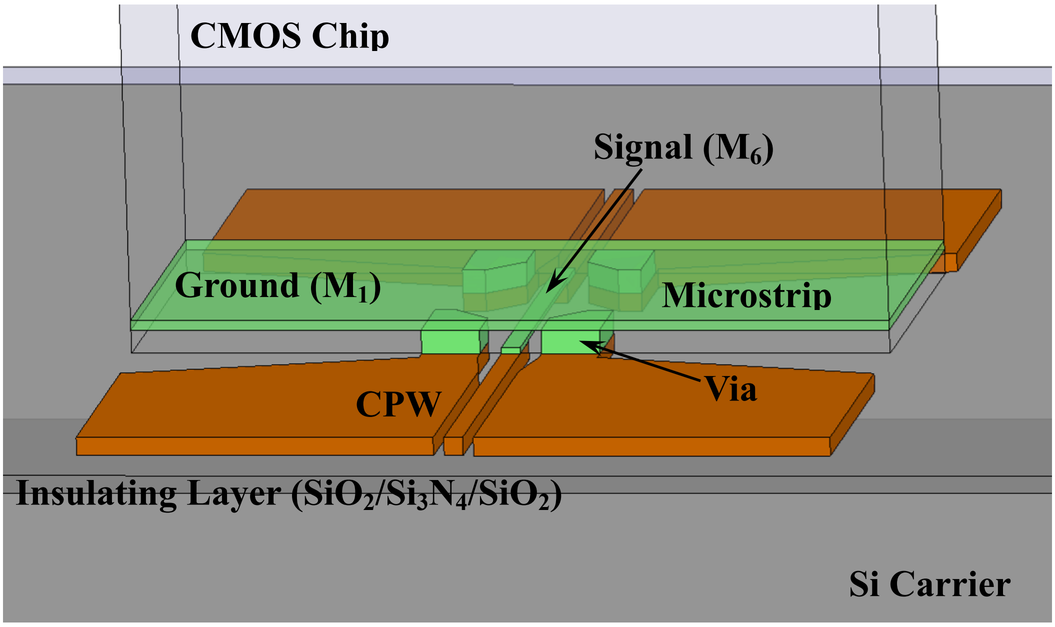


Figure 2.6 The RF transition structure for characterization of the proposed bumpless interconnecting technology from CPW on the Si carrier to microstrip line on the CMOS chip fabricated in a standard 0.18μm CMOS process.

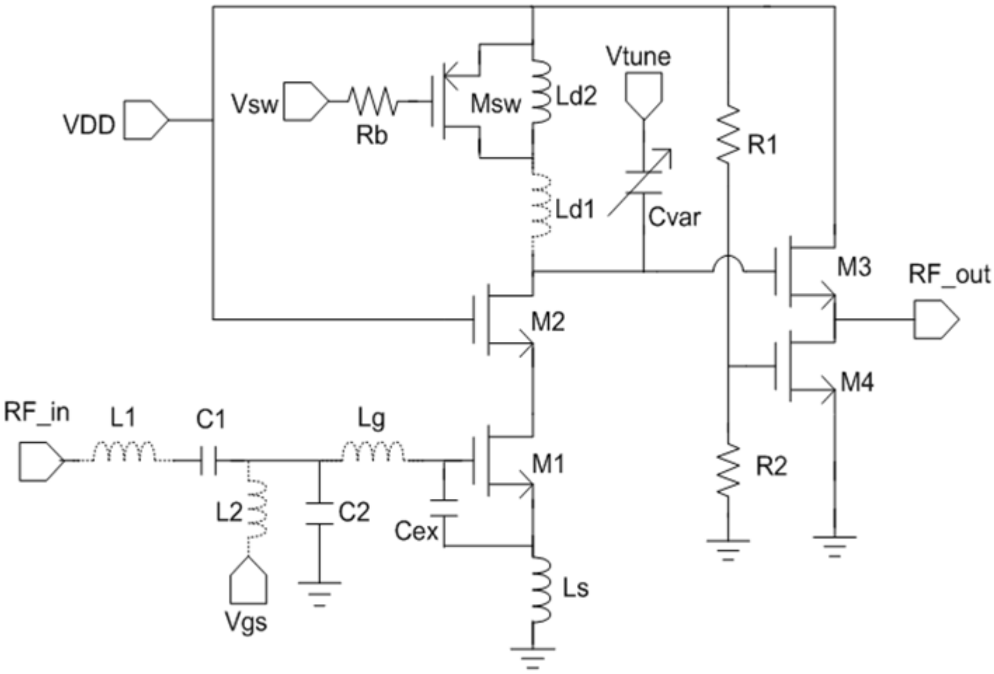


Figure 2.7 Tunable LNA circuit. Four high Q MEMS inductors (as shown in dashed lines) are utilized to improve the circuit performance.

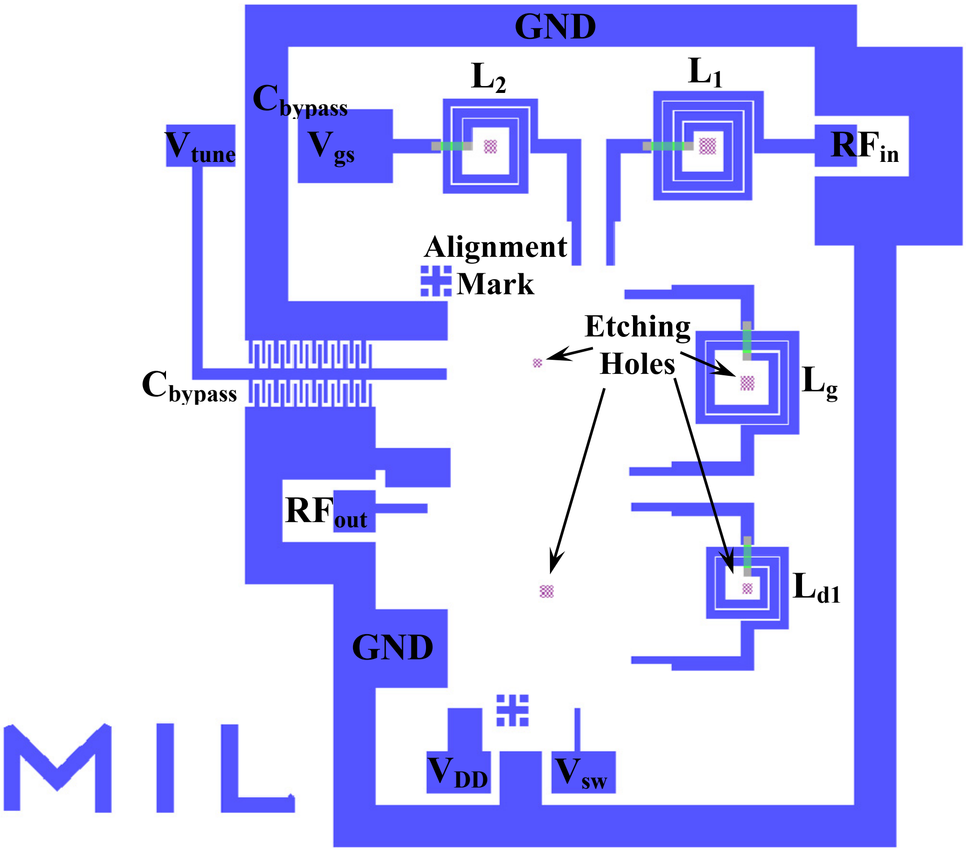


Figure 2.8 The layout of Si carrier for UWB tunable LNA integration.

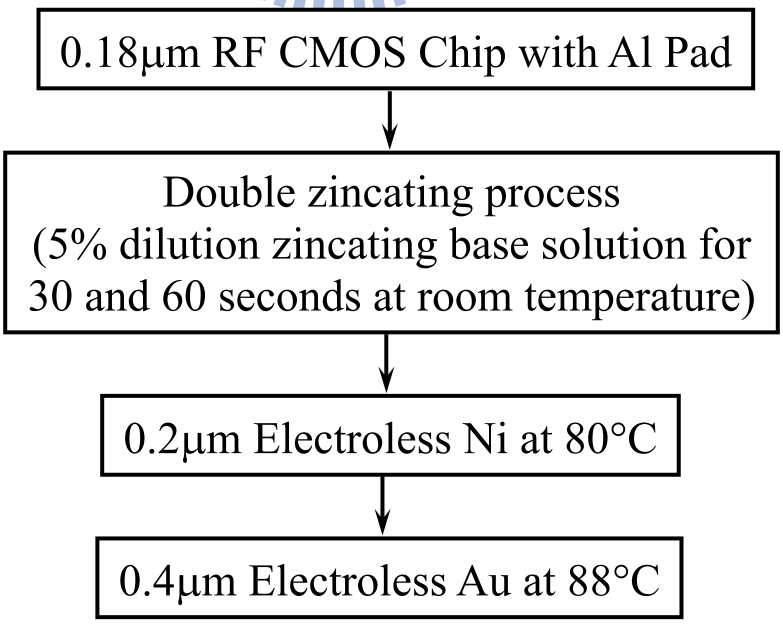


Figure 2.9 Process flow of maskless metallization to the CMOS chip.

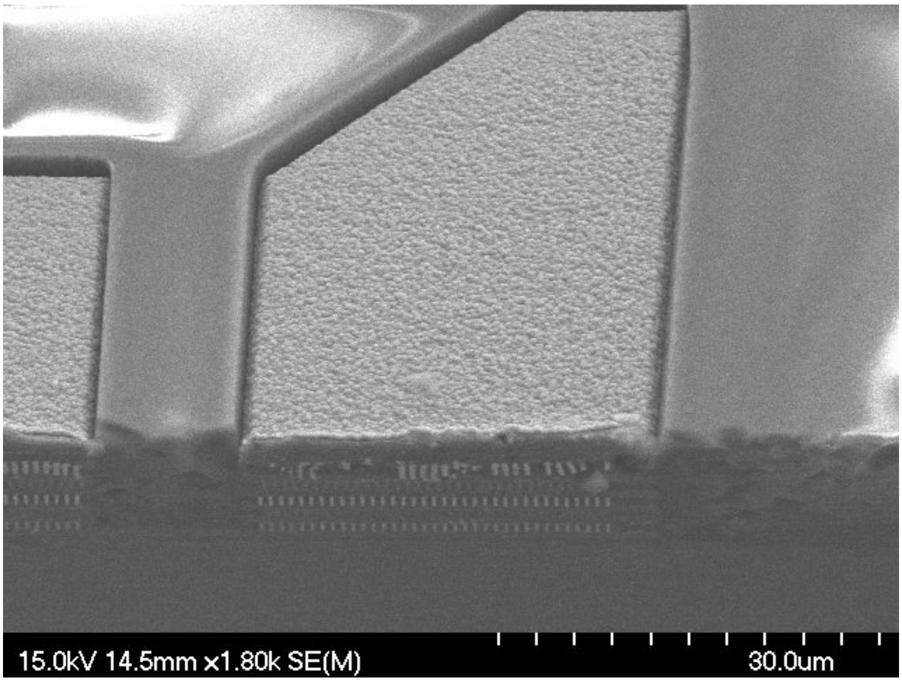


Figure 2.10 SEM photograph of the enlarged view on the diced edges of the CMOS chip.

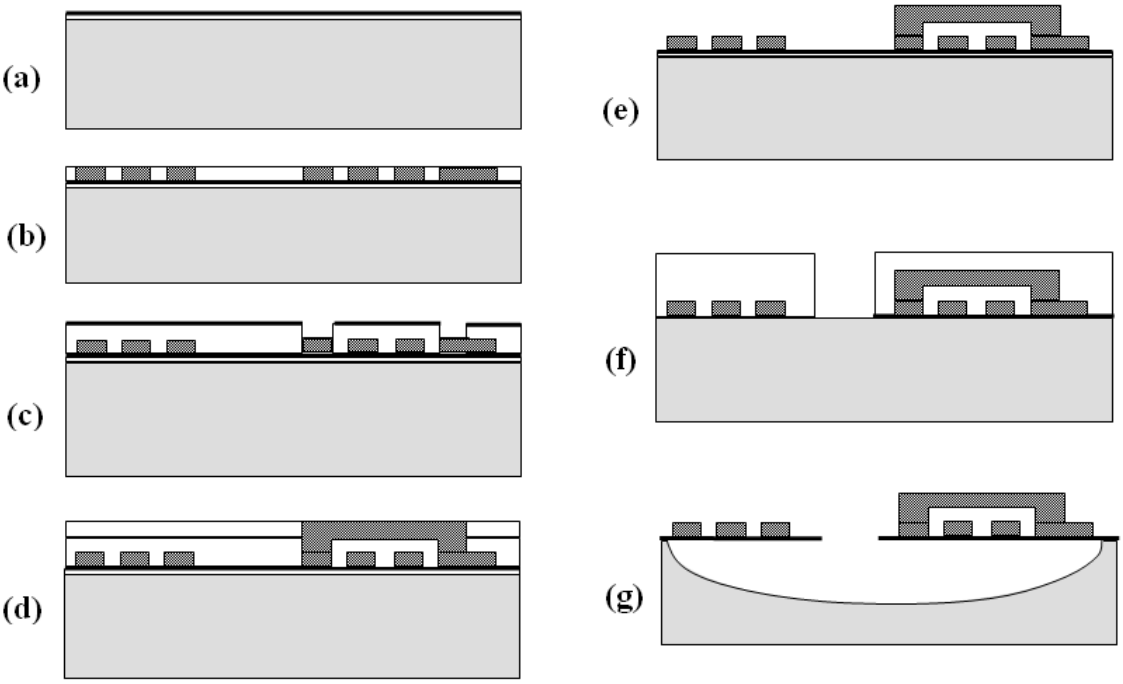


Figure 2.11 Silicon carrier fabrication processes: (a) $SiO_2/Si_3N_4/SiO_2$ membrane and Ti/Cu seeding layer deposition, (b) first Cu plating, (c) via patterning and air-bridge seeding layer deposition, (d) air bridge and via plating, (e) photoresist and seeding layer removal, (f) membrane patterning by reactive ion etching, and (g) silicon substrate removal using XeF_2 gas followed by a photoresist strip.

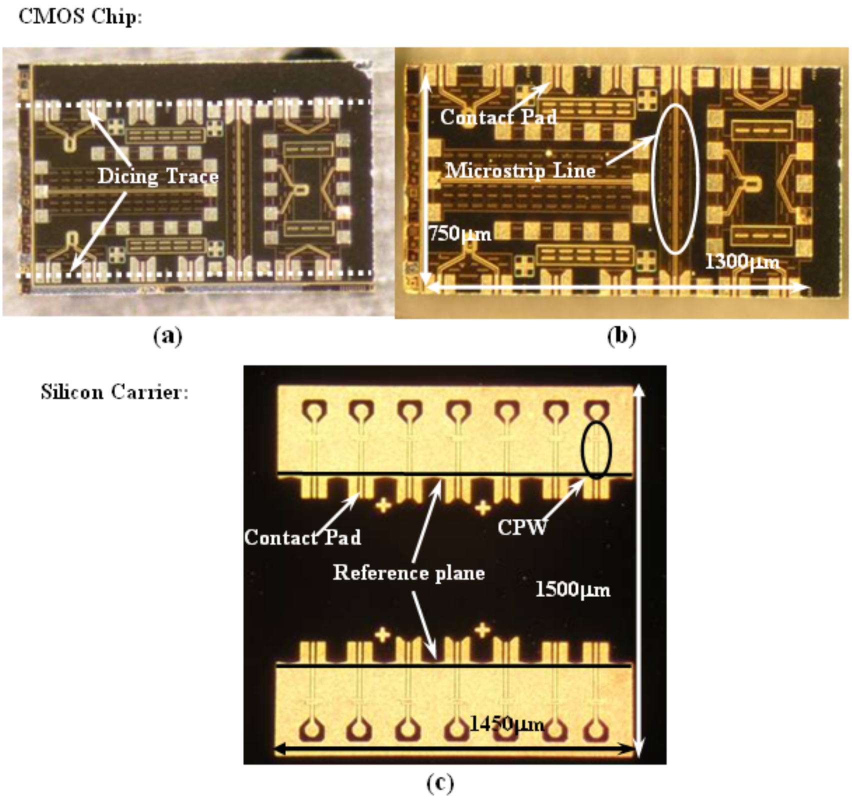


Figure 2.12 Optical micrographs of (a) before, (b) after a blade dicing the CMOS chip, and (c) as-fabricated silicon carrier.

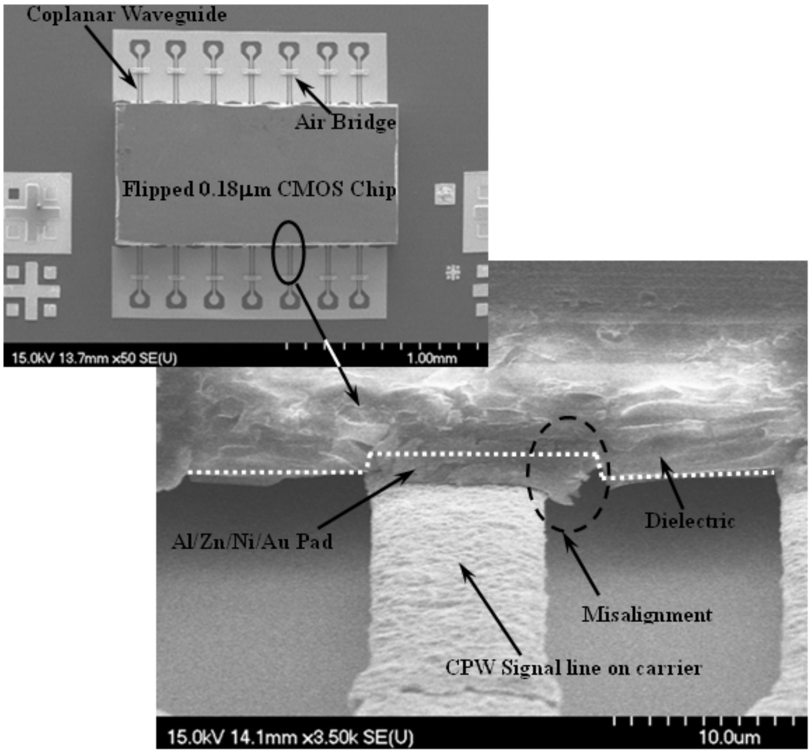
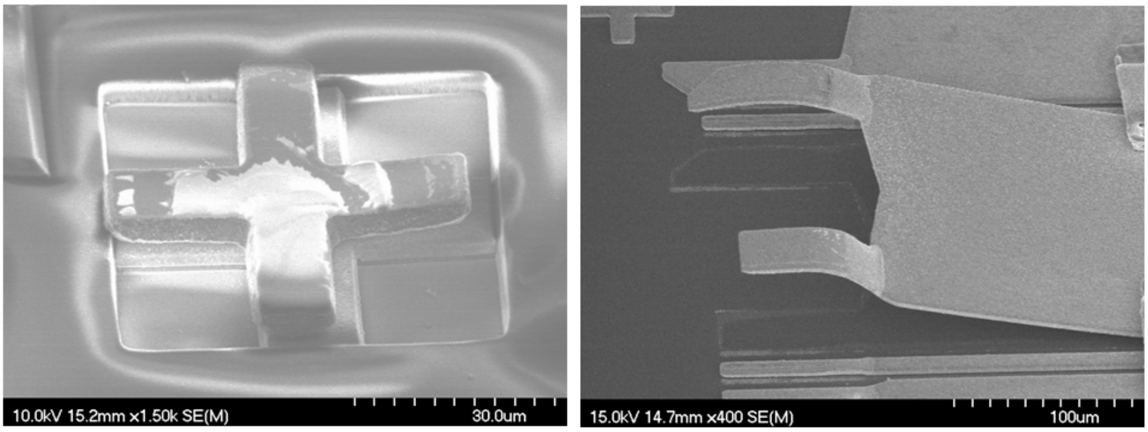


Figure 2.13 SEM photographs of (Top) the chip-assembly result and (bottom) an enlarged view at the bonding area.



(a) (b)

Figure 2.14 Enlarged SEM photographs of (a) alignment mark on the silicon carrier transferred onto the CMOS chip and (b) lifted Cu line on the silicon carrier after forcefully separating the bonded transition structure.

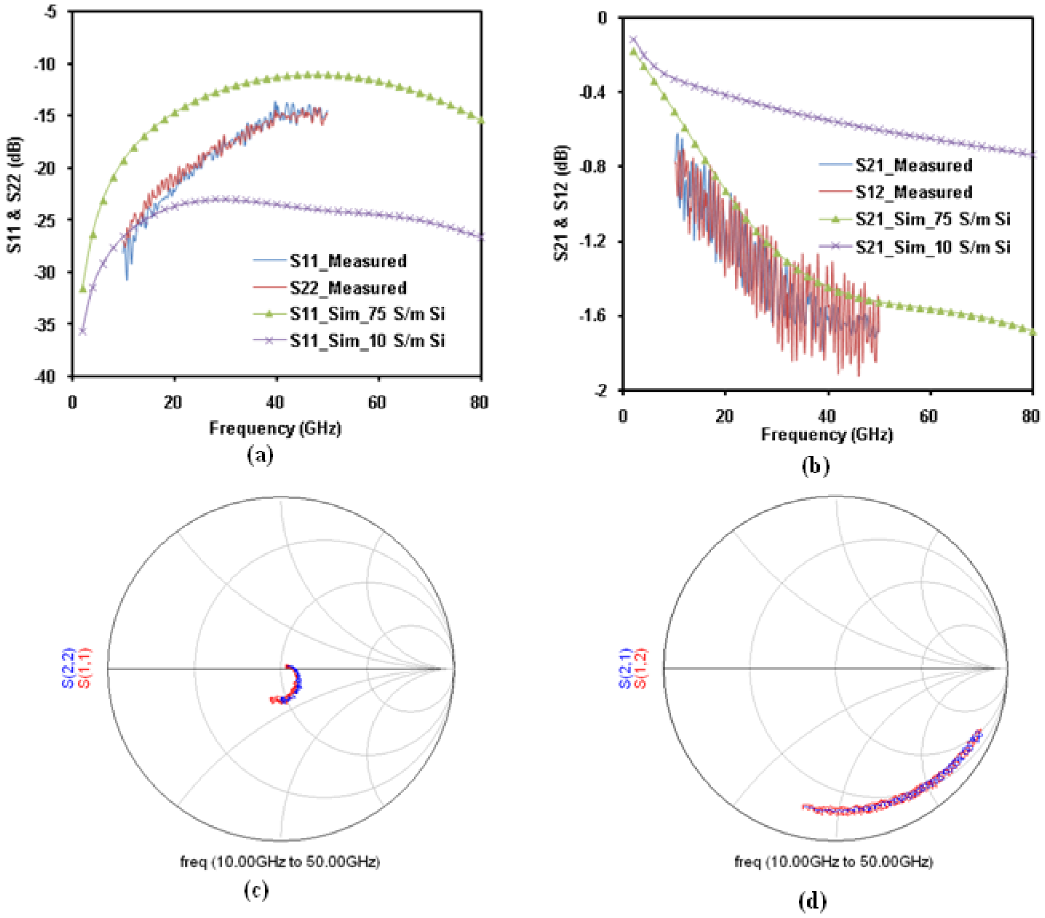


Figure 2.15 Simulation and measurement results of (a) return loss and (b) insertion loss of the EM signal propagating through the transition design with the transmission lines, a CPW, and a microstrip line, and corresponding measurement results of (c) return loss and (d) insertion loss shown in Smith charts.

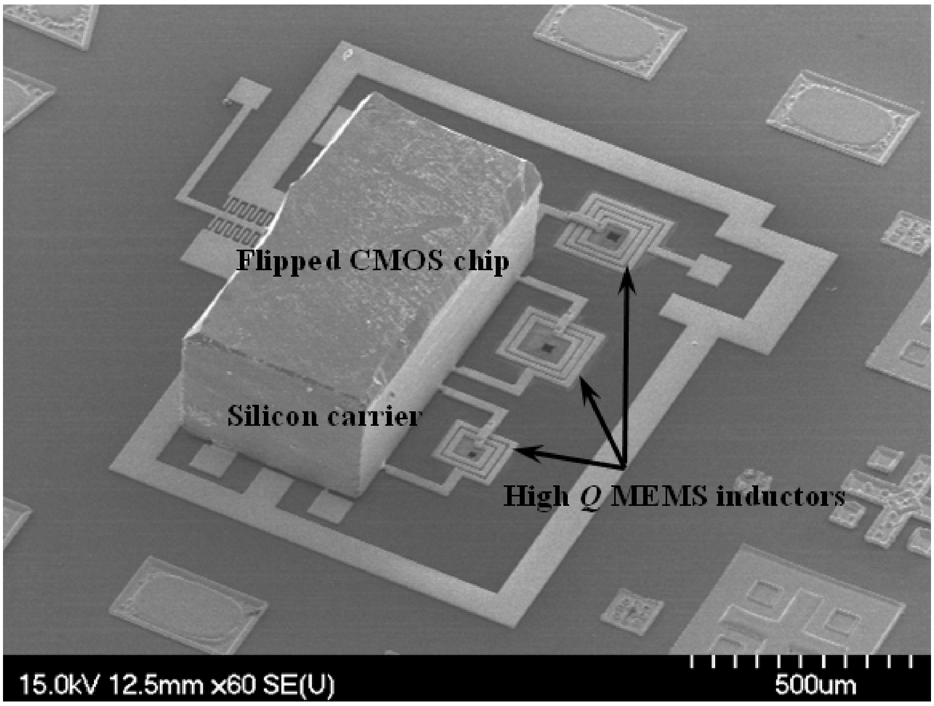
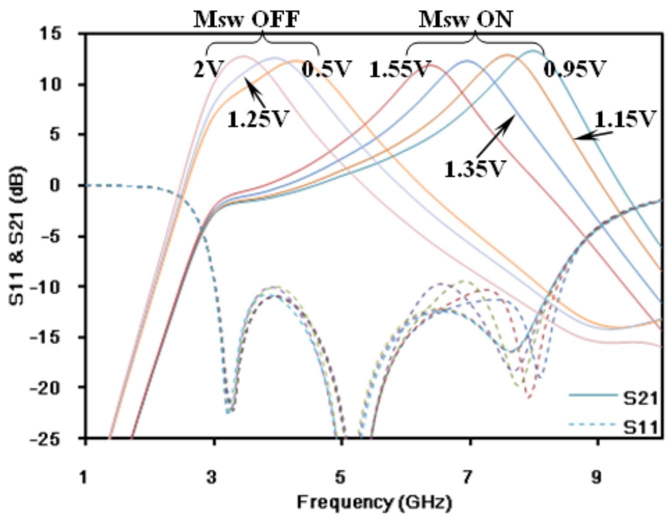
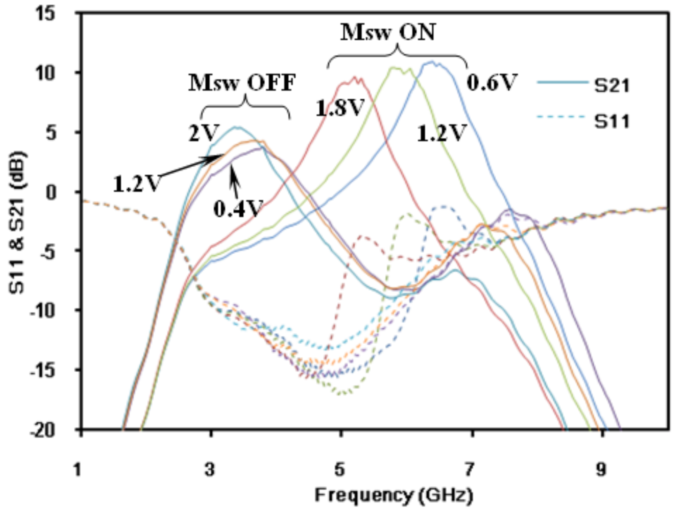


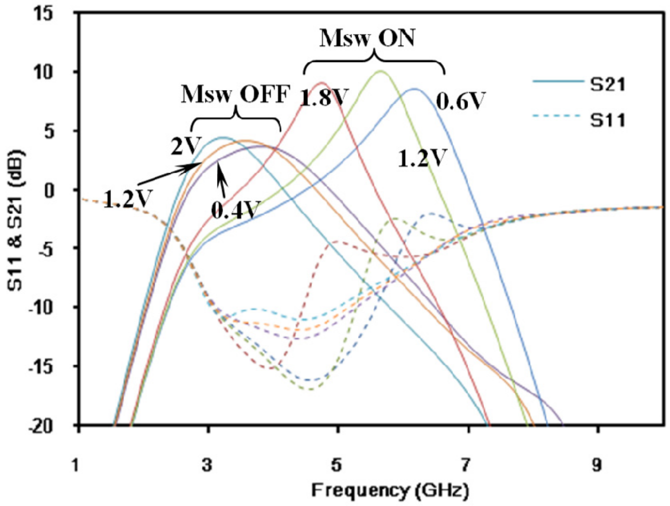
Figure 2.16 SEM photograph of the UWB tunable LNA with high *Q* MEMS inductors. The rectangular holes located in the center of inductors provide a path for XeF_2 vapor isotropic etching.



(a)



(b)



(c)

Figure 2.17 (a) Schematic simulation, (b) measurement results, and (c) full layout simulation of the return loss and gain with a different tuning voltage of the UWB LNA circuit.

Table 2.1 Comparison of Au Bump, Au Stud Bump, and Ni/Au Bumpless Processes [49,50]

Bump type	Au bump	Au stud bump	Ni/Au bumpless (This work)
Process Technique	Electroplating	Wire bumping	Electroless deposition
Advantages	● Flexible bump shape ● High throughput in a batch process	● Cost-effective for low bump counts ● Rapid prototyping	● Maskless metallization and a typical process in packaging house ● Flexible bump geometry and pitch size ● Almost zero bump height ● High throughput in a batch process
Disadvantages	● Lithography process required for bump formation ● Not a typical metallization process in foundry and packaging house ● Large pitch size due to the lateral flow of bumps	● Low throughput for bump formation ● Large pitch due to the lateral flow of the bumps	● Bond pads limited to the periphery of a chip ● High chip dicing accuracy required on bump pads

Chapter 3 SU-8-Based Low-temperature Fabrication Process for Flexible Microsystem Fabrication

3.1 Introduction

Flexible electronics have attracted a lot of research attention in recent years due to their various potential applications such as flexible displays, stretchable solar cells, wearable wireless sensors and circuit systems. One of the technical challenges in the development of flexible electronics is fabrication temperature limitation due to the low glass transition point of a substrate. The flexible electronics fabricated on an organic substrate are generally accompanied by the characteristics of light weight, high flexibility, and low manufacture cost. However, the temperature limitation (<200°C) makes existing semiconductor processing techniques impracticable for the device fabrication of flexible electronics that require new materials with low manufacturing temperature characteristics [52–57].

Previously, Chang *et al.* developed a customized low-temperature high-density inductively coupled plasma chemical vapor deposition (HDICPCVD) technique to deposit SiN_x at 100°C for the fabrication of RF MEMS on a printed circuit board [52]. Guo *et al.* utilized a special glue to thermally compressive bonded thin Si wafer (50–100 μm thick) with a flexible FR-4 substrate (0.1 mm thick) so that the Si-based active MOS transistors and RF passive components can be transferred onto the flexible substrate with superior device performance [53]. In addition, Yuan *et al.* proposed a silicon on insulator (SOI) wafer transferring technique whose processing temperature can be controlled well below 120°C to demonstrate single-crystal Si thin-film transistors on a flexible polymer with the unit gain cut-off frequency, f_T, of 1.9 GHz and the maximum oscillation frequency, f_{max}, of 3.1 GHz [54].

SU-8, a photo-definable plastic polymer invented by IBM, has been widely used for MEMS fabrication in recent years due to several superior material properties including excellent chemical stability for good biocompatibility, transparency to visible light suitable for device fabrication with a high aspect ratio, and low Young's modulus (~3.4 GPa) for better structure flexibility. Besides, its low processing temperature characteristic makes it a fascinating material for RF MEMS fabrication on a flexible substrate.

Thus, in this chapter, a SU-8 based low-temperature wafer-level process is presented for flexible microsystem fabrication. Firstly, a new low-temperature SU-8 micromachining process is developed for RF MEMS passive fabrication to demonstrate the feasibility of RF MEMS fabrication on flexible organic substrate. Besides, based on the bumpless interconnecting technology presented in Chapter 2, a surface cleaning step is adopted before Au-Au thermocompressive bonding to lower the bonding temperature below 200°C for heterogeneous integration CMOS chip on SU-8. With cleaning technique, a flexible microsystem fabrication scheme using metal sacrificial release process is developed for the batch manufacturing of various flexible microsystems in one release step. Furthermore, the fabrication scheme is also used to integrate biomedical Si probe with SU-8 ribbon cable for signal transmission. Unlike the aforementioned techniques which require special tools or might have low manufacturing yield during wafer transferring, such a low-temperature fabrication scheme can provide an alternative to realize cost-effective integration on organic substrate for high performance flexible RF SOP applications.

3.2 An SU-8 Serial MEMS Switch

RF MEMS switches possess a lot of advantages such as low series resistance, high isolation, and inherently negligible inter-modulation distortion [6]. It, therefore, has become a key component in the next generation RFIC systems. Previously, Shi *et al.* had already demonstrated the first SU-8 MEMS switch with a lateral, direct contact beam structure for potential RF applications [58]. Although the switch with a self-cleaning design exhibits not only a low contact resistance but also a longer device lifetime, the lateral contact structure still needs further design to be integrated with conventional transmission lines for RFIC application that requires the design of 50 Ω characteristic impedance and mode-matched transition. Thus, a typical RF MEMS series switch fabricated using the proposed low-temperature SU-8 micromachining technique to demonstrate the process feasibility for the application of flexible electronics is presented as follow.

3.2.1 Switch Design and Fabrication Process

The switch is designed with an electrostatically actuated clamped–clamped beam structure as shown in Figure 3.1, which is a conventional MEMS series switch. The switch is fabricated on the top of a 50 Ω CPW. There is a 100 μm separation between two disconnected 450 μm long, 76 μm wide signal lines which would be connected if the switch is operated at ‘on’ state. The clamped–clamped beam structure of the switch is 1350 μm long, 320 μm wide and has a 10 μm gap spacing between the upper and lower driving electrodes. The beam is made of an SU-8/Cu/SU-8 sandwich layer to effectively eliminate the effect of induced residual stress on device performance. According to the switch design of Hyman *et al.* [59], a sandwich layer structure could ease the coefficient of thermal expansion (CTE) mismatch that causes structural bending due to process temperature variance. After the beam is released, the stress compensation in the sandwich layer can further enhance device reliability.

Figure 3.2 shows the schematic process flow of the proposed SU-8 MEMS switch. The fabrication starts with 0.7 μm thick wet thermal oxidation at 1050°C for 2 h for electrical isolation on a commercial 4" silicon wafer with a resistivity of around 5 Ω·cm as shown in Figure 3.2(a). As shown in Figure 3.2(b), a layer of Ti (100 Å)/Cu (1200 Å) is then dc sputter-deposited as seed layer covered by 7 μm thick AZ4620, and selectively electroplated with 1.2 μm thick Cu with a current density of about 1 A/dm^{-2} as the aforementioned structure fabrication of the CPW, the ground plane, and the bottom biasing electrodes that are used for beam actuation. After removing AZ4620 and the Ti/Cu seed layer using acetone, buffered oxide etch (BOE) and CR-7T, a 10 μm thick negative photoresist (PR), JSR THB-120N [60], is spin-coated and patterned as a sacrificial layer for the suspended switch structure fabrication as shown in Figure 3.2(c). The thickness of JSR will define the initial gap between the contact metal of the switch and the CPW signal line underneath the contact. The gap spacing determines the switch isolation while it is operated at 'off' state. Once the JSR layer is defined, the first 3 μm thick SU-8 (GM1040) layer is spin-coated as the beam structure of the switch. However, due to the non-uniformity resulting from spin-coating on the 10 μm thick sacrificial layer, the thickness of the first SU-8 layer is measured to be about 5 μm by the surface profiler ET-4000 (Kosaka Laboratory Ltd). Prior to the hard baking, the SU-8 must be photo-patterned for the mechanical anchor and electrical contact fabrication of the switch. The anchor and metal contact are used for connecting the metal layer of the switch beam to the electrode for biasing the switch structure and to the CPW for electrical contact, respectively. Thus, before depositing a secondary Cu layer, the unmasked JSR region is slightly etched with the O_2 plasma reactive ion etching (RIE) process to expose a part of the metal layer deposited later for the switch contact as shown in Figure 3.2(d).

For the secondary Cu layer deposition of the switch, another layer of Ti (100 Å)/Cu (1200 Å) is dc sputtered as the seed layer covered by 7 μm patterned AZ4620 PR for 2 μm thick selective Cu electroplating as shown in Figure 3.2(e). After electroplating Cu, the patterned AZ4620 and Ti/Cu are stripped first and then another layer of 3 μm thick SU-8 is spin-coated, photo-patterned, and hard baked again as shown in Figure 3.2(f). Finally, the JSR sacrificial layer is removed using JSR stripper THB-S1 at room temperature until the sacrificial layer is totally removed to form a freely suspended MEMS series switch as shown in Figure 3.2(g). The as-fabricated switch structure contains two layers of SU-8 and one Cu layer within. Figure 3.3 shows optical micrographs taken from one end of the switch before and after stripping away the JSR sacrificial layer. It is clearly shown that the removal of the JSR layer can be observed under an optical microscope due to the transparency of SU-8 to visible light. It is noted that the average surface roughness of electroplated Cu characterized by an atomic force microscope (AFM), as shown in Figure 3.4, has been well controlled by the aforementioned current density so as to get a good contact surface. The roughness of about 12.26 nm indicates that our electroplating process is as good as the published results [61,62].

3.2.2 Experimental Results and Discussions

The driving voltage of the as-fabricated SU-8 switch is determined from the measurement of dc contact resistance versus driving voltage. The contact resistance, R_C, is derived as follows:

$$R_c = \frac{R_{on} - R_{GND}}{2} \tag{3.1}$$

where R_{on} and R_{GND} are the resistance of the signal line of the CPW at the 'on' state and the measured resistance of the ground line, respectively. The resistance measurement of the as-fabricated switch shows that the device with the input of 63 V will have an electrical contact with a contact resistance of 24.38 Ω. With the increase of the input voltage up to 92 V, the contact resistance will decrease to ~2.87 Ω which is close to the previously reported Cu–Cu contacts loaded with the contact force of ~20 μN [63].

Figure 3.5 shows the experimental setup for the as-fabricated switch RF measurement where Infinity I50-GSG-150μm probes connected to an Agilent E8364B PNA network analyzer are utilized for the measurement of the *S* parameter and Cascade EP-03-150W power bypass probes connected to serially linked Good Will Instrument PPT-1830 power supplies are utilized for actuating the switch. Figure 3.6 shows the measurement and simulation results of the SU-8 switch. The simulation results are calculated by an Ansoft high-frequency structure simulator (HFSS) with the conditions of 6 Ω·cm silicon resistivity and 2 Ω contact resistance for each contact. Insertion loss and isolation represent the S_{21} performance of the switch operated at the 'on' and 'off' states, respectively. While the contact metal fully contacts with two disconnected CPW signal lines, i.e. at the 'on' state, the insertion loss is about −3.46 dB at 4 GHz/−4.48 dB at 12 GHz that includes the intrinsic loss of two disconnected CPW, contact loss and the loss originating from the contact metal in the switch. On the other hand, the isolation represents the performance of the switch operated at the ‘off’ state. Due to the large contact distance between the switch metal contact and the CPW while the switch is operated at the ‘off’ state, the switch has a good isolation of −49.09 dB at 100 MHz/−28.23 dB at 12 GHz.

Although the switch performance of −4.48 dB insertion loss and −28.23 dB isolation at 12 GHz is worse than the reported results [6,64], the high insertion loss can be attributed to the substrate loss from the low resistivity of a Si substrate while the signal is transmitted along the 1000 μm long CPW. According to the simulation as shown in Figure 3.6, the insertion loss can be greatly reduced down to −0.75 dB at 12 GHz once the resistivity of the Si substrate increases up to 100 Ω·cm. Since the contact loss in the switch is around −0.38 dB without counting the CPW loss, which is comparable to the latest published Au contact switch whose loss is about −0.37 dB [64], it indicates that the as-fabricated switch performance can be further improved using the flexible organic substrate instead of the silicon substrate and a shorter transmission line to effectively reduce substrate, metal resistive losses. Nevertheless, the SU-8 process indeed provides an alternative approach for the fabrication of MEMS switches with a decent RF performance.

The bending moments M_e of a sandwich structure cantilever beam can be calculated as follows [65]:

$$M_e = \sigma_a w t_a (y_e - y_a) - \sigma_b w t_b (y_b - y_e) - \sigma_c w t_c (y_c - y_e) + \frac{1}{6} \nabla \sigma_b w t_b \qquad (3.2)$$

where t_a, t_b and t_c are the thicknesses of each layer; y_a, y_b and y_c are the neutral axes of each layer; σ_a, σ_b and σ_c are the mean stresses of each layer; and

w, y_e and $\nabla\sigma_b$ are the width of the beam, the neutral axis of the sandwich beam and the stress gradient of the middle layer, respectively. If the top and bottom layers are made of identical material and have the same thickness, then y_e is equal to y_b. Therefore, the first three terms of equation (3.2) can be fully canceled to minimize the residual stress. However, it is inevitable to have process non-uniformity resulting in thickness difference of two SU-8 layers, which is 3 and 5 μm, respectively, at the laboratory and the residual stress cannot be eliminated in our case. Since we do not observe any deformation of the sandwich clamped–clamped beam by an optical microscope after sacrificial layer release, this means that the residual stress has been reduced and it would not dramatically induce an unwanted effect on the proposed sandwich beam. The details of residual stress characterization in each layer of the sandwich beam still need further investigation. In addition, the spin coating has been widely studied for film planarization [66,67]. SU-8 is a spin-coated PR whose thickness can be well controlled in terms of the spraying amount of the PR, spinning speed and time, soft baking temperature and time for reflowing, and so on. In fact, the non-uniformity problem can be well resolved with further process optimization.

Figure 3.7 shows the preliminary cycling test results of the SU-8 switch which has been actuated at 92 V 2000 times. The result shows that the variance of contact resistances of Cu–Cu contacts is less than 10%. No drastic contact resistance increase has been found. Besides, the measured contact resistance is still larger than that of the Au contact [68]. Since the residual stress which may influence the contact resistance is reduced by the sandwich structure, the contact resistance could be mainly attributed to very thin native oxide formation on the Cu surface. For future applications of the switch to flexible electronics, the insertion loss of the switch can be further improved using the SU-8 low-temperature process combined with Au plating instead of Cu plating.

3.3 Heterogeneous Chip Integration Process

Flexible microsystems have attracted lots of research attention recently due to its great potential in the applications of personal portable devices. Several technologies which can be divided into three major fabrication approaches such as direct fabrication, transfer technique and multi-chip module integration have been developed for the realization of flexible microsystem at a low temperature (<200°C) on an organic substrate [69-74]. The direct fabrication methods utilize low temperature deposition of amorphous silicon (a-Si:H) [69] or organic semiconductor [70] for making flexible thin film transistors (TFTs) directly on flexible substrate. Due to the lower carrier mobility of these materials than that of inorganic single-crystal semiconductor, poor active device performance makes this method impractical for the fabrication of high performance electronics systems. On the other hand, transfer techniques usually fabricate active devices on the device substrate before thinning and transferring on to a flexible substrate [71,72]. However, high manufacturing cost and complexities indicate more research effort is required in the development of flexible microsystem fabrication. Different from the aforementioned two methods which do not have ability of heterogeneous integration for better process compatibility and flexibility, and multi-functionality, Cu lateral interconnections [73] and conventional flip chip process [74] using solder bump or anisotropic conductive adhesive can integrate individually optimized chips which are fabricated by different process technology, such as CMOS, III-V and MEMS…etc., onto a flexible substrate based on the concept of multi-chip module. Although the process temperature can be lower than 200°C, inevitable structure discontinuity between chips and structures and high contact resistance in the interconnecting transition using the solder bumps are not suitable for high frequency applications. Therefore, a new exploratory flexible electronics fabrication scheme is needed for flexible wireless microsystem applications

Wireless body sensor networks (WBSN) is chosen to clarify the proposed flexible microsystem fabrication scheme in this work as shown in Figure 3.8. WBSN is a wireless sensor platform for remote healthcare monitoring and it should have multi-functionality such as inductive coil, rectifier circuit and super capacitor for energy harvesting, MEMS sensors and actuators for bio-signal extraction, Analog/Digital circuit for signal analysis and data processing, RF front end circuit with integrated passive devices and antenna for data communication and so on. However, the previously developed heterogeneous integration techniques are insufficient for the implementation of such a microsystem which needs not only low process temperature but also low cost, good process compatibility and good interconnecting performance…etc.

Although the bumpless interconnecting technology presented in Chapter 2 has shown its great potential in RF system-on-package integration, high-temperature Au–Au thermocompressive bonding process (> 300°C) would make the technology impractical for the chip integration on a flexible substrate. Prior investigation has shown that the cleanness of bonding surface is a key process parameter to lower the bonding temperature [75]. Although Saito *et al.* has demonstrated a room-temperature surface-activated Cu–Cu bonding (SAB) [76] for chip assembly, the SAB has the characteristics of low process uniformity tolerance, long activation time (~30 min), and special customized tool requirement difficult for the implementation of mass production.

Therefore, by employing the previously developed bumpless chip assembly scheme using Au-Au thermocompressive bond [7,8] and a special surface cleaning process for the realization of low temperature bonding, a low-cost wafer-level chip scale flexible wireless microsystem fabrication scheme for wireless microsystem applications is proposed as follow. Flexible substrates can be deposited and patterned on a Si handle wafer with a sacrificial layer. Metal interconnects, bonding pads, or high quality passives…etc. can be directly fabricated on the flexible substrate by conventional wafer-level CMOS or MEMS process. After surface cleaning and flip chip bonding various high performance circuit/device chips which are fabricated individually by different process technology, a flexible microsystem can be simultaneously obtained once the flexible substrates are released from the Si handle wafer by removing the sacrificial layer. The presented wafer-level chip scale fabrication scheme for flexible wireless microsystem applications using the sacrificial release process and the low temperature bumpless Au-Au thermocompressive (TC) bonding technology can indeed realize a low cost and reliable flexible wireless microsystem.

3.3.1 Integration Process

The same flip-chip transition structure which proposed in Chapter 2 is utilized to demonstrate the proposed integration process on an SU-8 flexible substrate as shown in Figure 3.9. The integration process, as shown in Figure 3.10, begins with the flexible substrate fabrication given here.

Figure 3.10(a) shows a silicon substrate that is first sputtered with 10/300 nm thick Cr/Cu as a sacrificial layer, followed by SU-8 spin-coating. The thickness of the SU-8 layer is about 26 μm. After photopatterning the SU-8, the substrate is hard-baked at 200°C for 2 h in order to make a fully cross-linked SU-8 for having a higher glass transition temperature T_g [77]. The baking process can enhance TC bonding reliability by preventing the sudden changes in terms of the coefficient of thermal expansion increase and the stiffness decrease in the SU-8 once the bonding temperature is larger than the T_g of SU-8. In addition, it can also increase the SU-8's chemical stability in the surface-cleaning process for bonding. After substrate baking, a 10/90 nm Ti/Cu seeding layer is deposited on the SU-8, followed by a photolithograph process using a 10 μm thick AZ 4620 photoresist to define the region for the CPW fabrication, as shown in Figure 3.10(b). After electroplating an 8 μm thick copper CPW on that region, a serial process of 1 μm electroless Ni and 0.4 μm electroless Au is performed to metallize the Cu surface for the bonding, as shown in Figure 3.10(c). Figure 3.10(d) shows that the AZ 4620 and Ti/Cu seed layers are then sequentially removed using ACE, CR-7 T, and then BOE. On the other hand, the contact surfaces of TSMC 0.18 μm CMOS chip will be metallized using a maskless double-zincating process, followed by 0.2 μm electroless Ni deposition and 0.4 μm electroless Au. Detail CMOS chip preparation for the bumpless integration has been detailed in Chapter 2.4.1.

Piranha clean has been used as a standard cleaning procedure in CMOS front-end processes [78]. In fact, the piranha clean process can also be utilized in the proposed integration technique for bonding surface cleaning since the Au pads and passivation layer on the CMOS chips in the proposed integration scheme are all chemical inert to the cleaning chemical. Meanwhile, SU-8 is a photopatternable polymer with several superior material properties including good chemical stability, high flexibility, good electromagnetic properties, and wafer-level process capability that make it fascinating as a flexible substrate material. Thus, in the integration scheme, the acidic mixture solution of H_2SO_4 and H_2O_2 with the volume ratio of 3:1 is then employed as a cleanser for realizing low-temperature Au–Au TC bonds. Once both surfaces of the CMOS chip and SU-8 substrate are cleaned at about 50°C, the CMOS chip is flip-chip bonded to the SU-8 substrate at the conditions of 180°C and 100 MPa applied pressure for 3 min, as shown in Figure 3.10(e). At final, the sacrificial Cr/Cu layer is chemically etched away in Cu etchant (100:5:5 H_2O : CH_3COOH:H_2O_2) to release the SU-8 substrate, which can be directly attached to a PDMS (Sylgard 184) supporting substrate to form a flexible microsystem, as shown in Figure 3.10(f).

3.3.2 Results and Discussions

The surface-cleaning process for low-temperature Au–Au TC bonding is characterized using a daisy chain structure with ten bumps formed within two Si chips. Table 3.1 lists X-ray photoelectron spectrometer measurements regarding the surface contents of Au bonding pads before and after the surface-cleaning treatment using the aforementioned cleaning process. The increase in Au content from 41.9% to 64.6% and the reduction in carbon and oxygen contents indicate that organic contamination has been effectively removed from the pad surface. Table 3.2 lists the measured specific contact resistance (SCR) versus the bonding temperature of Au–Au bonds under the conditions of 100 MPa applied pressure for 3 min. For a 4 min cleaning treatment, the bonding temperature can be lowered down to 160°C with a $(5.65 \pm 1.86) \times 10^{-7}$ $\Omega\cdot\text{cm}^2$ SCR.

Two-port *S*-parameters of the transition structure are measured using Agilent E8364B PNA and Cascade Infinity GSG probe in the frequency range of 10–50 GHz. In order to maintain measurement and calibration accuracy, the designed interconnect measurement is performed before handling wafer detachment rather than directly probing on the released SU-8. The measured *S*-parameters have excluded parasitic effects from measurement pads and moved reference planes near the edge of bonding pads using thru-reflect-line calibration. Figure 3.11 shows the RF performance of the CPW–microstrip–CPW flip-chip transition, i.e., including two interconnect transitions and a microstrip. Better than −15 dB return loss and lower than −0.8 dB insertion loss up to 40 GHz have been achieved and closely matched with HFSS simulation results, as shown in Figure 3.11(a). The measured return loss is as good as that of the microstrip-to-CPW flip-chip compensated interconnects with pure Au line structures on an Al_2O_3 substrate demonstrated by Wu *et al.* [79]. In fact, the return loss can be further improved with a better impedance match between the CPW and the microstrip by process optimization in terms of the CPW dimensions and metal thickness control. In addition, according to the simulation results, there is no obvious RF performance difference between the transition on the SU-8 substrate with a Si handle wafer and that with a PDMS substrate, as shown in Figure 3.11(a). It can be attributed to the SU-8 layer, which is thick enough to prevent the possible influence of the sacrificial Cu layers on the performance.

After deducting the loss of microstrip (−0.31 dB at 40 GHz) from the measured insertion loss (−0.8 dB at 40 GHz), the loss of a bumpless interconnect transition can be calculated about −0.25 dB at 40 GHz. Owing to process limitation, electroless Ni simultaneously acting as the diffusion barrier layer between Au and Cu and the seeding layer of electroless Au is used in the fabrication of the interconnect transition and CPW in our case. Since the electroless Ni has a larger resistivity (~100 μΩ·cm), which will result in a larger ohmic loss in comparison with that of Cu (1.7 μΩ·cm) and Au (2.2 μΩ·cm), the insertion loss performance is, therefore, worse than Wu's result (−0.065 dB at 40 GHz). Figure 3.11(b) shows the comparison results of the transition on the SU-8/PDMS substrate with the CPW made by either Cu (8 μm)/Ni (1 μm)/Au (0.4 μm) or pure Au (9.4 μm), respectively. The insertion loss of one transition can be reduced down to −0.14 dB due to lower metal loss once the material of CPW is changed from Cu/Ni/Au to pure Au. Although there is still −0.075 dB loss difference between our technology and Wu's work, the first demonstration of the integration of CMOS chip to a flexible substrate with the characteristics of small bonding pad (minimum 10.5 μmin width) and simple structure design has revealed the potential of this technology for the integration of high-performance flexible wireless microsystems.

Figure 3.12 shows optical photographs of the SU-8 film assembled with a CMOS chip, released from the handle wafer and attached to a PDMS film, respectively. In addition, the bended morphology of the SU-8 substrate, as shown in Figure 3.12(a), reveals the existence of thermal stress resulting from coefficient of thermal expansion (CTE) mismatch between SU-8 and Cu sacrificial layer. Nevertheless, the thermal stress issue could be improved by well-chosen sacrificial material and SU-8 process condition optimization and thickness control. In addition, the released SU-8 substrate can be attached to a thick stress-free PDMS substrate for supporting to enhance mechanical reliability as shown in Figure 3.12(b). The bonding strength of the low temperature Au-Au bonds is qualitatively characterized by forcefully separating two bonded substrates as shown in Figure 3.13. The designed four alignment marks are fully stripped away from the SU-8 and bonded to the CMOS chip after breaking the bonded interface. This result indicates the bonding is reliable and uniform within all bonding pads and the bonding strength is larger than the adhesion force between Ti and SU-8 interface which is about 6MPa [80].

The proposed wafer-level chip scale flexible microsystem fabrication technology is demonstrated as shown in Figure 3.14. Forty separated SU-8 dies whose size is 9.5×6mm^2 are patterned on a 4-inch Si wafer with a Cu sacrificial layer. After the formation of metal interconnections and surface cleaning, twelve Si chips are bonded onto twelve flexible substrates on the silicon handle wafer, respectively, as shown in Figure 3.14(c). Therefore, the twelve flexible microsystem "dies" can be fabricated simultaneously after the sacrificial release process. It is worth to mention that the consideration of a temperature hierarchy for bonding is no more required in the proposed integration scheme. In order to preserve structural integrity and mechanical stability of all assembly parts, temperature hierarchy should be carefully considered in the entire assembly process to prevent remelting of the joined solder bumps in subsequent flip chip assembly. Au-Au bonds can totally avoid this issue due to no melt occurrence at bonding temperature. Figure 3.15 shows enlarged optical photographs of a flexible substrate which is immersion into Cu etchant for removing the sacrificial layer after 1mins, 10mins, 20mins and 25mins, respectively. Due to the transparency characteristic of SU-8, the removal of Cu sacrificial layer underneath the SU-8 substrate can be clearly observed to check whether the process is completed.

In comparisons with the prior works proposed for flexible microsystem fabrication as listed in Table 3.3 [69, 71-74], the presented integration scheme and wafer-level processes have shown a great potential for future flexible wireless microsystem fabrication in terms of good interconnection performance for high frequency chip integration, heterogeneous integration capability for good process flexibility, and wafer-level processing capability for low manufacturing cost.

3.4 An SU-8 Flexible Ribbon Cable

Recent research progress on the development of biomedical microsystems mainly focused on the design and fabrication of micromachined biomedical devices, such as silicon neural probes, ultrasonic transducers and so on [81,82]. However, it is also very critical to have flexible and reliable electrical interconnection from these micromachined devices to external instruments for better system performance, especially when the microsystems are used for in vivo monitoring. There are two kinds of interconnection technologies, i.e. wireless and wire, for such applications. Wireless interconnection can also be called "active connection" requiring power to transmit and receive signal. Although the wireless interconnecting system can offer many benefits in untethering the subjects from bulky external hardware [83], it is inevitable to have a complicate hardware system in the medical devices for obeying the federal wireless regulation [84]. In contrast, the wire interconnect scheme can provide a simple but secure and robust solution for the microsystem especially for in-situ operation applications. The only technical challenge in the development of the wire interconnections is the design and fabrication of a flexible and scalable wire.

Several polymer cables and assembly methods have been developed for flexible interconnecting applications [85-89]. Nevertheless, complex process steps based on the simultaneous usage of polyimide and parylene and impracticality for the integration of various chips have led to a new exploratory regarding the flexible interconnecting scheme for biomedical microsystem applications. Thus, a flexible interconnecting scheme as shown in Figure 3.16 is presented by adopting a SU-8 flexible ribbon cable to integrate biomedical devices with a system-on-package (SOP) circuit system. SU-8, a negative photoresist (PR), has been widely used in BioMEMS fabrication owing to its superior material and process characteristics, such as photo-patternable, chemical stable, biocompatible and suitable for fabricating a feature with a high aspect ratio in terms of thickness control…etc., which make SU-8 suitable for the fabrication of flexible cable. Furthermore, the traditional flexible cables usually provide a short distance interconnection (only several cm) and have little stress relief capability easily resulting in cable breakage and failure during biomedical device handling. Previously, Huang *et al.* demonstrated a 3-D parylene coiled cable which is able to be stretched by 100% of its original length for prosthesis application [89]. In the coiled cable fabrication, since a 48 hours heat treatment at 200°C in vacuum is needed to form the coiled structure, it becomes impractical for mass production. Therefore, a new flexible cable structure is developed and implemented in the proposed integration scheme to provide a robust and reliable flexible interconnection in the work.

Via a wafer-level sacrificial release process for the SU-8 spiral ribbon fabrication and the previously developed low temperature bumpless Au-Au thermocompressive bonding process [7,10], a low cost and reliable heterogeneous integration of biomedical microsystems, such as a Si neural probing system interfaced with a system-on-package (SOP) circuits, can be truly realized.

3.4.1 Flexible Interconnection Design and Fabrication

For the purpose of large actuation displacement, low driving voltage, small dimension and so on, structures, such as serpentine spring and spiral spring, have been widely used in MEMS sensors and actuators designs to replace straight line structure as a result of a low stiffness. The spring constant of a simple cantilever beam, k_{beam}, and the spiral spring, k_{spiral} consisting of two semicircular beams can be calculated, respectively, as follows [90]:

$$k_{beam} = \frac{3EI}{L^3} \tag{3.3}$$

$$k_{spiral} = \frac{2}{\pi}\left(\frac{R_1^3 + 4R_1^2R_2 - 4R_1R_2^2 + R_2^3}{EI} + \frac{3R_1^3 + 4R_1^2R_2 - 4R_1R_2^2 + 3R_2^3}{GJ}\right)^{-1} \tag{3.4}$$

where E, G, I, J, L and R_1 and R_2 are young's modulus, shear modulus, moment of inertia, polar moment of inertia, length of cantilever beam, and average radius of the first and second semicircular beams, respectively. Therefore, for the same design of a 50μm in width and 50μm thick structure made of SU-8, the spring constants are 9.81×10^{-5} N/m and 5.76×10^{-5} N/m for a 4cm long cantilever spring and a spiral spring where the first and second beam radii are designed with 1.2 cm and 2 cm, respectively. Obviously, the spiral spring structure has a lower stiffness than the cantilever beam which makes itself suitable for being used in the structure design of a flexible ribbon cable.

A SU-8 spiral ribbon structure designed with 10 semicircular beams, 4 mm in width, 82.6 cm in total length and 4 mm line spacing, respectively, is fabricated on a 4" silicon wafer for the demonstration of a long flexible electrical interconnect between a biomedical probe and an interface circuitry system which performs bio-signal processing. The three different metal line structures embedded in two layers of SU-8, whose line width/spacing/number of metal lines are designed with 200μm/100μm/12, 100μm/100μm/20, and 50μm/50μm/40, respectively, are then fabricated on the ribbon to demonstrate the feasibility for sensor array which needs a large number of interconnections.

The whole process sequence of the proposed flexible interconnecting scheme is listed as follows: a silicon handling substrate is first sputtered with 10nm/300nm thick Cr/Cu as a sacrificial layer followed by 26μm thick SU-8 (Gersteltec Sarl GM 1060) spin-coating. After photo-patterning the SU-8 with the aforementioned spiral structure, the SU-8 is hard-baked at 200°C for 2 hours in order to make a fully cross-linked SU-8, as shown in Figure 3.17(a), for having a higher glass transition temperature (T_g). Figure 3.17(b) shows that a 10nm/90nm Ti/Cu seeding layer is deposited on the SU-8 and followed by a photolithograph process using a 7μm thick AZ 4620 photo-resist to define the region for the metal lines. After electroplating a 5μm thick copper on that region, a serial of processes including 1μm electroless Ni and 0.4μm electroless Au plating are performed to metallize the Cu surface for later bonding as shown in Figure 3.17(c). Figure 3.17(d) shows that AZ 4620 and Ti/Cu seed layer are then removed using ACE, CR-7T, and then BOE, sequentially. Finally, the SU-8 ribbon cable is ready for bonding with a biomedical device after a secondary 26μm thick SU-8 spin-coating and patterning step to protect the Cu metal line. Once the biomedical device is assembled with the inner end of the ribbon cable using low temperature Au-Au TC bonding, the sacrificial Cr/Cu layer is chemically etched away in Cu etchant (100:5:5 H_2O:CH_3COOH:H_2O_2) to release the SU-8 ribbon cable from the handling wafer as shown in Figure 3.17(e).

3.4.2 Results and Discussions

Figure 3.18 shows optical photographs of the as-fabricated SU-8 flexible ribbon with metal interconnection lines before sacrificial release. The enlarged optical photograph of the SU-8 flexible ribbons with 200μm, 100μm, and 50μm wide Au lines are shown in Figure 3.18(b), (c), and (d), respectively. Figure 3.19 shows the micrographs taken from one end of SU-8 flexible ribbon before and after sacrificial release in Cu etching solution. Due to the transparency characteristic of SU-8 under an optical microscope, the removal of Cu sacrificial layer underneath the SU-8 ribbon can be clearly observed to check whether the process is completed.

While handling a biomedical device with the ribbon, the low stiffness in the spiral structure design in comparison with that in a straight line cable can not only increase an out-of-plane displacement but also play the role of a spring to ease the stress built on the assembly joint between the device and cable. The stress release can effectively avoid possible bonding reliability issues during the device handling. Figure 3.20(a) and (b) show the comparison between the experimental and ANSYS simulation about a 22 cm long SU-8 flexible ribbon deformation under gravity load. About the same vertical displacement (3.5 cm) and similar deformation shape predictions indicate the correctness of the simulation. Figure 3.20(c) and (d) further show the simulated SU-8 ribbon deformation shape and stress distribution respectively for a 5 cm vertical displacement at the outer end. The result indicates that the stress near the bonding area can be restrained for about 0.6 MPa.

The proposed heterogeneous integration scheme of biomedical microsystems is preliminarily demonstrated as shown in Figure 3.21(a). A micromachined Si probe with polysilicon resistance temperature detectors (RTDs) is bonded with a 2.4cm long SU-8 flexible ribbon using proposed low-temperature Au-Au TC bonding after the sacrificial release from the Si handling wafer. A push-pull test is performed to characterize shear bonding strength which is about 3.3 MPa and obviously larger than the aforementioned simulated stress, i.e. 0.6 MPa. Furthermore, partial Ni/Au bonding pad on the silicon probe is broken and pulled away after the push-pull test as shown in Figure 3.21(b). It indicates that the bonding strength of the proposed low temperature Au-Au TC bonding is as strong as the adhesion force of the Ti layer under the bond pad to silicon. Figure 3.22 shows the resistance measurements of the temperature probe before and after bonding with the SU-8/Cu flexible cable for the temperature coefficient of resistance (TCR) characterization [91]. The resistance versus temperature measurement validates the linear relationship and shows less than 5% TCR variation resulted by the integration of flexible interconnects. Thus, the SU-8 flexible ribbon cable reveals the potential of clinical applications like microsurgical tools for electrically connecting the in-situ microdevices to outside instruments.

3.5 Summary

In this chapter, two SU-8 based low-temperature process techniques, including a SU-8 micromachining process for RF MEMS passive fabrication and a low temperature Au-Au TC bonding for chip integration on SU-8, are presented for RF SOP applications on flexible organic substrate. A low-temperature micromachining process for the fabrication of SU-8 RF MEMS series switches has been developed and demonstrated. Owing to the low processing temperature characteristics, which can be kept below 135°C, and the simple spin-coating process, the proposed micromachining process can provide an alternative for making other RF MEMS components such as tunable capacitor, inductor and antenna for flexible RF applications. Next, a flexible wireless microsystem fabrication scheme in regard to wafer-level sacrificial release process and low temperature Au-Au TC bonding has been successfully demonstrated with a good broadband electrical performance and reliable bonding strength within CMOS chips and polymer substrates. By adopting a surface cleaning step, bonding temperature of Au–Au bond can be lower than 200°C. Not only CMOS chips but also other heterogeneous chips, like MEMS and III-V chips, can be fully integrated with a flexible organic substrate using the proposed technology to form a high performance wireless microsystem. Besides, a SU-8 flexible ribbon cable has been successfully fabricated using the proposed flexible microsystem fabrication scheme. In this work, low temperature Au-Au TC bonding is utilized for electrically and mechanically joining within various chips by the flexible cable. Such a SU-8 ribbon with the characteristics of simple process, low stress spiral structure, and high density metal interconnects has shown its potential application for the heterogeneous integration of biomedical microsystems.

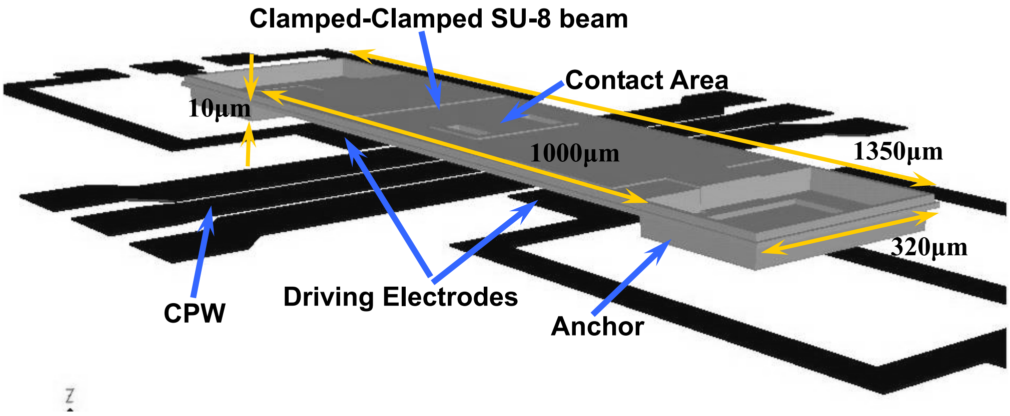


Figure 3.1 The scheme of clamped-clamped SU-8 beam MEMS series switch.

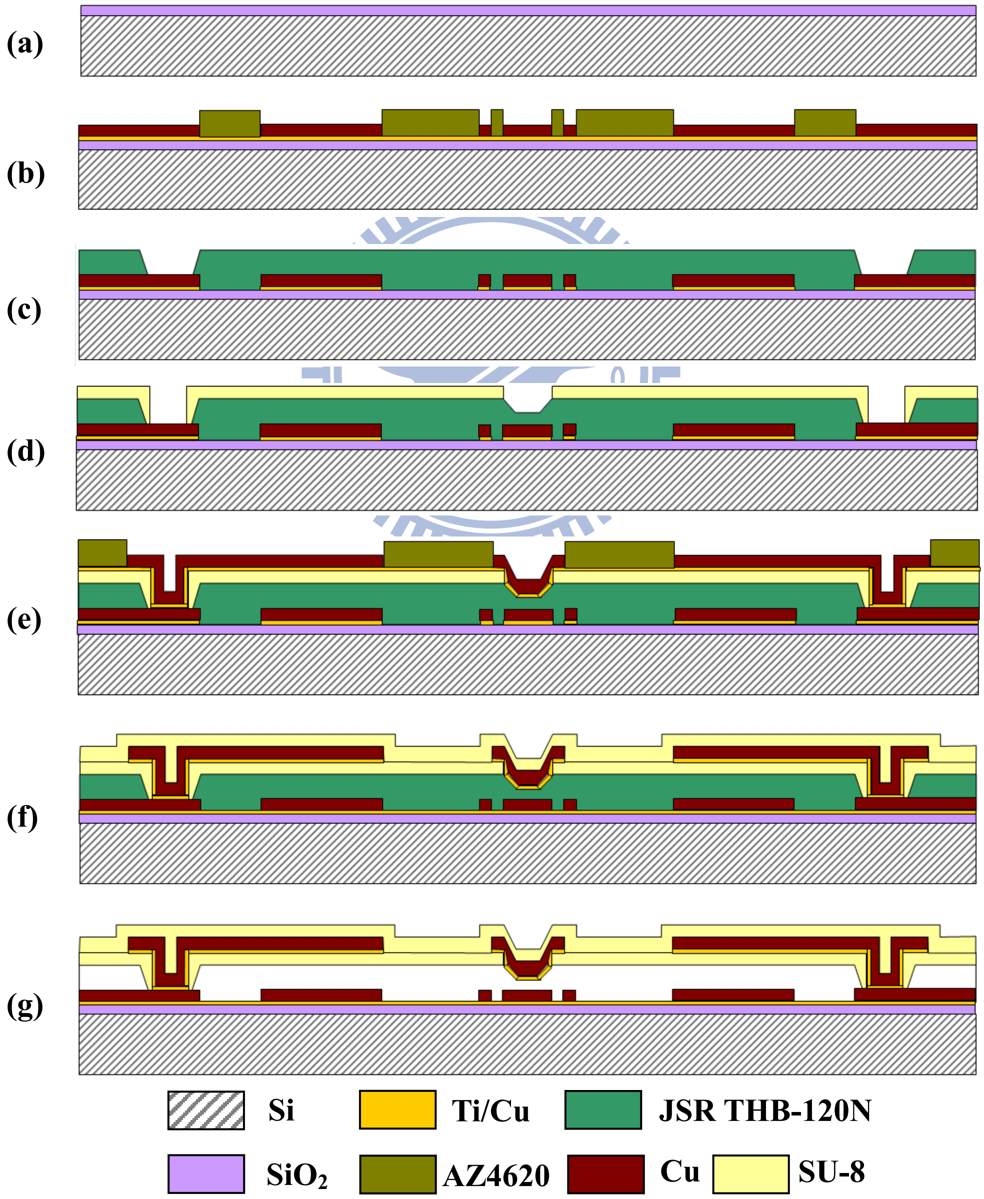


Figure 3.2 The schematic process flow of proposed SU-8 serial MEMS switch.

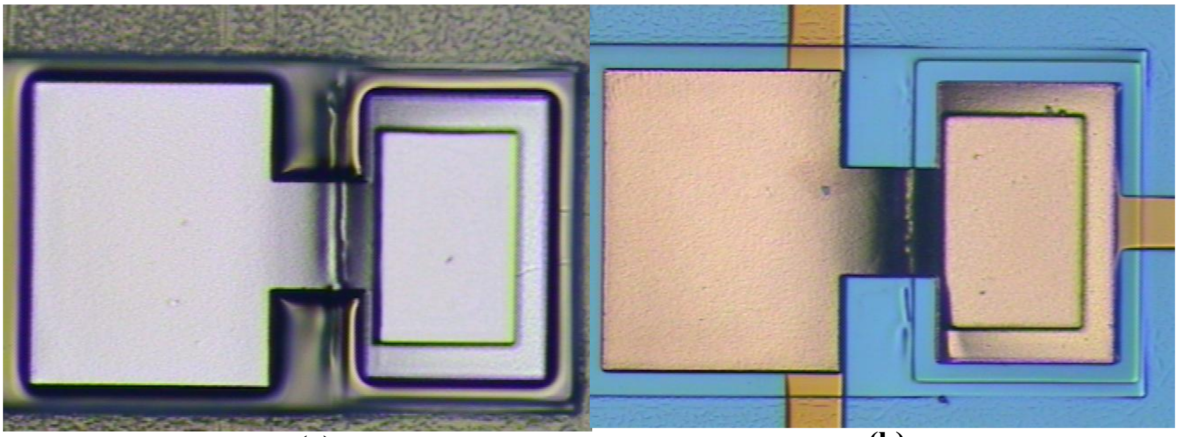

(a) (b)

Figure 3.3 Optical micrographs of the enlarged view on the area of driving electrode of the switch (a) before and (b) after sacrificial JSR layer removal.

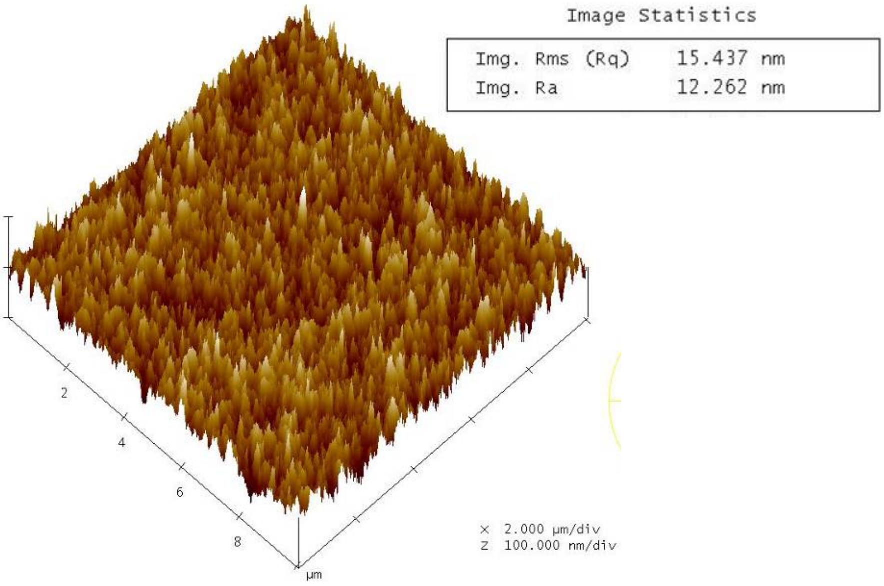


Figure 3.4 The AFM 3D profile image and average roughness of electroplating Cu surface.

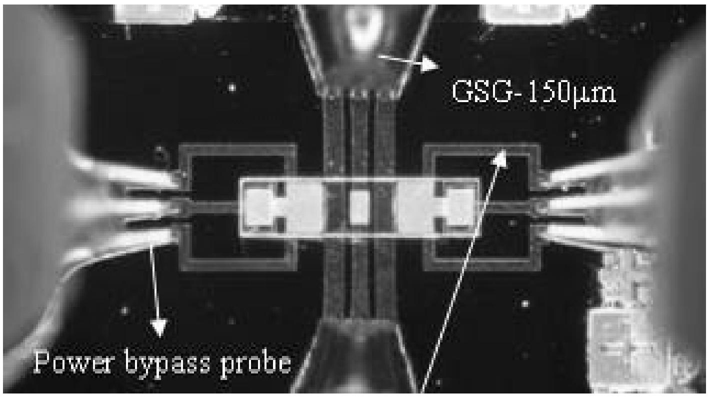


Figure 3.5 High frequency measurement setup for the MEMS switch.

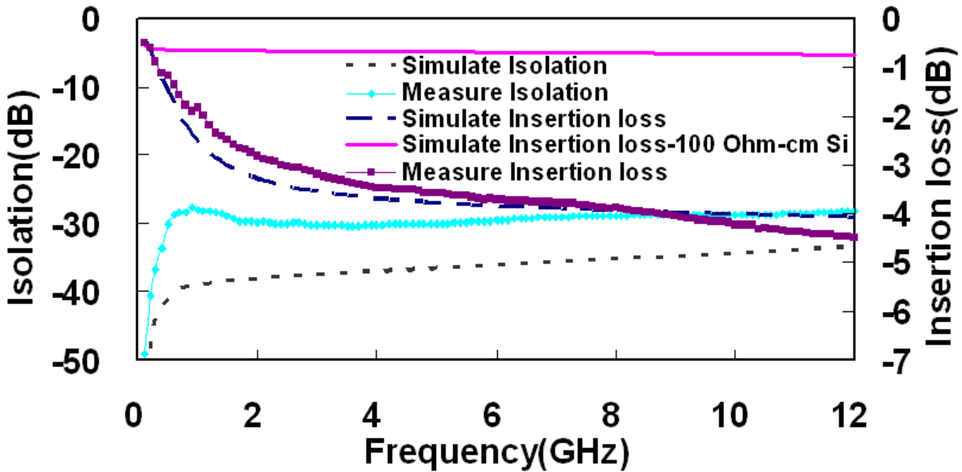


Figure 3.6 The measurement and simulation results of the SU-8 switch while the switch is operated at “on” and “off” states.

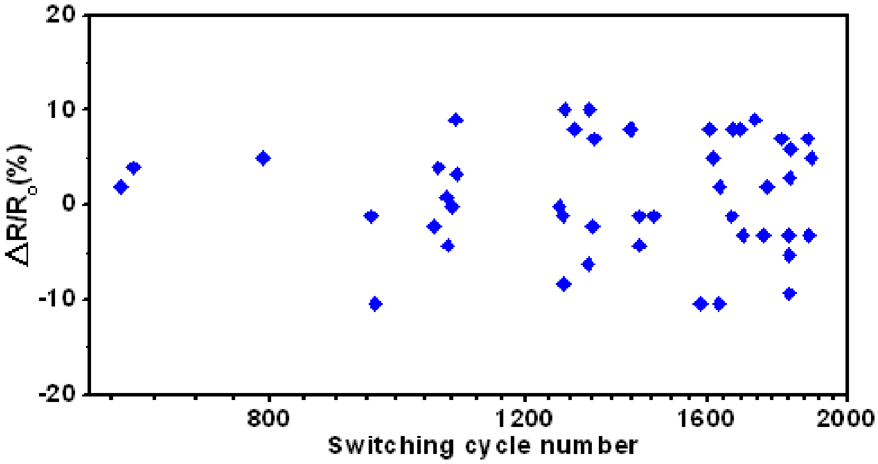


Figure 3.7 The percentage of contact resistance deviation of SU-8 MEMS switch at preliminary 2000 times cycling test.

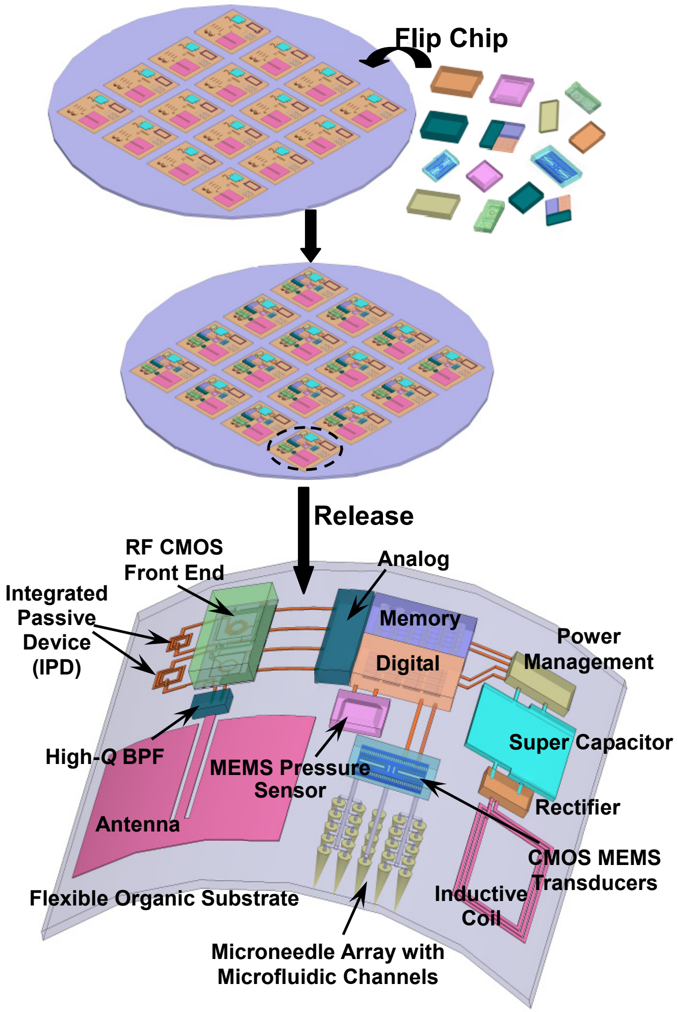


Figure 3.8 Scheme of wafer-level chip scale flexible wireless microsystem fabrication.

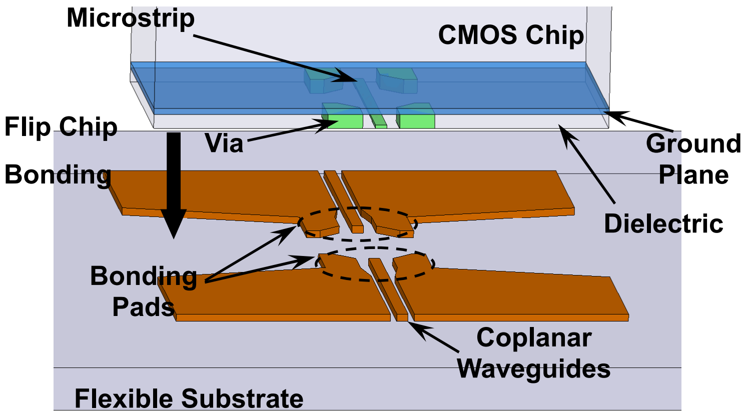


Figure 3.9 Scheme of designed interconnection structure includes two coplanar waveguides (CPWs) on flexible substrate and microstrip on CMOS chip for characterization of the proposed integration technology.

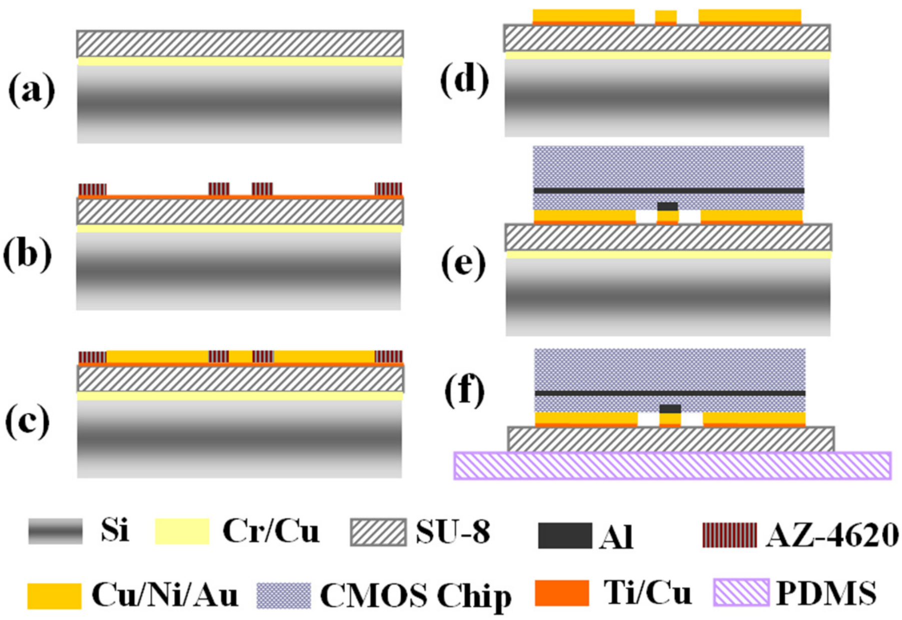


Figure 3.10 Scheme of the integration process. (a) Deposition of a Cr/Cu sacrificial layer covered with a fully cured SU-8. (b) Ti/Cu seed layer deposition with PR patterning on the top. (c) Cu plating for the fabrication of CPW structure, followed by electroless Ni/Au plating for bonding. (d) PR and seed layer removal. (e) CMOS chip to SU-8 substrate bonding. (f) Si handle wafer detachment by sacrificial layer release in Cu etchant and then SU-8 film attachment on PDMS.

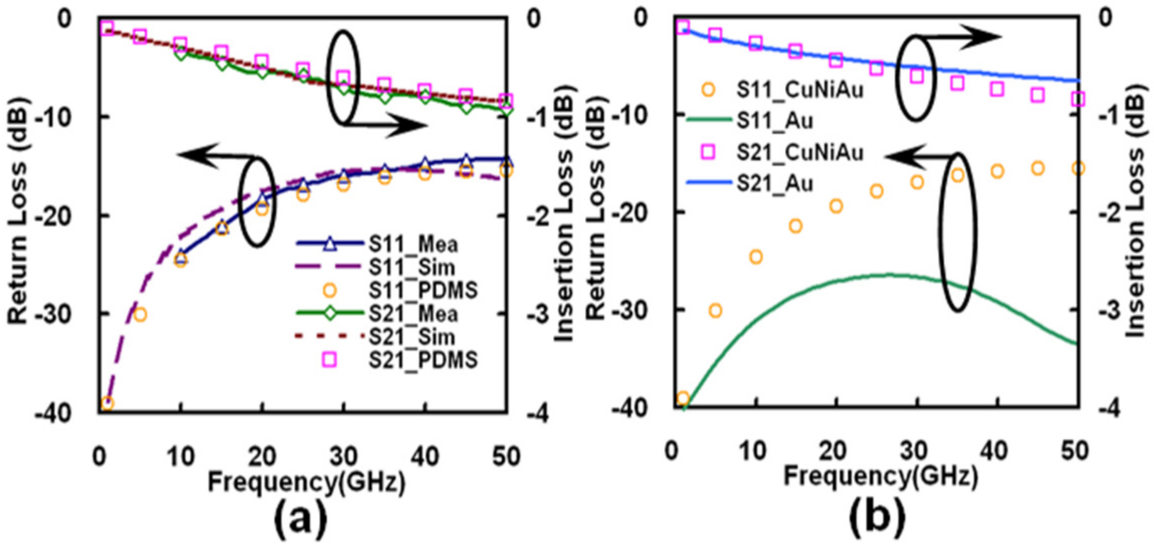
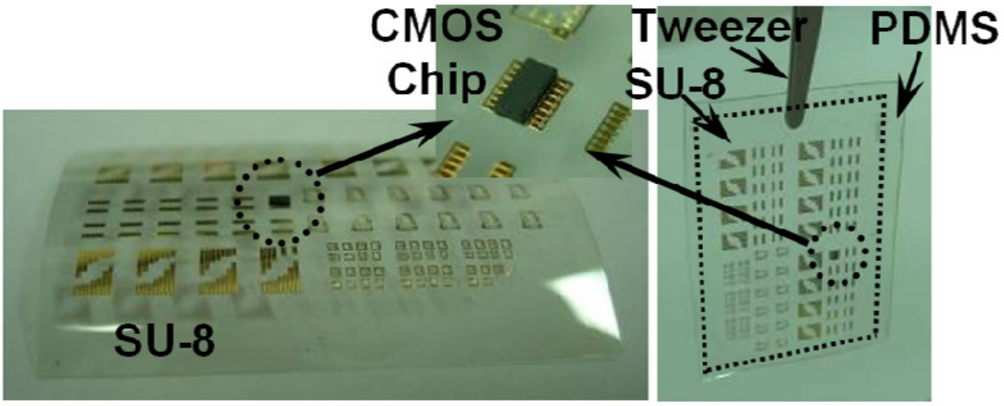
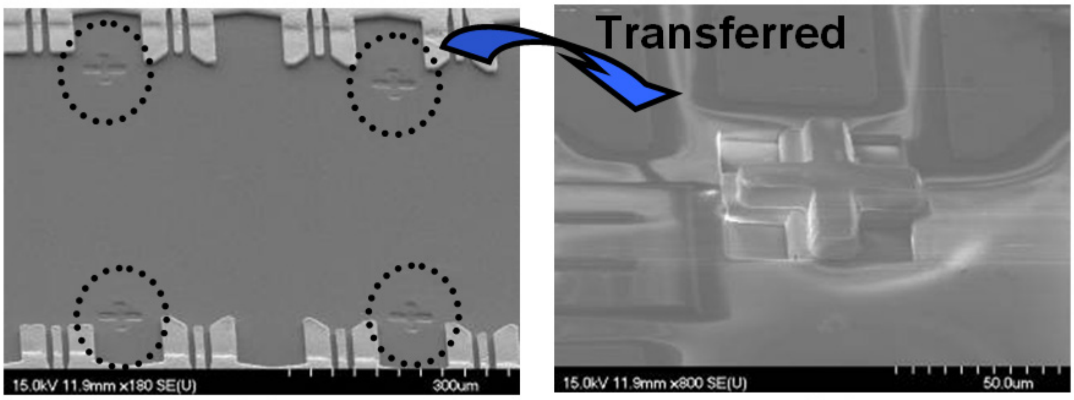


Figure 3.11 (a) Comparison of the RF measurements and HFSS simulations on SU-8/Si and on SU-8/PDMS, respectively, of the designed transition structure. (b) Comparison of the simulation results of the transition on SU-8/PDMS with CPW made by either Cu/Ni/Au or pure Au, respectively.



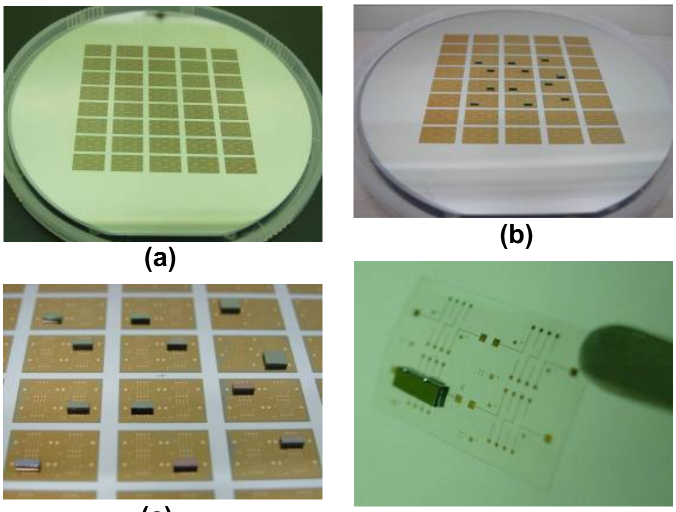
(a) (b)

Figure 3.12 The optical photographs of (a) the detached SU-8 substrate, the enlarged inset photograph shows CMOS chip successfully bonded onto SU-8 substrate. (b) SU-8 attaches to thick PDMS substrate.



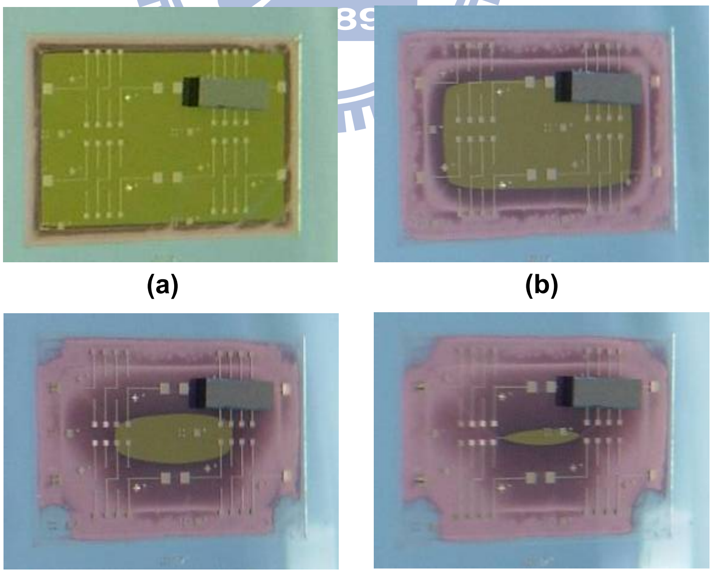
(a) (b)

Figure 3.13 Enlarged SEM micrographs of two bonded substrates, CMOS and SU-8 respectively, after forcefully separating the compressive bond. (a) The four alignment marks totally torn away from the SU-8 substrate, and (b) transferred onto the CMOS chip.



(a) (b) (c) (d)

Figure 3.14 The optical photographs of the demonstration of wafer-level chip scale flexible microsystem fabrication. (a) A 4-inchs Si wafer is patterned with forty separated SU-8 which each size is 9.5×6mm^2, (b) twelve chips are bonded to twelve flexible substrate, respectively, (c) the enlarged view on the area of twelve bonded flexible microsystem before sacrificial release, and (d) released flexible microsystem “die”.



(a) (b) (c) (d)

Figure 3.15 The optical photographs of a SU-8 flexible substrate which is immersion into Cu etchant after (a) 1mins, (b) 10mins, (c) 20mins and (d) 25mins, respectively.

Table 3.1 Surface element content analysis by XPS before and after acidic surface cleaning

Cleaning time (seconds)	Surface Contents (at.%)		
	C	O	Au
0	1.71	56.38	41.91
180	1.45	33.95	64.4

Table 3.2 Specific contact resistance vs. bonding temperature

Temperature(°C)	160	200	240
SCR(10^{-7} Ω·cm^2)	5.65±1.86	4.74±1.69	2.84±1.03

Table 3.3 Comparisons between previously developed technologies and this work.

	Ref. [69]	***Ref. [71]***	***Ref. [72]***	***Ref. [73]***	***Ref. [74]***	***This Work***
Method	Direct Fabrication	Transfer Printing	Wafer Transfer	Lateral Interconnection	Convectional Flip Chip	Bumpless Au-Au TC Bonding
Substrate Material	PI	PI/PDMS	FR4	N/A	PI or LCP	SU-8/PDMS
Wafer-level Process	Yes	Yes	Yes	Yes	No	Yes
Process Complexity	Simple	Complex	Complex	Complex	Simple	Simple
Multi-Chip Module	Incapable	Incapable	Incapable	Capable	Capable	Capable
Heterogeneous Integration	Incapable	Incapable	Incapable	Capable	Capable	Capable
High Frequency Performance	Poor	Moderate	Moderate	Poor	Moderate	Good

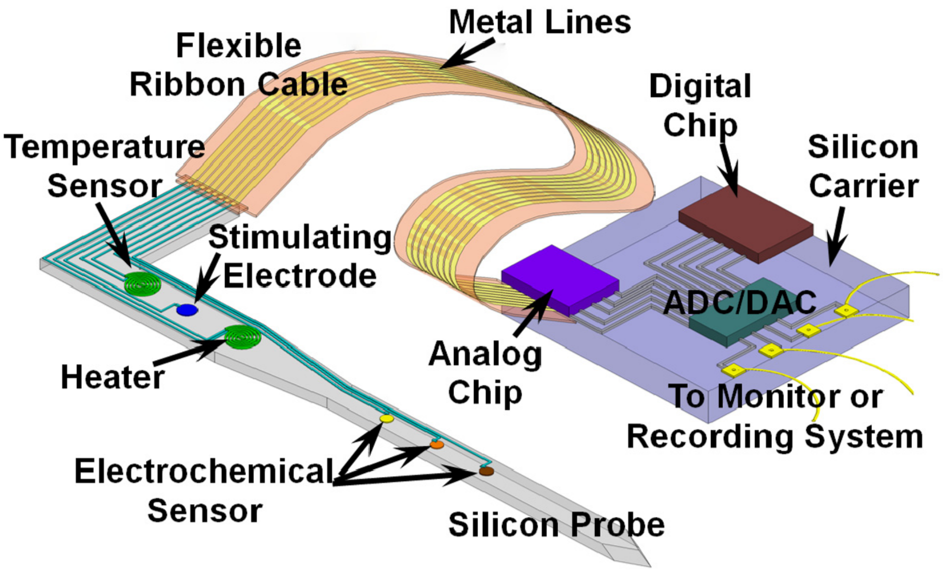


Figure 3.16 Scheme of the heterogeneous integration of biomedical microsystems. A Si neural probe is interfaced with a system-on-package (SOP) circuit system via the SU-8 flexible ribbon cable using a low-temperature bumpless Au-Au thermocompressive bond.

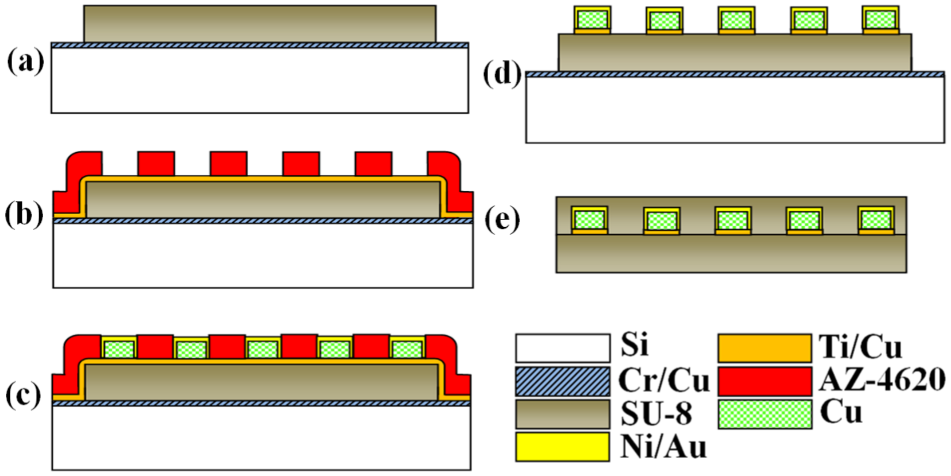
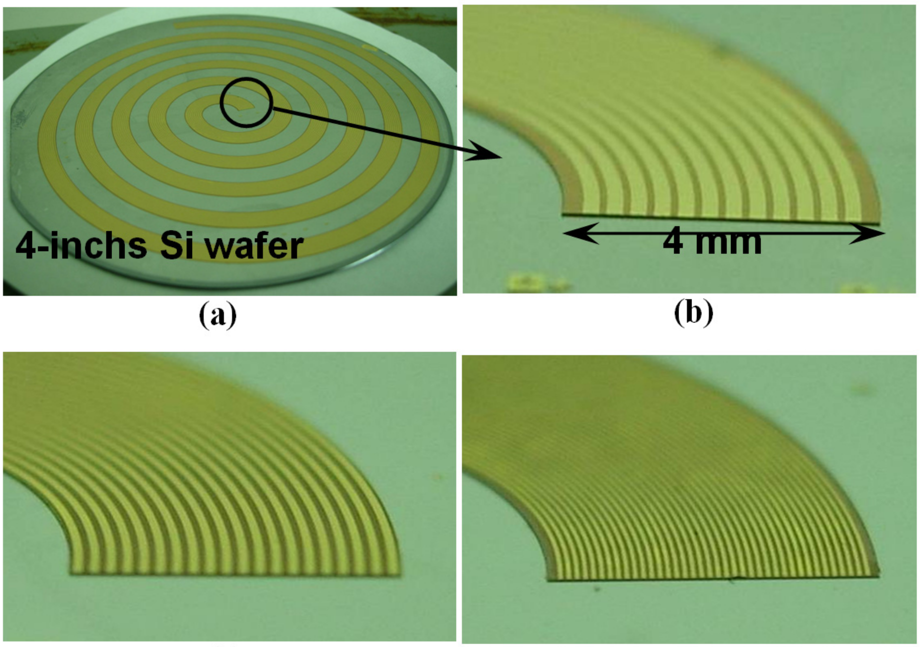


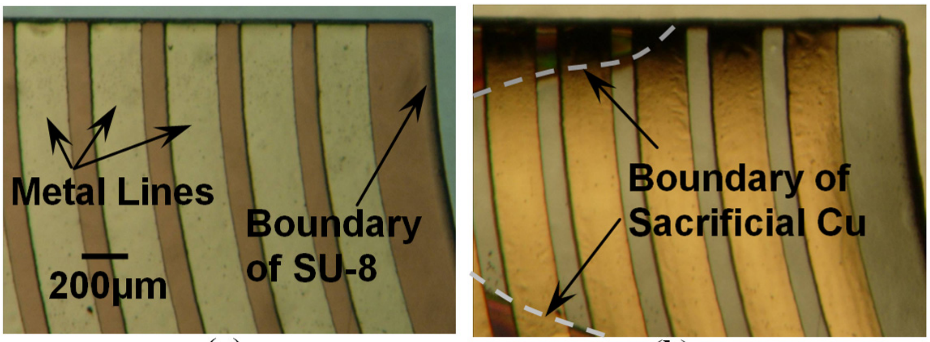
Figure 3.17 The fabrication processes of the proposed SU-8 flexible ribbon cable. (a) Deposition of (10nm) Cr/ (300nm) Cu sacrificial layer and 26μm fully cured SU-8. (b) Deposition of (10nm) Ti/ (90nm) Cu seeding layer and spin coating 7μm AZ-4620 to define metal lines. (c) 5μm thick copper electroplating to make metal structure followed by a series of (1μm) electroless Ni and (0.4μm) Au plating. (d) PR and seeding layer removal. (e) Secondary SU-8 deposition and then etching sacrificial layer in Cu etchant to remove Si handle wafer.



(a) (b)

(c) (d)

Figure 3.18 Optical photographs of as-fabricated SU-8 flexible ribbon cable. (a) The SU-8 is patterned as spiral structure for long electrical interconnection. Enlarge view on the one end of SU-8 ribbon, the width of metal lines are designed with (b) 200µm, (c) 100µm, and (d) 50µm, respectively.



(a) (b)

Figure 3.19 Optical micrographs of the enlarged view on the area of the one end of SU-8 flexible ribbon (a) before and (a) after sacrificial layer removal.

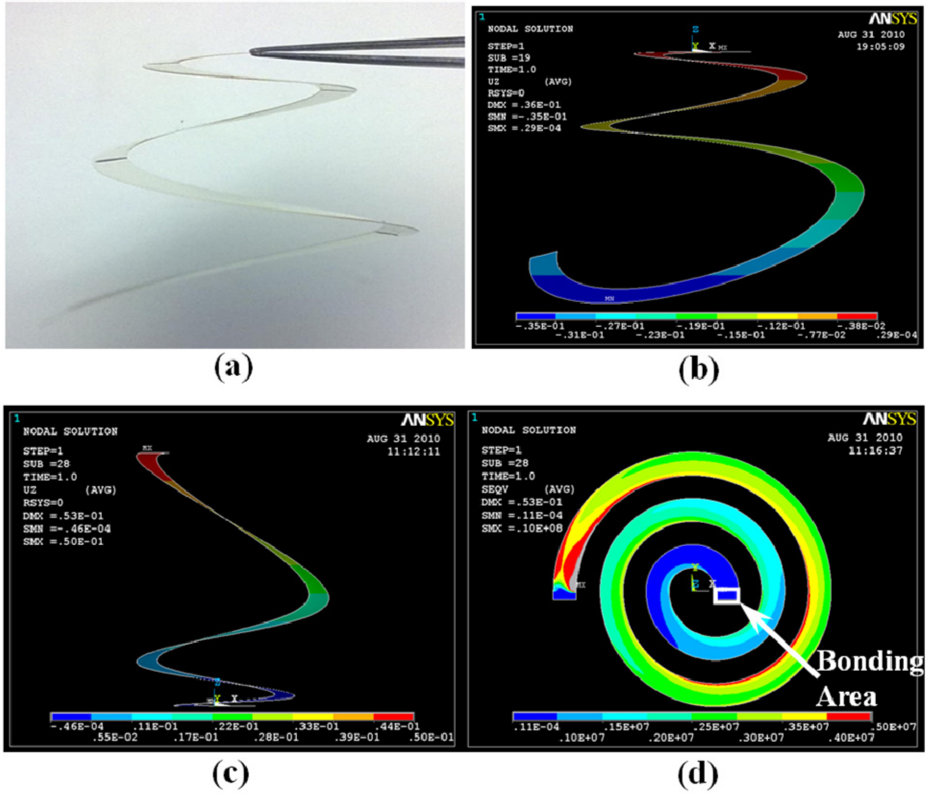


Figure 3.20 (a) Experiment and (b) ANSYS simulation of SU-8 ribbon hang down under gravity force. ANSYS simulated (c) out-of-plane deformation and (d) stress distribution of the 3.5-turn, 22cm long, 4mm width and 52μm thick SU-8 spiral ribbon under the condition of 5cm vertical displacement in outer end.

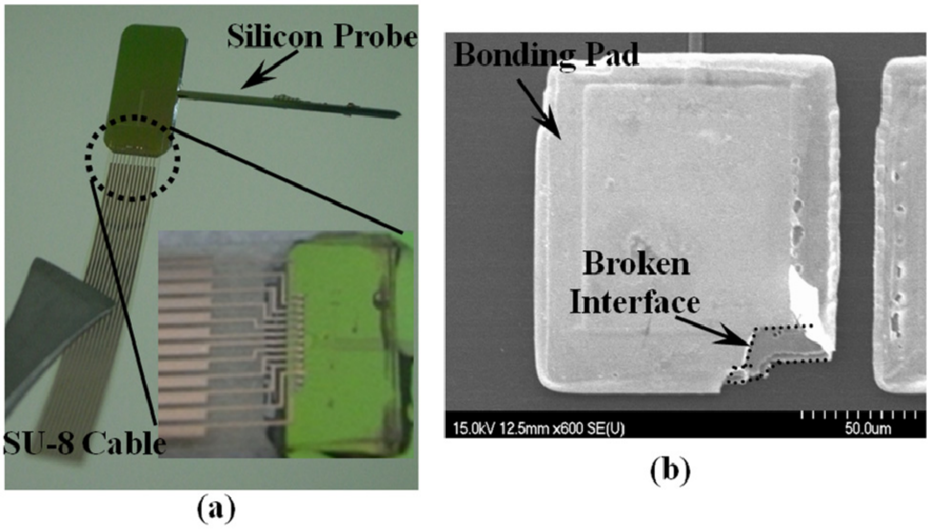


Figure 3.21 (a) Optical photograph of micromachined silicon probe bonded with a 2.4cm SU-8 flexible ribbon cable with 12 interconnect line after sacrificial release from Si handle substrate and inset enlarged view on the area of bonding pads, and (b) SEM photograph of broken metal pad on silicon probe after the push-pull test.

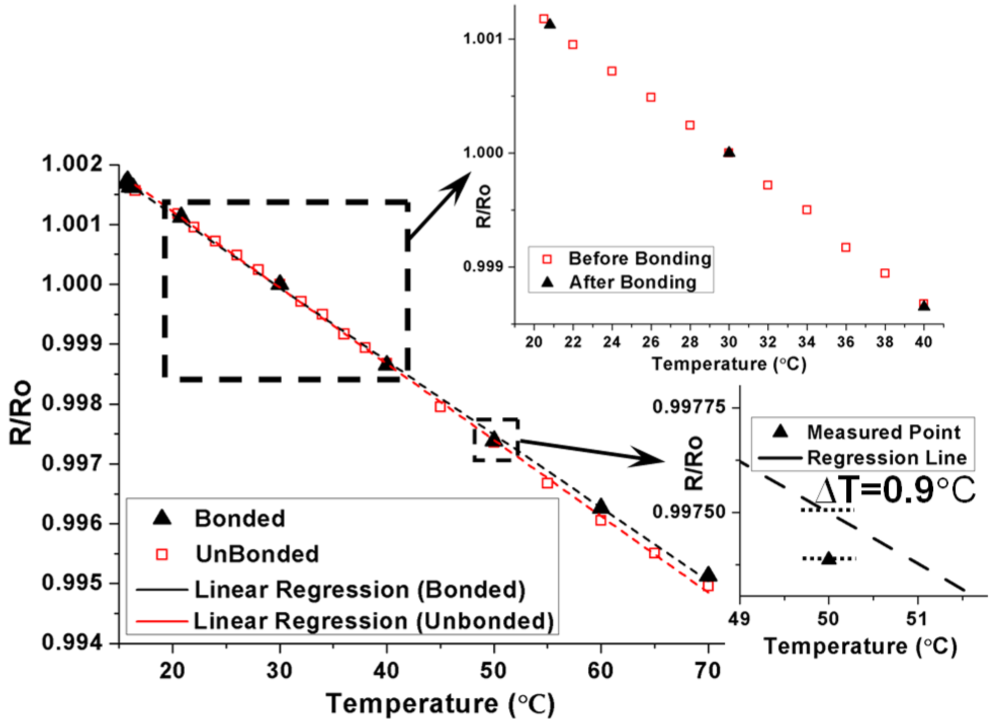


Figure 3.22 Relative resistance variation of the temperature sensor before and after bonded with ribbon cable. The resistances are measured from about 15°C to 70°C and then normalized with the resistance at 30°C (R_0). The upper right inset shows the measured result from 20°C to 40°C and the lower right inset shows the sensing accuracy is ~0.9°C.

Chapter 4 Ferromagnetic-AAO Nanocomposite for Performance Enhancement of On-Chip Spiral Inductors

4.1 Introduction

One of the technical challenges in the cost reduction and performance boost of RFIC for consumer electronic applications is how to effectively reduce the area occupation of on-chip inductors. For instance, on-chip inductors for GHz RFIC operation ranging from 1.5 to 3.5 nH can have the size of 0.06 to 0.08 mm^2 [92]. The larger size the inductor is, the higher inductance it can have. In addition, it is required to have at least three inductors for a second order bandpass filter design whose size will be up to 0.62 mm^2 [93]. In general, inductor performance including the inductance and *Q* factor can be enhanced via the incorporation of ferromagnetic material for the size reduction of the inductor associated with less eddy current and resistive losses. However, such inductors usually accompany with poor performance at high frequency resulted by ferromagnetic resonance (FMR) effect and the eddy current loss occurrence in the layer of magnetic material [94-97].

The inductance, L, is the ability of an inductor to store energy in a magnetic field which is induced by current source, I, passing through the metal coil of inductor. Thus, the inductance can be derived with the associated magnetic energy, W_m, in the inductor [98]:

$$L = \frac{2W_m}{I^2} \qquad (4.1)$$

$$W_m = \frac{1}{2}\int_V \vec{H} \cdot \vec{B} dv \qquad (4.2)$$

$$\vec{B} = \mu_0\left(\vec{H} + \vec{M}\right) = \mu_0(1 + \chi_m)\vec{H} = \mu_0\mu_r\vec{H} \qquad (4.3)$$

where μ_0, μ_r, χ_m, $\vec{B}$, $\vec{H}$, $\vec{M}$ are the permeability of free space, relative permeability, magnetic susceptibility, magnetic flux density, magnetic field, and magnetization of the medium, respectively. The ferromagnetic-integrated inductor takes the advantage of high permeability of ferromagnetic material to amplify the magnetic flux density. As equation (4.3), the magnetization of ferromagnetic will align with the magnetic field, $\vec{H}$, of inductor which is generated by current source and, therefore, increase stored magnetic energy and inductance. Thus, the reversal of magnetization of ferromagnetic following the high frequency electromagnetic field is a key issue for the performance enhancement of inductor.

There are two primary modes of magnetization reversal following the applied magnetic field: domain-wall motion and magnetization rotation. However, previous researches have reported that domain-wall motion only can follow external magnetic field change up to ~100 MHz while magnetization rotation does so all the way up to GHz [99]. The available frequency range of magnetization rotation is limited by FMR (Ferromagnetic Resonance Effect) effect resulting in strong absorption of high frequency EM field in ferromagnetic materials when the frequency of applied EM field near the frequency of Larmor precession of magnetic moments known as the Larmor frequency [100]. While the frequency of EM field is larger than the FMR frequency of ferromagnetic, the magnetization no longer follows the change of applied EM field and results in negative permeability characteristic [101]. There is no more contribution from the magnetization to the aforementioned inductance enhancement. The basic theory of ferromagnetic resonance is provided as follow.

The discussion of FMR starts form precessing of magnetic dipole moment, $\vec{M}$, about a magnetic field, $\vec{H}$, as shown in Figure 4.1 [102]. When a magnetic moment is placed in a magnetic field, the magnetic field exerts a torque on it then produces a change in angular momentum which is perpendicular to that angular momentum, causing the magnetic moment to precess around the direction of the magnetic field. This is called Larmor precession. The basic equation for modeling the precessional motion of magnetization is the simplified Landau–Lifshitz–Gilbert equation [103]:

$$\frac{d\vec{M}}{dt} = -\gamma \vec{M} \times \vec{H} \tag{4.4}$$

$$\vec{M} = M_x \hat{i} + M_y \hat{j} + M_z \hat{k} \tag{4.5}$$

$$\vec{H} = \vec{H}_{eff} + \vec{H}_{ac} \tag{4.6}$$

where γ is the gyromagnetic ratio. The magnetic field, $\vec{H}$, is vector sum of all fields acting upon the magnetization and including effective DC field, H_{eff}, along the z-axis and RF field, H_{ac}, applying in the x-axis. Because H_{ac} is much small than H_{eff}, under a strong enough static magnetic field, the magnetization of the materials is assumed to be saturated in z-direction, i.e. M_z is equal to M_s which is the saturation magnetization of ferromagnetic material. For the sample with finite size, the demagnetization effects raise resulting to shape anisotropy. Thus, according to (4.6), the actual magnetic field components inside the material should be modified as follow:

$$H_x = H_{ac} - N_x M_x \tag{4.7a}$$

$$H_y = -N_y M_y \tag{4.7b}$$

$$H_z = H_{eff} - N_z M_z \tag{4.7c}$$

where N_x, N_y, and N_z are demagnetization factors. The equation of motion (4.4) is then substituted by equation (4.7), the component equations of (4.4) become:

$$\frac{dM_x}{dt} = j\omega M_x = -\gamma [H_{eff} + (N_y - N_z) M_z] M_y \tag{4.8a}$$

$$\frac{dM_y}{dt} = j\omega M_y = \gamma[H_{eff} + (N_x - N_z)M_z]M_x \tag{4.8b}$$

$$\frac{dM_z}{dt} \cong 0 \tag{4.8c}$$

Finally, on solving above equations, the resonance frequency is given by:

$$f_{FMR} = \frac{\gamma}{2\pi}\sqrt{[H_{eff} + (N_y - N_z)M_s][H_{eff} + (N_x - N_z)M_s]} \tag{4.9}$$

For the case of the DC magnetic field is applied parallel to the surface of ferromagnetic film and assuming surface normal is along the *y*-axis, the demagnetization factors become N_x=N_z=0 and N_y=4π in cgs unit. The FMR frequency of a ferromagnetic film can be calculated as follows:

$$f_{FMR} \cong \frac{\gamma}{2\pi}\sqrt{(H_0 + H_k)(H_0 + H_k + 4\pi M_s)} \tag{4.10}$$

In fact, the effective DC field can be consist of a external magnetostatic field, H_0, and a effective anisotropy magnetic field, H_k, which is a internal field originating from crystal anisotropy, shape-dependent dipolar interactions, and exchange interactions. The natural FMR frequency (H_0=0) of the ferromagnetic film usually falls in a range of several hundred megahertz to 1 GHz, which is just coincident with the operational frequency range of the present wireless carrier frequencies. Since FMR effect would result in a large inductance variance in the region nearby the resonant frequency, such an inductor with ferromagnetic core is not suitable for RFIC applications. To effectively elevate the FMR frequency well above several gigahertz ranges for the practical application of the inductor with ferromagnetic core to RFIC,, it is required further study to improve material characteristics such as H_k and M_s since it is not a realistic to utilize a huge hard magnet to exert a large magnetostatic field H_0 on the inductors to boost the FMR frequency

According to (4.10), the increase of both H_k and M_s can effectively inhibit the occurrence of FMR effect by shifting the resonant frequency to several gigahertz range. Recently, Yamaguchi *et al.* have proposed a patterned magnetic CoNbZr layer [94] for modifying demagnetizing field distribution and thus the H_k of the magnetic layer can be enhanced to result in a higher FMR frequency up to 2 GHz. Viala *et al.* have demonstrated 100% hard axis excitation to ensure high H_k performance simply by devising FeHfN laminated film only under the metal structure of inductor [95]. Jiang *et al.* further proposed and employed anitferromagnetic/ferromagnetic multilayers (IrMn/CoFe) to increase H_k via the exchange-coupled mechanism without having any Q performance degradation [97]. Although these approaches can achieve the inductance enhancement and eliminate the disturbance resulted by the FMR phenomenon, CMOS-incompatible material, and complex fabrication processes make themselves not fascinating for real CMOS on-chip spiral inductor fabrication. Besides, it is still inevitable to have the eddy current loss existing in the layer of the magnetic materials. Previous work has reported that Ni-anodic alumina oxide (Ni-AAO) nanocomposite fabricating by electrodeposition of Ni into AAO template can have a high FMR frequency larger than 5 GHz without applying an external DC magnetic field. The composite exhibits a higher operation frequency owing to very high aspect ratio of the Ni nanowires [104]. Furthermore, since the Ni nanorods is grown within AAO template which is an electrical insulator to isolate each nanorod, the eddy current loss in the layer of the magnetic materials could be effectively reduced. Therefore, an inductance enhancement scheme using new composite materials that are ferromagnetic-AAO nanocomposites including Ni-P-AAO and NiFe-AAO with CMOS compatible fabrication processes is presented in this chapter. The schematic 3-D cross-sectional view of the proposed on-chip spiral inductor with ferromagnetic-AAO nanocomposite is shown in Figure 4.2.

The inductance enhancement scheme takes the advantage of magnetic shape anisotropy property of the rod-like structure which has a high aspect ratio to gain higher anisotropy field H_k [105] and the nanorods are well isolated with each other by the non-conductive AAO matrix to reduce eddy current loss induction within magnetic material. The eddy current is, therefore, restricted in a small area whose size is only in the order of nm^2. In comparison with the average power loss, which comes from eddy current induced by time-varying magnetic field, of a cylinder with radius of a, $P_{r=a}$, the power loss of N insulated cylinders with radius of b, $P_{r=b}$, can be calculated as follows:

$$P_{r=b} = N\frac{b^4}{a^4}P_{r=a} \cong \frac{b^2}{a^2}P_{r=a} \qquad (4.11)$$

where we assume the total conductive areas are the same for both cases, i.e. $N\pi b^2=\pi a^2$, the eddy current loss can be effectively suppressed in the isolated nanorods array owing to $b \ll a$.

Thus, in this chapter, a CMOS-compatible process is developed for high-performance spiral inductor fabrication in which Ni-P-AAO [106] or NiFe-AAO [107] magnetic nanocomposite layer is incorporated as a magnetic core, respectively. The related material synthesis, characterization, and device fabrication and performance measurement are depicted in detail as follows.

4.2 Ni-P-AAO Nanocomposite

4.2.1 Synthesis and Characterization

Porous AAO with uniformly self-organized hexagonal nanopores is made as the template for 1-D Ni nanorod synthesis. The template can be fabricated by anodizing Al film in various acidic solutions with certain processing parameters, such as applied voltage, current, temperature, and time, which are strongly correlated with the diameter and length of the nanopores [108,109]. In this study, AAO template is first synthesized by one-step anodizing process where Al film is applied with 40V in a 0.3 M oxalic acid ($H_2C_2O_4$) solution at room temperature until that the film is fully oxidized. The oxidized film is then annealed at 400°C for 2 hours for strengthening its structure. After thermal anneal, the AAO template is put in a 5% H_3PO_4 solution at 30°C for 50 min to form a uniformly distributed nanopore structure with the size of 70 nm in diameter, as shown in Figure 4.3(a).

For the synthesis of Ni-P-AAO nanocomposite, the as-fabricated AAO template is first dipped into $SnCl_2$ and $PdCl_2$ solutions for 2 min and 30 s, respectively, for AAO surface activation, which is followed by electroless Ni deposition at 60°C for 1 min. Once the top surface of Ni-P-AAO nanocomposite film is mechanically polished to remove overplated Ni the composite with electrically isolated Ni nanorods, as shown in Figure 4.3(b), is rapid thermally annealed (RTA) at 400°C for 2 min for better magnetic characteristics [110], which can then be used for following inductor fabrication. According to the previous investigations, the easy axis and hard axis of ferromagnetic nanorods/nanowires [111,112] would be along out-of-plane and in-plane directions, respectively, due to a large aspect ratio of rod/wire length to diameter. Figure 4.4 shows the superconducting quantum interference device (SQUID) measurements of Ni-P-AAO nanocomposite, which are applied with in-plane and out-of-plane magnetic fields, respectively. The relative permeability of the nanocomposite can be calculated from the slope of M–H curve as follows:

$$\mu_r = 1 + \frac{4\pi M}{H_0} \tag{4.12}$$

where H_0 and M are applied magnetic field and corresponding magnetization in Gaussian unit, respectively. The relative permeabilities of the composite at 10 Oe are 1.8 and 1.75 for the out-of-plane and in-plane applied fields, respectively. The measurement results also indicate that the Ni-P-AAO nanocomposite has little anisotropic behavior, which is very similar to the nanowire behavior [111]. In addition, from (4.10), the FMR frequency of ferromagnetic film is estimated about as high as 5.3 GHz due to large H_k, which is about 1700 Oe.

4.2.2 Inductor Fabrication

In this study, the spiral inductors of 3.5 and 4.5 turns, which are made of 5-µm-thick electroplated Cu and designed with 100 µm in inner diameter, 15 µm in line width, and 5 µm in line spacing, are utilized for characterizing the inductance enhancement using the Ni-P-AAO nanocomposite core. Figure 4.5 illustrates the process flow of the spiral inductor fabrication. It begins with 0.7-µm-thick thermal oxidization on a p-type (100) silicon substrate. Then, a 1-µm-thick Al film is deposited for AAO template fabrication, as shown in Figure 4.5(a). Then, the Ni-AAO nanocomposite film is fabricated using the aforementioned one-step anodic-oxidation method followed by electroless Ni plating, as shown in Figure 4.5(b) and (c), respectively. Same RTA process is performed at 400°C for 2 min for Ni crystallization. As Figure 4.5(d) shows, a layer of 0.2-µm-thick SiO_2 is then sputtered on the top of the composite film as an electrical insulation layer followed by Cr/Cu (300Å/900Å) adhesion/seed layer deposition for following Cu plating process for spiral inductor fabrication. The detail inductor fabrication can be referred to Chapter 2.4.2. Figure 4.6

shows as-fabricated 3.5-turn spiral inductors with magnetic Ni-P-AAO nanocomposite core underneath the inductor in a whole area and only placed in the central part of spiral inductor.

4.2.3 Measurement and Discussion

In the experiment, the two-port scattering parameters (*S*-parameters) of the inductors are measured up to 20 GHz with an on-wafer probe station using the high-frequency probes (Cascade Microtech, Inc., ACP-40-GSG-100 μm) and Agilent E8364B PNA network analyzer. The parasitic parallel capacitance between the contact pads of inductor is de-embedded using the measured result of designed dummy pattern [92]. The de-embedded *S*-parameters are then transformed into *Y*-parameter, and the equivalent series inductance (*L*) and quality factor (*Q*) of inductor are extracted from the *Y*-parameters based on the following equation [43,92], respectively:

$$L = \frac{\mathrm{Im}(1/Y_{11})}{2\pi f} \tag{4.13}$$

$$Q = \frac{\mathrm{Im}(1/Y_{11})}{\mathrm{Re}(1/Y_{11})} \tag{4.14}$$

where f is the signal frequency. The frequency-dependent inductance and *Q*-factor of the fabricated inductors are depicted in Figure 4.7. Figure 4.7 (a) and (b) shows that the spiral inductor of 3.5 turns with Ni-P-AAO nanocomposite magnetic core can have 3% larger inductance (3.58 nH at 3 GHz) than that of inductor without the core (3.47 nH at 3 GHz), and the enhancement trend has been kept up to 6.9 GHz. Meanwhile, the maximum *Q*-factor decreases from 15 to 14 at 1.1 GHz, which is about 6.7% reduction. Similar inductance enhancement and *Q* degradation also occur in the case of the spiral inductor of 4.5 turns. The spiral inductor of 4.5 turns with Ni-P-AAO nanocomposite magnetic core can have about 2.5% larger inductance (4.54 nH at 3 GHz) than that of inductor without the core (4.43 nH at 3 GHz) but the *Q* decreases from 12 to 11.6 at 1.1 GHz, which is also about 6.5% reduction.

For both cases of the spiral inductors with nanocomposite core in the center of 3.5 and 4.5 turns, no noticeable inductance enhancement of the inductor has been found in the high-frequency measurement. On the other hand, the measurement shows that the maximum *Q*-factors of the inductors decrease from 15 to 13.2 at 1.1 GHz, and 12 to 10.7 at 1.1 GHz, respectively. More than 12% *Q* reduction has been found in the inductors using the Ni-P-AAO nanocomposite core only placed inside the spiral inductor. The worse *Q* performance can be attributed to little inductance enhancement but the eddy current loss and magnetic loss still exist in the magnetic core. Therefore, the total *Q*-factor would decrease as expected once the inductance enhancement of the spiral inductor with Ni-P-AAO nanocomposite core in the center is minute.

Figure 4.8 shows the simulated magnitude distribution of magnetic field just underneath a spiral inductor with a 3 GHz electromagnetic wave signal input using Ansoft HFSS. The distribution indicates the magnitude of magnetic field in the central part of inductor is about one order smaller than that underneath the coil structure. Besides, in comparison with the total area of Ni-P-AAO nanocomposite core that fully covers the whole area of spiral inductor and provides only 3% inductance enhancement, the area of Ni-P-AAO nanocomposite only placed in the central region of the inductor is about one-tenth of the total area or even smaller. Therefore, it can be expected with minute inductance enhancement and worse *Q* performance when the Ni-P-AAO nanocomposite is only implemented in the central region of spiral inductor. Although there is only 3% inductance enhancement in the work, the magnetic properties can be further enhanced by improving the permeability of the composite material, such as increasing the porosity of AAO for more Ni incorporation in the composite, thermally annealing the electroless deposited Ni for the phosphorus content reduction [113], and using electroless CoP, CoNiP, or NiFe that has larger permeability instead of Ni [114] for nanocomposite synthesis, etc. Thus, relative process in regard to the synthesis of AAO with a conductive layer and the electrodeposition of NiFe into AAO template are developed as follow.

4.3 NiFe-AAO Nanocomposite

4.3.1 Synthesis and Characterization

In comparison with the previously developed electroless deposited Ni-P-AAO nanocomposite process, the synthesis of NiFe-AAO nanocomposite requires a seed layer, Ti, under AAO layer as a conducting layer for electroplating. Therefore, two additional steps, applied voltage adjustment while Al is anodized and reversed-biasing in KCl, are applied for thinning the alumina oxide barrier layer located at the bottom of AAO nanopores to ensure electroplating stability. The detail process steps are listed as follows.

The composite synthesis begins with a Ti (200 nm)/Al (1000 nm) layer deposition by e-gun evaporator on a 4” silicon substrate grown with a layer of 0.75 μm thermal oxide as an electrical isolation layer. The AAO template is then fabricated in a 0.3M oxalic acid ($H_2C_2O_4$) solution at 2°C with a bias of 40V applied on the substrate. The low temperature anodization process can reduce excessive current flow and heat evolution to make the AAO with the characteristics of small-pore films [115]. Once the film is anodized, the voltage is reduced from 40V to 15V and then kept for 15mins for thinning the alumina oxide barrier layer. The insulting barrier layer is then further thinned down to completely anodize Al film by applying a reversed-bias voltage (~-2V) to the substrate in a 0.5M saturated KCl for 10mins [115, 116]. Finally, the AAO temple is put in a 5% H_3PO_4 solution at 30°C for 25mins to form uniformly distributed nanopores which are 70 nm in diameter. At final, the as-fabricated AAO temple is electroplated in a Ni-sulfate-based NiFe bath to form a layer of NiFe-AAO nanocomposite which the inductor can then be fabricated on.

Figure 4.9 shows the top view and cross sectional view of as-deposited NiFe-AAO nanocomposite. NiFe nanorods are grown within the AAO matrix. Figure 4.10(a) shows hysteresis loop of the Ni-based-AAO nanocomposite film measured by SQUID. The relative permeability which can be calculated from the slope of *M-H* curve of the NiFe-AAO nanocomposite is about 20.3, 11-times larger than that of Ni-P-AAO nanocomposite. The energy dispersive spectrometer (EDS) spectrum, as shown in Figure 4.10(b), of NiFe-AAO nanocomposite verifies the composition NiFe.

4.3.2 Measurement and Discussion

Figure 4.11 shows extracted inductance and quality factor of as-fabricated inductors. The 3.5-turns inductor with a NiFe-AAO nanocomposite core averagely has 25% inductance enhancement up to 1GHz in comparison with that of the inductor without the core. Meanwhile, the maximum *Q*-factor decreases from 12.1 to 5.9, which is about 51% reduction. Similar inductance enhancement and *Q* degradation are also found in the case of the 4.5-turns inductor. Furthermore, the self-resonance frequency of inductors with the nanocomposite core has drastically decreased from about 14GHz to about 3GHz. In comparison with the previously developed Ni-P-AAO inductor which is about 6.5% *Q*-factor reduction and has almost no self-resonance frequency shift, the reduction of inductor performance using NiFe-AAO magnetic core could be attributed to the existence of a conductive 200nm Ti layer underneath the NiFe-AAO. From the point of view of self-resonance frequency, the continuous Ti layer obviously contributes extra parasitic capacitance to the inductor as a result of a lower frequency. Meanwhile, the shunt parasitic capacitance would also degrade the *Q* value of inductors. For a conventional on-chip spiral inductor, the *Q* can be depicted as the following equation [117]:

$$Q = \frac{\omega L_s}{R_s} \cdot \frac{R_p}{R_p + [(\omega L_s / R_s)^2 + 1] R_s} \cdot \left[1 - \frac{R_s^2 \left(C_s + C_p \right)}{L_s} - \omega^2 L_s \left(C_s + C_p \right) \right] \qquad (4.15)$$

where L_s, R_s, C_s, C_p, R_p, and ω are the inductance, series resistance, and series feed-forward capacitance of the inductor, parasitic shunt capacitance, resistance, and signal frequency, respectively. The last term of (4.15) is a self-resonance factor with the value less than 1. The existence of Ti seed layer would increase the parasitic shunt capacitance, C_p, so as to not only limit the usable bandwidth of inductor but also decrease the *Q* performance. In addition, another source of the *Q* degradation can be attributed to the induced eddy current loss within Ti layer and magnetic loss in NiFe.

In order to eliminate the effect of Ti layer, thermal annealing process at 450°C is utilized to form an amorphous TiO_x layer at the interface between Ti and the SiO_2[118]. Figure 4.12 shows the frequency dependence of the inductance and *Q*-factor of the fabricated inductors annealed for 60 and 120 mins, respectively. After the thermal anneal, the inductance of NiFe-AAO doesn't have a great difference. However, the self-resonance frequency has increased ~600MHz and 400MHz for the cases of the 4.5-turns and 3.5-turns inductors, respectively. On the other hand, the maximum *Q* values increase with the annealing time. For the case of a 4.5-turns inductor after with 120mins thermal anneal at 450°C, the maximum *Q* factor can be improved with a larger value than that of the inductor without the core. These results indicate that the presence of Ti layer indeed degrades the inductor performance and must be removed for practical use. Therefore, a series of micromachining process is designed and still under way to remove the Si substrate and Ti seed layer underneath NiFe-AAO layer for the reduction purpose of the eddy current loss and parasitic capacitance. After that, the high frequency magnetic property and loss mechanism including eddy current loss and hysteresis loss of NiFe-AAO can be well understood.

Although FMR effect can not be observed in the proposed NiFe-AAO inductor due to the low self-resonance frequency, the potential of inductance enhancement using the ferromagnetic-AAO nanocomposite material has been verified again in this study. The work further validates the conjecture with the performance improvement summarized in Table 4.1. Table 4.2 summarizes the comparison of this work with the prior arts. It indicates the NiFe-AAO nanocomposite core can provide an alternative cost-effective and practical solution for the performance enhancement of on-chip inductors in terms of CMOS foundry manufacturability.

4.4 Summary

The performance enhancement scheme of on-chip spiral inductor using ferromagnetic-AAO nanocomposite core is presented in this chapter. Two nanocomposite structures, Ni-P-AAO and NiFe-AAO, with different synthesis procedure have been successfully developed for inductance enhancement up to GHz region. By take advantage of high aspect ratio and isolated ferromagnetic nanorods structure, it can be expected that such a nanocomposite could has great potential for integrated inductor with high FMR frequency and low eddy current loss behavior. The high-frequency characteristics of on-chip spiral inductor with Ni-P-AAO nanocomposite core have been investigated. Incorporated with the nanocomposite core, the 3.5-and 4.5-turn inductors can have improved inductance up to 6.9 and 5.5 GHz, respectively. The insignificant inductance enhancement and Q degradation have been found in the inductors with the nanocomposite core, it could be further improved by incorporation of ferromagnetic metal with larger permeability. Thus, NiFe-AAO nanocomposite core has been synthesized and demonstrated its promise capability for inductance enhancement up to 1 GHz. Although the eddy current loss and the parasitic capacitance effect resulted by Ti seed layer cause the degradation of Q factor and limited usable bandwidth of the inductor, the drawbacks can be overcome by thermal annealing to form high resistive TiO_x. Based on the proposed CMOS-compatible fabrication scheme, it is believed that the ferromagnetic-AAO nanocomposite can have a great potential application for future RF SOP manufacture.

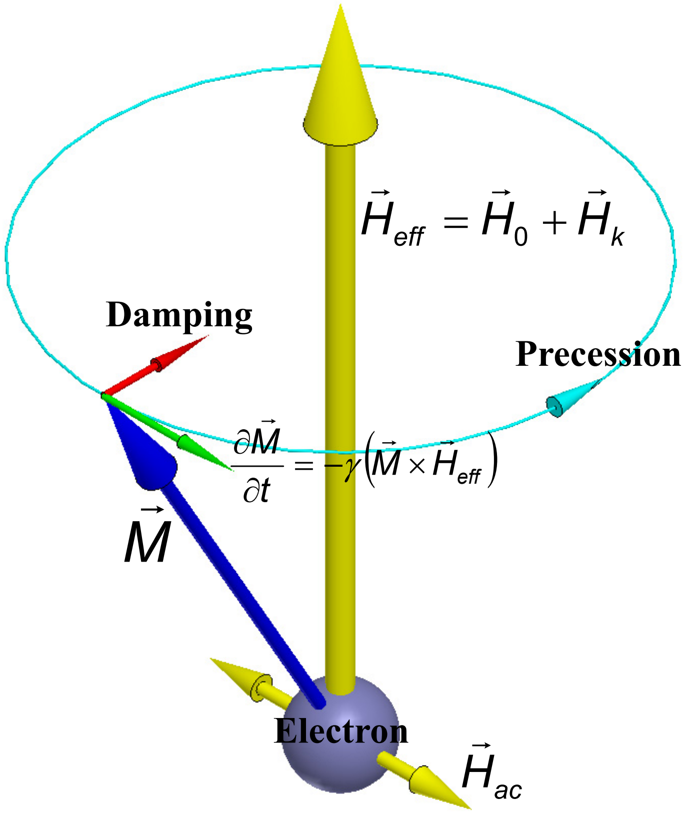


Figure 4.1 A schematic of dipole moment $\vec{M}$ precessing about a static magnetic field, H_{eff}. The alternating magnetic field, H_{ac}, is applied normal to the static field.

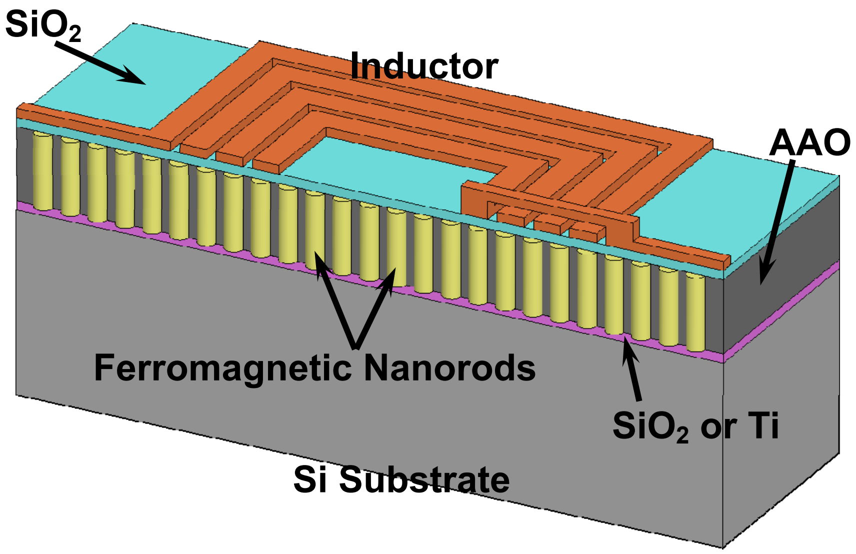
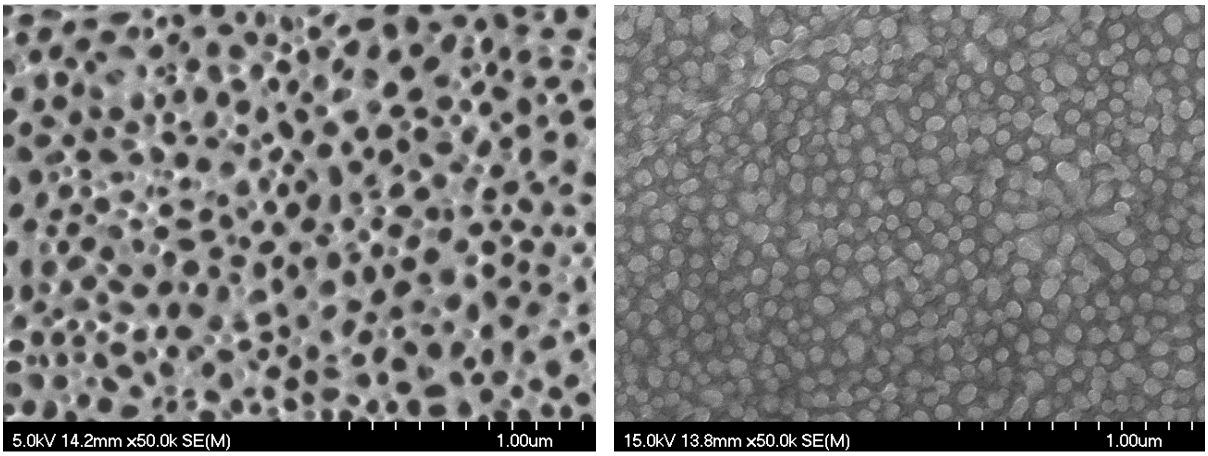
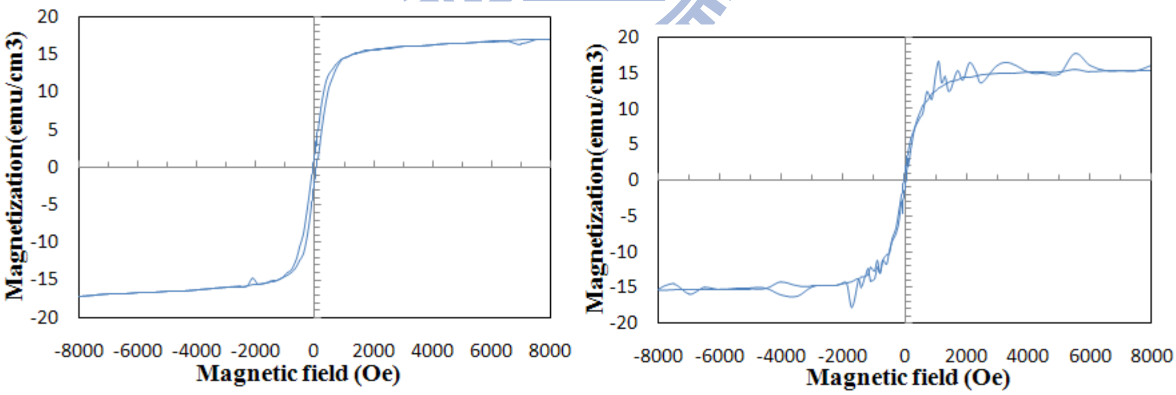


Figure 4.2 A schematic 3-D cross section view of the on-chip spiral inductor with Ferromagnetic-AAO nanocomposite core.



(a) **(b)**

Figure 4.3 SEM photographs of the top views of (a) AAO template and (b) Ni nanorods



(a) **(b)**

Figure 4.4 M-H loops of Ni-P-AAO nanocomposite with different forms of applied magnetic fields. (a) Out-of-plane. (b) In-plane.

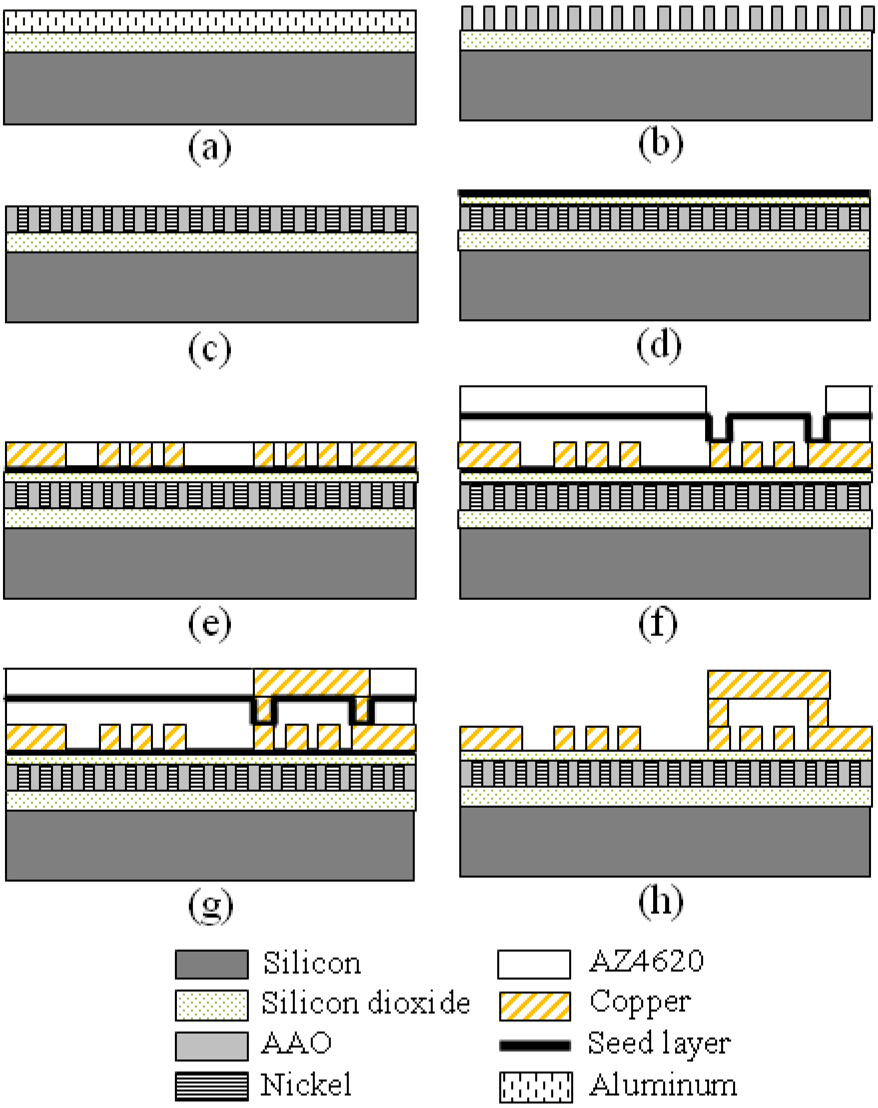
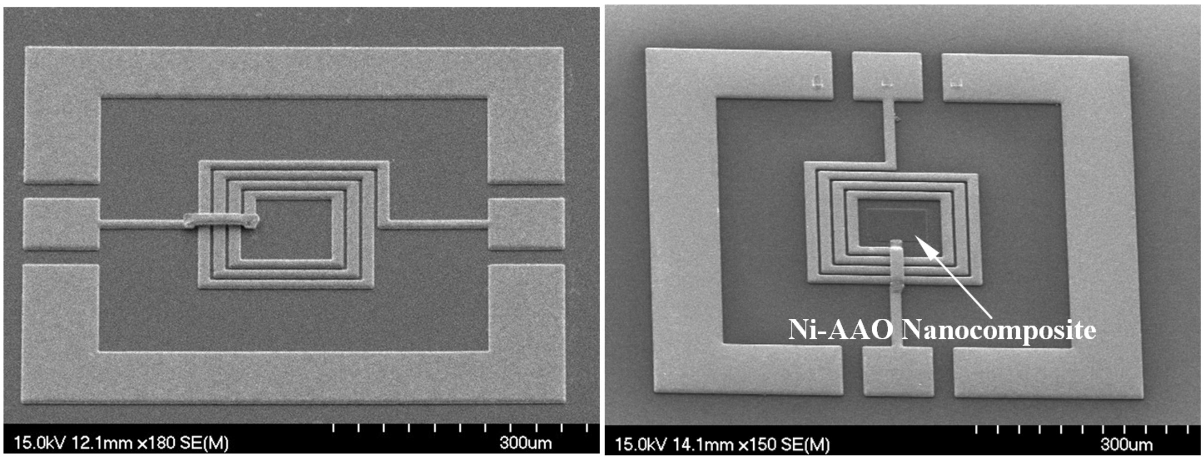
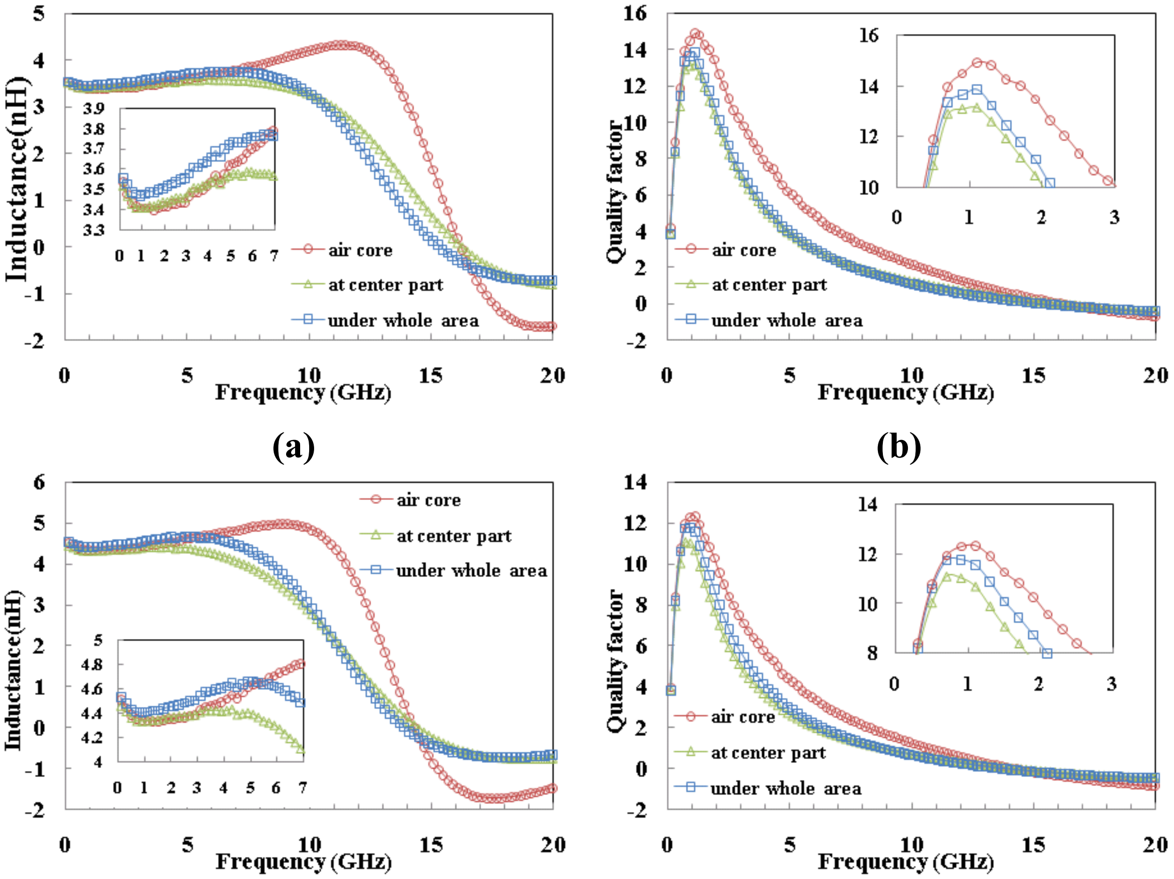


Figure 4.5 Fabrication process flow. (a) SiO_2 and Al layer deposition. (b) Al anodized as AAO template. (c) Electroless Ni plating. (d) SiO_2 and Cr/Cu seed/adhesion layer deposition. (e) First Cu plating for the coil part of the inductor. (f) Air bridge seed layer deposition and patterning. (g) Air bridge and via plating. (h) Seed layer and PR removal.



(a) (b)

Figure 4.6 SEM photographs of as-fabricated on-chip spiral inductors with the Ni-P-AAO nanocomposite (a) under whole area and (b) only in the central region.



(a) (b)

(c) (d)

Figure 4.7 Measured high-frequency characteristics of spiral inductors with Ni-P-AAO nanocomposite core. (a) Inductance and (b) *Q*-factor of spiral inductor with N=3.5, din =100 μm. (c) Inductance and (d) Q-factor of the spiral inductor with N=4.5, din =70 μm.

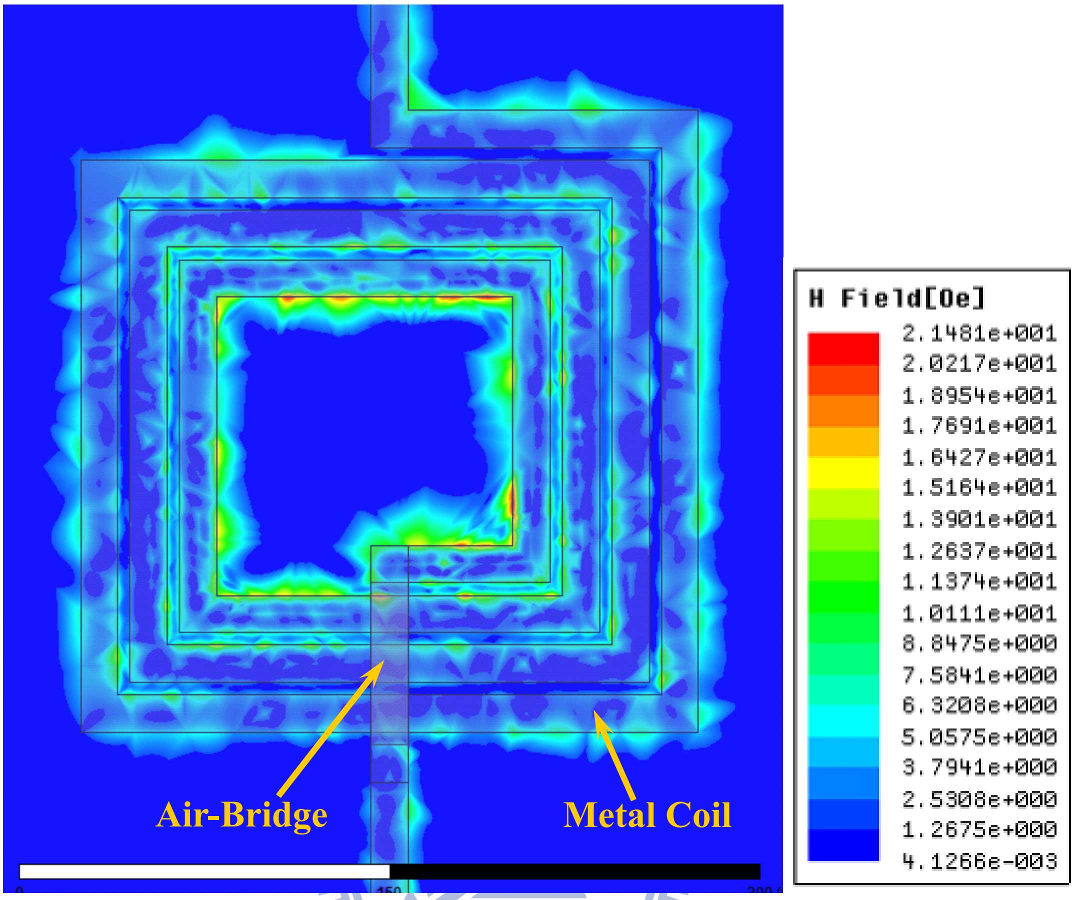


Figure 4.8 Simulated magnitude distribution of magnetic field of spiral inductor using Ansoft HFSS.

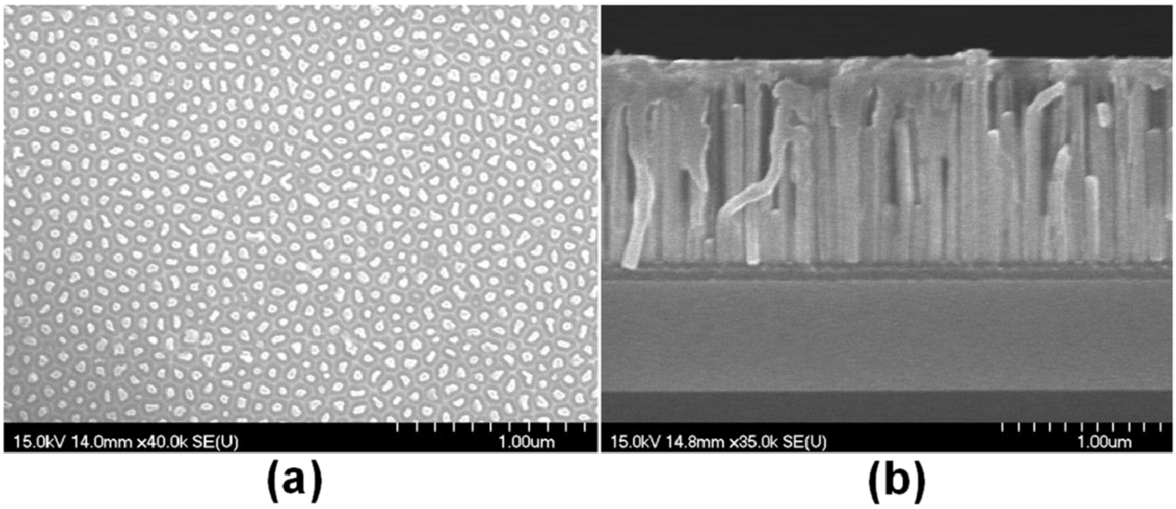
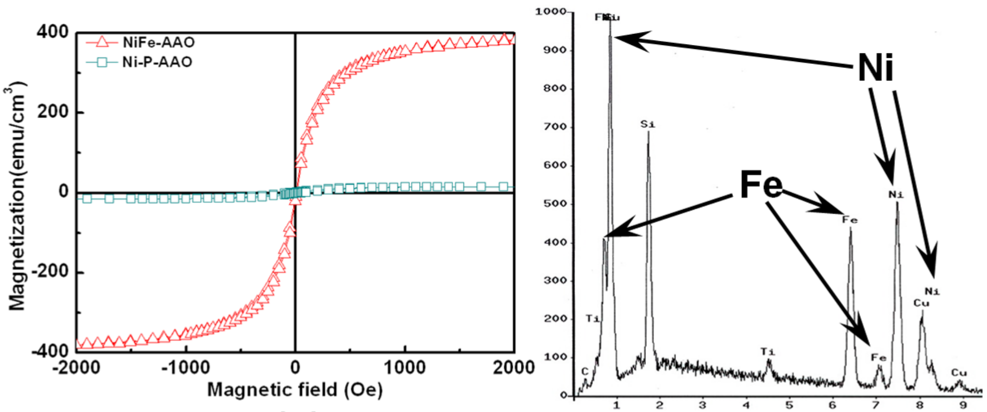
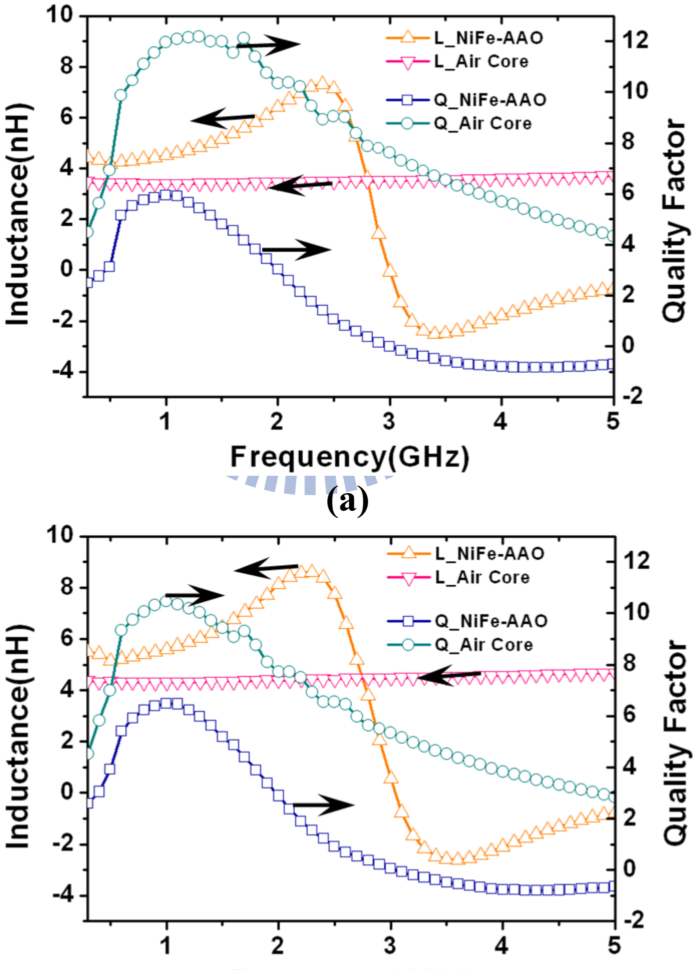


Figure 4.9 The (a) top view and (b) cross section view SEM micrographs of as-deposited NiFe-AAO magnetic nanocomposite.



(a) (b)

Figure 4.10 (a) The *M-H* loops of Ni-P-AAO and NiFe-AAO nanocomposite with applied out-of-plane magnetic field, and (b) the EDS analysis of NiFe-AAO nanocomposite.



(a)

(b)

Figure 4.11 The measured inductance and quality factor of rectangular spiral inductors which are designed with (a) n=3.5, din=100μm and (b) n=4.5, din=70μm, with and without NiFe magnetic nanocomposite core.

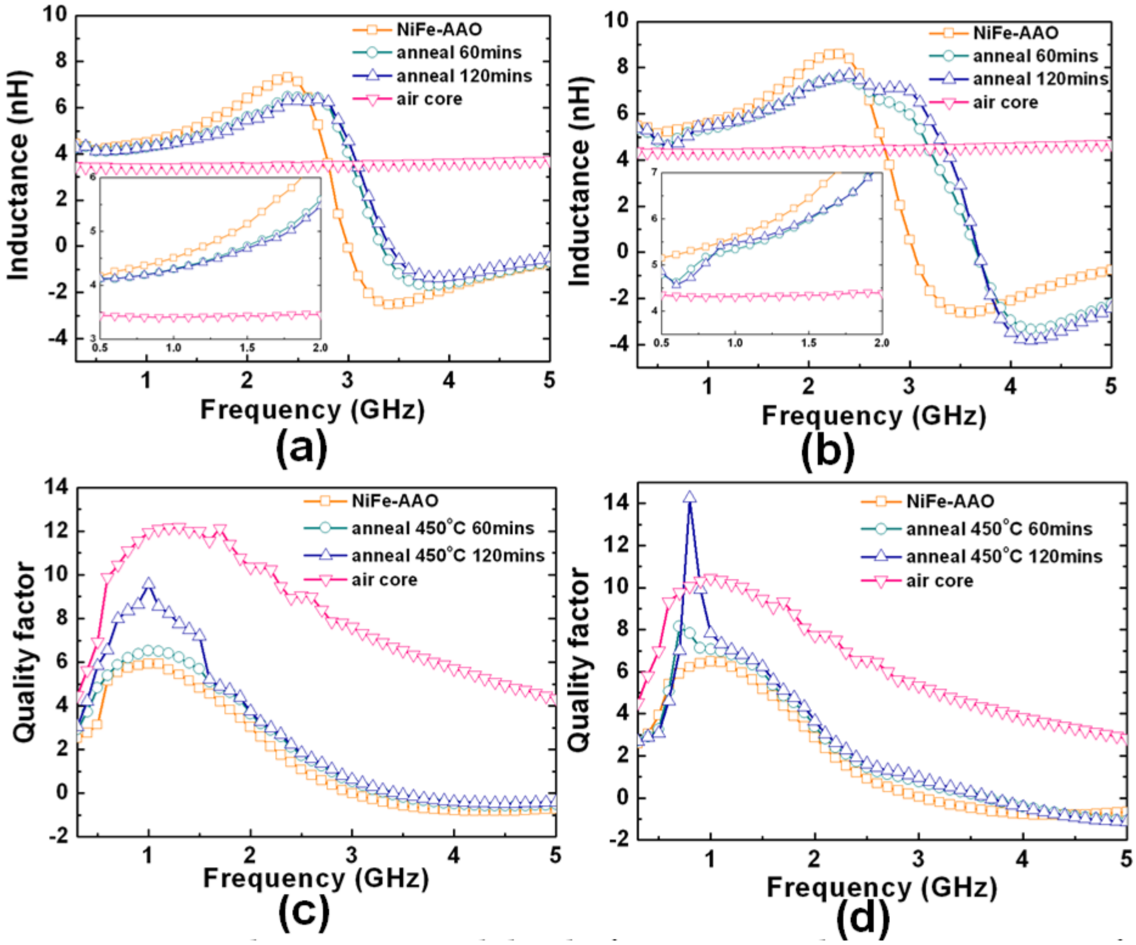


Figure 4.12 The measured high-frequency characteristics of NiFe-AAO spiral inductors after annealing at 450°C for 60mins and 120mins. The Inductance of inductor with (a) n=3.5 and (b) n=4.5, and the quality factor of inductor with (c) n=3.5 and (d) n=4.5.

Table 4.1 Comparisons of performance variation between developed Ni-Based-AAO nanocomposite inductors with relative to air-core inductor.

	Material	**Inductance enhancement**	**Quality factor reduction**	**μ**
Chapter 4.2	Ni-P	3%	6.7%	1.8
Chapter 4.3	NiFe	>25%	No degradation	20.3

Table 4.2 Comparisons between previously developed technologies [94-97] and this work.

	Ref. [94]	***Ref. [95]***	***Ref. [96]***	***Ref. [97]***	***This Work***
Magnetic Material	$Co_{85}Nb_{12}Zr_3$	$(Fe_{97.6}Hf_{2.6})_{90}N_{10}$	Fe_3O_4	IrMn/CoFe	NiFe-AAO
Deposition Method	RF Sputter Ion milling	RF Sputter	Gel-sol method	DC Sputter	Electroplating
Structure	Patterned sandwich magnetic film	Laminated film	Magnetite nanorod core	Mulitayers	Planar nanorod
Inductance Enhancement	8.3% @1GHz	33% @1.5GHz	3.5% @3GHz	30% @1.8GHz	Max. 32% @1GHz

Chapter 5 Conclusion and Future Research Direction

5.1 Conclusion

For the purpose to realize a high performance miniaturized RF SOP microsystem, several important heterogeneous integration technologies, including a bumpless interconnecting technology using Au-Au TC bonding, a low temperature SU-8 micromachining process for RF MEMS passives fabrication on flexible organic substrate, a flexible microsystem fabrication scheme using a metal sacrificial release process and low temperature Au-Au bonding, a SU-8 spiral ribbon cable for signal transmission between an biomedical MEMS device and the outer circuit system and a performance enhancement scheme for spiral inductors using ferromagnetic-AAO nanocomposite materials, are developed in this dissertation. Flip chip is the essential technology for assembling the advanced ICs on a SOP carrier to build a high density microelectronic system. When the signal frequency is larger than 20GHz or even higher, the parasitic effects resulted by inevitable structure discontinuity in the conventional flip chip joint is no longer neglectable, and then the time-consuming design for impedance matching is needed for a low loss interconnection. A bumpless interconnecting scheme using Au-Au TC bonding is proposed for providing a broadband low loss RF interconnection by replacing conventional solder ball to Au-Au bond with almost zero bump height. Relative fabrication process and metallization procedure are detailed in Chapter 2. Meanwhile, a UWB LNA with high Q MEMS inductors is demonstrated to show the great potential of proposed interconnecting technology. Furthermore, the proposed technology with arbitrary bonding pad shape and minute pad size can provide best design flexibility for RF SOP application.

One of the technical challenges to fabricate flexible microsystems is to keep whole process temperature below the T_g of organic substrate. Thus, SU-8-based low temperature fabrication processes are developed and presented for RF SOP application on flexible organic substrate. Firstly, by means of simple spin-coating process and low process temperature, the SU-8 micromachining process is demonstrated to fabricate RF MEMS passives on a flexible substrate. The clamped-clamped beam of RF serial MEMS switch is made by SU-8 instead of conventional SiO_2 or Si_3N_4 to avoid high temperature CVD process. Furthermore, a low temperature Au-Au TC bonding is achieved using a low cost surface cleaning procedure to clean the Au surface prior to the bonding step. Combining low temperature Au-Au bonding with a metal sacrificial release process, a wafer-level flexible microsystem fabrication scheme is presented for the batch manufacturing of flexible RF SOP products. It is believed that such a low temperature bonding scheme can not only assembly chips onto the flexible organic substrate but also enhance bonding reliability regard to lower thermal stress resulting from CTE mismatch within chips with different substrate material. Additionally, the proposed wafer-level fabrication scheme is also suitable for biomedical application. An SU-8/Cu flexible ribbon cable is designed and integrated with a Si probe for signal transmission to the instrument reader outside human body. The experimental results reveal that the spiral design of flexible cable and reliable electrical and mechanical interconnect make this technology possible to practical usage in surgery.

To reduce occupied area by numerous inductors in RF transceiver IC, the ferromagnetic integrated inductor has been researched for inductance enhancement in the past decade. In order to overcome the shortcoming of conventional thin film ferromagnetic materials, the ferromagnetic-AAO nanocomposites, including Ni-P-AAO and NiFe-AAO, are developed as core material for performance enhancement of spiral inductor. The composite materials exhibit the properties of high FMR frequency and low eddy current loss resulted by large shape anisotropy of high aspect ratio nanostructure and limiting the induction of eddy current within isolated nanorods, respectively. It can be expected that the size of inductor can be effectively shrunk via the incorporation of ferromagnetic-AAO material for higher *Q* performance of inductor due to less eddy current and resistive losses.

5.2 Future Research Direction

Recently, based on the proposed fabrication process for flexible electronics in Chapter 3, a MEMS power sensor tag for the electricity monitoring of two-wire household application is successfully developed. It needs further investigation to fabricate a complete wireless sensor tag including MEMS sensors, readout circuits, battery, RF front-end module and miniaturized antenna on a flexible substrate.

Ferromagnetic-AAO nanocomposite materials have been attracted lots of research attention as next generation metamaterial in microwave society in recent years because the RF responses of the material can be determined by its geometrical properties. Thus, a more complete study in terms of magnetic properties, high frequency performance and loss mechanism with relation to AAO structure such as pore diameter and interpore distance is required for the performance optimization of ferromagnetic-AAO nanocomposite inductor. It can be expected that ferromagnetic-AAO can utilize for performance enhancement of other RF passive devices such as circulators, isolators, and phase shifters in the further.

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Publication List

Journal papers:

1. (Full Paper) Tzu-Yuan Chao, Guang-Ren Shen, and Y. T. Cheng, "Comparative Study of Ni-P-Diamonds and Ni-P-CNTs Nanocomposite Films," *Journal of the Electrochemical Society*, vol. 153, pp. G98-G104, 2006.
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1. Tzu-Yuan Chao and Y. T. Cheng, “Synthesis and Characterization of Cu/$CoFe_2O_4$ Magnetic Nanocomposite for RFIC Application,” *in IEEE Int. Conf. on Nanotechnology*, pp. 810-813, 2006.
2. (1 point) Tzu-Yuan Chao and Y. T. Cheng, “Wafer-Level Chip Scale Flexible Wireless Microsystem Fabrication,” *in IEEE MEMS 2011 Conference*, pp. 344-347, 2011.
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Patents:

1. Tzu-Yuan Chao, Ming-Chieh Hsu, Yu-Ting Cheng, Chih Chen, and Chien-Min Liu, “An On-Chip Inductor Structure and Method for Manufacturing the same,” TW and US Patent under pending.
2. Tzu-Yuan Chao, Chia-Wei Liang, and Yu-Ting Cheng, “Flexible Micro-System and Fabrication Method Thereof,” TW, US, JP and KR Patent under pending.

著作總點數：8（依新法計點）