國立交通大學

電子工程學系 電子研究所

博 士 論 文

用於頻率合成器及無線通訊之金氧半積體電路技術

CMOS CIRCUIT TECHNIQUES FOR FREQUENCY SYNTHESIS AND WIRELESS COMMUNICATION

研 究 生：盧台祐 (Tai-You Lu)

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中華民國一〇〇年七月

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摘要

隨著通訊系統及互補式金氧半導體之快速發展，應用於當代無線通訊系統之收發器電路技巧仍然是被迫切需要。頻率合成技巧是一項在收發器裡面不可或缺的技術，主要是用來執行產生穩定且低雜訊之本地振盪信號(Local oscillator, LO)，或是用於直接調變(Direct modulation)傳送。這些頻率合成器必需要符合低成本、低功率及低電壓操作之單晶片設計，並且也要能滿足相位雜訊及切換速度之系統規格。於各式各樣的通訊系統中，頻率合成器將面對不同的挑戰需要去克服。一訊號源操作於 sub-THz(0.1-1 THz)頻率範圍被需要應用於感測、進階影像及生化偵測等應用。同時，射頻電路也被嘗試數位化並與基頻電路整合。對於生活的品質來說，一個低尺寸(form factor)及低功率之收發器則被需要用於生醫電子。

有鑒於此，本論文將開發金氧半電路技巧於頻率合成技術與無線通訊系統去克服將面臨的挑戰。發展數位輔助之射頻電路而應用於 sub-THz 影像系統與無線個人區域網路。除此之外，一高整合度之無線收發器也完成於無線身體區域網路而讓其應用能更普及。主要的研究主題有四項，其包括：(1)設計與分析一個數位控制且可切換模式之駐波振盪器，能產生基頻與三倍頻信號於 sub-THz 頻帶; (2)設計與分析具數位可重組傳輸線之寬調節範圍數位控制振盪器(Digitally controlled oscillator, DCO)於無線高畫質傳輸; (3)一具數位正交信號校正於突波衰減之快速跳頻多頻帶超寬頻正交多頻分工系統頻率

合成器; (4)一無參考信號源(reference-less)且具 1 Mbps QPSK 調變之單晶片無線接收器應用於無線身體感測網路。

本論文第二章首先探討各種頻率合成技術並探究其特點。直接、間接及數位頻率合成技巧將被介紹並總結其特點於此章節。

第三章，介紹電感電容共振腔式電壓控制振盪器(LC-tank voltage-controlled oscillator)之設計考量。接下來，提出一個 38/114 GHz 可切換模式且能同步鎖定之駐波振盪器(Standing wave oscillator, SWO)。三倍頻之輸出頻率可以被數位控制激發以操作於不同模式。實驗模型以低漏電 65 nm 互補式金氧半導體技術製造。結合同步鎖定技巧，於 38 GHz 偏移 1 MHz 頻率所量測之相位雜訊在鎖定前後分別為-102 dBc/Hz 與-120 dBc/Hz。在模式 1 操作於 38 GHz 及模式 3 操作於 114 GHz 下，所消耗之功率於 1.2 V 之偏壓下分別為 4 mA 及 20 mA，其晶片面積為 720×880 μm^2.

第四章，介紹電感電容共振腔式數位控制振盪器之設計考量。之後，設計完成一具 75 kHz 解析度之 10 GHz 電感電容共振腔式數位控制振盪器應用於全數位鎖相迴路。其更精細之頻率解析度可進一步藉由高速之合差調變器(ΔΣ modulator)達成。所量測於 1 MHz 偏移頻率之相位雜訊為-102 dBc/Hz，使用 90 nm 互補式金氧半導體技術製造其共消耗 3.9 mW 於 1 V 之偏壓下。除此之外，一使用線性可變電感之 40 GHz 且具 14%調節範圍之數位控制放大器應用於 60 GHz 超寬頻系統也被介紹於此。藉著所提出之技術，寬調節範圍及多頻帶操作可以被完成而不犧牲其振盪頻率。使用 90 nm 數位互補式金氧半導體技術，其能涵蓋 38.6 GHz 至 43.4 GHz 之操作頻率。自 43 GHz 所量測 10 MHz 偏移頻率之相位雜訊為-109 dBc/Hz，輸出功率為-11 dBm。此數位控制振盪器於 1.2 V 偏壓下共消耗 19 mW。晶片面積為 0.5 x 0.15 mm^2。

第五章提出一使用直接頻率合成技巧之 3 至 10 GHz、14 個頻帶且具突波(Spurs)縮減之頻率合成器應用於多頻帶超寬頻正交多頻分工系統。基於單一個鎖相迴路及兩級混頻之架構，其能降低諧波混合(Harmonic mixing)與頻率拉扯(Frequency pulling)之效應以抑制突波產生。同時，於鎖相迴路之迴授路徑上也只需要除二除頻器。因此更精準之正交次諧波項 (I/Q sub-harmonics) 能夠被單旁波帶混波器(Single sideband mixer, SSB mixer)利用以產生 14 個載波頻率。經實驗結果，於正交信號校正後，鏡像突波(Image spur)可以被改善 22dB 且抑制至-45 dBc 以下。使用 0.18 μm 互補式金氧半導體技術製造，此晶片於 1.8 V 電壓供應下共汲取 65 mA。晶片面積為 2.5 x 2.2 mm^2 且提供 14 個頻帶之正交相位輸出。

第六章描述一 2.4 GHz 無參考信號源之單晶片無線接收機具 1 Mbps 正交信號相位調變(QPSK modulation) ，使用 0.18 μm 互補式金氧半導體技術製造。此接收器直接由接收的射頻信號中，完成本地振盪載波之回復與資料解調變，而不需要振盪器形式之參考源及額外之類比至數位信號轉換器(Analog to digital converter, ADC)於基頻。其整合低雜訊放大器(Low noise amplifier, LNA)、混頻器、本地振盪載波回復迴路(LO recovery loop)、後級放大器(Post amplifier)及數位解調變器(Digital demodulator)於單一晶片，於 1.8 V 電壓供應下共消耗 20.4 mW。由回復之載波於 2.432 GHz 所量測到 1 MHz 偏移頻率之相位雜訊為-112 dBc/Hz。晶片面積為 1.75 x 1.55 mm^2。

第七章總結本論文之主要成果。對於未來之建議也於此章節闡述。

CMOS CIRCUIT TECHNIQUES FOR FREQUENCY SYNTHESIS AND WIRELESS COMMUNICATION

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Abstract

With the rapid development of communication system and CMOS technology, the circuit techniques of contemporary transceivers for wireless communication remain to be imperatively desired. The frequency synthesis technique is an essential technique in transceivers to perform a stable and high purity local oscillator (LO) generation, or direct modulation transmission. These synthesizers need to meet the stringent requirements of low cost, low power and low voltage monolithic implementation while also meeting the phase noise and switching transient specifications. For various communication systems, the frequency synthesizers have to face different challenges that need to be overcome. The signal source at sub-THz (0.1-1 THz) is required for sensing, advanced imaging or bio-agent chemical detection application. Also, the RF circuits are tried to be digitalized and to be integrated with baseband. For quality of life, a small form factor and low power transceiver is needed for healthy electronics.

This dissertation develops the CMOS circuit techniques for frequency synthesis and wireless communications to conquer the encountered challenges. The digital assisted RF techniques are developed for sub-THz imaging system and wireless personal area network. Besides, a highly integrated wireless transceiver for wireless body area network is achieved to promote pervasive adaptations. There are four major topics in this dissertation, including: (1) the design and analysis of a digitally controlled switched-mode standing wave oscillator

capable of generating fundamental and triple output frequency in the sub-THz range; (2) the design and analysis of wide tuning range digitally controlled oscillators with digitally reconfigurable transmission line for wireless high definition; (3) a fast hopping MB-OFDM UWB (multi-band orthogonal frequency division multiplexing) frequency synthesizer with digital I/Q calibration for spurs reduction; (4) a reference-less single chip wireless receiver for 1 Mbps QPSK demodulation applied in wireless body sensor network.

Chapter 2 reviews various types of frequency synthesis techniques and explores their characteristics. The direct, indirect and digital frequency synthesis are introduced and summarized in this chapter.

In chapter 3, the design considerations of a LC-type voltage controlled oscillator (VCO) are introduced. Furthermore, a 38/114 GHz switched-mode standing wave oscillator (SWO) capable of synchronous locking is presented. Triple output frequency can be excited by digital control of different mode operations. The experimental prototype was fabricated using a low leakage 65 nm CMOS technology. Incorporating a synchronous lock scheme, the measured phase noise from a 38 GHz carrier before and after the phase locked at 1 MHz offset are -102 dBc/Hz and -120 dBc/Hz, respectively. For the mode 1 operation at 38 GHz and mode 3 operation at 114 GHz, the experimental prototype consumes 4 mA and 20 mA , respectively, under a 1.2 V biasing voltage and with a chip size of 720×880 μm^2.

In chapter 4, the design considerations of a LC-type digitally controlled oscillator (DCO) are introduced. Afterwards, the LC-type DCO achieves a 75 KHz frequency resolution with 10 GHz operating frequency for an all digital PLL (ADPLL) is presented. The frequency resolution can be further enhanced by employing high speed dithering through a $\Delta\Sigma$ modulator. The measured phase noise is -102dBc/Hz at 1MHz offset, while consuming 3.9 mW from a 1V power supply using 90 nm CMOS technology. Additionally, a 40 GHz and 14% tuning range DCO using proposed linear variable inductor (VID) is introduced for 60 GHz UWB system. By employing the proposed frequency tuning scheme, wide-tuning range as well as multi-band operations are achieved without sacrificing its operating frequency. Fabricated in 90-nm digital CMOS process, the DCO is capable of covering frequency range from 37.6 to 43.4 GHz. The measured phase noise from a 43 GHz carrier is about -109 dBc/Hz at 10 MHz offset, and the output power is -11 dBm. The DCO core dissipates 19 mW from a 1.2-V supply. Chip size is 0.5 × 0.15 mm^2.

Chapter 5 demonstrates a 3-10 GHz, 14 bands CMOS frequency synthesizer with spurs reduction for MB-OFDM UWB system using direct frequency synthesis technique. Based on a single phase locked loop and two-stage frequency mixing architecture, it alleviates

harmonics mixing and frequency pulling to diminish spurs generation. Also, only divide-by-2 dividers are needed in the feedback path of the PLL. Thus more precise I/Q sub-harmonics can be derived for the SSB mixer in the 14 bands carrier generation. From experimental results, the image spurs are suppressed below -45 dBc and improved by more than 22 dB incorporating with I/Q calibration. Implemented in a 0.18 μm CMOS technology, this chip drains 65 mA from a single 1.8 V supply. The chip size is 2.5 by 2.2 mm^2 providing 14 bands I/Q phases.

Chapter 6 describes a 2.4 GHz reference-less single chip wireless receiver for 1Mbps QPSK demodulation using 0.18 μm CMOS technology. The receiver accomplishes LO carrier recovery and data demodulation directly from the RF received signal without a need of resonator-based reference source and extra baseband ADC. Integrating LNA, mixer, LO carrier recovery loop, post amplifier, and digital demodulator on a single chip, the total power consumption is 20.4mW from a 1.8 V power supply. The measured phase noise from a recovered carrier at 2.432 GHz is about -112 dBc/Hz at 1 MHz offset. The chip size is 1.75 x 1.55 mm^2.

Chapter 7 summarizes the main results of this dissertation. The recommendations for future works are also addressed.

To my dear parents 盧國禎，陳淑慧 and my family

To my advisor Prof. Wei-Zen Chen

To all my classmates and all my friends

Without all your supports, this dissertation could never be done

TAI-YOU LU

National Chiao-Tung University
2011, July

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Chapter 1

Introduction

In this chapter, the background and the organization of this dissertation are discussed. First, the background of frequency synthesis is introduced. Finally, the organization of this dissertation is well described.

1.1. Motivation

With the rapid development of communication system and CMOS technology, the circuit techniques of contemporary transceivers for wireless communication remain imperatively to be desired. Frequency synthesis is an essential technique in transceivers to perform a stable and high-purity local oscillator (LO) generation, or direct modulation transmission. These synthesizers need to meet the stringent requirements of low cost, low power and low voltage monolithic implementation while also meeting the phase noise and switching transient specifications. For varied communication systems, the frequency synthesizers have to face various challenges that need to be overcome.

In 2002, the Federal Communication Commission (FCC) regulations released the unlicensed spectrum from 3.1 to 10.6 GHz for ultra wideband (UWB) wireless communication. It opens an opportunity to develop a short range and high data rate communication for wireless personal area network (WPAN), or for wireless universal serial bus (USB). As proposed by MB-OFDM (multi-band orthogonal frequency division multiplexing) alliance, the spectrum for UWB communication system ranges is divided into 14 bands with each band of 528 MHz and categorized into 5 groups [1]. According to the recommendation, the frequency hopping time for band switching should be less than 9.5 ns. These challenges have drawn tremendous research efforts [2]-[18].

From the viewpoint of rapid evolution in CMOS technology, millimeter wave applications in sensing, advanced imaging, and bio-agent chemical detection become more feasible and have drawn tremendous research efforts in the past few years [55]-[64]. For pervasive adaptations, compact and cost-effective signal source is a key component to

materialize these systems. Hence, CMOS synthesizers in nano-meter technology have strong potential to be applied in the sub-Tera Hz frequency range (0.1-1 THz).

Not only the opportunity of sub-THz application but also a highly integrated system on chip (SOC) is benefited by the advanced CMOS technology. However, it is difficult to integrate CMOS circuits including radio frequency, analog baseband and digital baseband on a single chip to achieve a solution of high volume, high power efficiency and effective cost. Therefore, a new paradigm of digital RF processor (DRP) [40]-[50] is reported. To take more advantages of nanometer CMOS technology, the RF circuits including frequency synthesizers are tried to be digitalized and be integrated at baseband. Hence, the all-digital phase locked loops (ADPLL) for SOC are reported [40]-[47], while the interface between continuous behavior of oscillators and discrete domain of digital circuits is an important issue. To conquer this issue, a high resolution digitally controlled oscillator is an essential circuit block.

On the other hand, the wireless sensor network (WSN) and bio-inspired electronics, which attract more stress on small form factor and low power, are another significant research [90]-[100], in contrast to consumer electronics pursuing maximum data rate. For bio-inspired electronics, the human signals, such as electrocardiogram, body temperature and blood pressure are monitored by wireless sensor node attached to the human body. Then the signals are transmitted to the medical server through portable wireless receiver. For the sensor node integrated circuits (ICs) design, small form factor, low power, and system cost are of special interests to promote pervasive and ubiquitous adaptations. Consequently, the transceiver ICs have to face these challenges for healthy electronics.

To sum up, the transceiver ICs need to have various research efforts to be adopted in specific communication systems. The stringent frequency hopping time of 9.5 ns is required for MB-UWB OFDM system. A signal source at sub-THz frequency band is required for sensing, advanced imaging or bio-agent chemical detection application. The frequency synthesizer at radio frequency needs to be digitalized for highly integrated SOC solution. Also, a small form factor and low power transceiver IC must to achieved to promote pervasive adaptations for disposable and healthy electronics. To conquer these various issues, this dissertation develops the frequency synthesis techniques and circuit skills for different challenges in recent communication systems.

1.2. Organization

This dissertation is composed of seven chapters and the organization is as follows:

Chapter 2 reviews different types of frequency synthesis technique and explores the characteristics between them. The direct, indirect and digital frequency synthesis is introduced and summarized in this chapter.

In chapter 3, the design considerations of a LC-type voltage controlled oscillator (VCO) are introduced. Then a 8.4 GHz and a 2.4 GHz VCO are implemented with experimental results, respectively. They will be respectively employed in chapter 5 and chapter 6 for proposed frequency synthesis. Furthermore, a switched-mode standing wave oscillator capable of generating fundamental and triple output frequency in sub-THz frequency range (0.1-1 THz) is proposed with experimental results. It can be further employed by a frequency multiplier based PLL.

In chapter 4, the design considerations of a LC-type digitally controlled oscillator (DCO) are introduced. Afterwards, a high resolution LC-type DCO at 10 GHz is designed and measured for an all digital PLL (ADPLL). Finally, a wide tuning range DCO at 40 GHz using proposed linear variable inductor are described with measurement for 60 GHz UWB system.

Chapter 5 describes a 14 bands CMOS frequency synthesizer with spurs reduction for MB-OFDM UWB system using direct frequency synthesis technique. The spurs issues encountered in direct frequency synthesis are investigated and analyzed. To alleviate the spurious tones, I/Q calibration algorithm applied in carrier generation are described. Moreover, the detailed circuit blocks are presented and experimental results of the synthesizer are discussed.

Chapter 6 demonstrates a 2.4 GHz single chip wireless receiver incorporating with frequency synthesizer without a need of resonator-based reference source. The receiver accomplishes LO carrier recovery and data demodulation directly from the RF received signal without a need of resonator-based reference source and extra baseband ADC. The established behavior model is included to discuss stability and noise issues. Then the major building blocks are presented. Finally, the experimental results are shown and discussed.

Chapter 7 summarizes the main results of this dissertation. The recommendations for future works are also addressed.

Chapter 2

Frequency Synthesis

Frequency synthesis is an essential technique employed in RF systems to achieve local oscillator (LO) generation or direct modulation transmission. In this chapter, we review the different types of frequency synthesis technique and explore the tradeoffs between them. The techniques of fractional-N synthesis typically are extended from integer-N. Thus we focus on the review of integer-N frequency synthesis. For a frequency synthesizer, the output signal purity, frequency settling time, frequency resolution and power consumption are important indexes. In section 2.2 the associated frequency synthesis technique is summarized for comparison.

2.1. Introduction

To constitute a complete data link for wireless communication system, one indispensable building block is required by both receive and transmit path. That is the building block which generates a stable local oscillator (LO) signal: the frequency synthesizer. Wherever frequencies are translated, frequency synthesis is crucial to provide a high purity, stable and programmable local oscillator signal. Depend on the requirement of communication systems, the frequency synthesizer may need to be fast switching to perform the addressing sufficiently fast, or it needs to be high purity since low oscillator noise is vital for the quality and reliability of the information transfer.

The techniques of frequency synthesis typically can be mainly categorized into two types. One is the direct frequency synthesis shown in Fig. 2.1(a)(b), and another is the indirect frequency synthesis shown in Fig. 2.2. Generally, the differentiation between direct and indirect techniques is determined by whether the synthesized loop is open or closed. The direct synthesis (open loop synthesis) can further be sorted as digital direct synthesis (DDS) and analog direct synthesis. Fig. 2.1(b) shows the diagram of DDS. DDS is a technique using digital data processing blocks as a means to generate a frequency and phase tunable output signal referenced to a fixed-frequency precision clock source. The major building blocks include a memory and a digital to analog converter (DAC). Due to the limited speed of the memory and high resolution DAC, high frequency operation is not feasible.

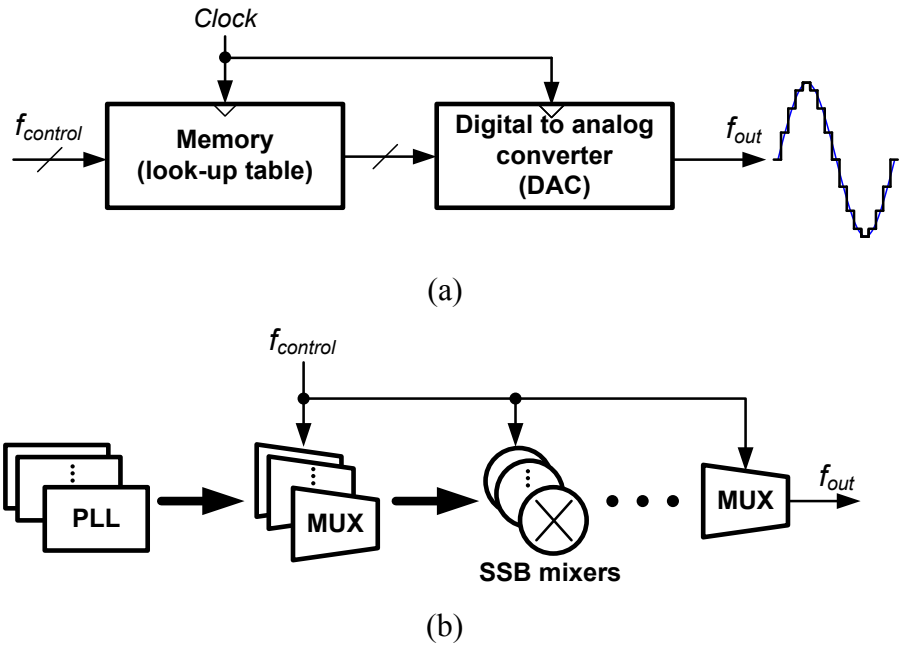


Fig. 2.1 The direct frequency synthesis of (a) direct digital synthesis and (b) direct analog synthesis

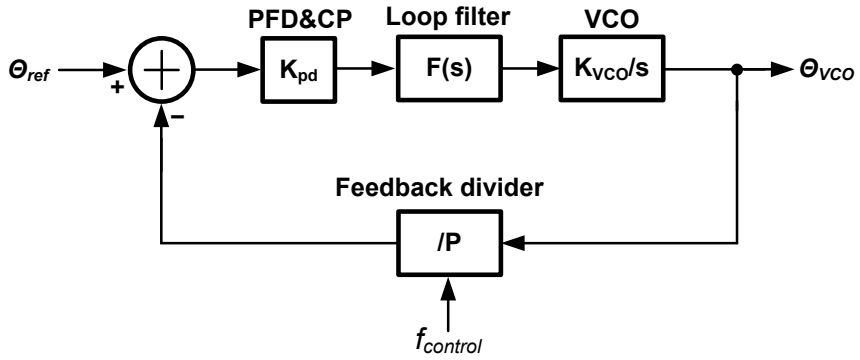
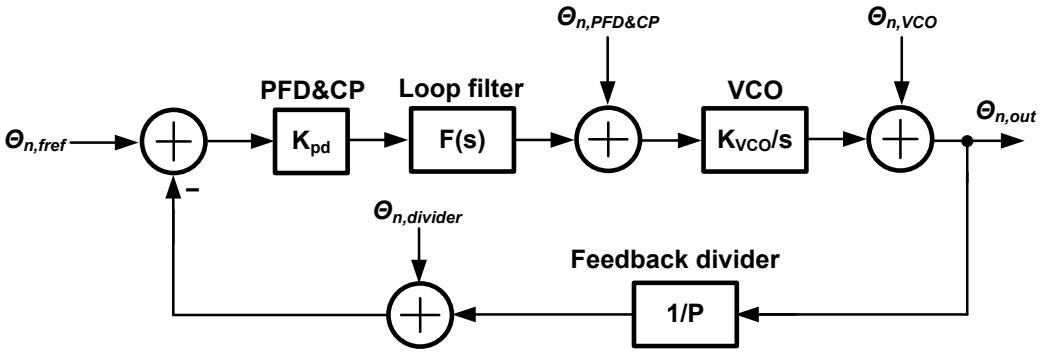
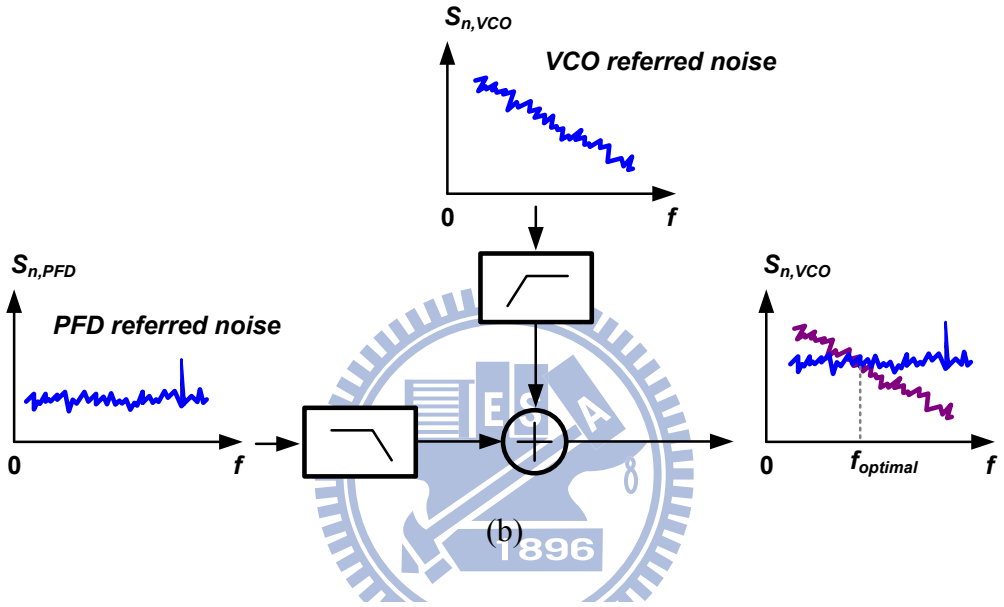


Fig. 2.2 The indirect frequency synthesis

On the other hand, the analog direct synthesizer synthesizes the wanted output frequency from PLLs by multiplying, mixing and dividing, as shown in Fig. 2.1(b). By repeatedly mixing and dividing, any frequency spacing is possible to achieve. Besides, based on the direct frequency mixing scheme, the frequency hopping time is mainly depend on the switching speed of multiplexers and single sideband (SSB) mixers. Hence it results in fast settling time of only several nano-seconds. Ideally, the output spectrum is as clean as the reference sources from PLLs. However, when implementing the direct synthesizer, cross coupling and harmonic mixing between stages is a problem for the spectral purity and the large number of components causes the synthesizer to be power hungry. Thus the frequency mixing scheme of direct synthesis has to consider these practical issues. An ultra wideband



(a)



(b)

Fig. 2.3 The noise model of (a) indirect digital synthesis and (b) its simplified model

(UWB) and fast settling frequency synthesizer utilizing open loop frequency synthesis will be demonstrated and analyzed in chapter 5.

The indirect frequency synthesizer generates its output by phase locking the divided output to a reference signal. Fig. 2.2 shows the block diagram of a closed loop frequency synthesis, where the gain of PFD and charge pump is K_{pd}, VCO gain is K_{VCO}, and the transfer function of loop filter is F(s). When a frequency hopping occurs, the loop need additional settling time to settle down since the loop configuration is readjusted by feedback divider. Generally, the settling time requires more than one hundred periods of reference cycle. It results in at least several micro seconds according to a typical reference frequency. The noise model of a PLL is shown in Fig. 2.3(a) and noise transfer function from each circuit blocks to output can be derived as

$$\frac{\theta_{n,out}}{\theta_{n,PFD-referred}} = P\frac{A(s)}{1+A(s)} = PG(s) \tag{2.1}$$

$$\frac{\theta_{n,out}}{\theta_{n,VCO-referred}} = \frac{1}{1+A(s)} = 1-G(s) \tag{2.2}$$

where

$$A(s) = 1/P \cdot K_{PD} \cdot K_{VCO} \cdot F(s)/s$$

The above can be observed that the noise come from reference signal, charge pump and feedback circuit contribute in band noise to output, while the VCO contributes out band noise. Fig. 2.3(b) shows the simplified noise model that the noise source is summarized as PFD referred noise (in band noise) and VCO referred noise (out band noise). It can be observed that in band noise is scaled by square of divide ratio and inverse of PFD gain. The optimal loop bandwidth is determined at the frequency that PFD referred noise meets the VCO referred noise. To suppress in band noise contributed from PFD and charge pump, a sub-sampling PLL were proposed [37]. This prior art improves the loop gain from charge pump to output, and mitigates the noise contributed from PFD and charge pump.

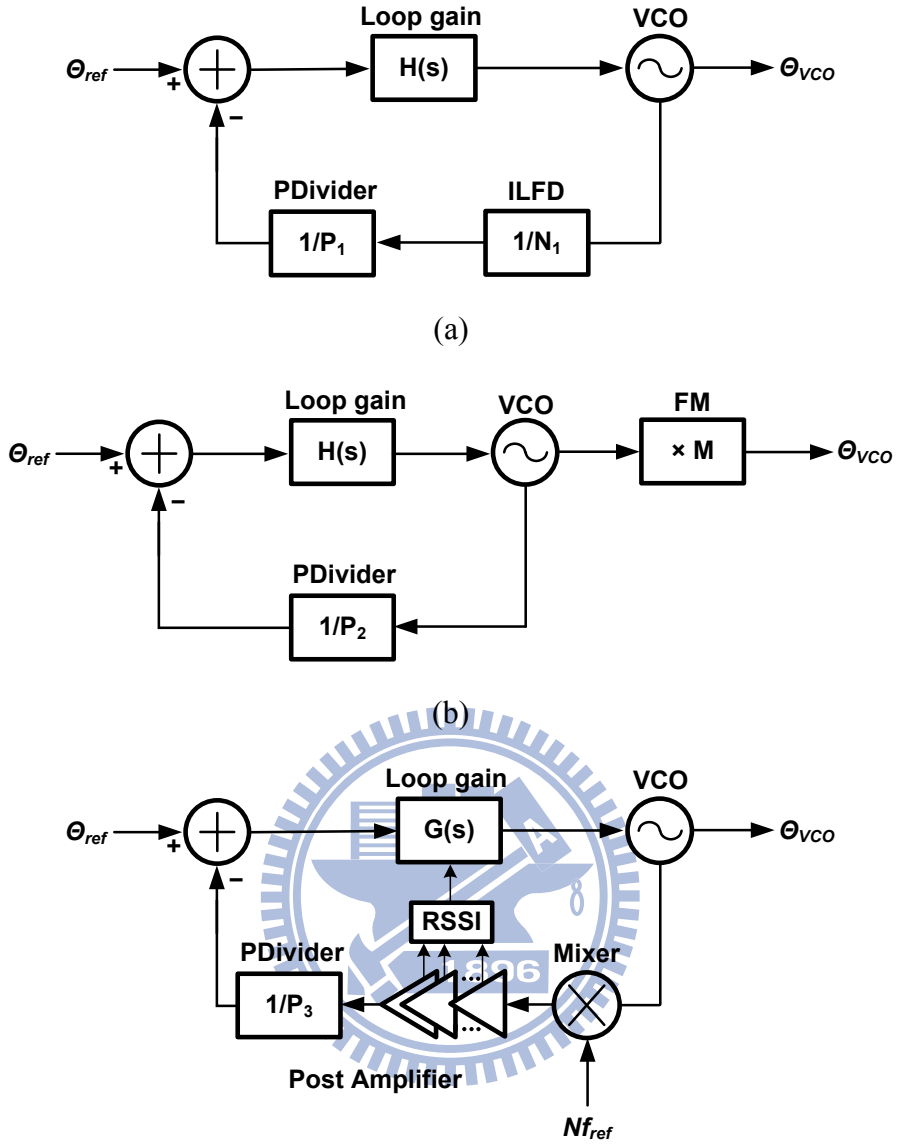


Fig. 2.4 The indirect frequency synthesis includes (a) ILFD-PLL (b) FM-PLL and (c) RX-PLL

For millimeter wave communication, a frequency synthesizer must generate high frequency LO for transceiver. However, the feedback frequency divider based on high speed D flip-flops is difficult to work at such high frequency. Therefore, some techniques for millimeter wave frequency synthesis were proposed [39], [55]-[59], [63]-[65]. Fig. 2.4 illustrates the indirect frequency synthesizers based on the techniques of injection locked frequency divider (ILFD), injection locked frequency multiplier (ILFM), multiphase edge combining, and the proposed receiver-based frequency synthesis.

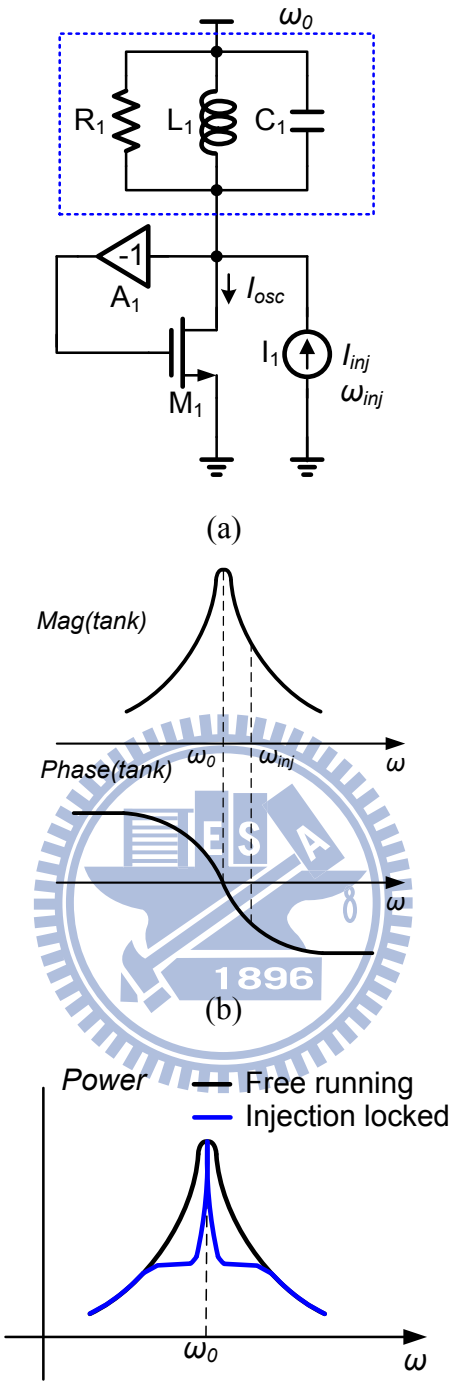


Fig. 2.5 (a) The conceptual ILFD circuit, (b) the diagram in frequency domain and (c) locked spectrum

Fig. 2.5(a) shows the conceptual ILFD circuit [38]. By injecting a proper signal I_{inj} with frequency ω_{inj} into a resonant tank with a quality factor Q and center frequency ω_0, the circuit indeed oscillates at ω_{inj} rather than at ω_0 and injection locking occurs, as shown in Fig. 2.5(b). The locking range of a injection locked phenomenon depend on the magnitude of injected signal I_{inj} and the quality factor of resonant tank Q and can be derived as [38]

$$\omega_L = \left|\omega_0 - \omega_{inj}\right| = \frac{\omega_0}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}} \tag{2.3}$$

where I_{osc} denotes the magnitude of original oscillation tank, and ω_L presents the locking range. For $I_{inj} << I_{osc}$, the above equation can be further approximated as

$$\omega_L \approx \frac{\omega_0}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \tag{2.4}$$

Obviously, the frequency locking range of a injection locked circuit is proportional to the magnitude of injected signal and inversely proportional to the quality factor of oscillation tank. From the viewpoint of time domain behavior, a free running oscillator could be phase synchronized by an injected signal when injection locked occurs. The phase noise within the frequency range of $\omega_0 \pm \omega_L$ can be corrected likes a spectrum of phase locked, as shown in Fig. 2.5(c).

The ILFM and multiphase edge combining techniques can be summarized as frequency multiplier-based PLLs (FM-PLL). It is composed of a synthesizer with low frequency output cascaded with a frequency multiplier to generate the desired output frequency [39], [56]. In this structure, the low frequency synthesizer is operated at the sub-harmonic of the desired frequency and the target frequency is generated by the frequency multiplier such as ILFM [39] or multiphase edge combiner [56]. In contrast to fundamental mode PLLs, it has the smaller divide ratio and lower power dissipation from prescaler. However, the design of a low power and high conversion efficiency frequency multiplier is a key point.

The operation principle of an ILFM circuit is similar to an ILFD circuit which is based on the mechanism of injection locking. The n^{th} harmonic term of the input signal is enhanced by the nonlinear input stage and then injects to a tank which resonates at n^{th} harmonic frequency, as shown in Fig. 2.6. Typically, the input stage is designed to have an optimal gain at the wanted harmonic term.

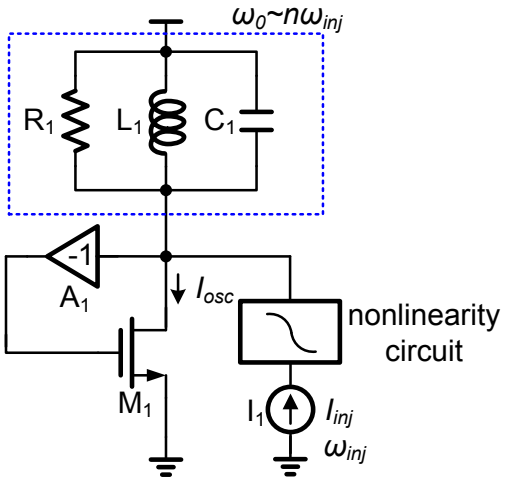


Fig. 2.6 The conceptual ILFM circuit

On the other hand, the multiphase edge combining technique employs linear superposition of multiple shifted phase (in $2\pi/n$ sequence, where n is an even integer) and rectified fundamental signals (at the angular frequency ω_0) to produce a superimposed output signal at the intended frequency of $n\omega_0$. The diagram is illustrated in Fig. 2.7 by taking n=4 for example. The conversion efficiency from fundamental to nth harmonic can be derived as [56]

$$\eta = \frac{2n}{(n-1)(n+1)}\pi \cdot A_I \tag{2.5}$$

where A_I is the rectification gain. As the operating frequency increases, matching, cross-coupling, and insertion loss of transmission lines between the oscillators and edge combiner become critical to the realization of a successful design. In addition, the edge combiner itself may become an obstacle to the achievement of the desired frequency range. These result in a low rectification gain (A_I) and then low conversion efficiency (η). From the perspective of power efficiency, an edge combiner seeks to eliminate lower order harmonics through vector cancellation. However, it turns out to consume a considerable amount of DC power wastefully since its output signal becomes quite small as the multiplication factor increases.

Furthermore, with the explosive growth of CMOS technology recently, the analog charge-pump based PLLs may encounter issues such as leakage from MOS capacitor, serious

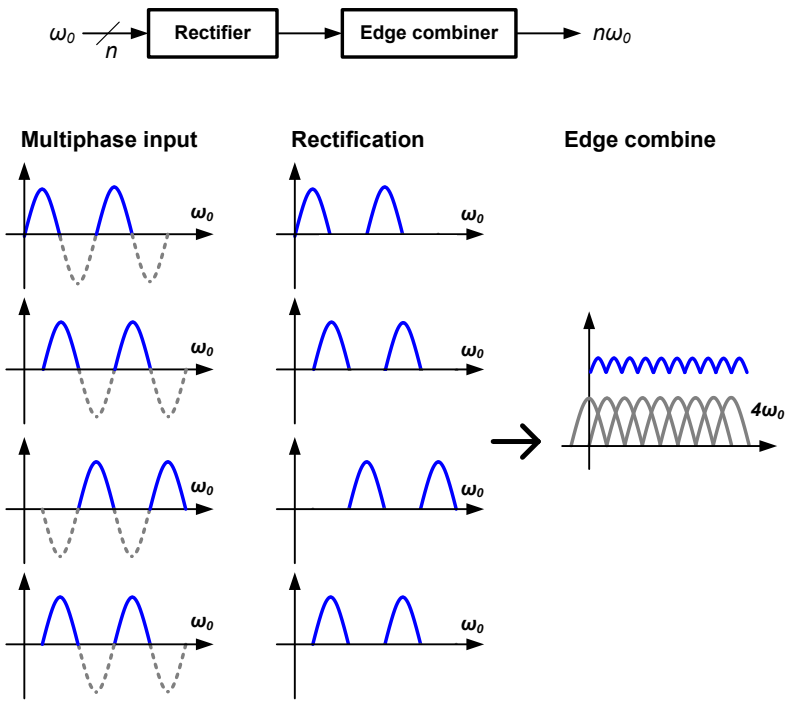


Fig. 2.7 The diagram of a frequency multiplier based on multiphase edge combining

current mismatch from charge pump circuits and limited voltage headroom under low power supply. These may lead to higher noise floor and spurious tone. Besides, the highly integrated level of an SOC allows more digital noise coupled to analog part. In other words, the analog circuit may not take too much advantage with the advance nano-meter technology. Consequently, the digital intensive approaches of PLLs have drawn tremendous research efforts recently [40]-[50]. The diagram of the all-digital PLL (ADPLL) is shown in Fig. 2.8. The ADPLL is mainly consisted of a digitally controlled oscillator, a time to digital domain interface and a digital loop filter. Although the ADPLL has advantages such as fast settling time, spurs free or direct modulation and so on [40]-[47], the resolution of the interface between continuous and discrete time domain is an issue and need extra efforts to overcome. In chapter 4, the proposed high resolution 10 GHz DCO and a wide tuning range 40 GHz DCO at is demonstrated respectively for 10 GHz ADPLL and 60 GHz UWB system.

To design a frequency synthesizer applying in THz image system, we propose a receiver-based PLL (RX-PLL) that employed a receiver-signal-strength-indicator (RSSI) to frequency tracking, as shown in Fig. 2.4(c). Because the VCO fundamental mode oscillates at THz such high frequency which almost closes to the maximum limitation in a CMOS technology, the output power is certainly small. Under this situation, the locking range of

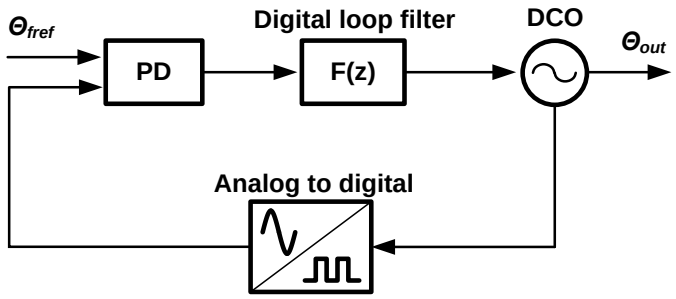


Fig. 2.8 The diagram of an ADPLL

feedback divider must be small. Besides, the issues of the center frequency mismatch between ILFD and VCO due to PVT variation still exists. In contrast to an ILFD-PLL, the RX-PLL utilizes a frequency down-converted mixer to let the THz frequency down to intermediate-frequency and can be amplified by the proceeded post amplifier. Due to the low IF architecture, the magnitude of image tone caused by double sideband mixer can be filtered out below the noise floor.

Excepted to the crystal-based PLLs, a proposed crystal-less frequency synthesizer and receiver [99] will be introduced in chapter 6. Based on the concept of wireless remote frequency synchronization to the transmitter side, it eliminates extra reference generator at the receiver side, and also facilitates wireless clock distribution. Since the LO carrier at the receiver side is tracking the frequency at the transmitter side directly during data receiving, the issue of carrier frequency offset between the transmitter and receiver in conventional wireless transceivers is eliminated. Meanwhile, it accomplishes data demodulation along with carrier and timing recovery without resort to an extra base-band ADC.

2.2. Summary

This chapter introduces the synthesis techniques of direct frequency synthesis, indirect frequency synthesis, and proposed crystal-less frequency synthesis. The indirect frequency synthesis is based on the PLLs including ILFD-PLL, FM-PLL and RX-PLL. A frequency synthesizer has some important characteristics such as frequency locking range, frequency resolution, settling time, signal purity and power consumption. Table 2.1 summarizes the comparison of the indirect frequency synthesis techniques. Assume the following parameters are the same among them:

Reference frequency f_{ref}, target frequency f_{out}, loop bandwidth of the PLL, frequency tuning

Table 2.1 Comparison of indirect frequency synthesis techniques

Reference	ILFD-PLL	FM-PLL		RX-PLL
		ILFM	Multiphase edge combining	
Frequency locking range	narrow	narrow	wide	wide
$\mathbf{f_{out}/f_{ref}}$	P_1N_1	P_2M	P_2M	P_3+N
Frequency resolution (normalized to f_{ref})	1	M	M	1
Settling time	normal	normal	normal	fast
Output power	large	small	small	large
PFD referred noise to output (Normalized to ILFD-PLL)	1	1	1	1
Power Consumption	small	small	large	large

percentage of the VCO, power dissipation and noise of the circuit block are all the same

Based on the assumption, the PLLs employ ILFD and ILFM have narrow frequency range limited by the nature of injection locking, while it generally consume less power than other techniques due to its high Q. At the point of frequency resolution, the FM-PLLs have worse resolution caused by the frequency multiplier. Also, the output power in FM-PLLs is smaller than the fundamental mode PLLs. Generally, the RX-PLL has wide locking range and faster settling time due to its inherent post amplifier can be employed to frequency tracking. The RX-PLL may intuitively be observed that it has larger in band noise than the other types due to it cascades two PLLs. However, the second PLL of the RX-PLL has larger loop gain from charge pump to output and the total PFD referred noise contributed to output can be derived as

$$f_{n,out,RX-PLL} = \left(N + P_3\right) f_{n,PFD} \tag{2.6}$$

Based on the assumption of same fout/fref, the RX-PLL has equal in band noise contributed from PFD referred noise of both two PLLs.

In addition to indirect synthesis, the direct synthesis techniques can achieve ultra wide frequency locking range in contrast to indirect synthesis which is limited by VCO. Besides,

the frequency settling time is faster than indirect synthesis than about 1000 times at the expenses of the circuit complexity and power consumption. These issues will be discussed in chapter 5. Moreover, a crystal-less frequency synthesizer and receiver [99] will be introduced in chapter 6.

Chapter 3

LC-Type Voltage Controlled Oscillator

This chapter introduces the design of LC-type oscillators for wireless communications. As discussed in chapter 1, the VCO plays an important role in a frequency synthesizer. For high frequency circuit designs, LC-type oscillators can achieve higher speed than ring-type oscillators, and have relatively good phase noise and ease of implementation. This chapter is focused on the design of LC-type oscillators and organized as follows. In section 3.2, the noise analysis in cross-coupled LC oscillators will be introduced [51]-[52]. By this noise analysis, the circuit technique for low noise design is presented [53]. Also, a performance comparison between only N-MOS (or P-MOS) and complementary is reported [54]. Two complementary VCO respectively operates at 8.4 GHz and 2.4 GHz both in 180 nm CMOS technology is implemented for an ultra wideband and fast settling frequency synthesizer in chapter 5, and for a crystal-less frequency synthesizer and receiver in chapter 6. In contrast to LC-type oscillators, a 38/114 GHz switched-mode standing wave oscillator (SWO) capable of synchronous locking [64] is presented in section 3.3 which can be utilized in a FMPLL. This section proposes a switched-mode standing wave oscillator capable of generating fundamental and triple output frequency in the sub-THz range by nature. Different excitation modes are enabled by digital control without resort to other high speed circuits or edge combiner. Additionally, incorporating mode enabling and sub-harmonic injection locking, the proposed SWO can be synchronized to an external reference to further improve phase noise performance. The close-in phase noise is improved by about 18 dB with the proposed scheme when the SWO is with synchronous lock. The experimental prototype was fabricated using a low leakage 65 nm 1P9M triple-well CMOS technology.

3.1. Introduction

$$\frac{Out(s)}{In(s)} = \frac{H(s)}{1-H(s)\beta(s)} \qquad \begin{matrix} \angle H(s)\beta(s) = 0 \\ |H(s)\beta(s)| \geq 1 \end{matrix}$$

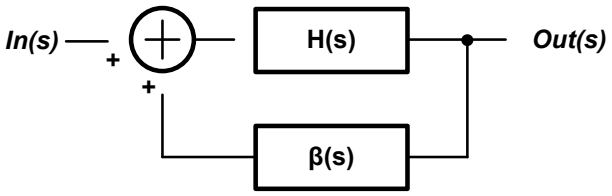


Fig. 3.1 The diagram of feedback oscillatory system

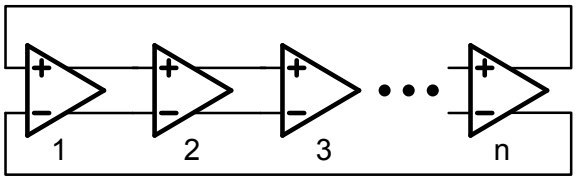


Fig. 3.2 The diagram of a ring-type oscillator

Oscillators are extensively used in frequency synthesis and clock generation. The design of oscillators on monolithic implementation can be categorized as ring-type and LC-type. Generally, ring-type oscillators consist of a number of gain stages in a loop. On the other hand, LC-type oscillators typically are also treated as a number of gain stages in a loop but with inductors in each gain stage. To sustain oscillation, the phase shift of a loop must be a positive feedback (or 360^{o}), and the frequency that a positive feedback loop occurs determines the oscillation frequency. Besides, the other requirement is that the loop gain at the oscillation frequency must be larger than unity. Fig. 3.1 shows the diagram of feedback oscillatory system, and these two conditions are called “Barkhausen criteria”. The ring-type oscillators shown in Fig. 3.2 have output frequency as

$$f_{osc} = \frac{1}{2n \cdot T_d} \tag{3.1}$$

where n and T_d is the number and the delay time of each gain stage. Frequency tuning is achieved by varying the delay time which is dominated by the time of charge and discharge to output capacitor of each gain stage. The resulting tuning range is large. However, the circuit complexity limits the speed of ring oscillators. Also, the lack of noise filtering (as in LC-tank oscillators) and the transistors in the gain stages cause the intrinsically high phase noise. On the other hand, the oscillation frequency of a LC-type oscillator is determined by

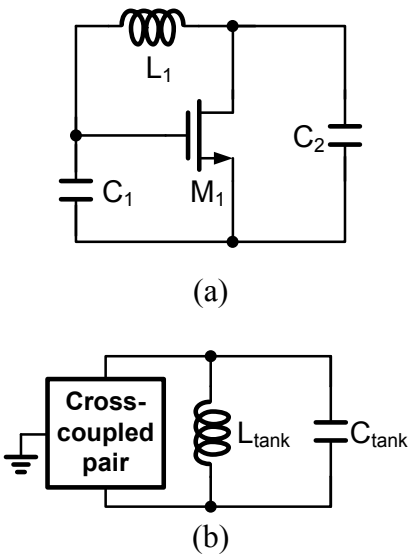


Fig. 3.3 (a) A Colpitts oscillator and (b) A cross-coupled oscillator with differential output

the resonance of an inductor and capacitor, as

$$f_{osc} = \frac{1}{\sqrt{L_{tank} C_{tank}}} \tag{3.2}$$

where L_{tank} and C_{tank} presents the inductor and capacitor values, respectively. Due to the phase shift by inductors, a LC-type oscillator can satisfy the Barkhausen criteria with minimum gain stage. As shown in Fig. 3.3, a Colpitts oscillator demonstrates a topology of one stage and single-ended output, and a cross-coupled oscillator is a two stage and differential output topology which is commonly used in wireless communication. Due to its simple architecture and a band pass filter of LC-tank, LC oscillators perform relatively good phase noise and high resonant frequency. For wireless communications, the oscillators in a PLL operates at the highest frequency and usually determines the out band noise of the frequency synthesizer. For wireless communication, the out band noise picks up the interferers from adjacent channel and then degrades SNR of a receiver. Thus, this chapter focuses on the design of the LC-type oscillators. The considerations will be introduced in next section. In section 3.3, a switched-mode standing wave oscillator (SWO) capable of synchronous locking [64] which can be employed by a FMPLL is demonstrated.

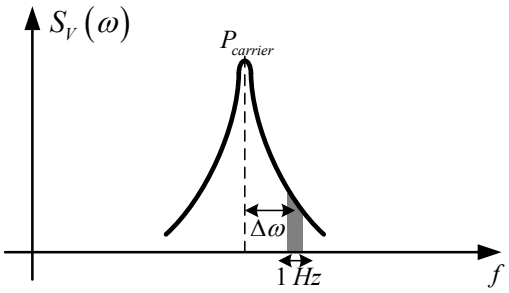


Fig. 3.4 The phase noise of an oscillator

3.2. Design Consideration

An oscillator generates a periodic output. The circuit must entail a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal. According to Barkhausen's criteria, a positive feedback loop and that the loop gain larger than unity are both vital requirements for oscillation. When design an oscillator for a wireless communication system, there are some important specifications need to take into considerations.

Phase noise: It is a parameter for signal purity in the frequency domain viewpoint. An oscillator's instabilities are usually characterized in terms of the single sideband noise spectral density shown in Fig. 3.4. It defines that the units of decibels below the carrier per Hertz (dBc/Hz) as

$$L\{\Delta\omega\} = 10\log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega,\ 1\ Hz)}{P_{carrier}}\right] \tag{3.3}$$

where $P_{sideband}(\omega_0+\Delta\omega,\ 1\ Hz)$ denotes the single sideband power at a frequency offset $\Delta\omega$ from the carrier in a measurement bandwidth 1 Hz, and $P_{carrier}$ is the total power at carrier frequency ω_0. In the time domain viewpoint, the uncertainty of the transition spacing is known as timing jitter. The clock jitter often dominates the maximum speed of digital circuits and high speed SERDES. A relation between phase noise and cycle to cycle jitter can be derived from the integral of phase noise profile [51]

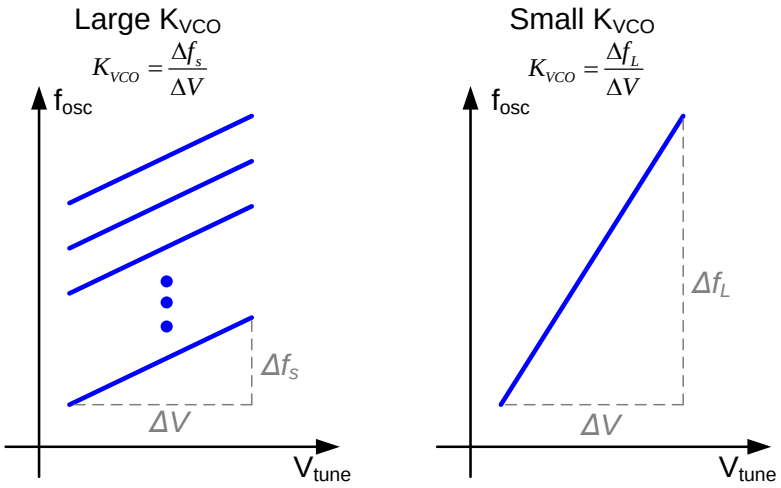


Fig. 3.5 Frequency tuning curve with multiband and single band

$$J_{UI} = \frac{\sqrt{2\int_{f1}^{f2} L\{f\}\,df}}{2\pi} \tag{3.4}$$

Frequency tuning range: The frequency tuning range of an oscillator dominates the output frequency of a frequency synthesizer, and it must cover the entire frequency band for a communication system. The frequency tuning range usually designs larger than specification to cope with variation of process, voltage and temperature.

VCO gain: For a given noise amplitude on the control line of a voltage-controlled oscillator, the noise in the output frequency is proportional to VCO gain (K_{VCO}). Hence, to minimize the effect of noise on the control line, K_{VCO} must be minimized. There has a constraint in direct conflict with the required tuning range. The multiband operation can be adopted to lower the sensitivity of the noise, as illustrated in Fig. 3.5.

Output power: Typically, the output of an oscillator drives next stages of frequency dividers and mixers. Thus large amplitude swing at output is desirable to drive next stages. Besides, it has less sensitivity to noise when output power is large. The amplitude trades with power dissipation, supply voltage and even the tuning range.

Generally, a LC-type VCO has better phase noise and higher operating frequency than a ring-type VCO due to its higher quality factor. The equivalent circuit of a LC oscillator is

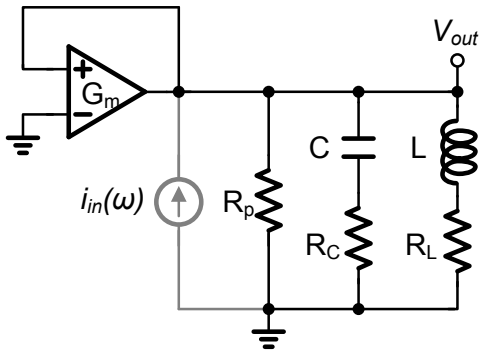


Fig. 3.6 Equivalent circuit for the LC oscillators

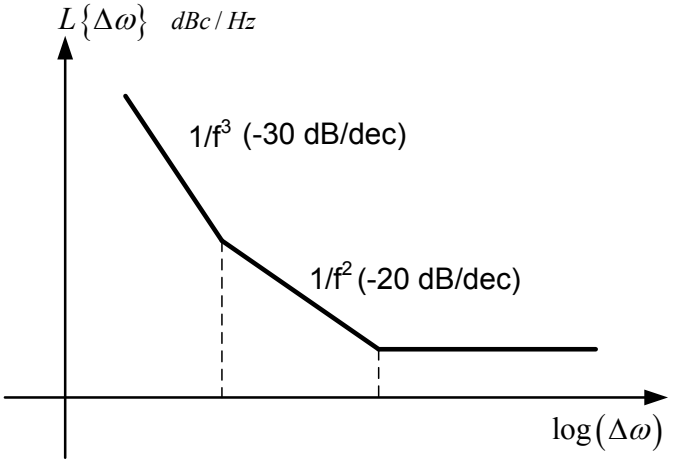


Fig. 3.7 A typical phase noise plot for a free running oscillator

shown in Fig. 3.6, which is composed of a RLC tank with loss and a positive feedback loop. To maintain oscillation, the loop gain must be larger than 1. The phase noise performance as well as start-up condition is both relative to effective series resistance in Fig. 3.6, which can be derived as [51]

$$R_{eff} = R_L + R_C + \frac{1}{R_p\left(\omega_{osc}C\right)^2} \tag{3.5}$$

The above reveals that the more electric power stores in capacitor of tank, the more quality factor can be obtain. Also, effective series resistance can be reduced more to obtain better phase noise performance. A typical phase noise plot for a free running oscillator is illustrated in Fig. 3.7. The second order transfer function of LC-tank converts a flicker and thermal noise of circuits φ into $1/f^3$ and $1/f^2$ region, respectively. A flat region occurs at the frequency far away from center frequency of LC-tank. To capture how the noise sources

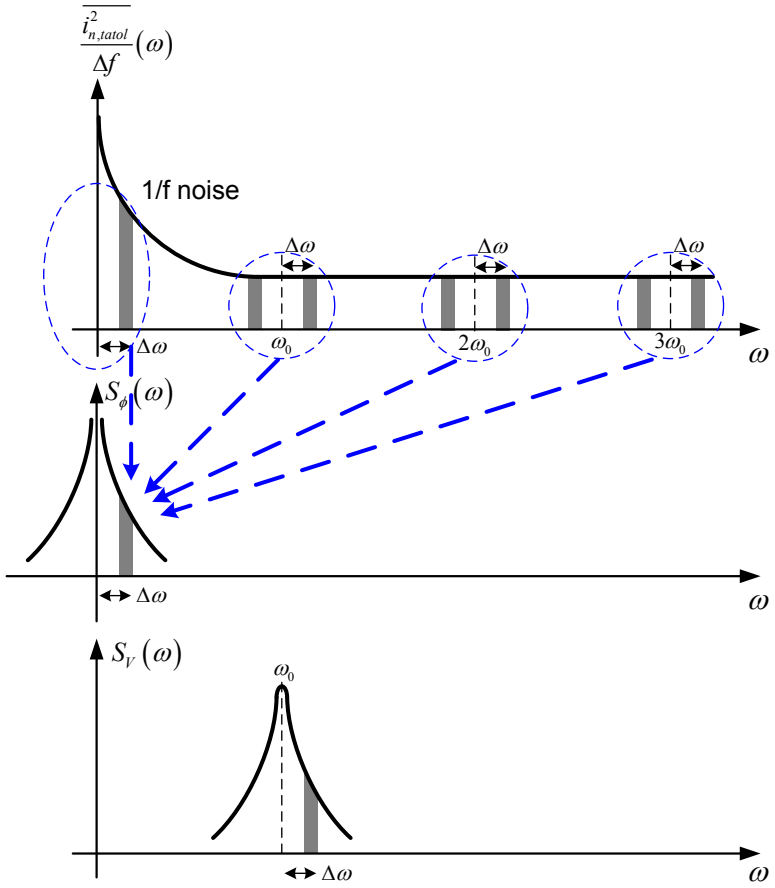


Fig. 3.8 Conversion of noise to phase instabilities and phase noise sideband

contaminate resonant tank, Fig 3.8 illustrates a diagram in spectrum. Fig 3.8 shows that noise components located near integer multiple of resonant frequency are integrated to form the low frequency sidebands for $S_\varphi(\omega)$. These sidebands in turn become close in phase noise as $S_V(\omega)$ through phase modulation. The close-in ($1/f^3$ region) phase noise is mainly caused by the flicker noise of tail current through the mechanism of up-converted single balance mixer performed by cross-coupled pair [53], or a time-variant phase noise model with impulse sensitivity function [51]. Then the $1/f^3$ noise due to tail current will be further filter out by LC-tank band pass filter, which is depend on its quality factor. On the other hand, the noise in $1/f^2$ region is deteriorated by cross-coupled pair and effective series resistance of tank. The [51] derived phase noise in $1/f^2$ region and $1/f^3$ region is described as

$$L\{\Delta\omega\} = 10\log\left(\frac{\Gamma_{rms}^2}{q_{\max}^2}\times\frac{\overline{i_n^2}/\Delta f}{2\cdot\Delta\omega^2}\right) \quad \text{for} \quad \omega > \omega_{1/f} \tag{3.6}$$

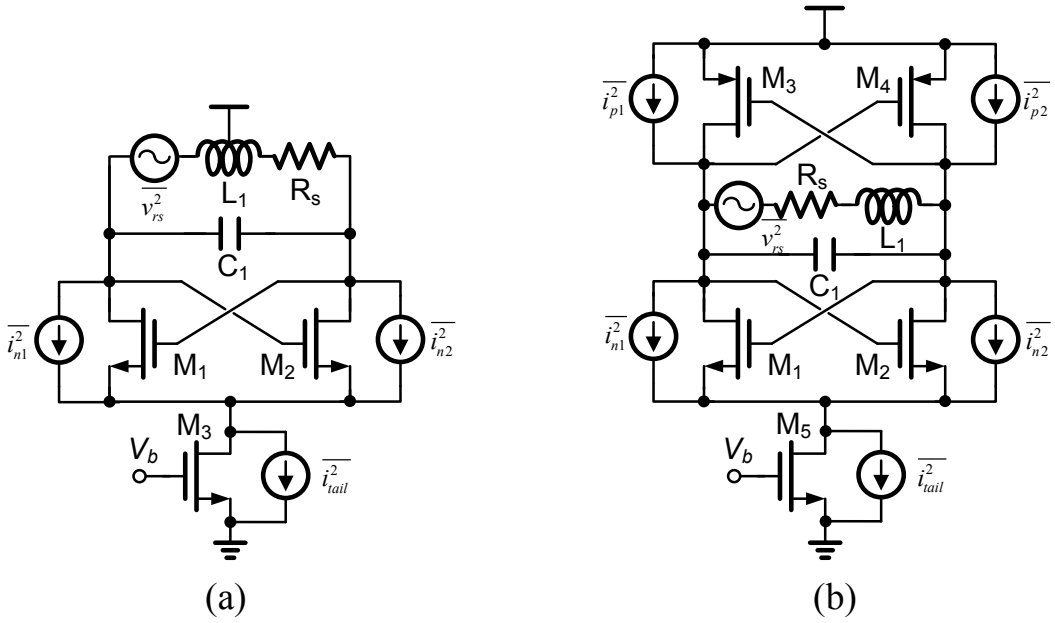


Fig. 3.9 Circuit schematic of a (a) SSO and (b) DSO with N-MOS tail current

$$L\{\Delta\omega\} = 10\log\left(\frac{c_0^2}{q_{\max}^2} \times \frac{\overline{i_n^2}/\Delta f}{2\cdot\Delta\omega^2} \times \frac{\omega_{1/f}}{\Delta\omega}\right) \quad \text{for} \quad \omega < \omega_{1/f} \tag{3.7}$$

where Γ_{rms} and C_0 respectively denote the root-mean-square and DC value of ISF, q_{max} is the maximum charge stored in tank and $\omega_{1/f}$ is the corner frequency of device.

The cross-coupled LC oscillators can be categorized as double-switch-pair oscillator (DSO) and single-switch-pair oscillator (SSO) two types. Fig. 3.9 illustrates the circuit schematics of SSO and DSO both with N-MOS tail current source, and their noise source are contributed from cross-coupled pairs, tail current, and LC tank itself. The phase noise in $1/f^2$ region for DSO and SSO can be respectively derived [54]

$$L_{DSO}(\Delta\omega) = 10\ \log\left[\frac{k_B T}{A_{DSO}^2 C_{\tan k}{}^2 (\Delta\omega)^2 R_p}\left(1+\frac{\gamma_n+\gamma_p}{2}\right)\right] \quad \text{for DSO} \tag{3.8}$$

$$L_{SSO}(\Delta\omega) = 10\ \log\left[\frac{k_B T}{A_{SSO}^2 C_{\tan k}{}^2 (\Delta\omega)^2 R_p}(1+\gamma_n)\right] \quad \text{for SSO} \tag{3.9}$$

The γ_p and γ_n presents the channel noise of P-MOS and N-MOS, respectively. Assume γ_p and γ_n are equal, and everything else is also the same, except the oscillation amplitudes A_{dso} and

Table 3.1 Comparison with DSO and SSO

	DSO	SSO	
V_{DD}	1	1	0.5
I_{tail}	1	1	2
Phase noise	1	0.25	1
Figure of merit	1	0.25	1

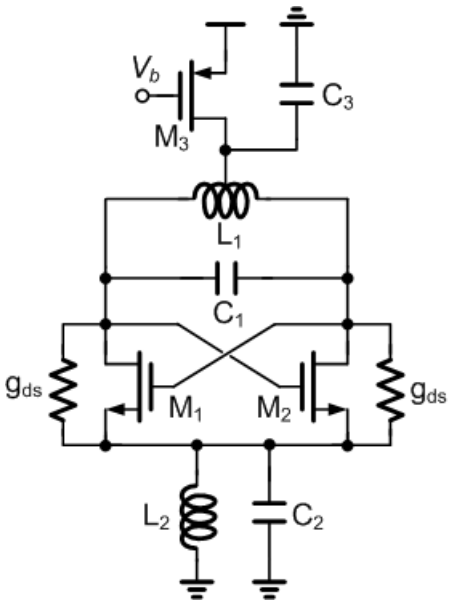


Fig. 3.10 Circuit schematic of a SSO with noise filtering technique

A_{sso}. We have seen that, for the same bias current, the DSO has double oscillation amplitude, compared to the SSO and results in a phase noise which is 6 dB lower in the DSO. It figured out that DSO does not have to pay any noise penalty associated to the second switch pair. In fact, what happens is that each switch in the DSO generates only half as much noise as each switch in the SSO, so that the total noise is the same in both oscillators.

Although DSO has better phase noise performance when operating at the same bias current and power supply, the SSO can operate at half power supply and twice bias current to achieve the same FoM of DSO, as summarized in Table 3.1 which the values are normalized to DSO. Therefore, SSO is suitable for low voltage supply than DSO by its nature. On the other hand, if a chip with power management cannot offer an extra half power supply to SSO, DSO is more properly to be adopted in this situation.

To suppress more phase noise, a noise filtering technique can be adopted [53]. As discussed before, noise components located near integer multiple of resonant frequency are

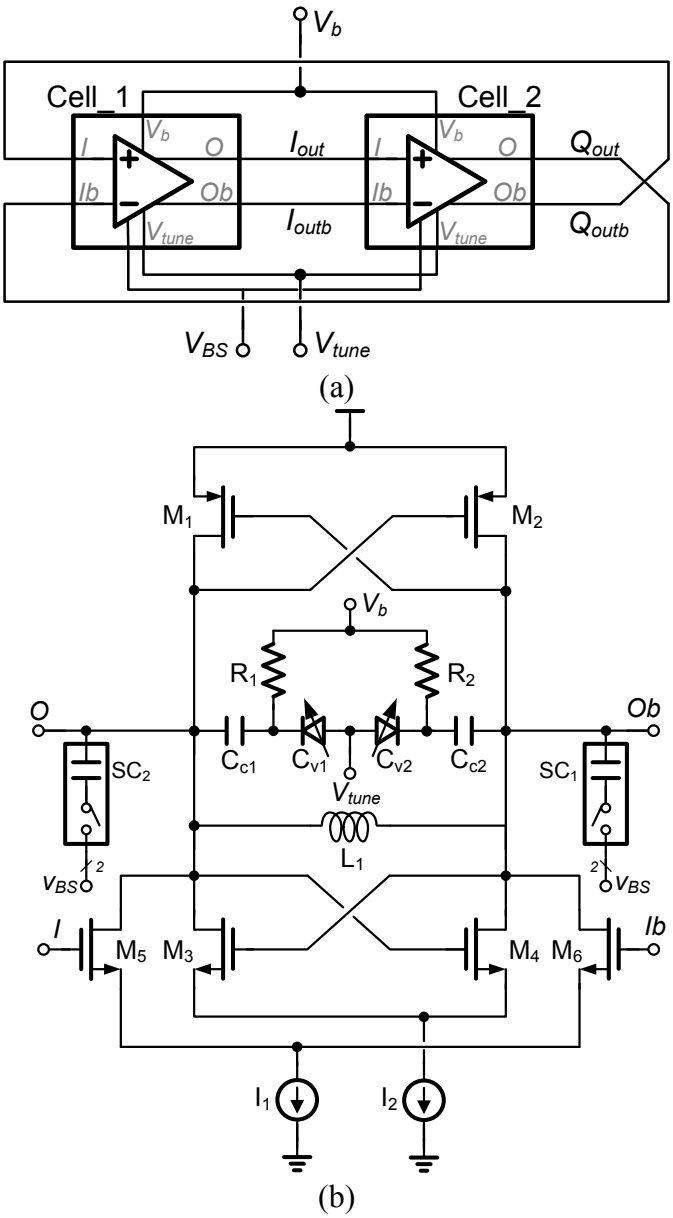


Fig. 3.11 (a) The LC tank QVCO and (b) its cell

integrated to vicinity of resonant frequency results in close in phase noise. Hence, we can design a filter to filter out the significant noise in $2\omega_0$ to achieve a low noise oscillator. Fig 3.10 illustrates a SSO with noise filtering technique. A top bias with P-MOS has adopted to obtain lower flicker noise floor, a bypass capacitor at node A also utilizes to bypass the noise at $2\omega_0$. Besides, an auxiliary LC-tank is added at the source of cross-coupled pair and resonates at $2\omega_0$ to prevent g_{ds} of the switch pair in triode region to degrade the quality factor of LC-tank.

A quadrature VCO (QVCO) and a differential VCO respectively operates at 8.4 GHz and 2.4 GHz is implemented using 180 nm CMOS technology. Under a single 1.8 V power

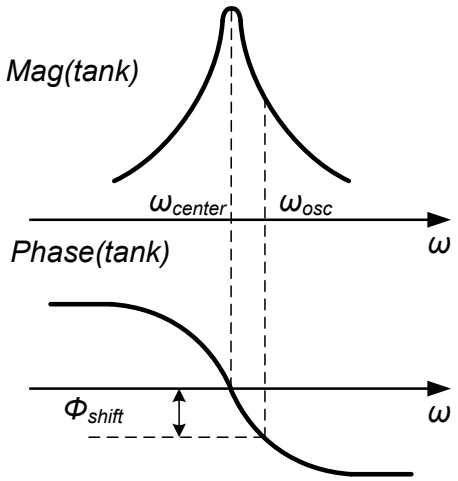


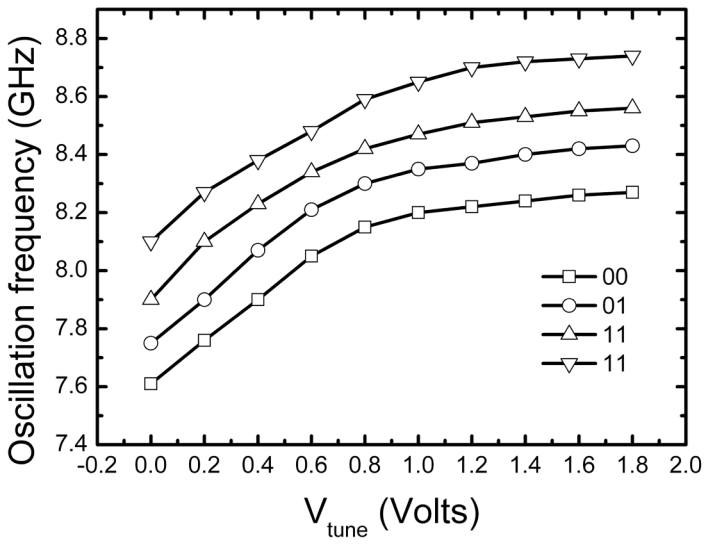
Fig. 3.12 The conceptual diagram of QVCO

supply, both of them are base on a complementary architecture. Fig. 3.11 illustrates the LC tank QVCO and its core cell. Both C_{v1} and C_{v2} are accumulation mode MOS varactors for fine frequency tuning. In addition, the switched capacitor SC_1 and SC_2 are added in parallel for coarse tuning to cope with PVT variations. The quadrature output employs anti-phase coupling technique to form a two stage ring oscillator between two differential VCOs. By injecting out phase current to tank through M5 and M6, the oscillation frequency must deviate from ω_{center} by a greater amount so that tank provides the required phase shift, as shown in Fig. 3.12. As the frequency is increasingly farther from the resonant frequency, the Q falls and the phase noise raises as well. Thus it is desirable to sustain anti-phase coupling while minimize the coupling factor defined as

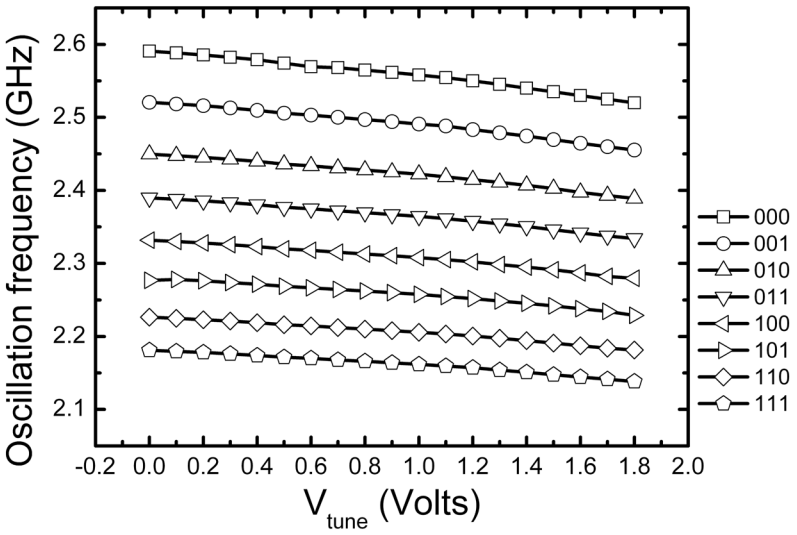
$$coupling\ factor = \frac{I_1}{I_2} \tag{3.10}$$

A coupling factor of approximately 25% typically provides a reasonable compromise between Q degradation and oscillation reliability for synchronization. Under this condition, the oscillation frequency can be derived as

$$\omega_{osc} = \frac{1}{\sqrt{LC}} \times \sqrt{1 - \frac{1}{4Q}} \tag{3.11}$$



(a)



(b)

Fig. 3.13 Measured frequency tuning curve of (a) the 8.4 GHz and (b) the 2.4 GHz VCO with multiband tuning

Fig. 3.13(a) shows the measured oscillation frequency versus tuning voltage under 2 bits coarse tuning. The oscillation frequency of QVCO can cover the wanted frequency of 8448 MHz at code 01 while drawing about 5 mA from a 1.8 V power supply. The QVCO will be employed in chapter 5 to design an ultra wideband and fast settling frequency synthesizer. On the other hand, Fig. 3.14 shows another complementary VCO operating at 2.4 GHz. The 2.4 GHz VCO have 3 bits coarse tuning due to the requirement of low K_{VCO}. The design policy is the same with QVCO and the measured oscillation frequency versus tuning voltage under 2 bits coarse tuning is shown in Fig. 3.13(b). The VCO consumes 2 mA under a 1.8 V power

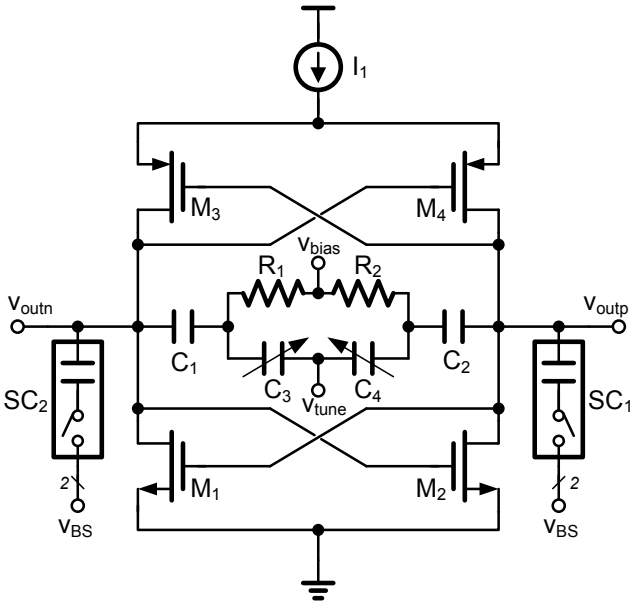


Fig. 3.14 Circuit schematic of the 2.4 GHz VCO

supply with K_{VCO} around 100 MHz/V. This 2.4 GHz VCO will be utilized in Crystal-less frequency synthesizer and receiver introduced in chapter 6.

3.3. Switched-Mode Standing Wave Oscillator

Millimeter wave applications in sensing, advanced imaging, and bio-agent chemical detection have drawn tremendous research efforts in the past few years. For pervasive adaptations, compact and cost-effective signal source is a key component to materialize these systems. Recently, CMOS oscillators in nano-meter technology have demonstrated strong potential to be applied in the sub-Tera Hz frequency range (0.1-1 THz) [55]-[57]. These designs are basically based on LC-tank architecture and try to multiply its output frequency through a multi-phase edge combing [56] or push-push techniques [57]. As the operating frequency advances to hundreds of GHz range, matching, cross-coupling, and insertion loss of transmission lines between oscillators and edge combiner become more and more critical for a successful design. Besides, the edge combiner itself may become the bottleneck of the achievable frequency range. From the view point of power efficiency, edge combiner tries to eliminate lower order harmonics by vector cancellation. It turns out to burn a lot of DC power in vain since its output signal becomes quite small for a higher multiplication factor.

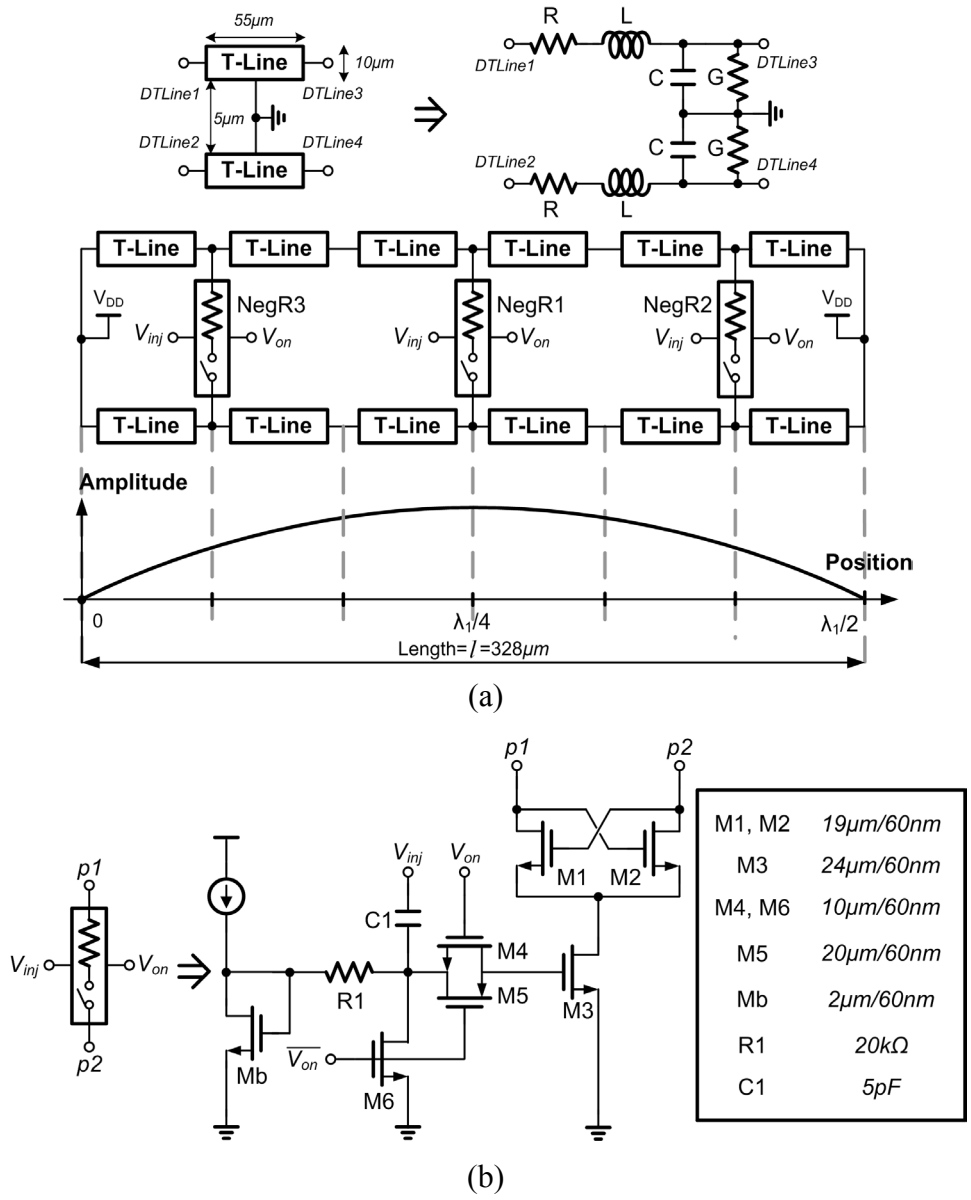


Fig. 3.15 (a) The proposed switched-mode standing wave oscillator architecture and (b) detailed circuit schematic

In contrast to LC-tank oscillators, wave-based oscillators are capable of pushing their output frequency close to devices' cut-off frequency (f_T) by distributing parasitic capacitance along the transmission line [58]-[62]. The output frequency can be varied by switching capacitor and varactor tuning [60]. Under the ultimate frequency limitation, the oscillation speed is primarily determined by the characteristics of the transmission line. Conventional standing wave or traveling wave oscillator or distributed oscillator is operated at its fundamental mode [58]-[62], and is difficult to generate double or triple output frequency in a single oscillator in contrast to its multi-band LC oscillator based counterparts [9]. In order to facilitate multi-band operation, this section proposes a switched-mode standing wave

oscillator capable of generating fundamental and triple output frequency in the sub-THz range by nature. Different excitation modes are enabled by digital control without resort to other high speed circuits or edge combiner. Additionally, incorporating mode enabling and sub-harmonic injection locking, the proposed SWO can be synchronized to external reference to further improve phase noise performance. The close-in phase noise is improved by about 18 dB with the proposed scheme when the SWO is with synchronous lock.

3.3.1. Circuit Implementation

Fig. 3.15(a) shows the proposed standing wave oscillator architecture [64]. As an experimental prototype, it is composed of circular differential transmission lines (TL) and three negative impedance converters equally-spaced along the TL to compensate power loss and sustain oscillation. Under the boundary condition of AC ground at the both ends of TL, odd mode excitations are preserved and the resonant frequency can be derived as

$$\omega_{osc} = \frac{\omega_{phase\_velocity}}{\lambda} = \frac{1/\sqrt{LC}}{2l/(2n+1)} = \frac{2n+1}{2l\sqrt{LC}} \quad n = 0,1,2,... \tag{3.12}$$

where L and C respectively represent the equivalent inductance and capacitance per unit length of the TL, l denotes the TL length, λ is the wavelength under resonant frequency, and n stands for different excitation modes. It reveals that the resonant frequency of a given TL can be increased by n-fold if a higher order mode is excited. On the other hand, output frequency can be fine-tuned by adjusting its wave velocity. However, in a typical SWO, a large portion of oscillation energy is concentrated on its fundamental mode by nature, while other modes co-exist and manifest themselves as high order harmonics. In order to improve its power efficiency for different mode excitation, the fundamental mode should be suppressed to boost energy at higher order modes by imposing other constraints. As the SWO reaches the steady state, the TL poses zero or maximum power at fixed points, where the locations are varied under different mode operations. It stands to reason that different operation mode can be excited if the power recovery stations, i.e., negative impedance converters, are located right at the nodes where maximum power is generated. Fig. 3.15(b) shows the multi-mode SWO architecture and its position-dependant amplitude for fundamental mode operation. Here only the negative impedance converter NegR1 at $l/2=\lambda_1/4$ is enabled by setting the digital control signal $(V_{on}, \overline{V_{on}}) = (1,0)$, thus the transmission gate (M4, M5) is turned on. On

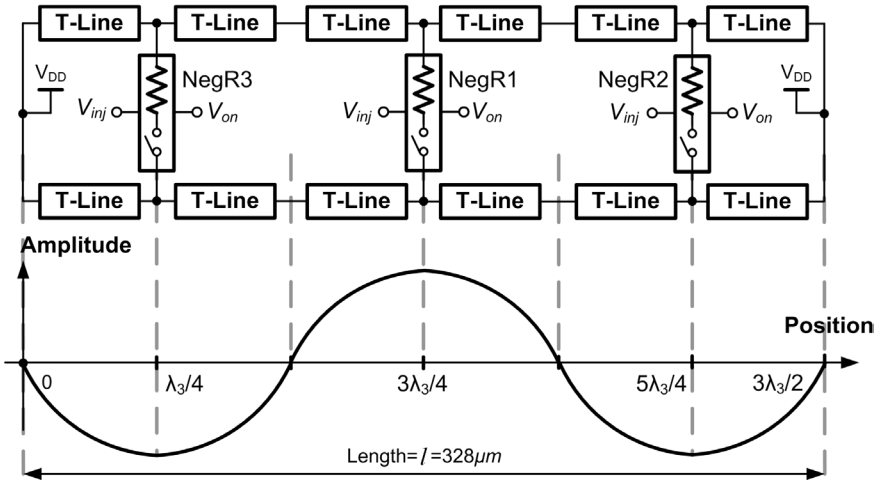


Fig. 3.16 Standing wave oscillator for mode 3 operation

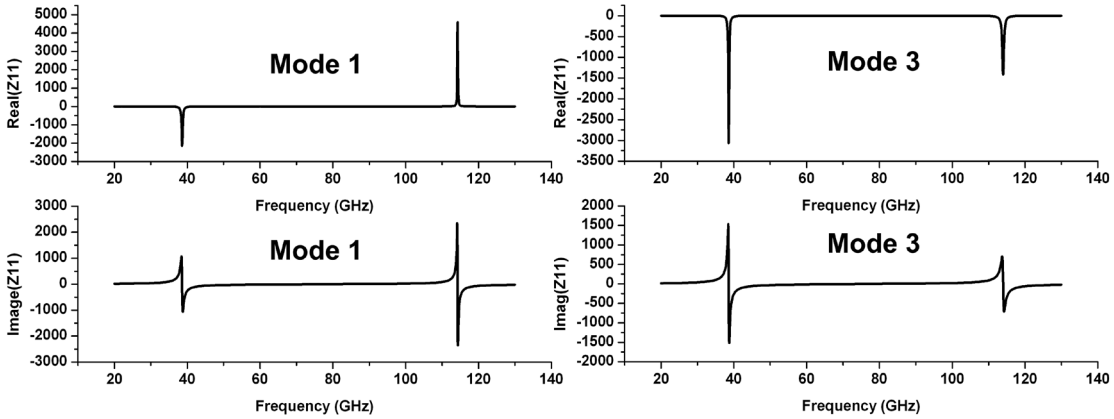
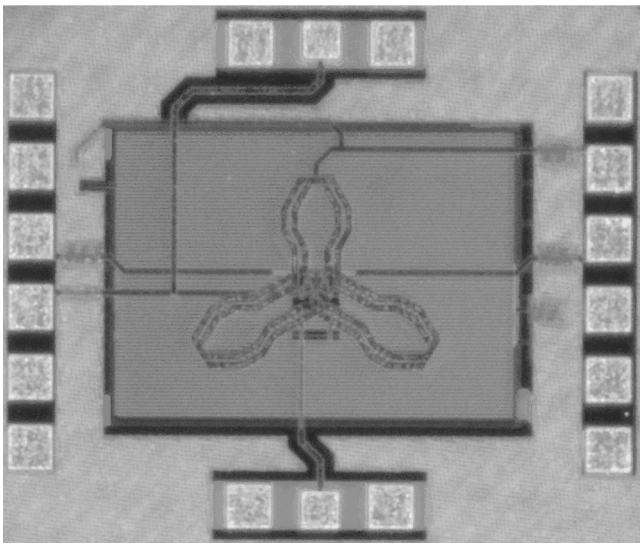


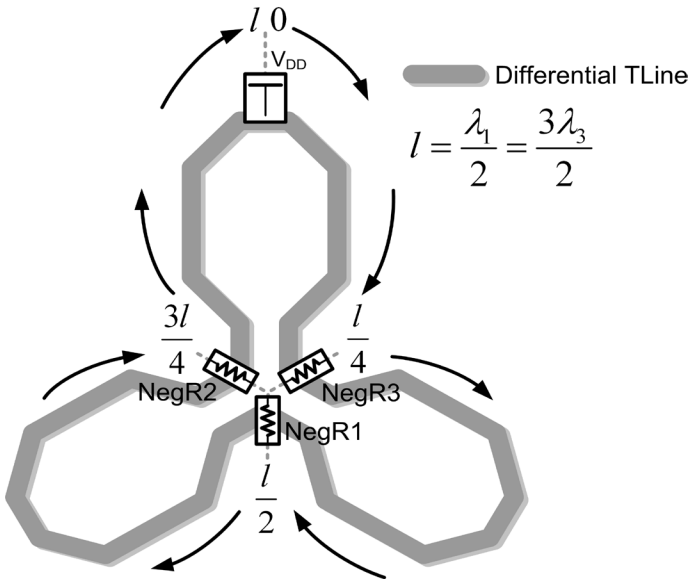
Fig. 3.17 Simulated Z_{11} at node *l/2* with different excited mode

the other hand, other negative impedance converters NegR2 and NegR3 at *l/6* ($\lambda_1/12$) and *5l/6* ($5\lambda_1/12$) are disabled by setting $\left(V_{on},\overline{V_{on}}\right)=(0,1)$ to turn on M6. Contrarily, for the mode 3 operation in Fig. 3.16, all the negative impedance converters are activated by setting the digital control signal $\left(V_{on},\overline{V_{on}}\right)=(1,0)$. In this scenario, operating points at $l=1,\ 3,\ 5\lambda_3/4$ are forced to pose maximum power as well, thus the constraints oblige the SWO to operate at mode 3.

To validate this concept, the equivalent negative impedance looking at the middle of TL (*l/2*) under different modes are summarized as shown in Fig. 3.17. For mode 1 operation, the impedance (Z_{11}) at 114GHz is positive while that at 38 GHz is negative, indicating that the SWO intends to concentrate more power on the fundamental mode. In contrast to mode 1, the negative impedance ratio for its fundamental and 3rd order harmonic becomes



(a)



(b)

Fig. 3.18 SWO (a) chip micrograph and (b) physical layout

$$\left| \frac{\mathrm{Re}\left[Z_{11}(f_1) \right]_{@38GHz}}{\mathrm{Re}\left[Z_{11}(3f_1) \right]_{@114GHz}} \right| = 2.3 \tag{3.13}$$

It reveals that most of the energy pumping into the SWO is pushed to the triple frequency. The power ratio for the triple to fundamental frequency is about 47 dB in mode 3 operation

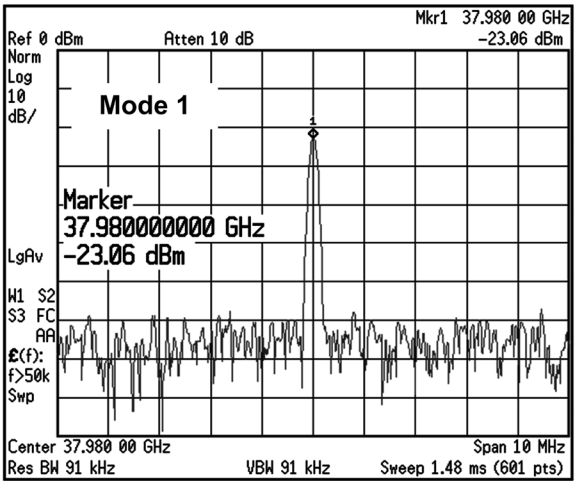


Fig. 3.19 Measured output spectrum at mode 1 (38 GHz)

by simulation. Fig. 3.18 shows the chip photo and layout of the SWO prototype. The differential TL is laid out in 3 arcs (leaves) of 328 μm long. Based on EM simulation, the quality factor of the differential transmission line is about 10 and 12 at 38 GHz and 114 GHz, respectively. To maintain layout symmetry and facilitate power picking up, all the negative impedance converters are centralized in the middle to eliminate potential transmission line mismatches, and the output signal is picked up at ($l/2$) for it manifests largest output power at any odd-mode. Besides, dummy buffers are added at the transmission line to compensate asymmetry under different mode excitation. The digital control scheme of the SWO can be applied in conjunction with phase synchronization technique [10]. In this prototype, sub-harmonics (f_{ref}) of the SWO are injected by applying V_{inj} to periodically enable and disable all the negative impedance converters as shown in Fig. 3.1. It leads to a synchronous lock/injection locked SWO. Let $f_{swo}/f_{ref}=N$, where N is a positive integer. Its frequency locking range is proportional to the power ratio between reference signal and SWO output, and inversely proportional to N. Incorporating the phase synchronization technique, the in band noise can be suppressed significantly.

3.3.2. Experimental Result

The experimental prototype is fabricated in a low leakage 65nm CMOS technology whose f_T is about 150GHz. Limited by the bandwidth of in house instruments at this moment, the fundamental mode is designed around 38 GHz, and its corresponding 3rd mode is operated at 114 GHz. Fig. 3.19 shows the measured output spectrum at 37.98 GHz (mode 1). The 3rd mode oscillation is measured at 113.67 GHz. A frequency deviation of 270 MHz in 3rd mode

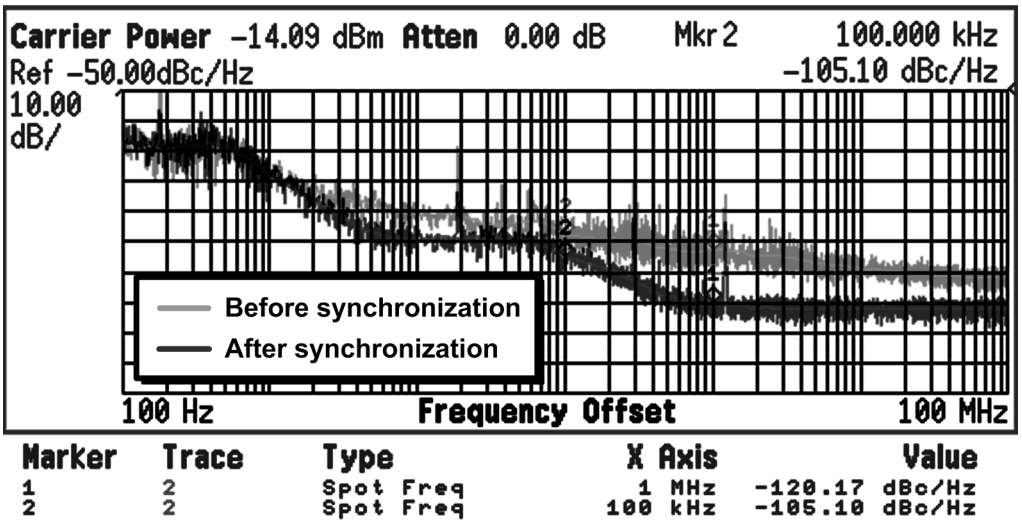


Fig. 3.20 Measured phase noise before (grey) and after (dark) synchronous lock

is observed due to the parasitic variations during mode switching, which can be overcome by fine tuning scheme. By taking signal loss from instrument into account including the loss of probes, cables and adapters, the output power at 38GHz (for mode 1) is about -15dBm. The measured output power at 114 GHz (for mode 3) is -41.2dBm, which is underestimated due to insufficient equipment bandwidth. The measured free running phase noise from a 38 GHz carrier is -102dBc/Hz at 1MHz offset, and the simulated phase noise at 38 GHz and 114 GHz is about -105 dBc/Hz and -94 dBc/Hz at 1 MHz offset, respectively. With the injection of a sub-harmonic reference f_{swo}/N (N=1, 2, 3), whose phase noise at 1 MHz offset are -127 dBc/Hz, -133 dBc/Hz and -135 dBc/Hz, the SWO phase noise improvement is about 18 dB thanks to the clean reference source. It opens the opportunity to realize an ultra low noise signal source in the sub-THz range. Fig. 3.20 shows the phase noise profile before (grey) and after (dark) synchronous lock condition. With a minimum power of -30 dBm, -12 dBm and -3 dBm sub-harmonic (f_{swo}/N=*38 GHz, 19 GHz, 9.5 GHz, N=1, 2, 3*) injection, the frequency locking ranges are 1500MHz, 40MHz and 6MHz respectively without resort to other frequency tuning schemes. The locking range can be extended with the aid of varactors or frequency tracking loop. For mode 1 and mode 3 operations, this chip respectively consumes 4 mA and 20 mA under a 1.2V power supply. The chip size is 720×880 μm^2.

This section proposes a novel concept to triple the SWO output frequency by exciting different mode operations without reconfiguring the transmission line, switched resonator, or other high speed circuits like edge combiner. Additionally, incorporating mode enabling and sub-harmonic injection locking, the proposed SWO can be synchronized to external reference

Table 3.2 Performance benchmark with SWO

	This work	[63]	[59]	[62]	[61]	[60]
Technology	65nm CMOS	90nm CMOS	180nm CMOS	180nm CMOS	120nm SOI	130nm CMOS
Power supply (V)	1.2	N/A	1.5	1.8	1.5	1.2
Power dissipation	4.8mW 24mW(1)	14mW	27mW	4.7mW	7.5mW	30mW
Max. freq. (GHz)	38 114 (1)	21 55(4)	40	14	44	12
PN@1MHz (dBc/Hz)	-102(2) -120(3)	-101 -87	-100	-110	-101	-105
P_{out} (dBm)	-15(3) -41(1)	N/A	-13.6	-15.3	-6	N/A
FoM	187(2) 205(3)	176 170(4)	178	188	185	172
Topology	standing wave	LC -resonator	standing wave	standing wave	traveling wave	traveling wave
Operation mode	Mode1 Mode3	Mode1 Mode3	Mode1	Mode1	Mode1	Mode1

(1) Mode 3 operation for $f_{osc}=(2n+1)\times f_{fundamental}$, where n=1

(2) Mode 1 operation without synchronous lock

(3) Mode 1 operation with synchronous lock

(4) Mode 3 operation (by switched resonator) with $f_{osc}=(n/2+1)\times f_{fundamental}$, where n=3

to further improve phase noise performance. The measured close-in phase noise is improved significantly with the proposed scheme when the SWO is with synchronous lock. Table 3.2 shows the performance benchmark with the prior art using standing wave [59][62], traveling wave [60][61], and LC-tank topologies [63]. Based on the figure of merit in terms of noise performance and power consumption

$$FoM = -PN + 20\log\left(\frac{f_o}{\Delta f}\right) - 10\log\left(\frac{P_{diss}}{1mW}\right) \tag{3.14}$$

The proposed SWO manifests superior phase noise performance and FoM (187 and 205 without and with synchronous lock) compared to traveling wave or LC-tank based architectures, and is the only SWO that is capable of switched mode operation.

3.4. Conclusion

The design considerations of LC-type oscillators including noise analysis, noise filtering techniques, and comparison of SSO and DSO topology are introduced in this chapter. By these analysis proposed from prior arts [51]-[54], we implement a multiband 8.4 GHz and 2.4 GHz VCO based on DSO topology and they will be employed in chapter 5 and chapter 6 for proposed frequency synthesizers. Furthermore, a switched-mode standing wave oscillator capable of generating fundamental and triple output frequency in the sub-THz range is presented. It proposes a novel concept to triple the SWO output frequency by exciting different mode operations without reconfiguring the transmission line, switched resonator, or other high speed circuits like edge combiner. Additionally, incorporating mode enabling and sub-harmonic injection locking, the proposed SWO can be synchronized to external reference to further improve phase noise performance. Experimental results are compared to the prior arts [59]-[63] and good performances can be observed.

Chapter 4

LC-Type Digitally Controlled Oscillator

In past few years, the design flow and circuit techniques for multi-gigahertz wireless applications are typically quite analog intensive and utilize process technologies that are integrated with a digital baseband. Recently, the digital baseband migrates to advanced nanometer digital CMOS process, while the limited voltage headroom does not offer any advantages to analog circuits except to higher f_T and f_{max} of devices. Hence the RF circuits at the ISM band take very few advantages from advanced technologies. To design a high-volume, power and cost effective SOC solution for mobiles, a new paradigm of DRP [40]-[50] is reported. Due to the time domain resolution of a digital signal edge transition is superior to the voltage resolution of analog signals in nanometer technologies, an all digital PLL (ADPLL) for GSM system was proposed [42]-[43]. A DCO also plays an important role in ADPLL, just likes VCO to an analog PLL. To move a SOC for DRP to higher frequency band and data rates, we proposed two DCOs at 10 GHz and 40 GHz of operation frequency in this chapter. One is for 10 Gbps of OC-192 communication, and another is for dual-IF 60 GHz UWB system. The organization of this chapter is as follows. A design consideration of a DCO is introduced in section 4.1. A wide tuning range DCO for 60 GHz UWB system with experimental results is reported in section 4.2. Section 4.3 proposed a 10 GHz high resolution DCO for OC-192 with measurement result.

4.1. Design Consideration

A DCO system includes a core circuits and a tuning circuits. The DCO core is the same with a continuous time oscillator, and its design considerations such as noise, jitter and oscillation criteria are discussed in section 3.1 and section 3.2. In addition to core circuits, the tuning circuits are interface that converts continuous controlled voltage to discrete controlled code. Thus not only the controlled signal is discrete, but also the output frequency becomes discrete. To obtain a finer frequency resolution, a delta-sigma modulator is typically added to modulate controlled code as a frequency interpolation. An extra noise contribution effect the ADPLL due to finite frequency resolution of DCO. The noises are summarized as quantization noise and dithering noise which will be introduced as follows.

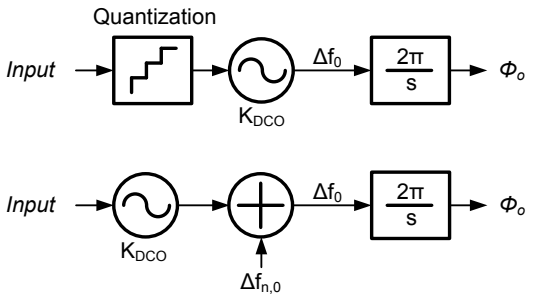


Fig. 4.1 DCO quantization noise model

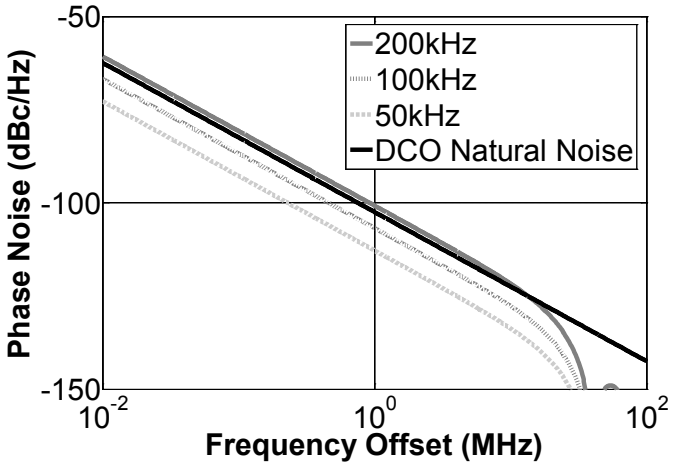


Fig. 4.2 Phase noise due to frequency quantization of different frequency resolution step

Due to the finite DCO frequency resolution, the quantization error will introduce noise to the RF output signal. To gain insight into the quantization effects on the DCO phase noise, consider the quantization noise model [45], shown in Fig. 4.1. The quantization process can be modeled as an infinite-precision tuning signal added by an uniformly distributed random variable $\Delta f_{n,0}$ with white noise spectral characteristics. The quantization noise is then converted to phase noise through the $2\pi/s$ integration. The output phase noise due to the finite quantization error can be expressed as [45]

$$L_{Quantize}(\Delta f) = \frac{1}{12} \times \left(\frac{\Delta f_{res}}{\Delta f} \right)^2 \times \frac{1}{f_{REF}} \times \left(2\mathrm{sinc} \frac{\Delta f}{f_{REF}} \right)^2 \tag{4.1}$$

In (4.1), Δf_{res} is the DCO quantization step which indicates the corresponding frequency deviation of one DCO control code. It can be seen that the output phase noise due to quantization process can be reduced by increasing the DCO frequency resolution. With careful design, the phase noise contributed from the quantization can be made below the

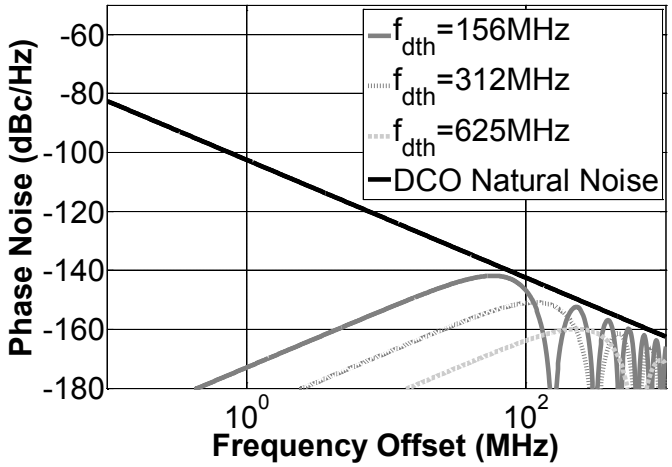


Fig. 4.3 Phase noise due to ΣΔ-shaped frequency quantization with different dithering frequency

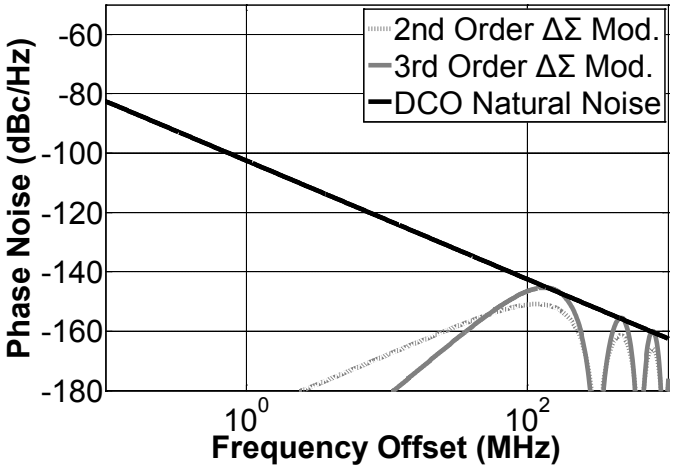


Fig. 4.4 Phase noise due to ΣΔ-shaped frequency quantization with different order of ΣΔ modulator

natural DCO phase noise resulted from the finite quality factor of the LC tank and noise of active devices. As mentioned in section 3.2, the phase noise of the LC tank oscillator can be expressed as [51]

$$S_{\varphi_{n,DCO}}(\Delta f) = \frac{\overline{i_n^2}/\Delta f}{q_{\max}^2} \frac{\Gamma_{rms}^2}{8\pi^2 \Delta f^2} \tag{4.2}$$

where $\overline{i_n^2}/\Delta f$ is the PSD of the equivalent parallel current noise, Γ_{rms} is the rms value of the impulse sensitivity function (ISF) associated with that noise source, q_{max} is the maximum signal charge swing which is defined as the product of the tank capacitance and maximum

signal swing $C_{tank}V_{swing}$, and Δf is the the offset frequency from the carrier. Consider the DCO with different frequency step Δf_{res} and assume that the quality factor of the inductor is 8. By estimated parameters, the phase noise spectrum due to frequency quantization is shown in Fig. 4.2. The spectrum shows that the quantization noise is below the DCO natural noise when Δf_{res} is less than 100kHz. This result suggests that the DCO frequency gain K_{DCO} should be less than 100kHz/LSB. Besides, as also mentioned in chapter 3, smaller K_{DCO} (K_{VCO}) can reduce the peaking in the phase noise spectrum and thus improves the jitter performances. However, the achievable finest frequency step by switching a minimum size varactor is about 120kHz when tank inductance is 1.2nH. Finer resolution can be accomplish by means of high-speed ΣΔ dithering [45]. Due to the wordlength limitation of the digital dithering circuit, there will still be a phase noise contribution due to the finite resolution per (4.1), with $\Delta f_{res}=\Delta f_{res,I}/2^{WF}$, where $\Delta f_{res,I}$ is the frequency step without utilizing ΣΔ dithering and WF is the wordlength of the dithering circuit.

Due to the noise shaping capability of the ΣΔ modulator, the quantization noise energy induced by the finite frequency step Δf_{res} is moved toward the high frequency offset at the RF output. The phase noise spectrum due to the ΣΔ-shaped frequency deviation is [45]

$$L_{\Delta\Sigma}(\Delta f)=\frac{1}{12}\times\left(\frac{\Delta f_{res}}{\Delta f}\right)^2\times\frac{1}{f_{dth}}\times\left(2\sin\frac{\pi\Delta f}{f_{dth}}\right)^{2n} \tag{4.3}$$

where f_{dth} and n denote the sampling frequency and the order of the ΣΔ modulator, respectively. The f_{dth} is normally much higher than f_{REF} and can be easily derived from the DCO by dividing the DCO output signal. Fig. 4.3 shows the phase noise spectrum due to ΣΔ-shaped frequency quantization with different dithering frequency f_{dth}. The 2nd ΣΔ modulator is assumed to plot this figure. It can be seen that the ΣΔ-shaped quantization noise is below the DCO natural noise with a margin of 5dB when f_{dth} is higher than 312 MHz (divided-by-32 of the DCO output). Fig. 4.4 shows the phase noise spectrum due to ΣΔ-shaped frequency quantization with 2nd and 3rd order ΣΔ modulator. Despite of the low in-band noise for 3rd order ΣΔ modulator, the noise energy appeared in high frequency offset rises over the DCO natural phase noise. Consequently, a 2nd order ΣΔ modulator triggered by the divided-by 32 of the DCO output is selected in this design.

4.2. Wide Tuning Range Digitally Controlled Oscillator

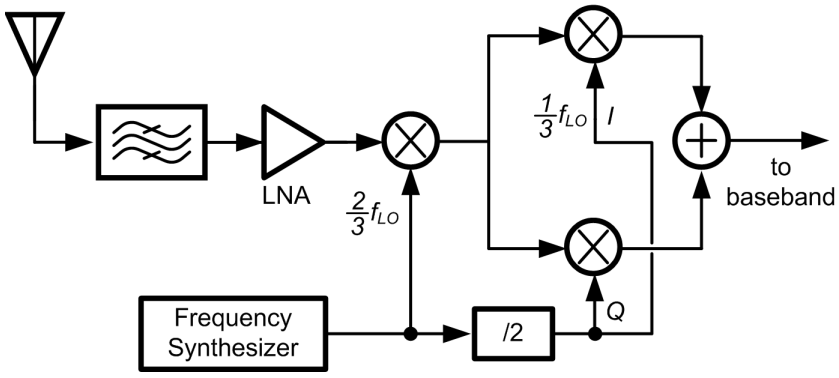


Fig. 4.5 The front-end architecture for a 60 GHz dual-IF UWB system

4.2.1. Circuit Implementation

Short range multi-Gbps wireless interconnects has motivated marvelous research efforts recently [66]-[76]. At 60-GHz unlicensed frequency band, a 7-GHz wide spectrum is provided for up to 6-Gbps UWB applications. With the rapid developments of the VLSI process, nano-meter CMOS is considered as promising technologies to make RFICs for the broadband wireless interconnects cost effective and feasible. In the RF transceiver front-end, LC voltage-controlled oscillators (VCOs) are extensively used in frequency synthesizers to provide local carriers for up and down frequency conversion. Thus its performance is essential to the wireless transceiver. Major design issues of a VCO are focused on oscillating frequency, phase noise, output power level, and frequency tuning range. For portable devices, the power dissipation is also of special concern.

Conventionally, millimeter-wave (MMW) band LC-VCOs employ accumulation-mode MOS (A-MOS) varactors for frequency tuning [77]-[82]. For a typical LC-VCO, the loading capacitance includes the parasitic capacitance contributed by the succeeding buffer stage and path routings. In order to achieve 60-GHz operating frequency, the varactor capacitance (C_{var}) and the corresponding tuning range become severely limited. This issue becomes even more critical under low supply voltage, which is required for nanometer CMOS operation.

It is well known that the phase noise performance of a VCO degrades when the VCO gain, K_{VCO}, increases [84]. However, for a single band VCO, K_{VCO} is proportional to its oscillating frequency for the same frequency tuning percentage. Considering an oscillator with 10% frequency tuning range and 1-V tuning voltage, its K_{VCO} is 180 MHz/V at oscillating frequency of 1.8 GHz, but increases to 6 GHz/V if the output frequency is raised to 60 GHz. Therefore, for broadband MMW applications, multi-band VCO is necessary to degenerate VCO gain K_{VCO} and alleviate phase noise performance degradation. However,

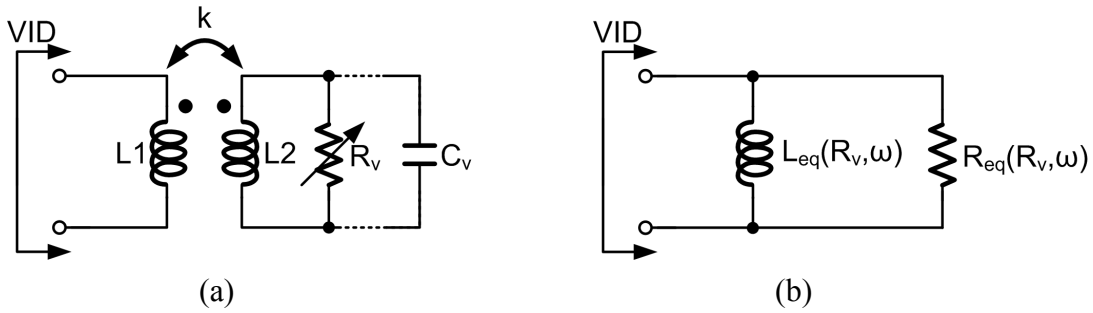


Fig. 4.6 (a) The proposed variable inductor (b) equivalent circuit model

conventional capacitor bank for multi-band operation is hardly applicable in the 60-GHz case since the C_p in the capacitance bank is too large to be tolerable. Some magnetic tuning methods have been reported [85]-[76] to increase the frequency tuning ranges of LC-tank VCOs though. Their oscillating frequencies are far less than 60 GHz.

In this section, a 40 GHz DCO employing a novel variable inductor (VID) is proposed. Based on magnetic tuning scheme, it achieves multi-band as well as broad-band operations without sacrificing its oscillation frequency. On the other hand, measurement results show that the output frequency of a 40 GHz DCO is distributed from 37.6 GHz to 43.4 GHz corresponding to 14% tuning range. It is suitable to a dual-IF architecture for a 60 GHz UWB system shown in Fig. 4.5, and can be incorporated with digital RF processor [40]-[50] in further.

Fig. 4.6(a) illustrates the schematic of the proposed VID, which consists of a transformer T_1 and a variable resistor R_v. L_1 and L_2 respectively represent the self inductance of the primary and secondary coils of T1, k is the coupling factor of the primary and secondary coils, and C_v is the parasitic capacitor at the secondary coil. The VID can be modeled as a variable inductor L_{eq} in parallel with a variable resistor R_{eq}, as is illustrated in Fig. 4.6(b). Both L_{eq} and R_{eq} are functions of R_v and the radian frequency ω. The L_{eq} and R_{eq} can be derived as that

$$L_{eq}\left(R_v,\omega\right)=\frac{R_v^2L_1\left[1-\omega^2C_vL_2\left(1-k^2\right)\right]^2+\omega^2L_1L_2^2\left(1-k^2\right)^2}{R_v^2\left(1-\omega^2C_vL_2\right)\left[1-\omega^2C_vL_2\left(1-k^2\right)\right]+\omega^2L_2^2\left(1-k^2\right)} \tag{4.4}$$

and

$$R_{eq}\left(R_v,\omega\right)=\frac{R_v^2L_1\left[1-\omega^2C_vL_2\left(1-k^2\right)\right]^2+\omega^2L_1L_2^2\left(1-k^2\right)^2}{R_vk^2L_2} \tag{4.5}$$

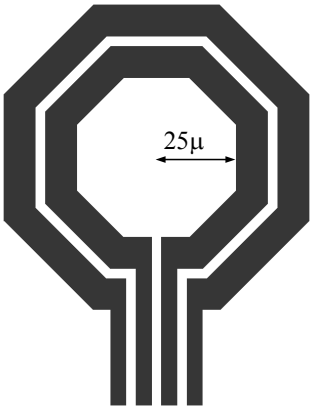


Fig. 4.7 The 1:1 Transformer layout view

If the self resonant frequencies of C_v and L_2 are larger than the operating frequency ω, i.e. $\omega_2 C_v L_2 < 1$, L_{eq} increases with the increment in R_v. Thus, the minimum equivalent inductance L_{min} is equal to $L_{eq}(0,\omega)$, and can be calculated as

$$L_{eq}(0,\omega) = L_1(1-k^2) \tag{4.6}$$

Contrarily, the maximum equivalent inductance L_{max} is equal to $L_{eq}(\infty,\omega)$, and can be calculated as

$$L_{eq}(\infty,\omega) = L_1\left(1+\frac{\omega^2 L_2 C_v}{1-\omega^2 L_2 C_v}k^2\right) \tag{4.7}$$

From (4.6) and (4.7), it can be seen that only L_{max} depends on the parasitic capacitance C_v, and its lower bound is L_1 (i.e. $L_{max} > L_1$). In this situation, the inductance tuning ratio α, defined as $[L_{eq}(\infty,\omega)-L_{eq}(0,\omega)]/L_{eq}(\infty,\omega)$, and its lower bound can be derived as

$$\alpha = \frac{k^2}{1-\omega^2 C_v L_2(1-k^2)} > k^2 \tag{4.8}$$

On the other hand, if $\omega_2 C_v L_2 > 1$, L_{eq} may become non-monotonic against R_v, and even become negative if R_v is too large. This situation should be avoided in the VID design for the VCO application.

Some simulations are performed to verify the derived results. Fig. 4.7 shows the layout

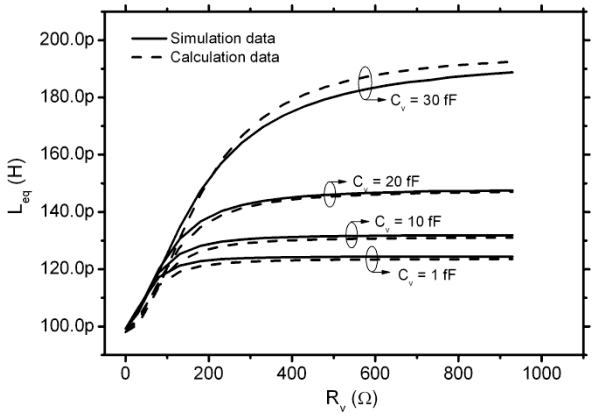


Fig. 4.8 Simulated and calculated L_{eq} for $\omega_2 C_v L_2 < 1$

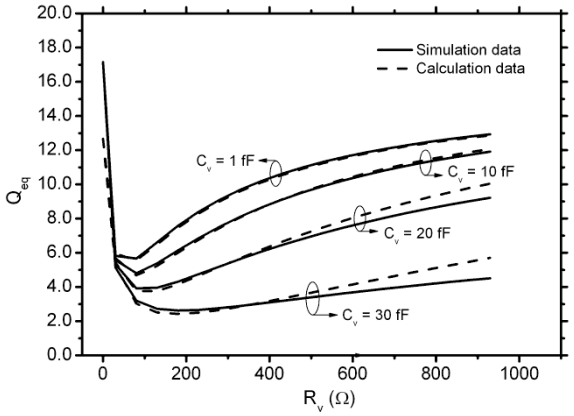


Fig. 4.9 Simulated and calculated Q_{eq} when $\omega_2 C_v L_2 < 1$

of the transformer used in the simulations. The inner radius of the primary (secondary) coil is 25 μm (37 μm); the metal width is 9 μm; and the space between the first and second coils is 3 μm. By EM simulation, the self-resonant frequency of the transformer is about 194 GHz. The self inductance of the primary (secondary) coil is about 123 pH (175 pH) and the coupling factor is about 0.45.

Fig. 4.8 shows the simulation results of L_{eq} against R_v with different C_v around 60 GHz under the constraint of $\omega_2 C_v L_2 < 1$. The L_{eq} derived in (4.4) is also shown for comparison. It can be seen that L_{eq} increases along with the increment in R_v. The inductance tuning ratio α is larger than or equal to k^2 (i.e. 0.2) in all cases. Also, only L_{max} is dependent on C_v as predicted by (5). The proposed lumped model shown in Fig. 4.6(a) can accurately represent its inductance. The other important parameter of the proposed VID is its quality factor Q_{eq}. However, Q_{eq} is strongly dependent on the parasitic resistors of the transformer which are neglected in the lumped model shown in Fig. 4.6(a). By taking the parasitic resistors into account, the Q_{eq} can be calculated as

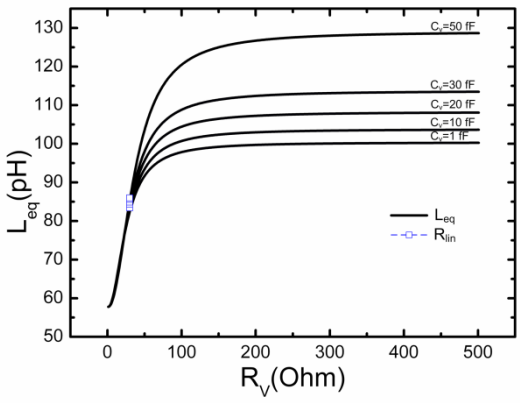


Fig. 4.10 The calculated L_{eq} and derived R_{lin} of the VID

$$Q_{eq} = \omega \cdot \frac{R_v^2 L_1 \left(1-\omega^2 C_v L_2\right)^2 + \omega^2 L_1 L_2^2 \left(1-k^2\right) + \omega^2 k^2 R_v^2 C_v L_1 L_2 \left(1-\omega^2 L_2 C_v\right)}{R_1 R_v^2 \left(1-\omega^2 C_v L_2\right)^2 + \omega^2 L_2 \left(k^2 L_1 R_v - R_1 L_2\right)} \tag{4.9}$$

where R_1 is the equivalent parasitic resistor of the primary coil. When $\omega_2 C_v L_2 < 1$, the simulated and calculated Q_{eq} with different C_v are plotted against R_v at 60 GHz in Fig. 4.9. The frequency response of the quality factor has a "V" shape, which reveals that the VID has a better quality factor in the extreme cases where R_v is nearly short or open circuit. In either case, the magnetic energy dissipated in the passive R_v can be minimized.

On the other hand, a linear operation of DCO is also proposed. The oscillating frequency of LC-tank oscillators can be derived as

$$\omega_{OSC}(\Delta L) \approx \omega_{center}\left(1-\frac{\Delta L}{2L_{center}}\right) \quad \text{when} \quad \frac{\Delta L}{L_{center}} \ll 1 \tag{4.11}$$

where ω_{center} is the center frequency of oscillator and L_{center} is the corresponding inductor value, ΔL denotes the deviation value from L_{center}. In the proposed VID, the inductance tuning ratio $\Delta L / L_{center}$ is about 0.13. Hence, a linear frequency tuning of proposed VCO can be realized by a linear VID.

According to the curve of L_{eq} shown in Fig. 4.10, it can be observed that L_{eq} has an almost linear region when R_v is small. Therefore, we rearrange the equation (4.4) of L_{eq} and the linear region can be approximated as

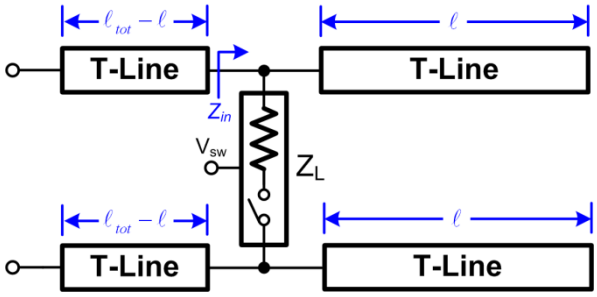


Fig. 4.11 The reconfigurable transmission line

$$R_{lin}^2 = \omega^2 L_2^2 \left(1-k^2\right)\left(6k^2-1\right) \quad \text{when} \quad \omega^2 C_v L_2 < 1 \tag{4.12}$$

Furthermore, the linear inductance under R_{lin} can be also approximated as

$$L_{eq\_lin}\left(R_v,\omega\right) = L_1\left[\frac{1}{6}\sqrt{\frac{6k^2-1}{\omega^2 L_2^2\left(1-k^2\right)}}R_v + \left(1-k^2\right)\right] \tag{4.13}$$

The above equation reveals that the linear multi-band operation can be designed by employing a linear variable resistor under R_{lin}. Fig. 4.10 shows the calculated results of L_{eq} against R_v with different C_v in solid line and the derived R_{lin} in dot line. Fig. 4.10 can be observed that the linear region is almost unaffected by the varied C_v. It means that the linear range of VID is nearly independent to the $\omega_2 C_v L_2$.

In order to design a linear resistor, a reconfigurable transmission line is proposed, as shown in Fig. 4.11. The input impedance of a terminated resistance shunt with a variable length open stub and can be derived as

$$Z\left(\ell\right) = Z_L \,\|\left[Z_0 / j\tan\left(\beta\ell\right)\right] \approx Z_0 \frac{1}{Z_0/Z_L + j\tan\left(\beta\ell\right)} \tag{4.14}$$

where Z_0, β and ℓ denotes the characteristic impedance, phase velocity and length of the transmission line, respectively. The Z_L presents terminated resistance. When Z_0 is designed to impedance match to Z_L, the real part of Z_{in} can be approximated as

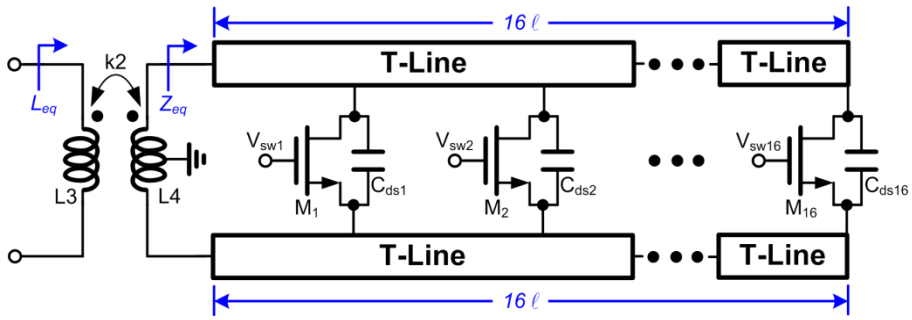
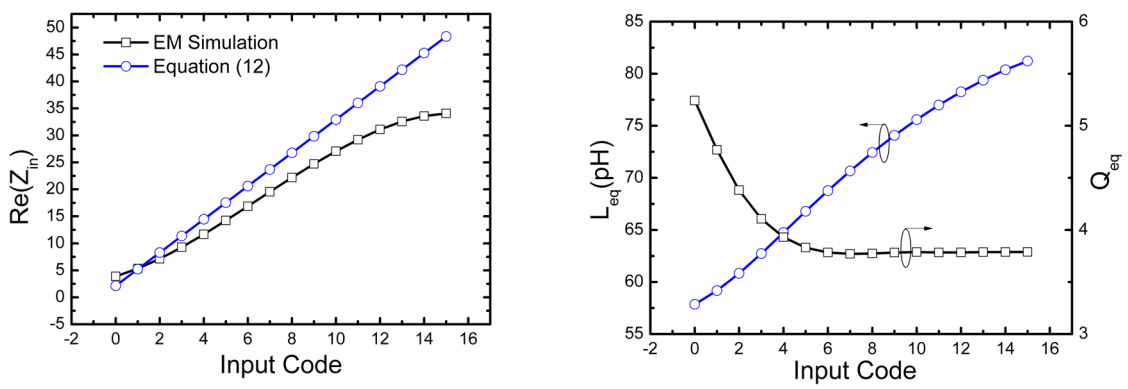


Fig. 4.12 The proposed 4-bits linear VID



(a) (b)

Fig. 4.13 (a) The EM simulated and theoretic real part of Z_{eq} and (b) equivalent inductance and quality factor of linear VID

$$\begin{aligned}\mathrm{Re}\left[Z_{in}(\ell)\right] &\approx Z_0 \frac{1}{1+\tan^2(\beta\ell)} \\ &= 0.5Z_0\left[1+\sin\left(\pi/2-2\beta\ell\right)\right] \approx 0.5Z_0\left(1+\pi/2-2\beta\ell\right)\end{aligned} \tag{4.15}$$

It reveals that the real part of Z_{in} is proportional to the length of open stub (ℓ). To prevent the self resonant frequency of secondary coil approaches oscillating frequency caused by parallel open stub, the capacitive loading on imaginary part of Z_{in} can just be compensated by the residual transmission line ($\ell_{tot} - \ell$) connected to the secondary coil of transformer. According to Fig. 4.10, the influence on the imaginary part of Z_{in} to equivalent inductance can be neglected under the linear region of VID.

The detail schematic of a 4-bits linear VID is shown in Fig. 4.12. The transmission line is divided equally into 16 segments by 16 equal MOS switches. The switches are turn one by one to reconfigure the length of open stub. One the other hand, the parasitic capacitance (C_{ds}) of each switch can be absorbed in transmission line by nature, and the turn on resistance (Z_L)

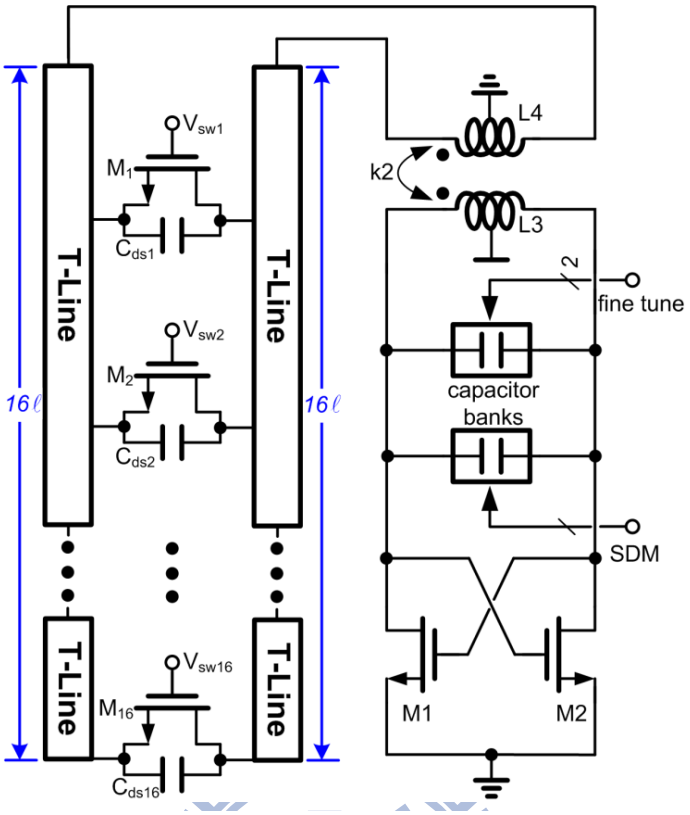


Fig. 4.14 The circuit schematic of DCO using 4-bits linear VID

is matching with Z_0. Based on EM simulation, L3, L4 and k2 of the transformer are 100 pH, 129 pH and 0.6, respectively, and Z_L (Z_0) and β of the transmission line are 46 Ω and 0.08 rad/ ℓ , respectively. Fig. 4.13(a) shows the theoretical approximated and EM simulated real part of Z_{eq}. The equivalent inductance and quality factor of linear VID is distributed from 58 pH to 82 pH and 5.5 to 3.8, respectively, as shown in Fig. 4.13(b).

By using the proposed linear VID, a 40-GHz DCO is designed and fabricated in a 90-nm CMOS technology for a dual-IF 60GHz UWB system. The circuit schematic is shown in Fig. 4.14, where the transformer L3 and L4 is implemented by the single-turn 1:1 transformer. In this experimental prototype, the 4 bits linear VID is controlled by digital codes V_{sw1} to V_{sw16} for coarse tuning, a 2-bits capacitor bank is for fine frequency tuning, and also preserves a delta-sigma inputs for frequency interpolation.

In order to reduce the parasitic capacitance at the resonator, the negative impedance converter is composed of M1 and M2 cross-coupled pair. The negative resistance provided by the cross-coupled pair M1 and M2 is denoted as $-R_{neg}$, which is approximately equal to $-2/g_m$, and g_m is the small-signal transconductance of M1/M2. R_{neg} must be smaller than R_{eq} to guarantee oscillation start-up. In this design, R_{neg} is chosen to be smaller than $R_{eq}/2.5$ within

the entire frequency range. The oscillating frequency ω of the VCO can be derived as

$$\omega = \frac{1}{\sqrt{C_t L_{eq\_lin}\left(R_v, \omega\right)}} = \sqrt{\frac{1}{C_t L_1 \left[\frac{1}{6}\sqrt{\frac{6k^2-1}{\omega^2 L_2^2\left(1-k^2\right)}}R_v + \left(1-k^2\right)\right]}}, \quad R_v \le R_{lin} \tag{4.16}$$

The VCO frequency tuning range ω_{max} and ω_{min} can be calculated as

$$\omega_{\max} = \frac{1}{\sqrt{C_t L_{eq}\left(0, \omega_{\max}\right)}} = \frac{1}{\sqrt{C_t L_1\left(1-k^2\right)}} \tag{4.17}$$

and

$$\omega_{\min} = \frac{1}{\sqrt{C_t L_{eq}\left(R_{lin}, \omega_{\min}\right)}} < \frac{1.1}{\sqrt{C_t L_1}} \tag{4.18}$$

Based on (9) and (10), the frequency tuning range (β) of the VCO can be derived as

$$\beta \equiv \frac{2\left(\omega_{\max} - \omega_{\min}\right)}{\omega_{\max} + \omega_{\min}} > \frac{2\left(1-1.1\cdot\sqrt{1-k^2}\right)}{1+1.1\cdot\sqrt{1-k^2}} \tag{4.19}$$

which is determined by the coupling factor k of the transformer. Therefore, for a given transformer to implement the VID, the frequency tuning range of the VCO employing the VID can be quickly estimated.

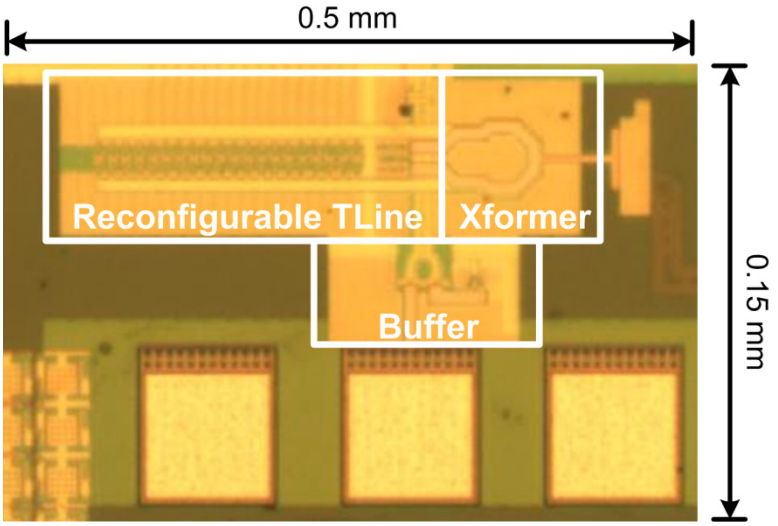


Fig. 4.15 The chip microphotograph of DCO

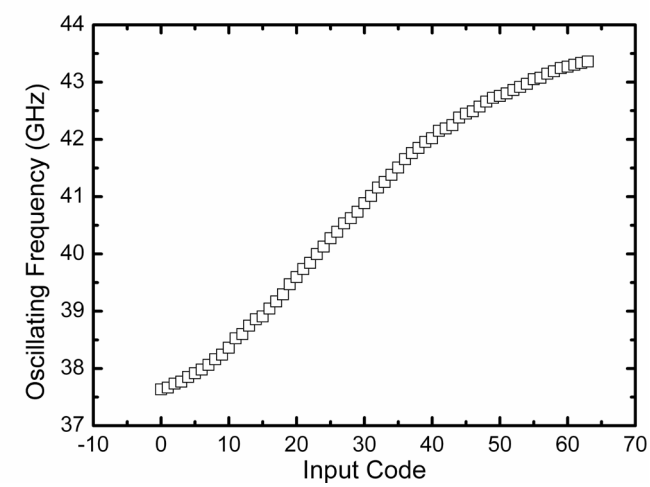


Fig. 4.16 Measured frequency tuning range versus input code of the DCO

4.2.2. Experimental Result

The chip micrograph of DCO is shown in Fig. 4.15. The core size is 0.5 × 0.15 mm^2. The circuit is measured with on-chip probing. The DCO consumes 16 mA under a 1.2 V power supply. There are two buffers at output of DCO results in about 90 fF loading capacitance, one is for measurement and another is for next stage frequency divider. Under this condition, the measured output frequency versus digital control code is shown in Fig. 4.16. The output frequency is distributed from 37.6 GHz to 43.4 GHz which meets the requirement of dual-IF 60GHz UWB system (38.8 GHz to 43.2 GHz). The proposed DCO have 14 % tuning percentage while frequency resolution is about 100 MHz per step. A finer frequency resolution can be achieved in further by incorporating with high speed dithering

Table 4.1 Performance comparison with MMW DCO

Reference	[89]	[88]	This work
Technology	90 nm	90 nm	90 nm
VDD	1.2	1.2	1.2
Frequency range (GHz)	51.3-53.3	58.27-63.83	37.6-43.4
Tuning percentage	4%	9.3%	14%
For 60 GHz UWB receiver	N/A	N/A	Dual-IF
Resolution	10 bits	2.3 bits	6 bits
PN at Δf	-116.5 at 10MHz	-90.1 at 1MHz	-109 at 10MHz
Power consumption	2.34 mW	10.6 mW	19 mW
FOM	-187.2	-175.5	-168.9
FOM_T	-179.2	-174.9	-171.9

as frequency interpolation. By taking instrument signal loss into account (including the loss of probes, cables and adapters), the output power varies from -15 dBm to -11 dBm due to the variation of quality factor within the entire frequency range. The measured phase noise performance at 10-MHz offset within the entire frequency tuning range is plotted in Fig. 4.17. Fig. 4.18 shows the measured VCO output spectrums at different frequencies.

The performance benchmark of the proposed oscillator and the prior art in the literature are summarized in Table 4.1. Three different figures of merits are illustrated to investigate their advantages. They are

$$FOM = PN - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{cons}}{1mW}\right) \tag{4.20}$$

$$FOM_T = PN - 20\log\left(\frac{f_o}{\Delta f}\frac{TP}{10\%}\right) + 10\log\left(\frac{P_{cons}}{1mW}\right) \tag{4.21}$$

where PN is the phase noise at the offset frequency Δf, f_o is the oscillating frequency, Pcons is the power consumption, and TP is the frequency tuning percentage. The proposed DCO has the widest tuning range and moderate resolution but sacrificing some FOM_T among the DCO beyond 40 GHz. Besides, for application in 60 GHz UWB system, the proposed DCO meets the requirement while has a finest frequency resolution.

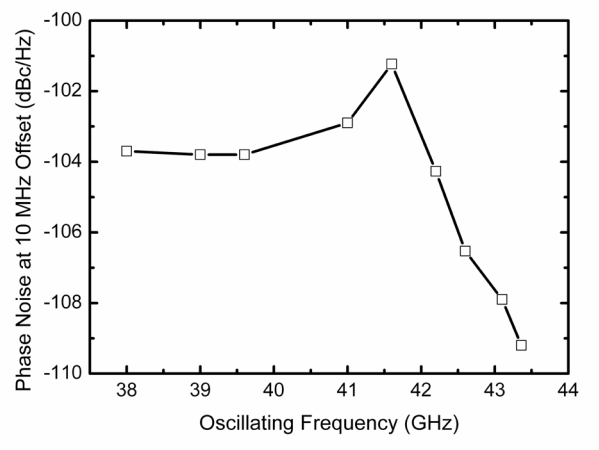
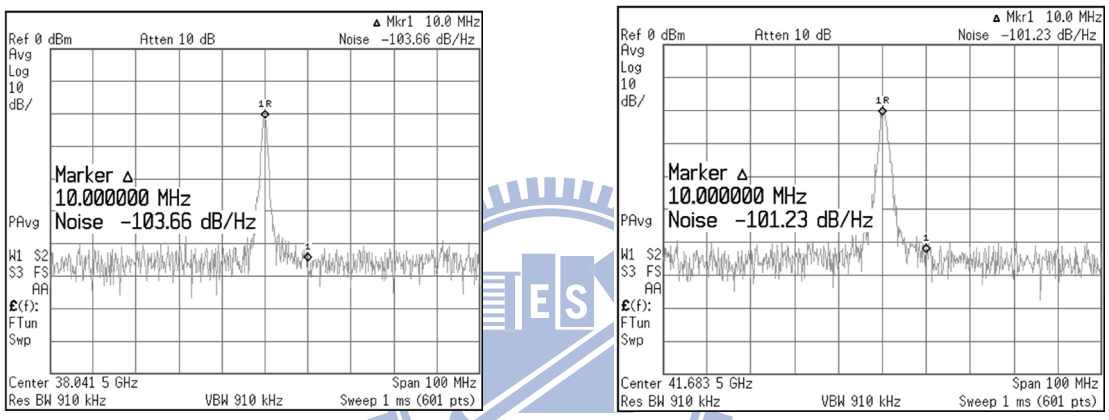
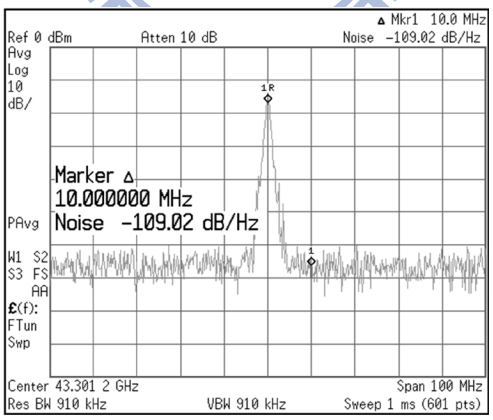


Fig. 4.17 Measured DCO phase noise at 10-MHz offset of the DCO



(a) (b)



(c)

Fig. 4.18 Measured output spectrums with noise markers at (a) 38 GHz (b) 41.6 GHz (c) 43.3 GHz

A novel variable inductor is proposed in this section. By using the variable inductor, a DCO is designed in the MMW frequency band and the DCO has a wider tuning range than the conventional VCO using varactors. Moreover, in comparison with conventional capacitor

bank, multi-band operation can be achieved without severely decreasing the oscillating frequency and increasing the chip area. The measurement results of 40 GHz DCO using proposed VID is suitable to a Dual-IF architecture for 60 GHz UWB system, and can be incorporated with digital RF processor [40]-[50] in further.

4.3. High Resolution Digitally Controlled Oscillator

In this section, the design and implementation of the digitally controlled oscillator (DCO) will be illustrated. The implemented block diagram of the DCO system is shown in Fig. 4.19. The DCO receives a 25-bits wide control word $C_{DCO}[24:0]$ from the loop filter without a sign bit and delivers a differential signal with frequency around 10 GHz to the buffers.

Due to its relatively good phase noise, ease of implementation, and better rejection of common-mode additive noise, a cross-coupled inductance capacitance (LC) oscillator is chosen. The MOS implementation of a LC oscillator can be classified into two major categories: NMOS only structure and complementary structure which uses both NMOS and PMOS in a cross-coupled fashion to compensate the power loss in LC resonator.

It has been reported that there are several reasons for the superiority of the complementary cross-coupled pair over the NMOS-only structure. The complementary structure offers higher transconductance for a given current, which results in faster switching of the cross-coupled differential pair. It also offers better symmetry of the waveform, which results in a smaller $1/f^3$ noise corner. Nevertheless, the single NMOS-only topology is chosen over the complementary one to enable the oscillators to operate in the current limited region for low voltage supply.

Since the tail current can contribute as much as 15% to the total phase noise [47] when the MOS of the current source is operated in saturation region, a PMOSs operated in linear region is used as biasing to reduce its noise contribution. The nominal bias current is 3mA and an on-chip regulator is introduced to stabilize the bias condition.

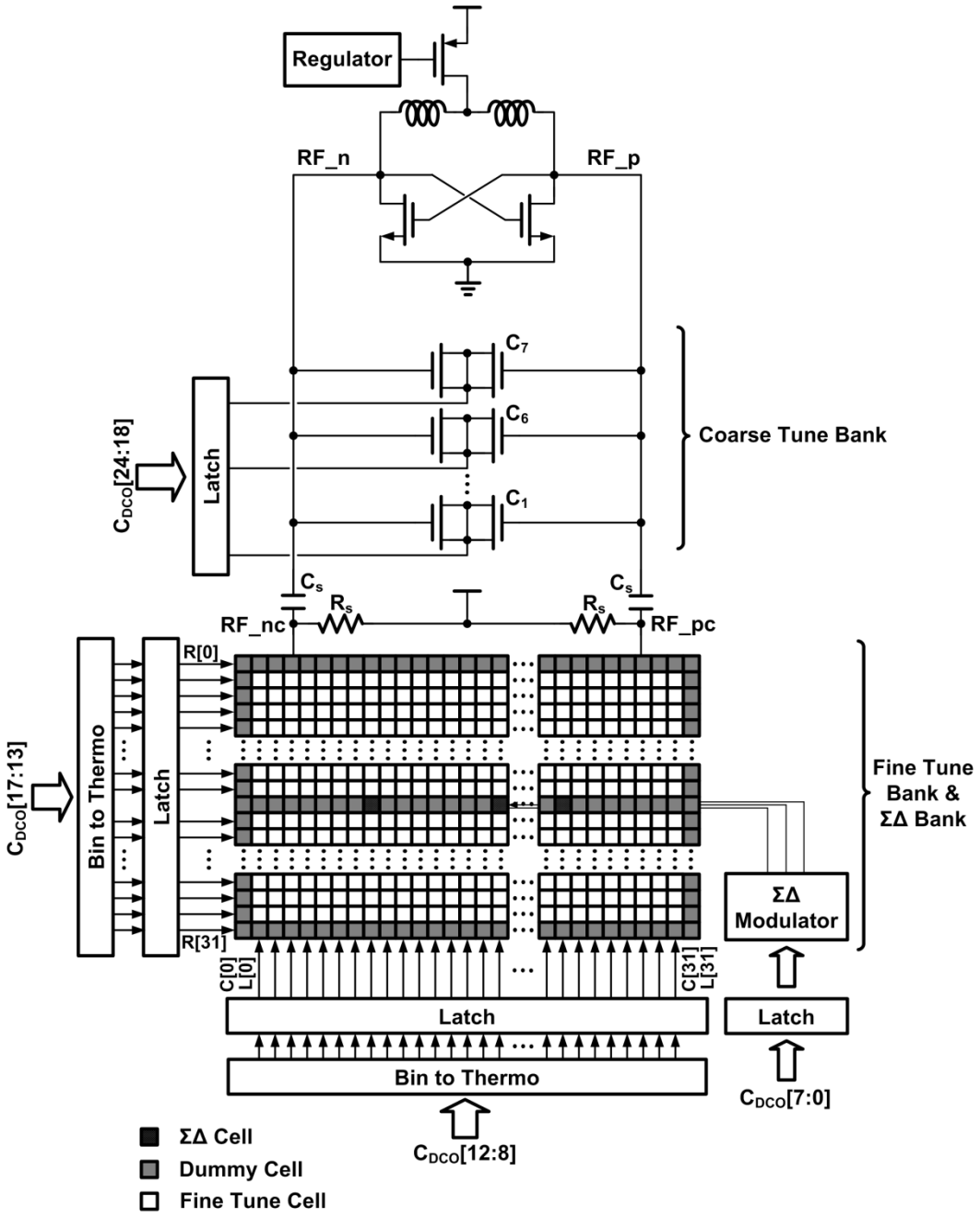


Fig. 4.19 Diagram of DCO system

4.3.1. Circuit Implementation

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Since the tail current can contribute as much as 15% to the total phase noise [47] when the MOS of the current source is operated in saturation region, a PMOSs operated in linear region is used as biasing to reduce its noise contribution. The nominal bias current is 3mA and an on-chip regulator is introduced to stabilize the bias condition.

In an ideal LC oscillator, the frequency f_{OSC} and the period T_{OSC} of the oscillation are a nonlinear function of the tank capacitance $C_{tank.}$ In the traditional voltage controlled LC oscillator, frequency tuning is achieved by controlling the effective tank capacitance with an analog control signal. The variable capacitor is typically implemented by the diode or the MOS varactor which has a non-linear relationship between the capacitance and the tuning voltage.

In the concept of the digital tuning, the oscillation frequency is made to be proportional to the input digital control word C_{DCO}. To achieve digital tuning of the oscillation frequency, the varactor can be used but only two voltage levels are applied. In the implemented DCO system, NMOS with control signal short to drain and source is used as the inversion type varactor and each varactor operates in either high or low capacitance state. When the source voltage, drain voltage drop to zero and the gate potential V_G is 1V, an inversion layer exists below the gate oxide region. This structure behaves likes a parallel-plate capacitor with only a silicon oxide dielectric in between and the capacitance of the varactor is relatively high. As the control signal rise to 1V, the depletion region is formed under the gate oxide and a small overlap capacitance dominants the capacitance of the varactor. By this way, the digital tuning can be achieved by controlling the amount of the MOS varactors in high capacitance state. Today's advanced CMOS process makes it possible to create extremely small varactors which have controllable capacitance in the order of hundreds of atto farads and results in relatively fine frequency resolution in the digital tuning LC oscillator. Fig. 4.20 shows the simulation result of the C-V curve of a NMOS varactor with gate voltage tie to 1V.

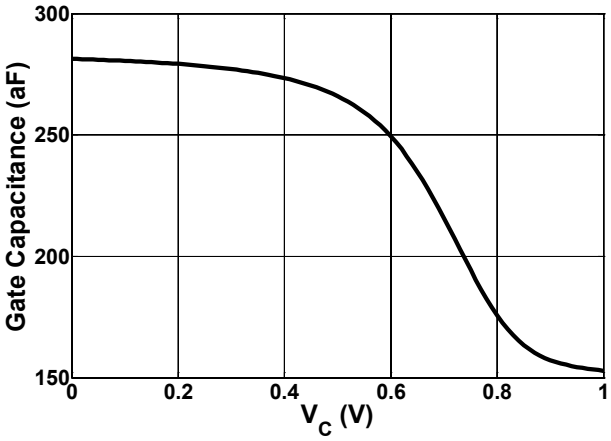


Fig. 4.20 Gate capacitance v.s. drain and source voltage, V_C, of a simulated NMOS varactor with L=0.08μm, W=0.16μm

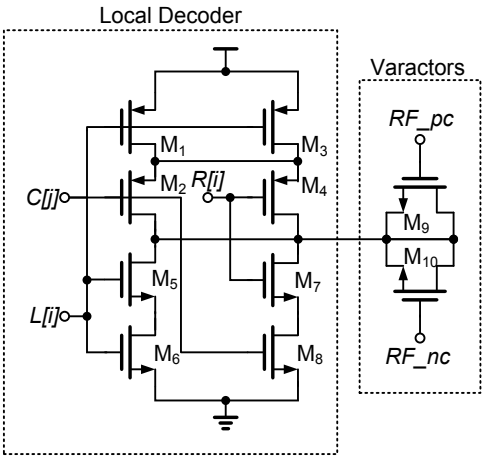
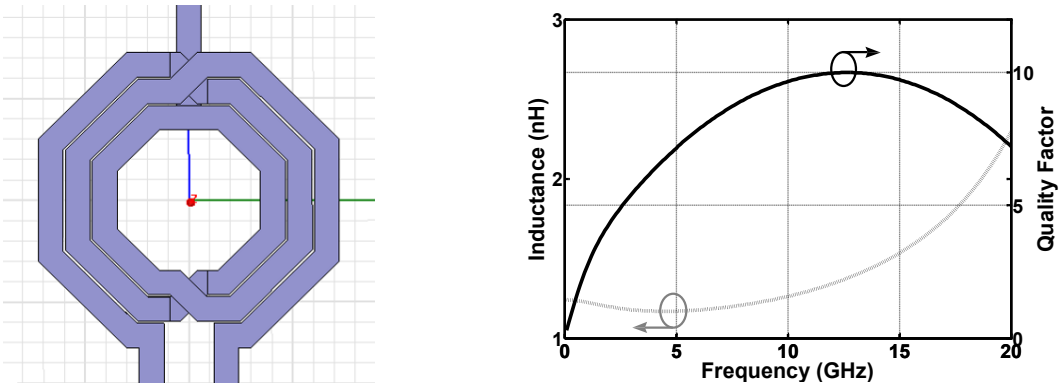


Fig. 4.21 The schematic of fine tune cell

In order to lower the area and the parasitic capacitance of the varactor bank, the whole bank is divided into 3 different weighted sub-banks. As shown in Fig. 4.19, the varactor bank incorporating 7-bits binary-weighted coarse tuning to cover the required tuning range and a 10-bits unity weighted fine tuning to ensure linearity. The layout of the coarse tuning bank is constructed with 128 identical NMOS varactors and each control signal drives different number of the varactors. For instance, $C_{DCO}[17]$ drives a single varactor while $C_{DCO}[18]$ controls a pair of the varactors.

In order to optimize the area usage, the 10-bit fine tuning bank is organized in the matrix of the elementary cells. As shown in Fig. 4.21, each cell includes a local decoder and two varactors with shorted drain and source terminals. The gate terminals of the 1024 cells are shorted together and AC coupled to the tank through a series capacitor C_s, which reduces the equivalent capacitance and enhanced the frequency resolution. Depending on the control



(a) (b)

Fig. 4.22 (a) The layout view and (b) the EM simulation results of the inductor

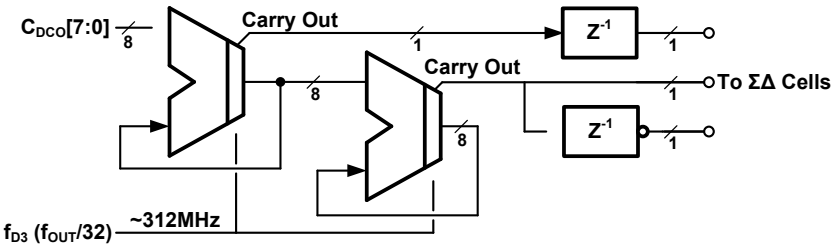


Fig. 4.23 Diagram of the 2nd MASH-II order ΣΔ modulator

signals R, L and C, each cell can be turned either into high capacitance mode or low capacitance mode. The condition for the cell to behaves as a large capacitance is

$$L[\mathrm{i}]+\left(R[\mathrm{i}]\cdot C[\mathrm{j}]\right)=1 \tag{4.22}$$

The binary weighted control code $C_{DCO}[17:8]$ is first converted to thermometer code and then the tuning information R[31:0], L[31:0] and C[31:0] are latched to avoid glitches. The local logic implemented in the cells decode the row and column information in such a way that each odd row is filled up from column 1 to column 32, while each even row is filled up from column 32 back to column 1 of the matrix. The serpentine topology [46] and the dummy cells on the boundary of the matrix ensure good matching between the elements in adjoining rows.

The structure of the ΣΔ modulator is illustrated in Fig. 4.23. It is implemented as digital second-order MASH-type architecture [47] which can be conveniently realized in digital

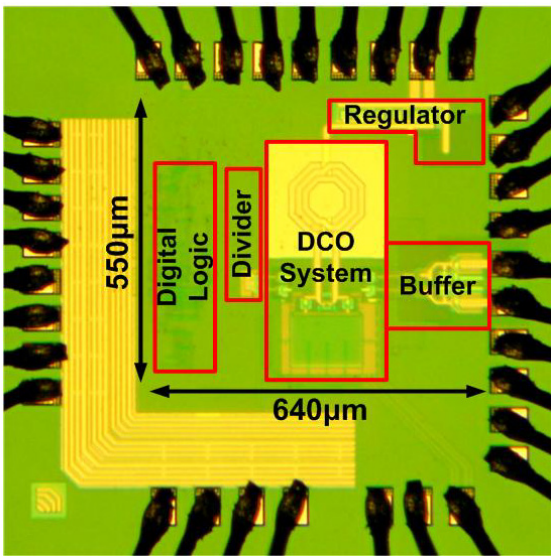


Fig. 4.24 Chip microphotograph of the DCO applied to an ADPLL

domain by cell based design flow. Its output is fed to three ΣΔ cells which have the same structure as the fine tuning cell with R[i] and L[i] tie to 1 and 0, respectively. Table 4.1 reports the tuning characteristics of the DCO.

Due to the lack of the inductor models in the process development kit (PDK) of this 90nm mixed-mode CMOS process, a symmetric inductor coil with center tap is drawn and an EM simulation is taken to extract the characteristic of the inductor. In order to improve the quality factor, the top copper metal layer with 810nm thickness is used to construct the inductor. Also, the inductor layout is covered by some dummy-block layers to prevent automatic metal pattern filling procedure which is now standard in advance sub-micron process. Fig. 4.22 shows the layout view, the inductance and the quality factor of the symmetric inductor. It can be seen from simulation results that the inductor has a quality factor of about 9 around 10 GHz.

4.3.2. Experimental Result

To evaluate the performance of the implemented DCO, the DCO is applied to an ADPLL. The chip microphotograph is shown in Fig. 4.24. The DCO core area occupies about 480μm × 250μm of area and is mounted on a FR-4 PCB to verify. The DCO tuning curves have been characterized in open loop configuration by externally setting a 25 bits digital input code via the multiplexer in front of the DCO. The output frequency measurement is performed by the Agilent E4448A spectrum analyzer with internal frequency counter function. Since measuring the whole tuning curve of the DCO entails the programming of

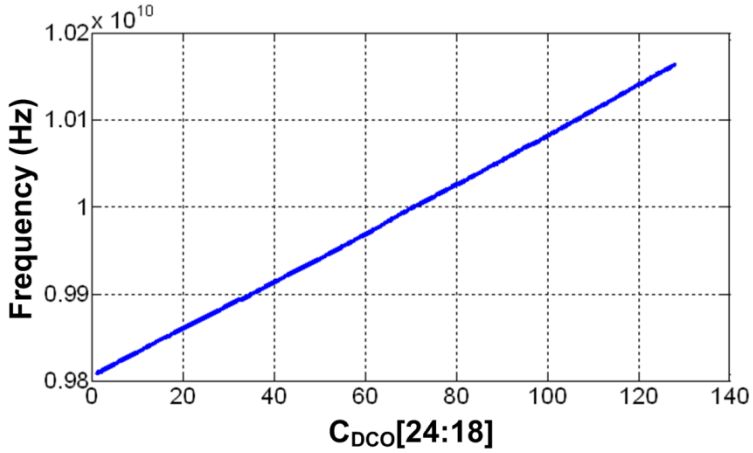


Fig. 4.25 Measured DCO frequency versus control code of coarse tuning bank C_{DCO}[24:18]

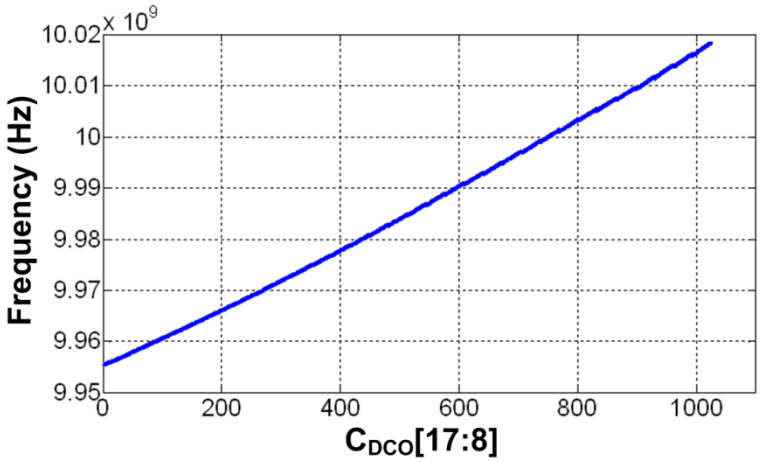


Fig. 4.26 Measured DCO frequency versus control code of fine tuning bank C_{DCO}[17:8]

2^{25}=33554432 different DCO control codes which consumes extremely long time to complete the measurement, the tuning curve of each varactor bank was characterized individually while keeping other control code of other banks unchanged. The measurement process has been automatized using a PC with a GPIB IEEE488.1 interface card and a MATLAB program. The MATLAB routine generates sequentially all the input codes and provides the serial control data to the chip via the parallel port. After each code has been sent, the output frequency of the synthesizer is measured by the Agilent E4448A, and the result is communicated back through the GPIB interface to the PC. The results are automatically stores to the memory of the PC and can be post-processed by MATLAB. Higher accuracy of the measurement is obtained by averaging up to 100 measurement results with the same DCO control code.

Linearity is important to have a value of K_{DCO} which is independent from the operating point of the BBPLL on the tuning curve. Nevertheless, more important is the uniformity of

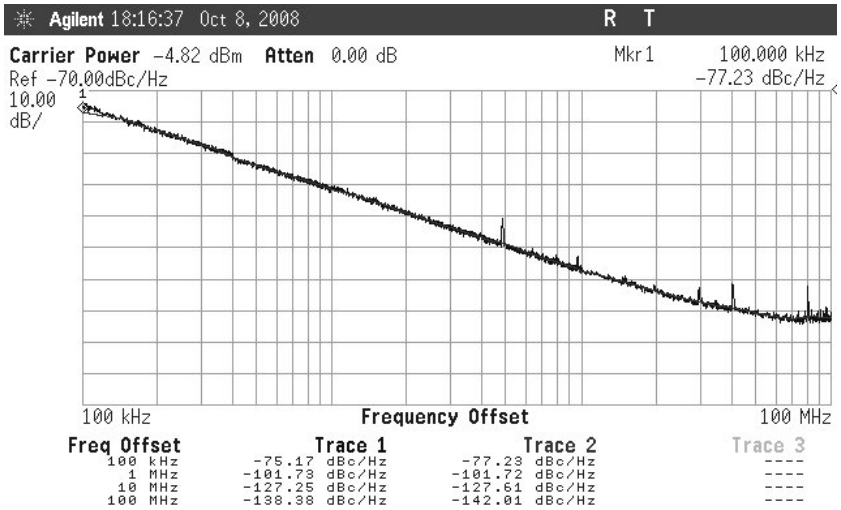


Fig. 4.27 Measure open loop phase noise from 9.98GHz carrier

the minimum frequency step, or, in other terms, the differential nonlinearity (DNL) of the tuning curve. Too large nonlinearity may cause unstable condition in locking process and would worsen the output jitter and spurious tone performance. Under nominal conditions, the maximum (C_{DCO}=33554432) and minimum (C_{DCO}=0) output frequency measured are 10.2GHz and 9.78GHz, respectively. Fig. 4.25 shows the measured tuning characteristics of the DCO versus different control codes of coarse tuning bank C_{DCO}[24:18] while the control code of fine tuning bank C_{DCO}[17:8] and ΣΔ bank C_{DCO}[7:0] are set to 2'b1000000000 and 2'b10000000, respectively. Due to the digital tuning scheme which does not suffer from the highly nonlinear frequency versus voltage characteristics and low voltage headroom, it can be seen that the tuning curves are much more linear than the typical tuning curves of a conventional LC VCO. The measured average frequency step is 2.8MHz per LSB of coarse tuning bank and the DNL is less than 0.42LSB. Fig. 4.26 reports the DCO output frequency with the frequency step as functions of control code of the unity-weighted fine tuning bank C_{DCO}[24:18]. The average frequency step measured is about 75kHz per LSB of fine tuning bank. The frequency resolution is further enhanced to 250 Hz per LSB by employing high speed dithering through an 8-bit ΣΔ second order modulator.

Fig. 4.27 shows the phase noise plot of the free running DCO at 9.98GHz, measured with Agilent E4448A spectrum analyzer with phase noise personality. The measurement results are (-102dBc/Hz at 1MHz offset) agreed with the simulation counterpart where the phase noise at 1MHz offset is about -103 dBc/Hz. Better phase noise value is obtained for higher output frequency where the varactor banks are in low capacitance mode. When the

MOS in the varactor bank enters inversion mode, the energy loss due to the effective resistance of channel and metal connections would increase. Thus, the quality factor of the LC tank reaches its minimum value at high capacitance state when the output frequency is lowest.

4.4. Conclusion

The design considerations of a DCO including quantization and dithering noise are introduced. The proposed linear variable inductor consists of a transformer and a reconfigurable transmission line. By employing the proposed frequency tuning scheme, wide-tuning range as well as multi-band operations are achieved without sacrificing its operating frequency. The 6-bits DCO can operate at 40 GHz with 14% frequency tuning range. It is capable of covering frequency range from 37.6 to 43.4 GHz. The measured phase noise from a 43 GHz carrier is about -109 dBc/Hz at 10-MHz offset, and the output power is -11 dBm. On the other hand, a 10 GHz LC-type DCO achieves a 75 KHz frequency resolution with 10 GHz operating frequency. The frequency resolution is further enhanced to 250 Hz per LSB by employing high speed dithering through an 8-bit MASH-11 ΔΣ modulator. The measured phase noise is -102dBc/Hz at 1MHz offset, while consumes 3.9 mW from a 1V power supply.

Chapter 5

Fast Hopping and Ultra Wide-Band Frequency Synthesizer

This chapter describes a frequency synthesizer utilizing direct frequency synthesis technique to realize a fast hopping performance that closed loop architecture cannot achieve. As discuss in chapter 2, the settling time of closed-loop frequency synthesis is proportional to loop bandwidth. However, the loop bandwidth is limited by reference frequency for stability. In general, the settling time needs to spend at least a hundred reference cycles. Since the reference frequency is restricted by the crystal oscillator, it turns out that the requirement of about few micro-seconds. In contrast to closed loop techniques, direct frequency synthesis only requires few nano-seconds to settle down, which mostly depends on the speed of switches and mixers. In this chapter, a 14 bands CMOS frequency synthesizer with spurs reduction for MB-OFDM UWB system using direct frequency synthesis technique is demonstrated. Based on a single phase locked loop and two-stage frequency mixing architecture, it alleviates harmonics mixing and frequency pulling to diminish spurs generation. Also, only divide-by-2 dividers are needed in the feedback path of the PLL. Thus more precise I/Q sub-harmonics can be derived for the SSB mixer in the 14 bands carrier generation. From experimental results, the image spurs are suppressed below -45dBc and improved by more than 22 dB incorporating with I/Q calibration. Implemented in a 0.18-μm CMOS technology, this chip drains 65 mA from a single 1.8 V supply. The chip size is 2.5 by 2.2 mm^2 providing 14 bands I/Q phases.

This chapter is organized as follows. Section 5.1 introduces the background of the proposed frequency synthesizer. Section 5.2 describes the proposed frequency synthesizer architecture, and investigates the spur issues encountered in the full-band frequency synthesis through SSB harmonic mixing. To alleviate the spurious tones, I/Q calibration algorithm applied in carrier generation will be described. Section 5.3 presents the detailed circuit blocks, including the main phase locked loop design, single side band mixer, multiplexer, and I/Q calibrated buffer stages. The experimental results are shown in section 5.4. Finally, conclusion is drawn in section 5.5.

5.1. Introduction

The Federal Communication Commission (FCC) regulations released in 2002 establish that UWB (bandwidth at least 500 MHz or at least 0.2 fractional bandwidth) devices for communication can operate in the unlicensed spectrum of 3.1-10.6 GHz while employing about 500 MHz of bandwidth. At PHY level, the output power density must not exceed the specified -41.25 dBm/MHz, which is corresponding to an average effective isotropic radiated power (EIRP) of 0.56 mW. It opens an opportunity to develop a short range high data rate communications for wireless personal area network (WPAN), or for wireless USB. An approach to UWB is to divide the entire frequency band from 3.1 to 10.6 GHz into several sub-bands for a multiband band system. As proposed by MB-OFDM (multi-band orthogonal frequency division multiplexing) alliance, the spectrum for UWB communication system ranges from 3.1-10.6 GHz, which is divided into 14 bands with each band of 528 MHz and categorized into 5 groups [1]. According to IEEE 802.15.3a recommendation, the frequency hopping time for band switching should be less than 9.5 ns. It provides 480 Mbps for WPAN application. Recently, many research works on RF front-end for MB-OFDM UWB systems have been reported [2][3]. To meet the stringent frequency hopping time requirement, several frequency synthesizers based on single-side band (SSB) frequency mixing were proposed recently [4]-[15]. Nevertheless, these architectures demand multiple phase locked loops [4]-[8] or sophisticated dividers [4][9][10] to provide adequate sub-harmonics for the full band frequency synthesis. For 14 bands carrier generation, the prior arts in the literatures require 3 stages cascaded SSB mixers in the signal chain [4][12], or employ an external VCO instead of an integrated PLL [12]. As a consequence, they are susceptible to in-band spurs generation, harmonic pulling, and encounter difficulties in I/Q carrier generation.

In contrast to the prior arts, this chapter proposes a 14 bands, I/Q phases, CMOS frequency synthesizer based on single phase-locked loop architecture [16]. The proposed architecture extends the previous work in [13] to 14 band frequency generation. Moreover, in order to overcome the spurious tones in the prior art [11][13][15], the spur generations are studied extensively and image suppression adopting I/Q calibration algorithm and on-chip digitally controlled vector buffer is proposed. By adopting the proposed technique, the SFDR is improved by 13 dB, and the spurious tones is reduced by more than 10 dB compared to the prior art [11][13][15]. With adequate frequency planning, only divide-by 2 dividers are needed in the feedback path of the PLL. Thus, more precisely in phase and quadrature phase (I/Q) sub-harmonics can be derived from the divider chain by nature for SSB frequency

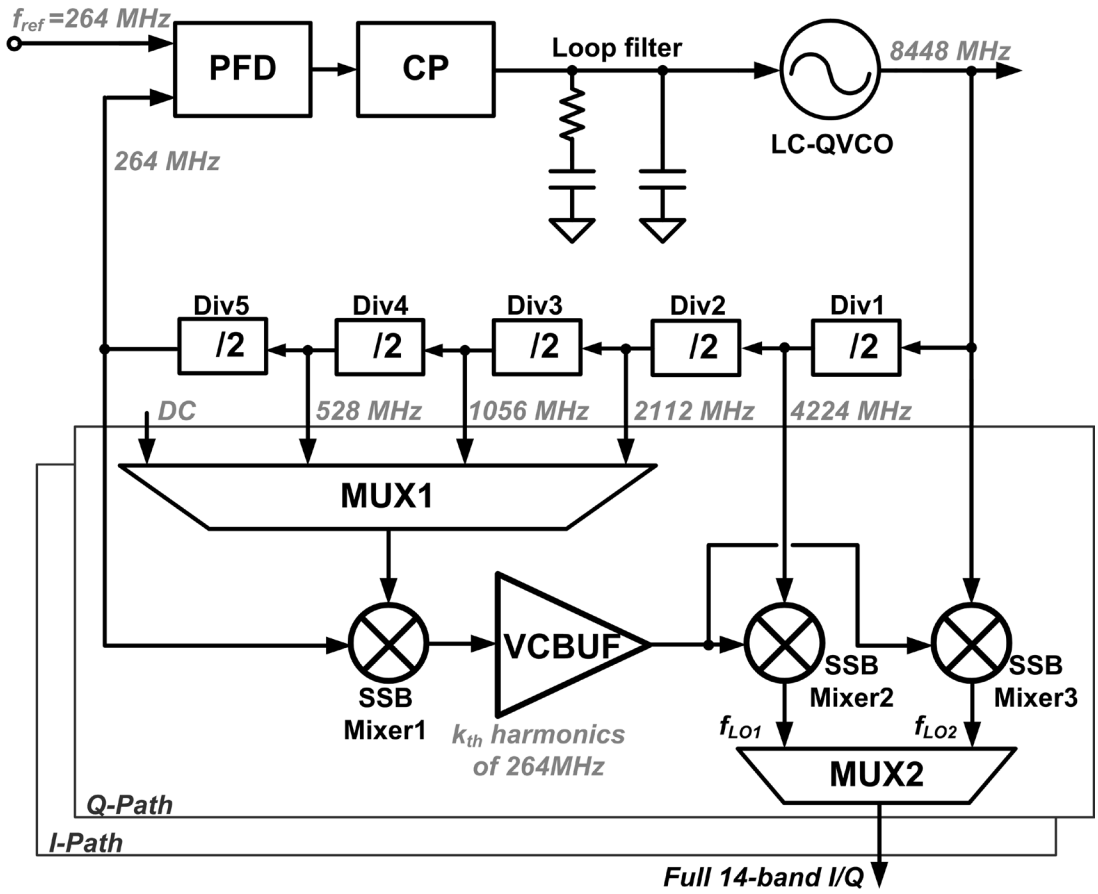


Fig. 5.1 The 14 bands frequency synthesizer architecture for MB-OFDM transceiver

mixing. On the other hand, the number of mixer stage in cascade is reduced to 2 for full-band carrier generation. With the aid of sub-harmonic I/Q calibration, the image spurs are suppressed below –45 dBc, and more than 33 dB spurious free dynamic range is achieved for the full band carrier generation.

5.2. Architecture

The frequency planning of direct frequency synthesis has to take practical non-idealities into consideration. The non-idealities such as harmonic mixing and pulling will induce unwanted harmonic spurs and degrades the SNR of receiver. Fig. 5.1 shows the proposed 14 bands frequency synthesizer architecture, which is composed of only one PLL, two stage SSB mixers (3 pairs for I/Q operations), and two stage multiplexers. The PLL is operated at 8448 MHz, providing I/Q phases from a LC-QVCO, and phase-locking to an external 264 MHz reference. The frequency planning for the 14-band carrier generation is shown in Fig.

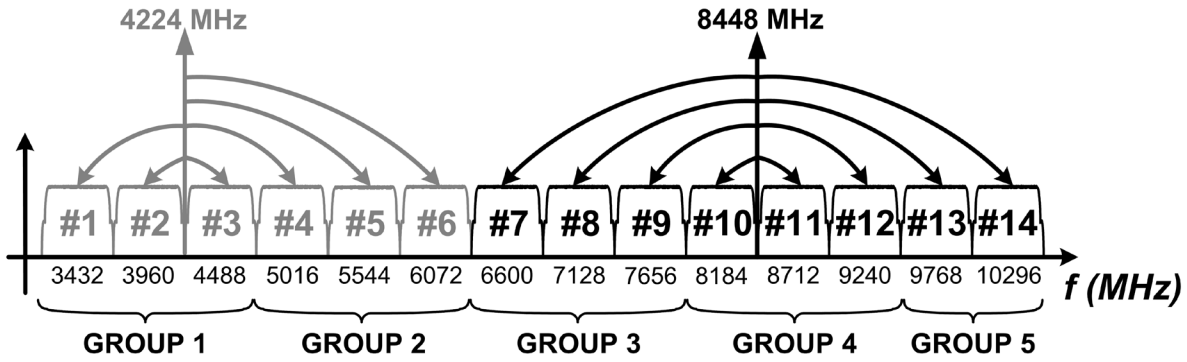


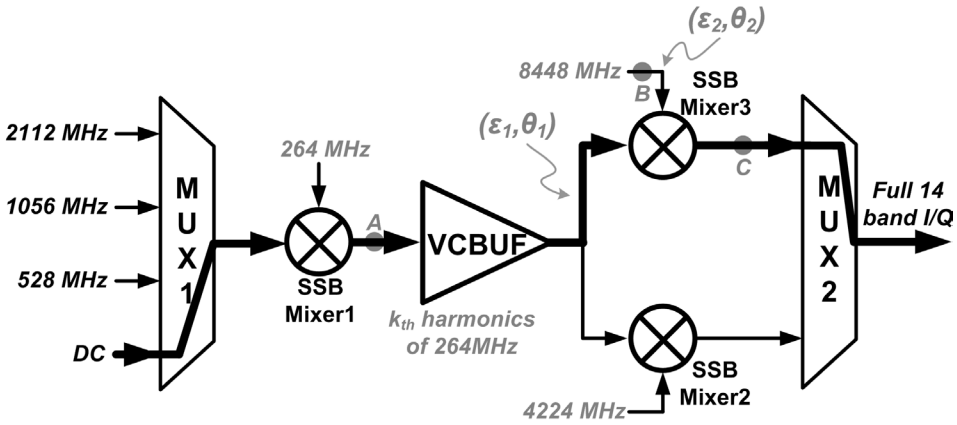
Fig. 5.2 Frequency planning for 14 bands carrier generation

5.2, which is categorized into two folds

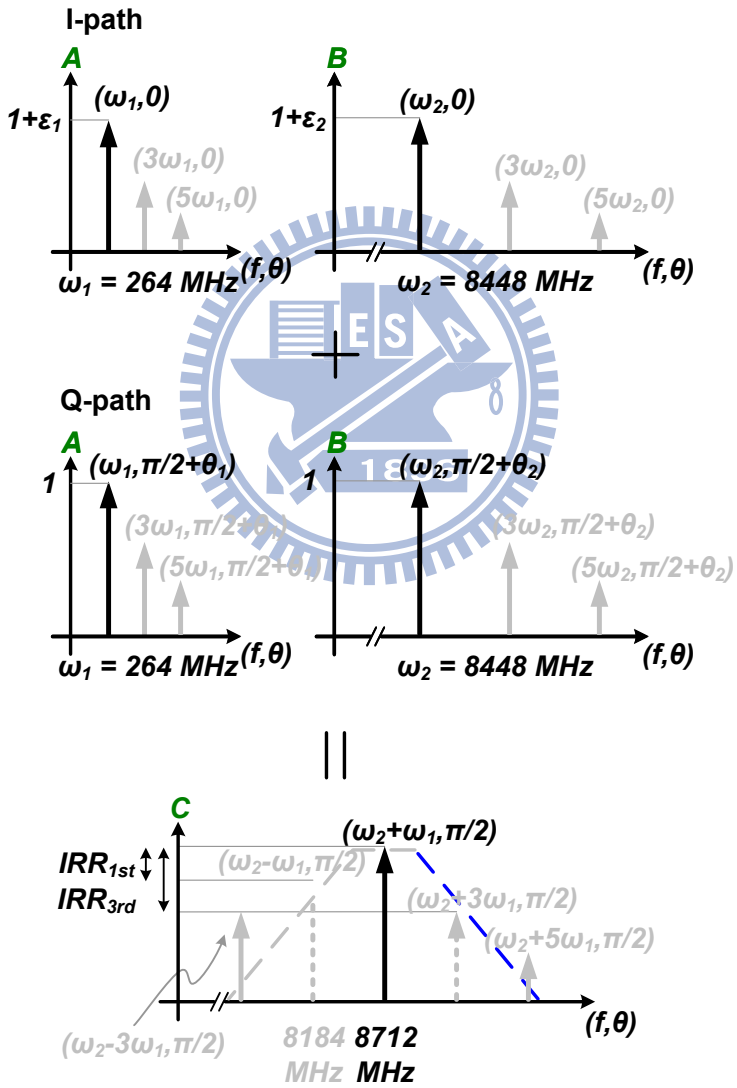
$$
\begin{aligned}
&f_{LO1} = 264 \times (16 \pm k) = 4224 \pm 264k \\
&f_{LO2} = 264 \times (32 \pm k) = 8448 \pm 264k \\
&k \in \{1,3,5,7\}
\end{aligned}
\tag{5.1}
$$

Here f_{LO1} generated by SSB Mixer2 covers the carrier generation for band 1 to 6, and f_{LO2} generated by SSB Mixer3 covers band 7 to 14. As the divider chain in the feedback path is composed of 5 stages divide-by-2 dividers, the 4224 MHz I/Q carrier is available at the output of the first stage divider, while the even order harmonics (8^{th}, 4^{th}, and 2^{nd}) of 264 MHz can be derived from the 2^{nd} to the 4^{th} stage dividers. The odd order harmonics (3^{rd}, 5^{th}, and 7^{th}) of 264 MHz are then indirectly synthesized from the reference frequency (264 MHz) and its even order harmonics, which are performed by SSB Mixer1 and MUX1. In order to achieve broad band operations while relaxing the complexity of signal routings, the full 14 bands, f_{LO1} (Group 1, 2) and f_{LO2} (Group 3, 4 ,5), are then derived by mixing the odd order harmonics of 264 MHz (1^{st}, 3^{rd}, 5^{th}, and 7^{th}) with 4224 MHz and 8448 MHz respectively. They are performed separately by the 2^{nd} stage SSB mixers, where SSB Mixer2 is employed for f_{LO1} and SSB Mixer3 for f_{LO2} generations. The inactive 2^{nd} stage SSB mixer will be shut down to save power and provide better side band isolation. Finally, the output carrier is picked up by MUX2 and delivered into the output buffer.

5.2.1. Spur Issue



(a)



(b)

Fig. 5.3 (a) Signal path for band 11 generation and (b) Signal spectrum at point A, B and C

In order to investigate the spur issues along with harmonic mixing, the signal path of the frequency synthesizer is recapitulated as shown in Fig. 5.3(a). The spurs generations mainly stem from two reasons, the mixer nonlinearity and I/Q imbalances of the sub-harmonics that drive the SSB mixers. The former one results in harmonic spurs, while the later one induces image spurs.

The SSB mixer is composed of two double side band mixers to cancel either the upper or lower sideband signal. Let the input frequencies of the SSB mixer be ω_1 and ω_2, by taking the mixer nonlinearity into account, its output can be derived as

$$
\begin{aligned}
V_{SSB\_Mixer} &= V_{DSB\_Mixer1} - V_{DSB\_Mixer2} \\
&= \left[\begin{array}{l} \frac{8}{\pi} X_1 \cos\omega_1 t \left(\cos\omega_2 t - \frac{1}{3}\cos 3\omega_2 t + \frac{1}{5}\cos 5\omega_2 t + \ldots \right) \\ + \frac{8}{\pi} X_3 \cos 3\omega_1 t \left(\cos\omega_2 t - \frac{1}{3}\cos 3\omega_2 t + \frac{1}{5}\cos 5\omega_2 t + \ldots \right) \\ + \ldots \end{array} \right] \\
&\quad - \left[\begin{array}{l} \frac{8}{\pi} X_1 \sin\omega_1 t \left(\sin\omega_2 t - \frac{1}{3}\sin 3\omega_2 t + \frac{1}{5}\sin 5\omega_2 t + \ldots \right) \\ - \frac{8}{\pi} X_3 \sin 3\omega_1 t \left(\sin\omega_2 t - \frac{1}{3}\sin 3\omega_2 t + \frac{1}{5}\sin 5\omega_2 t + \ldots \right) \\ + \ldots \end{array} \right] \\
&= \frac{8}{\pi}\left[X_1 \cos(\omega_2 + \omega_1)t + X_3 \cos\left[(\omega_2 - 3\omega_1)t\right] + X_5 \cos\left[(\omega_2 + 5\omega_1)t\right] + \ldots \right] \\
&\quad - \frac{8}{3\pi}\left[X_1 \cos(3\omega_2 - \omega_1)t + X_3 \cos\left[(3\omega_2 + 3\omega_1)t\right] + X_5 \cos\left[(3\omega_2 - 5\omega_1)t\right] + \ldots \right] \\
&\quad + \ldots
\end{aligned}
\tag{5.2}
$$

where X_1, X_3 and X_5 respectively denote the 1st, 3rd and 5th order harmonic coefficients of the SSB mixer. It can be seen that the desired tone at $(\omega_1+\omega_2)$ is accompanied by many other spurious tones caused by mixer nonlinearity. However, if I/Q mismatch occurs for the input signal, the SSB mixer output will become [17]

$$
\begin{aligned}
V_{SSB\_Mixer} &= A\cos(\omega_1 t+\theta_1)\cos(\omega_2 t+\theta_2)-A(1+\varepsilon_1)(1+\varepsilon_2)\sin\omega_1 t\sin\omega_2 t \\
&= \frac{A}{2}\left[\cos(\omega_1 t+\omega_2 t+\theta_1+\theta_2)+\cos(\omega_1 t-\omega_2 t+\theta_1-\theta_2)\right] \\
&+ \frac{A}{2}(1+\varepsilon_1)(1+\varepsilon_2)\left[\cos(\omega_1 t+\omega_2 t)-\cos(\omega_1 t-\omega_2 t)\right] \\
&= \frac{A}{2}\left[\cos(\theta_1+\theta_2)+(1+\varepsilon_1+\varepsilon_2+\varepsilon_1\varepsilon_2)\right]\cos(\omega_1+\omega_2)t+\frac{A}{2}\left[-\sin(\theta_1+\theta_2)\right]\sin(\omega_1+\omega_2)t \\
&+ \frac{A}{2}\left[\cos(\theta_1-\theta_2)-(1+\varepsilon_1+\varepsilon_2+\varepsilon_1\varepsilon_2)\right]\cos(\omega_1-\omega_2)t+\frac{A}{2}\left[-\sin(\theta_1-\theta_2)\right]\sin(\omega_1-\omega_2)t
\end{aligned}
\tag{5.3}
$$

where ε_1, ε_2 and θ_1, θ_2 represent the amplitude and phase error of I/Q signals in ω_1 and ω_2 respectively. It turns out that image spurs at $(\omega_2-\omega_1)$ will appear, which is even closer to the desired tone.

The spectrum of the output signals at node A, B, and C are illustrated in Fig. 5.3(b), the spurs caused by nonlinear effect are shown as the grey solid arrows, and the others are side band images due to I/Q gain and phase imbalance, which are shown as the gray dot arrows. The IRR_{1st} and IRR_{3rd} are the image rejection ratio respectively caused by 1st and 3rd order harmonics under I/Q amplitude and phase imbalance.

The worst case image spur occurs in generating the carrier frequency of 8712 MHz (band 11), and the signal path is highlighted as shown in Fig. 5.3(a). In this case, MUX1 passes DC voltage to drive SSB Mixer1, whose outputs are at harmonics of 264 MHz due to mixer nonlinearity. SSB Mixer3 is activated with output frequency centered at 8448 MHz. Meanwhile, the image spur caused by I/Q imbalance is located at 8184 MHz, which is 528 MHz away from the desired tone at 8712 MHz. To sufficiently suppress the image spur, a band pass filter with quality factor higher than 16 is demanded at the mixer output, which is difficult to be realized at such a high frequency with rapid switching speed. In this work, this issue is overcome by sub-harmonics I/Q calibration.

The image rejection ratio of a single side band mixer due to 1st harmonic (IRR_{1st}) can be derived in terms of its I/Q imbalance caused by gain error and phase error according to (5.3), where

$$
IRR_{1st} = 10\log\left(\frac{1+(1+\varepsilon_1+\varepsilon_2+\varepsilon_1\varepsilon_2)^2+2(1+\varepsilon_1+\varepsilon_2+\varepsilon_1\varepsilon_2)\cos(\theta_1+\theta_2)}{1+(1+\varepsilon_1+\varepsilon_2+\varepsilon_1\varepsilon_2)^2-2(1+\varepsilon_1+\varepsilon_2+\varepsilon_1\varepsilon_2)\cos(\theta_1-\theta_2)}\right) \tag{5.4}
$$

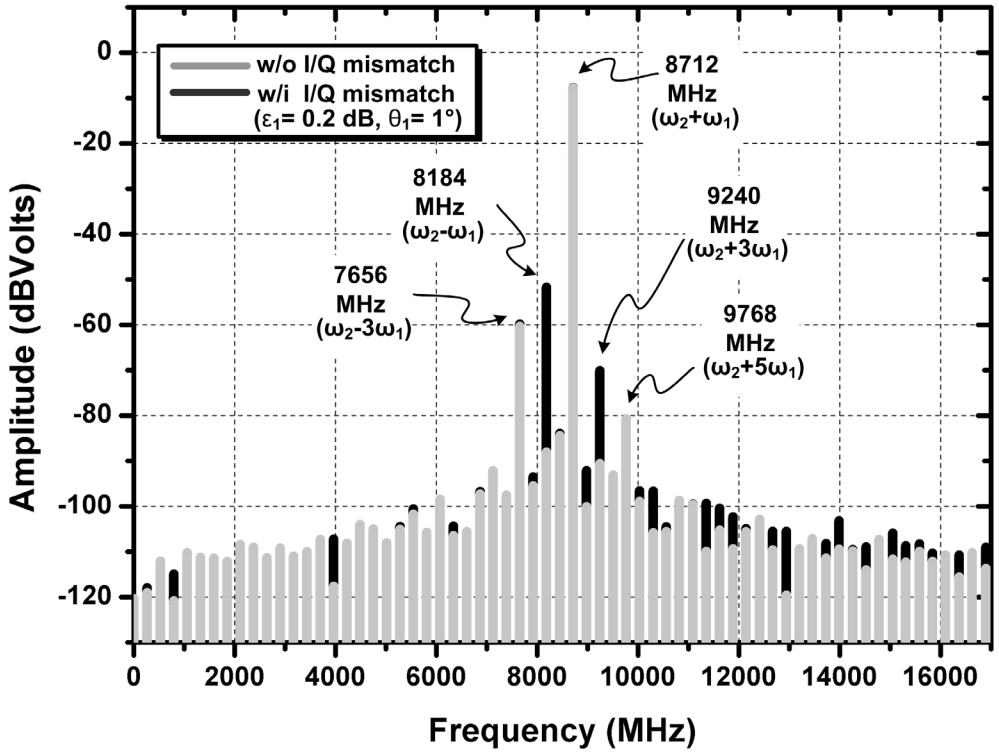


Fig. 5.4 The simulated output spectrum of second stage SSB mixers with and without I/Q imbalance

On the other hand, the IRR_{3rd} can be derived from IRR_{1st}, the fundamental (X_1) and third harmonics (X_3) of the SSB mixer, where

$$IRR_{3rd} = IRR_{1st} - 20\log(\frac{X_1}{X_3}) \tag{5.5}$$

As the I/Q signals of ω_1 is indirectly synthesized by the 1st stage mixer, their gain and phase imbalance ε_1 and θ_1 would dominate the IRR performance compared to ε_2 and θ_2 in ω_2, which is generated by divide-by-2 dividers. For IRR higher than 40 dBc, the gain error should be less than 0.1 dB and the phase error should be less than 1 degree, which are demanding for the full-band sub harmonics generations. Fig. 5.4 shows the simulated output spectrum at the 2nd stage SSB mixer output with (dark line) and without (gray line) I/Q imbalance. For a desired tone at $(\omega_2+\omega_1)$, it reveals that the image at $(\omega_2-\omega_1)$ can be significantly suppressed by improving I/Q matching. However, this situation will be inverted for the third harmonics, where $(\omega_2+3\omega_1)$ can be suppressed by improving I/Q balance.

Contrarily, the harmonics at $(\omega_2 - 3\omega_1)$ will leak to the output, which should be suppressed by improving the linearity of mixer itself.

5.2.2. I/Q Calibration Algorithm

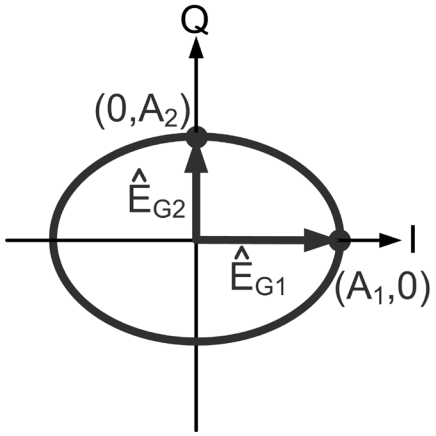
For frequency synthesis utilizing SSB mixer, I/Q vectors of the sub harmonics in the first stage SSB travel through different traces and inevitably suffer from gain and phase mismatches. It leads to spur generation at the mixer output. To effectively suppress the image spurs, I/Q calibration algorithm is needed to get rid of gain and phase error.

Typically, I/Q corrections in wireless receiver can be classified into three folds. The first type detects and corrects I/Q imbalances all in the digital base band [18]-[20]. The second type detects I/Q imperfection in the digital base band, while corrects it in the RF/analog front-end [21]-[23]. The third type accomplishes I/Q calibrations in the analog domain [24]-[28] with auxiliary circuits like tunable RC networks or DLL. In this design, I/Q calibration algorithm [29] is implemented with digital tuning capability using phase interpolator. It only requires additional power detector and comparator operated at low frequency without complicated digital circuitries to save power.

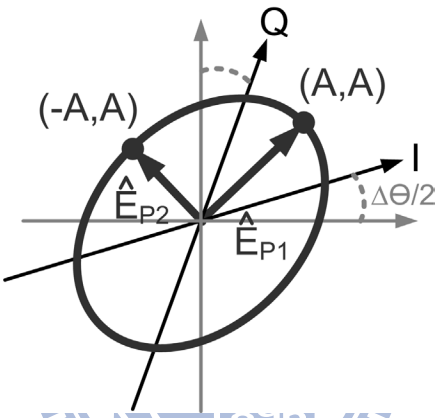
Let the I/Q vectors with gain imbalance be represented as $\hat{E}_{G1}(A_1,0)$ and $\hat{E}_{G2}(0,A_2)$, the amplitude and gain error are denoted as A and ΔA, we have

$$\begin{aligned} \left|\hat{E}_{G1}\right| &= A\times\left(1+\frac{\Delta A}{2}\right) \\ \left|\hat{E}_{G2}\right| &= A\times\left(1-\frac{\Delta A}{2}\right) \end{aligned} \tag{5.6}$$

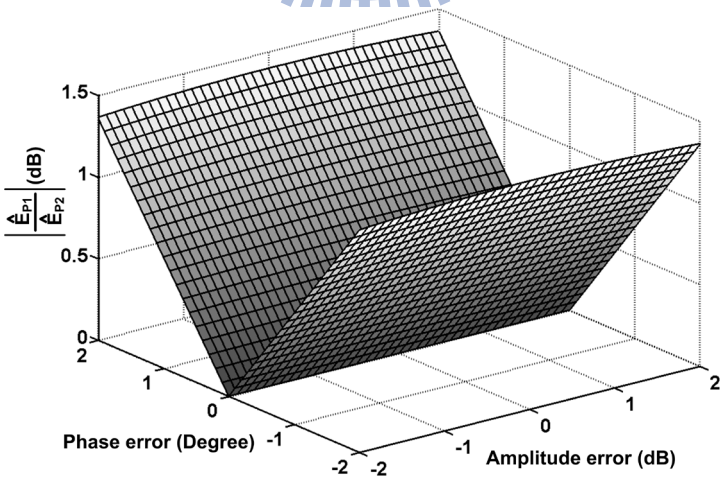
Under this circumstance, the I/Q trace diagram would become elliptic, as is shown in Fig. 5.5(a). To monitor $\hat{E}_{G1}$ and $\hat{E}_{G2}$, test vectors (1,0) and (0,1) are applied at the input of the 2nd stage SSB mixer (SSB Mixer2 and SSB Mixer3), as is shown in Fig. 5.6. The gain error is extracted through power detector and comparator, whose output adjust the weighting factors of a vector calibrated buffer (VCBUF), so as to diminish ΔA.



(a)



(b)



(c)

Fig. 5.5 The trace diagram under (a) gain mismatch, (b) phase mismatch and (c) ratio of output vectors with phase and amplitude error during phase calibration

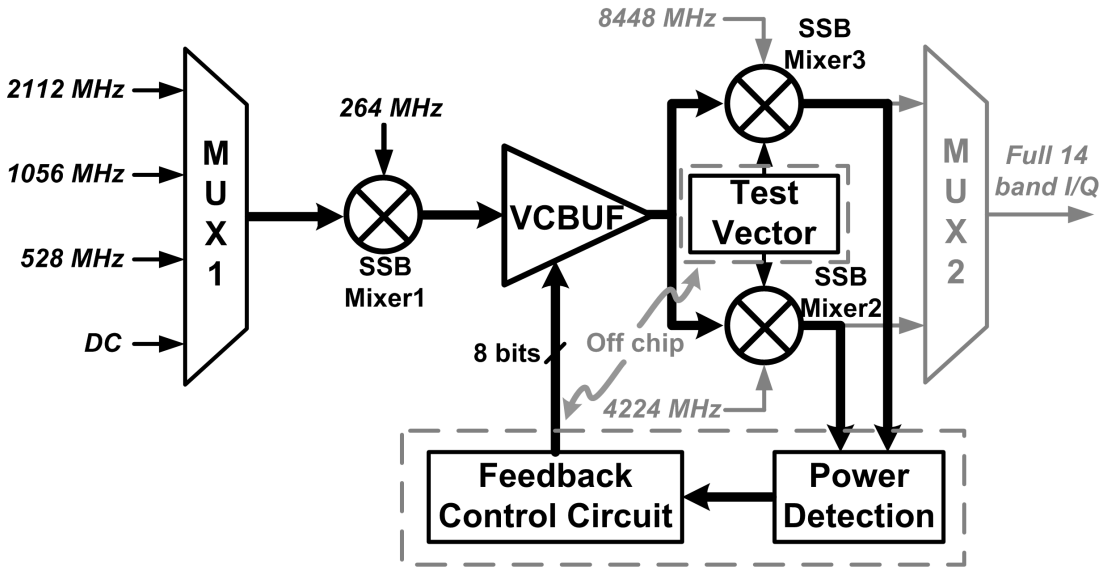
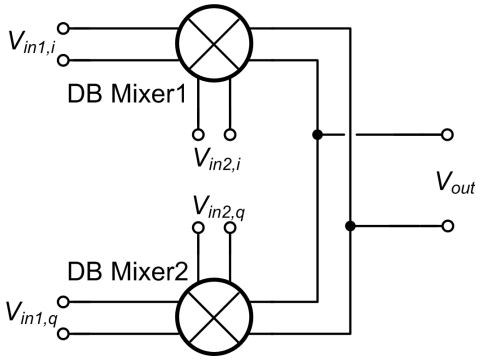


Fig. 5.6 The I/Q calibration architecture

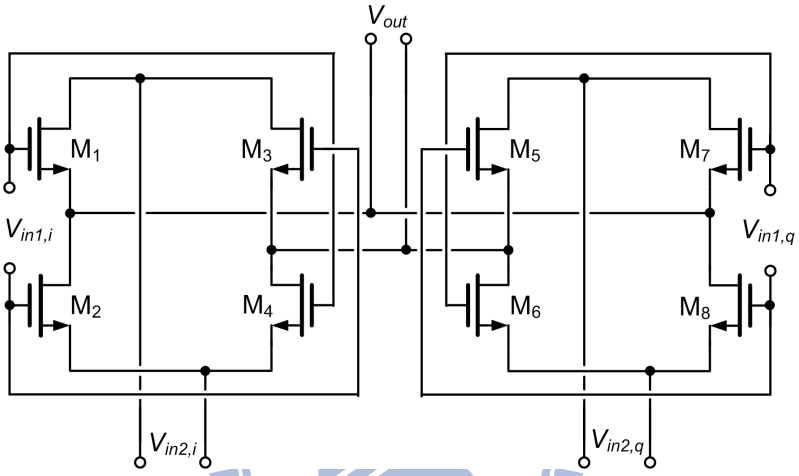
On the other hand, for I/Q vectors with phase error ($\Delta\theta$), the trace diagram would become inclined elliptic shape with tilting angle ($\Delta\theta$), as shown in Fig. 5.5(b). Let $\hat{E}_{P1}$ and $\hat{E}_{P2}$ respectively represent vectors (A, A) and (A, -A), we have

$$\begin{aligned} \left|\hat{E}_{P1}\right| &= \sqrt{2\left(1+\sin\Delta\theta\right)}A \\ \left|\hat{E}_{P2}\right| &= \sqrt{2\left(1-\sin\Delta\theta\right)}A \end{aligned} \tag{5.7}$$

For phase error calibration, test vectors (1,1) and (-1, 1) are applied at the input of the 2nd stage SSB mixer, whose output are then captured by power detector and compensated by the VCBUF as well, as illustrated in Fig. 5.6. By forcing $\left|\hat{\hat{E}}_{P1}\right| = \left|E_{P2}\right|$, it turns out that $\Delta\theta = 0$. If a small gain error still exists after gain calibration, the output vectors $\left|\hat{E}_{P1}\right|$ and $\left|\hat{E}_{P2}\right|$ can be derived as



(a)



(b)

Fig. 5.7 (a) The SSB mixer architecture and (b) the 1st stage SSB mixer

$$\left|\hat{E}_{P1}\right| = \sqrt{2\left[\left(1+\frac{\Delta A^2}{4}\right)+\left(1-\frac{\Delta A^2}{4}\right)\sin\Delta\theta\right]}A$$
$$\left|\hat{E}_{P2}\right| = \sqrt{2\left[\left(1+\frac{\Delta A^2}{4}\right)-\left(1-\frac{\Delta A^2}{4}\right)\sin\Delta\theta\right]}A \quad (5.8)$$

It can be shown that (5.8) becomes (5.7) if ΔA^2 is negligible. Fig. 5.5(c) illustrates the convergent analysis for gain and phase calibration. With a gain error distribution form 0 to 2 dB, the phase error can be diminished to zero by equalizing $\left|\hat{E}_{P1}\right|$ and $\left|\hat{E}_{P2}\right|$.

The phase calibration is preceded by gain calibration, and this procedure is exercised alternatively to equalize the amplitudes of the testing vectors, so as to diminish the gain and phase error. In this design, the gain and phase tuning are 4 bits digitally controlled to fulfill

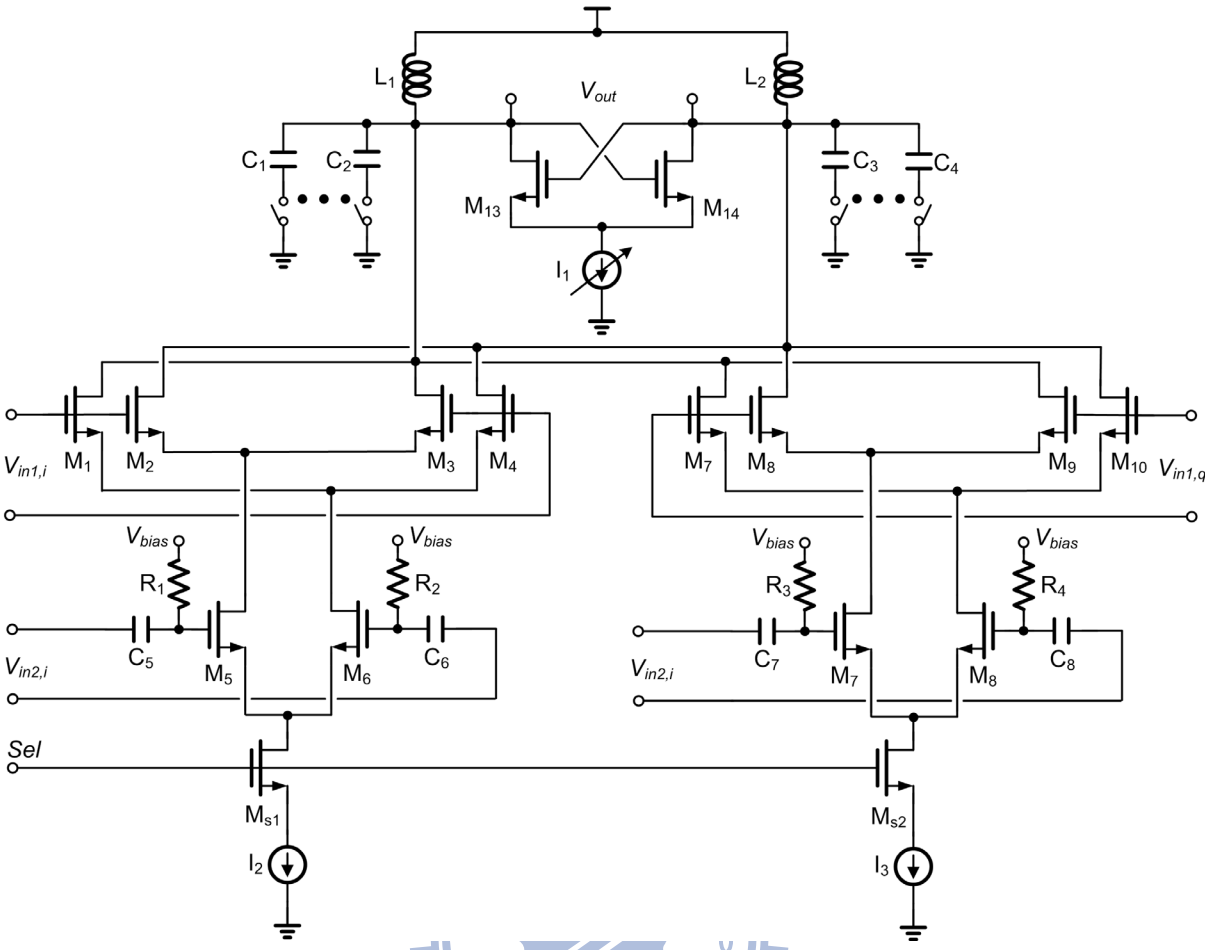


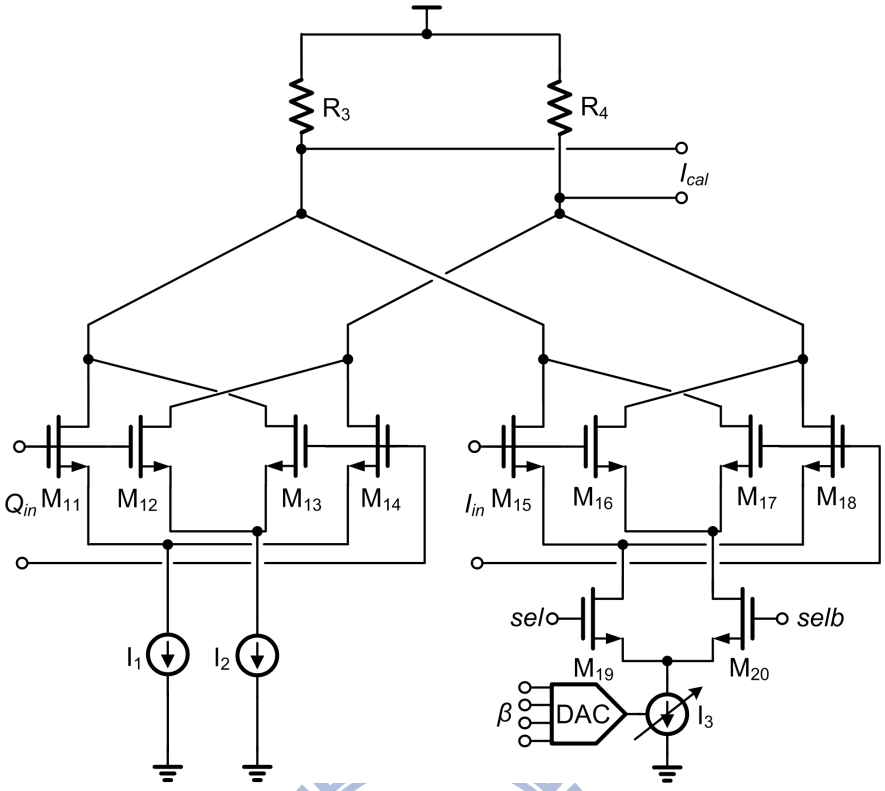
Fig. 5.8 The 2nd stage SSB mixer

the accuracy for side band rejection (> 40 dB).

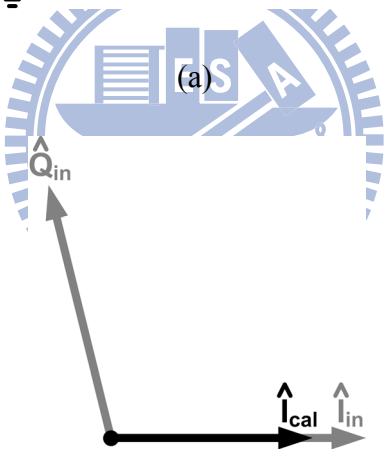
5.3. Circuit Implementation

This section illustrates circuit design of the building blocks in Fig. 5.1 including SSB mixers, VCBUF, multiplexers and PLL. The two stage SSB mixers are design based on different topology due to its input power level and required linearity. The VCBUF are composed of gain-calibrated and phase-calibrated buffers which have similar frequency response over wide frequency range. To speed up the switching time, current steering technique is adopted. An active shunt-shunt feedback is employed to achieve broadband operation. Finally, a second order charge-pump PLL operating in 8.448 GHz is demonstrated.

Fig. 5.7 (a) illustrates the architecture of the 1st stage SSB mixer, and its core cell is shown in Fig. 5.7 (b). As the voltage swing at the divider output is as high as 300 mV_{pp}, passive mixer is adopted for the 1st stage SSB mixer (SSB Mixer1) to mitigate linearity and



(a)

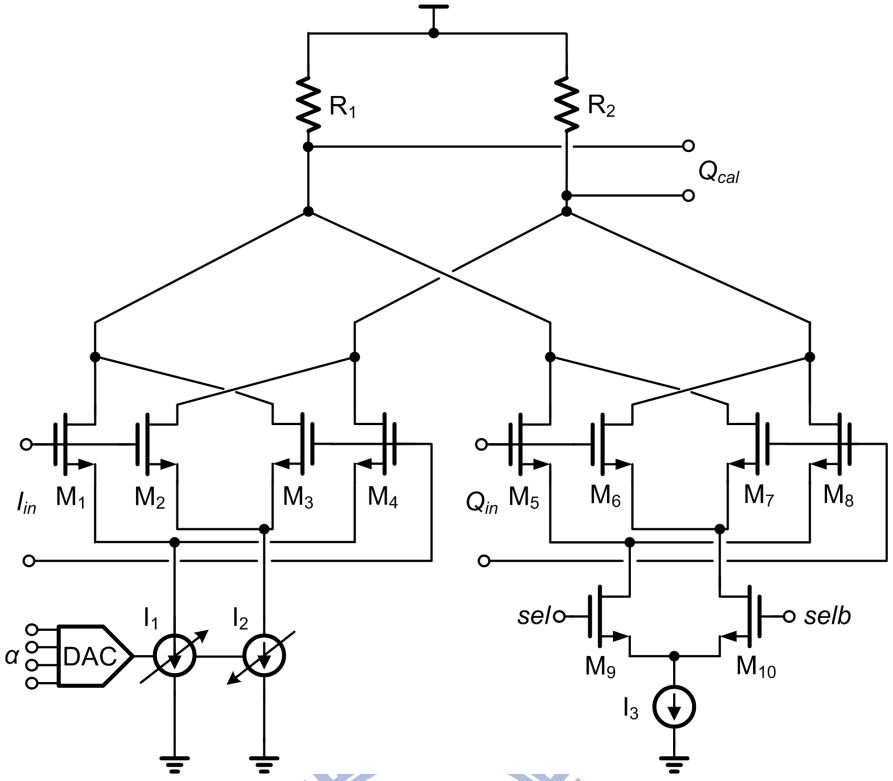


(b)

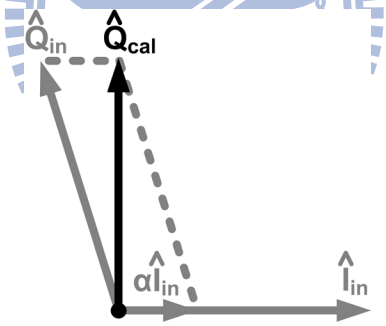
Fig. 5.9 (a) Gain calibration buffer (b) I vector after gain calibration

noise issues while reducing power consumption. According to simulation result, the input 1-dB compression point of the mixer is approximately 0 dBm, and the conversion gain is -5 dB.

On the other hand, to suppress harmonic tones and compensate gain loss of the preceding stage, the 2nd stage SSB mixers (SSB Mixer2 and SSB Mixer3) are composed of Gilbert-type mixers (M_1-M_6, M_7-M_{12}, M_{s1}-M_{s4}) with tunable resonator as output load, as is shown in Fig. 5.8. The center frequency of the resonator is adjusted by tuning a capacitor



(a)

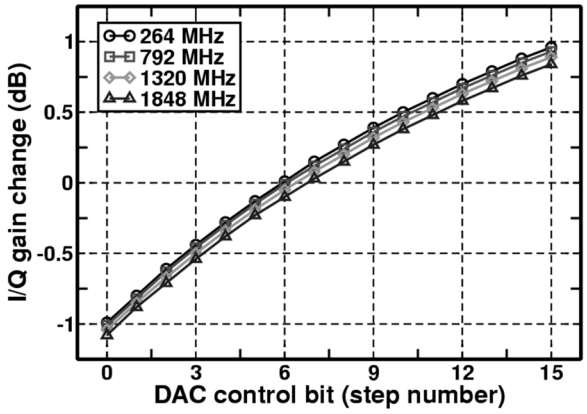


(b)

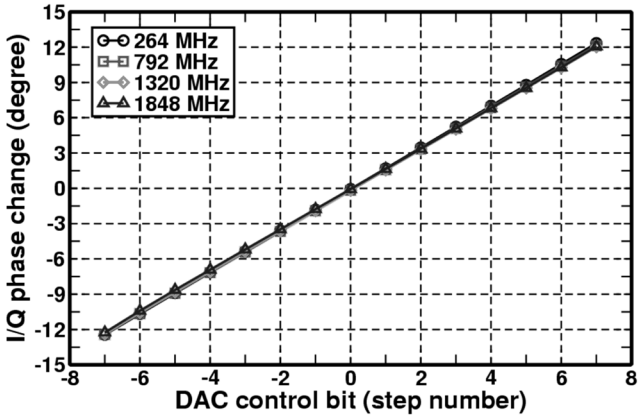
Fig. 5.10 (a) Phase calibration buffer (b) Q vector after phase calibration

bank (C_1-C_4) along with the band switching of the frequency synthesizer. Also, the quality factor of the resonator is enhanced by a negative impedance converter (M_{13} and M_{14}), which is controlled along with band switches to compensate LC-tank Q variations.

The I/Q vectors of the odd harmonics of 264 MHz travel through different traces and inevitably suffer from gain and phase mismatches when they reach the 2nd stage SSB mixers. To alleviate the image spurs caused by I/Q imbalance, a vector calibrated buffer (VCBUF) incorporating current DAC is inserted between the two stage mixers to compensate the gain



(a)



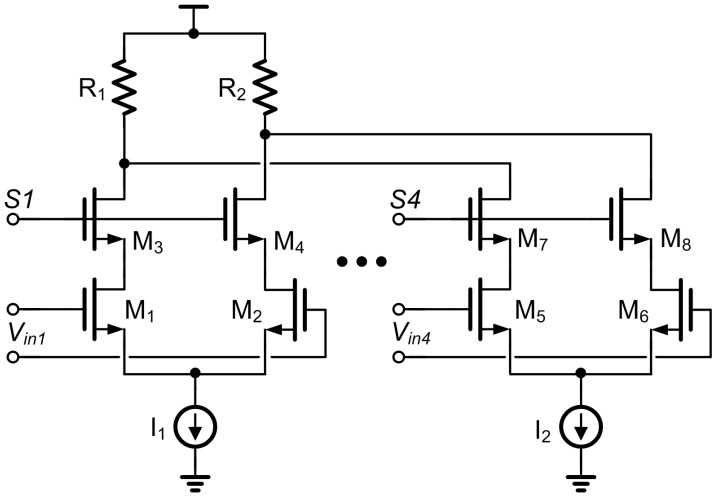
(b)

Fig. 5.11 (a) Gain and (b) phase simulation results of VCBUF

and phase error, as is shown in Fig. 5.1.

Fig. 5.9 and Fig. 5.10 illustrate the circuit schematic and vector diagram for gain and phase calibration respectively. The two circuitries are identical and have similar frequency response over a wide frequency range. Both the I/Q vectors after calibration ($\hat{I}_{cal}, \hat{Q}_{cal}$) is indirectly synthesized by phase interpolations. We have

$$\begin{aligned} \hat{\hat{Q}}_{cal} &= Q_{in} + \alpha \times \hat{I}_{in} \\ \hat{\hat{I}}_{cal} &= 0 \times \hat{Q}_{in} + \beta \times I_{in} \end{aligned} \tag{5.9}$$



(a)

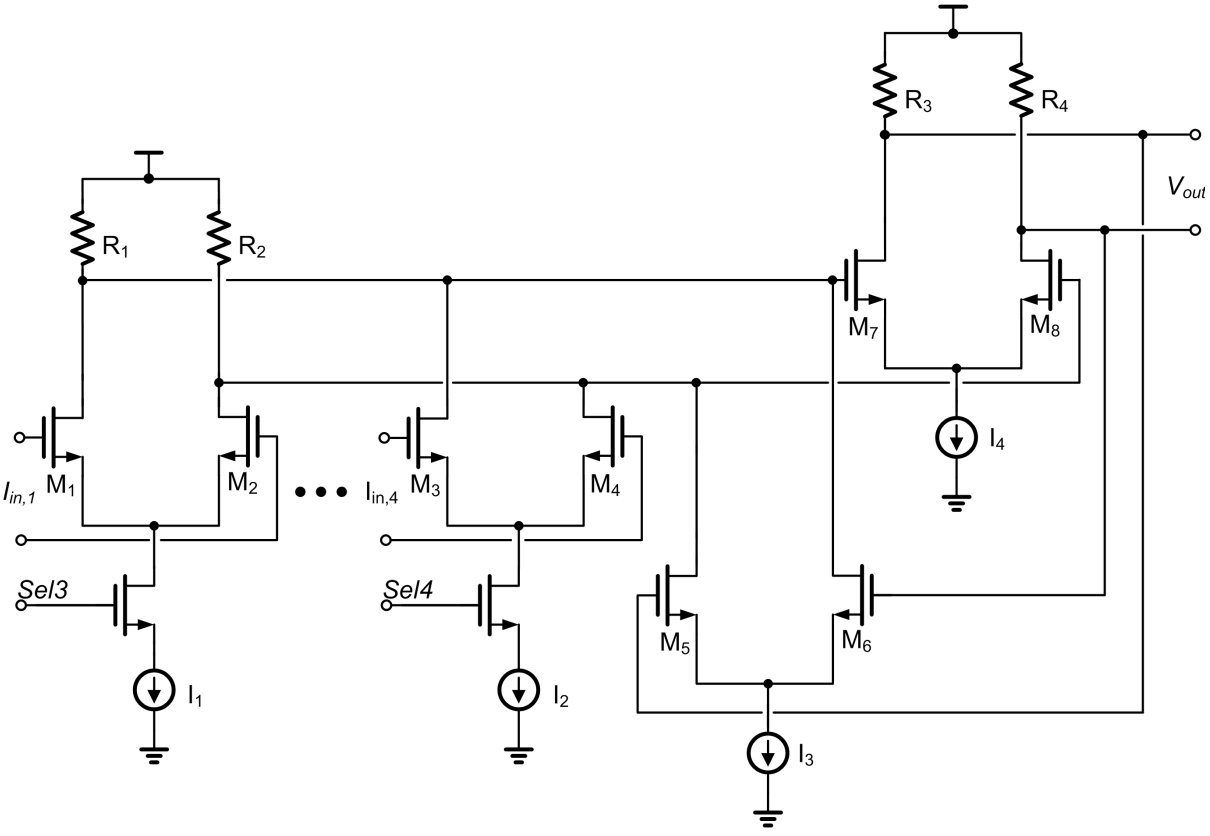


Fig. 5.12 (a) MUX1 and (b) MUX2 circuit schematic

Here the weighting factors α and β are utilized for phase and gain calibration respectively, which are adjusted by 4 bits current DACs with about 100μA per step and can be calibrated and stored separately for each channel. Fig. 5.11 shows the simulation results of VCBUF. The

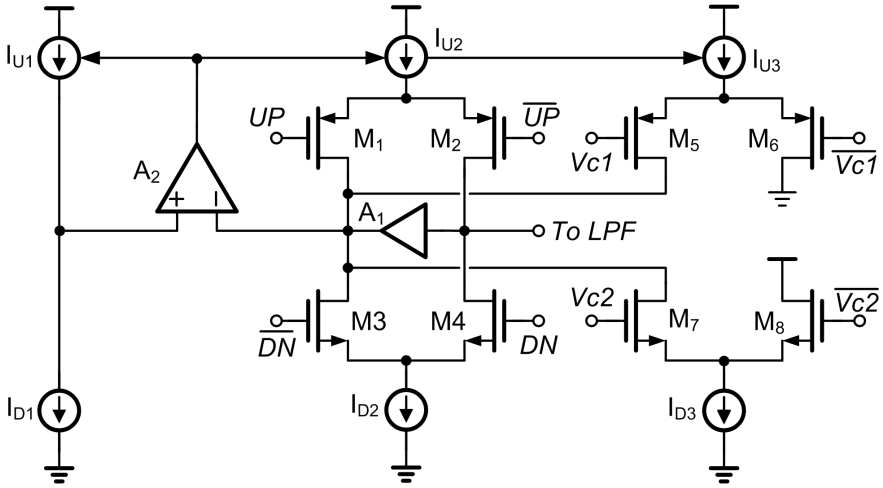


Fig. 5.13 The charge pump circuit

gain controlled range is ±1dB with 0.07dB per step, and the phase tuning range is ±12° with 0.8° per step which is designed based on the Monte-Carlo simulation under process variation. Besides, the *sel* and *selb* signal is utilized to invert *I* and *Q* vectors for up or down single side band frequency conversion. Incorporating with the vector calibrated buffer, the image rejection ratio for the SSB mixer can be suppressed below –45 dBc.

Fig. 5.12(a) shows the 1st stage multiplexer. A common gate switching stage is utilized to improve signal isolation and suppress harmonic mixing in SSB Mixer1. The circuit schematic of the 2nd stage multiplexer is shown in Fig. 5.12(b), where one of the 14-band carriers is selected by the parallel input transconductance stage. Broad band operation of 10 GHz is achieved by employing active shunt-shunt feedback [30][31][32]. The 2nd stage SSB mixers along with MUX2 provide 5dB gain to compensate the power loss of the preceding stage. It provides side band rejection up to 60 dB incorporating with the dynamically active 2nd stage SSB mixer.

A charge-pump based phase-locked loop is adopted for generating the harmonics of 264 MHz. The PFD in this design incorporates true-single phase clocking (TSPC) D flip-flop with combinational logic for higher resolution. The simulated dead zone is less than 5 ps.

The core circuit of the charge pump is shown in Fig. 5.13, which is basically composed of current steering switches (M_1-M_4) and pumping current I_{U2} and I_{D2}. As the terminal voltage of the LPF is approaching the rail potential (V_{DD} or ground), the pumping up and down currents (I_{U2} and I_{D2}) will become unbalanced due to the channel length modulation effect. This will result in unequal up and down pulse width in the locked state, and thus induces reference spur. To alleviate this problem, a regulated current feedback loop consisted of A_2, I_{U1}, and I_{D1} is

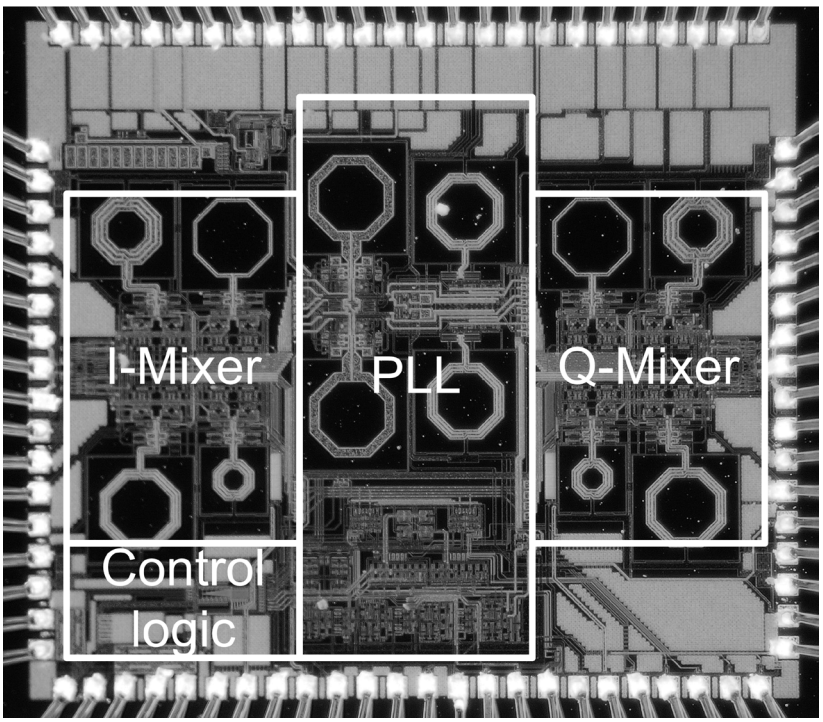


Fig. 5.14 Chip microphotograph

employed. Here I_{U1} and I_{D1} are replica of I_{U2} and I_{D2}, and the pumping currents can track each other by adjusting the gate voltage of the current source [33].

Moreover, when both UP and DN are disabled, a unity gain buffer A_1 is utilized to track the terminal voltages of the current source to that of the loop filter, so as to alleviate charge sharing effect when the pumping circuits are resumed. However, during the locking process when only UP or DN is asserted, for example, UP is high and DN is low, the tail current source intends to pull down the source node of M_3 and M_4 if the slew rate of A_1 is limited. Consequently, when the DN pulse is resumed, the imbalance of pumping currents is unavoidable. To solve this problem, we propose an improved charge pump circuit with auxiliary current steering switches (M_5, M_6) and (M_7, M_8) [34], which are controlled by Vc1 and Vc2. Here

$$V_{C1} = \overline{UP \cdot \overline{DN}}$$
$$V_{C2} = DN \cdot \overline{UP} \tag{5.10}$$

The currents I_{U3} and I_{D3} are also replica of I_{U2} and I_{D2}. The auxiliary current switches are employed to keep the tail current I_{U2} and I_{D2} alive to prevent the source node of current

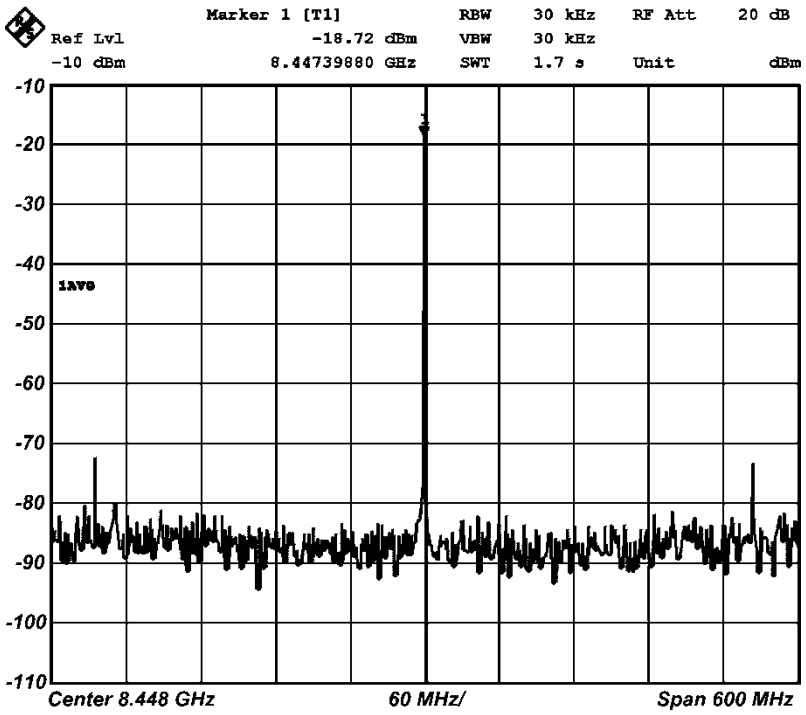


Fig. 5.15 The measured PLL output spectrum

switches from being over charged or discharged. According to simulation results, the reference spurs induced by pumping current imbalance can be improved by about 20 dB with the proposed circuit technique.

The LC tank QVCO is discussed in section 3.2 with experimental results. Based on complementary architecture, it improves phase noise performance thanks to a more symmetric output waveform [35]. Also, it benefits from two fold negative conductance for power saving. Both C_{v1} and C_{v2} are accumulation mode MOS varactors for fine frequency tuning. In addition, C_1, C_2, C_3 and C_4 are added in parallel for coarse tuning to cope with PVT variations.

The divider chain in the feedback path of the PLL is composed of CML flip-flops. For the first stage divider which operates at 8.5 GHz, shunt-peaking technique is adopted.

5.4. Experimental Result

The experimental prototype of the UWB frequency synthesizer has been fabricated in a 0.18-μm CMOS technology. It provides in-phase and quadrature phase signals for the 14 band carriers through I/Q mixer pairs. Fig. 5.14 shows the chip micrograph. The chip size is 2.5×2.2 mm^2, which is mainly occupied by LC resonators. Operating under a single 1.8 V

power supply, this chip dissipates 65 mA.

The PLL output spectrum at 8448MHz is shown in Fig. 5.15. The output power is about -12 dBm after the cable loss is taken into account. The reference spur at 264MHz offset is lower than 55 dBc. Fig. 5.16 illustrates the phase noise performance from the 8448 MHz carrier. The measured phase noise is about –98 dBc/Hz at 1 MHz offset, and the integrated rms jitter is about 2.2°.

The worst case image spurs occur for band-11 frequency synthesis (8.712 GHz). As the gray lines shown in Fig. 5.17, the image spur at 8184 MHz is about –22 dB below the main carrier without SSB mixer I/Q calibration. It can be suppressed below –45 dBc when the calibration is on. The improvement is more than 22 dB. On the other hand, as are discussed in section 5.2.1, the remaining spurs at 7656 MHz and 9768 MHz are dominated by the nonlinearities of the SSB mixers, which are 40 dB below the main carrier. Fig. 5.18 shows the output spectrum for band 2 (3.96 GHz, ω_1-ω_2) carrier generation, whose closest spur is also 528 MHz away from the main carrier. It can be seen that the image spur at 4488 MHz can be reduced by 8 dB after calibration. The remaining spurs generated by the nonlinearities of the SSB mixers are also 40 dB below the main carrier. Fig. 5.19 summaries output spectrum for other frequency bands generations, including band-7 (ω_1-7ω_2), band-9 (ω_1-3ω_2), and band-13 (ω_1+5ω_2). In these cases, their spurious free dynamic rang is mainly dominated by the harmonics of mixers, while their image spurs are less pronounced. The output power is distributed from -18 dBm to -26 dBm, and corresponding spurious free dynamic range is more than 33 dB for the full band carrier generation. When the output frequency hops from band-10 to band-11, the measured settling time is 1.59 ns, as is shown in Fig. 5.20.

Table 5.1 summarizes the performance benchmark with the prior arts. The proposed architecture is reduced the number of PLLs and SSB mixers in cascade, so as to mitigate spurs generation and reduce power consumption. Additionally, the image spurs cause by I/Q imbalance of SSB mixers can be alleviated by applying off-line I/Q calibration. In contrast to conventional analog tuning technique [12], the I/Q vector can be adjusted by 8 bits DAC to facilitate digital control. The spurious tones is reduced by more than 10 dB in contrast to the prior art [11][13][15]. For a fully integrated (PLL included) full-band carrier generation, the experimental prototype consumes the least power compared to the prior art [4].

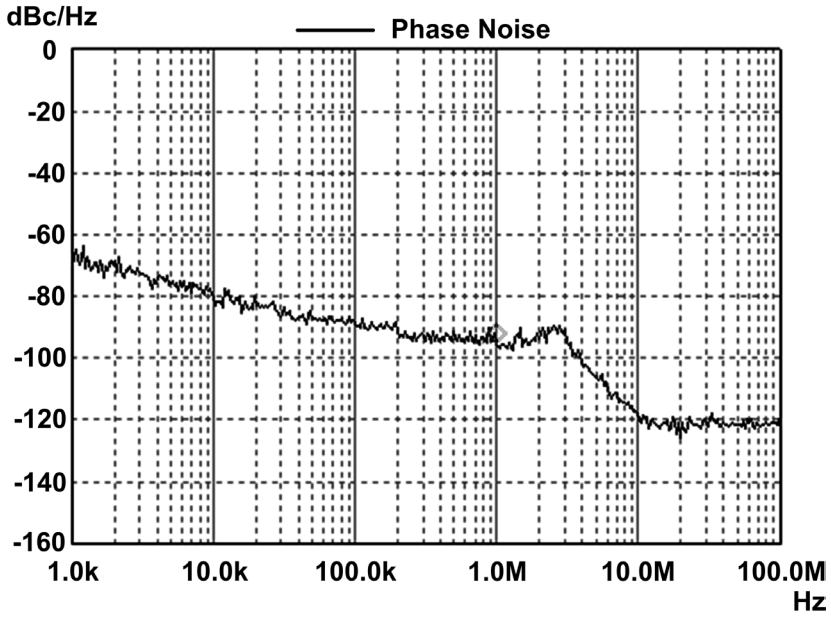


Fig. 5.16 The measured PLL phase noise

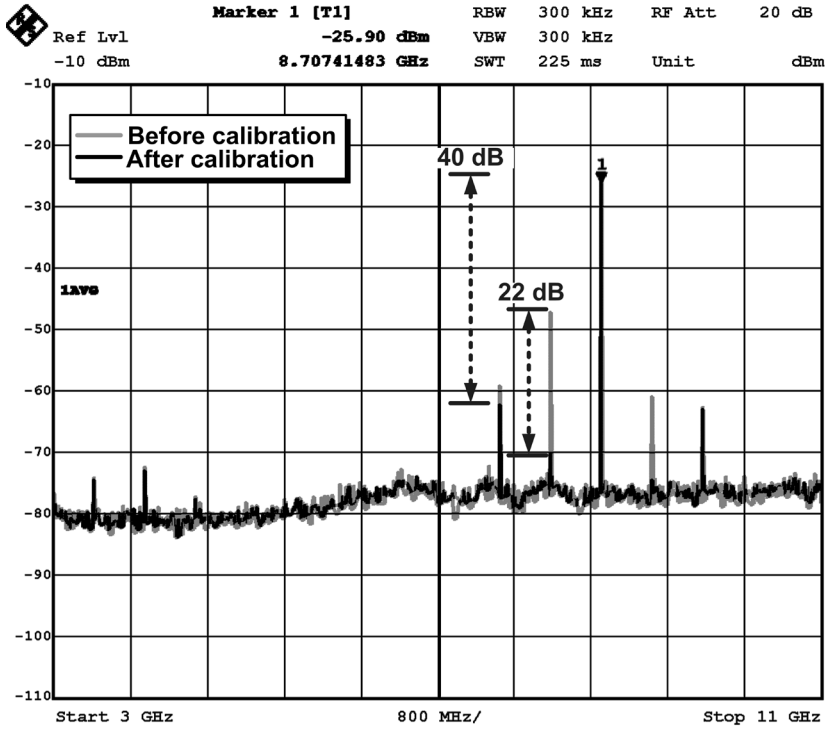


Fig. 5.17 The measured output spectrum at 8712 MHz (band 11)

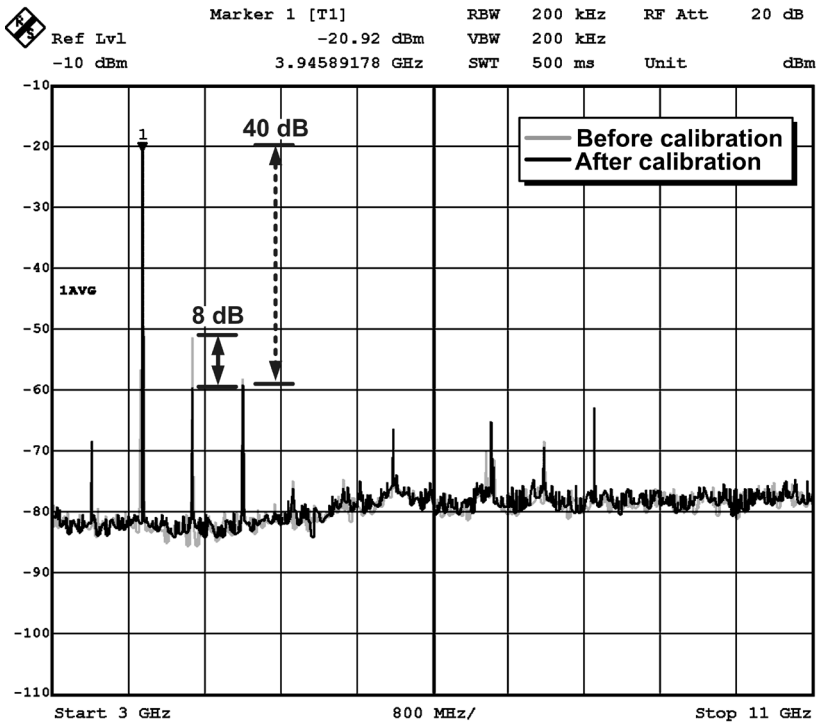
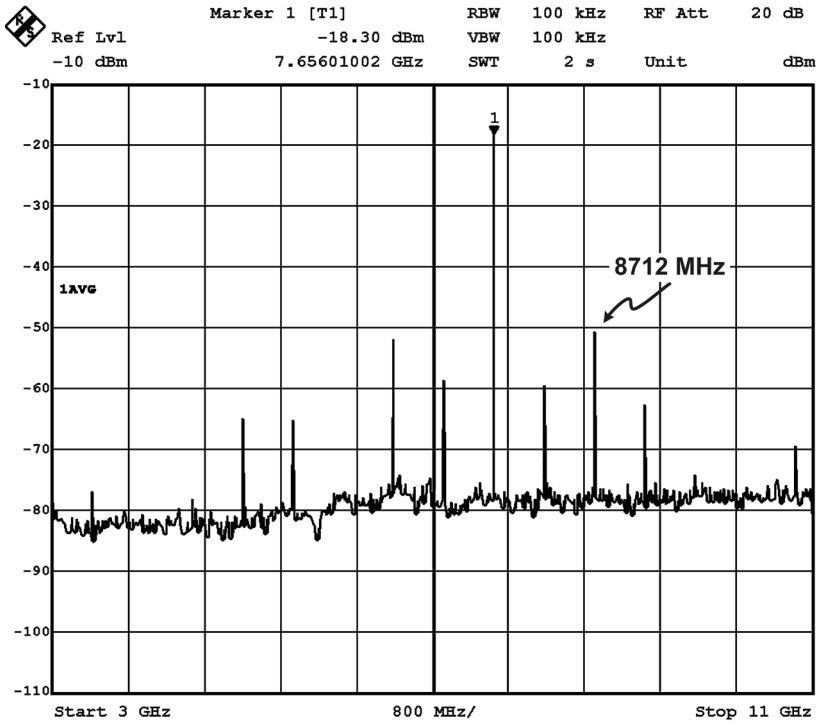
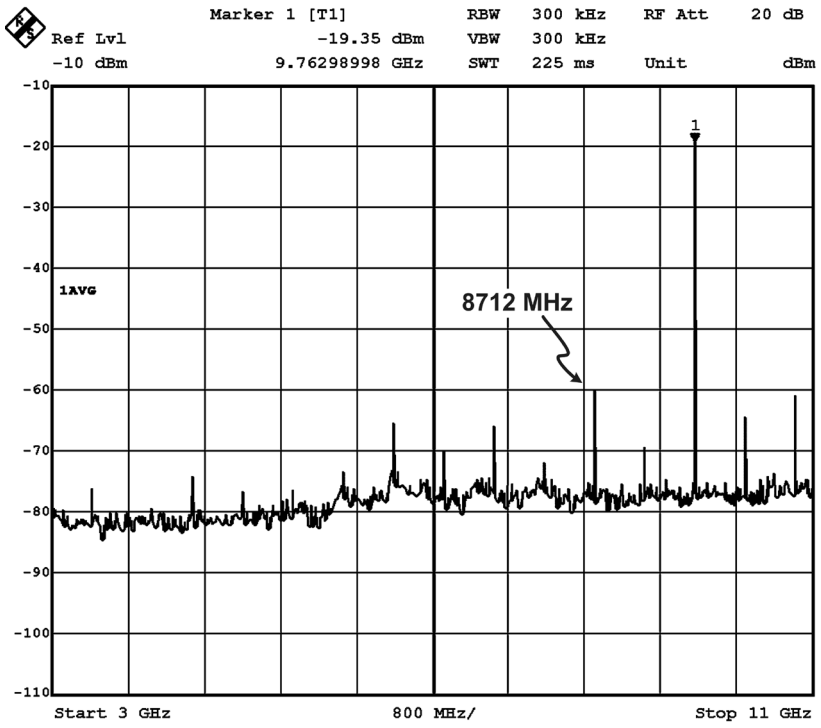


Fig. 5.18 The measured output spectrum at 3960 MHz (band 2)



(a)



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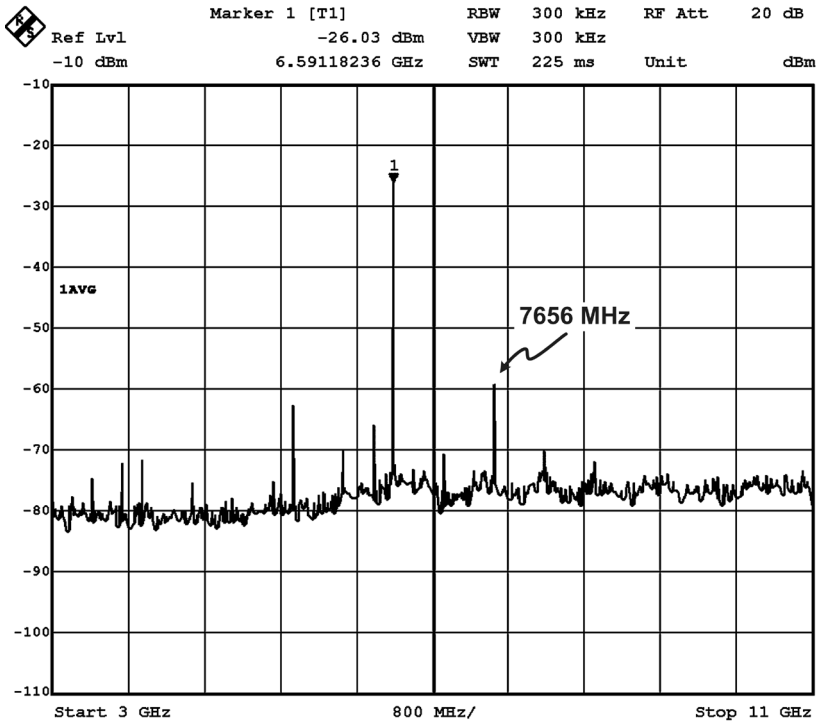


(c)

Fig. 5.19 The measured output spectrum at (a) 7656 MHz (band 9) (b) 9468 MHz (band 13) and (c) 6600 MHz (band 7)

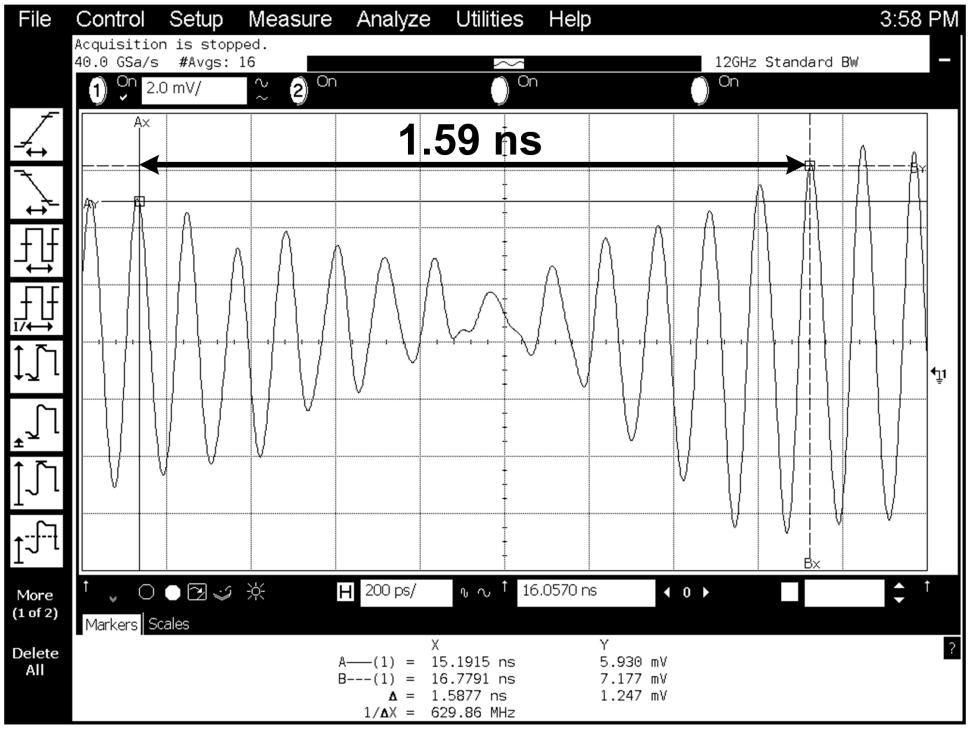


Fig. 5.20 Measured switching behavior from 8.1 GHz to 8.7 GHz

5.5. Conclusion

In conclusion, we propose a 3-10 GHz, 14 band CMOS frequency synthesizer with spurs reduction for MB-OFDM UWB system. The spur issues of cascaded SSB mixers in direct frequency synthesis method are investigated in detail, and also verified with theoretical analysis, circuit simulation, and experimental results. The frequency synthesizer is based on a single PLL and two stages SSB frequency mixing architecture. It alleviates harmonics mixing and pulling to diminish spurs generation. Also, only divide-by-2 dividers are needed in the feedback path of PLL. Thus more precise I/Q sub-harmonics can be derived for the SSB mixer. It also improves the side band leakage issues. Finally, we further improve the spurious tones by applying off-line I/Q calibration. By gain and phase adjustment, the image spurs can be reduced and suppressed below -45dBc. Implemented in a 0.18-μm CMOS technology, this chip drains 65 mA from a single 1.8 V supply.

Table 5.1

Performance benchmark of MB-OFDM UWB frequency synthesizers

Reference	This work	[14] 08'ISSCC	[4] 06'ISSCC	[12] 07'ASSCC	[13] 06'ISSCC	[11] 07'JSSC	[15] 07'JSSC
Number of bands	14	14	14	14	12	11	9
Operation frequency	3-10 GHz	3-10 GHz	3-10 GHz	3-10 GHz	3-9.5 GHz	3-10 GHz (5 GHz notch)	3-8 GHz (Dual-conversion)
Number of PLLs	1	1	2	VCO only	1	1	1
SSB mixers in cascade	2	2	3	3	2	3	2
I/Q calibration for spurs reduction	digital	no	no	analog	no	no	no
Phase noise at 1MHz offset	-98 dBc/Hz	N/A	N/A	-97 dBc/Hz	-108 dBc/Hz	N/A	-103 dBc/Hz
Sideband level	-33 dBc	N/A	-35 dBc	-35 dBc	-20 dBc	-18 dBc	-22 dBc
Measured hopping time (Band group)	<3ns (BG-4)	<3ns (BG-3)	<3ns (N/A)	<7ns (N/A)	<2ns (N/A)	<5ns (BG-1)	<1ns (BG-3)
Current	65mA	N/A	90mA	49mA	43mA	80mA	59mA
Supply	1.8V	1.2V	1.8V	1.2V	1.1V	2.5V	1.5V
Chip area	2.5×2.2 mm^2	N/A	1.27×1.2 mm^2	1.8×1.6 mm^2	N/A	2.4 mm^2 *	2.5×1.4 mm^2
Technology	180 nm CMOS	130 nm BiCMOS	180 nm CMOS	130 nm CMOS	90 nm CMOS	250 nm BiCMOS	180 nm CMOS

* Without pads

Chapter 6

Reference-Less Frequency Synthesizer and Receiver

The architecture of frequency synthesis discussed in chapter 2 must have a stable reference source for carrier frequency synthesis, such as crystal oscillators or other resonator-based reference. However, the crystal oscillator itself dissipates extra power and is too bulky to integrate on PCB. Meanwhile, the mismatch of crystal frequency between transmitter and receiver will cause carrier frequency offset (CFO), and hence a compensated circuit is needed in digital baseband. In this chapter, we propose a wireless receiver incorporating with frequency synthesizer without a need of resonator-based reference source. A 2.4 GHz reference-less single chip wireless receiver for 1Mbps QPSK demodulation is implemented for demonstration. The receiver accomplishes LO carrier recovery and data demodulation directly from the RF received signal. Integrating LNA, mixer, LO carrier recovery loop, post amplifier, and digital demodulator on a single chip, the total power consumption is 20.4mW. The measured phase noise from a recovered carrier at 2.432 GHz is about -112 dBc/Hz at 1 MHz offset. The chip size is 1.75 x 1.55 mm^2.

This chapter is organized as follows. Section 6.1 introduces the motivation of proposed frequency synthesis and its applied wireless system. Section 6.2 presents the system architecture and its principle. The established behavior model also is included in this section to discuss stability and noise issues. Section 6.3 presents the detailed circuit blocks, including the carrier recovery loop, low noise amplifier, frequency down-converted mixer, and post amplifier incorporating with receiver signal strength indicator (RSSI). The experimental results are shown in section 6.4. Finally, section 6.5 concludes this work.

6.1. Introduction

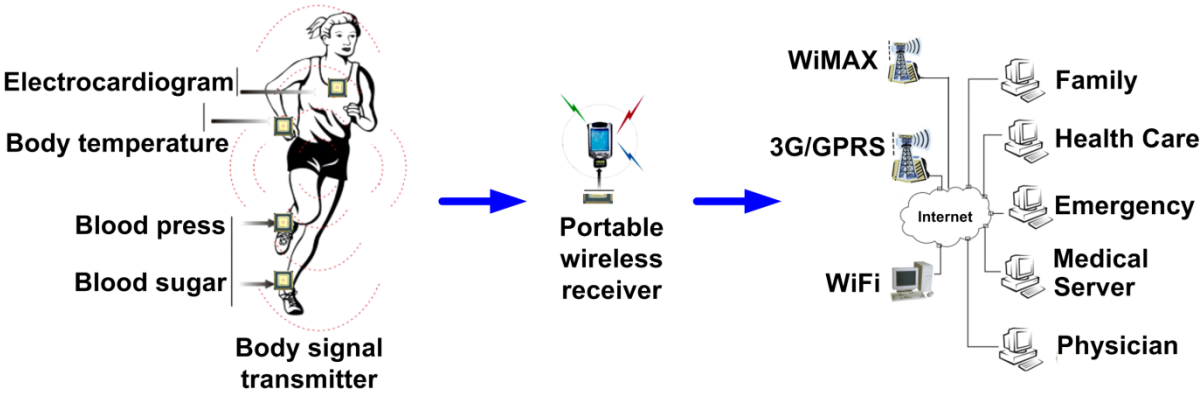


Fig. 6.1 The wireless sensor network and bio-inspired electronics

Wireless sensor network (WSN) and bio-inspired electronics have drawn tremendous research efforts [90]-[99] recently. The human signals are monitored by wireless sensor node and then transmit to the medical server through portable wireless receiver, as shown in Fig. 6.1. For the sensor node integrated circuits design, small form factor, low power, and system cost are of special interests to promote pervasive and ubiquitous adaptations. Conventionally, RF receiver front-end includes a LO (local oscillator) generator that utilizes crystal or other resonator based reference for carrier frequency synthesis. The crystal oscillator itself in general dissipates extra power and is too bulky for single chip integration. Meanwhile, due to unavoidable crystal frequency mismatches between the transmitter and receiver side, carrier recovery loop is required at the digital base band to compensate frequency offset for data demodulation.

Recently, several techniques are proposed to generate on chip reference frequency in integrated circuit technologies to replace crystal [100]-[106]. Most of their accuracy falls in the range of a few percent while consuming milli-watt power. For the frequency accuracy to be closer to that of a temperature-compensated crystal oscillator (TCXO), it may require additional costly trimming process [107].

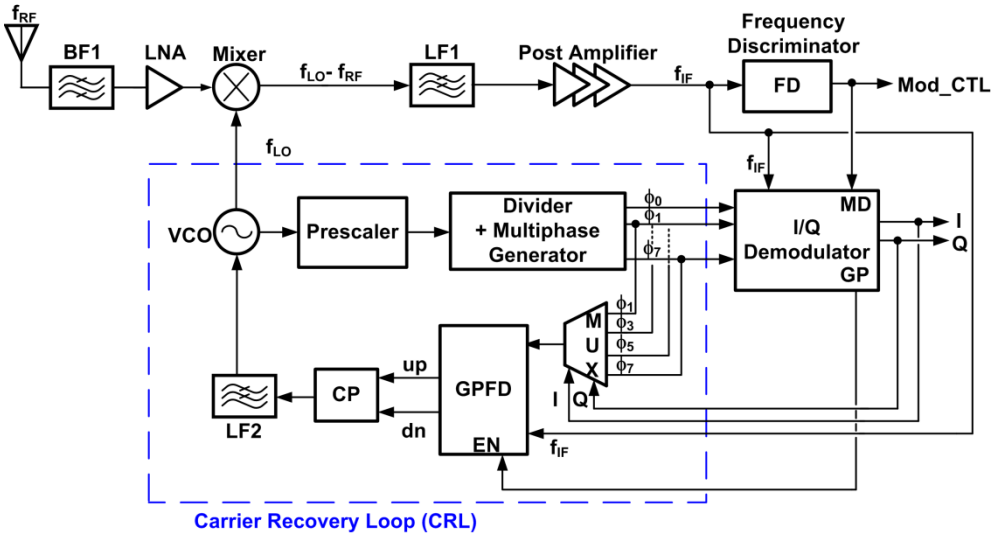
This chapter proposes a low cost, small form factor, single chip reference-less wireless receiver which recovers the LO frequency directly from the received RF signal [99]. Based on the concept of wireless remote frequency synchronization to the transmitter side, it eliminates extra reference generator at the receiver side, and also facilitates wireless clock distribution. Since the LO carrier at the receiver side is tracking the frequency at the transmitter side directly during data receiving, frequency offset problem between the transmitter and receiver in conventional wireless transceivers is eliminated. Meanwhile, it

accomplishes data demodulation along with carrier and timing recovery without resort to extra base-band ADC.

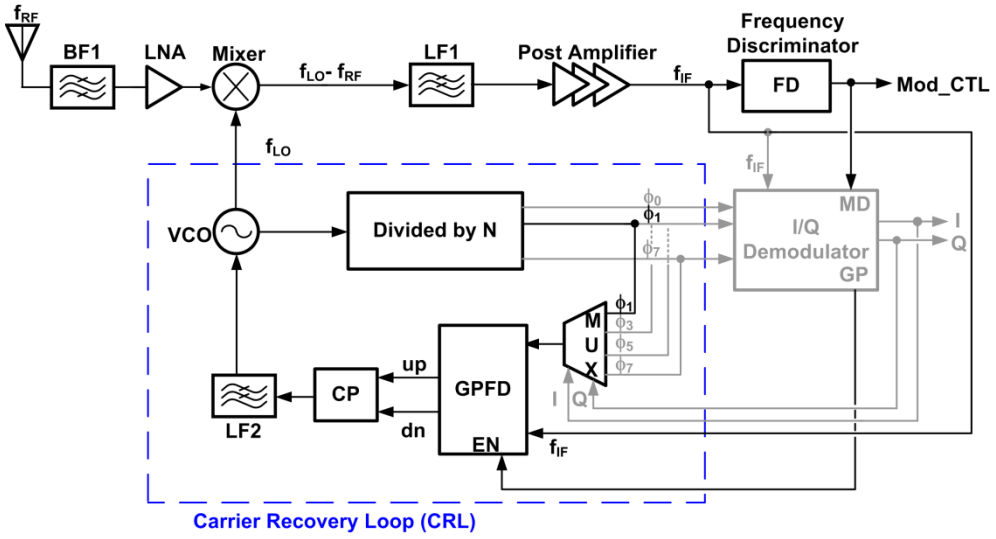
6.2. Architecture

In order to demonstrate the proposed concept, an experimental prototype for QPSK wireless receiver at 2.4 GHz is implemented. Fig. 6.2(a) shows the receiver architecture. It integrates LNA, mixer, channel selection filter, post amplifier, data demodulator, frequency discriminator, and LO carrier recovery loop (CRL) on a single chip. As a single channel experimental prototype, the interference is rejected by both external band selection filter and on chip channel selection filter. The LNA and mixer respectively provide 16.6 dB and 6.7dB gain. The post amplifier incorporating channel selection filter are composed of 6 stages, which enlarge the output to digital swing.

The CRL composes of a VCO, prescaler, divider and multiphase generator, phase selector (MUX), and a gating phase frequency detector (GPFD). Incorporating with the data demodulator, it recovers carrier frequency and clock from the QPSK modulation signal for frequency down conversion and data demodulation.



(a)



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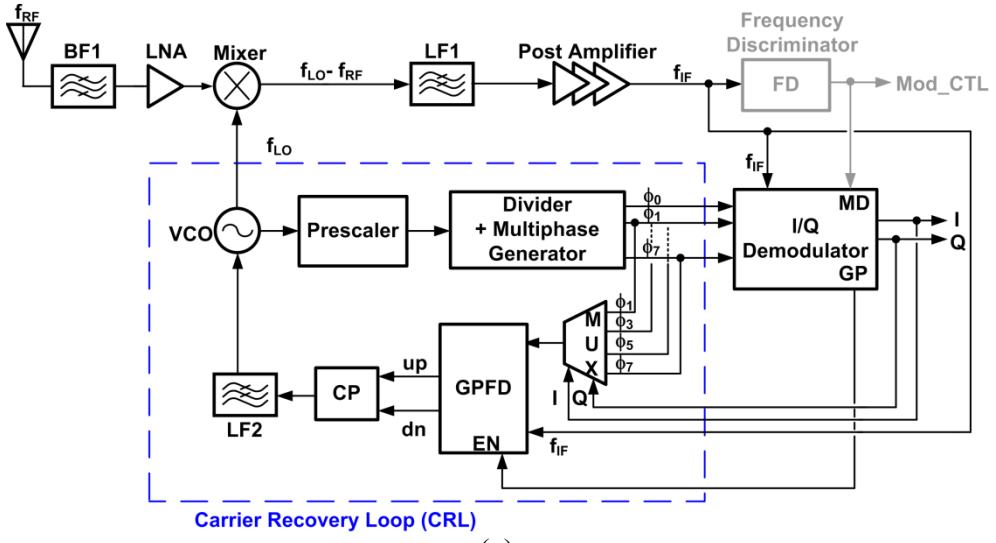


(c)

Fig. 6.2 (a) The proposed receiver architecture (b) frequency acquisition mode (c) phase tracking and data demodulation mode

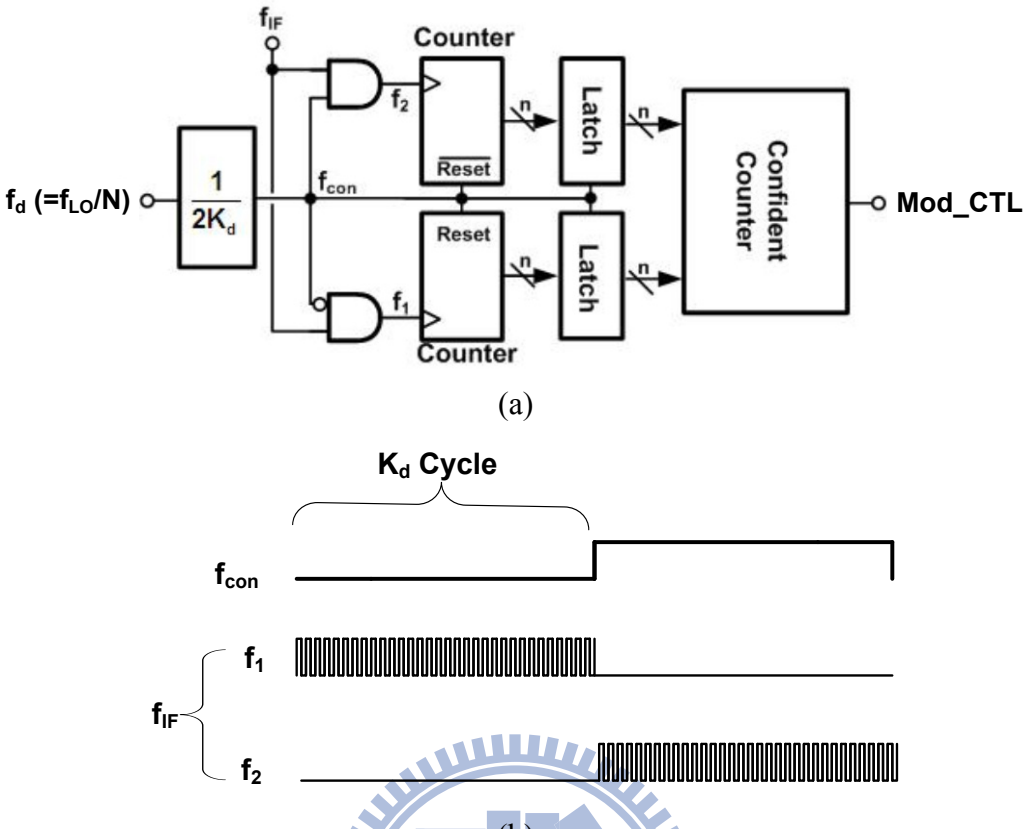


Fig. 6.3 (a) Frequency discriminator (b) timing diagram of edge counter

6.2.1. Frequency Acquisition and Phase Tracking

Let the cascade divide ratio of the prescaler and feedback divider be N, f_{LO} denote the VCO frequency, and f_{IF} represent the IF frequency. At the onset for data receiving, a constant phase preamble (f_{RF}) from the transmitter is received, and the voltage controlled oscillator (VCO) is preset to its highest frequency which is larger than f_{RF}. The CRL is operated in the frequency acquisition mode, as illustrated in Fig. 6.2(b). Meanwhile, the phase selector (MUX) passes a fixed divider output phase (one of ϕ_0 to ϕ_7) to the GPFD. The down converted signal f_{IF}, where $f_{IF} = f_{LO} - f_{RF}$, is then compared to f_{LO}/N by the GPFD. If $f_{LO} - f_{RF} > f_{LO}/N$, f_{LO} decreases so that f_{IF} is reduced more than f_{LO}/N for $N > 1$. Contrarily, if $f_{LO}/N > f_{LO} - f_{RF}$, f_{LO} increases so that f_{IF} is increased more than f_{LO}/N. By the negative feedback mechanism, when the loop is settled

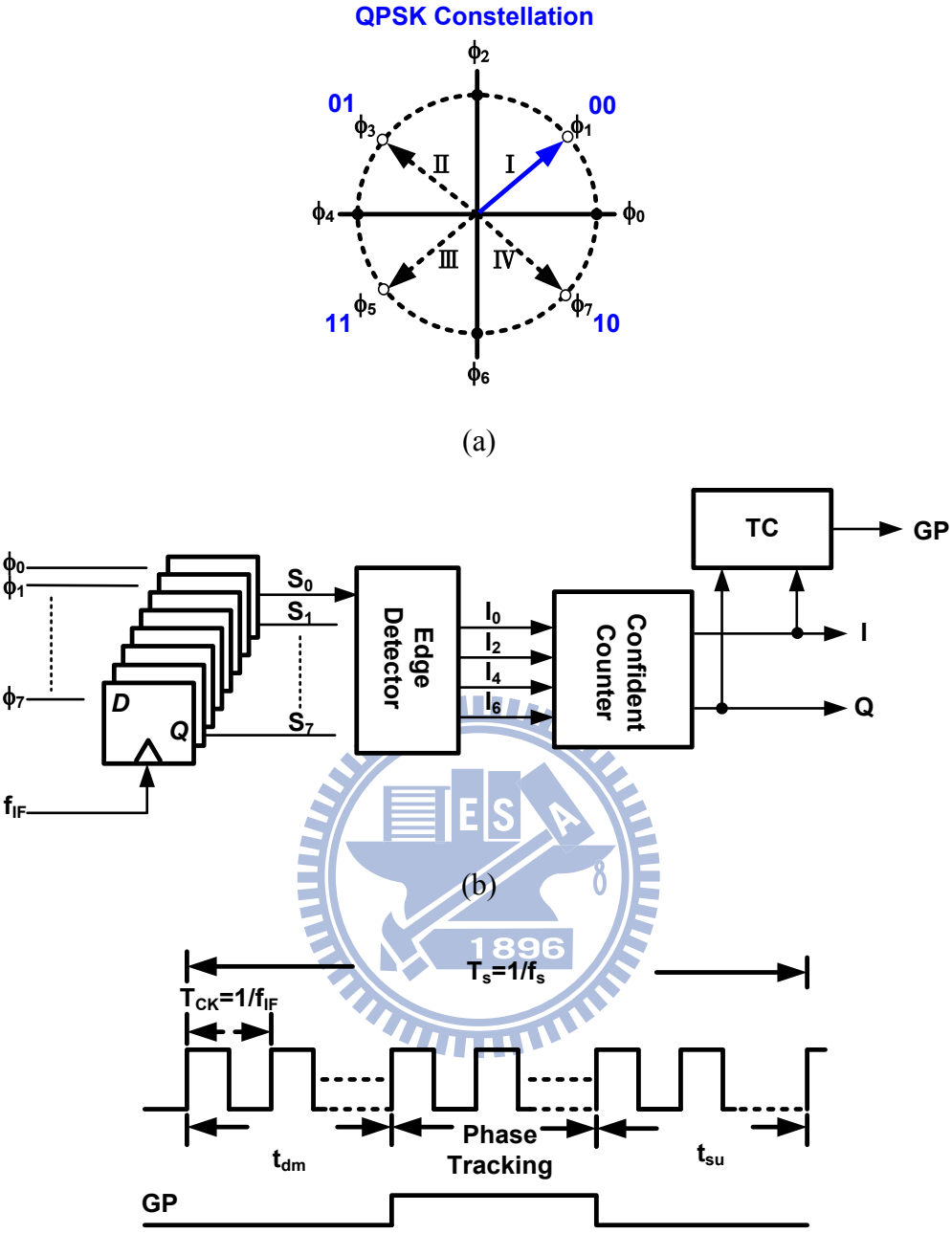
$$f_{IF} = f_{LO} - f_{RF} = \frac{f_{LO}}{N} \tag{6.1}$$

Thus the local frequency is determined by N and the RF input frequency, where

$$f_{LO} = \frac{N}{N-1} f_{RF} \tag{6.2}$$

The frequency locking detector is realized by a frequency discriminator. Fig. 6.3 illustrates detailed circuit schematic, which is based on the concept of edge counting [18]. As is described in (6.1), when the loop approaches locked, the IF frequency (f_{IF}) would be equal to the divider output ($f_d = f_{LO}/N$). In order to improve the resolution for frequency detection, f_d is scaled down by $2K_d$ to generate a control signal f_{con}. The high and low level of f_{con} alternatively performs as gating pulse of f_{IF}, whose counting edges are stored in two latches. In this design, if the contents of latches fall within ($K_d \pm 2$), the confident counter will be toggled. When the contents in latches hit the target consecutively, implying that f_{LO} approaches locked state, the status of frequency locked is then resolved by the confident counter.

To successfully demodulate M-ary phase modulation signal, the IF signal should fall into one of the M phase zones during data demodulation. It means that the frequency difference between f_{IF} and f_d should be within a locking window before the CRL steps into phase demodulation. For an M-ary PSK modulation signal, let f_s be the symbol rate, it can be shown that the lower bound of K_d can be derived as



(a)

(b)

(c)

Fig. 6.4 (a) QPSK signal constellation (b) demodulator (c) timing diagram

$$K_d \geq 2M \times \frac{f_{IF}}{f_s} \tag{6.3}$$

When the loop approaches locked, the receiver will acknowledge transmitter for data receiving. The mode control signal (Mod_CTL) will then switch the CRL to phase tracking

mode, as illustrated in Fig. 6.2(c). Afterwards, the CRL will keep track the carrier frequency as well as demodulate the QPSK signal simultaneously.

Fig. 6.4 illustrates the scheme for QPSK demodulator and timing diagram for the gating PFD. At the post amplifier output, f_{IF} switches its phase among (0^o, 90^o, 180^o, and 270^o) periodically at symbol rate (f_s), as is shown in Fig. 6.4(a). For QPSK demodulation, the divider output f_d ($f_d = f_{LO}/N$) generates 8 phases (ϕ_0 to ϕ_7) to capture f_{IF}. Here (ϕ_0, ϕ_2, ϕ_4, ϕ_6) divides the signal constellation into 4 zones, and the IF signal is directly demodulated by detecting the operating zones (I, II, III, IV) that f_{IF} falls into. This is accomplished by sampling (ϕ_0 to ϕ_7) using f_{IF} followed by edge detector and decoder. The I/Q digital output is then demodulated after confident counter, as is shown in Fig. 6.4(b).

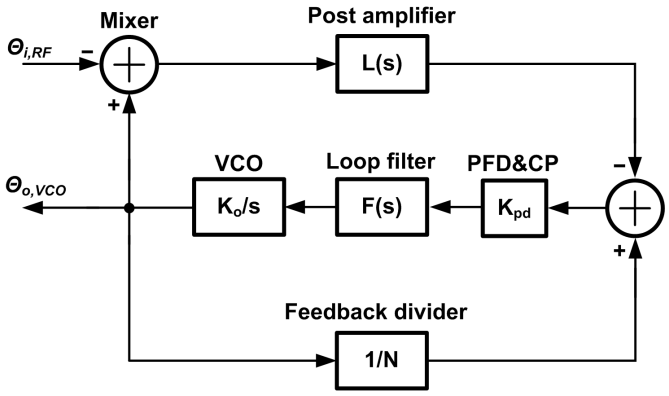
In each phase zone, the targeted phase for frequency tracking and phase synchronization is (ϕ_1, ϕ_3, ϕ_5, ϕ_7) respectively. The demodulator then switches its corresponding targeted phase according to the demodulated I/Q data through the MUX to the GPFD. Thus the CRL can continuously track the RF signal to maintain the stability of VCO output frequency during data receiving. To avoid mis-disturbing the carrier frequency during phase switching in QPSK signaling, a timing controller in the demodulator will generate gating pulse (GP) to enable the GPFD, as also shown in Fig. 6.4(c). In each symbol time ($T_s=1/f_s$), let the clock cycles ($T_{ck}=1/f_{IF}$) for data demodulation (zone detection) be t_{dm}, the setup time for next data period phase transition be t_{su} , and the ratio between IF frequency (f_{IF}) and symbol rate (f_s) be K, i.e.,

$$K = \frac{f_{IF}}{f_s} \tag{6.4}$$

During these intervals ($t_{dm}+t_{su}$), the GPFD is disabled by GP. The active period (GDC) for the GPFD becomes

$$GDC = \frac{K - t_{dm}/T_{ck} - t_{su}/T_{ck}}{K} \tag{6.5}$$

The loop bandwidth for the CRL during phase tracking and data demodulation mode is designed by taking GDC into account. On the other hand, the tracking bandwidth against noise disturbance for data demodulation reflects in t_{dm}. Both suggest that a higher K improves



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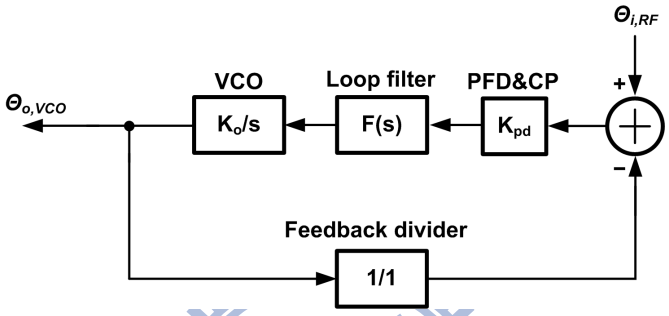

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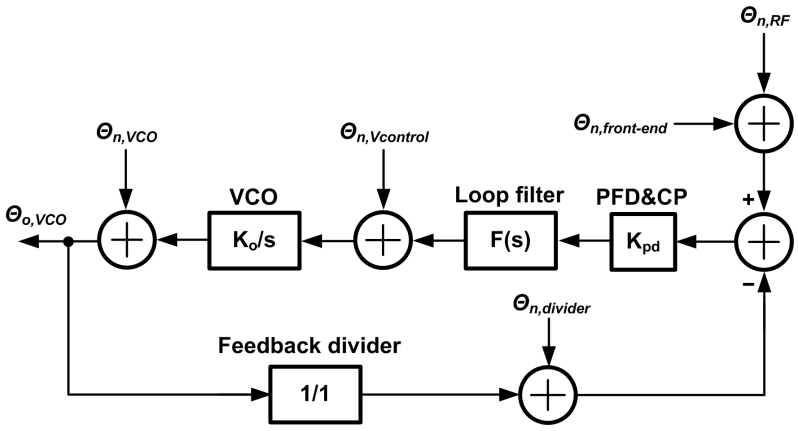


(c)

Fig. 6.5 (a) Receiver behavior model (b) equivalent model and (c) noise model

its robustness for demodulation and carrier tracking performance, but also demands a wider bandwidth IF amplifier and demodulator.

6.2.2. Behavior

The stability of the wireless carrier recovery loop is investigated using a PLL-like linear model. Fig. 6.5(a) shows the system block diagram. Let the gain of PFD and charge pump be

K_{pd}, VCO gain be K_o, and the transfer function of loop filter and post amplifier be $F(s)$ and $L(s)$ respectively.

The phase transfer function from the received RF signal $\theta_{i,RF}$ to the VCO output $\theta_{o,VCO}$ can be derived as

$$\frac{\theta_{o,VCO}}{\theta_{i,RF}} = \frac{-L(s)G(s)}{-1-G(s)\left(L(s)-1/N\right)} \tag{6.6}$$

where $G(s)=K_{pd}K_oF(s)/s$. In this design, the bandwidth of post amplifier is much higher than the IF frequency such that the phase shift caused by $L(s)$ is negligible. Thus the system transfer function can be simplified as

$$\frac{\theta_{o,VCO}}{\theta_{i,RF}} = \frac{G(s)}{1+G(s)\left(1-1/N\right)} \tag{6.7}$$

If $N >> 1$ (N = 152 in this case), the system transfer function can be approximated as

$$\frac{\theta_{o,VCO}}{\theta_{i,RF}} \approx \frac{G(s)}{1+G(s)} \tag{6.8}$$

Thus the signal transfer function is the same as that of a typical PLL with feedback factor equal to 1, as is shown in Fig. 6.5(b). The loop gain $G(s)$ can be designed to maintain its stability accordingly. Fig. 6.5(c) illustrates the noise model of the receiver front end, where $\theta_{n,front\text{-}end}$ denotes the excess noise caused by the receiver front-end, and NF is the corresponding noise figure. We have

$$\begin{aligned}\theta_{o,VCO} &\approx \frac{G(s)}{1+G(s)}\theta_{n,RF} + \frac{G(s)}{1+G(s)}\theta_{n,front-end} \\ &= \frac{G(s)}{1+G(s)}\theta_{n,RF} \times (1+\frac{\theta_{n,front-end}}{\theta_{n,RF}}) \\ &= \frac{G(s)}{1+G(s)}\theta_{n,RF} \times NF\end{aligned} \tag{6.9}$$

Thus the VCO phase noise will be elevated by the noise figure of the receiver front-end after phase locked. The designed parameters are summarized in Table 6.1, and the simulated settling behavior is shown in Fig. 6.6.

The GPFD is compared at IF frequency ($K\omega_s$) and is periodically enabled and disabled by the gating pulses (GP) for an active period of GDC, which is generated from the I/Q demodulator at a symbol rate (ω_s). Assuming that the voltage ripple caused by the nonidealities of PFD, charge pump and periodically gating is represented as

$$V_{ripple}(t) = V_{GP}(t) \times V_m \sin(K\omega_s t) \tag{6.10}$$

where V_m presents the ripple amplitude and $V_{GP}(t)$ is the gating pulse. If the VCO gain is represented as K_{VCO}, and its output frequency is ω_0, the VCO output can be represented as

$$\begin{aligned} V_{VCO}(t) &= V_0 \cos\left[\omega_0 t + K_{VCO}\int V_{ripple}(t)\,dt\right] \\ &\approx V_0 \cos(\omega_0 t) - \sum_{n=1}^{\infty} X[n]\left[\cos(\omega_0 - n\omega_s)t - \cos(\omega_0 + n\omega_s)t\right] \end{aligned} \tag{6.11}$$

$$\text{where} \quad X[n] = \frac{K_{VCO}V_0V_m}{2k\omega_s}\left[\frac{\sin\left[\pi(n-K)\times GDC\right]}{\pi(n-K)} + \frac{\sin\left[\pi(n+K)\times GDC\right]}{\pi(n+K)}\right]$$

where GDC should be greater than zero to maintain the close loop system. Eq. (11) reveals that the reference spurs will spread at multiples of ω_s at double side of the center frequency. On the other hand, the higher data rate results in a lower reference spurs. The maximum spurs will occur at $n=K$ ($\omega_{spurs}=\omega_0 \pm K\omega_s$) which dominates the SFDR of output spectrum. Therefore, the SFDR can be approximated as

$$SFDR = 20\log\left(\frac{2K\omega_s}{GDC\times K_{VCO}V_m}\right) = 20\log\left(\frac{2\omega_{IF}}{GDC\times K_{VCO}V_m}\right) \tag{6.12}$$

It can be seen that the SFDR is improved by a factor of *20log(GDC)* since the GPFD only activates for a short period. The SFDR will be the same as that of a conventional PLL if GDC equals to 1. In this design, ω_s is the 1 MHz symbol rate, ω_m (ω_{IF}) is the 16MHz IF signal, and GDC is around 0.25.

Table 6.1 Designed parameters

System parameters	**N**	152
	K	f_{IF}/f_s=16
	K_d	128
	GDC	0.25
CRL parameters	**VCO frequency**	2.2 – 2.6 GHz
	VCO gain (K_o)	100 MHz/V
	Charge pump current (I_{cp})	60 μA
	Loop bandwidth	500 KHz
	Phase margin	65°

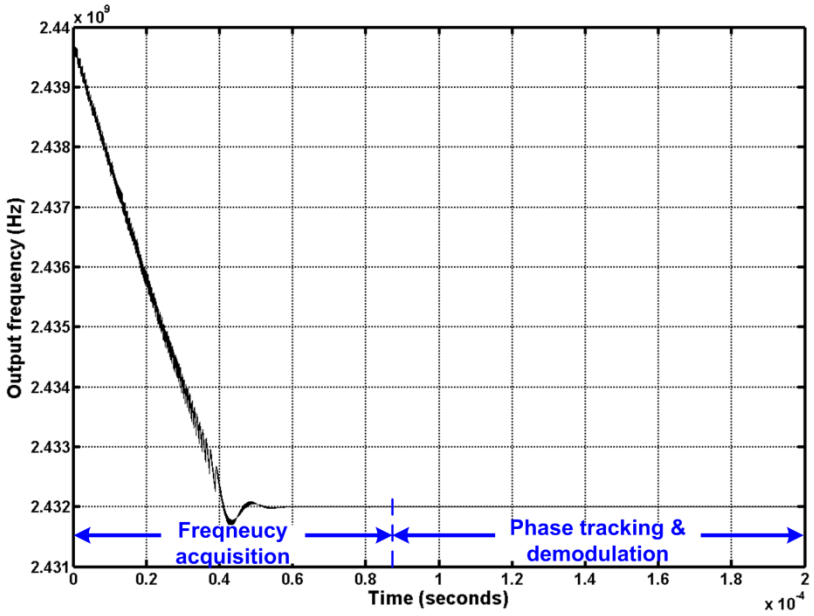


Fig. 6.6 The simulated settling behavior

6.3. Circuit Implementation

This section illustrates circuit design of the building blocks in Fig. 6.2 including SSB mixers, VCBUF, multiplexers and PLL. The two stage SSB mixers are design based on different topology due to its input power level and required linearity. The VCBUF are

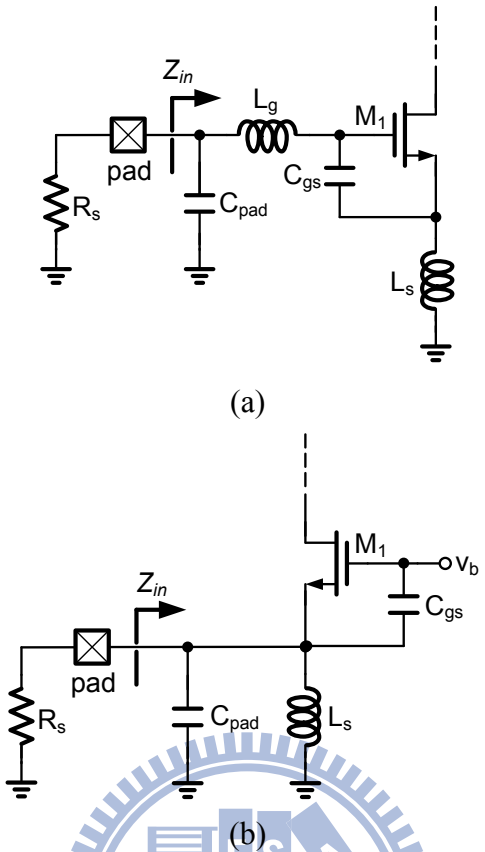


Fig. 6.7 Low-noise amplifier based on (a) common-source and (b) common-gate topology

composed of gain-calibrated and phase-calibrated buffers which have similar frequency response over wide frequency range. To speed up the switching time, current steering technique is adopted. An active shunt-shunt feedback is employed to achieve broadband operation. Finally, a second order charge-pump PLL operating in 2.4 GHz is demonstrated.

6.3.1. Low Noise Amplifier

Conventionally, low noise amplifiers in RF receiver are based on common-source [108] or common-gate [109] architectures, as are shown in Fig. 6.7. Common-source LNA (CSLNA) in general has better noise performance compared to their common-gate counterpart (CGLNA). However, it requires two on-chip inductors for narrow band input matching [110]. Contrarily, CGLNA only needs a single inductor for input matching, as shown in Fig. 6.7(b). It can provide broadband matching depending on the quality factor of the resonator (L_s, C_{pad} + C_{gs}). The noise figure of a common gate LNA can be derived as

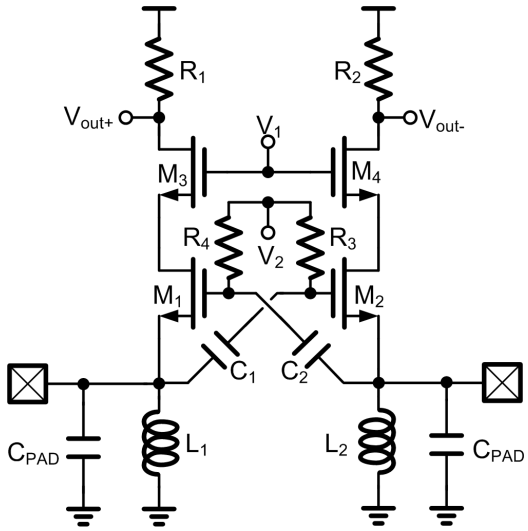


Fig. 6.8 The differential gm-boosted CGLNA

$$F_{CGLNA}=1+\frac{\overline{i_{nd}^2}\left(\frac{1}{1+g_mR_s}\right)^2}{\overline{i_{ns}^2}\left(\frac{g_mR_s}{1+g_mR_s}\right)^2}=1+\frac{\gamma g_{d0}}{g_m^2R_s}=1+\frac{\gamma}{\alpha}\Big|_{g_mR_s=1} \tag{6.13}$$

where α and γ are bias-dependent parameters. To further improve its noise performance, differential gm-boosted CGLNA topology is adopted in this design [109]-[111]. Fig. 6.8 shows the detailed circuit schematic. Its noise figure can be derived as

$$\begin{aligned} F_{CGLNA,gm-boosted} &=1+\frac{\gamma}{\alpha}\frac{1}{(1+A)} \\ &=1+\frac{\gamma}{\alpha}\frac{1}{\left(1+\frac{C_C}{(C_C+C_{gs})}\right)}=1+\frac{\gamma}{\alpha}\left(\frac{C_{gs}+C_C}{C_{gs}+2C_C}\right) \end{aligned} \tag{6.14}$$

where A ~ 1 by differential excitation. By choosing $C_C >> C_{gs}$, the noise figure can be derived as

$$F_{CGLNA,gm-boosted}=1+\frac{\gamma}{2\alpha}\Big|_{g_mR_s=1/2} \tag{6.15}$$

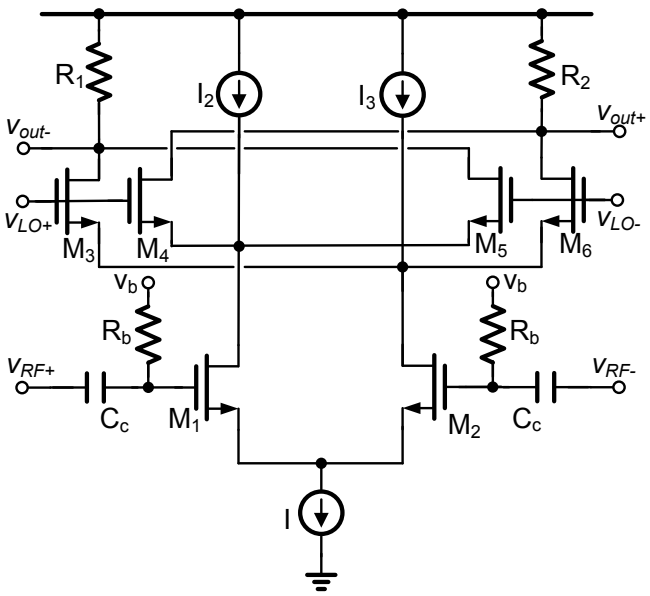


Fig. 6.9 The frequency down-converted mixer

(6.15) shows that the noise figure performance can be improved compared to (6.13) thanks to differential g_m boosted technique. On the other hand, its power consumption can be reduced for input matching.

6.3.2. Frequency Down-Converted Mixer

A double-balanced Gilbert mixer with active load is adopted for frequency down conversion. Fig. 6.9 shows the circuit schematic. In a typical Gilbert mixer, the low frequency and high frequency noise contribution can be derived as [112]

$$\begin{aligned} i_{o,low\_frequency\_noise} &= 4I\frac{V_n}{S\times D} \\ \overline{i^2_{o,high\_frequency\_noise}} &= 4kT\gamma\frac{I}{\pi A} \end{aligned} \tag{6.16}$$

where A and S respectively shows the amplitude and slope of the LO signal, I is the DC current, D is the LO period, V_n denotes low frequency input-referred noise of LO, k is Boltzman's constant, T is absolute temperature and γ is the channel noise factor. Eq. (6.16) reveal that both the noise contribution from switching pair is proportional to I. Let V_{ov} represents the overdrive voltage of M_1 and M_2, the conversion gain can be approximated as

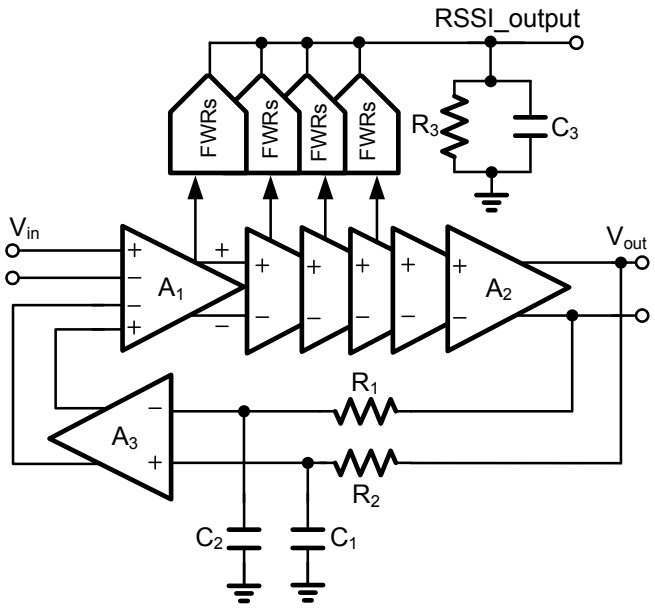


Fig. 6.10 Post-amplifier architecture

$$A_v = \frac{2}{\pi} g_{m1,2} R_{1,2} = \frac{4 I_{2,3} R_{1,2}}{\pi V_{ov}} \tag{6.17}$$

To relax the severe trade-off between the conversion gain and noise figure, current bleeding technique is adopted in this design [113]. By injecting currents I_2 and I_3 into the transconductance stage, it can decrease the DC current flowing through the commutating stage and lower the noise contribution from switching pair while sustaining the conversion gain. The simulated conversion gain of LNA and mixer are about 16.6 dB and 6.7 dB, and noise figure are about 3.5 dB and 13.3 dB respectively. The corresponding single sideband noise figure of front-end circuits is about 7.3 dB.

6.3.3. Post Amplifier

The received RF signal is amplified to digital output swing by a post amplifier. Fig. 6.10 shows the circuit schematic. It provides received signal strength indicator (RSSI) to adjust the conversion gain in the receiver front-end. The post-amplifier is composed of an offset-cancellation amplifier (A_1) followed by five identical gain cells (A_2) and an offset cancellation network (R_1-R_2, C_1-C_2, A_3).

To achieve low power design goals, all the amplifiers are based on Cherry-Hooper topology [114] to have a better power efficiency in terms of gain-bandwidth performance. Fig.

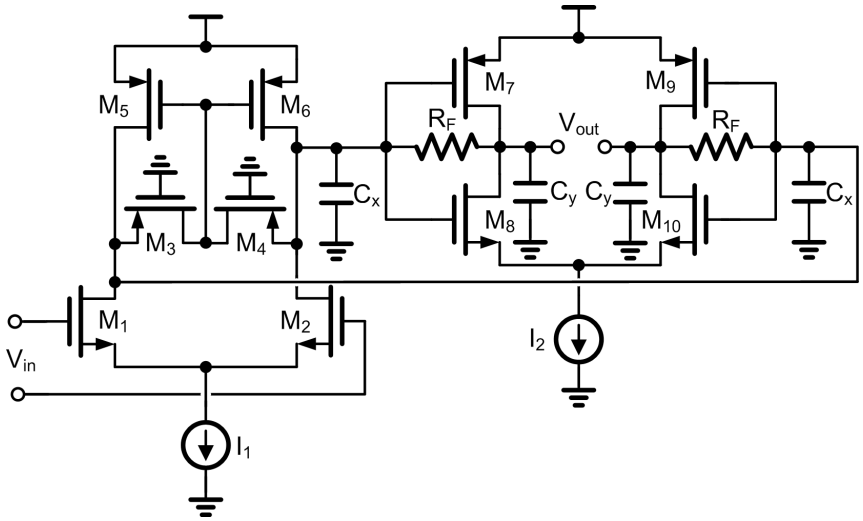


Fig. 6.11 Gain cell of post-amplifier

6.11 shows the detailed circuit schematic of a gain cell. Here M_1-M_6 performs as a transconductance stage, while M_7-M_{10} and R_F performs as the transimpedance stage.

The common mode feedback loop of the transconductance stage is realized by PMOS operating in linear region (M_5, M_6) to save chip area. The core amplifier of the TIA is an inverter based architecture for gain enhancement and low power operation by reusing DC biased current. The transfer function of each gain stage can be derived as

$$\frac{v_{out}}{v_{in}} = \frac{A_{vo}\omega_n^2}{s^2 + 2\xi\omega_n^2 + \omega_n^2} \tag{6.18}$$

where

$$A_{vo} \approx \frac{g_{m1}\left[\left(g_{m7}+g_{m9}\right)R_F - 1\right]}{\left(g_{m7}+g_{m9}\right)+1/r_{out1}+1/r_{out2}} \approx g_{m1}\left[R_F - \frac{1}{\left(g_{m7}+g_{m9}\right)}\right]$$

$$\omega_n^2 \approx \frac{\left(g_{m7}+g_{m9}\right)+1/r_{out1}+1/r_{out2}}{C_x C_y R_F}$$

$$r_{out1} = r_{o1,2} \,||\, r_{o5,6} \,||\, r_{o3,4} \;;\; r_{out2} = r_{o9,10} \,||\, r_{o7,11}$$

$$\xi \approx \frac{C_x + C_y}{2\sqrt{C_x C_y R_F \left(g_{m7}+g_{m9}\right)}}$$

For a maximally-flat Butterworth response (ζ ~0.707), the -3dB bandwidth of the gain stage can be approximated as

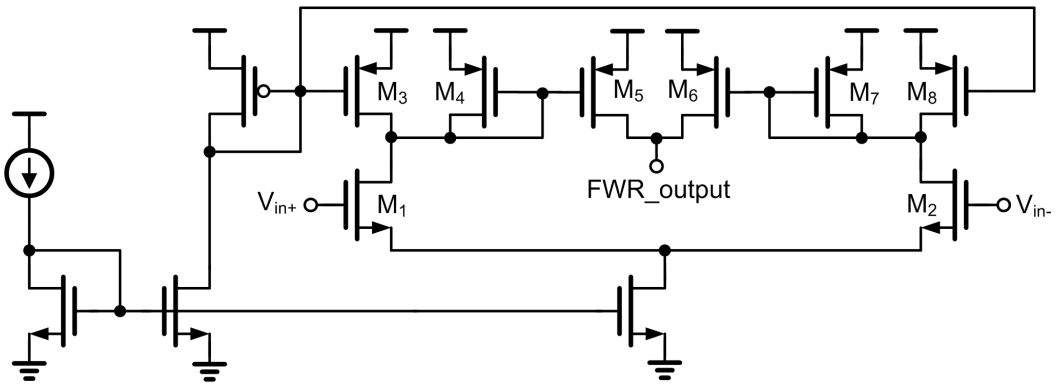


Fig. 6.12 Full wave rectifier for RSSI

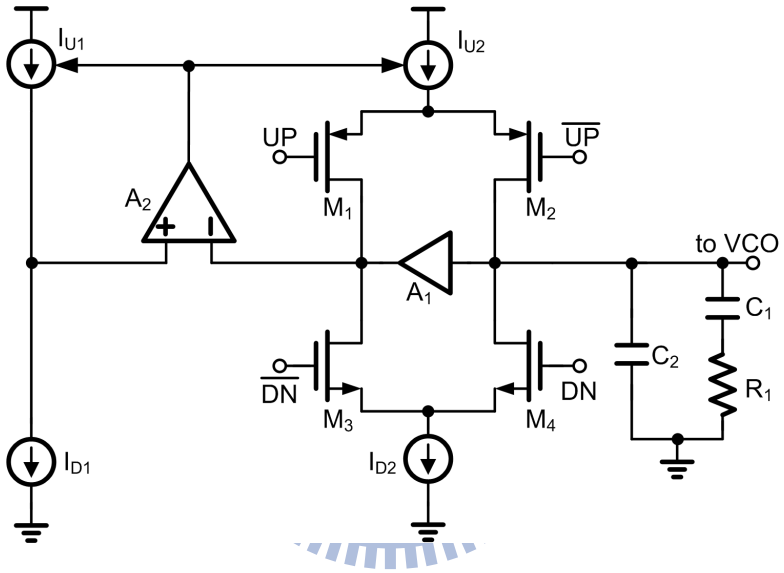
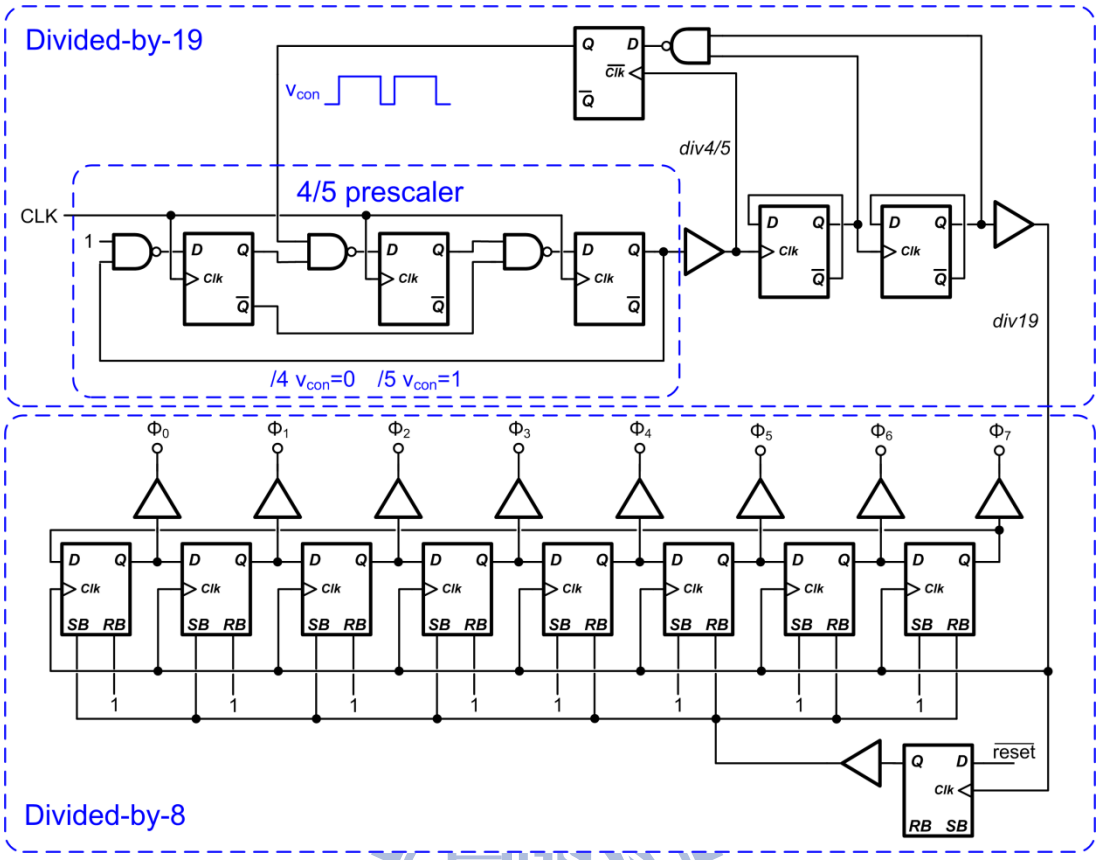


Fig. 6.13 The circuit schematic of charge pump and loop filter

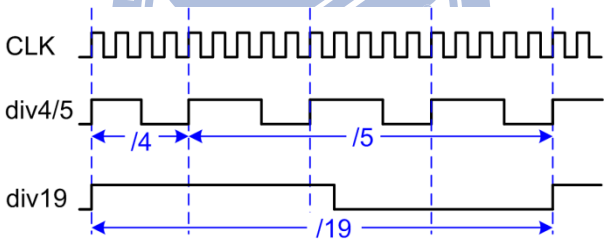
$$\omega_{-3dB} = \sqrt{\frac{(g_{m7} + g_{m9}) + 1/r_{out1} + 1/r_{out2}}{C_x C_y R_F}} \tag{6.19}$$

The plateau gain of the post amplifier is about 70 dB and the high frequency -3 dB bandwidth is 80 MHz, which is five times more than the IF bandwidth to alleviate group delay variations.

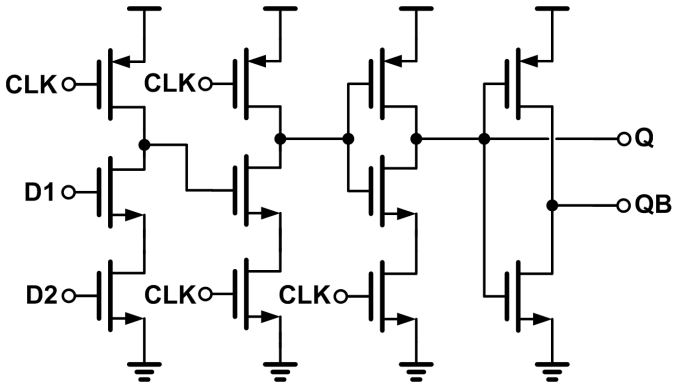
The RSSI is composed of a RC low-pass filter (R_3 and C_3) and four stage full wave rectifiers (FWR), which are connected to the output of gain cells. Fig. 6.12 shows the detailed circuit schematic of the full wave rectifier. The input voltage is converted to current form by the differential pair (M_1-M_2), and then rectified through current mirrors (M_4-M_5) and (M_6-M_7). The dynamic range of RSSI is about 40 dB.



(a)



(b)



(c)

Fig. 6.14 The architecture of (a) feedback divider, (b) timing diagram of divided-by-19 divider and (c) NAND gate embedded TSPC filp-flop

6.3.4. Carrier Recovery Loop

The CRL consists of a VCO, prescaler, divider, multiphase generator, phase selector (MUX), and a gating phase frequency detector (GPFD). Incorporating with the data demodulator, it recovers carrier frequency and clock from the QPSK modulation signal for frequency down conversion and data demodulation.

The LC tank VCO at 2.4 GHz with 3 bits coarse tuning is introduced in section 3.2. Based on complementary architecture, it improves phase noise performance thanks to a more symmetric output waveform [36]. Also, it benefits from two fold negative conductance for power saving. Here both C_3 and C_4 are accumulation mode MOS varactors for fine frequency tuning. In addition, SC_1 and SC_2 are added in parallel for coarse tuning to cope with PVT variations.

Fig. 6.13 shows the schematic of charge pump and loop filter. To alleviate reference spurs induced by current mismatch of up and down currents (I_{U2} and I_{D2}) due to channel length modulation, a regulated current feedback loop consisted of A_2, I_{U1}, and I_{D1} is employed. Here I_{U1} and I_{D1} are replica of I_{U2} and I_{D2}, and the pumping currents can track each other by adjusting the gate voltage of the current source [34].

The divider chain in the feedback path of the CRL is composed of a high speed divided-by-19 divider followed by a divided-by-8 divider, as shown in Fig. 6.14. The divided-by-19 divider is composed of a 4/5 prescaler, a divide-by-4 divider and a control logic. Fig. 6.14(b) shows the timing diagram. To reduce power dissipation as well as propagation delay, TSPC flip-flops with embedded NAND gate are incorporated in the dividers, as shown in Fig. 6.14(c). The synchronous divided-by-8 divider also performs as a multi-phase generator. Fig. 6.14(a) shows the circuit schematic. The 8 phases output signals are then utilized to capture QPSK symbols, and one of them is passed to the GPFD for phase tracking.

6.4. Experimental Result

The single-chip crystal-less wireless receiver has been fabricated in a 0.18 μm CMOS process, and powered by a 1.8 V supply. A single channel experimental prototype is implemented to demonstrate the concept. The power dissipation for the RF/analog front-end (LNA + mixer + post amplifier + channel selection filter) is about 9.6mW, while the data demodulator and CRL consumes about 10.8mW. Fig. 6.15 shows the chip photograph. The

chip size is 1.75 x 1.55 mm^2, and is mounted on a printed circuit board for measurement.

The rejection of out band interferers mainly relies on external band selection filter. By using TA0532A SAW filter, the out band interferers are suppressed 40 dB. Besides, a 6^{th} order low pass filter is implemented incorporating post amplifier for channel selection in this design. To emulate the RF signal at the transmitter side, a 1Mbps QPSK modulated signal is generated by Tekronix AWG7000B arbitrary waveform generator, and then up converted to 2.416 GHz through R&S SMIQ03 signal generator. For BER < 10^{-3}, the in band signal to interference ration must be higher than 15 dB to maintain phase locked. With -65dBm input signal at the receiver side, the measured recovered spectrum is shown in Fig. 6.16. It can be seen that the closest spurs are at 1MHz offset corresponding to the data rate.

The measured settling time of the CRL is shown in Fig. 6.17, the duration of preamble should be larger than 90 μsec for frequency synchronization. The proposed architecture can extract the carrier frequency directly from the RF signal without resort to extra resonator based reference. The measured phase noise performance is shown in Fig. 6.18, which is about -111 dBc/Hz at 1 MHz offset. The phase noise performance is also comparable to RF frequency synthesizer with crystal reference. Fig. 6.19 shows the eye diagram of demodulated I/Q signal. It reveals clear eye for the data demodulation as well.

Table 6.2 shows the performance benchmark for 2.4 GHz wireless sensor applications. Compared to the prior art, the proposed receiver accomplishes frequency down conversion as well as OQPSK demodulation without extra ADCs, on chip reference, and additional carrier recovery loop in the base band. It achieves much higher data rate (1Mbps) in contrast to the prior art. Besides, the measured phase noise is also comparable to RF frequency synthesizer with crystal reference.

6.5. Conclusion

This paper proposes a novel single chip wireless QPSK receiver without resort to extra resonator based reference. In contrast to conventional architectures, the receiver recovers the RF carrier frequency directly from the incident radio signal for frequency down conversion. Meanwhile, it accomplishes phase and frequency tracking as well as QPSK demodulation simultaneously. Thus no additional base-band ADCs or timing recovery loop are required in this receiver. It greatly improves the system integration level.

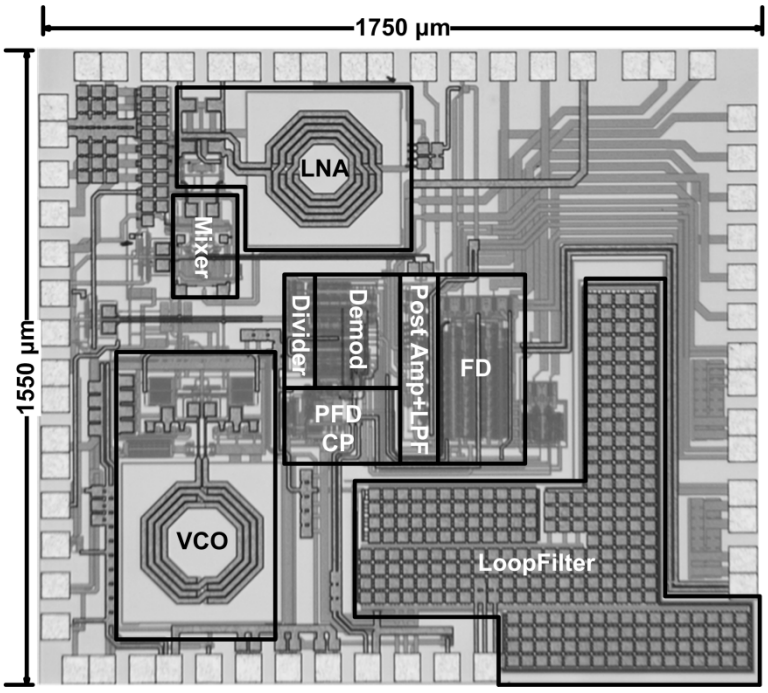


Fig. 6.15 Chip microphotograph

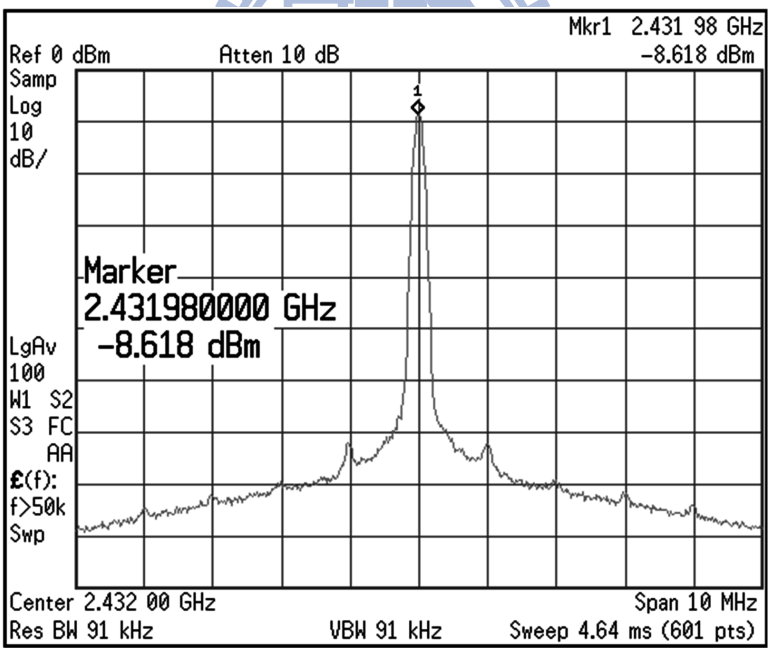


Fig. 6.16 Measured recover spectrum of the local oscillator

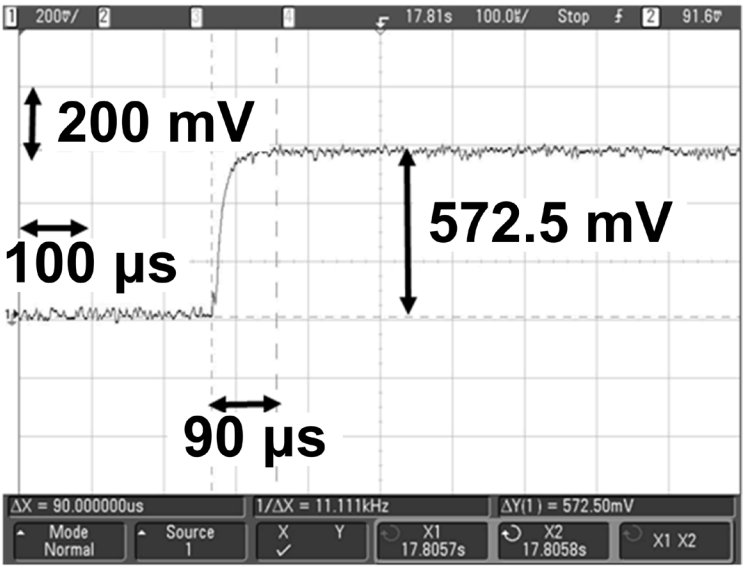


Fig. 6.17 Measured frequency locking time

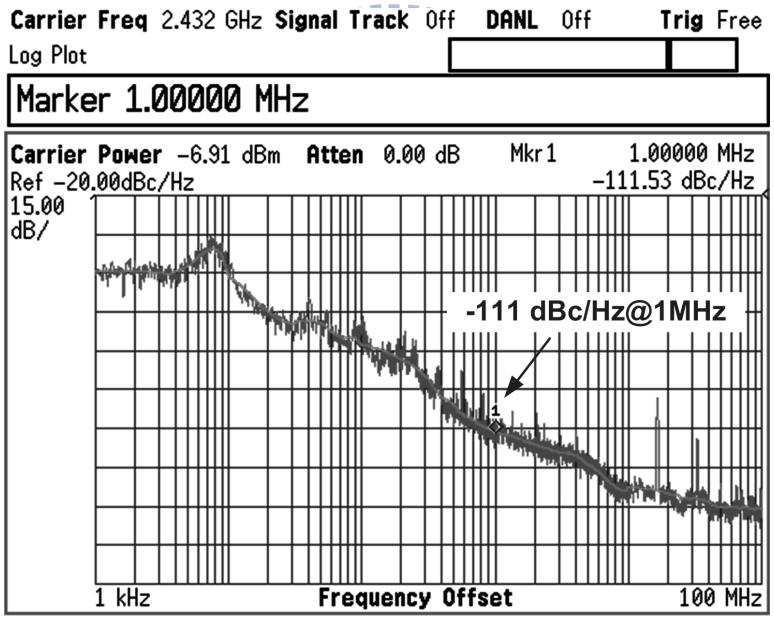


Fig. 6.18 Measured phase noise performance

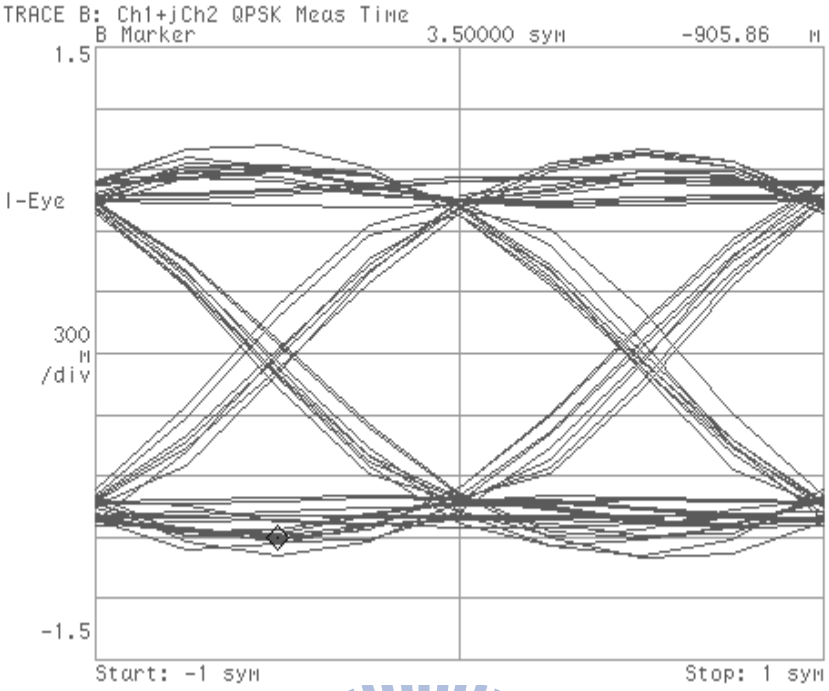


Fig. 6.19 Eye diagram for demodulated signal

Table 6.2 Performance benchmark for 2.4 GHz receiver for WSN

Reference	This work	[115]	[116]	[117]
Center frequency	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz
Data rate	1 Mbps	N/A	N/A	200 Kbps
Sensitivity (BER < 10^{-3})	-65 dBm	-60 dBm	N/A	-75 dBm
LO phase noise	-111 dBc/Hz @1MHz	N/A	-127 dBc/Hz @3MHz	-136 dBc/Hz @1MHz[a]
Additional components required	RF filter	RF filter A/D X'tal Osc.	RF filter A/D X'tal Osc.	RF Filter A/D X'tal Osc. BAW Osc. BAW Filter
System level integration	PCB	PCB	Receiver	PCB
Power consumption	20.4 mW	6.3 mW[b]	32.5 mW[c]	18.7 mW[d]
Receiver chip size	2.7 mm^2	N/A	2.9 mm^2	N/A
Technology	180 nm CMOS	180 nm CMOS	90 nm CMOS	180 nm CMOS

(a) BAW DCO locked by a crystal-based ADPLL
(b) LNA and mixer only
(c) LNA, mixer and LO
(d) excludes crystal oscillator
(e) receiver mode

Chapter 7

Conclusion

7.1. Summary

In this dissertation, the CMOS circuit techniques for frequency synthesis and wireless communication is presented. To conquer the encountered challenges in contemporary communication systems, the frequency synthesis techniques and circuit skills are developed.

First, a 38/114 GHz switched-mode standing wave oscillator (SWO) capable of synchronous locking is presented. The SWO is capable of generating fundamental and triple output frequency in the sub-THz range by nature. Different excitation modes are enabled by digital control without resort to other high speed circuits or edge combiner. Additionally, incorporating mode enabling and sub-harmonic injection locking, the proposed SWO can be synchronized to external reference to further improve phase noise performance. The close-in phase noise is improved by about 18 dB with the proposed scheme when the SWO is with synchronous lock. The experimental prototype was fabricated using a low leakage 65 nm 1P9M triple-well CMOS technology.

Secondly, a 10 GHz LC-type DCO achieves a 75 KHz frequency resolution with 10 GHz operating frequency for an all-digital PLL (ADPLL). The frequency resolution can be further enhanced by employing high speed dithering. The measured phase noise is -102dBc/Hz at 1MHz offset, while consumes 3.9 mW from a 1V power supply. Besides, a 40 GHz 11% tuning range DCO using the proposed linear variable inductor (VID) is introduced for 60 GHz UWB system. By employing the proposed frequency tuning scheme, wide-tuning range as well as multi-band operations are achieved without sacrificing its operating frequency. Fabricated in 90-nm digital CMOS process, the DCO is capable of covering frequency range from 37.6 to 43.4 GHz.

Thirdly, a 14 bands CMOS frequency synthesizer with spurs reduction for MB-OFDM UWB system using direct frequency synthesis technique is demonstrated. Based on a single phase locked loop and two-stage frequency mixing architecture, it alleviates harmonics mixing and frequency pulling to diminish spurs generation. Also, only divide-by-2 dividers

are needed in the feedback path of the PLL. Thus more precise I/Q sub-harmonics can be derived for the SSB mixer in the 14 bands carrier generation. From experimental results, the image spurs are suppressed below -45dBc and improved by more than 22 dB incorporating with I/Q calibration using 0.18-μm CMOS technology.

Finally, a 2.4 GHz reference-less single chip wireless receiver for 1Mbps QPSK demodulation is implemented for demonstration. The receiver accomplishes LO carrier recovery and data demodulation directly from the RF received signal without a need of resonator-based reference source and extra baseband ADC. Integrating LNA, mixer, LO carrier recovery loop, post amplifier, and digital demodulator on a single chip using 0.18-μm CMOS technology, the total power consumption is 20.4mW.

The proposed techniques in this dissertation can conquer the challenges coming from modern communication systems. Additionally, more circuit techniques can be inspired for future development.

7.2. Future Work

This section presents several suggestions for future investigations into the techniques for frequency synthesis.

- Higher oscillation mode can obtain a multiple output frequency but lower the output power in penalty. The antenna array techniques that could be employed to combine the electromagnetic power in space domain, which has no limitation of voltage head room, to enhance output power. The on chip antenna arrays have low area in sub-THz frequency range, or a flip chip and MEMs techniques could achieve low cost and high antenna gain.
- The frequency resolution of DCO for 60 GHz UWB is an issue. A finer frequency resolution could be achieved by high speed dithering through ΔΣ modulator. A transmission line with programmable phase velocity may be another solution.
- In chapter 5, the chip size is large. It can be improved by using more advance CMOS technology instead of 0.18 μm CMOS process.
- To be more robust against in band interferers in reference-less receiver, a more elaborate channel selection filter can be adopted. Besides, the noise outside of a channel can also be filtered out to improved sensitivity level.

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Vita

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Publication List

(A) Referred Journal Papers:

[1]. Wei-Zen Chen, **Tai-You Lu**, Wei-Wen Ou, Shun-Tien Chou, and Song-Yu Yang, " A 2.4 GHz Reference-less Wireless Receiver for 1Mbps QPSK Demodulation," accepted by *IEEE Trans. Circuits and Systems I.*

[2]. **Tai-You Lu** and Wei-Zen Chen, "A 3-10 GHz, 14-Band CMOS Frequency Synthesizer with Spurs Reduction for MB-OFDM UWB System," accepted by *IEEE Trans. Very Large Scale Integration System*.

[3]. **Tai-You Lu** and Wei-Zen Chen, "A 38/114 GHz Switched-Mode and Synchronous Lock Standing Wave Oscillator," *IEEE Microwave and Wireless Components Letters,* vol. 21, no. 1, pp. 40-42, Dec. 2010.

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(B) International Conference Papers:

[1]. Wei-Zen Chen, Wei-Wen Ou, **Tai-You Lu**, Shun-Tien Chou, and Song-Yu Yang, "A 2.4 GHz Reference-less Wireless Receiver for 1Mbps QPSK Demodulation," *2010 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1627-1630, Feb. 2010.

[2]. Chi-Yao Yu, Wei-Zen Chen, Chung-Yu Wu, and **Tai-You Lu**, "A 60-GHz, 14% Tuning Range, Multi-Band VCO with a Single Variable Inductor," 2008 *IEEE Asian Solid-State Circuits Conference (ASSCC)* , pp. 129-132, Feb. 2008.

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(D) Patents:

[1]. Wei-Zen Chen and **Tai-You Lu** "Method and Apparatus for Frequency Synthesizing," U.S. patent (US7792497).

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