國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

奈米尺寸金氧半場效電晶體之重要製程開發

Key Process Development

in Nano-scale MOSFETs Manufacturing

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指導教授 ：陳明哲 博士

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摘　　要

半導體工業自 1970 年代以來，成功地把電晶體的尺寸與製造成本，隨著時間以指數的方式減小。同時，電晶體的效能在過去的幾十年間也持續地增強，並且在可預見的未來也被預期必須能繼續提升。現代的超大規模積體電路(VLSI)極度仰賴應力工程，氧化層厚度微縮，極淺接面，以及通道結構之設計，以期提升電晶體效能並且維持合理的短通道電晶體靜電特性。我們在本論文中，針對以上所提及的重要製程模組進行討論，並且提出利於製程整合又符合成本效益的改善方案。

首先，我們以載子遷移率之一致性(mobility universality)為基礎，提出了一個新穎的方法用以萃取源極/汲極串聯電阻(R_{sd})。本方法的優點源自於使用特定的偏壓條件所創造的高電場之下，固定的載子遷移率。這個的特性的應用，是第一次在文獻中被討論。源極/汲極串聯電阻可以使用單一電晶體元件的直流電流-電壓量測所萃取，而不需要知道閘極氧化層厚度，閘極長度，有效通道寬度。正是這一個特點，使得本方法特別適用於短通道電晶體。本方法被廣泛的實驗資料所驗證，隨後被用在評估本文所提出各個製程。

由毫秒退火(millisecond-annealing， MSA)所促成的全矽化閘極(FUSI-gate)技術，首次由本論文提出。這個特殊的技術使用毫秒退火於鎳矽化物(nickel silicide)相變化製程，導致具有強伸張力的全矽化閘極，進而施加壓縮力於通道區域。對於欲防止產生全矽化閘極的區域，氮原子的離子植入提供了良好的選擇性。前人所提出的全矽化閘極製程，普遍需要化學機械研磨製程(CMP)，複晶矽凹陷製程，以及額外的微影光罩顯影製程。相較之下，本方法的製程整合架構十分符合成本效益。增強的電洞遷移率與被消除的複晶矽空乏效應(polysilicon depletion effect)，共同導致 p-型電晶體推動電流的顯著提升。本技術亦實現了均勻的全矽化閘極形成，直下到 30 奈米的閘極長度。

對於調變嵌入式矽鍺(e-SiGe)之尖端與通道區域的距離(proximity)，我們提

出一個新穎的作法。以傳統的技術而言，繁複的蝕刻製程搭配隔離物(spacer)結構是常見的方法。然而，由製程所引發的嵌入式矽鍺之 proximity 偏差卻又導致嚴重的 p-型電晶體之效能偏差。在本文中，我們使用在氫氣環境中的熱處理，達到了極度接近又能自行對準的嵌入式矽鍺之 proximity。相異於傳統的作法通常使用隔離物去定義嵌入式矽鍺之 proximity，我們所提出的技術可以將嵌入式矽鍺之尖端自動對齊至閘極的邊緣。本文的論點獲得了穿透式電子顯微鏡分析之證實。P-型電晶體效能也獲得顯著的提升。

提高閘極電壓的 overdrive headroom (V_g-V_{th}) 對於低供應電壓之奈米尺寸電晶體非常的關鍵。除了在傳統上常使用的次臨界電流斜率(sub-threshold swing)以外，我們提出了一個新的指標，“V_{th_lin}-V_{th_gm}”，用以描述電晶體開-關轉變的急劇程度。這個新指標在低供應電壓及低臨界電壓之操作環境之下，益顯得重要，因為它佔據了閘極電壓在 turn-on 之前愈來愈大的部份。藉由使用一個新穎的極淺接面離子植入技術，我們增強了電晶體效能並且降低了電晶體受到供應電壓不穩定所影響的敏感度。這應歸功於快速的開-關轉變與載子遷移率的增加。

關鍵字：源極/汲極串聯電阻，全矽化閘極，毫秒退火，通道應力，遷移率增強，
嵌入式矽鍺，矽回流，極淺接面，低供應電壓操作，

Key Process Development in Nano-scale MOSFETs Manufacturing

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ABSTRACT

The semiconductor VLSI technology is so successful that the transistor feature size and cost have been reduced exponentially with time since 1970s. Meanwhile, the transistor performance has increased constantly in the past decades and is expected to improve in the foreseeable future. The modern VLSI technology deeply relies on mechanical strain engineering, equivalent-oxide-thickness (EOT) reduction, ultra-shallow-junction (USJ) formation, and channel structure design for the purpose of boosting transistor performance and maintaining reasonable electrostatic characteristics of the short-channel transistors. In this dissertation we discussed and proposed novel methods to improve the aforementioned key process modules in an integration-friendly and cost-effective manner.

At first, a novel source/drain parasitic series resistance (R_{sd}) extraction method was proposed on the basis of carrier mobility universality. The merit of the method stems from the specifically arranged bias conditions in which the channel carrier mobility remains constant for high vertical electric fields. R_{sd} can be extracted using simple DC I-V measurements on a single test transistor

without requiring information such as gate-oxide thickness, physical gate length, or effective channel length. It is this unique property which makes this method suitable for short-channel transistors. This method was verified with extensive experimental data and then utilized to evaluate the efficacy of the propose processes in the following chapters.

A novel millisecond-annealing-assisted fully-silicide (MSA-assisted FUSI) gate formation was discussed for the first time. This unique technique utilized an MSA for nickel silicide phase transformation, leading to a highly tensile FUSI gate electrode that exerts compressive stress in the channel region. Great selectivity of FUSI-gate formation was realized by implanting nitrogen in the area where FUSI-gate was to be prevented. The proposed integration scheme is highly cost-effective as compared with the conventional FUSI-gate process, which may need chemical-mechanical-polish (CMP), polysilicon recess, and extra lithography mask layers. Significant improvement in p-type transistor driving current was thereby achieved resulting from enhanced hole mobility and the elimination of polysilicon depletion effect. Uniform FUSI-gate formation across various transistor dimensions was achieved with gate electrode feature size down to 30nm.

A novel process was proposed to modulate the distance, or proximity, between the tip of embedded silicon-germanium (e-SiGe) and the channel region in pMOSFETs. Traditionally, sophisticated etching treatment was adopted in a spacer structure; however, process-induced variation in the e-SiGe proximity may lead to serious variation in pMOSFET performance. In this dissertation, an extremely close proximity was achieved using self-aligned silicon-reflow (SASR) in hydrogen ambient. As opposed to the conventional approaches which had e-SiGe proximity determined by spacer width, the tip of e-SiGe with SASR can be positioned flush with the gate edge as corroborated by

transmission-electron-microscopy (TEM) analysis. Significant improvement in pMOSFET performance was also measured.

Enlarging gate voltage overdrive headroom is crucial to low-V_{dd} operation for nano-scale MOSFETs. We defined a new index, "V_{th_lin}-V_{th_gm}", in order to describe the on-off transition abruptness in addition to the conventionally used index, sub-threshold swing. This new index is increasingly important to the advanced nano-scale MOSFETs for low-V_{dd} and low-V_{th} operation because it comprises an increasing portion of gate voltage consumed before turn-on. By introducing a novel USJ ion implantation (I/I) technique with reduced halo I/I dose, enhanced transistor performance and low V_{dd}-sensitivity were achieved because of quick on-off transition and improved carrier mobility.

Keyword: S/D parasitic resistance, FUSI gate, millisecond annealing, channel strain, mobility enhancement, e-SiGe proximity, silicon-reflow, USJ, low-V_{dd} operation

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Having been working heart and soul in tsmc for one decade, developing transistors for the coming generations is my key focus. I deeply appreciate tsmc's economical support so that I can sustain my family while pursuing academic achievement. I see so many talented individuals in this big family. They are my paradigms to imitate in order to better myself again and again. This PhD dissertation is truly a collective work of their wisdom and professionalism. I deeply appreciate the guidance from C.C. Wu, M. Cao, Y.J. Mii throughout my PhD research. Special thanks should be given to Dr. Carlos H. Diaz for his appearance at so many of my critical moments. He is indeed my mentor in tsmc.

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僅以此論文，獻給我的家人以及來不及等我畢業的母親。

CONTENTS

Table Captions

Figure Captions

LIST OF SYMBOLS

C_d	Depletion capacitance
C_g	Gate capacitance
C_{jb}	Bulk type junction capacitance
C_{ox}	Gate dielectric capacitance
E_{eff}	Effective silicon vertical electrical field
E_{eff_ana}	Effective silicon vertical electrical field in an analytic formula
E_{eff_CV}	Effective silicon vertical electrical field extracted using split-CV measurement
G_{ds}	Output conductance
G_m	Trans-conductance
I_{boff}	Gated diode junction leakage
I_d	Darin current
I_{dlin}	MOSFET linear driving current
I_{eff}	Effective MOSFET driving current defined in [5.18]
I_{off}	MOSFET off-state current
I_{on}	MOSFET on-state driving current
J_g	Gate leakage current density
J_{g_inv}	Gate leakage current density in inversion state
L_{eff}	Effective channel length
L_{gate}	Gate length
L_{mask}	Mask gate length
N_{sub}	Substrate doping concentration
Q_d	Depletion charge
Q_i	Inversion layer charge
R_s	Sheet resistance
R_{sd}	Source/drain series resistance
T_d	Ring oscillator delay time
T_{ox}	Gate dielectric thickness
T_{ox_inv}	Gate dielectric
T_{ox_inv}	Gate oxide thickness in inversion state
$V_{bs}(V_b)$	Substrate bias voltage
V_{dd}	Applied voltage in a circuit
V_{ds} (V_d)	Drain to source voltage
V_{FB}	Flat band voltage
V_{gs} (V_g)	Gate to source voltage
V_{th}	Threshold voltage
V_{th_gm}	Threshold voltage extracted using maximum trans-conductance method
V_{th_lin}	Threshold voltage defined with a constant current criterion
W_D	Channel depletion width
W_{mask}	Mask gate width
Xj	Junction depth
Z_c	Distance between Si/SiO_2 interface and carrier centroid in the channel.
α	Bulk charge linearization coefficient

ε_{si}	Silicon permittivity
η	Empirical factor with common values of ~1/2 and ~1/3 for electrons and holes
η_{ana}	Fitting parameter that describes η in an analytic formula
μ_{eff_ana}	Carrier mobility described in an analytical formula
$\mu_{universal}$	Universal carrier mobility
Ψ_B	Surface potential

Chapter 1

Introduction

1.1 Backgrounds

Maximizing complementary metal-oxide-semiconductor field-effect transistor (CMOSFETs) density while keeping constant transistor performance improvement has been the most important task of the silicon-based very-large-scale integration (VLSI) semiconductor industry for more than half a century. Moore's law indicates that the transistor counts in a chip double every two years. This is the cornerstone of the entire IC industry and has been successfully driving the industry for more than three decades. The logic CMOSFET manufacturing technology has entered the era of nanometer scale since the beginning of this millennium [1.1-1.3]. In the last decade, the silicon MOSFET industry has undergone an amazing evolution of strain engineering, source/drain series resistance reduction, and high-K/metal gate technology [1.4-1.6]. All the efforts delivered to this industry are for the same purpose: to generate cost-effective and manufacturable process in order to sustain the constant progress of VLSI industry itself.

The basic principle of MOSFET operation doesn't change over time despite the astonishing progress of transistor scaling-down and development of novel techniques for transistor performance enhancement. The engineering toward a low source/drain series resistance (R_{sd}) has been always a key task. As the transistor gate length scales down, R_{sd} constitutes an increasing

portion of total resistance due to the reduced intrinsic channel resistance. Methods of R_{sd} extraction have been developed in the literature [1.7-1.10] in order to characterize R_{sd} and its impact on transistor performance. However, the extraction procedures in the former methods required either multiple I–V measurements over transistors with different channel lengths or sophisticated Capacitance–Voltage (C-V) measurements for short-channel transistors. In addition, the former methods [1.7] assumed constant carrier mobility for transistors with different channel lengths in the R_{sd} extraction procedure. However, these basic assumptions simply don't hold in the modern transistor design which greatly relies on mechanical strain and local doping profile engineering. In this work, we developed a new R_{sd} extraction algorithm [1.11-1.12], which is capable of extracting R_{sd} using a single transistor by measuring simple I-V characteristics. This algorithm stems from the well known behavior of constant carrier mobility in the high vertical electrical field regime. We extensively examined this algorithm and verified its validity in precisely correlating the process changes and the extracted R_{sd} values. This novel R_{sd} extraction method was applied throughout this work in order to assess the efficacy of every process improvement.

Strain engineering toward high carrier mobility for transistor performance improvement has been a major topic in the CMOSFET industry for about a decade [1.13-1.16]. The key approaches, including strained-capping layers, embedded silicon-germanium (e-SiGe) epitaxial stressor, stress-memorization-technique (SMT), etc., have been widely adopted in the mainstream VLSI technology (as shown in Fig. 1.1). These stressors provide mechanical strain from both intrinsic and extrinsic

components of the transistors. However, the space of implementing these stressors decreases as the transistor size keeps shrinking. As a result, the efficacy of stressors keeps decreasing. In the near future, aggressive strain engineering is therefore indispensible to continue the trend of carrier mobility enhancement in order to sustain the required transistor performance in the coming generations. Out of the various strain technologies, fully-silicided (FUSI) gate [1.17-1.19] is one of the most promising approaches due to the fact that the spatial ratio of the gate area over the channel area in transistors would not decrease as transistor size shrinks. Furthermore, being a stressor, gate material can be placed extremely close to the channel region because there is merely a thin dielectric layer in between them. Unlike the conventional stressors, such as extrinsic capping layers, strained gate material shows obvious advantage in the coming generations. A novel FUSI gate formation method was proposed in this work by using milli-second annealing (MSA) at a high temperature but in a short period of thermal anneal for nickel silicide phase transformation [1.20]. This technology not only significantly benefits carrier mobility but also eliminates poly-depletion effect by converting the gate material from doped poly-silicon to strained metal silicide.

Selective e-SiGe source/drain was for the first time implemented in the 90nm manufacturing VLSI technology [1.21]. PMOSFETs performance showed a drastic improvement because of the incorporation of uniaxial compressive strain as well as a reduced R_{sd}. This was a triumph in the manufacturing VLSI technology. In the following generations, e-SiGe has been further developed [1.22-1.25] for a variety of shapes and a higher

germanium concentration in order to increase the compressive strain in the channel region. The distance between tip of e-SiGe and the channel region, i.e. proximity, always plays a key role in the strain efficacy. As shown in Fig. 1.2, the e-SiGe tips get closer and closer to the gate edge as technology evolves. Close proximity would lead to a higher strain in the channel region but potentially worsen short–channel-effect (SCE). Many approaches [1.26-1.28] have been given to reduce the e-SiGe proximity as well as to push the tip of e-SiGe toward channel surface. Close e-SiGe proximity can raise the strain level while a shallow tip provides high immunity against SCE degradation. Nevertheless, these approaches often depend on sophisticated etching processes which lead to small process margin and considerable process variation. In order to position the e-SiGe tip right at the channel edge, we proposed a cost-effective method featuring self-aligned silicon reflow (SASR) [1.29]. This technique is able to achieve an extreme e-SiGe surface proximity without degrading process variation because the shape of e-SiGe is defined in a self-aligned manner. The etching process induced variation can be mitigated after silicon reflow while a close surface e-SiGe proximity is realized simultaneously. Significantly better transistor performance is therefore experimentally achieved as a result of high hole mobility and low R_{sd}. In addition, SASR is able to provide tighter distributions of on-state current and R_{sd} due to a self-aligned e-SiGe tip. This technique is especially appropriate to the coming generations of VLSI technology in which process variation will become more and more serious due to the scaling-down of transistor feature size.

Ultra-shallow-junction (USJ) formation is another key enabler of the

transistor scaling-down. The source/drain junction depth (X_j) must shrink accordingly as the gate length shrinks in order to maintain an acceptable electrostatic control in the short channel transistors. Meanwhile, the sheet-resistance (R_s) must reduce in order to reduce Rsd from one generation to another. Ion implantation followed by a high temperature thermal annealing has been adopted [1.30-1.32] to repair the silicon lattice damage and to activate implanted doping species. Within the last two decades, ultra low energy ion implantation with a subsequent rapid-thermal-annealing (RTA) has become the standard process in the VLSI technology. The low energy ion implantation guarantees that the projected doping species are located in the vicinity of surface while the following RTA can prevent too much doping diffusion and activate the doping species. In the sub-100nm technology nodes, the USJ formation is extremely demanding. Simple ion implantation followed by RTA can not achieve the required doping abruptness and shallow junction depth. Doping species suffer from transient-enhanced-diffusion (TED) upon thermal annealing [1.33-1.35] and result in a greatly diffused doping profile due to the fast dopant-defect pair diffusion. TED ruins the possibility of using conventional methods to accomplish the required USJ criteria in the nanometer scale transistors. In addition, these dopant-defect pairs/clusters are electrically inactive so that the doping activation level cannot be further improved. Many approaches were proposed in the publications [1.36-1.38] for the purpose of suppressing TED by engineering the implantation-induced crystalline defects. Pre-amorphization implantation (PAI) by heavy electrically inactive species is widely used to prevent the ion channeling effect [1.39] during the implantation process and to separate the end-of-range (EOR)

defects from the wanted doping species by locating the doping species inside the amorphous region. However, this approach can induce serious side effects such as leaving a defect-rich layer below the amorphous/crystal (A/C) interface after RTA. Serious junction leakage was therefore often observed. Furthermore, those defects can be the source for the TED of the pre-existing doping species. Recently, co-implantation (co-IMP) has also been intensively studied and applied to the manufacturing technology [1.40-1.42]. The concept of co-IMP is using another species (such as carbon, fluorine, and nitrogen) to interact with crystalline defects in order to keep them immobile by clustering the defects and/or to release the counter defects (interstitial to compensate vacancy and vice versa) in order to reduce the mobile defect concentration upon the following annealing process. Therefore, the focused doping species is less likely to be impacted by TED. However, the co-IMP species and the defect clusters may lead to unacceptable junction leakage. In this work, we proposed a new concept of doping technique featuring fast PAI using light species. Because of a high implantation dose rate, the defects in the substrate are generated and accumulated efficiently [1.43-1.44]. The crystalline defects generated by light implanted species at low energy are dominated by point defects which can be easily recovered upon the following thermal annealing. Both less TED and higher doping activation level are expected by reducing the residual crystalline defects. By implementing this concept in the source/drain extension (S/D-ext), we experimentally demonstrated a significant improvement in the R_s-X_j performance. Because of less residual defects in the EOR region resulting from S/D-ext ion implantation, the halo doping species become more confined (less TED) and show a higher

dose-efficiency. The transistor's electrical behavior clearly reflects the advantage of this new doping technique. Shallow S/D-ext combining an abrupt halo doping profile, fast turn-on/turn-off transition is one consequence. This characteristic is particularly important to the low supply-voltage (V_{dd}) operation in which the on/off transition consumes a considerable portion of gate voltage.

1.2 Organization of the Dissertation

After the introduction given in Chapter 1, Chapter 2 describes a novel R_{sd} extraction method. Starting from the theoretical study, the basic model setup, the experimental data analysis, to the TCAD verification, a self-consistent algorithm is established. This algorithm was then examined in various cases in order to prove its capability. It was used throughout this work to give accurate assessment on all the experiments.

A series of novel approaches for the purpose of improving transistor performance were given consecutively. At first, Chapter 3 introduces an integration-friendly method of FUSI gate electrode formation by using milli-second-annealing. We discussed the process window of selectively forming FUSI gate on PMOSFET and characterized the stress level of nickel-silicide under a desired crystalline phase. The elimination of poly depletion effect and silicide-induced mechanical strain were carefully discussed.

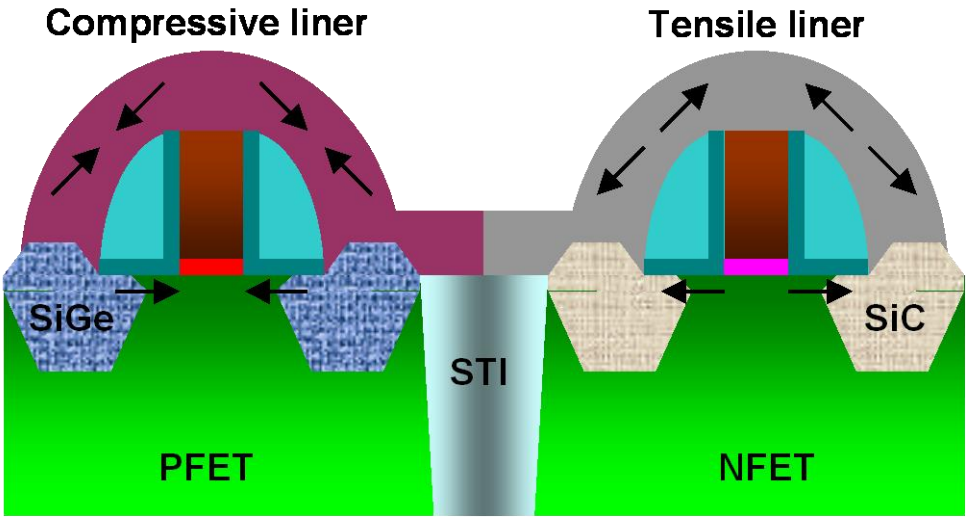
Chapter 4 proposes a new hydrogen-annealing technique to push the e-SiGe proximity flush with the gate edge in a self-aligned manner. The advantage of this self-aligned technique was statistically demonstrated in terms of process

control. The benefit on strain engineering and R_{sd} reduction resulting from the extremely close e-SiGe proximity was corroborated by both the TEM analyses and TCAD simulation.

Chapter 5, at first, introduces a novel USJ doping technique featuring fast PAI with light species. Significant improvement in R_s-X_j performance was achieved and the mechanism was then conceptually discussed. Secondly, we discussed the fast turn-on/turn-off transition resulting from this novel doping technique. The benefits in DC, AC, and ring-oscillator speed were addressed. We also proved the advantage of this doping technique for low-V_{dd} application as compared to the conventional ion implantation doping technique.

Finally in Chapter 6, we summarize the contribution of this work and propose our suggestions to the further works.

(a)



(b)

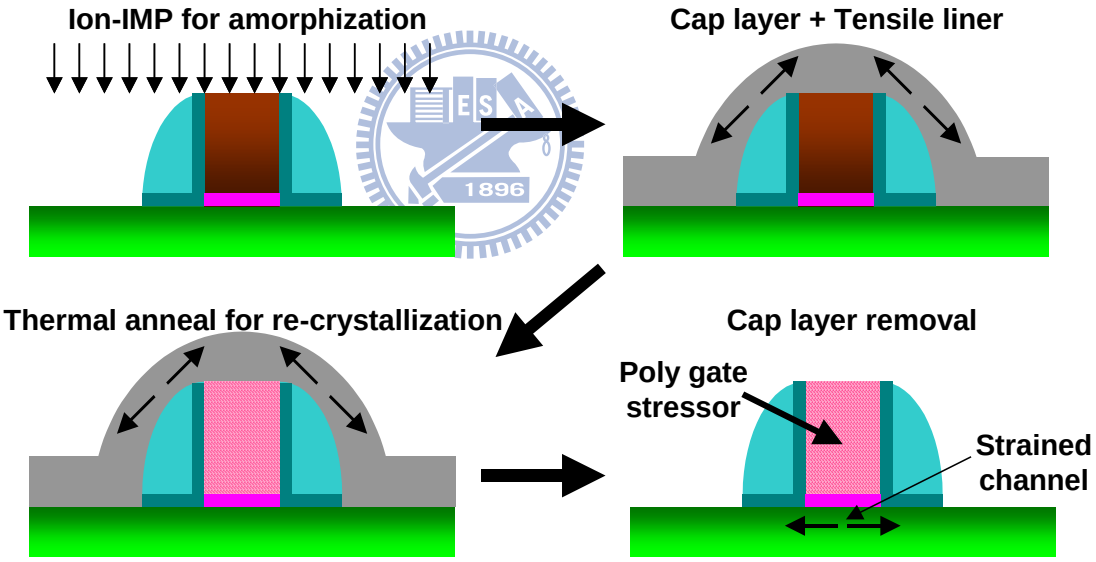


Fig. 1.1(a) Schematic plots of the frequently used stressors in the MOSFET VLSI technology.

Fig. 1.1(b) A standard stress-memorization-technique (SMT) process flow.

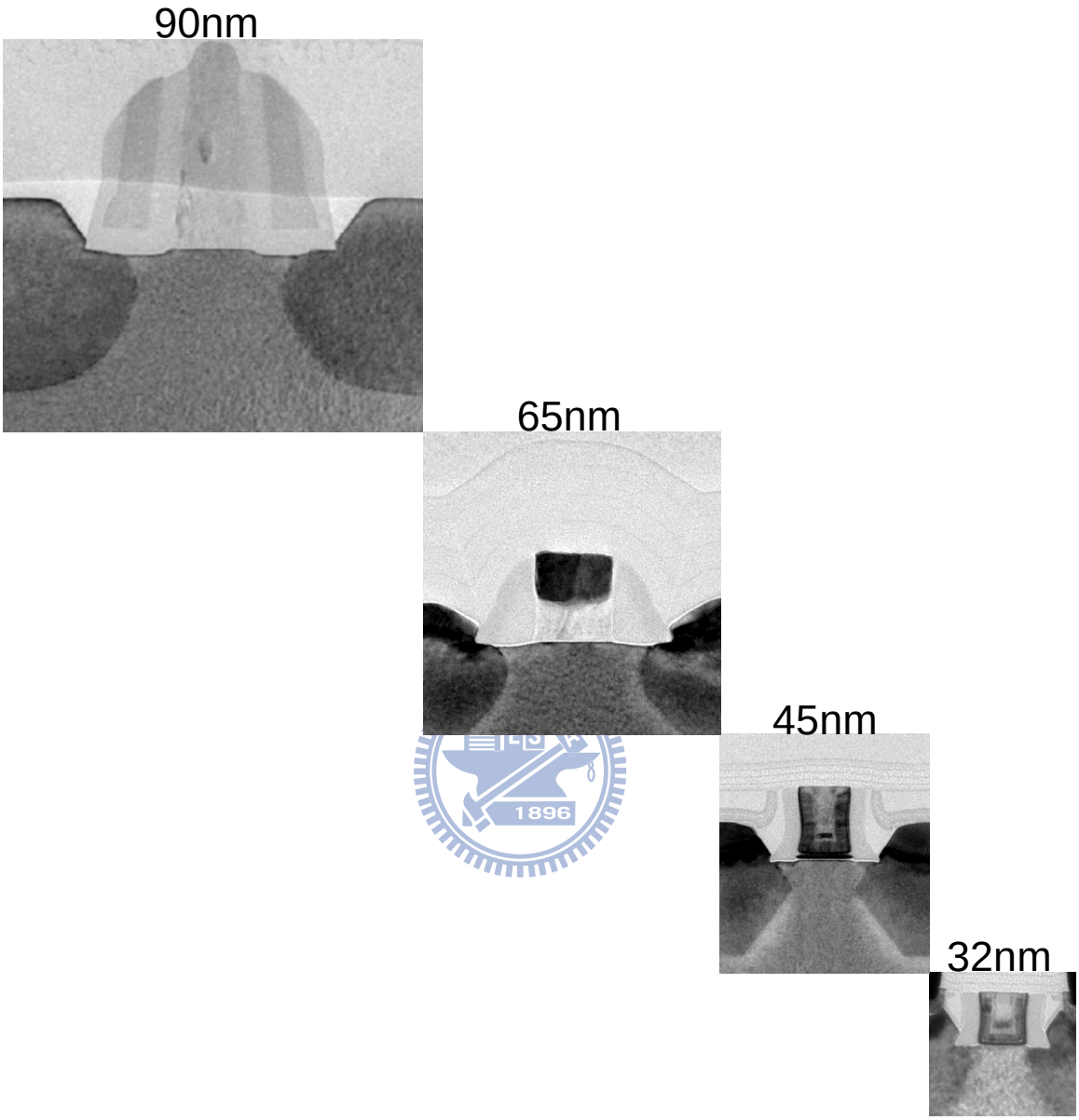


Fig. 1.2 VLSI industry's e-SiGe structures of 90nm [1.21], 65nm [1.22], 45nm [1.23], and 32nm [1.26] technologies. The e-SiGe tips get increasingly close to the gate edge.

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Chapter 2

Methodology of R_{sd} Characterization: A Novel Method of MOSFET Series Resistance Extraction Featuring Constant Mobility Criteria and Mobility Universality

2.1 Preface

MOSFET source/drain series resistance (R_{sd}), as shown in Fig. 2.1, leads to a voltage drop within source and drain diffusion regions, reducing the voltage across the intrinsic device and degrading drive capability. It constitutes an increasing portion of total resistance as gate length (L_{gate}) shrinks due to reduced intrinsic channel resistance. Hence, the degradation of drive current becomes most serious in short channel devices. In IC technology development, R_{sd} extraction remains one of the most critical tasks during the device characterization and simulation. Many R_{sd} extraction methods [1]-[3] have one assumption in common: both the channel dopant concentration and carrier mobility are independent of L_{gate}. However, the significance of the halo ion implantation and mechanical-stress-dependent dopant diffusion [4] as encountered in modern MOSFETs renders this model inadequate. Recently, a constant mobility criterion in the high surface electrical field regime was proposed [5], which can not only considerably improve R_{sd} extraction precision but also eliminate the disadvantages of conventional methods [1]-[2] & [6] such as requiring multiple I-V measurements over different channel

lengths and/or sophisticated C-V measurements for short channel devices.

Contrary to the drain current model used in the literature [1]-[3], [5]-[6], a bulk charge linearization coefficient (α) is adopted in this work. This leads to a cancellation of the debiasing effect and the threshold voltage change induced by IR-drop. Hence, an exact and compact drain current formulation results. In addition, a self-consistent algorithm is established by combining the constant mobility criterion [5] and an updated method of effective surface electrical field (E_{eff}) extraction. In contrast to [5] which uses a constant η in the analytic expression of E_{eff}, this empirical factor is treated as a fitting parameter (η_{ana}) in this work. The values of R_{sd} and η_{ana} are determined by using an iterative procedure. With the constant mobility criterion taken into account, the R_{sd} can be more accurately extracted for a certain short channel device by matching the shape of its universal mobility curve with that of a long channel device. The procedure is conducted without requiring knowledge of the effective channel length (L_{eff}), substrate doping concentration (N_{sub}), or channel stress. With this unique feature in mind, the proposed method is particularly suitable for the short channel devices for which unambiguous definition of L_{eff} is often hard to make. Reasonable values of extracted R_{sd} are successfully demonstrated in a wide range of gate lengths. The validity of the constant mobility criterion is addressed as well.

The device samples used in this work are fabricated using a 40nm-low-power process technology. This technology features abrupt and heavily doped ultra shallow junction for source/drain extensions (SDE). Millisecond annealing is implemented to enhance dopant activation level. Aggressive strain engineering is used to boost device performance.

2.2 Universal Mobility and Analytic E_{eff} with η_{ana} as a Fitting Parameter

The universality of carrier mobility in the high electrical field regime is demonstrated in Fig. 2.2 for a long channel MOSFET. The effective silicon vertical electrical field (E_{eff}) at the SiO_2/Si interface can be expressed as a function of the depletion charge (Q_d) and inversion layer charge (Q_i). The charge components Q_d and Q_i can be obtained via split C-V measurements [7], [8]. The E_{eff} formula can read as

$$E_{eff\_CV} = \frac{1}{\varepsilon_{Si}}\left(|Q_d| + \eta |Q_i|\right) \tag{2.1}$$

where ε_{si} is the silicon permittivity and η is an empirical factor with common values of ~1/2 and ~1/3 for electrons and holes at room temperature, respectively [9]-[13]. Note that in this work η, which is the reciprocal of that in [5], follows the convention in existing publications [9]-[13]. In order to obtain accurate carrier mobility, split C-V and I-V measurements are performed on a long channel MOSFET in which fringing capacitance and R_{sd} are insignificant as compared with intrinsic gate capacitance and channel resistance, respectively. As shown in Fig. 2.2, under various back bias (V_{bs}) conditions, carrier mobility appears to converge toward a universal carrier mobility ($\mu_{universal}$) curve in the high E_{eff} region. This means that if the device is operated in the high E_{eff} region, a constant mobility is achieved at a given E_{eff}, regardless of the varying impurity scattering element. At sufficiently high E_{eff}, carrier mobility is well described by [14]-[16]:

$$\mu_{universal} = \frac{\mu_0}{1 + (E_{eff}/E_0)^{\nu}} \tag{2.2}$$

where μ_0, E_0 and ν are process-specific constants. Best fitting result, also shown in Fig. 2.2, is obtained with μ_0 = 720 cm2/V-s, E_0 = 0.82 MV/cm and ν =1.63 for the long channel device used in this work.

To further investigate Eq. (2.1), it is transformed into an analytical form:

$$E_{eff\_ana} = \frac{V_{gs} + (\frac{1}{\eta_{ana}} - 1)V_{th} - \frac{1}{\eta_{ana}}V_{FB} - \frac{2}{\eta_{ana}}\psi_B}{\frac{3}{\eta_{ana}}T_{OX}} \tag{2.3}$$

The parameters associated with Eq. (2.3) have the usual meanings [5]. The threshold voltage V_{th} in Eq. (2.3) is extracted using maximum transconductance method under a low drain bias (25mV) ensuring a linear operation mode. In the derivation of Eq. (2.3), a constant N_{sub} is presumed. However, aggressive engineering of channel doping profile, such as retrograded channel and/or heavy halo ion implantation, is commonly used in modern MOSFETs. In addition, non-uniform doping profile caused by mechanical-stress-dependent diffusion is also evident. These factors make the constant N_{sub} assumption problematic and a specific treatment is needed.

In this work, η_{ana} in the analytic expression Eq. (2.3) is treated as a fitting parameter in order to accommodate the error introduced by the constant N_{sub} assumption as mentioned above. Similar to the method described in [15], the E_{eff_ana} values acquired through Eq. (2.3) are compared to those of split C-V method. A long channel NMOSFET (L_{mask}=W_{mask}=1μm) is used to examine the consistency between the two methods. One should note that the value of η

used for split C-V is set at 1/2 for NMOSFETs fabricated on wafers with (100) surface orientation. As shown in Fig. 2.3, in order to match the E_{eff} values between both methods, η_{ana} = 1/1.7, instead of 1/2, is suggested when applying the analytic expression, Eq. (2.3).

2.3 R_{sd} Extraction Methodology: Constant Mobility Criterion

The R_{sd} extraction method based on a constant mobility criterion is firstly described in [5]. Here, to testify to the validity of the constant mobility criterion, an extra parameter is introduced: the bulk charge linearization coefficient denoted as α. First of all, for the intrinsic MOSFET (Fig. 2.1) operated in linear region, drain current can be expressed as [17], [18]

$$I_d = \frac{C_{ox} W_{eff} \mu}{L_{eff}} (V_{gs}' - V_{th}' - \frac{\alpha}{2} V_{ds}') V_{ds}' \tag{2.4}$$

where $V_{th'} = V_{th} - (\alpha - 1)V_{bs'}$ and $V_{bs'} = -R_s I_d$. V_{th} is the threshold voltage measured without IR-drop on the source side. Under the assumption of $R_s = R_d = R_{sd}/2$ for a symmetric MOSFET and to account for the debiasing effect at the terminals, Eq. (2.4) can be expressed in terms of the externally applied voltages:

$$\begin{aligned} I_d &= \frac{C_{ox} W_{eff} \mu}{L_{eff}} \left[(V_{gs} - \frac{R_{sd}}{2} I_d) - (V_{th} + (\alpha - 1)\frac{R_{sd}}{2} I_d) - \frac{\alpha}{2}(V_{ds} - R_{sd} I_d) \right] (V_{ds} - R_{sd} I_d) \\ &= \frac{C_{ox} W_{eff} \mu}{L_{eff}} (V_{gs} - V_{th} - \frac{\alpha}{2} V_{ds})(V_{ds} - R_{sd} I_d) \end{aligned} \tag{2.5}$$

The above derivation process clearly demonstrates that cancellation of the debiasing effect and the threshold voltage change induced by IR-drop

takes place. As a result, the term in the first parentheses of Eq. (2.5) reduces to (V_{gs}-V_{th}- α V_{ds}/2), thus constituting an exact and simple formulation for the drain current. By incorporating the criterion described in [5], a constant mobility can be achieved at two sets of bias conditions: ($V_{gs}^{(1)}$, $V_{th}^{(1)}$) and ($V_{gs}^{(2)}$, $V_{th}^{(2)}$) where $V_{gs}^{(2)} = V_{gs}^{(1)} + (1/\eta_{ana}-1)(V_{th}^{(1)}-V_{th}^{(2)})$. Again using the same derivation procedure in [5] with the incorporation of α, series resistance can be written as

$$R_{sd} = \left(\frac{B}{I_d^{(2)}} - \frac{A}{I_d^{(1)}}\right)\frac{\eta_{ana} V_{ds}}{(V_{th}^{(1)} - V_{th}^{(2)})} \tag{2.6}$$

where $A = V_{gs}^{(1)} - V_{th}^{(1)} - 0.5\,\alpha V_{ds}$ and $B = V_{gs}^{(1)} + (1/\eta_{ana}-1)V_{th}^{(1)} - V_{th}^{(2)}/\eta_{ana} - 0.5\,\alpha V_{ds}$.

The expression of R_{sd}, Eq. (2.6), shows no dependency on C_{ox}, L_{eff} and W_{eff}. Therefore, this method is especially suitable for modern MOSFET with small geometries in which accurate measurements of C_{ox}, L_{eff} and W_{eff} are hard to achieve.

For a modern MOSFET with thin gate oxide, α is close to 1, as will be explained later. In the following discussion, α is presumed as 1 and the error caused by this assumption will be further examined.

2.4 Algorithm of Self-consistent R_{sd} and η_{ana} Calculation

As device feature size shrinks, fringing capacitance and R_{sd} become no longer negligible. It is difficult to extract carrier mobility and E_{eff_CV} by using simple split C-V and I-V measurement. Thus, at small feature sizes, analytical derivations for μ and E_{eff} become necessary. Once R_{sd} has been extracted by

using Eq. (2.6), an analytical expression of mobility, μ_{ana}, can be written as

$$\mu_{ana} = \frac{L_{eff}}{W_{eff} C_{ox}} \frac{I_d}{(V_{gs} - V_{th} - \frac{\alpha}{2} V_{ds})(V_{ds} - R_{sd} I_d)} \quad (2.7)$$

Because R_{sd} is a function of η_{ana} as described in Eq. (2.6), μ_{ana} is consequently also a function of η_{ana}. For a given η_{ana}, corresponding E_{eff_ana}, R_{sd} and μ_{ana} are generated analytically. Moreover, a series of E_{eff_ana} and μ_{ana} can be defined for bias conditions in the vicinity of the specific V_{gs} where R_{sd} is extracted. It is worth noting that V_{gs} should be sufficiently high as mentioned in Section 2.3 In a sense, V_{gs} of ~2.5V is typically used in this work.

Process-induced strain and intensive strain engineering are pervasive in modern MOSFETs. These may lead to significant variability in carrier mobility [19]-[22] and changes to μ-E_{eff} behavior. The difference in μ-E_{eff} behavior in high E_{eff} regime between strained and unstrained MOSFETs approaches a constant ratio as mentioned in the literature [16], [23]-[25]. This implies that only μ_0 in Eq. (2.2) is sensitive to strain engineering in the high E_{eff} regime. Consequently, the μ-E_{eff} behavior in high E_{eff} regime extracted using long channel MOSFETs is valid for shorter channel devices by simply modifying it with a constant ratio. μ_0 is therefore regarded as a fitting parameter for shorter channel MOSFETs in this work. In addition, determining L_{eff} for short channel MOSFETs remains one of the most challenging issues in the industry. Without explicitly assigning a value to L_{eff}, mask gate length (L_{mask}) is used in this work. The difference between L_{mask} and L_{eff} of a given short channel MOSFETs is also absorbed by μ_0. As shown in Eq. (2.6), no information about L_{eff} is necessary for R_{sd} extraction as mentioned in Section 2.3. Therefore, the ambiguous definition of L_{eff} does not lead to

erroneous R_{sd} extraction [5]. In the vicinity of the V_{gs} where R_{sd} is extracted, μ_0 is a fitting parameter accounting for the difference introduced by long channel to short channel mobility shift and also the constant ratio between L_{eff} and L_{mask} of a given shorter channel MOSFET. As shown in Fig. 2.4(a) and Fig. 2.4(b), μ_0 dominates the magnitude of $\mu_{universal}$-E_{eff} behavior while η_{ana} changes the slope of μ_{ana}-E_{eff} for a shorter channel device in which significant effects from strain engineering may take place. The most important task in this work is to determine a set of η_{ana} and μ_0 which minimizes the difference between μ_{ana} and $\mu_{universal}$.

An iterative method to determine R_{sd}, η_{ana} and μ_0 is detailed in Fig. 2.5(a). For a given η_{ana}, the summation of the square of the difference between μ_{ana} and $\mu_{universal}$ at each E_{eff} with modified μ_0 is plotted in Fig. 2.5(b). By using the MOSFET with 0.5μm gate length as an example, it is obvious that a minimum exists at η_{ana} = 1/1.7 (~0.59). This is consistent with the value obtained in Section 2.2 which exhibits a good correlation between E_{eff_CV} and E_{eff_ana}. For state-of-the-art MOSFETs, localized doping profiles introduced by halo ion implantation from both source and drain side are not strongly overlapped for gate length longer than 100nm. As a result, the substrate doping profile should not change significantly for the MOSFETs with gate length longer than 100nm. A consistent value of η_{ana} is therefore extracted by using the analytical method described in Section 2.2 and by using the iteration introduced in this section for devices having similar substrate doping profiles.

2.5 Experimental Results

The algorithm introduced in Section 2.4 has been applied to a series of

test devices and the extracted R_{sd} values are shown in Fig. 2.6(a). Similar R_{sd} values are observed for long channel devices and short channel devices. This result is expected because all devices are located on a single wafer and share the same process conditions. Please note that the drain currents have been normalized to device channel width. Therefore, the unit of R_{sd} is shown in ohm-μm. As also shown in Fig. 2.6(a), μ_0 increases as L_{mask} shrinks from 1 μm and reaches a peak at 0.1~0.2μm. Below 0.1μm, μ_0 decreases. This implies the effects of strain engineering in these devices are more pronounced at L_{mask} values around 0.1~0.2μm. The root cause of the decreasing μ_0 needs more theoretical study.

The gate length dependency of η_{ana} is shown in Fig. 2.6(b). It stays at a constant value for gate length longer than 0.1μm and starts to roll off gradually for shorter gate lengths. As gate length shrinks, substrate doping concentration changes because of overlap of halo ion implantation from the source and drain sides. Consequently, the value of η_{ana} may deviate from that of the long channel devices. In addition, η_{ana} itself is also a function of sub-band occupancy [26]. When gate length shrinks, two-dimensional charge sharing from source and drain junctions leads to a reduction in charge confinement in the channel region [27], [28]. This reduction in confinement reduces the sub-band separation. As a result, η decreases due to higher probability of carriers occupying high level sub-bands [26]. The trend of decreasing η_{ana} with decreasing gate length supports this argument.

In this section, a self-consistent algorithm has been successfully demonstrated for the extraction of R_{sd} from long channel to sub-100nm devices. The extracted R_{sd} shows weak dependency on gate length. The

reason for the gate length dependence of each parameter has also been proposed and discussed. This algorithm can be easily implemented with aforementioned analytical equations, and no C-V measurement for short channel devices is required. These features avoid unnecessary error caused by fringing capacitance and therefore result in an accurately extracted R_{sd}.

2.6 Discussion

(a) TCAD as Corroborating Evidence

Based on calibrated Tsuprem and Medici [29] (also used in [4] and [5]), the net doping concentration near the gate edge of a typical NMOSFET (L_{mask} = 0.1μm) used in this work is shown in Fig. 2.7(a). In a state-of-the-art MOSFET, the doping concentration inside the SDE region is higher than 10^{20} cm^{-3}. It takes only several nanometers to change the doping polarity in the transition region from SDE to channel (lateral transition) and SDE to substrate (vertical transition). Fig. 2.7(b) illustrates the electron concentration on the drain side along the lateral direction A-A′ defined in Fig. 2.7(a). Over a wide range of bias conditions, V_{gs} shows little effect on modulating the electron concentration inside highly doped SDE region, while the modulation of carrier concentration in the channel region is obvious. In addition, the current flow in SDE is mainly located in a region where the carrier concentration is insensitive to V_{bs} as shown in Fig. 2.7(c) which is plotted along vertical direction B-B′ defined in Fig. 2.7(a). It is obvious that the applied bias shows little effect on modulating both the carrier concentration and current flow inside the highly doped SDE region. Therefore, the R_{sd} values extracted under high V_{gs} and high V_{bs} bias conditions well represent the R_{sd} values under

regular operating bias conditions for devices with highly doped and abrupt SDE.

On the other hand, when the carrier concentration is lower than a critical value ($4x10^{19}$ cm^{-3} for the device used in this work based on TCAD simulation), it is sensitive to V_{gs} bias conditions as shown in Fig. 2.7(b). R_{sd} should comprise the regions (on both source and drain sides) where electrical conductivity is V_{gs}-independent. Therefore, R_{sd} can be estimated by subtracting the V_{gs}-dependent resistance from total resistance: $R_{sd} = V_{ds}/I_d - \Delta V_c/I_d$, where ΔV_c is the potential-drop ($V_{c\_drain} - V_{c\_source}$) between two characteristic points where the carrier concentration meets the critical value at drain side and source side. Based on this method, R_{sd} values are calculated under various bias conditions and the results are summarized in the inset of Fig. 2.7(b). The R_{sd} values obtained by using this simulation study are reasonably consistent with the extracted R_{sd} values shown in Section 2.5.

Since the surface potential is modulated by V_{bs}, the centroid of the carrier distribution (Z_c) changes accordingly due to the quantum mechanical confinement [30]-[32]. One may challenge the change in Z_c would impact T_{ox_inv} under different V_{bs} and in turn impact the accuracy of extracted R_{sd}. In order to clarify this issue, we used TCAD simulation to check the carrier distribution under different V_{bs}. Fig. 2.8 illustrates the inversion-layer carrier distribution normal to the channel surface. As V_{bs} changes from 0V to -1.5V, Z_c decreases by ~0.1nm which is equivalent to ~0.03nm change in the T_{ox_inv}. This difference is no more than 1.5% for the aggressively scaled gate dielectric thickness down to 2nm. This effect on the extracted R_{sd} is therefore negligible.

(b) On the Bulk Charge Linearization Coefficient α

Bulk charge linearization coefficient (α) is treated as unity in previous sections. The error caused by this assumption is discussed in this section. By definition, $\alpha = 1 + 3T_{ox\_inv}/W_D$ [17], where W_D is the channel depletion width. Based on TCAD simulation, W_D is about 43nm for a 0.1μm-L_{mask} NMOSFET operated in the linear region (V_{gs}=1.5V~2.5V, V_{ds}=0.05V and V_{bs}=0V) as shown in Fig. 2.8(a). W_D is much thicker as compared to T_{ox_inv} which is 2.4nm in this work. As a result, the value of α is 1.17 under this bias condition. When a negative V_{bs} is applied, the value of α further decreases because W_D further increases. A table of values of α under different bias conditions is shown in the inset of Fig. 2.9(a). As shown in Fig. 2.9(b), the impact of different values of α, from 1 to 1.4, on the extracted R_{sd} is minor. The assumption of "α = 1" is therefore adequate for the proposed R_{sd} extraction method.

(c) Experimental Verification

In this work, 40nm technology low power devices featuring 17.5Å (EOT) gate oxide and heavily doped source/drain extensions were utilized to verify our R_{sd} extraction algorithm. The devices underwent advanced strain engineering including a neutral STI gap-fill process, stress memorization technique (SMT) [2.21] and tensile contact etch stop layer. A millisecond annealing process was also employed to improve device performance.

Experimental demonstration of R_{sd} extraction with L_{mask} of 100nm is presented here. In order to obtain constant carrier mobility under different bias conditions, a sufficiently high E_{eff} (high V_{gs}) is necessary to force the carrier mobility to converge toward the universal curve. When E_{eff} is insufficiently high, the carrier mobility does not converge even under the same E_{eff}. The extracted R_{sd}, as displayed in the low E_{eff} region in Fig. 2.10,

shows anomalous values as well as a strong dependency on the V_{bs} bias. This undesired result is due to the failure of the constant mobility conditions. As we further increase E_{eff}, the electron mobility begins to converge toward the universal curve. Consequently, the extracted R_{sd} values approach a constant and no dependency on the V_{bs} bias can be observed, as shown in the high E_{eff} region in Fig. 2.10. In this work, the gate current is at least six orders of magnitude lower than the drain current under all bias conditions because the tunneling current is limited by the gate area of a short channel device. Hence, the gate current has a negligible effect on the R_{sd} extraction.

The proposed method has also been applied to both NMOSFETs and PMOSFETs. The table inserted in Fig. 2.10 lists some of the extracted R_{sd} values. Also shown for comparison are those extracted from a considerable number of devices using BSIM simulation [2.33]. A reasonable agreement is achieved between the two methods.

In Fig. 2.11, an obvious degradation in driving capability is observed when external resistors are additionally connected to the device under test. R_{sd}, including these external resistors, are extracted using the proposed method. A SPICE model is calibrated using the extracted R_{sd} in the case of "R_{ext} = 0". The SPICE simulation results match the measurement in this case. The quality of the SPICE model is therefore verified. Without further modifying any SPICE model parameters, the simulated data reasonably match the measurement in both cases of "$2R_{ext}$ = 102Ω" and "$2R_{ext}$ = 200Ω". Obviously, R_{sd} and R_{ext} are additive to each other. Hence, any difference in R_{sd} caused by process change can be extracted by this proposed method. The total R_{sd} values faithfully reflect the presence of the external resistors as shown in

the inserted table of Fig. 2.11. Therefore, this proposed method is well qualified.

2.7 Applications

(a) NMOSFET Poly-Space-Effect (PSE)

This extraction method was applied to the analysis of R_{sd} variations arising from poly-space (PS) changes. Fig. 2.12(a) schematically illustrates the device layout showing different PS. It is well known that silicide/silicon interfacial resistance plays a key role in the total R_{sd} values [2.34]. As PS increases, the silicided area enlarges and hence a lower R_{sd} is expected. An apparent reduction in the NMOSFET R_{sd} is observed by increasing PS from 0.14μm to 0.32μm. No obvious reduction is observed by further increasing PS to 0.68μm and beyond as shown in Fig. 2.12(b). We believe that the silicide/silicon interfacial resistance is no longer the bottleneck of current flow as PS >=0.32μm. Therefore, enlarging PS doesn't further decrease R_{sd} as PS >=0.32μm. The I_{ON}-I_{OFF} performance is well correlated with the R_{sd} change as shown in Fig. 2.12(c).

(b) PMOSFET R_{sd} Degradation due to Silicide PAI

A pre-amorphization-implantation (PAI) is frequently utilized to improve silicide formation in terms of silicide thickness uniformity and silicide/silicon interface roughness. A brief process flow is shown in Fig. 2.13(a). Without deliberately manipulating the crystal defects introduced by PAI, R_{sd} degrades seriously as shown in Fig. 2.13(b). This results in a severe I_{ON}-I_{OFF} degradation as shown in Fig. 2.13(c). The degraded I_{ON}-I_{OFF} can be recovered by using a thermal annealing process. A clear correlation between

I_{ON}-I_{OFF} performance and R_{sd} is verified using this R_{sd} extraction method.

2.8 Conclusion

R_{sd} extraction is realized by using a self-consistent algorithm combining the constant mobility criterion and an updated analytic calculation of the effective surface electrical field. By matching the shape of universal mobility curves of short channel and long channel devices using an iterative procedure, reasonable R_{sd} values have been obtained for a wide range of gate lengths without requiring information about L_{eff}, C_{ox} and W_{eff}. Even in the presence of process variation-induced uncertainty, the proposed method has proved promising for short channel devices with heavily doped SDE.

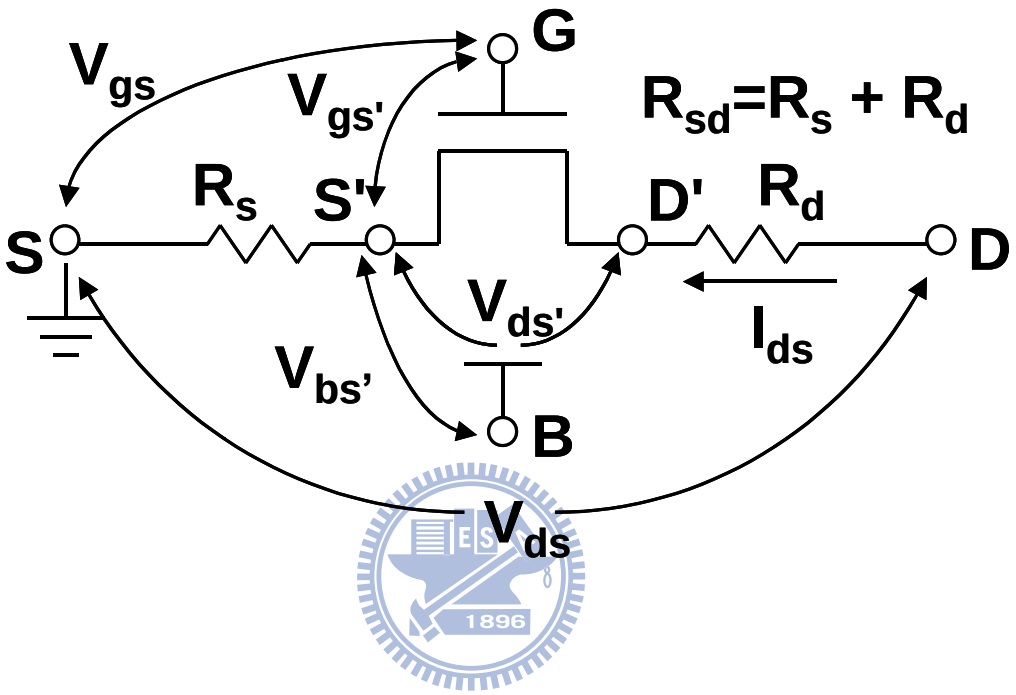


Fig. 2.1 Schematic illustration of the equivalent circuit of the device used in R_{sd} extraction.

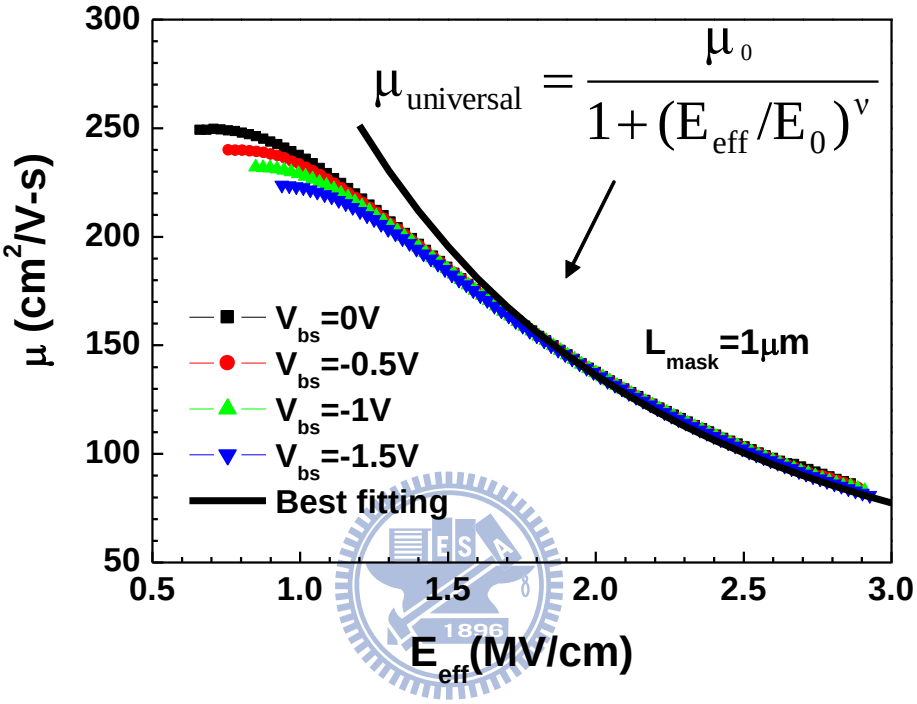


Fig. 2.2 Measured inversion carrier mobility (μ) vs. effective surface electric field (E_{eff}) under different V_{bs} bias conditions of a long channel NMOSFET. The inversion carrier mobility converges to the same trend when E_{eff} is sufficiently high. The curve of "best-fitting" is obtained with μ_0 = 720 cm^2/V-s, E_0 = 0.82 MV/cm and ν =1.63 for the long channel device used in this work.

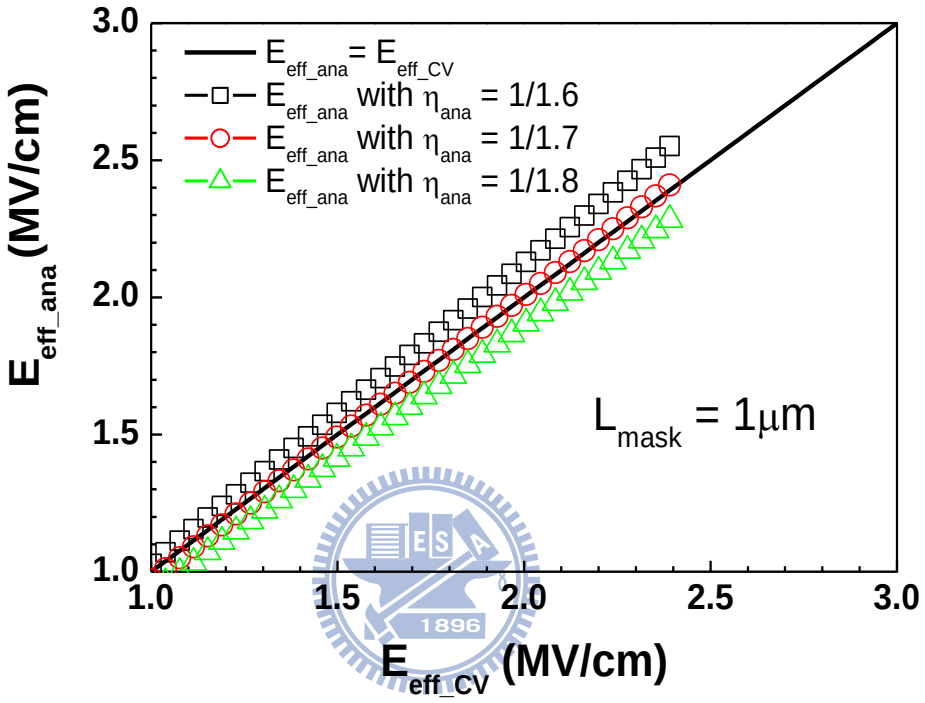
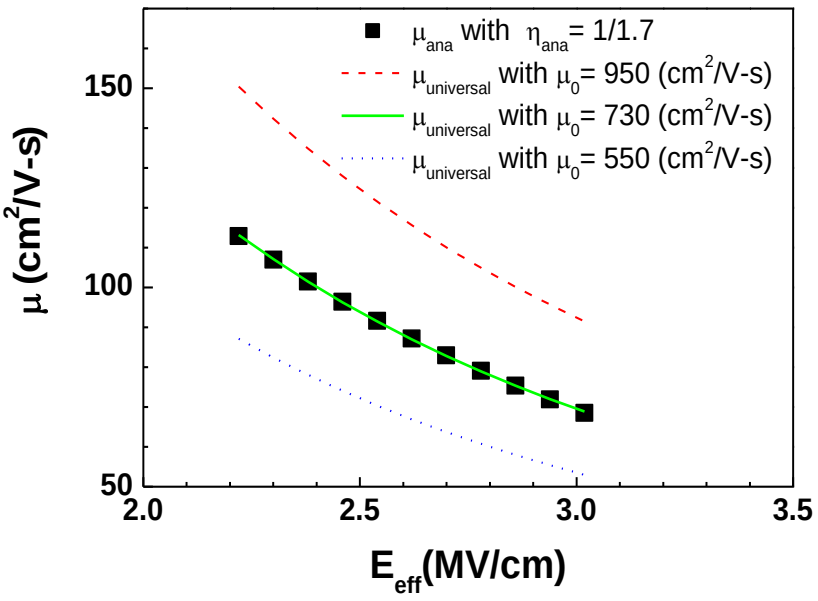


Fig. 2.3 Comparison between the effective surface electric field obtained from analytical equation (E_{eff_ana}) and split C-V measurement ($E_{eff\_C\text{-}V}$). η_{ana}=1/1.7 provides the best fitting result.

(a)



(b)

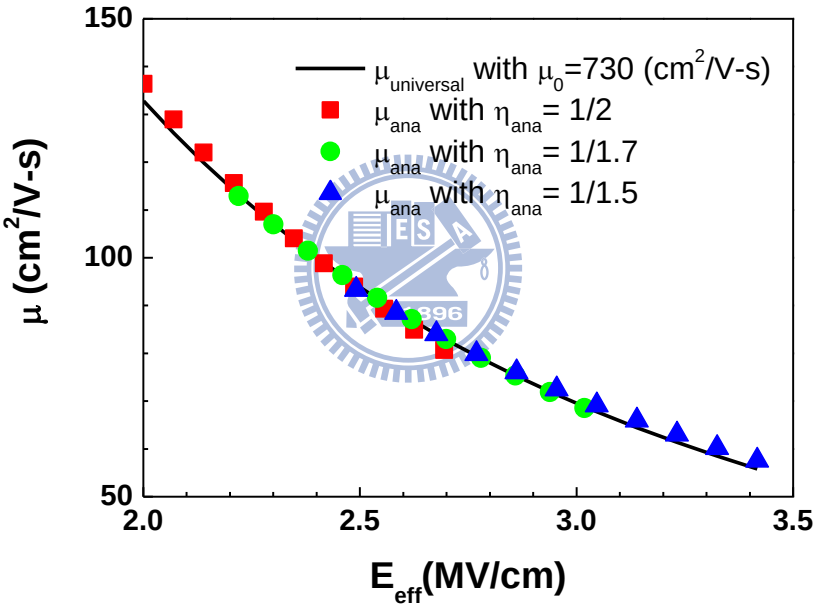


Fig. 2.4(a) An illustration showing that fitting parameter μ_0 dominates the magnitude of $\mu_{universal}$ vs. E_{eff} behavior.

Fig. 2.4(b) An illustration showing that fitting parameter η_{ana} dominates the slope of μana vs. E_{eff} behavior.

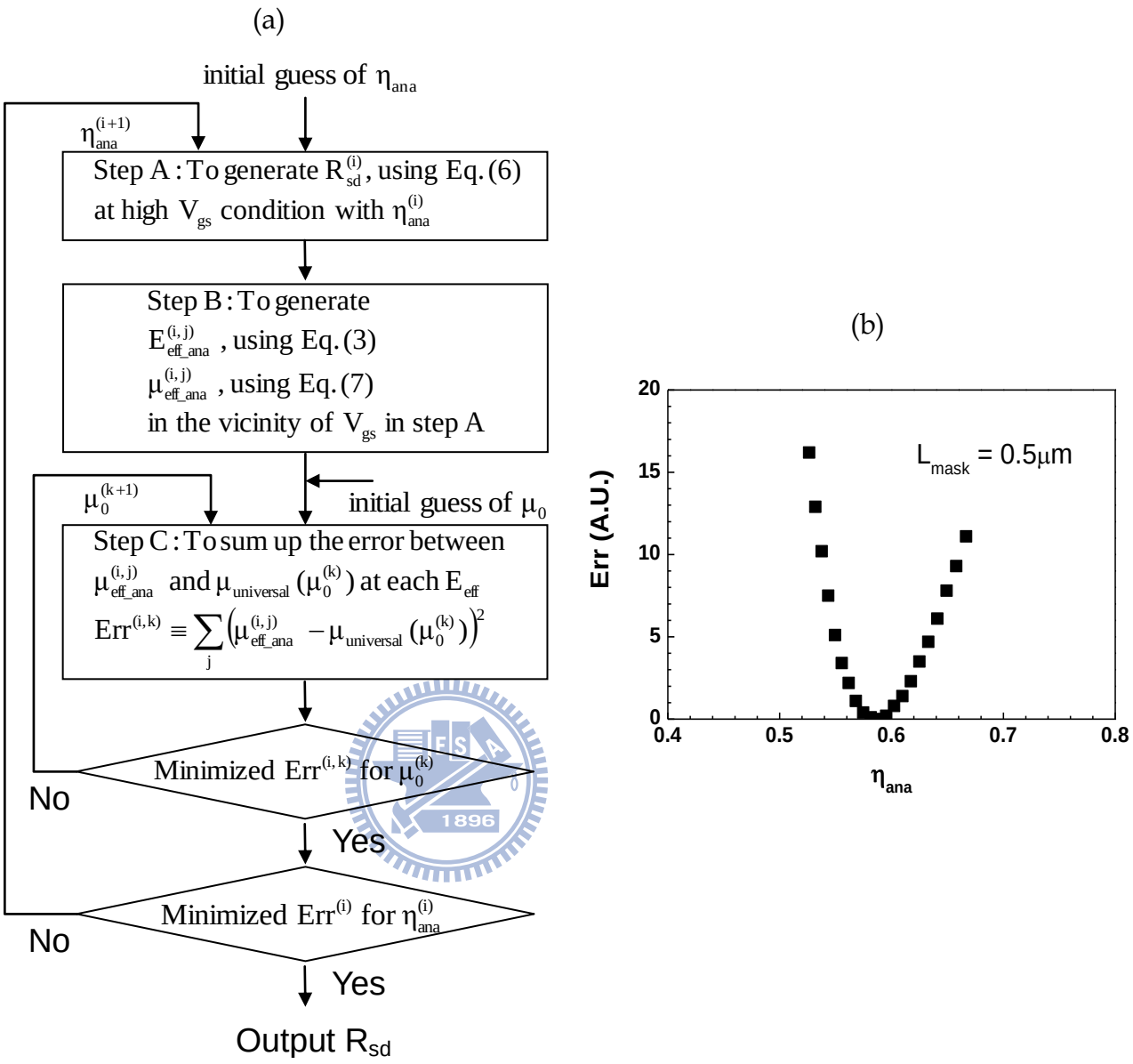
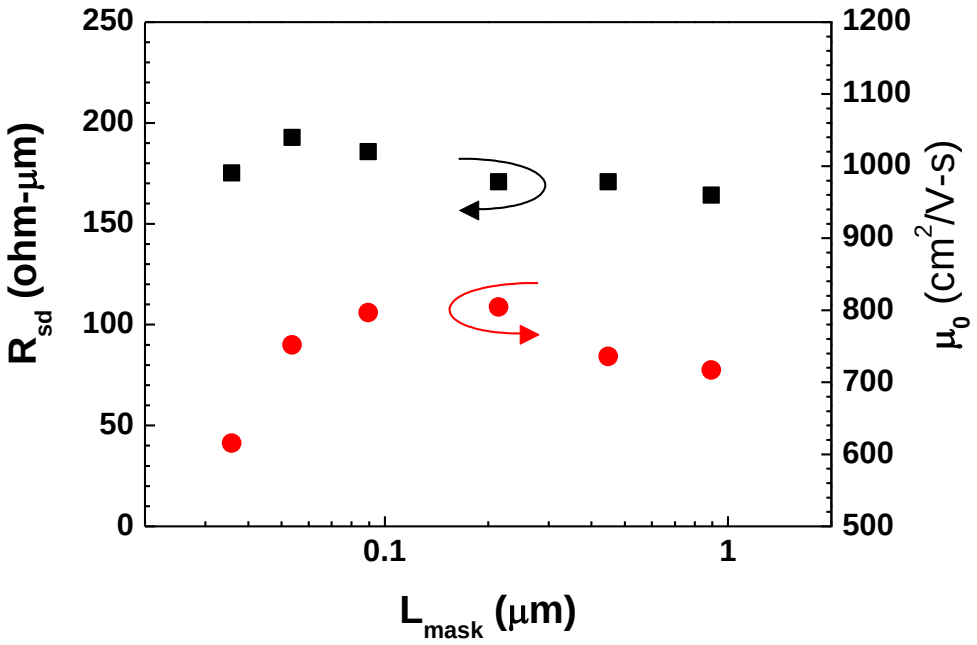


Fig. 2.5(a) A self-consistent method of R_{sd} extraction using both μ_0 and η_{ana} as fitting parameters in order to minimize the difference between $\mu_{universal}$ and μ_{ana}.

Fig. 2.5(b) Summation of $(\mu_{ana} - \mu_{universal})^2$ over a wide range of E_{eff} in the vicinity of V_{gs} where R_{sd} is extracted. NMOSFET with 0.5μm L_{mask} is used as an example. η_{ana}=1/1.7 provides the lowest error.

(a)



(b)

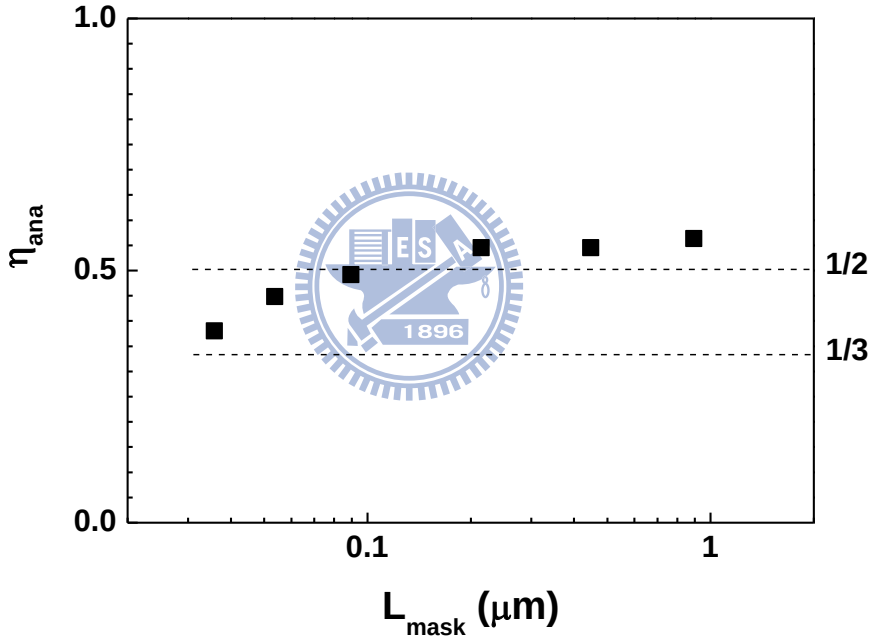


Fig. 2.6(a) R_{sd} and μ_0 extracted using the method proposed in this work. Similar R_{sd} values are extracted over a wide range of L_{mask}. μ_0 increases from L_{mask}=1μm down to L_{mask}~0.1μm and then decreases toward short channel regime.

Fig. 2.6(b) Extracted η_{ana}-L_{mask} behavior. η_{ana} keeps at a constant level for long channel devices and then decreases for L_{mask} shorter than 0.1μm.

(a)

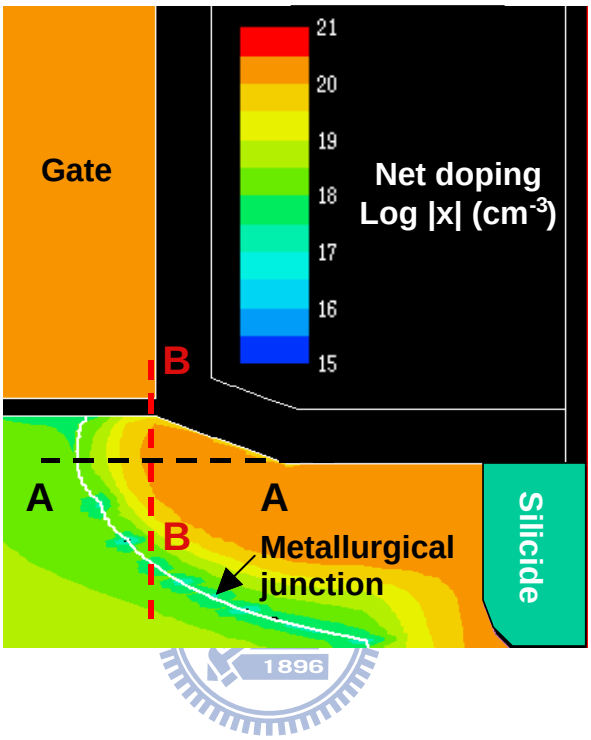
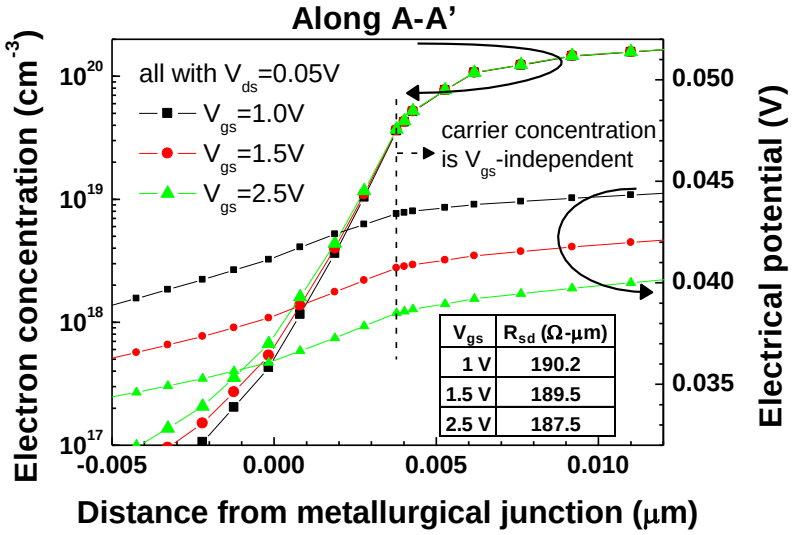


Fig. 2.7(a) TSUPREM-4 simulated 2-dimensional doping concentration in the vicinity of gate edge of the NMOSFET used in this work.

(b)



(c)

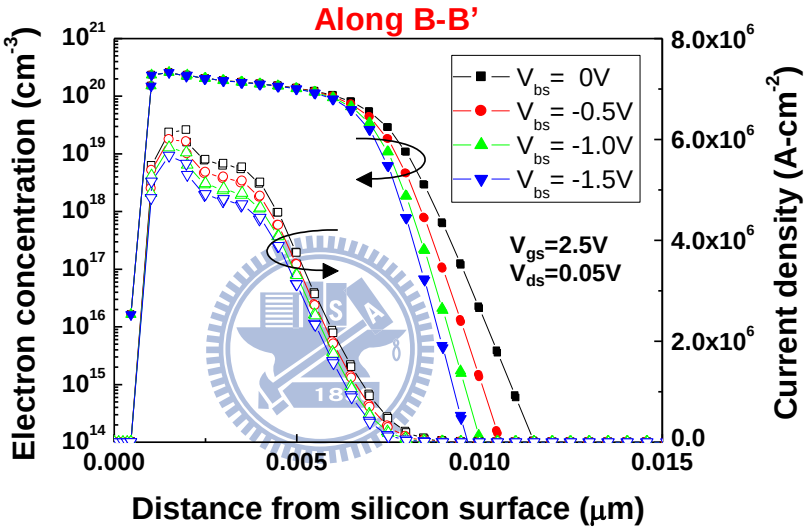


Fig. 2.7(b) Carrier concentration on the drain side along the horizontal direction (A-A') as shown in Fig. 2.7(a) under various V_{gs} conditions. V_{gs} shows little effect on modulating the carrier concentration inside source/drain extension regions. The inset table provides an example of TCAD-simulated R_{sd} values based on the potential drop between two characteristic points on the drain and the source side of a 0.1μm L_{mask} MOSFET. The R_{sd} values are reasonably consistent with the extracted ones shown in Section V.

Fig. 2.7(c) Carrier concentration along the vertical direction (B-B') as shown in Fig. 2.7(a) under various V_{bs} conditions. The current flow in source/drain extension is mainly located in a region where the carrier concentration is insensitive to V_{bs}

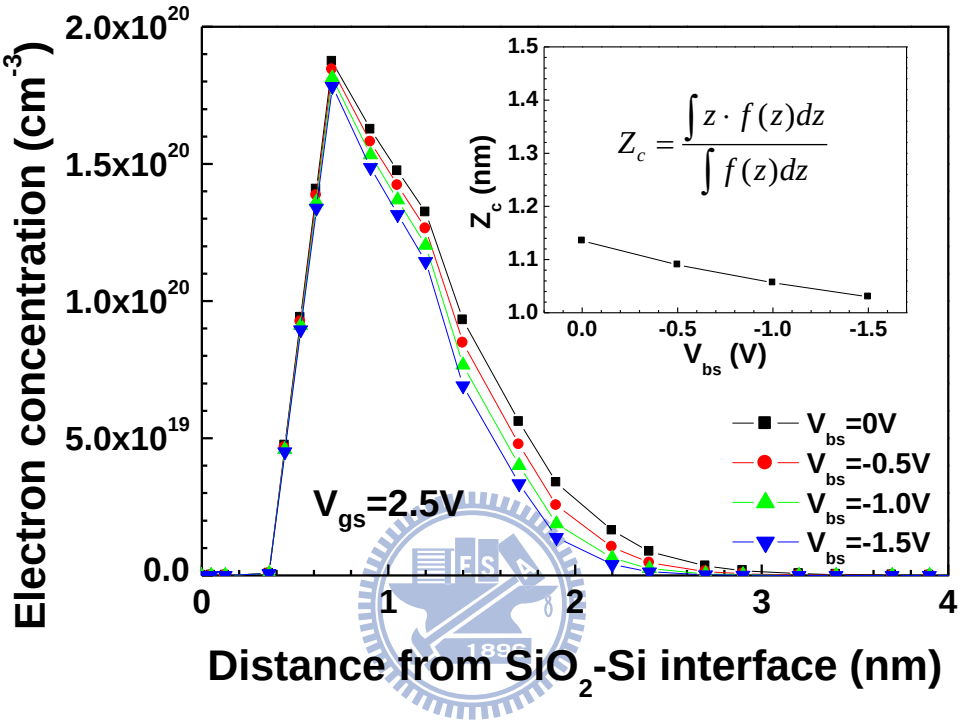
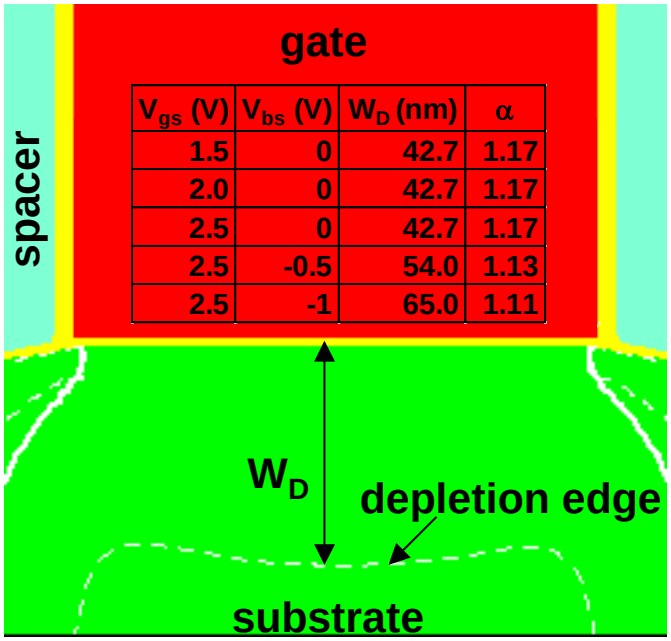


Fig. 2.8 Inversion-layer electron density distribution f, calculated using 2-D numerical simulators TSUPREM4 and MEDICI, normal to the channel surface under various V_{bs} conditions. The inserted figure illustrates the centroid of the carrier distribution (Z_c). When V_{bs} changes from 0V to –1.5V, Z_c decreases by only ~0.1nm which is equivalent to ~0.03nm decrease in T_{ox_inv}. This change should have a negligible effect on R_{sd} extraction proposed in this work.

(a)



(b)

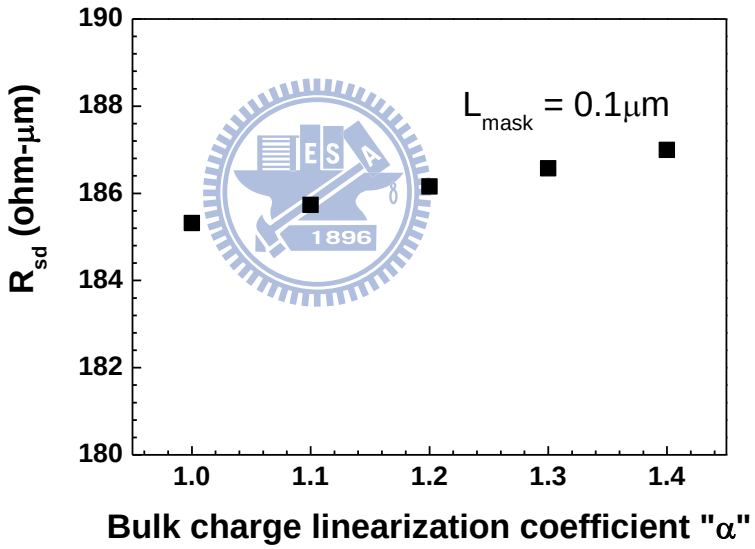


Fig. 2.9(a) A schematic plot of depletion width under gate area of a 0.1μm L_{mask} NMOSFET. A table of values of bulk charge linearization coefficient "α" under various bias conditions is shown in the inset. The values of "α" are typically lower than 1.2.

Fig. 2.9(b) The extracted R_{sd} shows negligible sensitivity on the bulk charge linearization coefficient. Therefore, the assumption of "α=1" is adequate in this extraction procedure.

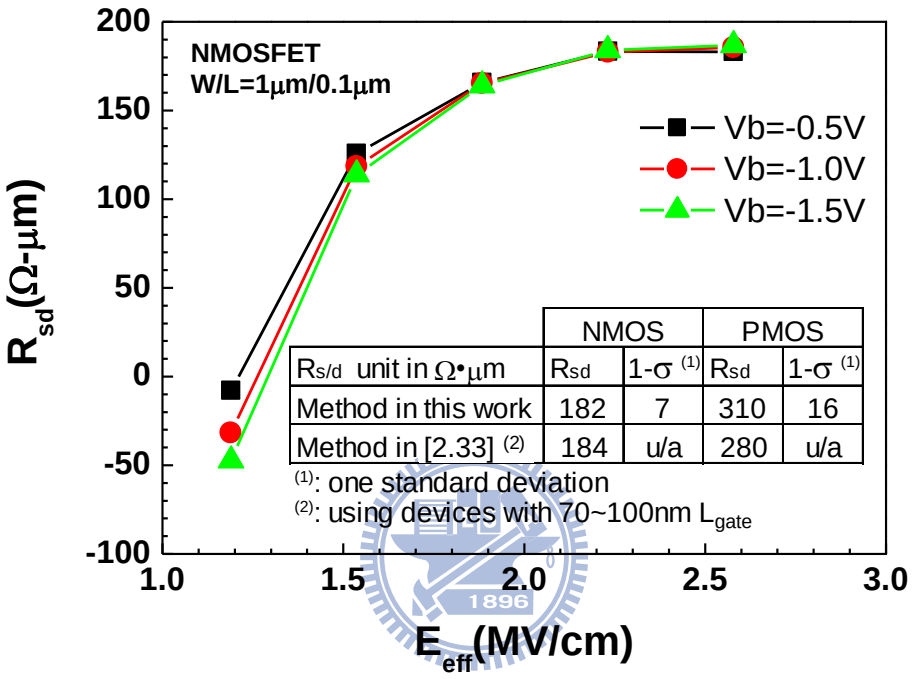


Fig. 2.10 Extracted R_{sd} as a function of E_{eff}. Erroneous R_{sd} values appear in the low E_{eff} region because the E_{eff} is insufficiently high and the "constant mobility" criterion is not satisfied. R_{sd} approaches a constant and exhibits no dependency on V_{bs} in the sufficiently high E_{eff} region. The inset shows the R_{sd} values extracted from the proposed method in this work and the method in [2.33]. A good agreement is achieved.

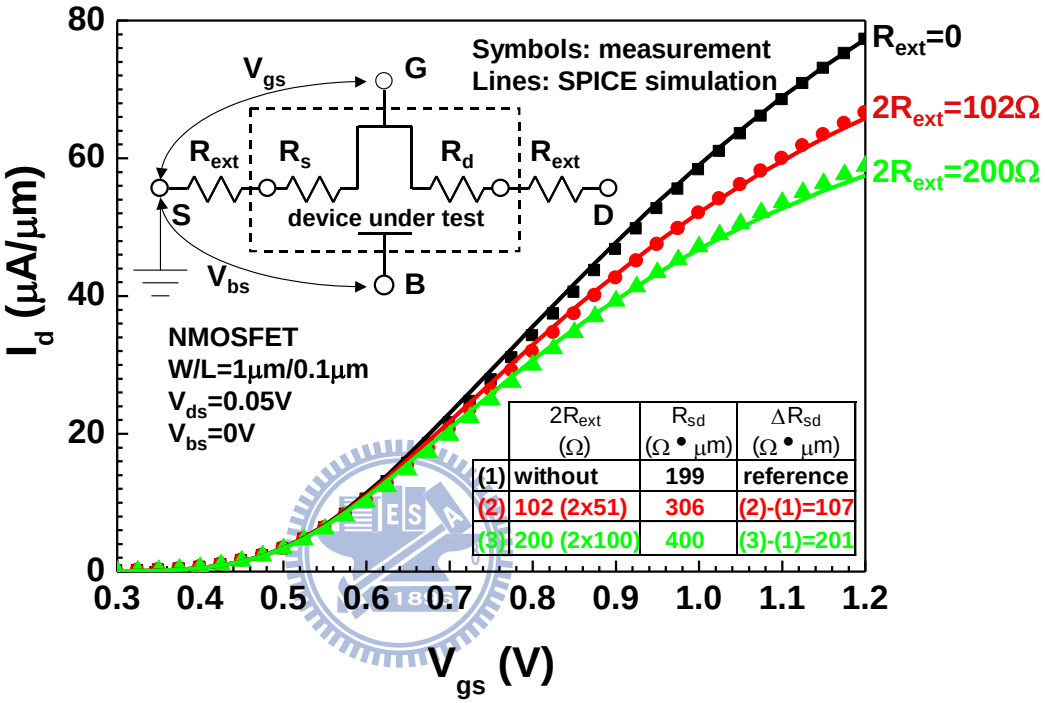
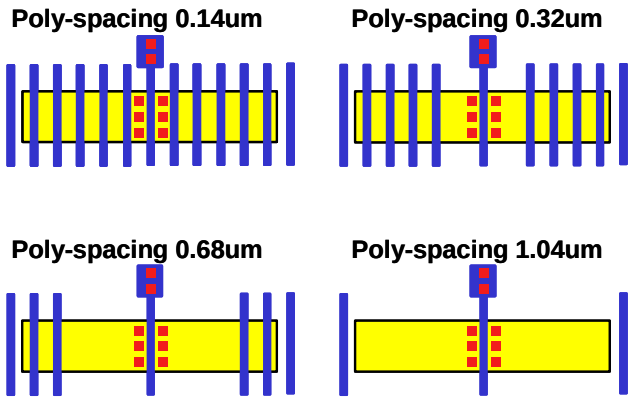
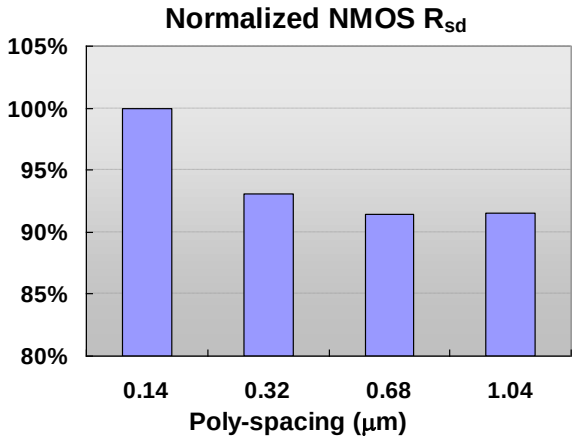


Fig. 2.11 Measured and simulated I_d-V_{gs} characteristics of a typical NMOSFET with W_{mask} /L_{gate} = 1μm/0.1μm under V_{ds}=0.05V. External resistors, R_{ext}, are connected to the device as shown in the inserted plot. The extracted R_{sd} values, listed in the inserted table, faithfully reflect the presence or absence of the R_{ext}

(a)



(b)



(c)

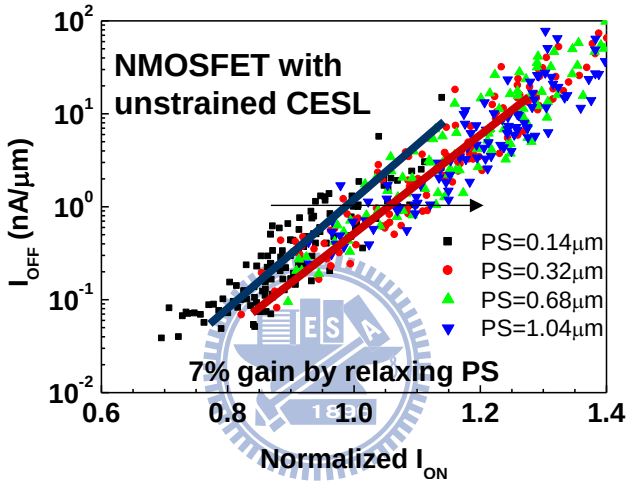
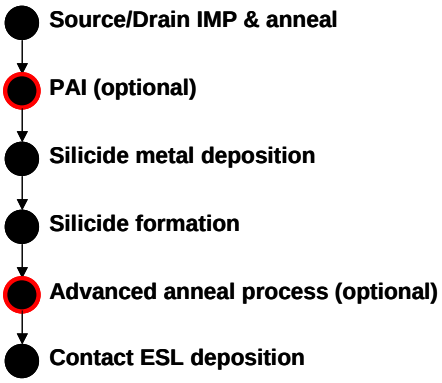


Fig. 2.12(a) A schematic illustration of device layouts with different poly-spacing (PS).

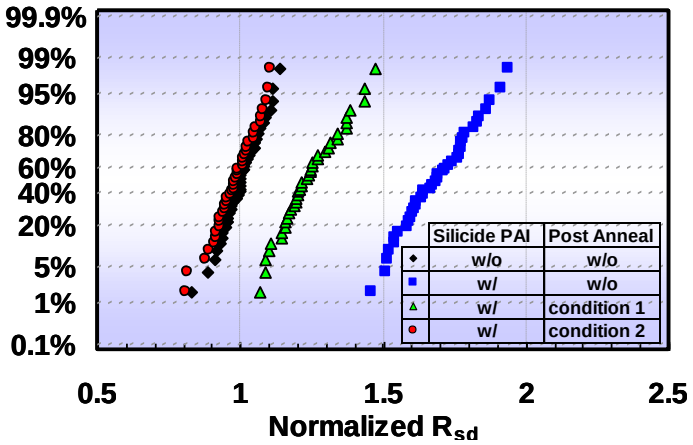
Fig. 2.12(b) R_{sd} vs. poly-spacing. An obvious reduction in R_{sd} is observed by increasing the poly-spacing from 0.14μm to 0.32μm. No obvious reduction is obtained by further increasing PS to 0.68μm and beyond.

Fig. 2.12(c) NMOSFET I_{on}-I_{off} performance exhibits a clear dependency on R_{sd} as shown in Fig. 2.12(b). An obvious improvement is observed by increasing the poly-spacing from 0.14μm to 0.32μm. Little difference is obtained by further increasing PS to 0.68μm and beyond. The stress effect of contact etch-stop-layer (CESL) is ruled out because an unstrained CESL is used in this comparison.

(a)



(b)



(c)

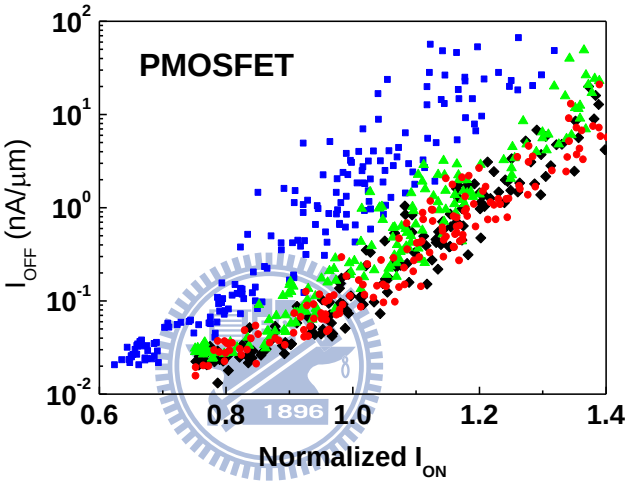


Fig. 2.13(a) A schematic process flow of silicide formation with optional PAI and anneal processes.

Fig. 2.13(b) A cumulative probability plot of PMOSFET R_{sd} under different PAI and post anneal conditions for silicide formation. R_{sd} extracted by our method shows good sensitivity to the process conditions.

Fig. 2.13(c) PMOSFET I_{on}-I_{off} performance shows a good correlation with the extracted R_{sd} in this work. Larger R_{sd} values result in degraded I_{on}-I_{off} performance. Higher R_{sd} variations correspond to increased I_{on}-I_{off} spreading.

Chapter 3

Gate Strain and EOT Engineering: A Millisecond-Anneal-Assisted Selective Fully Silicided (FUSI) Gate Process

3.1 Preface

For the advanced technology, poly-depletion-effect becomes unacceptable because it significantly decreases the gate inversion capacitance and in turn degrades MOSFET electrostatic characteristics and driving force. With the aim of eliminating poly-depletion-effect, FUSI gates have been intensively evaluated as an alternative to the deposited metal gates as a result of their excellent process compatibility with the VLSI poly-silicon gate processes. In the previous works of FUSI gates [3.1-3.10], poly-silicon gates and source/drain (S/D) regions required independent silicidation processes for the purpose of forming FUSI exclusively in the gate region without forming too thick silicide layers in the S/D regions. In addition, extra CMP and lithography mask layers were typically required for FUSI gate formation. This consequently led to a greater process complexity.

Unlike the conventional FUSI gate processes which usually needed additional long time thermal annealing steps, we introduced, for the first time, a novel process featuring milli-second-annealing-assisted (MSA-assisted) nickel silicide phase transformation. We attempted to use this MSA to form FUSI gates and thin silicided S/D regions simultaneously. By incorporating

nitrogen dopant in the N^+ poly-silicon gates during the front-end fabrication processes, the silicidation rate was retarded in the N^+ poly-silicon gates. Therefore, the following MSA-assisted silicidation process exhibited an excellent selectivity between N^+ and P^+ poly-silicon gates. In addition to eliminating the poly-depletion-effect, this P^+ FUSI gate may potentially introduce mechanical strain upon silicide phase transformation and imposes stress in PMOSFET channel region. Its effect on modulating the hole carrier mobility in PMOSFETs will be carefully addressed in this work and corroborated by TCAD simulation. The proposed method is proven fully compatible with the existing strain engineering techniques including e-SiGe S/D and strained contact-etch-stop layers.

3.2 Device Fabrication and Experiments

The devices shown in this work were fabricated with an 1.2 nm equivalent-oxide-thickness (EOT) nitrided gate oxide on the 40nm technology ground rules [3.11]. Various strained silicon technology was used, including neutral shallow-trench-isolation (STI) gap-fill material, stress memorization technique (SMT) [3.12], embedded SiGe (e-SiGe) and dual contact-etch-stop-layer (d-CESL). An MSA was used for ultra shallow junction (USJ) formation and dopant activation before silicidation. Other device and process features were described in [3.11].

Fig. 3.1 describes the process steps in the vicinity of silicidation process. A two-step silicidation was used for both the regular and FUSI gate processes. After first silicidation using soak-annealing RTA1 and non-reacted nickel removal, the traditional silicide phase transformation soak-annealing RTA2 is

replaced with an MSA. The MSA conditions were intensively investigated in this work in order to obtain an optimum process window. Without implementing any additional process steps, the selective P^+ FUSI gate can be realized by mainly optimizing the MSA conditions as will be discussed in the follow section.

It is reasonable that the effective temperature in the poly-silicon gate is higher than that in the active area during the MSA process because the poly-silicon gate is surrounded by spacer liner oxide and gate oxide, which efficiently retards the heat dissipation during the silicidation thermal cycles. The silicon substrate serves as a heat sink for the active area and leads to a relatively lower temperature during the MSA process. As a result, there should be a process window for the MSA conditions that allows for both FUSI gate formation and normal silicidation in the active areas. In order to keep the efficacy of SMT-induced poly gate strain, the prevention of FUSI formation on N^+ poly-silicon gate was ensured by incorporating nitrogen into the N^+ poly-silicon. The main purpose of this work was to verify the existence of the process window of forming FUSI on P^+ Poly-silicon gate exclusively.

3.3 Results and Discussion

Fig. 3.2 shows the TEM cross-section of both the NMOSFET and PMOSFET under a series of silicide phase transformation conditions (silicidation-RTA2 using MSA). It is evident that a process window of MSA conditions exists in terms of forming FUSI gate on the P^+ poly-silicon gate while the N^+ poly-silicon gate keeps non-FUSI. Because of the heavy incorporation of nitrogen impurity of more than 10^{15} cm^{-2} ion implantation

dose in the N^+ poly-silicon gate, silicidation rate is significantly retarded. The retardation of silicidation rate caused by nitrogen was also observed in [3.4]. Consequently, selective P^+ FUSI gate can be formed by modulating the MSA thermal budget and the nitrogen concentration in the N^+ poly-silicon gate. The silicide phase of the P^+ FUSI gate, confirmed by analyzing the electron diffraction pattern, is $NiSi_2$ as also depicted in Fig. 3.2.

(a) On the Device Performance

As shown in Fig. 3.3 and Fig. 3.4, both the threshold voltage (V_{th}) shift of long channel PMOSFET and flat band voltage (V_{FB}) shift of the PMOSFET CV curve clearly demonstrate a workfunction (WF) shift of ~150mV. Therefore, this P^+ FUSI gate has a WF about 150mV above the valence band edge and it still behaves likes a p-metal. The original P^+ poly silicon gate was heavily doped with boron dopant during the P^+ S/D ion implantation with a dose > $3x10^{15}$ cm^{-2}. It is confirmed that the heavily boron-doped FUSI can be used as a p-metal [3.5-3.10]. Because of a limited WF shift, the adjustment of doping profile toward a reasonable V_{th} level is not difficult. In order to provide a similar V_{th} level for short channel devices, a lower halo ion implantation dose was utilized to compensate for the 150mV WF-shift. As a result, similar PMOSFET V_{th} level was achieved in the short channel MOSFETs. Smooth PMOSFET V_{th} roll-off behavior also indicates a single-phase P^+ FUSI gates for gate length ranging from 10μm to 30nm. As shown in Fig. 3.5, a tight PMOSFET V_{th} distribution guarantees a single-phase and uniform P^+ FUSI gate formation.

As to the NMOSFET, using a moderate MSA condition provides little V_{th} difference compared to the conventional soak-annealing for all gate lengths as exhibited in the upper part of Fig. 3.3. As shown in Fig. 3.5, a tight NMOSFET V_{th} distribution indicates that all of the N^+ poly-silicon gates remained non-FUSI. It is evident that this MSA-assisted FUSI gate formation process shows no dependency on gate length for both NMOSFETs and PMOSFETs. This is a noticeable advantage on the process simplicity over the conventional methods which may need extra mask layers, partial poly gate recess processes, and separate nickel supply for long channel and short channel devices.

NMOSFET showed an unchanged relation of the inversion state gate oxide thickness and the inversion state gate current (T_{ox_inv} vs. J_g) while PMOSFET clearly demonstrated a 0.3nm thinner T_{ox_inv} as indicated in Fig. 3.6. This is the evidence of the elimination in PMOSFET poly-depletion-effect with P^+ FUSI gate formation.

Fig. 3.7 shows the difference in device I_{on}-I_{off} performance between non-FUSI and FUSI gates. NMOSFET shows an obvious degradation when N^+ FUSI gates are formed under a non-optimal MSA condition. This implies that the "memorized" strain resulting from SMT may be relaxed because of the consumption of strained N^+ poly-silicon gate. This result is consistent with what has been proposed in [3.4] showing poor compatibility between N^+ FUSI gate and the performance enhancement resulting from SMT for NMOSFETs. In order to prevent this NMOSFET I_{on}-I_{off} degradation, we optimized the MSA-assisted silicidation process for FUSI gate formation exclusively on P^+ poly-silicon gate while preventing FUSI gate formation on N^+ poly-silicon

gate. The NMOSFET I_{on}-I_{off} degradation was thereby prevented, while the FUSI-gated PMOSFET devices showed an enhancement in I_{on}-I_{off} performance of more than 20%. It is believed that this PMOSFET enhancement can be attributed to at least three factors. 1st: the reduced halo ion implantation dose which reduced impurity scattering. 2nd: the thinner T_{ox_inv} resulting from elimination of poly-gate-depletion. 3rd: the change in mechanical stress induced by the FUSI gate. Based on the measurement data shown in Fig. 3.8, the stress level of MSA-assisted FUSI gate is ~500MPa more tensile than the stress level of the poly-silicon gate after silicidation. Hence, a FUSI gate may impose a stronger compressive stress on the underlying PMOSFET channel region. This fact was verified by using TCAD simulation as shown in Fig. 3.9 by implementing the measured stress level in the gate region into a well calibrated device simulator [3.13]. It is clear that FUSI-gated device shows a ~460MPa higher compressive strain in the middle of channel region as compared to the poly-silicon gated device. The hole carrier mobility is thereby enhanced.

(b) On the Silicide Morphology and Junction Leakage Performance

In this work, the MSA-assisted silicidation process also improved the nickel silicide formation quality. Compared to the conventional RTA2 process using soak-annealing, a smoother silicide/silicon interface was obtained by replacing soak-annealing with MSA as shown in Fig. 3.10. Consequently, MSA-assisted silicidation process can potentially improve the junction leakage resulting from random silicide spiking. Fig. 3.11 compares the SRAM junction leakage behavior between soak-annealing and MSA-assisted

silicidation. Compared to the soak-annealing process, a tighter junction leakage distribution was observed in the N^+ diffusion/P_Well junction structure by using MSA-assisted silicidation while an unchanged P^+ diffusion/N_Well leakage behavior was obtained. In terms of junction leakage control, MSA-assisted silicidation outperforms the conventional soak-annealing process.

Fig. 3.12(a) compares the sheet resistance distributions for narrow silicided N^+ and P^+ diffusion regions between two poly-silicon lines. This is often the most sensitive test-pattern than tells the quality of silicide formation. Equally tight distributions were achieved between RTA2 using soak-anneal and RTA2 using MSA. The values of the sheet resistance are the same in these two processes, indicating the same silicide phase in the diffusion regions. The sheet resistance distributions for 30nm-wide silicided poly-silicon lines are shown in Fig. 3.12(b). RTA2 using MSA led to a remarkably higher sheet resistance of the silicided P^+ poly-silicon lines due to the FUSI gate formation in a different phase of nickel silicide ($NiSi_2$) while the sheet resistances of the silicided N^+ poly-silicon lines were not significantly changed. No matter for N^+ or P^+ poly-silicon lines, MSA-assisted silicidation provides tight distributions for the narrow silicided poly-silicon lines.

3.4 Conclusion

An MSA-assisted silicidation process is proposed in this work. By using optimum MSA conditions for the silicide phase transformation, single-phase ($NiSi_2$) FUSI gates can be uniformly and exclusively formed for PMOSFETs in various device dimensions while preserving a FUSI-free N^+ Poly-silicon gate

with feature size down to 30nm. There is definitely a process window for the MSA-assisted silicidation process to simultaneously form FUSI gates and thin silicided diffusion regions without using additional CMP, lithography layers and poly-silicon etch-back processes.

An enhancement in PMOSFET I_{on}-I_{off} performance of more than 20% is experimentally realized because of the elimination of poly-depletion-effect and the FUSI-gate-induced compressive channel strain. Considering the significant improvement in device performance and the unique integration-friendly features, this MSA-assisted FUSI gate formation is very promising for the current and coming VLSI generations.

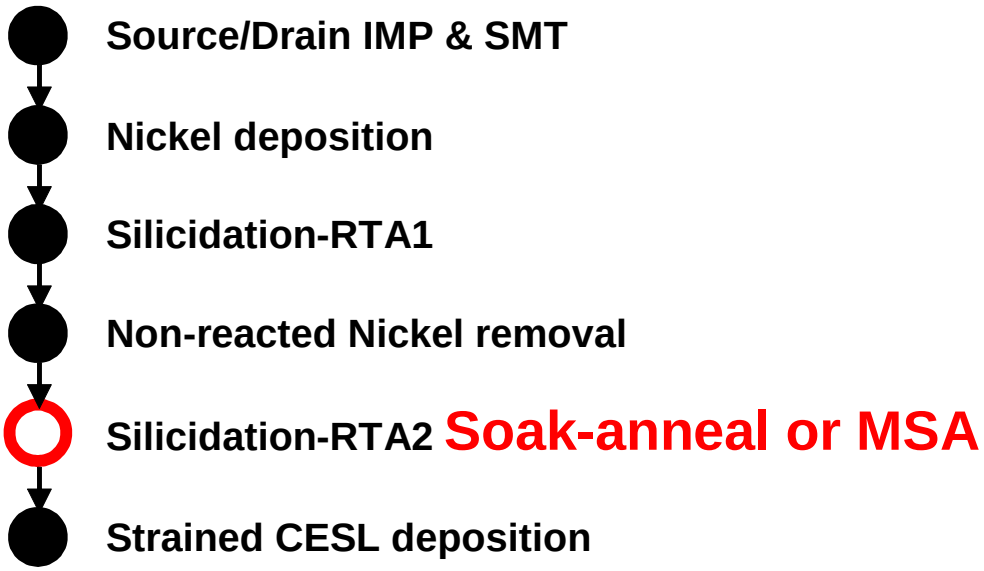


Fig. 3.1 Process steps in the vicinity of silicidation process. Either a soak-annealing or an MSA is utilized for RTA2 for silicide phase transformation.

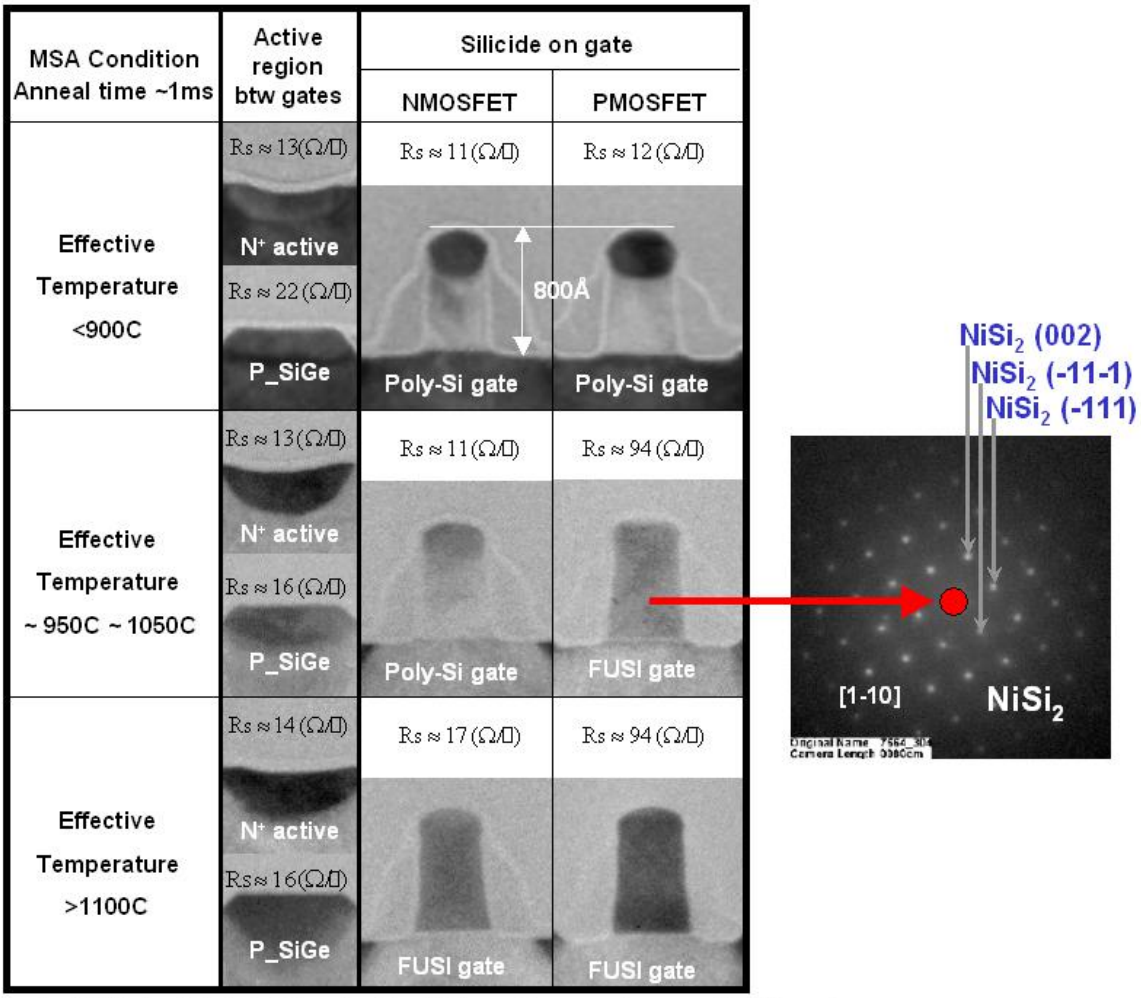


Fig. 3.2 TEM cross-sectional pictures of NMOSFET and PMOSFET under three MSA conditions. FUSI gate forms exclusively on PMOSFET while N^+ poly-silicon gate remains non-FUSI under a moderate MSA condition. The silicide phase of the P^+ FUSI gate is $NiSi_2$.

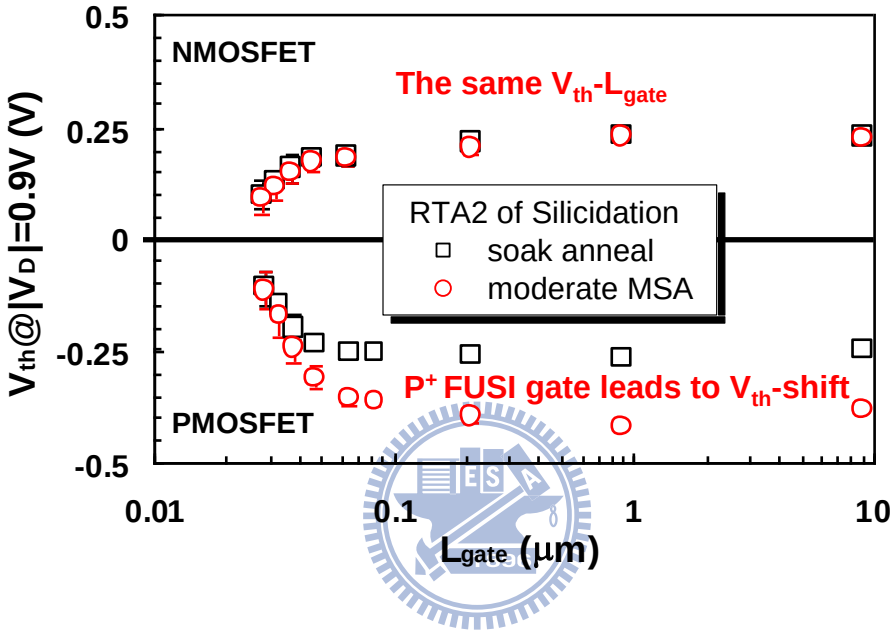


Fig. 3.3 V_{th_sat} vs. L_{mask} behavior. Only PMOSFETs exhibit V_{th} shift. This indicates a selective FUSI gate formation exclusively on PMOSFETs. A lower halo ion-implantation dose was used for PMOSFET to compensate for the WF-shift. Smooth V_{th} roll-off curve indicates a single-phase P^+ FUSI gate.

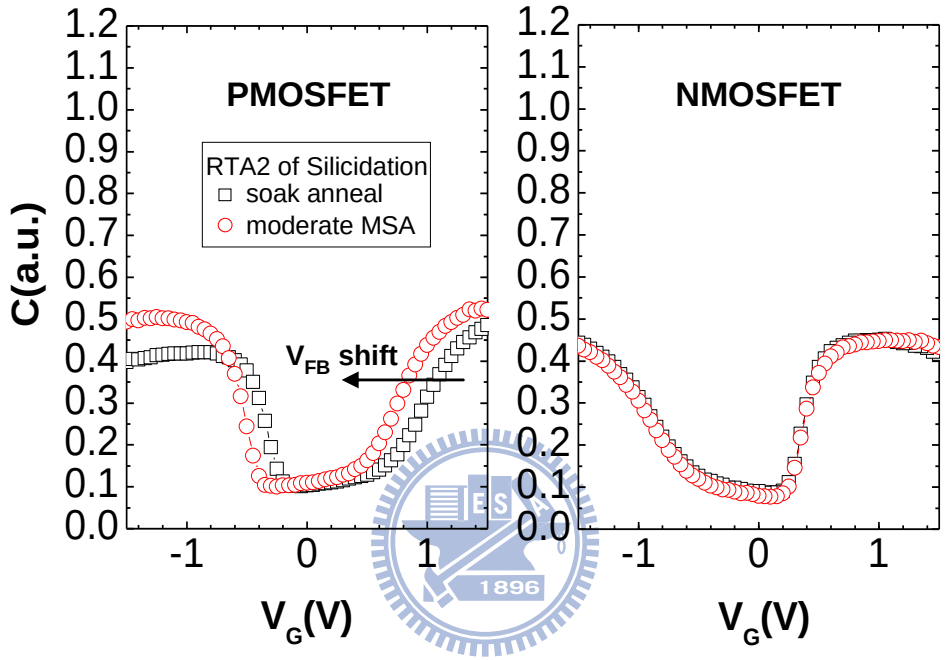


Fig. 3.4 C-V curves of NMOS and PMOS using a moderate MSA condition for silicidation. PMOS shows a clear VFB shift that indicates WF-shift for only PMOSFET.

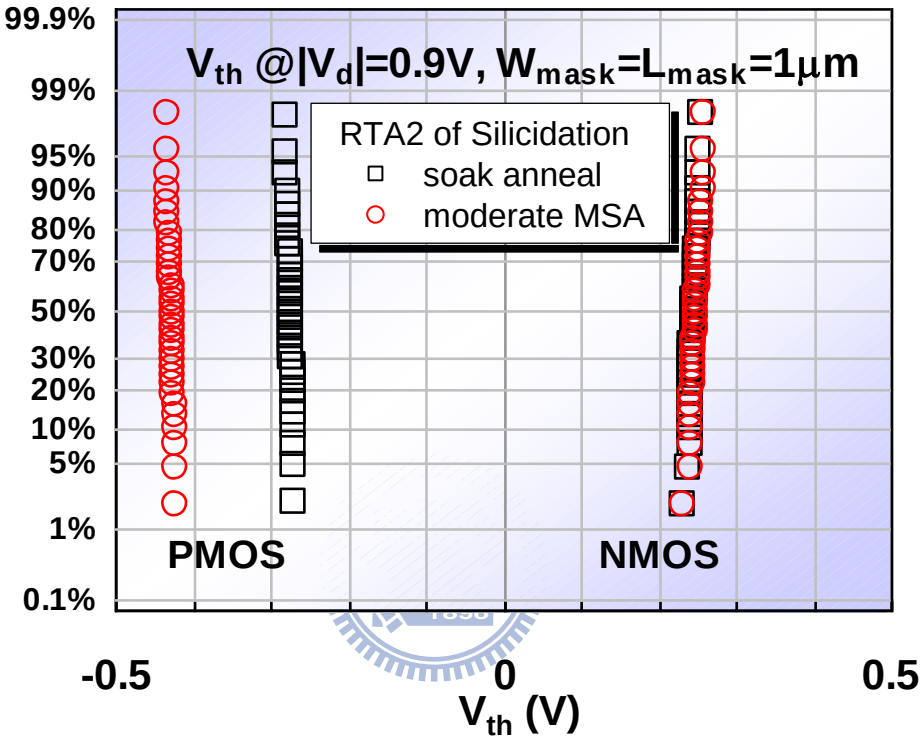


Fig. 3.5 Tight V_{th} distributions are observed under a moderate MSA condition. V_{th} is unchanged for NMOSFET while an obvious PMOSFET V_{th} shift with a tight distribution indicates a uniform and single-phase P^+ FUSI gate formation.

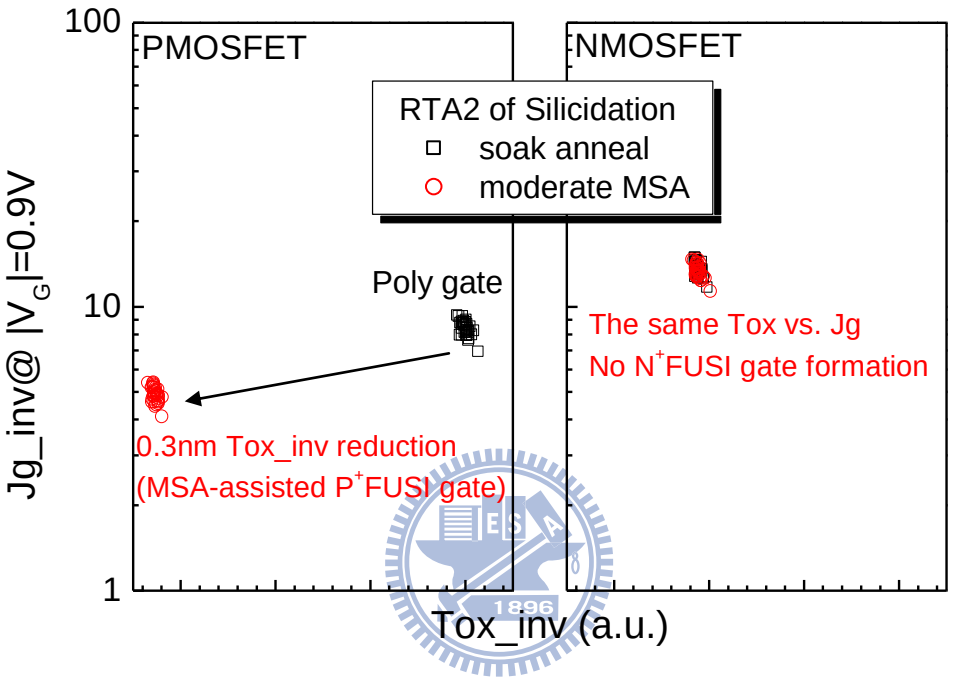


Fig. 3.6 PMOSFET with FUSI gate shows a 0.3nm thinner T_{ox_inv} because of the elimination of poly-depletion-effect. NMOSFET shows no noticeable change under a moderate MSA condition.

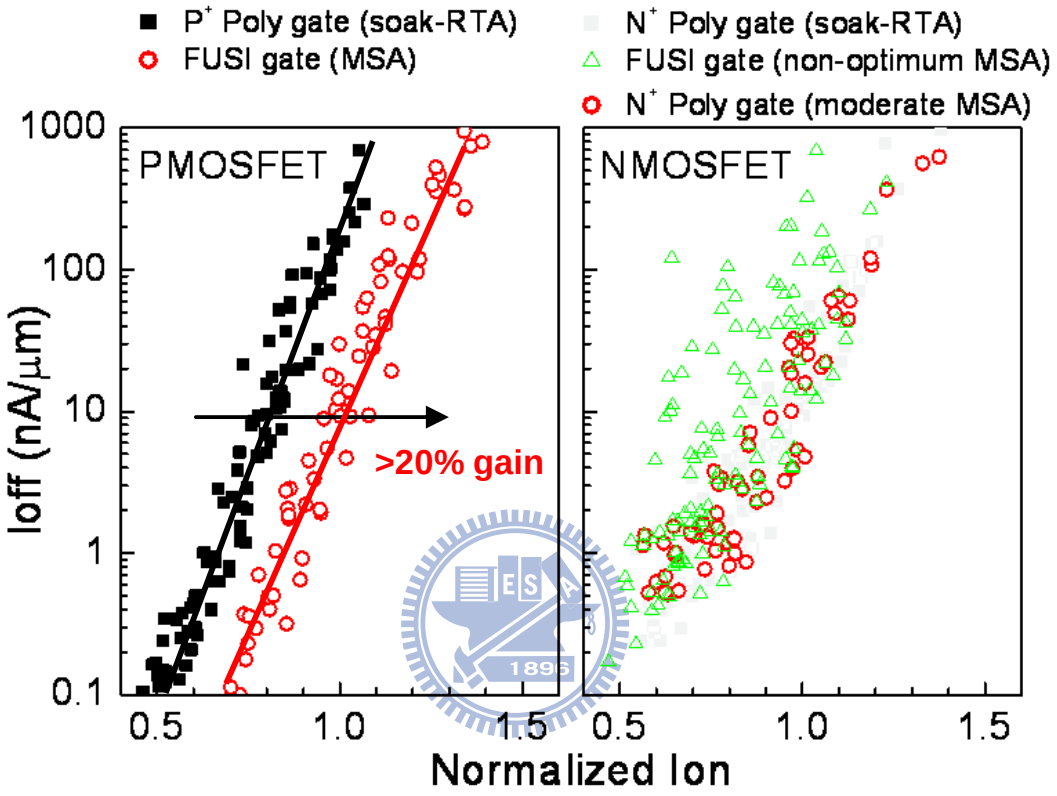


Fig. 3.7 P^+ FUSI gate improves PMOSFET I_{on}-I_{off} by more than 20% while NMOSFET keeps similar I_{on}-I_{off} performance when a moderate MSA condition is utilized for FUSI gate formation exclusively on P^+ poly-silicon gates while preventing FUSI gate formation on N^+ poly-silicon gates.

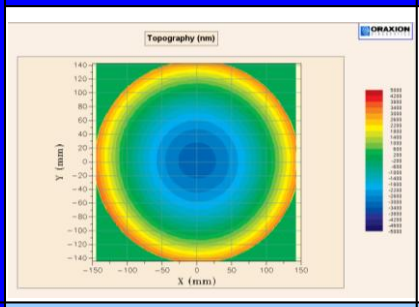
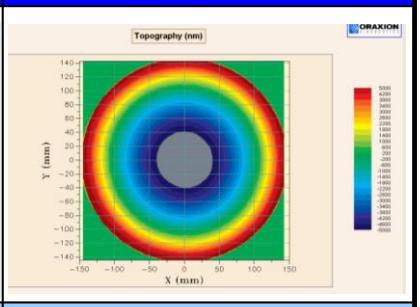
	Soak-annealing	MSA-assisted
Wafer Bow Measurement in-line plots		
Bow height	6750 nm	12167 nm
3-D Δ stress	Δ stress	
σ11	551.6 Mpa	1001.3 MPa
σ22	546.7 MPa	990.3 MPa
σ12	2.5 MPa	2.7 MPa

Fig. 3.8 Nickel silicon strain measurement (difference between before- and after- silicidation-RTA2 process) using wafer-bowing indicates that highly tensile $NiSi_2$ silicide was formed by using MSA-assisted silicidation.

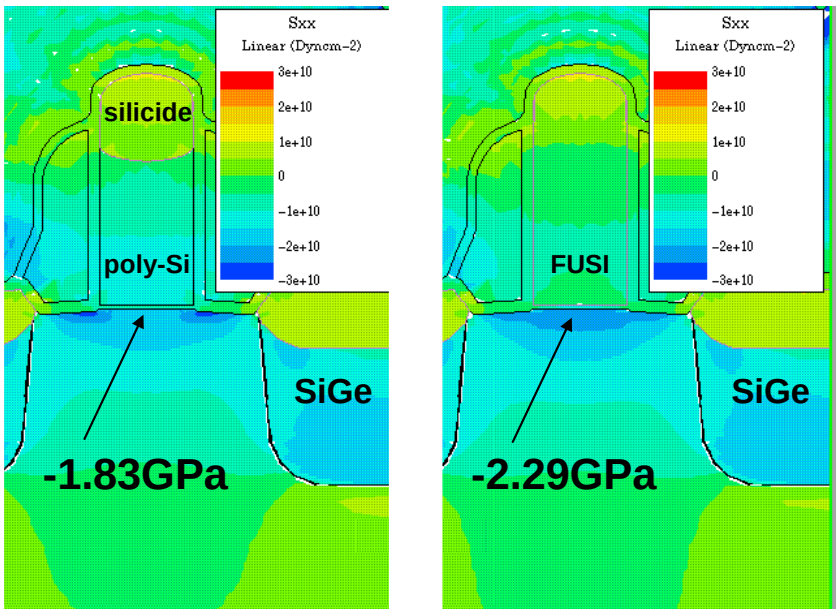


Fig. 3.9 By implementing the change in the stress level measured in Fig. 3.8 into a TCAD simulator (T-suprem4), the simulation result verifies that a highly tensile FUSI gate imposes a stronger compressive stress in the PMOSFET channel region compared to the poly-silicon gate.

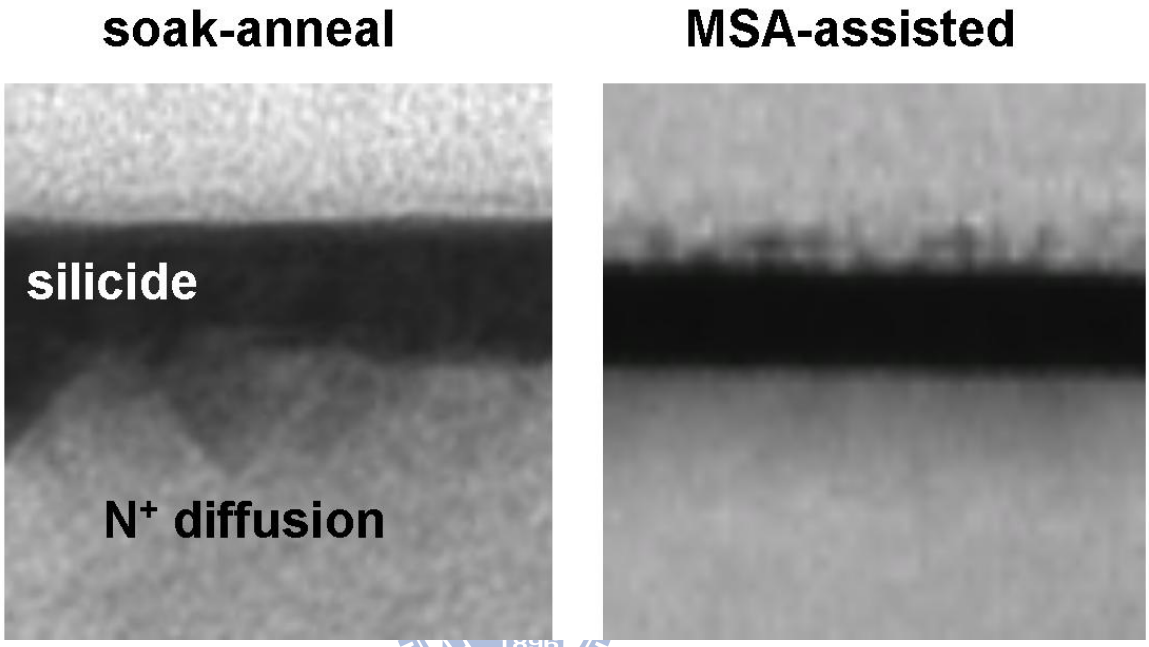


Fig. 3.10 MSA-assisted silicidation improves the interface quality between silicide and silicon. As compared to the conventional silicidation-RTA2 using soak-annealing, MSA-assisted silicidation provides a smoother interface without silicide spiking.

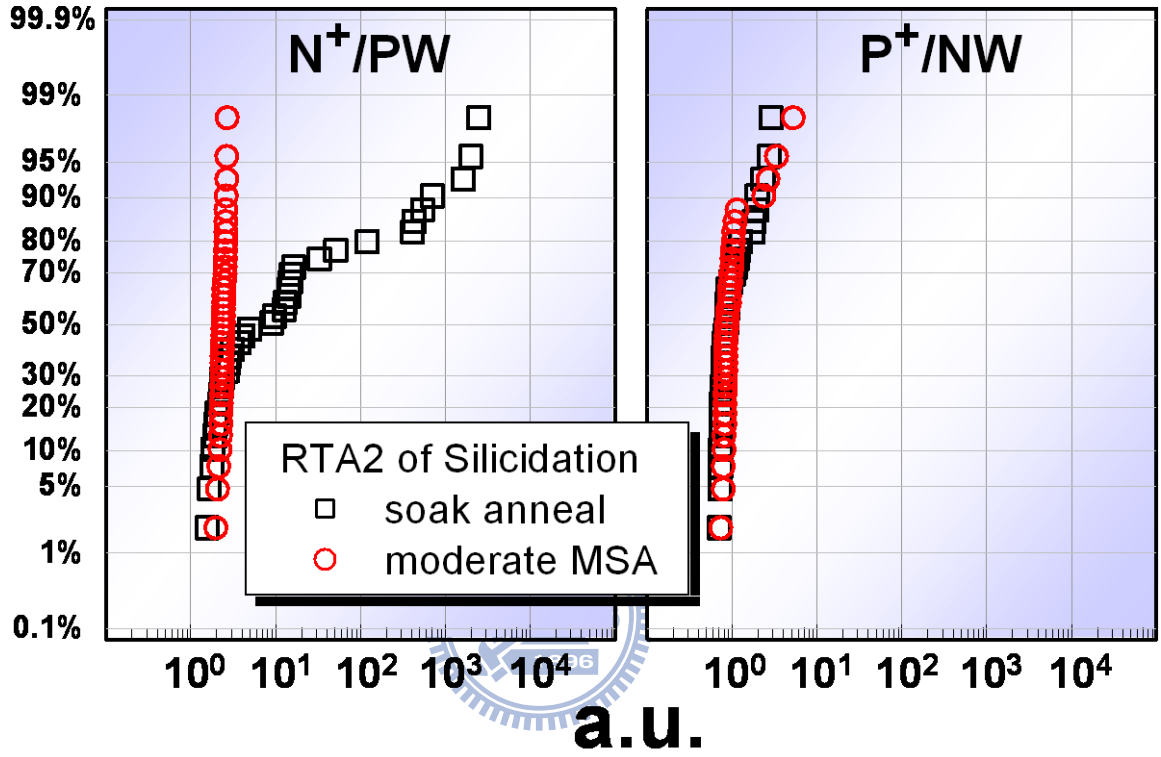


Fig. 3.11 Junction leakage behavior is compared between silicidation-RTA2 using soak-annealing and MSA. An obviously tighter N^+diffusion/P_well junction leakage distribution is observed by using MSA.

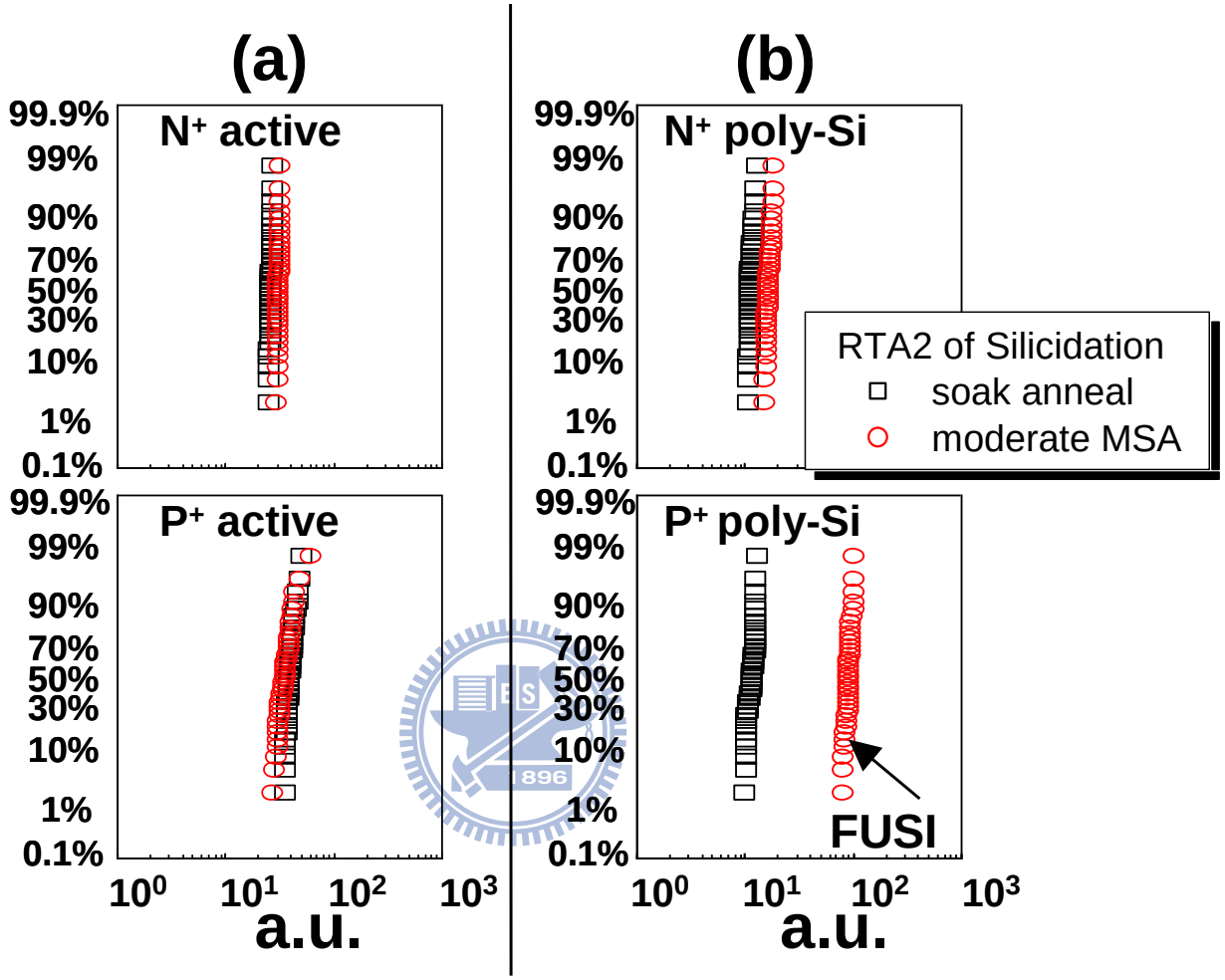


Fig. 3.12(a) Sheet resistance of N^+ and P^+ diffusion regions between poly-silicon lines with pitch = 0.108μm. Tight distributions guarantee uniform silicide thickness and continuity.

Fig. 3.12(b) Sheet resistance of poly-silicon lines with line_width = 30nm. P^+ FUSI shows a significantly higher sheet resistance because the MSA-assisted silicidation process transforms whole P^+ poly-silicon into $NiSi_2$ phase. The distributions of the sheet resistance are equally tight between silicidation-RTA2 using soak-annealing and MSA.

Chapter 4

Channel Strain and R_{sd} Engineering: An Extreme Surface Proximity for Embedded-SiGe in pMOSFETs Featuring Self-Aligned Silicon-Reflow (SASR)

4.1 Preface

During the past decade, e-SiGe has been widely utilized in modern CMOS technology with aim to enhance pMOSFET performance [6.1]-[6.13]. Not only can hole mobility benefit from lattice-mismatch-induced mechanical strain, but also source/drain series resistance (R_{sd}) can be reduced with the optimization of in-situ boron doping techniques. The continuous endeavors of e-SiGe strain and R_{sd} engineering lead to astonishing improvement in PMOFET performance. The drive current ratio of PMOSFET over NMOSFET increased constantly from 90nm to 32nm technology [6.13] as shown in Fig. 4.1. Until recently, PMOFET linear drive current (I_{dlin}, the drain current measured at V_d = 0.05V, and V_g=V_{dd}) outperformed NMOFET at the first time [6.13].

The surface proximity-push remains one of the most essential factors concerning the efficacy of e-SiGe strain and R_{sd} engineering. To address this issue, sophisticated etching treatments were adopted in the previous work [6.6], [6.9]. Nevertheless, as the tip of e-SiGe gets closer to the gate edge, the variation in proximity-push resulting from the etching process is more

pronounced and in turn the variation in mechanical strain and R_{sd} inevitably becomes more significant.

The purpose of this study was to provide a self-aligned process of e-SiGe surface proximity-push without using sophisticated etching process. In this study, a novel technique featuring silicon reflow was instead adopted to produce an enhanced e-SiGe proximity-push at the channel surface. Following a conventional isotropic silicon recess-etch which created a large curvature under a spacer structure, the silicon wafer was then annealed in the hydrogen ambient at a moderate temperature. This annealing process leads to silicon volume transfer, or reflow, [6.14]-[6.16] which can enlarge the top opening of the recessed profile while reducing the opening in the bottom region. Consequently, an undercut is formed beneath the spacer with an alignment to the gate edge. This leads to an extreme surface proximity-push suitable for the subsequent e-SiGe epitaxy process. The results of this study may provide a solution to the long-lasting problem of process instability caused by complicated e-SiGe recess-etch process.

4.2 Silicon Reflow Experiment in Hydrogen Ambient: Process Window and Results

The undertaken process flow is briefly described in Fig. 4.2. Following the gate patterning process, a spacer of ~15nm wide consisting of chemical-vapor-deposition (CVD) oxide and nitride was formed. Silicon was then etched to form an isotropic recess. An optional hydrogen annealing step was performed before e-SiGe epitaxy process. During the hydrogen annealing process, the reflow of silicon may occur, especially in the region where a large

curvature existed. The silicon tended to reduce surface energy through a reduction in the curvature. It is believed that the CVD liner oxide and silicon substrate were weakly bonded and can be separated during the hydrogen annealing process. In contrast, the gate oxide (thermally grown silicon oxide) and silicon substrate was strongly bonded. Silicon can therefore reflow with the aid of the hydrogen annealing process beneath the spacer, and this reaction will cease at the interface between silicon and the gate oxide at an appropriate hydrogen annealing temperature. Fig. 4.3(a) shows the TEM results of silicon-reflow under different annealing temperatures in the hydrogen ambient for 1 minute. At a low annealing temperature (750°C in this study), insufficient and asymmetric silicon-reflow under spacer was observed. An undercut was formed at one side between the gate edge and the spacer edge while no silicon-reflow occurred at the other side. This situation is definitely unacceptable because the device performance would vary seriously due to the unstable e-SiGe shapes. Under a moderate temperature (800°C), the silicon reflowed while stopping at the gate edges in a self-aligned manner. With a 50°C higher process temperature (850°C), the interface between gate oxide and silicon substrate did not split and no further silicon-reflow can take place. A self-aligned extreme e-SiGe surface proximity-push with a large margin of process temperature was therefore achieved by exploiting this self-aligned silicon-reflow (SASR) technique. Fig. 4.3(b) schematically compares the contours of e-SiGe between samples with and without SASR. Thanks to SASR, the e-SiGe contour in the middle and bottom regions was pushed away from the gate edge due to the redistribution of silicon. Hence, the sub-surface punch-through current can be suppressed as

will be discussed in the next section. SASR is, so far, the only published method that pushes e-SiGe surface proximity forwards gate edge and push e-SiGe bottom region away from channel region, simultaneously.

4.3 Device Analysis

In order to quantify the benefit in strain engineering by using SASR, we implemented the e-SiGe profiles of the control and SASR samples into a well calibrated TCAD simulator. The simulation results of mechanical strain are displayed in Fig. 4.4 which reveals the key advantage of SASR in strain engineering. The tip of the e-SiGe was modulated from sub-surface to the silicon surface. This led to a much closer e-SiGe surface proximity as compared to the control sample. According to the simulation results, the SASR sample exhibits a highly localized strain inside the channel region around the gate edge which is most efficient to enhance the carrier mobility. On the contrary, the control sample shows a highest strain outside the channel region and therefore a lower strain efficiency is evident as compared to the SASR sample. Without modifying the following e-SiGe epitaxy composition, the longitudinal compressive strain in the channel region of the SASR sample is increased by a factor of more than 15% and thereby a higher hole carrier mobility is expected as compared to the control sample.

In addition to the benefit resulting from higher strain efficiency, the hole carrier mobility and boron doping activation level are higher in SiGe as compared to those in silicon. Therefore, SASR can lower the R_{sd} as long as the e-SiGe stays at the gate edge. Here, a 14% difference in R_{sd} is obtained (as shown in Fig. 4.5) in terms of the statistical distributions in samples with and

without SASR. It is noted that the R_{sd} values are measured using the extraction method described in the previous work [6.17], [6.18]. The figure also clearly points out the fact that a tighter distribution of R_{sd} is associated with SASR. This implies that SASR can mitigate the process variation caused by the silicon-recess etching process.

Unlike the conventional proximity-push by using merely etching process which may potentially lead to undesirable short-channel-effect (SCE), SASR can actually alleviate the undesirable SCE because of a less encroachment of e-SiGe in the sub-surface region as depicted in Fig. 4.3(b). This was experimentally confirmed by the measured threshold voltage versus gate length (V_{th} vs. L_{gate}) characteristics as given in Fig. 4.6. The figure indicates that a higher degree of SCE suppression is achieved with the implementation of SASR. One should note that there is no other process difference between these two samples. The improvement in the SCE characteristics should purely result from SASR-induced e-SiGe profile change. Because of a higher V_{th} level in the short channel region by using SASR, we should have room to reduce the halo ion-implantation dose in order to further boost the device performance.

Fig. 4.7 compares and shows the measured I_{on}-I_{off} performance between the samples with and without using SASR. Evidently, a more than 10% improvement is obtained with SASR, which certainly can be attributed to the combinational effects of the higher hole carrier mobility and lower R_{sd} as mentioned above. The variation in the I_{on}-I_{off} performance is also significantly reduced in the presence of SASR. Both the tightened distributions of R_{sd} and I_{on}-I_{off} performance reflect the advantage of this self-aligned process (SASR)

over the conventional approaches.

4.4 Conclusion

An integration-friendly and cost-effective process used for strain engineering, SASR, is at the first time highlighted in this chapter. Owing to the nature of self-aligned silicon-reflow in the hydrogen ambient, extreme surface proximity-push is achieved without using sophisticated etching process. SASR is proven stable in a wide range of process temperature, which is highly desired in the advanced CMOS manufacturing.

Significantly improved I_{on}-I_{off} performance is experimentally demonstrated by implementing SASR on a 40nm technology pMOSFET, resulting from the combinational effects of the higher hole carrier mobility and lower R_{sd}. The statistical distributions of R_{sd} and I_{on}-I_{off} performance are tightened up for the reason that the e-SiGe proximity-push is realized in a self-aligned manner. Improved drain-induced-barrier-lowering (DIBL) is also obtained because of a less e-SiGe encroachment in the bottom region. These analyses are supported by TEM photos and corroborated by TCAD simulation. Our study may provide an alternative approach to the extreme e-SiGe surface proximity for the current and coming VLSI generations.

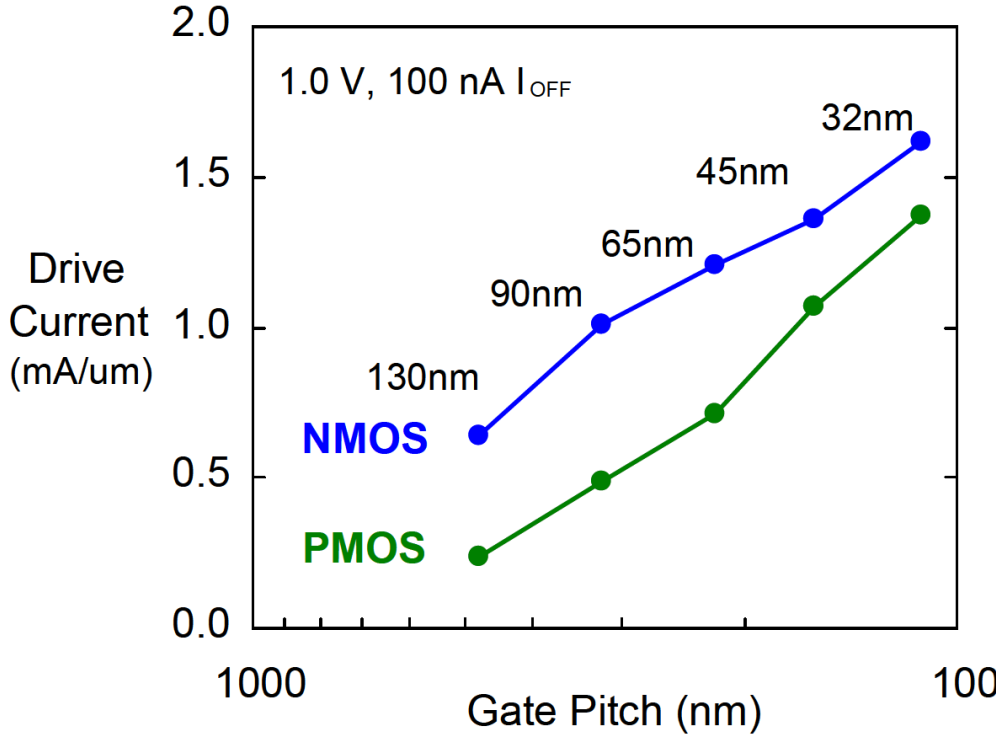


Fig. 4.1 Cross-generation drive current (drain current measured at V_g=V_d=1V) comparison [4.13]. The gap between NMOS and PMOS decreased constantly from 90nm to 32nm technology. The strain and R_{sd} engineering of e-SiGe played an important role in the PMOSFET performance enhancement.

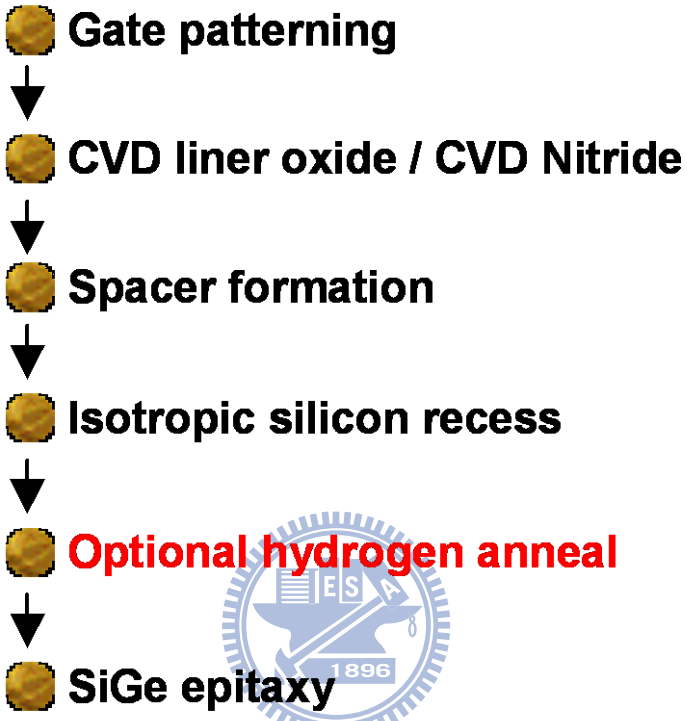


Fig. 4.2 A brief process flow in the e-SiGe formation loop. An optional hydrogen annealing step is inserted before e-SiGe selective epitaxy process.

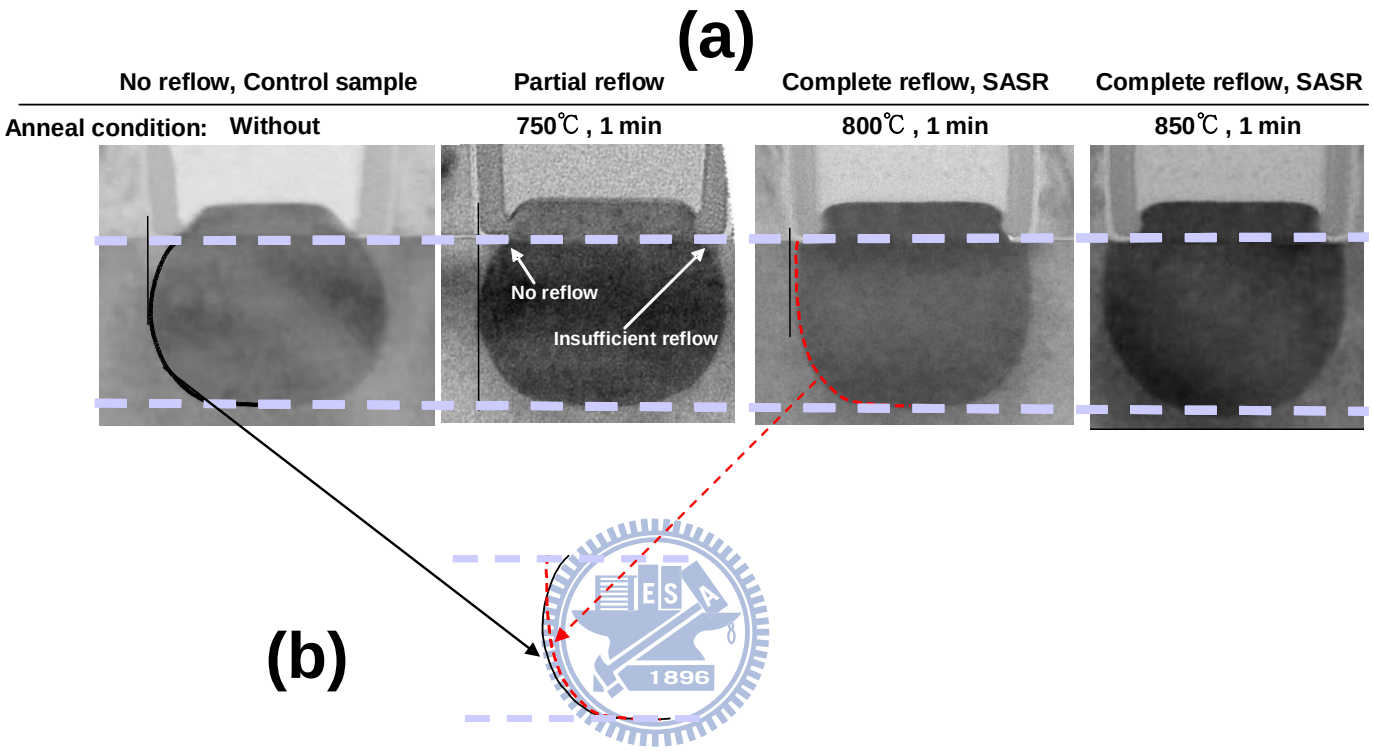


Fig. 4.3(a) Cross-sectional TEM analyses of e-SiGe profile under different hydrogen annealing temperatures. Complete and self-aligned silicon-reflow occurs above a moderate temperature which is 800°C in this work. Wide process window of annealing temperature is demonstrated. The hydrogen annealing time is 1minute for each process.

Fig. 4.3(b) A comparison of e-SiGe contour between the control sample and SASR. SASR provides a closer proximity at the top and less e-SiGe encroachment at the middle and bottom regions.

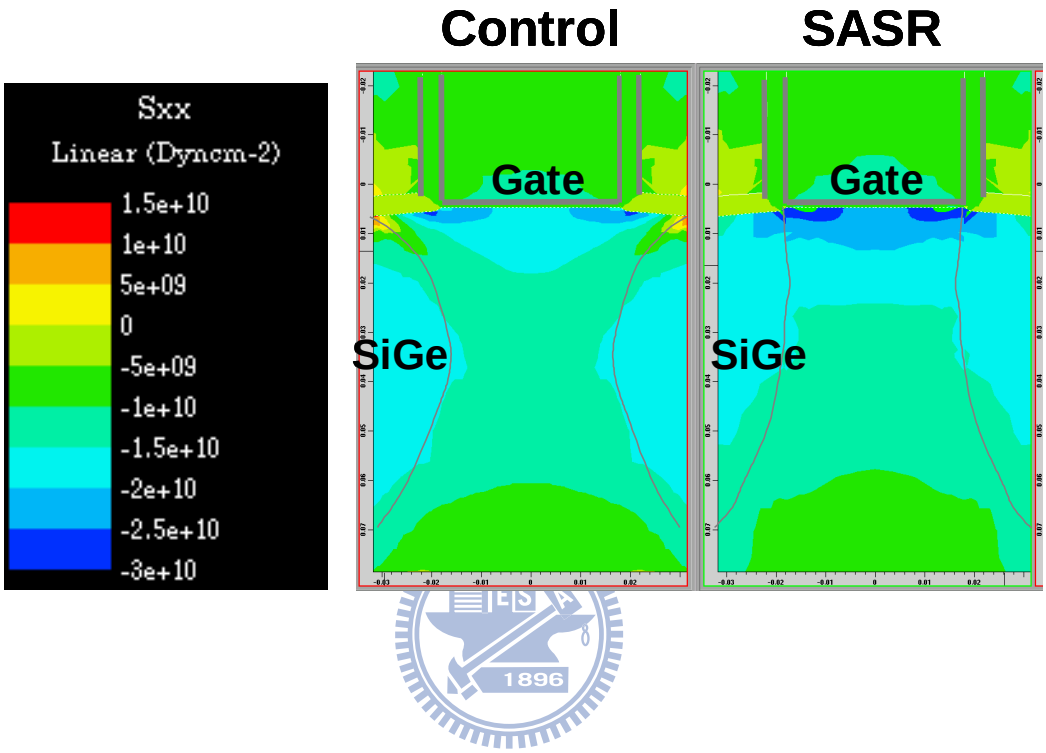


Fig. 4.4 A two-dimensional TCAD simulation of stress distribution along the channel direction. SASR provides higher compressive stress which improves hole carrier mobility.

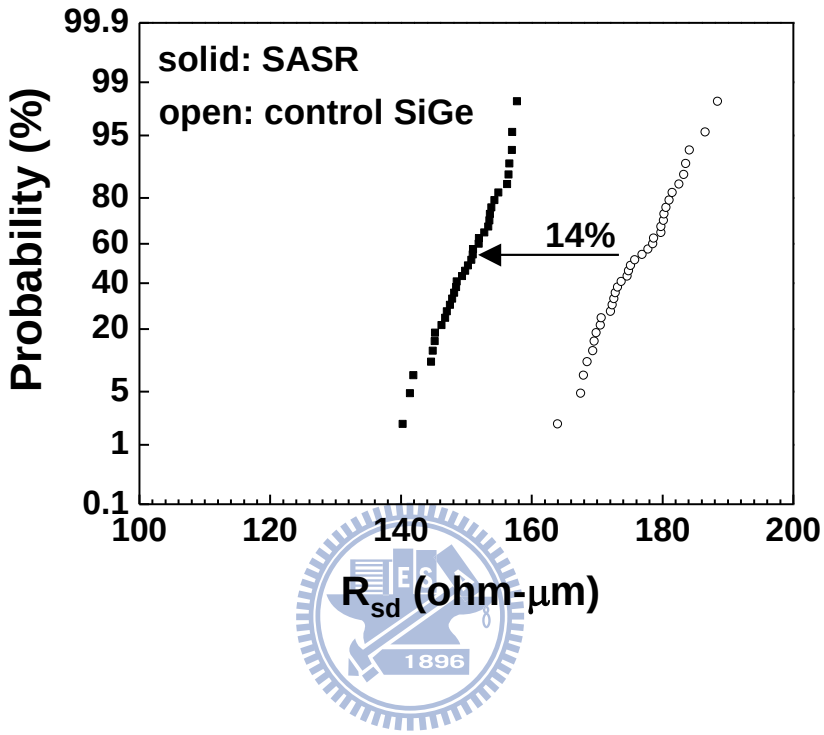


Fig. 4.5 SASR leads to lower source/drain series resistance. The tighter distribution implies that SASR mitigates the device variation resulting from the silicon-recess process.

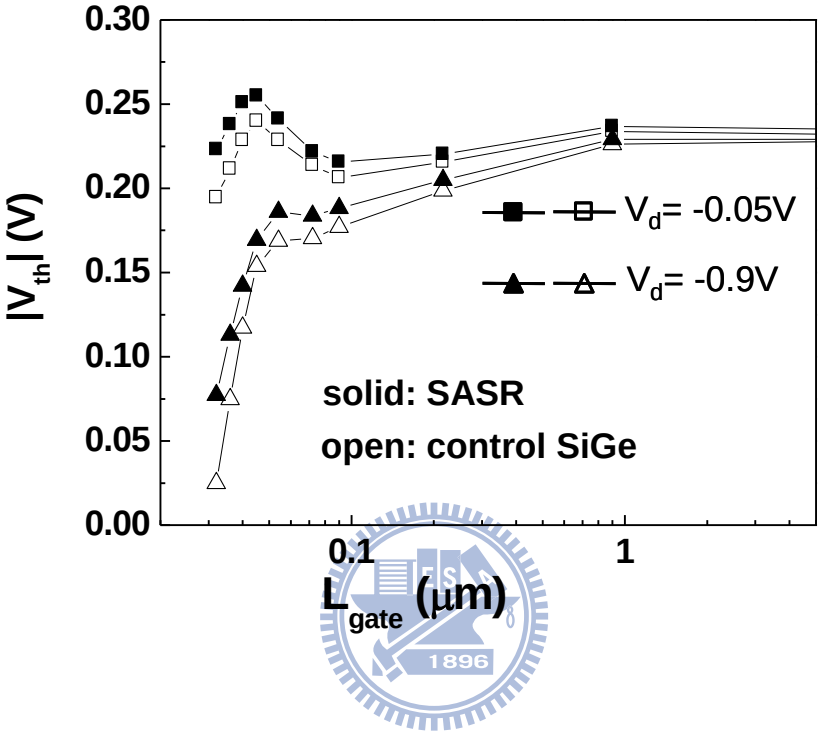


Fig. 4.6 SASR leads to a better immunity against undesired SCE degradation because of a less e-SiGe encroachment at the middle and bottom region.

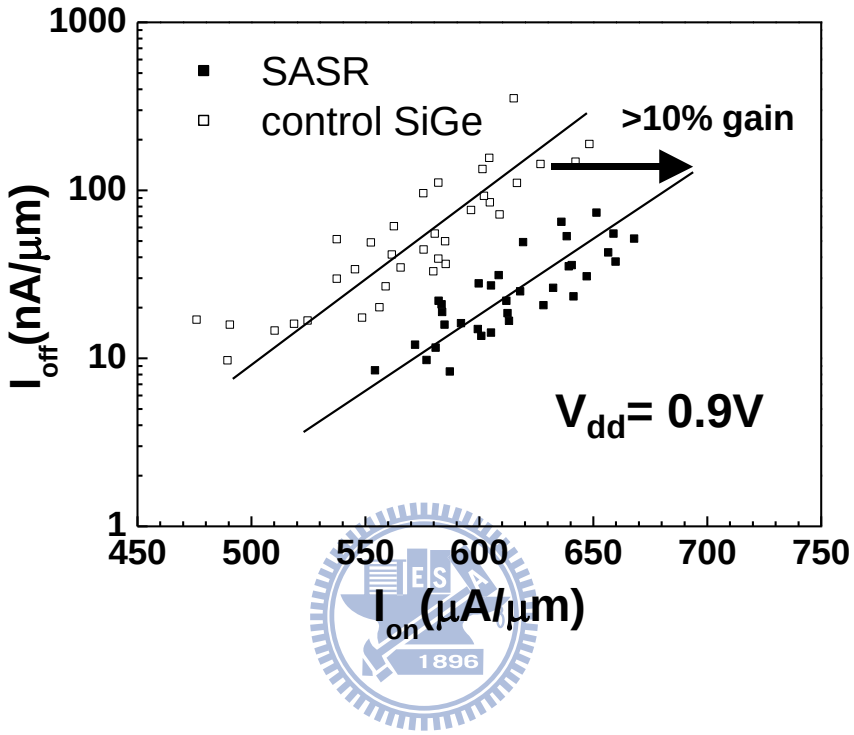


Fig. 4.7 SASR improves I_{on}-I_{off} performance by more than 10% as compared to the control-sample. It also tightens the I_{on}-I_{off} distribution because the surface proximity is created in a self-aligned manner.

Chapter 5

USJ Engineering:

A Novel Ultra-Shallow-Junction (USJ) Technique for MOSFET under Low-V_{dd} Operation

5.1 Preface

The issues of integrated-circuit power consumption and heat dissipation are increasingly difficult to handle because of the increasing leakage current, switching-speed and MOSFET density. Reducing applied-bias (V_{dd}) is therefore inevitable in order to keep reasonable power consumption for the modern VLSI MOSFETs. However, the MOSFET threshold voltage (V_{th}) is not scaled down at the same ratio as V_{dd} for the purpose of suppressing sub-threshold leakage current. As a result, the gate voltage (V_g) overdrive headroom (V_g-V_{th}) decreases and device/circuit performance becomes susceptible to both V_{dd} and V_{th} variations. In order to achieve low V_{th} and low off-stage leakage (I_{off}), abrupt MOSFET on-off transition is highly demanded.

We defined an index to evaluate the abruptness of on-off transition in this work. The abruptness of on-off transition between sub-threshold region and strong turn-on was quantified by the difference between V_{th_lin} (extracted using constant-current method in the sub-threshold region where $\log(I_d)$-V_g keeps a simple slope, or deep sub-threshold region) and V_{th_gm} (extracted using maximum transconductance method in the on-state). As V_{th} keeps reducing for low V_{dd} operation, gate voltage consumed in the deep

sub-threshold region decreases consequently. In addition to the deep sub-threshold region, one should also pay attention to the voltage drop consumed by the on-off transition region, namely the difference between V_{th_gm} and V_{th_lin}.

In order to constantly reduce MOSFET feature size, the channel doping profile engineering with heavy ion-implantation (I/I) dose and localized halo I/I in the vicinity of gate edge have been widely used to maintain a reasonable sub-threshold swing for the short channel devices [5.1-5.7]. With a heavy and localized doping profile in the channel region, the short channel effect can be successfully suppressed. However, this approach degrades carrier mobility because of the increased impurity scattering rate. In addition, junction capacitance (C_{jb}) and junction leakage current increase evidently as a result of the strongly coupled S/D-substrate junction [5.8-5.9]. Moreover, the issues of reliability degradation caused by heavily doped junction are often observed [5.10]. This approach also increases channel-depletion capacitance (C_d) and weakens gate-control due to a high C_d/C_g ratio (C_g: gate-to-channel capacitance) [5.11-5.12]. In addition to the aggressive channel doping engineering, more attention should be paid to the abruptness of S/D-ext doping profile. With an abrupt S/D-ext doping profile, good electrostatic control can be achieved with a low substrate and/or halo I/I dose. Therefore, the aforementioned issues can be alleviated.

In this work, the doping abruptness of shallow source/drain-extension (S/D-ext) was investigated in order to characterize its impact on V_{th_gm} - V_{th_lin}. By utilizing a novel I/I technique featuring pre-amorphization-implantation (PAI) using light species at a high dose rate [5.13-5.17], boron USJ was

achieved without degrading doping activation. Therefore, a lower halo I/I dose can be used to sustain a similar short-channel-effect (SCE) performance. The reduction of depletion capacitance leaded to a significantly faster on-off transition between V_{th_lin} and V_{th_gm}. A lower sensitivity of device driving force (I_{on} and I_{eff} [5.18]) as well as circuit speed against V_{dd} variation was proven experimentally.

The objective of this work is to accentuate the importance of a reduced V_{th_gm} - V_{th_lin} to the low-V_{dd} operation and to provide a novel doping technique in order to experimentally achieve a reduced V_{th_gm} - V_{th_lin}. The results contained in this work will help the modern MOSFET designers understand more about the device operation in the low V_{dd} regime.

5.2 A New Concept of Doping Technique

Halo I/I is frequently used to control short-channel-effect and to adjust V_{th} in modern MOSFETs. As shown in Fig. 5.1, without adjusting S/D-ext doping abruptness, a higher halo I/I dose leads to an insignificantly lower sub-threshold swing for the short channel devices (Standard-V_{th} and Low-V_{th} PMOSFETs in [5.19]). However, a larger gap between V_{th_lin} and V_{th_gm} are clearly demonstrated for the device using higher halo I/I dose. This means a slower transition from off-state to on-state and degraded gate overdrive headroom. Therefore, the negative impact on electrostatic characteristic of heavy substrate doping is obvious in this transition region. In order to reduce halo I/I dose, shallow and abrupt S/D-ext is highly demanded. USJ formation has been one of the most critical tasks for many generations of VLSI technology. With the aim of creating an abrupt boron S/D-ext, many I/I

techniques, such as heavy mass molecule I/I and PAI using heavy ions, are intensively investigated in the past decades [5.20-5.22].

Unlike the traditional approaches, a novel USJ formation technique featuring PAI with light species in a plasma environment under a high dose-rate is utilized in this work. The accumulation of crystal defects during I/I is more effective as dose-rate increases [5.17]. This can be attributed to the fact that fast impinging dose rate can reduce the possibility of recombination of silicon interstitial and vacancy between two individual impinging events. Therefore, light species can form PAI layer when the I/I dose-rate is high enough. The as-implanted boron doping profile, analyzed by using secondary-ion-mass-spectroscopy (SIMS), is shown in Fig. 5.2 along with other I/I techniques. The doping profile shows a sharp transition from the peak concentration down to the resolution limitation of the SIMS analysis while the traditional approaches show either obvious profile tailing or worse doping abruptness in the entire range. This excellent doping abruptness leads to less dopant compensation between S/D-ext and halo I/I dose. Hence, a lower halo I/I dose can be used to maintain a similar SCE behavior. This novel I/I technique also leads to a significant improvement in R_s-X_j as shown in Fig. 5.3. It is believed that the end-of-range (EOR) defects caused by lighter species are easier to be annealed out [5.17]. A higher boron activation level is therefore achieved as compared to the traditional approaches. The reduced EOR defect also guarantees a reduced transient-enhanced-diffusion (TED) of both the S/D-ext and the halo dopant upon following annealing processes. As a result, both abrupt S/D-ext and halo doping profiles can be achieved. The halo I/I dose effectiveness can be further improved due to the improved halo

doping abruptness. Combining the effects of reduced doping compensation and improved doping abruptness, our novel doping technique significantly improved halo I/I dose effectiveness (by 30% in this work) over the traditional approach. Hereafter, we named this "abrupt S/D-ext + low halo I/I dose" as "new approach"

5.3 Device Characterization

5.3.1 Effects of Doping Abruptness on DC & AC

As compared to the traditional I/I approach that utilized heavy ion PAI prior to the S/D-ext IMP (hereafter named as reference approach), our new approach exhibits a weaker reverse-short-channel-effect (RSCE), lower DIBL and lower V_{th} roll-off slope as shown in Fig. 5.4. Gamma-L_{mask} curves (Fig. 5.5) indicate the fact that the effective substrate doping concentration is lowered by using new approach especially for short channel devices for which significant overlap of halo I/I dose takes place. Fig. 5.6 compares the junction leakage currents of the short channel devices with the same V_{th_sat} as shown in Fig. 5.4. The new approach provides an obviously lower junction leakage than the reference approach. It reflects the truth that our new approach reduces the residual defects caused by I/I.

I_d-V_g characteristics are shown in both linear-scale and logarithmic-scale in Fig. 5.7. In order to match V_{th_lin} between the new approach and the reference approach, about 30% lower halo I/I dose was used in the new approach as compared to that used in the reference approach. Sub-threshold swing shows no significant difference between two approaches while V_{th_gm} - V_{th_lin} is obviously lower, namely a faster on-off transition, for the new

approach. The difference in the abruptness of on-off transition is statistically proven and shown in Fig. 5.8.

The key device parameters are summarized in Table 1. Junction capacitance, junction leakage and Gamma are reduced obviously because of a significantly reduced halo I/I dose in the new approach. The obvious improvement in G_m/G_{ds} (gain factor measured at L_{mask}=1μm) is also beneficial to analog applications. With a shallower and more abrupt S/D-ext doping profile resulting from our new approach, a similar R_{sd} (S/D serious resistance extracted using method introduced in [5.23]) is achieved as compared to the reference approach. It reflects that truth that an improved doping activation of S/D-ext dopant compensates for the effects of a shallower junction.

The reduction of halo I/I dose also leads to better carrier mobility in addition to higher gate voltage overdrive. Higher driving force and higher trans-conductance are achieved by using our new approach as illustrated in Fig. 5.9. The obviously improved trans-conductance is the best evidence of improved carrier mobility. Fig. 5.10 compares the I_{on}-I_{off} performance between the reference approach and the new approach. A significant I_{on}-I_{off} improvement of more than 7% was achieved by using our new approach. In terms of I_{eff} [5.18] performance, IL (drain current measured at V_g= 0.5V_{dd}, V_d = V_{dd}) was further improved because of a higher gate overdrive voltage as shown in Fig. 5.11. Therefore, 10% I_{eff}-I_{off} improvement is achieved as shown in Fig. 5.12. It is evident that the improvement in I_{eff}-I_{off} is more profound than that in I_{on}-I_{off} when the gate overdrive voltage is increased.

The comparisons of inverter ring-oscillator time-delay (T_d) are illustrated in Fig. 5.13 and Fig. 5.14. Evident improvement was demonstrated even

though this new approach was applied for only PMOSFETs in this work. By utilizing the new approach, the improvement in T_d is more profound than what I_{eff} predicts (Fig. 5.13). The obviously different T_d-I_{eff} characteristics between these two approaches strongly suggests different capacitive loading during the ring-oscillator switching. The 6% faster T_d at the same I_{eff} is believed to be the combinational results of lower channel depletion capacitance and lower junction capacitance as shown in Table 5.1. As depicted in Fig. 5.14, 8% faster T_d is observed at the same standby leakage.

5.3.2 Effects of Doping Abruptness on V_{dd}-sensitivity

With a higher V_g overdrive resulting from fast on-off transition by utilizing new approach, a lower V_{dd}-sensitivity is expected for the driving force as well as the circuit performance. In order to compare V_{dd}-sensitivity, I_{on} and I_{on}-I_{off} performance are normalized to the values at V_{dd}=1V for the reference device and the one using new approach, respectively. Fig. 5.15 clearly indicates a lower sensitivity of I_{on} and I_{on}-I_{off} performance against V_{dd} variation by using new approach. The same behavior is also evident for I_{eff} and I_{eff}-I_{off} performance as demonstrated in Fig. 5.16. This guarantees a lower sensitivity of circuit speed variation against V_{dd} variation as shown in Fig. 5.17. Therefore, our new approach renders the circuit more applicable for low V_{dd} operation.

5.3.3 Effects of Doping Abruptness on Reliability

Driving force degradation caused by hot-carrier-injection (HCI) stress is one of the critical concerns for abrupt junction. However, this new approach

forms shallow junction and maintain short-channel electrostatic control by improving the intrinsic S/D-ext doping abruptness instead of using heavy halo I/I dose. In fact, the halo I/I dose is reduced by 30% in the new approach as compared to the reference approach. A lower electrical field is hence expected in the p/n junction between p-type S/D-ext and n-type halo region. Therefore, no degradation in HCI lifetime is observed as clearly illustrated in Fig. 5.18.

5.4 Conclusion

A critical index, V_{th_gm} - V_{th_lin}, describing MOSFET on-off transition characteristics is presented and experimentally discussed in this work. Unlike the conventional emphasis on the only deep sub-threshold region, this index is increasingly important to the advanced nano-scale MOSFETs for the low-V_{dd} and low-V_{th} operation because this on-off transition region comprises an increasing portion of gate voltage consumed before turn-on when both V_{dd} and V_{th} are scaled down. A novel USJ formation technique, featuring fast PAI using light I/I species at a high dose-rate, is introduced in this work to successfully reduce the gap between V_{th_gm} and V_{th_lin} by creating abrupt S/D-ext doping profile and reducing halo I/I dose. The improvement in gate voltage overdrive and carrier mobility leads to 10% higher driving force. Finally, low V_{dd}-sensitivities in both DC performance and circuit speed are successfully demonstrated.

The fundamental concept of this novel technique is applicable for both n-type and p-type USJ formation although it was utilized for boron S/D-ext in this work. We believe this concept can be easily applied to phosphorus

S/D-ext. Arsenic has been used as the major n-type S/D-ext doping species because of its lower diffusivity as compared to phosphorus. However, the phosphorus doping activation level is about twice as compared to that of arsenic. Therefore, phosphorus S/D-ext is highly promising as long as its doping abruptness can be as good as arsenic. The results in this work should be very important to the investigation of using phosphorus as S/D-ext.

PMOS key parameters	Reference device	New approach
Cjb (fF/μm^2)	ref.	-11%
Bulk junction leakage	ref.	-60%
Gm/Gds @ L_{mask}=1μm	ref.	34%
DIBL @ L_{mask}=40nm	ref.	-10mV/V
Gamma @ L_{mask}=40nm	ref.	-24%
Swing @ L_{mask}=40nm	ref.	equal
R_{sd}* (ohm-μm)	ref.	equal

*extracted using method introduced in Chapter 2

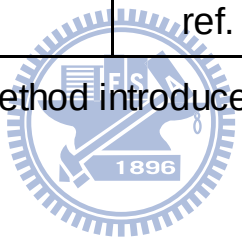


Table 5.1 A summary table of key DC and AC parameters. New approach (Abrupt S/D-ext + low halo I/I dose) gives a better short channel control and analog performance without degrading S/D series resistance.

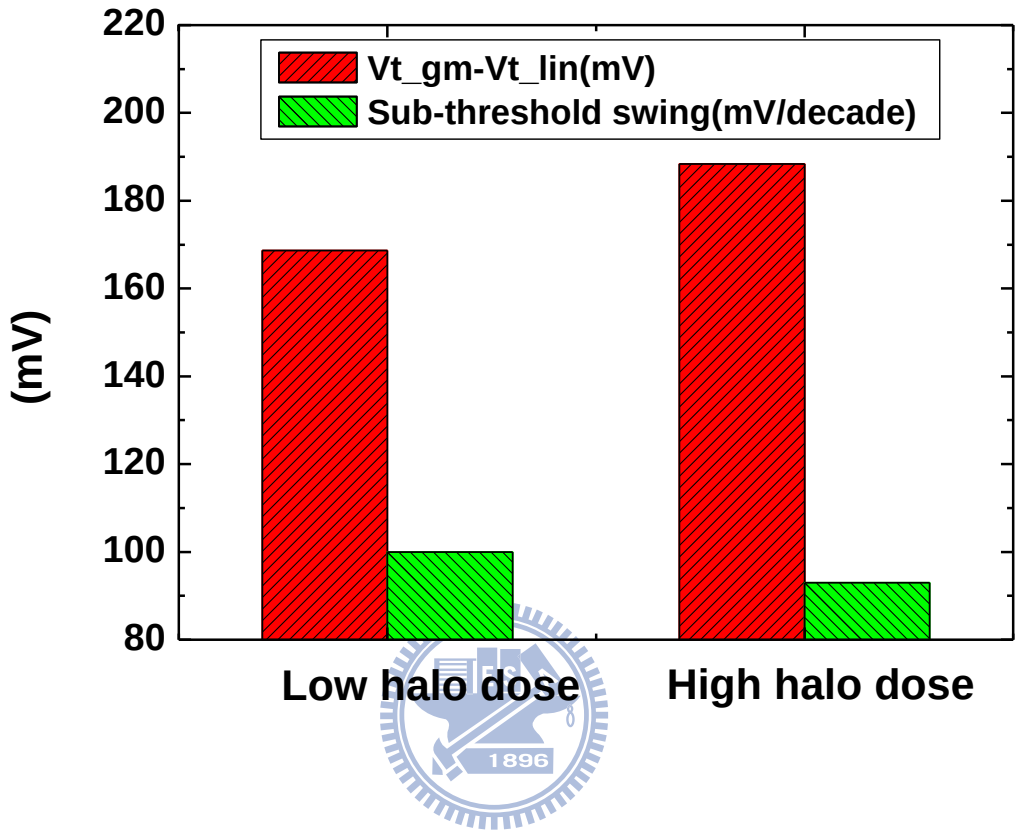


Fig. 5.1 Higher halo I/I dose leads to slightly lower sub-threshold swing but a larger gap between V_{th_gm} and V_{th_lin}. Gate overdrive is therefore degraded.

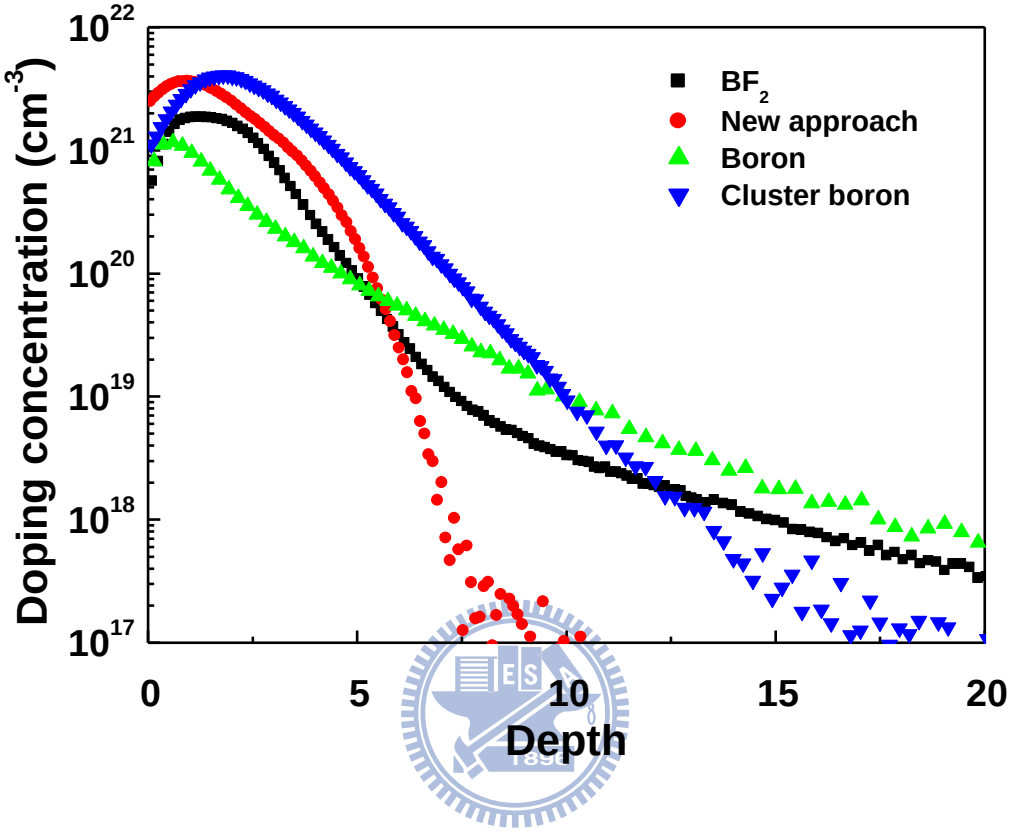


Fig. 5.2 Excellent as-implanted boron doping abruptness is achieved by using an I/I technique featuring PAI with light species. Other traditional approaches show either worse abruptness or profile tailing.

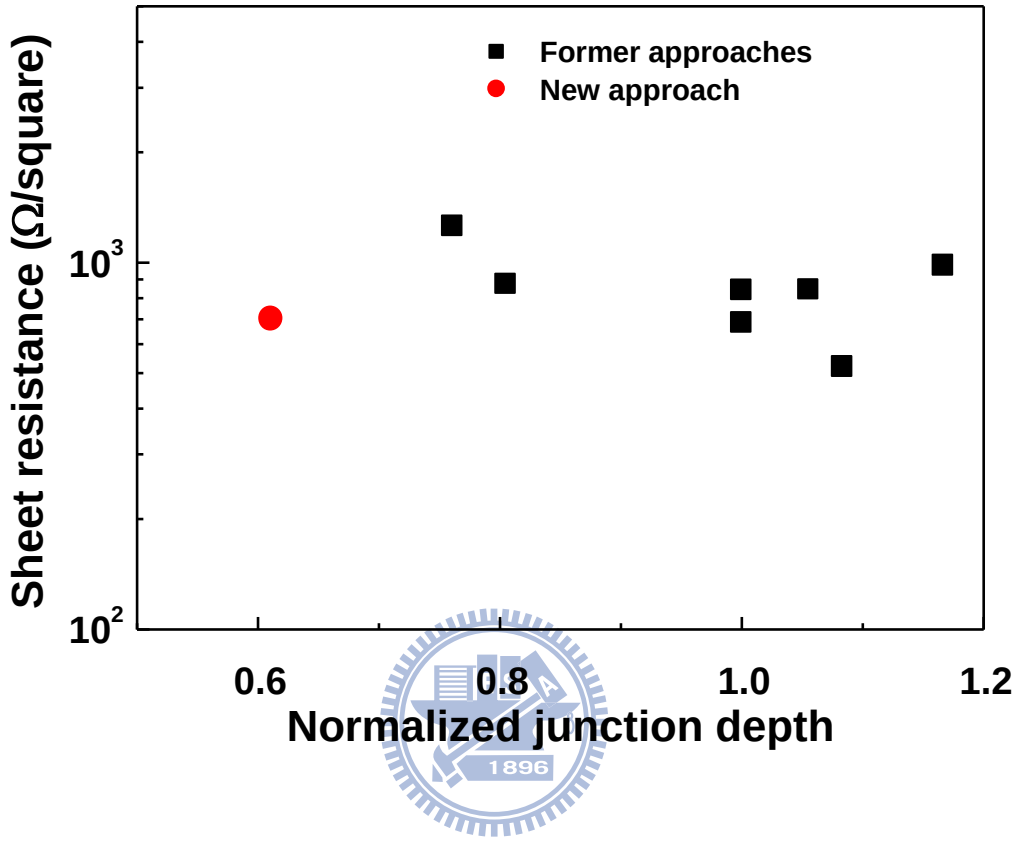


Fig. 5.3 Better R_s-X_j performance of boron USJ is observed by using new I/I technique. Highly activated boron dopant is achieved with 40% shallower X_j. R_s-X_j behaviors of both BF_2 and cluster boron are included in "Former approaches".

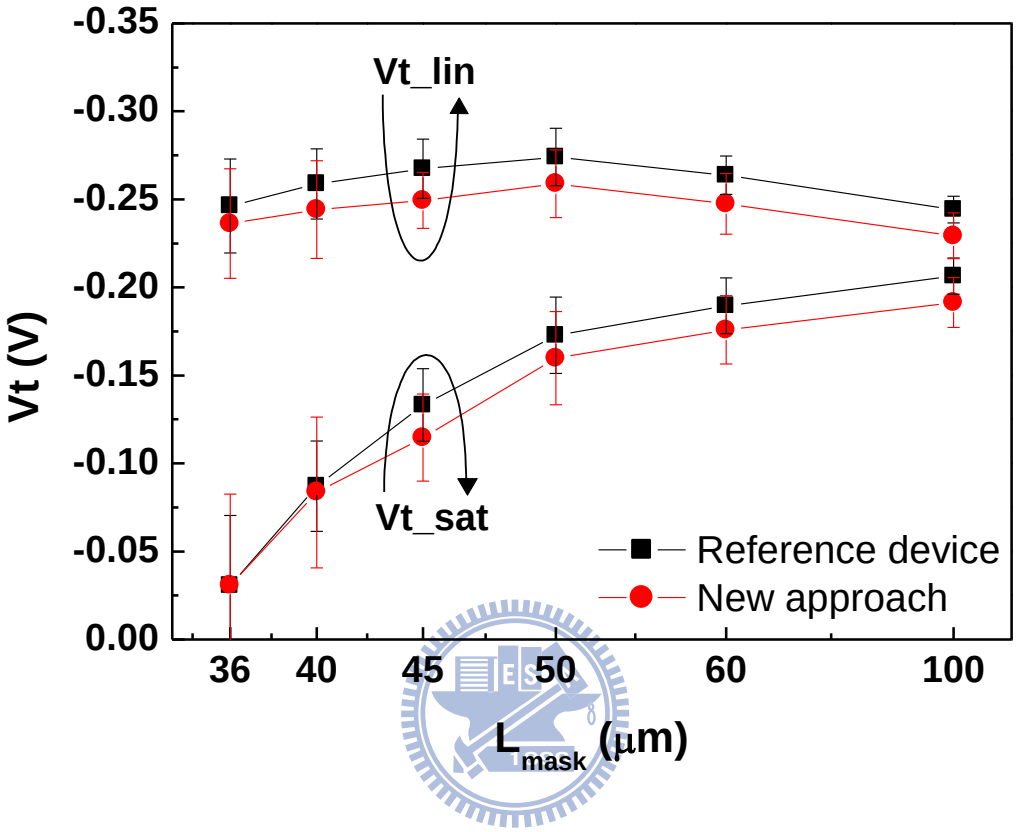


Fig. 5.4 New approach gives a weaker reverse-short-channel-effect (RSCE) which indicates a lower substrate doping concentration. Both V_{th} roll-off slope and DIBL are improved in the short channel regime. V_{th_lin} and V_{th_sat} are the threshold voltage extracted using constant-current method at V_d=50mV and 1V, respectively.

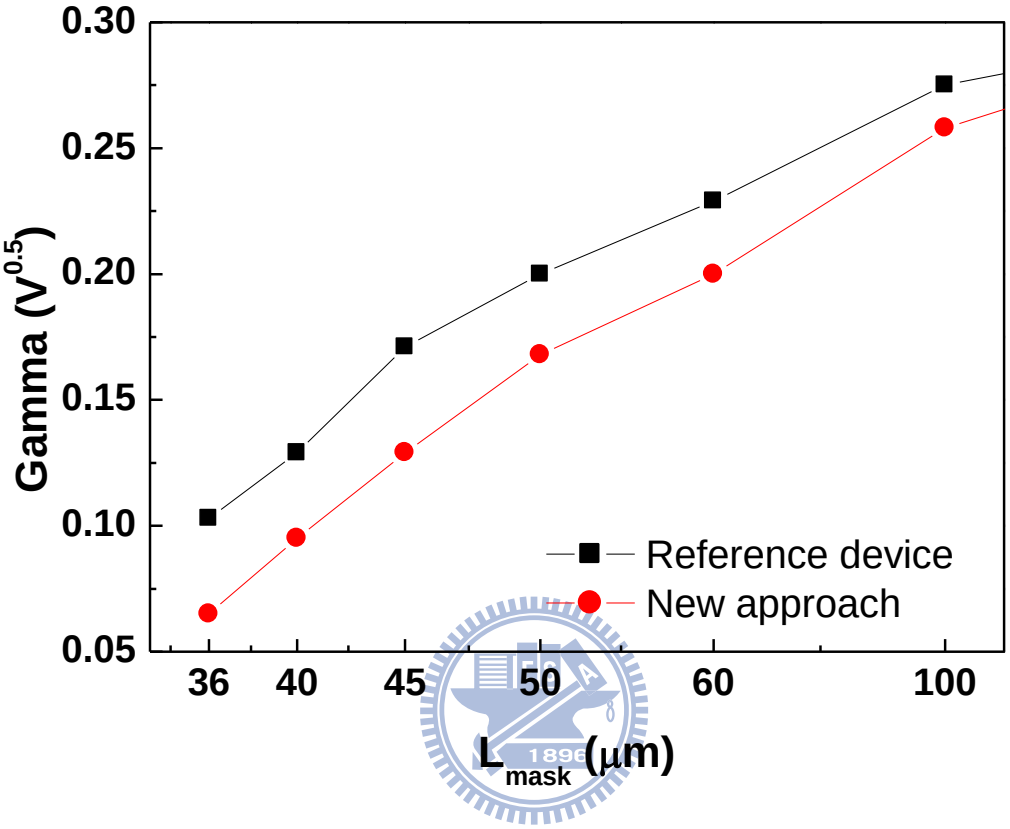


Fig. 5.5 New approach leads to a lower body-bias sensitivity in the short channel regime because of a lower substrate doping concentration resulting from lower halo I/I dose.

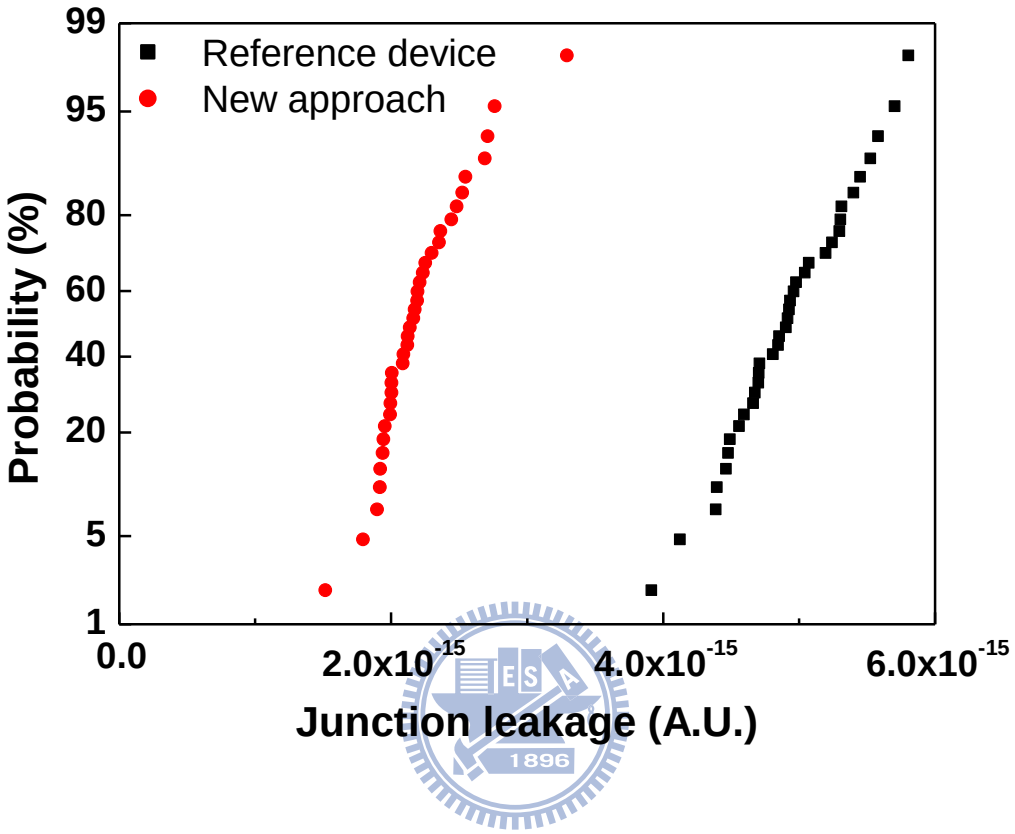


Fig. 5.6 Lower junction leakage is observed for new approach. Lower halo I/I dose and less EOR defects are believed to be the key contributors.

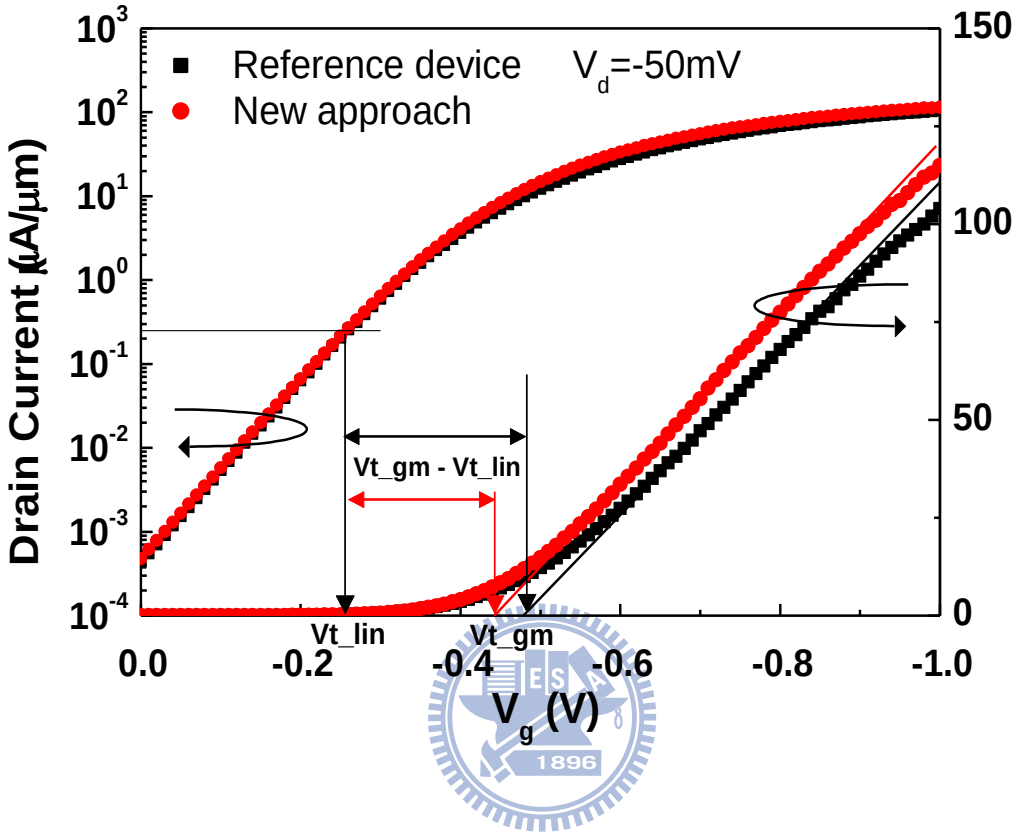


Fig. 5.7 New approach leads to a lower V_{th_gm} – V_{th_lin} as V_{th_lin} values are similar. This behavior guarantees no I_{off} increase but an I_{on} improvement because of a higher gate overdrive.

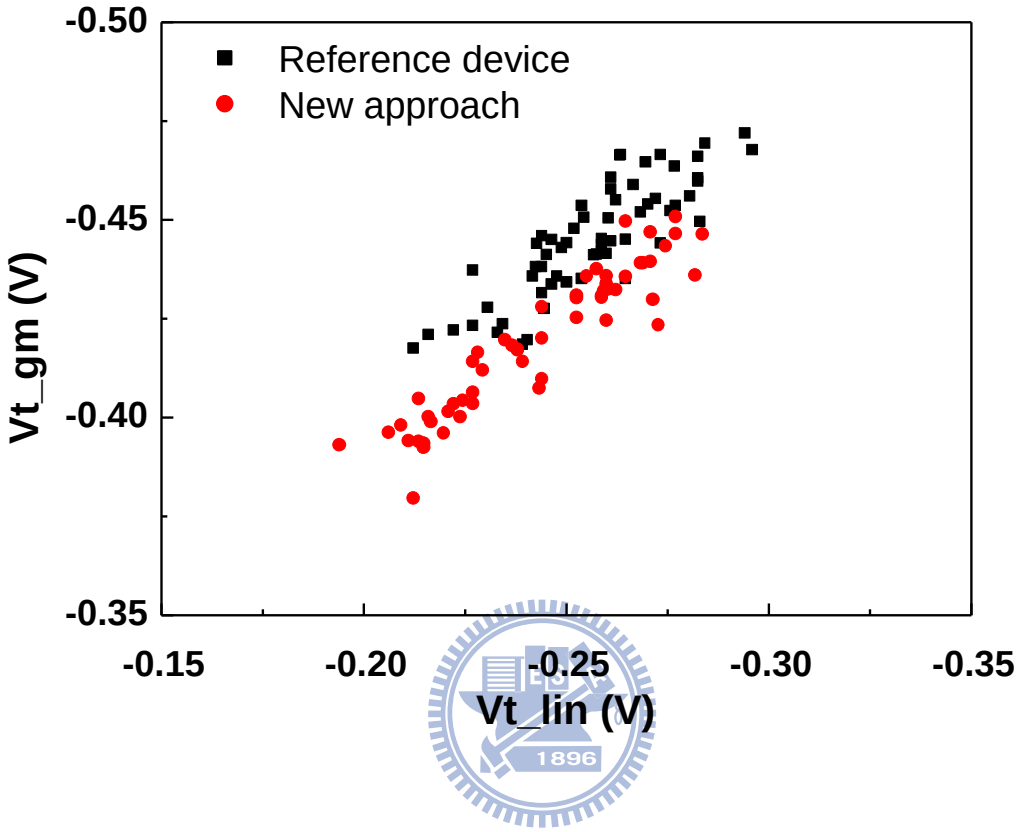


Fig. 5.8 A clear statistical trend of V_{th_gm} – V_{th_lin} is demonstrated for short channel devices. Devices using new approach obviously outperform the reference ones.

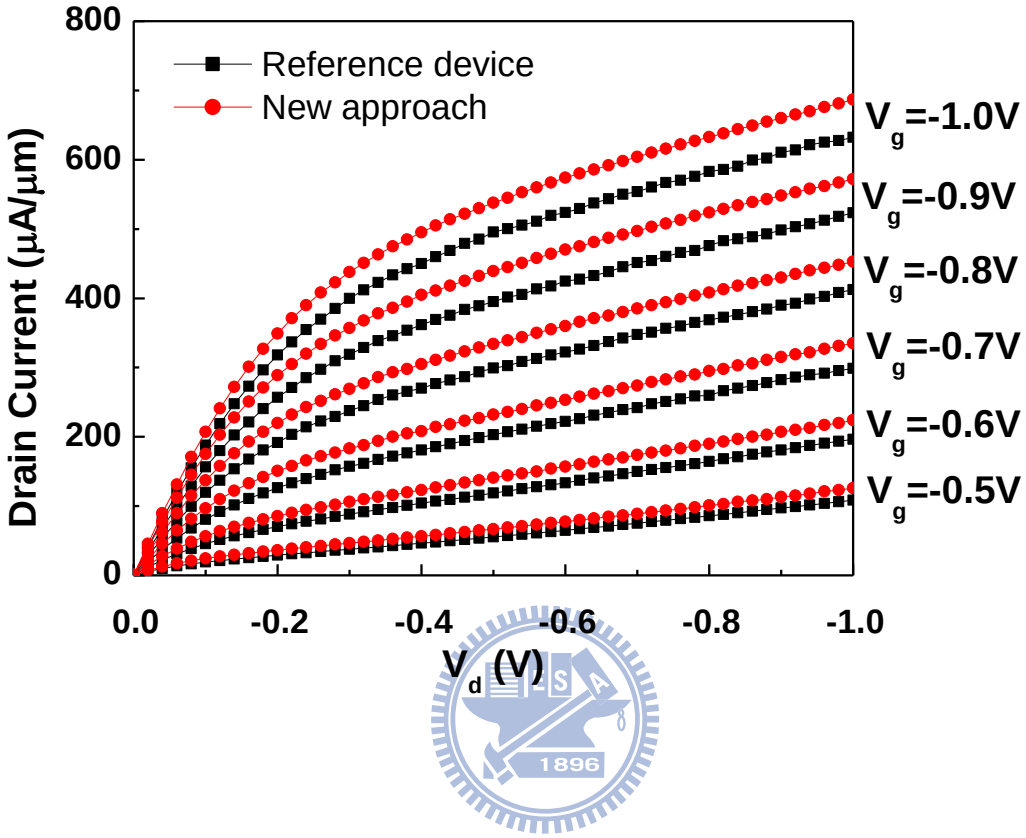


Fig. 5.9 I_d-V_d curves show higher G_m and driving force for new approach. This indicates a higher mobility caused by reducing halo I/I dose.

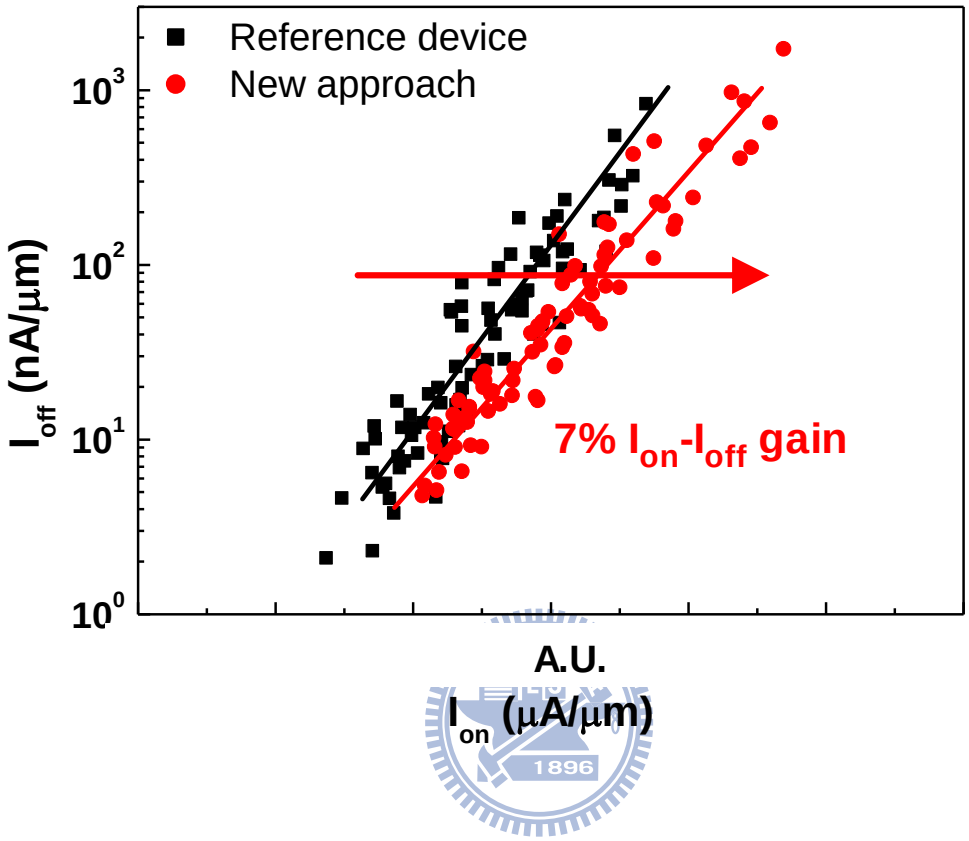


Fig. 5.10 7% PMOSFET I_{on}-I_{off} gain at V_{dd} = 1V is achieved by using new approach.

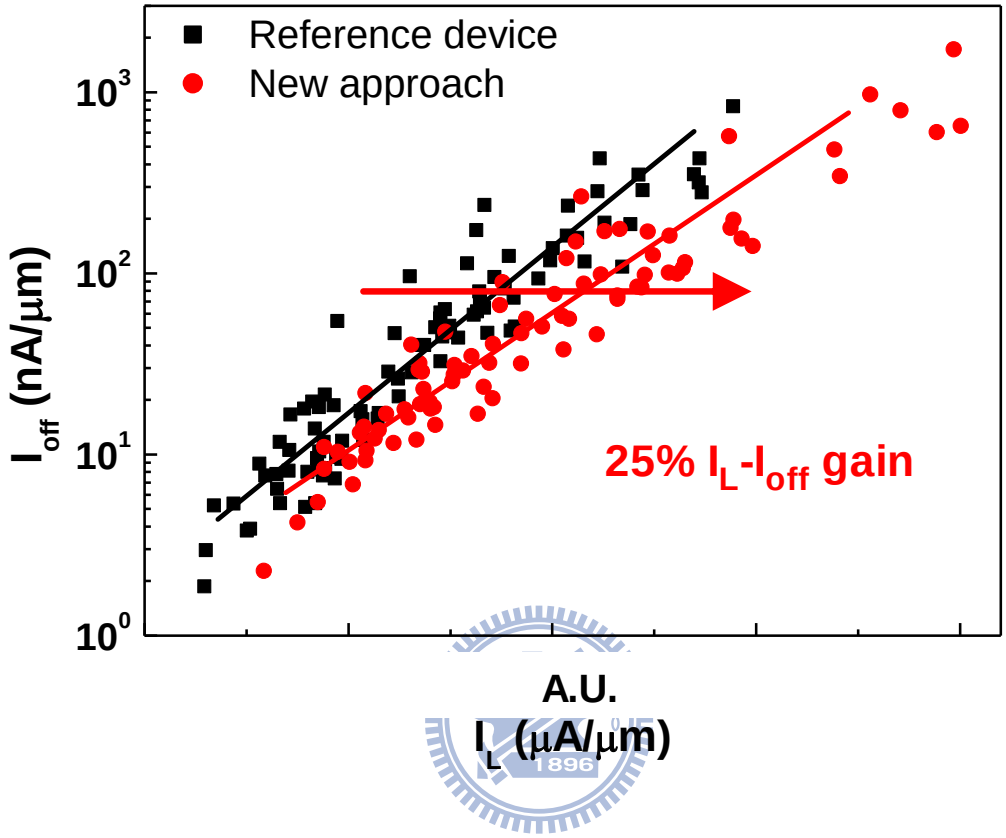


Fig. 5.11 Because of higher carrier mobility and higher gate overdrive, 25% PMOSFET I_L-I_{off} gain at V_{dd} = 1V is achieved by using new approach. (I_L is I_d measured at V_d=V_{dd}, V_g=0.5V_{dd})

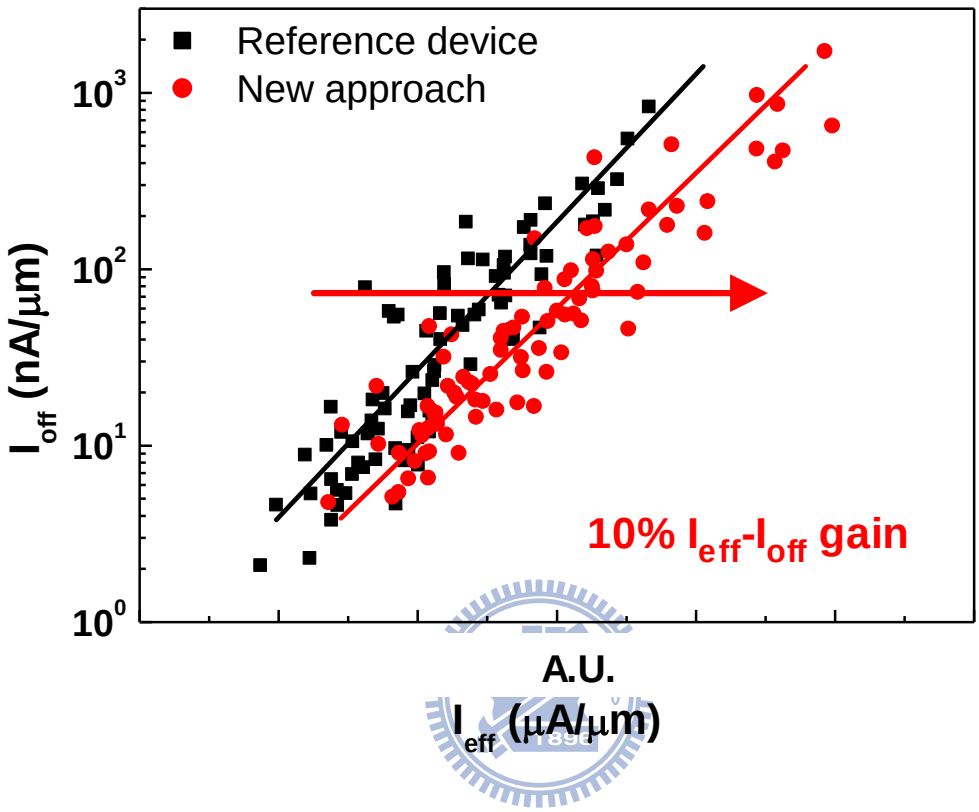


Fig. 5.12 I_{eff}-I_{off} gain (10%) is more obvious than I_{on}-I_{off} gain (7%) by using new approach. Significant I_L increase is the major reason. I_{eff} = $0.5(I_H+I_L)$, where I_H is I_d measured at $V_d=0.5V_{dd}$, $V_g=V_{dd}$.

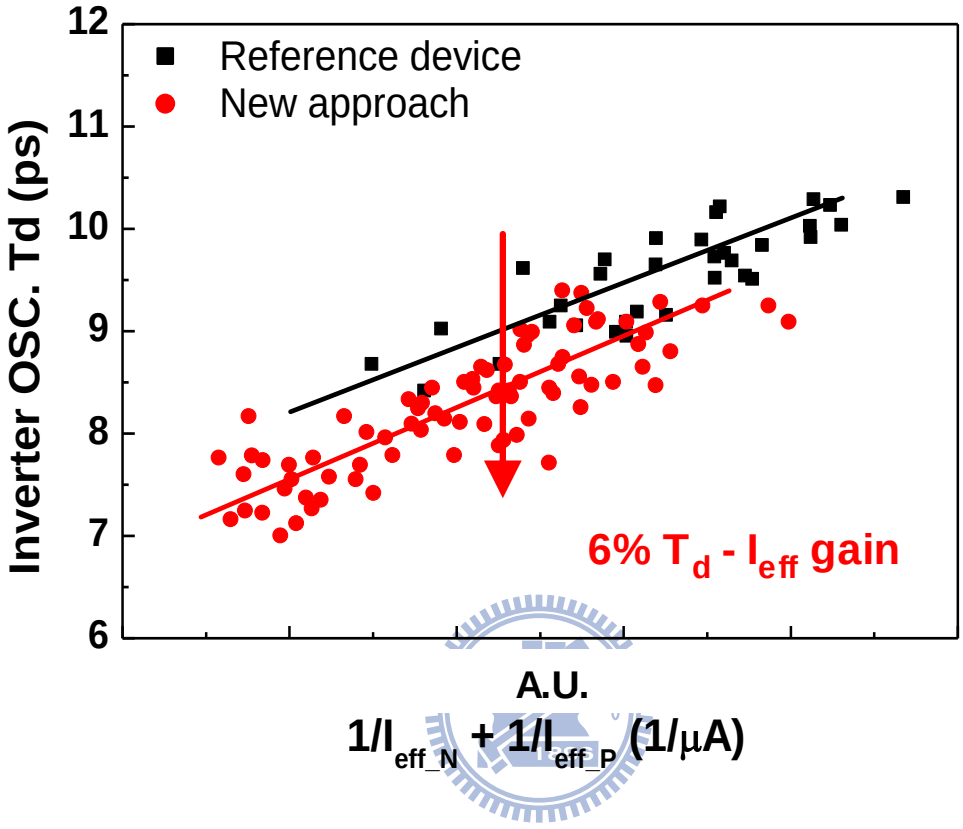


Fig. 5.13 New approach leads to 6% faster T_d at a given I_{eff}. It is believed to be the combinational results of lower channel depletion capacitance and lower junction capacitance.

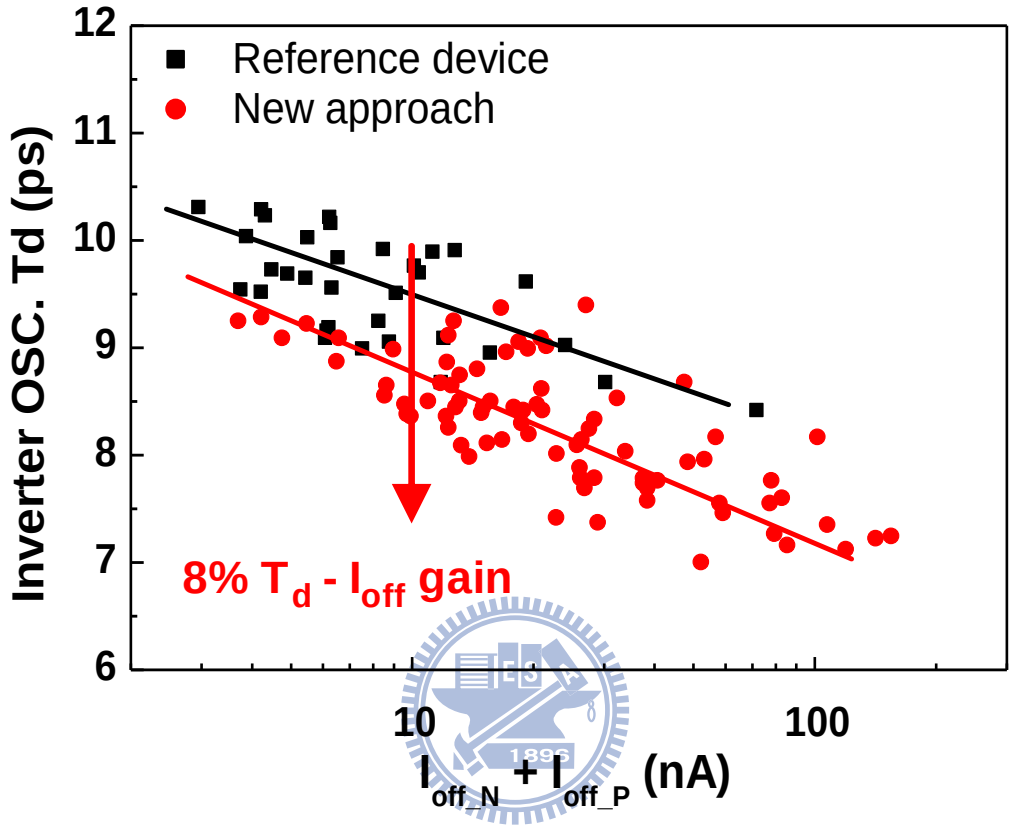


Fig. 5.14 New approach leads to 8% faster T_d at a given standby leakage current.

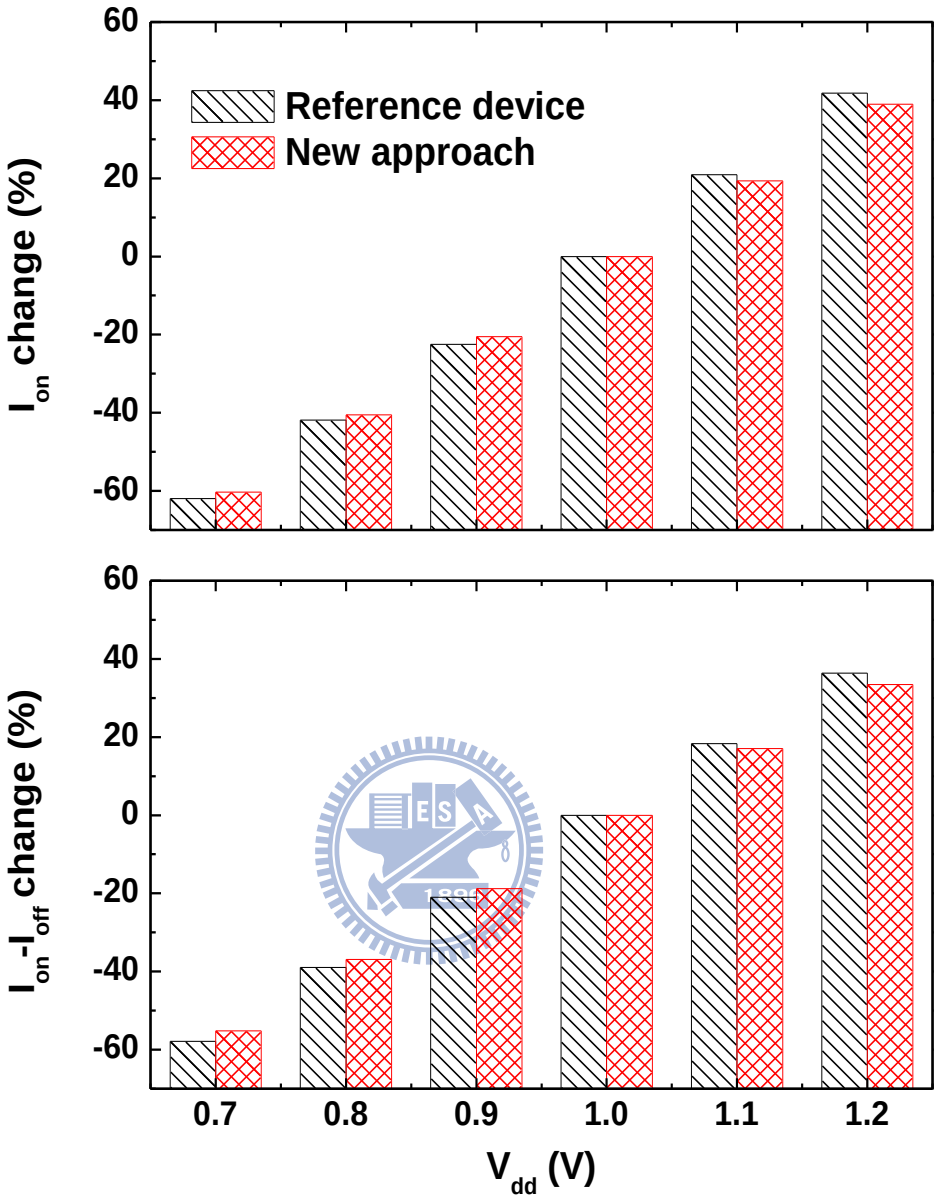


Fig. 5.15 Relative I_{on} and I_{on}-I_{off} performance normalized to V_{dd}=1V. New approach provides a lower sensitivity to V_{dd} change.

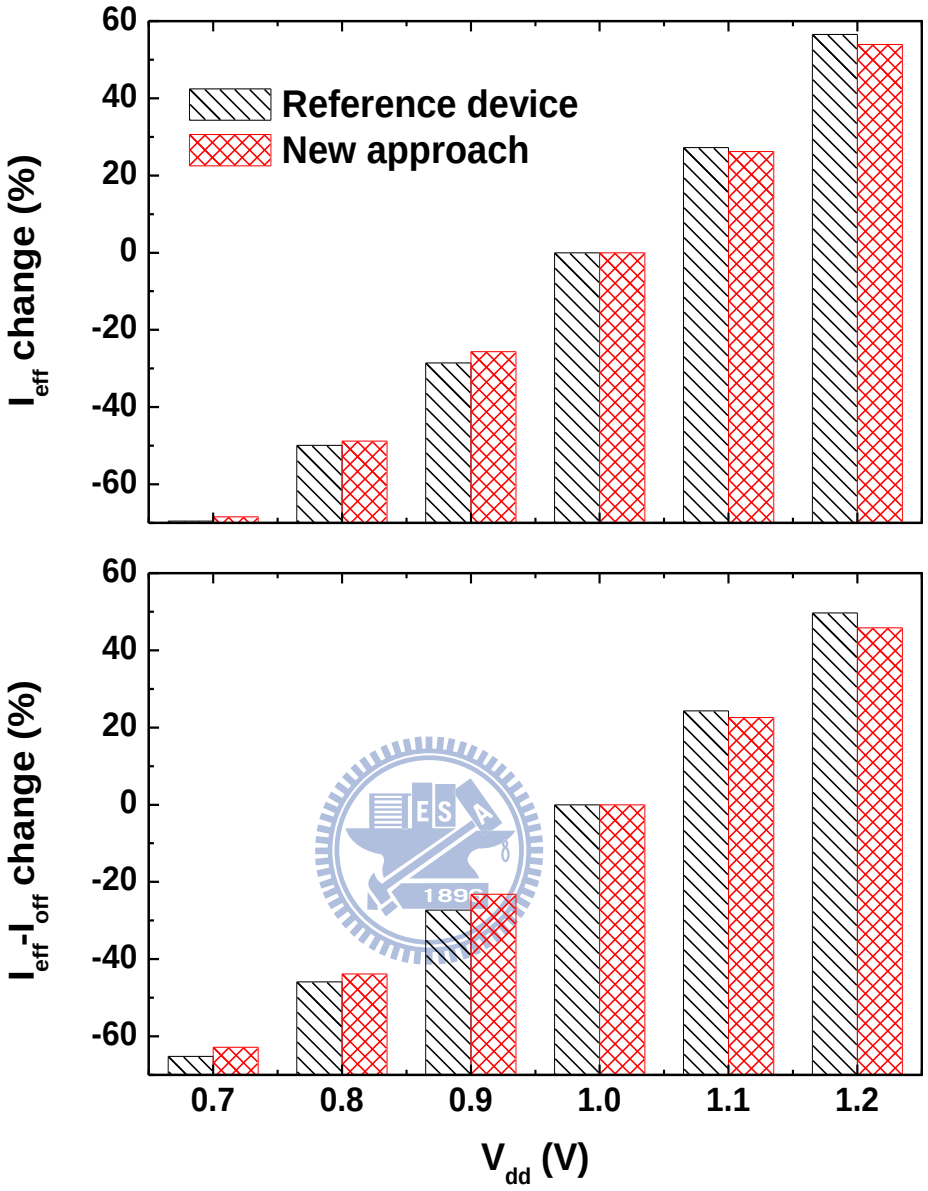


Fig. 5.16 Relative I_{eff} and I_{eff}-I_{off} performance normalized to V_{dd}=1V. New approach provides a lower sensitivity to V_{dd} change. This guarantees a lower sensitivity of circuit speed variation to V_{dd} variation.

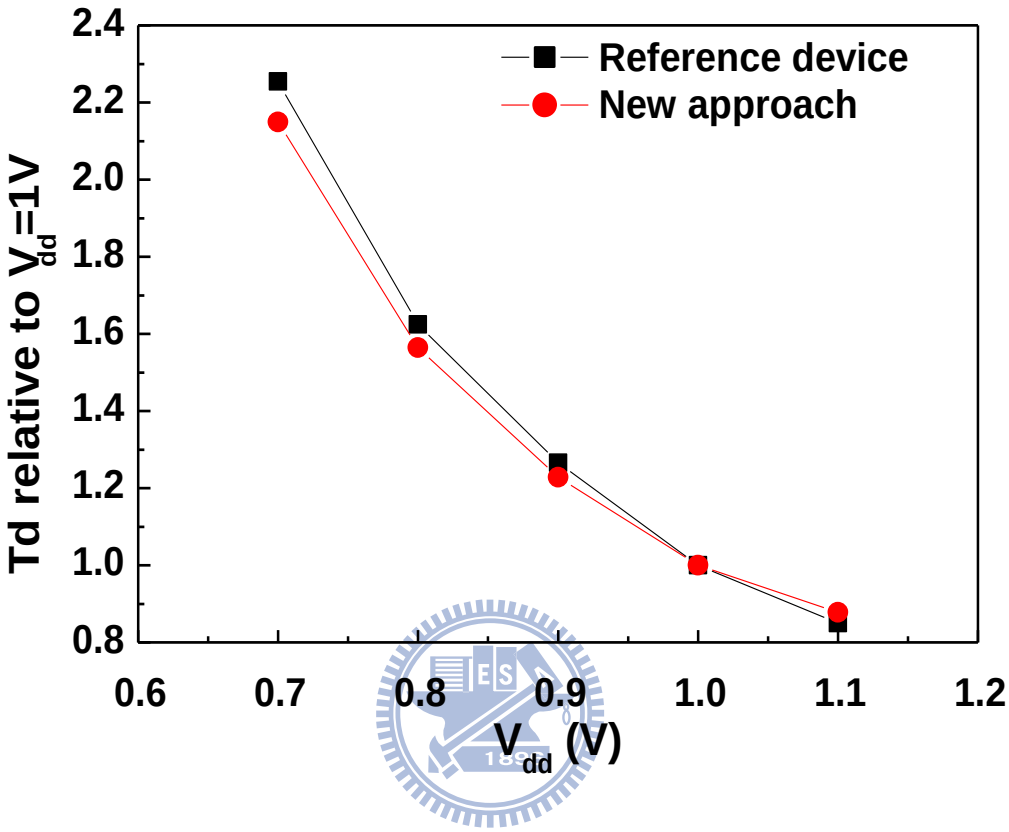


Fig. 5.17 Relative time-delay of inverter oscillator normalized to V_{dd}=1V. Weaker dependency is observed for new approach.

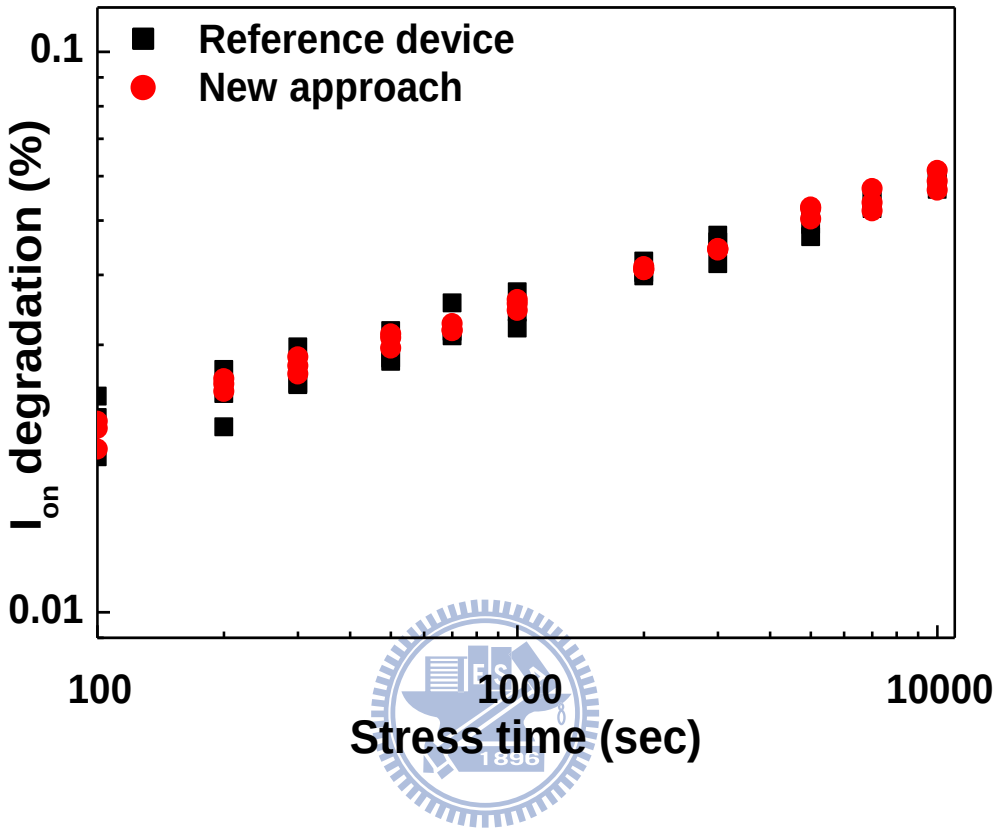


Fig. 5.18 New approach and reference device show the same I_{on} degradation caused by hot-carrier stress.

Chapter 6

Conclusion

6.1 Summary of contributions

This dissertation started with the extraction of MOSFET R_{sd}. Stemming from the universality of carrier mobility in high surface electric field regime, we established a self-consistent methodology that is able to extract R_{sd} by using a single MOSFET with simple I-V measurement. Extensive examination of this novel methodology certified its correctness. It is unique that the parasitic resistance can be extracted without requiring information about T_{ox_inv}, L_{eff}, and W_{eff}. Therefore, this method is especially suitable for the advanced MOSFETs technology in which significant variation of the aforementioned parameters may take place.

Afterwards, we focused on the most critical process modules in the modern VLSI technology, including strain engineering, EOT reduction and USJ formation. A millisecond-annealing-assisted FUSI gate formation was experimentally demonstrated for the first time in the literature. Unlike the conventional FUSI-gate formation process which may need complicated CMP, polysilicon recess, and lithography mask layers, our FUSI-gate formation required only an optimized MSA-assisted silicide phase transformation. Thanks to the highly strained FUSI-gate and elimination of polysilicon-depletion effect, significant improvement in transistor performance was measured. This FUSI-gate technique also demonstrated uniform silicide phase from long-channel to short-channel devices. Selective

FUSI-gate formation was realized by a cost-effective nitrogen ion implantation in certain polysilicon region where silicidation rate was significantly reduced. Our FUSI-gate approach is therefore obviously advantageous over the conventional FUSI-gate approaches in terms of process uniformity, simplicity, and cost.

In terms of e-SiGe strain enhancement, we delivered a hydrogen-annealing process which can position the e-SiGe tip at the gate edge in a self-aligned manner. This extremely close e-SiGe surface proximity leads to both enhanced channel strain and reduced R_{sd}. Furthermore, this technique counts on self-limited silicon-reflow instead of the sophisticated etching process. As a result, an improved transistor driving current is achieved without degrading the transistor variation. We believe that this technique will be increasingly important to the modern VLSI technology for which the process variation may be the bottleneck of manufacturing.

We provided a new index, "V_{th_lin}-V_{th_gm}", in Chapter 5 in order to describe the transistor on-off transition abruptness in addition to the widely used sub-threshold swing. This index is increasingly important to the advanced nano-scale MOSFETs for the low-V_{dd} and low-V_{th} operation because this on-off transition region comprises an increasing portion of gate voltage consumed before turn-on when both V_{dd} and V_{th} are scaled down. By implementing a novel doping technique for S/D-extension, halo IMP dose can be significantly reduced while achieving a low "V_{th_lin}-V_{th_gm}". The benefit from "S/D-ext USJ formation + low halo IMP dose" to low-V_{dd} operation was for the first time discussed and confirmed in the literature.

6.2 Suggestions to Future Work

The high-K/metal-gate manufacturing technology is currently dominated by the layer-by-layer CVD process. However, the void-free gap-fill process of multiple layers is increasingly challenging as gate length further decreases. Polysilicon deposition is well-known for its great gap-fill capability. Therefore, more attention should be given to the FUSI-gate process because of the relatively simple process, tunable workfunction (by incorporating dopant), tunable stress level (by adjusting silicide phase), in addition to the excellent gap-fill capability.

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Chapter 1

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