前瞻矽元件製作技術開發與感測器應用之研究

研究生:陳豪育　　　　　　　指導教授:簡昭欣　博士

國立交通大學

電子工程學系暨電子研究所

摘要

在本篇論文中，主要研究專注開發前瞻的矽基半導體元件結構，製程技術與元件於跨領域如化學/生物感測的應用。在20世紀以來，積體電路效能與密度的持續提升提昇了生活品質與科技進步。不斷的微縮元件尺寸是目前提升電路效能與密度的唯一選擇。以ITRS 2009發表的技術藍圖，到 2016年，元件的閘極寬度將進入16奈米世代。在如此小的間距要產生兩個分明的P/N接面作為通道中少數載子的輸出入節點，製程難度將明顯提高。因此，若仍沿用傳統的元件結構可預期將面臨嚴重的短通道效應而導致元件的開/關功能喪失，造成漏電流問題與功率損耗。為了解決這個問題，各種不同的元件結構也被相繼提出。

近年來，使用絕緣層上矽(SOI)的元件結構因具有相當薄的矽厚度（<10 nm）因此相較於使用塊材矽基板具有更低的寄生電容並可提供絕對的電性隔離而被應用於製作利基型電路;P/N 接面深度的控制也可透過改變矽層的厚度來達成改善元件短通道效應的問題。因此，特別是超薄絕緣層上矽FD-SOI(完全空乏SOI)技術的在高效

能的電路應用上有明顯的進展。但是，周邊電路元件如 I/O、ESD元件等需要較高的崩潰電壓的元件若要以超薄絕緣層上矽來製作具有先天的困難度。此外，完全空乏SOI的矽層厚度控制與通道中隨機攙雜雜質對臨限電壓的影響將產生相當明顯的電性變異而造成降低電路設計的容忍度。在第二章中，將提出使用超薄底部氧化層的絕緣層上矽來取代超薄絕緣層上矽的結構。此種元件結構具有優異的抵抗短通道效應的特性(降低DIBL)與效能(提高有效電流I_{deff})，其可利用基板電壓調節臨限電壓的特性更是與矽塊材元件具有相似的功能性。由於透過降低超薄底部氧化層來減少汲極電場的邊際耦合效應，絕緣層上矽的厚度可維持而降低了矽厚度變異性所造成的電性匹配問題。此結構並有利於與傳統矽塊材晶圓結合提供高度整合的元件于SoC電路之應用。

此外，由於需要提供更好的閘極控制能力來抑制短通道效應，奈米線被視為是16奈米以下CMOS元件最有希望被廣泛採用的結構。由於元件的尺寸已和生物或化學物質的大小相當。因此，近十年來，許多文獻紛紛在探討，如何利用具有奈米線結構的電子式生醫感測器來取代傳統標記式的化學生物分子檢測方法。在過去大多數研究中，常用的半導體矽奈米線製作所採用的“bottom-up”製造方法，因為其個別奈米線的定位問題，將會導致製造量產化的困難。因此，完全相容於目前商業的矽CMOS技術的“top-down”矽奈米線製造方式的生醫感測器，提供了另一種可靠的解決方案。為了得到高表面體積對體積比(surface-to-volume ratio)的奈米線來提升檢測靈敏度，利用“top-down”製造方式的矽奈米感測器必須使用特殊的技術或昂貴的黃光機台才可製作出更細長的奈米線元件。因此，我們在第三章將提出三種與CMOS製程相容並可快速製作大量可靠的矽奈米線感測元件製作技術與其生醫感測的應用。未來可結合CMOS的高速與降低雜訊的電路設計，應用於精準、即時且可攜式的生物檢測。提供未來半導體元件與生物醫學的跨領域應用。

隨著元件尺寸不斷的縮小，微影技術一般被認為可能是16奈米以下CMOS製程技術的其中一個主要技術瓶頸。許多國外大廠目前視短波長的超紫外線（Extreme Ultraviolet lithography, EUV）為可能的解決方案，但它的光罩製作不易與設備

昂貴，每組光罩的價格預計在16奈米世代將高達數百萬美元。從經濟層面來看，若晶片製造端無法降低生產製造成本，將降低IC設計業者對於使用16奈米進行生產的興趣。因此，無須使用光罩的電子束微影技術 (Electron-beam lithography) 相對就顯得具吸引力了。然而，在電路密度持續提高的情況下，如何同時能得到高密度與高解析度的成像技術一直是傳統光學微影製程開發的挑戰。傳統光學微影技術因為必須透過光阻作為成像的媒介，鄰近的圖像成型時易受到光學近接效應(optical proximity effect)或電子散射影響產生干涉作用，因此要得到高密度與高解析度的成像相對困難。為了克服這個問題，我們在第四章中，探討一種不須使用光罩與光阻的顯影技術-奈米噴印成像技術 (Nano Injection Lithography, NInL)。利用此技術搭配蝕刻技術與元件製程整合，可用來製作16奈米等級的傳統矽基奈米線金氧半場效電晶體元件並探討應用於靜態隨機存取記憶體的製作。

在第五章中，我們將利用脈衝雷射退火來製作可降低金屬矽化物與矽接面的蕭特基能障的矽化鎳材料。在次16奈米的元件尺寸，金屬矽化物與矽的異質介面電阻將是元件寄生電阻的主要部份。此部份的寄生電阻值將影響元件效能是否能在尺寸持續微縮時仍可具有改善效能的重要關鍵。而如何製作與控制包含界面的平坦度與其蕭特基能障將是金屬矽化物於奈米元件應用最重要的課題。文中將探討透過脈衝的雷射退火(PLA)的在nMOSFETM 元件上產生高的抗拉應力和低的界面蕭特基能障的鎳矽化物的形成。透過脈衝的雷射退火除了有效降低CMOS製程中的熱預算考量並可得到相當平坦的金屬矽化物與矽的異質接面而降低0.2 eV的蕭特基能障，並可有效避免金屬矽化物琢面的產生因此可用於具有超淺接面的短通道元件。透過最佳化的雷射能量，應用在NDL製作90奈米的元件上可得到大於 8 % 的元件效能改善。由於此製程與CMOS製程具高相容性，可立即應用於現行的半導體製程技術中。

Studies of Exploratory Silicon Device Fabrication and Sensor Application

Abstract

In the past decade, SOI CMOSFETs have become attractive because they provide full dielectric isolation and reduced junction capacitance for high-performance circuit. Very recently, remarkable progress has been achieved in fully-depleted silicon on insulator (FD-SOI) technology. However, to maintain sufficient control of the short-channel effects (SCE), the body thickness has to be reduced to less than one-third of the gate length, thus introducing another difficulty on the variation control of the devices. In the second chapter, a new SOI device scheme featuring thin buried oxide (TBO-SOI) was investigated. The TBO-SOI scheme alleviates the Si thickness reduction requirement for shorter channel. It eases the process variation effects on the characteristics of the devices as well as the parasitic resistance impact due to reduction in the Si thickness. Furthermore, this SOI technology is able to combine both the benefit of an SOI and bulk device without additional complicated process. The superior SCE with a bulk-device-like body effect characteristic makes this device scheme more convincing than the ultra-thin Si SOI.

Beyond the planar SOI, nanowire is the most compelling device channel architecture for complementary metal-oxide semiconductor (CMOS) device scaling towards 10 nm. The 2009 ITRS projected that gate lengths below 16 nm will be launched before 2015. From the perspective of the device gate length scalability, the nanowire channel with multiple-gate structure is expected to be the prospective candidate due to its superior gate

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control ability. More broadly, not only for the logic operation such as metal-oxide-semiconductor field-effect transistor (MOSFET), application of such a tiny semiconductor device for biomolecules sensing is evolving due to their similar dimensions. Thus, in the third chapter, we introduced three novel poly-Si nanowire field-effect transistor (NW FET) pH sensors fabrication using the conventional CMOS process. The nanowire width was scaled to sub-40 nm without requiring expensive lithography equipment. The surface ionic coupling operation of the buried-channel field-effect sensor exhibited superior pH sensitivity (threshold voltage shift > 100 mV/pH), which was beyond the Nernst limitation. The DNA detection capability and built-in memory functionality of NW FET enable interdisciplinary integration in very-large-scale integration (VLSI) circuits. The simple nanowire fabrication approaches realized manufacturing of uniform nanowire devices on a VLSI circuit, which provides a high sensitivity, compact, and cost-efficient biosensor systems-on-a-chip application.

Although optical lithography has been a key driver for semiconductor development, meeting the resolution requirements for continued shrinkage in the technology roadmap is making it difficult to use traditional optical imaging systems when the wavelength of the light source must be reduced. Unlike increasing the exposure tool numerical aperture (NA) to fulfill the resolution requirement, change of a light source to the ultraviolet region demands development of its relative component, such as optics system and photoresist. Thus, extreme ultraviolet (EUV) lithography is a possible solution to the 16-nm node lithography, but its mask set price (extrapolated from 45- to 32-nm nodes) of up to 3 million US dollars is punitive for testing chips and pilot productions in the 16-nm era. E-beam lithography, a maskless process, is a highly attractive lithography alternative—at least in the initial circuit-verification stage. Nevertheless, recent experimental results revealed that e-beam lithography still suffered from line-width roughness and proximity

effects when preparing high-density patterns. The unwanted secondary electron scattering increases the extent of chemical reactions in the photoresist, which results in the loss of resolution for adjacent features. In this chapter, we introduced a novel maskless and photoresist-free technology, which we named as "Nano Injection Lithography" (NInL) that prepared fine patterns for highly integrated devices. The application of NInL is to deposit pattern-transferred materials on the substrate surface directly through electron beam assisted chemical reactions to form the resulting pattern as etching hard mask for subsequent anisotropic etch. In the past decade, the electron beam assisted chemical reactions were used to define nanometer-scale structures having tiny pitches of periodic gratings, but not for the fabrication of MOSFETs. Herein, we reported the fabrication of a 6T-SRAM cell having an area of 0.039 μm^2, by using the NInL. This lithography technique disclosed a new way to explore low-volume and high-value 16-nm CMOS device and circuit design with minimal additional investment, and obtained early access to extreme CMOS scaling.

Finally, an attractive approach to form the exquisite metallic junction for ultra-scaled device was reported. The formation of a uniform, high tensile stress and low interfacial resistance nickel silicide (NiSi) on a 90-nm nMOSFET by introducing pulsed laser annealing (PLA) was investigated. This annealing approach eases NiSi phase transformation to $NiSi_2$ through sufficient annealing temperatures using a low thermal budget laser irradiation, and introduces increased silicide tensile stress and a 0.2-eV reduction in Schottky barrier height (SBH). This $NiSi_2$ layer has a superior film morphology at the silicon interface and avoids {111} $NiSi_2$ facet induced junction leakage for shallow junction devices. By optimizing the laser energy, an 8 % nMOSFET I_{on}-I_{off} enhancement was achieved, when compared with a conventional two-step rapid thermal annealing (RTA) process because of strain enhancement and interfacial resistance reduction.

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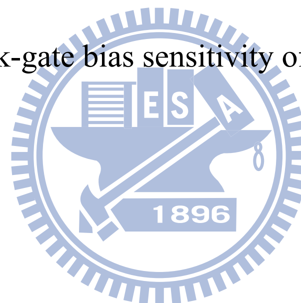

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