Chapter 1

Introduction

According to the 2009 ITRS' roadmap, the semiconductor technology will reach 16-nm node generation in 2015. However, there is still no common consensus regarding what the device scheme would be and how to fabricate numerous devices with the design rule of 16-nm node generation. Thus, the major objective of this dissertation is to investigate the potential alternative device structure, techniques, and application for early exploration of exploratory semiconductor devices technology. Furthermore, we investigated CMOS compatible poly-silicon nanowire technology that not only achieved label-free biochemical sensing, but facilitated system-scale integration of nanosensors. With a high sensitivity and real-time response for low-concentration-level biological molecular detection, the biosensor can warn of the presence of toxic in the early stage before particular diseases become lethal. This technology allows the inclusion of laboratory functions and data processing within the VLSI chip, enabling portability, improving versatility and reducing cost.

1.1 The Overview and Motivation

With the shrinking of the dimension of the semiconductor devices, evolution of either new device structures or techniques are urgently required to maintain device functionality and manufacture-ability [1,2]. Soon, the traditional planar bulk metal-oxide-semiconductor field-effect transistor (MOSFET) structure, commonly

used in the past decades, is expected to encounter the worse short-channel effects (SCE) at sub-16 nm node due to severe depletion field penetration, as shown in Fig. 1.1. Based on Brews' empirical relation [3], the gate-oxide thickness, device-junction depth, and channel-dopant concentration were the key knobs to control the short channel device characteristics for planar bulk MOSFET. However, to adjust those knobs to keep gate length scaling will reach the block soon due to facing the physics limitation, such as high gate leakage, band-to-band tunneling junction leakage, raising parasitic resistance, and mobility degradation. Therefore, the device scheme has to be inevitably evaluated to trade-off the critical metrics through the structure change from traditional bulk MOSFET. In the first chapter, the potential silicon on insulator (SOI) device structure for sub-16 nm node was discussed and promoted, providing a manufacturing friendly and SoC capable device structure to replace the ultra-thin body SOI before employing exotic 3D device structure.

When the dimension of the device is approaching to nanometer scale, the size of a single device is comparable to the molecular dimension. Thus, development of the application of semiconductor nanostructure for biomolecular sensing is evolving rapidly. Among the different approaches employed for biosensing, silicon nanowire is promising for its label-free, real-time response and high sensitivity for biomolecular detection [49–50]. To study the operation principle of nanowire for biomolecule sensing, three simple and low-cost methods were investigated to fabricate the high-sensitive nanowire devices. More importantly, these processes are compatible for complementary metal-oxide semiconductor (CMOS) manufacturing. Without depending on any expensive lithography tools to obtain the sub-40 nm nanowire diameter, the low-cost and simple fabrication process not only produced devices with superior performance than the traditional surface channel sensing device, such as the ion-sensitive field-effect transistor. It also acted as an interface to bridge solid-state

devices and life science to extend the application of semiconductor technology.

Although optical lithography is a key driver for semiconductor development, meeting the critical dimension and high-density requirements for shrinking device makes the use of traditional optical imaging systems difficult. Therefore, for most of the device researchers exploring the characteristics of ultra-scaled devices, the biggest challenge is how to fabricate it though simple lithography. In this work, a lower cost approach was introduced to provide the pathway for low-volume, high-value sub-16 nm device fabrication without the use of expensive apparatus. This method provides fine-patterning fabrication for the critical layer of a device without using mask and photoresist, thus simplifying the process steps and striding the obstacles of conventional optical lithography. This method paves way to build 16-nm node devices for early evaluation.

Finally, a crucial challenge of sub-16 nm devices is to form a smooth heterojunction between the silicide and silicon for parasitic resistance reduction as well as SCE control. An attractive technique with sufficiently energetic, low thermal budget annealing by pulsed laser irradiation for low Schottky barrier height junction formation was investigated in this chapter, which introduced a viable approach for junction formation of ultra-scaled devices.

1.2 The Organization of The Thesis

1.2.1 A SOI Device Scheme with Thin Buried Oxide

With the shrinking of the semiconductor technology to sub-16 nm node, the device is bound to undergo simple dimensional scaling to quickly reach a bottleneck

due to critical challenges faced, such as thermal budget limitation, shallow junction formation, incremental parasitic resistance, severe gate leakage, and reducing V_{dd} requirement for power consumption constraint. The major cause of these challenges is from the SCE-induced unacceptable sub-threshold leakage. When the distance of adjacent S/D junction is approaching, the drain depletion field affects the barrier height at source site. When the barrier height is no longer controlled by the gate potential, the device fails to switch. Therefore, device engineers try to reduce the gate dielectric continuously to obtain better gate control. However, inevitably increasing gate leakage current cannot be ignored due to the increasing device density at a VLSI chip.

From the early 2000s, several reports have demonstrated sub-100 nm devices using conventional planar MOSFET structure [4,5]. These devices demonstrated excellent driving current due to their shorter gate length with lower channel resistance; however, the extremely high off-state current made them impractical to be implemented in the very-large-scale integration (VLSI) circuit due to the sub-threshold leakage current and gate leakage current control, establishing the criteria for chip production. Therefore, it is difficult when the dimension of the bulk MOSFET devices keeps shrinking to sub-16 nm by direct gate length shrinkage along with adjustment of device parameters, such as junction depth and gate oxide thickness, without introducing any innovation in device structure.

To maintain the electrostatic characteristics of short channel devices, there are various device schemes proposed and evaluated. Among these schemes, devices fabricated on SOI are attractive due to their simple fabrication process and reduced leakage path [6,7]. The switching power consumption formula of a logic inverter can be given as follows:

$$P=C_l \times V_{dd}^2 \times f$$

Where C_l is the total loading capacitance and f is the circuit operation frequency. According to the above-mentioned formula, SOI technology is most suitable for low-power applications due to its lower parasitic junction capacitance. In addition, isolation scaling in bulk substrate might probably result in process complexity that is not present in SOI, thus narrowing the SOI/bulk cost differential. Based on the ITRS roadmap [8], the 18-nm gate length device requires a $6.6\times10^{18}/\text{cm}^3$ channel concentration for sub-threshold leakage control. Thus, by using the approximation in a uniform channel doping profile, the gate depletion width (W_d) is observed to be around 10 nm:

$$W_d = \sqrt{\frac{2\varepsilon_{si}}{qN_A}\phi_F} \; ; \; \phi_F = \frac{kT}{q}\ln(\frac{N_A}{n_i}) \; ;$$

The device junction depth should be designed to be smaller than the gate depletion depth to maintain acceptable threshold voltage roll-off characteristics [9]. However, it is very challenging to control the junction depth precisely in such a shallow region without enduring the defect. This shallow junction requirement for scaling bulk MOSFET not only introduces high parasitic resistance, but also produces junction leakage current. On the contrary, by controlling the silicon thickness of the SOI substrate, we can fabricate ultra-scaled semiconductor devices on a naturally insulating material instead of junction isolation, thus significantly alleviating the so-called “SCE” and junction leakage concerns. Therefore, interest in SOI as a prospective candidate to bulk technologies is currently increasing.

In this chapter, we evaluated the sub-20 nm SOI device from the perspective of strain effect and scalability by using Synopsys ISE-TCAD. TCAD is a powerful numerical simulation tool to help us to predict and optimize the device structure at the early stage before expensive fabrication. We investigated the strain effect on the design of various device parameters and the best device scheme according to the

trade-off between strain strength and parasitic resistance. Furthermore, we proposed and discussed the performance benefit of a thin buried oxide SOI (TBO-SOI) device in terms of DC/AC performance. Eventually, from the integration prospect of the system on a chip and SCE control, a TBO-SOI device was experimentally demonstrated and recommended as an alternative instead of the ultra-thin SOI technology in terms of manufacturability.

1.2.2 The Nanowire Device Fabrication and Its Sensing Application

In past decade, narrow-width and multiple-gate SOI devices have been widely investigated due to its excellent gate control ability than planar devices [10-12]. As shown in Fig. 1.2, the 3D device with surrounding gate structure as so-called “nanowire” device could exhibit superior electrostatics characteristics and it is also foreseeing as the prospective candidate scheme for future semiconductor technology nodes. On the other hand, the developments of nanostructure are widely investigated for biosensor applications for the substitution of traditional time-consuming biomoleculars detection since 1990. In addition to the function as logic device, the semiconductor nanowire field-effect transistor reveals its great potential to serve to the label-free and real-time detection of extremely low concentrations of proteins [13], virus [14], and DNA [15]. Table 1.1 compares pro and con among different biomolecular sensing approaches. In current situation, due to lack of a high sensitive inspection of biomolecular, the detection could be limited to identification rather than prevention. In recent years, a nanowire structure was initiated as a sensor and it showed excellent sensitivity since their wire diameter was comparable to the biological or chemical species sizes. The basic operation principle of the biomolecular sensing using nanowire is shown in Fig. 1.3. A significant device conductance

change occurs when the analyte is reacted with the corresponding reactant. The chemical reaction generates the faint electrical signal at nanowire surface hence affects conductance of nanowire. During the past ten years, the bottom-up approach was the most popular technique to fabricate the nanowire devices. However, the bottom-up approach is very unfriendly to mass production due to the difficulties of individual nanowire positioning and complicated post processes for device integration. In the recent years, accompany with the evaluation of semiconductor technology, the critical dimension of the individual device will come to sub-20 nm regime soon with good uniformity. Consequently, the development of nanowire device using manufacturing semiconductor technology is progressive and its multidisplinary exploration is in a great demand.

The “top-down” process for fabricating silicon nanowires provides a solution for manufacturing reliable biosensors due to its compatibility with current commercial silicon-based CMOS technology [16]. Nevertheless, to achieve large surface to volume ratio nanowire with extraordinary detection sensitivity, special techniques or advanced lithography tools were employed to get the slender nanowire patterns [17-18]. Therefore, how to quickly fabricate large amount of reliable devices, control the electrical properties response at relatively simple detection and down the productive cost in commercial scale will be an important issue for using silicon NW FET in future biomedical applications. In this chapter, three simple processes for integrating poly-Si NWs into the CMOS process were developed (See Fig. 1.4). Using these approaches along with CMOS production technology, both the number of process steps and the chip size of the integrated sensor system can be reduced; this in turn will provide cost-efficient, highly integrated devices for potential healthcare applications. Furthermore, different from the surface sensing operation of conventional ISFET, this buried channel sensor exhibits high pH detection sensitivity

even beyond Nerst limitation due to its potential coupling effect. The sensing mechanism of nanowire transistor、its multiple functionality and integrated application were discussed and investigated.

1.2.3 Nano-Injection Lithography (NInL) Technology for Sub 16-nm Node Application

For more than 30 years, photosensitive materials have been used for pattern transfer during the lithographic manufacturing of very-large-scale integration (VLSI) circuits. With semiconductor technology nodes continuing to shrink, and the requirements of stable circuits operation at high density and resolution with low variability and low-cost manufacturing, optical lithography is being driven to its limits. Although optical lithography has been one key driver for semiconductor development, meeting the resolution requirements for continued shrinking in the technology roadmap is making it difficult to use optical imaging systems when the wavelength of the light source must be reduced [8,19-20]. Unlike increasing the exposure tool numerical aperture (NA) to achieve the smaller half-pitch, the change of a light source to smaller wavelength to the ultraviolet regime demands development of its relative component, such as optics system and photoresist. Therefore, although extreme ultraviolet (EUV) lithography is one possible solution to this problem [21], its mask set price is punitive for testing chips and pilot productions in the 16-nm era.

E-beam lithography, a maskless process, is a highly attractive alternative for lithography—at least in the initial circuit-verification stage. However, that e-beam lithography suffers from line width roughness and proximity effects when preparing high-density patterns. Besides, how to achieve the high throughput is also a topic for maskless lithography.

In this study, we investigated a novel maskless and photoresist-free technology, which we named "nano injection lithography" (NInL), that prepared finely patterned SRAM devices. Table 1.2 shows the benefit of NInL compared to advanced lithography. Three key features make NInL more attractive than conventional optical, EUV, or e-beam lithography for low-volume fabrication for 16-nm node technology and beyond. First, this approach requires no mask and no photoresist, which greatly reduces the number of patterning process steps from five down to only one, as Table 1 shows. Second, photoresist free technology is less influenced by incident light/electron interference, and thus produces much less proximity effects and better spacing resolution. Third, the conventional approach to eliminate the aforementioned proximity effect by "Double Exposure" for high-density circuits [22-24] can be skipped. The double exposure approach increases the process complexity, cost, and stochastic device variation. Indeed, using this NInL technique allows the rapid fabrication of nanometer-scaled devices exhibiting high pattern densities and low line width roughness (LWR) with minimal entry costs—a desirable feature for preliminary evaluation of the performance of ultra-scaled devices. The introduction of NInL could be a potential paradigm shift to meet the technical requirements and complexities for continued adherence to Moore's Law at sub-22 nm half-pitch and beyond. This paradigm shift will drive major changes throughout the lithography infrastructure.

1.2.4 Device Silicidation using Pulsed Laser Annealing

For a typical MOSFET, the total device resistance could be differentiated into channel resistance and parasitic resistance. According to a recent survey on device performance, channel resistance is reduced due to the shorter conduction path of the carriers and channel stress is enhanced, which improves carrier mobility as well as

carrier density by increasing the gate capacitance. Therefore, continuous reduction in device resistance due to its shrinkage in gate length had been one of the major metrics to achieve performance gain from generation to generation in the past. However, when the device was scaled into the sub-100 nm regime, to maintain good electrostatic characteristics of the devices, the junction depth must be scaled, thus producing an impact on performance gain.

To obtain high driving current while reducing the applied voltage for active power reduction, it is no shrinking that is responsible for the reduction in the parasitic resistance. According to the device resistance data based on 2009 ITRS roadmap [8], the declining rate of total device resistance is significant than that of parasitic resistance from 65 to 32 nm due to mobility enhancement technologies were intensively implemented. However, by instinctively projecting this trend, the parasitic resistance will be the dominated part of the total device resistance when the gate length approaches the 10-nm regime, and the specific contact resistance will play key roles in parasitic resistance, as shown in Fig. 1.5. Besides, how to obtain two distinct junctions connected to the channel in such a small device dimension is a very challenging task for any kind of device structures [25]. Although there were several groups proposed the "junction less" transistor [26] or "metal S/D" transistor [27] to avoid the crucial requirement for junction formation, a low specific contact resistance is still required to maintain the performance of the devices.

In this chapter, we proposed a novel pulse laser annealing approach for the formation of nickel silicide (NiSi) to reduce interface resistance and improved the strain for nMOSFET. In addition, to avoid the diffusion of the metal atom into the device channel region, especially for sub-20 nm devices, the morphology of the silicide was controlled for device fabrication.

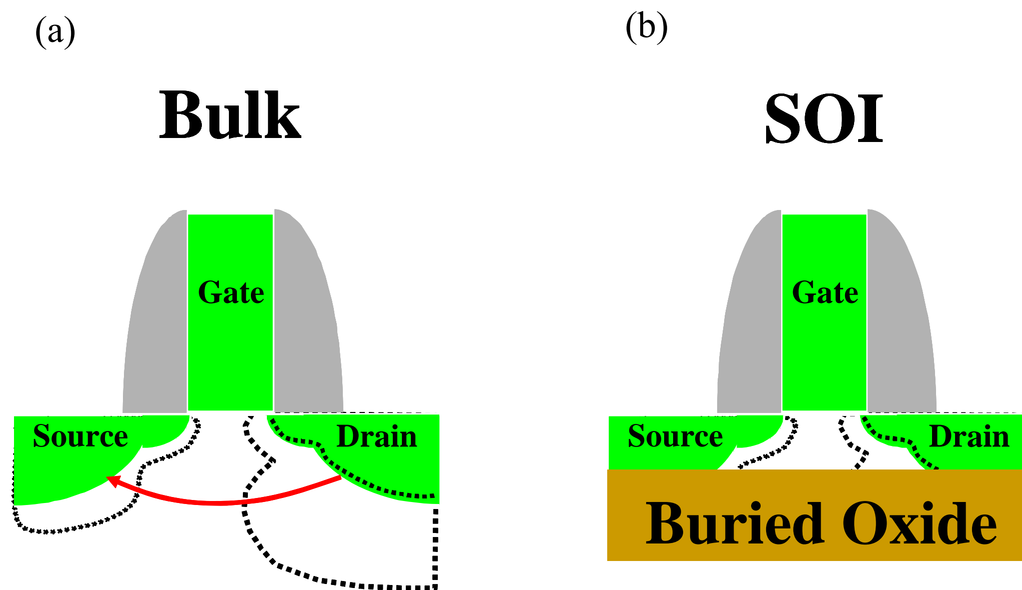


Fig. 1.1 Illustrations of two major device schemes and its depletion field during device operation. (a) A planar bulk device. (b) A SOI device.

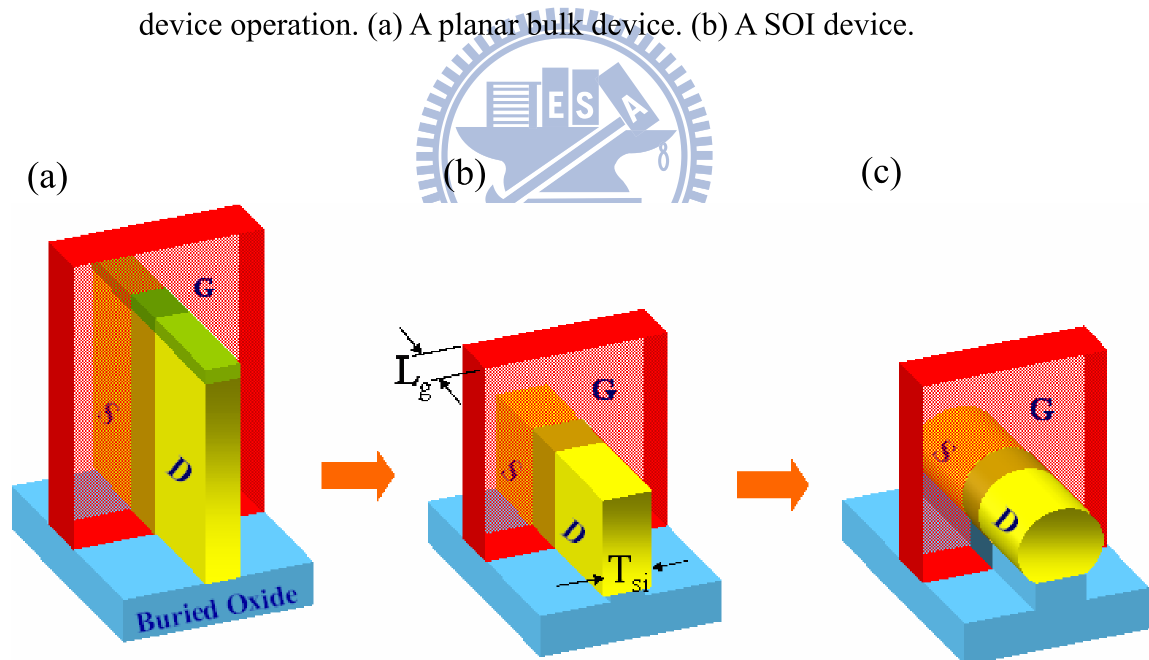


Fig. 1.2 Evolution of multiple gate devices structure. (a) Double gate device. (b) Trigate device. (c) Nanowire Device. (Ref [10] F. L. Yang *et al.*, “5nm-Gate Nanowire FinFET,” in *VLSI Tech. Dig.*, 2004, pp.196-197)

Technology platform	Structure	Analyte	Detection limit	Ref.
Surface plasmon resonance	BIAcore2000 SPR	Bacteria	25 cfu/ml	Food Process Eng. 29 (2006) 373.
Interferometer	Mach-Zehnder interferometer	Bulk solution	10^{-7} RIU	Sens. Actuators B Chem. 61 (1999) 100.
Ring resonator	Ring on chip	DNA Protein Bacteria	~100 nM 20-250 pg/mm^{-2} 10^5 cfu/ml	Biosens. Bioelectron. 23 (2008) 939.
Photonic crystal	PC waveguide	Protein	0.15 uM	Opt. Express 15 (2007) 3169.
Cantilever	Microfabricated cantilever	Aspergillus	10^3 cfu/ml	Nugaeva et al. (2007)
Electrode	Piezoelectric	IgG	7 pg/ml	Anan.Chem.77,7758,2005
QCM	QCM	Virus	1 ng	Eun et al. (2002)
CNT	CNT sensor	DNA		APL 91, 093507 (2007)
SiNW FET	NW sensor	PSA	50-100 fg/ml	Nature biotechnology 23, 1294, 2005

Table 1.1 Evaluation of different biomolecule detection approaches.

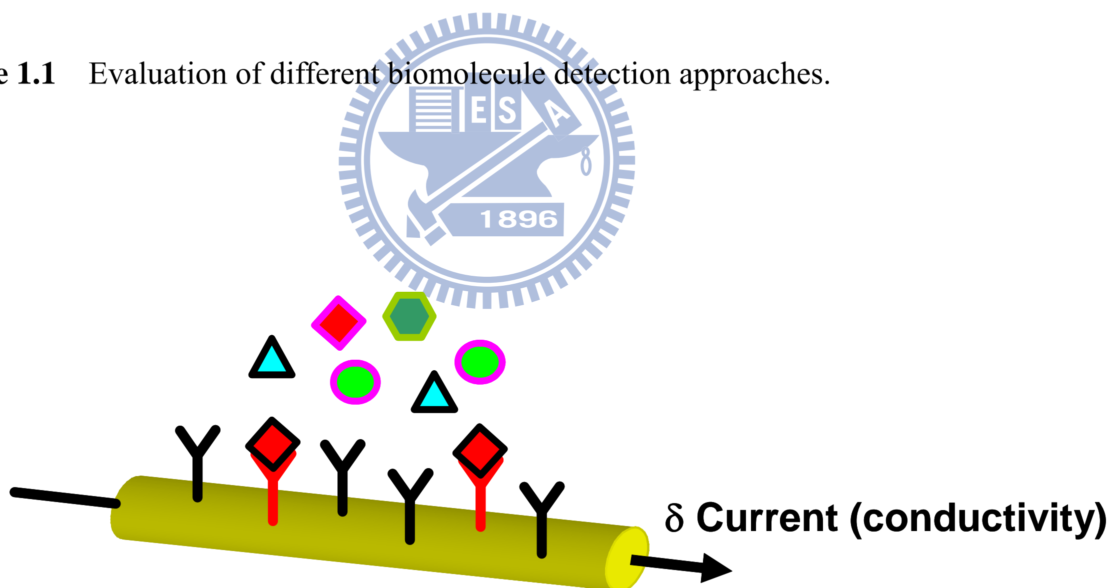


Fig. 1.3 Biomolecular sensing principle of nanowire devices. The reactant bounding on the nanowire reacts with target analyte, generates the charges and changes the conductivity of nanowire.

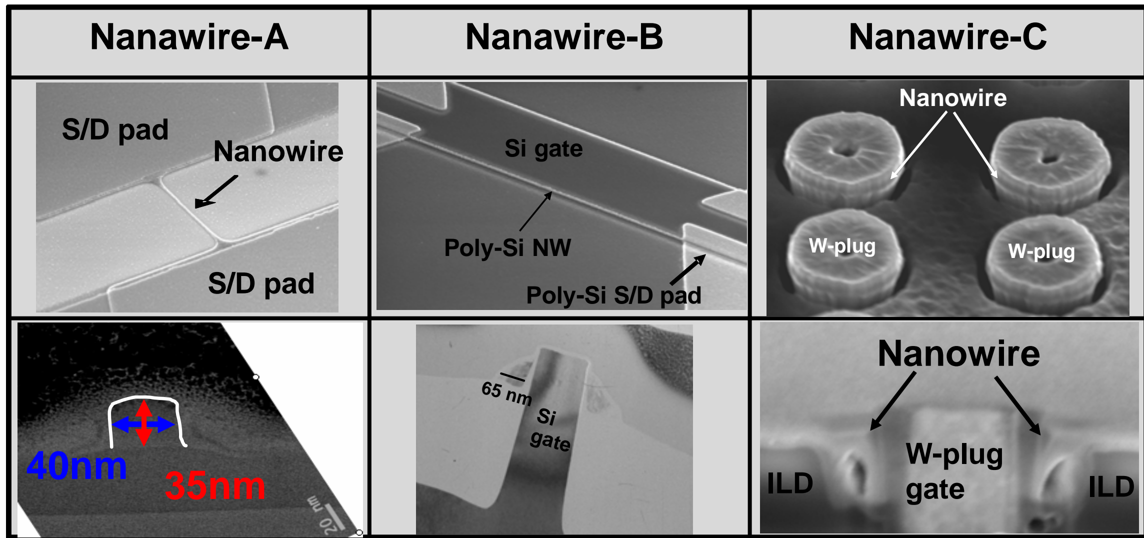


Fig. 1.4 Microscopical pictures of three CMOS-Compatible Poly-Silcon nanowire fabrication methods.

	EUV	E-beam Lithography	Nano Injection Lithography (this work)
Photo Mask issue	1. Defect repair 2. Mask costly	**Maskless**	
Photoresist process issue	1. EUV resist induced flare effect 2. Polymer P.R. related line width roughness 3. Proximity effect	1. Polymer P.R. related line width roughness 2. Tradeoff exposure throughput with resolution and proximity effect	**Photoresist Free**
Patterning process steps	1. Blanket hard mask deposit 2. Resist coating 3. Exposure 4. Develop 5. Resist stripping		**One step** (hard mask deposited directly at the desired site)

Table 1.2 The comparison of three major lithography technology.

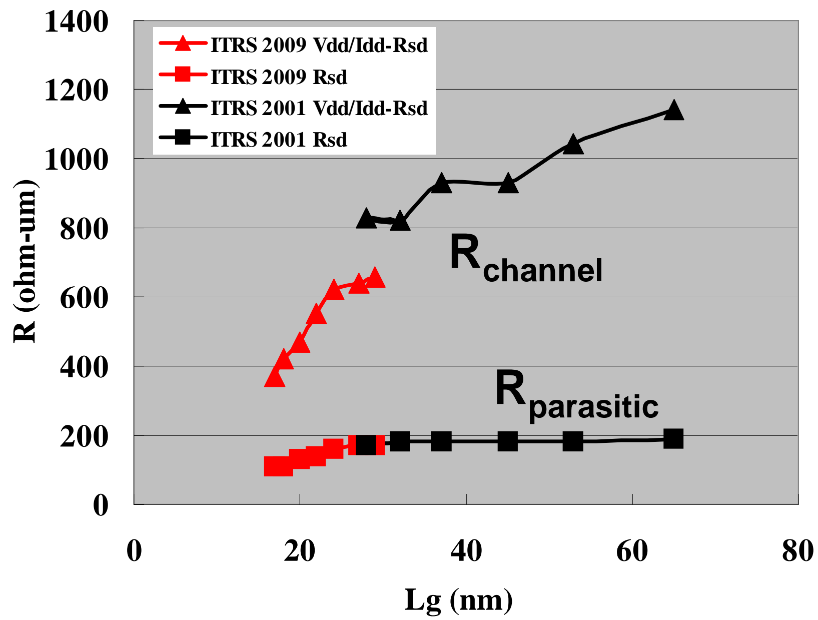


Fig. 1.5 A historical trends of device parasitic resistance of various L_g from different technology nodes. (Reference: ITRS Roadmap 2001/2009 edition)

Chapter 2

A SOI Device Scheme with Thin Buried Oxide

2.1 Introduction

Silicon on insulator (SOI) has been well known owing to its advantages on high-performance applications with low active power. In recent years, the scaling ability of the SOI device has also been addressed by several researches [28–30]. A large portion of performance gain in SOI technology comes from its reduced junction capacitance and depletion field to support its superior scalability, and this benefit will be more significant in thin-body SOI (TB-SOI). Meanwhile, strained silicon has become a crucial technique for scaling CMOS, and numerous techniques are being developed to boost the strain level at the device channel for enhancing the carrier mobility [31–35]. As the active region of the SOI device is decoupled from the substrate by buried oxide, the channel strain should be more pronounced and sensitive to device features rather than the conventional bulk devices [36].

In the first part, scaling of SOI transistor by reducing the thickness of silicon and structure evolution will be discussed. Although excellent short channel control can be obtained by simply reducing the SOI's silicon thickness, the increasing resistance、threshold voltage control, as well as integration of periphery devices, such as I/O devices and ESD devices, could be obstacles due to the intrinsic low breakdown voltage of TB-SOI [37]. In addition, mobility degradation due to TB-SOI has also been revealed [38] and the possible random dopant fluctuation [39] has been observed to always impede the aspiration for its chip production.

To alleviate the difficult challenges of TB-SOI device without compromising on the SCE, a novel SOI device scheme using thin-buried-oxide (TBO) layer has been discussed based on the TCAD simulation perspective. The thin buried oxide alleviates the requirement to reduce the silicon layer while maintaining the same SCE control. In addition, the trade-off between increasing parasitic capacitance and SCE toleration of TBO-SOI has also been discussed.

2.2 SOI Device Structural Design in View of Strain and Resistance

The process strain had been approved to be advantageous on the carrier mobility enhancement for devices [31-35]. Among the various process approach, the deposited dielectric films with high stress is the most effective stressor for devices mobility enhancement with lower cost, simple process and less defect generation than the biaxial strain [40]. The stress level of deposited film can be modulated by simply changing the composition of dielectric or changing the ion bombardment rate during dielectric deposition. Therefore, the opposite (tensile/compress) stress can be employed for n/pFET respectively for electron/hole mobility enhancement [32]. For the state-of-the-art strained CMOS technology, the stressed materials are usually inserted after the spacer formation as a contact-etch-stop layer. To deliver the stress effectively to the channel region underneath the gate area, the design of an optimal device scheme to take account of the device performance metrics before starting the costly SOI device fabrication process is very important. So, a 2D numerical process simulator TSUPREM4 (Synopsys ISE-TCAD) considering the process-induced strain effect was chosen to perform the evaluation in advance.

The device configuration and device parameter setting is shown in Fig. 2.1. To have accurate stress calculation, the stress history model is included to take account of

the volume change during the thermal oxidation process、thermal mismatch between different materials and the intrinsic strain in a deposited layer. Since active silicon region is fully isolated, channel stress cannot be relaxed through silicon substrate underneath buried oxide. This results in a phenomenon that the magnitude of channel stress eventually depends on device aspects (L_g, width, and T_{Si}). As shown in Fig. 2.2, channel stress monotonically increases with scaling silicon thickness (T_{Si}) from 100-nm to 20-nm. Meanwhile, drive current improvement tends to be larger in short-length, narrow-width devices, showing larger strain in small dimension as shown in Fig. 2.3 [41]. The scaling-strengthened strain in SOI transistor is desired since it makes a positive feedback during technology scaling.

On the other hand, continuously scaling T_{Si} introduces an undesired increment of source/drain sheet resistance ($R_{s/d}$). For TB-SOI devices (T_{Si} < 20 nm), a costly raised source/drain (RSD) technique is usually required to keep its performance benefit. The requirement of the RSD thickness is depend on the silicide depth. In general, a larger than 20~30 nm (silicide thickness) is a common requirement for the TB-SOI devices to avoid current crowding effect and silicide spiking effect [42]. However, after including the RSD, the channel stress induced by highly uniaxial stressed CESL was attenuated due to an increased distance from channel to stressor. The simulation predicted a significantly decreasing strain magnitude with increasing RSD thickness due to the extra distance from CESL to channel as well as the topography change which is shown the Fig. 2.4. To compensate the increasing resistance and attenuated strain of the TB-SOI, a smaller spacer is able to improve source/drain resistance while making T_{si} very thin to avoid SCE. Simulation showed $R_{s/d}$ was maintained even though T_{Si} was scaled from 20 nm to 8 nm, while spacer width was also shrunk from 40 nm to 25 nm, is shown in Fig. 2.5. As a result, SOI transistor scaling will continue with silicon thickness reduction.

Strained silicon incorporated with SOI will benefit transistor scaling, yet it may face the tradeoff between sheet resistance and mobility enhancement. Therefore, a best device design such as spacer width, RSD thickness and SCE control uses early evaluation by TCAD simulation would be beneficial before device fabrication.

2.3 Thin Buried Oxide (TBO) SOI Device Evaluation

2.3.1 Motivation

At 32 nm node technology generation, SOI silicon body thickness is very likely to be less than 20 nm to keep SCE control. However, integration of periphery devices, such as I/O devices and ESD devices, could be obstacles due to intrinsic low breakdown voltage in TB-SOI. Fig. 2.6 shows the SOI devices fabricated for It_2 (secondary breakdown current) measurement [43], the thinner Si SOI devices had lower It_2 current which means the devices can not sustain high ESD current. On the other hand, it is also difficult to achieve multiple V_t (threshold voltage) on TB-SOI for circuit design through the conventional well/channel implantation. Besides, the high accuracy requirement for analog devices is always a concern with SOI substrate due to its floating body characteristics. The carriers generated by impact-ionization will cumulate at the bottom channel region and cause the unstable threshold voltage variation [44]. For general SOI, the noise overshoot due to its floating-body effect has been observed even T_{Si} thinned down to 20 nm, which induces phase noise for analog circuit [45]. These obstacles hinder SOI from completely replacing the bulk substrate. Therefore, to fulfill the SoC requirement for devices characteristics, the new structural evolution of SOI devices is discussed in this work.

One major benefit of using SOI for short channel device is that device drain-side

depletion region is effectively suppressed by the bottom oxide layer. The bottom oxide layer naturally restricts the junction depth hence weakens the lateral electric field penetration into the channel. However, even though the drain side junction is blocked by the thicker buried oxide. The attenuated drain-side field still cannot be completely terminated in the substrate region and cause fringe field penetration in the channel. Thus, the fringe-field affects the channel potential, leading to the source-side barrier lowing and SCE degradation. To alleviate the electric field penetration, reducing the buried oxide layer is an option to partially bypass drain-side fringe-field into the substrate. Figure 2.7 shows the electric field vector of the SOI devices with different buried oxide thickness. Part of the drain-side field was conducted to the substrate hence TBO-SOI shows less fringe-field effect in the channel region. As a result, in the bottom of silicon, the off state leakage is significant reduced which is shown in Fig. 2.8. Table 2.1 summarizes benefits of TBO-SOI devices in terms of manufacturability. The major advantage of introducing TBO-SOI is that silicon thickness constraints for SCE control can be relaxed hence increase the device variations tolerance [46-47]. Besides, due to the buried oxide thickness reduction, the integration of SOI device with bulk substrate is viable and the aforementioned issues for periphery devices integration are therefore solved by transferring these transistors to neighbor bulk area [48-49].

2.3.2 The DC characteristics of TBO-SOI Devices

Two SOI device schemes were used for MEDICI evaluation. One is the TB-SOI device and silicon thickness was assigned as the variable; the other was the 20 nm silicon SOI and the buried oxide thickness was assigned as the variable. Figure 2.9 shows the off-state leakage current performance comparison. The data shows that

when the buried oxide was reduced to 40 nm, the SOI silicon thickness can be still maintained at 20 nm instead of using 8 nm silicon with thicker buried oxide (100 nm) SOI. Figure 2.10 shows the significance of the DIBL improvement when reducing the buried oxide due to the lateral drain-side electric field reduction. The DIBL improvement not only enables the gate length reduction for further drive current enhancement, the device switching speed can be further improved due to the effective current enhancement. According to the propagation delay expression [51]:

$$\tau_{PD} = \frac{CV_{dd}}{2}\frac{1}{I_{deff}}$$

Where $I_{deff} = \frac{(I_H + I_L)}{2}$; $I_H = I_{ds}(V_{gs}=V_{dd}, V_{ds}=V_{dd}/2)$; $I_L = I_{ds}(V_{gs}=V_{dd}/2, V_{ds}=V_{dd})$

The I_H is relative to the device transconductance (g_m) and the I_L is relative to the output conductance (g_{ds}). If the DIBL of devices can be reduced, the lower channel dopant concentration or device threshold voltage (V_{th}) is required for a given I_{off} hence both I_H and I_L can be improved. It is worth to note that the sub-threshold swing (*S.S*) is monolithically increased when the TB-SOI Si thickness is less than the 10 nm. When the Si is less that 10 nm, the channel is fully depleted and by referring to the analytical model derived by S. Deb for TB-SOI [52]:

$$\text{S.S.} = 2.3\kappa_b T\left\{(C_{si,d} + \frac{A}{C_{gox}}) - \frac{C_{si,d}}{B - \frac{C_{box}{}^2}{C}}\right\}$$

Where $C_{si,d} = \frac{qN_a T_{si} L_{eff}}{\psi_F - \psi_B}$, ψ_F is the front channel potential and ψ_B is the back channel potential. A is $C_{gox}+C_{if}$; B is $C_{box}+C_{FD}+C_{if2}$; C is $C_{box}+C_s+C_{if3}$; C_{FD} is the drain-coupling capacitance; C_{if} is the oxide to channel interface capacitance; C_{if2} is the channel to bottom oxide interface capacitance and C_{if3} is the bottom oxide to substrate interface capacitance and C_s is the substrate depletion capacitance. The *S.S.* will be strongly affected by Si thickness, buried oxide thickness and also drain-side coupling

capacitance. From the simulation result, keeping the Si thickness of TB-SOI at around 20 nm can alleviate this *S.S.* degradation during buried oxide thickness reduction. In addition, a well-known issue of the SOI device is the self-heating effect [53]. The heat generated during device operation and it's difficult to dissipate the heat into the substrate due to the low thermal conductivity of bottom oxide layer. The heat in the channel reduces the mobility and saturation velocity of carriers hence reducing the drive current up to 20 % depending on the Si thickness and operation frequency. However, this heat conservation effect can be diminished by reducing the buried oxide thickness. Based on the simulation result considering the lattice temperature effect, a larger than 10 % I_{dsat} gain can be recovered by reducing the buried oxide thickness from 100 nm to 20 nm which is shown in Fig. 2.11, delivering the further performance benefit of TBO-SOI devices than TB-SOI devices.

One critical issue for the SOI application is the body bias tuning feasibility. In normal bulk devices, the device threshold voltage can be adjusted through channel depletion regulation by tuning body bias. This threshold voltage adjustment can be applied to optionally modulate the device performance and leakage for power management [54]. However, for the thin silicon SOI, the body effect is almost negligible due to the high resistance of body contact [55]. By reducing the buried oxide thickness, this gives the opportunity to control the device threshold voltage with the substrate bias. The body potential can be effectively modulated through the buried oxide coupling of substrate bias to the back channel which is shown in Fig. 2.12. In that sensing, the device body factor is comparable to the bulk device which offers the additional low-power/high-performance operation option for device/circuit application [50].

2.3.3 The AC characteristics of TBO-SOI Devices

The major suspense of employing thin buried oxide SOI is the increasing parasitic capacitance. As the buried oxide thickness reduced, the drain side parasitic capacitance increased which lost the superiority on capacitance reduction of SOI. Figure 2.13 shows the TCAD simulation result showing that the maximum parasitic capacitance appears when the buried oxide capacitance (C_{box}) is almost equal to the substrate depletion capacitance ($C_{d\text{-}sub}$). To minimize the overall drain side capacitance, it is better to keep the substrate dopant concentration as low as possible to reduce the substrate depletion capacitance. As shown in Fig. 2.14, when the SOI thickness and buried oxide thickness are both reduced, the low thermal budget process for S/D formation is required to avoid S/D dopant diffusion into the substrate to reduce substrate depletion capacitance.

Although the parasitic drain capacitance of TBO-SOI is increasing along with reducing buried oxide thickness, the advantage of its superior SCE control contributes benefits on propagation delay by side-wall capacitance reducing and effective current enhancement. Figure 2.15 shows that less channel or pocket implant dose are required to suppress the drain field hence the side-wall parasitic capacitance can be significantly reduced while maintaining good SCE control. The significant DIBL gain improves the $S.S$ and I_{dlin} current, as shown in Fig. 2.16, introduces the inverter speed gain. In the switching speed evaluation, a three-stage ring oscillator was programmed for gate delay evaluation using circuit analysis advanced application module of MEDICI. By combining all the effect, there were 12 % gate delay improvement when the buried oxide thickness was reduced from 100 nm to 20 nm, is shown in Fig. 2.17. The significant DIBL gain leads to higher I_{deff} of the TBO-SOI leads to the propagation delay benefit and make it a viable candidate for 16 nm generation technology.

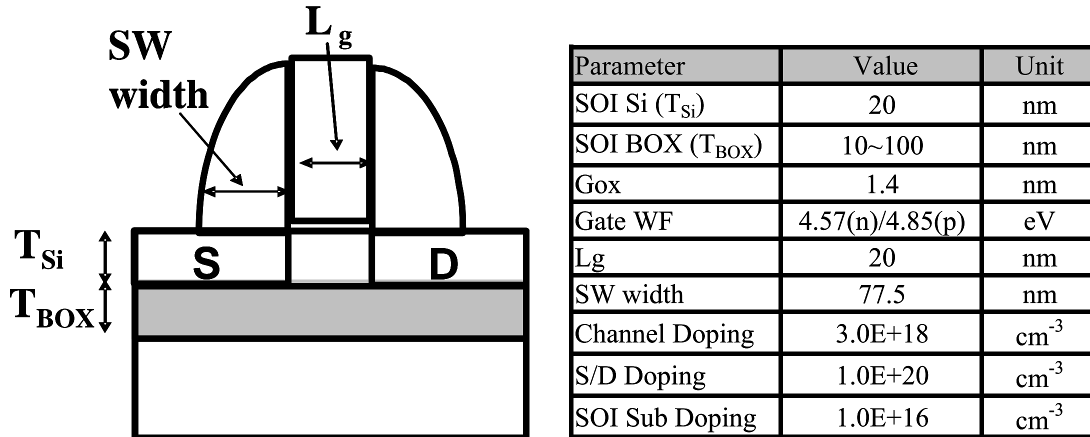
2.3.4 TBO-SOI and Bulk Substrate Hybrid Technology

The proposed process flows to integrate the TBO-SOI with a bulk substrate is shown in Fig. 2.18. The photoresist was applied to define the TBO-SOI and bulk region. After using the anisotropic plasma etching to remove the SOI layer of bulk substrate, the 9 nm pad oxide and 70 nm nitride layers were deposited sequentially by using furnace. The active area patterning was performed and then Si etch was adopted using anisotropic plasma etching for following isolation gap filling region. Figure 2.19 shows the TEM cross-sectional view of TBO-SOI with bulk region after the active area definition. To avoid the buried oxide deformation induced stress on the silicon layer, a low-temperature STI gap filling module is needed to alleviate the bird's bead effect on buried oxide due to thermal oxidation. In this scheme, the demands of high performance and high density devices can be fabricated in the SOI region and on the other hand, the high voltage devices can be fabricated on the bulk substrate area. For the SOI devices fabrication, the MESA isolation was performed. A 2-nm pure thermal oxide layer (for its dielectric properties), a 120-nm poly-Si layer (serving as a gate electrode), and a 50-nm tetraethyl orthosilicate (TEOS) capping oxide layer (serving as an etching hard mask) were deposited sequentially. The poly-Si gate was patterned using an I-line stepper and trimmed to 70 nm using a photo resister and the "ashing and etching" approach, followed by 5-nm poly-Si re-oxidation (as an offset spacer) in a furnace. BF_2 was used for 30° tilted-angle halo implantation at 10 keV and a dose of 3×10^{13} cm^{-2}; the deposition and etching of 70-nm-thick SiN was performed for spacer formation. The poly-Si hard mask was then removed through HF dipping. Figure 2.20 shows the cross-sectional TEM of the TBO-SOI after spacer formation. The wafers then underwent deep source/drain implantation using As implantation (7 keV, 1×10^{15} cm^{-2}). After exposing the wafers to

RTA (900 °C, 10 s) to activate the dopant, we measured the device characteristics using HP-4145B. The I_d–V_g characteristics in Fig. 2.21 (a) reveals the superior DIBL characteristic of TBO-SOI device than TB-SOI devices. The significant body effect through a substrate bias of the TBO-SOI devices is shown in Fig. 2.21 (b), exhibits the feasibility of power management by using a thin-Si SOI device.

2.4 Summary

SOI transistor scaling will continue with silicon thickness reduction for SCE control. Strained silicon incorporated with thin-Si SOI will benefit transistor scaling, yet it may face the tradeoff between sheet resistance and mobility enhancement. Therefore, a new SOI structure featuring thin buried oxide layer was investigated and suggested as a prospective candidate. The thin buried oxide device scheme can further extend the gate length limitation and increase the body factor for digital/analog circuit application, which is not available using conventional ultra-thin-body SOI. The excellent DC characteristics and short channel control ability of TBO-SOI recover its penalty of parasitic capacitance increasing. Because the thin buried oxide also enables a low step height between SOI area and bulk area, this device scheme eases the hybrid SOI/bulk structure integration thus makes conventional bulk devices easily incorporated into SOI-based technology for high performance and high density SoC applications.



Parameter	Value	Unit
SOI Si (T_{Si})	20	nm
SOI BOX (T_{BOX})	10~100	nm
Gox	1.4	nm
Gate WF	4.57(n)/4.85(p)	eV
Lg	20	nm
SW width	77.5	nm
Channel Doping	3.0E+18	cm^{-3}
S/D Doping	1.0E+20	cm^{-3}
SOI Sub Doping	1.0E+16	cm^{-3}

Fig. 2.1 The device structural template and variable setting for TCAD simulation.

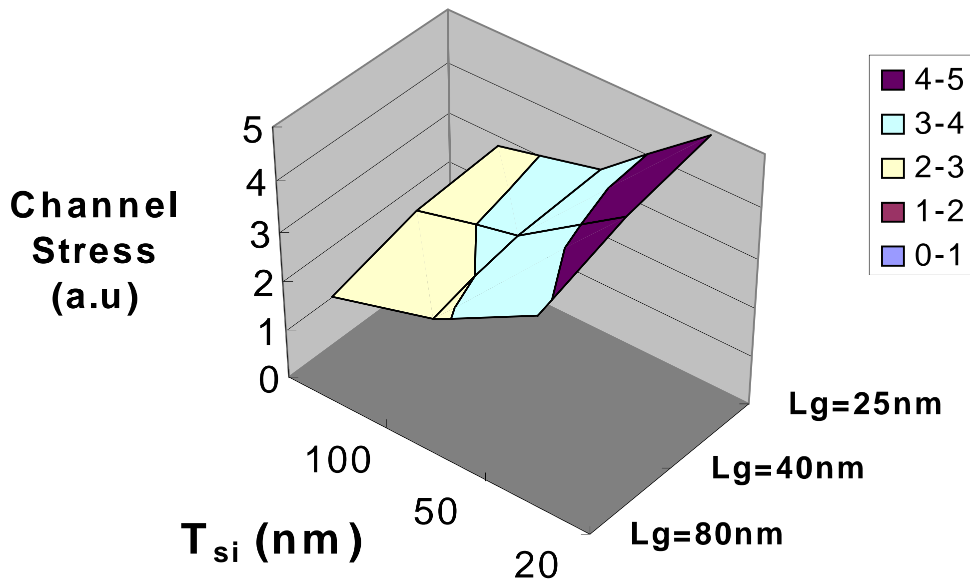


Fig. 2.2 Simulated device channel stress increased with decreasing T_{si} and L_g.

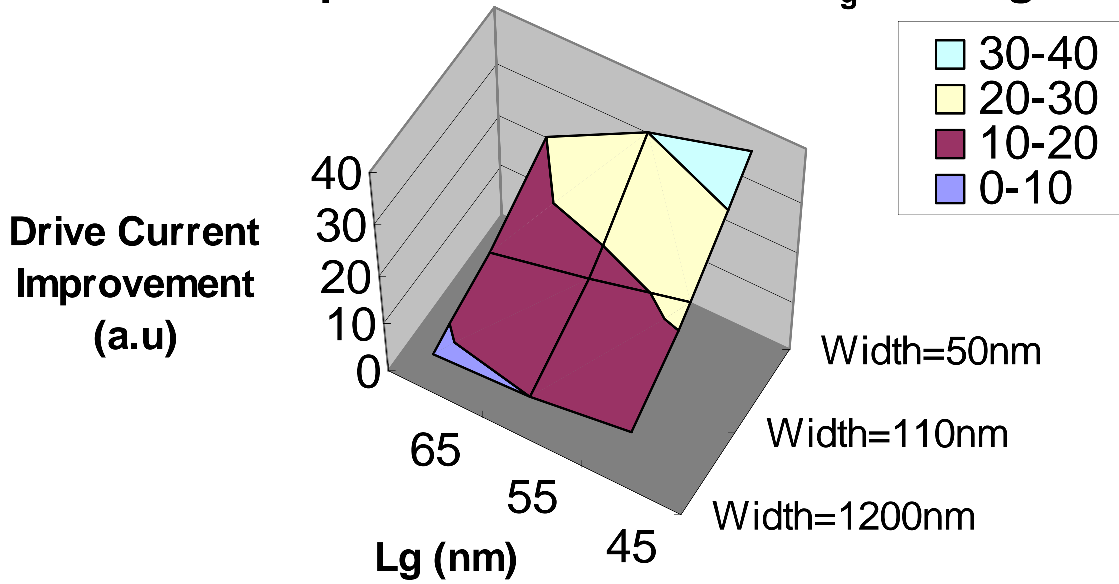
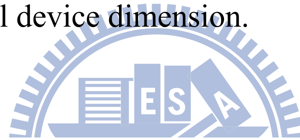


Fig. 2.3 Device driving current improvement from channel strain is more significant in small device dimension.



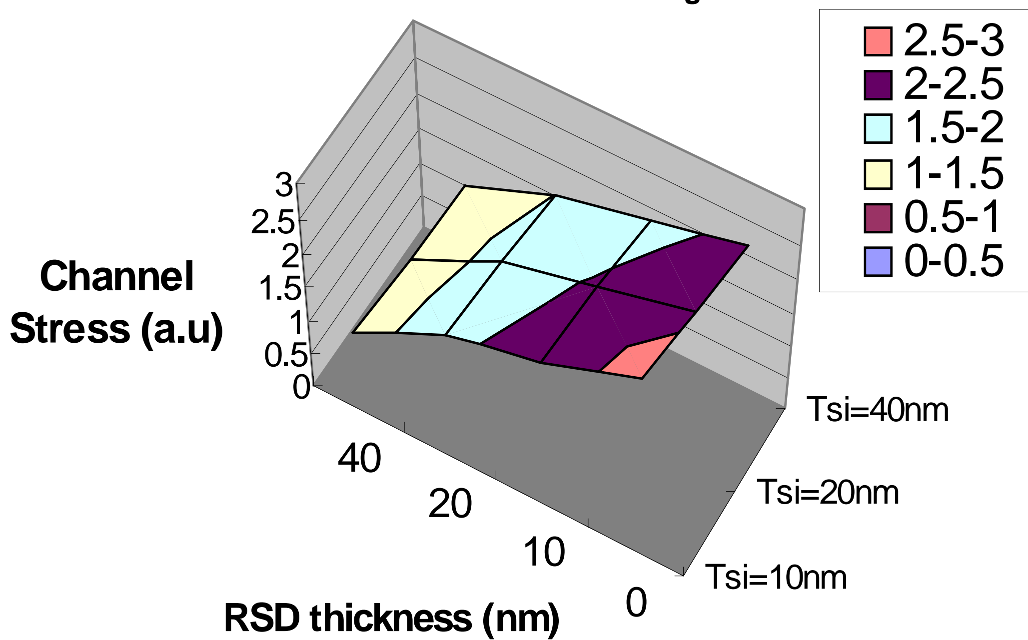


Fig. 2.4 Device channel stress versus different T_{si} and raised source/drain (RSD) thickness.

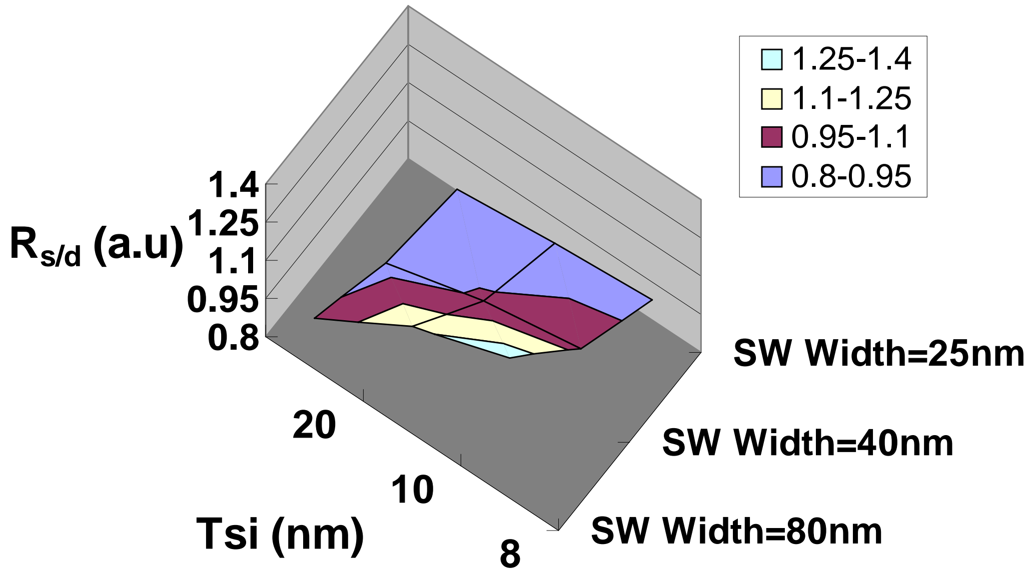


Fig. 2.5 Sheet resistance ($R_{s/d}$) versus different T_{si} and spacer width.

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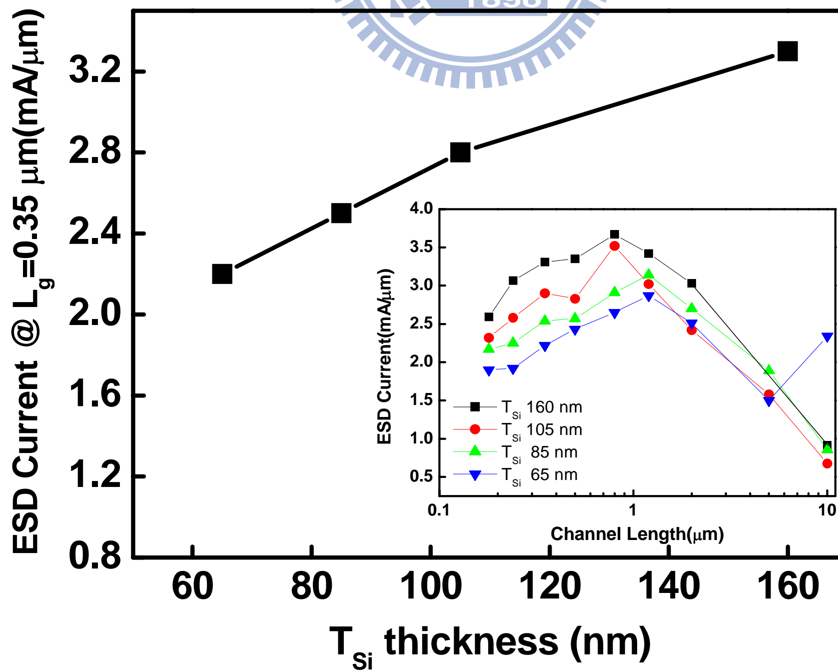

Fig. 2.6 ESD IT_2 current measurement of SOI devices with various Si thickness.

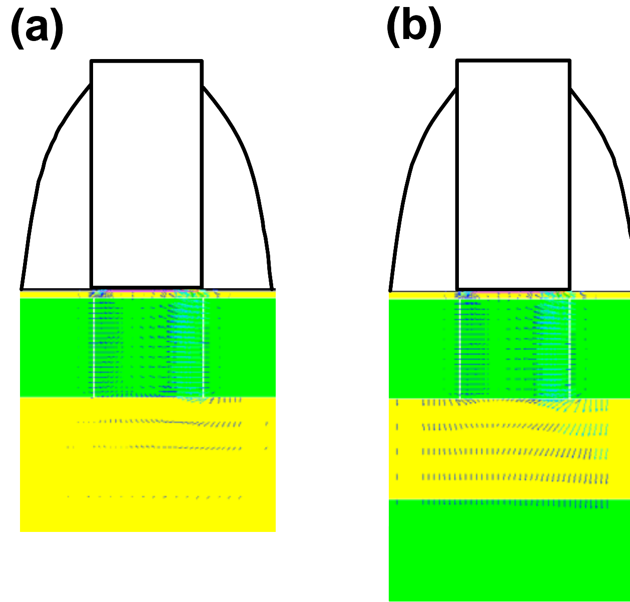

Fig. 2.7 Device drain-side fringe-field vector comparison between (a) TB-SOI and (b) TBO-SOI devices.

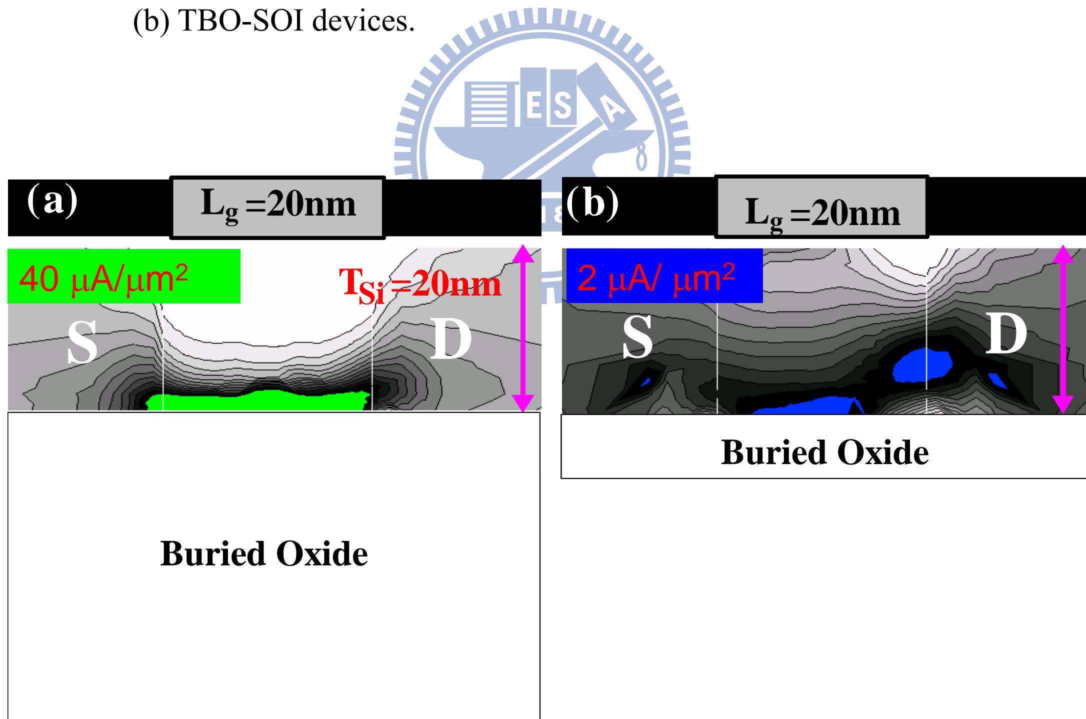

Fig. 2.8 Sub-threshold leakage current contours of (a) 100 nm buried oxide; (b) 20 nm TBO-SOI (thin buried oxide SOI) devices. SOI buried oxide thickness reduction suppresses the drain side field penetration and therefore decrease bottom channel leakage.

	Thin Body SOI	Thin Buried Oxide SOI
Short-channel effect control	Thin down Tsi to ~5nm; Gate has more control on channel than drain.	Direct most drain field to silicon substrate, not to channel
Tolerance to 2nm Tsi fluctuation	That is 40% of 5nm Tsi. (Not acceptable due to serious Vt variation)	2nm is just 10% of 20nm Tsi. (Reasonably acceptable for manufacture)
Parasitic R/C	High parasitic R at extention or S/D area.(Raised S/D is necessary)	High Cj,bottom than conventional SOI; (The Cj can be reduced by lightly doped substrate)

Table 2.1 Key manufacturability metrics comparison between TB-SOI and TBO-SOI.

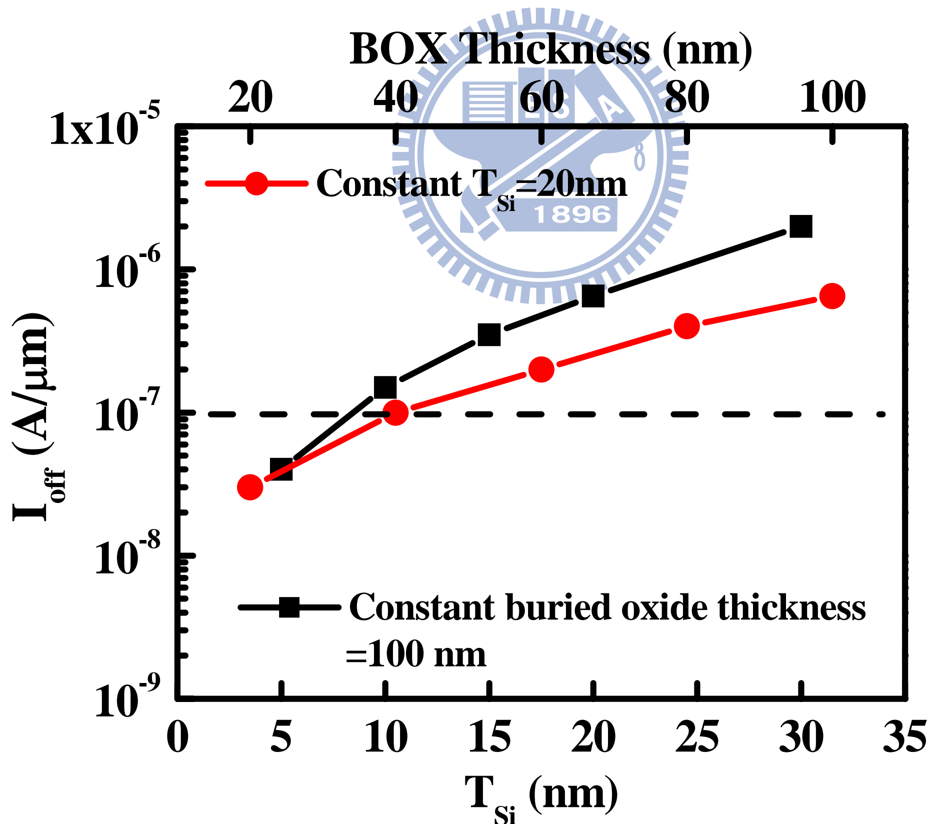

Fig. 2.9 Device I_{off} evaluation for two SOI scheme with using different structural parameter as variables.

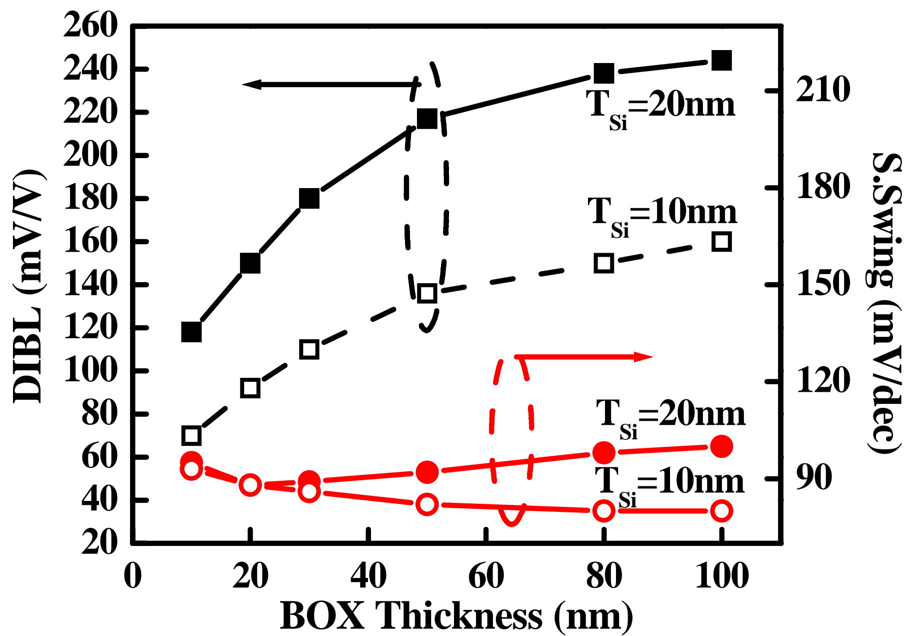

Fig. 2.10 Simulated DIBL (drain induced barrier lowering)/Sub-threshold swing characteristics versus SOI buried oxide thickness. The buried oxide thickness decreased to less than 20 nm induces sub-threshold swing degradation due to increasing parasitic capacitance.

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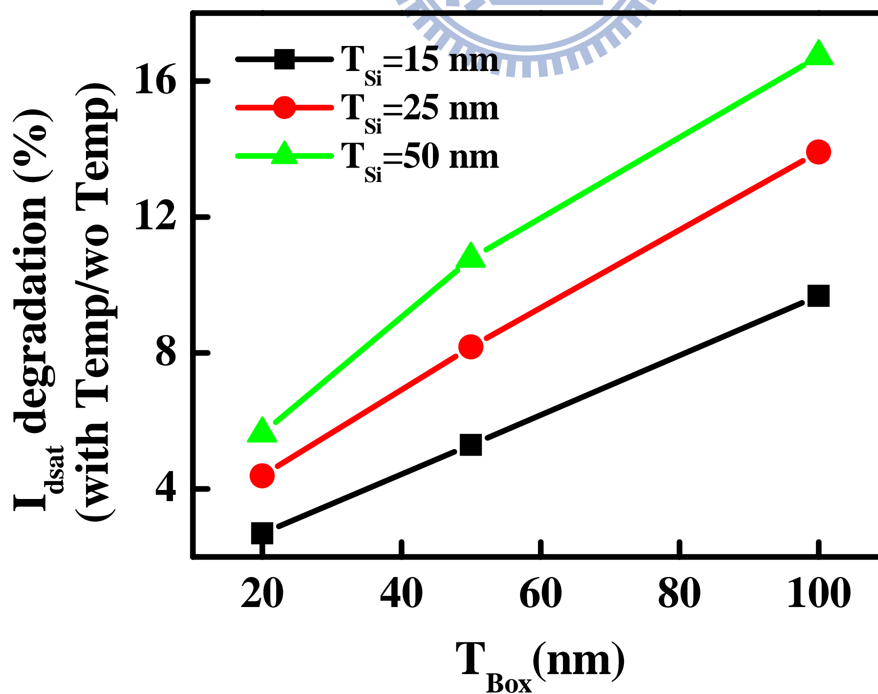


Fig. 2.11 Device drain current degradation ratio between with and without turning on the lattice temperature model in MEDICI.

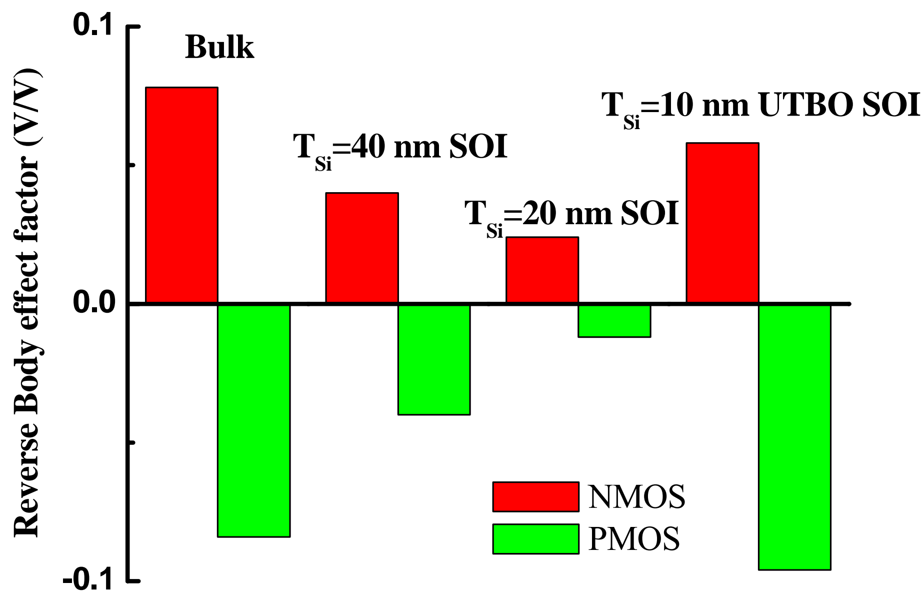


Fig. 2.12 Body effect factor comparison between various device schemes.

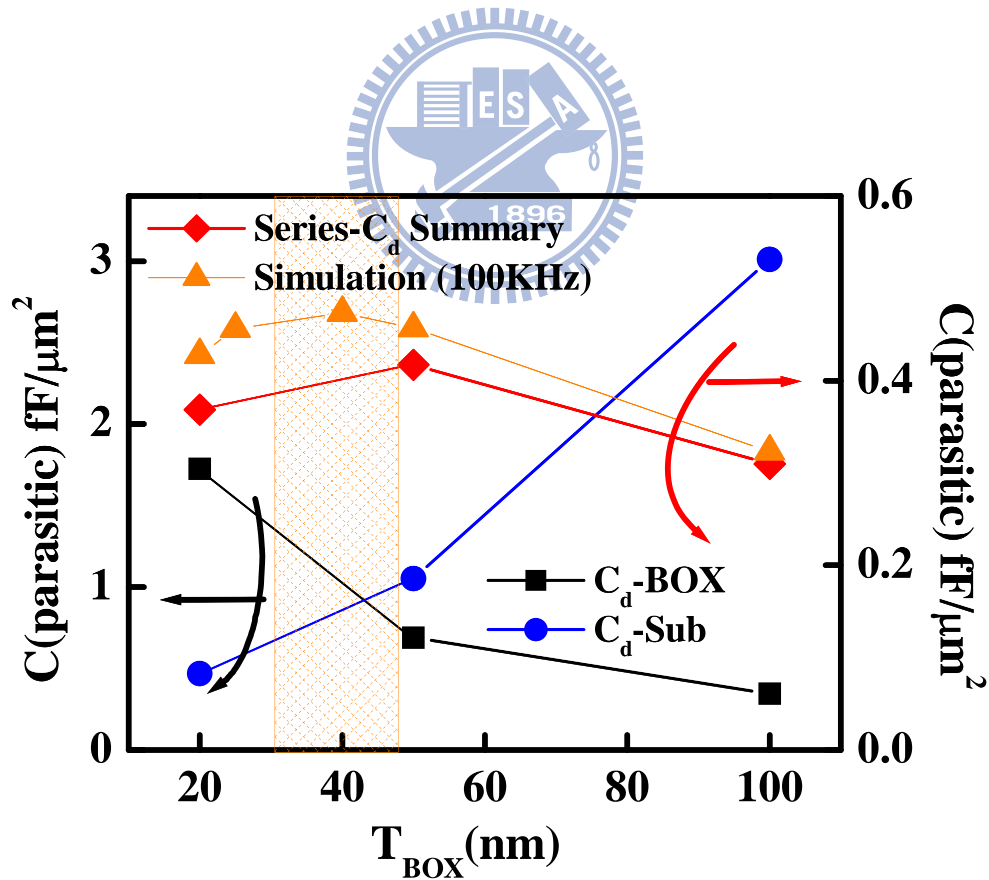


Fig. 2.13 The device parasitic capacitance at drain side with various buried oxide thickness.

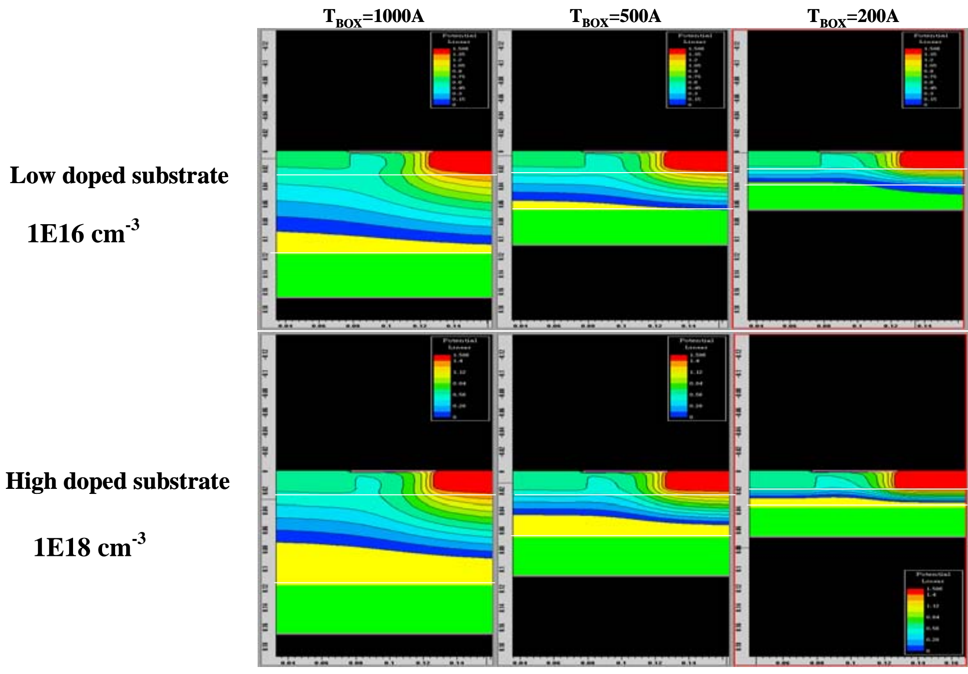


Fig. 2.14 Simulated device drain electric field with various buried oxide thickness and substrate doping concentration.

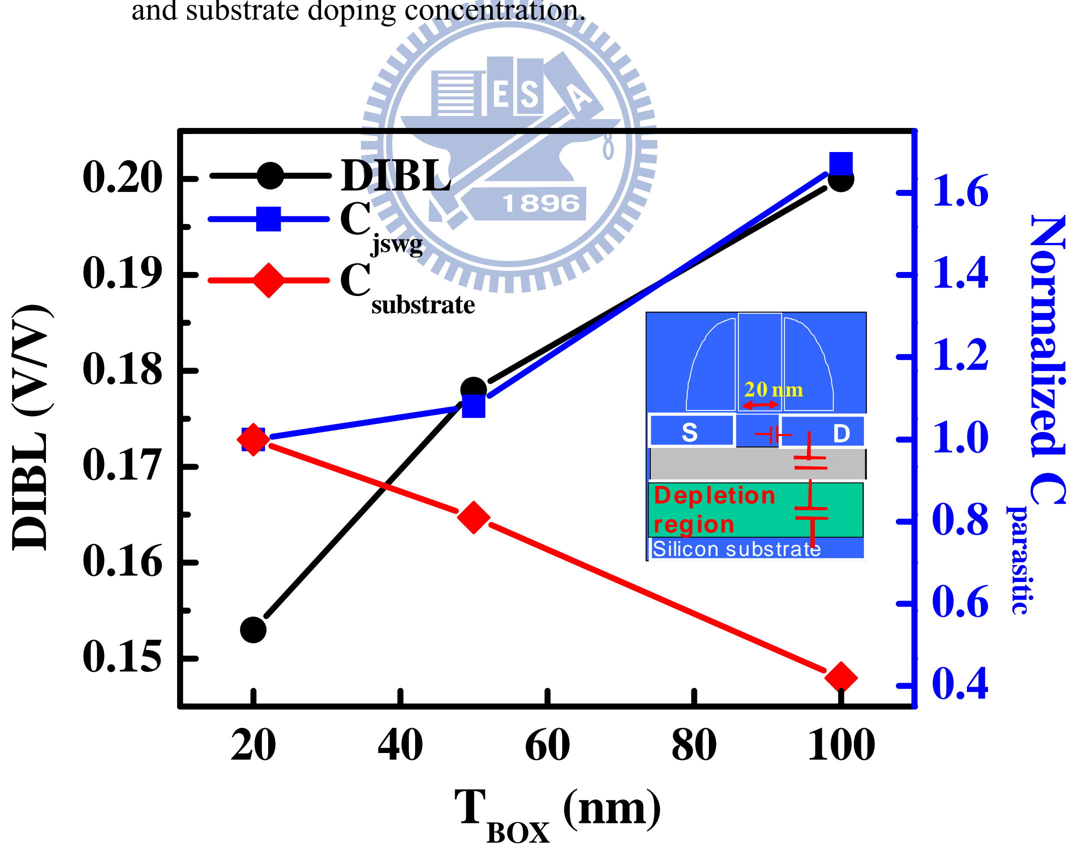
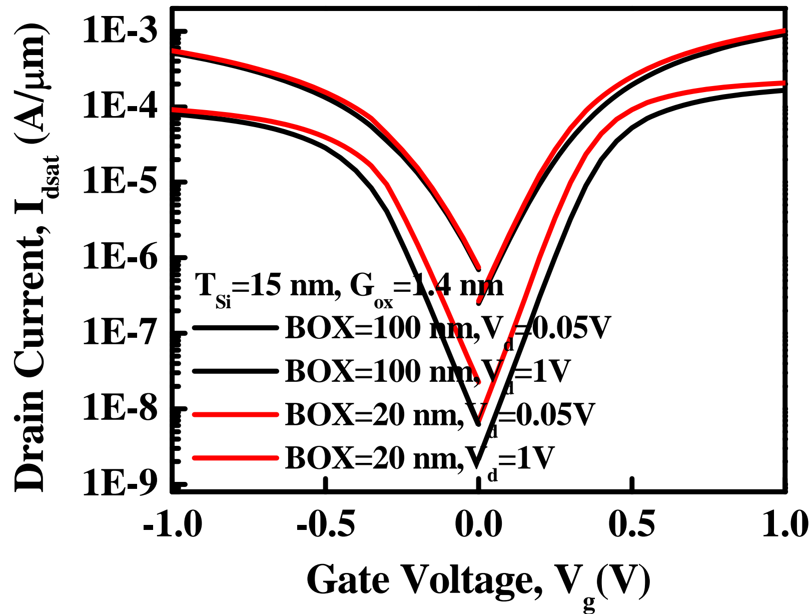


Fig. 2.15 Simulated device parasitic capacitance and DIBL with various buried oxide thickness.



N_b($1/cm^3$)	NMOS (4.57eV)	PMOS (4.85eV)
20 nm	1.0E+16	1.0E+16
100 nm	5.2E+17	2.5E+17

Fig. 2.16 Simulated I_d-V_g comparison between 20 nm L_g TB-SOI and TBO-SOI at a given I_{off}. The applied channel concentration of devices were listed below the figure.

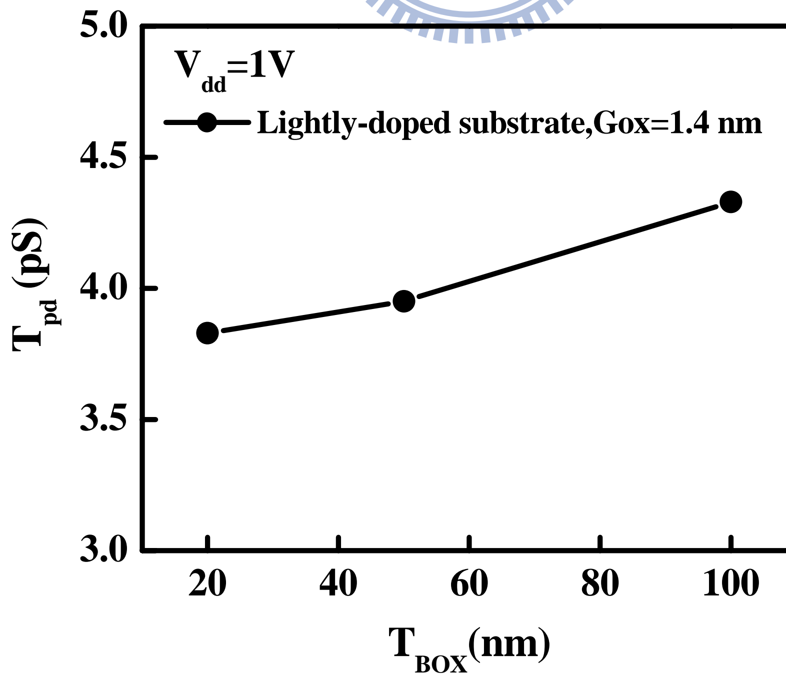


Fig. 2.17 Gate delay evaluation using 3-stages ring inverter by changing the buried oxide thickness of 20 nm L_g n/pFET while keeping a given I_{off} current.

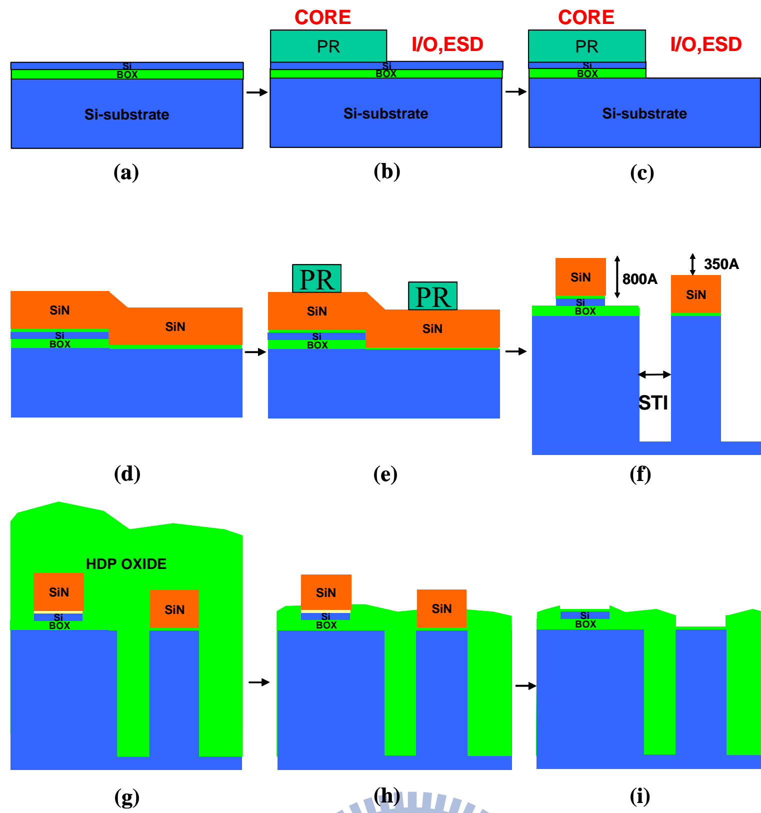


Fig. 2.18 The proposed integration flow of TBO-SOI with bulk substrate. (a) SOI/bulk definition; (b) STI etch; (c) STI gap filling; (d) STI oxide CMP, followed by SiN hard mask removing.

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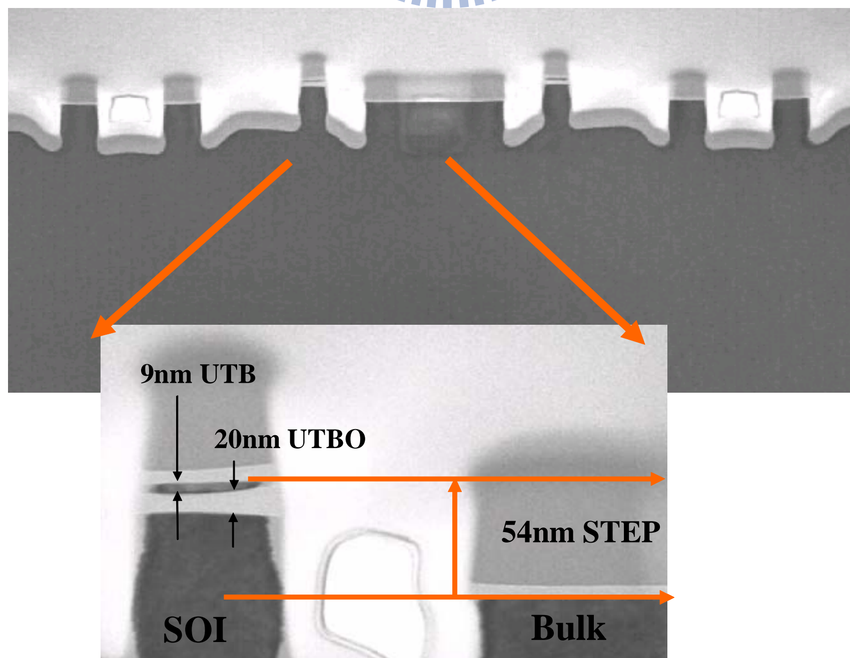


Fig. 2.19 TEM cross-section view of TBO-SOI and bulk substrate integration.

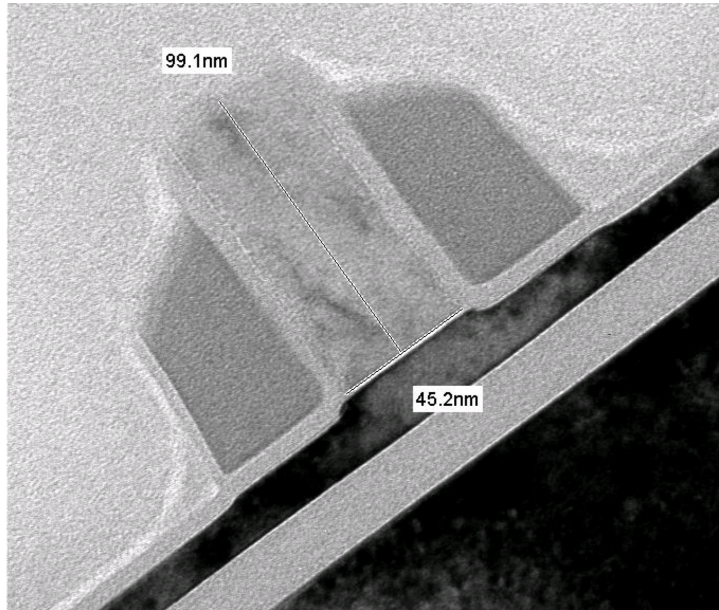


Fig. 2.20 TEM cross-section view of TBO-SOI device.

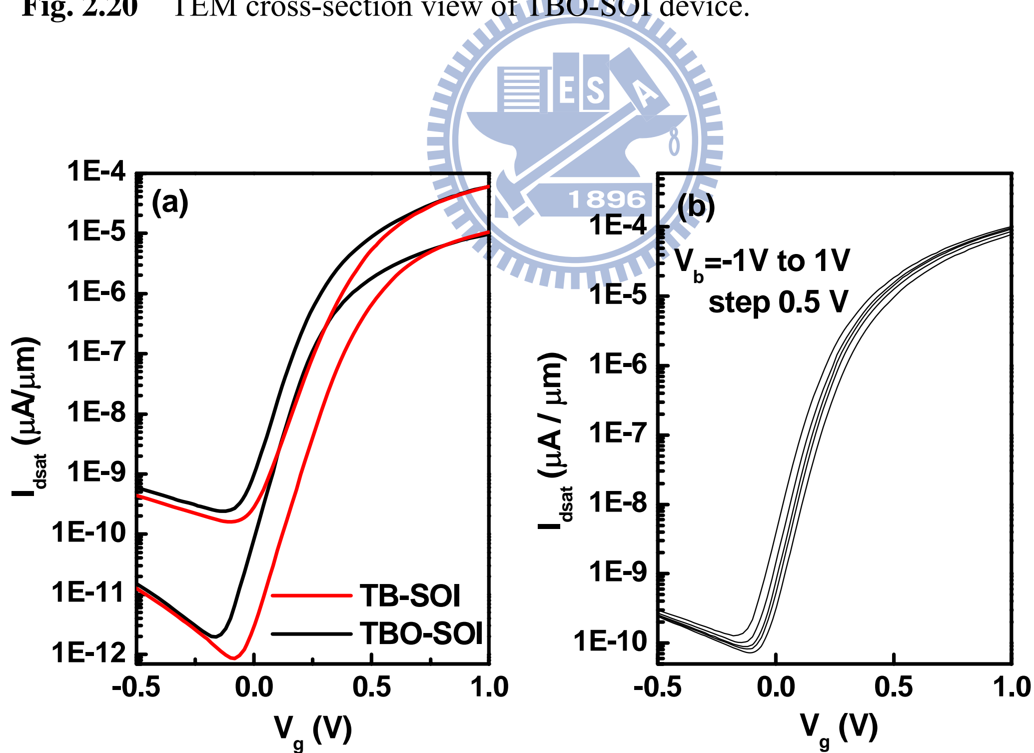


Fig. 2.21 The experimental I_d-V_g characteristics of (a) the comparison between TB-SOI and TBO-SOI with the same silicon thickness 20 nm and L_g=100 nm. (b) the back-gate bias sensitivity of TBO-SOI device.

Chapter 3

The Nanowire Device Fabrication and Its Sensing Application

3.1 Introduction

The nanostructures are widely investigated in electronic biosensor applications for the substitution of traditional chemical biomolecules detection, because their critical dimensions are comparable to the sizes of the biological or chemical species. In particular, the ability to detect ions in liquid solutions with nanoelectronic ion-selective field-effect transistor (ISFET) is attractive in several fields [56,13-16]. Among them, semiconducting nanowires field-effect sensors [16] have the great potential in label-free and real-time detection of low concentrations of proteins [13], virus [14], and DNA [15]. The Si nanowire used for sensor was proposed in early 2000 by Professor Liber's group, which initiated biomedical sensing using a nanometer-scale silicon nanowire device [56]. The excellent electrical characteristics and biosensing functionalities of these systems were originally demonstrated using single-crystalline Si nanowires fabricated by a bottom-up approach. At that time, most of the nanowires were fabricated by a bottom-up approach, such as CVD growth through the catalytic reaction to obtain a slender semiconductor nanowire. However, the nanowire needs post processing to locate it at dedicated location and requires an electrode, the microfluid, for real sensor functionality. Consequently, these sensor fabrication approaches are unique and difficult for mass production. The "top-down"

silicon nanowires fabricating process has been proposed to provide a solution for manufacturing reliable biosensors using commercial silicon-based CMOS technology [16].

Research on biosensing functionality using CMOS-compatible devices is evolving, taking advantage of the state-of-the-art CMOS technologies, including scaling of the feature sizes of the devices, mature fabrication techniques, and precise process control. Owing to the continuous progress in semiconductor technology, the dimension of the device has been scaled to the sub-20 nm regime, which is feasible for nanowire fabrication using manufacturing technology. Nevertheless, to obtain slender nanowires with large surface to volume ratio and extraordinary detection sensitivity, expensive techniques or advanced lithography tools were required [16, 57]. Thus, to use silicon nanowire field-effect transistor (NW FET) in future biomedical applications, quick fabrication of large amount of uniform, reliable devices, control of the electrical response at relatively simple detection, and reduction in the productive cost at a commercial scale are important issues that must be addressed.

In recent years, Si NW FETs fabricated using CMOS-compatible, top-down approaches on SOI substrates have been used for high-sensitive detection of biomolecular species [16]. To further reduce the manufacturing cost, a manufacture-friendly nanowire fabrication process, in which poly-Si was used as a channel material, was recently developed for the detection of pathogenic avian influenza DNA and avidin/streptavidin [17–18,58]. Nevertheless, all the above-mentioned nanowire fabrication methods are difficult to implement with commercialized, low-cost Si CMOS processing. However, fabrication of transistors with poly-Si nanowire channels is suitable for the manufacturing of low-cost semiconductors. Here, we demonstrated three label-free and real-time electrically based pH sensor using *n*-type poly-Si NW FET fabricated by the top-down process

using the conventional 0.35-μm CMOS-compatible semiconductor process. Table 3.1 compares the advantages of nanowire fabrication using top-down poly-Si as the channel material. In this work, no expensive lithography tools were employed for the definition of nano-scale pattern, and obvious electrical properties responses of pH sensing were detected at a normal circuit operation region. With no expensive lithography tools and better detective variation control, poly-Si NW FET pH sensor fabrication is potentially favorable in substituting the traditional chemical sensor for single-chip integration in future commercial applications.

3.2 CMOS-Compatible Planar Poly-Si Nanowire

3.2.1 Planar Poly-Si Nanowire Fabrication

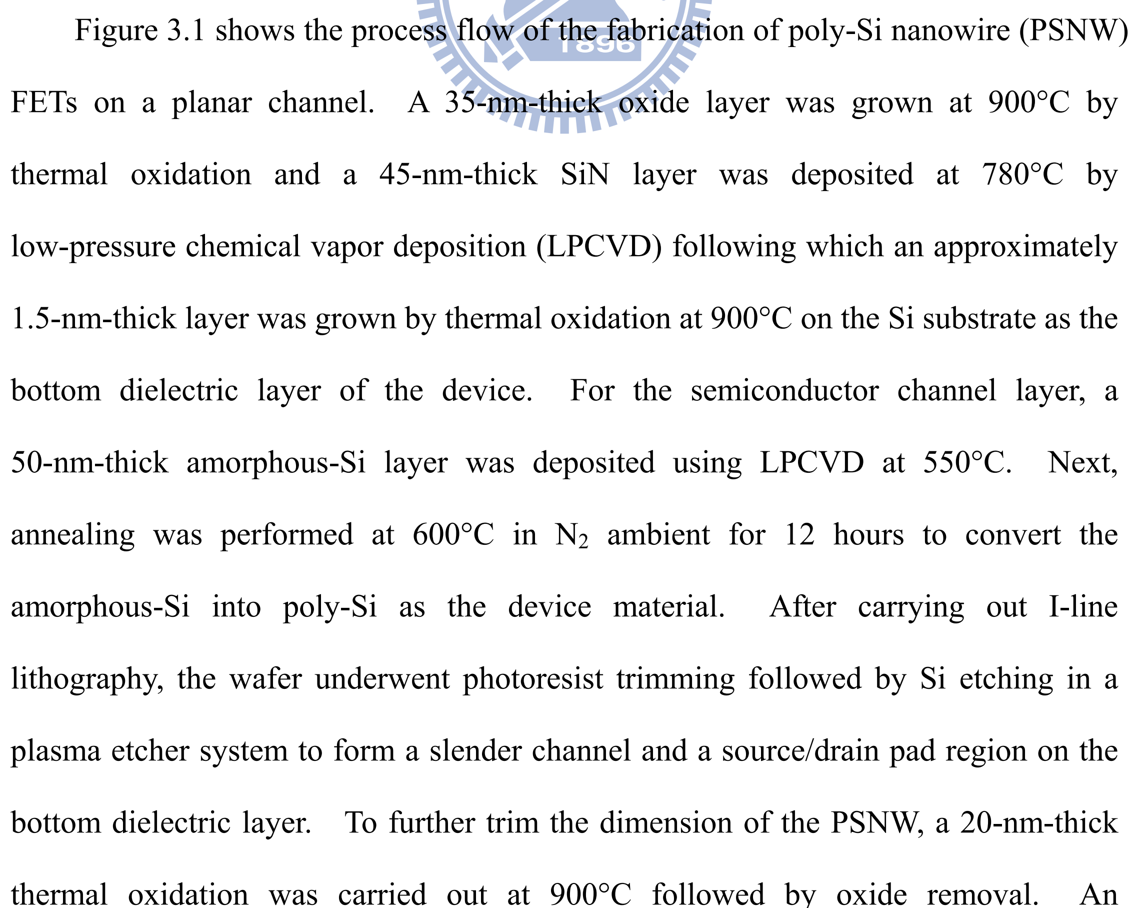


Figure 3.1 shows the process flow of the fabrication of poly-Si nanowire (PSNW) FETs on a planar channel. A 35-nm-thick oxide layer was grown at 900°C by thermal oxidation and a 45-nm-thick SiN layer was deposited at 780°C by low-pressure chemical vapor deposition (LPCVD) following which an approximately 1.5-nm-thick layer was grown by thermal oxidation at 900°C on the Si substrate as the bottom dielectric layer of the device. For the semiconductor channel layer, a 50-nm-thick amorphous-Si layer was deposited using LPCVD at 550°C. Next, annealing was performed at 600°C in N_2 ambient for 12 hours to convert the amorphous-Si into poly-Si as the device material. After carrying out I-line lithography, the wafer underwent photoresist trimming followed by Si etching in a plasma etcher system to form a slender channel and a source/drain pad region on the bottom dielectric layer. To further trim the dimension of the PSNW, a 20-nm-thick thermal oxidation was carried out at 900°C followed by oxide removal. An

approximate 40 nm PSNW width reduction can be obtained after the reoxidation and oxide stripping process. Figure 3.2 shows the scanning electron microscopy (SEM) images of the PSNW; the line edge roughness of the PSNW is preserved during the two-step trimming process and the nanowire width can be directly scaled to around 40 nm as determined by the transmission electron microscopy (TEM) analysis which is shown in Fig. 3.3. Subsequently, a channel protection photoresist was used to define the intrinsic Poly-Si channel region to increase PSNW sensitivity [59]; in addition, the n+ source/drain (S/D) region was implanted to reduce the resistance of the contact pad. Finally, the channel protection photoresist was removed and the S/D dopant was activated by annealing at 600 °C for 30 min.

3.2.2 Characterization of Planar Poly-Si Nanowire

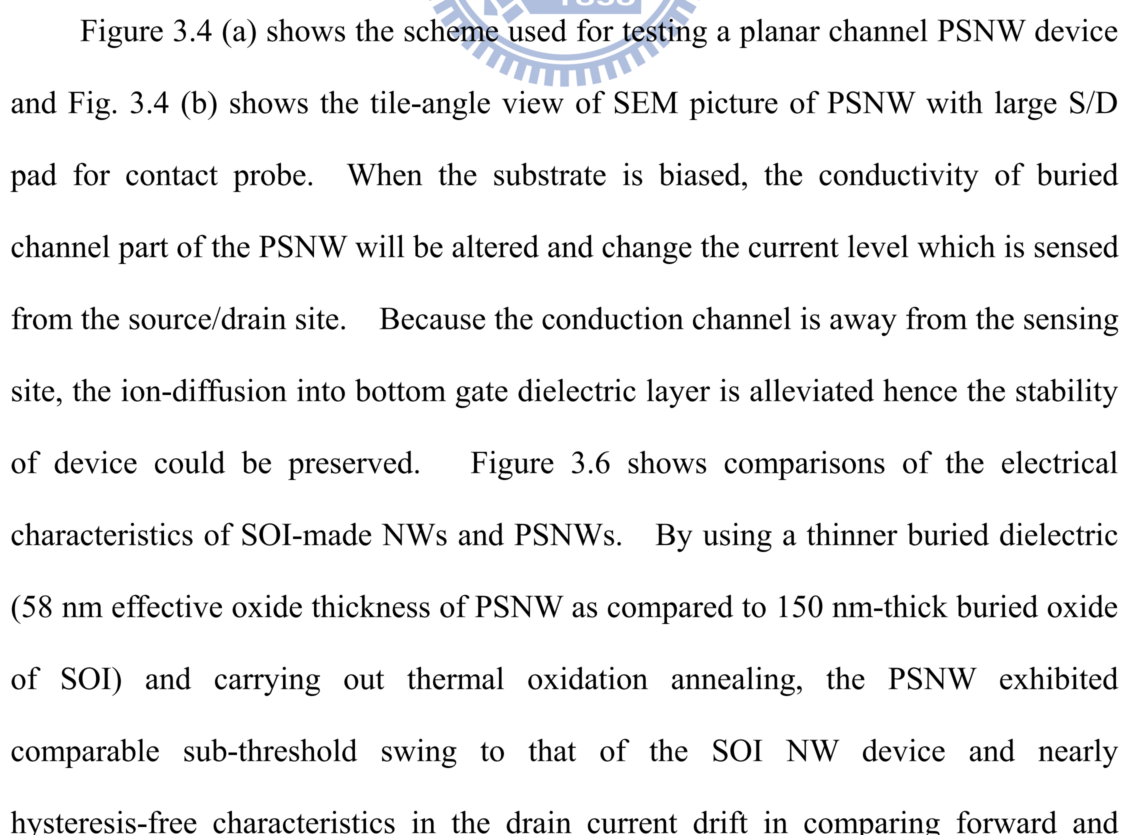


Figure 3.4 (a) shows the scheme used for testing a planar channel PSNW device and Fig. 3.4 (b) shows the tile-angle view of SEM picture of PSNW with large S/D pad for contact probe. When the substrate is biased, the conductivity of buried channel part of the PSNW will be altered and change the current level which is sensed from the source/drain site. Because the conduction channel is away from the sensing site, the ion-diffusion into bottom gate dielectric layer is alleviated hence the stability of device could be preserved. Figure 3.6 shows comparisons of the electrical characteristics of SOI-made NWs and PSNWs. By using a thinner buried dielectric (58 nm effective oxide thickness of PSNW as compared to 150 nm-thick buried oxide of SOI) and carrying out thermal oxidation annealing, the PSNW exhibited comparable sub-threshold swing to that of the SOI NW device and nearly hysteresis-free characteristics in the drain current drift in comparing forward and

reverse gate-voltage sweep directions which indicates that no significant mobile oxide charge is present and the density of slow interface trap is low [60,61]. Figure 3.7 shows the PSNW FET statistics of the comparisons of the electrical characteristics for various wire widths with and without shrinkage due to the reoxidation process, and these characteristics were collected from 32 dies in each wafer. The driving current measured as the bottom gate bias was 5 V and drain bias was 0.5 V without any liquid solution on the nanowire surface. After the reoxidation process, the scaled PSNW exhibited tighter current distribution and superior performance. The reoxidation process not only increases the surface-to-volume ratio of the nanowire but also improves the PR trimming induced by the surface roughness. Irene et al. [62] found that a thin layer of intergranular oxide was formed between the poly grain during the high-temperature oxidation process that reduces the charge state density at the poly grain interface and passivates the grain boundary without introducing a series resistance. Additionally, the tighter distributions imply higher production yield and more accurate detection ability for nanosensor fabrication. Figure 3.8 shows the driving current versus time data as phosphate buffer solutions with pH 5, 7 and 9 were sequentially delivered onto the NW sensors without surface treatment. The reoxidation split had larger I_{on} change as pH increment than without reoxideation split. The nanowire reoxidation shrinkage technique did improve driving current accumulation distribution and enhance the pH sensitivity of electrical properties. On the other hand, the poly-silicon NW FET pH sensor have higher manufacturing production yield and larger signal to noise ratio tolerance [63] in further single chip system integration of nanosensors. Figure 3.9 plots the NW FET driving current can increase and back to original value as the pH value raised from 5, 7, 9 and reversed to 7, 5 sequentially for various channel length NW FET. Consequently, the positive current shifts with pH value increment were repeatable in our n-type poly-silicon NW

FET pH sensors. The pH sensitivity of poly-Si NW FET electrical properties responses with different nanowire geometry were also evaluated in this work. Figure 3.10 illustrates the driving current sensitivity and V_{th} shift with different PH solution in various nanowire width and channel length conditions. The devices threshold voltage were defined by the gate voltage at a constant current:

$$I_d = 10^{-7} \times \frac{L_g}{W}$$

where V_d=0.5 V, L_g is intrinsic nanowire channel length and and W is the nanowire width. In nanowire width direction, narrower widths NW FET have higher pH sensitivity, and it is consist with the mention of most previous researches [64]. However, short channel split did not show apparent pH sensitivity in our experiment. The short channel devices had smaller intrinsic channel area and the rest of nanowire was doped with heavy S/D dopant to reduce nanowire parasitic resistance reduction and the influence of noise. However, the channel coupling effect is attenuated at the heavy doped nanowire region thus the pH sensitivity of short channel nanowire is reduced. Although short channel device have large current shift in different pH solution, the higher origin driving current of short channel effect will degrade the nanowire surface potential control ability and the pH sensitivity. Thus, the optimal device design is required to obtain sufficient sensitivity and noise tolerance for better pH sensitivity in the NW FET pH sensors.

To ensure stable device operation in a liquid solution environment, the plasma treatment was employed after S/D activation. NH_3 plasma treatment was carried out for 30 min, which effectively passivated the dangling bond of the PSNW buried channel interface and improved the device performance [65]. The device stability measurement under constant voltage stress (V_d = 0.5 V and V_g = 5 V) in a liquid solution environment is shown in Fig. 3.11. The plasma passivation reduces the

polysilicon-bottom oxide interface trap and avoids threshold voltage (V_{th}) variations due to mobile-ion diffusion in the aqueous solution. In addition, the NH_3 plasma can passivate the trap-state in the channel region hence the grain boundary barrier potentials are reduced which leads to significant performance improvement [65]. Figure 3.12 presents the I_d-V_g characteristics of the PSNW FET when the channel was exposed to buffered solutions with various pH values. At first, the PSNW I_d-V_g characteristics were measured in the dry environment and then solutions were injected. Compared to the I_d-V_g characteristics, the device characteristics measured in the aqueous solution exhibited performance improvement than measured in the dry environment. The H^+ and/or OH^- ions of solution may diffuse into the poly-silicon grain boundaries and terminate on the dangling bonds hence improve the device performance [66]. The increased conductivity of device when the pH was above 7 can be attributed to silanol (≡SiOH) groups present in the surface oxide layer. Because the acidity (pKa) of the silanol groups is ca. 6.8, deprotonation of the surface oxide layer occurs when the pH of the solution is higher than 7; this leads to the formation of negative charges on the surface [67]. As Fig. 3.13 shows, these changes in the net charge modifies the surface potential and generates space charges at the surface silicon-thin oxide interface, in turn modifying the channel conductivity. It's worth noting that when the solution was switched from pH=5 to 9 and then back to 5 again, the two I_d-V_g curves were not completely overlapping. The hysteresis is believed to be caused by the presence of buried OH sites just below the surface. The buried OH sites are generated due to the water (H_2O) diffuse into SiO_2 and react with the SiO_2 and forms Si-OH sites. Although this number of Si-OH site buried below the surface is small compared to the number of sites on the surface, those slow response buried site will alter the pH_{pzc} of the surface oxide and the response of NW FET is changed as a consequence and leads to the hysteresis [68,69]. As compared to the V_{th}

shift of the conventional surface channel ISFET, that of this buried-channel pH sensor (110 mV/pH) was significantly higher than the Nernst limit of 59.5 mV/pH [70,71]. By considering an analytical threshold voltage model and the body potential effect for thin Si SOI device, the back channel threshold voltage can be expressed by [72] :

$$V_{tb} = V_{fbb} + (1 + \frac{C_{si}}{C_{box}})\varphi_t + \frac{qN_a T_{Si}}{2C_{box}} - \frac{C_{si}}{C_{box}}\varphi_b ,$$

the coupling effect of the pH sensitivity can be approximately calculated by:

$$\delta V_{gb} \sim -\frac{C_{si}}{C_{box}}\delta\varphi_s$$

where V_{gb} is the threshold voltage of the buried-channel device; φ_s, the surface channel potential of the exposed device; and C_{si}, the Si-film capacitance ($\approx \varepsilon_s / T_{Si}$). The coupling factor magnifies the potential difference hence the pH sensitivity increases rather than conventional surface channel ISFET devices. In this experimental device, the coupling factor was 2.2 based on the bottom dielectric capacitance calculation; hence a 129.8 mV/pH sensitivity could be reached when the surface potential sensitivity reached the Nernst limit. In addition, the device exhibited excellent reversible electrical characteristics after sequential measurement, indicating its sensitivity and repeatability in response to the variation of the surface charge. Such behavior makes this device suitable for applications to electrochemical detection.

3.3 The Self-aligned Vertical Poly-Si Nanowire

3.3.1 FEOL Self-aligned Vertical Poly-Si Nanowire Fabrication

Another process flow for the fabrication of a vertical-channel PSNW device is presented in Fig. 3.14. After defining the Si-active region, Si etching was performed and followed by gap filling. After performing oxide chemical-mechanical polishing

(CMP) planarization, the SiN hard mask was stripped to form the device active area. A photoresist hard mask was used to protect the planar MOSFET device areas; the wafer was then subjected to an HF dip to partially remove the STI oxide regions in the unprotected areas. The approach is a simplified bulk FinFET process [78]; the fin-shaped active region acted as the gate electrode for the PSNW device. Using this sidewall NW formation approach, the vertical channel width and channel thickness of the NW in the device are readily controlled by varying the topography of the STI oxide recess region and the poly etch time. To increase the uniformity of PSNW fabricated in both side of fin-shape wall, an optimal dummy pattern insertion technique [74] as well as the advance CMP process [75] can be included to alleviate the pattern loading effect to obtain the same topographies in both side of STI recess areas. Notably, no costly lithography tools are required to achieve such nanometer-scale NWs and further dimensional shrinkage, to enhance the sensitivity, is achieved merely by increasing the poly etch time. The photoresist hard mask was stripped and then a 10-nm-thick layer of TEOS was deposited using LPCVD at 750°C, to function as the gate dielectric layer. A 50-nm-thick layer of poly-Si was deposited and then n+ doping implantation using arsenic (dose: 1×10^{15} /cm^2) was employed to induce PSNW source/drain doping. Patterning of the PSNW source/drain were performed using I-line lithography, followed by a reactive plasma etch for poly etching. This process led to the formation of a self-aligned undoped PSNW as a spacer of the fin-shaped active region. Next, a rapid thermal annealing (RTA; 900°C, 30 s; N_2 ambient) was used for dopant activation and defect reduction. After annealing, a thin oxide layer was grown on the poly-Si surface that acts as a passivation layer for the PSNW.

3.3.2 Characterization of Self-Aligned Vertical Poly-Si Nanowire

With this PSNW scheme, a significant portion of the PSNW channel was exposed to the environment during operation hence the device surface could be used as a sensing site by exploiting electrochemical reactions. An electrochemical reaction between the ambient and the device surface would induce charges at the channel surface, thus affecting the value of V_{th} of buried-channel devices. Because the sensitivity of the detection of small variations in conductance depends on the concentration or ionic strength of the undetermined species [64], an embedded electronic circuit that exhibits different degrees of signal amplification, with corresponding noise reduction, would increase the detection limits. Figure 3.15 shows the CMOS devices and PSNW can be fabricated simultaneously with one extra mask. By using this integration approach, involving a CMOS-compatible manufacturing process, the production cost, device uniformity, and chip dimensions can all be reduced significantly. Figure 3.16 shows the SEM images of the self-aligned vertical-channel PSNW formed around the fin-shaped Si. The cross-sectional TEM of PSNW is shown in Fig. 3.17. By using a regional shallow trench isolation oxide excess removal process during the fabrication of logic devices, we obtained self-aligned 65 nm-wide poly-Si nanowires without the need costly lithography tools. The resulting vertical and undoped channel poly-Si thin film transistor device exhibited independent gate bias control and a tunable gate work function for adjustment of the threshold voltage (V_t), facilitating its possible integration in very-large-scale integration circuits.

Figure 3.18 shows the I_d-V_g and I_d-V_d characteristics of PSNW devices. A current flow occurred along the vertical sidewall and, the carrier density was

modulated by the bias in the bulk Si. The on/off ratio of the device was ca. 10^5 with an applicable current level and a sub-threshold swing of 0.65 V/dec. Unlike in the case of previous studies, the gate-bias of each NW could be determined independently—a highly desirable property when such sensors are embedded in a very-large-scale integration (VLSI) circuit. In addition, the value of the V_{th} of this undoped NW could be readily controlled by varying the degree of gate-electrode doping, thereby allowing a reduction in the sub-threshold leakage current. Because a significant portion of the poly-Si NW channel was exposed to the environment during operation, the device surface could be used as a sensing site operating through electrochemical reactions. An electrochemical reaction between the ambient and the device surface would induce charges at the channel surface and, thereby, affect the value of V_t of buried channel devices. Figure 3.19 presents the I_d-V_g characteristics of the poly-Si NW FET and Fig. 3.20 shows the real-time I_d recording when the channel was exposed to buffered solutions of various values of pH. Similar to the sensing principle of planar-channel PSNW, the vertical-channel PSNW also exhibits the high pH sensitivity than conventional ISFET and the pH sensitivity is beyond Nerst limitation. Figure 3.21 shows and investigates the TCAD simulation using Synopsys ISE for elementary FET characteristics and channel carrier responses to surface charge. Those changes in net charge at exposed sensing site would modify the surface potential and generate space charges at the silicon–native oxide interface, thereby adjusting the channel conductivity. In addition, device also exhibited excellent reversible electrical characteristics after sequential measurement, indicating its sensitivity and repeatability in response to the variation of the surface charge. Such behavior is required if such a device is to find applicability for electrochemical detection. Because the sensitivity of the detection of small variations in conductance depends on the concentration or ionic strength of the undetermined species, an

embedded electronic circuit that exhibits different degrees of signal amplification, with corresponding noise reduction, would increase the detection limits.

3.3.3 Poly-Si Nanowire Surrounding the W-plugs

A new triangle-shape NW FETs surrounding the W-plug was also demonstrated in this work. Simplified manufacturing flow of triangle-shape NW is presented in Fig. 3.22. The poly-Si spacer NW can be self-formatted around the exposed W-plug without lithograph patterning. The top-view SEM image of triangle-shape NW array is shown in Fig. 3.23. As shown in the FIB cross-sectional picture (Fig. 3.24), the triangle-shape NW was formed around the W plug with self-alignment. The S/D and gate pad of triangle-shape NW also can be defined simultaneously by poly Si patterning. By using the triangle-shape NW formation method, the low temperature NW FETs can be integrated in existing VLSI circuit more simply.

3.4 Applications of Poly-Si Nanowire (PSNW)

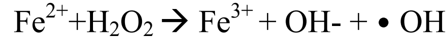
3.4.1 Nanoparticle-Capped PSNW for Chemical Sensing

In terms of devices chemical sensing evaluation, the ferritin and hydrogen peroxide reaction was investigated using vertical-channel PSNW. The ferritin is a ubiquitous iron storage protein that plays a key role in iron metabolism and serves as an intracellular iron reserve. Some previous literatures have shown that iron release from ferritin and its associated toxicity is a risk factor of neurodegenerative diseases including Parkinson disease and Alzheimer disease [76,77]. In addition, the redox

processes of the iron can generate free radicals and strongly oxidizing species capable of causing biological damage. Thus, we employed this device to monitor the ferritin and hydrogen peroxide reaction induced electrical characteristics variation. Regarding to the surface modification of devices, the nanowires chip was firstly sonicated in 100 % Ethanol for 1 min to remove contaminants and then dried with N_2 air flow. The chip was further cleaned and oxidized with UVO for 5 minutes and then soaked in 2 % APTES in pure Ethanol for 30 minutes. Then chip was washed with 100% Ethanol and dried with N_2 again. The chip was then soaked in 2.5 % Glutaradehyde in PBS buffer with 4 mM Sodium cyanoborohydride for 1.5 hr and then washed the chip with PBS buffer. Then soaked the chip in 500 ug/ml equine spleen ferritin (Sigma, F4503) in PBS buffer with 4 mM Sodium cyanoborohydride for proper treatment time and finally washed the chip with PBS buffer and distilled water violently. In this work, two different ferritin particle density were deposited on the nanowires by controlling the soaking time and SEM pictures are shown in Fig. 3.25. By increasing the soaking time, the 10-nm diameter ferritin were uniformly distributed around the nanowire which is shown in Fig. 3.25 (b) [77]. After the ferritin were coated on the device surface, the chips were then soaked into the different concentration of hydrogen peroxide solution for 10 minutes and then dried in the N_2 gas for subsequently electrical testing.

Figure 3.26 shows the devices I_d-V_g characteristics after the chips were treated at different concentration of hydrogen peroxide solution. With the lower density of ferritin-coated sample, Fig. 3.26 (a) shows no significant devices characteristics change unless the concentration of hydrogen peroxide was increased to 31%. On the contrary, a significant device conductance variation was observed for low concentration of hydrogen peroxide solution reacted with the high density of ferritin-coated chip. The ferrous ion of the ferritin will react with hydrogen peroxide

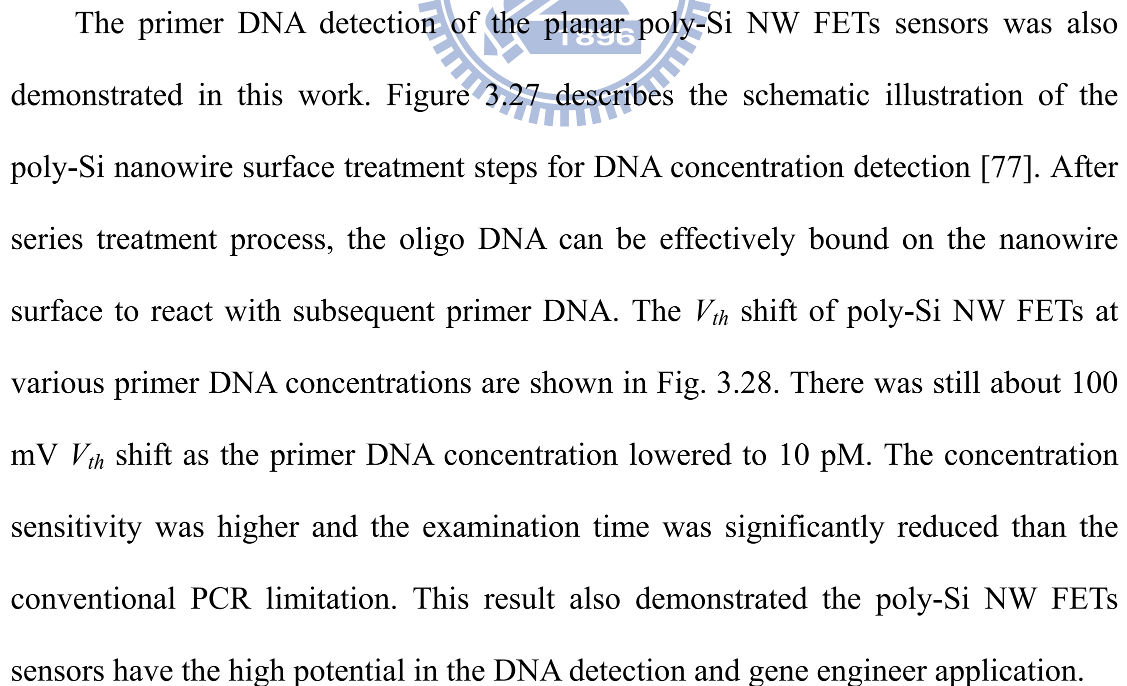
hence the so-called “Fenton Reaction” may occurs:



$$Fe^{2+} + H_2O_2 \rightarrow Fe^{3+} + OH- + \bullet OH$$

The process will generate the Ferric ion at the device surface and increase positive charges density which induce the negative charges in the device surface channel and reduce the buried-channel device conductivity. When the ferritin density is not reach a critical value, the quantity of ferrous ion are not sufficient therefore there is no significant surface charge varied to induce the device *I-V* characteristics change unless a very high hydrogen peroxide concentration is applied. By using this method, the ferrous ion concentration could be monitor which is a implicative index of the free radical generation.

3.4.2 DNA Detection using PSNW



The primer DNA detection of the planar poly-Si NW FETs sensors was also demonstrated in this work. Figure 3.27 describes the schematic illustration of the poly-Si nanowire surface treatment steps for DNA concentration detection [77]. After series treatment process, the oligo DNA can be effectively bound on the nanowire surface to react with subsequent primer DNA. The V_{th} shift of poly-Si NW FETs at various primer DNA concentrations are shown in Fig. 3.28. There was still about 100 mV V_{th} shift as the primer DNA concentration lowered to 10 pM. The concentration sensitivity was higher and the examination time was significantly reduced than the conventional PCR limitation. This result also demonstrated the poly-Si NW FETs sensors have the high potential in the DNA detection and gene engineer application.

3.4.3 PSNW Sensor with Embedded Memory

By replacing the gate dielectric layer to the composite oxide/nitride/oxide layer like conventional non-volatile memory as shown in Fig. 3.29, the electrical characteristics of the nanowire devices can also be adjusted by programming or erasing the nitride charge of the special designed ONO bottom oxide. This embedded EEPROM cell can be easily integrated into the CMOS sensor circuit. The combination of sensor, memory and circuit into the FEOL/BEOL CMOS-compatible process will provide a system-scale integration solution of the smart biosensor application for low cost commercial manufacturing. In high dielectric field, the nitride trap charge of the ONO bottom oxide can be filled or removed, and then the poly-Si nanowire buried-channel potential would be modified. Figure 3.30 plots I_d–V_g characteristics of the ONO bottom oxide poly-Si NW FETs at different operation mode. After a short initial pre-stress (V_g= -10V, 10 sec), the V_{th} of the poly-Si NW FETs can be adjusted after adequate programming condition. And the electrical characteristics of various operation conditions were reappearance. Figure 3.31 compares the programming and erasing efficiency characteristics. The V_{th} shift of the ONO bottom oxide poly-Si NW FETs were over 3V when the programming time was around 10 ms at the adequate operation bias. The endurance characteristics of the ONO bottom oxide poly-Si NW FETs are shown in Fig. 3.32 (a). The programing/erasing V_g bias condition is 20V/-12V, respectively. The memory V_{th} programming/erasing window was still large than 2V even after 10^5 operation cycles. Data retention characteristics of the poly-Si NW FETs device are also shown in Fig. 3.32 (b). The memory V_{th} P/E window can be larger than 2V after 3 days long time bake. These reliability characteristics both demonstrated that the ONO bottom oxide poly-Si NW FETs have great potential as EEPROM cell in the embedded memory application. The pH testing of the poly-Si NW FETs were also implemented at various V_{th} level. Figure 3.33 shows that the V_{th} shift of the surface pH ionic coupling

and nitride charge trapping follows the same I_{on}-V_{th} trend. The strongly V_{th} adjustable nanowire device provides a consistent electrical response for self-alterable correction and memory integrated applications. The versatile poly-Si NW FETs can be employed to integrate the sensor and logic-based devices in a VLSI chip, as illustrates in Fig. 3.34.

3.5 Summary

In this chapter, we demonstrated an inexpensive and high-production yield fabrication process for poly-Si nanowire FET devices that can be used for applications to electrochemical sensors. The device uniformity was controlled well by using certain manufacturing processes. Additionally, the highly integrated process will help to serve as an interface to connect the sensor and logic-based devices, as illustrates in Fig. 3.34. The proposed process should lead to the development of portable and inexpensive sensor systems-on-a-chip that are mass produced using conventional semiconductor technology for applications to healthcare. Furthermore, we reported a V_{th}-adjustable poly-Si nanowire biosensor with FEOL/BEOL CMOS-compatible process. The poly-Si NW FETs had obvious positive pH sensitive slope (V_{th} shift > 100 mV/pH) and very sensitive DNA concentration detection (V_{th} shift > 100 mV in 10 pM). In addition, the ONO bottom oxide poly-Si NW FETs also exhibited robust endurance and retention characteristics (V_{th} P/E window >2 V after 100K P/E cycle or 3 days bake time) as non-volatile memory for smart biosensor integrated with CMOS circuit.

Reference	A	B	C	D	This work-I	This work-II
NW Formation	CVD	TMAH (Wet)	SNAP (Imprint)	E-beam	I-line	Spacer
NW material	Si	Si (SOI)	Si (SOI)	Poly Si	Poly Si	Poly Si
On/Off ratio	~10^4	~10^5	~10^4	N/A	~10^6	~10^6
Current level	>uA	~uA	>uA	nA	~uA	~uA
Pro	• Small diameter. (<10nm)			• Small diameter. (< 30nm) • Compatible to VLSI process.	• Simple process, lower cost. • Be able to mass production. • Can be integrated to VLSI.	
Con	• To integrate with VLSI is difficult. • Higher manufacture cost. • Mass production is a challenge. • Uniformity control.			• Higher manufacture cost. • Lower throughput.	• Limited diameter.	• Uniformity.

Table 3.1 Comparisons of Si NW FETs made with previous papers and this work.

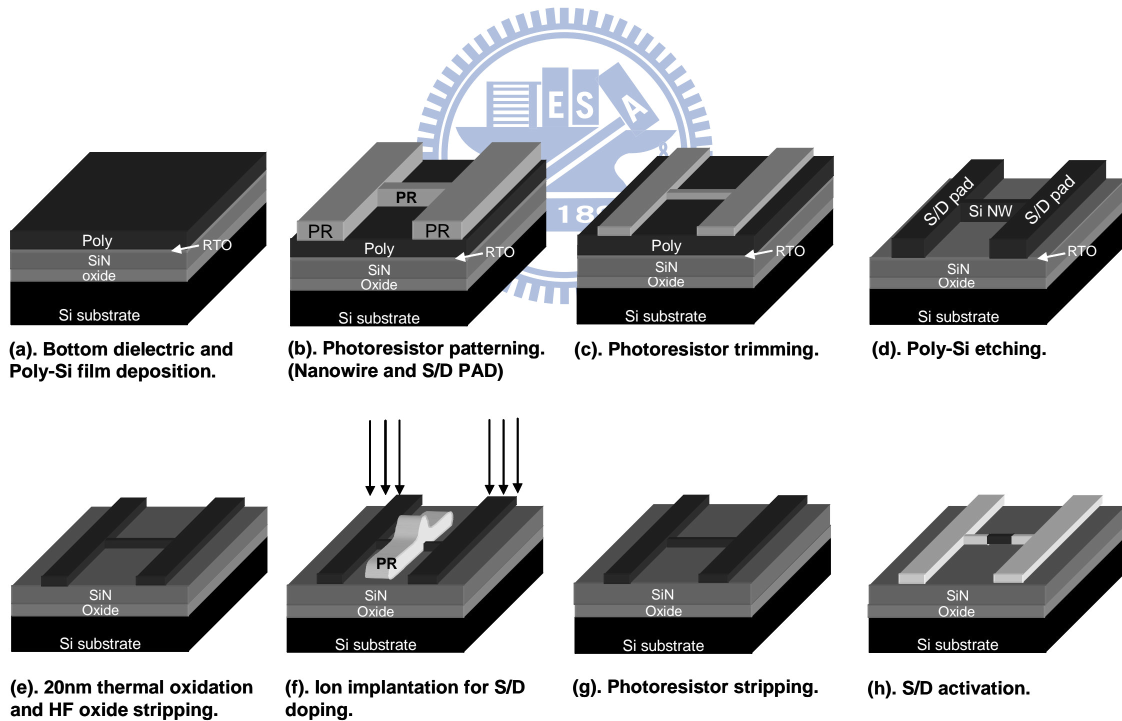


Fig. 3.1 Process flow for the fabrication of planar channel PSNW. A 10 keV and 5×10^{15} /cm^2 phosphorus implantation is used for S/D pad resistance reduction. RTA is carried out at 900°C for 30 s for dopant activation.

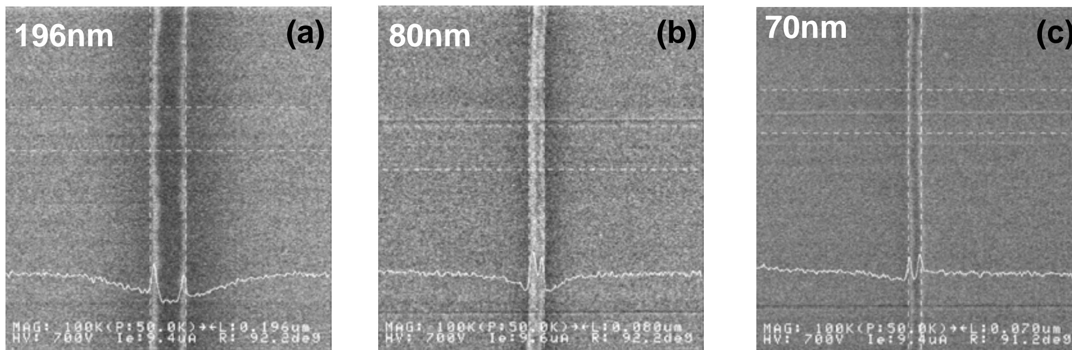


Fig. 3.2 The top-down SEM images of the poly-Si nanowire two-step trimming process flow. (a) The nanowire photoresistor pattern after I-line exposure. (b) The photoresistor pattern after first plasma trimming. (c) The nanowire after Si etch and thermal oxidation trimming. (d) The cross-sectional TEM image of two-step trimmed nanowire.

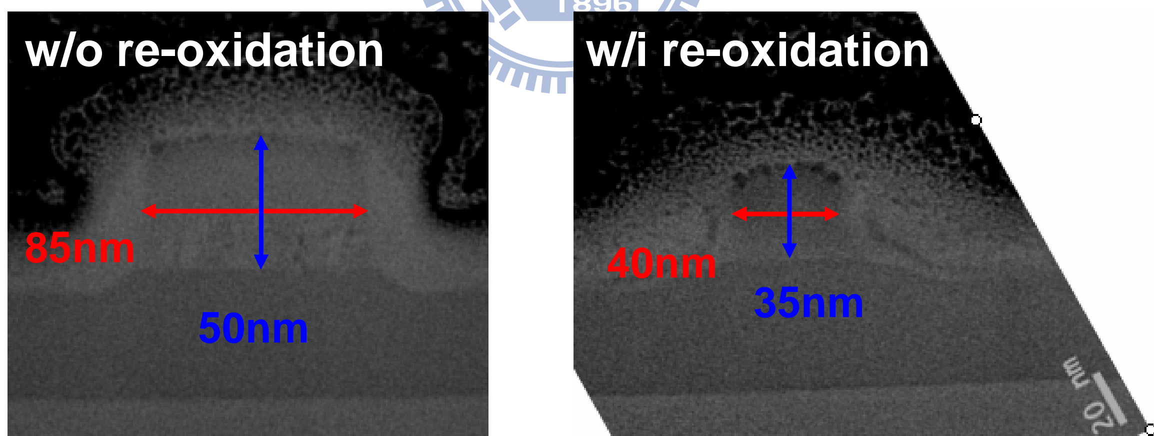


Fig. 3.3 The cross-sectional TEM image of PSNW. (a) with only PR trimming process (b) with two-step trimmed process.

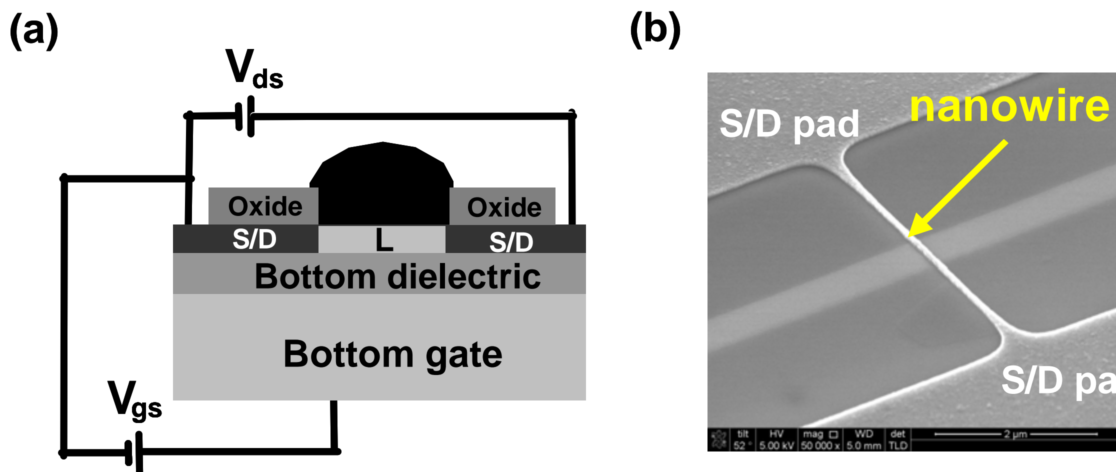


Fig. 3.4 (a) The schematic illustration of the PSNW electrical testing configuration. (b) Tilt-angle SEM image of the single poly-Si nanowire with S/D pad.

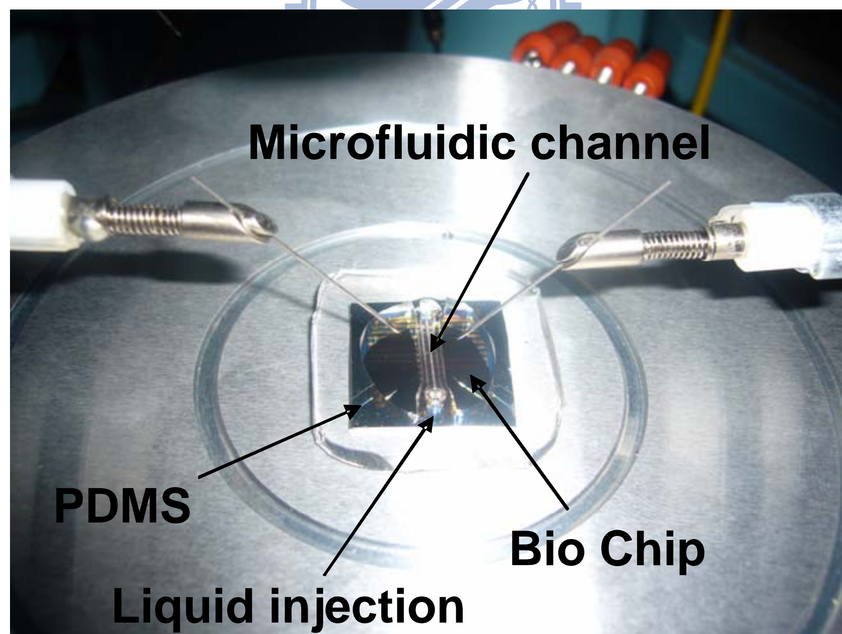


Fig. 3.5 The electrical testing configuration of the PSNW in the aqueous environment. The solution was conducted to the nanowire by a PDMS made microfluid capping over the PSNW chip.

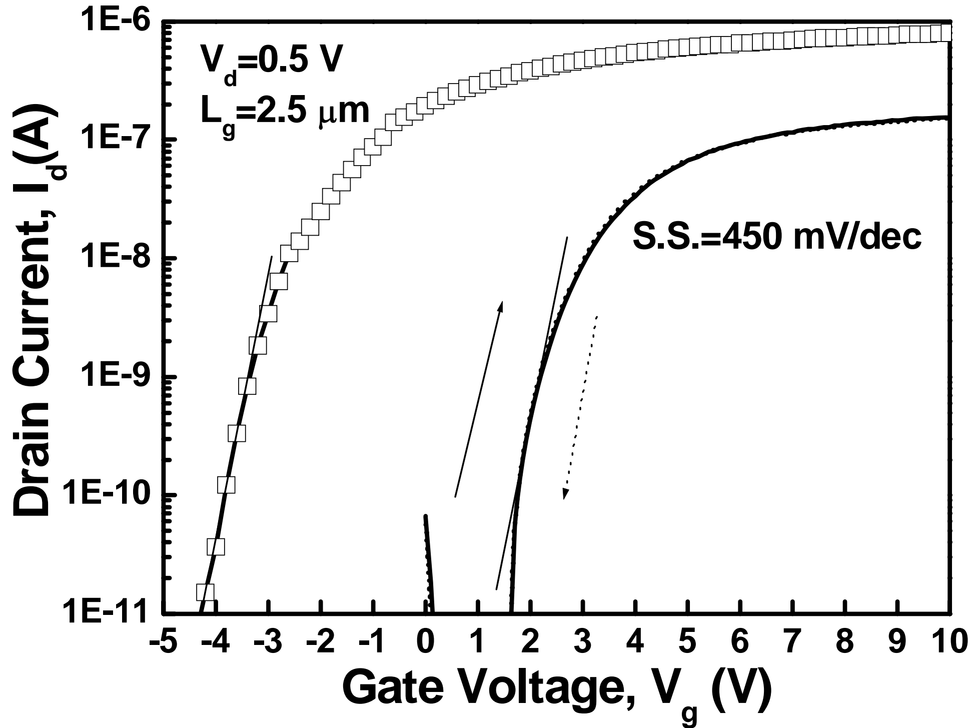


Fig. 3.6 Comparison of I_d-V_g characteristics of a fabricated PSNW FET device and SOI maded NW FET.

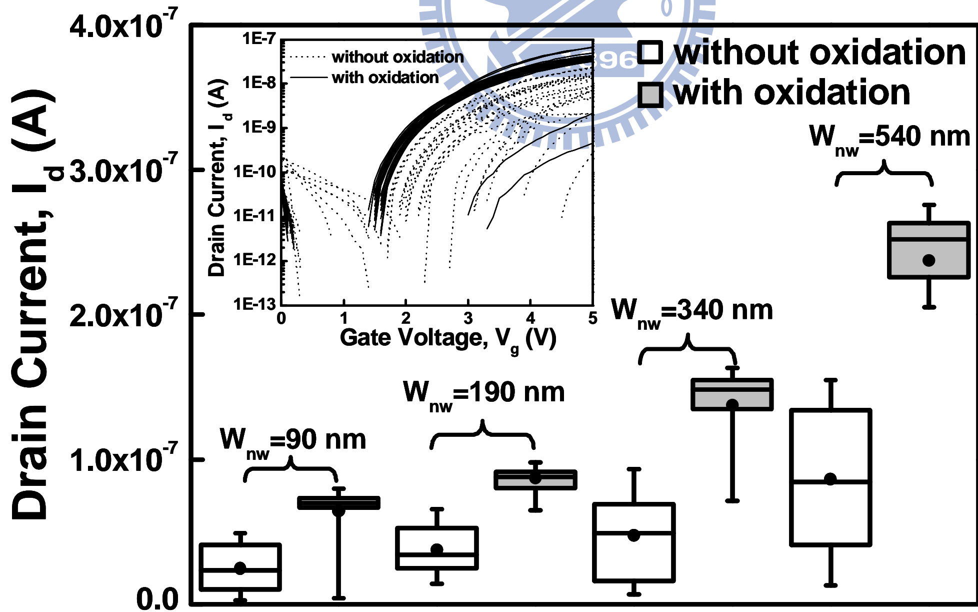


Fig. 3.7 PSNW FETs I_{dsat} distribution within the wafer with various nanowire widths measured by SEM before oxidation. Those devices with second oxidation trimming exhibit superior current uniformity and device performance. Inset shows a comparison of the 32 dies I_d-V_g characteristics for different oxidation effects.

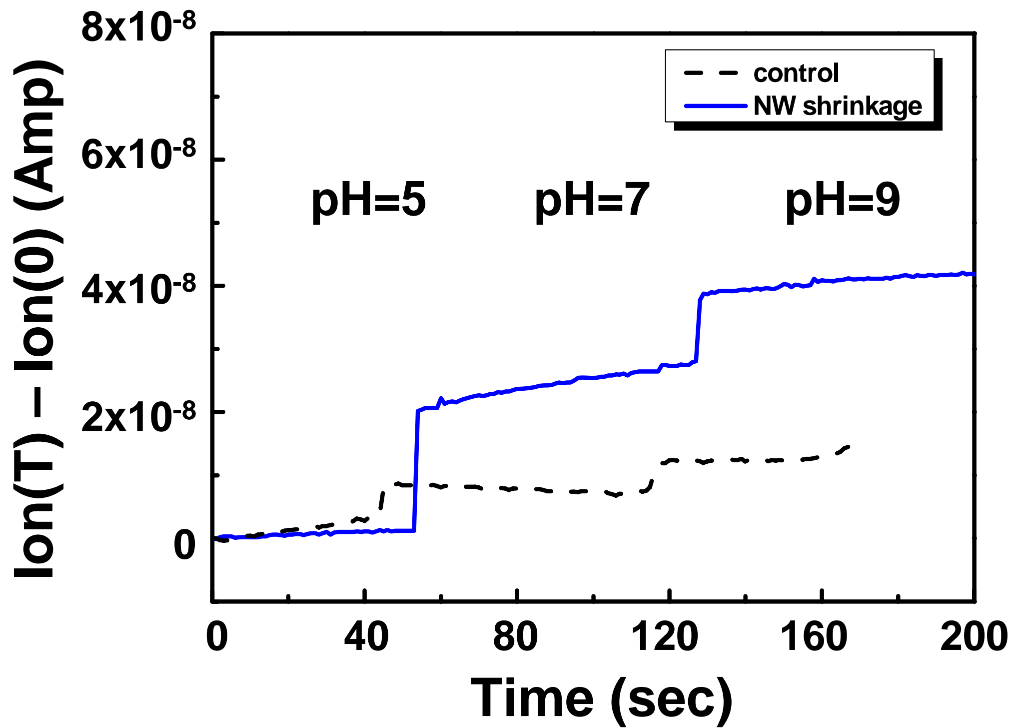


Fig. 3.8 Real-time driving current data for pH sensing at bottom gate bias, V_g, is 5V for without and with reoxidation split.

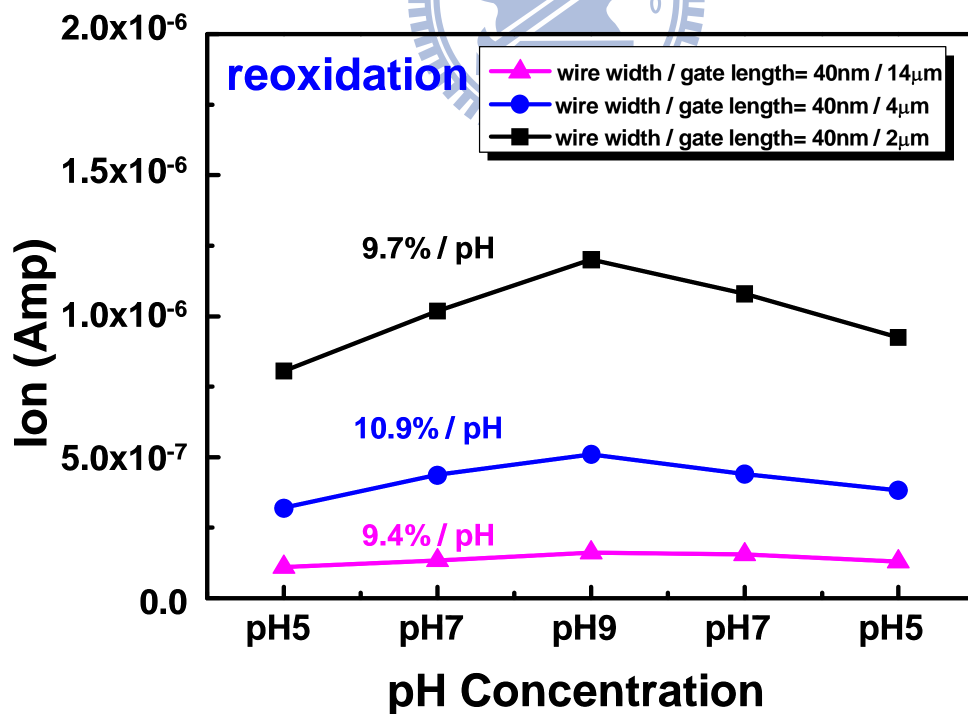


Fig. 3.9 Driving current pH sensitivity of poly-silicon NW FETs with pH value increases from 5, 7, 9 and reverse to 7, 5 sequentially.

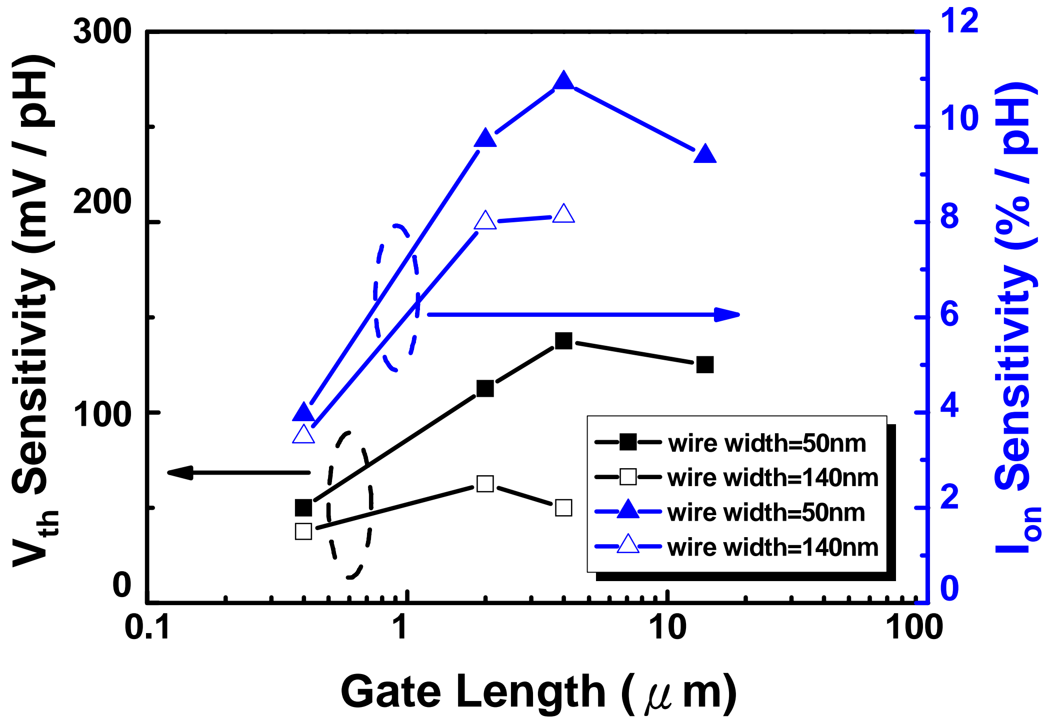


Fig. 3.10 Electrical characteristics pH sensitivity of poly-silicon NW FET device for various nanowire geometry.

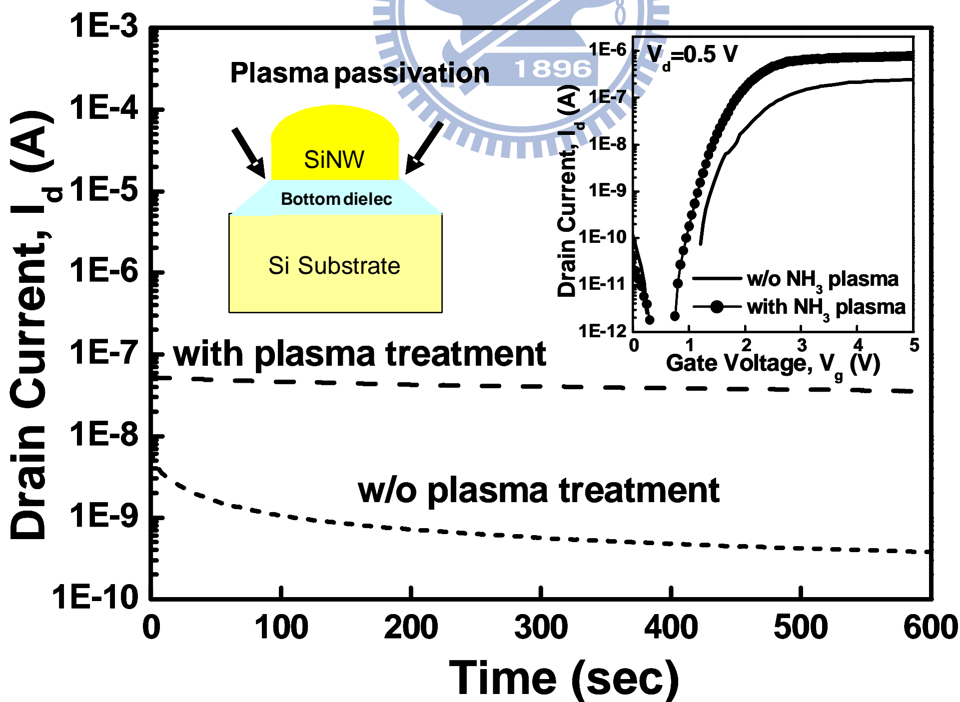


Fig. 3.11 NH_3 plasma treatment improves the Poly-Si nanowire FET performance and stability under high V_g (V_g= 5V) stress condition in the aqueous environment.

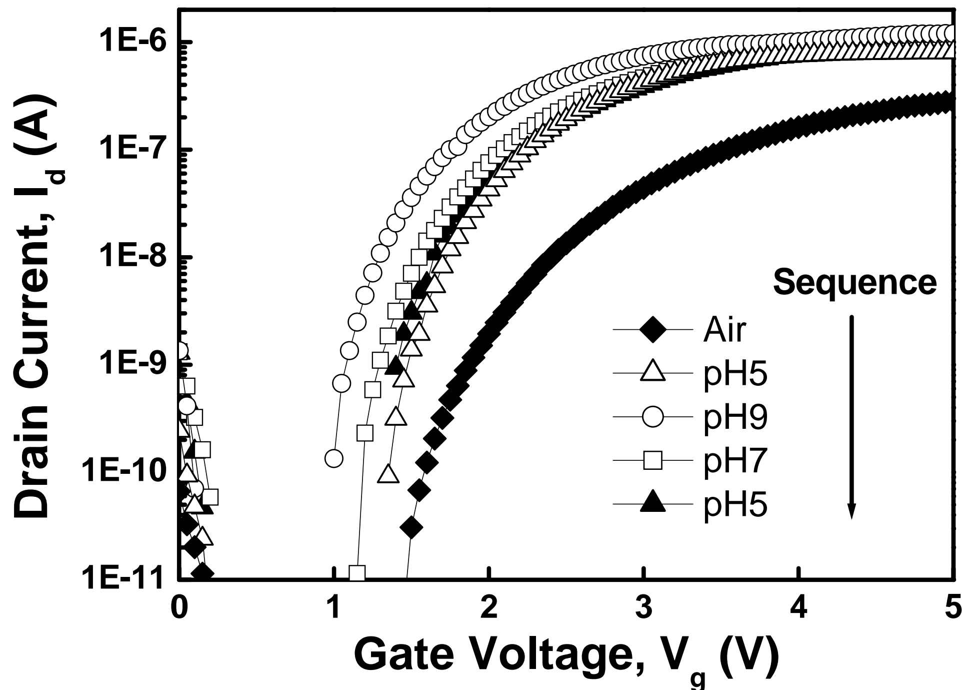


Fig. 3.12 The poly-Si nanowire FET I_d-V_g measurement in aqueous solutions with varied pH concentration. The testing sequence is indicated by the arrow symbol. Each testing is performed after the solution is injected into the channel for 5 min.

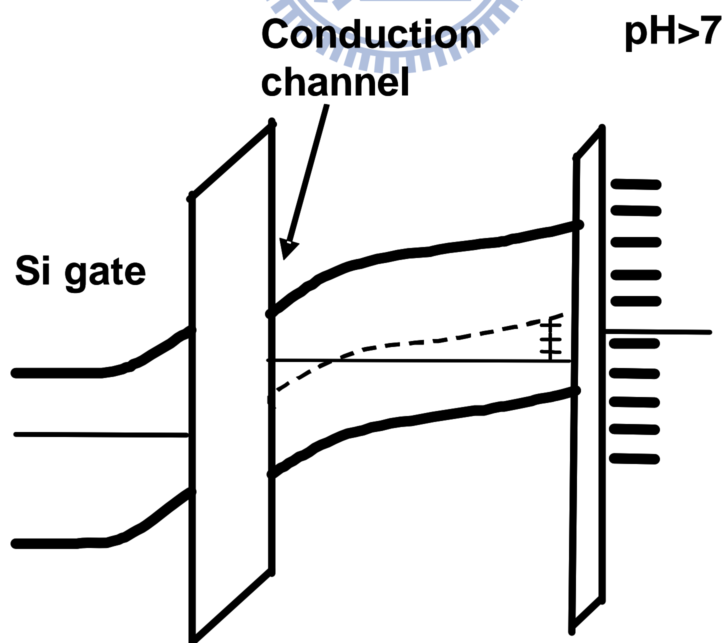


Fig. 3.13 The band diagram of this buried channel NW sensor under channel inversion in the pH>7 solution.

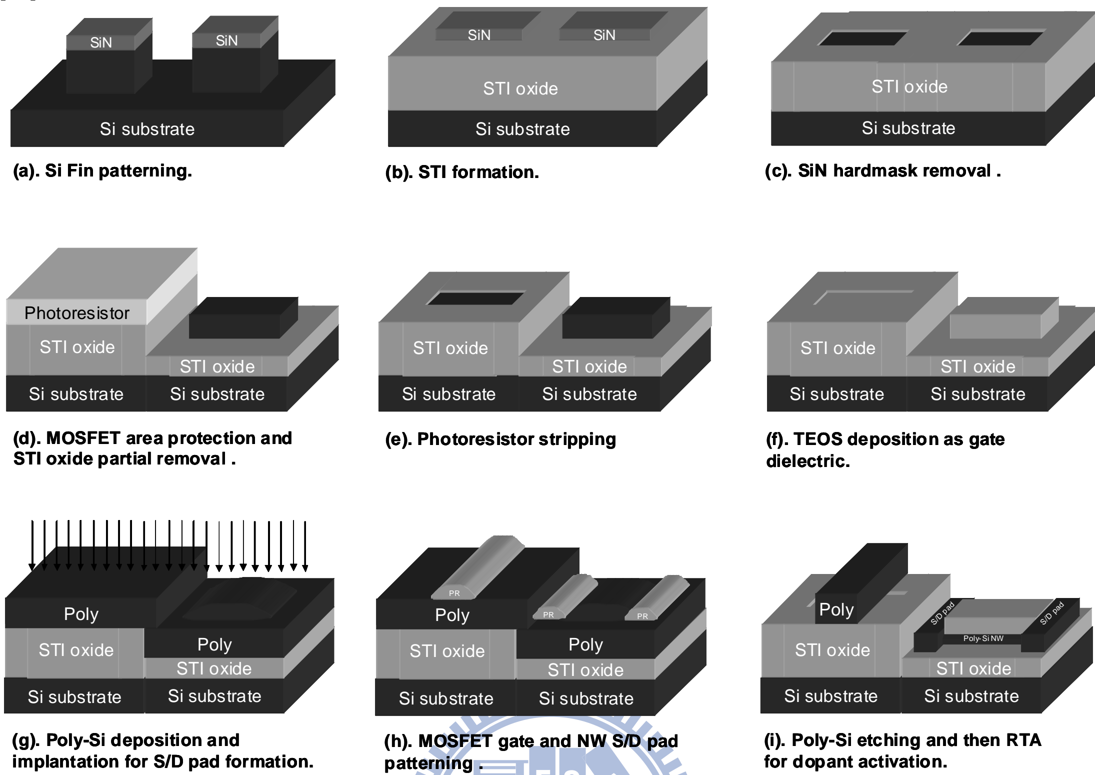


Fig. 3.14 Process flow for the fabrication of self-aligned vertical-channel PSNWs using bulk-Si technology.

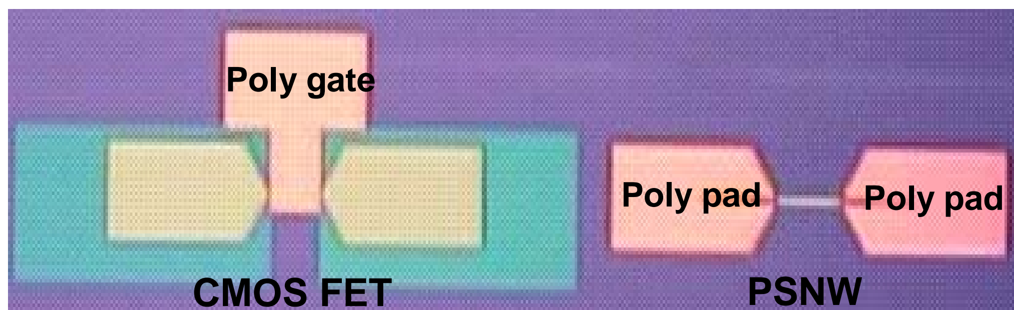


Fig. 3.15 Top-view optical microscope picture of the PSNW and CMOS devices after poly gate etching.

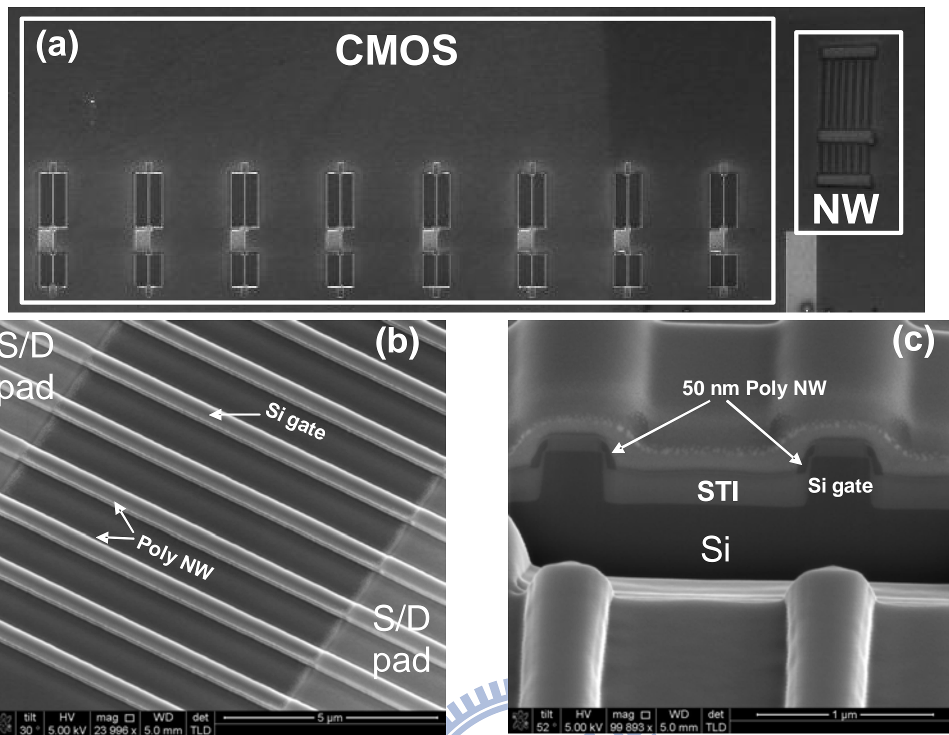


Fig. 3.16 (a) Top-View SEM image of the NW and CMOS homogeneous integration. (b) Tilt-angle SEM image of the poly-Si NW array. (c) Focus ion beam (FIB) image of a self-aligned poly-Si NW with fin-shaped Si gate electrode.

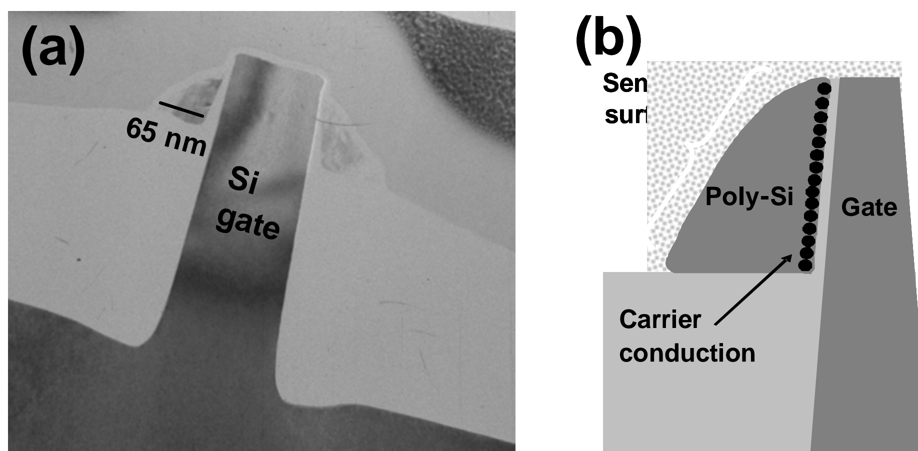


Fig. 3.17 (a) TEM image of a self-aligned poly-Si NW with a fin-shaped Si gate electrode. (b) Schematic illustration of PSNW and its sensing principle.

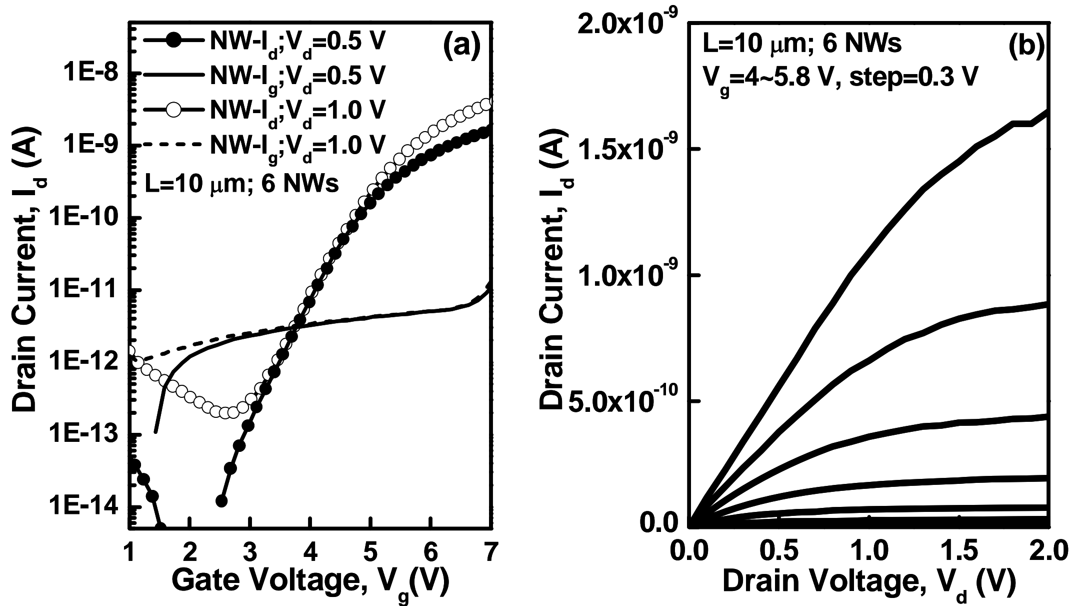


Fig. 3.18 *I-V* characteristics of a fabricated self-aligned PSNW FET device. (a) Sub-threshold I_d-V_g characteristics with gate leakage current. (d) I_d-V_d output characteristics.

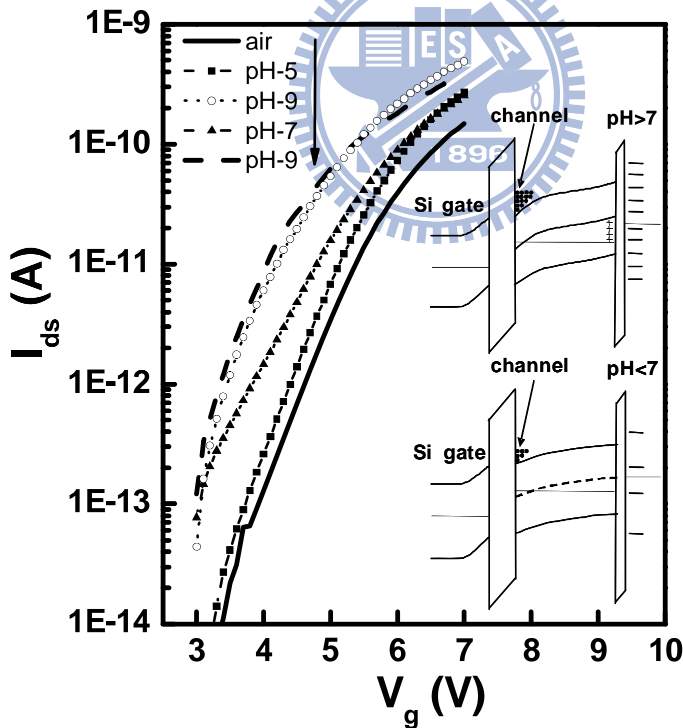


Fig. 3.19 I_d–V_g characteristics of a poly-Si NW FET measured in aqueous solutions having various values of pH. The testing sequence is indicated by the arrow. Each test was performed 5 min after the solution had been injected into the channel. Insets: Band diagrams explaining the changes in the I_d–V_g characteristics upon changing the pH of the solution.

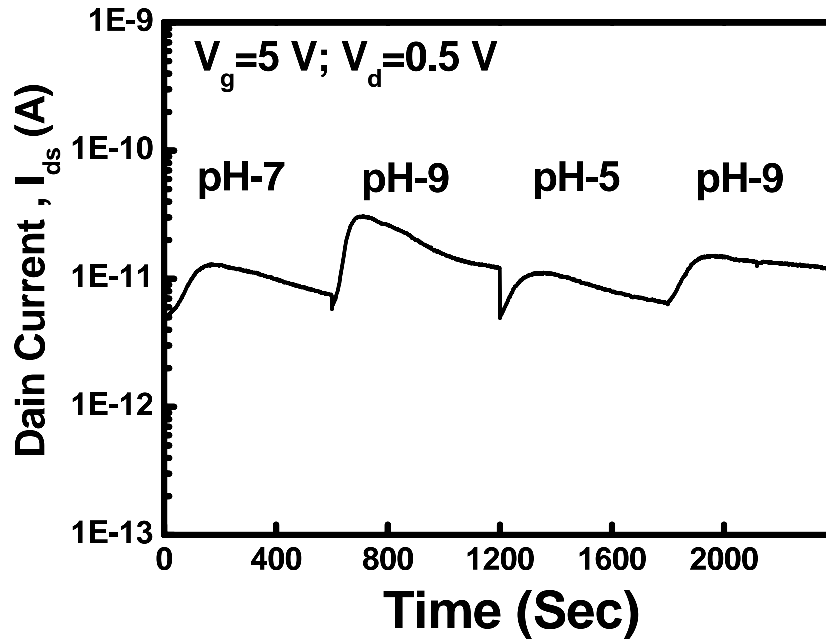


Fig. 3.20 The real-time I_d response of PSNW in aqueous solutions with varied pH concentration.

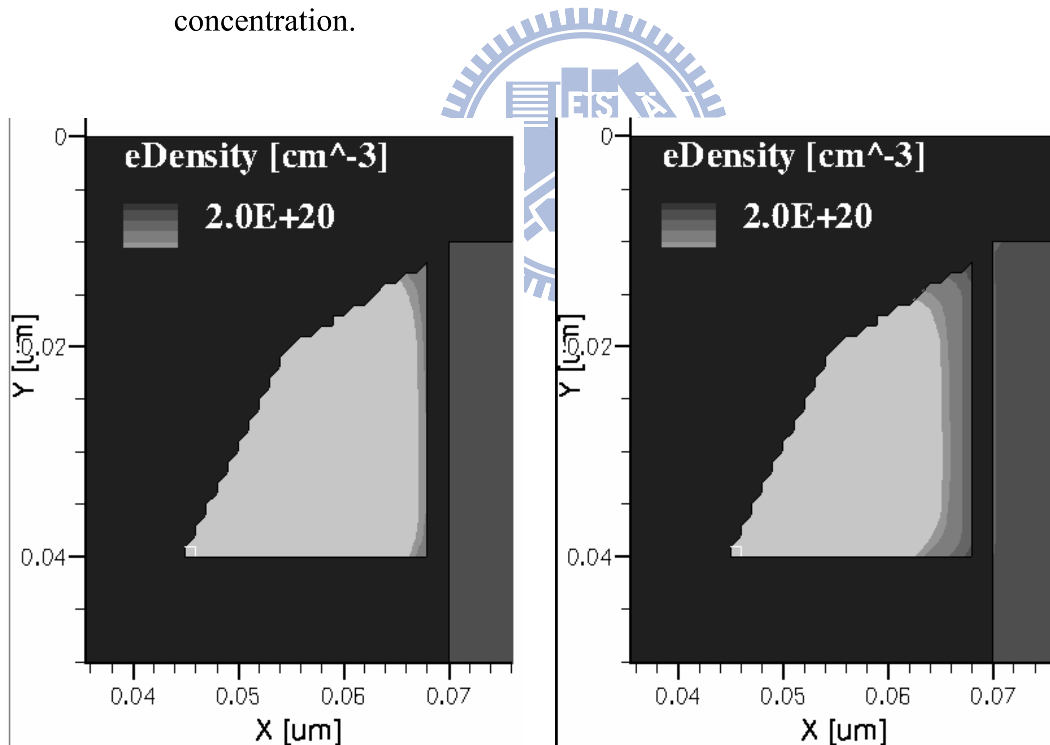


Fig. 3.21 The TCAD simulation of self-aligned trench Poly-Si nanowire FET electron density contour at V_g=0.1 V. (a) No charge at the device surface. (b) The positive fixed charge at the device surface with density up to $1\times10^{10}/cm^2$. The gray region indicates the electron density contour which set the $1\times10^{18}/cm^3$ as start-up concentration.

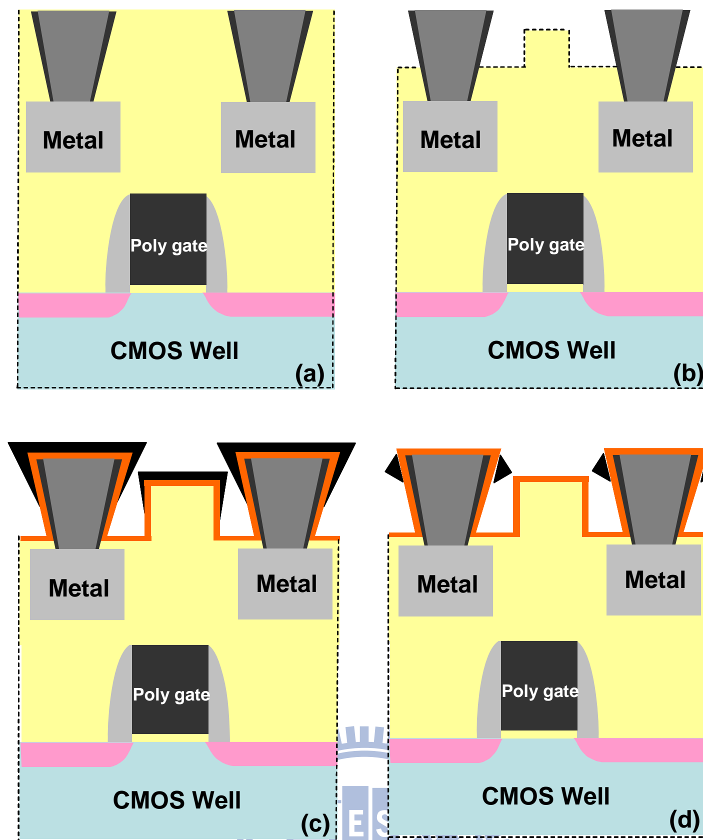


Fig. 3.22 A simplified process flow of BEOL triangle-shape NW. (a) W-CMP. (b) ILD removal. (c) Dielectric/Poly deposition. (d) Poly etch process.

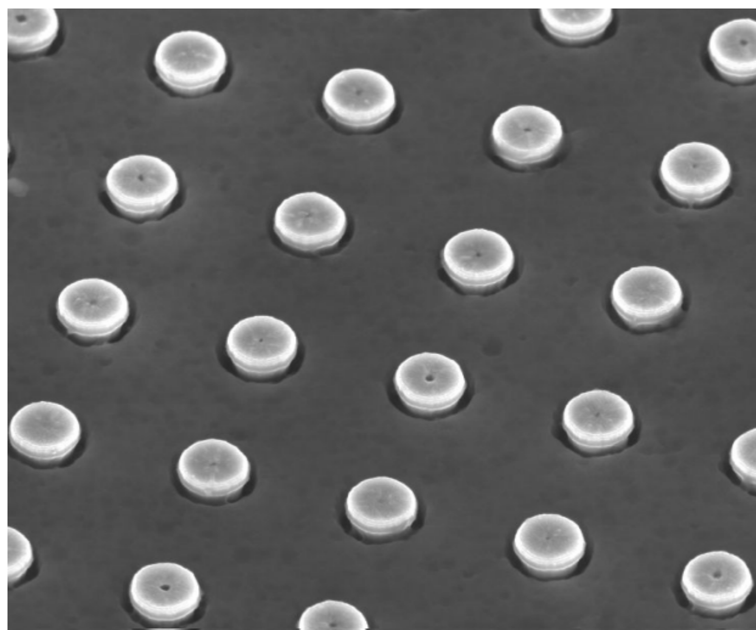


Fig. 3.23 SEM picture of triangle-shape nanowire array.

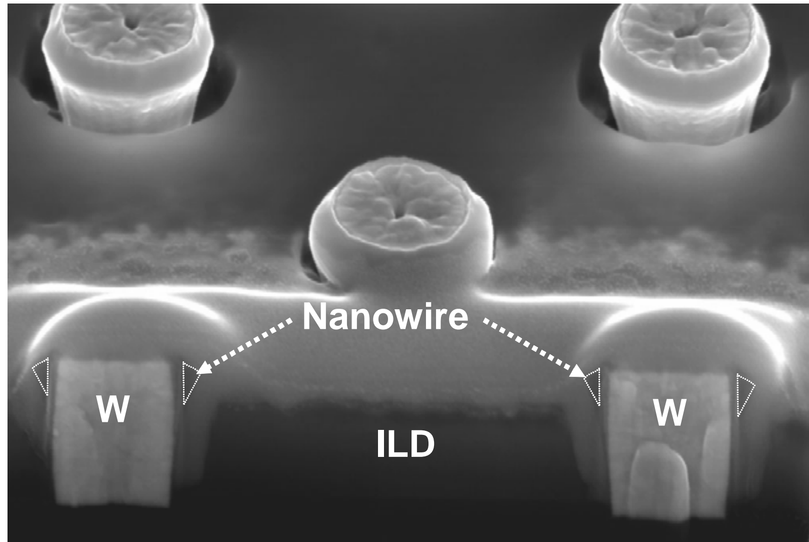


Fig. 3.24 FIB cross-section view of triangle-shape nanowire.

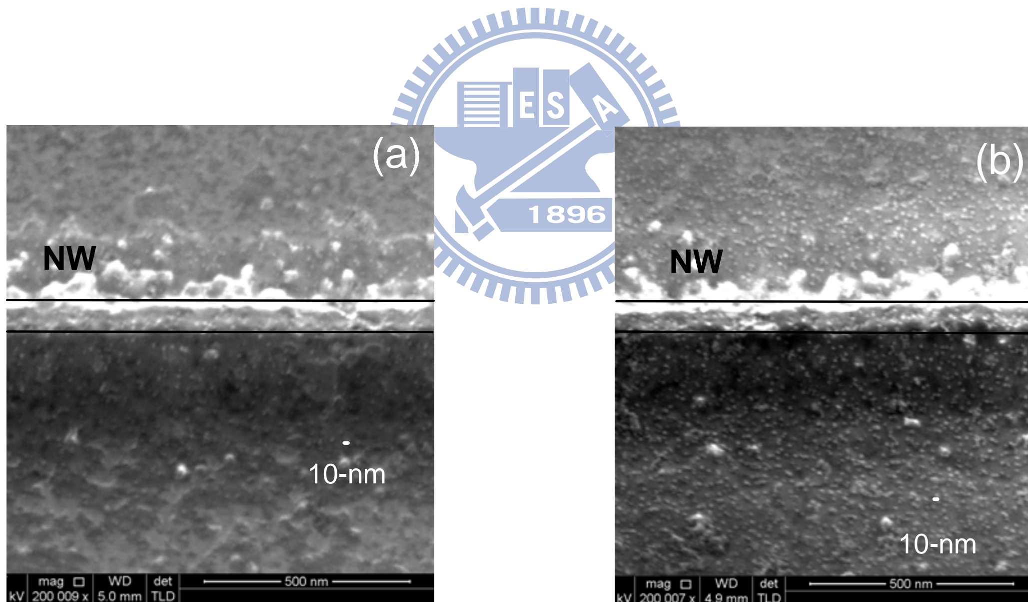


Fig. 3.25 SEM image of the poly-Si nanowires with different ferritin-buffer solution soaking time. (a) The soaking time is 3 hours. (b) The soaking time is 14 hours.

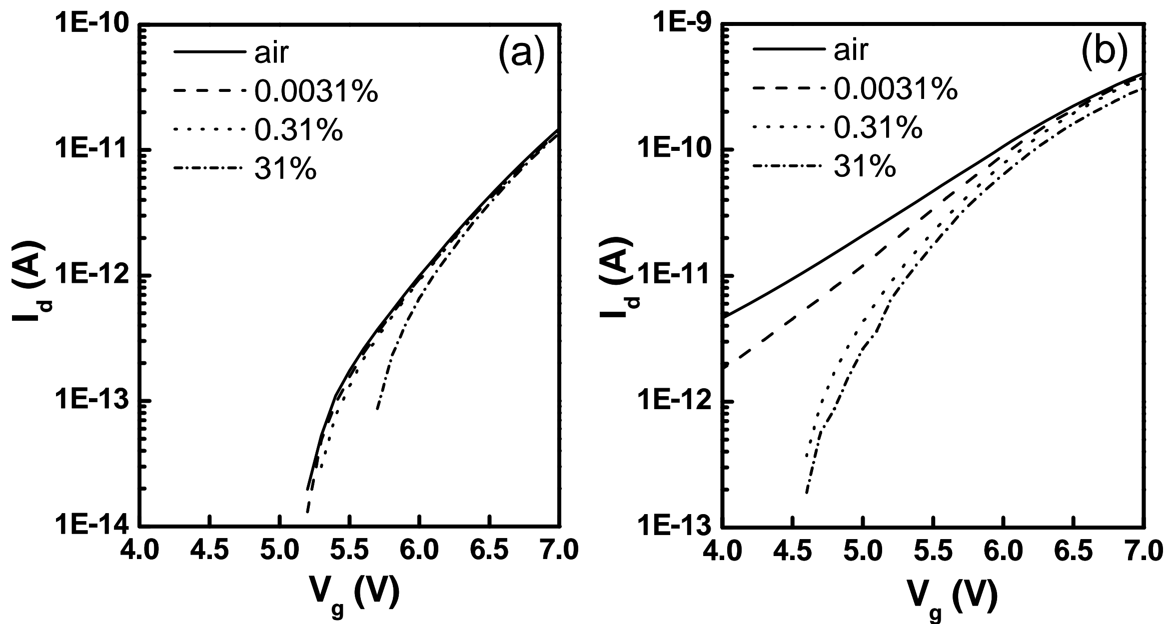


Fig. 3.26 *I–V* response to the different hydrogen peroxide concentration. (a) The sensitivity of 3-hours ferritin soaked device. (a) The sensitivity of 14-hours ferritin soaked device.

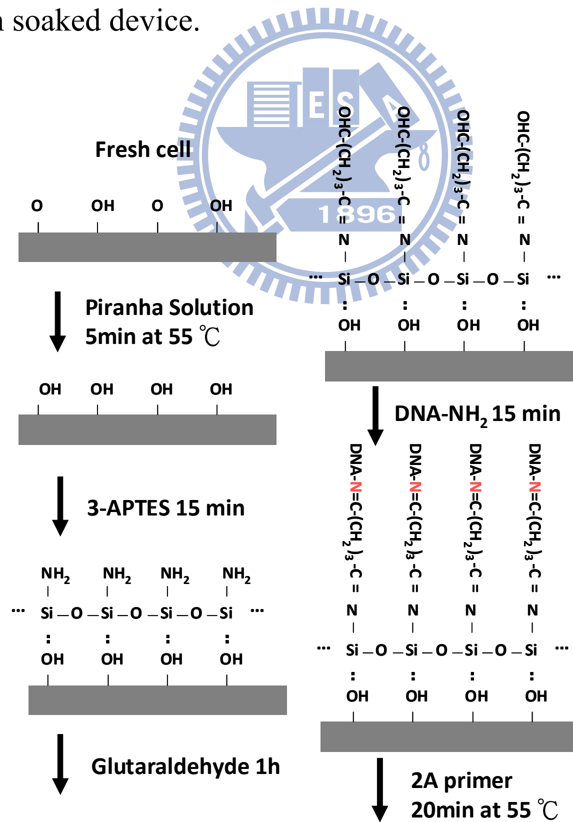


Fig. 3.27 Schematics representation of the NW surface after functionalized treatment steps. (Ref [78] M. C. Chen *et al.*, “A Novel Smart Nanowire Biosensor with Hybrid Sensor/Memory/CMOS Technology,”in *IEDM Tech. Dig.,* 2010, pp. 820-823).

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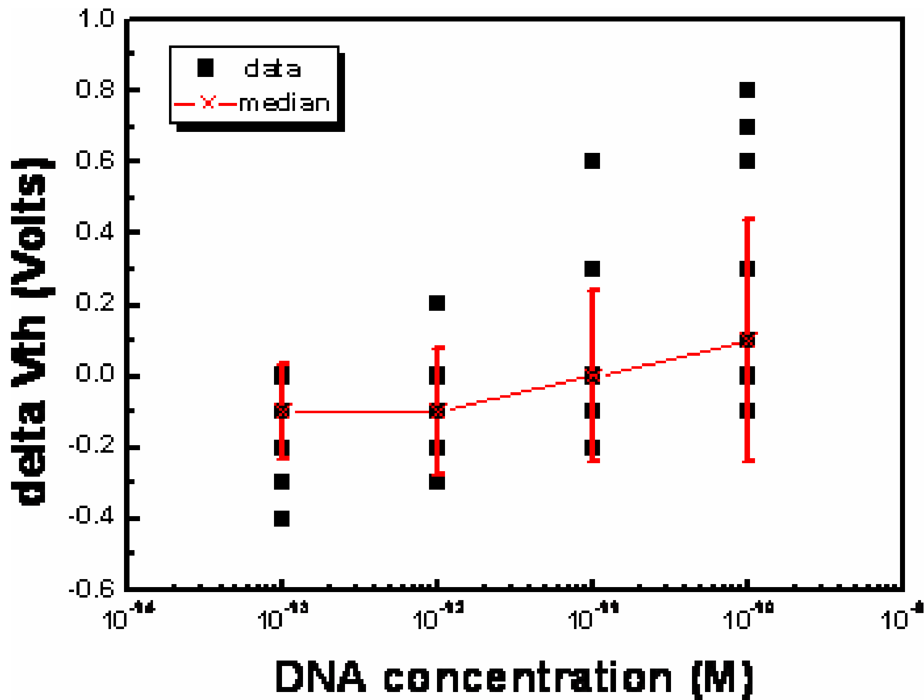


Fig. 3.28 V_{th} shift of the PSNW device at various primer DNA concentrations. (Ref [78] M. C. Chen *et al.*, "A Novel Smart Nanowire Biosensor with Hybrid Sensor/Memory/CMOS Technology,"in *IEDM Tech. Dig.,* 2010, pp. 820-823)

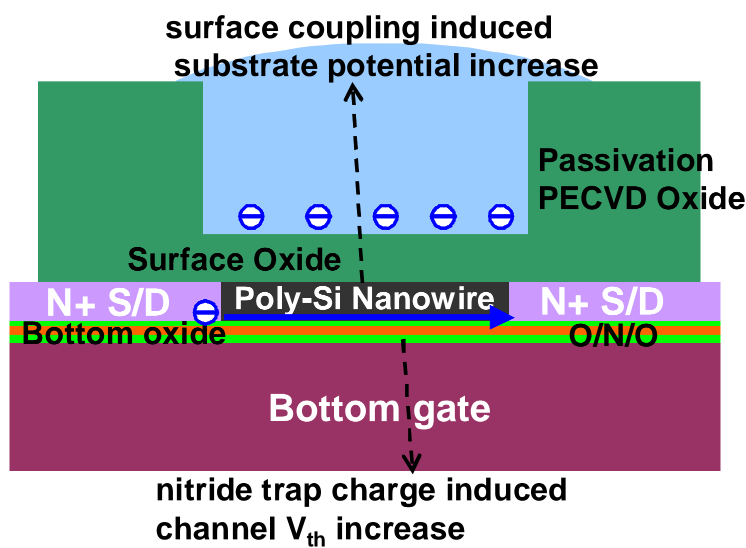


Fig. 3.29 The PSNW bottom dielectric composition for non-volatile memory.

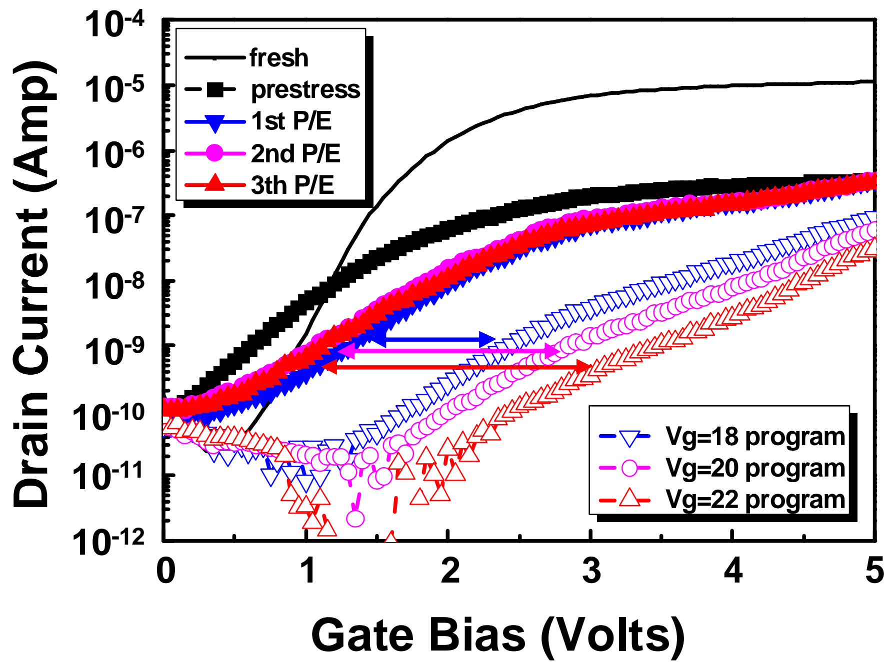


Fig. 3.30 I_d-V_g characteristics of the bottom-gated PSNW with ONO bottom oxide at different operation mode. After the initial pre-stressing, the V_{th} can be adjusted after adequate programming.

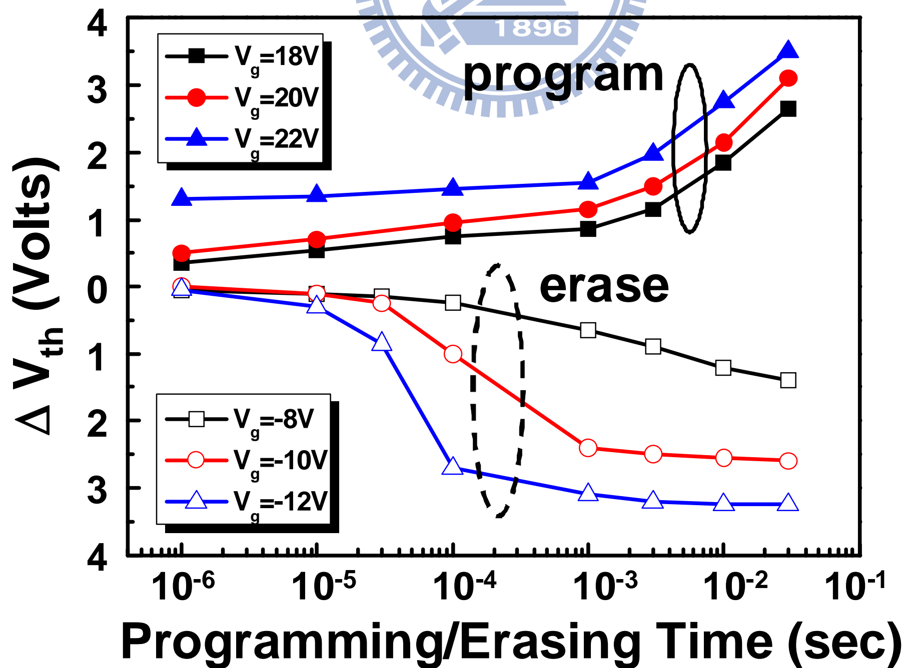


Fig. 3.31 Program and erase efficiency of ONO bottom gate dielectric PSNW. The V_{th} shift can be larger than 3V at the adequate operation bias as the P/E time is around 10 mS.

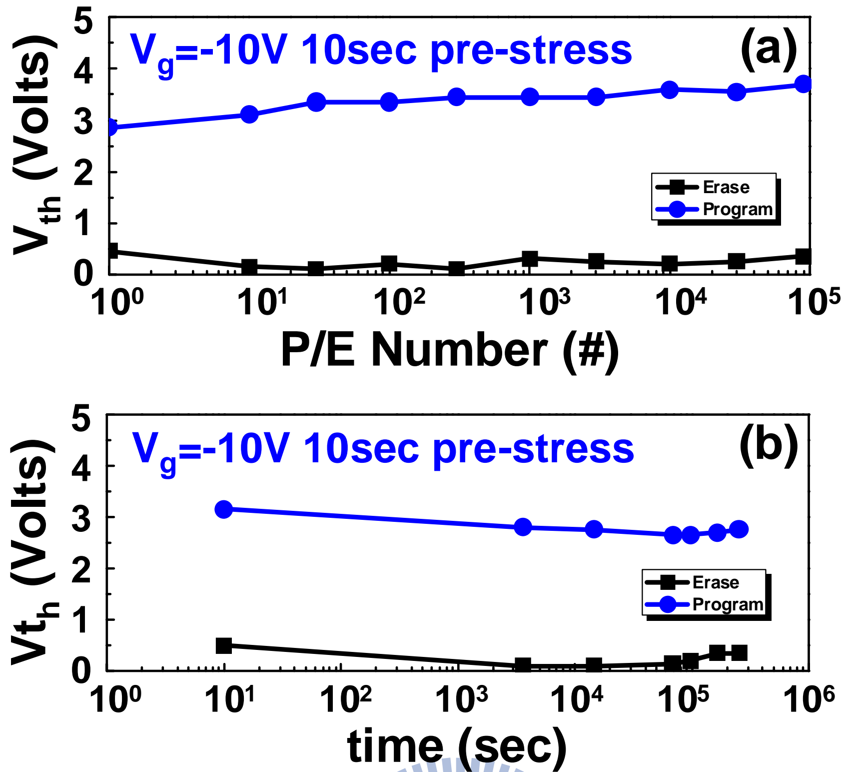


Fig. 3.32 Endurance and retention characteristics of the ONO bottom oxide poly-Si NW FETs device. The P/E window is still larger than 2V after 100K P/E cycle or 3 days long time bake.

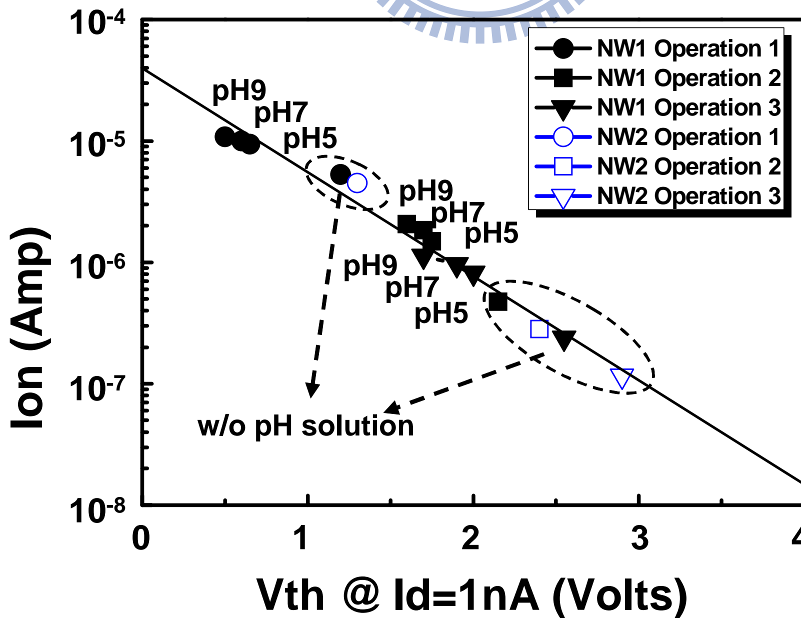


Fig. 3.33 I_{on}-V_{th} distribution of the polysilicon NW FETs device at various program V_{th} region. There is a universal curve of I_{on}-V_{th} transform at different devices or operation condition.

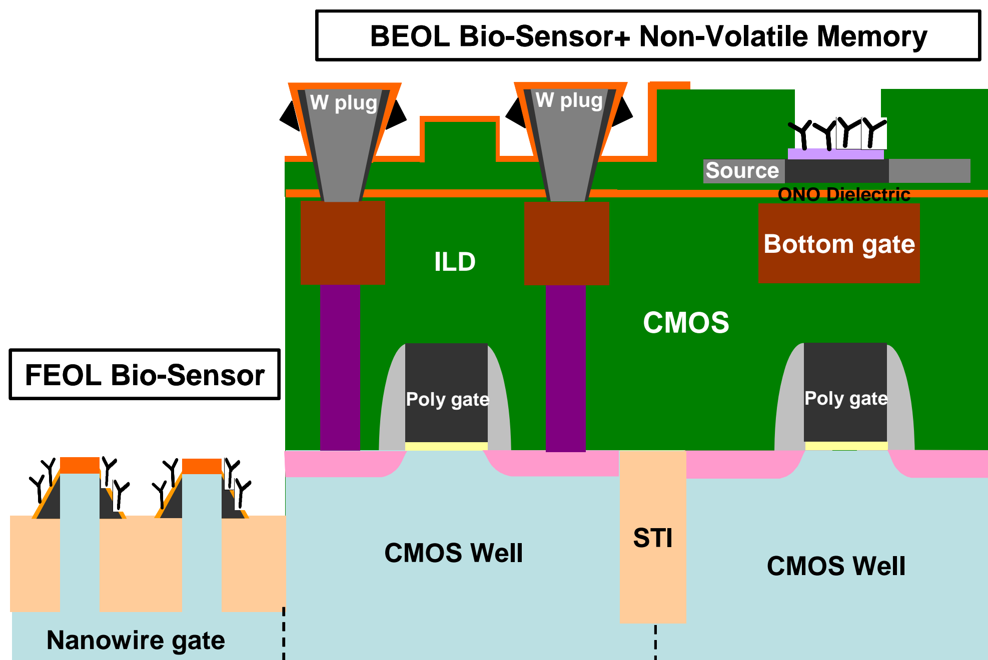
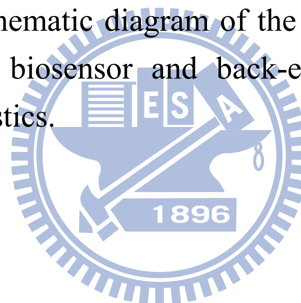


Fig. 3.34 Cross-sectional schematic diagram of the hybrid technology with CMOS devices, front-end biosensor and back-end biosesnsor embedded with memory characteristics.



Chapter 4

Nano-Injection Lithography (NInL) Technology for Sub-16 nm Node Application

4.1 Introduction

Although lithography has been a spectacularly successful enabler for semiconductor development, meeting the resolution requirements for the technology roadmap at 16 nm will be extremely difficult for optical lithography systems [79]-[82]. Based on the ITRS roadmap [79], the half-pitch of key critical layers will be smaller than 22-nm when the technology node is beyond 16-nm node. Among the patterning techniques, EUV is a leading candidate due to its potentially lower cost than extending the conventional 193-nm DUV lithography with the double-patterning approach [79]. In 2009, IMEC demonstrates the first 22-nm node SRAM using the EUV lithography and single patterning in the contact/metal critical layers [83]. In this pioneering work, the contact minimum pitch is 90 nm with 2~3 nm 3-sigma line-width roughness, enabling the formation of dense array pattern without optical proximity correction (OPC) or resolution enhancement techniques (RET). Furthermore, Veloso et al. reports a record-high resolution 11-nm half pitch by using the EUV interference lithography [84]. However, EUV mask fabrication is still a challenge [82] and mask set price of up to three million US dollars is punitive for test chips and pilot productions in the 16-nm era. E-beam lithography, a maskless

process, is an attractive lithography alternative—at least in the initial circuit-verification stage. Our experimental data have shown however, that e-beam lithography suffers from line-width roughness (LWR) and proximity effect when preparing high-density patterns. These problems arise from electron scattering in the photoresist as shown in Fig. 4.1. The unwanted secondary electron scattering results in the loss of resolution (See Fig. 4.2). Although 10-nm half-pitch can be resolved [85], the high aspect ratio of the electron resist structures cause the resist lines to collapse and the photoresist line-edge roughness is not satisfactory for device fabrication.

In this report, we presented a novel maskless and electron photoresist-free technology, which we named "Nano-Injection Lithography" (NInL), and employed it to fabricate the first reported 16 nm finely patterned static random access memory (SRAM) devices. Indeed, using this NInL technique allows the rapid fabrication of nanometer-scaled devices with high pattern densities and low line-width roughness (LWR) and minimal entry costs—ideal for preliminary evaluation of the performance of ultra-scaled devices. NInL deposits a pattern-transfer hard mask or metal interconnect and dielectric patterns on the substrate surface directly depending on the precursor gas through electron beam–assisted chemical reactions. In the past, electron beam–assisted chemical reactions have been used to define nanometer-scale periodic lines or dots structure [86-87], but not to fabricate metal–oxide–semiconductor field-effect transistors (MOSFETs). Here, we reported the fabrication of a 6T-SRAM cell having an area of 0.039 μm^2 [88], which is 43 % the size of the smallest SRAM previously reported [22]. SRAM device designs and SRAM cell circuit operations are also important for realizing such a small SRAM cell device. We used straight patterns for the active areas and gates of the SRAM cell to minimize stochastic device mismatch. This SRAM device featured a nanowire

FinFET channel to provide the best short-channel-effect and a single TiN gate for simple process integration. As the cell size decreases, using a high-beta-ratio SRAM cell design to obtain a sufficient static noise margin becomes difficult because of increasing variations in device characteristics [89]. In this study, we used the dynamic V_{dd} regulator approach (DVR) [90] to increase the signal-to-noise margin of the tiny SRAM cell.

4.2 Lithography Alternatives Surveys for Sub-22nm Half-Pitch

To achieve demand of highly integrated, smaller dimension devices with more economical die cost, several next generation lithography techniques are employed for high resolution and small pitch patterning development. Base on the ITRS roadmap [79], the half-pitch of key critical layer will be smaller than 22-nm when the technology node is beyond 16-nm node. Among the different techniques, the EUV is the leading candidate due to its potentially lower cost than the extending of 193-nm DUV lithography with double-patterning approach. In 2009, IMEC demonstrate the first 22-nm node SRAM using the EUV lithography and single patterning in the contact/metal critical layers [83]. In this paper, the contact minimum pitch is 90 nm with 2~3 nm 3-sigma line edge roughness, enable the formation of dense array pattern without requiring OPC/RET. In 2009, the scientists in Paul Scherrer Institut report a record-high resolution 11-nm half pitch by using the EUV interference lithography [84]. The technique uses a coherent beam light source generated from a third-generation synchrotron facility and the light is diffracted at a grating mask and creates interference patterns to be recorded on a substrate coated with photoresist. The technique suffers from the same hurdles as EUV and even the pattern alignment will be the concern for multilayer process.

Regarding to the maskless lithography, the sub-10 nm half-pitch resolution had been demonstrated by H. Duan et. al. using the e-beam Lithography [85]. Although the 10-nm half-pitch can be clearly resolved, the high aspect ratio of the structures cause feature collapse and the photoresist line-edge roughness is not gracious for device fabrication. Furthermore, there are some potential bottom-up approach had disclosed its feasibility for dense feature patterning [91]. However, the large scale fabrication had not been reported yet. Figure 4.3 shows the recent sub-32nm SRAM demonstration with various lithography techniques and the ITRS roadmap. Although the e-beam lithography has demonstrated the excellent scalability, however, the worse LER of photoresist are still under development. Electron beam–assisted chemical reactions have been used previously to define nanometer-scale structures having pitches of their periodic gratings as low as 5.1 nm [86] or periodic nanodots array with 3 nm feature size [87]. A field-effect transistor and inverter fabrication flow featuring the direct-write Electron/Ion beam–assisted chemical reactions as gate/drain/source electrode for ZnO nanowire was revealed [92], but not to the fabrication of metal–oxide–semiconductor field-effect transistors (MOSFETs).

4.3 Principle of Nano-Injection Lithography (NInL)

The technology of Nano-Injection Lithography was developed through using Electron/Ion dual-beam system. Figure 4.4 shows the schematic illustration of this dual-beam system. This system uses electron beam energy to initiate and localize chemical vapor deposition in the specific location by a direct-writing technique. Figure 4.5 shows the focus electrom-beam induced deposition processing. The gas nozzle of system can inject variety of organometallic precursor gases depend on the requirement on the target surface in a vacuum chamber. The injected molecule will

adsorb, diffuse or desorbs at the substrate surface and are dissociated by the impact of energetic electron. The energetic electron decomposes the organometallic molecules adsorbed on the substrate which leads to the release of nonvolatile product such as metal atoms to deposit coaxially into the beam. Meanwhile, the remaining species resulting from the decomposition reaction are generally volatile and be eventually removed from the vacuum chamber by the pumping apparatus [96]. A gas nozzle is usually controlled at a height of 0.1 to 1 mm above the target surface with an angle and the precursor gas is evaporated from a heated container. The fine pattern-transferred hark mask material can be deposited onto the substrate precisely through e-beam scanning when accompanied by injection of an ($(CH_3)_3CH_3C_5H_4Pt$) metallorganic precursor gas with a typical pressure in the range of 3×10^{-6} Torr. To obtain a smaller dimension of deposited material, the 5-keV, 4.6-nm-diameter electron beam was usually chosen as the beam source rather than the ion-beam to incite gas phase reactions in the presence of a precursor gas ambient to form the fine pattern, replacing the function of the photoresist for subsequent etching. Due to the lower energy of electron beam, the deposited layer will have high carbon contain which atomic percentage is close to the 75% of the deposited material [93]. It indicates that the material characteristic of this deposited hard mask material could be similar to the photoresist hence the same chemical materials and equipments of photoresist stripping on CMOS process can be applied. The thickness of the hard mask is depended on the dwell times and the posses setting for the direct-writing process. Figure 4.6 shows the deposited Pt had mask with an aspect ratio by 2.5 of a 25-nm line patterning, which is satisfactory for high selective etching process. By loading the layout design into the control computer of system, the holder stage can move rapidly and precisely to transfer the required layout pattern onto the substrate (See Fig. 4.7). Figure 4.8 demonstrated the different line/space pitch patterning by using this nano-injection

lithography. Because the hard mask is deposited onto the substrate, the concerns of photoresist exposure or development are alleviated and 20-nm line/spacing pitch can be obtained with superior line edge roughness and also aspect ratio for subsequently etching process.

In the conventional optical lithography, to compensate the image errors due to diffraction or process effects, the optical proximity correction (OPC) is technique commonly used to maintain the edge placement integrity of the original design. Without the OPC for mask or pattern, the projected images appear with irregularities such as line widths that are narrower or wider than designed which may significantly alter the electrical properties of devices. Figure 4.9 (a) shows an example of the SRAM patterning using OPC, to solve the short distance line-end shortening issue as well as to obtain the uniform critical dimension (CD) for each device in the dense pattern, a complicate and costly OPC is needed to correct these errors by moving edges or adding extra polygons to the pattern written on the photomask. This may be driven by pre-computed look-up tables based on width and spacing between features or by using compact models to dynamically simulate the final pattern and thereby drive the movement of edges. On the contrary, by using this NInL, the 30-nm line-end spacing with excellent CD control can be easily achieved without any OPC or resolution enhancement technique (See Fig. 4.9(b)), such as scattering bars insertion. Besides, the electron beam–assisted chemical reaction can be used to deposit dielectric or conductive masking materials, depending on the precursor gas and its application. This method enables the simple devices fabrication with ultimate scaled for advance devices evaluation.

4.4 Fabrication Flow of 16-nm Node Devices using NInL

The most important application of NInL is to deposit finely patterned material as etching hard mask without using the expensive lithography. The high resolution and high aspect ratio platinum lines for a pattern transfer hard mask can be obtained by optimizing the gas flux control, e-beam energy, diameter selection, and dwell time. Because this technique requires no pattern transfer media, such as photoresist, the electron induced scattering or proximity effect induced interference does not severely impact the pattern resolution. As a result, NInL can achieve high-density patterning with a single step process. This technology is attractive for overcoming the limits of conventional lithography techniques in terms of pattern fidelity and critical dimension variation, especially for multiple nanowire fabrication. Nanowire thickness non-uniformity is a potential concern of multiple-gate devices such as FinFETs and Tri-Gate FETs. As Fig. 4.10 shows, when the source to drain distance have to be reduce for increasing device density and decreasing parasitic resistance, the inherent imperfections of optical lithography make the width of the fins may vary from source to drain. This will gives rise to variations of threshold voltage and DIBL of devices when the misalignment of the gate electrode occurs [94]. The device variation will not only affect the device performance but also impact the circuit functionality, such as SRAM and signal amplifier due to degraded device mismatching characteristics. However, by using the NInL, the device width variation is suppressed for the multiple nanowire devices as shown in Fig. 4.11. Even when the source to drain distance shrunk to 70 nm for series resistance reduction and the nanowire pitch decreased to 40 nm for increase of effective width, no oval shape of the hardmask appeared in the opening area. This effectively reduces the nanowire width variation and also increases the nanowire device density compared to the optical lithography patterning approach. Furthermore, the optical proximity correction procedure is no longer necessary and the process cost is significantly reduced.

For devices fabrication, this study used a (100) surface and 30 nm silicon thickness p-type SOI wafers as substrates. Prior to the active area definition, wafers were chemically cleaned in HF acid and rinsed with de-ionized water. The wafers were then subjected to NInL for hard mask platinum deposition. Figure 4.12 illustrates the active area patterning process flow. After the NInL hardmask deposition, the wafers were subjected to a TCP9400 etcher for Si etching at a chamber pressure of 8×10^{-3} torr with HBr reaction gas. After the etching process, a hard mask removal process was performed using reactive ion etching with O_2 plasma, followed by wet etchant cleaning using H_2SO_4 and H_2O_2. Thermal oxidation followed by oxide stripping was applied to reduce etching damage and corner rounding. Using this process, it is easy to achieve a high-density and accurate nanowire channel with a 64 nm minimum pitch, as Fig. 4.12 (d) shows. A nearly surrounding gate structure with scaled channel dimensions can prevent the drain side electric field from penetrating the channel without requiring a heavily doped channel. Hence, it is beneficial for device V_t uniformity. After nanowire formation, a 1.6 nm oxy-nitride was grown as the gate dielectric. The TiN metal deposition and then NInL hard mask deposition was performed for gate electrode definition. The result gate patterns of TiN metal nanowires were performed in an anisotropic ion etching system TCP9400 with the 8×10^{-3} torr chamber pressure and $Cl_2/BCl_3/CHF_3$ reaction gas and the TEM result is shown in Fig. 4.13. After the TiN gate etching, a 25 nm oxide layer was deposited using an electron-beam assisted chemical reaction. Due to the TEOS base oxide was deposited at around 50°C, the dopant diffusion can be significantly reduced to improve the device SCE. The SEM and TEM investigation at specific device fabrication stages are shown in Fig. 4.14. Figure 4.15 shows the SIMS profile comparison, the NInL process reduce the dopant diffusion than the conventional furnace process which is beneficial for approaching shorter gate length devices.

Wafers then underwent deep source-drain implantation using arsenic at 7 keV and a dose of 1×10^{15} cm^{-2} for nFET and BF_2 at 7 keV and a dose of 1×10^{15} cm^{-2} for pMOS. The electron-beam assisted chemical reaction of the oxide was used as an implant mask, and the oxide hard mask was stripped using XeF_2 in the NInL system after implantation. A 1000 $^{\circ}$C, 10 sec rapid thermal annealing (RTA) for dopant activation was performed. In this study, conventional silicidation is not applied. Instead, good improvement is made to the device performance and short channel effect (SCE) are obtained by using ultra-shallow junction formation, a novel silicide process and super annealing. By using this NInL, the device fabrication steps can be significantly reduced and there is no expensive apparatus are needed.

4.5 16-nm Node SRAM Fabrication using NInL

Specific SRAM device designs and SRAM cell circuit operations are also important considerations toward realizing this small-cell SRAM device. As the cell size and operating voltage decrease, using a high beta ratio design to achieve sufficient cell stability becomes difficult due to increased variations in the device characteristics. As the cell size and operating voltage decrease, using a high beta ratio design to achieve sufficient cell stability becomes difficult due to increased variations in the device characteristics. The device variations are attributed to the critical dimension (CD) control, LER, and SCE control and intrinsic dopant fluctuation, all contributing to the threshold voltage mismatch between the neighboring cell transistors and degrading SNM [95]. In this work, we used simple straight patterns for the active areas and gates of the SRAM cell to avoid stochastic device mismatch due to geometry effect. For the cell layout design, a symmetrical type of cell, illustrated in Fig. 4.16 with simple straight patterns for the active areas

and gates, was applied to utilize the low LWR advantage of the NInL. To achieve shorter channel devices, nanowire or multiple channel devices are becoming attractive due to their superior short channel effect (SCE) immunity for ultra-scaled devices. A surrounding gate structure with scaled channel dimensions can effectively prevent the drain side electric field from penetrating the channel without having a heavily doped channel. Hence, it is beneficial for device stability control. Figure 4.17(a) shows a top-view SEM image of a NInL patterned SRAM gate array. The 2 nm 3-sigma LWR of the 18 nm gate length patterning was obtained to alleviate the critical dimension variation of the SRAM devices. Figure 4.17(b) shows the top-view SEM image of the SRAM cell after gate etching. Due to the pattern formation without the aiding of the mask and photoresist as optical lithography, neither optical proximity correction (OPC) nor RET (Resolution enhancement technique) were required to expose the 30 nm line-end spacing. Therefore, the conventional double exposure and double etching process were abbreviated and the process cost, complexity and device variability can be significant reduced.

Figure 4.18 (a) shows that the active to gate and to Pt contact overlays are well controlled using a close neighbor cell alignment mark. Figure 4.18 (b) shows an SEM image of local interconnect using NInL Pt deposition. There are no bird's beaks, even with very narrow spacing, when using NInL. Due to the critical dimension restriction of line-width for SRAM metal routing, NInL deposited Pt was employed for the interconnect material, i.e. Pt pattern was deposited with NInL technology as interconnects rather than hard masks. However, as compared to the Ion-beam deposited or conventional platinum, the e-beam deposited material included higher carbon content therefore the sheet resistance was ρ =9.9 ohm-m which was as relatively higher than conventional metal conductor (ρ of intrinsic Si is 640 ohm-m). As compare to the Ion-beam deposited platinum strip with a 10 μm × 5 μm strip with

a 0.1 μm thickness, the resistance of e-beam deposited platinum was 4-fold higher than ion-beam deposited platinum (See Fig. 4.19). The high energy impinge of the atoms may generate the more secondary electron and lead to the higher dissociation rate for the deposited material. The 9.9 ohm-m sheet resistance is several times higher than the conventional metal conductors. To fulfill the resistance requirement for the high performance circuit, a thermal treatment or improved precursor may improve the sheet resistance.

Figure 4.20 shows n/pFET nanowire devices with I_d-V_g characteristics. To obtain an adequate static noise margin (SNM) of the low beta ratio SRAM the device threshold voltages (V_t) were designed to give low V_t for pFET and high V_t for nFET, giving better cell stability by optimizing the RTA thermal budget. In this study, because no silicidation was involved, improvement was expected for the device performance and short channel effect (SCE) by using state-of-the-art device technology such as ultra-shallow junction formation, a novel silicide process and super annealing [22]. In addition, due to the FEB deposited Pt was used as the contact material. The nFET performance was suffered because of its high schottky barrier height of Pt to n^+ Si layer therefore the N/P ratio of the SRAM devices was not the optimal. This higher pFET drive ability will increase the disturbance voltage and degrade the SNM characteristics of SRAM [89]. In general, as the SRAM cell size decreases, using a high beta ratio design to obtain a sufficient static noise margin becomes difficult, due to increased variations in the device characteristics and high disturbance voltage [89]. To accommodate the high disturbance voltage induced low SNM, this study employed a dynamic V_{dd} regulator approach (DVR) for SNM enhancement [90]. In contrast to the 8T-SRAM design for disturbance voltage reduction [89], this DVR approach enhances the SNM by raising the cell voltage during read operations the the schematic is shown in Fig.4.21. During the read

operation, when the bit-line and word-line voltage are raising to high and a cell supply voltage regulator will provide a higher V_{dd} to magnify the charge of SRAM storage node. On the other hand, when the SRAM cell is at stand-by, the cell supply voltage regulator will provide a lower V_{dd} to sufficiently keep the storage information and reduce the standby leakage, remedying the extra active power consumption during data accessing. By using this cell voltage regulator approach, the overall power consumption can be managed and the SNM is enhanced even though the SRAM V_{dd} is necessitous to be reduced. Figure 4.22 shows the simulation results, which clearly illustrates the benefit of DVR on the SNM enlargement. This process requires no cell and process changes, and the cell area is smaller than the 8T-SRAM, which is beneficial for scaled SRAM design. Figure 4.23 shows the experimental results for a 0.039 μm^2 cell SNM with using 1.5 V DVR voltage. We performed the TCAD simulation (Synopsys ISE-TCAD) to compare the experimental result and realize whether there were any device issues to cause the SNM degradation. After calibrating the *I*-*V* characteristics of each devices based on the Fig. 4.23. We used the MEDICI with circuits analysis advanced application modules (AAM) model to characterize the SNM of SRAM devices. Based on the simulation result, even though the disturbance voltage was higher than the experimental result due to the high pFET/nFET current ratio, the voltage transfer characteristic (VTC) of simulated SRAM cell was still superior than the simulation case. It indicated that the SNM can be further improved after process optimization for external resistance of interconnection between pull-up (PU) and pull-down (PD) devices and also the leakage reduction at the pull-down device. Figure 4.24 shows that the DVR provides a better SNM for 6T SRAM cell, especially at lower V_{dd}, which is attractive for 16 nm node UHD-SRAM applications.

4.6 Summary

This study demonstrated a maskless, photo and electron resist-free and one-step patterning technology called Nano-Injection Lithography (NInL) with 16-nm SRAM fabrication. The NInL technique demonstrated a non-optical patterning capability of 40 nm line pitch, less than 2 nm 3-sigma line-width roughness without employing proximity effects correction techniques. NInL technology employed similar exposure dose as high throughput compared to the E-beam lithography using HSQ as resist. NInL is a versatile technology. It can deposit a hard mask for a subsequent etch step. Or it can directly deposit a metal pattern for interconnects or a dielectric pattern. The simplicity and versatility makes NInL a promising technology for early evaluation or low-volume fabrication of 16 nm devices and circuits. By integrating the NInL technique, a single TiN gate material and nanowire FinFET device structure, a record size of 0.039 μm^2 SRAM cell was demonstrated. To accommodate low beta ratio cell design and achieve good SNM, a dynamic V_{dd} regulator was employed to enhance the SNM, especially beneficial for low V_{dd} operation. NInL is a low-cost, lower-throughput option for device and circuit verification at 16-nm node and beyond.

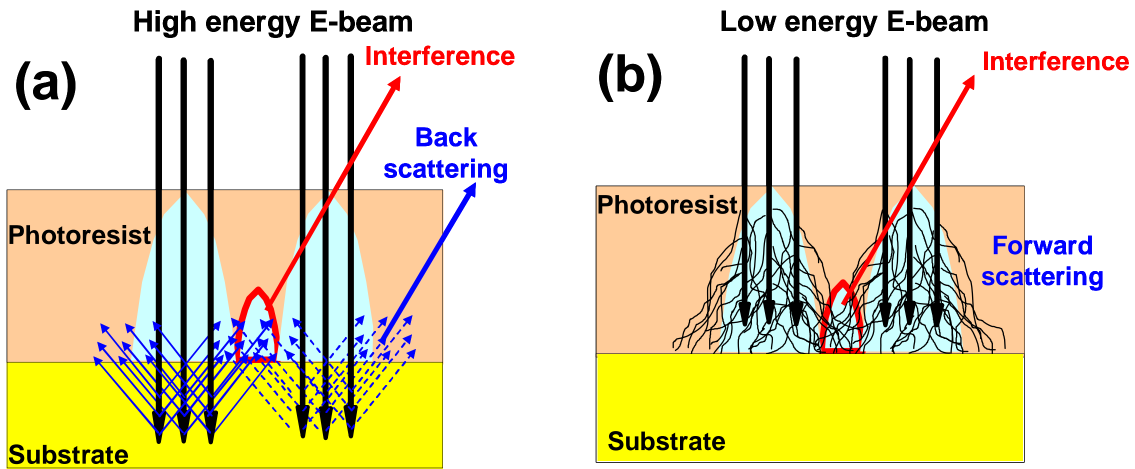
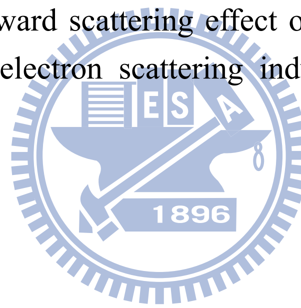


Fig. 4.1 Schematic illustration and SEM top view pictures of e-beam lithography. (a) Illustration of back scattering effect of high energy e-beam. (b) Illustration of forward scattering effect of low energy e-beam. (b) SEM top view of the electron scattering induced interference with e-beam lithography.



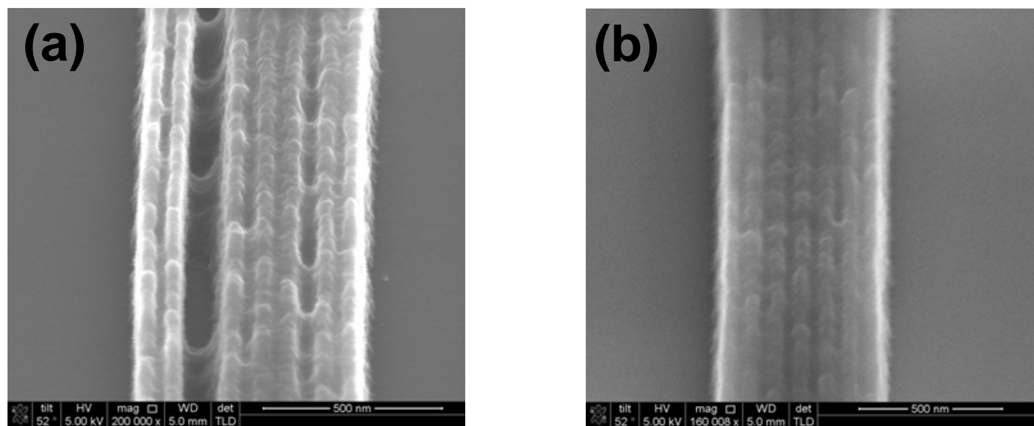


Fig. 4.2 (a) SEM top view of the back scattering effect induced interference of high energy e-beam lithography. (b) SEM top view of forward scattering effect of low energy e-beam lithography.

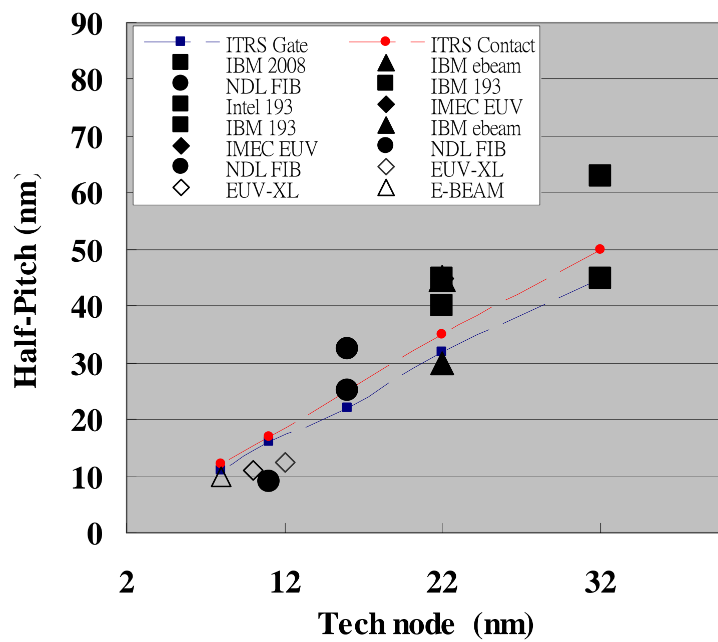


Fig. 4.3 Half-pitch evaluation of recent reports and the ITRS requirement.

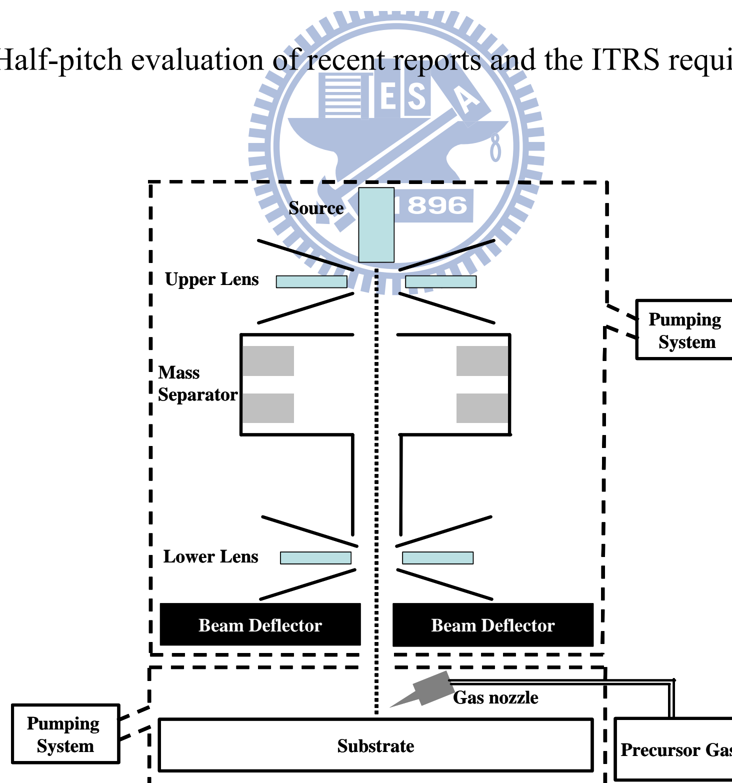


Fig. 4.4 The schematic illustration of dual beam system configuration using for Nano-Injection Lithography (NInL).

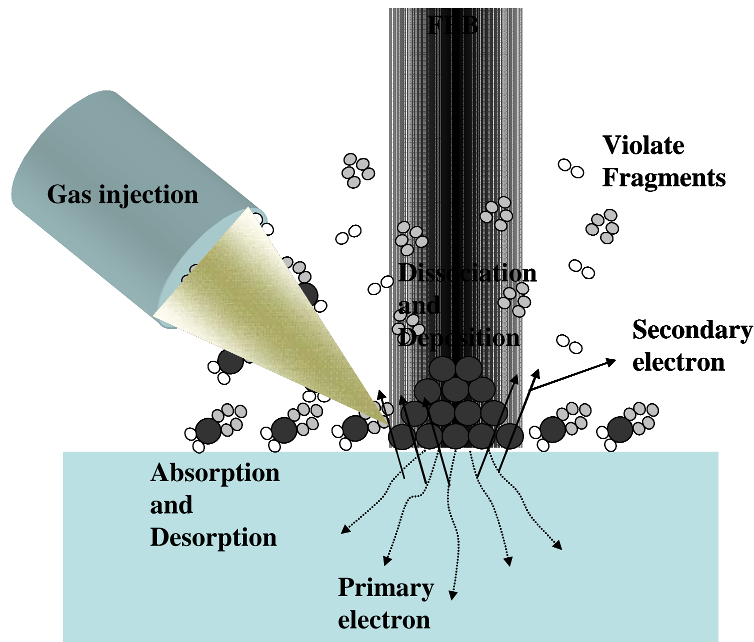


Fig. 4.5 The schematic illustration of focus electron beam (FEB) induced deposition process. (Ref [85] I. Utke *et al.*, "Gas-assisted focused electron beam and ion beam processing and fabrication," *J. Vac. Sci. Technol. (B)*, vol. 26, no. 4, pp.1197–1275, 2008)

Fig. 4.6 The 25 nm etchant hard mask formation using focus-electron beam deposition. The e-beam energy is 5 keV and the beam current is 0.4 nA with using $(CH_3)_3CH_3C_5H_4Pt$ as precursor gas.

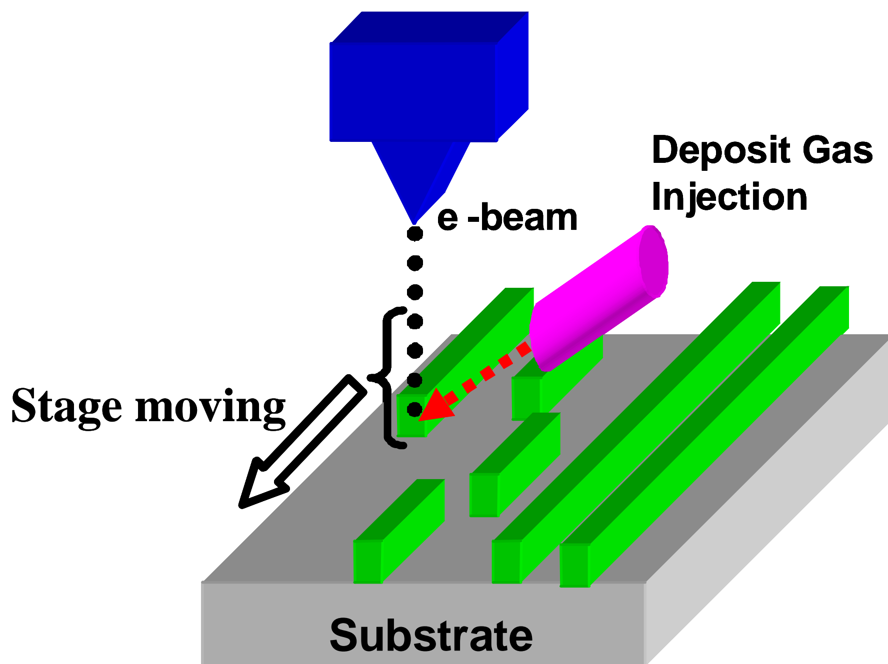


Fig. 4.7 Schematic illustration of NInL pattern generation. The electron-beam assisted chemical reaction to deposit pattern-transferred hard mask on substrate surface directly and the stage control the location for pattern generation.

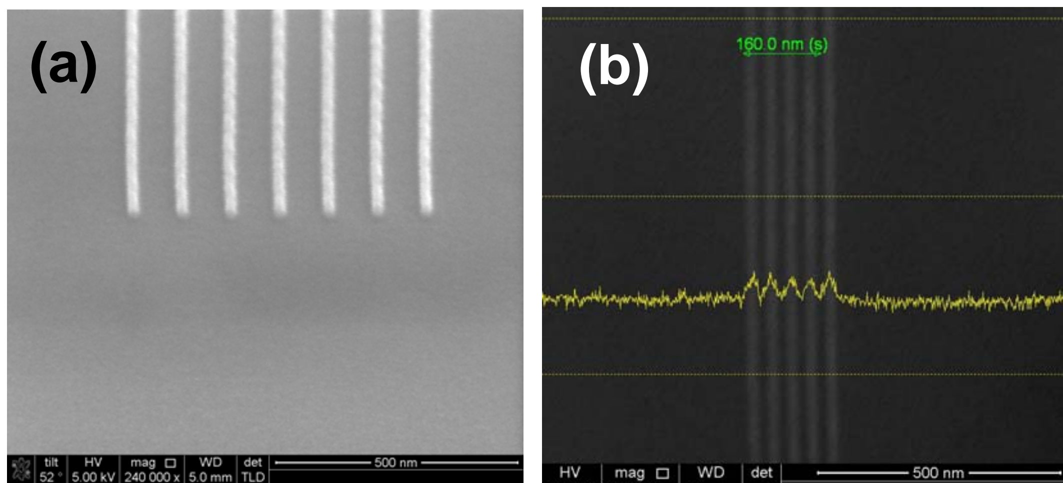


Fig. 4.8. (a) 20 nm Pt line hardmask deposition with 90 nm pitch. (b) 20 nm Pt line hardmask deposition with 40 nm pitch.

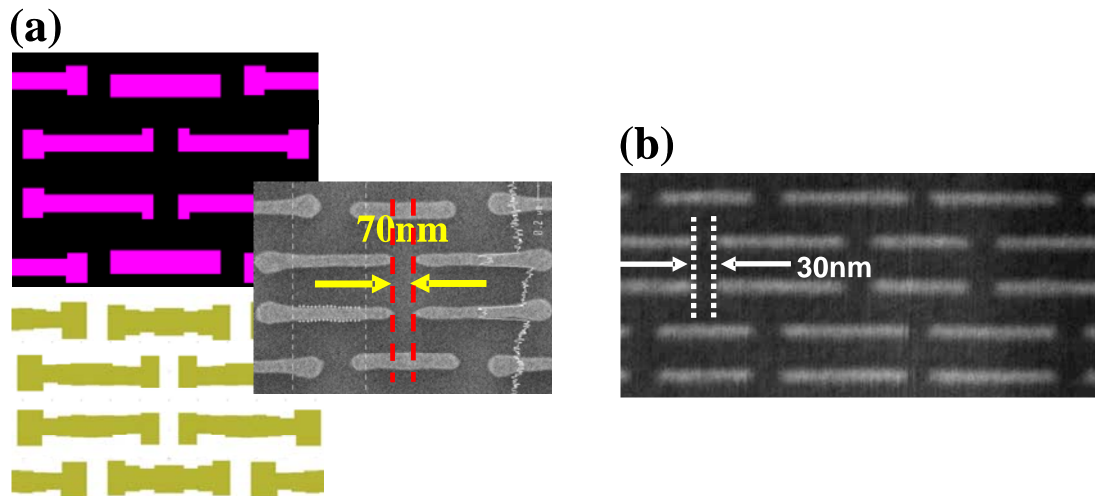


Fig. 4.9. (a) The complicate OPC is commonly used to solve the image errors by optical lithography. (b) The 30-nm line-end spacing is achieved without OPC by using NInL.

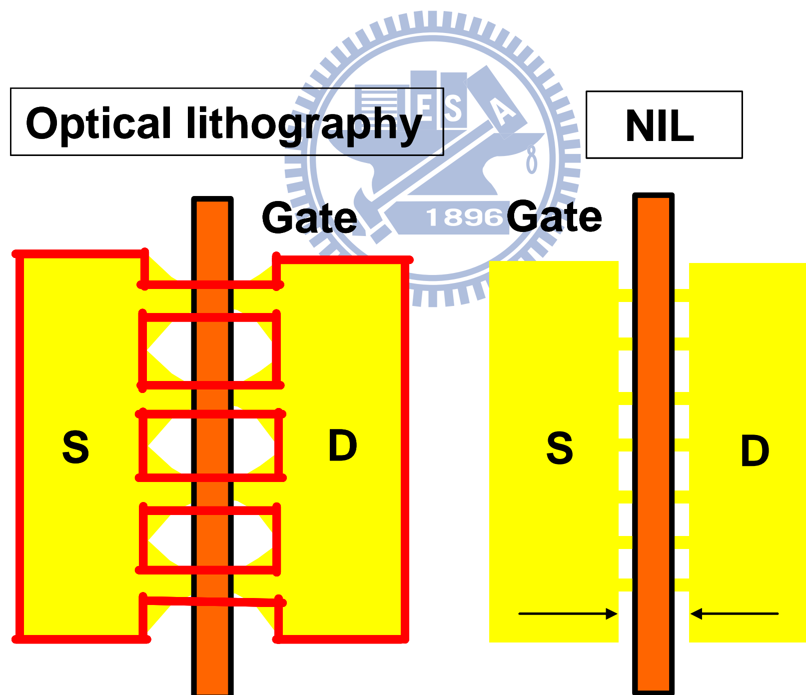


Fig. 4.10. (a) Illustration of significant fin width variation occurs by using optical lithography especially when the S/D distance is reducing. The red line indicates the origin layout shape and the yellow color marks the resulting pattern after lithography. (b) Tighter design rule, less dimension variation are required for nanowire performance enhancement.

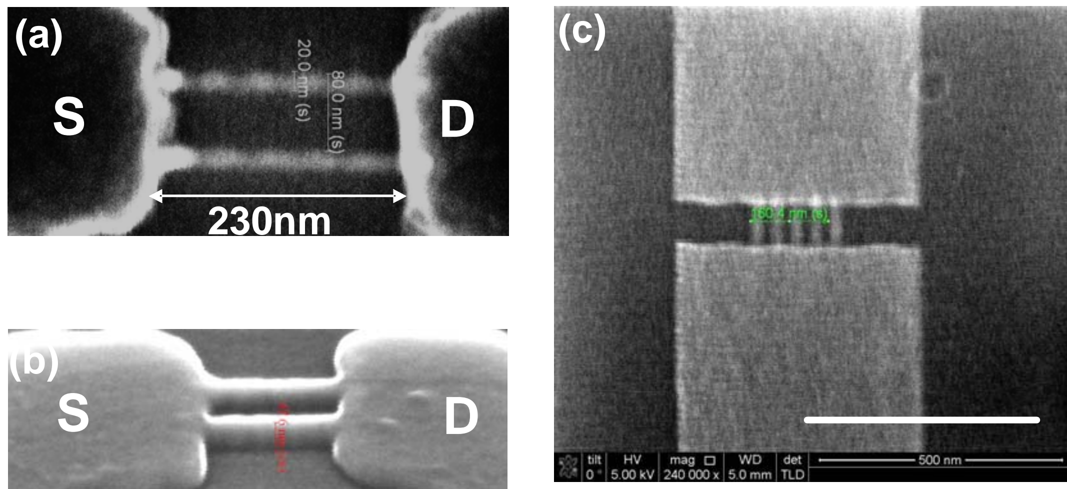


Fig. 4.11. SEM top view of high density nanowire devices. (a) NInL hard mask deposition. (b) After Si pattern etch. The nanowire pitch is 80 nm and source to drain distance is 230 nm. (c) NInL hard mask deposition with 40 nm nanowire pitch where the source to drain distance is 70 nm.

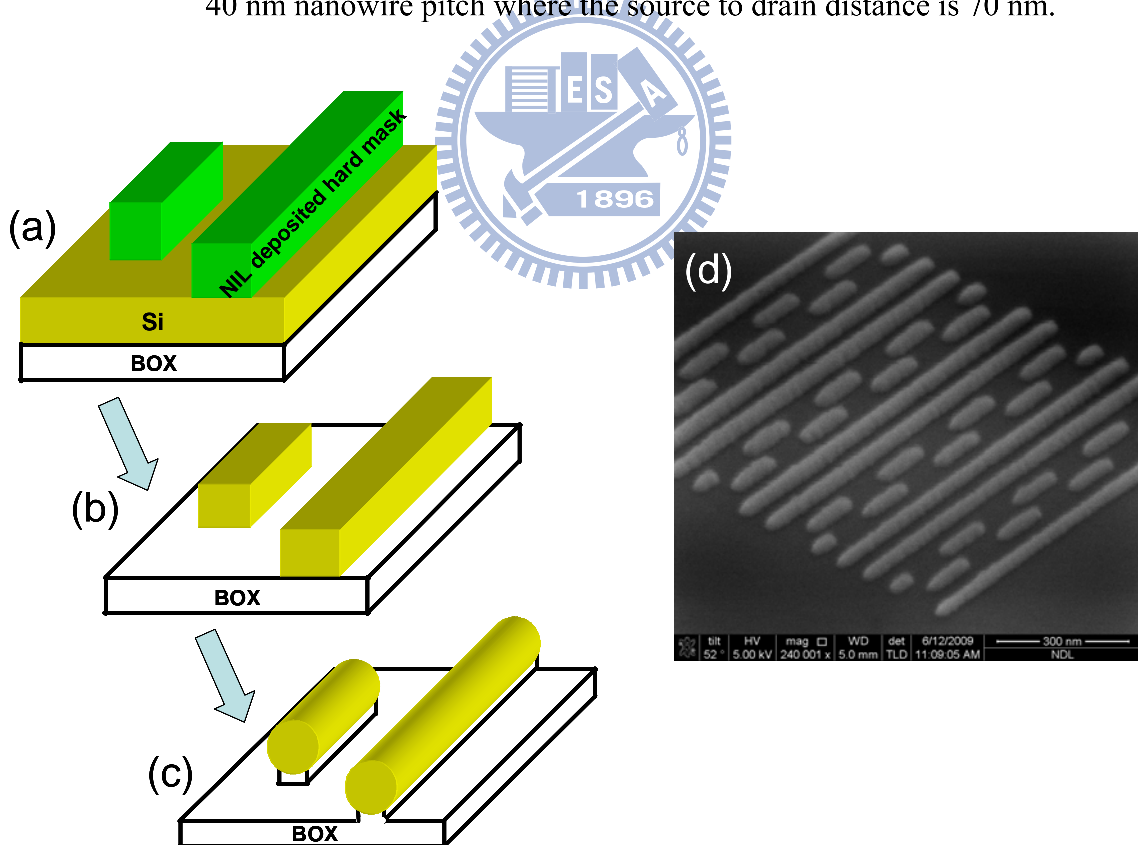


Fig. 4.12. Process flow chart of nanowire formation: (a) NInL hard mask deposition. (b) Si pattern etch. (c) Formation of nanowire channel. (d) Tilt-angle SEM view of Si nanowire array.

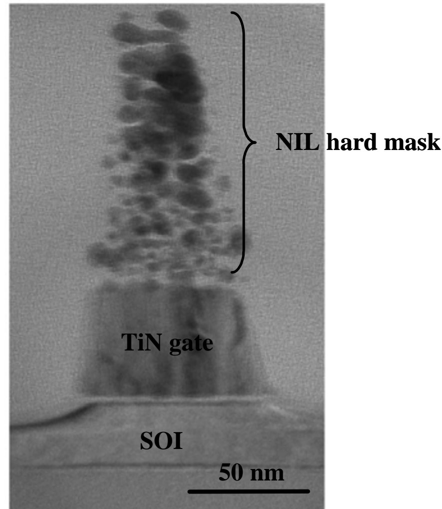


Fig. 4.13. The cross-section TEM image of TiN gate after etching and the NInL deposited hard mask layer. (Ref [93] C. C. Huang *et al*., " Sub-15nm Nanowire FETs and Nanogap Devices Fabricated by Electron Beam Nano Injection Lithography (EBNIL)," in *Europe MRS Conference*, *Spring*, 2010.)

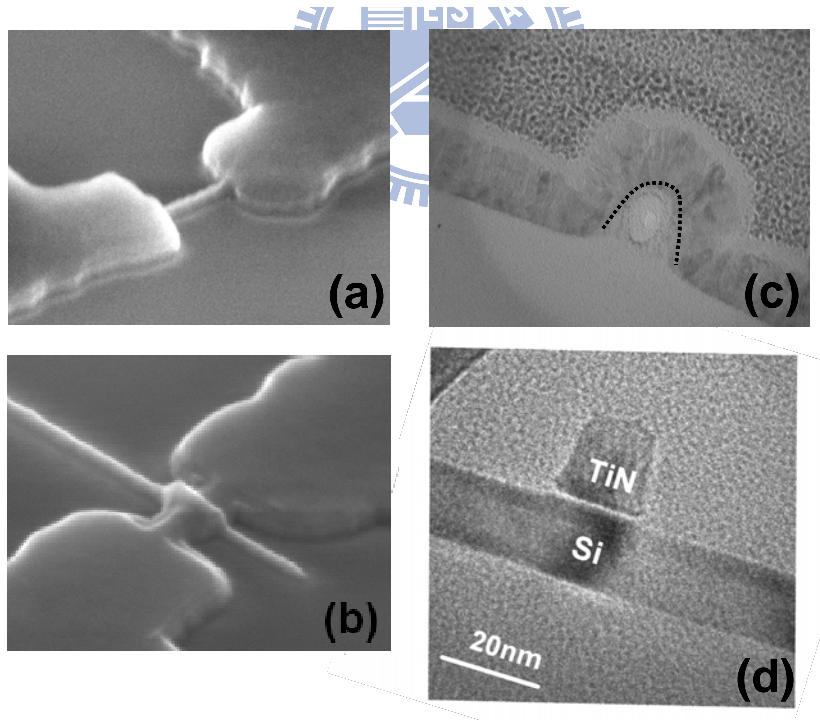


Fig. 4.14 (a) Tilt-angle view of Si nanowire channel formation. (b) Tilt-angle view of Si nanowire after gate patterning and a locally defined spacer deposition. (c)Cross-sectional TEM view showing silicon nanowire covered with omega shape TiN gate. (d) Cross-sectional TEM view of 18 nm TiN gate.

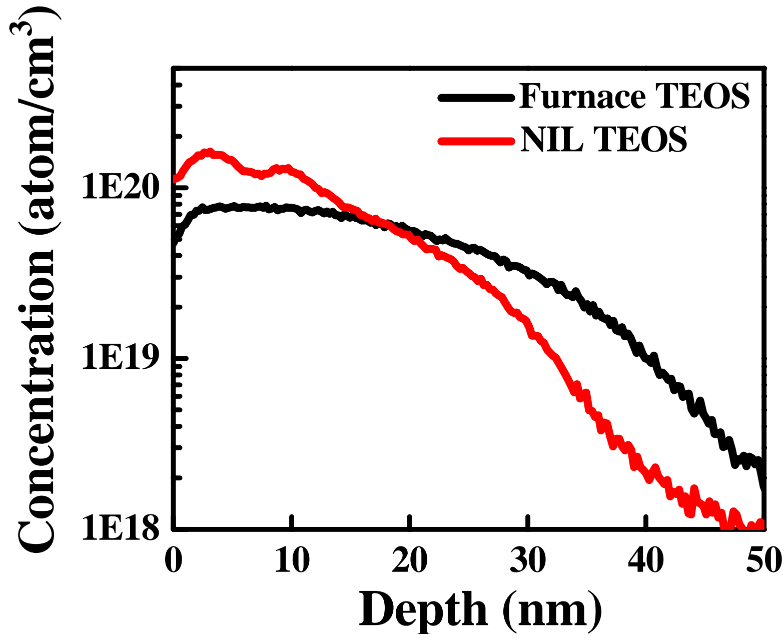


Fig. 4.15 Boron SIMS profile comparison with two different TEOS deposition approach. The boron implant condition is 10 keV with a dose of 1×10^{15} atom/cm^2. The 25-nm furnace TEOS was deposited at 750°C and the NInL TEOS was deposited at around 50°C. The sample are then annealed at 1000 °C,10 sec for dopant activation.

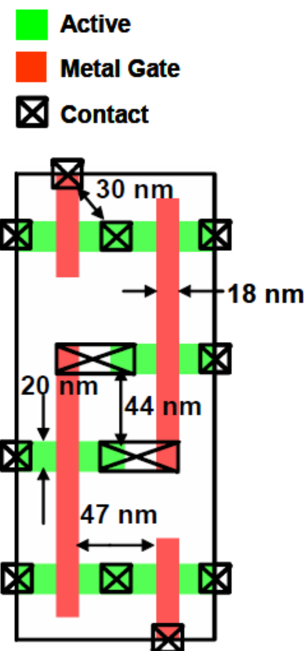


Fig. 4.16 The 0.039 μm^2 6T-SRAM cell layout and key design rule.

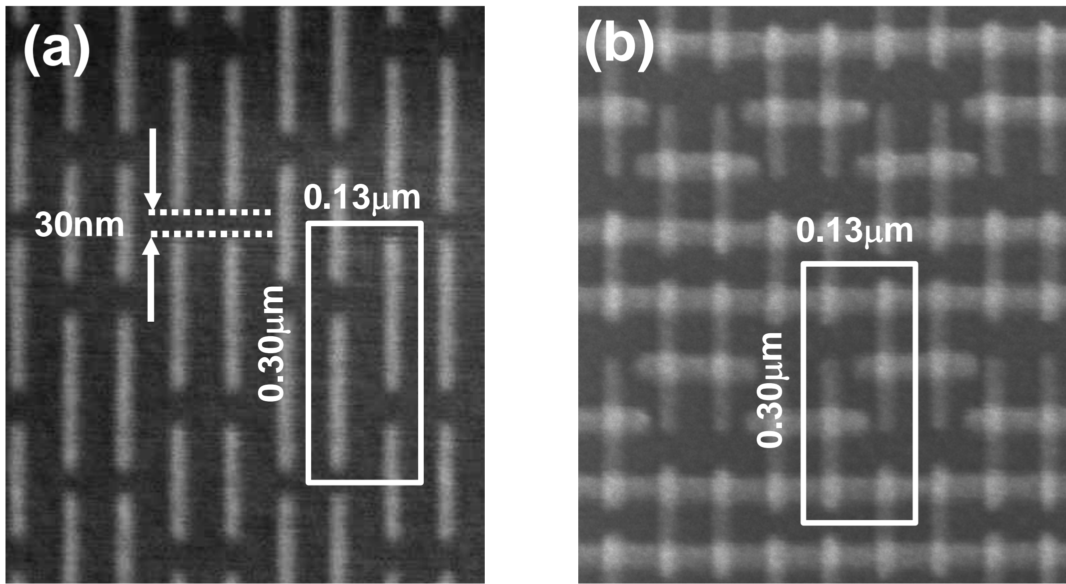


Fig. 4.17 (a) Top-down SEM image of the 6T- SRAM gate hard mask deposition with 30 nm gate-to-gate spacing and 2 nm LWR formed by single NInL patterning. (b) Top-down SEM image of the 6T- SRAM after gate etching.

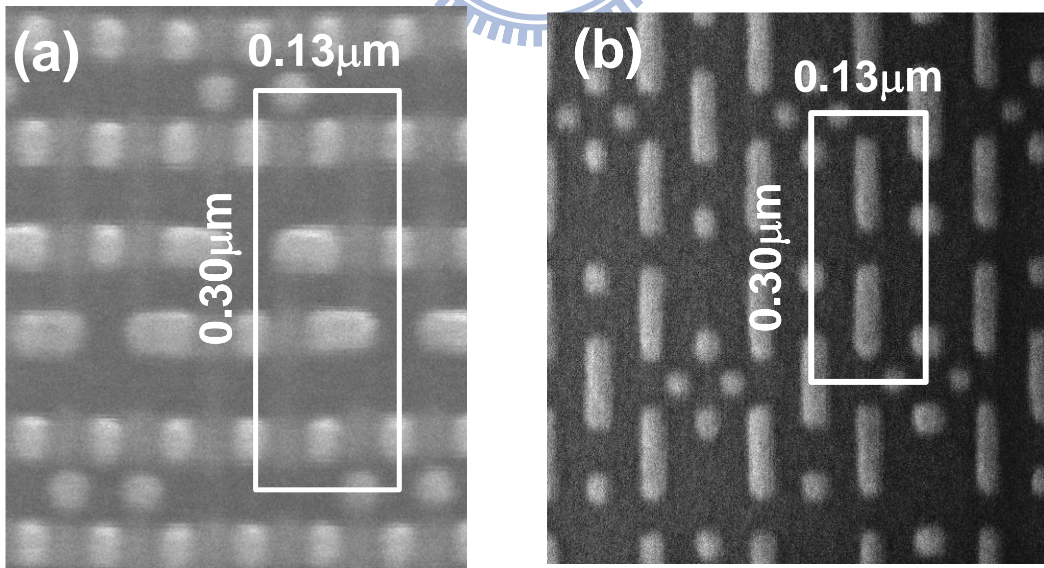


Fig. 4.18 SEM to views of (a) three critical layer superposition showing active region, metal gate and contact and (b) Metal local interconnects.

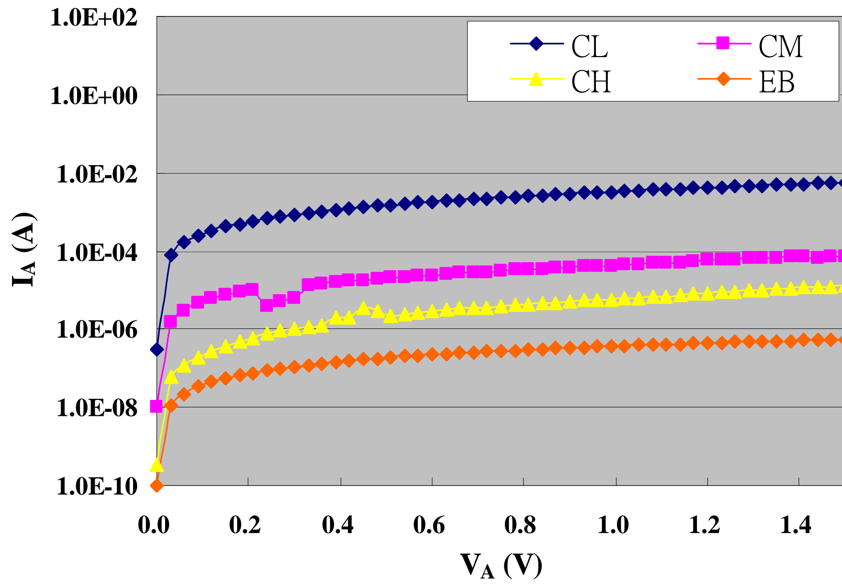


Fig. 4.19 The *I-V* characteristics of the metal strip deposited by various approach and deposition current. The E-beam deposited metal exhibits highest resistance than the Ion-beam deposited metal.

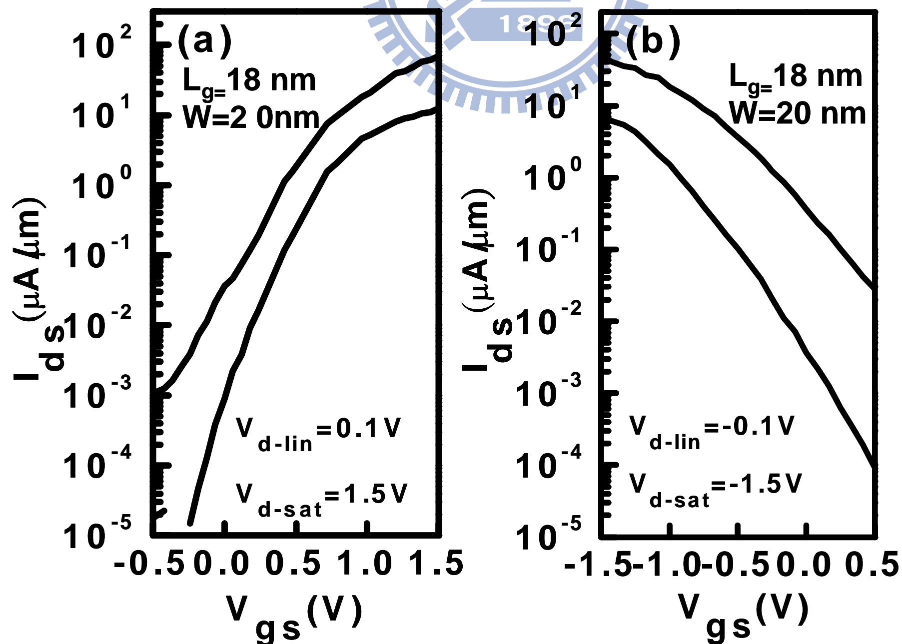


Fig. 4.20 (a) nFET nanowire device I_d-V_g characteristics. (b) pFET nanowire device I_d-V_g characteristics.

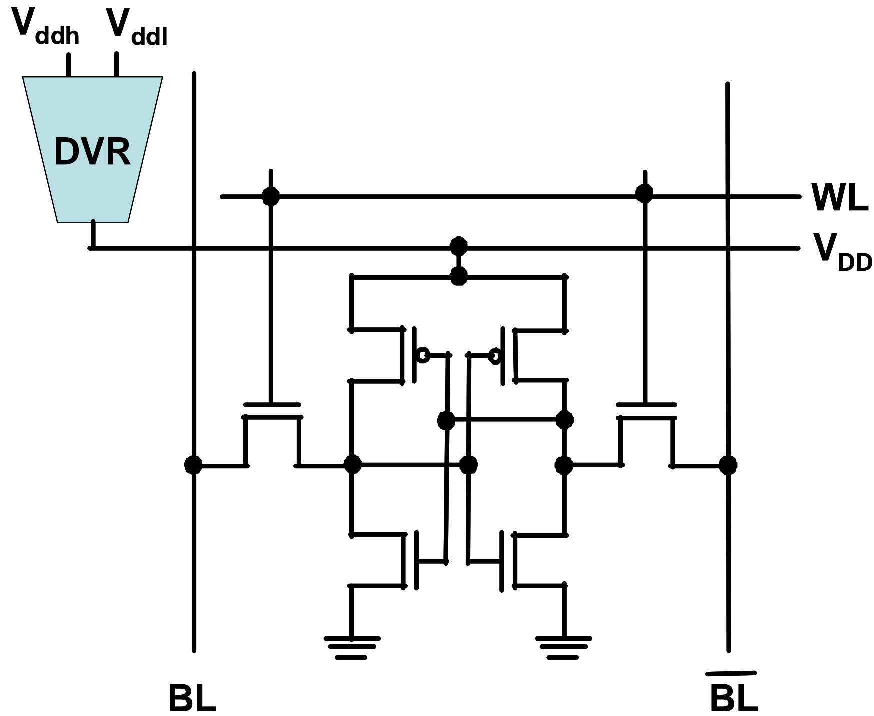


Fig. 4.21 The schematic diagram of dynamic voltage regulator (DVR) configuration of a SRAM cell.

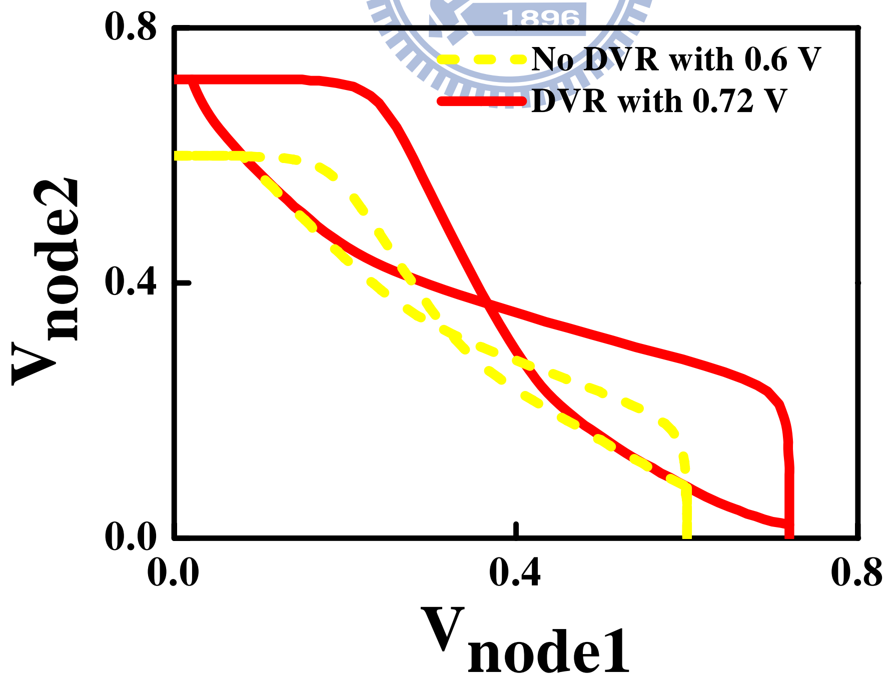


Fig. 4.22 6T-SRAM static noise margin (SNM) improvement by a 20% V_{dd} increasing of the cell voltage during read operation.

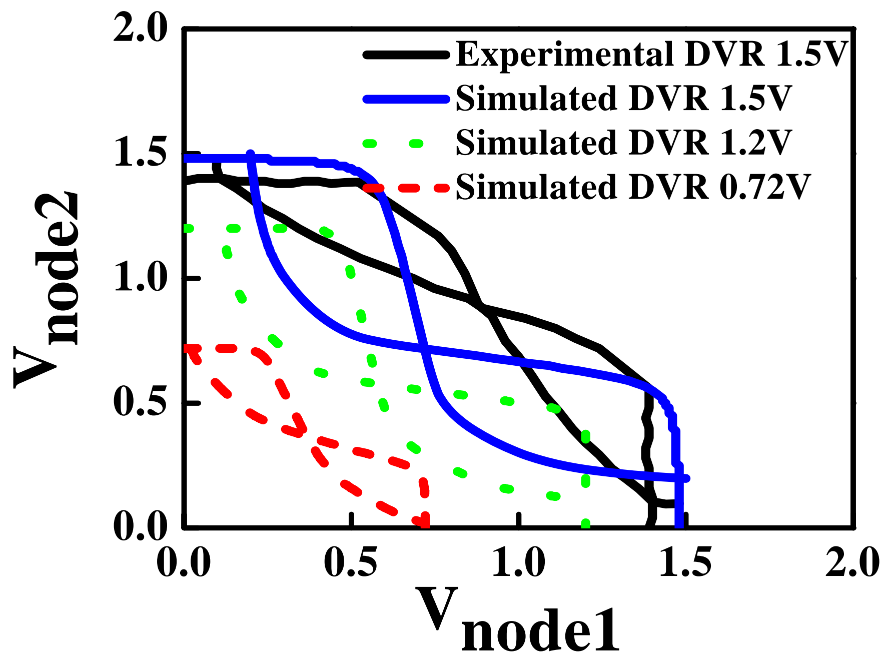


Fig. 4.23 Butterfly curve of experimental 0.039 μm^2 6T –SRAM. The simulated SNM exhibit superior characteristics indicate the high resistance and not optimal devices characteristics such as junction leakage impact the SNM characteristics of SRAM.

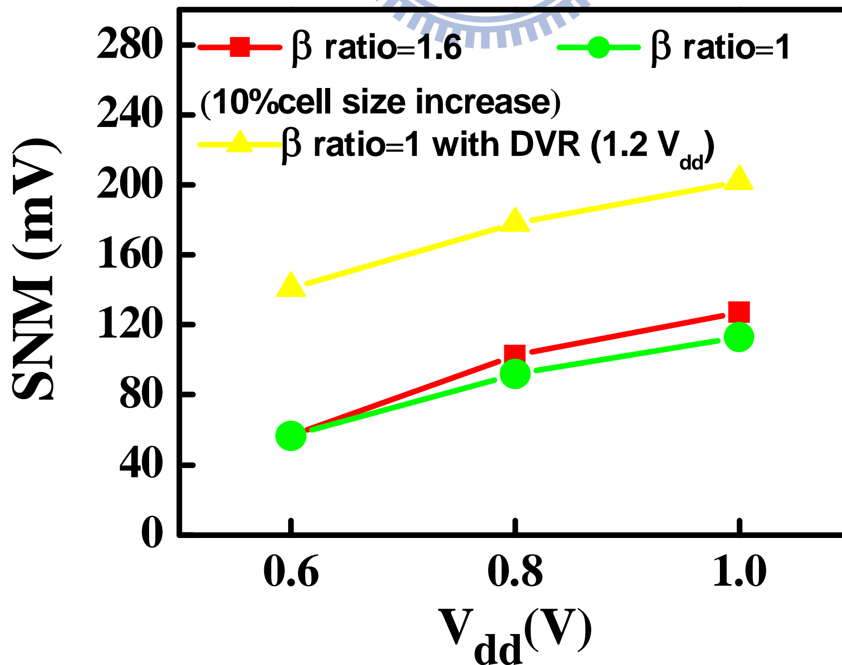


Fig. 4.24 Simulated SNM versus V_{dd} at varied β ratio and with/without DVR. The data shows DVR can greatly increase SNM, especially at low V_{dd}.

Chapter 5

Device Silicidation using Pulsed Laser Annealing (PLA)

5.1 Introduction

With the shrinking of the device dimension, the external parasitic resistance reduction becomes more challenging due to the restriction of the junction-depth requirement for SCE control. Figure 5.1 shows each component of parasitic resistance in a general planar MOSFET structure. The total external resistance includes:

$$R_{ext} = R_{ov} + R_{ldd} + R_{sd} + R_{co}$$

With the device design rule shrinkage, the device spacing is reduced and the device scheme is redesigned for performance and SCE trade-off. Based on the TCAD simulation (Synopsys ISE-TCAD), by fixing the DIBL value as 150 mV/V for each device scheme, the R_{co} suffers severe penalty when the device spacing is reduced to 0.3 μm (in the ITRS roadmap, the poly spacing of contact-landed devices is 0.13 μm for 32-nm node generation) as shown in Fig. 5.2. To limit the junction abruptness of the device for short channel devices, the junction depth as well as dopant concentration of the junction are forced to reduce, and the ρ_c will be affected based on the formula [97]:

$$\rho_c = \rho_{co} \exp\left(\frac{2\phi_b}{\hbar}\sqrt{\frac{\varepsilon_s m^*}{N}}\right)$$

Where ρ_{co} is a constant dependent on the metal and semiconductor. The specific contact resistivity, ρ_c, primarily depends on: (1) the metal-semiconductor work

function, φ_b, (2) doping density, N, in the semiconductor, and (3) the effective mass of the carrier, m^*. Owing to the SCE constraint, poly spacing reduction with the shrinking technology, as well as the limited impurity solid solubility in silicon, it is difficult to increase the dopant density to reduce ρ_c. To overcome this obstruction, the most straightforward method is to select the low SBH material for silicide. Several reports had demonstrated that SBH can be reduced to sub-0.1 eV by using some novel approach or novel metal material, such as the silicide material [98]. Here, we proposed a novel approach to modulate the SBH of NiSi by using CMOS-compatible approach.

NiSi is a common silicide material used in advanced MOS transistors due to its low formation temperature, low Si consumption, and low line width sheet resistance dependence, when compared with cobalt or titanium silicide. However, Fermi-level pining at the NiSi/Si interface sets the work function of NiSi to a mid-gap value of around 4.7 eV, leading to a high source/drain resistance. Therefore, techniques that can potentially reduce the NiSi SBH are of interest, because they will allow the continued use of NiSi in future transistors. A previous study showed that the single crystalline and uniform $NiSi_2$ phase can effectively reduce the SBH by approximately 0.3 eV [99]. However, $NiSi_2$ phase transformation needs high temperature and is generally much less stable on the (100) Si surface than on the (111) surface [100]. In this chapter, the PLA was introduced, which can replace the conventional rapid thermal annealing (RTA) approach, and the advantage of using PLA for $NiSi_x$ formation on (100) Si was implemented to demonstrate device performance. The PLA application is attractive for the fabrication of ultra-scaled semiconductor devices due to its sufficient effective temperature for dopant activation with diffusionless junction profile. In addition, strain application for the enhancement of carrier mobility is more challenging with the continuing shrinkage of the technology node. The aggressive

scaling design rules limit the strength of the strain developed in the process due to shrinking device dimensions and issues of proximity [101]. Hence, process strain enhancement, approached from either the type of material aspect or another process that leads to device process optimization, becomes an indispensable procedure for maintaining the strain benefit of ultra-scaled devices [102,103]. In addition, the tensile stress enhancement of $NiSi_x$ silicide formation by using PLA was observed and discussed.

5.2 Analysis of PLA Effects on NiSi Formation

For experimental study, 6 inch (100) n and p-type wafers were used as substrates. Before Ni deposition, the wafers were cleaned in HF acid and rinsed with de-ionized water. Inductively-Coupled Plasma (ICP) pre-sputter was performed for 10 sec for native oxide removal, the 20 nm Ni and 15 nm Ti were then deposited sequentially by physical vapor deposition (PVD). The Ti was used as a capping layer to avoid oxygen contamination during silicidation [104]. Wafers then underwent different two-step annealing processes for silicidation and the process flow is shown in Fig. 5.3. The flow-1 sample employed a two-step rapid thermal anneal (RTA) at 300 ºC for 15 s and 400 ºC for 30 s in ambient N_2 as a baseline condition. The flow-2 sample was prepared by replacing the first RTA with PLA, and the flow-3 sample was prepared by replacing the second RTA with PLA. The RTA was conducted with Heat Pulse 610 and the PLA was conducted with a pulsed N_d:YAG laser with a 355 nm wavelength and 10 ns pulse period. After the first annealing process, un-reacted Ni and Ti was removed by a wet etchant consisting of H_2SO_4 and H_2O_2 with a ratio of 4:1. The sheet resistance of the sample was measured using a 4-point probe. The blank wafer stress was measured using a Tencor FLX-2320, which measures the change in the radius of

curvature of the substrate.

The correlations of sheet resistance and blanket wafer stress capacities for different annealing conditions and PLA energy density is shown in Fig. 5.4. Increased sheet resistance and significant tensile stress enhancement of laser annealed samples were observed compared to the RTA samples. Glancing-Incidence XRD was used for silicide phase characterization and result is shown in Fig. 5.5. The resulting spectrum of the two-step RTA sample revealed inhomogeneous phases of Ni silicide, including Ni-rich silicide and NiSi formed with two-step RTA. By replacing the second RTA with PLA, the rising peak intensity of the Si-rich $NiSi_x$ phase was observed in the spectrum. Increasing the PLA energy density above 1.5 J/cm^2 caused the Ni silicide phase to mostly transfer to $NiSi_2$ and induce significant sheet resistance increasing. Figure 5.6 shows Transmission Electron Microscopy (TEM) images of different silicidation conditions. Figure 5.6 (a) shows that the sample using two-step RTA which exhibited a rough silicide to silicon interface due to the coexistence of inhomogeneous phases. Figure 5.6 (b) shows that the sample using PLA first which exhibited an ultra-thin $NiSi_2$ formation. The composition of the thin silicide was verified by an energy dispersive X-ray Spectrometer (EDS), revealing that 0.6 J/cm^2 of PLA energy is sufficient to incite the Ni to react with Si to form $NiSi_2$. The resulting thin silicide is favorable for ultra shallow junction, however, a $NiSi_2$ {111} facet appeared which would induce junction spiking issue for devices with shallow junction profile. Compared to the PLA-first sample with the same laser energy (laser energy: 0.6 J cm^{-2}), the sample replacing the second RTA with PLA exhibited a flat silicide to silicon interface which is shown in Fig. 5.6 (c). Alberti et al. found that nickel profile in the silicon layer plays a crucial role to activate the Si crystallization during excimer laser annealing [105]. In this work, the flow-2 employed a conventional RTA prior to the PLA to distribute sufficient nickel atoms within the

desired silicidation depth, which is beneficial to improve the crystalline characteristic of silicide and its interface to the underneath silicon. However, when PLA energy density rose above a critical level, either $NiSi_2$ began to agglomerate, or Silicon precipitation occurred, leading to an abrupt increase in sheet resistance which is shown in Fig. 5.6 (d). The proposed model of this PLA enhanced smooth $NiSi_2$ formation is illustrated in the Fig. 5.7.

After the first thermal RTA annealing for the Ni_xSi_y formation, the PLA energy induced the melting of nickel silicide, and this melt front propagated down to the silicide and silicon interface. The mixing of silicide and silicon occurred via a liquid phase diffusion, which leaded to a flat interface and silicon-rich silicide melting near the interface [106]. Therefore, to avoid the $NiSi_2$ facet formation, the laser power and duration have to be lager enough to melt the Si substrate underneath the silicide to provide sufficient Si atom diffusion for $NiSi_2$ formation otherwise the Ni diffusion will dominate the silicide formation and the {111} facet will be inevitable appear. The silicide thickness and stress difference correlation was further investigated to exclude the volume change effect, results are shown in Fig. 5.8. The different silicide thickness were obtained by increasing the RTA temperature and PLA energy density for flow-1 and flow-3 respectively and the silicide layer thickness were investigated by TEM. Based on the result, the combined effect of an increased effective temperature of PLA with different silicide phases formed after PLA can lead to thermal stress differences and result in higher tensile stress. Although the strain benefit decreases as the silicide thickness decreases, the improved silicide morphology using pulsed laser annealing is beneficial for process control with an aggressive reduction in silicide to channel proximity, as it obtains higher channel strain with resistance reduction for future extremely scaled transistors.

5.3 Electrical Characteristics of Silicided Schottky Diode

The Schottky diode fabrication was initiated with LOCOS isolation and followed by 35 nm thermal oxide growth. The active area was implanted with BF_2 at 70 keV and a dose of 2×10^{13} cm^{-2} for p-type substrate and phosphorus at 120 keV and a dose of 7.5×10^{12} cm^{-2} for n-type substrate. After implantation, samples were annealed in a 1100 ºC furnace for 10 minutes to activate the dopant. Finally, different Ni silicide formation processes were evaluated and electrical testing was performed using a HP4156. Figure 5.9 (a) shows the comparison of two favorable Schottky diode *I-V* characteristics. The area of the measured diode is 4×10^{-6} cm^2 and the zero bias SBH of each sample was deduced by linear fitting of the forward-bias *I-V* characteristics based on the thermionic emission model at room temperature, using an effective Richardson constant of 32 A/cm^2 K^2 in the calculation [107].

$$J = A^{*}T^{2}[\exp(-\frac{q\phi_b}{kT})][\exp(-\frac{qV}{nkT})-1];$$

The diode with the PLA showed an 0.2 eV SBH increase for hole from a highly rectifying diode with improved ideality factor (n=1.28) and the obtained SBH (Φ_{bo}=0.68 eV) was close to the reported value for $NiSi_2$ on a (100) p-type substrate [108-109] compared to the sample treated with conventional two-step RTA annealing (ideality factor n = 1.28 and extracted Φ_{bo} = 0.52 eV). The observed hole barrier height increased from 0.52 eV to 0.68 eV suggests that the Fermi-level of silicide is shifted from the mid-gap level to a level close to the conduction band of silicon, reducing the barrier height of the electron. The result is also examined by using the slope of the Arrhenius plot in the reverse-bias region and the result is in good agreement with the value deduced from forward bias current which is shown in Fig. 5.9(b). At the same time, Fig. 5.9(c) shows an ohmic-like characteristic of laser

irradiated sample which was fabricated on n-type substrate, also proves SBH modulation effect. In the conventional MOSFET, the low SBH silicide is desired to connect to a heavy doped source/drain region for parasitic resistance reduction. The heavy doped region creates a narrow depletion region at the silicide/silicon interface and in addition, the low SBH enhances the carrier tunneling probability. Consequently, the carrier conduction mechanism at the interface is tunneling dominated thus the so-called specific resistance is reduced [97]. According to the study using the theoretical field emission model and considering the dopant concentration effect, a 0.2 eV SBH reduction will lead to a decrease of approximately one third in the specific resistance observed for a heavily doped source/drain [110]. By adjusting the energy density of PLA within the adequate range improves the diode ideality factor, which is shown in Fig. 5.10, due to the formation of smooth $NiSi_2$ morphology at the silicon interface. However, increasing the laser energy density above a critical range caused a significant increase of leakage current and a drop in the ideality factor due to degraded interface morphology (See Fig. 5.11). From TEM investigation, a Si-rich ($Ni_{0.23}Si_{0.77}$) Ni silicide forms and leads to deterioration in the interface flatness which cause the diode characteristics degradation which is shown in the Fig. 5.6 (d). For further improvement of the diode ideality factor, while maintaining a reasonable sheet resistance under sufficient laser energy, special consideration should be made of the silicide with uniform composition at the equilibrium phase before the PLA to improve the microstructure of both the interface and the bulk region of silicide.

5.4 Application of PLA Silicidation for nMOSFET Devices

Recent advance CMOS scheme is illustrated in Fig. 5.12. To make best use of the process strain, nFET employed the source and drain recess with high tensile stress

contact etch stopping layer for electron mobility enhancement. On the contrary, pFET employed embedded SiGe source and drain which generate the higher compressive strain in channel region due to lattice mismatch and also used high compressive stress contact etch stopping layer for hole mobility enhancement. Compared to pFET, the silicide stress enhancement for nFET is more favorable due to the its closer proximity to channel for strain enhancement with less process complexity. To evaluate the effect of silicide proximity on devices performance, Device TCAD simulation template using Synopsys ISE-TCAD was built for silicide stress and performance evaluation and result is shown in Fig. 5.13. The energy-balance and quantum-mechanical model, based on the modified local density approximation were used for simulation. Two major approach were interested for silicide strain enhancement: (1) Reducing the silicide to channel proximity by reducing the spacer width before silicidation and, (2) Increasing the Ni silicide thickness to increase the strain. From the simulation results shown in Fig. 5.14, it indicated that strain strength enhancement is more significant when the spacer width was reduced before silicidation. Unfortunately, excessively reduce silicide to channel proximity and further increase the silicide thickness will severely degrade the device performance. Increased silicide thickness under an identical junction profile will lead to on-current degradation due to severe current crowding effect which is shown in Fig. 5.14 and will cancels the mobility gain. As a result, to enhance the Ni silicide strain with controllable silicide thickness and adequate silicide to channel proximity are required to obtain silicide strain benefit.

For the devices sample preparing, LOCOS isolation was performed, followed by threshold voltage (V_{th}) implantation using BF_2 at 90 keV and a dose of 1×10^{13} cm^{-2}. A 3-nm pure thermal oxide layer (for its dielectric properties), a 120-nm poly-Si layer (serving as a gate electrode), and a 50-nm tetraethyl orthosilicate (TEOS) capping

oxide layer (serving as an etching hard mask) were deposited sequentially. The poly-Si gate was patterned using an I-line stepper and trimmed to 130 nm using a photo resister and the “ashing and etching” approach, followed by 5-nm poly-Si re-oxidation (as an offset spacer) in a furnace. BF_2 was used for 30° tilted-angle halo implantation at 50 keV and a dose of 3×10^{13} cm^{-2}; As implantation (7 keV, 1×10^{15} cm^{-2}) provided the lightly doped drain (LDD). The deposition and etching of 100-nm-thick SiN was performed for spacer formation. The TEOS hard mask employed for poly-Si gate patterning was then removed through HF dipping to ensure that the SiN spacer height was not less than or higher than the poly-Si gate height to protect the poly-Si from melting during the PLA process. The wafers then underwent deep source/drain implantation using As (20 keV, 5×10^{15} cm^{-2}). After exposing the wafers to RTA (1000 °C, 10 s) to activate the dopant, the two different silicidation processes were compared for their effects on performance. Plasma-enhanced chemical vapor deposition (PECVD) was used to provide a 400-nm TEOS layer for inter-metal layer deposition; finally, physical vapor deposition (PVD) of Aluminum was used for contact and electrode pad formation.

We employed a total resistance slope-based approach [111] to evaluate the effect of the laser energy density on the silicidation effect of the S/D series resistance R_{sd} and on the carrier mobility. We used scanning electron microscopy (SEM; top-view measurement) to calibrate the device’s gate length, and used a constant gate overdrive voltage ($V_g - V_t$) of 2.5 V and a value of V_d of 0.5 V in the calculation of the total resistance. Figure 5.15 presents the R_{on}–L_g characteristics of the devices prepared under various PLA energy densities. Relative to the two-step RTA control wafer, increasing the PLA laser energy density had a beneficial effect on the value of R_{sd}. We hypothesize that $NiSi_2$, initially formed in the interfacial region, modulated the SBH. When the laser energy density increased further within a critical range, the crystalline

quality at the silicide interface improved; the change in the slope of the R_{on}–L_g plot indicates that the interface benefited from strain and achieved a minimum total resistance. Although higher PLA energy densities improved the strain strength, they also degraded the morphology of the silicide and led to agglomeration of $NiSi_2$, resulting in high silicide resistance and increased leakage. Consequently, there is no benefit in performance after increasing the PLA power beyond a critical threshold. Figure 5.16 (a) compares the I_{on}–I_{off} gains for short-channel devices on the PLA wafer and control wafer prepared using a laser energy density of 1.5 J cm^{-2}; adopting PLA for silicidation provided an 8 % gain over that of the RTA control. The I_d–V_g characteristics in Fig. 5.16 (b) reveal higher "on" and lower "off" currents for the PLA devices. To investigate the causes of the improved device performance, cross-sectional TEM images of the various structures were investigated and shown in Fig. 5.17. Unlike the two-step RTA-annealed devices, using PLA for silicidation at an appropriate energy density produced a flat silicide interface and $NiSi_2$ (111) facet beneath the spacer. Formation of this facet improved the SCE, in accord with previous studies [112]. The shape of silicide beneath the spacer was affected by the spacer profile as well as the thermal profile difference between the exposed source/drain area and the channel area covered by gate/spacer to form the self-organized (111) orientation of $NiSi_2$. We believed that further strain benefits would result from further reductions in silicide-to-channel proximity; we have not, however, explicitly tested the effects of changes in the silicide proximity on the process or device stability. Figure 5.18 shows the silicided n+/p diode leakage characteristics. A 10×10 array of square active area (each active area is 20 μm × 20 μm) and a bulky active area (active area is 100 μm × 100 μm) were employed as the monitor structure. From the result, the samples treated by PLA with the energy density of 1.5 J cm^{-2} exhibit tighter junction leakage distribution than the samples treated by the two-step RTA.

However, when samples treated by PLA with the energy density up to 2.3 J cm^{-2}, both the leakage distribution and the leakage current were degraded due to morphology degradation especially at a periphery-intensive structure. The thermal profile and non-uniform Si topography along the Si to LOCOS interface worsened the silicide morphology and caused severe junction leakage. Consequently, there is no benefit in performance after increasing the PLA power beyond a critical threshold.

To investigate the effect of silicide proximity on device performance, we used TCAD simulation templates (Synopsys ISE-TCAD) configured for evaluation of silicide stress and performance. The templates provide the current gain without using data related to the effect of mobility enhancement gained from the strain. Figure 5.14 reveals that the enhancement in strain strength was significant after reducing the spacer width prior to silicidation. In contrast, excessive reduction of the silicide-to-channel proximity severely impaired device performance, due to a current crowding effect, canceling any gain in mobility. Accordingly, an adequate silicide thickness, silicide shape, and silicide-to-channel proximity all provide the benefits of silicide strain without suffering from current crowding penalties. When we factor the shape of the PLA sample's silicide layer into the templates, we observed two effects that help alleviate the performance penalty that arises from reduction in the silicide-to-channel proximity: (i) a current crowding effect, illustrated in Fig. 5.19 (a) and (b), and (ii) a decrease in interfacial resistance resulting from a decrease in the SBH. Furthermore, the distance from the silicide to the depletion region was larger for the PLA sample, thereby reducing the non–V_g dependent I_{off} current, as revealed in the simulation results in Fig. 5.20(a) and (b). This behavior is consistent with our experimental results. Despite the benefits gained from strain, the performance may decrease as silicide thickness decreases; the improved silicide morphology and intrinsic silicide strain enhancement attained would be beneficial for a large reduction

in the silicide-to-channel proximity. Using PLA for the silicidation process, therefore, reduces shallow junction leakage and increases nMOSFET strain relative to those of conventional annealing processes. Although high PLA energy density might accompany with the integration concern such as poly-Si melting and gate dielectric defect issue were disclosed with current device scheme, the integration concern might be excluded when the device process flow is changed from our current "gate-first" process to a "gate-last" process [113]. Notably, the pattern geometry effect of PLA can be alleviated by using a longer-wavelength laser or by inserting an absorption layer to improve the device's uniformity and fluctuation [114-115].

5.5 Summary

We demonstrated the modulation of nickel silicide SBH and tensile strain achieved through a two-step annealing that combines the conventional rapid thermal annealing (RTA) with pulsed laser annealing (PLA) for silicidation. At the laser energy density of 1.5 J cm^{-2}, smooth $NiSi_2$ was formed at the silicide/Si interface on a (100) substrate, reducing the possibility of (111) facet induction and junction leakage. The smooth $NiSi_2$ modulated the 0.2 eV Fermi-energy from mid-gap of silicon compared to the conventional two-step RTA annealing, reducing the SBH as well as specific resistance. For device application, the PLA method produced an 8 % gain in the nMOSFET's I_{on}–I_{off} characteristics due to the interfacial resistance, carrier mobility and junction leakage were improved under the laser energy density of 1.5 J cm^{-2}. In addition, the PLA formed $NiSi_2$ exhibited a reduced silicide-to-channel proximity; with accommodation for additional current crowding and junction leakage. This method holds promise for replacing current nickel silicide annealing approaches for future applications of extremely scaled-down transistors.

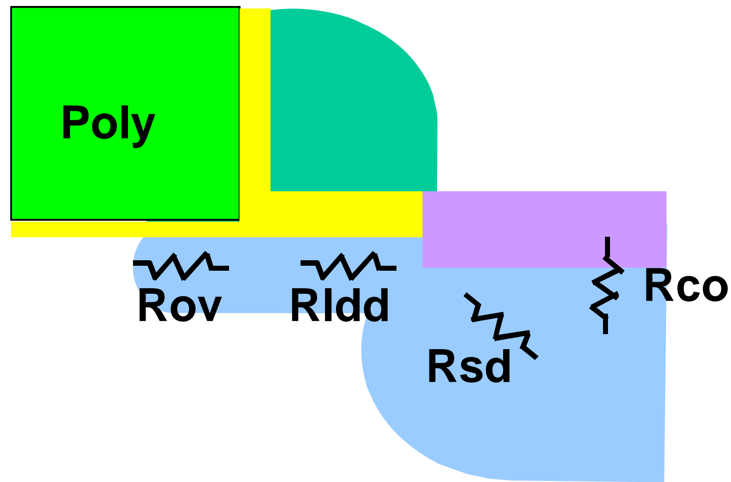


Fig. 5.1 Parasitic resistance components illustration of a conventional MOSFET structure.

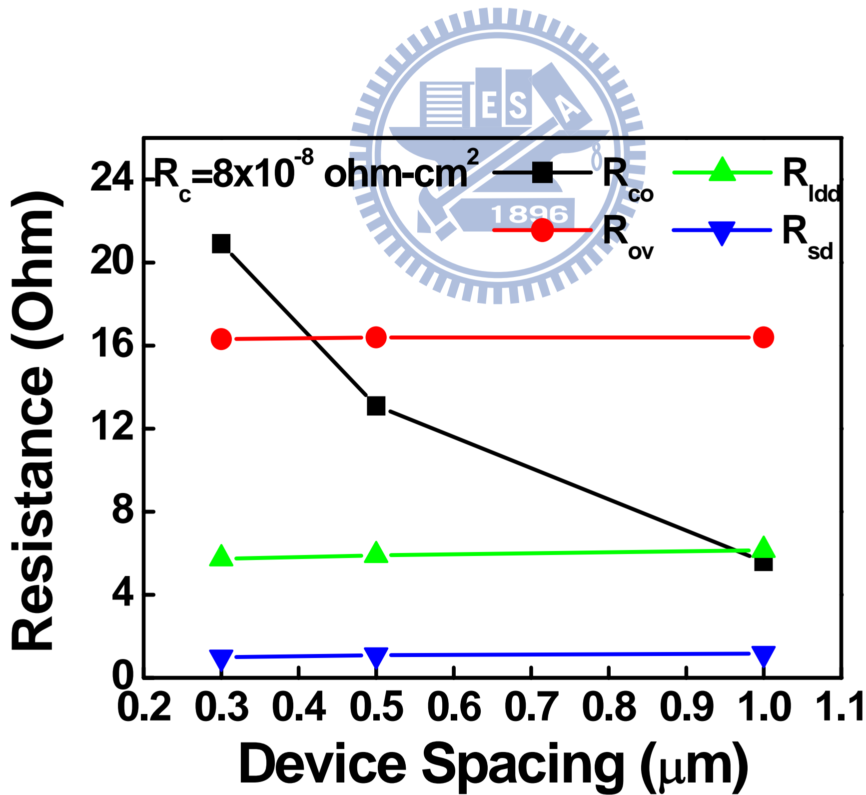


Fig. 5.2 The TCAD simulation result of each resistance component of MOSFET. The resistance is extracted by by the R=V_d/I_{dlin}. The device is designed to meet a fixed DIBL value and the V_d is obtained from the potential difference between dedicate locations.

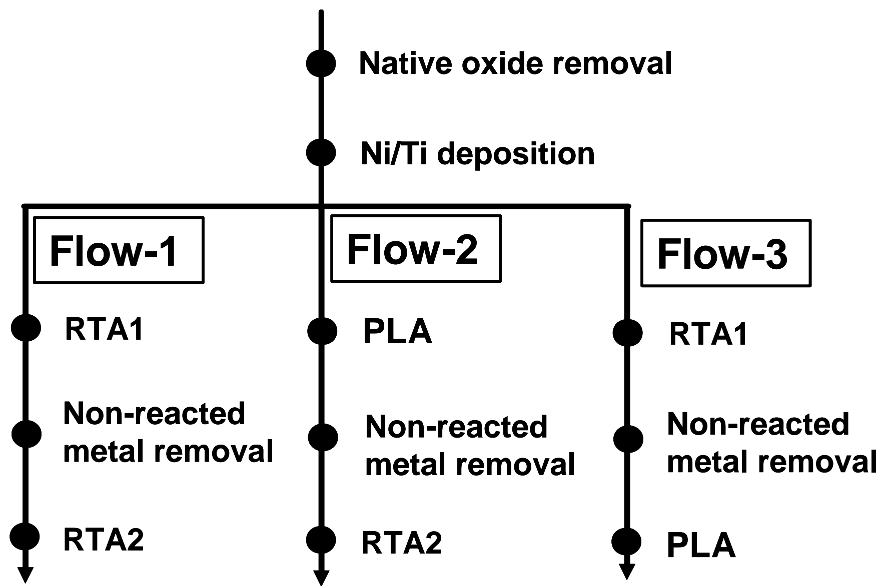


Fig. 5.3 Three different annealing process flows for silicidation evaluation.

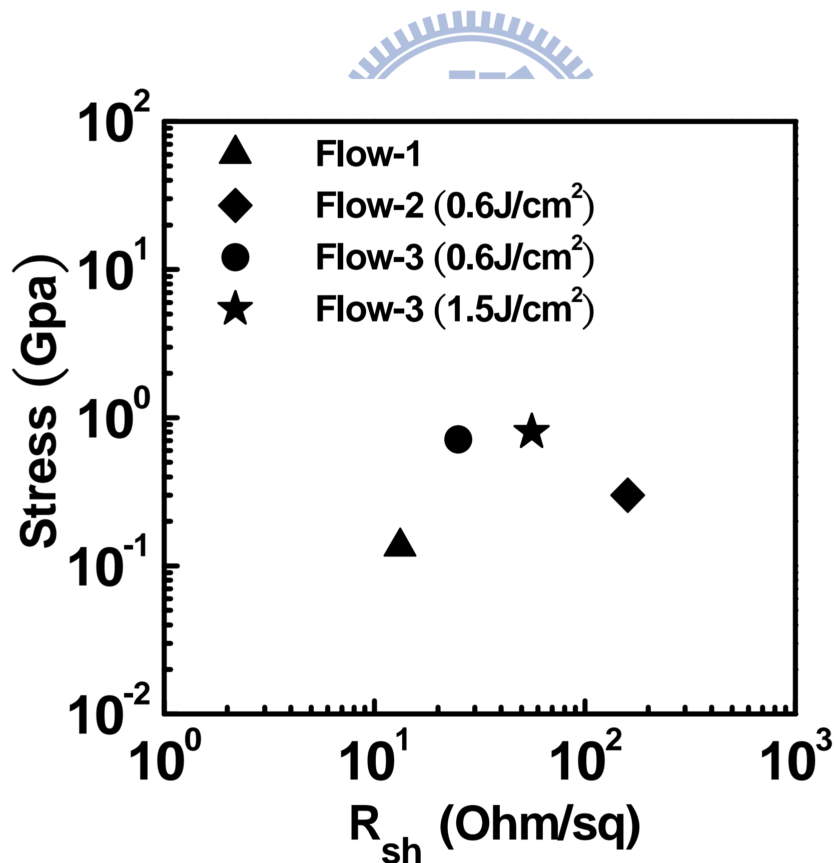


Fig. 5.4 The stress and sheet resistance correlations of different annealing sequences. The PLA energy density of the flow-3 samples were 0.6 J/cm^2 and 1.5 J/cm^2.

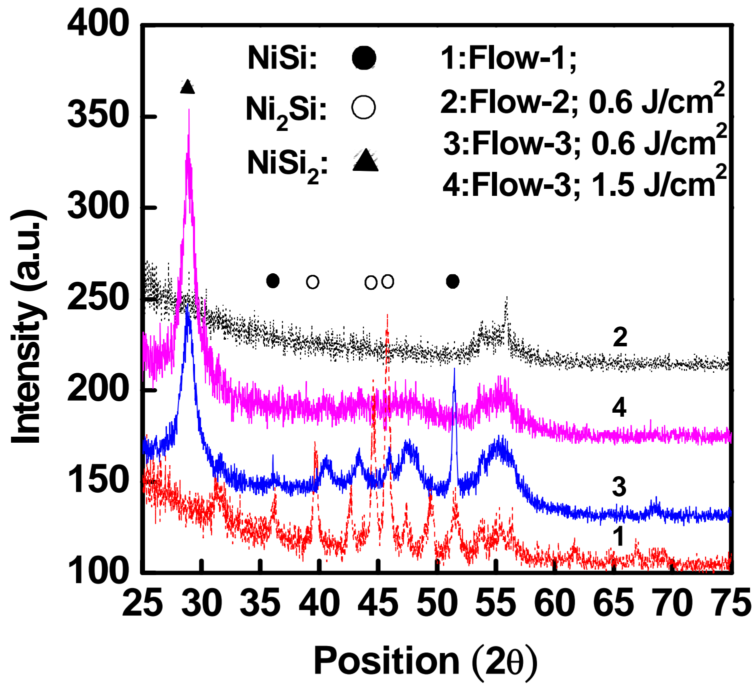


Fig. 5.5 GIXRD spectrums of different silicidation sequences.

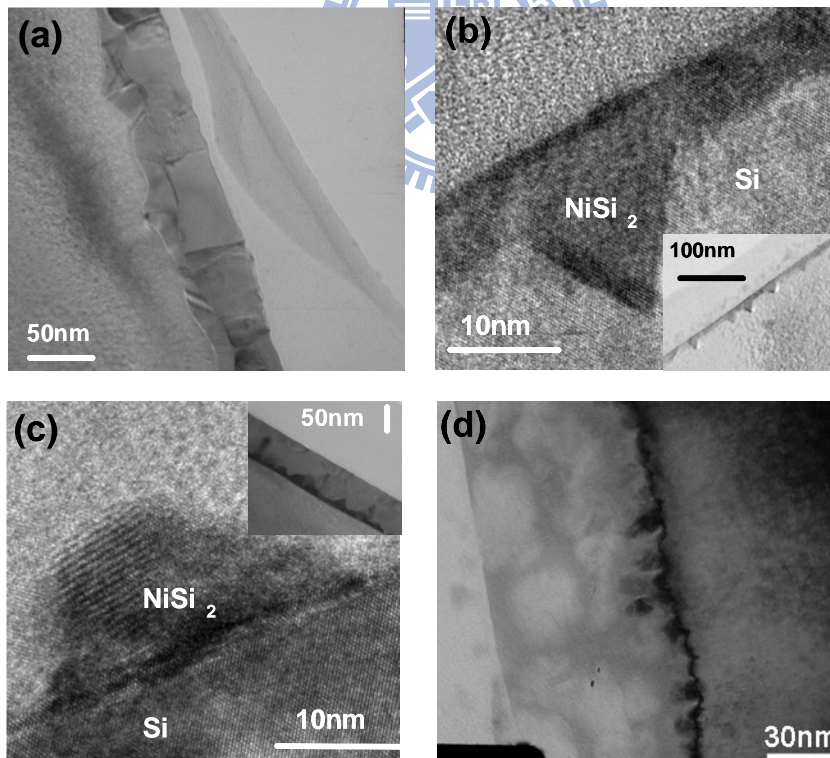


Fig. 5.6 Cross-sectional TEM images of (a) Flow-1 (two-step RTA) sample. (b) Flow-2 sample with 0.6 J/cm^2 laser annealing. (c) Flow-3 sample with 0.6 J/cm^2 laser annealing. (d) Flow-3 sample with 2.3 J/cm^2 laser annealing.

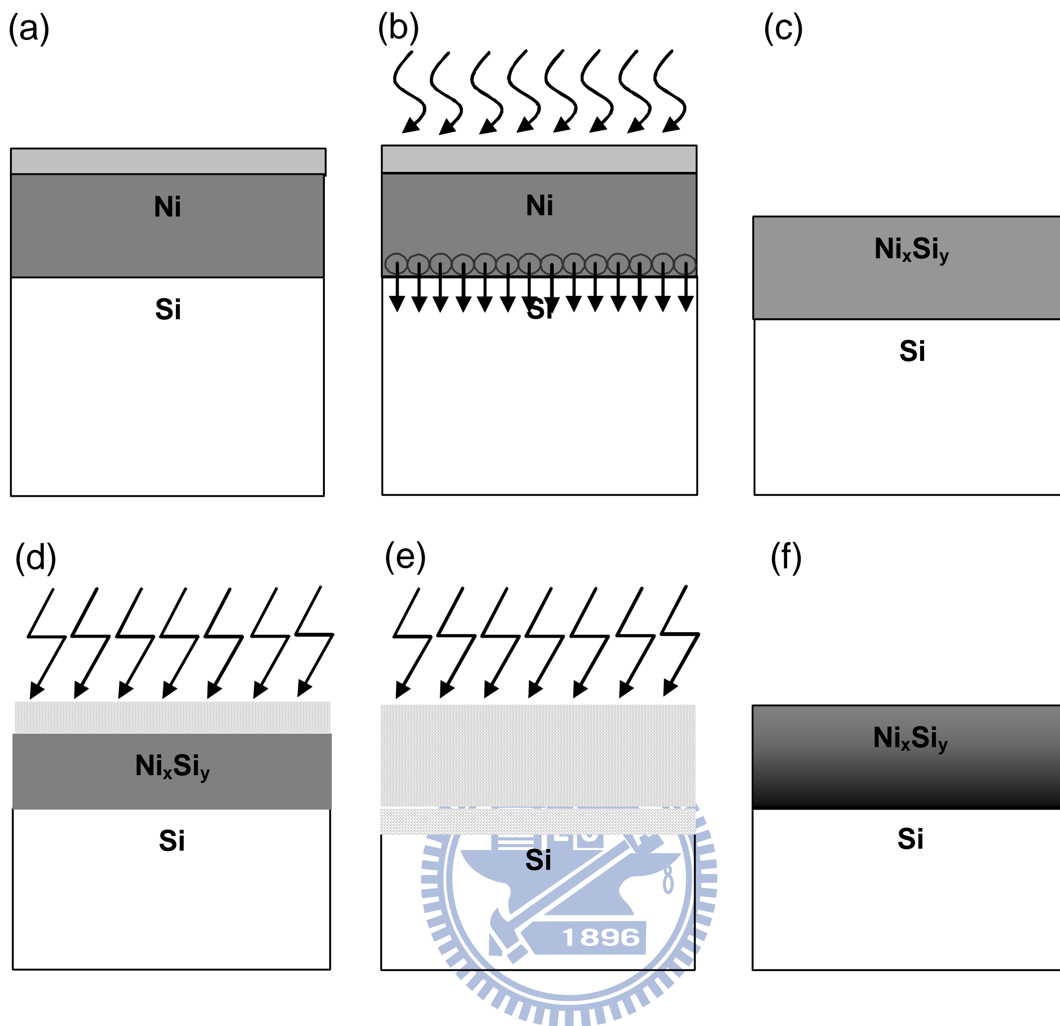


Fig. 5.7 The schematic illustration of PLA enhanced NiSi formation. (a) 10 nm Ni and 10 nm Ti capping layer deposition. (b) The first RTA (400°C,15 sec) for nickel silicidation. (c) Remove Ti and non-reacted Ni. (d) Employ PLA for second annealing, the melting front generated from top layer. (e) The melting front reach silicide and silicon interface and lead to mixing of melting silicide and silicon. (f) The excess Silicon atom appeared at interface and the quench effect of PLA formed the uniform $NiSi_2$ at interface.

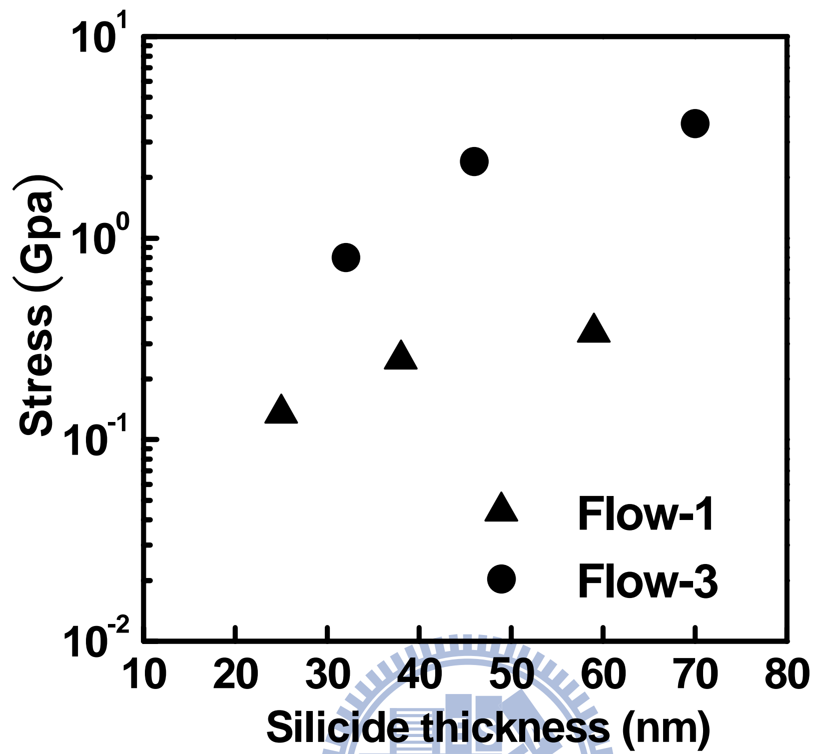


Fig. 5.8 The stress and silicide thickness correlations. Different 1st RTA conditions (300 ºC, 350 ºC and 400 ºC, all for 15 s) were used to obtain different silicide thickness for the flow-1 and different PLA energy density (0.6 J/cm^2 ,1.5 J/cm^2 and 2.3 J/cm^2) were used to obtain different silicide thickness for the flow-3.

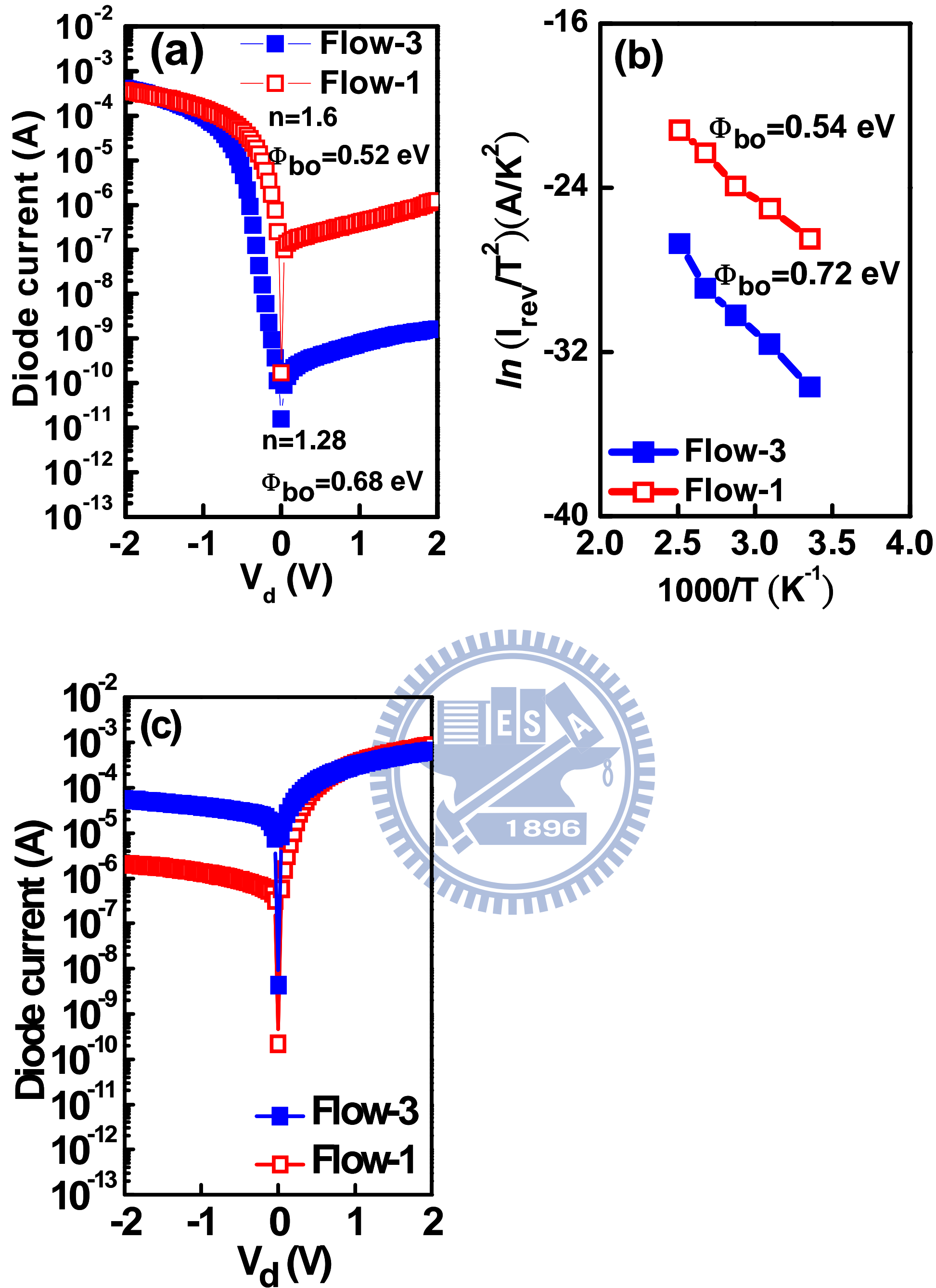


Fig. 5.9 (a) The rectifying p-Si substrate diode of flow-3 with laser energy density equal to 1.5 J/cm^2 indicates SBH increased for hole. (b) The Arrhenius plot of reverse-biased (V_d= 0.5V) diode current for SBH extraction. (c) A ohmic-like *I-V* characteristic of flow-3 with n-Si substrate which indicates the SBH reduced for electron.

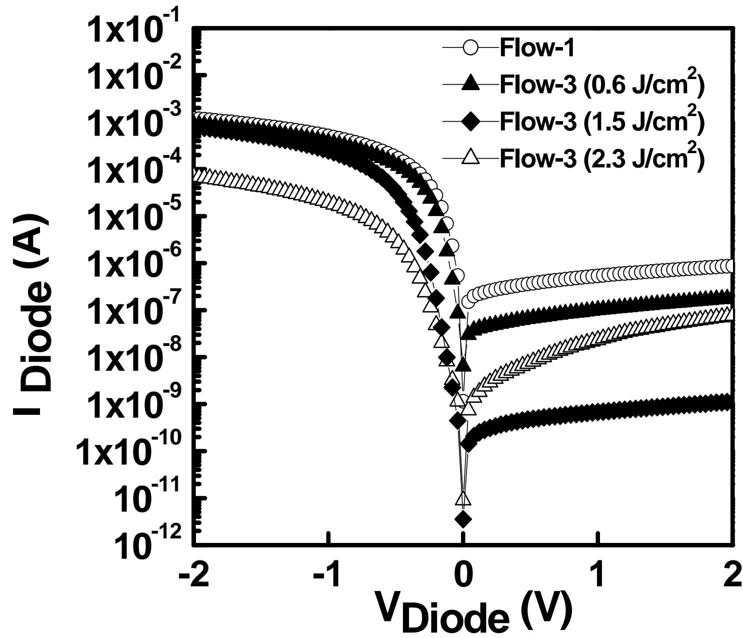


Fig. 5.10 *I-V* characteristics of p-type Schottky diodes formed under various silicide annealing conditions.

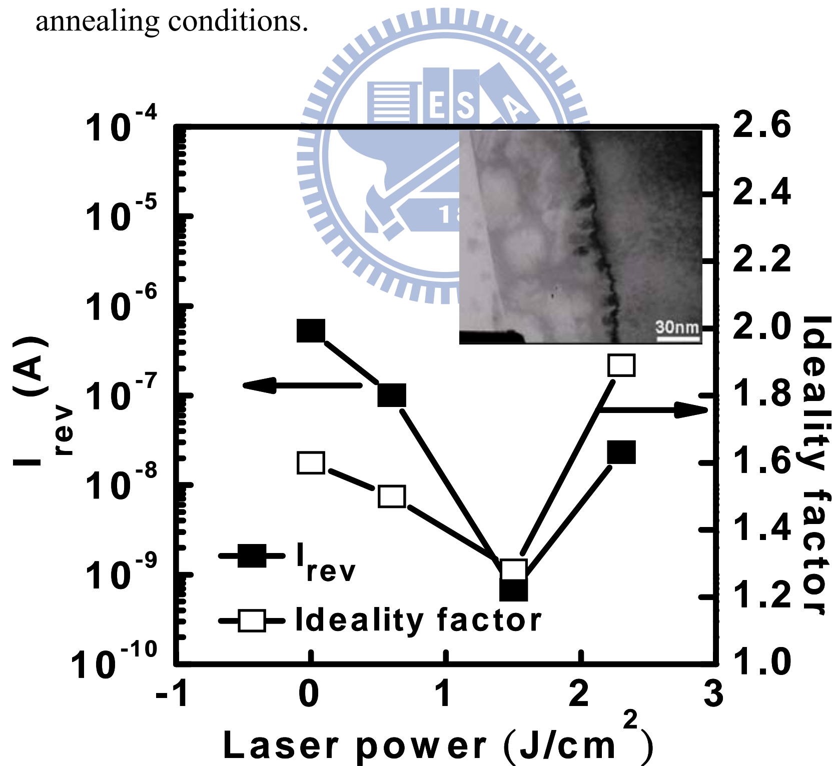


Fig. 5.11 The reverse-biased (V_d = 0.5 V) diode current and the diode ideality factor of different laser energy densities. The different energy densities are obtained by changing the laser power from 0.7 W to 2.6 W. Inset shows the TEM cross-section view of samples with laser energy density increase to 2.3 J/cm^2.

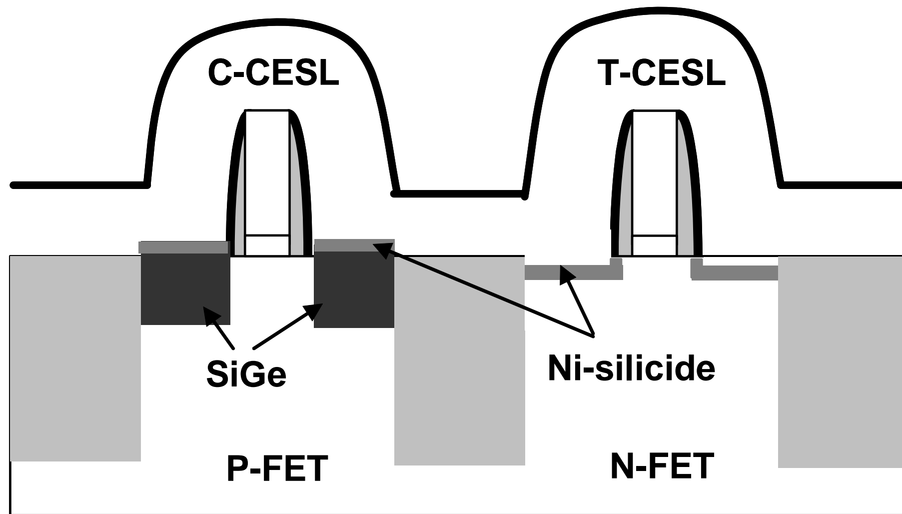


Fig. 5.12 Schematic illustration of state-of-the-art process strain enhanced cMOSFET technology.

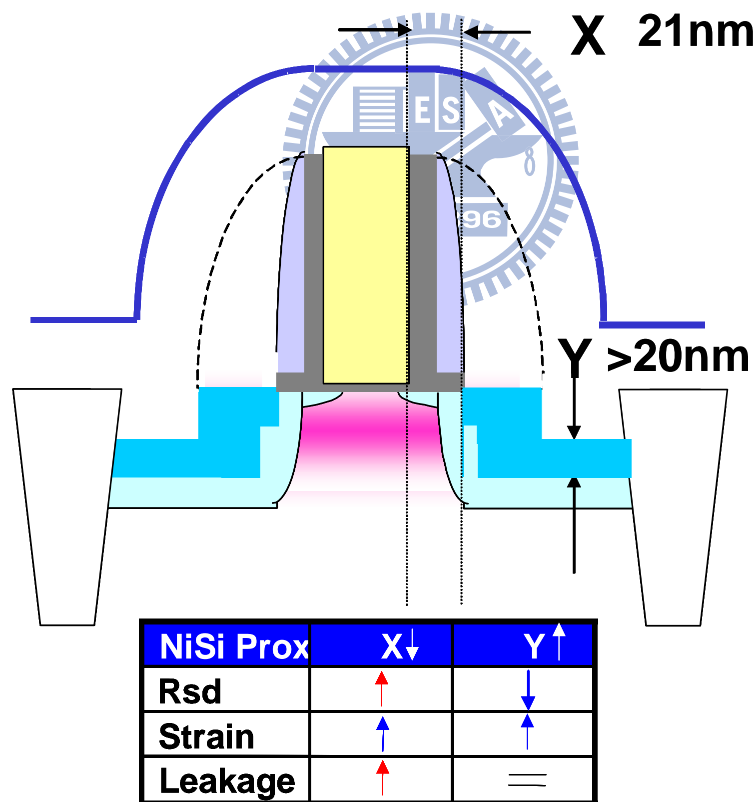


Fig. 5.13 Schematic illustration of the device performance qualitative evaluation due to NiSi proximity effect.

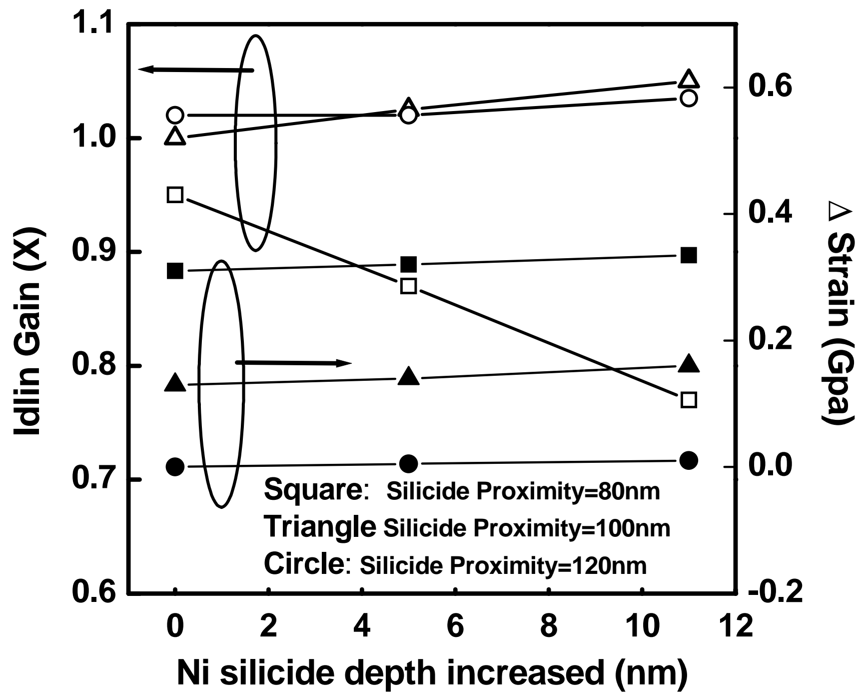


Fig. 5.14 Simulated silicide-to-channel proximity influence on the values of $I_{d\text{-}lin}$ gain and channel strain. Nickel silicide strain: 0.7 G_{pa}; initial thickness: 15 nm.

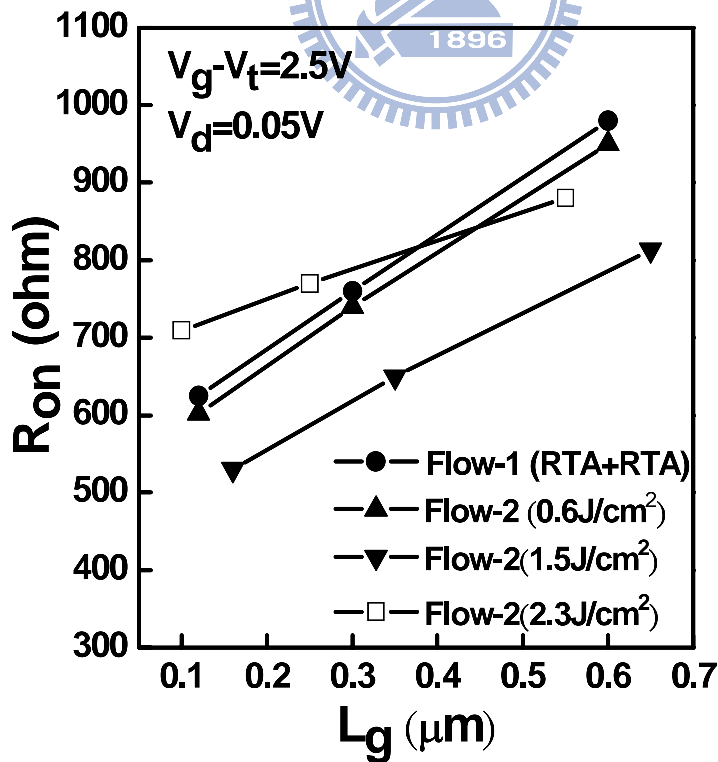


Fig. 5.15 R_{on}–L_g plots of nMOSFET devices prepared under various annealing conditions.

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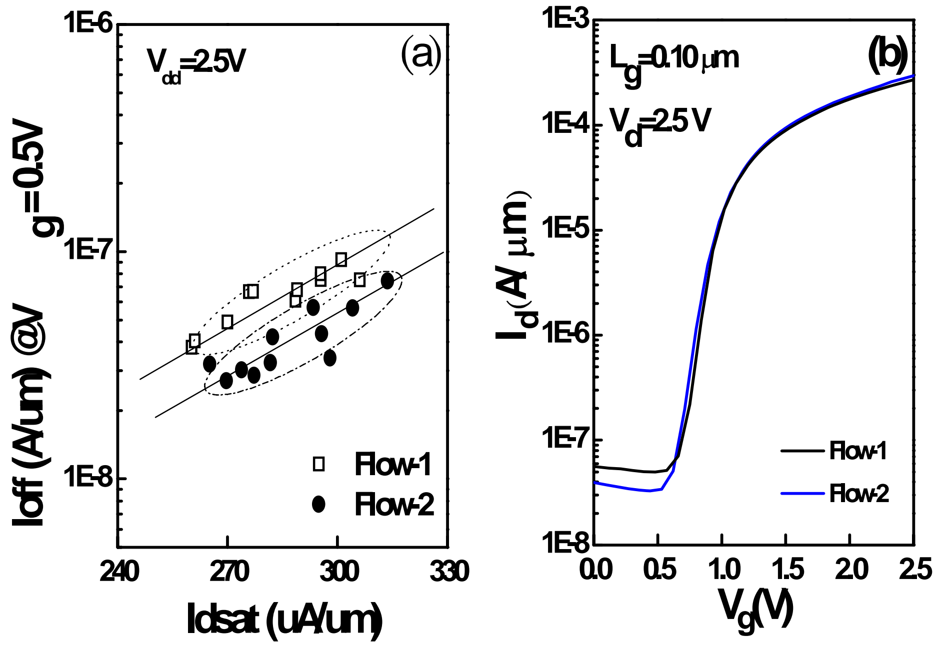


Fig. 5.16 (a) I_{on}–I_{off} characteristics of the control and PLA (energy density: 1.5 J cm^{-2}) devices. (a) I_d–V_g characteristics of the control and PLA samples.

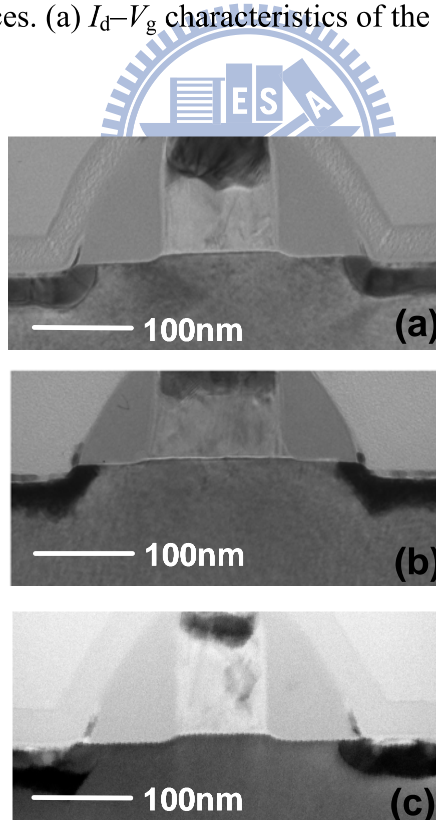


Fig. 5.17 TEM cross-sectional images of the (a) flow-1 sample, (b) flow-2 sample prepared under a laser energy density of 1.5 J cm^{-2}, and (c) flow-2 sample prepared under a laser energy density of 2.3 J cm^{-2}.

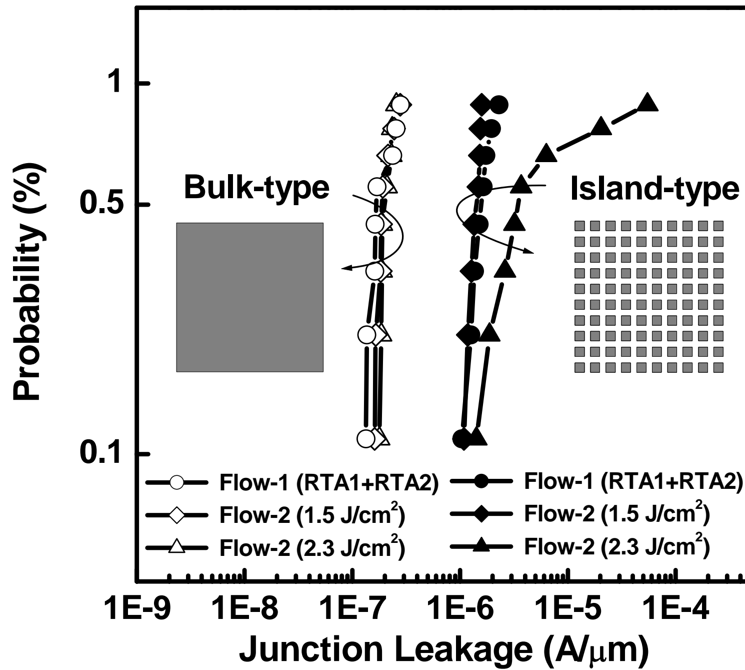


Fig. 5.18 The statistics n+/p diode leakage distribution of different silicidation splits. The dimension for the bulk-type junction structure is 100 μm ×100 μm. For the island-type junction structure, a 10 ×10 array of 10 μm× 10 μm active area is employed.

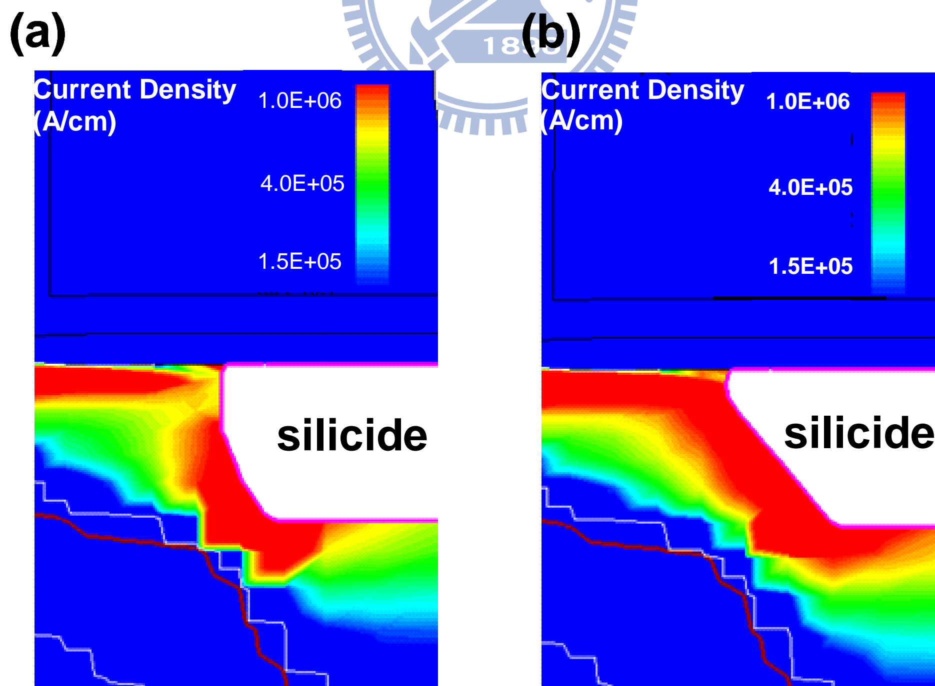
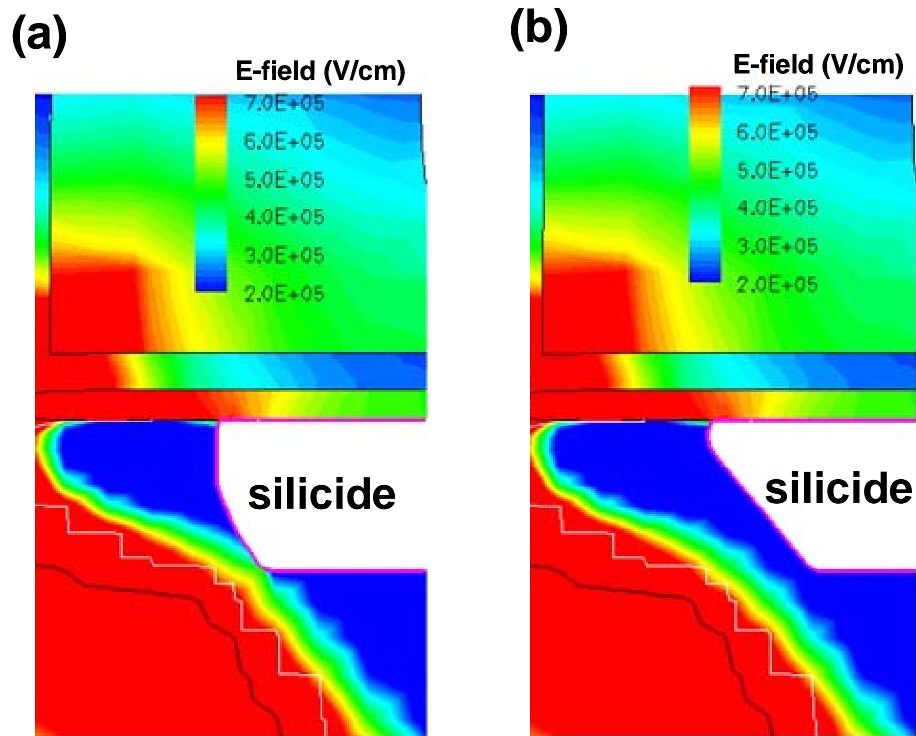


Fig. 5.19 TCAD device simulation diagrams. (a) Current crowding effects of the thicker and laterally encroached silicide. (b) {111}-Faceted silicide profile conducive to alleviating the current crowding effect.



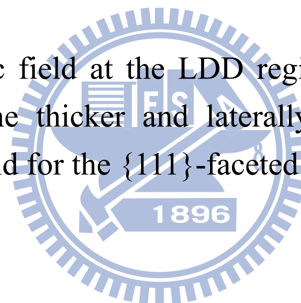


Fig. 5.20 (a) Device electric field at the LDD region, under "off"-state operation conditions, for the thicker and laterally encroached silicide. (b) The device electric field for the {111}-faceted silicide.

Chapter 6

Conclusion

6.1 Conclusion

SOI transistor scaling will continue with silicon thickness reduction before the Si thickness uniformity can not be maintained. Multiple gate or nanowire devices with 3D structure could be the most popular candidate for extremely scaled transistor. Strained silicon incorporated with SOI will benefit transistor scaling, yet it may face the tradeoff between sheet resistance and mobility enhancement. A simplified hybrid SOI/bulk structure for sub-16nm node CMOS technology study was developed. The new SOI device scheme enabled the integration of high performance/high density SOI device with high voltage periphery bulky devices. The SOI devices scheme also relaxed the short channel devices thickness requirement in terms of manufacturability. In addition to the devices exploration for logic circuit application, we demonstrated an inexpensive and high-production yield fabrication process for poly-Si nanowire FET devices that can be used for electrochemical sensors. The device uniformity was controlled well by using CMOS compatible manufacturing processes. The poly-Si NW FETs demonstrated positive pH sensitive slope (V_{th} shift $>$ 100 mV/pH) and very sensitive DNA concentration detection (V_{th} shift $>$ 100 mV in 10 pM). In addition, the ONO bottom oxide poly-Si NW FETs also showed robust endurance and retention characteristics (V_{th} P/E window >2 V after 100K P/E cycle or 3 days bake time) as non-volatile memory for smart biosensor integrated with CMOS circuit. The highly integrated process will help to serve as an interface to combine the sensor and logic-based devices. The proposed process facilitated the development of real-time,

portable and inexpensive sensor systems-on-a-chip that are mass produced using conventional semiconductor technology for healthcare applications. In order to have a early exploration for sub-16nm node devices challenges without restricting by the optical lithography, this work demonstrated that a "One-Step" non-optical patterning by Nano Injection Lithography. Single TiN gate, and nanowire channel can be integrated to achieve a record area size of 0.039 μm^2 for a functional 6T-SRAM cell. This is a low cost low throughput option for device and circuit verification at 16nm and beyond. In the final, we compared the modulation of nickel silicide resistance and tensile strain achieved through conventional RTA and PLA annealing methods applied during silicide formation. At an optimized laser energy density, smooth $NiSi_2$ was formed at the silicide–Si interface on a (100) substrate, reducing the possibility of (111) facet induction and junction leakage. The PLA method produced an 8 % gain in the nMOSFET's I_{on}–I_{off} characteristics; furthermore, the interfacial resistance and junction leakage both improved upon optimizing the laser energy density. Using PLA, the formed $NiSi_2$ exhibited a reduced silicide-to-channel proximity; with accommodation for additional current crowding, this approach would provide further improvements in strain strength. This method holds promise for replacing current nickel silicide annealing approaches for future applications of extremely scaled-down transistors.

6.2 Suggestion for Future Work

For the thin Si SOI devices, the most serious problem is the series resistance. Although the raised source/drain can alleviate the resistance problem, it also introduces extra cost and process variability and complexity. In the future, to use a simple metal with low Schottky barrier height to direct contact to the Si with uniform

and sharp interface may be necessitous for ultra-scaled devices. Therefore, the Si interface treatment before metal contacting may be an attractive topic for parasitic resistance reduction no mater for SOI or nanowire structure devices. For the nanowire application, the critical issue is the reliability of nanowire when operating in the aqueous environment. The passivation material, such as High-K dielectric, to protect the nanowire after fabrication may be beneficial but the result is still needed to be verified. The effect of poly trap density and its correlation to the surface ion concentration variation is also needed to be identified. For the nano-injection lithography, the throughput of this technology is still similar to the e-beam lithography which limits its application for chip level production, the multiple e-beam or the precursor composition improvement to enhance the deposition rate would be the next steps to promote this technology for wafer level manufacturing.

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