

應力記憶技術應用於奈米尺寸

N 型金氧半場效電晶體特性之研究

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本論文主要研究主題為單軸應變應力記憶技術對奈米尺寸之 N 型金氧半場效電晶體特性之影響。所謂的應力記憶技術即，當閘極的多晶矽及源、汲極被 N 型摻雜離子注入後，電晶體將被覆蓋一層氮化矽。在之後退火使得摻雜活化的過程中，因為閘極多晶矽及源、汲極矽原子的重新結晶，其在通道的所產生垂直壓應力及延著元件長度方向的拉應力，正好能夠增進電子在 N 型金氧半場效電晶體的遷移率。

首先，在第一章中，我們本論文的結構和描述研究的動機。

第二章主要概述應變矽技術對載子遷移率提升的理論。當互補式金氧半場效電晶體的結構因微縮而達到其極限時，應變矽技術會改變 矽晶體及其電子和電

洞的能帶結構，所產生的應變矽通道 (strained channel) 正可用來提升載子的遷移率。我們亦簡介了應變矽技術的兩種製備方法。第一種為雙軸伸張引起的應變矽。早期已有研究證明，可利用矽與矽鍺之間晶格的大小差異，而在矽鍺基板上製造出形變矽元件。雖然雙軸伸張形變矽在近年來被廣泛重視地應用為增進載子遷移率的技術，但此技術被證明有如下缺點。如在界面上有大量的貫穿差排而使得元件難以製作，以及鍺原子會向外擴散、源極與汲極延伸區的摻雜易快速擴散和其基板的高成本…等等。相形之下，第二種單軸形變卻可用簡單的製程改變而製作出來，從而避免雙軸形變中複雜的晶圓製作、高成本以及大量缺陷等問題。單軸形變元件逐漸成為用來增進載子遷移率的主要技術。

在第三章中主要介紹應力記憶技術，最佳化的低成本應變記憶技術 (SMT) 已經應用在先進奈米製程技術上，並有明顯改善 N 型金氧半場效電晶體特性的能力，如電導和驅動電流的提升。然而，應力記憶技術對 P 型金氧半場效電晶體的影響，例如硼原子擴散及其空乏效應等，故需要額外蝕刻製程去控制應變記憶技術對 P 型金氧元件的退化。最後進一步提出應力記憶技術的產生、儲存機制，以及其應力傳導的模型。

在第四章裡我們用國家奈米元件實驗室六吋晶圓實驗來證實應力記憶技術應用在 N 型金氧半場效電晶體的表現。藉由應力記憶技術可以改善元件的電特

性；包括因提高電子的遷移率的轉移電導，較佳的短通道控制能力，如抑制臨界電壓的下滑(V_t roll-off) 表現，較佳的 DIBL，可以應用於高度微縮元件的操作。除此之外，我們第一次發現到應力記憶技術是一種可以改變 N 型源、汲極接面擴散深度的製程。其所形成的超淺、陡峭接面，正可用來改善 N 型金氧半元件的短通道控制能力。然而，元件的熱電子可靠度卻會因此而變差。我們推測是由於在應變矽的通道結構中，靠近汲極端的電場強度會增加，而導致更嚴重的碰撞游離(Impact Ionization)所造成。

第五章裡，我們對不同的應力記憶技術氮化矽覆蓋沉積製程反應在六吋晶圓 N 型金氧半場效電晶體元件特性的影響進行了研究。所使用兩種的氮化矽覆蓋沉積製程分別是爐管低壓化學氣相沉積和電漿增強式化學氣相沉積。也探討氮化矽薄膜退火前、後的基本特性，如厚度，收縮率，化學成分的變化，應力的變化。我們發現不同氮化矽的沉積過程中，不同的熱預算 (thermal budget) 與氮化矽在晶片正反面覆蓋的行為，皆會影響載子的遷移率、臨界電壓的下滑變化及閘極氧化層缺陷形成的數量。我們也發現閘極氧化層缺陷的形成、界面品質的劣化與晶片因應力記憶技術所造成的彎曲有關。藉由最佳化的應力記憶技術製程，元件將能達到較高的遷移率、電晶體的轉移電導，同時維持相同的短通道特性。最後，在應變矽晶片製作過程中，應避免晶片的彎曲，以盡量減少閘極邊緣的破壞、閘

極氧化層缺陷的形成，以滿足高品質電路生產的要求。

第六章裡，我們研究單軸應變力對奈米製程之 N 型金氧半場效電晶體的背向散射效應。背向散射特性是藉由電晶體的臨界電壓與導通電流和溫度關聯性所萃取得到。通過對比測量結果，我們證明單軸應變可以減少 N 型金氧半場效電晶體通道的背向散射。此外，單軸應變也降低了載子的有效質量，並提高了熱注射速度，效率和彈道傳輸效率。這些現象隨著閘極長度的減少變得更加明顯。因此，單軸應變的優勢預期在高度微縮的電晶體將會保持，甚至可以延伸其應用範圍到彈道傳輸的電晶體上。

在論文最後的第七章裡，摘要幾個關鍵結果，並對未來方向做一些建議。



Study of Stress Memorization Technique on the Characteristics of Nanoscale nMOS Transistors

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ABSTRACT

As the scaling of CMOS structure reaches its fundamental limits, the carrier mobility enhancement has been intensively pursued by introducing strain in the channel region. The uniaxial strain can be realized by stress memorization technique (SMT) fabrication process. After the gate polysilicon is amorphized by implantation, the transistor is then capped with SMT nitride. During the source/drain dopant activation annealing, the recrystallization of amorphous silicon would generate compressive vertical stress to the channel underneath. Such strain can be used to boost electron mobility for nFET device enhancement.

In Chapter 1, the overview of our study and motivations of this thesis are

described.

Chapter 2 gives an introduction of strain silicon theory upon the change of electronic and hole band structures. Furthermore, a brief summary of the evolution of strained silicon technology is outlined. Modern strain silicon fabrication methods such as substrate-induced strain and process-induced strain are also described.

After reviewing the basic concepts of the strain silicon theory, the process and literature overview of SMT are discussed in Chapter 3. The SMT effect and its influence on nFET and pFET device performance are summarized, with an emphasis on the SMT strain formation mechanisms for electron carrier mobility enhancement.

In Chapter 4, we've realized the fabrication of SMT strained nFET on the National Nano Device Laboratories (NDL) 6" wafers using conventional nitride as the SMT strain cap layer. The introduction of the SMT process for the as-fabricated nFET device can improve its transconductance and short-channel effects (SCE). N-type dopant diffusion retarded by the SMT-strain is explained by the point defect engineering.

In Chapter 5, we've demonstrated the SMT fabrication process and analyzed the nFET electrical characteristics with different SMT cap nitride processes again on the

6” wafers. Both PE-SiN and LP-SiN were investigated. Basic physical and chemical properties of nitride films, such as thickness, shrinkage, bonding composition change, and stress change upon S/D activation annealing are also characterized. The nFET electrical performance and interfacial quality degradation have been well correlated to the effect of the wafer bowing exerted by SMT cap nitride. This suggests that wafer bowing induced by strain silicon process should be carefully controlled in order to minimize gate edge damage for high-yield production.

In Chapter 6, the channel backscattering characteristics for strained and non-strained nFETs using the temperature-dependent extraction method are examined for highly scaled nFET. We demonstrate that nFET channel backscattering can be effectively reduced by the uniaxial strain. Furthermore, the strain-reduced conductivity effective mass also increases the thermal injection velocity and ballistic efficiency. Such phenomenon becomes more appreciable as the gate length is reduced. It is thus expected that the performance enhancement induced by the uniaxial strain will be maintained even in the ballistic transport regime with very short gate length.

Finally, conclusions of this dissertation and recommendation for further research are presented in Chapter 7.

誌謝

首先我要向我的指導教授 雷添福博士致上最高的敬意，感謝他在學業研究與生活上給我的指導與鼓勵。我也要感謝另一位指導教授 侯拓宏教授的指導，令我獲益良多。另外也要謝謝公司同仁及主管 陳建豪博士，廖泓漢博士，李啟弘博士，李資良博士，章勳明博士的幫忙和對吾人在職進修的支持。

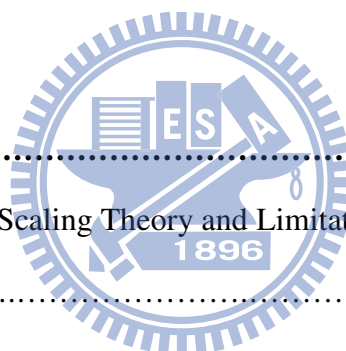
由衷感謝國家奈米元件實驗室提供了良好的研究環境及資源，使我能順利進行研究。另外，特別感謝奈米元件實驗室的製作與製程整合組提供在實驗上的設計討論，及徐台鳳小姐、蔣秋芬小姐及薛富國先生、巫振榮先生和其他工程師們在設備儀器技術上的協助。若沒有你們的大力幫忙，我無法順利地完成此論文，在此獻上我的謝意。也感謝實驗室裡一起研究的夥伴，郭伯儀、黃俊嘉、林冠良和羅文呈等人的協助。

最後，謝謝我親愛的父親、母親、妻子、兩位弟弟與我可愛的幼子。感謝父、母親對我的養育、教育之恩。感謝太太對我的付出，感謝我的家人們在我需要溫暖時給我照顧，謝謝你們陪我一路走過這漫長的求學生涯，僅此論文獻給所有關心我的家人及朋友。謝謝大家！

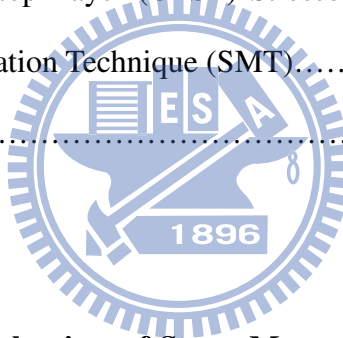
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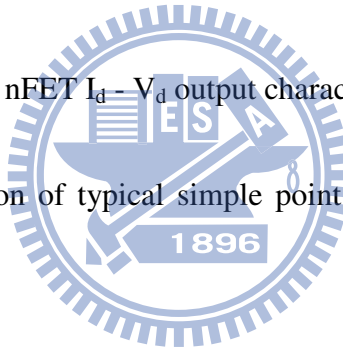


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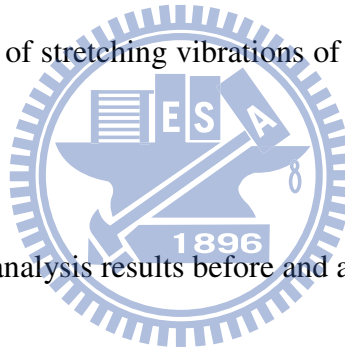


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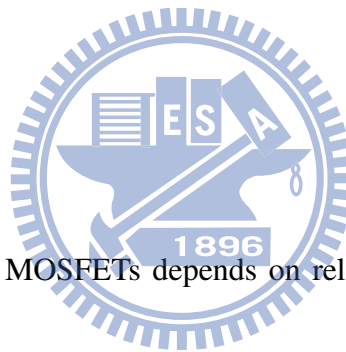


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