國立交通大學

電控工程研究所

博 士 論 文

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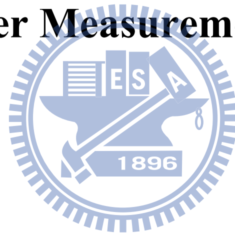
Built-In Self-Tests for Jitter Measurement of Phase-Locked Loops



研 究 生： 徐仁乾

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中 華 民 國 九 十 九 年 五 月

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研 究 生：徐仁乾　　Student：Jen-Chien Hsu

指導教授：蘇朝琴　　Advisor：Chau-Chin Su

國 立 交 通 大 學

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國立交通大學電控工程研究所博士班

摘要

資料傳輸之品質受到時脈抖動之影響甚巨，然而針對時脈抖動的量產測試卻因成本過高而難以實現，因此，時脈抖動的內建自我測試電路成為量產測試的一個解決方案。時脈抖動的內建自我測試電路一般皆透過時間對數位轉換器來完成，將時脈抖動轉換成為數位訊號，以低速數位訊號的方式提供量測機台進行量測，因此一個良好的時間數位轉換器是內建自我測試的重要元件。在本論文中，我們提出了三種不同的時間對數位轉換器以及內建自我測試電路，第一種是針對電荷幫浦式鎖相迴路的時脈抖動量測所設計，它使用了新穎的高解析度時間對數位轉換器，可將受測電路本身的元件重複利用做為時間對數位轉換器的一部份，因此縮小了額外的電路面積。量測結果顯示其量測解析度可以達約兆分之一秒，而量測誤差小於百分之二十。第二種內建自我測試電路是針對展頻時脈鎖相迴路所設計，它可分離展頻時脈的低頻調變訊號以及高頻的時脈抖動訊號，同時建立一時脈抖動的估算方式，以驗證此電路的可行性。我們實做了一個時脈頻率每秒十二億次、十個相位的鎖相迴路以及時脈抖動量測電路，並比對量測結果與估算值，顯示量測誤差低於0.0026個單位區間。第三種內建自我測試電路可量測資料與時脈回復電路的時脈抖動，並依據所量得之結果，估算資料之位元誤差率，這種內建自我測試電路不需高解析度的延遲訊號線即可達到高精準度的量測結果，它利用校正的機制和曲線對應的方式獲得高精準度。校正的機制是將壓控震盪器切換至自由震盪模式，以機率統計的方式獲得時間對數位轉換器中延遲緩衝器的延遲時間。此內建自我測試電路還可透過曲線對應的方式分離不同類別的時脈抖動，以預估在位元誤差率為兆分之一的系統規格上的總時脈抖動大小。

Built-In Self-Tests for Jitter Measurement of Phase-Locked Loops

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ABSTRACT

Signal quality of data transmission is significantly affected by clock jitter of Phase-Locked Loops (PLLs). However, production test for clock jitters is too expensive to implement. Built-In Self-Test (BIST) for clock jitter measurement becomes an alternative solution for production test. Basically, BIST methodologies are based on Time-to-Digital Converters (TDCs) which convert phase differences of a tested clock and a reference clock into low-speed digital signals for test equipments to measure. In this thesis, we proposed three kinds of TDCs and BIST circuits for different applications. The first one is designed for measuring clock jitter of charge-pump PLLs. The BIST is based on a novel high resolution TDC. Small area overhead is achieved by reusing the Voltage-Controlled Oscillator (VCO) and loop filter of the tested PLL as part of the TDC. The experiment result shows that the resolution is about one pico-second and the measurement error is smaller than 20%. The second BIST circuit is proposed for measuring timing jitter of Spread-Spectrum Clocks (SSCs). The BIST circuit can separate low-frequency phase drifting caused by frequency modulation and high-frequency jitter. Because of lack of dedicated instruments for SSC timing jitter measurement, a jitter estimation method is also developed for validating the feasibility of the BIST circuit. A 1.2GHz 10-phase Spread-Spectrum Clock Generator with a jitter measurement circuit is designed and fabricated. The experimental results show that the proposed built-in measurement approach has an error of less than 0.0026UI. The third BIST circuit is developed for testing the relative timing jitter of data and clock recovery circuits. This BIST circuit doesn't need a high resolution delay line to achieve high accuracy measurement result, but uses calibration and curve-fitting algorithms. Calibration is done by switching the VCO of the tested PLL into free-running mode and using statistical theories to acquire accurate delay time of the delay buffers in the TDC. This BIST circuit also separates deterministic jitter and random jitter by adopting the bathtub curve-fitting algorithm and estimates total jitter at bit-error rate=10^{-12} level.

誌謝

首先我要感謝法輪大法（法輪功）讓我恢復健康的身體。我在就讀研究所前，不幸罹患一種稱為「僵直性脊椎炎」的免疫系統疾病，這種重大疾病一旦發病即可免除兵役，且發展到後來必須長期靠類固醇藥物控制，嚴重時將長期臥病在床。所幸我在發病初期，就開始接觸並修煉法輪大法。法輪大法是一種「性命雙修」的功法，除了強調心性的提高外，還可以使修煉者身體得到健康。因為學煉法輪大法，我的身體漸漸得到康復，所以如今才能過著正常人的生活，且順利完成研究所的學業。

接著我要感謝指導老師蘇朝琴教授，在跟隨蘇老師做研究的過程中，我學習到一種做學問的方式，蘇老師要求我們凡是從基本的物理意義上去看問題，不要被複雜的公式所迷惑。養成這種習慣之後，往往對問題的認識能更為深入。還有蘇老師常說：「模擬軟體是用來驗證自己的想法的，並不是用來指導做研究的。」我覺得這點也讓我受益良多，所以使用模擬軟體前，我都會先想想自己能否預期將有什麼樣的模擬結果。

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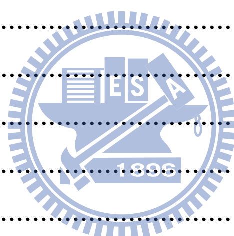

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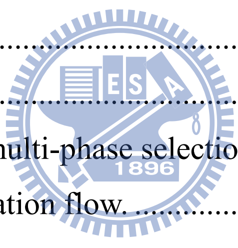

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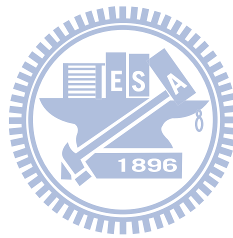

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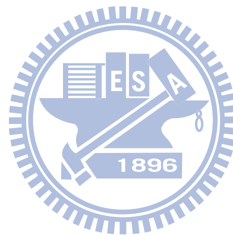


Chapter 1

Introduction

1.1. Jitter Definition

Phase-Locked Loops (PLLs) are extensively employed as clocking signal sources in digital and mixed-signal circuits. In high speed link applications, jitter represents the problem of data uncertainty. Thus, clock jitter of PLLs is one of the most important properties to be measured.

Clock jitter is defined as the timing deviation of the tested clock from the ideal clock. Jitter can be categorized into several types according to different definitions. Fig. 1 illustrates three jitter definitions: period jitter, cycle-to-cycle jitter, and timing jitter. Period jitter is defined as the difference between the tested clock period and the reference clock period. Cycle-to-cycle jitter is defined as the difference between the current period and the previous one of the tested clock. Timing jitter, also known as long-term jitter, is the timing difference between the tested clock edge and reference clock edge. In general, timing jitter is more useful for Bit-Error Rate (BER) estimation because a bit-error occurs when the

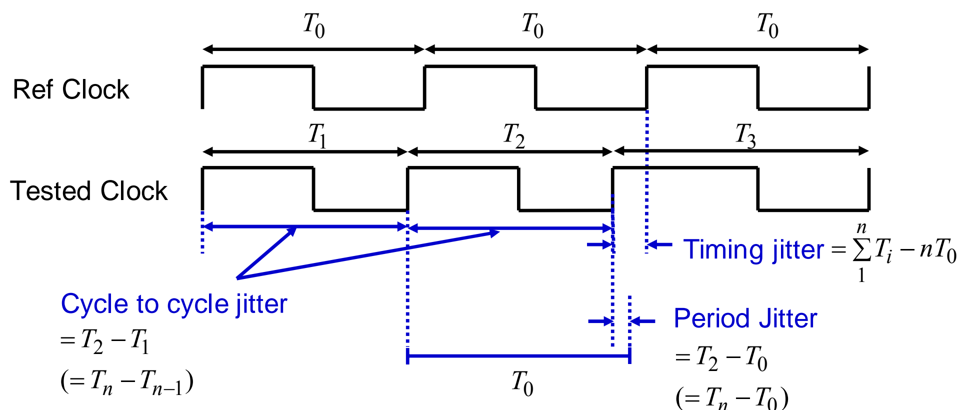


Fig. 1 Jitter definitions.

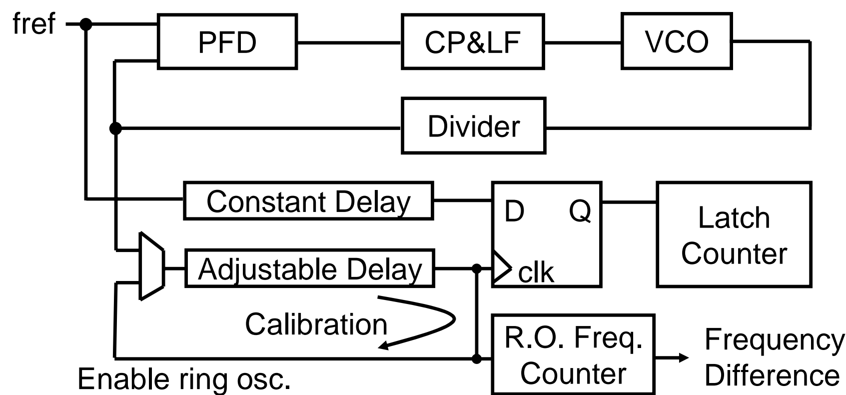


Fig. 2 Delay line TDC.

timing of the tested clock edge deviates from its ideal position for an intolerable magnitude.

Jitter can also be categorized by its noise sources such as Deterministic Jitter (DJ) and Random Jitter (RJ). The amplitude of DJ is bounded, since the noise sources are the Duty-Cycle Distortion (DCD), Inter-Symbol Interference (ISI), switching noise of the power supply, and other noise sources whose values can be estimated. RJ is unbounded, since the noise sources are thermal noise, flicker noise, and other noises induced by electronic movements. Total Jitter (TJ) is the combination of DJ and RJ. Besides, jitter is usually presented in two statistical forms: RMS jitter is the root-means square values of the jitter, and peak-to-peak jitter is the maximal value of the jitter.

1.2. BIST for Measuring PLL Jitter

As clocks speeds reach GHz in recent years, measuring clock jitter using external high speed test equipments becomes increasingly expensive. To reduce testing cost, a Built-In Self-Test (BIST) method is considered as a feasible alternative. The most common method of BIST is based on Time-to-Digital Converters (TDCs). Several state-of-the-arts of BIST and TDC approaches are introduced as follows:

1. Delay line [1]-[10]: The method is based on a delay line to obtain a cumulative

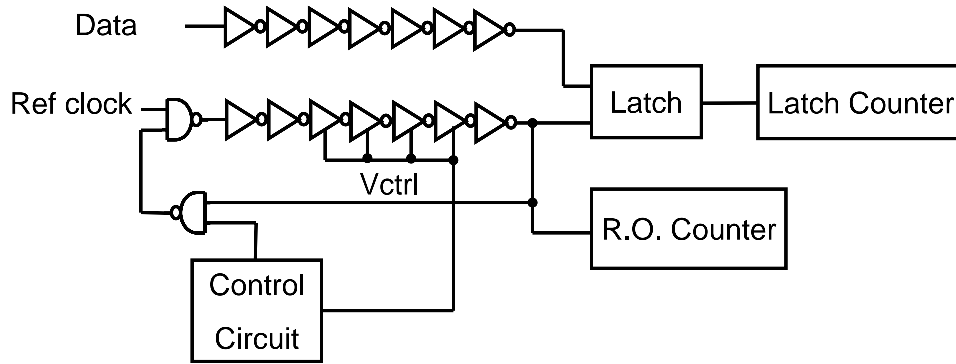


Fig. 3 Delay line with fine resolution.

distribution function of jitter, as shown in Fig. 2. This is the simplest and straightforward method to implement TDCs. By adjusting the delay line, the timing differences of the reference and tested clock edges are measured. The calibration of the delay buffer is done by connecting two ends of the delay buffer to form an oscillator, so the delay time can be estimated based on its oscillation frequency. Various calibration techniques are also developed to improve the accuracy of the delay-line-based approaches [11]-[13].

A digitally controlled delay line has a coarse resolution of about one gate delay. Therefore, a voltage-controlled delay line is used to improve the delay line resolution [7]. As shown in Fig. 3. The resolution can be as good as sub-picosecond using accurate analog bias voltage.

2. Vernier Delay Line [14]-[20]: The Vernier Delay Line is also developed to increase

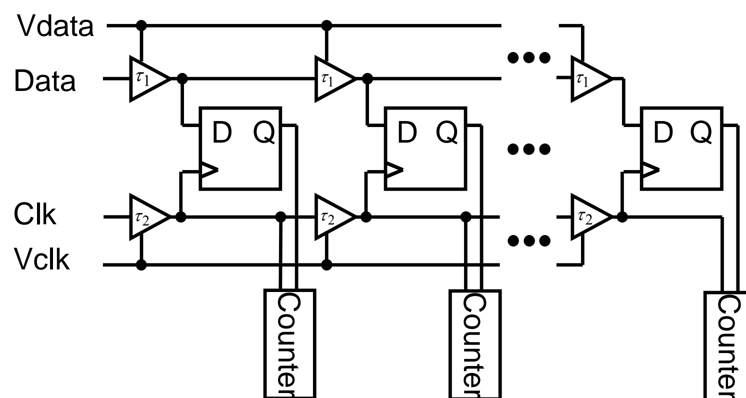


Fig. 4 Vernier Delay Line.

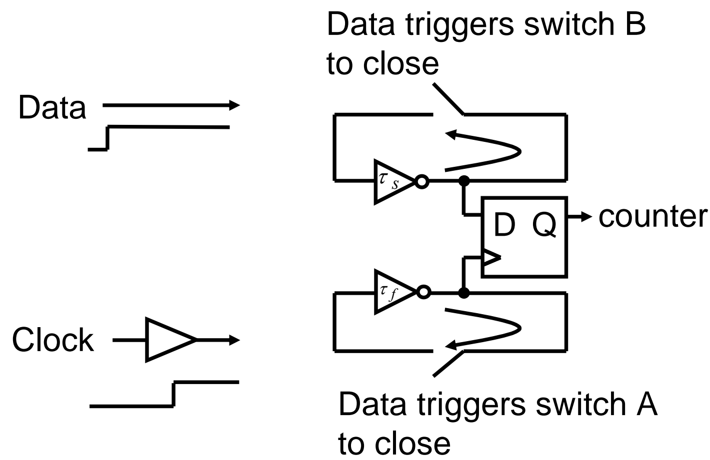


Fig. 5 Ring Type Vernier Delay Line.

the TDC resolution. As shown in Fig. 4, the resolution is determined by the delay difference of two delay buffers; thus the resolution is improved. However, the area overhead is large and accurate analog bias voltages are also required.

3. Ring Type Vernier Delay Line [21]-[25]: The Ring Type Vernier Delay Line (also called Component-Invariant Vernier Delay Line) is developed to solve the problems of mismatch and large area overhead of the Vernier Delay Line. As shown in Fig. 5, a delay buffer is connected as a ring oscillator to replace all the other delay buffers of the Vernier Delay Line. Both Vernier Delay Line and Ring Type Vernier Delay Line require an additional Digital-to-Analog Converter (DAC) to generate accurate analog control voltages to fine-tune the delay time of each delay line.

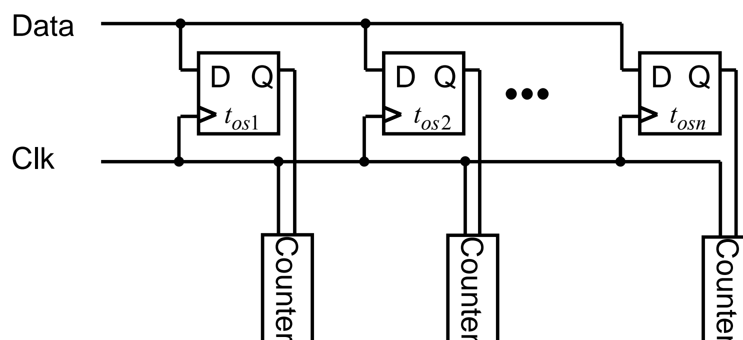


Fig. 6 Sampling Offset TDC.

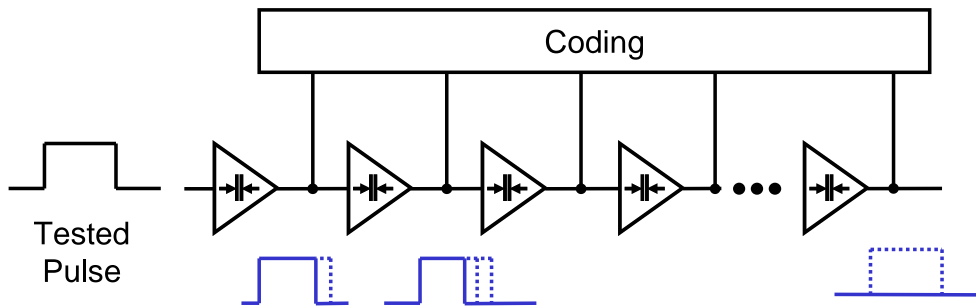


Fig. 7 Pulse-Shrinking Delay Line.

4. Sampling Offset TDC [26]-[28]: Sampling Offset TDC uses non-ideal DFFs as comparators to produce different sampling time offset to mimic the function of Vernier Delay Lines. As shown in Fig. 6, the sampling time of each DFF is different due to different sizing of the transistors of the DFF. The merit of this approach is that delay buffers and its analog bias voltages are not needed. However, each DFF requires careful sizing and the linearity is not guaranteed.

5. Pulse-Shrinking Delay Line [29]: As shown in Fig. 7, Pulse-Shrinking Delay Line takes advantage of the difference between the propagation delay of the charge and discharge paths of the delay buffers to quantify timing jitter, so the resolution is smaller than one gate delay. However, the propagation delay of the charge and discharge paths should be carefully designed since those paths are sensitive to process variation.

6. Ring Type Pulse-Shrinking Delay Line [30][31]: As shown in Fig. 8, the Ring Type Pulse-Shrinking Delay Line (also called Cyclic Pulse Width Modulator) uses the Pulse-Shrinking Delay Element to build a cyclic loop, so the area overhead is smaller than

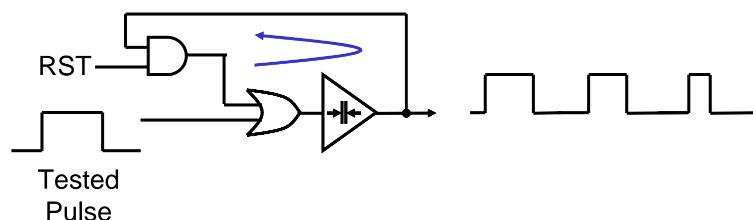


Fig. 8 Pulse-Shrinking Delay Line Ring Type.

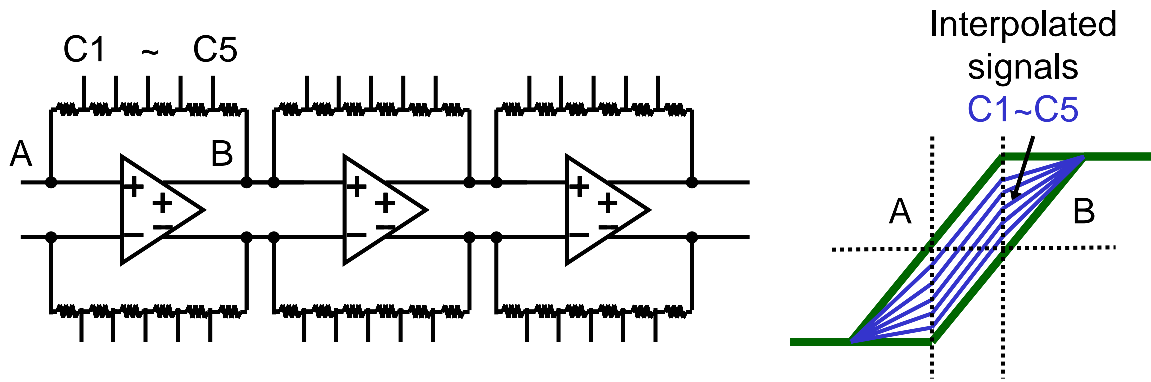


Fig. 9 Local Passive Interpolation.

that of the Pulse-Shrinking Delay Line.

7. Local Passive Interpolation [32][33]: The coarse resolution of the delay line approach is subdivided by a passive interpolation technique. As shown in Fig. 9, this method uses passive components for phase interpolation and provides a time domain resolution of 4.7ps. This approach has the merit of monotonic phases, but the shortcoming is that the layout of the passive components should be carefully designed, and more comparators and counters are needed.

8. Analog-to-Digital Converter [34]: As shown in Fig. 10, the Analog-to-Digital Converter (ADC) converts clock jitter into digital codes by applying a sine wave to the ADC input and the tested signal to the ADC clocking input. This approach exhibits high resolution and short test time, but it requires the generation of a sinusoidal waveform with high spectral purity and requires the use of a high-performance ADC.

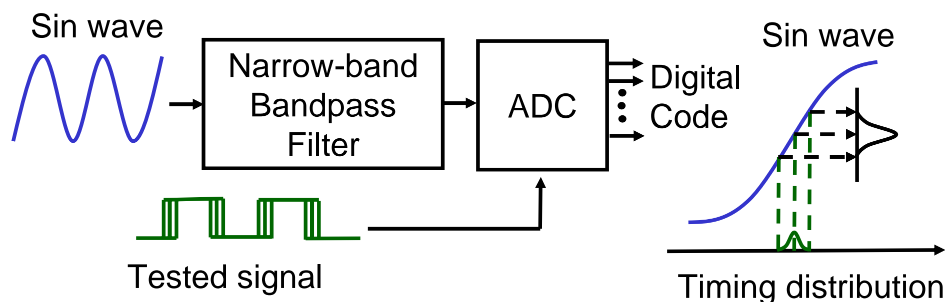


Fig. 10 Analog-to-Digital Converter for Jitter Measurement.

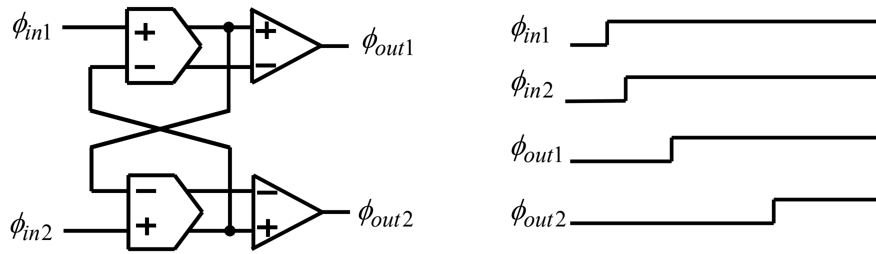


Fig. 11 Time amplifier.

9. Time amplifier [35]-[39]: As shown in Fig. 11, the method is developed to improve the resolution of TDC by adding a time amplifier to the input of poor-resolution TDCs. This approach can enhance the resolution of TDCs to 2 pico-second [35][36]. Another type of time amplifier is also presented in [37]. Fig. 12 shows dual-slope ADC designed for amplifying the pulse width of the tested signal. The shortcoming of these time amplifiers is that they are sensitive to noise because of their gentle signal slopes.

10. Time-to-Voltage Converter [40]-[46]: The Time-to-Voltage Converter (TVC) approach converts phase difference into voltage using a charging pump and a capacitor. The voltage is further converted into a digital code using a specially designed ADC. As shown in Fig. 13, this approach uses its analog characteristics to achieve high resolution [40]. However, the shortcomings of this approach are that the measurement sensitivity of the TDC is limited by the dead-zone of the phase detector, and the constant phase error between the reference clock and the tested clock induces measurement error. Additionally,

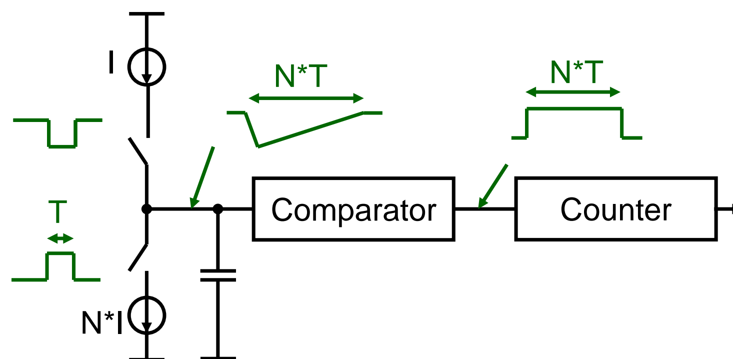


Fig. 12 Dual-slope ADC for time amplifying.

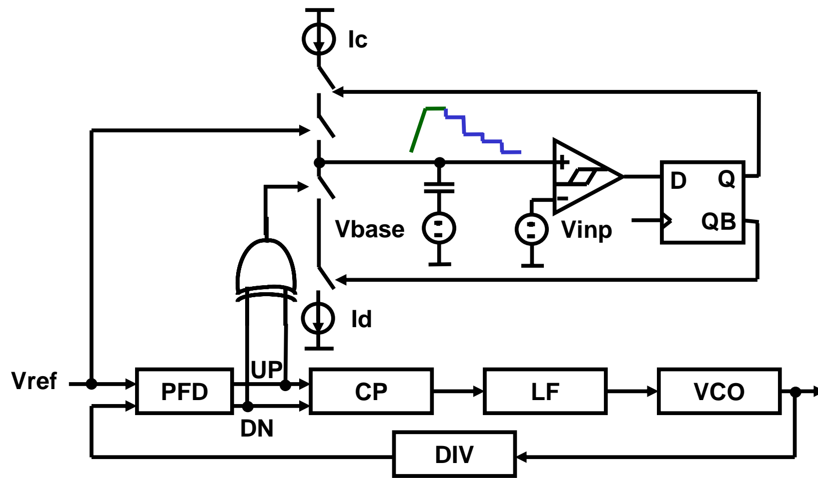


Fig. 13 Time-to-Voltage Converter for average jitter measurement.

the BIST circuit measures average jitter but not RMS jitter. Fig. 14 shows another TVC with a flash ADC converting voltage signals into digital codes. This approach has fast conversion speed but large area overhead is a problem due to the need of a high resolution flash ADC.

11. Hybrid of TVC and delay line [47]-[49]: This approach adopts both delay line and TVC to perform a jitter measurement without a reference clock. As shown in Fig. 15, it uses a delay line to measure the period jitter and then uses a TVC to accumulate the period jitter to have timing jitter. Although some similar works for omitting reference clocks have been done [3][8][9][20][25], the novelty of this hybrid approach is that it can measure timing jitter instead of period jitter, even without a reference clock. However, a very accurate delay buffer to extract period jitter is needed.

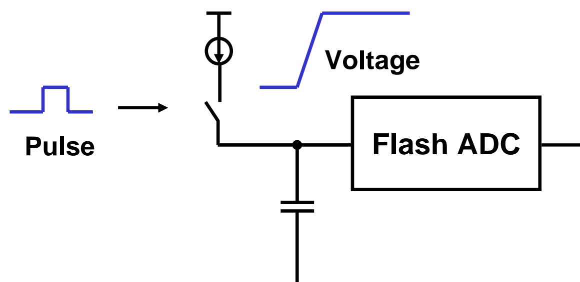


Fig. 14 Time-to-Voltage Converter with flash ADC.

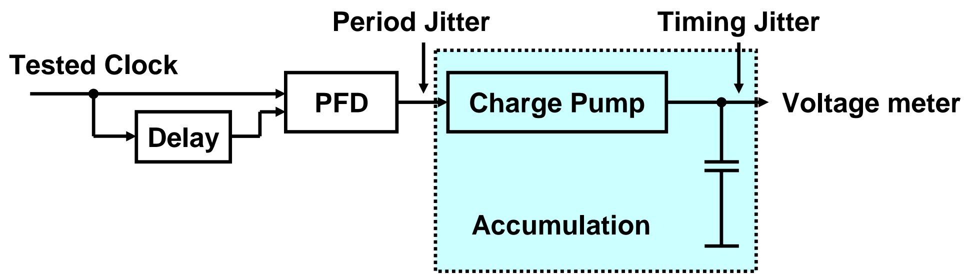


Fig. 15 Hybrid of TVC and delay line.

12. Under-sampling-based technique [50]-[53]: As shown in Fig. 16, the tested clock is sampled by a slightly lower frequency clock, so a phase resolution is determined by the frequency difference between the tested clock and sampling clock. The advantage of this approach is that only a D flip-flop (DFF) is needed, so it can be synthesizable, but the disadvantage is that it requires two oscillators on PCB board which are fine-tuned to have oscillation frequencies with very slight difference.

Because the BIST approach with TVC has the potential of high resolution, but has large hardware overhead. The fist part of this work tries to modify the TVC approach by developing a high-resolution and small-area circuit. A high-resolution TVC is achieved by adopting a voltage-to-frequency conversion, i.e. a Voltage-Controlled Oscillator (VCO). Small area overhead is achieved by using the VCO of the tested circuit as part of the BIST circuit.

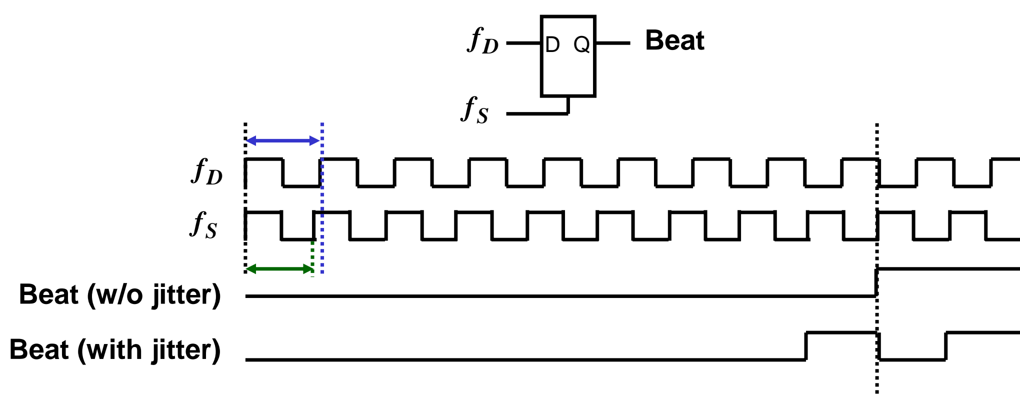


Fig. 16 Under-sampling-based technique.

1.3. BIST for Measuring SSC Jitter

The second part of this work is for jitter measurement of Spread-Spectrum Clocks (SSCs). Conventionally, BIST circuits for jitter measurement use Time-to-Digital converters (TDCs) to compare the phase difference between a generated clock and reference clock. The resolution of TDCs determines the accuracy of jitter measurement results. Unfortunately, a Spread-Spectrum Clock (SSC) has a frequency deviation due to a predefined modulation profile that attenuates peak power, as shown in Fig. 17. The phase variation of the SSC includes jitter and the phase drifting resulting from the designed frequency deviation. Separating those by using conventional TDC approaches or external instruments is difficult.

Although the phase drifting caused by the frequency modulation is a deterministic jitter, and the deterministic jitter and random jitter separation algorithm [54] can be used to separate jitter. However, if a phase drifting is larger than 1UI, the histogram becomes flat and meaningless. It happens for most SSCs. Furthermore, even if the deterministic jitter can be separated from the random jitter, the deterministic jitter induced by the tested Phase-Locked Loop (PLL) and the SSC phase drifting cannot be separated because they all are deterministic jitter. More importantly, the SSC phase drifting is a low-frequency signal that is not crucial for receivers to recover the data, but other high-frequency deterministic

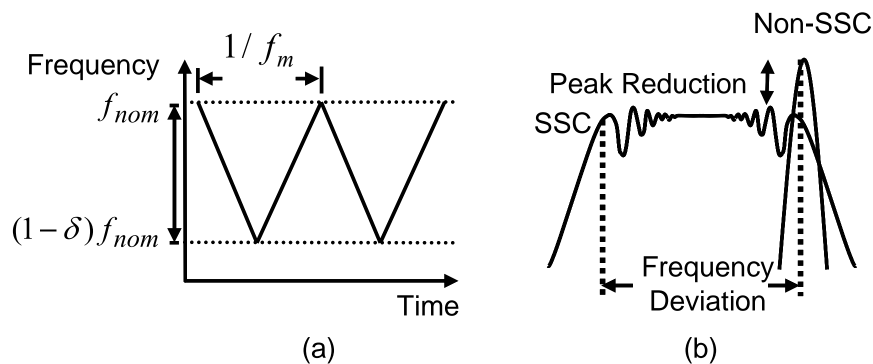


Fig. 17 (a) Modulation profile. (b) Power spectral density of Spread-Spectrum Clock.

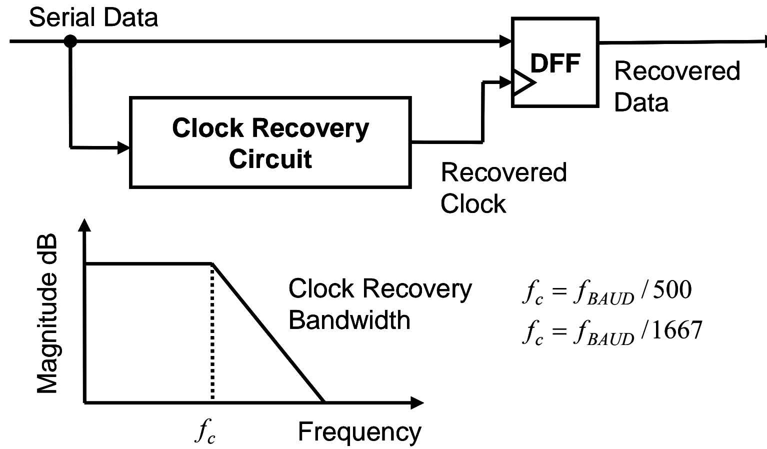


Fig. 18 Jitter measurement methodology.

jitter is important, so separating different types of deterministic jitter is necessary.

Timing jitter of SSCs cannot be measured using traditional approaches, thus spectrum analyzers are frequently used to measure the power spectrum of SSCs for roughly estimating the signal quality. The self-trigger function of oscilloscopes is typically utilized to measure period jitter. However, period jitter is not useful for estimating BER.

Because the timing jitter is more appropriate for BER estimation than the period jitter [57]-[60]. Serial ATA (SATA) develops a timing jitter measurement methodology [55] as shown in Fig. 18. Jitter is defined as the time difference between a recovered clock and a data edge. The clock recovery circuit has a low-pass transfer function with a corner frequency of $f_{BAUD}/500$ or $f_{BAUD}/1667$ depending on different applications, where f_{BAUD} is the nominal rate of data through the channel. However, the jitter includes the transmitted jitter and the jitter induced by the clock recovery circuit if an ideal recovery circuit is not used. Moreover, an additional clock recovery circuit is needed when using this methodology.

In the second part of this work, a BIST methodology for measuring timing jitter and the modulation profile of SSCs is proposed. The measured results are validated by the

estimation based on the measured results using external instruments.

1.4. BIST for Measuring CDR Jitter

The third part of this work is to measure the TJ and BER of the clock and data recovery circuits using an accurate BIST circuit and jitter decomposition algorithm. Conventionally, oscilloscopes and time interval analyzers provide some convenient jitter decomposition algorithms to estimate BER. In this work, a combination of jitter decomposition and jitter measurement is proposed to implement a BER testing by BIST circuits. A calibration method is also proposed to improve the accuracy of the TDC.

Most state-of-the-arts of the jitter BISTs are measuring the clock jitter and jitter histogram. In this work, a method is proposed to measure relative timing jitter between received NRZ data and recovered clock of CDR and then estimate the peak-to-peak jitter at bit error rate (BER) of 10^{-12} level. Fig. 19 and Fig. 20 show the application of the BIST. The relative timing jitter between the received data and recovered clock of CDR represents the timing performance of the communication system, including transmitter, channel, and

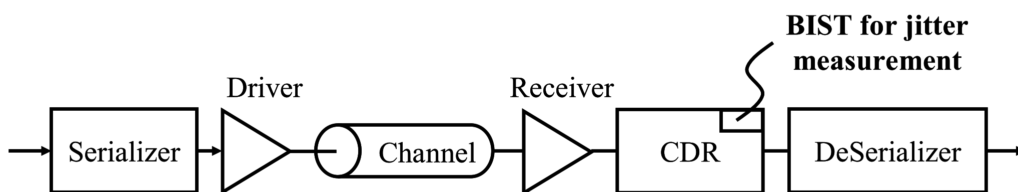


Fig. 19 Tranceiver architecture and BIST.

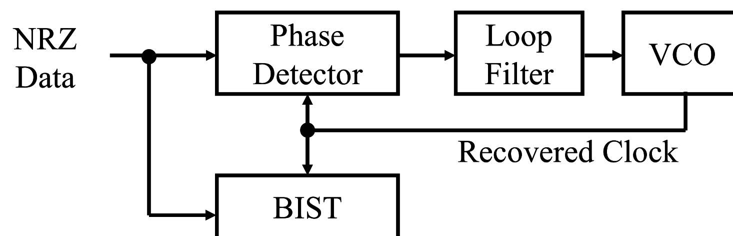


Fig. 20 Clock Recovery circuit and BIST.

receiver. Thus, the relative timing jitter helps to estimate the BER [56].

Because directly measuring the peak-to-peak jitter at the 10^{-12} BER level consumes a lot of time, the techniques of jitter decomposition are commonly used. TJ in a typical system is the combination of DJ and RJ. DJ has a non-Gaussian PDF and bounded peak-to-peak amplitude. RJ is characterized by a Gaussian distribution and assumed to be unbounded.

Some techniques for decomposing the TJ are presented in [54]. For example, Oscilloscopes and Time Interval Analyzers provide some convenient jitter decomposition algorithm, such as TailFit algorithm created by Wavecrest. A bit error rate tester (BERT) utilizes scan/bathtub curve for jitter decomposition, as shown in Fig. 21.

In this work, a new definition of a bit-error is given and the data provided for bathtub curve-fitting is obtained by BIST circuit instead of BER tester. Additionally, the hardware overhead in this work is small because only several data points of jitter magnitude is measured instead of a jitter histogram, which needs a high resolution TDC for depicting the whole scale of the jitter amplitude.

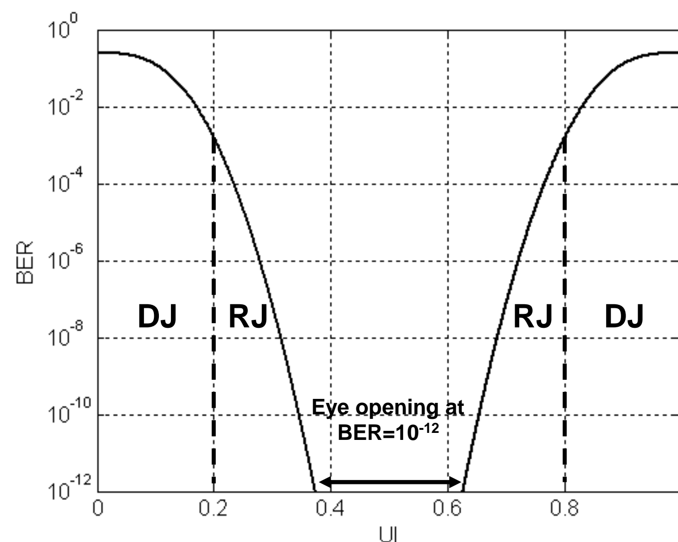
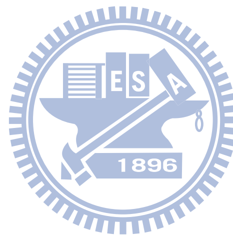


Fig. 21 Bathtub curve characterized by the jitter of RJ=0.2UI and DJ=0.04UI

1.5. Organization of the Dissertation

The dissertation is organized as follows. Chapter 1 introduces the motivation of this work and the dissertation organization. Chapter 2 presents the BIST circuit for measuring jitter of charge-pump PLLs. Chapter 3 presents the BIST circuit for measuring timing jitter of Spread-Spectrum Clock Generators (SSCGs) and the jitter estimation method for validating the BIST circuit. Chapter 4 describes the BER estimation method using a BIST circuit and the calibration method to improve the accuracy of the BIST circuit. Chapter 5 concludes this work.



Chapter 2

BIST for Charge-Pump Phase-Locked Loops

2.1. Time-to-Digital Converter

The use of TDC to measure jitter is the concept that underlies BIST circuits. TDC detects each phase difference between the reference clock and the tested clock to obtain the jitter histogram. As shown in Fig. 22, the proposed TDC is composed of Phase-Frequency Detector (PFD), Charge Pump (CP), Capacitor (C), VCO, Divider (DIV) and Counter.

Two clocks CLK1 and CLK2 with a phase difference, ΔT, is input to PFD. The phase difference is detected using PFD only once and the PFD is disabled before the next clock edge arrives. CP and Capacitor convert the phase difference into a voltage variation ΔV.

$$\Delta V = \frac{I_p}{C} \Delta T, \tag{1}$$

where I_p is the current magnitude of CP and C is the capacitance of Capacitor.

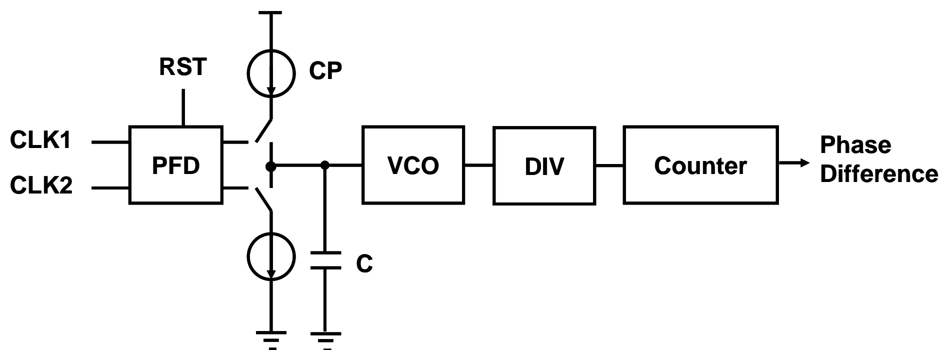


Fig. 22 Time-to-Digital Converter.

The frequency of VCO is changed from f_{VCO0} to f_{VCO1}. The frequency variation Δf of the DIV output is

$$\Delta f = \frac{f_{VCO1} - f_{VCO0}}{N} = \frac{K_{VCO}\Delta V}{N}, \tag{2}$$

where N is the division ratio of DIV and K_{VCO} is the gain of VCO.

DIV slows down the clock frequency of VCO N times for the low-speed counter to count. Counter counts the DIV clock edges in time, T_C, to measure the frequency. Counter value, N_C, and DIV frequency, f_{DIV}, are related as follows.

$$N_C = f_{DIV} T_C. \tag{3}$$

If N_{C1} is the count in T_C when the DIV frequency is f_{DIV1}, and N_{C0} is the count when the DIV frequency is f_{DIV0}, then the frequency variation and count difference, ΔN, are related as follows.

$$\Delta N = N_{C1} - N_{C0} = (f_{DIV1} - f_{DIV0})T_C = \Delta f T_C. \tag{4}$$

Equations (1), (2) and (4) yield the relationship between the count difference, ΔN, and the phase difference, ΔT.

$$\Delta T = \frac{NC}{K_{VCO} I_P T_C} \Delta N. \tag{5}$$

The count difference yields the phase difference. One count difference denotes that a phase difference of k_{RES} has been detected, where the coefficient, k_{RES}, represents the measurement resolution.

$$k_{RES} = \frac{\Delta T}{\Delta N} = \frac{NC}{K_{VCO} I_P T_C} \text{(ps/count)}. \tag{6}$$

Due to the process variation, the gain of VCO, current magnitude of CP and capacitance of the capacitors of the fabricated chip will not be as the same as the ones from

the simulation results. To calibrate the TDC and obtain the accurate coefficient, k_{RES}, of the fabricated chip, a pulse with the known pulse width ΔT is input to CP. The count difference ΔN is obtained and the accurate coefficient is calculated.

The proposed TDC measures small phase differences between two clocks because the dead-zone of PFD is zero. The commonly-used zero dead-zone PFD is implemented using two edge-triggered, resettable D flipflops. The UP and DN signals of the PFD are simultaneously high for a short time. Even if the phase difference of two inputs are nearly zero, the UP and DN signals still have short pulses to turn on the transistors of CP. The difference between their pulse widths represents the phase difference. Thus zero dead-zone is achieved.

A constant phase offset between CLK1 and CLK2 must be considered. If there is current mismatch between the charging and discharging path of CP, the PLL will compensate the mismatch automatically by keeping the pulse widths of these two short pulses different, so the constant phase offset between CLKA and CLKB occurs. The phase offset can also be measured and separated from the jitter by observing the histogram of the phase differences. The mean in the histogram represents the phase offset error and the variance represents the jitter.

The parameters of CP and Capacitor should be carefully designed to have a proper detection range. If the current is too large and the capacitance is too small, the voltage variation will fall out of the VCO control voltage range. If the current is too small and the capacitance is too large, then the voltage variation will be too small and then the noise on the node of Capacitor will induce more measurement error.

The value, T_C, is the parameter that determines the measurement resolution. For longer T_C, the measurement resolution is higher, but the effect of the leakage current increases and the test time also increases.

Capacitor and VCO have a large area and dominate the area overhead of the BIST circuit. Fortunately, the loop filter, the VCO and the divider of the tested PLL can be adopted as part of the TDC. Therefore, the area overhead is reduced. PFD and Counter only comprise several logic gates; therefore, the total area is small.

One noise source may deteriorate the accuracy of this approach. The TDC utilizes the VCO and the loop filter of the tested PLL as part of the circuit, but the initial value of the VCO control voltage is not constant due to power supply noise and a PLL tracking ability. Fig. 23 shows the timing diagram of a VCO in a PLL and the noise of the power supply. Assume the frequency of the noise is much lower than the loop bandwidth of the PLL. A phenomenon is observed that the voltage of the loop filter is varying in the opposite phase of the power supply noise to cancel the effect of the noise and keeping the frequency of VCO constant. It is reasonable because the frequency of the supply noise is much lower than the loop bandwidth so the PLL can keep the frequency of the VCO constant and lock the phase of the reference clock. If the loop of PLL is opened at a particular time, the

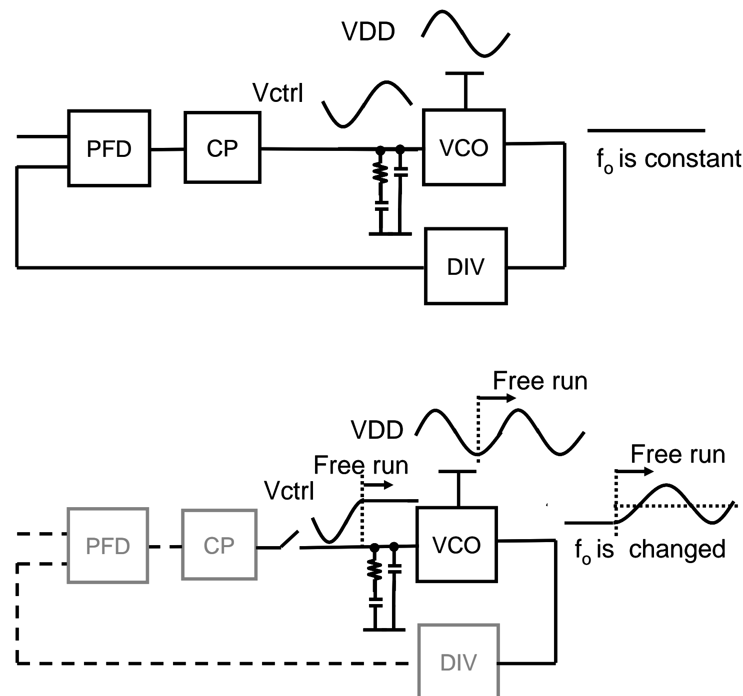


Fig. 23 Initial control voltage of VCO.

voltage of the loop filter is kept in a particular value by the capacitors of the loop filter at that moment. This value becomes the initial value of the VCO control voltage of the TDC. However, this value is determined by the power supply noise voltage at the moment when the loop is opened, so the value is not predictable.

The frequency deviation of the VCO caused by the noise is derived as the power supply noise multiplying the VCO power supply gain, K_{VCO2}. The VCO power supply gain is defined as VCO frequency variation over power supply variation. For example, the peak value of power supply noise is 2mV and the VCO power supply gain is 200MHz/V. The maximum frequency deviation of the VCO is 0.4MHz and the maximum frequency deviation of the divider output is 25kHz, if the division ratio is 16. After counting time 200μs, the count of the counter deviates from its ideal value for $25k \cdot 200\mu = 5$. Then 5 is multiplied by the measurement resolution of 1ps/count to be 5ps. So the measurement error is 5ps. The measurement error, ΔT_1, is derived as follows.

$$\Delta T_1 = V_n K_{VCO2} T_C k_{RES} = \frac{V_n K_{VCO2} NC}{K_{VCO} I_P}, \tag{7}$$

where V_n is the power supply noise.

The only parameter which can be adjusted to suppress the measurement error is the current of CP, so the current should be designed as large as possible. If the complete avoidance of this noise source is desired, an additional capacitor instead of the loop filter should be used to generate constant initial control voltage of VCO.

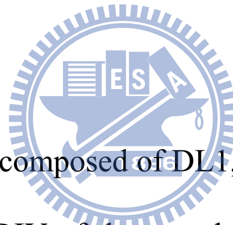
2.2. Circuit Description

As shown in Fig. 24, the BIST circuit comprises three main parts - TDC, Control Unit and Calibration Circuit. TDC is composed of Delay Buffer1 (DL1), PFD2, MUX, Charge

Pump2 (CP2), Loop Filter, VCO and Divider (DIV). Loop Filter, VCO and DIV are also parts of the tested PLL. Control Unit is the finite state machine using CLK0 as its clocking signal. Calibration Circuit calibrates the coefficient of the measurement resolution, which is determined by the parameters of the charge pump current of CP2, the equivalent capacitance of Loop Filter and VCO gain. Calibration Circuit is composed of VCO, DIV, Delay Buffer2 (DL2), MUX, CP2 and Loop Filter.

The BIST measures the jitter of divider output instead of the VCO jitter because the jitter of the VCO and divider are almost the same since the divider has a retiming circuit to synchronize the VCO phase and divider phase. Furthermore, measuring divider output jitter is more convenient since divider output has a clock frequency equal to that of the reference clock.

2.2.1. TDC



As shown in Fig. 24, TDC is composed of DL1, PFD2, MUX, CP2, Loop Filter, VCO and DIV, VCO, Loop Filter and DIV of the tested PLL are reused as components of the

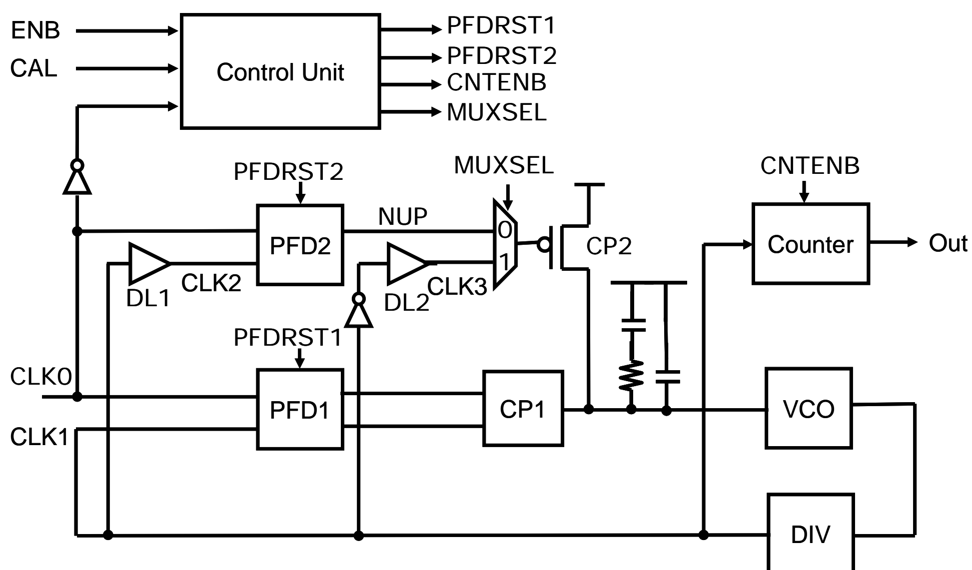


Fig. 24 Proposed BIST circuit.

TDC circuit to minimize the area overhead. When a phase difference between CLK0 and CLK1 is detected, the PLL shuts down immediately by disabling PFD1. After that, Loop Filter and VCO function as part of TDC. Fig. 25 shows the modified PFD, which can be disabled using a reset signal.

The TDC structure is modified to simplify the calibration process and enlarge the current capacity. CP2 is designed as a single switch that is controlled using the signal NUP only. Fig. 26—Fig. 28 show the modified circuit and timing behavior. DL1 delays CLK1 to generate the signal, CLK2. CLK2 is always lagging behind CLK0, so UP or NUP contains all of the timing information about CLK0 and CLK1 and signal DN can be neglected.

As shown in Fig. 29, the capacitor of TDC is replaced by Loop Filter. When the loop filter of the tested PLL is used as a capacitor, the charge is pumped into the smaller capacitor C2 first and then redistributed in both capacitors, so the equivalent capacitance is the sum of the capacitances of these two capacitors. The resistor of the loop filter can be neglected since the current flowing through the resistor is zero and the voltage drop across the resistor is zero in the steady state. Loop Filter can be modeled as a capacitor with capacitance C.

$$C = C_1 + C_2 \tag{8}$$

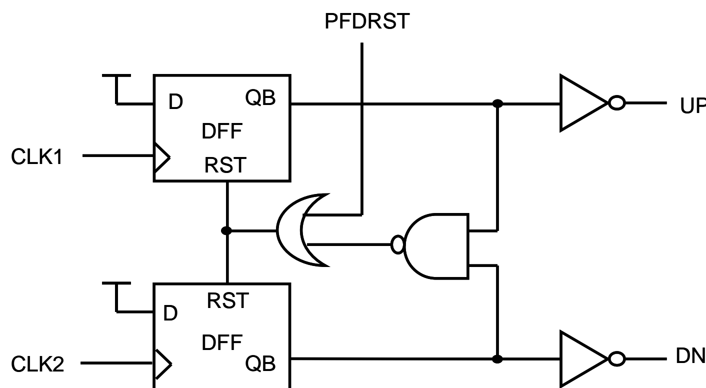


Fig. 25 Modified Phase-Frequency Detector.

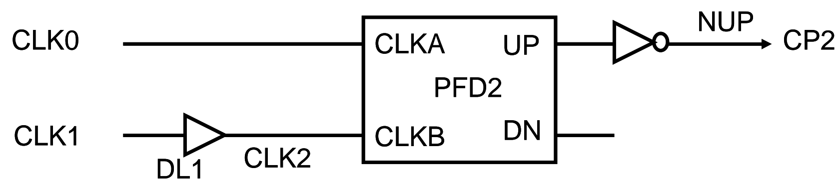


Fig. 26 PFD2 circuit design.

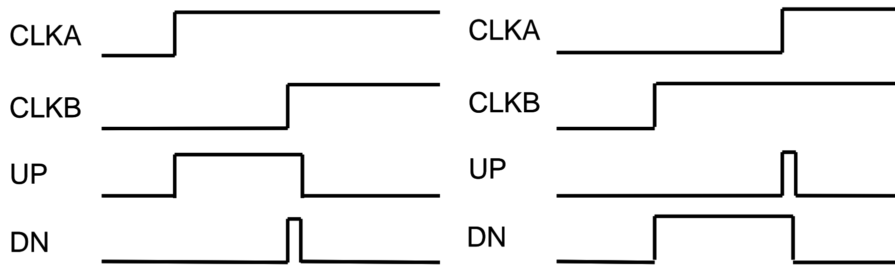


Fig. 27 Timing behavior of PFD2.

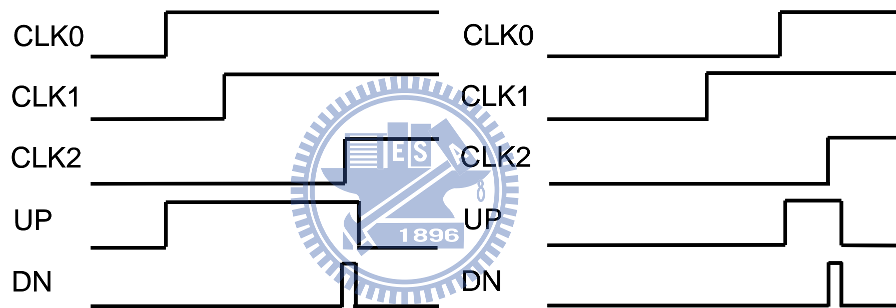


Fig. 28 Timing behavior of circuit with DL1.

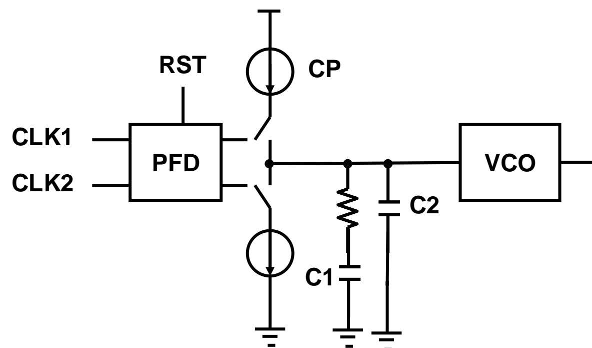


Fig. 29 Loop Filter is modeled as a capacitor.

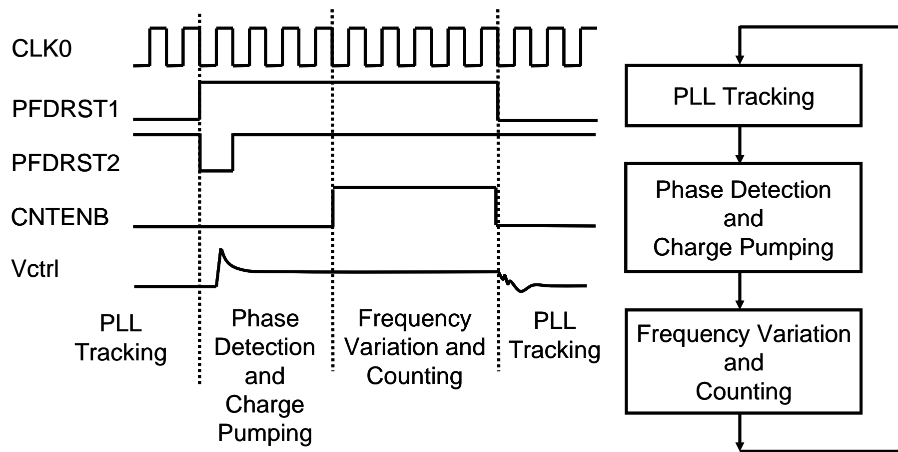


Fig. 30 Timing diagram of Control Unit.

2.2.2. Control Unit

The BIST process repeats three steps - PLL Tracking, Phase Detection and Counting. Control Unit can be implemented using a finite state machine, as shown in Fig. 30. The PLL Tracking step is the lock-in or pull-in process of the PLL. In step 1, PFD1 is turned on and PFD2 is turned off to allow the PLL to track the phase of the reference clock. In Phase Detection step, PFD1 is turned off and PFD2 is turned on to enable the TDC to detect the phase difference between the reference clock and feedback clock. CP2 pumps some charge to Loop Filter and the voltage of Loop Filter settles down to a particular value. Then, Control Unit proceeds to step 3. In this step, Counter is turned on to count the number of pulses from the DIV output.

The finite state machine uses the negative edge of the reference clock as its clocking signal instead of the positive edge, so PFD1 is turned on for preparation before the positive edges of the reference clock and the feedback clock arrive and it is turned off after the phase detection is completed. The durations of step 1 and step 2 should be longer than the lock-in time of the PLL and the settling time of the loop filter. The duration of step 3 equals Tc in (3).

2.2.3. Calibration

The measurement resolution, k_{RES}, of TDC in (6) must be calibrated. Using the clock period, T_o, of VCO as the reference yields an accurate pulse width to calibrate TDC. The divider is modified to yield a pulse width that equals the clock period of VCO. As shown in Fig. 31, a logic gate and a retiming latch are added to change the duty cycle of the output signal of Divider. After this modification, the pulse width of the Divider output equals the period of the VCO clock.

Fig. 32 shows the calibration circuit of the BIST. The DIV output is connected to CP2 via MUX. In the calibration mode, the control signal MUXSEL changes to a logic high to allow the DIV output signal to pass through MUX. The pulse signal is input to CP2 and changes the voltage of Loop Filter and the frequency of VCO. The pulse width T_0 is the clock period of VCO and the count N_{CAL} of Counter can be obtained. The pulse width is related to the count as

$$T_0 = k_{RES}(N_{CAL} - N_0), \tag{9}$$

where N_0 is the count of Counter if the DIV frequency does not deviate from the original frequency.

The clock period T_0 of VCO varies. It is known as the period jitter. Repeating the calibration process a particular number of times produces a histogram of different N_{CAL}.

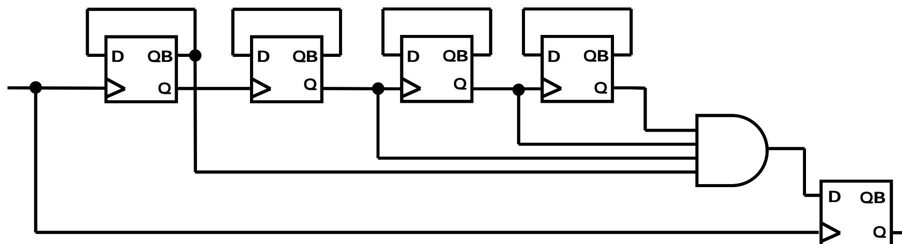


Fig. 31 Divider with an output pulse width that equals the period of VCO.

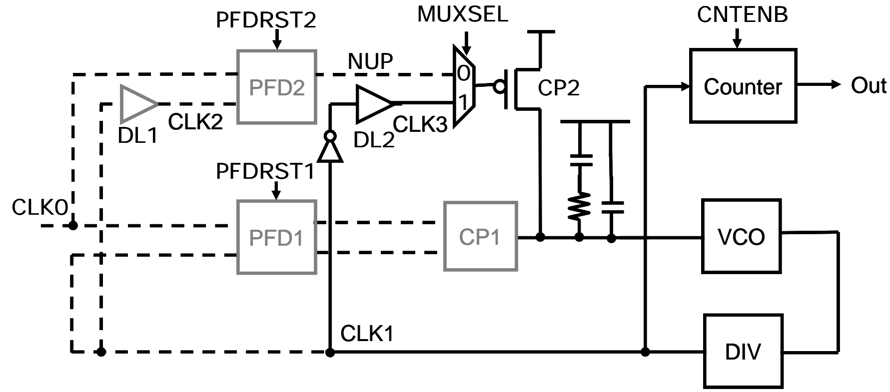


Fig. 32 Calibration circuit.

The average clock period $\overline{T_0}$ equals the reference clock period divided by N. The measurement resolution can be calibrated using the equation,

$$k_{RES} = \frac{\overline{T_0}}{\overline{N_{CAL}} - N_0}, \tag{10}$$

where $\overline{N_{CAL}}$ is the average value of N_{CAL}.

The purpose of adding DL2 to the calibration circuit is to delay the DIV output signal CLK1 for a clock period of VCO or some longer time to maintain the pulse width of the DIV output after the VCO frequency is changed. Fig. 33 plots the timing diagram of the calibration. The pulse width W_1 equals the clock period of VCO before the frequency is changed. W_2 is the clock period of VCO after the frequency is changed. DL2 successfully maintains the pulse width of the CLK1 at W_1.

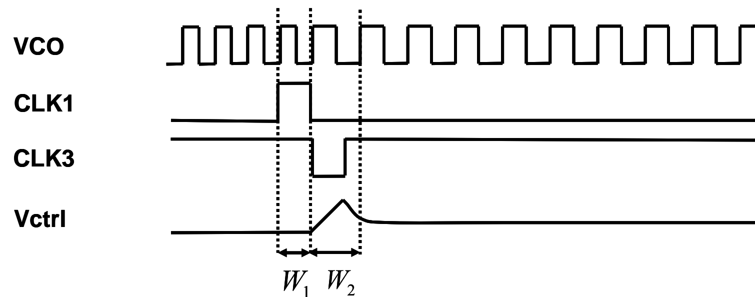


Fig. 33 Timing behavior of calibration.

2.3. Experimental Results

Fig. 34 shows the chip photograph. Fig. 35 presents the measurement equipments. The chip is implemented using 0.18μm CMOS technology. The BIST circuit includes the digital part and analog part. The power supplies are separated to prevent the disturbance of the noise from the digital circuit. The Divider output clock signal is measured using an oscilloscope and the BIST output digital signal is measured using a logic analyzer. The noise injected for measurement is produced using a function/arbitrary waveform generator.

As shown in Fig. 36, the noises of various amplitudes and forms are injected into the power line on the PCB through a coupling capacitor to measure the BIST performance in various environments. The power line on PCB can be modeled as an ideal power source in series with a parasitic resistor. The combination of the coupling capacitor and the parasitic resistor constitutes a high-pass filter. A high frequency noise is injected to the tested chip while low-frequency noises are filtered out. The coupling capacitor is designed to be as large as possible to allow more noise to pass through. In this experiment, a 10μF coupling capacitor is used.

The operating frequency of the PLL is 1.25GHz. The reference clock and the feedback clock are operated at 78.125MHz. Fig. 37 shows the PLL feedback clock waveform measured using an oscilloscope and the jitter histogram of 16k hits. 40mV peak-to-peak random noise is injected into the power line. The measured RMS jitter and peak-to-peak jitter are 8.8603ps and 69.3ps, respectively.

Fig. 38 shows the histogram of the BIST output in the calibration mode in the same environment described above. In the calibration mode, the histogram of the output values of BIST is that of period jitter. According to (10), the average clock period of VCO, which is 800ps when PLL is operated at 1.25GHz, can be used to calibrate the measurement

resolution. The counting time, N_o, is designed to be 16384 times of the period of the reference clock. From the histogram of the BIST output, the average value, $\overline{N_{CAL}}$, is calculated at 15702. The coefficient, k_{RES}, can be calculated using (10) as 800/(16384-15702)=-1.1730 ps/count. The negative sign of the coefficient means that a negative VCO gain is used.

Fig. 39 shows the histogram of the BIST output in test mode with 40mV peak-to-peak random noise. For comparison, the total number of the data samples measured to produce the histogram equals the number of the hits measured using oscilloscope. Each output value of BIST in test mode represents the phase difference between the reference clock and feedback clock, and the histogram of the BIST output values represents that of timing jitter. Since the measurement resolution, k_{RES}, in (6) was calibrated, the jitter magnitude can be determined by simply multiplying the output values of the BIST output data by the measurement resolution. The peak-to-peak jitter and RMS jitter of the PLL in this case are 1.1737*(15877-15940)=73.899ps and 1.1737*8.937=10.4893ps, respectively.

Fig. 40, Fig. 41, and Fig. 42 show the histograms measured using the oscilloscope, BIST in calibration mode and BIST in test mode, respectively, when the power line is injected with 40mV, 10MHz sinusoidal noise. The RMS jitter and peak-to-peak jitter measured using the oscilloscope are 18.6970ps and 80.4ps, respectively. The RMS jitter and peak-to-peak jitter measured using the BIST are 22.8011ps and 95.8357ps, respectively. Since the noise is sinusoidal, the histograms of period jitter and timing jitter have bowl shapes, as expected.

Table 1 presents more cases. Fig. 43 and Fig. 44 compare the RMS jitter and peak-to-peak jitter measured using the oscilloscope and BIST circuit. The measurement errors in most of the cases are under 20%, except in the case with 1MHz noise. As

mentioned, the TDC utilizes VCO and Loop Filter of the tested PLL as part of the circuit, but the initial value of the VCO control voltage is not constant due to supply noise and PLL tracking ability. This is believed to be the main cause of the measurement error in the experimental results. Table 2 and Table 3 summarize this work. The area overhead is 36.7%. The supply voltage is set to 1.85V because the BIST circuit does not function well when the voltage is under 1.85V. The problem has not been solved. However, the problem may probably arise in the analog circuit of BIST because the digital circuit is insensitive to a power supply voltage.

The measurement time, 3.44s, is too long for test application. To improve the performance, a high speed counter such as a ripple counter could be connected directly to the VCO for frequency measurement. It could shorten the measurement time to be about one tenth or less. The Multi-Phase Phase Detector [61] could also be applied to further shorten the measurement time to be less than one-hundredth of this work.

Table 4 compares the results herein with previous works. This work has a resolution of 1.17ps, which is the finest of all, except the one (1ps) using an accurate analog bias to fine tune the delay line [8]. The measurement error is relatively small (14.6%), but dependent on the noise frequency, so modifying the circuit to have a constant initial VCO control voltage is required. The test time is much longer than the other approaches because this work achieves good resolution at the expense of measurement time.

Fig. 34 Chip photograph.

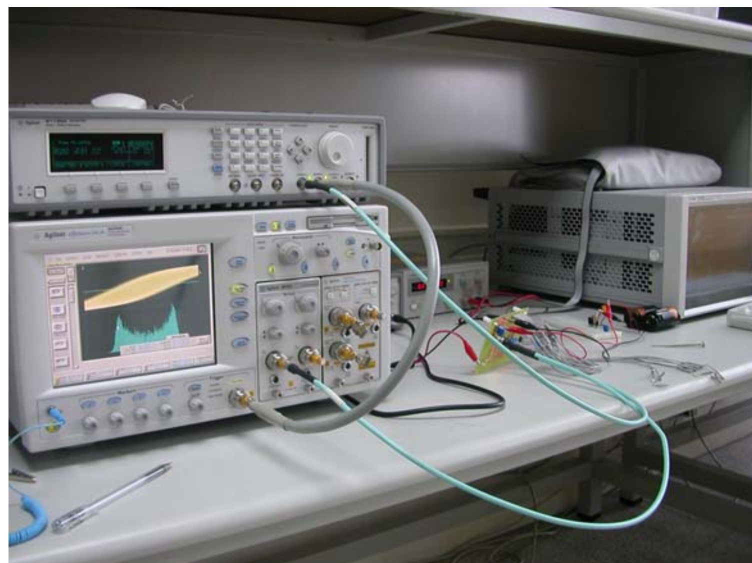


Fig. 35 Measurement equipment.

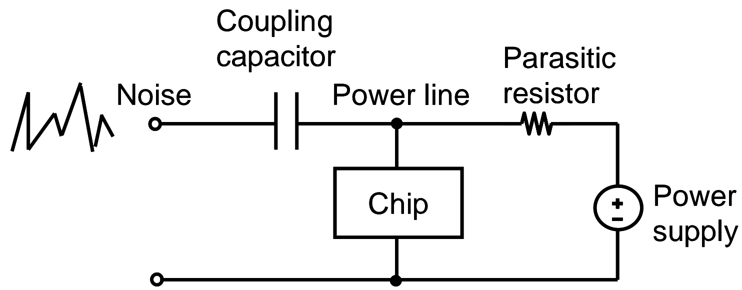


Fig. 36 Injecting noise into the power line.

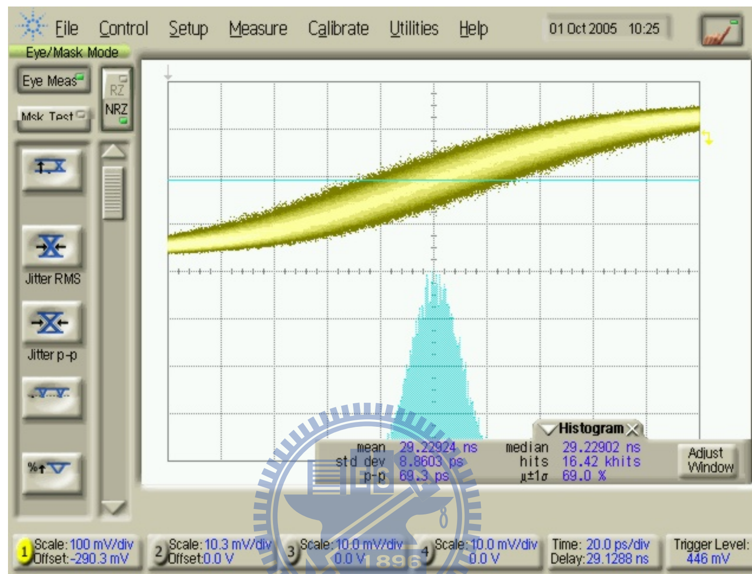


Fig. 37 PLL DIV output clock jitter with 40mV p-p random noise.

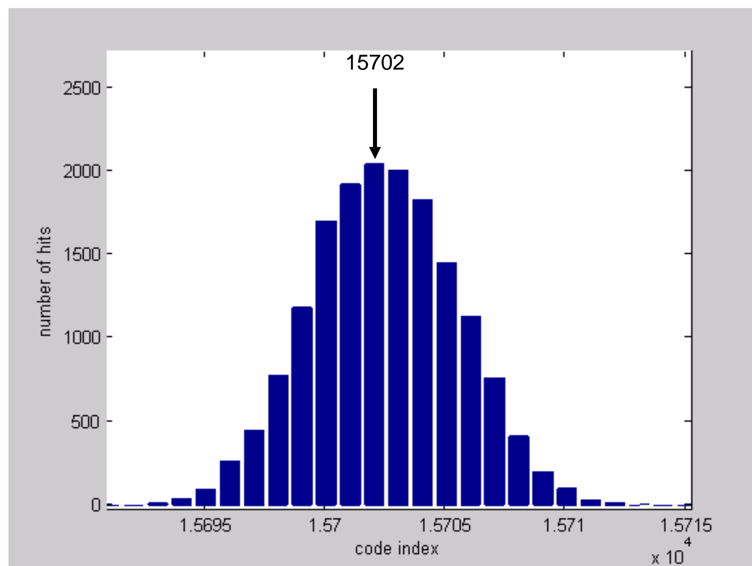


Fig. 38 Histogram of BIST output in calibration mode with 40mV p-p random noise.

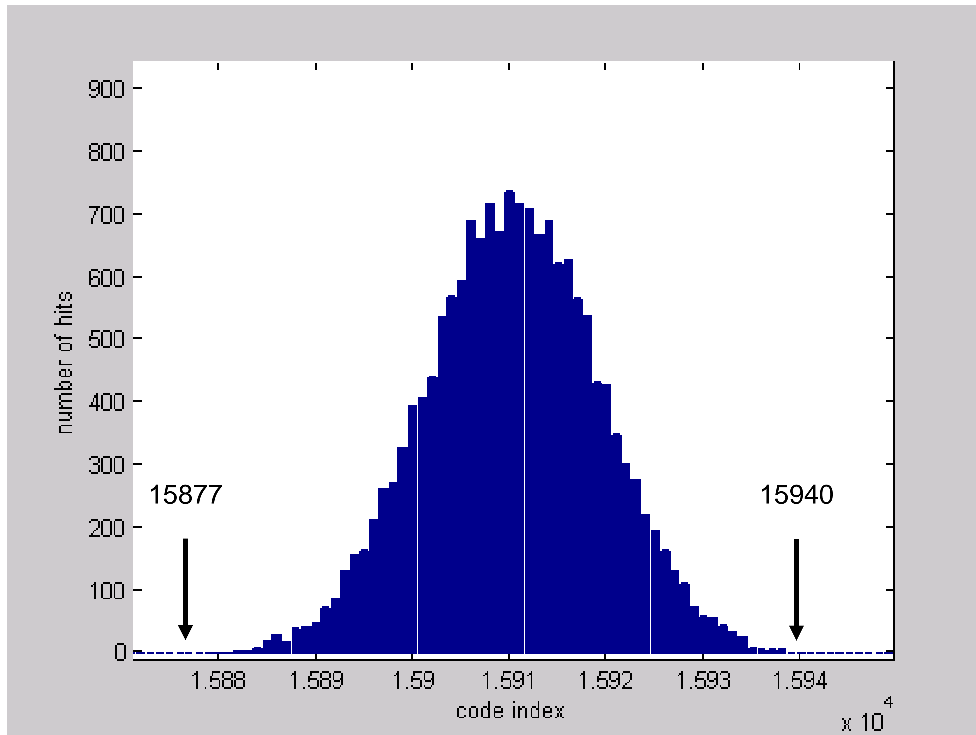


Fig. 39 Histogram of BIST output in test mode with 40mV p-p random noise.

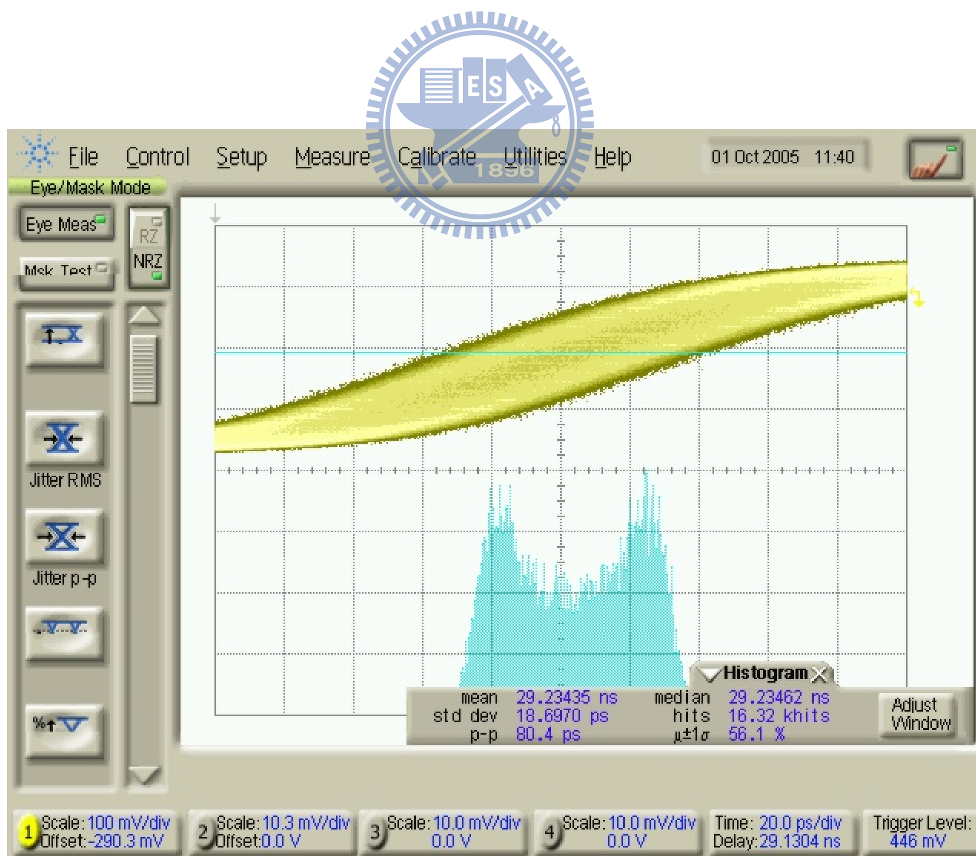


Fig. 40 PLL divider output jitter by oscilloscope (40mV p-p 10MHz sinusoidal).

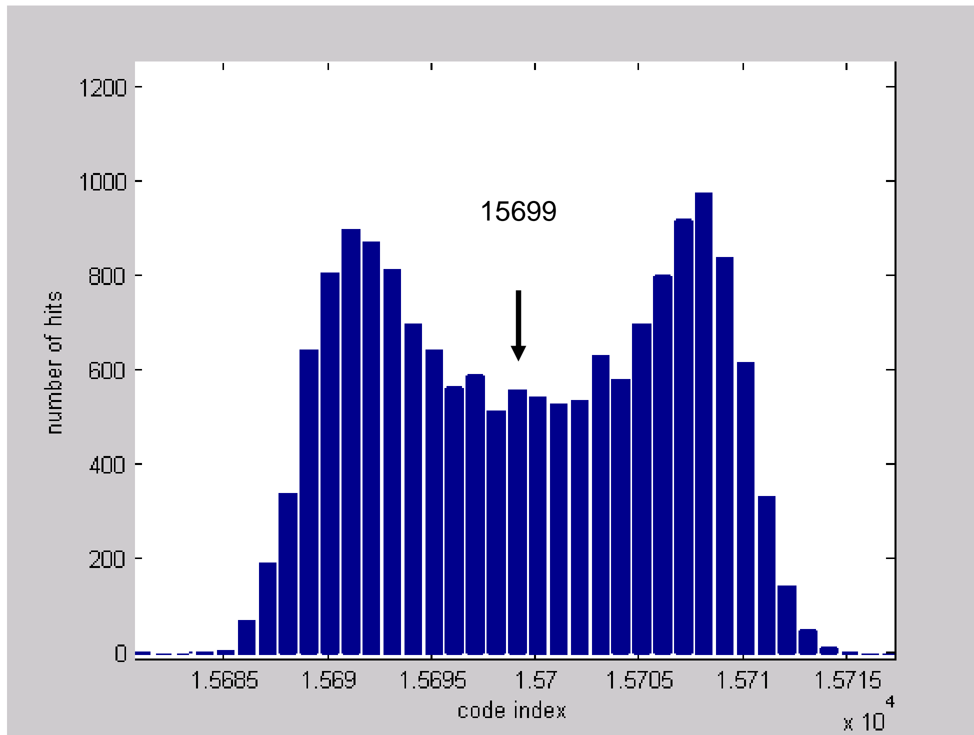


Fig. 41 Histogram of BIST output in calibration mode (40mVp-p 10MHz sinusoidal).

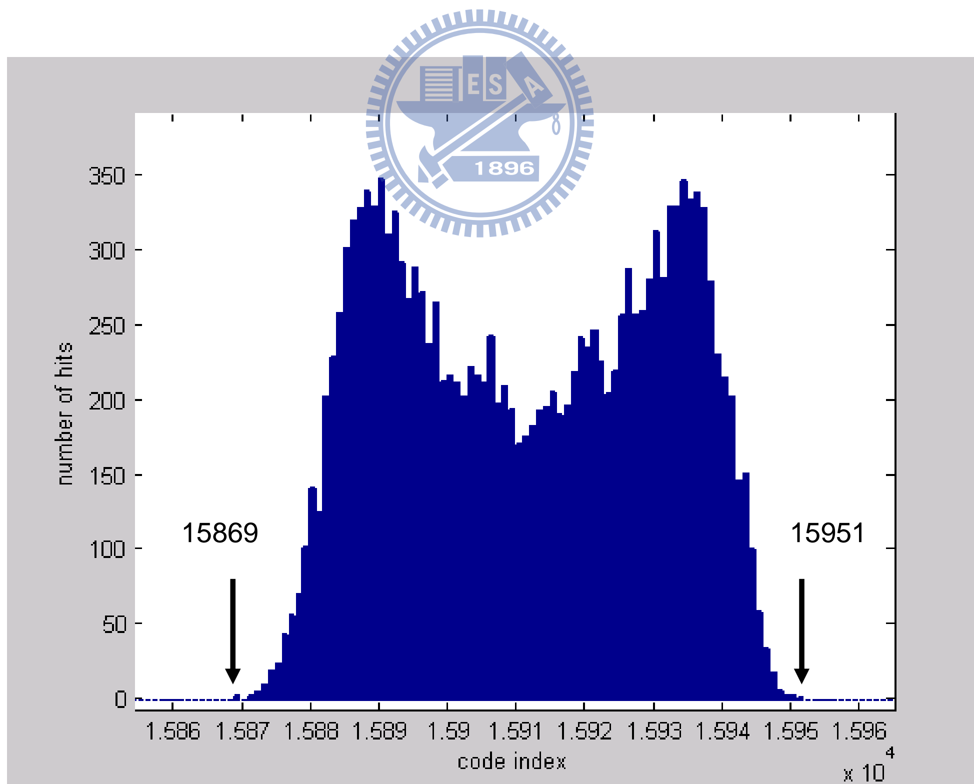


Fig. 42 Histogram of BIST output data in test mode (40mVp-p 10MHz sinusoidal).

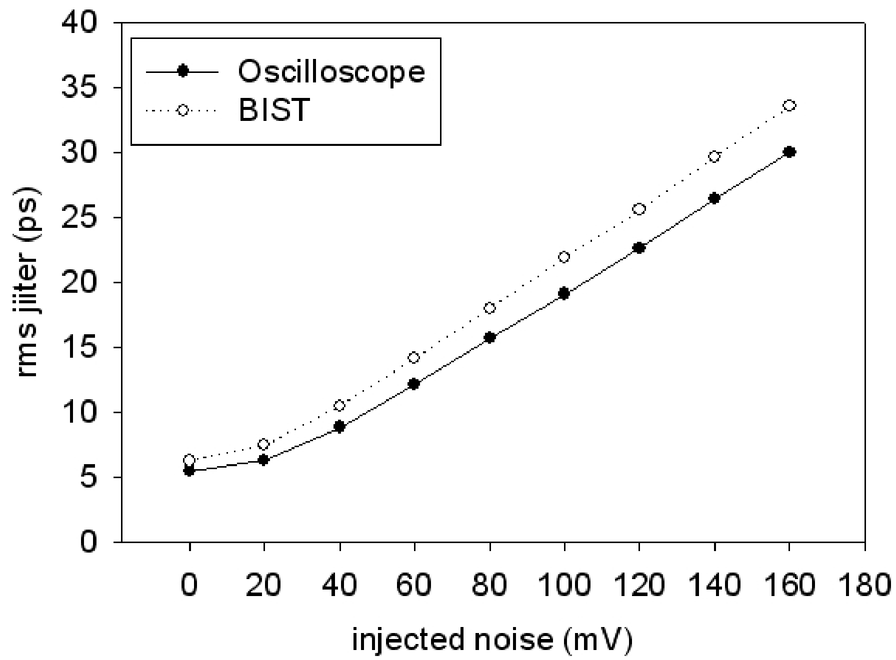


Fig. 43 RMS jitter measured using oscilloscope and the BIST circuit.

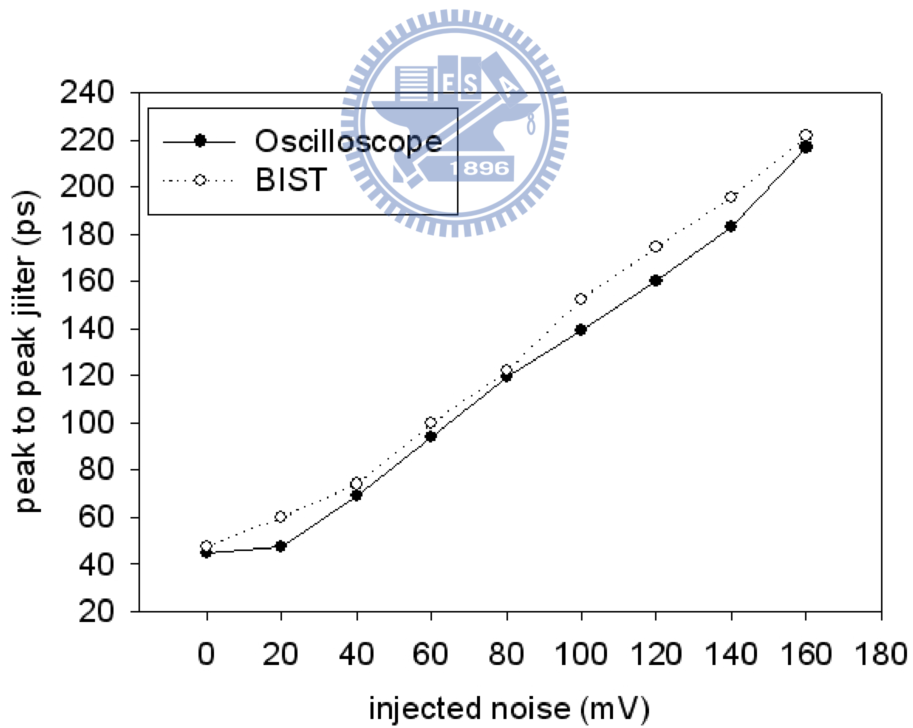


Fig. 44 Peak-to-peak jitter measured using oscilloscope and the BIST circuit.

Table 1 Jitter measured using oscilloscope and the BIST circuit.

Type	Amp. p-p (mV)	Fr (MHz)	Osc RMS (ps)	Osc p-p (ps)	BIST RMS (ps)	BIST p-p (ps)	RMS error (%)	p-p error (%)
Random	0	-	5.4502	44.9	6.2464	47.6284	14.60864	6.076615
Random	20	-	6.3349	47.6	7.4476	59.9492	17.5646	25.9437
Random	40	-	8.8603	69.3	10.4831	73.899	18.38538	6.701299
Random	60	-	12.1454	94.2	14.1385	99.682	16.41033	5.819533
Random	80	-	15.724	119.6	17.9926	121.9933	14.42763	2.001087
Random	100	-	19.1059	139.1	21.9112	152.5462	14.6829	9.666571
Random	120	-	22.588	160	25.5602	174.5728	13.15831	9.108
Random	140	-	26.4569	183.3	29.687	195.7189	12.20891	6.775177
Random	160	-	30.0448	216.7	33.597	221.509	11.82301	2.219197
Sin	40	50	10.9452	60	13.2048	72.5872	20.64467	20.97867
Sin	80	50	20.089	87.1	24.0374	104.1341	19.65454	19.55695
Sin	40	10	18.697	80.4	22.8011	95.8357	21.95058	19.19863
Sin	80	10	36.8383	133.3	43.8717	161.5182	19.09263	21.16894
Sin	80	1	5.2596	41.8	7.6686	54.8198	45.80196	31.14785
Sin	160	1	7.0429	46.7	10.9957	66.5088	56.12461	42.41713

Table 2 PLL specifications.

CMOS technology	0.18μm CMOS
VDD	1.85V
Power consumption (PLL+BIST analog part)	40mW
Area	300X300μm^2
Reference clocks	78.125MHz
VCO frequency	1.25GHz
RMS jitter	5.4502ps
Peak-to-peak jitter	44.9ps

Table 3 BIST specifications.

VDD	1.85V
Power consumption (Digital part)	0.22mW
Area (BIST analog)	190X35μm^2 (7.4%)
Area (BIST digital)	310X85μm^2(29.3%)
Resolution	1.17ps
Error	14.6%
Reference clocks	78.125MHz
Measurement time (16k data)	3.44s

Table 4 Performance Comparison.

	Type	Res.	Scope (RMS jitter)	BIST (RMS jitter)	Error	Meas. time (one-shot)	Tech.
Sunter, ITC, 1999 [1]	Delay line	40ps	88.8ps	72ps	18.9%	4.16ns	0.6μm CMOS
Jenkins, CICC, 2007 [8]	Delay line	1ps	5.7ps	5.5ps	3.5%	1.85ns	90nm CMOS
Aloisio, NSSCR, 2009 [10]	Delay line	11.3ps	-	-	-	12.6ns	FPGA
Abaskharoun, CICC, 2001 [16]	Vernier	18ps	30.4ps	27.6ps	9.2%	40ns	0.35μm CMOS
Levine, CDT, 2005 [27]	Sampling Offset	9.8ps	13.5ps	14.5ps	7.4%	40ns	0.18μm CMOS
Chan, CICC, 2001 [22]	Vernier Ring	67ps	22ps	66ps	200%	154ns	0.18μm CMOS
Xia, ISVLSI, 2005 [25]	Vernier Ring	18.5ps	42.7ps	62.7ps	46.8%	-	0.18μm CMOS
Chen, CICC, 1999, [30]	Pulse-shrinking Ring	68ps	-	-	-	10μs	0.35μm CMOS
Henzler, ISSCC, 2008 [33]	Local Passive	4.7ps	-	-	-	5.56ns	90nm CMOS
Chen, ESSCIRC, 2006 [39]	Time Amplifier	50ps	-	-	-	6.67us	0.35μm CMOS
Taylor, ITC, 2004 [43]	TVC with flash ADC	55ps	52ps	80ps	53.8%	10ns	0.25μm BICMOS
Ishida, ISSCC, 2005 [47]	Hybrid	-	95.7ps	83.5ps	12.7%	-	0.18μm CMOS
Sunter, DTC, 2004, [50]	Under-sampling	1.4ps	43ps	50ps	16.3%	103.7ns	FPGA
This work	TVC with VCO	1.17ps	5.45ps	6.25ps	14.6%	210μs	0.18μm CMOS

Chapter 3

BIST for Spread-Spectrum Clocks

3.1. BIST Methodology Overview

Fig. 45 shows an SSC generator (SSCG) and the proposed BIST methodology. A triangular waveform is generated according to the modulation profile of a 5000ppm down-spreading and a 30kHz modulation frequency. The Sigma-Delta Modulator (SDM) is used to control the 10-phase 5-stage Voltage-Controlled Oscillator (VCO) such that it oscillates in accordance with the modulation profile.

The BIST module is composed of hardware and software. The hardware comprises a 10-phase Multi-Phase Phase Detector (MPD), as shown in Fig. 46. The MPD uses ten D Flip-Flops (DFFs) to compare the reference clock with the ten clock phases generated by the VCO. The reference clock is used as a triggering signal of the DFFs, and the ten clock phases are the signal being sampled. When the clock edge of the reference clock comes,

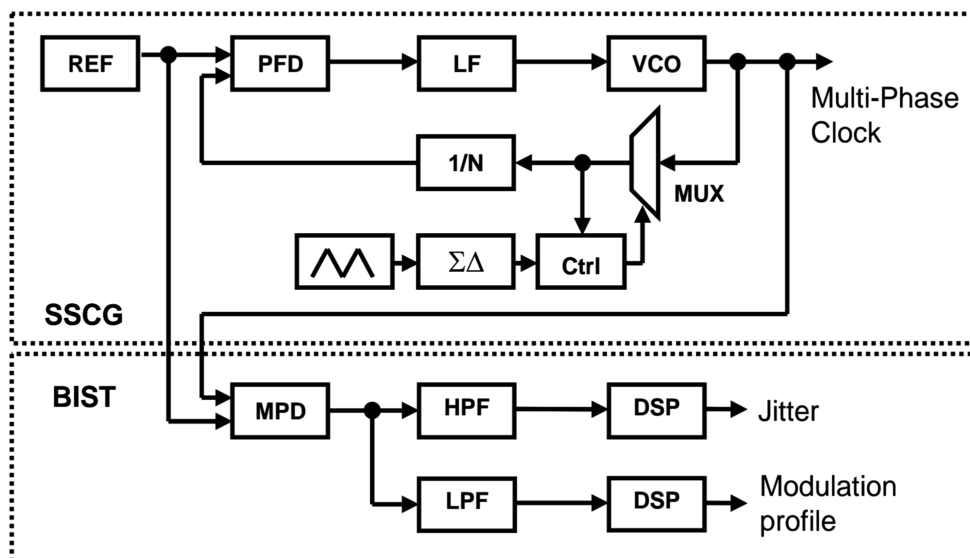


Fig. 45 Proposed BIST methodology.

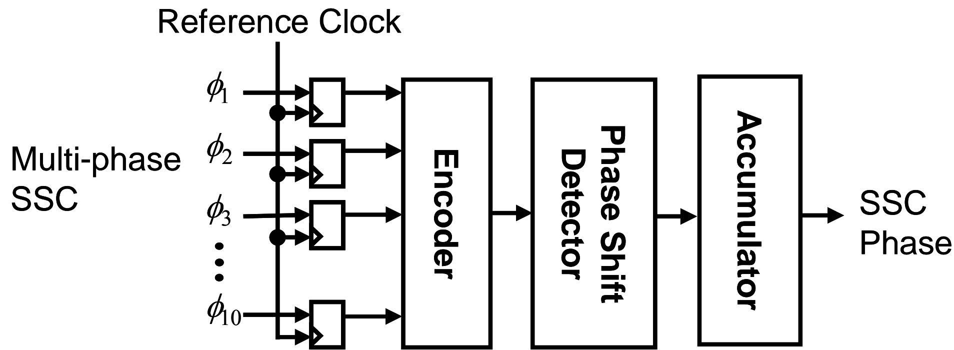


Fig. 46 Multi-Phase Phase Detector.

the ten clock phases are sampled and the DFFs output 10-bit thermal meter code. The transition bit of the thermal meter code represents the detected phase. The phase-shift detector detects the phase shift by comparing the detected phases at the first triggering time and the next triggering time.

An example is shown in Fig. 47. Phase 5 is sampled by the first reference clock edge, and Phase 7 is sampled by the next reference clock edge. A phase shift of 0.2UI is detected. Notably, if the frequency deviation of the SSC is too large, the phase shift may exceed 1 UI. If so, a faster reference clock is needed. When frequency deviation is 6MHz (5000ppm) and a reference clock period of 50ns, phase shift is 0.3UI, which is smaller than 1UI. The next step in phase detection process is to accumulate each phase shift to recover the absolute phase. Notably, without jitter, the accumulated phase is the integration of the modulation profile (Fig. 17(a)). Because modulation profile is the timing diagram of the SSC frequency, the integration of frequency in time is the absolute phase.

If the SSCG doesn't have multi-phase clocks, the single phase clock must be operating at higher speed. This clock can be input to a high speed single-phase phase detector, such as a DFF, and the detected serial data is processed by a de-serializer to have the output similar with that of the MPD. Another approach is converting a single-phase clock to a multi-phase clock by a ring type shift registers.

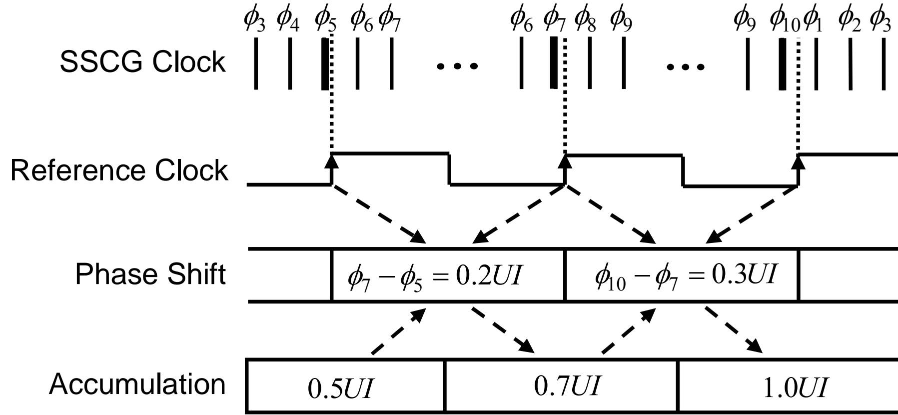


Fig. 47 Timing diagram of the MPD.

The software in the BIST modules comprises a digital signal processing (DSP) program that utilizes the on-chip DSP or microprocessor to extract jitter and the modulation profile after obtaining the accumulated phase using the MPD. Conceptually, the modulation profile can have a frequency as low as 30kHz. Therefore, a Low-Pass Filter (LPF) can extract the modulation profile from the accumulated phase. The high-frequency components of jitter are defined by the SATA standard. Therefore, jitter can be obtained using a High-Pass Filter (HPF). Notably, additional DSP functions are required to acquire the modulation profile and jitter after filtering. Fig. 48 shows the jitter measurement model, where ϕ_{SSC} is the ideal accumulated phase. Two added noise sources are jitter (ϕ_J) and MPD phase quantization noise (ϕ_E). The methodology has two processing paths—the HPF path for jitter measurement and LPF path for modulation profile extraction.

For jitter measurement, the accumulated phase passes through the HPF. After that, only high-frequency components (ϕ_{JH+EH}) remain, where JH is high-frequency jitter and EH is high-frequency quantization noise. The power spectral density (PSD) function of high-frequency components, $S_{\phi_{JH+EH}}$, can be obtained by taking the square of the Fast Fourier Transform (FFT).

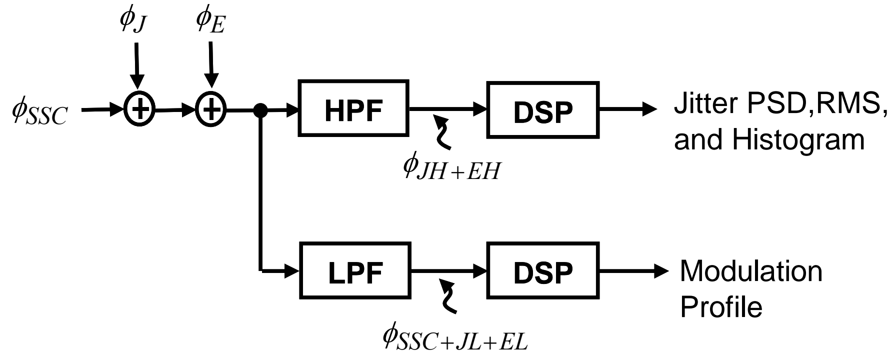


Fig. 48 BIST methodology model.

$$S_{\phi_{JH+EH}}(f) = FFT^2(\phi_{JH+EH}(t)). \tag{11}$$

The jitter variance, or jitter power, is the integration of $S_{\phi_{JH+EH}}$ in the frequency domain.

$$\phi^2_{JH+EH,RMS} = \int_{-f_{ref}/2}^{f_{ref}/2} S_{\phi_{JH+EH}}(f)df, \tag{12}$$

where f_{ref} is the reference clock frequency and RMS is root mean square value. Because f_{ref} is the sampling rate of MPD, so the frequency band of the signals within DSP circuit does not exceed the range of half of f_{ref}, based on DSP theories.

Since jitter and quantization noise are independent random variables, jitter variance can be obtained by

$$\phi^2_{JH,RMS} = \phi^2_{JH+EH,RMS} - \phi^2_{EH,RMS}. \tag{13}$$

Since quantization noise is typically regarded as white noise, its PSD is

$$S_{\phi_E} = \frac{\Delta^2_{MPD}}{12 \cdot f_{ref}}. \tag{14}$$

Since the transfer function of the HPF is known, $\phi_{EH,RMS}$ is obtained as

$$\phi^2_{EH,RMS} = \int_{-f_{ref}/2}^{f_{ref}/2} \left| H_{HPF}(j2\pi f) \right|^2 \cdot S_{\phi_E} df. \tag{15}$$

The modulation profile is extracted using the LPF. After the accumulated phase passes

through the LPF, only the low-frequency component $\phi_{SSC+JL+EL}$ remains, where JL is low-frequency jitter and EL is low-frequency quantization noise. $\phi_{SSC+JL+EL}$ approximates ϕ_{SSC}, because low-frequency jitter is relatively small. Most of the low-frequency jitter of the VCO is filtered out by the PLL, as PLL acts like a high pass filter for VCO noise. Most high-frequency components of quantization noise are filtered out by the LPF. As mentioned, the accumulated phase shift is the integration of the modulation profile in time. Now, by taking the reverse operation, the derivative of $\phi_{SSC+JL+EL}$ generates the modulation profile.

$$f(t) = \frac{d\phi_{SSC+JL+EL}(t)}{dt}. \tag{16}$$

Via (11)~(16), the jitter and modulation profile can be extracted from the accumulated phase obtained by the MPD.

The next step is to validate the extracted result. Without dedicated SSC timing jitter measurement instruments, verifying that such a methodology can effectively measure SSC jitter is difficult. In next section, the work derives an equation that correlates timing jitter in SSC mode and non-SSC mode of the same PLL. In non-SSC mode, jitter can be measured by external instruments. SSC jitter is estimated using measured results from the non-SSC mode and the derived equation. Thus, this work can cross check and validate both the BIST methodology and the jitter estimation method.

3.2. SSC Jitter Estimation

In this section, a jitter estimation method that correlates a non-SSC clock timing jitter and the corresponding SSC jitter is used to validate the BIST methodology. An equation for SDM noise calculation is also presented for the specific SSCG in this work.

The SSCG is made by a fractional-N PLL with a triangular modulation profile. Some prior arts have developed the jitter estimation methods for fractional-N PLLs [62][63]. In

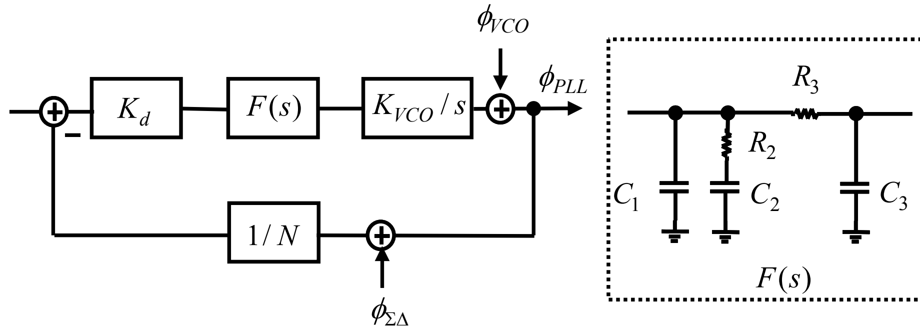


Fig. 49 Noise model of the SSCG.

these studies, a PLL is modeled as an ideal filter and a common SDM is used. However, a PLL transfer function has a peak, which increases jitter magnitude. Additionally, the SDM used in this work is specially designed so a common analysis is not applicable. More accurate model and a dedicated analysis are presented as follows.

Fig. 49 shows the noise model of a SSCG circuit with a third-order loop filter. Based on spectral analysis, the output jitter PSD of the SSCG and noise sources are related as follows:

$$\begin{aligned} S_{\Phi_{PLL}}(f) &= S_{\Phi_{PLL\Sigma\Delta}}(f) + S_{\Phi_{PLLVCO}}(f) \\ &= \left|H_{\Sigma\Delta}(j2\pi f)\right|^2 \cdot S_{\Phi_{\Sigma\Delta}}(f) \\ &+ \left|H_{VCO}(j2\pi f)\right|^2 \cdot S_{\Phi_{VCO}}(f), \end{aligned} \tag{17}$$

where $S_{\Phi_{PLL}}$ is the PSD of the PLL output jitter. $S_{\Phi_{PLL}}$ is composed of $S_{\Phi_{PLL\Sigma\Delta}}(f)$ and $S_{\Phi_{PLLVCO}}(f)$, the PSD of the PLL output jitter caused by the noise from the SDM and VCO. Additionally, $S_{\Phi_{\Sigma\Delta}}$ and $S_{\Phi_{VCO}}$ are the PSDs of the SDM and VCO noise, respectively, and $H_{\Sigma\Delta}$ and H_{VCO} are the transfer functions from noise sources, $\phi_{\Sigma\Delta}$ and ϕ_{VCO}, to the PLL output, respectively. With this information, $S_{\Phi_{PLL}}$ can be derived by (17). The RMS jitter is calculated as

$$\phi_{J,RMS}^2 = \int_{-\infty}^{\infty} S_{\Phi_{PLL}}(f)\,df. \tag{18}$$

The high-frequency RMS jitter is calculated as

$$\phi_{JH,RMS}^{2} = \int_{-\infty}^{\infty} \left| H_{HPF}(j2\pi f) \right|^{2} \cdot S_{\phi_{PLL}} df. \tag{19}$$

Next, the derivation and calibration of $S_{\Phi_{\Sigma\Delta}}$, $H_{\Sigma\Delta}(s)$, $S_{\Phi_{VCO}}$ and $H_{VCO}(s)$ are discussed.

3.2.1. Derivation of $\mathbf{H_{VCO}(s)}$ and $\mathbf{H_{\Sigma\Delta}(s)}$

Transfer functions $H_{\Sigma\Delta}(s)$ and $H_{VCO}(s)$ are defined as

$$H_{\Sigma\Delta}(s) = \frac{\phi_{PLL\Sigma\Delta}(s)}{\phi_{\Sigma\Delta}(s)} = -\frac{G(s)}{1+G(s)}; \tag{20}$$

$$H_{VCO}(s) = \frac{\phi_{PLLVCO}(s)}{\phi_{VCO}(s)} = \frac{1}{1+G(s)}, \tag{21}$$

where $\phi_{PLL\Sigma\Delta}$ and ϕ_{PLLVCO} are the PLL output phases caused by the SDM and VCO noise, respectively. The open-loop transfer function $G(s)$ is

$$G(s) = \frac{K_d F(s) K_{VCO}}{sN}, \tag{22}$$

where K_d and K_{VCO} are the gains of the phase detector and the VCO, respectively, and N is the division ratio. The transfer function of the loop filter, $F(s)$, is defined as

$$F(s) \cong \frac{K_h(s+z_1)}{s\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)}. \tag{23}$$

The gain, zero, and poles of the third-order loop filter are

$$K_h = \frac{C_2 R_2}{C_1 + C_2},\ z_1 = \frac{1}{C_2 R_2}, \qquad p_1 = \frac{C_1 + C_2}{C_1 C_2 R_2},\ p_2 = \frac{1}{C_3 R_3}. \tag{24}$$

$H_{\Sigma\Delta}(s)$ and $H_{VCO}(s)$ deviate from the design target due to the process variation. A

proposed calibration flow is used to calibrate the parameters of the transfer functions. First, we assume all capacitance values shift in the same ratio under process variation by a factor, k_1, and resistance values shift by a factor k_2. The assumption is reasonable because the manufacturing process for all components in a single chip is similar, such as doping concentration and temperature. If the assumption is true, the values of the poles and the zero deviate proportionally with a factor, α, where α is related to k_1 and k_2 as

$$\alpha = \frac{1}{k_1 k_2}. \tag{25}$$

The poles and zero can be written as

$$z_1 = \alpha z_{1o},\ p_1 = \alpha p_{1o},\ p_2 = \alpha p_{2o}, \tag{26}$$

where z_{1o}, p_{1o} and p_{2o} are the design target. By substituting (26) and (23) into (22), and transform (22) into frequency domain. The open-loop gain, G, can be rewritten as

$$\begin{aligned} G &= \frac{K_d F(j2\pi f) K_{VCO}}{j2\pi f N} \\ &= K_o \cdot H_o(\alpha, f) \\ &= F_G(K_0, \alpha, f), \end{aligned} \tag{27}$$

where

$$K_o = \frac{K_d K_{VCO} K_h}{N}, \tag{28}$$

and H_0 is the remaining part of G. From this derivation, The open-loop gain, G, is a function of K_o, α and f. Thus, H_{VCO} is also a function of K_o, α and f.

$$H_{VCO} = F_{H_{VCO}}(K_0, \alpha, f). \tag{29}$$

One can approximately define the natural frequency, f_n, as the frequency at which the maximum gain of H_{VCO} occurs. The natural frequency, f_n, is obtained by solving the equation,

$$\frac{\partial}{\partial f}\left|F_{H_{VCO}}(K_0,\alpha,f)\right| = 0. \tag{30}$$

From (29) and (30), f_n is a function of K_0 and α.

$$f_n = F_{f_n}(K_0,\alpha). \tag{31}$$

Rearranging (31) shows that the constant, K_0, is a function of α and f_n.

$$K_0 = F_{K_0}(\alpha, f_n). \tag{32}$$

By substituting (32) into (29), H_{VCO} is a function of α, f_n and f.

$$H_{VCO} = F_{H_{VCO}}(\alpha, f_n, f). \tag{33}$$

This means that when the natural frequency and process variation factor, α, are known, H_{VCO} and $H_{\Sigma\Delta}$ can be derived. f_n and α are obtained using the following method. We assume the output phase noise of a PLL in non-SSC mode is dominated by VCO noise, and the output phase noise of a PLL and VCO noise are related as follows:

$$S_{\Phi_{PLL},nonSSC} = S_{\Phi_{VCO}}(f)\cdot\left|H_{VCO}(j2\pi f)\right|^2, \tag{34}$$

where $S_{\Phi_{PLL},nonSSC}(f)$ is the PSD of the PLL output jitter in non-SSC mode. The charge pump current of the phase detector determines phase detector gain, K_d, and the values of K_o and f_n in (27) and (31), but the value of α is not affected by the charge pump current. When the charge pump current is changed, the phase noises with different natural frequencies f_{n1} and f_{n2} are produced. Notably, the charge pump current is affected by process variation and it is difficult to know the exact values. However, knowing the exact values of charge pump current is not necessary. The parameter of charge pump current is included in the natural frequency as shown in (31), and the natural frequency can be observed by a spectrum analyzer. It is the same reason why knowing the exact values of other parameters such as VCO gain is not necessary. The non-SSC jitter PSD and transfer

functions are related as follows:

$$S_{\Phi_{PLL1},nonSSC} = S_{\Phi_{VCO}}(f) \cdot \left|F_{H_{VCO}}(\alpha, f_{n1}, f)\right|^2; \tag{35}$$

$$S_{\Phi_{PLL2},nonSSC} = S_{\Phi_{VCO}}(f) \cdot \left|F_{H_{VCO}}(\alpha, f_{n2}, f)\right|^2. \tag{36}$$

This work divides (36) by (35) to eliminate VCO noise.

$$\frac{S_{\Phi_{PLL2},nonSSC}}{S_{\Phi_{PLL1},nonSSC}} = \frac{\left|F_{H_{VCO}}(\alpha, f_{n2}, f)\right|^2}{\left|F_{H_{VCO}}(\alpha, f_{n1}, f)\right|^2}. \tag{37}$$

The equation is expressed in log scale as follows:

$$\begin{aligned} \Delta S &= 10\log\left(S_{\Phi_{PLL2},nonSSC}\right) \\ &\quad - 10\log\left(S_{\Phi_{PLL1},nonSSC}\right) \\ &= 10\log\left(\left|F_{H_{VCO}}(\alpha, f_{n2}, f)\right|^2\right) \\ &\quad - 10\log\left(\left|F_{H_{VCO}}(\alpha, f_{n1}, f)\right|^2\right) \\ &= \Delta H^2(\alpha, f_{n1}, f_{n2}, f), \end{aligned} \tag{38}$$

where ΔH^2 is the difference between two transfer functions in log scale, and ΔS is the difference between PSDs in log scale measured by a spectrum analyzer. The value of α is calibrated as follows. Using the originally designed charge pump current, f_{n1} is measured. Next, the charge pump current is increased to obtain f_{n2} and ΔS. If f_{n1}, f_{n2}, ΔS and f are known, α can be calculated by (38). To increase calibration accuracy, several f_{n2} and ΔS are obtained by increase charge pump current again and using curve-fitting procedure to determine the value of α that best satisfies (38).

3.2.2. Derivation of $S_{\Phi_{\Sigma\Delta}}$

Fig. 50 shows the tested SSCG [64]. A 10-phase clock is generated and fed into the multiplexer (MUX). The SDM and MUX select a suitable phase shift according to the frequency deviation determined by the given modulation profile. The division ratio for a

20MHz reference clock and a 1.2GHz output clock is 60. Since the phase shift is 0.1UI, confined with the division ratio of 60, the frequency deviation is 0.167%. This is 33% of the 5000ppm frequency deviation. Thus, the phase shift speed must increase by 300%, and the SDM must operate at 300% of the reference clock rate to achieve a 5000ppm frequency deviation. Because the data rate of the SDM is 300% of the frequency of the reference clock and the divider output, three consecutive data of SDM is summed in one reference clock period. The equivalent output of the SDM is the sum of three consecutive data of the original SDM.

The output signal of the SDM is denoted as x[n], and the sum of three consecutive data is

$$y[k] = x[3k-2] + x[3k-1] + x[3k]. \tag{39}$$

It can be regarded as three-time down sampling of the moving sum $x'[n]$.

$$x'[n] = x[n-2] + x[n-1] + x[n]. \tag{40}$$

The PSD of the noise at the output of a MASH-111 SDM is

$$S_{QE}(z) = \left|(1-z^{-1})^3\right|^2 \cdot S_E, \tag{41}$$

where S_E is the quantization noise in the SDM with the following PDF.

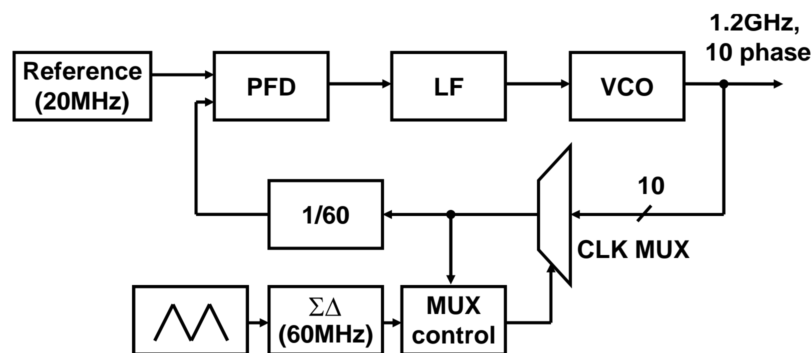


Fig. 50 The SSCG structure with multi-phase selection.

$$S_E = \frac{\Delta^2}{12 f_s}, \tag{42}$$

where Δ is 1 Least-Significant Bit (LSB) of the quantizer, or 0.1UI for a 10-phase MUX; f_s is 300% of the reference clock rate.

$$f_s = 3 f_{ref}. \tag{43}$$

Additionally, (41) is transformed into frequency domain as

$$S_{QE}(f) = \Delta^2 \frac{16}{3 f_s} \sin^6\left(\frac{\pi f}{f_s}\right). \tag{44}$$

The PSD of the moving sum is

$$S_{QE1}(z) = \left|1 + z^{-1} + z^{-2}\right|^2 \cdot S_{QE}(z). \tag{45}$$

The PSD of the moving sum is transformed into frequency domain as

$$S_{QE1}(f) = \left(3 + 4\cos\left(\frac{2\pi f}{f_s}\right) + 2\cos\left(\frac{4\pi f}{f_s}\right)\right) \cdot S_{QE}(f). \tag{46}$$

After down sampling three times, the PSD of $y[k]$ is

$$\begin{aligned} S_{QE2}(f) &= S_{QE1}(f) + S_{QE1}\left(f + \frac{f_s}{3}\right) \\ &\quad + S_{QE1}\left(f + \frac{2 \cdot f_s}{3}\right). \end{aligned} \tag{47}$$

The PSD of the equivalent noise at the divider input is calculated as

$$S_{\Phi_{\Sigma\Delta}}(z) = \left|\frac{1}{1 - z^{-1}}\right|^2 \cdot S_{QE2}(z). \tag{48}$$

The PSD of the equivalent noise at the divider input is transformed into frequency domain as

$$S_{\Phi_{\Sigma\Delta}}(f) = \frac{1}{4\sin^2\left(\frac{\pi f}{f_{ref}}\right)} \cdot S_{QE2}(f). \tag{49}$$

3.2.3. Derivation of $S_{\Phi_{VCO}}$

The next step is to estimate VCO noise. We assume that the PSD of VCO noise is

$$S_{\Phi_{VCO}}(f) = \frac{A_{VCO}}{f^2}. \tag{50}$$

The jitter of the non-SSC clock and the PSD of VCO noise are related as follows:

$$\begin{aligned}\phi^2_{\mathrm{JnonSSC,RMS}} &= \int_{-\infty}^{\infty} \left|H_{VCO}(j2\pi f)\right|^2 \cdot S_{\Phi_{VCO}}(f)df \\ &= \int_{-\infty}^{\infty} \left|H_{VCO}(j2\pi f)\right|^2 \cdot \frac{A_{VCO}}{f^2} df.\end{aligned} \tag{51}$$

After measuring the RMS jitter of the non-SSC clock, $\phi_{\mathrm{JnonSSC,RMS}}$, A_{VCO} can be obtained by (51).

Fig. 51 shows the jitter estimation and the calibration flow. First, the phase noise of the non-SSC clock is measured, and the natural frequency and peak values at the natural frequency are observed from the phase noise diagrams. Then the charge pump current is increased and the phase noise is measured again to identify another natural frequency and the peak value. Using these measured parameters and (38), α, which represents pole/zero

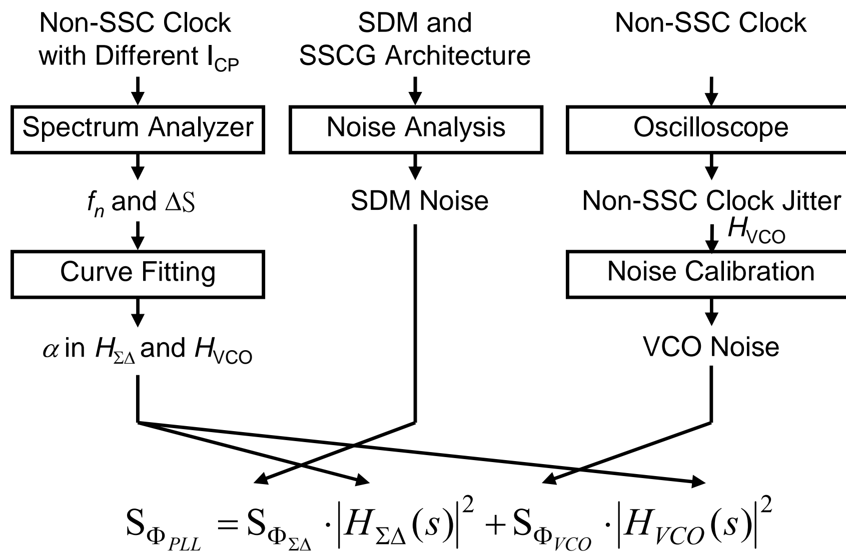
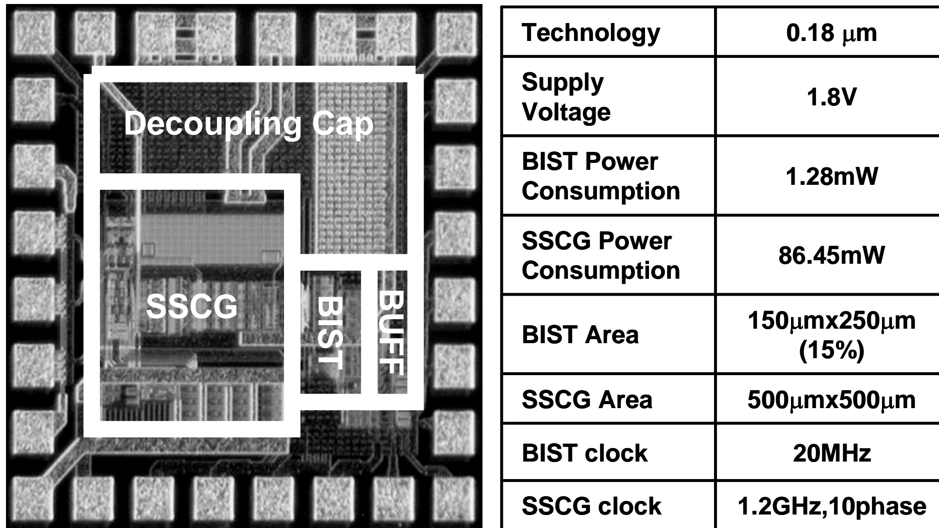


Fig. 51 Jitter estimation and calibration flow.



Technology	0.18 μm
Supply Voltage	1.8V
BIST Power Consumption	1.28mW
SSCG Power Consumption	86.45mW
BIST Area	150μmx250μm (15%)
SSCG Area	500μmx500μm
BIST clock	20MHz
SSCG clock	1.2GHz,10phase

Fig. 52 Chip photograph.

deviations due to process variation, is calibrated. To increase estimation accuracy, this step can be repeated several times for curve-fitting procedure. SDM noise is obtained theoretically. The RMS jitter of the non-SSC clock is measured by an oscilloscope, and (51) is applied to obtain the PSD of the VCO noise. After all the parameters are acquired, (17) is used to calculate jitter PSD and its RMS value.

Fig. 52 presents a chip photograph of this work and its specification. The technology used is 0.18μm CMOS with a supply voltage of 1.8V. The BIST circuit area is 15% of the SSCG, which includes the DFFs and phase shift detector of the MPD, but does not include

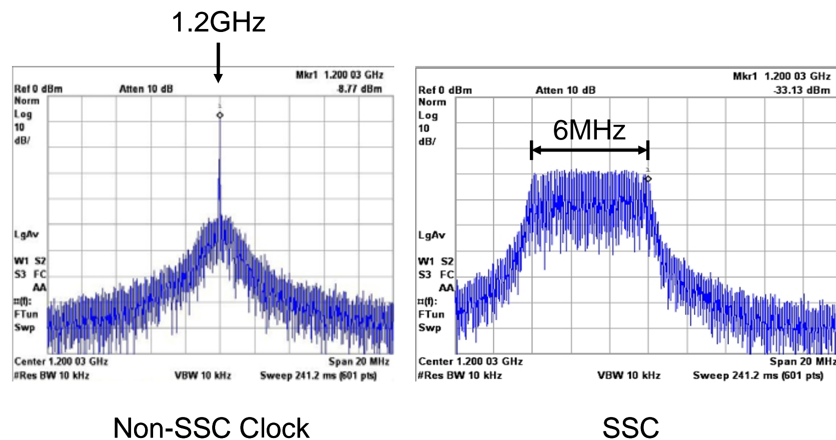


Fig. 53 PSD of the non-SSC clock and SSC measured using a spectrum analyzer.

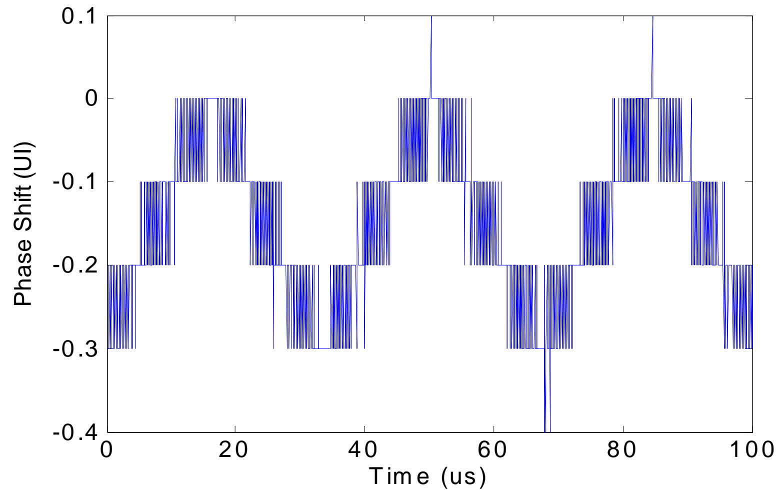


Fig. 54 Phase shift detector output signal.

the accumulator or other digital circuits. The BIST is operated at 20MHz, which is the same as the reference clock frequency. The SSCG is a fractional-N PLL with a 10-phase 1.2GHz VCO, a third-order loop filter, and a MASH-111 SDM to meet the SATA-III specification. In total, 10^4 data output by the phase shift detector are recorded by a logic analyzer. A personal computer is used for digital signal processing. The SSC and non-SSC clock are measured using a spectrum analyzer and oscilloscope.

3.3. Experimental Results

Fig. 53 shows the power spectrums measured using a spectrum analyzer of a non-SSC clock and an SSC. Measured results indicate that the non-SSC clock has a frequency of 1.2GHz and the SSC has a maximum frequency deviation of 6MHz (5000ppm) from a nominal frequency of 1.2GHz.

Fig. 54 shows the phase shift detector outputs. As expected, a 6MHz frequency deviation in a 50ns reference clock period causes a maximum phase shift of 0.3UI. With noise, an additional phase shift of 0.1UI can be generated. Fig. 55 shows the accumulated phase, which includes the ideal SSC phase drifting, phase quantization noise produced by

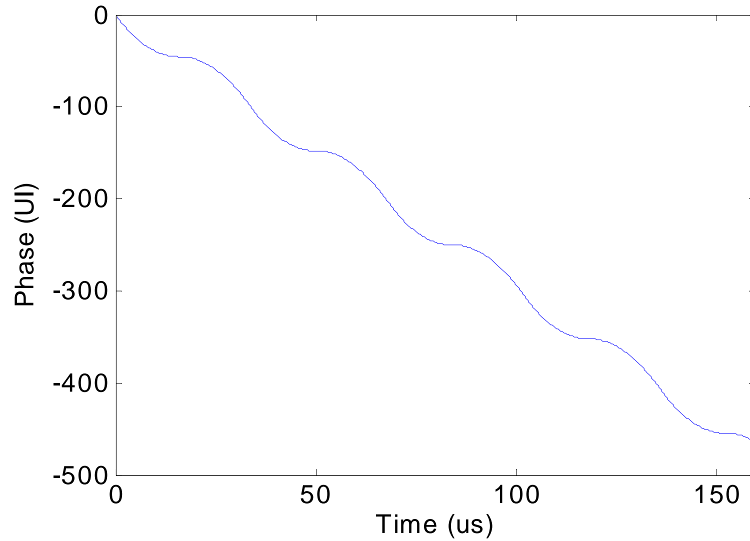


Fig. 55 Accumulator output signal.

the MPD, and jitter. The MPD output is passed through the digital filters and DSPs for further analysis.

Fig. 56 shows the SSC modulation profile of the SSC obtained using a fifth-order Infinite Impulse Response (IIR) LPF with a corner frequency of 500kHz. The corner frequency is selected to filter out as much noise as possible to retrieve the SSC phase and its harmonics. Measurement results for the BIST show that the frequency deviation is 6.1MHz, which agrees with the value measured by the oscilloscope, as shown in Fig. 53.

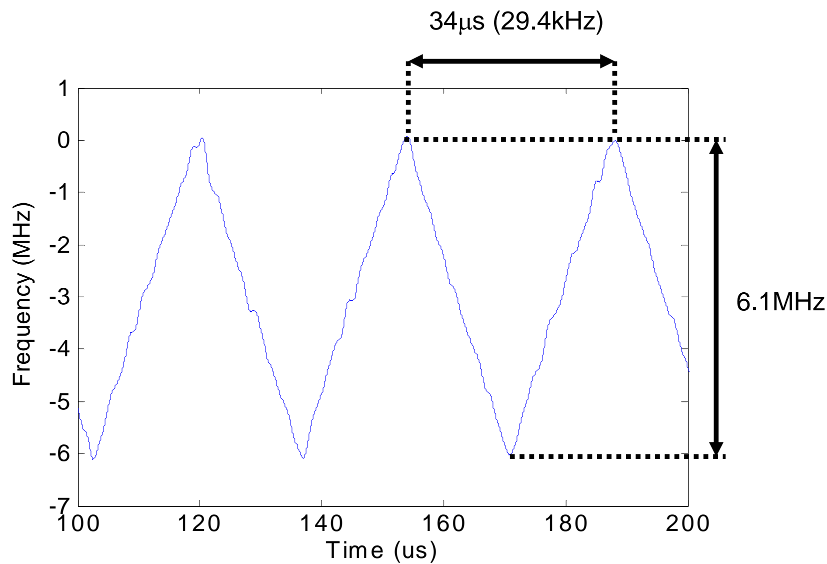


Fig. 56 Modulation profile of the SSCG.

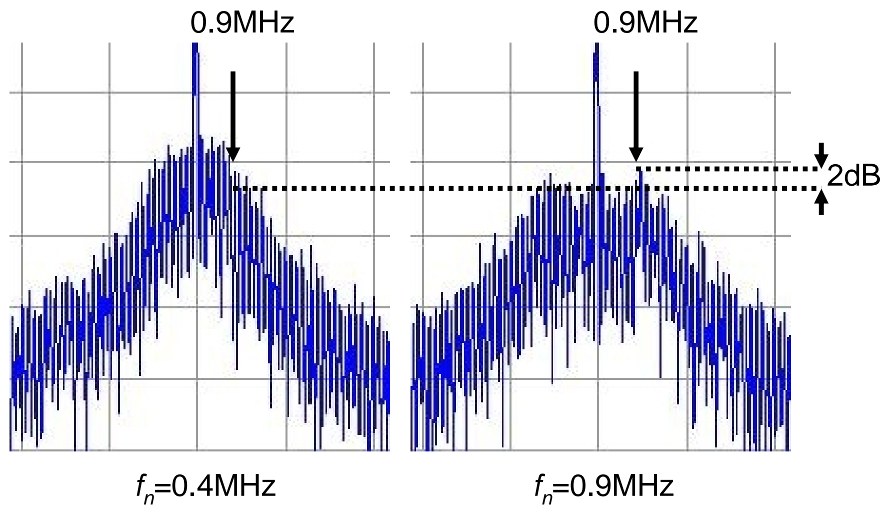


Fig. 57 Phase noise of non-SSC clocks with natural frequencies of 0.4MHz and 0.9MHz.

Modulation frequency is 29.4kHz, as compared with the design target of 29.3kHz.

The calibration process is done as follows: First, a phase noise of the non-SSC clock of the PLL is measured. Second, the charge pump current is increased and phase noise is measured again. The natural frequencies are observed from these two phase noise diagrams. Fig. 57 shows the phase noise of the non-SSC clocks with natural frequencies of 0.4MHz (f_{n1}) and 0.9MHz (f_{n2}), as defined in (38). The frequency, f, is chosen to equal f_{n2}. Comparing the phase noise at 0.9MHz (f_{n2}), the difference in phase noise, ΔS, is 2dB.

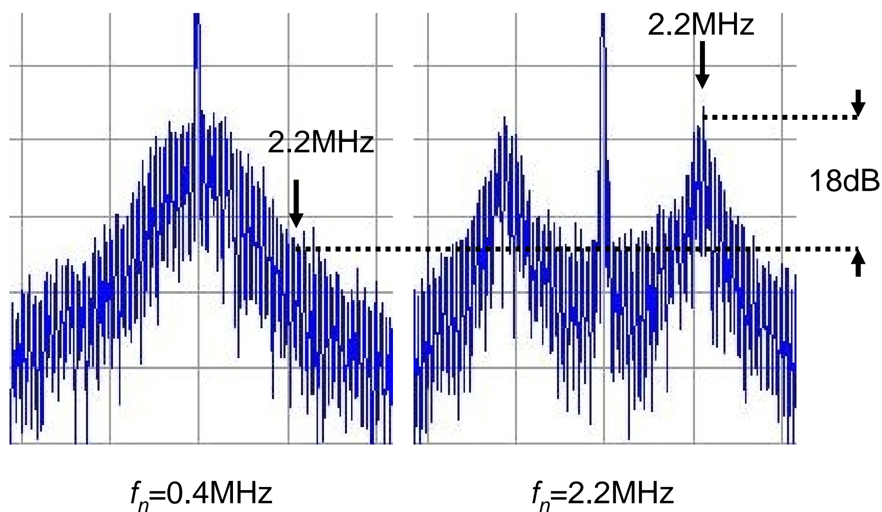


Fig. 58 Phase noise of non-SSC clocks with natural frequencies of 0.4MHz and 2.2MHz.

For curve-fitting procedure, this step is repeated several times with different charge pump currents. Fig. 58 shows the case with an f_{n2} of 2.2MHz. In this case, ΔS is 18dB at 2.2MHz.

Fig. 59 shows the curve-fitting procedure; the Y-axis is ΔH^2 and the x-axis is the natural frequency, f_{n2}. Additionally, f_{n1} is fixed at 0.4MHz and the f equals f_{n2}. Curves with different values of α are shown. The most appropriate value of α is 0.85 in this case. Calibration of the VCO noise is presented as follows.

Fig. 60 shows the non-SSC jitter with a natural frequency of 0.4MHz, which is measured by the oscilloscope. The measured RMS jitter is 12.59ps; thus, A_{VCO} in the PSD of VCO noise is estimated as $24\,(UI^2/Hz)$ in (50). The SDM noise is also analyzed using (39)–(49). The SSC has 10 phases; the frequency of the reference clock is 20MHz, and the frequency of the SDM is 60MHz. Fig. 61 shows the estimated $S_{\Phi_E}(f)$, $S_{\Phi_{PLLVCO}}(f)$ and $S_{\Phi_{PLL\Sigma\Delta}}(f)$. Each line represents the PSD of the jitter with different charge pump currents. The natural frequencies in this figure are 0.1MHz–2.3MHz. The optimal bandwidth of the PLL is 0.2MHz in this work. If the bandwidths exceed the optimal bandwidth, jitter

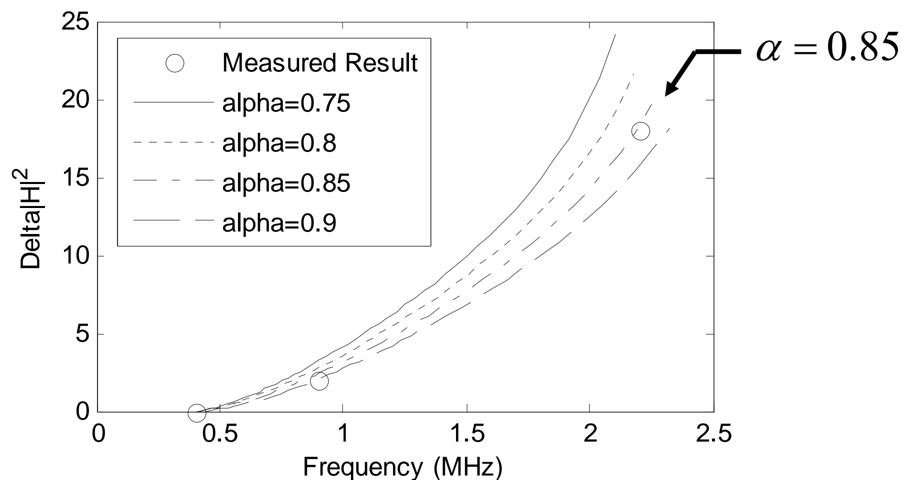


Fig. 59 Curve-fitting procedure for calibration of transfer functions.

increases as natural frequency increases.

Fig. 62—Fig. 64 show the estimated and measured values of PSDs of the HPF output signal $S_{\Phi_{JH+EH}}(f)$ in (11) for different natural frequencies. The estimated jitters (thick lines) are the sum of the PSD of SDM noise, VCO noise and quantization noise (thin lines). Measurement results are acquired from the HPF outputs. A fifth-order IIR HPF with a corner frequency of 500kHz is utilized. The corner frequency of 500kHz is chosen to filter out most of the SSC 30kHz phase drifting and its harmonics caused by the frequency modulation. Using calculation tools, it is estimated that a 500kHz fifth-order HPF can filter out most of the undesired SSC phase drifting with a modulation frequency of 30kHz. The unfiltered phase drifting is 0.003UI (RMS), that causes 1% error when jitter being measured is, for example, 0.02UI (RMS). If the corner frequency is decreased to 400kHz, the error increases to 4%. So a corner frequency of 500kHz is chosen if error below 1% is required. The BIST results of the SSCs are very close to the estimated results based on the phase noise of the non-SSC clock measured by a spectrum analyzer, as shown in Fig. 57 and Fig. 58, and the RMS jitter measured by an oscilloscope, as shown in Fig. 60.

It is shown in the measured results that the phase quantization noise is indeed a white noise as expected. However, the quantization noise may not be a white noise in every case, for example, in the case where the modulation profile changes to another type or the sampling rate is higher than the quantization noise. To conquer this problem, a dithering noise could be injected into the input of the phase detector to forcibly make the phase quantization noise be a white noise. After injecting dithering noise, an additional calibration method should be developed to estimate the magnitude of the dithering noise and cancel it from the measured results.

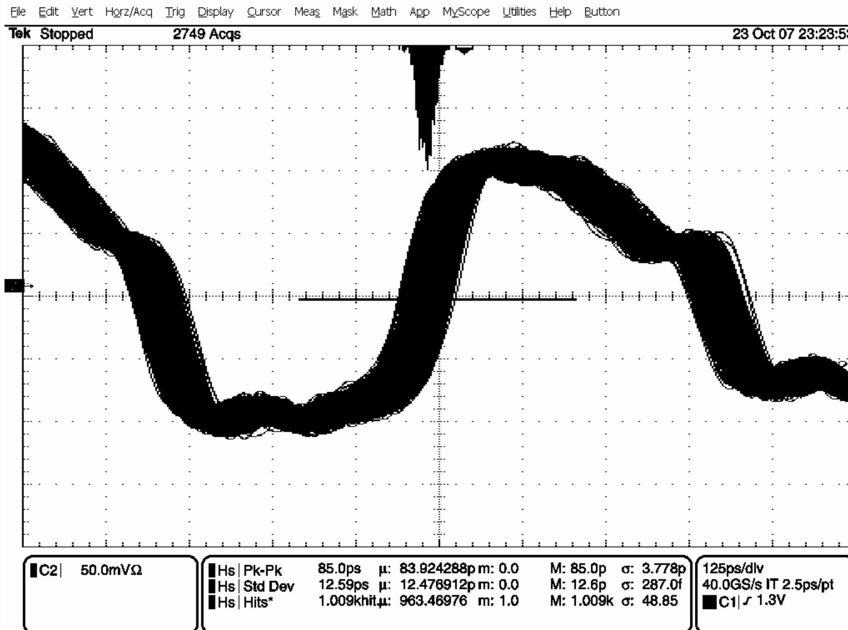


Fig. 60 Non-SSC jitter with a natural frequency of 400kHz.

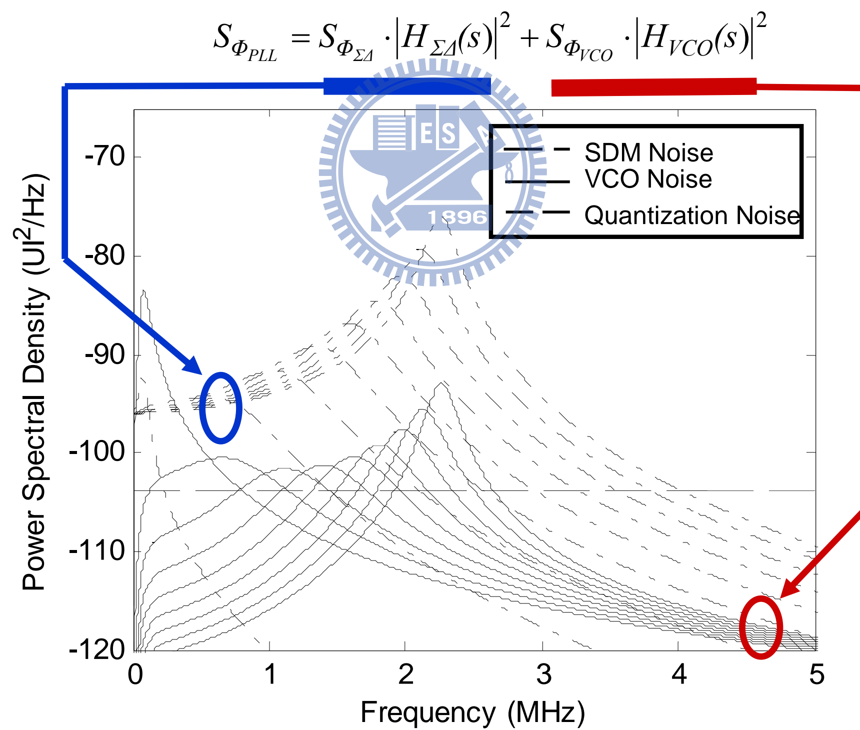


Fig. 61 Theoretical PSDs of the jitter and phase quantization noise.

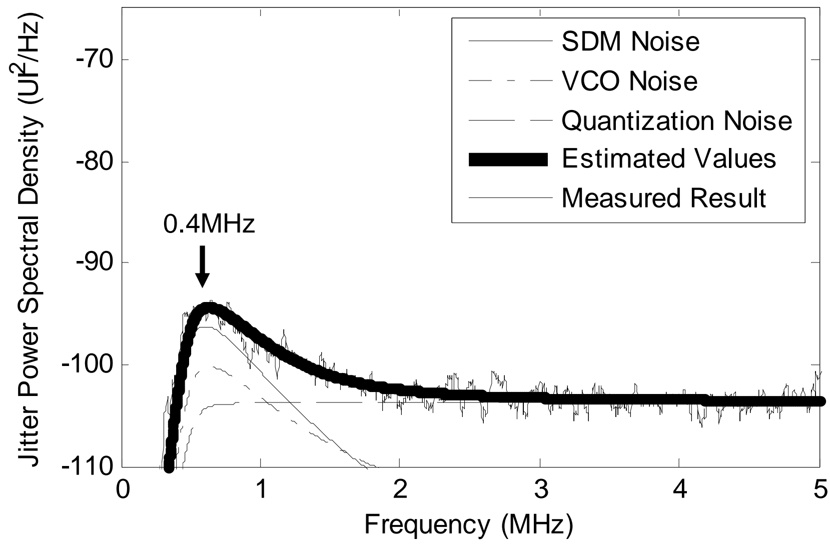


Fig. 62 Theoretical and measured PSDs of jitters (f_n = 0.4MHz)

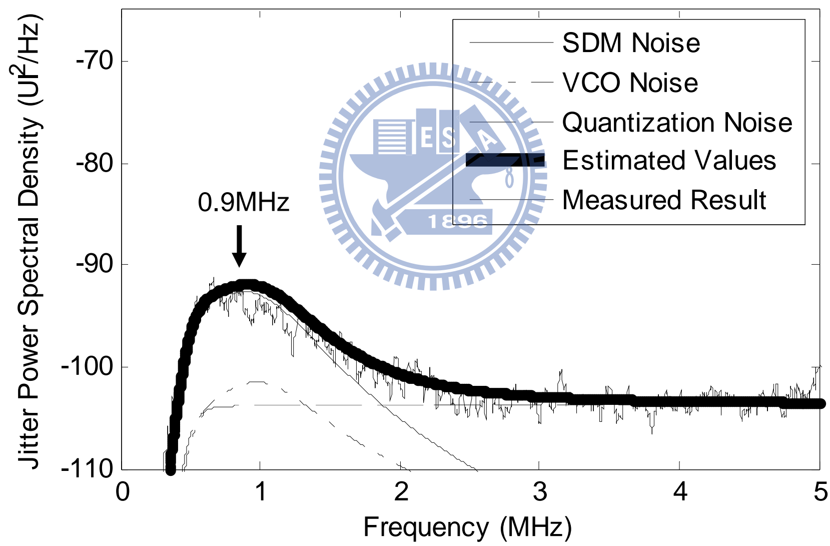


Fig. 63 Theoretical and measured PSDs of jitters (f_n = 0.9MHz)

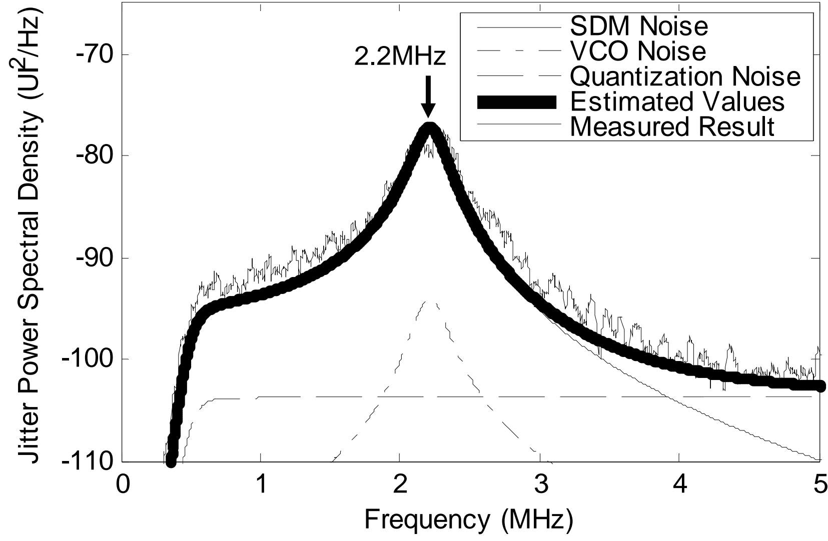


Fig. 64 Theoretical and measured PSDs of jitters (f_n = 2.2MHz)

Fig. 65 shows the histogram of the jitter plus high-frequency phase quantization noise calculated based on HPF output. The RMS jitter can be obtained statistically from the histogram. A fifth-order HPF with a corner frequency of 500kHz and a third-order HPF with a corner frequency of 3.6MHz are used. The latter complies with the SATA standard requiring $f_{BAUD}/1667$, where f_{BAUD} is 6Gbps. Fig. 66 shows BIST results and estimation results.

Table 5 lists the BIST results and estimation result for the 500kHz case and 3.6MHz case, which complies with the SATA standard. The maximal error is 0.026UI. Such errors are systematic errors as all measured results exceed estimated ones. This may be due to phase imbalance of the multi-phase clock. Such an imbalance generates an additional phase noise at the MPD output. Moreover, the estimation result is based on the non-SSC clock which does not involve the multi-phase clock. If phase imbalance is considered, (13) can be modified into

$$\phi^2_{JH,RMS} = \phi^2_{JH+EH+PIM,RMS} - \phi^2_{EH,RMS} - \phi^2_{PIM,RMS}, \tag{52}$$

where ϕ_{PIM} is phase imbalance noise, and PIM is phase imbalance. Comparing the estimation and BIST results, and using linear regression to estimate the unknown term, ϕ_{PIM}, the phase imbalance noise is likely to be 0.0053UI. However, this noise cannot be tested or calibrated individually, so the phase imbalance noise becomes the limit of the measurement range in this BIST approach.

Table 5 Comparison of measured and estimated RMS jitter.

Natural Frequency	500kHz High Pass Filter		
	Estimate (UI)	Measure (UI)	Error (UI)
0.4MHz	0.0200	0.0207	0.0007
0.9MHz	0.0319	0.0280	-0.0039
2.2MHz	0.1212	0.1316	0.0104
	3.6MHz High Pass Filter (Complies with SATA)		
Natural Frequency	Estimate (UI)	Measure (UI)	Error (UI)
0.4MHz	0.0034	0.0060	0.0026
0.9MHz	0.0042	0.0067	0.0025
2.2MHz	0.0298	0.0315	0.0017

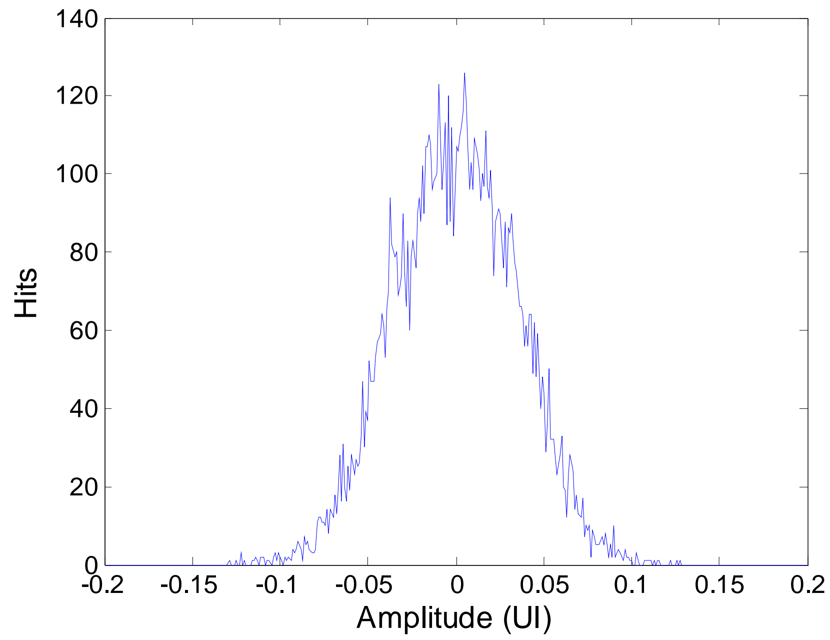


Fig. 65 Jitter histogram measured by BIST (f_n =0.4MHz)

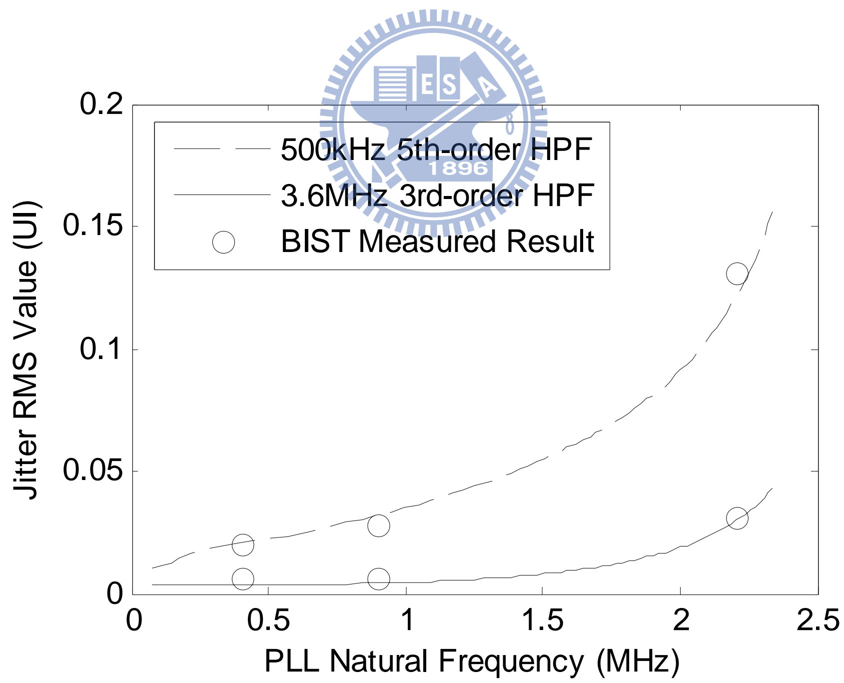


Fig. 66 Jitter RMS value, BIST vs. estimation results

Chapter 4

BIST for Clock and Data Recovery Circuits

4.1. Proposed BIST circuit

In this section, the proposed BIST circuit and the basic ideas are described. Although some ideas are widely used in today's circuit measurement design, such as delay line or bathtub curve-fitting, however, the BIST application for Bit-Error Rate (BER) estimation is new.

4.1.1. Timing Capture Scheme

The proposed BIST circuit measures relative timing jitter between the received Non-Return to Zero (NRZ) data and the recovered clock of CDR. As shown in Fig. 67, the NRZ data is sampled by three sampling phases to measure bit-errors. These sampling phases are generated from the negative edge of recovered clock and delay lines. The relative timing jitter between the NRZ data and the sampling phases are also depicted as probability density function (PDF) in Fig. 67.

We assume that the sampling ϕ_0 is the ideal sampling phase used for data recovering and the phases ϕ_- and ϕ_+ are non-ideal sampling phases. In [56], it defines a bit-error occurs if the phase difference exceeds 1/2 UI. Therefore when the timing of data transition edge is deviated to be slower or faster than ϕ_0, a bit-error occurs. If ϕ_- is used as sampling phase instead of ϕ_0, a bit-error occurs when the data transition edge is slower than ϕ_- or the next data transition edge is faster than ϕ_-. The same definition can also be

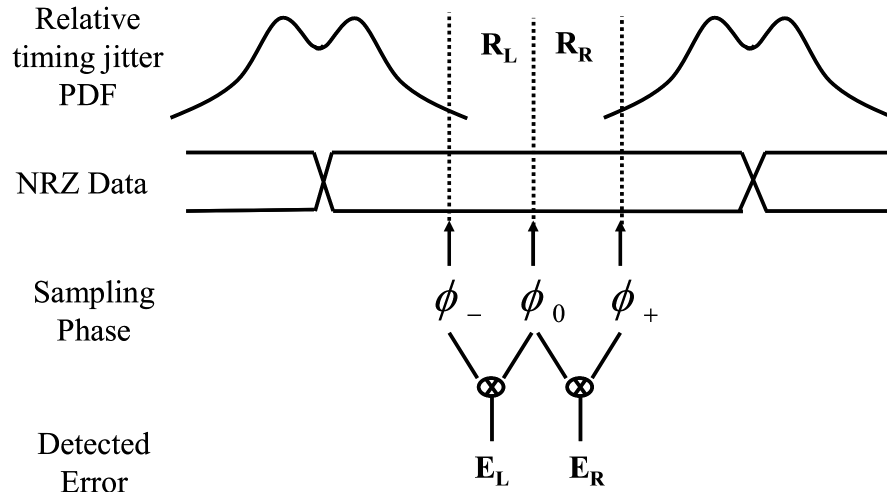


Fig. 67 Timing capture scheme of BIST and error detection

used for the ϕ_+ case.

For circuit simplification, we define a bit-error occurs when data transition edge is in the region R_L if ϕ_- is used for data recovering. We also define a bit-error occurs when data transition edge is in the region R_R when ϕ_+ is used for data recovering.

The error detection can be simply done by XORing the sampled results of ϕ_- and ϕ_0 or ϕ_+ and ϕ_0. If the data transition edge leads ϕ_0 and lags ϕ_-, the sampled results of the two phases must be different. The E_L and E_R signals are the outputs of XOR gates representing the occurrence of an error event. Then the number of error events is accumulated by a counter to calculate the BER. The BER can be obtained by dividing the number of error events by the total counting time of the counter.

4.1.2. Bathtub Curve-Fitting

Fig. 68 shows the PDF of data transition edges and the Cumulated Density Function (CDF) in log scale, which is known as a bathtub curve. The CDF is the integration of the PDF from infinite to the value, T. In this application, the PDF is the distribution of the relative jitter between NRZ data and VCO clock, and CDF is the probability that jitter is

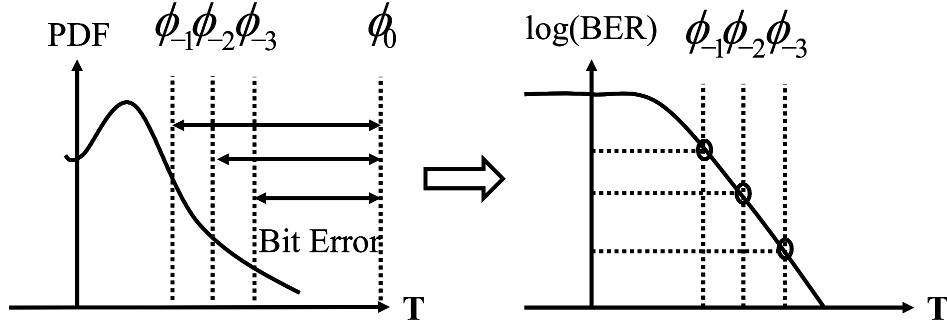


Fig. 68 Measured data points and bathtub curve.

larger than the value, T.

In order to plot the curve of CDF, different value of ϕ_{-} is given to measure the BER of different data points, e.g. ϕ_{-1}, ϕ_{-2}, and ϕ_{-3}. Several data points can be measured and then be applied to curve-fitting to decompose the Deterministic Jitter (DJ) and Random Jitter (RJ).

The bathtub curve-fitting algorithm [65][66] is briefly described here. The model used in bathtub curve-fitting is called "Double Delta Model". The Double Delta Model for DJ is represented by two delta functions with peak-to-peak amplitude, T_{DJ}.

$$P_{DJ} = \frac{1}{2}[\delta(t - \frac{T_{DJ}}{2}) + \delta(t + \frac{T_{DJ}}{2})]. \tag{53}$$

The RJ is a Gaussian function with standard deviation, T_{RJ}.

$$P_{RJ} = \frac{1}{\sqrt{2\pi T_{RJ}^2}} e^{\frac{-t^2}{2T_{RJ}^2}}. \tag{54}$$

The PDF of Total Jitter (TJ) is the convolution of the DJ and RJ PDFs.

$$P_{TJ} = P_{DJ} \otimes P_{RJ}. \tag{55}$$

The BER is the integrated tail of the jitter distribution from each side multiplying data transition density d.

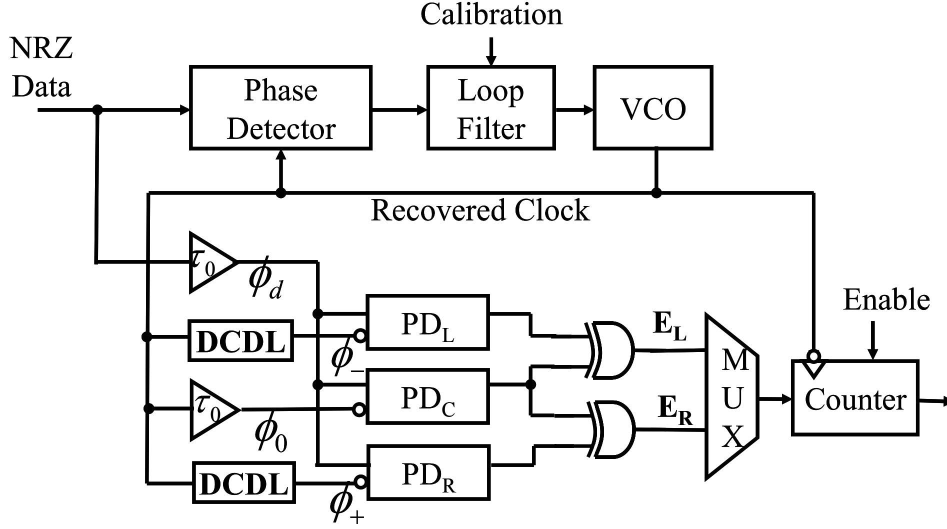


Fig. 69 Proposed BIST circuit.

$$
\begin{aligned}
BER(t_s, DJ, RJ) = d[&\int_{t_s}^{\infty} P_{TJ}(t, DJ, RJ)dt \\
&+ \int_{t_s}^{\infty} P_{TJ}(t - UI, DJ, RJ)dt]
\end{aligned}
\tag{56}
$$

Next step is to apply bathtub curve-fitting. The best curve is the curve which has the least mean-square error. The slope of the bathtub curve with BER less than about 10^{-3} is purely caused by the RJ. The data points with BER lower than 10^{-3} are better choices to fit the curve. It is worth to mention that if the input DJ is not double-delta distributed, using double-delta function will cause error. In real cases, the DJ is composed of Sinusoidal Jitter (SJ), Inter-Symbol Interference (ISI), and Duty Cycle Distortion (DCD). More analysis is given in [65] [66].

4.1.3. Circuit Description

Fig. 69 shows the proposed BIST circuit. It is composed of a Digitally Controlled Delay Lines (DCDLs), delay buffers, phase detectors (PDs), XOR gates, a multiplexer (MUX) and a binary counter. Input signals are the NRZ data and the recovered clock of CDR. Output signals are digital signals of the binary counter.

The combination of the delay buffers and DCDL generates the sampling phases as mentioned before. Delay buffers are the matched devices that have the same delay τ_0 and do not change the phase differences of the NRZ data and the recovered clock. The maximum delay of the DCDL for generating the sampling phase ϕ_- is equal to or smaller than that of the delay buffers ϕ_0, and the minimum delay of another DCDL for generating the sampling phase ϕ_+ is equal to or larger than that of the delay buffers. The resolution of the DCDL is a key parameter. The slope of the bathtub curve is caused by RJ. If the magnitude of the RJ is small, the slope will be steep and lesser data points can be measured when the resolution of DCDL remains constant. The resolution is designed to roughly equal the magnitude of RJ, which is a few picoseconds in PCE Express for example. The implementation of the DCDLs is the main issue. For example, if the tuning range of 200ps and resolution of 4ps are required, a 6bit DCDL is capable of doing it. It is not difficult to implement this DCDL using recent CMOS technology. Another issue is that the jitter induced by DCDL should be as small as possible. It should be carefully designed to make sure that there is no ISI when NRZ data passes through the delay buffer.

The PD is made of a single D Flip-Flop (DFF). The nonzero offset of the PD can be absorbed by DCDL and be calibrated later. The XOR gates detect the transition edges and then output bit error signals E_L and E_R. MUX is used for reducing the hardware, thus one counter is enough to calculate bit error rates in all cases.

BER is calculated by the counter. The measured result is analyzed using the Binomial Process for its specific statistical character. The mean and variance of the measured BER P_{em} is derived as

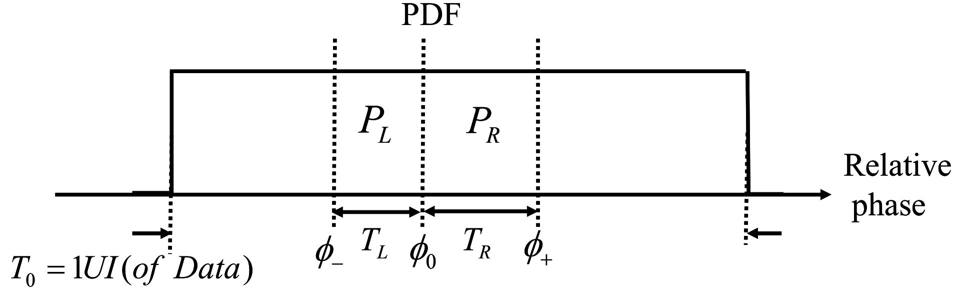


Fig. 70 PDF of phase difference between NRZ data and free running VCO clock

$$
\begin{aligned}
& n = N_0 \\
& p = P_e \\
& \mu_{P_{em}} = \frac{np(1-p)}{n} \approx P_e \\
& VAR(P_{em}) = \frac{np(1-p)}{n^2} \approx \frac{P_e}{N_0},
\end{aligned}
\tag{57}
$$

where n is the number of the trials, p is the probability of success, N_0 is the counting number for measurement, P_e is the actual bit error rate, and P_{em} is the measured BER.

4.2. Calibration

The process variation causes variation of the delay time of the buffers and DCDLs. Calibration of the delay time is the main problem to be solved. This idea of calibrating a Time-to-Digital Converter (TDC) by two uncorrelated signals [15] and free-running VCO [12][13] is applied.

For two uncorrelated signals, the phase difference between them is from 0 to 1UI and uniformly distributed. Fig. 70 shows the PDF of the phase difference between the NRZ data and the VCO clock if the CDR is unlocked and the two signals are uncorrelated. The PDF is a uniform distribution and its width is equal to one unit interval (UI) of NRZ data. The probability that the phase of NRZ data leads ϕ_0 but lags ϕ_- is proportional to $\phi_0 - \phi_- = T_L$.

The CDR can be made unlocked by supplying a constant voltage to the loop filter of

CDR to switch the VCO into free running mode. Then the VCO clock is uncorrelated to NRZ data even if the VCO clock frequency remains constant.

The phase difference T_L is measured by counting the events that the NRZ data phases which leads ϕ_0 but lags ϕ_- for N_C clock period time. Then the number of events over total counting time should be proportional to the phase difference T_L.

The accuracy of the measurement depends on the counting time. The mean and variance of the calibration results of T_L and T_R can be calculated by applying the Binomial Process as mentioned before.

4.3. BIST Operation Steps

The BIST operating steps including calibration, testing, and curve-fitting is presented. First, the delay of DCDL is set to its minimum value and the phase difference T_L of ϕ_- and ϕ_0 is the smallest. VCO is switched to free-running mode to calibrate the phase difference TL.

In the second step, the CDR is switched into locked mode and the BER is measured. Therefore, one data point for bathtub curve-fitting is obtained by combining the phase difference T_L and the corresponding BER.

The first step and second step are repeated for several times with different delay time of DCDL and several data points are obtained. These data points and curve-fitting algorithm are combined to find the optimum bathtub curve for DJ and RJ values. Theoretically, two to three data points of bathtub curve is enough to decompose the DJ and RJ values.

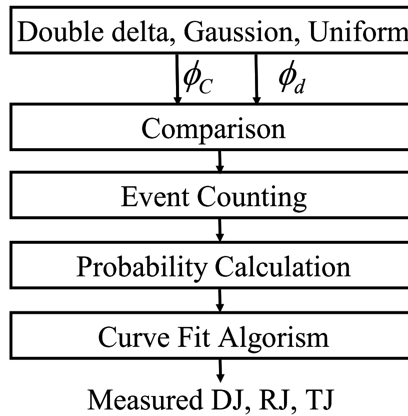


Fig. 71 System level simulation flow of BIST

4.4. Simulation Results

Since HSPICE simulation consumes a lot of time and it is almost impossible to fully verify the BIST function, the system level simulation with Matlab is adopted. The relative phase difference is modeled as a random variable, ϕ_d, which is the combination of the double delta DJ and Gaussian distribution RJ. If BIST is operating in calibration mode, phase difference, ϕ_C, is modeled as a random variable with a uniform distribution.

Fig. 71 shows the system level simulation flow of the BIST. DJ and RJ are random variables generated by the built-in function of Matlab. Adding up DJ and RJ variable can generate the TJ random variable, ϕ_d. Secondly, The random variable, ϕ_d, is compared with the constant value, ϕ_-. This step is repeated for N_o times and the comparison results are summed to obtain the measured BER. In calibration mode, another random variable, ϕ_C, with a uniform distribution is generated, and the step is repeated for N_C times. The transition density d is set to be 0.5.

The process is repeated three times with different values of ϕ_- to obtain tree data points and then the curve-fitting algorithm is applied to estimate DJ, RJ, and TJ at BER=10^{-12} level. The same flow is applied to the ϕ_+ case. The parameters of BIST are

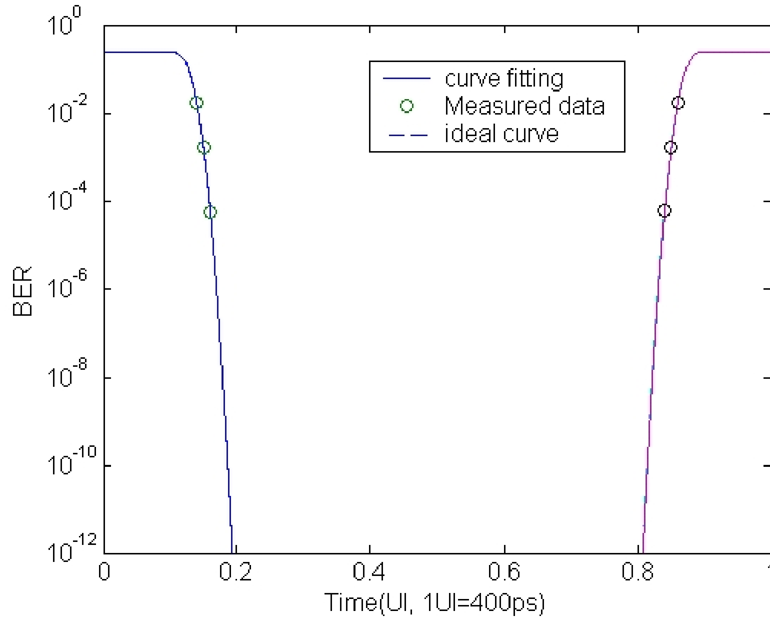


Fig. 72 Measured data points and curve-fitting compared with ideal bathtub curve

shown in Table 6.

Fig. 72 shows one case of simulation result. DJ=100ps and RJ=4ps are input to the simulation program and the measured result are DJ=100.4ps at left side of the bathtub curve and DJ=100ps at the right side, and RJ is 3.96ps at both sides. The TJ at BER=10^{-12} level is 155.16ps, compared to ideal TJ=155.52ps.

More simulation results are shown in Table 7. The measured jitter of the left side and right side of bathtub curve is unbalanced. The error is caused by the finite counting length of N_o and N_C. However, the errors of the TJ are all smaller than 3%. The DCDL resolution is also an important parameter. If the resolution is not high enough, the number of useful data points being sampled is not enough for curve-fitting. There is a trade-off between the hardware and the accuracy.

To the best of our knowledge, no BIST for jitter decomposition is found, so the decomposition methods of other techniques are chosen to compare with this work. Table 8 shows the comparison of this work and various techniques [66]. Using the TJ measured by

BERT as a reference, one can find that the measured result using an oscillator has the worst accuracy. TIA has a very good performance. The measured result of the BIST circuit has an error of 2.5ps, which is acceptable for product testing.

Table 6 Parameters of BIST.

Operation speed	2.5Gbps
One unit interval T_0	400ps
Data transition density d	0.5
Calibration time N_c	10^6 VCO clocks
Test time N_0	10^6 VCO clocks
DCDL resolution	4ps
Curve fit data point	3 points
DJ range (Double delta)	30ps~300ps
RJ range (Gaussian)	2ps~6ps

Table 7 Simulation results.

Input jitter (ps)			Measured jitter (ps)				
DJ_I	RJ_I	TJ_I	DJ_{OL}	RJ_{OR}	DJ_{OL}	RJ_{OR}	TJ_O
30	2	57.76	30	2	30.4	1.92	57.4
30	6	110.84	34	5.28	28.4	6.2	113.28
300	2	327.76	300.04	1.96	299.6	2.04	327.76
300	6	383.28	300	6.08	294.8	6.84	387.0
100	4	155.52	100.4	3.96	100	3.96	155.16

Table 8 Comparison of different jitter decomposition techniques.

2.5Gb/s	RJ(ps)	DJ(ps)	TJ(ps)	Error(ps)
BERT Direct at 10^{-12} BER	-	-	75	-
BERT Bathtub 2-point Q-factor	6.25	9.5	95	20
Wavecrest SIA-3000	3.42	31.3	75	0
Curve-fitting	4.29	14.7	75.7	0.7
Oscilloscope(1500 Waveforms)	-	-	47	-28
This work (Input jitter for Simulation)	6	30	110.8	-
This work (Simulation result)	5.28/6.2	34/28.4	113.3	2.5

Chapter 5

Conclusions and Future Work

5.1. Conclusions

The first part of this work presents a BIST circuit to measure charge-pump PLL jitter. Using the proposed TDC, the resolution can be as good as sub-picoseconds or even better, at the expense of measurement time. When the loop filter and VCO of the tested PLL are utilized as part of the BIST circuit, the area overhead is small. The chip is fabricated using 0.18μm CMOS technology. The BIST circuit is run at 78.125MHz and the VCO of PLL is run at 1.25GHz. The measurement results show a resolution of 1.17 picoseconds, a measurement error of 14.6%, and an area overhead of 36.7% are achieved.

The second part of the thesis presents the feasibility of a built-in jitter measurement method for multi-phase SSCGs. This method is based on a 10-phase phase detector and DSP algorithms for extracting the jitter histogram and power spectral density, with the timing jitter definition complying with the SATA standard. The method for measuring the modulation profile, which includes modulation frequency and frequency deviation, is also presented. The jitter estimation method that correlates SSC jitter and non-SSC jitter is used to validate the jitter measurement methodology. A 1.2GHz 10-phase SSC PLL with the proposed jitter measurement circuit was designed and implemented using 0.18μm CMOS technology. Measurement results show that the difference between the estimated and BIST results are less than 0.0026UI.

The third part of this work proposes a BIST circuit for CDR jitter measurement and BER estimation. Using a new definition of a bit-error combined with the traditional

bathtub curve-fitting algorithm, the total jitter at BER=10^{-12} level can be estimated without consuming a lot of time, and the hardware overhead is small. The calibration method reusing the free-running VCO of the tested CDR is also presented. The simulation results show that the measurement error is less than 3% and the random jitter being measured can be as small as 2ps when deterministic peak-to-peak jitter of 300ps exists.

5.2. Future Work

The idea of the BIST for SSCGs could be applied to non-SSC clocks. By doing so, it is expected that using a coarse digitally controlled delay line or a coarse interpolated multi-phase is enough to achieve high-resolution TDC. But some wobbling or dithering technique should be adopted to generate a frequency modulation effect similar with that of the SSCs. A calibration method should also be developed to separate the dithering and wobbling noise from the tested clock.

There is an assumption in the SSCG BIST as mentioned in Chapter 3 that the phase quantization noise of the phase detector is a white noise. If the quantization noise is white, after low-pass filtering, the quantization noise is filtered out and the mean of the jitter is extracted. When this approach is applied to a non-SSC clock, the phase quantization noise is apparently not a white noise. For example, if the jitter is smaller than one LSB of the phase detector, the output of the MPD is always stuck in one code. In order to make the quantization noise be a white noise, a dithering noise should be added at the input path of the phase detector. The frequency of the dithering noise is another important issue, for it will determine the power spectral density (PSD) of the quantization noise. Additionally, the probability density function (PDF) and the magnitude of the dithering noise should also be considered, for it may also determine the PSD of the quantization noise.

The second assumption of the SSCG BIST is that the quantization noise and jitter are

independent. The independency of the quantization noise is naturally achieved by the existence of a phase drifting caused by the frequency modulation. If jitter and quantization noise are independent, the PDF of the summed signal is the convolution of their respective PDFs. The independency of these two signals can be simply verified by observing the PDF of the summed signal and their respective PDFs. For non-SSC clock, the PDF of the summed signal is not the convolution of the PDFs of jitter and quantization noise, so adding a wobbling noise to the input signal path is needed for making the quantization noise and jitter independent.

The resolution of the coarse TDC is another issue to be discussed. Typically, dithering noise should be larger than the resolution of the TDC. However, if the resolution of TDC and the dithering noise is much larger than the jitter, the dithering noise will dominate the measured results and the measurement error will be large. It is necessary to assess the impact of the magnitude of the dithering noise to the measurement accuracy.

Calibration is needed for separating dithering and wobbling noise. The systematic errors due to phase imbalance of the multi-phase clock should also be calibrated. Calibration can be simply done by switching the tested non-SSC clock to an ideal clock, so the output signal contains only the dithering, wobbling and phase imbalance noises. Then the tested clock is input to the BIST circuit. Theoretically, the variances of the jitter and the calibrated dithering, wobbling and phase imbalance noise can be linearly summed if they are independent. The histogram of the jitter can also be obtained by traditional decomposition methods.

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