Chapter 1

Introduction

1.1 The Background and Motivation

In recent years the demand of III-V HEMTs for high-frequency applications is increasing especially in major two areas: high-speed optical fiber communication systems and high-frequency wireless systems. For development of the wireless communication systems, the requirements for low cost, low power consumption, high-level integration and high frequency operation devices become more and more necessary. For high frequency applications, compound semiconductor devices such as GaAs pseudomorphic high electron mobility transistors (PHEMTs), $In_xGa_{1-x}As$ metamorphic HEMTs (MHEMTs), conventional lattice-matched or pseudomorphic InAlAs/InGaAs/InP HEMTs (InP HEMTs), and InAs-channel HEMTs, have shown superior performance as compared to Si devices for high-frequency applications. $In_xGa_{1-x}As$ HEMT have received much attention due to its capability of being operated at very high frequency region with ultra-low power consumption. Many efforts have been made to improve the device performance. Devices with higher carrier concentration, higher electron mobility and shorter gate length by use of refined heterojunction structure and novel gate shrinkage technique have been demonstrated and have shown outstanding performances. In this study, high RF, outstanding performance and low-power consumption $In_xGa_{1-x}As$ and InAs-channel HEMTs with sub-micron gates were developed by using advanced device structures and novel gate definition technologies. In

addition, InAs-channel MOS-HEMTs with high-κ gate dielectric Al_2O_3 was demonstrated for an alternative device beyond Si CMOS.

1.2 Overview of High Electron Mobility Transistors (HEMTs)

High electron mobility transistor (HEMT) is one of the most mature III-V semiconductor transistors which rely on the use of heterojunction for its operation. Fig. 1.1 shows a conventional HEMT structure. As compared with the silicon-based transistors, such as metal-oxide-semiconductor field effect transistors (MOSFETs) and bipolar-junction transistor (BJTs), GaAs transistors exhibit inherent advantages over Si-based transistors for high frequency applications [1-1].

GaAs HEMT was invented by Takashi Mimura [1-2] and have been successfully manufactured and commercialized for many applications. The epitaxial layers of the HEMT structure are designed to form two-dimension electron gas (2-DEG) in the channel layer with an un-doped spacer in the high band gap material to separate the ionized donors from the channel to increase the electron mobility. Consequently, GaAs HEMTs have superior carrier transport properties due to the band-gap engineering design.

Conventional HEMT structure is consisted of AlGaAs barrier layer and GaAs channel structure. The band gap discontinuity between AlGaAs/GaAs increases as the Al content increases and the large discontinuity in the band gap results in better confinement of the electrons in the channel. However, the deep-complex center (DX center) phenomenon exists while Al content is over 20% which traps the electrons and influences the device performance [1-1]. In order to avoid the DX center phenomenon and increase the electron mobility, AlGaAs/InGaAs/GaAs pseudomorphic HEMT (PHEMT) structure was developed. InGaAs is a preferred channel material over GaAs for HEMTs because of its superior transport

properties as compared to GaAs. The In content in the channel was increased to enhance the electron transport properties and improve the confinement of the carriers in the channel. However, InGaAs channel in PHEMTs is limited to an In content of 25% [1-3] to avoid lattice relaxation of the channel.

Higher In mole fractions are feasible in the HEMT structure on InP substrates, e.g., lattice matched $In_{0.52}Al_{0.53}As/In_{0.53}Ga_{0.47}As$ heterostructures. InP-based HEMTs have shown very high frequency characteristics, low noise figure, high gain, and high efficiency as compared to the GaAs-based PHEMTs [1-4]-[1-5]. Therefore, the high In content in the InGaAs channel can be achieved in spite of the large lattice mismatch between the active epilayers and the substrate. The relation between the lattice constant and the bandgap of $In_xAl_{1-x}As$ and $In_yGa_{1-y}As$ is shown in Fig. 1.2.

Generally, higher electron mobility and velocity can be realized by the increase of the Indium content in the InGaAs channel, which makes InAs-channel heterostructure FETs (HFETs) well suitable for low-power and high-speed logic applications due to the extremely high electron mobility of more than 30000 $cm^2/V \bullet s$.

Therefore, this study will focus on the development of high performance InAs-channel HEMT technology. The high frequency performance of the HEMTs can be improved by optimizing the device structure and using a sub-micron gate length. A shorter gate is very essential for achieving ultra-high frequency operation. Therefore, in next section we will discuss the technologies of sub-micron gate fabrication.

1.3 Sub-micron Gate Definition

In this work, a nano-fabrication technology of the T-shaped gate for the ultrahigh-speed $In_xGa_{1-x}As$ HEMTs is developing. E-beam lithography using tri-layer resist was employed to

form the expected resist profile for nanometer T-shaped gate formation. High-resolution scanning electron microscope (SEM) was then used to measure the dimension of the footprint.

Fig. 1.3 summarizes the process flow of the fabrication of a T-shaped gate. First, the tri-layer resist of ZEP-520/PMGI/ZEP-520-12 (150nm/450nm/250nm) was coated on the substrate. The first E-beam exposure for top two layers was used to only define the head (Tee-top) of the T-shaped gate by modulating the exposure doses. After that, the ZEP and PMGI development were executed by using xylene and MF622, respectively. Then, single center exposure with high dose was used to define the footprint of the bottom ZEP-520 layer also developed by xylene. The other tri-layer resist of ZEP-520/PMGI/FEP-171 (top layer is FEP-171) was also tried to compare with the top-layer ZEP-520-12.

In addition, the samples were descumed using inductively coupled plasma (ICP) in a 1:3 gas mixture of O_2 and Ar for 30 sec. Finally, Ti/Au (10nm/30nm) Schottky gate metal layers were sequentially deposited on the InP substrate by electron gun evaporation. After lift-off process using ZDMAC solution, the 50-nm T-shaped gate with thickness of about 400nm was form on the substrate.

Fig. 1.4 shows a cross sectional SEM image of the profile of ZEP-520/PMGI/ZEP-520-12 (180nm /450nm/240nm) tri-layer resist after E-beam lithography and development. The desired short foot-print was defined as 50nm for the bottom ZEP-520. The foot-print was matched with the center Tee-top opening correctly, and the under-cut profile was made for gate-metal lift-off. The Fig. 1.5 shows the cross sectional SEM view of the T-shaped gate. The Ti/Au (10/30nm) gate metal was deposited by E-gun evaporator and the gate length at the bottom is about 50nm.

The multilayer ZEP-520/PMGI/FEP-171 (top layer is FEP-171) was also tried to compare with the difference of the top-layer ZEP-520-12. The FEP-171 is also an E-beam positive resist for mask process which was made by FUJIFILM Arch Company. There are

some problems if the top layer is FEP-171. The T-top opening is too wide and not easy to be controlled. On the other hand, the top FEP-171 was attacked by the xylene development. Therefore, the ZEP-520-12 is a more suitable top layer than FEP-171 for our E-beam lithography process.

1.4 Outline of this dissertation

This dissertation covers the study of InGaAs Power HEMTs and InAs-channel HEMTs for high speed, low power consumption, and logic applications. It is divided into 8 chapters. In chapter 2, the details of the fabrication process of the $In_xGa_{1-x}As$ and InAs HEMT are introduced. The epi-structure, layout design, and front-side metallization are described. In addition, the DC and RF characterization of the device are studied and stated in chapter 3.

In chapter 4, a 70-nm $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ power MHEMT with double δ-doping was fabricated and evaluated. The excellent DC and RF performance of the 70-nm power MHEMT shows a great potential for Ka-band power applications.

In chapter 5, an 80-nm InP HEMT with InAs channel and InGaAs sub-channels has been fabricated. The high current gain cutoff frequency (f_t) of 310 GHz and maximum oscillation frequency (f_{max}) of 330 GHz were obtained at V_{DS} = 0.7 V due to the high electron mobility in the InAs channel. With the design of InGaAs/InAs/InGaAs composite channel, the impact ionization was not observed until the drain bias reached 0.7 volt, and at this bias the device demonstrated very low gate delay time of 0.63 psec. The high performance of the InAs/InGaAs HEMTs demonstrated in this study shows great potential for high speed and very low power logic applications.

In chapter 6, an InAs-channel high-electron-mobility transistor (HEMT) with an 80 nm gate length for ultralow-power low-noise amplifier (LNA) applications has been fabricated

and characterized on a 2-inch InP substrate. Small-signal S-parameter measurements performed on the InAs-channel HEMT at a low drain-source voltage of 0.2 V. Such a device also demonstrated a higher associated gain and a lower noise figure than other InGaAs-channel HEMTs at extremely low dc power consumption. These results indicate the outstanding potential of InAs-channel HEMT technology for ultralow-power space-based radar, mobile millimeter-wave communications and handheld imager applications.

In chapter 7, n-type metal-oxide-semiconductor HEMT (MOS-HEMT) devices with an InAs-channel using atomic-layer-deposited Al_2O_3 as gate dielectric have been fabricated and characterized. Device performance of a set of scaled transistors with and without high-k gate dielectric Al_2O_3 have been compared to determine the optimum device structure for low-power and high-speed applications.

Finally, chapter 8 is the conclusion of the dissertation. The InAs HEMTs show excellent DC and RF performances and demonstrated great potential for high-frequency applications.

FIGURES:

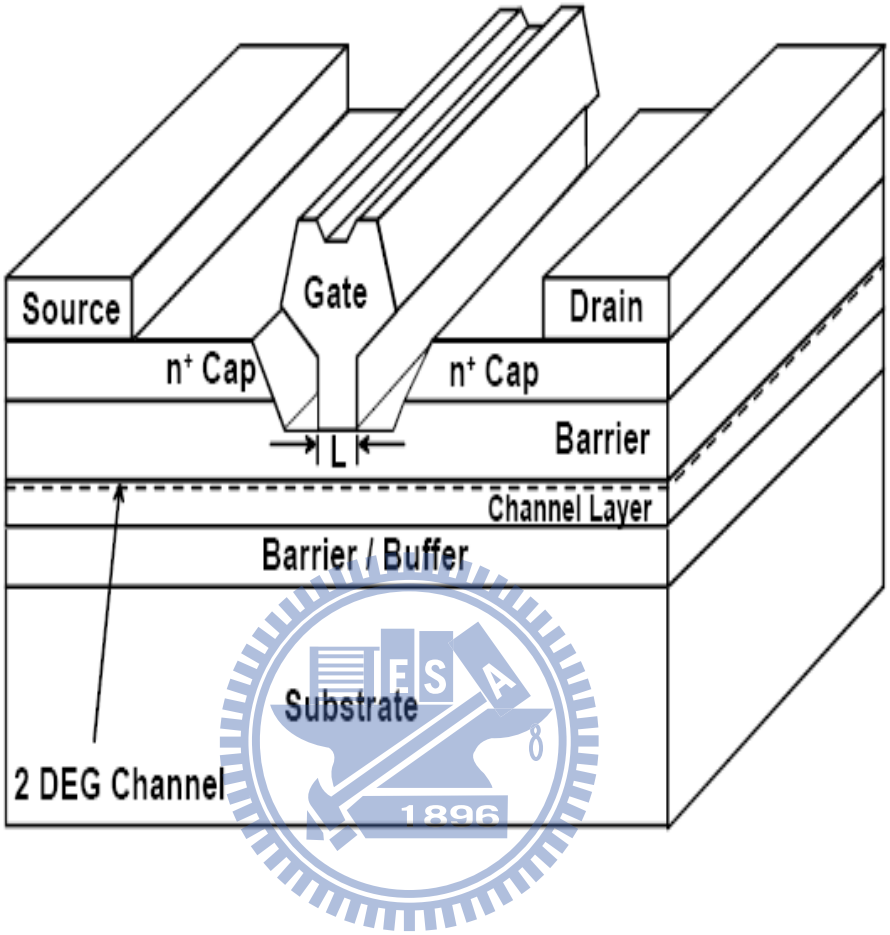


Figure 1.1 Conventional HEMT structure.

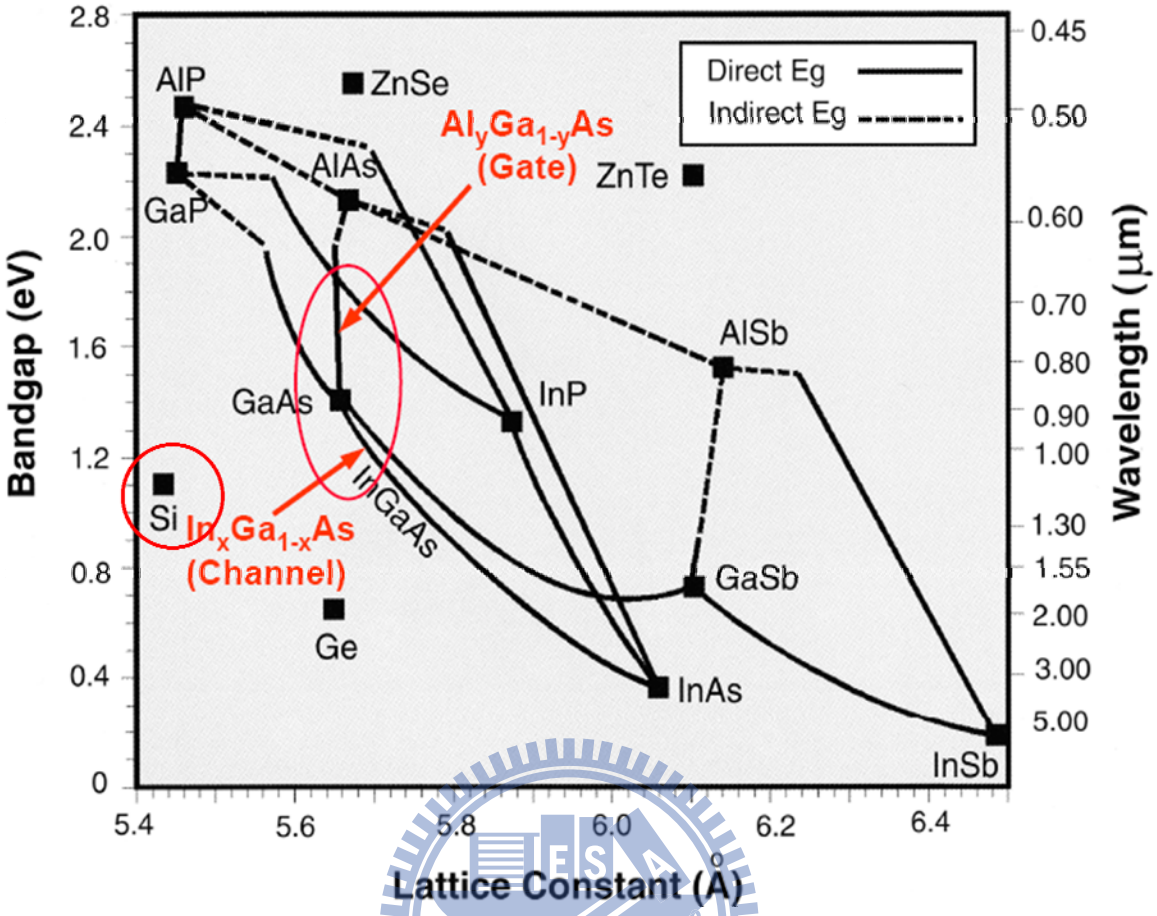


Figure 1.2 Energy band gap v. s. lattice constant for the $In_xAl_{1-x}As/In_yGa_{1-y}As$ system.

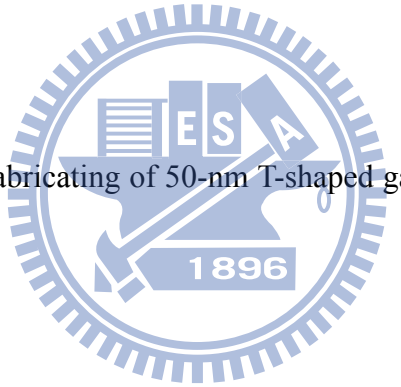


Figure 1.3 Process flow of fabricating of 50-nm T-shaped gate using E-Beam lithography and tri-layer resist.

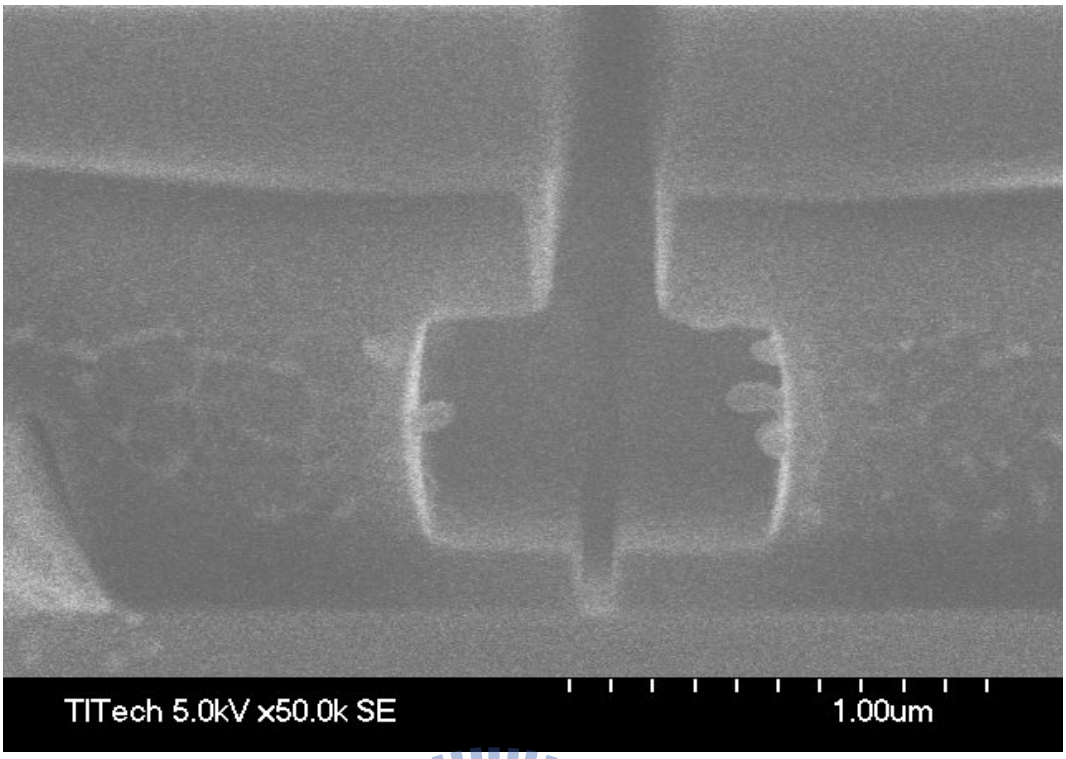


Figure 1.4 Cross sectional SEM image of the profile of tri-layer resist after E-beam lithography and development.

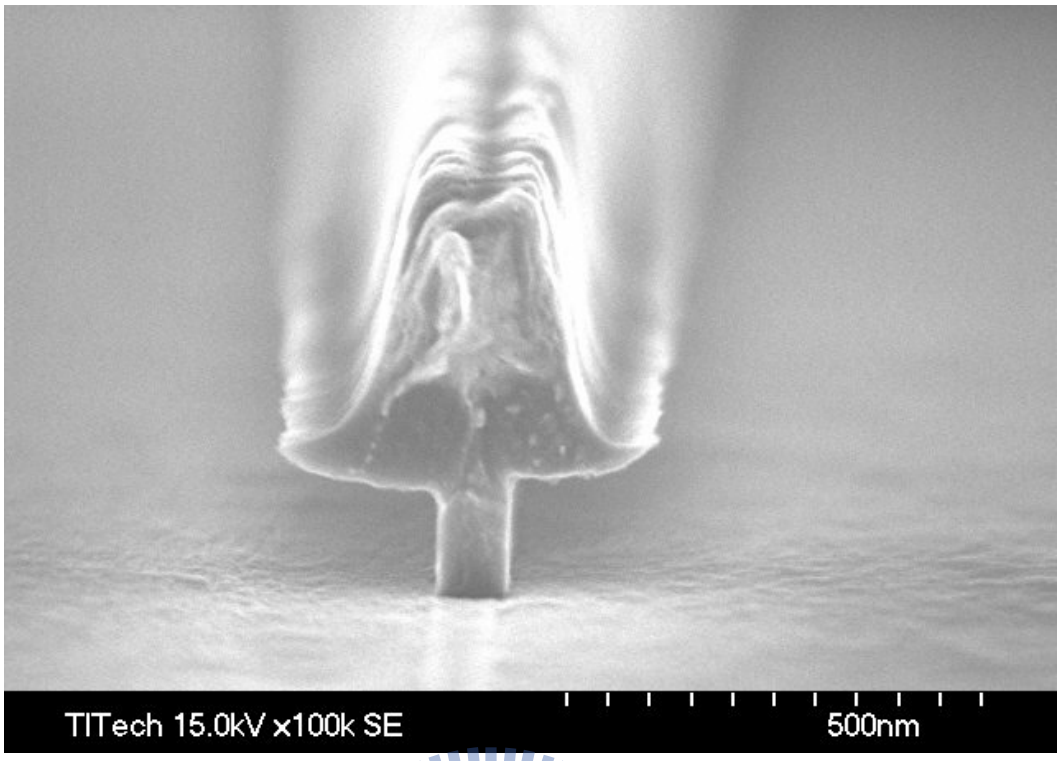


Figure 1.5 Cross sectional SEM image of the 50-nm Ti/Au (10nm/30nm) T-shaped gate on InP substrate.

Chapter 2

Fabrication of $In_xGa_{1-x}As$ High Electron Mobility Transistors

2.1 Material Properties and Growth of HEMT

Two types of wafer structure have been used in the dissertation. The first one is $In_{0.52}Ga_{0.48}As$ power MHEMs shown in fig. 2.1(a) for power applications. The epitaxial structure of the MHEMT was grown by molecular beam epitaxy (MBE) on 3-inch semi-insulating GaAs substrate. The structure from bottom to top consists of an InAlAs buffer layer, a Si δ-doping layer, an $In_{0.52}Al_{0.48}As$ spacer, an $In_{0.6}Ga_{0.4}As$ channel layer, an $In_{0.52}Al_{0.48}As$ spacer, a Si δ-doping layer, an $In_{0.52}Al_{0.48}As$ barrier layer, and a Si-doped $In_{0.53}Ga_{0.47}As$ cap. The double δ-doping structure and the $In_{0.6}Ga_{0.4}As$ channel layer of the MHEMT were designed to provide higher carrier concentration and superior electron transport properties.

The second type is InAs-channel HEMT shown in fig. 2.1(b) for high speed, low power consumption, and digital applications. The HEMT structure was grown on 2” semi-insulating InP substrate by molecular beam epitaxy (MBE). The structure from bottom to top consisted of a 600-nm-thick $In_{0.52}Al_{0.48}As$ buffer layer, a 3-nm-thick $In_{0.53}Ga_{0.47}As$ lower sub-channel, a 5-nm-thick InAs channel layer, 3-nm-thick $In_{0.53}Ga_{0.47}As$ upper sub-channel, a 3-nm-thick $In_{0.52}Al_{0.48}As$ spacer layer, a Si δ-doped (sheet density of $4\times10^{12}cm^{-2}$) layer, a 5-nm-thick $In_{0.52}Al_{0.48}As$ barrier, a 5-nm-thick InP etching stop layer, a 40-nm-thick Si-doped $In_{0.53}Ga_{0.47}As$ cap ($2\times10^{19}cm^{-3}$).

2.2 Device Fabrication

The fabrication process of the MHEMTs in this study includes:

1. Mesa/device isolation
2. Ohmic contact formation
3. Gate formation
4. Device passivation
5. Airbridge formation

The detail will be described in the following sections.

2.2.1 Mesa isolation

Device isolation is the very first step of the whole HEMT fabrication process which was used to define the active region of the device on the wafer. In these defined areas by lithography technique, the current flow is restricted to the desired path and each active device is isolated from each other (Fig. 2.2). There are three typical ways to achieve device isolation: wet etching, ion bombardment, and selective implantation. Wet etching is the simplest way of the three. In this study, mesa isolation was carried out by a phosphoric based solution etching. The active areas were masked by Shipley S1818 photo resist. According to the device structure, the mesa was etched to the buffer layer to provide good device isolation. In order to avoid the photo resist peeling during the etching, the wafer surface was pre-treated before resist coating by Hexamethyldisilazane (HMDS). Finally, the etching depth was measured by α-step or surface profiler after the photo-resist was stripped. The etched profile was checked by Scanning electron microscopy (SEM). To inspect the mesa isolation process, a test pattern with a 10μm gap is used to measure the leakage current.

2.2.2 Ohmic contact Formation

After wafer cleaning by using ACE and IPA, the negative photo resist and I-line aligner were used to define the Ohmic pattern and to form the undercut profile for the metal lift-off (Fig. 2.3). Ohmic metals multilayer Au/Ge/Ni/Au, from the bottom to the top, was deposited in the appropriate composition by e-gun evaporation system. After lift-off process, source and drain Ohmic contacts were formed by 320℃ annealing for 20 sec in nitrogen atmosphere (Fig. 2.4). Germanium atoms diffused into the InGaAs and heavily doped InGaAs during the thermal annealing process. The specific contact resistance was checked by the transmission line method (TLM) in the process control pattern monitor (PCM). The typical measured contact resistance was $< 1 \times 10^{-6}$ Ω-cm^2 (Fig. 2.9). The TLM patterns and the illustration of utilizing TLM to measure the Ohmic contact resistance were shown in Fig. 2.10 (a) and (b).

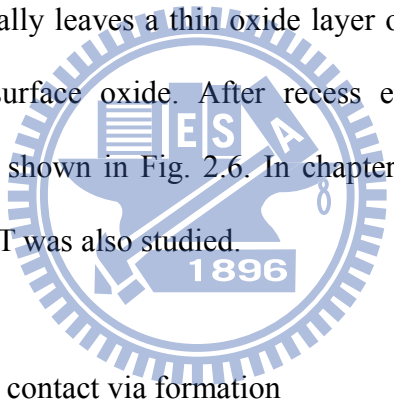
2.2.3 T-shaped gate and Recess process

For high frequency and high speed application, short gate length with low gate resistance is desired. T-shaped gate structure was the most common approach for obtaining low gate resistance. According to the T-gate structure design, the gate length is defined by the small footprint and the wide top offers low gate resistance.

T-shaped gates were achieved by using a multilayer resist technique with E-beam lithography. After patterning the T-shaped gate, the exposed HEMT active layers were recessed to achieve the desired channel current and pinch-off voltage characteristics. That means a groove is formed in the exposed surface of the wafer to “recess” the gate. This process is done by wet etch technique in this study, although dry etching methods may also be used. The recess etching was performed using PH-adjusted solution of succinic (S.A.) and

H_2O_2 mixture for selective etching of the heavily doped InGaAs cap layer over InAlAs Schottky layer. The concentration of the etchant should be adjusted to provide an etch rate that is sufficiently slow to allow good control over the recess process, thus enable the operation to approach the target current value, without over etching it. The etching selectivity of InGaAs cap layer over InAlAs Schottky layer was beyond 100.

The target current after the gate recess is a critical parameter affecting the HEMT performance. In order to get the desired recess depth, the recess process was controlled by monitoring the ungated I_{ds}. The method used to control the recess depth is to monitor the source-to-drain current during the etching process. For low noise PHEMT, the saturation current and the slope of the linear region go down as the recess groove was etched deeper and deeper. The wet etchant usually leaves a thin oxide layer on the InAlAs. HCl-based solution was used to remove the surface oxide. After recess etching, Ti/Pt/Au gate metal was evaporated and lifted off as shown in Fig. 2.6. In chapter 8, the Ti/Pt/Cu Schottky gate on InAlAs layer for the MHEMT was also studied.



2.2.4 Device passivation and contact via formation

FETs are very susceptible to the surface condition, especially in the gate region. As the device scales down, the gate length and spaces of source-to-drain and gate-to-drain become smaller. In situation like this, the devices are very sensitive to the damages and contaminations such as chemicals, gases, and particles. The passivation layer protects the device from damage during process handling (such as “airbridge”) and wafer probing (Fig. 2.7). The dielectric layer SiN_x is a common choice for device passivation.

In this study, Samco PECVD system was used for depositing the silicon nitride film. The processing gases of the passivation PECVD were Silane, ammonia, and nitrogen. The process

condition is: process pressure: 100Pa, process temperature: 300°C and process time: 10 minutes to form the silicon nitride film 1000Å. The reflection index was inspected by Ellipsometer about 2.0. Then the contact openings of the devices were formed by photo lithography (Fig. 2.8). The RIE was used to open the contact via hole region of the source and drain pads for interconnection. The plasma gases source for SiN_x etching were mixture of CF_4 and O_2.

In order to reduce the total device area, finger-type layout was adopted. As a result, airbridge process was necessary to contact the fingers. The use of airbridge had several advantages including lowest dielectric constant of air, low parasitic capacitance, and the ability to carry substantial currents. The airbridge process flow will be discussed in detail in next section.

2.3 Airbridge formation

Airbridge is built by metal with air between the metal interconnect and the wafer surface beneath. Airbridges are used extensively in GaAs analog devices and MMICs for interconnections. They may be used to interconnect sources of FETs, to cross over a lower level of metallization, or to connect the top plate of a MIM capacitor to adjacent metallization. The airbridges have several advantages including low parasitic capacitance, and the ability to carry substantial currents if the plated airbridge is thick enough.

Analog GaAs devices operating at high current density benefit from airbridges with thick plated metal layer. Low parasitic capacitance (between the bridge and any metallization beneath) follows from the large spacing and low dielectric constant of the intervening medium. The capacitance is a function of the thickness, and the dielectric constant of the intervening material. Air (k=1.0) has a much lower dielectric constant than any other dielectric, and the

space under the airbridge tends to be greater than the thickness of typical dielectrics. These considerations mean that airbridge crossovers are less capacitive than the dielectric type by a factor (typically) of five to twenty.

The following process flow was used to fabricate the airbridge interconnects.

1. The first photolithography for plating vias
2. Thin metals deposition
3. The second photolithography for plating Areas.
4. Electroplating.
5. Second PR removal and thin metal etching.
6. First PR removal

The thickness of the first layer of resist determines the spacing between the bridge and the material beneath (usually a dielectric). The thickness of the photo resist was about 2.5 μm. (Fig. 2.11) After the wafer was immersed in Acetone (ACE) and isopropyl alcohol (IPA) for 5 minutes, and dried by compressed dried air (CDA) blowing, the first layer of photo resist lithography was performed. The thickness was about 2.5 μm. In order to remove the thin PR residues in the exposed region, an O_2 descum process was required after the photolithography. The wafer was plate-baked immediately after the ICP descum. This bake was used to evaporate the remaining solvent in the photo resist. On the other hand, the first photo resist must be sufficiently baked to prevent the "bubbling" after thin metal deposition and the later thermal bake of the second photolithography.

The thin metal structure of the Au airbridge was Ti/Au with Ti as the adhesion layers. The thicknesses of these two metal layers were 300 Å, and 1000 Å, respectively, from the bottom to the top. (Fig. 2.12) The second photolithography was performed on thin multilayer metals. The thickness of the second PR was about 2.5 μm. Same as the first lithography,

descum is necessary to remove the polymer residues after development. (Fig. 2.13) The wafer was cleaned before plating to prevent contamination. The current density of the Au electroplating was 1 A/dm^2 and the plating time was 10 minutes for 2.5 μm thick Au. (Fig. 2.14)

The samples after electroplating were immersed in ACE to remove the second photo resist of the airbridges. The Au of the Ti/Au thin metal was then etched by KI/I2 solution for about 60 seconds. The etching rate of this step is high, and the etching of Au stops at the underlying Ti as the color turned from red to grey. Ti thin metal was also etched by mixed HF: H_2O (1:100) solution. HF is the active ingredient in this etchant, so it also etches oxides. Raising the fraction of HF in the solution increases the etching rate. Titanium is readily oxidized, so it is likely to form an oxide layer from the water, which is readily etched by the HF in this solution, resulting in the formation of bubbles of oxygen.

The samples were dipped in ACE for 20 minutes to remove the first photo resist for plating vias. The PR residues were stripped by O_2 plasma using ICP etcher. And then the specimens were dipped in IPA for 2 min. They were finally immersed in D.I. water, and then followed by CDA drying (Fig. 2.15). Finally, Fig. 2.16(a) shows the plan view for 40μm x 4 MHEMTs and Fig. 2.16(b) shows the SEM photo side view of Au airbridge of the device.

FIGURES:

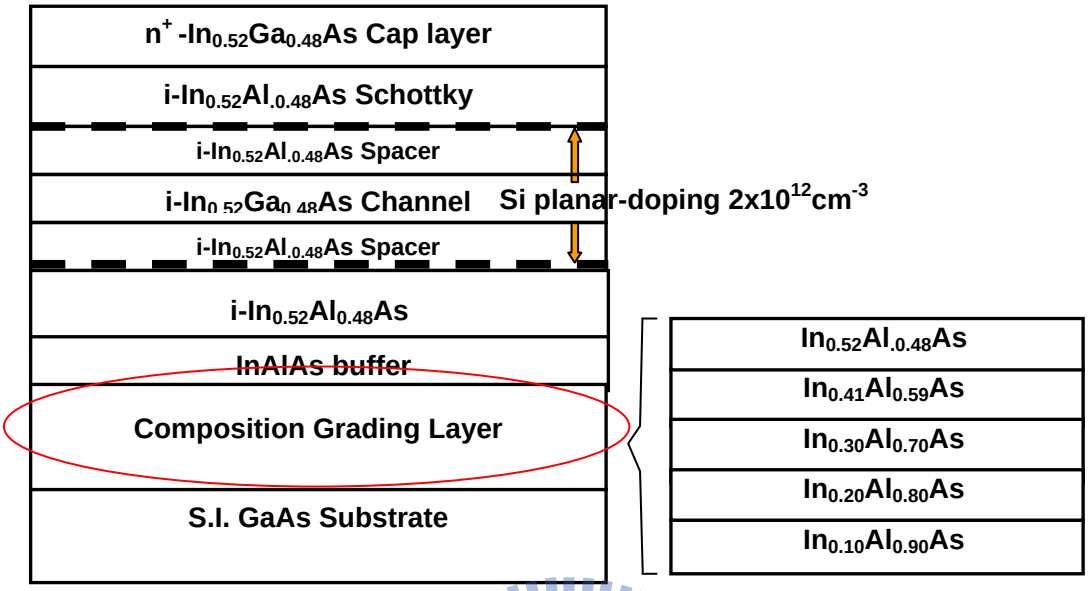


Figure 2.1(a) Double δ-doped MHENT structure for Power application

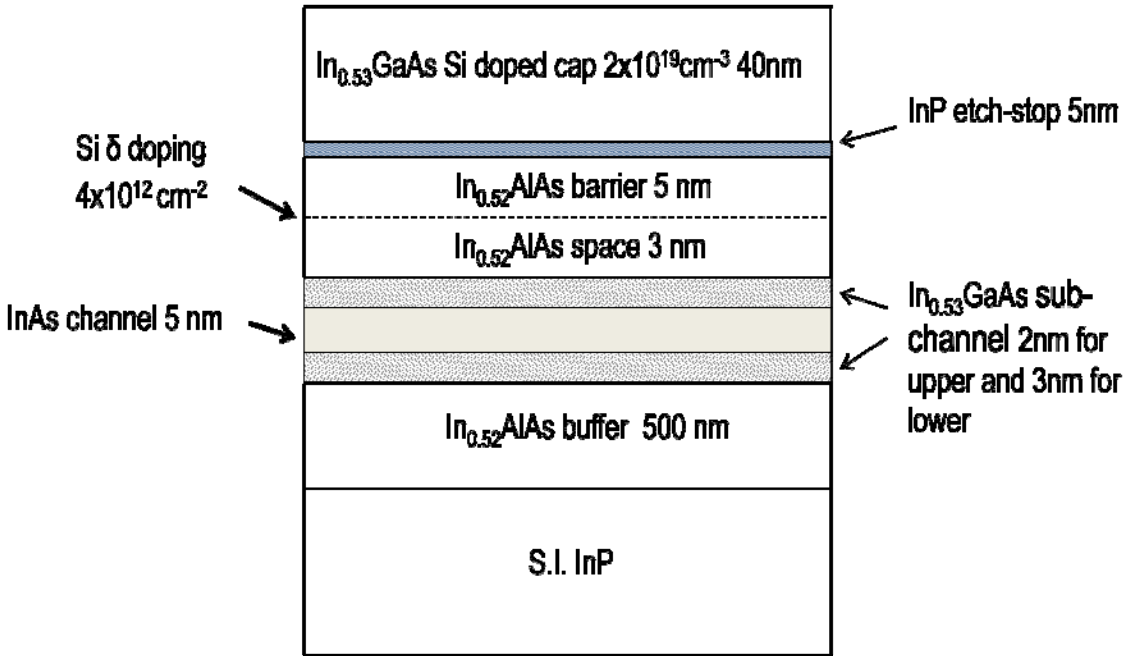


Figure 2.1(b) InAs-Channel HEMT for high-speed, low-power consumption applications.

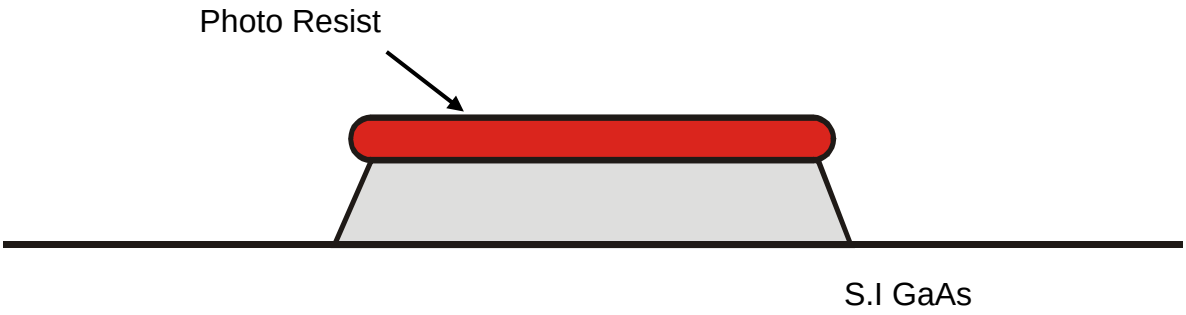


Figure 2.2 Mesa Etching

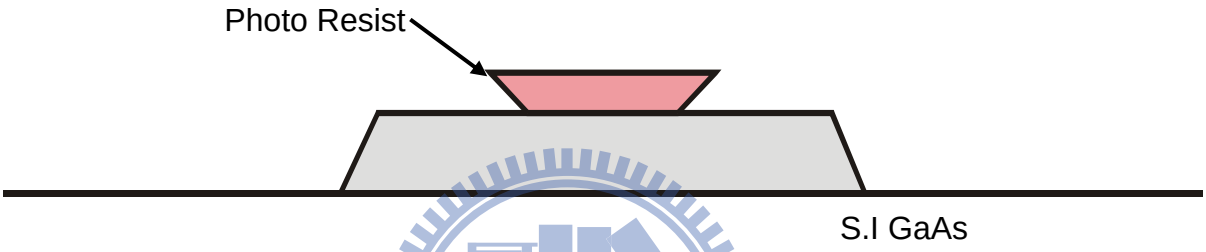


Figure 2.3 Ohmic photo

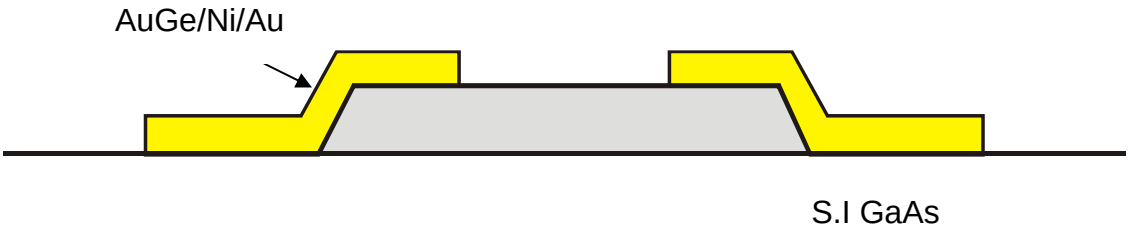


Figure 2.4 Ohmic metal

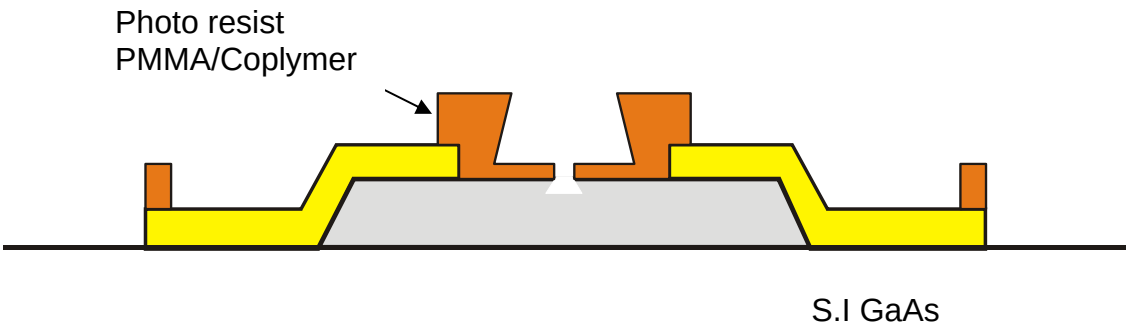


Figure 2.5 Ohmic window and ebeam T-gate followed by recess

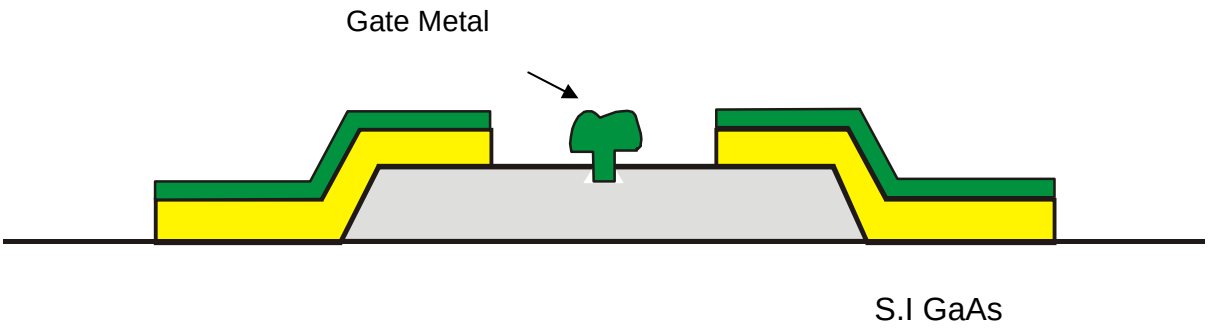


Figure 2.6 Gate metal deposition.

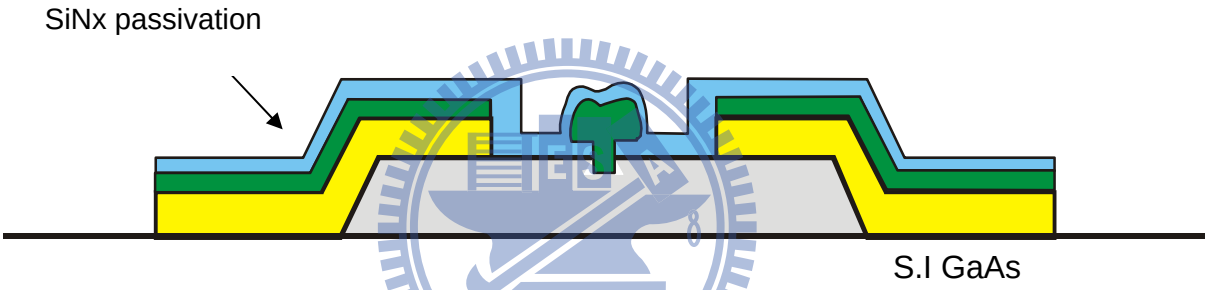


Figure 2.7 Passivation

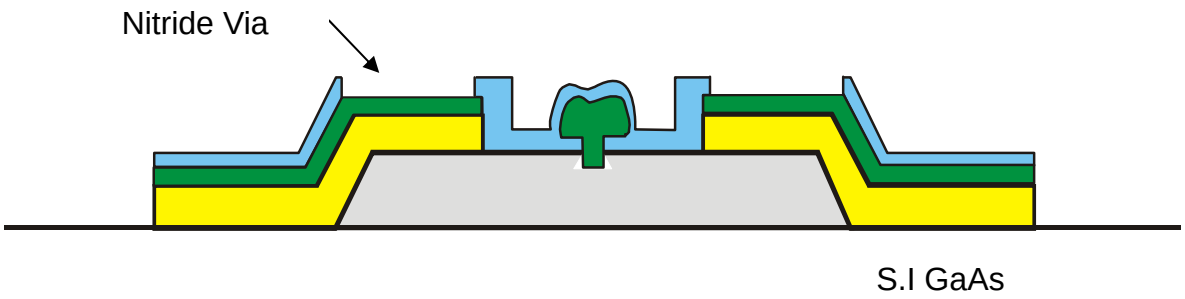


Figure 2.8 Nitride Via Etching

SPACE(μm)	3	5	10	20	36
Line 1 (Ω)	6.523	8.882	15.753	28.659	50.213
Line 2 (Ω)	6.872	9.001	15.972	29.123	51.345

Lien 1 (Ω/□)	9.8081E+01
Line 2 (Ω/□)	1.0010E+02
Line 1, rc(Ω-cm^2)	**8.77E-07**
Line 2, rc(Ω-cm^2)	**9.06E-07**

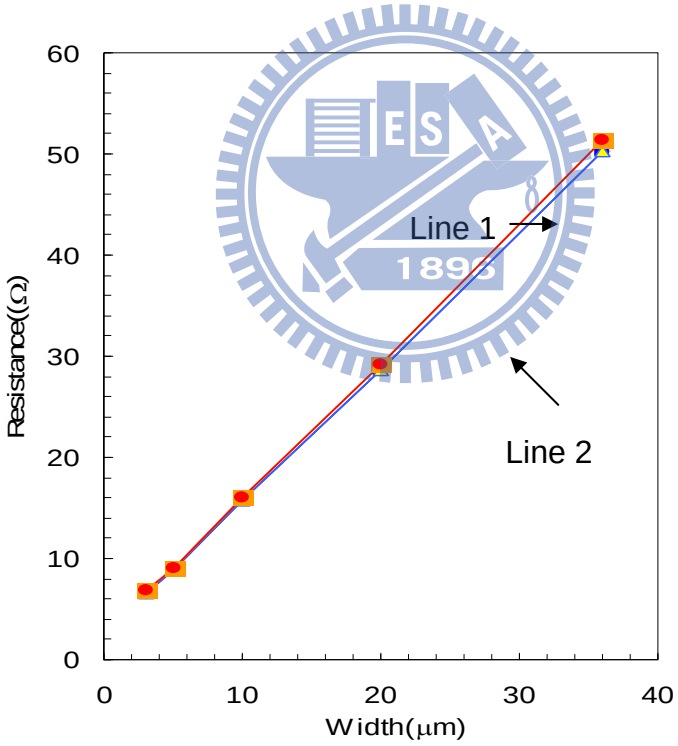


Figure 2.9 TLM measurement results of the AuGe/Ni/Au Ohmic contact for MHEMT.

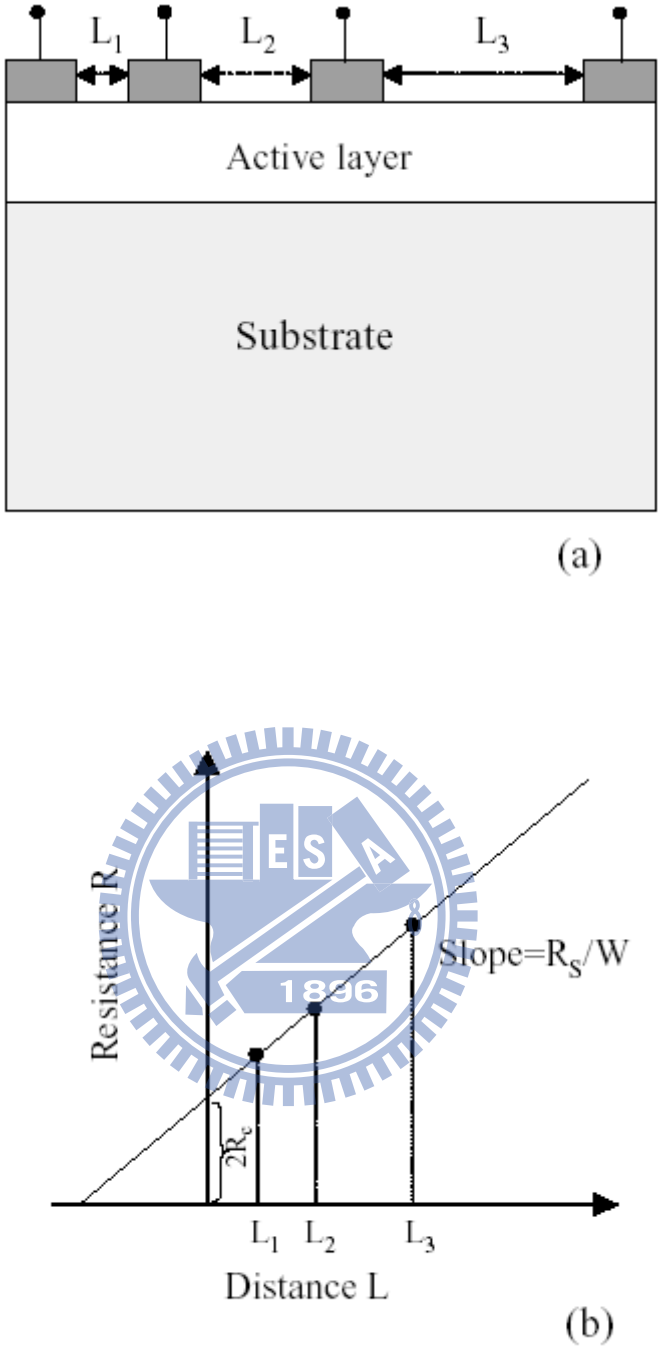


Figure 2.10 (a) The TLM patterns, (b) The illustration of utilizing TLM to measure the Ohmic contact resistanc.

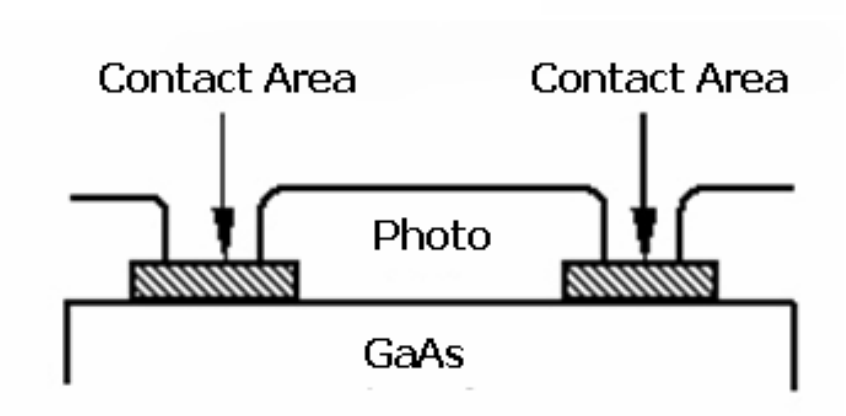


Figure 2.11 The First Photolithography for Plating Via.

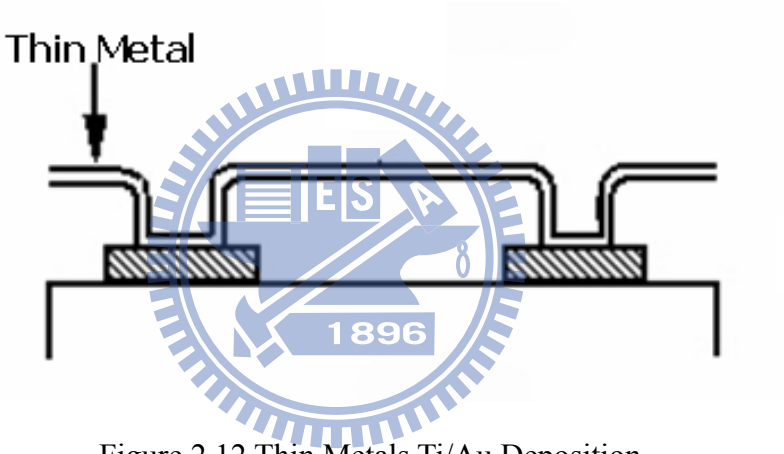


Figure 2.12 Thin Metals Ti/Au Deposition.

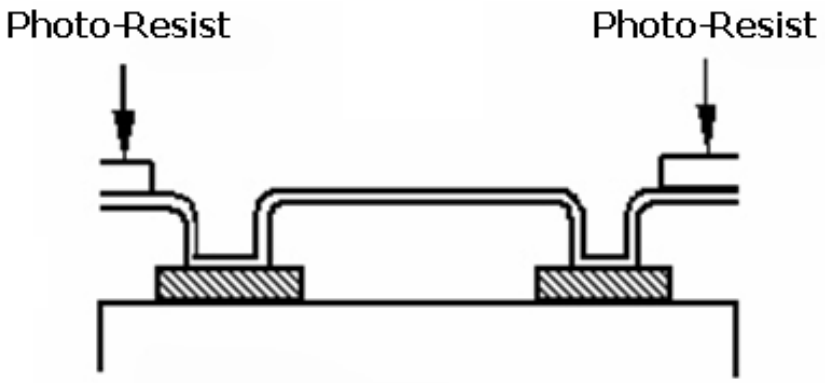


Figure 2.13 The Second Photolithography for Plating Areas.

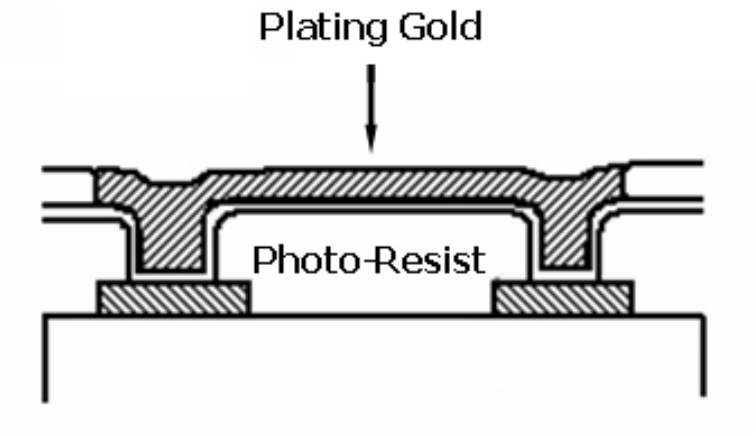


Figure 2.14 Au electroplating.

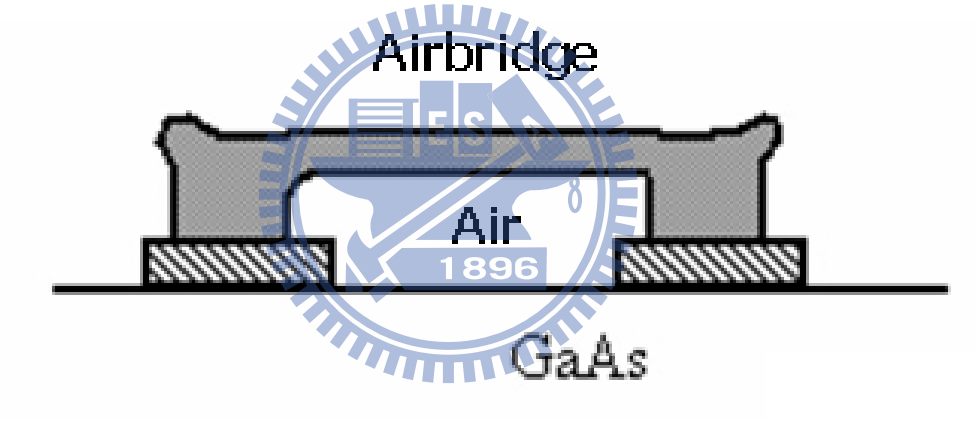
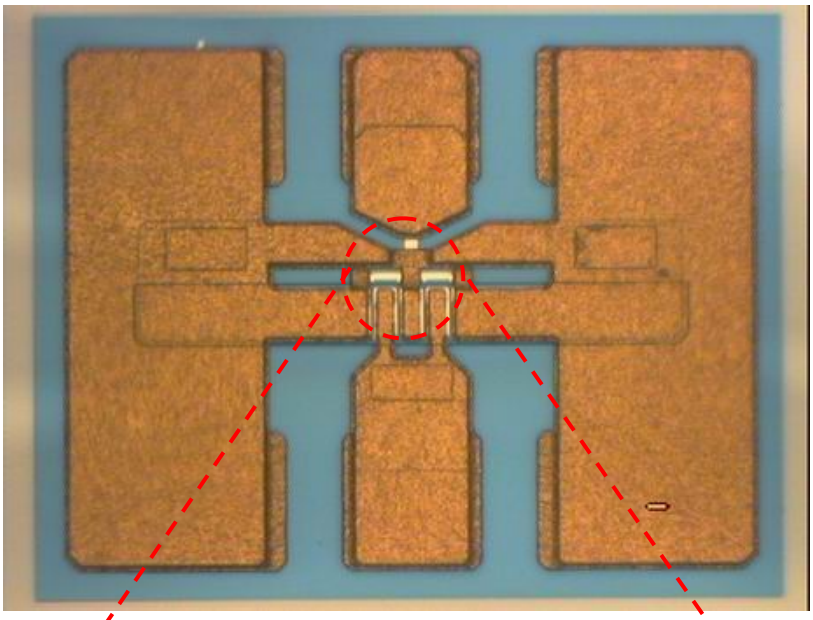
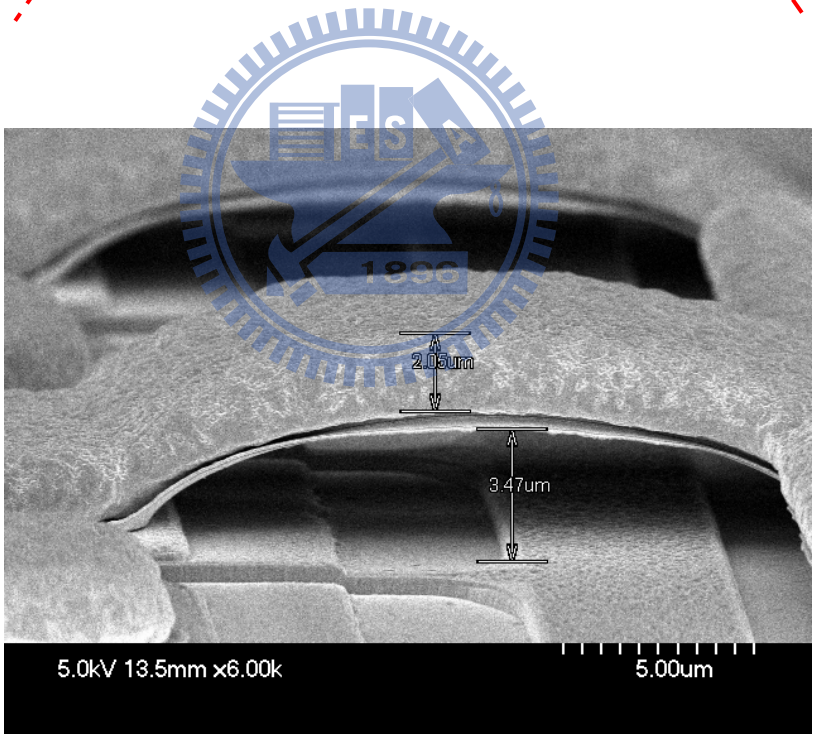


Figure 2.15 After thin metal etching and PR Removal



(a) Plan view for 40μm x 4 MHEMT



(b) SEM photo of Au airbridge side view

Figure 2.16 Photos of the Au airbridges of the device

Chapter 3

DC and RF Measurements of $In_xGa_{1-x}As$ High Electron Mobility Transistors

3.1 Device Characterization

After the device fabrication process, DC and RF performance of the InGaAs HEMTs must be measured using on-wafer measurement. For the DC measurement, the I-V characteristics were obtained easily by using an HP4142B Modular DC Source/Monitor and SUSS PA200 Semi-Auto Probe Station. The Transmission Line Model (TLM) method for determining specific contact resistance was adopted by using 4-wires measurement and Keithley 2400 SourceMeter. The *S*-parameters for the HEMT devices were measured by HP8510XF Vector Network Analyzer using on-wafer GSG probes from Cascade MicroTech. However, finding the RF behavior of a device on a wafer was a complicated process. For conventional RF measurement of a packaged device, the wafer needs to be diced and then an individual die should be mounted into a text fixture. Discriminating between the die's and the fixture's responses became an issue. Furthermore, fixturing die was a time-consuming process, making it impractical for high-volume screening. Thus the need for on-wafer RF characterization was arisen [3-1, 3-2].

3.2 DC characteristics

3.2.1 I-V characteristics [3-3]

The band diagrams at three different positions along the channel are illustrated in Fig. 3.1. There is a potential drop of channel charge density in the direction parallel to the channel, causing q'_{CH} to be a function of the position x. In order to relate the HEMT equations to the well-developed MOSFET equations, a per area gate oxide capacitance was define as C'_{OX}. [3-3] Therefore, the channel charge sheet density is expressed as:

$$q'_{CH} = -C'_{OX}[V_{GS} - V_T - V_{CS}(\chi)] \qquad (3\text{-}1)$$

We denote the channel-to-source potential resulting from the applied Gate-Source voltage V_{GS} and Drain-Source voltage V_{DS}. V_T is threshold voltage and the x means the position along the channel. The additional potential $V_{CS}(x)$ is called the channel-source potential. When $V_{DS} \neq 0$, the channel channel-source varies with x. In this figure, the channel-source potential measures the potential difference between any point x along the channel with respect to the potential of the source. The channel current equation which we are familiar with $I = qA\mu_n\varepsilon$ (A=area) is proportional to the cross-section area of the current conduction, the charge density, the mobility μ_n, and the electric field. Therefore, we obtain the form of the drift equation in HEMT:

$$I_{CH}(\chi) = -WC_{OX}\mu_n[V_{GS} - V_T - V_{CS}(\chi)]\frac{dV_{CS}(\chi)}{d\chi} \qquad (3\text{-}2)$$

We note that q'_{CH} is a negative quantity in HEMT, since electrons accumulated in the channel are negative charges. In fact, if we choose $x = L$ at the drain, this constant channel current is equal to the negative of the drain current. Hence, we have I_D=- I_{CH}, we find:

$$\int_0^L I_{DS}\,dx = -C'O\int_{V_{CS(O)}}^{V_{CS(L)}} C_{OX}\,\mu_n[V_{(GS)} - V_{(T)} - V_{(CS)}(\chi)]dV_{CS}(\chi) \qquad (3\text{-}3)$$

To carry out the integration in Eq. (3-3), we assume temporarily that we are working in the linear region such that current saturation due to channel pinch off at the drain does not occur. The *I-V* characteristics after pinch off will be dealt with shortly. In the linear operating region, the boundary conditions are $V_{CS}(L) = V_{DS}$ and $V_{CS}(0) = 0$. Hence, Eq. (3-3) leads to:

$$I_D = \frac{W_g C'_{OX}\,\mu_n}{L_g}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \qquad (3\text{-}4)$$

Eq. (3-5) is plotted schematically in Fig. 3.2, with I_D shown as a function of V_{DS}. The value of V_{DS} corresponding to the attainment of $I_{D,sat}$ is denoted as $V_{DS,sat}$, the saturation voltage. The saturation voltage can be obtained by taking the derivative of I_D will respect to V_{DS} and setting the result to zero. We find that:

$$V_{DS,SAT} = V_{GS} - V_T \qquad (3\text{-}5)$$

At this saturation voltage, q'_{CH} calculated from Eq. (3-1) is identically zero at the drain (pinch off). However, we realize that this conclusion originates from the fact that we are extending the validity of Eq. (3-1) all the way to where $q'_{CH}(L)$ is identically zero. Physically,

the channel at the drain does not pinch off completely. Instead, there is a finite thickness of accumulation of charges at which q'_{CH} $x=L$ is nonzero. The drift velocity is high, but nonetheless finite, so a constant current is maintained throughout the channel. Therefore, a complete model of the drain current is given by:

$$I_{DS} = \frac{W_g C'_{OX} \mu_n}{L g}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \qquad \text{for } V_{DS} < V_{DS,SAT}$$

$$= \frac{W_g C'_{OX} \mu_n}{L g}[\frac{(V_{GS} - V_T)^2}{2}] \qquad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (3\text{-}8)$$

For HEMTs, it is convenient to define the *saturation index (α)* as:

$$\alpha = 1 - \frac{V_{DS}}{V_{DS,SAT}} \qquad \text{for } V_{DS} < V_{DS,SAT}$$

$$= 0 \qquad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (3\text{-}9)$$

The drain current increases due to the perturbations in V_{GS} and V_{DS}. The mutual transconductance measures the amount of current increase due to the increment in the gate bias.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS} = const.} \qquad (3\text{-}10)$$

We also can write:

$$g_m = \frac{W_g C'_{OX} \mu_n}{L g}(V_{GS} - V_T) * (1 - \alpha) \qquad (3\text{-}11)$$

3.2.2 Transmission line model (TLM) [3-4]

The most widely used method for determining specific resistance is the method of Transmission Line Model (TLM) which is also mentioned in chapter 2. In this particular approach, a linear array of contacts is fabricated with various spacings between them as shown in Fig 3.3. The distances between TLM electrodes are 3μm, 5μm, 10μm, 20μm, and 36μm, respectively in this study. The resistance between the two adjacent electrodes can be plotted as a function of the space between electrodes. The plot is shown in the Fig. 3.4. Extrapolating the data to L= 0, one can calculate a value for the term R_c (Ω-mm).

$$R = 2R_C + \frac{R_S L}{W} \qquad (3\text{-}12)$$

where R is measured resistance, R_c is contact resistance, R_s is sheet resistance of the channel region, W is electrodes width, and L is space between electrodes. Another important parameter is the specific contact resistance ρ_c (Ω-cm^2), which is defined as

$$\rho_C = \frac{W^2 R^2}{R_S} \qquad (3\text{-}13)$$

This specific contact resistance is a practical figure of merit for contact resistance. It includes a portion of the metal immediately above the metal-semiconductor interface, a part of the semiconductor below the interface, current crowding effects, spreading resistance under

the contact, and any interfacial oxide that may present between the metal and the semiconductor.

3.2.3 Breakdown characteristics [3-5]

Breakdown mechanisms and models discussed in many articles. One of the models showing it is dominated by the thermionic filed emission (TFE) / tunneling current from the Schottky gate. This model predicts that the two-terminal breakdown voltage is lower at higher temperature because tunneling current increases with the temperature. Higher tunneling current occurs at higher temperature because carriers have higher energy to overcome the Schottky barrier. Other model suggests that impact-ionization determines the final two-terminal breakdown voltage, because the avalanche current decreases with increasing temperature. Lower avalanche current occurs at higher temperature because phonon vibrations as well as carrier-carrier scattering increase with increasing temperature. Either model is incomplete since coupling exists between TFE and impact ionization mechanisms. In addition, different devices may suffer from different breakdown mechanisms, depending on the details of the device design (insulator thickness, recess, channel composition, and so forth). In this study, the gate-to-drain breakdown voltage BV_{gd} is defined as the gate-to-drain voltage when the gate current is 1mA/mm.

3.3 RF Characteristics & Measurements

3.3.1 Scattering parameters [3-6]

Scattering parameters, generally referred to as *S*-parameters, are fundamental to microwave measurement. This section discusses *S*-parameters and the motivation for their use. For a device such as field-effect transistor with the input and output terminals can be treated as a two-port network as shown in Fig. 3.5. V_1 and I_1 are the voltage and current at the input, and V_2 and I_2 are the voltage and current at the output. Major characteristics, such as gain, return loss, and impedance matching can be calculated from known relationship among the input and output signals. The impedance parameters (*z*-parameters), conductance parameters (*y*-parameters) and hybrid parameters (*h*-parameters) are used to characteristic the devices because the parameter can be measured by open or short termination. The *z*-, *y*- and *h*-parameters can therefore be stated by the following equations:

z-parameters: $$\begin{bmatrix} V1 \\ V2 \end{bmatrix} = \begin{bmatrix} z11 & z12 \\ z21 & z22 \end{bmatrix} * \begin{bmatrix} i1 \\ i2 \end{bmatrix}$$

y-parameters: $$\begin{bmatrix} i1 \\ i2 \end{bmatrix} = \begin{bmatrix} y11 & y12 \\ y21 & y22 \end{bmatrix} * \begin{bmatrix} V1 \\ V2 \end{bmatrix}$$

h-parameters: $$\begin{bmatrix} V1 \\ i2 \end{bmatrix} = \begin{bmatrix} h11 & h12 \\ h21 & h22 \end{bmatrix} * \begin{bmatrix} i1 \\ V2 \end{bmatrix}$$

When the frequency is up to several GHz, the *z*-, *y*-, *h*- parameters can not be directly obtained by the open or short circuit because of the reflected wave from the open or short terminations. The open or short terminations will induce the network oscillation. Therefore the scattering parameters are used to characterize the performance of a device. Fig. 3.6 shows

the two-ports 1 and 2. The relation of the microwave signals and *s*-parameters can be described as

s-parameters: $\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} s11 & s12 \\ s21 & s22 \end{bmatrix} * \begin{bmatrix} a1 \\ a2 \end{bmatrix}$

a_1: the electric field of the microwave signal entering the component input

b_1: the electric field of the microwave signal leaving the component input

a_2: the electric field of the microwave signal entering the component output

b_2: the electric field of the microwave signal leaving the component output

By the definition, then,

$$s11 = \left.\frac{b1}{a1}\right|_{a2=0}, \quad s21 = \left.\frac{b2}{a1}\right|_{a2=0}, \quad s12 = \left.\frac{b1}{a2}\right|_{a1=0}, \quad s22 = \left.\frac{b2}{a2}\right|_{a1=0}$$

Therefore, s_{11} is the electric field leaving the input divided by the electric field entering the input, under the condition that no signal enters the output. The measurement includes instruments for the DC and RF measurement. Where a_1 and b_1 are electric fields, their ratio is a reflection coefficient. Similarly, s_{21} is the electric field leaving the output divided by the electric field entering the input, when no signal enters the output. Therefore, s_{21} is a transmission coefficient and is related to the insertion loss or the gain of the device. Similarly, s_{21} is a transmission coefficient related to the isolation of the device and specifies how much power leaks back through the device in the wrong direction. s_{22} is similar to s_{11}, but looks in the other direction into the device. The *s*-parameters have both the amplitude and phase.

3.3.2 Current gain cutoff frequency f_T

Traditionally, transistors are characterized using figures of merit such as the unity current-gain cutoff frequency (f_T). Consider a transistor characterized by the following small-signal *y*-parameters

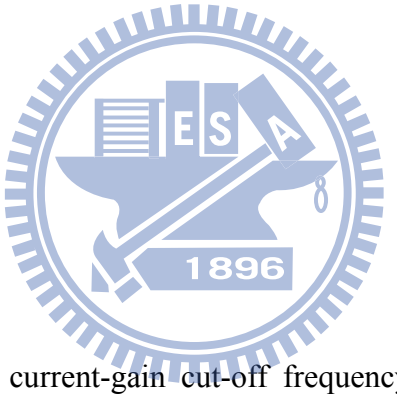
$$i_1 = y_{11}(\omega)V_1 + y_{21}(\omega)V_2$$

$$i_2 = y_{21}(\omega)V_1 + y_{22}(\omega)V_2$$

The currents and voltages are defined in Fig. 3.5. For example, we use the *y*-parameters of a FET in the common source configuration in Fig. 3.7.

$$i_g = y_{gg}(\omega)V_{gs} + y_{gd}(\omega)V_{ds}$$

$$i_d = y_{ds}(\omega)V_{gs} + y_{dd}(\omega)V_{ds}$$



The unity short-circuit current-gain cut-off frequency is defined as the frequency at which the short-circuit current gain is unity:

$$h_{21}(\omega) = \left| \frac{y_{21}(\omega_T)}{y_{11}(\omega_T)} \right| = 1$$

Since the HEMT is the common source configuration, the maximum short-circuit current gain can be approximated by

$$\left|\frac{y_{21}(\omega_T)}{y_{11}(\omega_T)}\right| = \left|\frac{y_{ds}(\omega_T)}{y_{gg}(\omega_T)}\right| \approx \frac{g_m}{\omega C_g W_g L_g}$$

Where g_m is the transconductance. Notice the 1/ω decrease with frequency (20 dB per decade) using $20\log(y_{21}/y_{11})$ of the short-circuit gain. The intrinsic *S* parameters are used to determine the unity current-gain cut-off frequency (f_T). It can be determined by extrapolation of the short-circuit current gain $h_{21} = 0$ dB. h_{21} can be defined as

$$h_{21} = \frac{2 s_{21}}{(1 - s_{11})(1 + s_{22}) + s_{12} s_{21}}$$

Fig. 3.8 shows the definition of the cut-off frequency (f_T).

3.3.3 Maximum frequency of oscillation f_{max}

The microwave performance of a transistor is usually characterized by the maximum stable power gain as a function of frequency. The maximum power gain is obtained by simultaneously matching the input and output to obtain a conjugate match. Conjugate match means that the source impedance Z_S and the load impedance Z_L satisfy simultaneously:

$Z_S = Z^*_{IN}$, $Z_L = Z^*_{OUT}$

Where Z_{IN} is the input impedance of the two-port network measured at port 1 with the load impedance Z_L connected at port 2 and where Z_{OUT} is the output impedance of the two-port network measured at port 2 with the source impedance Z_S connected at port 1. The maximum

power stable gain (G_{max}) consisting of the maximum available gain (MAG), and the maximum stable gain (MSG) were derived from the *S*-parameter data by the equation:

$$GMAX = \left|\frac{S21}{S12}\right| K - \sqrt{(K^2 - 1)},$$

where *K* is the Rollett stability factor

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2|S_{12}\,S_{21}|}$$

$$D = S_{11}\,S_{22} - S_{12}\,S_{21}$$

The MAG is the highest power gain of the two-port network with the impedance-matched input and output. The MAG of a transistor can only be obtained when the transistor is unconditionally stable, *i.e.* $K>1$. The MSG is the highest power gain of a two-port network with the resistive loaded in both input and output ports. The MSG can be obtained if the transistor where potentially unstable according to:

$$MSG = MAG|_{K=1} = \left|\frac{S21}{S12}\right|$$

The device maximum power gain cut-off frequency can then be defined as the frequency at $G_{max} = 0$ dB.

The comparison of the high-frequency performance of two-port devices is usually done using the unilateral power gain *U* derived by Mason [3.7]:

$$U = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{K\left|\frac{S_{21}}{S_{12}}\right| - Re\left(\frac{S_{21}}{S_{12}}\right)}$$

U is the maximum available power gain (MAG is introduced in the previous section) of a device once it has been unilateralized ($y_{12} = 0$) using lossless feedback techniques.

The maximum frequency of oscillation f_{max} is then defined as the frequency at which U is unity. f_{max} is often referred to as the frequency at which a three-port device switches form active to passive. U can then be written

$$U(\omega) = \left(\frac{\omega_{max}}{\omega}\right)^2$$

The unilateral power gain will then decrease at a rate of 20 dB per decade (using 10logU) like the short-circuit current gain.

3.3.4 Noise figure [3-8]

Noise is related to the device channel and capacitive coupling between the channel and the gate. The gate noise is represented by a gate-current noise generator i_{ng}^2 and is caused by charge fluctuation in the channel, which in turn induces the fluctuation of compensating charge on the gate electrode. The gate-noise is proportional to f^2 in HEMTs. The channel noise is represented by a drain-current noise generator i_{nd}^2 and is caused by various physical mechanisms driven by the electric field in the channel. In the linear region of the device

channel, the channel noise is caused by thermal noise (Johnson noise). A thermal noise voltage caused in the channel leads to a modulation of the channel resistance and causes a drain voltage fluctuation at the channel end (drain). The corresponding drain noise current is inversely proportional to $g_m I_{DS}$. In the high-field region, hot electron scattering, intervalley scattering, and high diffusion noise contribute to the channel noise.

Another noise source is gate leakage. A new model that takes this effect into account by an additional parallel resistor to the gate capacitance and the resistor R_i has been proven to a good correlation between predicted and measured minimum noise figures even at low frequencies. The negative influence of the gate leakage on the noise figure vanishes at higher frequencies. Noise figure reflects the noise added to the signal by the imperfect amplifier, and is defined as the signal-to-noise ratio (S/N) of the input signal divided by the signal-to-noise ratio of the output signal,

$$F = (S_i/N_i)/(S_0/F_0)$$

It is usually expressed in dB:

$$NF = 10\log F$$

We shall use F to designate absolute noise figure and NF to designate figure expressed in dB. The noise performance of a FET may be quantified by the noise figure, NF, which is a function of frequency, FET bias voltages, and impedance matching. Another noise figure of FETs structure is shown as the following equation.

$$NF = 1 + \sqrt{2}\frac{f}{f_t}\sqrt{g_m(R_S + Rg)}, f_t = \frac{g_m}{2\pi C_{gs}}$$

In general, high source-drain current contributes to noise by electron scattering, and this noise is reduced as the current is reduced. However, reducing the current too close to pinch-off reduces the transconductance, which causes increased noise figure because of decrease gain. There will exist an optimum gate bias that presents the best compromise.

3.3.5 RF measurement calibration [3-6]

Before the on-wafer measurement, the measuring system must be calibrated first to eliminate the extrinsic parasitic components of the cables, adaptors, probes and so on. The GSG (ground-signal-ground) probe tips are used in this study. The planar calibration was first carried out to make the tips are at the same height to prevent the nonuniform contacts. After the planar calibration of the probe tips, the calibrations for the measurement were made. The S-parameter of devices was measured using Cascade Microtech™ on-wafer probing system with vector network analyzer from 1 to 110 GHz. A standard Load-Reflection-Reflection-Match (LRRM) calibration method was used to calibrate the measurement system.

FIGURES:

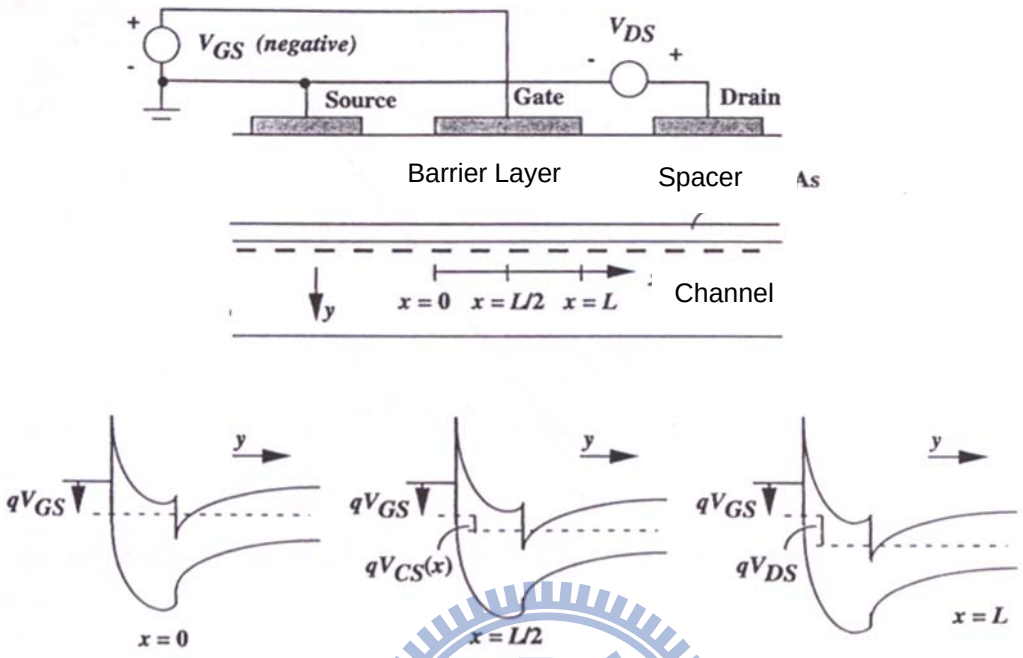


Figure 3.1 Band diagrams at three different locations along the channel of a HEMT

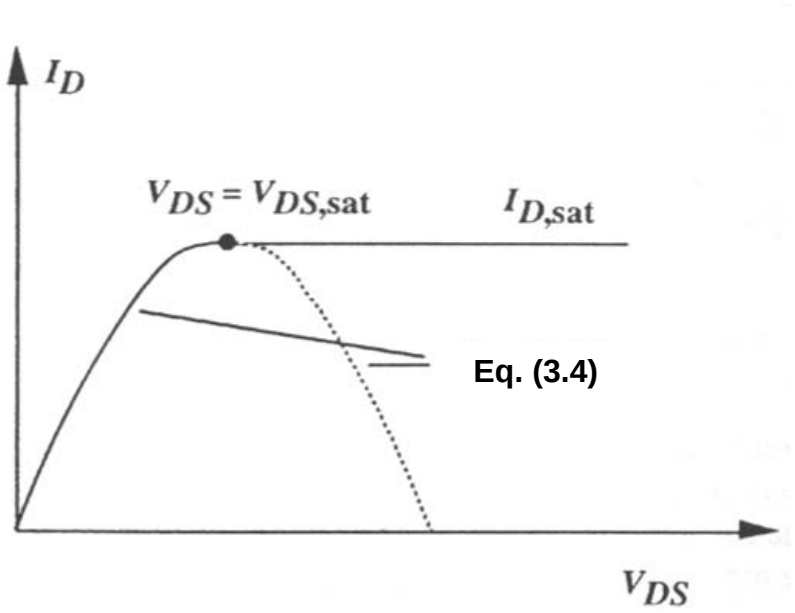


Figure 3.2 Actual characteristics and those predicted by Eq. (3-3)

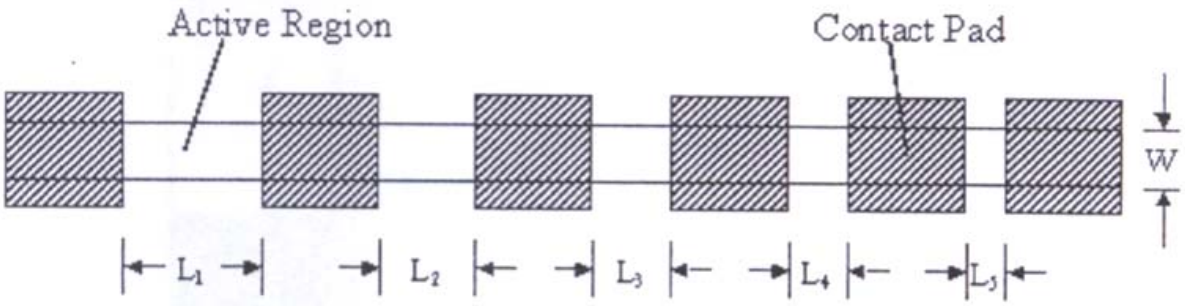


Figure 3.3 TLM pattern

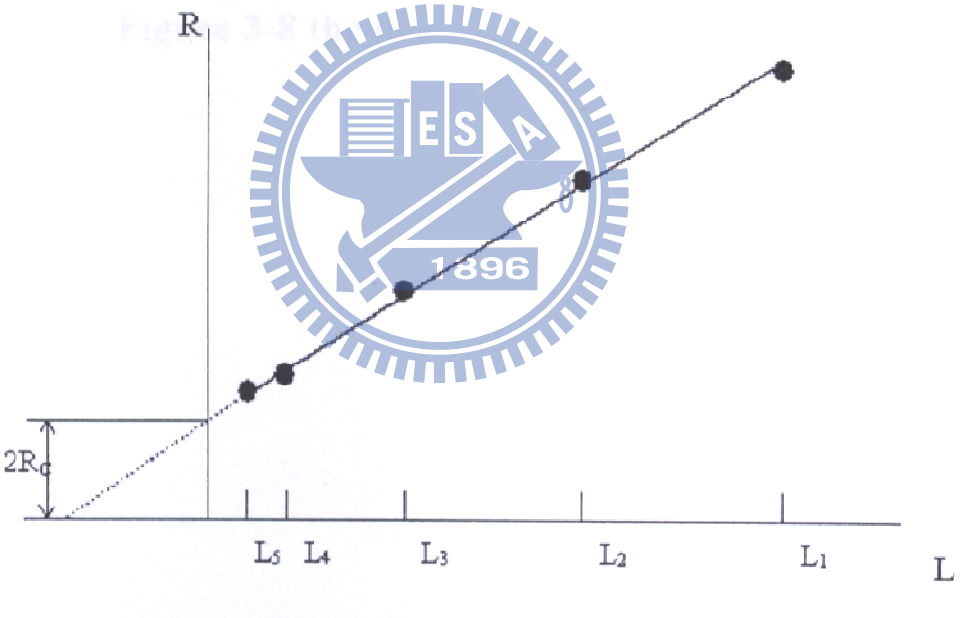


Figure 3.4 The illustration of utilizing TLM to measure ohmic contact resistance

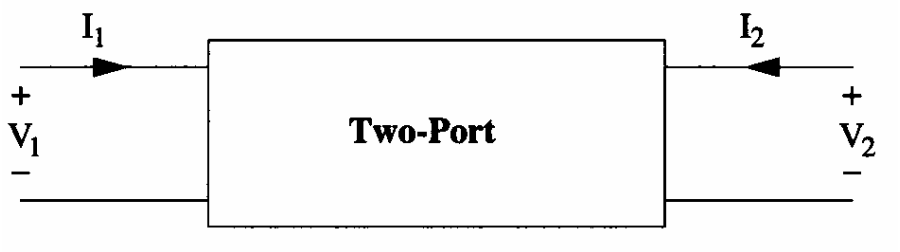


Figure 3.5 The equivalent two-port network schematic at low frequency

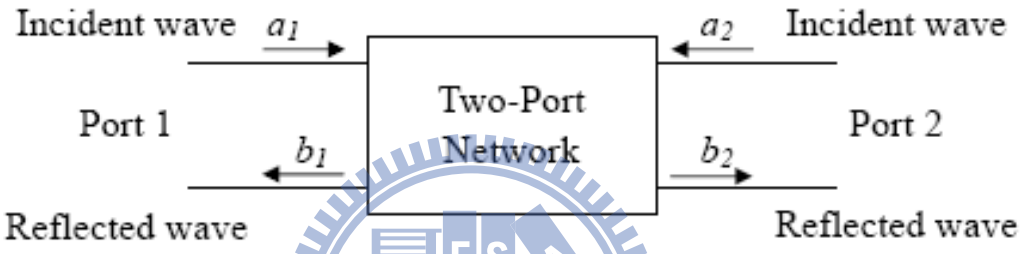


Figure 3.6 The equivalent two-port network schematic at high frequency

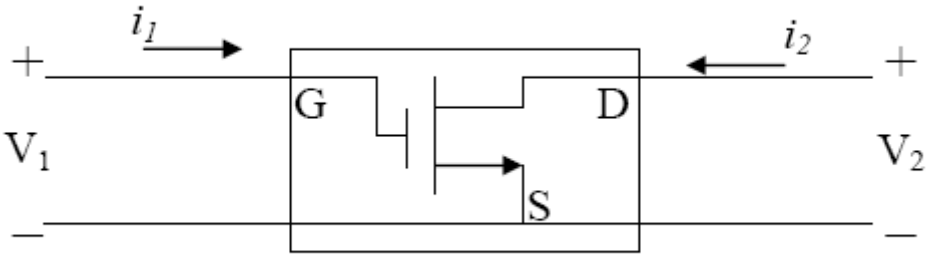


Figure 3.7 Small signal representation of a common source FET

fT is the cutoff frequency where H21 = 1 (0dB). This is usually extrapolated from H21 measurements by fitting a -20dB/decade slope, see below.

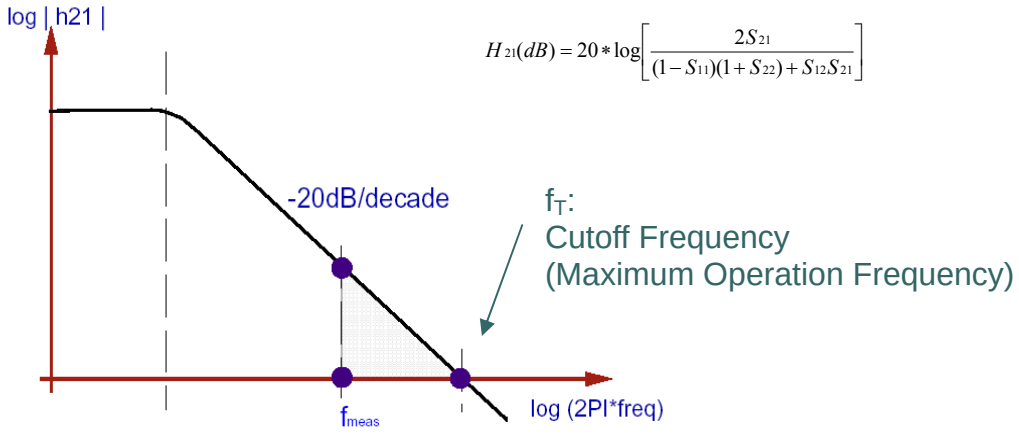


Figure 3.8 Definition of Cutoff Frequency f_T

Chapter 4

High-Performance $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ Power Metamorphic High Electron Mobility Transistor for Ka-Band Applications

4.1 Introduction

For high frequency communication system applications, such as communication satellites, radars, and mobile millimeter-wave communication devices, high-performance power amplifiers are required in the transmission part. Owing to its superior low noise and power performance characteristics in the millimeter-wave range, an InAlAs/InGaAs metamorphic high electron mobility transistor (MHEMT) is a good alternative to a pseudomorphic HEMT (PHEMT) on GaAs or lattice-matched HEMT on InP [4-1]. Although, the PHEMT grown on a GaAs substrate demonstrated a high output power density at 60 and 94 GHz in a previous work [4-2], the power gain and the power added efficiency (PAE) were limited by the low indium content of the pseudomorphic InGaAs channel. In contrast, InP-based HEMTs have shown excellent high frequency characteristics when the gate length (L_g) was reduced to sub-100 nm range [4-3], [4-4]. However, the advantages of InP-based HEMTs, such as a high electron saturation velocity, a high conduction band discontinuity and a low access resistance, can also be achieved with an MHEMT that can be grown on a GaAs substrate that is less expensive and larger than InP substrate [4-5]-[4-7]. In this work, a 70 nm $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ power MHEMT with a double δ-doping structure was fabricated and evaluated at the Ka-band. The device demonstrates excellent DC and RF performances at Ka-band, indicating its great potential for millimeter-wave power applications.

4.2 Experiments

The epitaxial structure of the MHEMT was grown by molecular beam epitaxy (MBE) on a 3-in semi-insulating GaAs substrate. The structure from bottom to top consists of an InAlAs buffer layer, a Si δ-doping layer, an $In_{0.52}Al_{0.48}As$ spacer, an $In_{0.6}Ga_{0.4}As$ channel layer, an $In_{0.52}Al_{0.48}As$ spacer, a Si δ-doping layer, an $In_{0.52}Al_{0.48}As$ barrier layer, and a Si-doped $In_{0.53}Ga_{0.47}As$ cap. The double δ-doping structure and the $In_{0.6}Ga_{0.4}As$ channel layer of the MHEMT were designed to provide a high carrier concentration and superior electron transport properties.

The active region of the device was defined by wet chemical etching. Source and drain Ohmic metals were formed with Au/Ge/Ni/Au. The T-shaped gate was fabricated by 50 KeV JEOL electron beam lithography (E-beam) using a conventional tri-layer E-beam resist with two-step exposure. The tri-layer resist system of ZEP-520/PMGI/ZEP520 was used for E-Beam lithography. The Ti/Pt/Au was evaporated as gate metal. The T-shaped gate length was set to be 70 nm. After T-shaped gate formation, a 100-nm-thick silicon nitride layer was deposited as a passivation layer. Finally, airbridges were formed with 2 μm plated Au.

4.3 Device Performance

Figure 4.1 shows the current-voltage characteristics of the 0.07 × 80 μm^2 MHEMT. The fabricated $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ MHEMT shows a maximum drain-source current of 890 mA/mm and a transconductance of 827 mS/mm. Its high current density is due to the double δ-doping structure providing a higher carrier concentration and superior electron transport properties in the $In_{0.6}Ga_{0.4}As$ channel. The two terminal gate-to-drain I-V characteristics of the studied $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ MHEMT are shown in Fig. 4.2. The two terminal

gate-to-drain breakdown voltage (BV_{GD}) is – 9V, defined at I_{GD}= –1 mA/mm. The studied MHEMT is suitable for power applications owing to its high breakdown voltage. S-parameter measurement was performed from 1 to 40 GHz using a vector network analyzer with an on-wafer configuration. Figure 4.3 shows the frequency dependence of the current gain (H21) and power gain (MAG/MSG) for the 0.07 × 80 μm^2 MHEMT with the gate and drain biases of – 0.6 and 1.5 V. The f_T and f_{max} of the MHEMT are 200 and 300 GHz, respectively, by extrapolating H21 and MAG/MSG by least-squares fitting with a –20 dB/decade slop. H21 is 13 dB at 40 GHz and MAG/MSG is 15 dB at 40 GHz. Figure 4.4 shows the noise figure (NF) of the MHEMT from 1 to 16GHz. The minimum NF is below 0.67 dB up to 16 GHz. This superior behavior is attributed to the low access resistance, large drain current and high transconductance across a wide gate bias range. Furthermore, the power performance of the device of 0.07 × 160 μm^2 gate width was measured at 32 GHz using load-pull systems for Ka-band applications. The result obtained at a drain bias of 2.5 V is shown in Fig. 4.5. With the tuner impedance matched for a maximum power, the device shows a maximum output power density of 176 mW/mm and a P1dB of 80 mW/mm with a 9.5 dB power gain at 32 GHz. This high power gain is attributed to the high indium content of the channel and the short gate length. These results are comparable to those of other InP-based power HEMT with an output power density of 185 mW/mm and a power gain of 13.5 dB at 20GHz when biased at a drain-source voltage of 2 V [4-8]. Overall, the MHEMT exhibits RF performances comparable to those of InP-based HEMTs owing to the appropriate epi-structure design and short gate length.

4.4 Conclusion

The $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ power MHEMT with a double δ-doping structure and 70

nm T-gate was designed and fabricated. This device showed excellent DC and RF performance, indicating its great potential for power applications at the Ka-band and in the millimeter-wave range.

4.5 Figures

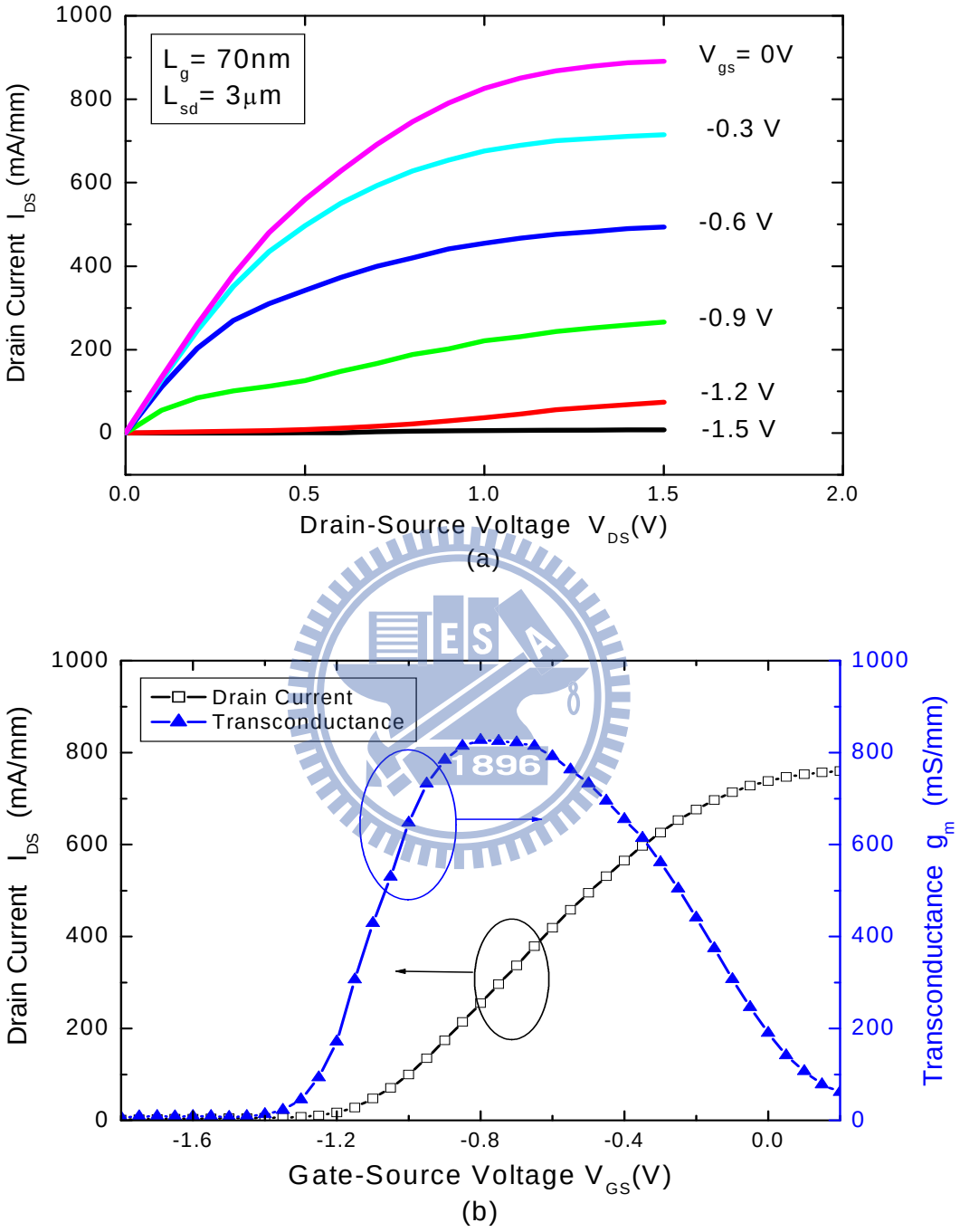


Figure 4.1 Current-voltage characteristics of 0.07 × 80 μm^2 MHEMT.

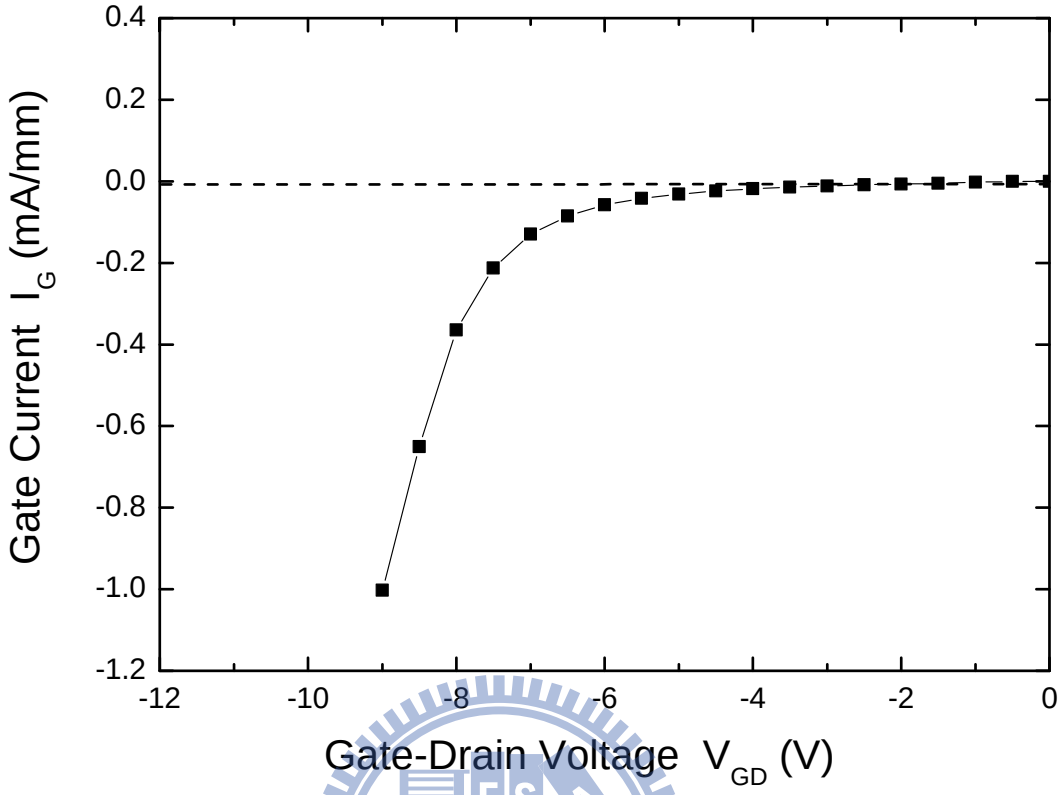


Figure 4.2 Two terminal gate-to-drain breakdown characteristics of 0.07 × 80 μm^2 MHEMT.

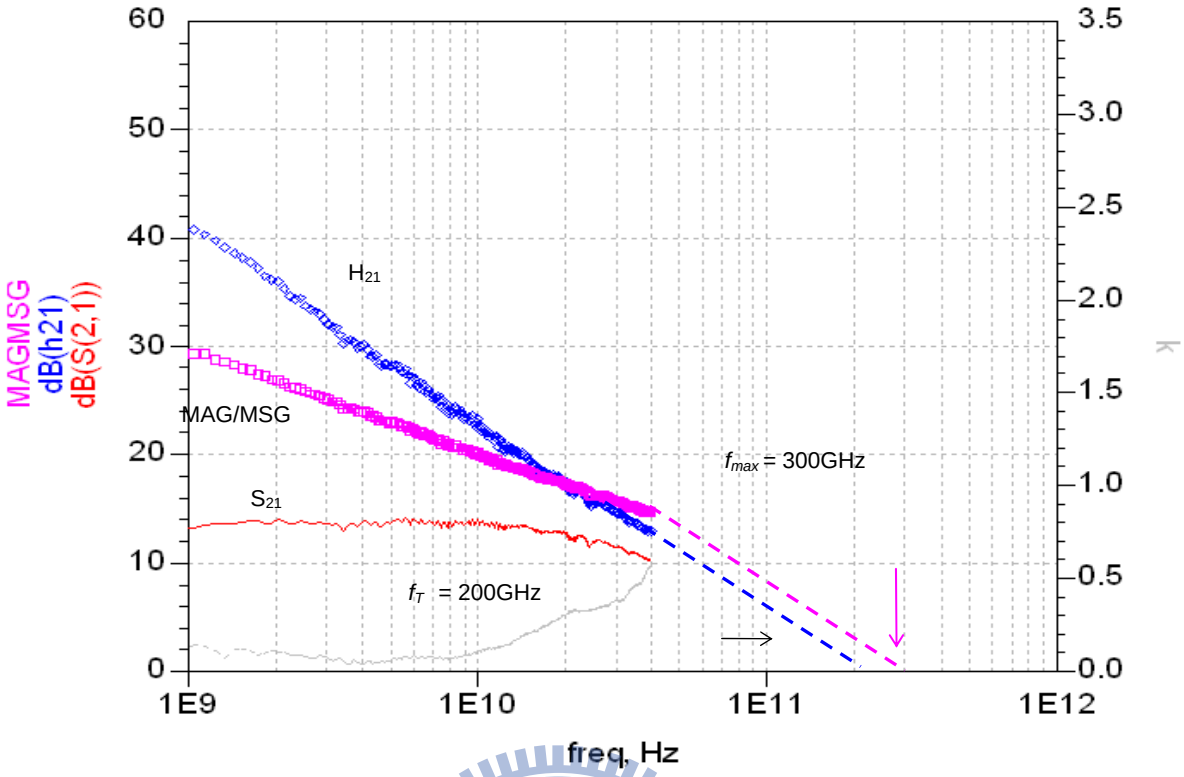


Figure 4.3 Frequency dependence of current gain (H21) and MAG/MSG of power MHEMT.

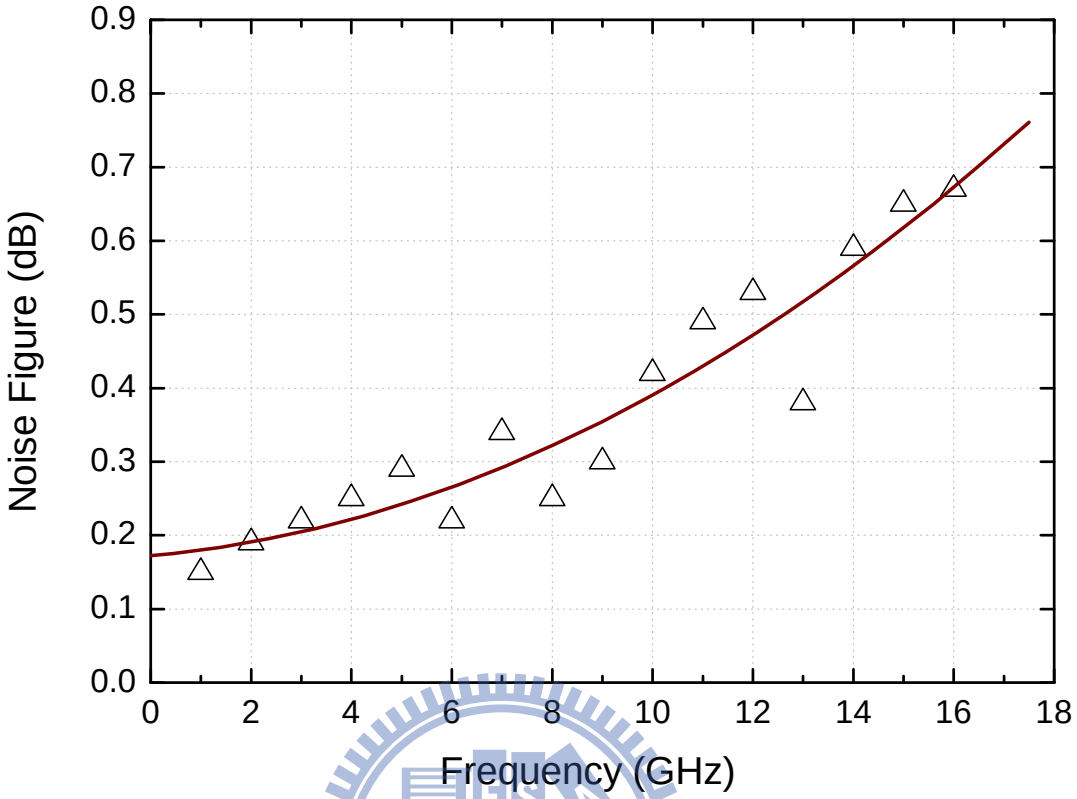


Figure 4.4 Noise figure (NF) of 0.07 × 80 μm^2 MHEMT measured from 1 to 16 GHz.

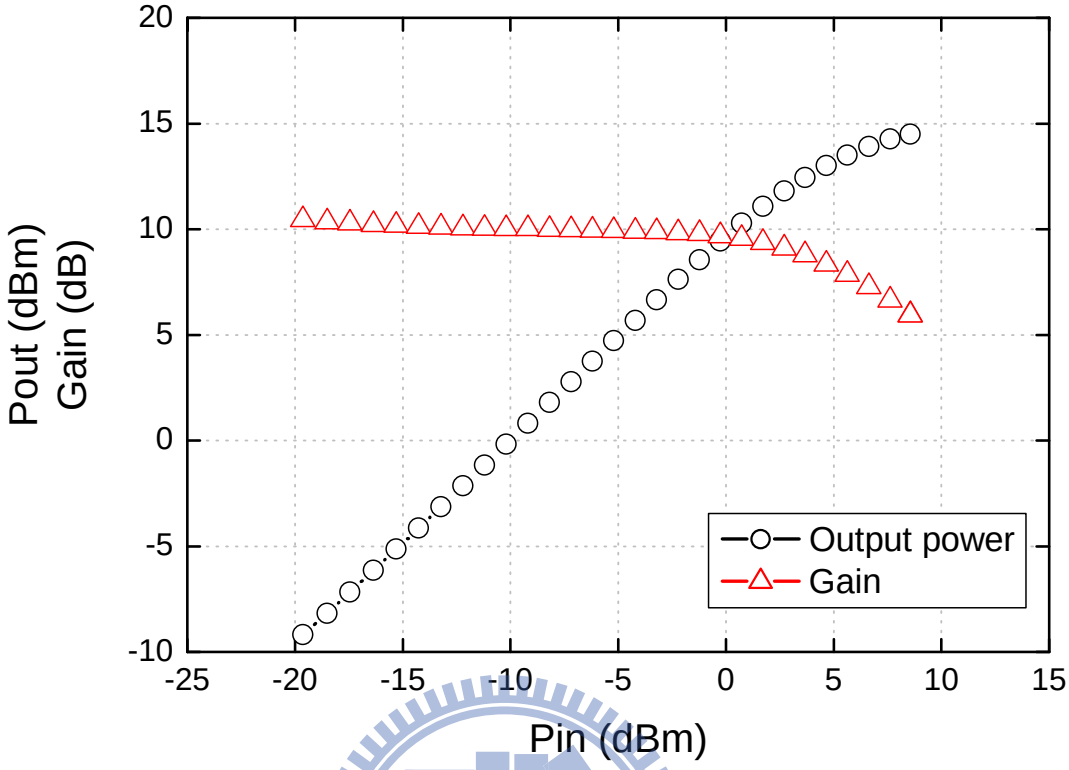


Figure 4.5 Measured 32 GHz power performance of 0.07 × 160 μm^2 power MHEMT at drain bias of 2.5 V.

Chapter 5

Investigation of Impact Ionization in InAs-Channel HEMT for High Speed and Low Power Applications

5.1 Introduction

With the ultimate limit for the scaling of Si devices for device performance improvement being approached, planar III-V compound semiconductor field effect transistors (FETs) have been identified as one of the most attractive devices for nanoelectronic applications. The excellent RF-performance has been demonstrated by InAlAs/InGaAs high electron mobility transistors (HEMTs) on InP substrate [5-1]. Generally, higher electron mobility and velocity can be realized by the increase of the Indium content in the InGaAs channel, which makes InAs-channel heterostructure FETs (HFETs) well suitable for low-power and high-speed logic applications due to the extremely high electron mobility of more than 30000 $cm^2/V \bullet s$ [5-2], [5-3].

However, high Indium content devices usually suffer from serious kink-effect, low breakdown voltage and high output transconductance caused by the electron-hole pair generation created by impact ionization. This phenomenon is even more remarkable for InAs/AlSb structures because of the lack of hole confinement due to type II alignment [5-2]. In general the output conductance limits the achievable gain and the breakdown voltage and has direct impact on the power performance of such devices [5-4], [5-5].

In this study, the impact ionization behavior in the RF and digital performances of the InAs HEMT with $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel structure were

investigated. Owing to the $In_{0.53}Ga_{0.47}As$ sub-channels with a higher energy bandgap, the InAs/$In_{0.53}Ga_{0.47}As$ heterostructure obtains a lower gate leakage current and a higher breakdown voltage. The effect of impact ionization on the device performance will also be discussed, with the optimum bias conditions determined through complete DC and RF characterizations.

5.2 Device Fabrication

The HEMT structure was grown on 2" semi-insulating InP substrate by molecular beam epitaxy (MBE). The structure from bottom to top consisted of a 600-nm-thick $In_{0.52}Al_{0.48}As$ buffer layer, a 3-nm-thick $In_{0.53}Ga_{0.47}As$ lower sub-channel, a 5-nm-thick InAs channel layer, 3-nm-thick $In_{0.53}Ga_{0.47}As$ upper sub-channel, a 3-nm-thick $In_{0.52}Al_{0.48}As$ spacer layer, a Si δ-doped (sheet density of $4\times10^{12}cm^{-2}$) layer, a 5-nm-thick $In_{0.52}Al_{0.48}As$ barrier, a 5-nm-thick InP etching stop layer, a 40-nm-thick Si-doped $In_{0.53}Ga_{0.47}As$ cap ($2\times10^{19}cm^{-3}$). The InP etching stop layer was used to improve the selectivity of wet chemical recess etch and provide semiconductor surface passivation on each side of the gate to reduce the trapping effect on the InAlAs surface [5-6]. With the use of the InP etching stop layer, the lateral recess length was easy to control and RF performance was improved [5-7].

The mesa isolation was done by wet chemical etch. Source and drain Ohmic metal were formed with 240-nm-thick Au/Ge/Ni/Au and alloyed by rapid thermal annealing at 250 °C for 30 sec. As a result of the highly Si doped cap, a low Ohmic contact resistance (R_c) of 0.025 Ω • mm and an sheet resistance (R_{sh}) of 35.3 Ω/□ were obtained by using the transmission line model method. The T-shaped gate lithography was carried out in 50-KeV JEOL electron beam lithography system (E-beam). The gate-recess was performed by wet chemical etching using succinic acid-based solution. The Ti/Pt/Au gate metal was formed by evaporation and

lift off. The gate length of 80 nm was estimated by scanning electron microscopy (SEM). Devices were passivated using a 100-nm-thick PECVD (plasma enhanced chemical vapor deposition) silicon nitride film. Finally, the airbridges were formed with 2 μm of plated Au.

5.3 Results and Discussion

Fig. 5.1(a) shows the current-voltage (I – V) characteristics of the 80-nm gate HEMT device with a 2×50 μm gate width. As observed from the figure, this device can be well pinched off with a threshold voltage of -0.7 V and demonstrates a high breakdown voltage with a low gate leakage current. Additionally, a relatively high drain current density of 700 mA/mm was observed at a low V_{DS} of 0.5 V, primarily due to the superior electron transport properties in the InAs channel. It is noted from the I-V curve that the drain current tends to increase at a constant slope for V_{DS} > 0.7 V. This is mainly due to the existence of impact ionization as evidenced by the hump occurred in the vicinity of V_{DS} = 0.7 V that was observed in the output conductance measurement as shown in Fig. 5.1(b). Fig. 5.2(a) shows the DC transconductance (g_m) as a function of gate voltage (V_G) at different V_{DS} from 0.3 V to 1.1 V. The device exhibits high g_m values, with peak of 1600 mS/mm at V_{DS} = 0.5 V and 2630 mS/mm at V_{DS} = 1.1 V. The drastic increase in peak g_m values for V_{DS} > 0.7 V is mainly due to the additional electron-hole pairs generated by impact ionization in the channel. Electrons merely flow in the channel which adds to the channel current and increase the transconductance. However, if the resulting holes are unconfined by band lineup, the holes will leave the channel and flow into the negatively bias Schottky gate either to cause an increase in the gate leakage current or to accumulate below the gate (or channel) area, contributing to a higher gate-to-source capacitance. A record-high on-state breakdown voltage (BV_{DS}, defined at 1mA/mm gate current) of 1.75 V was measured at V_G = – 0.8V, indicating

good hole confinement achieved by such a channel structure [5-4], [5-5], [5-8].

To investigate the effect of impact ionization on the RF performance, the S-parameter of the 2x50μm device was measured using Cascade Microtech^{TM} on-wafer probing system with vector network analyzer from 1 to 110 GHz. A standard Load-Reflection-Reflection-Match (LRRM) calibration method was used to calibrate the measurement system. Fig. 5.2(b) shows the measured $|S_{21}|$ (dB) at various frequencies as functions of drain voltage. DC transconductance g_m as a function of drain voltage is also included in the figure. It is clear that despite the monotonic increasing trend of g_m with the drain voltage, $|S_{21}|$ tends to saturate at a constant level for drain biases higher than 0.7 V. The primary reason was that the impact ionization occurred at drain biases higher than 0.7 V and the generated electrons can not catch up with the field modulation at RF frequencies. The gate current plotted as a function of gate voltage as shown in Fig. 5.3(a), further manifests the impact ionization phenomenon occurred when V_{DS} was higher than 0.7V. It also shows better gate leakage performance as compared to the Sb-based InAs-HFETs [5-8], [5-9]. To further investigate such phenomenon, the pad parasitic effects were carefully de-embedded through the S-parameter measurements and the intrinsic device parameters were extracted and listed in Table 5.1. The extracted RF g_m values at different bias levels are also listed in the table. It can be observed that the drastic increase in C_{GS} at higher drain bias levels together with the decrease in RF g_m caused by impact ionization degrades the cutoff frequency f_t severely, resulting in the peaked f_t value of 310 GHz at V_{DS} = 0.7 V.

Complete DC and RF analysis for the investigation of the effect of impact ionization on the device reveal that the device should be biased at V_{DS} = 0.7 V for optimum performance. Current gain ($|h_{21}|^2$), Mason's unilateral gain (U_g) and MAG/MSG as a function of frequency are plotted in Fig. 5.3(b). The intrinsic f_T and f_{max} obtained for the 2x50μm device are 310 GHz and 330 GHz at V_{DS} = 0.7V exhibiting better performance than other InAs-channel

devices with InAlAs or Sb-based barrier [5-8], [5-10] and comparable to the performance of InGaAs-channel HEMTs with high In concentration [5-1], [5-11], [5-12]. To characterize such device for high-speed logic applications, the gate delay time (CV/I), according to the definition in [13], was calculated to be 0.63 psec at the optimum bias V_{DS} = 0.5 V. This excellent intrinsic device speed of the InAs/InGaAs HEMT shows great potential for logic applications compared to the state-of-the-art planar and non-planar Si logic transistors.

5.4 Conclusion

In this study, a high performance InAs/InGaAs HEMT was demonstrated. High on-state breakdown voltage BV_{DS} of 1.75 V and very low gate leakage current were obtained by using $In_{0.52}Al_{0.48}As$ barrier layer and $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ composite channel structure. The effect of impact ionization on the device performance has been investigated through complete DC and RF characterizations which determine the optimum drain bias voltage to be 0.7 V. High current gain cutoff frequency (f_t) of 310 GHz and maximum oscillation frequency (f_{max}) of 330 GHz with very low gate delay time of 0.63 psec were achieved at the optimum drain voltage of 0.7 V. With the high gain and high speed at low drain voltage, such devices show tremendous potential in future high speed and low power logic applications.

5.5 Figures

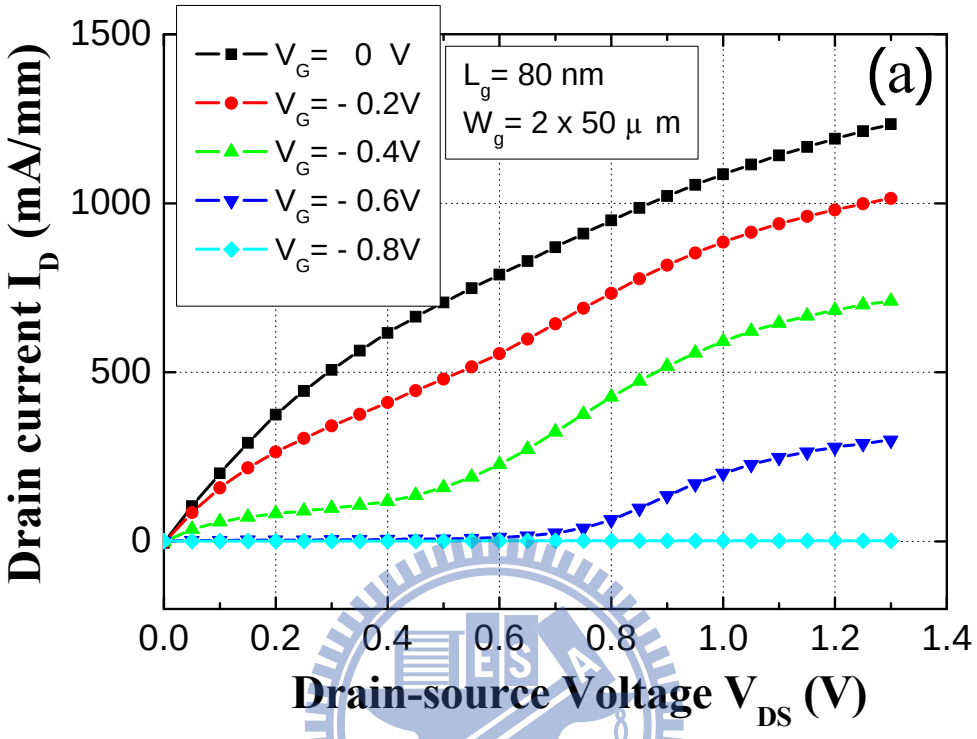


Figure 5.1(a) Output characteristics of a 0.08 μm × 100 μm InAs/InGaAs HEMT. Drain current I_D as a function of drain bias V_D with different gate voltage V_G from 0 V to -0.8 V.

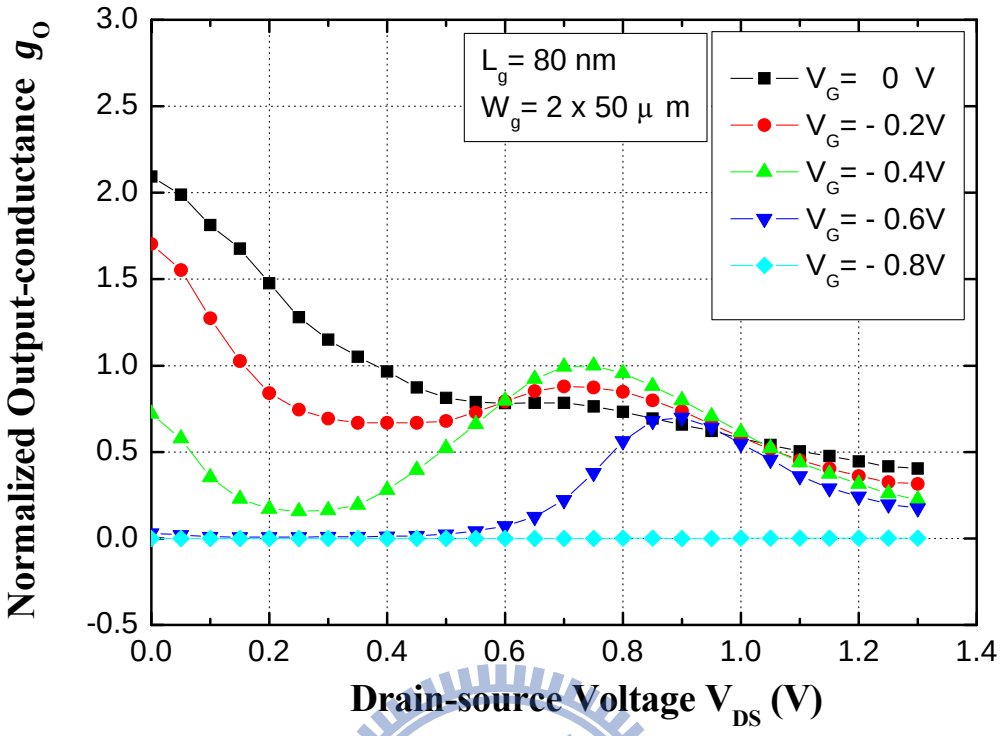


Figure 5.1 (b) Normalized output conductance g_o as a function of V_D of a 0.08 μm × 100 μm InAs/InGaAs HEMT.

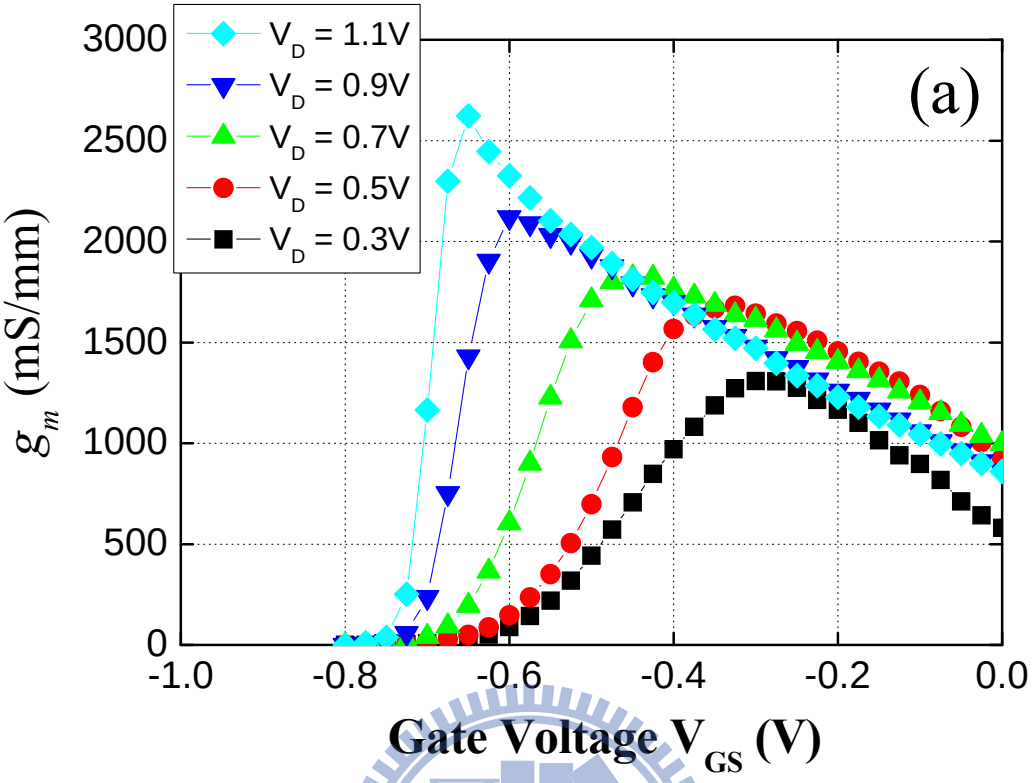


Figure 5.2 (a) DC transconductance g_m of a 0.08 μm × 100 μm device as a function of V_G with different drain voltage V_D.

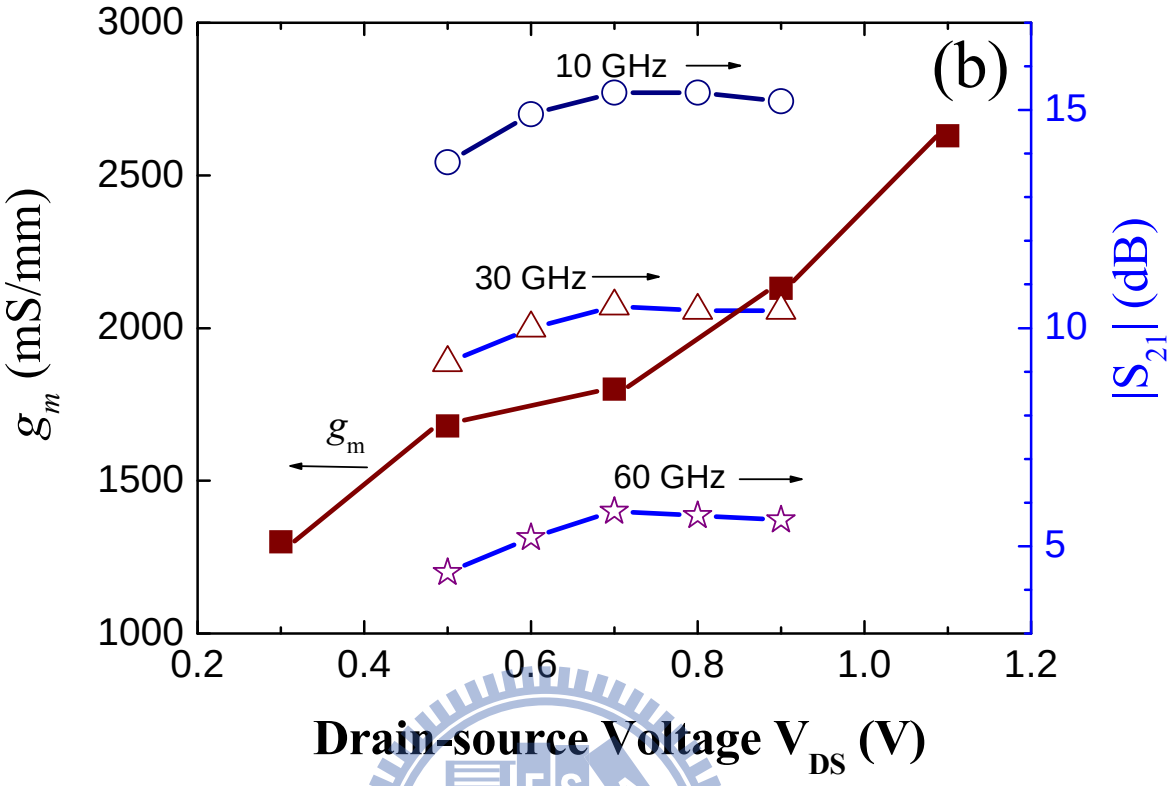


Figure 5.2(b) Plot of $|S_{21}|$ measured at 10, 30 and 60 GHz and g_m versus drain-source voltage of a 0.08 μm × 100 μm.

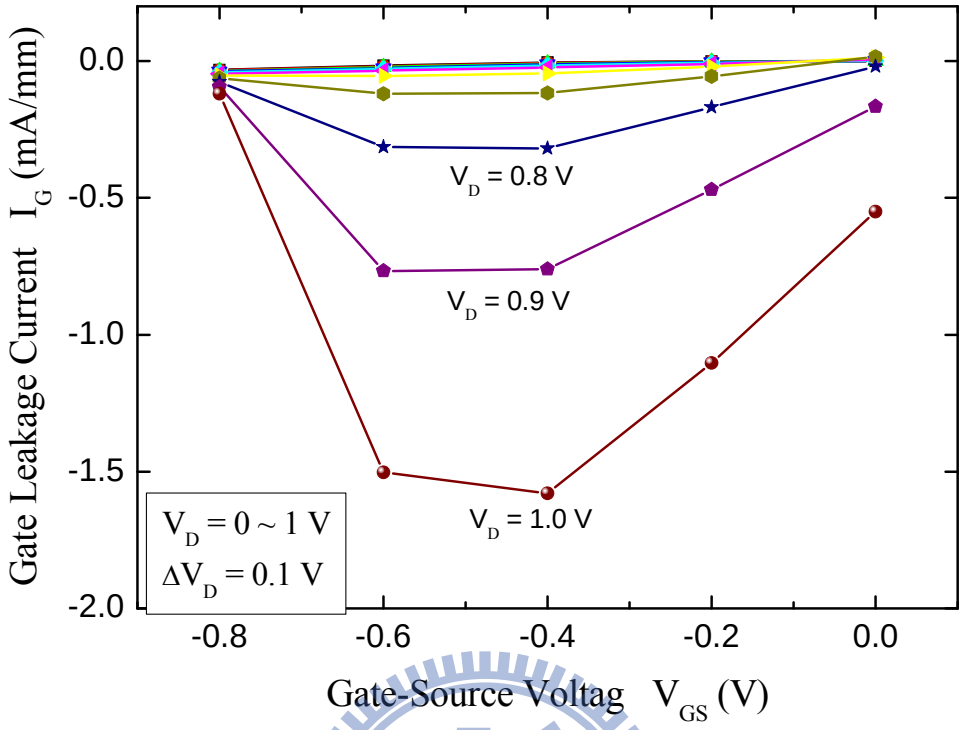


Figure 5.3(a) The gate current I_G plotted as a function of V_G at different V_D from 0 V to 1 V, 0.1 V per step.

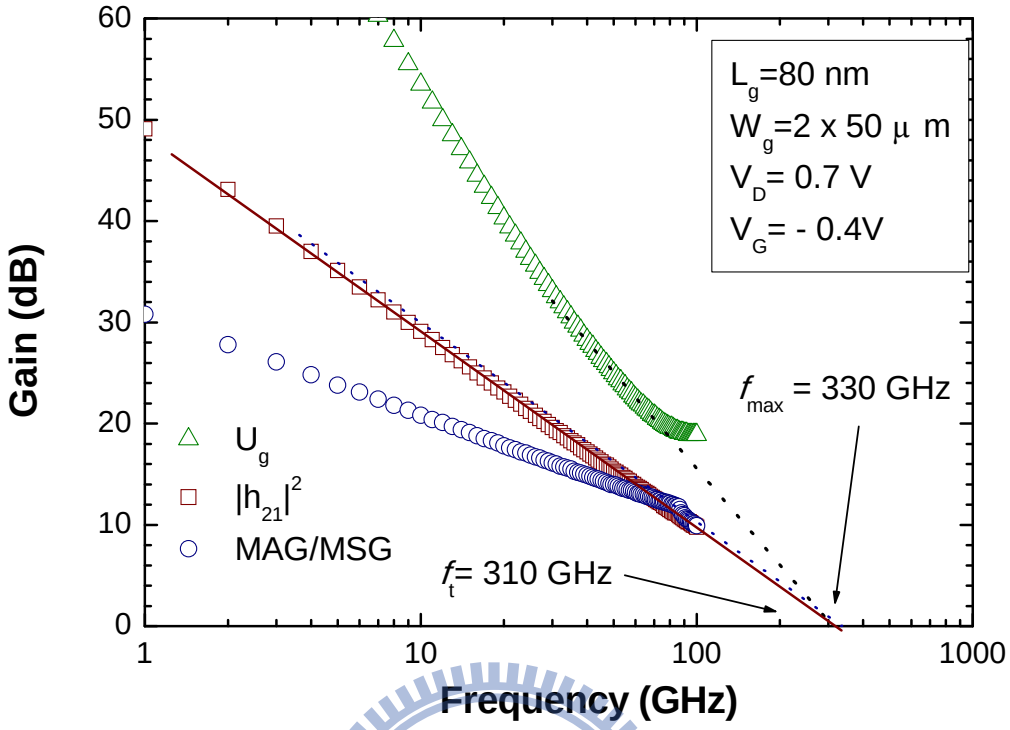


Figure 5.3(b) Typical current gain $|h_{21}|$, MAG/MSG and U_g as a function of frequency of a 0.08 μm × 100 μm InAs/InGaAs HEMT. The V_{DS} is 0.7 V, the V_G is –0.4 V.

V_{DS}	0.5V	0.6V	0.7V	0.8V	0.9V
C_{GS} (fF)	53.0	62.1	73.2	78.4	88.3
C_{GD} (fF)	35.0	24.8	23.1	20.0	18.3
RF g_m (mS/mm)	1380	1480	1870	1620	1550
f_t (GHz)	250	272	310	239	232

Table 5.1 Extracted intrinsic parameters of a 0.08 μm × 100 μm InAs/InGaAs HEMT with different drain-source voltage V_{DS} from 0.5 to 0.9 V.

Chapter 6

InAs-Channel High-Electron-Mobility Transistors for Ultralow-Power Low Noise Amplifier Applications

6.1 Introduction

Recently, space-based radar, mobile millimeter-wave communications, and handheld imagers have attracted considerable attention. Such designs favor high-gain and low-power antennas, where prime power is limited. Moreover, a large signal–to-noise ratio for feature recognition is also an important characteristic for such systems [6-1]-[6-3].

Excellent RF performance has been demonstrated by InAlAs/InGaAs high-electron-mobility transistors (HEMTs) on InP substrates[6-4]. Generally, higher electron mobility and velocity can be realized by increasing the indium content in the InGaAs channel, which makes InAs-channel heterostructure FETs (HFETs) very suitable for low-power and high-speed applications owing to their extremely high electron mobility of more than 30000 $cm^2/V \cdot s$ [6-5]-[6-6].

The superior performance of InAs-channel HEMTs is primarily attributed to their high electron mobility, peak electron velocity, and high sheet carrier density under low bias conditions that result in unparalleled speed-power performance [6-7]-[6-9]. As a result, while operating in the V_{DS} range below 0.5 V, InAs-Channel HEMT is capable of reducing dc power dissipation by an order of magnitude compared with equivalent GaAs pseudomorphic HEMTs and by a factor of 3 – 5 compared with equivalent GaAs metamorphic HEMTs [6-10]. Furthermore, the high-gain and high frequency responses of InAs-channel HEMTs have made such technology the best candidate for ultralow power low noise applications at very high

frequencies, such as space-based radar, mobile millimeter-wave communications, and handheld imager systems.

In this work, an 80-nm-gate-length InAs-channel/$In_{0.53}Ga_{0.47}As$ sub-channel HEMT for ultralow-dc-power and low noise application is presented. The excellent results clearly indicate the potential of such a device for ultralow-power circuits.

6.2 Material Growth and Device Fabrication

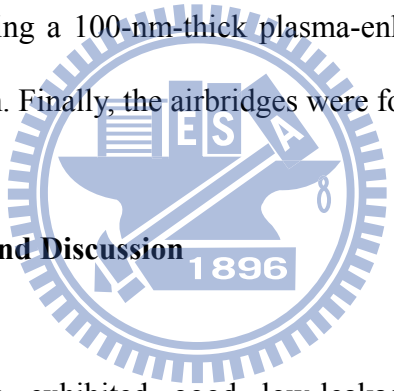
The schematic of the HEMT structure grown on a 2" semi-insulating InP substrate by molecular beam epitaxy (MBE) is shown in Fig. 6.1. The structure from bottom to top consisted of a 500-nm-thick $In_{0.52}Al_{0.48}As$ buffer layer, a 3-nm-thick $In_{0.53}Ga_{0.47}As$ lower sub-channel, a 5-nm-thick InAs channel layer, a 2-nm-thick $In_{0.53}Ga_{0.47}As$ upper sub-channel, a 3-nm-thick $In_{0.52}Al_{0.48}As$ spacer layer, a Si δ-doped (sheet density of 4×10^{12} cm^{-2}) layer, a 5-nm-thick $In_{0.52}Al_{0.48}As$ barrier, a 5-nm-thick InP etching stop layer, and a 40-nm-thick Si-doped $In_{0.53}Ga_{0.47}As$ cap ($2\times10^{19}cm^{-3}$). By succinic-acid-based wet etching, room-temperature Hall mobility measurement showed a mobility of 9520 cm^2 $V^{-1}s^{-1}$ with electronic sheet density of 2.44×10^{12} cm^{-2}.

High-indium-content devices typically suffer from a marked kink effect, low breakdown voltage, and high output transconductance caused by electron-hole pair generation. This phenomenon is even more marked for InAs/AlSb structures because of the lack of hole confinement due to type II alignment [6-5]. In this study, a higher-energy-bandgap InAs/$In_{0.53}Ga_{0.47}As$ heterostructure was used to obtain a lower gate leakage current and a higher breakdown voltage resulting in better device performance.

The InP etching stop layer was used to improve the selectivity of wet chemical recess etching and provide semiconductor surface passivation on each side of the gate to reduce the

trapping effect on the InAlAs surface [6-11]. With the use of the InP etching stop layer, the lateral recess length was easy to control and RF performance was improved [6-12].

Mesa isolation was carried out by wet chemical etching. Source and drain ohmic metals were formed with 240-nm-thick Au/Ge/Ni/Au and alloyed by rapid thermal annealing at 250 ^{o}C for 30 s. As a result of the highly Si-doped cap, a low ohmic contact resistance (R_c) of 0.025 Ω • mm and an sheet resistance (R_{sh}) of 35.3 Ω/ were obtained by the transmission line model method. T-shaped gate lithography was carried out in a 50 KeV JEOL electron beam lithography system (E-beam). The gate recess was fabricated by wet chemical etching using succinic-acid-based solution. The Ti/Pt/Au gate metal was formed by evaporation and lift off. The gate length of 80 nm was estimated by scanning electron microscopy (SEM). Devices were passivated using a 100-nm-thick plasma-enhanced chemical vapor deposition (PECVD) silicon nitride film. Finally, the airbridges were formed with 2 μm plated Au.



6.3 Experimental Results and Discussion

The fabricated device exhibited good low-leakage output current-voltage (I–V) characteristics with an 80 nm gate length and a 2×50 μm gate width, as indicated in Fig. 6.2. This device can be well pinched off with a threshold voltage of -0.7 V. Additionally, a relatively high drain current density of 430 mA/mm and a transconductance of 1120 mS/mm were observed at a low V_{DS} of 0.4 V, primarily due to the superior electron transport properties in the InAs channel.

The S-parameter of the 2×50 μm device was measured using a Cascade Microtech^{TM} on-wafer probing system with a vector network analyzer from 2 to 80 GHz. A standard load-reflection-reflection-match (LRRM) calibration method was used to calibrate the measurement system. Current gain ($|h_{21}|^2$), Mason's unilateral gain (U_g), and MAG/MSG as a

function of frequency are plotted in Fig. 6.3. The intrinsic f_T and f_{max} of the 2×50 μm device are 310 and 330 GHz at V_{DS} = 0.7V, respectively. This same device exhibits a peak cutoff frequency f_T of 120 GHz and an f_{max} of 157 GHz at a drain voltage of 0.2 V with the corresponding dc power consumption as low as 1.2 mW as shown in Fig. 6.4. Such high-gain and high-frequency responses indicate the potential of the InA-channel HEMT for ultralow-power and high-frequency applications. Figure 6.5 shows the capability of the InAs-channel HEMT technology for low power applications and the f_T/f_{max} plot with the measured maximum available gain (MAG)/maximum stable gain(MSG) at 40 GHz as a function of total dc power consumption. Note that the saturation in performance is observed at higher drain bias levels, possibly caused by the occurrence of impact ionization for small-energy-bandgap materials. The minimum noise figure and associated gain of the InAs-channel HEMT from 2 to 18 GHz at a V_{DS} of 0.2 V with a dc power dissipation of 1.2 mW are shown in Fig. 6.6. The device demonstrated a typical associated gain of 9.7 dB with a noise figure of less than 0.8 dB at 12 GHz. The same device shows a higher gain of 14.7 dB and a lower minimum noise figure of 0.29 dB at 12 GHz when biased at a higher V_{DS} of 0.5 V as shown in Fig. 6.7. Operations at different low bias voltages with different total dc power dissipations are also shown in Fig. 6.8, where possible tradeoffs between the performance and the dc power consumption can be made depending on the applications.

6.4 Conclusion

In this study, a promising candidate for ultralow-power and high-frequency applications has been demonstrated. A high f_T of 120 GHz and an f_{max} of 157 GHz were obtained at a very low bias of 0.2 V V_{DS} and a low dc power consumption of 1.2 mW. At such a low bias, the device achieved a 9.7 dB associated gain and a noise figure of less than 0.8 dB at 12 GHz.

With the high gain and low noise figure at an extremely low dc power consumption, the InAs-channel HEMTs showed tremendous potential for low-power and low-noise applications.

6.5 Figures

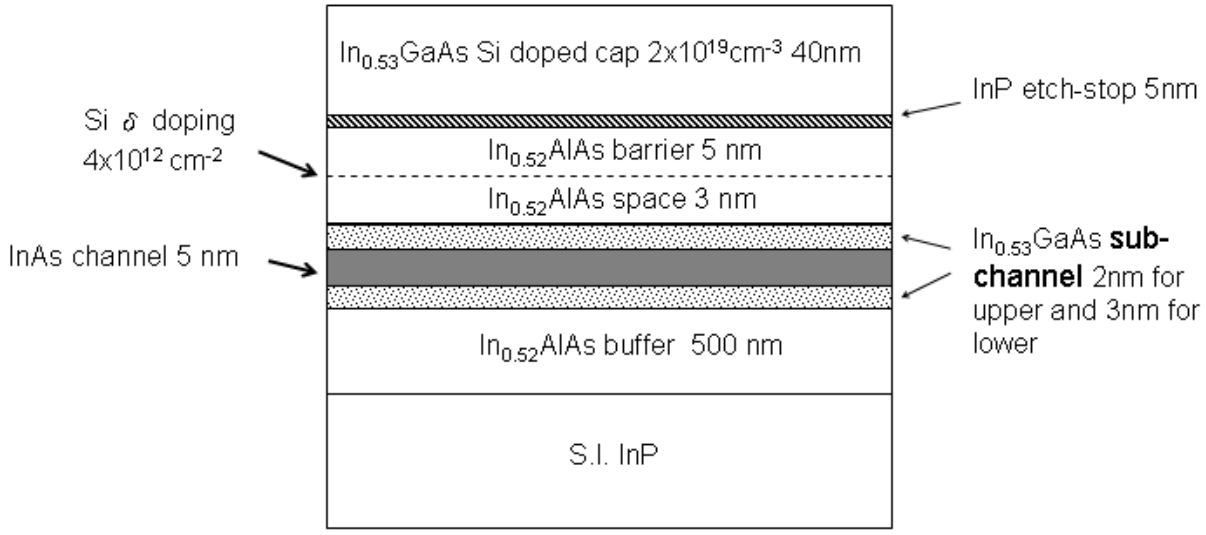


Figure 6.1. Layer structure of an InAs-channel HEMT grown by MBE on semi-insulating 2-in-diameter InP substrate.

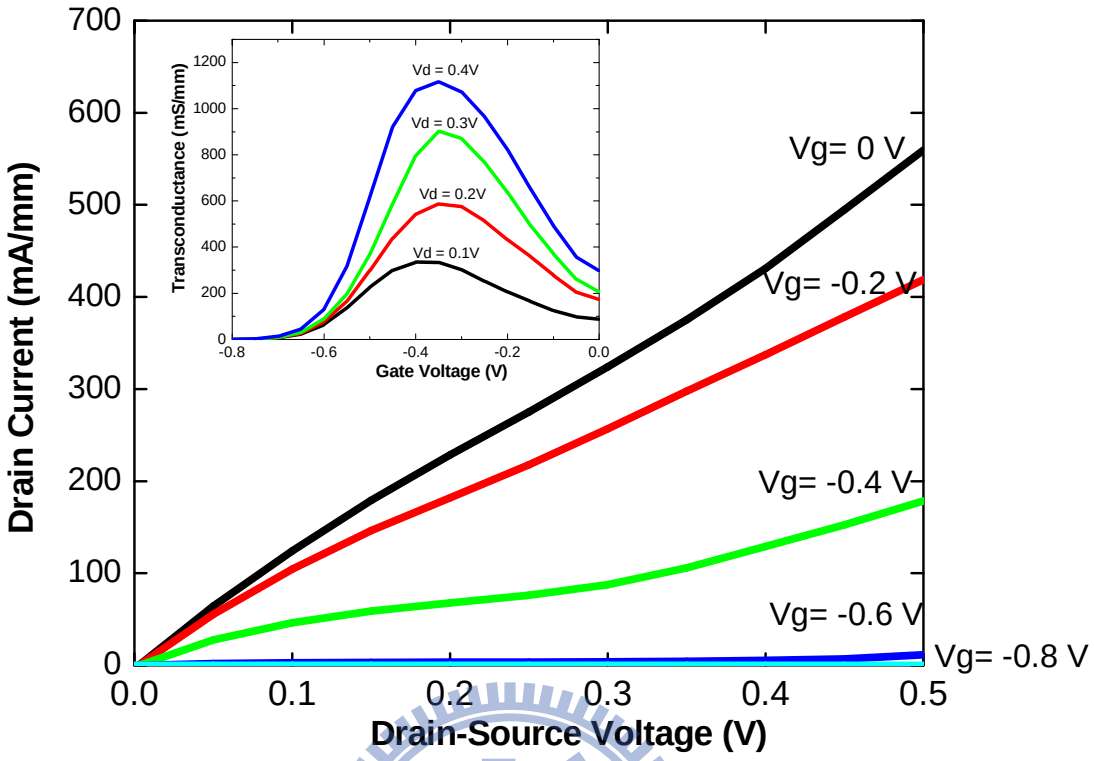


Figure 6.2. Current-voltage characteristics of 0.08 × 100 μm^2 InAs-channel HEMT.

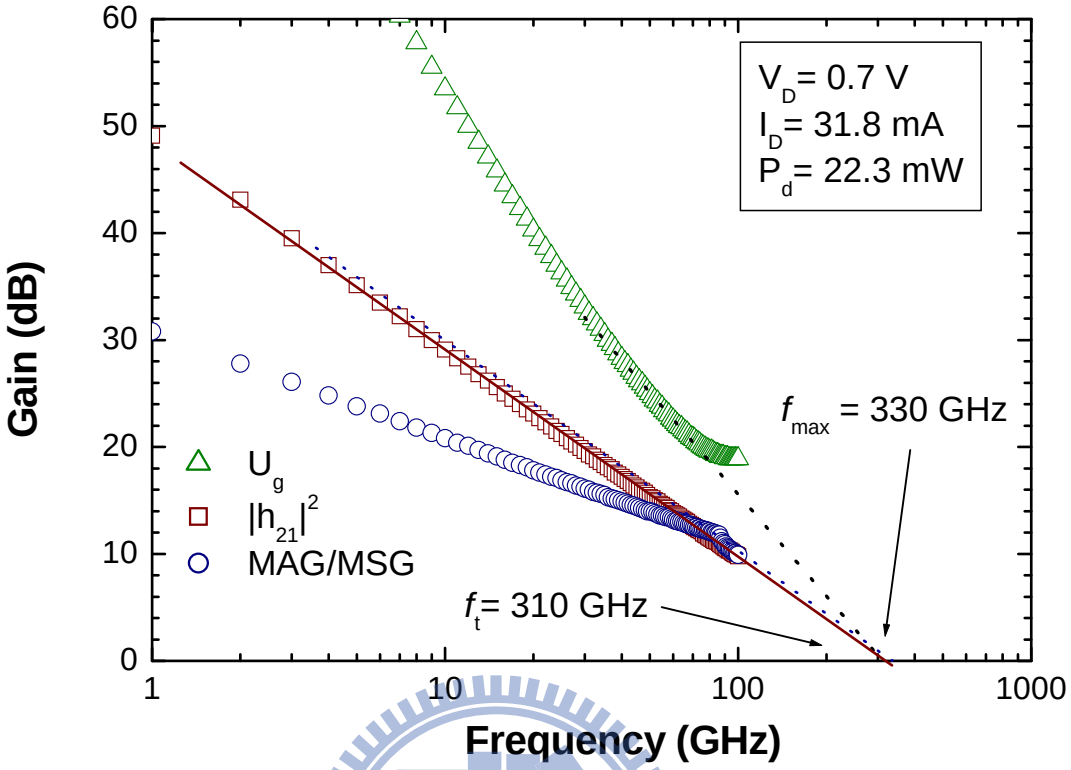


Figure 6.3. Typical current gain $|h_{21}|$, MAG/MSG and U_g as a function of frequency for a 0.08 × 100 μm^2 InAs-channel HEMT. V_{DS} is 0.7 V and the dc power is 22.3 mW.

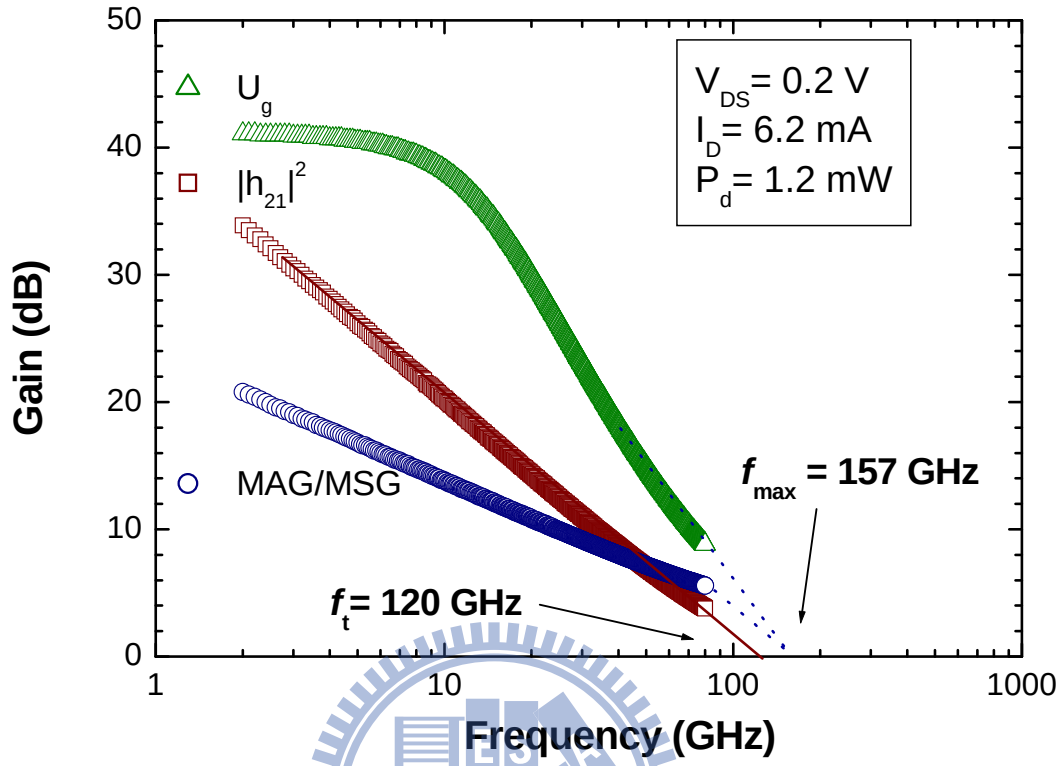


Figure 6.4. Typical current gain $|h_{21}|$, MAG/MSG and U_g as a function of frequency for a 0.08 × 100 μm^2 InAs-channel HEMT for ultralow-power operation. V_{DS} is 0.2 V and dc power is 1.2 mW.

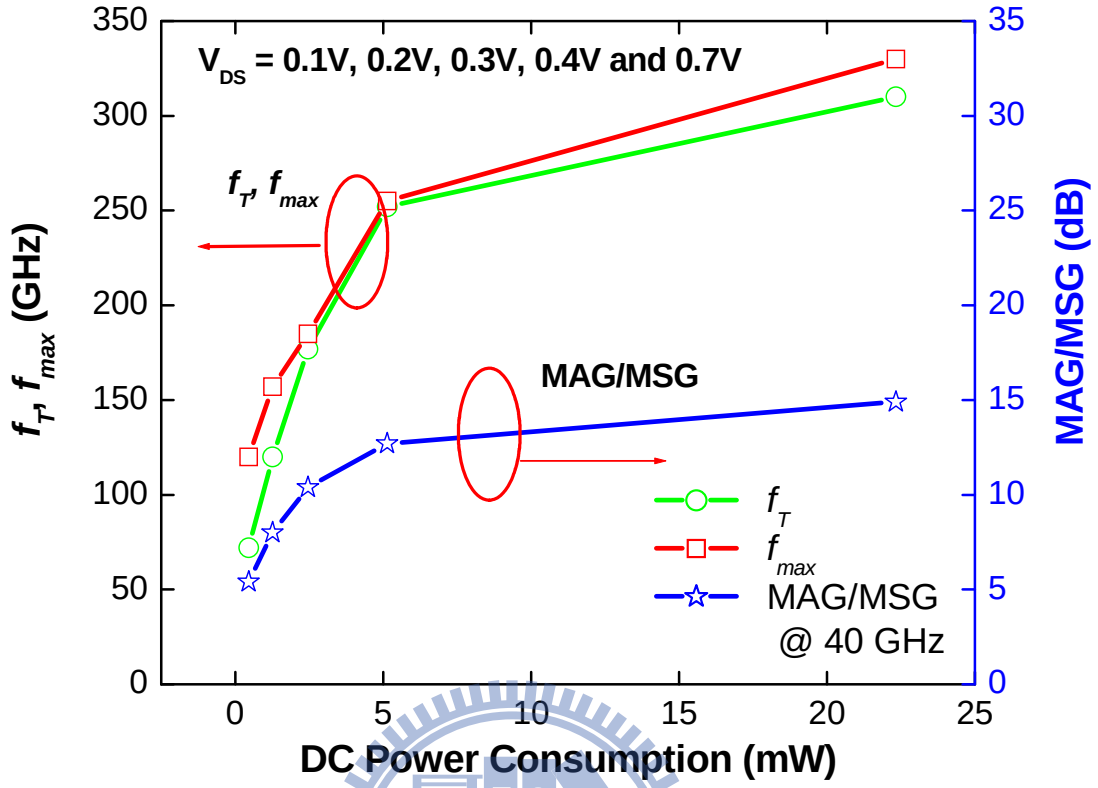


Figure 6.5. RF performance figures of merit as a function of dc power consumption for a 0.08 × 100 μm^2 InAs-channel HEMT.

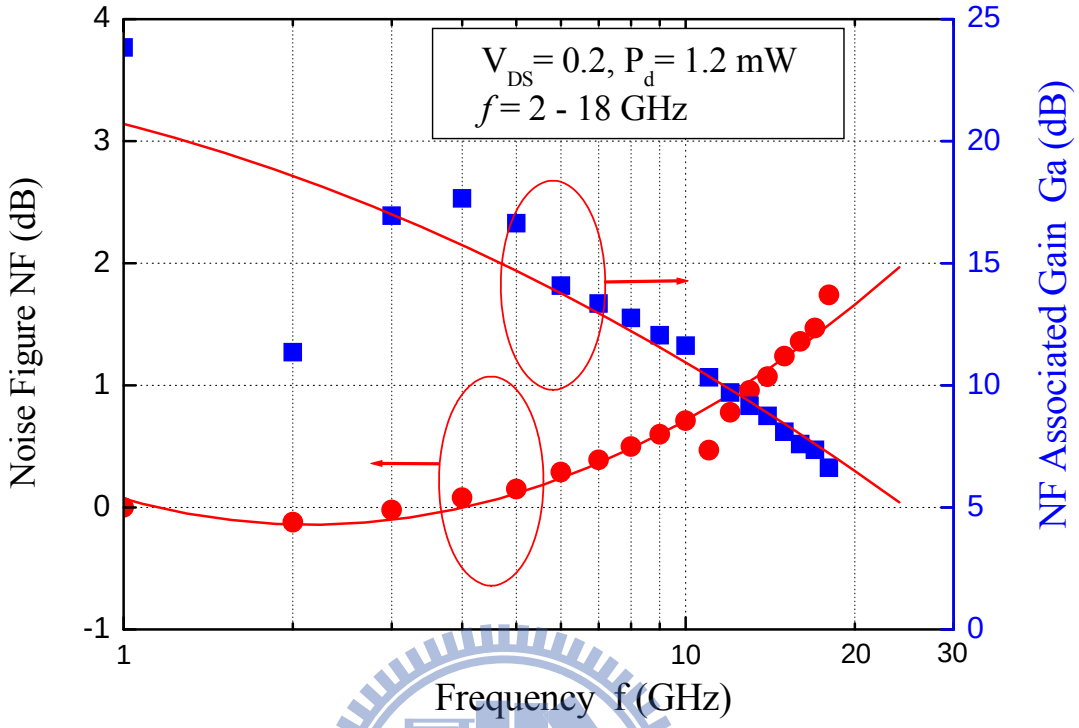


Figure 6.6. Measured minimum noise figure and associated gain of a 0.08 × 100 μm^2 InAs-channel HEMT from 2 to 18 GHz at V_{DS} of 0.2 V with a dc power dissipation of 1.2 mW.

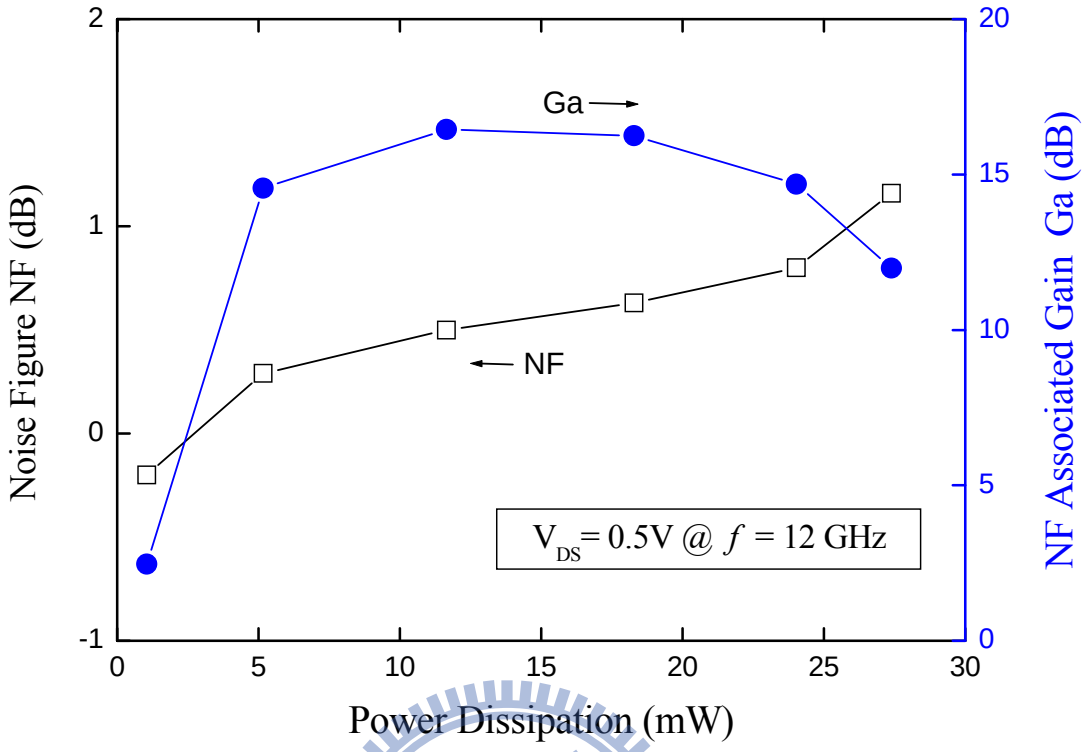


Figure 6.7. Measured minimum noise figure and associated gain of a 0.08 × 100 μm^2 InAs-channel HEMT at 12 GHz as a function of dc power consumption at a higher V_{DS} of 0.5 V.

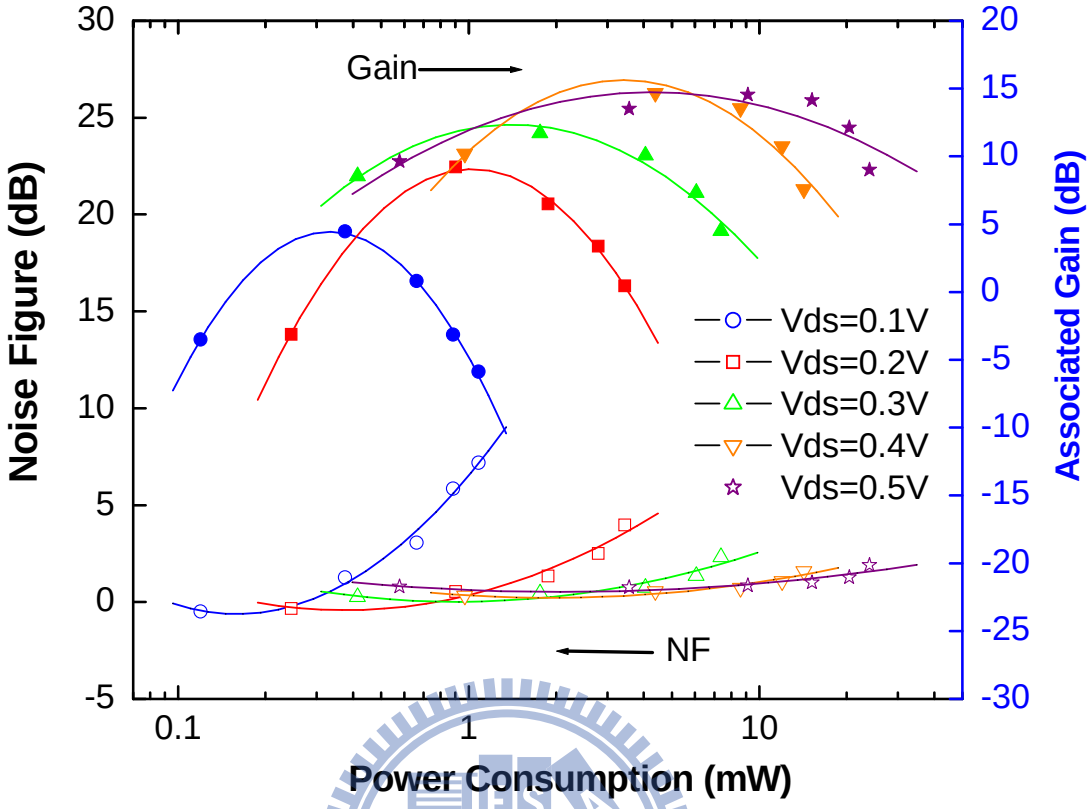


Figure 6.8. Measured minimum noise figures and associated gains of a 0.08 × 100 μm^2 InAs-channel HEMT at different V_{DS} from 0.1 V to 0.5 V with different total dc power dissipations at 12 GHz.

Chapter 7

InAs-Channel Metal-Oxide-Semiconductor HEMTs with Atomic Layer Deposited Al_2O_3 Gate Dielectric

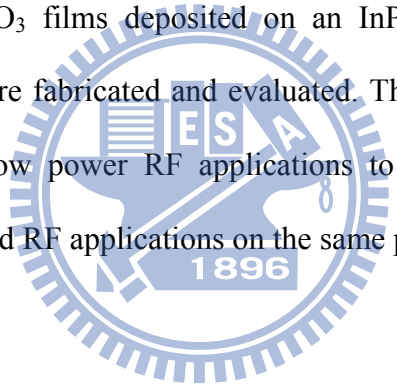
7.1 Introduction

In order to further integrate with Si complementary metal-oxide-semiconductor (CMOS) and extend CMOS front-end technique to 22 nm and beyond, planar III-V compound semiconductor field effect transistors (FETs) have been identified as one of the most attractive devices for nanoelectronic applications [7-1]-[7-3]. Intel Corporation proposed benchmarking techniques to gauge the progress of such novel nanotechnology researches for high-performance and low-power logic applications against the best Si MOSFET data [7-4]. The excellent RF-performance has been demonstrated by InAlAs/InGaAs high electron mobility transistors (HEMTs) on InP or GaAs substrate[7-5]-[7-6]. Generally, higher electron mobility and velocity can be realized by the increase of the Indium content in the InGaAs channel, which makes InAs-channel heterostructure FETs (HFETs) well suitable for low-power and high-speed logic applications owing to the extremely high electron mobility of more than 30000 cm^2/Vs [7-7]. Despite all the excellent performance, implementation of high-κ insulating gate dielectrics to further reduce the gate leakage current for performance improvement is inevitable to meet the future requirements of International Technology Roadmap for Semiconductors.

Recently, research efforts on the atomic-layer-deposited (ALD) growth of Al_2O_3 on III-V compound materials have attracted particular attentions, since the other familiar ALD Hf-based dielectrics have been widely used in Si industry [7-3], [7-8]-[7-9]. Owing to its

excellent dielectric properties with high thermal and chemical stabilities, Al_2O_3 is widely used as gate dielectric, tunneling barrier, and surface passivation. Al_2O_3 shows a high band gap (~9 eV), a high breakdown electric field (5–30 MV/cm), and a high thermal stability (over 850°C).[3] A high performance Al_2O_3/InGaAs MOSFET has been proposed and demonstrated with excellent DC performance [7-3]. For logic applications, the Al_2O_3/InGaAs MOSFET was also benchmarked with scaling metrics, such as current on/off ratio, subthreshold slop, and drain-induced barrier lowering (DIBL) and showed high potential as a candidate for integration in Si-platform [7-10].

Our previous work has successfully demonstrated high speed, low-power consumption, and low-noise InAs-channel devices with an 80-nm gate length[7-11]-[7-12]. In this letter, ALD high-κ dielectric Al_2O_3 films deposited on an InP etch-stop-layer of InAs-channel HEMTs for MOS-HEMTs are fabricated and evaluated. The main focus is on the evaluation of such devices for ultra-low power RF applications to study the feasibility of possible integration of both digital and RF applications on the same platform.



7.2 Experimental

The MOS-HEMT structure was grown on 2” semi-insulating InP substrate by molecular beam epitaxy (MBE), as shown in Fig. 7.1. The device isolation was achieved by wet chemical etch. Before ALD Al_2O_3 gate dielectric deposition, the $In_{0.53}Ga_{0.47}As$ cap layer was selectively etched by wet chemical etching using succinic-acid-based solution. The cap etching stopped at the InP etching-stop layer due to the high etching-selectivity between $In_{0.53}Ga_{0.47}As$ cap layer and InP etching-stop layer. Then wafer was treated in a diluted HCl solution (1:10) for 60 s and then the surface was dipped into an ammonium sulfide solution [$(NH_4)_2S_x$] at 60 °C for 25 min. Those treatments were performed to etch the native oxide and

tie up the dangling bonds of the surface. Following the surface clean, high quality Al_2O_3 was deposited by ALD at 300 °C and the annealed at 600 °C. Ohmic contact was formed by selectively etching the gate dielectric. Source and drain ohmic metals were formed with 240-nm-thick Au/Ge/Ni/Au and alloyed by rapid thermal annealing at 250 °C for 30 sec. In this work, the source-drain spacing for both regular HEMT and MOS-HEMTs is 3-μm. The T-shaped gate lithography was carried out in 50-KeV JEOL electron beam lithography system (E-beam). The Ti/Pt/Au gate metal was deposited by evaporation and lifted off to form the submicron T-shaped gate. The gate length of 80 nm was estimated by scanning electron microscopy (SEM). For comparison, conventional InAs-channel HEMTs without high-k dielectric have also been fabricated.

7.3 Results and Discussion

The fabricated MOS-HEMTs have a gate length of 80-nm with a high-k dielectric Al_2O_3 thickness of 3 nm. Fig. 7.2a and 7.2b show the DC current-voltage (*I–V*) characteristics with a gate bias from 0 to – 1.2 V in steps of – 0.2V. As observed from this figure, the MOS-HEMT device can be well pinched off with a threshold voltage of – 1.0 V. A maximum drain-source current (I_{DSS}) of 530 mA/mm and a high peak g_m of 1130 mS/mm were obtained for the device at a drain bias of 0.7 V. For comparison, the conventional InAs-channel HEMTs fabricated without Al_2O_3 high-k dielectric are also characterized at the same V_{DS} bias of 0.7 V, and the results are as shown in Fig. 7.2c and 7.2d. The conventional InAs-channel HEMT shows a slightly higher I_{DSS} of 830 mA/mm and peak g_m of 1550 mS/mm at a V_{DS} bias of 0.7 V. The results indicate that the addition of Al_2O_3 to the HEMT device did not cause much degradation. The InAs-channel MOS-HEMTs still maintained the superior electron transport properties in the InAs channel and demonstrated excellent DC performance. Furthermore,

there is no strong interaction between high-k dielectric interface and InAs-channel and the device operation did not rely on inversion carriers. Fig. 7.3 shows the reduction of the gate leakage current with the use of high-k gate dielectric Al_2O_3. With 7-nm ALD Al_2O_3, the InAs-channel MOS-HEMT shows the smallest gate leakage compared with the conventional one without high-k dielectric. However, for our specific device with 80-nm gate length, thinner than 5-nm gate dielectric is preferred and the Schottky layer thickness can be further reduced for the optimal aspect ratio to maintain low gate leakage and high speed logic performances simultaneously.

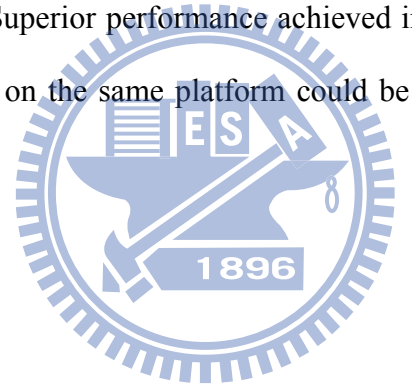
The minimum noise figure and associated gain of the InAs-channel MOS-HEMT from 20 to 60 GHz at V_{DS} of 0.6 V are shown in Fig. 7.4a. The DC power dissipation was 4.9 mW and the device demonstrated a typical associated gain of 6 dB with a noise figure of less than 2 dB as measured up to 60 GHz. To compare with the conventional InAs-channel HEMT shown in Fig. 7.4b, the MOS-HEMT devices show the same noise figure level but 2 dB lower of associated gain. Though, the MOS-HEMT showed lower transconductance compared to conventional HEMT due to the increase of the gate to channel distance, it still demonstrated excellent DC and RF performance. The InAs-channel MOS-HEMT shows great potential for high speed, ultra-low power and low-noise applications.

The S-parameter of a conventional InAs-channel HEMT without gate dielectric and an InAs-channel MOS-HEMT with 3-nm Al_2O_3 gate dielectric were measured using Cascade Microtech^{TM} on-wafer probing system with vector network analyzer from 5 to 80 GHz. A standard Load-Reflection-Reflection-Match (LRRM) calibration method was used to calibrate the measurement system. Current gain ($|h_{21}|^2$), Mason's unilateral gain (U_g) and MAG/MSG as a function of frequency are plotted in Fig. 7.5. The intrinsic f_T obtained for the InAs-channel MOS-HEMT were 185 and 265 GHz at V_{DS} = 0.3 V and 0.7 V respectively. No significant degradation was observed compared with 192 and 330 GHz for a conventional

InAs-channel HEMT at the same biases. Such high gain and high frequency response indicate the high quality of Al_2O_3/InAlAs interface is achieved and frequency response is not degraded by the interface trap density (D_{it}).

7.4 Conclusion

In this paper, we have demonstrated 80-nm InAs-channel MOS-HEMTs with high-κ gate dielectric Al_2O_3. With the high-κ gate dielectric, only small degradation of frequency response was observed. With the high gain and high frequency response, it is indicated that the InAs-channel MOS-HEMTs can be used for high frequency, low-noise figure and low-power consumption applications. Superior performance achieved indicated that future integration of digital and RF applications on the same platform could be possible with the optimal device structure.



7.5 Figures

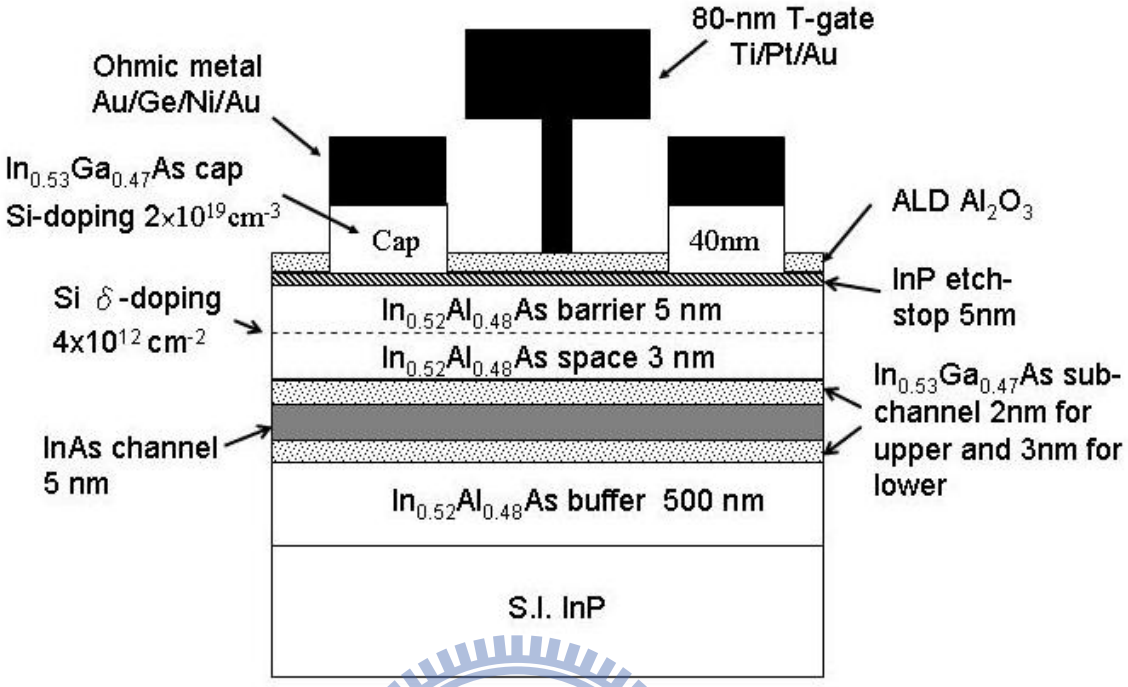


Figure 7.1. Schematic cross-sectional diagram of an InAs-channel MOS-HEMT with ALD Al_2O_3 gate dielectric.

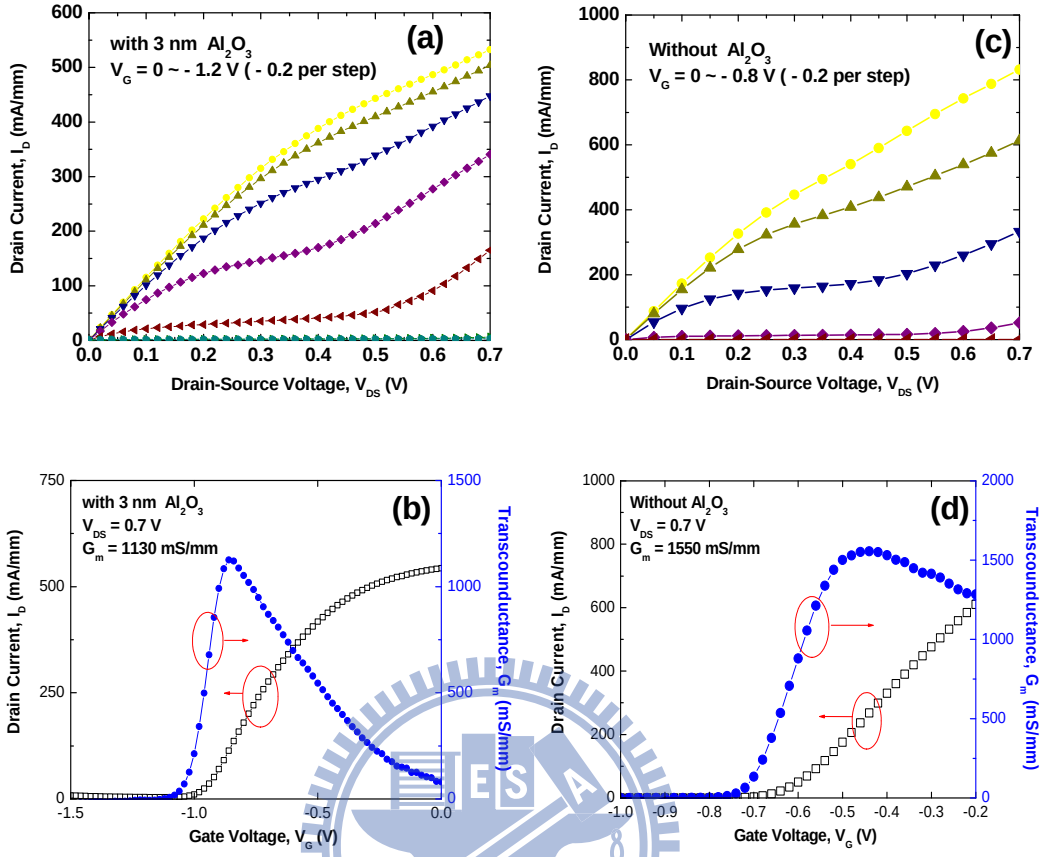


Figure 7.2. (a) Extrinsic drain current and (b) transconductance versus gate bias for an 80-nm InAs-channel MOS-HEMT with 3-nm ALD Al_2O_3 gate dielectric at a V_{DS} of 0.7 V; (c) and (d) an for InAs-channel HEMT without gate dielectric.

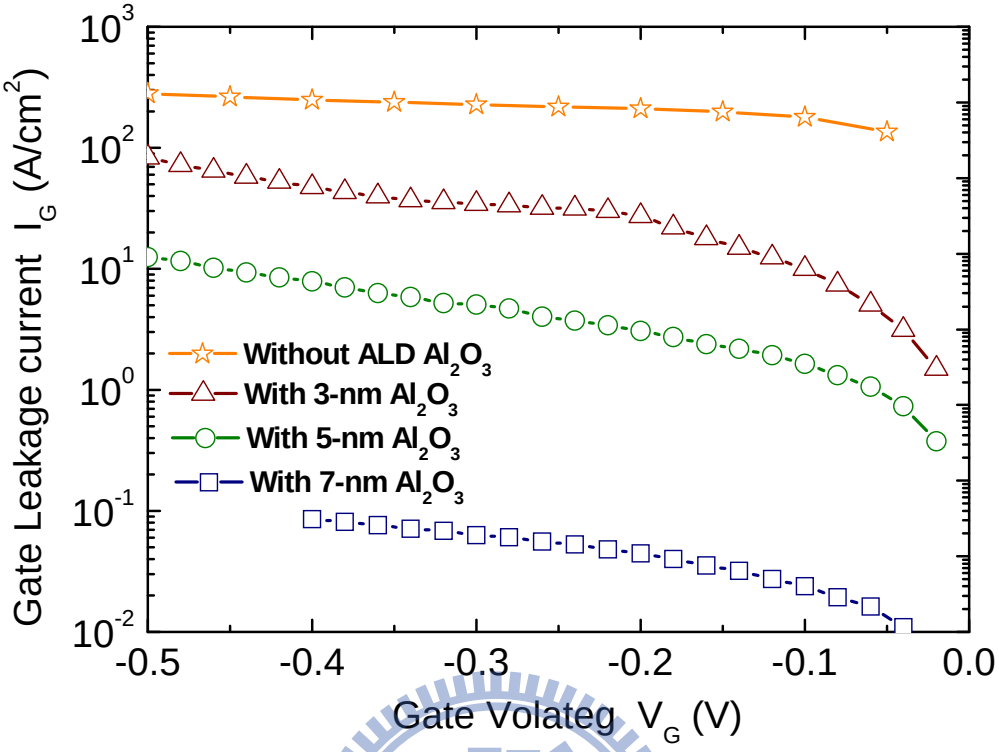


Figure 7.3. Gate leakage current versus voltage for a conventional InAs-channel HEMT and InAs-channel MOS-HEMTs with 3-nm, 5-nm, and 7-nm ALD Al_2O_3 gate dielectric.

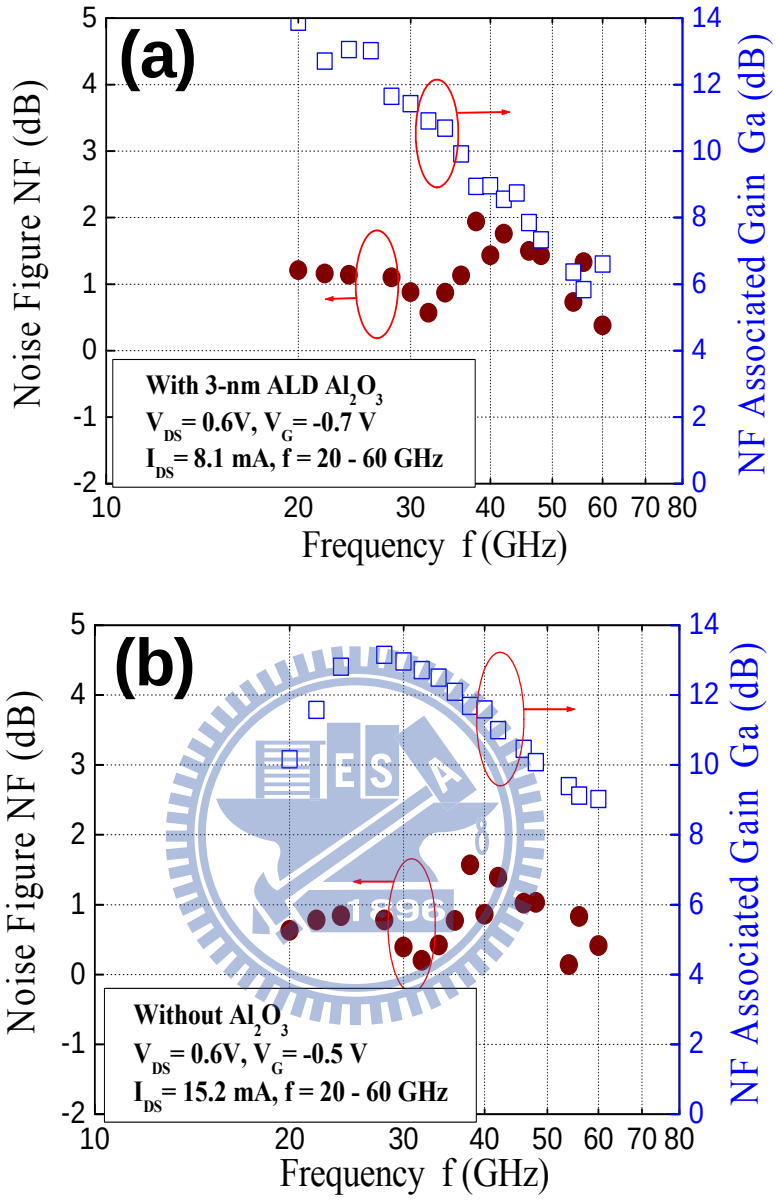


Figure 7.4. Measured minimum noise figure and associated gain (a) for an InAs-channel MOS-HEMT from 20 to 60 GHz at V_{DS} of 0.6 V with a DC power dissipation of 4.9 mW and (b) for a conventional InAs-channel HEMT from at V_{DS} of 0.6 V with a DC power dissipation of 9 mW.

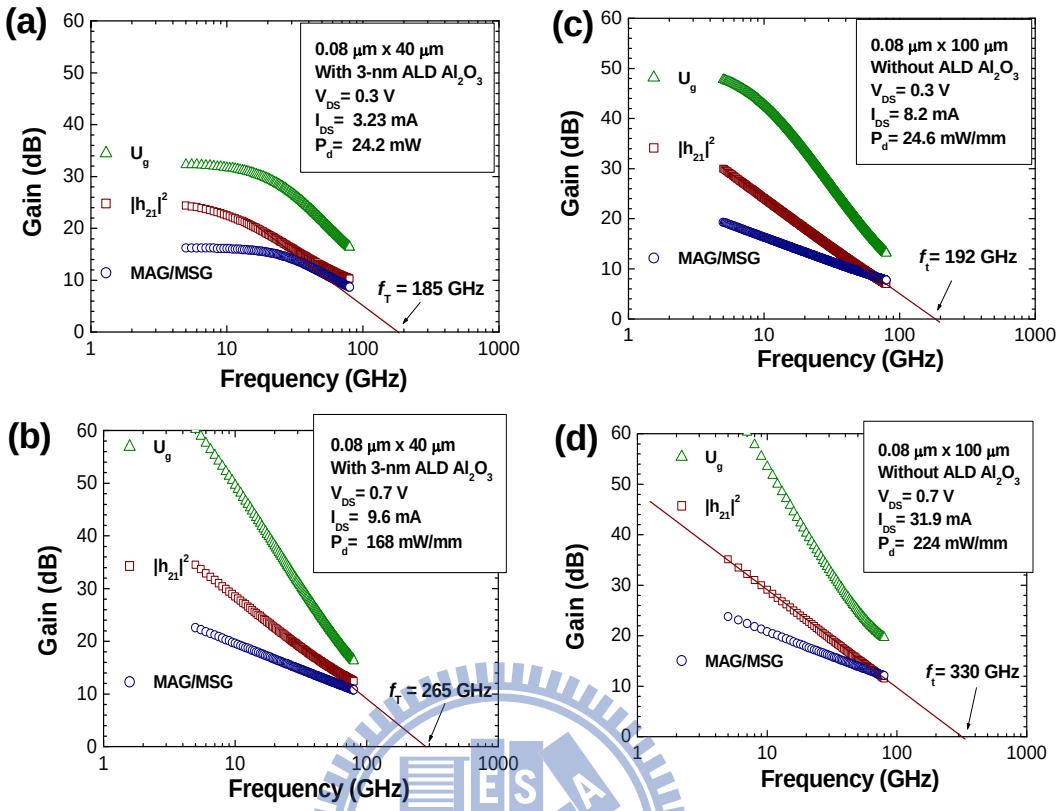


Figure 7.5. Typical current gain $|h_{21}|$, MAG/MSG and U_g as a function of frequency for an InAs-channel MOS-HEMT with 3-nm ALD Al_2O_3 at V_{DS} of (a) 0.3 V and (b) 0.7 V; for a conventional InAs-Channel HEMT without Al_2O_3 at V_{DS} of (c) 0.3 V and (d) 0.7 V respectively.

Chapter 8

Conclusion

In this dissertation, an $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ power MHEMT with double δ-doping structure and 70nm T-gate has been designed and fabricated for high frequency high power application. The MHEMT device developed shows excellent DC and RF performances with great potential for power applications at Ka-band and millimeter-wave range.

In order to enhance the device performance, the indium content in the channel region was increased to 100% to realize an InAs-channel HEMT for higher speed and low power consumption application. A high on-state breakdown voltage BV_{DS} of 1.75 V and very low gate leakage current were obtained by using $In_{0.52}Al_{0.48}As$ barrier layer and $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel structure. The effect of impact ionization on the device performance has been investigated through complete DC and RF characterizations and it is concluded that the optimum drain bias voltage for this InAs-channel device is 0.7 V. High current gain cutoff frequency (f_t) of 310 GHz and maximum oscillation frequency (f_{max}) of 330 GHz with very low gate delay time of 0.63 psec were achieved at the optimum drain voltage of 0.7 V. With the high gain and high speed at low drain voltage, such devices show tremendous potential for future high speed and low power logic applications.

The ultralow-power consumption of InAs-channel HEMTs for high frequency low noise application was also discussed. A high f_T of 120 GHz and an f_{max} of 157 GHz were obtained at a very low bias of 0.2 V V_{DS} with a low dc power consumption of 1.2 mW. At such a low bias, the device achieved a 9.7 dB associated gain and a noise figure of less than 0.8 dB at 12 GHz. With the high gain and low noise figure performance at an extremely low dc power consumption level, the InAs-channel HEMTs showed good potential for future low-power consumption ultra low-noise applications.

In order to look for alternative devices beyond Si CMOS, an 80-nm InAs-channel MOS-HEMTs with high-κ gate dielectric Al_2O_3 was fabricated and evaluated. With the high-κ gate dielectric, only small degradation of frequency response was observed. With the high gain and high frequency response, it indicates that the InAs-channel MOS-HEMTs can be used for high frequency, low-noise figure and low-power consumption applications.

Overall, in this dissertation, I have demonstrated that InAs HEMT is good for power application up to Ka-band; low noise application at Ka-band with very low power consumption; high speed logic application with very low power consumption. Furthermore, a very low noise InAs-channel MOS-HEMT structure is also proposed and demonstrated. Thus, InAs-channel HFET devices are good candidates for future very high frequency and very high speed device applications.

References

Chapter 1

[1-1] S.M. Sz, “High speed semiconductor device”, Murray Hill, New Jerey.

[1-2] T. Mimura, S. Hiyamizu, T. Fujii and K. Nanbu,” A new field-effect transistor with selectivity doped GsAs/n-$Al_xGa_{1-x}As$ Heterojunctuins,” *Jap. J. Appl. Phys.* 19, pp. L225-L227, 1980.

[1-3] Frederick H. Raab, Peter Asbeck, Steve Cripps, Peter B. Kenington, Zoya B. Popovic, Nick Pothecary, John F. Sevic and Nathan O. Sokal,” RF and Microwave Power Amplifier and Transmitter Technologies-Part 1, May 2003.

[1-4] M. I. Alsun et al., *IEDM Tech. Digest*, P. 822, 1986.

[1-5] A. Bessemoulin, “Achievements and Results”, Fraunhofer IAF, 2000.

Chapter 3

[3-1] Scott A. Wartenberg, “RF Measurements of Dies and Packages,” Artech House, Inc., 2002.

[3-2] G. F. Engen, and C. A. Hoer, “Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer,” *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-27, no. 12, pp. 987-993, Dec. 1979.

[3-3] William Liu, “Fundamentals of Ⅲ-Ⅴ Devices, HBTs, MESFETs, and HFETs/HEMTs.”

[3-4] Dieter K. Schroder, “Semiconductor Material and Device Characterization”, Wiley Interscience.

[3-5] H. Philip Li, Olin L. Hartin, and Marcus, “An Updated Temperature-Dependent Breakdown Coupling Model Including Both Impact Ionization and Tunneling Mechanisms for AlGaAs/InGaAs HEMTs,” *IEEE Transactions on Electron Devices,* vol. 49, no. 9, Sep 2002.

[3-6] Sun-Chin Wei, “Electrical Analysis and Low-Frequency Noise Investigations of the AlGaN/GaN High Electron Mobility Transistors,” Department of Electrical Engineering National Cheng Kung University, Tainan, Taiwan, R.O.C

[3-7] 本城和彦, ”微波通訊半導體電路,” 全華科技圖書.

[3-8] OSAMU WADA et al., "InP-Based Materials and Devices Physics and Technology," p.361.

[3-9] Jones, K. and E. Godshalk, "Waveguide Probe Tackles V-Band On-Wafer Tests," Microwaves & RF, vol. 29, no. 10, pp. 99-103, 1999.

Chapter 4

[4-1] M. Zaknoune, M. Ardouin, Y. Cordier, S. Bollaert, B. Bonte, and D. Théron: IEEE Electron Device Lett. **24** (2003) 724.

[4-2] M.-Y. Kao, P. M. Smith, P. Ho, P.-C. Chao, H. H. G. Duh, A. A. Jabra, and J. M. Ballingall: IEEE Electron Device Lett. **10** (1989) 580.

[4-3] Y. Yamasjita, A. Endoh, K. Shinohara, K. Hikosaka, and T. Matsui: IEEE Electron Device Lett. **23** (2002) 573.

[4-4] L. D. Nguyen, A. S. Brown, M. A. Thompson, and L. M. Jelloian: IEEE Trans. Electron Devices **39** (1992) 2007.

[4-5] D.-W. Tu, S. Wang, J. S. M. Liu, K. C. Hwang, W. Kong, P. C. Chao, and K. Nichols: IEEE Microwave Guided Wave Lett. **9** (1999) 458.

[4-6] C. S. Whelan, W. E. Hoke, R. A. McTaggart, S. M. Lardizabal, P. S. Lyman, P. F. Marsh, and T. E. Kazior: IEEE Electron Device Lett. **21** (2000) 5.

[4-7] D. C. Dumka, H. Q. Tserng, M. Y. Kao, E. A. Beam III, and P. Saunier: IEEE Electron Device Lett. **24** (2003) 135.

[4-8] S. C. Wang, J. S. Liu, K. C. Hwang, W. Kong, D. W. Tu, P. Ho, L. Mohnkern, K. Nichols, and P. C. Chao: IEEE Electron Device Lett. **21** (2000) 335.

Chapter 5

[5-1] Y. Yamasjita, A. Endoh, K. Shinohara, K. Hikosaka, and T. Matsui, "Pseudomorphic In0.52Al0.48As/In0.7Ga0.3As HEMTs with an ultrahigh f_T of 562 GHz," *IEEE*

Electron Device Lett., vol. 23, no. 10, pp. 573–575, Oct. 2002.

[5-2] C. R. Bolognesi, "Antimonide-based high-speed electronics: a transistor perspective," in *Proc. 14th Int. Conf. IPRM*, May 2002, pp. 55–58.

[5-3] G.. Tuttle and H. Kroememr, "An AlSb–InAs–AlSb quantum well HFET," *IEEE Trans. Electron Devices*, vol. ED-34, no. 11, pp. 2358, Nov. 1987.

[5-4] Y. Royter, K. R. Elliott, P. W. Deelman, R. D. Rajavel, D. H. chow, I. Milosavljevic, and C. H. Fields, "High-frequency InAs-channel HEMTs for low power ICs," in *IEDM Tech. Dig.*, Dec. 2003, pp. 30.7.1–30.7.4.

[5-5] Leuther, R. Weber, M. Dammann, M. Schlechtweg, M. Mikulla, M. Walther and G. Weimann, "Metamorphic 50 nm InAs-channel HEMT," in *Proc. 17th Int. Conf. IPRM*, May 2005, pp. 129–132.

[5-6] G. Meneghesso, D. Buttari, E. Perin, C. Canali, and E. Zanoni, "Improvement of DC, low frequency and reliability properties of InAlAs–InGaAs InP-based HEMTs by means of an InP etch stop layer," in *IEDM Tech. Dig.*, Dec. 1998, pp. 227–230.

[5-7] T. Suemitsu, H. Yokoyama, T. Ishii, T. Enoki, G. Meneghesso, and E. Zanoni, "30-nm two-step recess gate InP-based InAlAs/InGaAs HEMTs," *IEEE Trans. Electron Devices*, vol. 49, no. 10, pp. 1694–1700, Oct. 2002.

[5-8] C. Kadow, M. Dahlström, J.-U. Bae, H.-K. Lin, A. C. Gossard, M. J. W. Rodwell, B. Brar, G. J. Sullivan, G. Nagy, J. I. Bergman, "n^+-InAs–InAlAs recess gate technology for InAs-channel millimeter-wave HFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 151–158, Feb. 2005.

[5-9] C. R. Bolognesi, M. W. Dvorak, and D. H. Chow, "Impact Ionization Suppression by Quantum Confinement: Effects on the DC and Microwave Performance of Narrow-Gap Channel InAs/AlSb HFET's," *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 826–832, Feb. 1999.

[5-10] J. Bergman, G. Nagy, G. Sullivan, B. Brar, C. Kadow, H.-K. Lin, A. Gossard, and M. Rodwell, "InAs/AlSb HFETs with f_t and f_{max} above 150 GHz for low-power MMICs," in *Proc. 15th Int. Conf. IPRM*, May 2003, pp. 219–222.

[5-11] K. Shinohara, Y. Yamashita, A. Endoh, I. Watanabe, K. Hikosaka, T. Matsui, T. Mimura, and S. Hiyamizu, "547-GHz f_t $In_{0.7}Ga_{0.3}As$–$In_{0.52}Al_{0.48}As$ HEMTs with reduced source and drain resistance," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 241–243, Jan. 2004.

[5-12] D.-H. Kim, J. A. Alamo, J.-H. Lee, and K.-S. Seo, "The impact of side-recess spacing on the logic performance of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs," in *Proc. 18th Int. Conf. IPRM*, May 2006, pp. 177–180.

[5-13] R. Chau, S. Datta, M. Docyz, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, "Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications", *IEEE Trans. Nanotechnology*, Vol. 4, No. 2, pp. 153–158, 2005

Chapter 6

[6-1] S. Fiedler and B. Preiss: IEEE Aerospace Applications Conf., 1996, vol. 4, p. 77.

[6-2] W. R. Deal, R. Tsai, M. D. Lange, J. B. Boos, B. R. Bennett, and A. Gutierrez: IEEE Microwave Wireless Components Lett. **15** (2005) 208.

[6-3] J. B. Hacker, J. Bergman, G. Nagy, G. Sullivan, C. Kadow, H.-K. Lin, A. C. Gossard, M. Rodwell, and B. Brar: IEEE Microwave. Wireless Components Lett. **14** (2004) 156.

[6-4] Y. Yamashita, A. Endoh, K. Shinohara, K. Hikosaka, and T. Matsui: IEEE Electron Device Lett. **23** (2002) 573.

[6-5] C. R. Bolognesi: Proc. 14th Int. Conf. IPRM, 2002, p. 55.

[6-6] G. Tuttle and H. Kroemer: IEEE Trans. Electron Devices **34** (1987) 2358.

[6-7] J. B. Boos, W. Kruppa, B. R. Bennett, D. Park, S. W. Kirchoefer, R. Bass, and H. B. Dietrich: IEEE Trans. Electron Devices **45** (1998) 1869.

[6-8] J. Bergman, G. Nagy, G. Sullivan, B. Brar, C. Kadow, H.-K. Lin, A. Gossard, and M. Rodwell: Proc. International Indium Phosphide and Related Materials Conf., 2003, p. 219.

[6-9] C. Y. Chang, H. T. Hsu, E. Y. Chang, C. I. Kuo, S. Datta, M. Radosavljevic, Y. Miyamoto, and G.. W. Huang: IEEE Electron Device Lett. **28** (2007) 856.

[6-10] C. Y. Chang, E. Y. Chang, Y. C. Lien, Y. Miyamoto, C.-I Kuo, S.-H. Chen, and L.-H. Chu: Jpn. J. Appl. Phys. **46** (2007) 3385.

[6-11] G. Meneghesso, D. Buttari, E. Perin, C. Canali, and E. Zanoni: IEDM Tech. Dig., 1998, p. 227.

[6-12] T. Suemitsu, H. Yokoyama, T. Ishii, T. Enoki, G. Meneghesso, and E. Zanoni: IEEE Trans. Electron Devices 49 (2002) 1694.

Chapter 7

[7-1] R. Chau, S. Datta, and A. Majumdar, in IEEE Compound Semiconductor Integrated Circuit Symposium, pp. 4 (2005).

[7-2] M. Passlack, J. K.Abrokwah, R. Droopad, Z. Yu, C. Overgaard, S. I. Yi, M. Hale, J. Sexton, and A. C. Kummel, IEEE Electron Device Lett., **23**, 508 (2002).

[7-3] Y. Xuan, Y. Q. Wu, and P. D. Ye, IEEE Electron Device Lett., **29**, 294 (2008).

[7-4] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, IEEE Trans. Nanotechnology, **4**, 153 (2005).

[7-5] Y. Yamashita, A. Endoh, K. Shinohara, K. Hikosaka, and T. Matsui, IEEE Electron Device Lett., **23**, 573 (2002).

[7-6] W. Ha, K. Shinohara, and B. Brar, IEEE Electron Device Lett., **29**, 419 (2008).

[7-7] C. R. Bolognesi, in Proc. 14th Int. Conf. IPRM, 55 (2002).

[7-8] Y. Sun, E. W. Kiewra, J. P. de Souza, J. J. Bucchignano, K. E. Fogel, D. K. Sadana, and G. G. Shaidi, IEEE Electron Device Lett., **30**, 5 (2009).

[7-9] Y. Xuan, H. C. Lin, and P. D. Ye, Appl. Phys. Lett., **88**, 263518 (2006).

[7-10] Y. Q. Wu, W. K. Wang, O. Koybasi, D. N. Zakharov, E. A. Stach, S. Nakahara, J. C. M. Hwang, and P. D. Ye, IEEE Electron Device Lett., **30**, 700 (2009).

[7-11] C. Y. Chang, H. T. Hsu, , E. Y. Chang, C. I. Kuo, S. Datta, M. Radosavljevic, Y. Miyamoto, and G. W. Huang, IEEE Electron Device Lett., **28**, 856 (2007).

[7-12] C. Y. Chang, H. T. Hsu, E. Y. Chang, and Y. Miyamoto, Jpn. J. Appl. Phys., 48, 04C094 (2009).

個人簡歷（Vita）

Chia-Yuan Chang 張家源

Department of Materials Science and Engineering
National Chiao-Tung University 1001 Ta-Hsueh Rd. Hsin-Chu 30050, Taiwan, R.O.C.
Tel: (886)-3-5712121 ext.52969
Fax: (886)-3-5745497
E-mail: cychang.mse92g@nctu.edu.tw

Biography

He was born in Taiwan, R.O.C, on July 17, 1978. He received the B.S. degree in physics from National Changhua University of Education, Taiwan in 2000 and M.S. degree in physics from National Tsing Hua University, Taiwan in 2002.

He is currently pursuing the Ph.D. degree in material science and engineering at National Chiao-Tung University, Hsin-Chu. In Prof. Edward Yi Chang's research group, his research interests are fabrication and characterization of High Electron Mobility Transistor (HEMT) for high frequency applications.

With Prof. Edward Yi Chang's guidance, he has fabricated an InAs-channel HEMT with excellent performance of over 500 GHz f_T. Recently, his research focuses on the integration of high-k material on III-V HEMTs.

Education

2003- Ph.D. candidate, Department of Material Science and Engineering, National Chiao-Tung University, Taiwan.

2000 – 2002 M.S. Department of Physics, National Tsing Hua University, Taiwan.

1996 – 2000 B.S. Department of Physics, National Changhua University of Education, Taiwan.

Experience

2007. July – 2007. August Summer program research in Tokyo Institute of Technology

2009. May – 2010 Feb. Internship in Nippon Telegraph and Telephone Basic Research Laboratories.

Expertise:

- High-K MOS-HEMTs
- III-V compound semiconductor devices
- GaAs based mechanical resonators
- Semiconductor device physics
- Semiconductor process
- Materials characterization
- Electronics

Publication List

Journal:

[1] **Chia-Yuan Chang,** Heng-Tung Hsu, Edward Yi Chang, Hai-Dang Trinh, and Yasuyuki Miyamoto, "InAs-Channel Meta-Oxide-Semiconductor HEMTs with Atomic-Layer-Deposited Al_2O_3 Gate Dielectric", *Electrochemical and Solid-State Letters*, **12** (12) H456-H459 (2009).

[2] **Chia-Yuan Chang**, Heng-Tung Hsu, Edward Yi Chang and Yasuyuki Miyamoto, "InAs-Channel High-Electron-Mobility Transistors for Ultralow-Power Low Noise Amplifier Applications", Jpn. J. Appl. Phys., Vol. 48, No. 4, pp. 04C094-1 – 04C094-3, 2009

[3] **Chia-Yuan Chang**, Heng-Tung Hsu, Edward Yi Chang, Chien-I Kuo, Marko Radosavljevic, Yasuyuki Miyamoto, and Guo-Wei Huang, "Investigation of Impact Ionization in InAs-Channel HEMT for High-Speed and Low-Power Applications", *IEEE Electron Device Lett.*, VOL.28, No.10, pp. 856-858, 2007.

[4] **Chia-Yuan CHANG**, Edward Yi CHANG, Yi-Chung LIEN, Yasuyuki MIYAMOTO, Chien-I KUO, Szu-Hung CHEN, and Li-Hsin CHU, "High-Performance $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ Power Metamorphic High Electron Mobility Transistor for Ka-Band Applications", Jpn. J. Appl. Phys., Vol. 46, No. 6A, pp. 3385-3387, 2007.

[5] Chien-I Kuo, Heng-Tung Hsu, Edward Yi Chang, **Chia-Yuan Chang**, Yasuyuki Miyamoto, Suman Dat, Marko Radosavljevi, Guo-Wei Huang and Ching-Ting Lee, "RF and logic performance improvement of $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ composite-channel HEMT using gate-sinking technology" *IEEE Electron Device Lett.*, vol. 29, No. 4, pp. 290-293. 2008.

[6] Yi-Chung Lien, Szu-Hung Chen, Edward Yi Chang, Li-Hsin Chu, and **Chia-Yuan Chang**, "Fabrication of 0.15-μm Γ-Shaped Gate In0.52Al0.48As/ In0.6Ga0.4As Metamorphic HEMTs Using DUV Lithography and Tilt Dry-Etching Technique," *IEEE Electron Device Lett.*, vol. 28., pp. 93-95. 2007.

[7] Chien-I Kuo, Edward Yi Chang, Heng-Tung Hsu, Chun-Chi Chen, and **Chia-Yuan Chang**, "Metamorphic $In_{0.53}Ga_{0.47}As$ Metal-Oxide-Semiconductor Structure on a GaAs substrate with Zr high-k dielectrics," Japan Journal of Applied Physics, Vol 47, No. 5, 2008.

[8] Edward Yi Chang, Jui-Chien Huang, Yueh-Chin Lin, Yen-Chang Hsieh, and **Chia-Yuan Chang**, "AlGaAs/InGaAs High Electron Mobility Transistor Grown on Si Substrate with

Ge/Ge_xSi_{1-x} Metamorphic Buffer Layers," Japan Journal of Applied Physics, Vol 47, pp. 7069-7072, 2008.

Conference:

[1] **Chia-Yuan Chang,** Edward Yi Chang, We-Ching Huang, Yung-Hsuan Su, Hai-Dang Trinh, Heng-Tung Hsu, and Yasuyuki Miyamoto, "InAs-Channel Meta-Oxide-Semiconductor HEMTs with Atomic-Layer-Deposited Al_2O_3 Gate Dielectric", 216th ECS Meeting, Vienna, Austria, vol. 25, Issue 6, pp. 87-92, Oct. 4 – Oct. 9, 2009.

[2] **Chia-Yuan Chang**, Heng-Tung Hsu, Edward Yi Chang and Yasuyuki Miyamoto, "InAs-Channel HEMTs for Ultra-low-Power LNA Applications", 2008 International Conference on Solid State Devices and Materials (SSDM 2008), G-2-3, Tsukuba, Sept., 2008.

[3] **Chia-Yuan CHANG**, Edward Yi CHANG, Yi-Chung LIEN, Yasuyuki MIYAMOTO, Chien-I KUO, Szu-Hung CHEN, and Li-Hsin CHU, "High-Performance $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ Power Metamorphic High Electron Mobility Transistor for Ka-Band Applications", *IEEE* International Conference On Semiconductor Electronics, 2006.

[4] Chien-I Kuo, Heng-Tung Hsu, Edward Yi Chang, Chia-Ta Chang, **Chia-Yuan Chang** and Yasuyuki Miyamoto, "Investigation of Impact Ionization from $In_xGa_{1-x}As$ to InAs Channel HEMTs for High Speed and Low Power Applications," in 20th IPRM WP 62 2008.

[5] Edward Yi Chang , Chien-I Kuo, Heng-Tung Hsu, and **Chia-Yuan Chang**, "InAs/$In_{1-x}Ga_xAs$ Composite Channel High Electron Mobility Transistors for High Speed Applications," in EuMW IC 2008.

[6] Edward Yi Chang, **Chia-Yuan Chang**, Heng-Tung Hsu, "HEMT for high speed electronic applications: from InGaAs to InAs channel devices", The 34th International Symposium on Compound Semiconductors (ISCS 2007), Kyoto, Japan, Oct.15-18, 2007. (Invited)

[7] H. T. Hsu, **C. Y. Chang**, Edward Yi Chang, C. I. Kuo, and Yssuyuki Miyamoto, "High Performance InAs-Channel HEMT for Low Voltage Milimeter Wave Applications", Asia-Pacific Microwave Conference, TH A2-F4, Thailand 2007.

[8] Chien-I Kuo, Heng-Tung Hsu, **Chia-Yuan Chang**, Edward Yi Chang, and Heng-shou

Hsu, “Evaluation of RF and Logic Performance of 80 nm InAs/ $In_{0.7}Ga_{0.3}As$ Composite Channel HEMT using gate sinking technology,” 2007 IEEE Electron Device and Solid-State Circuits, E 07,pp. 255-258, Tainan.