國立交通大學

材料科學與工程學系

博 士 論 文

ESA 1896

(鎳、鈦與鎢)氧化物之電性及應用於電阻式隨機記憶體研究

Electric Characteristics and Application of (Nickel, Titanium and Tungsten) Oxides on Resistive Random Access Memory (RRAM)

研 究 生：李明道

指導教授：姚永德 教授

中 華 民 國 一百零一 年 一 月

(鎳、鈦與鎢)氧化物之電性及應用於電阻式隨機記憶體研究

Electric Characteristics and Application of (Nickel, Titanium and Tungsten) Oxides on Resistive Random Access Memory (RRAM)

研 究 生：李明道　　　　Student : Ming-Daou Lee

指導教授：姚永德　　　　Advisor : Yeong-Der Yao

國 立 交 通 大 學
材料科學與工程學系
博 士 論 文

A Thesis
Submitted to Department of Materials Science and Engineering
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy
in

Materials Science and Engineering

January 2012

Hsinchu, Taiwan, Republic of China

中華民國一百零一年一月

(鎳、鈦與鎢)氧化物之電性及應用於電阻式隨機記憶體研究

學生:李明道　　　　　　　　　　　　　　　　指導教授: 姚永德教授

國立交通大學 材料科學與工程 學系（研究所）博士班

摘　　要

近年來，由於傳統浮動閘極結構之非揮發性記憶體(Flash memory)在小於二十奈米節點技術將面臨其物理極限，一些新式非揮發性記憶體如磁阻式記憶體(MRAM)、相變化記憶體(PCRAM)、以及電阻式記憶體(RRAM)之研究在下世代資訊儲存應用也變得越趨重要。另一方面，由於某些電阻式記憶體材料具備 CMOS 製程完全相容、高存取速度、高可靠度、以及高容量等優越特性在下世代記憶體元件中具有高商業價值潛力，故本篇論文也聚焦於 RRAM 之相關研究。

雖然有很多金屬氧化物材料可應用於 RRAM 元件，然而與 CMOS 製程完全相容的材料包含氧化鎳、氧化鈦以及氧化鎢三種材料而且在 RRAM 特性上也有不錯的表現。在 CMOS 製程中鎳化矽(NiSi)用於中段製程，其作用為降低金氧半導體(MOS)接面上的阻值，氮化鈦(TiN)則用於中段以及後段製程(BEOL)，其目的為增加金屬附著性以及當作擴散阻障層，而金屬鎢(W)則廣用於中段接觸(Contact)製程，為 CMOS 元件與後段電路連接的主要金屬材料，綜觀以上特點，以氧化鎳、氧化鈦或是氧化鎢作為電阻式記憶體元件材料可與現今半導體 CMOS 製程完全相容。而在本篇論文中將深入探討這三種材料之 RRAM 特性包括電性表現、電阻翻轉機制以及相關之應用。

在實驗中我們發現氧化鎳材料屬於多晶結構而且具有雙極式 (Bipolar) RRAM 特性，其電性顯示出薄膜特性而且電性表現與氧化程度有著直接的關係，氧化程度越高的樣品其電阻變化也相對明顯，而電子的傳導遵循著蕭基發射(Schottky emission)傳導機制，藉由此一機制可以得知蕭基能障的變化與元件電阻的變化息息相關，此外更可以得知氧化程度越低的樣品其介電常數越高，這也進一步解釋了低氧化程度的樣品在電阻翻轉過程中需要更大的外加電壓才足夠抵銷樣品內部所產生的反向電場。

類似於氧化鎳材料系統，氧化鈦材料同樣擁有雙極式 RRAM 特性，其電性表現顯示出明顯的界面特性，薄膜厚度對其電性表現影響不大，其電子的傳導機制與氧化鎳材料相同都遵循著蕭基發射傳導機制，而且蕭基能障的變化也與元件電阻的變化有著直接的關係，而在氧化鈦/氧化矽複合材料的實驗當中進一步證實氧化鈦 RRAM 的界面特性，而且此一複合材料的資訊保存能力也比單一氧化鈦薄膜有著明顯的改善。

而在氧化鎢薄膜的實驗當中，我們發現這種材料有著多方面應用的潛力，舉例來說，它不但可以用於單次儲存(OTP)而且可以用於多次儲存(MTP)記憶體裝

置，而在多次儲存記憶體裝置中又可以使用雙極式以及單極式(Unipolar)操作來控制其電阻阻態，而且耐久性皆大於一千次，由於這種材料也具有相當大的電阻阻距，因此非常適合用於多層單元(MLC)儲存記憶體的應用，而且在製程微縮的實驗中得知氧化鎢電阻式記憶體有著製程微縮的可行性，這種材料也展現出高可靠度特性，例如在攝氏二百五十度的高溫環境之下表現出超過一千小時的熱穩定性。

而在電子傳導機制中氧化鎢電阻式記憶體之低電阻狀態表現出接近於導體的 minimum-metallic-conductivity (MMC) 傳導機制，而高電阻狀態則遵循著 variable-range-hopping (VRH) 傳導機制，而且根據計算可以得到高電阻狀態之躍遷距離大約為十五Å。

綜觀以上三種材料的電性表現，氧化鎳以及氧化鈦材料由於界面之電荷效應的影響在電子特性上並沒有比較傑出的表現，然而由於塊材特性的氧化鎢材料擁有包括單次儲存(OTP)、多次儲存(MTP)、多層單元(MLC)儲存記憶體應用、雙極式操作以及單極式操作等優越特性，在 RRAM 領域有著較高的商業應用潛力。

Electric Characteristics and Application of (Nickel, Titanium and Tungsten) Oxides on Resistive Random Access Memory (RRAM)

Student : Ming-Daou Lee Advisor : Yeong-Der Yao

Department of Materials Science and Engineering
National Chiao Tung University

ABSTRACT

Due to the fact that traditional nonvolatile memory (Flash memory) with polycrystalline floating-gate structure will face the physical limitation below 20nm technology node, some emerging non-volatile memories such as magnetic random access memory (MRAM), phase change random access memory (PCRAM), and resistive random access memory (RRAM) are widely investigated. Since the advantages of RRAM include CMOS fully compatibility, high speed operation, good reliability, and high capacity, RRAM exhibits high potential in commercial applications for the next generation. The RRAM study is thus the main theme of this thesis.

Although there are several materials successfully revealing resistance bistability under a certain electrical operation, it's a pity that their CMOS compatibility is limited. Recently, metallic oxides by nickel (Ni), titanium (Ti), and tungsten (W) are reported to present good RRAM performance. Meanwhile, in the CMOS integration, nickel silicide (NiSi) is used in the middle-end-of-line (MEOL) process for reducing the contact resistance of both N- and P-MOS. Titanium nitride (TiN) is utilized respectively for back-end-of-line (BEOL) and MEOL processes to increase the metal adhesion and diffusion barrier capability. Tungsten (W) is widely accepted in the contact plug fabrication and it is the main material for the interconnection between CMOS device and BEOL circuit. Accordingly, RRAM materials with nickel oxide (NiO_x), titanium oxide (TiO_x), and tungsten oxide (WO_x) are also the CMOS fully compatible materials. In this thesis, we discuss the RRAM characteristics of all these three materials in details, including the electrical performance, the switching model, and the applications.

In NiO_x-based RRAM study, bipolar resistance switching behavior in polycrystalline thin film shows obvious thin film contribution and oxygen content effects on on/off ratio; that is, the higher oxygen content sample exhibits higher on/off ratio. Also, its conduction mechanism entirely follows the Schottky emission, and the on/off ratio is strongly barrier height dependent. According to Schottky emission simulation, NiO_x-based RRAM thin film with low oxygen content presents higher

dielectric constant. The result could explain why NiO_x-based RRAM thin film with low oxygen content needs higher energy to countervail the inner opposite electric field in the resistive switching process.

In TiO_x-based RRAM study, similar to the previous NiO_x-based system, TiO_x-based RRAM also shows bipolar resistance switching behavior. It is clear that the interfacial characteristics between TiO_x-based thin film and electrode dominates the electrical performance, while the thickness effect of TiO_x thin film on resistance switching properties is relatively minor. Again, similar to NiO_x-based system, the transportation follows the Schottky emission and the on/off ratio is found to be strongly barrier height dependent. In addition, the designed experiment, TiO_x / SiO_2 hybrid system, indicates the importance of interfacial contribution, and the data retention is further found to be improved by this hybrid system.

In WO_x-based RRAM study, we found this system has high potential for several applications, such as the memory device with one-time-programming (OTP) and multi-times-programming (MTP) functionality. For MTP application, resistive state of WO_x-based system can be switched reversibly by either bipolar or unipolar operation with the cycle endurance of exceeding 1000. On the other hand, this RRAM system is suitable for the multi-level-cell (MLC) application, too, due to its sufficient on/off ratio higher than 1000X. The highly scalable ability of this system is also discussed in this thesis. Meanwhile, a reliable characteristics is also demonstrated: high thermal stability of over 1000 hours at 250℃.

With the mathematical fitting of WO_x-based RRAM system, the electron conduction of high resistance state and low resistance state respectively follow the variable-range-hopping (VRH) transportation and minimum-metallic-conductivity (MMC). According to the fitting results, the hopping distance of high resistance state is found to be around 15Å.

NiO_x, TiO_x, and WO_x materials, which are all CMOS fully compatible without contamination risk, are summarized here for RRAM applications. For the overall comparison of RRAM functionality, interfacial contribution (NiO_x or TiO_x) cannot provide better characteristics than bulk contribution (WO_x) because the electron charging affects at interface to worsen the electrical performance of such kind of RRAM system. And the system with bulk contribution in turn could provide high potential for several commercial applications on electron devices, such as OPT, MTP, MLC, and unipolar operation as well.

誌　　謝

首先要感謝指導老師姚永德教授這些年來的栽培，讓學生學習到很多做人以及做事的方法，在學期間不管是學業或者生活方面老師總是能夠適時給予指導以及幫助，在學業方面老師讓學生在面對問題的時候能夠正面思考以解決問題，而在待人處事方面老師更是學生的榜樣，凡事嚴以律己寬以待人，讓學生了解待人圓融的重要。

再來要感謝盧志權老師在工研院時的教導，讓學生在就學期間可以接觸許多製程以及分析儀器，從廠商的聯繫到機台的組裝都能夠讓學生親自參與，在這段期間讓學生學到相當多的專業技能，從軟體的機台設計到硬體的儀器組裝學生都有參與，而這些技能也在學生之後的就業上也幫了很大的忙。

之後要感謝何家驊博士的指導與提攜，讓學生瞭解半導體界的相關知識，不管是邏輯或是記憶體方面都讓學生受益良多，而在就業方面何博也讓學生明白人和的重要性，凡事以和為貴這樣公司所交代的事才能進行的順利，而在帶人方面也要善待下屬才能夠完全發揮團隊合作的功能。

這裡也要感謝劉瑞琛協理、謝光宇處長以及楊富量主任的栽培，感謝瀛文、藍青、泰彥跟維志在工研院時期的幫忙，也感謝所有共事過的同事夥伴，在這一路上的照顧以及扶持。

最後要感謝老婆育芬這些年默默付出的辛勞，為這個家盡心盡力讓我在工作以及學業上無後顧之憂。

目　　　錄

中文摘要	……	i
英文摘要	……	iii
誌謝	……	v
目錄	……	vi
表目錄	……	viii
圖目錄	……	ix
一、	Introduction……	1
1.1	Floating gate Flash……	3
1.1.1	NOR Flash……	4
1.1.2	NAND Flash……	5
1.2	Magnetic Random Access Memory (MRAM)……	6
1.3	Phase Change Random Access Memory (PCRAM)……	7
1.4	Resistance Random Access Memory (RRAM)……	9
1.4.1	The history of RRAM development……	10
1.4.2	Metal-Oxide RRAM……	13
二、	Experiment……	14
2.1	BEOL Process flow……	14
2.1.1	Deposition……	15
2.1.2	Lithography……	17
2.1.3	Etching……	18
2.1.4	Chemical Mechanical Polishing (CMP)……	19
2.2	Layout……	20
2.3	Analysis……	21
2.3.1.1	Cycle Endurance Measurement…………	22
2.3.1.2	Thermal Stability Measurement…………	22
2.3.1.3	Stress Test…………	23
2.3.1.4	Data retention Measurement	24
2.3.2.1	XPS Analysis	25
2.3.2.2	TEM Analysis	26
2.3.2.3	PPMS Measurement	27
2.3.1	Electrical analysis……	22
2.3.2	Material analysis……	25
三、	Principle……	28
3.1	Basic resistance switching characteristics and nomenclature…………	28
3.1.1	Bipolar, unipolar, nonpolar operation……	30
3.1.2	Basic resistance switching nomenclature…………………	32
3.2	Electron transportation mechanism ……	33
3.2.1	The metallic transportation mechanism ……	33
3.2.2	The Schottky emission ……	34
3.2.3	The Poole-Frenkel emission ……	35
3.2.4	The electron hopping transportation mechanism ……	37
3.2.5	The space-charge-limited-current (SCLC) ……	38
3.2.6	The trap-assisted-tunneling (TAT) ……	40
3.3	Resistance switching mechanism ……	42
3.3.1	The conducting filament characteristics ……	42
3.3.2	The oxygen vacancy phenomenon ……	44

3.4 Resistance switching model 45
3.4.1 The “Rupture Ball” model 46
3.4.2 The stochastic model 47
3.4.3 The thermal dissolution model 48
3.4.4 The two-variable-resistor model 51
3.4.5 The compact model 52
3.4.6 The filament anodization model 55
3.4.7 The numerical model 55
3.5 The key physical parameters influence RRAM performance 58
3.5.1 Thickness 58
3.5.2 Cell size 59
3.5.3 Electrode 60
3.5.4 Doping effect 61
3.5.5 Electric field 61
3.5.6 Density of oxygen vacancy 63
四、 Results.. 64
4.1 Outline of results.. 64
4.2 NiO_x based RRAM.. 65
4.3 TiO_x based RRAM.. 73
4.4 WO_x based RRAM.. 79
4.4.1 One-time-programming (OTP) RRAM.. 82
4.4.2 Bipolar multi-times-programming (MTP) RRAM........................ 87
4.4.3 Unipolar multi-times-programming (MTP) RRAM.................... 93
4.4.4 Scaling effect.. 100
4.5 Metal-oxide RRAM organization 103
五、 Summary.. 104
Reference.. 105
Publication List.. 114

表 目 錄

Table 1-1 Non-volatile memories comparison…………………………………… 1
Table 1-2 Five system Resistive Random Access Memory comparison……… 2

圖 目 錄

Figure 1-1 Floating gate structure Flash sketch 3
Figure 1-2 Programmed and Erased states of Flash 4
Figure 1-3 (a) The reading electrical character of Flash
(b) The electrical symbol of Flash device 4
Figure 1-4 NOR type Flash device circuit 5
Figure 1-5 NOR Flash (a) write process by channel hot electron injection.
(b) erase process by F/N tunneling 5
Figure 1-6 NAND type Flash device circuit 6
Figure 1-7 NAND Flash (a) write process
(b) erase process by F/N tunneling 6
Figure 1-8 The magneto resistance curve 7
Figure 1-9 The MRAM structure sketch 7
Figure 1-10 The sketch of PCRAM 8
Figure 1-11 The working mechanism of PCRAM 8
Figure 1-12 The sketch of RRAM 9
Figure 1-13 The electrical character of bipolar method RRAM 9
Figure 1-14 The electrical character of unipolar method RRAM 10
Figure 1-15 The early electric characteristics in niobium oxide film.............. 11
Figure 1-16 The cycle endurance data of CMR-based RRAM.................... 11
Figure 1-17 The thermal stability test of unipolar operation tungsten oxide film… 12
Figure 1-18 The elements (red marked) that their metal-oxide were found to exhibit resistance switching characteristics by bipolar (solid line) and unipolar operation. The metal oxide with dash line can be switched by both bipolar and unipolar operation.................................. 13
Figure 2-1 The sketch of semiconductor process 14
Figure 2-2 The BEOL process flow and the sketch of BEOL profile 14
Figure 2-3 The sketch of physics vapor deposition (PVD) system 15
Figure 2-4 The sketch of chemical vapor deposition (CVD) process 16
Figure 2-5 The sketch of IBD system... 17
Figure 2-6 The sketch of lithography process 18
Figure 2-7 The anisotropic and isotropic etching process 19
Figure 2-8 The sketch of dry etching process 19
Figure 2-9 The sketch of chemical mechanical polishing (CMP) process 20
Figure 2-10 The top-view and cross-section of nickel oxide and titanium oxide RRAM structure 20
Figure 2-11 The top-view and cross-section of tungsten oxide RRAM structure 21
Figure 2-12 The 2 bits/cell cycle endurance test of RRAM.......................... 22
Figure 2-13 The typical thermal stability test 23
Figure 2-14 The typical stress test of RRAM 23
Figure 2-15 The data retention test of 2bits/cell RRAM device 24
Figure 2-16 The typical read disturb test of RRAM device 25
Figure 2-17 The sketch of X-ray photoelectron spectroscopy (XPS) 26
Figure 2-18 The sketch of transmission electron microscopy (TEM) 27
Figure 3-1 The typical dc sweep bipolar operation characteristics................. 29
Figure 3-2 The bipolar operation characteristics by applied pulse voltage......... 30
Figure 3-3 The typical unipolar and nonpolar operation characteristics........... 31
Figure 3-4 The unipolar operation characteristics by applied pulse voltage...... 31

Figure 3-5 The resistance switching characteristics of unipolar RRAM………… 32
Figure 3-6 The multiple-level-cell (MLC) of 2bits/cell RRAM………………… 33
Figure 3-7 The temperature dependence relationship of metal electrical characteristics……………………………………………………… 34
Figure 3-8 The energy band diagram of a metal-semiconductor contact………… 34
Figure 3-9 The typical electrical curve of Schottky emission…………………… 35
Figure 3-10 The energy band diagram of Poole-Frenkel emission……………… 36
Figure 3-11 The typical electrical curve of Poole-Frenkel emission……………… 36
Figure 3-12 The band diagram of variable range hopping………………………… 37
Figure 3-13 The electrical curve of Mott variable range hopping (VRH)………… 38
Figure 3-14 The band diagram of space-charge-limited-current………………… 39
Figure 3-15 The electrical curve of space-charge-limited-current (SCLC)……… 39
Figure 3-16 The band diagram of trap assisted tunneling (TAT)………………… 40
Figure 3-17 The electrical curve of trap assisted tunneling (TAT)……………… 41
Figure 3-18 The electrical curve of trap assisted tunneling (TAT) of RRAM…… 41
Figure 3-19 Sketch of (a) RESET process (from LRS to HRS) and (b) SET process (from HRS to LRS)……………………………… 42
Figure 3-20 Sequence of EBIC image and I-V characteristic (a) Initial state (b) Switch to LRS (c) Back to HRS (d) sweep to LRS………………… 43
Figure 3-21 The conducting atom force microscopy (CAFM) of ON and OFF states………………………………………………………… 44
Figure 3-22 Schematic illustration of conduction transport in (a) LRS (b) HRS… 45
Figure 3-23 Schematic diagram of dielectric status of RRAM at (a) fresh (b) after "forming" process, and (c) after "reset" process (d) after "set" process, and (e) after "over reset" process, respectively…………… 46
Figure 3-24 Measured and calculated relationships between the set/reset voltage and (a) the sweep rate or (b) the set/reset transition times…………… 47
Figure 3-25 Calculated I-V curves for set and reset states. The dashed lines connect transition point at equal transition times on two curves…… 48
Figure 3-26 (a) The reset switching I-V curve and the temperature dependence relationship with resistance (inner) (b) Temperature has been evaluated from I-V curve…………………………………………… 49
Figure 3-27 Measured and calculated I-V curve during reset process…………… 50
Figure 3-28 Simulation results for thermal dissolution of the CF. The left four images show the four bias points A-D in figure 3-27 and the right image shows the temperature profile of A-D………………………… 50
Figure 3-29 Schematics to explain the resistive switching in the Al/TiO_x/Al structure considering the variation of the filled-trap region (R_{on}) of TiO_x by injected carrier…………………………………………… 51
Figure 3-30 Calculated I-V curve of the Al/TiO_x/Al device and the measured data……………………………………………………………… 52
Figure 3-31 (a) the structure of RRAM and the filament is in the RS layer. (b) The equivalent circuit of RRAM device. (c) The flowchart of the model……………………………………………………………… 53
Figure 3-32 The simulated I-V curves of bipolar RRAM by compact model…… 54
Figure 3-33 The simulated I-V curves of unipolar RRAM by compact model…… 54
Figure 3-34 A schematic view of the condition of the filaments in LRS and HRS 55
Figure 3-35 The I-V curve of multiple reset process……………………………… 56
Figure 3-36 The schematic for multiple states. (a) Full set state. (b) Intermediate state with small metallic CF. (c) dispersed CF (d) Full reset state…… 56

Figure 3-37	(a) The measured E_{AC} as function of resistance. (b) The calculated CF diameter as function of resistance…………………………………	57
Figure 3-38	The temperature dependence relationship of (a) LRS (b) HRS………	58
Figure 3-39	The "Forming" and "set" voltage dependence on TiO_2 thickness of $Pt/TiO_2/Pt$ RRAM……………………………………………………	59
Figure 3-40	(a) The relationship between device area and resistance state. (b) The relationship between shrinking ratio and SET voltage………………	59
Figure 3-41	The resistance characteristics of different metal and metal oxide cap layers in $Pt/HfO_2/TiN$ system………………………………………	60
Figure 3-42	The resistance characteristics of different metal and metal oxide cap layers in $TiN/HfO_2/TiN$ system……………………………………	60
Figure 3-43	Distributions of the HRS in (a) NiO and (b) Ti:NiO as a function of the pulse width in the reset process……………………………………	61
Figure 3-44	Electric enhancement structure (left) and the electric field distribution for 20nm (up-right) and 100nm (down-right) RRAM devices………	62
Figure 3-45	Forming voltage verse dielectric constant of RRAM…………………	62
Figure 3-46	The unipolar operation character with different oxidation time………	63
Figure 4-1	HRTEM image of polycrystalline NiO_x film ………………	65
Figure 4-2	The enlarged part of polycrystalline nickel oxide film (Inset shows the SAED image) ……………	66
Figure 4-3	The resistive switching character of different thickness NiO_x film …	67
Figure 4-4	The relationship between sample thickness and the on/off ratio……	67
Figure 4-5	The endurance test of different thickness NiO_x films…………	68
Figure 4-6	The on/off ratio of different thickness NiO_x films in the endurance measurement ………………………………………………	68
Figure 4-7	The resistive switching character of nickel oxide film with different oxygen flow ratio ………………………………………………………	69
Figure 4-8	The relation between on/off ratio and oxygen flow ratio …………	69
Figure 4-9	Schottky emission approximation of nickel oxide film ……………	70
Figure 4-10	Dielectric constant and the barrier high change with various oxygen flow ratio ………………………………………………………………	71
Figure 4-11	The influence of dielectric constant in the operation process ………	71
Figure 4-12	The temperature dependent electric character of NiO_x film …………	72
Figure 4-13	Cross-section view of TiO_x-based RRAM……………………………	73
Figure 4-14	The bipolar resistive switching characteristics of TiO_x film	73
Figure 4-15	The resistive switching phenomenon from high resistance state to low resistance state………………………………………………………	74
Figure 4-16	Voltage dependent on/off ratio ……………………………………	74
Figure 4-17	The resistive switching character of TiO_x film at various thicknesses	75
Figure 4-18	The thickness relationship with transition voltage and the on/off ratio…………………………………………………………………	75
Figure 4-19	The curving fitting of I-V data for TiO_x at various thickness ………	76
Figure 4-20	The temperature dependent electric characteristics of TiO_x film……	76
Figure 4-21	Data retention of titanium oxide RRAM with/without SiO_2 hybrid system …………………………………………………………………	77
Figure 4-22	Cycle endurance test of TiO_x-based RRAM…………………………	77
Figure 4-23	Cycle endurance test of TiO_x-based RRAM with SiO_2 hybrid system	78
Figure 4-24	Read disturb test of TiO_x-based RRAM with SiO_2 hybrid system …	78
Figure 4-25	The WO_x RRAM process flow ……………………………………	79
Figure 4-26	The TEM image of WO_x film ……………………………………	80

Figure 4-27 The enlarge part of TEM 80
Figure 4-28 The XPS data of WO_x for O and W analysis. (a)~(d) are peak profile of at surface, depth of 15 Å, depth of 70 Å, and depth of 140Å 81
Figure 4-29 Vertical variation of W-ion that are analysis by deconvolution of the XPS signal 81
Figure 4-30 The vertical distribution of oxygen content 82
Figure 4-31 The resistance state verse the number of pulse shots.. 83
Figure 4-32 The resistance switching by 70 ns and 100 ns pulse width.. 83
Figure 4-33 The one shot OTP operation character.. 84
Figure 4-34 The influence of the pulse width with applied voltage about 1.5V... 85
Figure 4-35 The 10mV read disturb of 2 bits/cell WO_x film.. 85
Figure 4-36 The data retention (left) and thermal stability (right) of 2bits/cell WO_x film.. 86
Figure 4-37 The electric character of four resistance states.. 86
Figure 4-38 Temperature effect on “00” state. The dashed lines is optimized fitting by power law.. 86
Figure 4-39 The resistance switching character by 80ns pulse bipolar operation... 87
Figure 4-40 Above thousand cycle operation in the cycle endurance test 88
Figure 4-41 The thermal stability test at 150 (left) and 250℃ (right) 89
Figure 4-42 The stress test for low resistance state 89
Figure 4-43 The resistive variation by applied bias with different pulse width ... 90
Figure 4-44 The relation between pulse width and threshold voltage 90
Figure 4-45 The endurance test of 2bits/cell bipolar operation memory............ 91
Figure 4-46 The I-V curve of LRS and HRS 91
Figure 4-47 The temperature dependent electrical character and VRH fitting curve (inner) for high resistance state.. 92
Figure 4-48 The temperature dependent electrical character for low resistance state 92
Figure 4-49 The temperature dependent electrical character of WO_x film 93
Figure 4-50 The pulse width influence of resistance state 94
Figure 4-51 The WO_x thickness relationship with different oxidation time 94
Figure 4-52 The unipolar operation character with different oxidation time...... 95
Figure 4-53 The resistance change by using negative voltage with varies pulse width.. 95
Figure 4-54 The cycle endurance test of unipolar operation.. 96
Figure 4-55 The thermal stability of unipolar operation at 150 and 250℃ 97
Figure 4-56 The stress influence of unipolar RRAM 97
Figure 4-57 The high stress test of high resistance state 98
Figure 4-58 The electric character of LRS and HRS.. 99
Figure 4-59 The VRH fitting curve of unipolar operation RRAM 99
Figure 4-60 The hopping distance varies in the cycle endurance test.............. 100
Figure 4-61 (a) The sketch of scaling reducing profile (b) TEM image of scaling reducing experiment (c) The enlarge part of WO_x film 101
Figure 4-62 The threshold voltage varies with different reducing scale 101
Figure 4-63 The relationship between shrinking ratio and set voltage 101
Figure 4-64 The shrinking ratio influence with hopping distance and density of state 102
Figure 4-65 The thermal stability with different shrinking ratio 102
Figure 4-66 The cycle endurance test with different shrinking ratio sample 103

Chapter 1: Introduction

Nonvolatile memory plays an important role in our lives. Almost all of the portable electric devices (such as cell phone, digital camera, walkman, USB Flash …etc.) need this memory for data storage or transfer. The traditional flash with floating gate structure has advantages in the electrical market with its high capacity and low price. By the end of 2010, the latest advanced technology of 25 nm node NAND flash with 64 Gbit was announced by Intel and Micron. However, with the technology shrinking below 25 nm node, the floating gate flash will meet the physical bottleneck: insufficient to identify the memory state. The development of new nonvolatile technology becomes urgent in recent years.

Table.1-1 compares the NAND Flash and novel nonvolatile memories. Three new nonvolatile memories: magnetic random access memory (MRAM), phase change random access memory (PCRAM), and resistive random access memory (RRAM), exhibit better performance than NAND flash. High program speed, low power consumption, and good endurance are the major advantages of these novel memories. Their good performance leads to high potential for the memory applications of the next generation.

For MRAM, there are several real products in recent years. According to the large cell size (10-45 F^2), the capacity of MRAM is only 4 Mbit and it is always used in special application such as aerospace industry. For PCRAM, the most popular emergence memory before 2010, lots of companies investigate the possibility for next generation memory, but high power consumption and pollution limited the production growth. Among them, RRAM with fully CMOS compactable exhibits suitable performance (smaller cell size, high program speed, low power consumption and better endurance) for next generation memory applications.

Table 1-1. Non-volatile memory comparison.

	NAND Flash	**MRAM**	**PCRAM**	**RRAM**
Cell size (F^2)	**4**	**6-45**	**6-16**	**2-10**
W/E time (ns)	**10µs/1ms**	**1-35**	**70/500**	**10-50**
W/E voltage (V)	**18**	**1-3**	**3**	**3**
Power consumption	**Low**	**High**	**High**	**Low**
Endurance	**10^5**	**10^{15}**	**10^9**	**10^6**
Scalable	**Yes (>1Xnm)**	**Yes (<20nm)**	**Yes (>20nm)**	**Yes (<10nm)**

For the past 70 years, numerous researches have been done in the resistive switching phenomenon. Several RRAM systems based on this resistive switching operation have been developed in recent years. These RRAM materials include colossal magneto-resistance (CMR) material[1-4], polymer[5-9] , conductive bridging RAM (CBRAM) [10-12], doped metal-oxide [13-19], metal-oxide[20-29], and so on. Table1-2 compares five RRAM systems. Due to the complex film stacked, CMR-base and polymer RRAM have no potential for production market. Recently, these two systems are only placed in the physics character study. CBRAM also faces the reliability problem because its low operation voltage and the thermal effect will interfere the memory states. The other doping-type RRAM of ternary $SrZrO_3$ (SZO) with low program speed and complex film stacked seems to be able to change the research direction to doping on binary metal-oxide.

Table 1-2. Comparison of five RRAM systems.

	CMR-base	**Polymer**	**CBRAM**	**Doping Metal-Oxide**	**Binary Metal-Oxide**
Material	$Pr_{0.7}Ca_{0.3}MnO_3$	P(VDF/TrFET) [5]	Ag in GeSe[10]	Nb-doped $SrZrO_3$[19] ...etc	WO_x[20], NiO[21], TiO_2[22]…etc
Retention	???	25C, 168hrs[6]	70C, 24 hrs[10]	125C, 1 month[19]	250C, 2000 hrs[20]
Endurance	1,000[1]	1,000[6]	1,000,000[10]	10,000,000 [19]	1,000,000[23]
W/E voltage (V)	2.5V / -2.5V[1]	15V 0.3ms/ 15V 0.5ms[5]	0.3V/-0.1V[10]	2V /-3V[19]	5V / -4V[20]
W/E time	50ns/ 10ns[1]	0.3ms/ 0.5ms[5]	N/A	500us[19]	80ns[20] (uni-polar:4V, 50ns,1us[24])
On/Off ratio	17[2]	10,000[7]	100,000[10]	100[19]	1,000[20]
Operation	Bipolar	Bipolar	Bipolar	Bipolar	Bi-polar Unipolar[24]
Fab. Compatible	No	No	No	No	Yes

In recently years, binary metal-oxide based RRAM becomes more and more popular with simple stacked film and better performance. Moreover, CMOS fully compatible materials (such as W, Ni, Cu and Ti) exhibit high potential for next generation nonvolatile memory.

In this chapter, we will show the overview of several non-volatile memories, including floating-gate flash, MRAM, PCRAM, and RRAM.

1.1 Floating Gate Flash

Flash, the first floating gate structure memory was published by Kahng and Sze[30] in 1967. Figure 1-1 shows the sketch of floating gate structure flash. The memory states can be identified by the charge storage status in floating gate (poly 1). Figure 1-2 shows the memory states of Flash device. For the programmed state ("0" state), the charge was stored in the floating gate region, and the floating gate without charge storage indicated the erased state ("1" state). For the electrical character reading, the source current between source and drain depends on the charge storage state. Figure 1-3 (a) shows the source current (I_{ds}) versus control gate bias (V_{cg}) of reading process. With an applied voltage in control gate, we can obtain the logic signal of this memory state. Moreover, figure 1-3 (b) shows the electrical symbol of flash device.

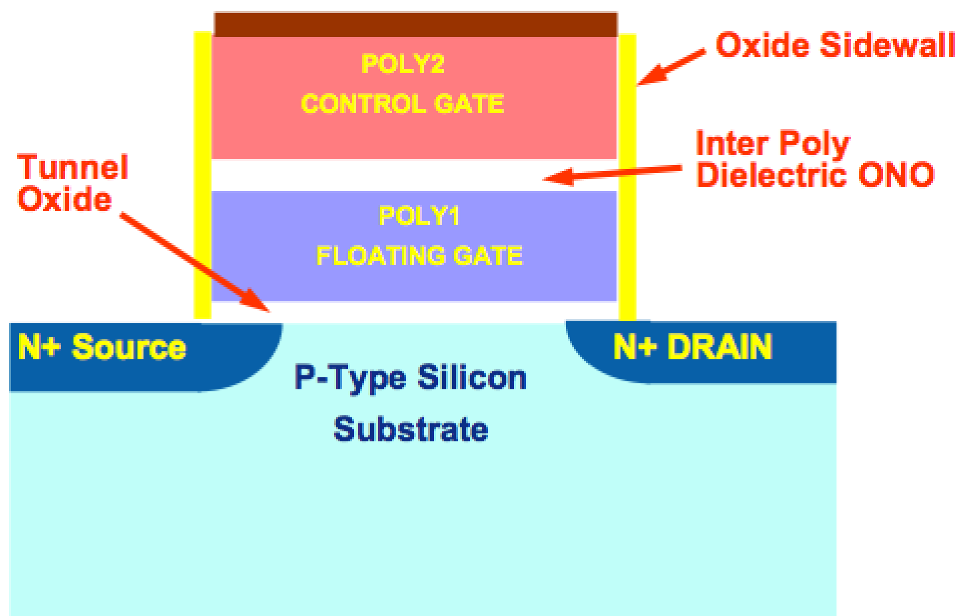

Figure 1-1. Floating gate structure flash sketch[1].

[1] http://www.linux-mag.com/id/7590/

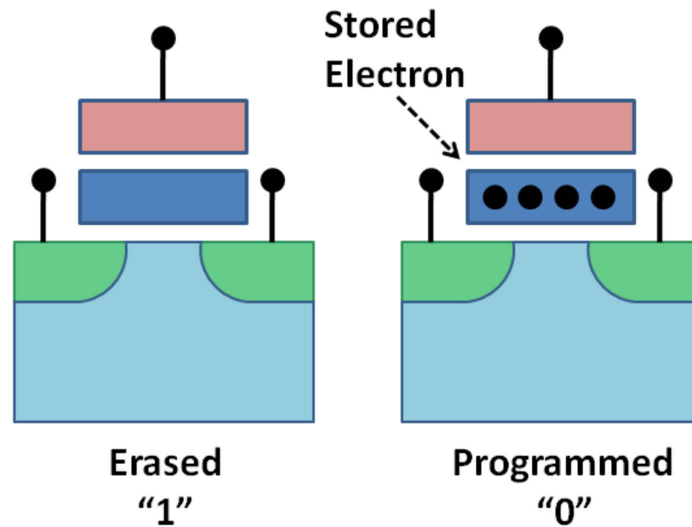

Figure 1-2. Programmed and Erased states of flash.

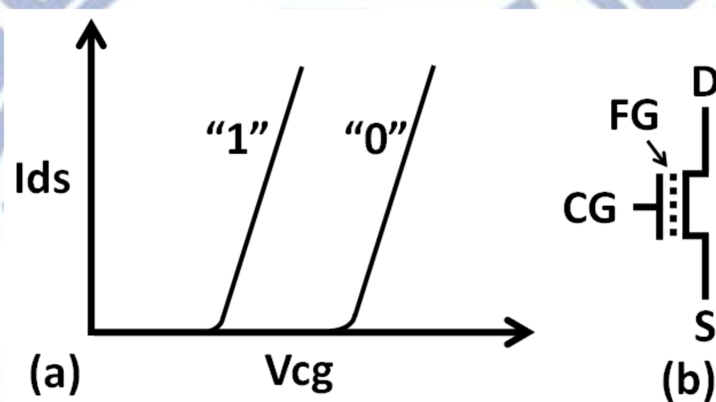

Figure 1-3. (a) The reading electrical character of flash. (b) The electrical symbol of flash device.

1.1.1 NOR Flash

The first NOR flash device circuit was designed by F. Masuoka[31] while working for Toshiba in 1985. Moreover, Intel Corporation saw the potential of the memory market and published the first NOR type flash chip in 1988. Recently, NOR flash was located at low capacity and high speed non-volatile memory application. Figure 1-4 shows the sketch of NOR flash device circuit. The random access function was defined by the applied bias on bit line (BL) and word line (WL). Moreover, the cell size was shrinked by means of the command drain site to increase the capacity. As figure 1-5 (a) shown, the channel hot electron injection mechanism was used for the writing process. With the applied perpendicular electric field by control gate (CG) and another applied electric field by source-drain voltage, the charge can be trapped from source-drain channel and stored in the floating gate to finish the writing process. On the other hand, the Fowler-Nordheim (FN) tunneling mechanism was used for the erasing process, which was shown in figure 1-5 (b). With the applied opposite electron field by CG and

another bias on source site, the charge can be pulled out from the floating gate to finish the erasing process.

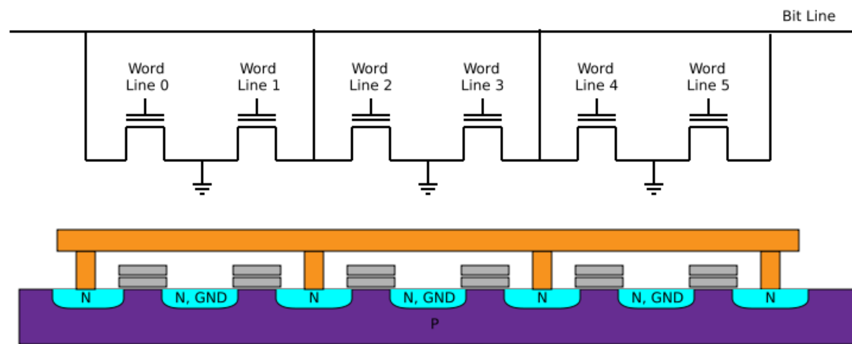

Figure 1-4. NOR type flash device circuit[2].

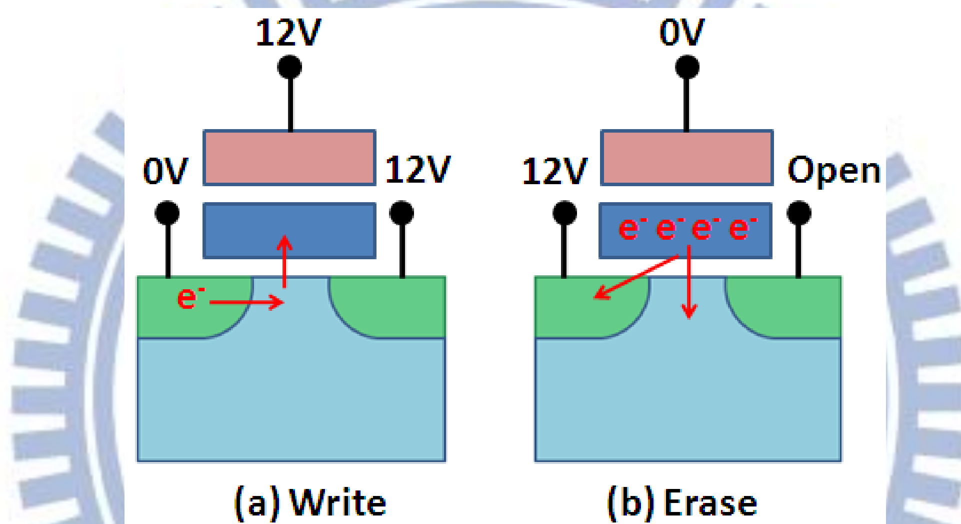

Figure 1-5. NOR flash (a) write process by channel hot electron injection. (b) erase process by F/N tunneling.

1.1.2 NAND Flash

The first NAND flash device circuit was also designed by F. Masuoka[32] in 1989. Recently, NAND flash was located at high capacity non-volatile memory application. Figure 1-6 shows the sketch of NAND flash device circuit. This circuit consists of an eight floating gate series structure and two necessary transistors at the end of this series. As figure 1-7 shows, the NAND flash used tunnel injection for writing and tunnel release for erasing. With applied bias at CG (~20 V) and zero bias for others (source, drain and substrate), the electrons can be injected to the floating gate from substrate to finish the writing process. On the other hand, by means of the zero bias at CG and applied bias for source, drain and substrate, the electrons can be tunnel released from floating gate to finish the erasing process.

[2] http://www.qdpma.com/Storage/SSD.html

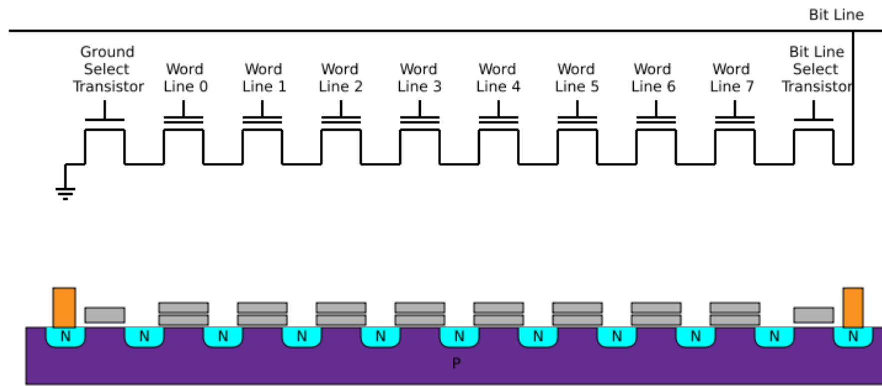

Figure 1-6. NAND type flash device circuit[3].

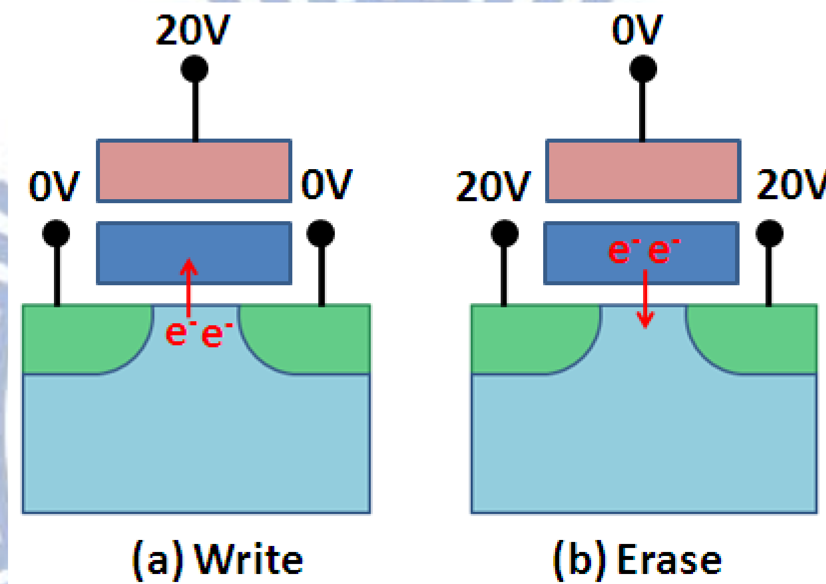

Figure 1-7. NAND flash (a) write process and (b) erase process by F/N tunneling.

1.2 Magnetic Random Access Memory (MRAM)

A. Fert and P. Grunberg are well-known for their discovery of the giant magneto resistance (GMR) in 1988[33]. The operation mechanism of MRAM was based on this magneto resistance. Recently, the greater magneto resistance (MR) ratio of ferromagnetic/isolation/ferromagnetic sandwich structure with tunnel magneto resistance (TMR) was used in the MRAM device. The first room temperature Fe/Al_2O_3/Fe TMR junction was published by T. Miyazaki in 1995[34]. With the different magnetization directions between these two Fe layers (parallel or anti-parallel), the resistance of this junction exhibits different resistance states. Figure 1-8 shows the typical TMR effect of Fe/Al_2O_3/Fe junction[34]. With the applied magnetic field changing, the resistance exhibits large MR ratio about 20 %. With this different resistance, we can define the memory states and use the applied magnetic field to

[3] http://www.qdpma.com/Storage/SSD.html

change the memory states. Figure 1-9 shows the sketch of MRAM structure. The bottom Fe layer is pin layer and the magnetization direction was fixed to one direction. The top Fe layer is free layer and the magnetization direction is changed by the magnetic field. However, this magnetic field was produced by two perpendicular currents. Finally, the memory access was controlled by the change of the magneto resistance.

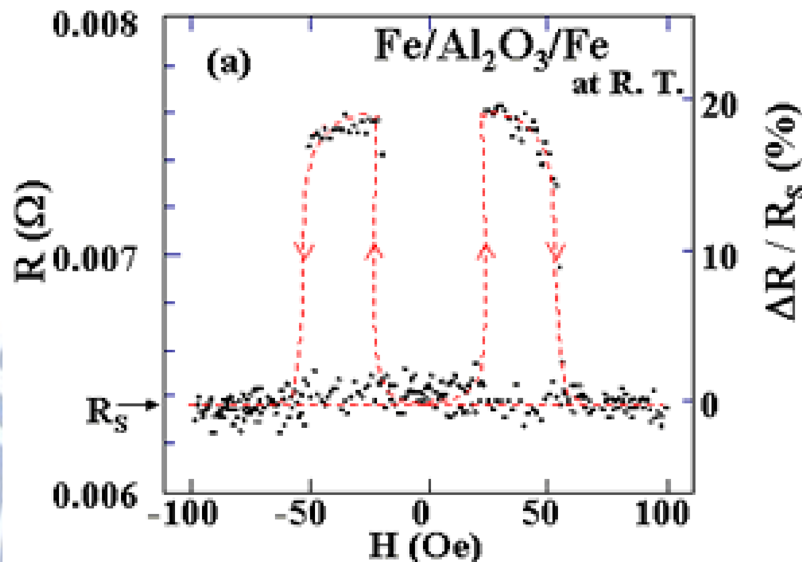

Figure 1-8. The magneto resistance curve.

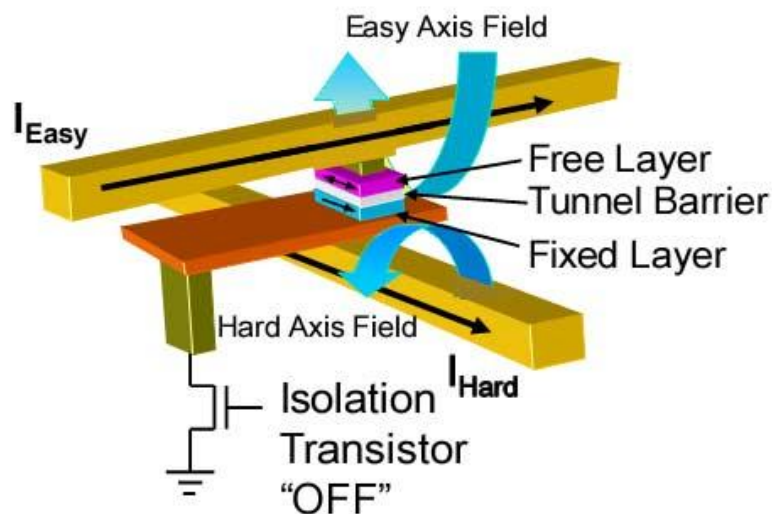

Figure 1-9. The MRAM structure sketch[4].

1.3 Phase Change Random Access Memory (PCRAM)

$Ge_2Sb_2Te_5$ (GST), the phase-change material is widely used on the rewritable optical media (such as CD-RW or DVD-RW) applications. The crystallinity of GST material can be distinguished as the different memory states by optical reflection or

[4] http://thefutureofthings.com/articles/36/mram-the-birth-of-the-super-memory.html

electrical resistance. For PCRAM, the resistance-identifying mechanism, the resistance of GST is dependent on the crystalline state. The crystalline, which presents low resistance state (LRS), indicates the memory state as “1” state, and the amorphous, which presents high resistance state (HRS), indicates as “0” state. As figure 1-10 shows, the GST material was placed between two metal layers and the crystalline state was defined by the pulse current. As figure 1-11 shows, the high-short pulse current provides power to make GST the amorphous state, and the low-long pulse current makes GST the crystallization state.

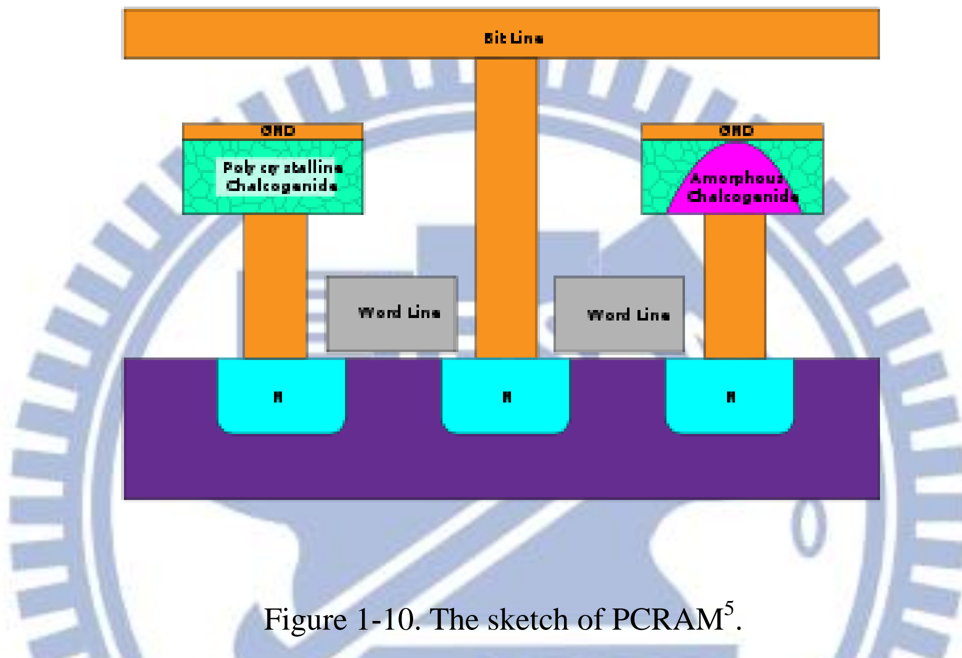

Figure 1-10. The sketch of PCRAM[5].

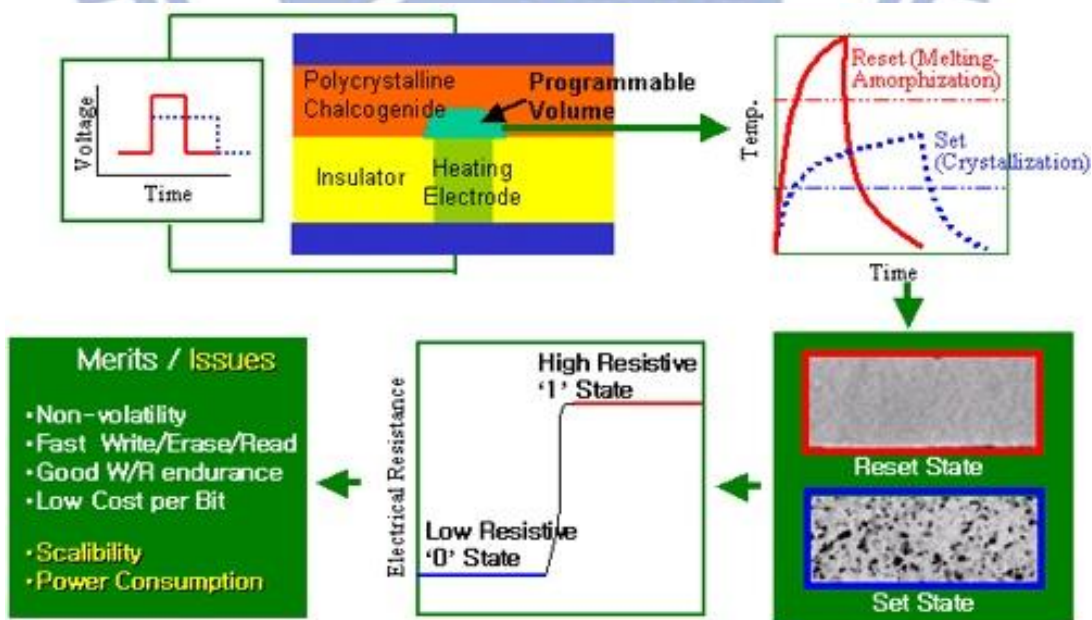

Figure 1-11. The working mechanism of PCRAM[6].

---

5 http://theelectronicfreak.blogspot.com/2010/06/future-memory-pcramphase-change-ram.html

1.4 Resistance Random Access Memory (RRAM)

RRAM, a new type of non-volatile memory component, is under the academic attention. While RRAM using material falls into many categories, the most eye-catching one is the metal oxide material. Due to the simpler compound and better performance, metal oxide based RRAM is more competitive than other materials. As shown in figure 1-12, the RRAM device structure is the same with PCRAM. Both are sandwiched between two metal layers, but the way of functioning is different.

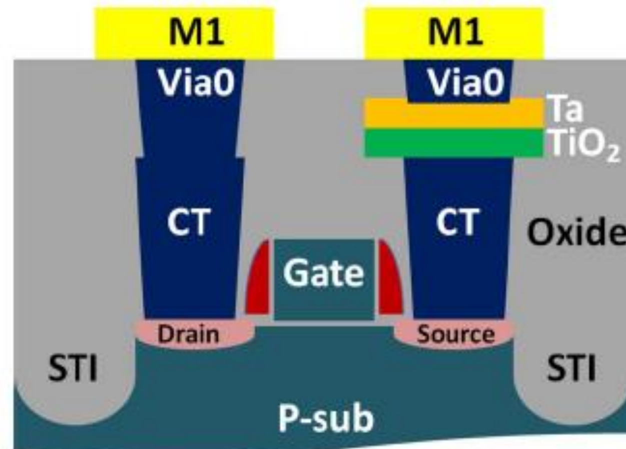

Figure 1-12. The sketch of TiO_2 RRAM.

The operational mechanism of RRAM is divided into bipolar and unipolar. For the bipolar method, the resistance state is dependent on the direction of applied voltage. As figure 1-13 shows, the resistance of memory device was switched from LRS to HRS with a positive applied voltage. Moreover, this resistance can also be switched back to LRS with a negative applied voltage. By using the polar of applied voltage, we can control the resistance state of this memory device.

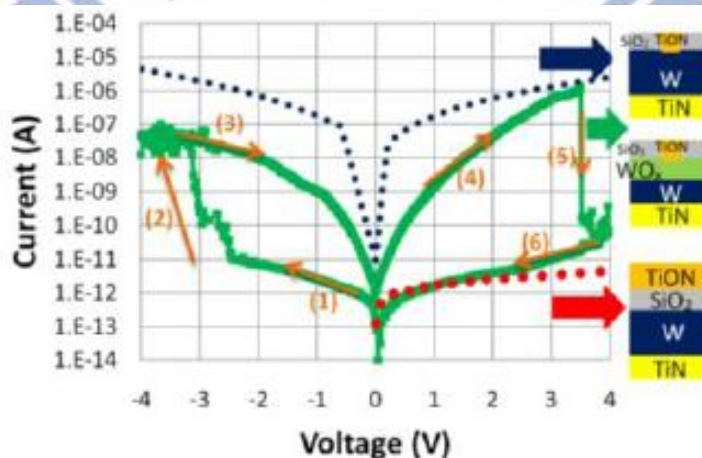

Figure 1-13. The electrical character of bipolar method RRAM[7].

---

[6] http://alfin2100.blogspot.com/2007/09/phase-change-memory-using-nanowires.html

[7] C.H.Ho et al, IEDM, 19.1, (2010)

As for the unipolar method, the resistance state is dependent on the waveform of applied voltage. As figure 1-14 shows, the resistance state is switched from LRS to HRS by means of a short applied pulse voltage. With the increase of wavelength, the resistance state is switched from HRS to LRS. This kind of resistance switching method controls the memory state with an applied waveform.

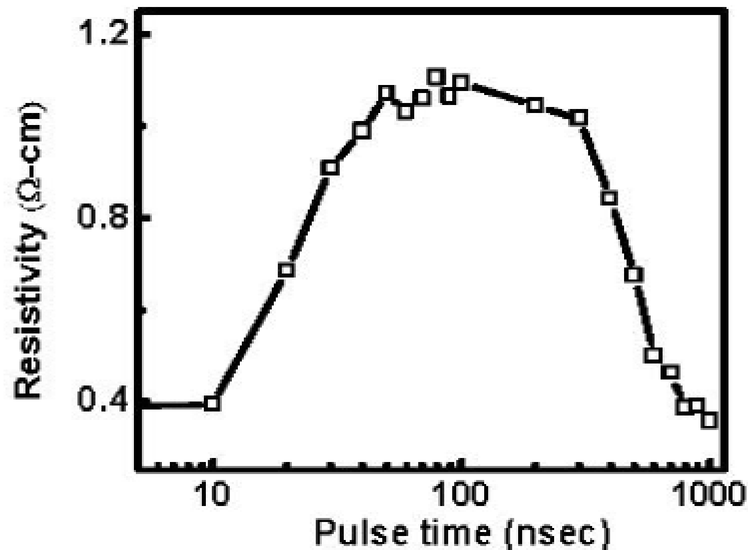

Figure 1-14. The electrical character of unipolar method RRAM.

However, the physical theory of RRAM switching mechanism is controversial today. Most theories that point to this mechanism have strong relationship with oxygen vacancy. The electrical characteristics exhibit the filament phenomenon while the electrons pass through these oxygen vacancies. Moreover, the electron transportation mechanism shows high relationship with the barrier. Despite the fact that the theoretical foundation of RRAM development is not very complete, RRAM has become a rising star in the non-volatile memory due to the high potential of researches in recent years.

1.4.1 The History of RRAM Development

According to the development of RRAM, the first research began in 1970s. During this period, Gibbon and Beadle[35] reported the resistance switching research of nickel oxide (NiO_x) material. In addition to the NiO_x, the research of resistance switching in niobium oxide (NbO_x) and titanium oxide (TiO_x) are reported by Hiatt and Hickmott[25] and Argall[22], respectively. In these studies, the performance of these resistance switching materials is not good enough for device applications. It can be attributed to the poor fabrication technology during that period. In 1970s, the research of resistance switching was focused on the characteristics description and the physics explanation. Most studies only showed the I-V curve of resistance switching characteristics and described the physics phenomenon. Figure 1-15 shows the I-V curve of NbO_x film[25]. Like other researches in this period, it didn't show the reliability, such as cycle

endurance, data retention, and thermal stability. People did not think it had any value in device applications during that period. Topped with poor fabrication technology, the research of the resistance switching was not the eye-catching technology in 1970s.

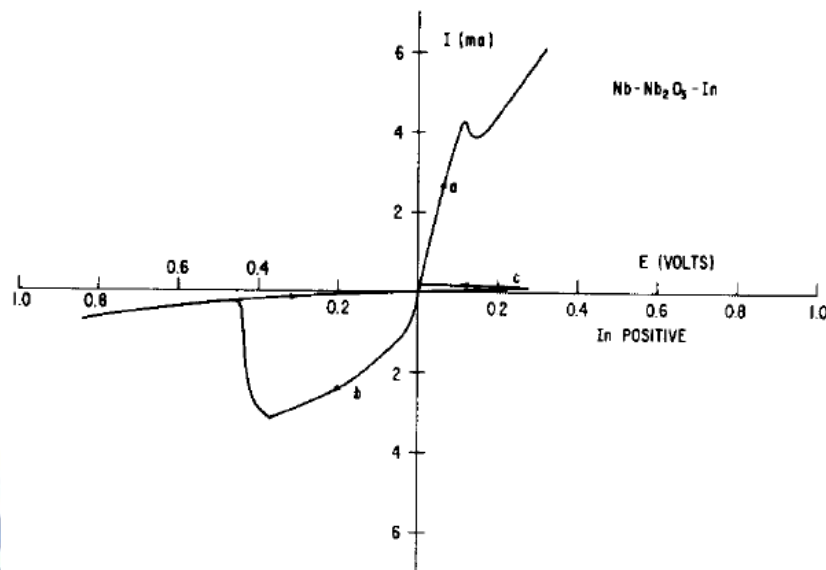

Figure 1-15. The early electric characteristics in NbO_x film.

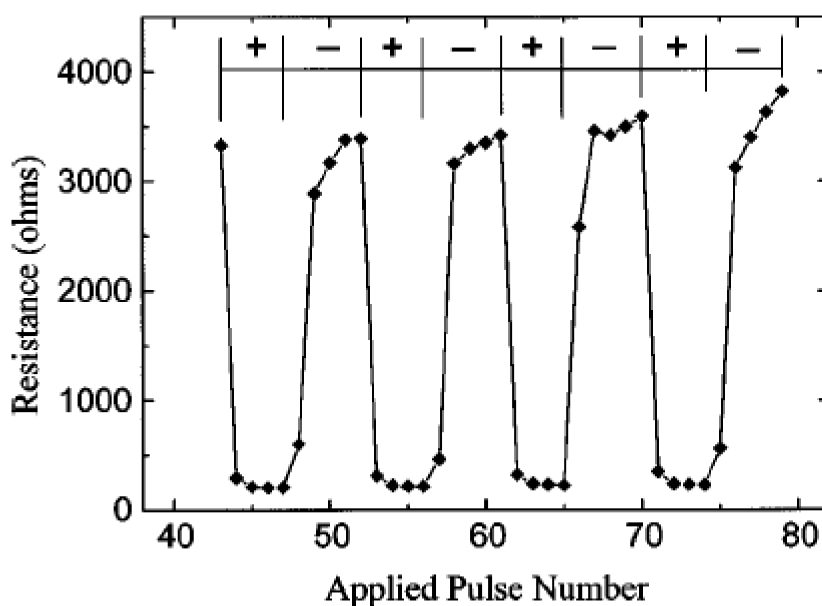

Figure 1-16. The cycle endurance data of CMR-based RRAM.

In 2000, Liu[2] reported his resistance switching research with better performance. In his research, the CMR material of $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) was used for the resistance switching material, and it showed several times of resistance switching phenomenon. Figure 1-16 shows the cycle endurance data of PCMO material. Moreover, the good reliability performance of high on/off ratio (1700 %) and fast switching time (100 ns) causes an attention in resistance switching research. First, the high on/off ratio has potential for multi-level-cell (MLC) application. It means this material can be used

for high density memory applications. Second, the fast switching time has potential for high speed programming applications. According to these results, the PCMO material shows high potential in non-volatile memory (NVM) application. After the publication of electric-pulse-induced reversible resistance NVM by Liu in 2000, many researchers started their study on resistance switching research, and the resistance switching has become the eye-catching technology of NVM application in recent years.

However, the CMR material is not so in industry fabrication because it is not the full CMOS compatible material. Moreover, this quaternary compound has more uncertainties than others in the manufacturing process. So, the binary oxide materials have attracted considerable interest in RRAM research. In 2007, the first tungsten oxide (WO_x) based RRAM was reported by Ho et al.[20]. In their study, the CMOS fully compatible tungsten oxide showed good reliability performance, such as good data retention, better cycle endurance, good thermal stability, high on/off ratio, fast switching time, and so on. These results indicated this material has high potential for NVM applications. In their extended research, this material also showed the unipolar operation resistance switching characteristics and good thermal stability. This unipolar operation characteristic also indicated the higher capacity density in memory applications. Figure 1-17 shows the thermal stability data of tungsten oxide film at 150 ℃. In this figure, it is clear to see that both resistance states keep their memory state for ten years at temperature about 150 ℃. The result indicates that this WO_x based RRAM can achieve the target of data retention in NVM applications.

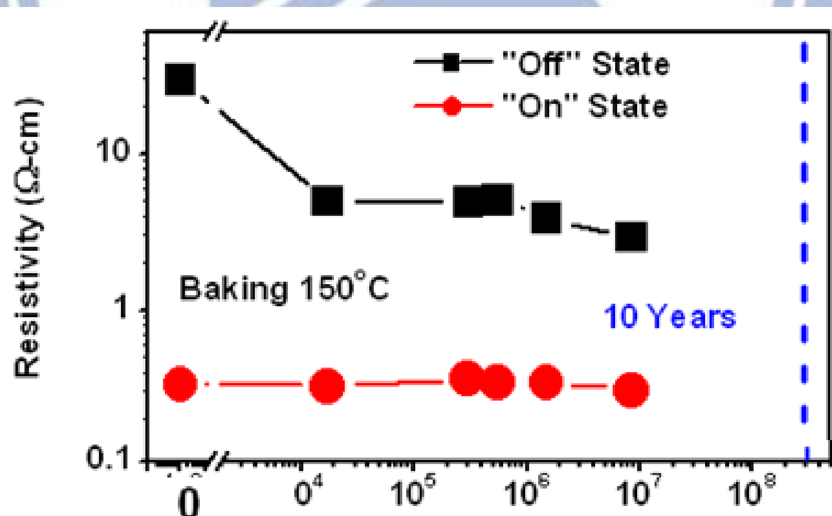

Figure 1-17. The thermal stability test of unipolar operation WO_x film.

Even though the RRAM performance shows great improvement in recent years, it still can't replace the flash memory. The bottleneck of RRAM application is the excessive switching current and the unclear resistance switching mechanism. However, there is one thing for sure that the binary oxide is the most possible candidate for RRAM applications.

1.4.2 Metal-Oxide RRAM

According to table 1-2, even though there are five types of RRAM materials, the suitable material of RRAM applications is the metal-oxide based RRAM. Due to its simple fabrication process, better performance, multiple application, and full CMOS compatibility, many studies have been involved in the metal-oxide material research in recent years. Moreover, binary metal oxides show potential in the RRAM applications. Those binary metal oxides include TiO_x, NiO_x, CuO_x, et al., which is shown in figure 1-18. In this figure, the metal oxides of elements with both solid and dash marked shows the bipolar resistance switching characteristics. Moreover, the metal oxides of elements with dash marked show both bipolar and unipolar resistance switching characteristics.

Figure 1-18. The elements (red marked) that their metal-oxide were found to exhibit resistance switching characteristics. The metal oxides with solid line can be switched by bipolar operation. The metal oxide with dash line can be switched by both bipolar and unipolar operation.

In non-volatile memory application, the unipolar operation RRAM shows higher capacity than bipolar operation due to its one-diode-one-resistor (1D1R) circuit. Moreover, the full CMOS compatible process also needs to be considered in device application. According to these factors, TiO_x, NiO_x, and WO_x show their promising RRAM application. Many companies (MXIC, Samsung etc.) focus their researches on these materials and file the patent to claim their inventions in RRAM for the next generation non-volatile memory applications.

Chapter 2 : Experiments

Semiconductor fabrication can be divided into two processes, one is the front-end-of-line (FEOL), and the other is back-end-of-line (BEOL). The process prior to contact process belongs to FEOL, and the process posterior to tungsten (W) deposition belong to BEOL. The sketch of semiconductor profile is shown in figure 2-1. Our memory cell process belongs to BEOL because the memory cell is located on the W plug. For the BEOL process, we introduce the main processes which are divided as deposition, lithography, etching, and chemical mechanical polishing (CMP).

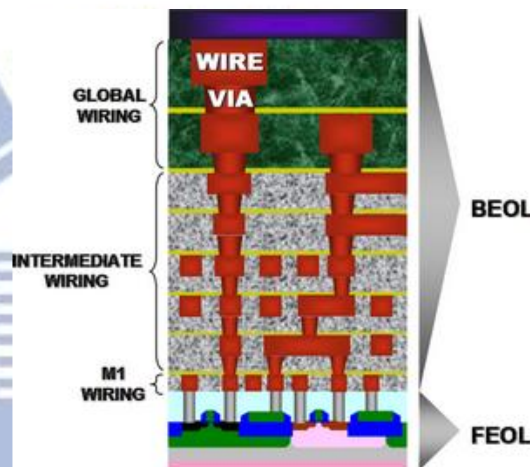

Figure 2-1. The sketch of semiconductor process[8].

2.1 BEOL Process Flow

There are many kinds of the processes for BEOL technology, including advance dual damascene for copper (Cu) interconnector, via first, trend first, and double exposure for 20 nm technology node. In this chapter, we introduce the traditional process for aluminum (Al) interconnector.

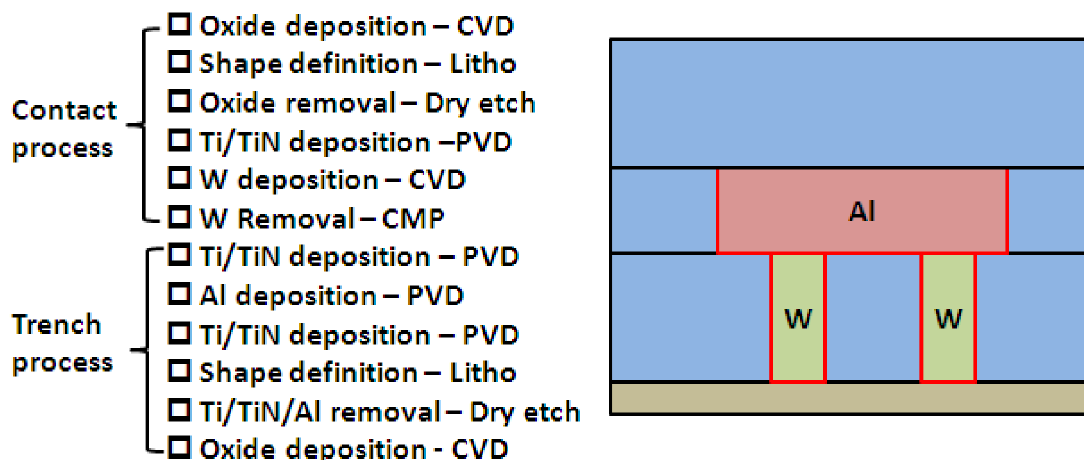

Figure 2-2. The BEOL process flow and the sketch of BEOL profile.

[8] http://www.almaden.ibm.com/st/chemistry/dm/

Figure 2-2 shows the process flow and the profile of BEOL. In the semiconductor fabrication, the interconnector process starts when the CMOS process is finished. First, the dielectric oxide was deposited for isolation and the via structure was defined by lithography and etching process. Second, a thin Ti/TiN was deposited for the barrier layer, followed by the thick W layer deposited for the main interconnector material. Third, the W via was formed by using CMP process, and another Ti/TiN was deposited for trench barrier layer. Next, Al was deposited and the trench structure was defined by another lithography and etching process. Finally, the completion of interconnect circuit could be done by repeating these process.

2.1.1 Deposition

This process is often used in the semiconductor industry to produce high-purity and high-performance thin films. The useful deposition systems in the semiconductor process are physical vapor deposition (PVD) and chemical vapor deposition (CVD) systems. As for which tool should be used, it is up to the purpose of the process.

Figure 2-3 shows the sketch of PVD system. The argon (Ar) plasma was produced by a high voltage in the vacuum environment. This plasma induces high speed Ar ions and they rush to the target (cathode side) at the same time. Then, the atoms of target will be hit out by these Ar ions, and they will fly to the substrate (anode side) to coat on the substrate surface. Moreover, with the addition of oxygen gas flow, we can control the oxygen content in the thin films.

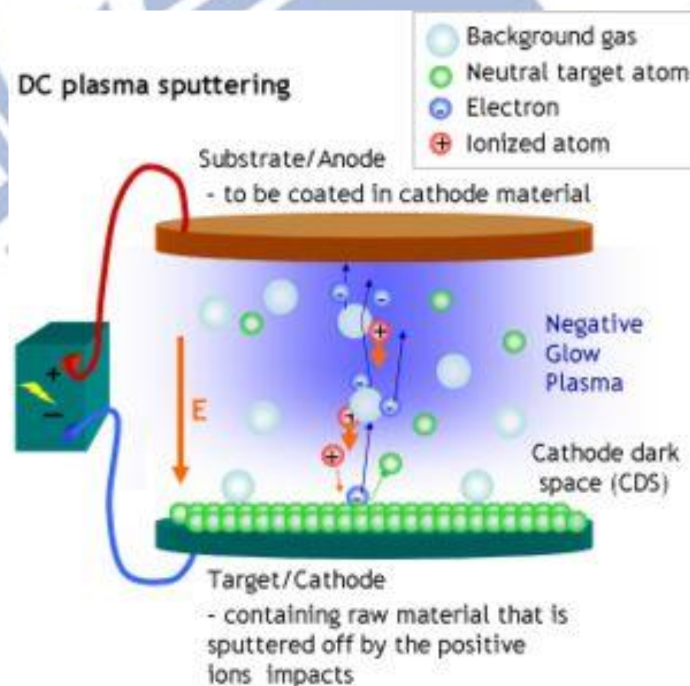

Figure 2-3. The sketch of PVD system[9].

[9] http://en.wikibooks.org/wiki/Microtechnology/Additive_Processes

Figure 2-4 shows the sketch of CVD process. In the CVD process, the substrate is exposed to the volatile precursor environment. Then, these precursors reactive on the substrate surface to produce the desired deposit. Finally, the volatile byproducts are removed by gas flow through the reactor.

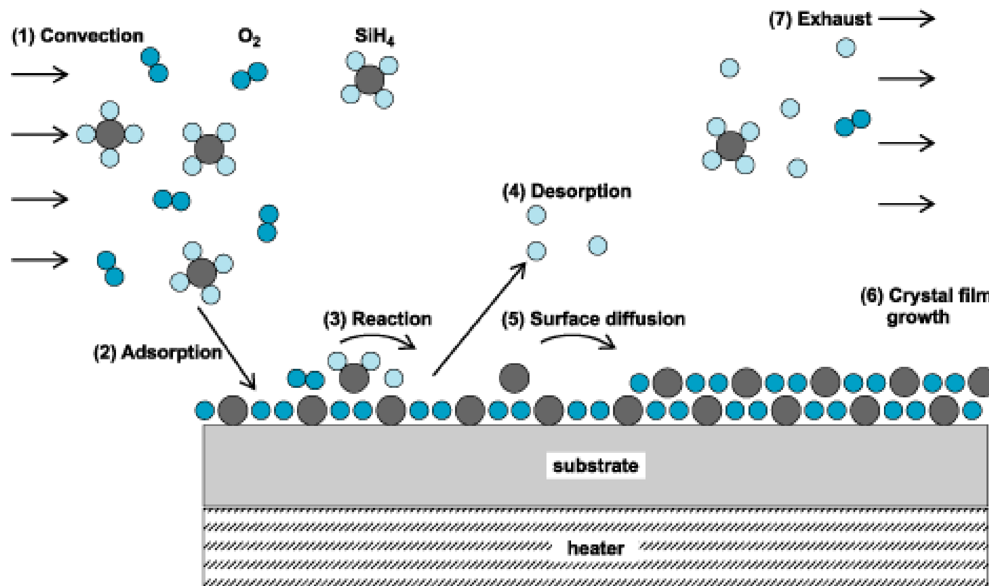

Figure 2-4. The sketch of CVD process[10].

In our research, the NiO_x and TiO_x film were prepared by the ion beam sputtering (IBS). Figure 2-5 shows the sketch of IBD. In the deposition process, the high energy ions beam was of electron cyclotron resonance (ECR) provided by microwave generator. With the controlling of electric field by microwave, the ECR produced high energy ion beam, and the ionization of gas molecule was done in the ion emission process. Then the ion beam rush to the target and the atoms of target will be hit out by this ion beam, and they will fly to the substrate to coat on the substrate surface. Moreover, with the addition of oxygen gas flow, we can prepare different oxygen content sample with different oxygen flow ratio.

[10] http://accessscience.com/content.aspx?id=800560

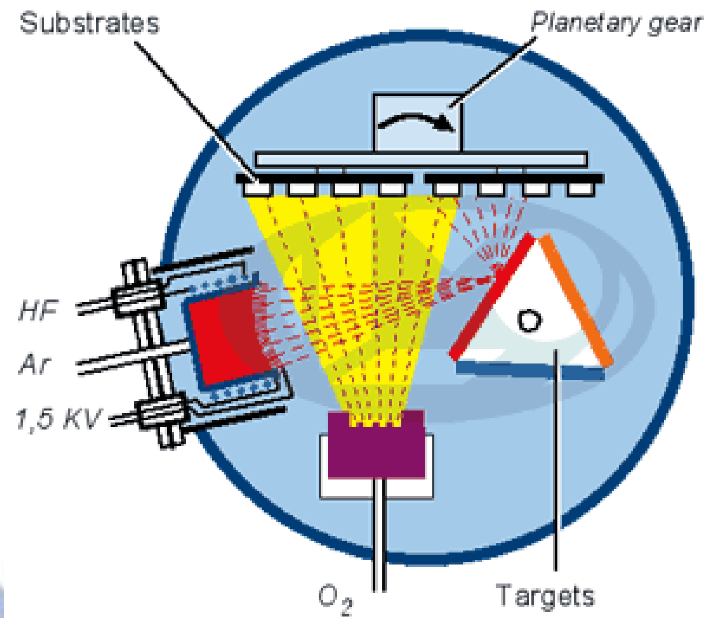

Figure 2-5. The sketch of IBD system[11].

2.1.2 Lithography

In the micro fabrication, photolithography is used to define the geometric pattern. Coating, exposure, and development are three parts of lithography process. Figure 2-6 shows the process flow of lithography. First, the substrate is coated with a light sensitive chemical material, which is called the photoresist (PR). This process is also called the coating. Second, the exposure process uses light to transfer a pattern from a mask to PR on the substrate. The area with light exposure can be removed or kept on the substrate, dependent on the PR character (positive or negative PR). Moreover, this light through mask will pass several lenses and scale down the size to micro or even nano meter scale on the substrate. The minimum size of pattern on the substrate is dependent on the light source. The light with shorter wavelength can define smaller pattern size. Finally, the developer is used to remove the undesired part of PR in the development process. E-beam lithography is another exposure technology without mask. It uses electron beam to define the pattern on the substrate. Although this technology can save the mask price, the process speed is much slower than traditional lithography technology. In our experiment, the both top metal and metal oxide pattern was prepared by JOEL6500.

[11] http://www.laseroptik.de/?Coating_Guide:Prod._Methods:Ion_Beam_Sputtering

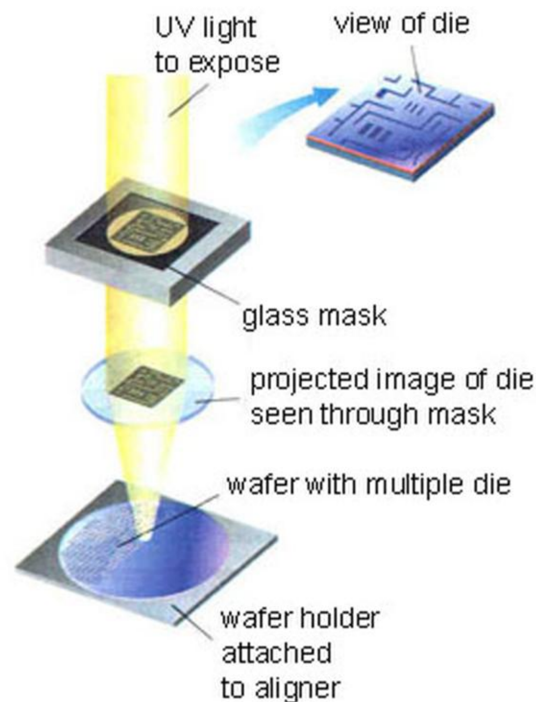

Figure 2-6. The sketch of Lithography process[12].

2.1.3 Etching

In the etching process, an aqueous chemical ("wet") or plasma ("dry") is used to remove the uppermost layer without protection. The isotropic wet etching process is used for highly selective material etching process. For example, the etching ratio between silicon oxide (SiO_x) and silicon nitride (SiN_x) is very high in the phosphoric acid solution. It is usually used to remove the SiN_x layer. However, another anisotropic dry etching process is generally used in order to avoid the significant undercutting of profile. Due to its straight profile, most etching processes use dry etching process in the semiconductor fabrication.

Wet etching, the simplest etching technology, requires nothing but a container with a liquid solution that will dissolve the material. Because this process uses liquid solution, the isotropic etching process can't be avoided. In this process, the protection layer becomes highly important because it can avoid the undercutting issue. Figure 2-7 shows the anisotropic and isotropic etching process. The isotropic etching process inevitably induces the undercutting issue.

[12] http://www.ncnanotechnology.com/public/features/TNLC.asp

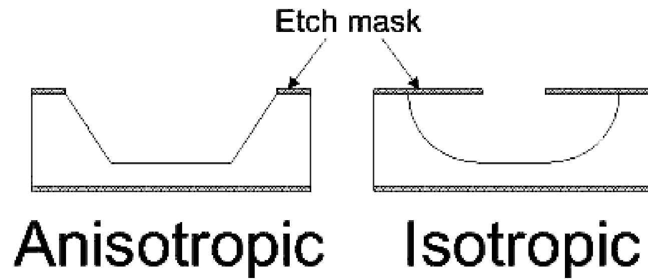

Figure 2-7. The sketch of etching process[13].

Dry etching, the anisotropic etching process, is usually used for general semiconductor fabrications. The dry etching process uses the plasma with chemical gas to remove the part without protection. Figure 2-8 depicts the dry etching process. Because the plasma has one way direction, the dry etching can avoid the undercutting issue. The anisotropic dry etching profile was shown in figure 2-7.

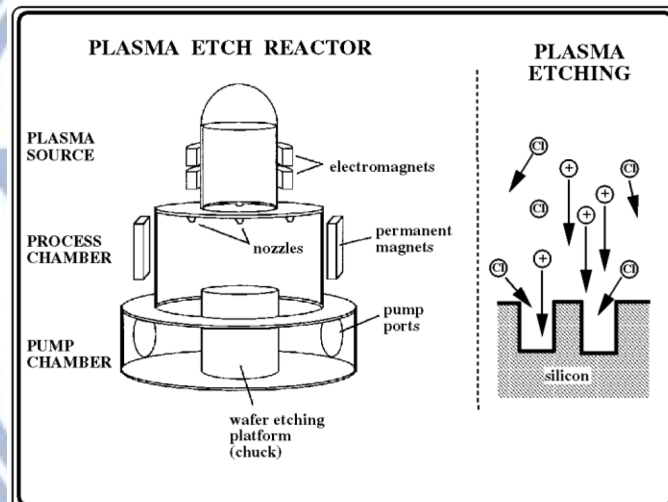

Figure 2-8. The sketch of dry etching process[14].

2.1.4 Chemical mechanical Polishing (CMP)

Figure 2-9 delineates the CMP process. In this process, the top material on wafer surface will react with the chemical solution, and then the mechanical polish is used to remove the material on wafer surface. Another purpose of this process is to make the wafer surface smooth. In the Cu interconnector process, the CMP process is used for the Cu material removal because Cu can't be removed by etching process.

[13] http://www.el-cat.com/silicon-properties.htm

[14] http://ngpdlab.engin.umich.edu/completed-projects/plasma-etching

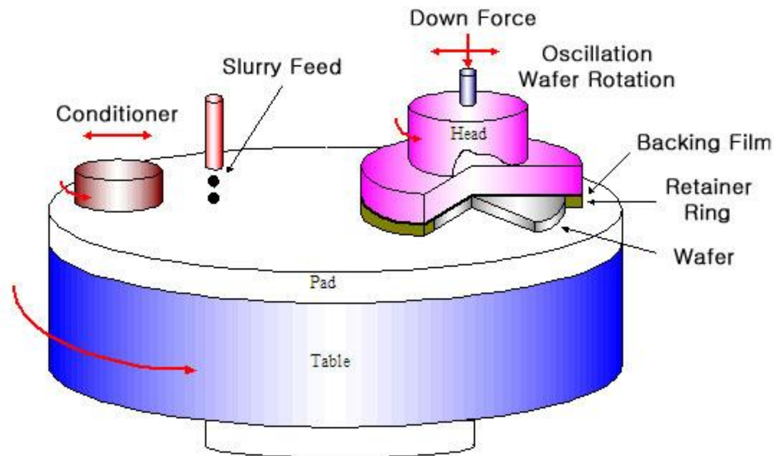

Figure 2-9. The sketch of CMP process[15].

2.2 Layout

In our experiment, the mushroom structure of NiO_x and TiO_x were deposited by IBS. Before these metal oxide deposition, the W plug structure was form by 0.18 um technology node BEOL fabrication. The metal oxide and top metal pattern was prepared by JOEL6500 E-beam lithography system. The real active area of RRAM was placed on the top of W plug. Figure 2-10 shows the top-view and the profile sketch of NiO_x and TiO_x RRAM.

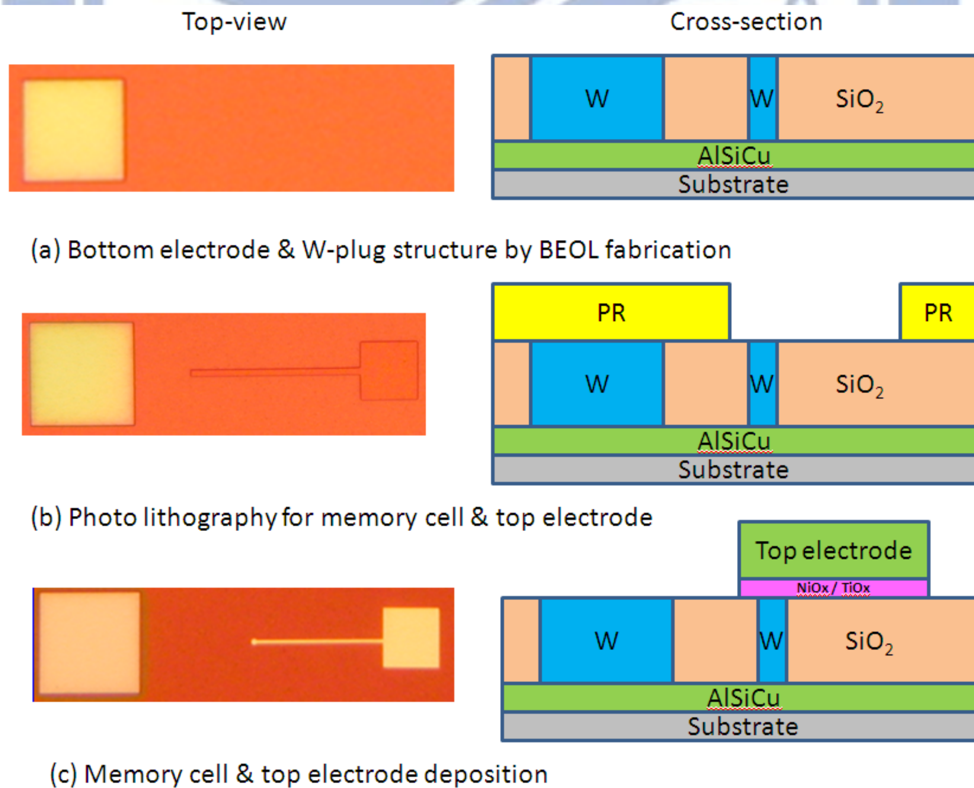

Figure 2-10. The top-view and cross-section of NiO_x and TiO_x RRAMs.

[15] http://www.ceramic.hanyang.ac.kr/paik/cmp.htm

However, the WO_x RRAM was formed on the top of tungsten plug by using plasma oxidation process. After this oxidation, the E-beam lithography was used to define the area of top electrode, and then we remove the other part to form the top electrode. The top-view and cross-section of W-based RRAM were shown in figure 2-11.

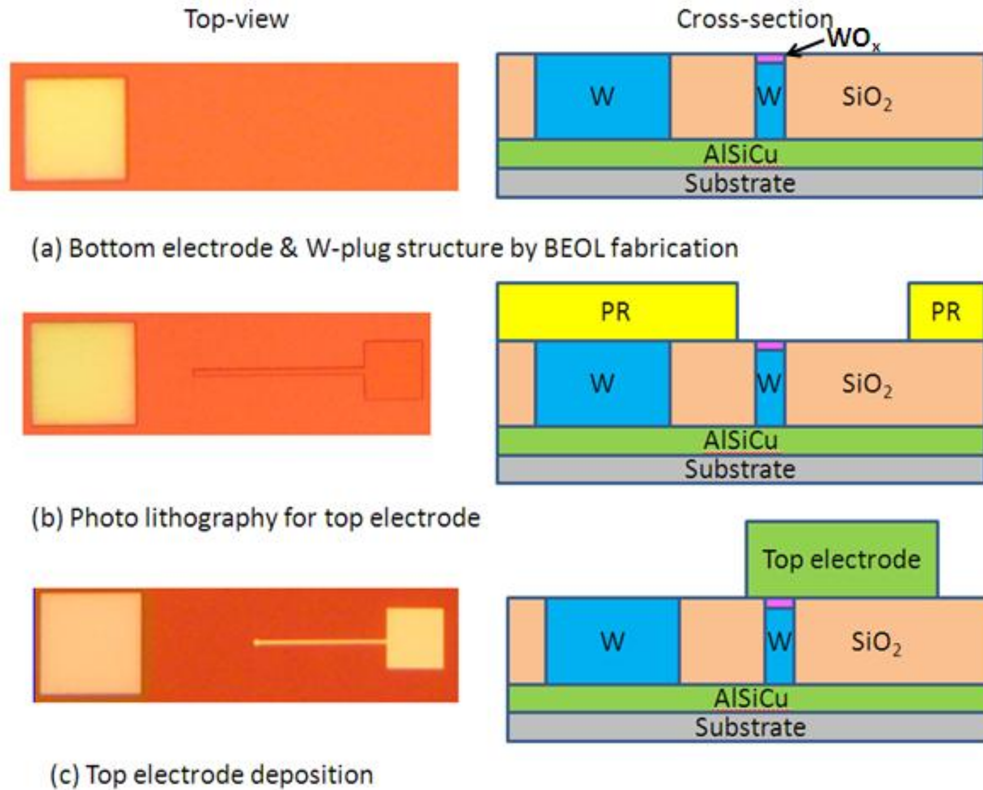

Figure 2-11. The top-view and cross-section of nickel oxide and WO_x RRAM.

2.3 Analysis

In the analysis process, the pulse generator (HP81110A) and semiconductor parameter analyzer (HP4156) were used for the electrical characteristic analysis. In the electrical analysis, the switching box (Keithley707) was also used for changing the measurement channel. There were several tests, including cycle endurance, thermal stability, stress analysis, data retention, and read disturb in the electrical analysis. The purposes of those measurements were for the reliability performance check.

For material analysis, the x-ray photoelectron spectroscopy (XPS) was used for the compositional analysis and profile analysis. The transmission electron microscopy (TEM) was used for the microstructure observation. Moreover, physical property measurement system (PPMS) was used for the temperature dependence electric character measurement.

2.3.1.1 Cycle Endurance Measurement

This cycle endurance measurement is one of the reliability performance tests. The better cycle endurance performance sample indicates the more programming operation times in the cycling process. Figure 2-12 shows the typical cycle endurance test. And the test steps are as follows. First, the initial resistance of memory cell was measured by HP4156. Second, the switching box (Keithley707) changes the channel to pulse generator (HP81110A) and then gives a pulse voltage to switch the resistance state. Third, return the channel to read the resistance state again. Finally, switch the channel to pulse generator again and apply a pulse voltage to switch back the resistance state. Repeating these previous processes is the cycle endurance test.

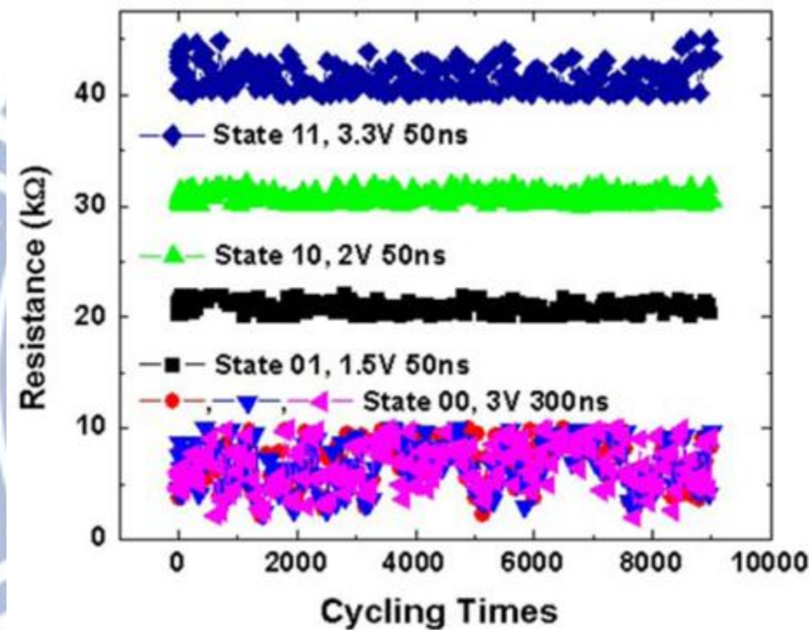

Figure 2-12. The 2 bits/cell cycle endurance test of RRAM[36].

2.3.1.2 Thermal Stability Measurement

The thermal stability test is another measurement of reliability performance test. In our thermal stability test, we program the resistance state to both high and low resistance state and then put those two resistance state samples in high-temperature (above 85℃) oven for long time baking. In the baking process, those samples was take out from oven to confirm the resistance state at room temperature for a period then put back to oven for long time baking. With this repeatedly and period test, we can observed the thermal stability performance. Figure 2-13 shows the typical thermal stability test. The memory cell exhibits better thermal stability performance with the higher baking temperature or long baking time test.

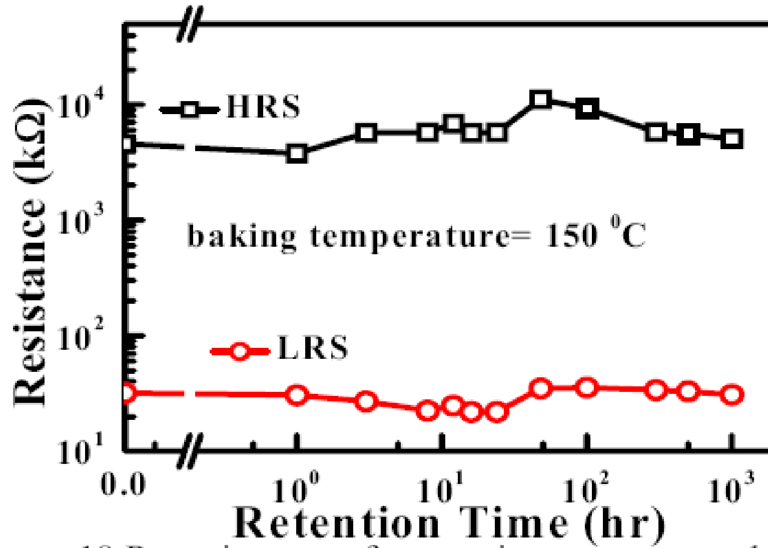

Figure 2-13. The typical thermal stability test[37].

2.3.1.3 Stress Test

In the stress test, we use the pulse generator to prove a long time stress, and the resistance is measured by HP4156 after the stress-applied bias. In this stress process, the direction of stress voltage is opposite to the switching voltage. For example, if the switching bias is positive voltage, the stress bias is the negative voltage. If the switching bias is negative voltage, the stress bias is the positive voltage. Figure 2-14 shows the typical stress test of RRAM. It shows the influence of applying a stress voltage on the resistance state.

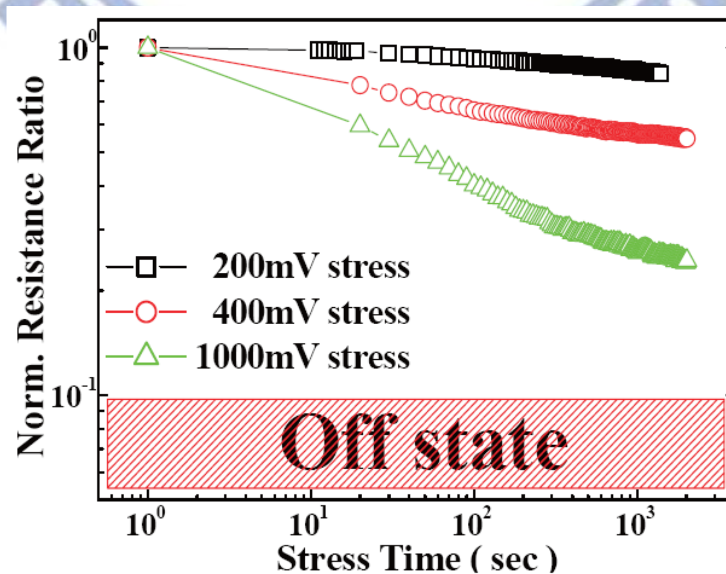

Figure 2-14. The typical stress test of RRAM[20].

2.3.1.4 Data retention Measurement

Before this data retention test, the switching voltage formed all resistance states. After the resistance switching process, HP4156 was used to detect the resistance of memory cell for a period of time. By means of this periodicity reading and waiting process, we can observe the data retention performance in this test. Moreover, the reading voltage of this data retention test must be small because the memory cell may be damaged by large voltages in the reading process. With this long time resistance reading process, we can obverse the data retention performance. Figure 2-15 shows a typical data retention test of 2bits/cell RRAM device. In this figure, all four-resistance states keep the same resistance value more than 10^4 src.

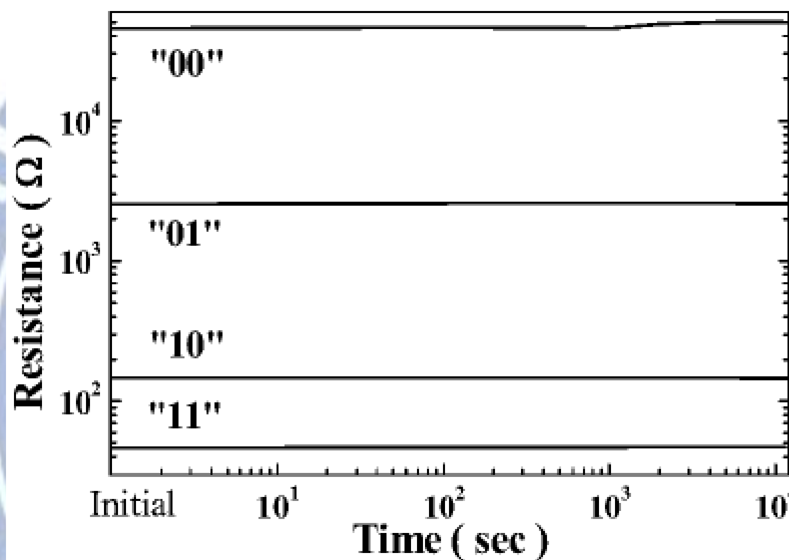

Figure 2-15. The data retention test of 2 bits/cell RRAM device[29].

2.3.1.5 Read Disturb Measurement

In the read-disturb performance test, it is similar to the data retention test. Before the read-disturb test, the switching voltage formed all resistance states. The different part with the data retention test is the waiting time. In this test, there are only reading processes in this measurement. With these repeating resistance reading process, we can observe the read-disturb performance of memory cell. Moreover, the small reading voltage is used to avoid damaging the memory cell in the test process. Figure 4-16 shows the typical read-disturb performance test. In this figure, The “On” state is influence by the reading voltage, and the “Off” state keeps the same value in the read-disturb process.

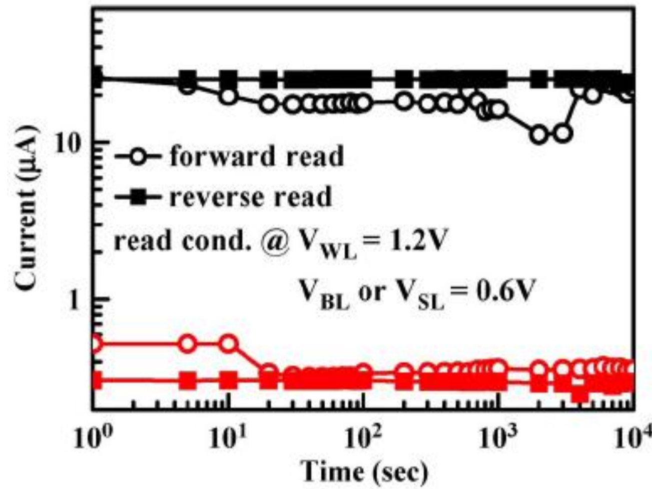

Figure 2-16. The typical read disturb test of RRAM device[37].

2.3.2.1 XPS Analysis

X-ray photoelectron spectroscopy (XPS) is a quantitative spectroscopy technology to determine the elemental composition, empirical formula, and electronic state of elements. It is the use of low-energy X-ray source as the excitation source and through the analysis of samples with a characteristic energy of emitted electrons to achieve the purpose of analyzing the chemical composition; that is an ample surface analysis technology. Figure 2-17 shows the construction of XPS. XPS analysis is made into the X-ray beam; the atoms interact with the sample surface after the electronic excitation of atomic inner-shell ionization to detect the sample composition and structure. This is the characteristic X-ray excitation, and the electron here is called ionization photoelectron. Because of the specific wavelength of the X-ray, its energy is known, and the electron binding energy can be calculated by Eq.(2-1).

$$E_{binding} = E_{photon} - (E_{kinetic} + \phi) \quad \text{.......... (2-1)}$$

Here, $E_{binding}$ is the binding energy of electron, E_{photon} is the energy of the X-ray photon, $E_{kinetic}$ is the kinetic energy of the electron as measured by the instrument, and $\psi$is the work function of the spectrometer. The XPS spectrum can be observed by using binding energy as X-axis and relative intensity as Y-axis. With this spectrum, we can get the informant of samples with elemental composition and chemical state. XPS is the most useful for chemical analysis, and it is also call “electron spectroscopy for chemical analysis” (ESCA).

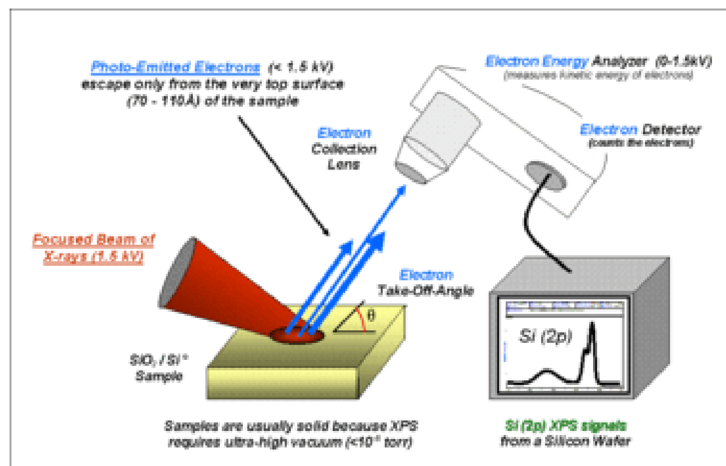

Figure 2-17. The sketch of XPS[16].

2.3.2.2 TEM Analysis

Transmission electron microscope (TEM) uses high-energy electron beam (about 100keV ~ 1MeV) through the thin samples (below 100nm), and various structure within the thin samples have different degrees of scattering. Scattering of electrons by means of different routes goes through the subsequent combination of lens aperture lens, forming the contrast images of light and dark, and the microstructure of these images is shown with the fluorescent plate. Therefore, transmission electron microscopy analysis of thin samples is acquired through transmitted electron or elastic scattering electron, or diffraction pattern microstructure, and thus resolves the structure of the thin samples and the crystal structure. Figure 2-18 shows the construction of TEM.

Moreover, the selected area electron diffraction (SAED) in TEM instrument is also can be used to check the sample structure. The SAED principle is in that thin crystal sample, the high-energy parallel ray electron beam can go through this thin sample. In this case, electron is the corresponding volatility, rather than the particle nature. As the energy of the electron wavelength is nanometers in length, and the wavelength is relatively much larger than the spacing between atoms, the atoms are arranged in this electron diffraction grating. This means that a portion of the wavelength will be scattered out of a particular point of view (different parallel surfaces) and will decide the crystal of the sample.

[16] http://wiki.utep.edu/display/~vrrangel/X-ray+Photoelectron+Spectroscopy+(XPS)

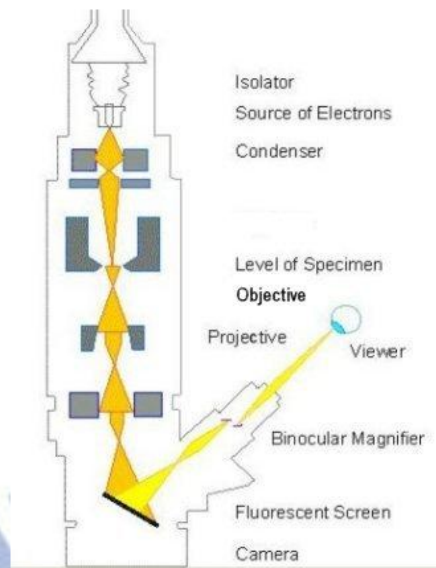

Figure 2-18. The sketch of TEM[17].

2.3.2.3 PPMS Measurement

The temperature dependent electric character data was analyzed by the PPMS system PPMS. The cooling system uses the liquid helium (He) to cool the measurement system, and the minimum temperature is about 4K. The temperature range is between the room temperature and 4K. In the cooling process from room temperature to 4K, we can observe the resistance change in this cooling process.

[17] http://universe-review.ca/R11-13-microscopes.htm

Chapter 3 : Principles

In recent years, many researches study the resistive switching mechanisms of novel RRAM. According to the result of these studies, we discuss several important physics parameters which influence the performance of RRAM. These physics parameters including cell thickness[38], cell size[39], doping material[40] , electrode[41], density of oxygen vacancies, and electric field[38,42]. Moreover, the RRAM performance can also be improved with modified operation process[36,43,44]. By applying suitable device structure and modified operation to potential materials, the RRAM device performance shows much improvement in the last ten years.

For the electric characteristics analysis of RRAM, many researches on different materials elucidate the electron transport mechanisms of both high and low resistance states follow various conduction mechanisms, such as metallic transportation[20], Schottky emission[45], tunneling, space-charge-limited-current (SCLC)[46], Frenkel-Poole emission[47-49], Trap-assisted-Tunneling (TAT)[50], electron hopping transportation[20], and so on.

Moreover, for the resistive switching mechanism studies, most of the literatures indicate the conducting filament[51-53] mechanism related to oxygen-vacancy[54,55]. Also, various models, such as stochastic model[56], two-variable resistor model[46,57], compact model[58], thermal dissolution model[48,59], rupture ball model[38], etc., were proposed to explain the resistive switching phenomenon in their researches.

In order to show a specific RRAM profile for readers, we introduce the basic resistance switching characteristics and nomenclature, electron transportation mechanism, resistance switching mechanism and model, key physics parameters and modified operation process in this chapter.

3.1 Resistance Switching Characteristics and Nomenclature

Before the introduction of RRAM principle, we describe the basic resistance switching characteristics including bipolar, unipolar, and nonpolar operations. Also, we discuss the basic resistance switching nomenclature, including forming process, set (programming) process, reset (erasing) process, forming voltage , set voltage (current), reset voltage, HRS (reset state), LRS (set state), resistance window (on/off ratio), dc voltage (current) sweep, and pulse switching in this section.

3.1.1 Bipolar, Unipolar, and Nonpolar Operations

For the resistance switching phenomenon in RRAM, bipolar and unipolar are the two major operational methods in the bistable resistance switching process. In earlier researches at 1970s, the most common resistance switching phenomenon of RRAM displays the bipolar operation. It means that the resistance state depends on the polarity

of applied bias. Biases with different polarities induce different memory states. However, the bipolar RRAM resistor always integrates with one transistor in device applications. This one-transistor-one-resistor (1T1R) device has a larger device size and it will limit the capacity in memory applications. In recent years, the unipolar RRAM becomes an important memory application because it can integrate with a diode to form a one-diode-one-resistor (1D1R) device for memory applications. This 1D1R device has a smaller device size and it shows higher potential for high capacity memory application. In this section, we describe the typical RRAM operation method.

Figure 3-1 shows the typical bipolar operation of resistance switching phenomenon[60]. The resistance state depends on the polarity of applied bias. For example, the resistance state can be switched from low resistance state (LRS) to high resistance state (HRS) by applying a sweep bias, which shows from loop 1 to loop 2 in figure 3-1. Also, this HRS can be switched back to LRS by applying an opposite bias (from loop 3 to loop 4). Moreover, in order to protect the memory cell in this resistance switching process from HRS to LRS, the current compliance is necessary in this resistance switching process, and it can be observed on the dash line of figure 3-1.

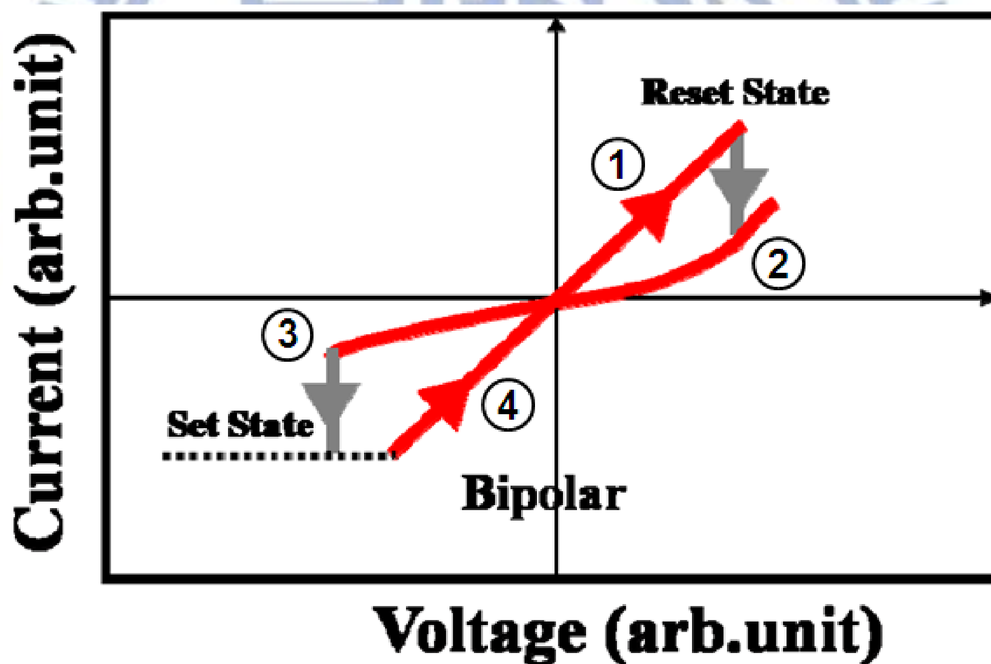

Figure 3-1. The typical dc sweep bipolar operation characteristics.

The bipolar operation, which is described in the previous page, belongs to the dc sweep operation. Another bipolar operation is the pulse voltage operation, which shows fast speed in the resistance switching process. For example, in figure 3-2 the resistance state can be switched with the applied pulse shot (~80ns) and this resistance switching characteristics exhibits polarity dependence relationship of pulse shot. The opposite pulse shot induces opposite resistance state. This kind of operation belongs to the pulse voltage operation.

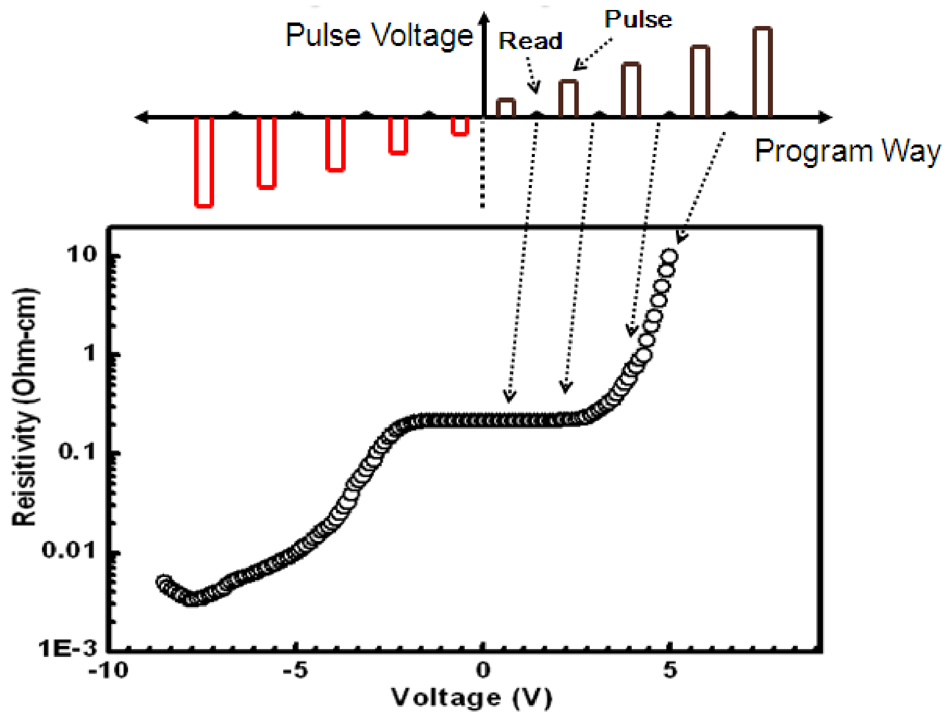

Figure 3-2. The bipolar operation characteristics by applied pulse voltage.

Another polarity operation of resistance switching phenomenon is the unipolar operation method. The typical unipolar operation is shown in the upper-right region of figure 3-3. The resistance state can be switched from LRS to HRS by applying a sweep bias, which shows from loop 1 to loop 2 in figure 3-3. Also, this HRS can be switched back to LRS (from loop 3 to loop 4) by a higher applied bias. In this unipolar operation process, the current compliance is necessary to protect the memory cell in resistance switching process from HRS to LRS, and it can also be observed on the dash line in figure 3-3.

Usually, most unipolar operation RRAM materials exhibit the resistance switching characteristics by only one-way polarity voltage. Moreover, the resistance state can’t be switched by the opposite polarity voltage. However, only several materials exhibit two-way unipolar operation, which we call “nonpolar operation”. The unipolar resistance switching characteristics can be observed by both positive and negative voltages. As shown in figure 3-3, the two unipolar operation characteristics can be observed in both upper-right and lower-left region. This operation method is called “nonpolar operation” and it shows symmetrical resistance switching behavior.

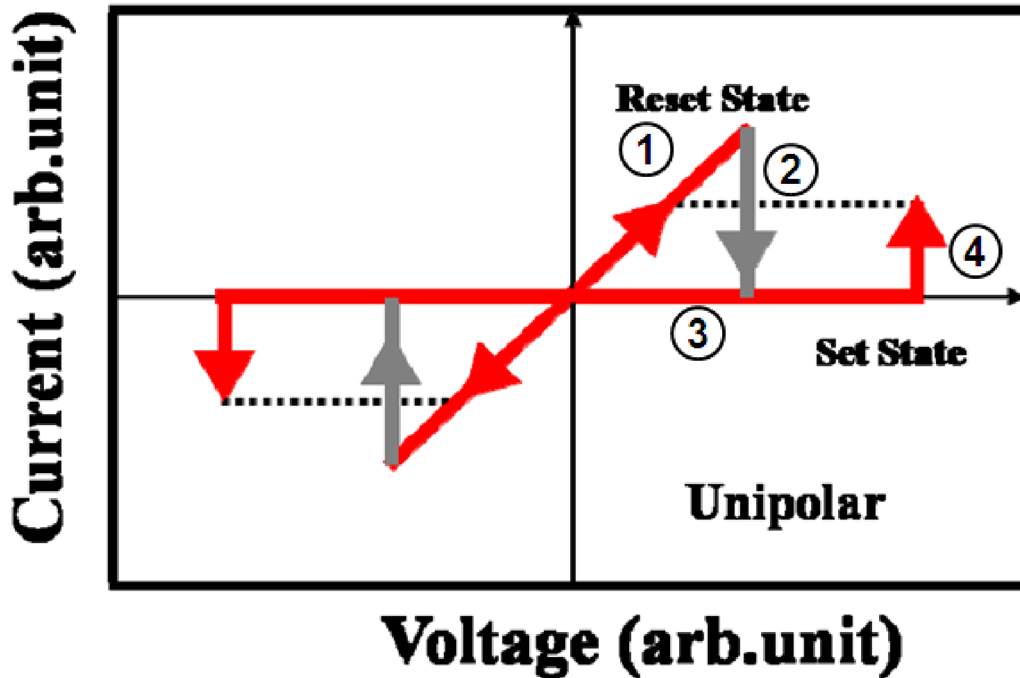

Figure 3-3. The typical unipolar and nonpolar operation characteristics.

In the unipolar operation, the resistance state can also be switched with an applied pulse voltage. Figure 3-4 shows the unipolar resistance switching characteristics[60] with the applied pulse voltage. In this case, we fix the applied voltage about 4V and increase the pulse width from 10ns to 1us. With the pulse width increasing, it is clear to see that the resistance state increases first and then decrease in the unipolar operation process.

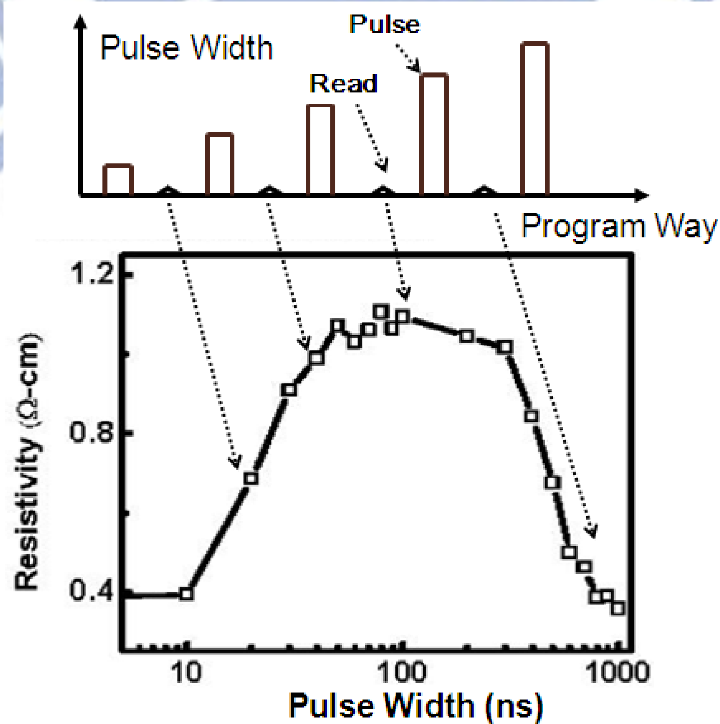

Figure 3-4. The unipolar operation characteristics by applied pulse voltage.

3.1.2 Basic Resistance Switching Nomenclature

In the researches of RRAM, different literature used different nomenclature that always confuses readers. Before the discussion of RRAM principles in this section, we introduce the nomenclature of RRAM to avoid the confusion.

First of all, we introduce the initial resistance state, which means the resistance of as-prepared. The resistance of this state is always higher than other states due to the high resistance metal oxide film. Before the resistance switching operation, most materials need a high voltage applied to work up the resistance switching characteristics. For the example of unipolar operation[61] RRAM in figure 3-5, this memory cell needs a high voltage about 7.5V applied to work up the memory characteristics. This voltage is called the "forming voltage" (V_{form}) and this process is called the "forming process" (from arrow 1 to arrow2). As shown in figure 3-5, the resistance state is switched from the initial resistance state to the LRS in this forming process. However, several researches use current sweep method in this forming process to protect the memory cell, and the resistance switching current is also called "forming current".

Secondly, the resistance state can also be switched from LRS to HRS with another applied bias. For example, in figure 3-5 the resistance state can be switched from LRS to HRS at about 2V. This voltage is called the "reset voltage" (V_{reset}) and this process is called the "reset process" (from arrow 3 to arrow 5). In other literature, this reset voltage is called the "erasing voltage" and this process is called the "erasing process", and this HRS the "reset state" or "off state".

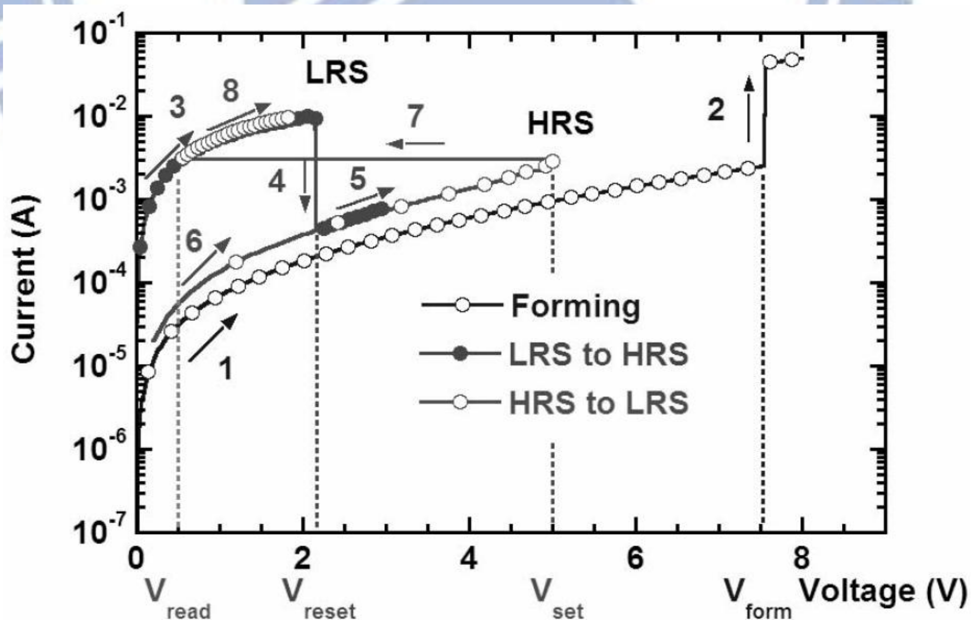

Figure 3-5. The resistance switching characteristics of unipolar RRAM.

Next, this HRS can also be switched to LRS with a higher applied voltage. For example, in figure 3-5 the resistance state can be switched from HRS to LRS at about 5V. This voltage is called the "set voltage" (V_{set}) and this process the "set process"

(from arrow 6 to arrow 8). In other literatures, this set voltage is called as “programming voltage”, this process as “programming process”, and this LRS as the “set state” or “on state”. However, several researches use current sweep method in the set process to protect the memory cell, and the resistance switching current is called “set current”.

What’s more, the on/off ratio between HRS and LRS is called the “resistance window”. Other researches also call it “On/Off ratio”. The larger On/Off ratio sample indicates that it has more potential for multiple-level-cell (MLC) application and is suitable for high density storage memory application, which is shown in figure 3-6.

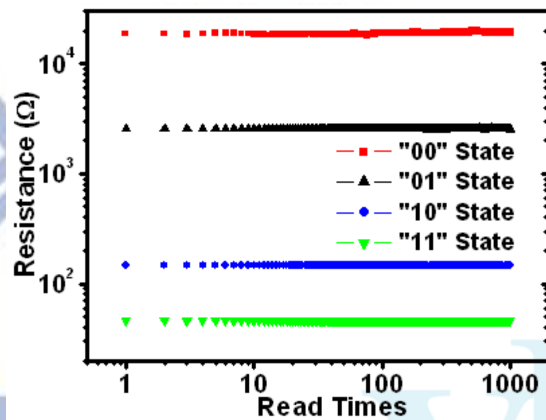

Figure 3-6. The multiple-level-cell (MLC) of 2bits/cell RRAM.

3.2 Electron Transportation Mechanism

After the discussion of RRAM resistance switching characteristics and nomenclature, we describe the electron transportation mechanism of both LRS and HRS in this section. In recent years, numerous electron transportation mechanisms have been proposed for the RRAM researches. These mechanisms include the metallic transportation[20], electron hopping transportation[20], Schottky emission[45], SCLC[46], TAT[50], Pool-Frenkel emission[47-49], etc. The metallic transportation mechanism with linear I-V curve, which follows Ohm’s law, is usually used to explain the electrical characteristics of LRS. Also, the Poole-Frenkel emission and TAT mechanisms with non-linear I-V curve are only used to explain the behavior of HRS. Furthermore, other mechanisms with non-linear I-V curve are used to explain both LRS and HRS in several literatures[45].

3.2.1 The Metallic Transportation Mechanism

The metallic transportation mechanism includes two parts. One is the linear I-V curve, and it follows the Ohm’s law. As shown in arrow 1 of figure 3-3, the LRS shows the linear I-V curve, and the current linearly depends on the voltage. The electrical character follows the Ohm’s law and it is also shown in Eq. (3-1).

$$I = \frac{V}{R} \quad \text{.......... (3-1)}$$

The other part is the temperature effect on the electrical characteristics[20]. When the temperature decreases, the resistance decreases in the meantime. As shown in figure 3-7, the resistance reduces when the temperature decreases both at high and low temperatures, and this characteristic displays the metal behavior.

This metal transportation mechanism is always used to describe the electrical characteristics of the LRS due to the linear I-V curve.

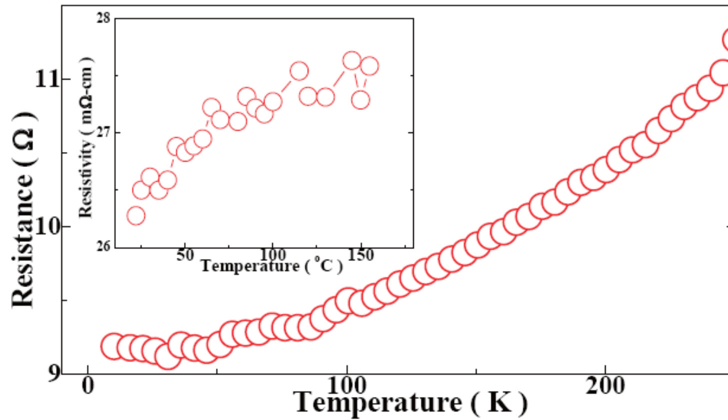

Figure 3-7. The temperature dependence relationship of metal electrical characteristics.

3.2.2 The Schottky Emission

Except for the metal transportation mechanism, all of the electrical transportation mechanisms show the non-linear I-V curve. Another common transportation mechanism of RRAM is the Schottky emission[45]. This mechanism is attributed to the metal-semiconductor contact, which induces the barrier height at the interface, and this barrier height also influences the characteristic of the electrical transportation characteristics. Figure 3-8 shows the energy band diagram of the metal-semiconductor contact and the electrical transportation follows the Schottky emission.

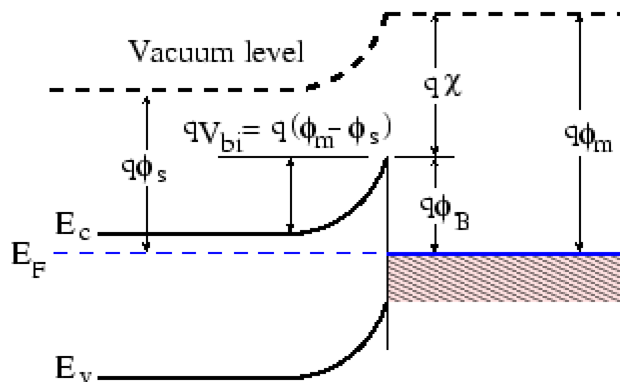

Figure 3-8. The energy band diagram of a metal-semiconductor contact[18].

[18] http://www.iue.tuwien.ac.at/phd/ayalew/node56.html

Moreover, this transport mechanism is dependent on the barrier height and the dielectric constant, as is shown in Eq. (3-2).

$$J = A^* T^2 \exp(\frac{-q}{k_B T}[\phi_B - \sqrt{\frac{q\xi}{4\pi\varepsilon_i}}]) \text{ ……………………..(3-2)}$$

where A* is the effective Richardson constant, φ_B is the barrier height, ξ is the electric field, and ε_i is the insulator dielectric constant. In the electrical character of this Schottky emission, the value of log current increases in the same amount with the square root of voltage, and the typical Schottky emission electrical curve[45] is shown in figure 3-9. The Schottky emission electric characteristic appears in both LRS and HRS of RRAM electrical transportation mechanism. Because several metal oxides (nickel oxide, etc.) are n-type semiconductors, the RRAM structure also forms the metal-semiconductor contact, and the electrical characteristics also shows the Schottky emission in both LRS and HRS.

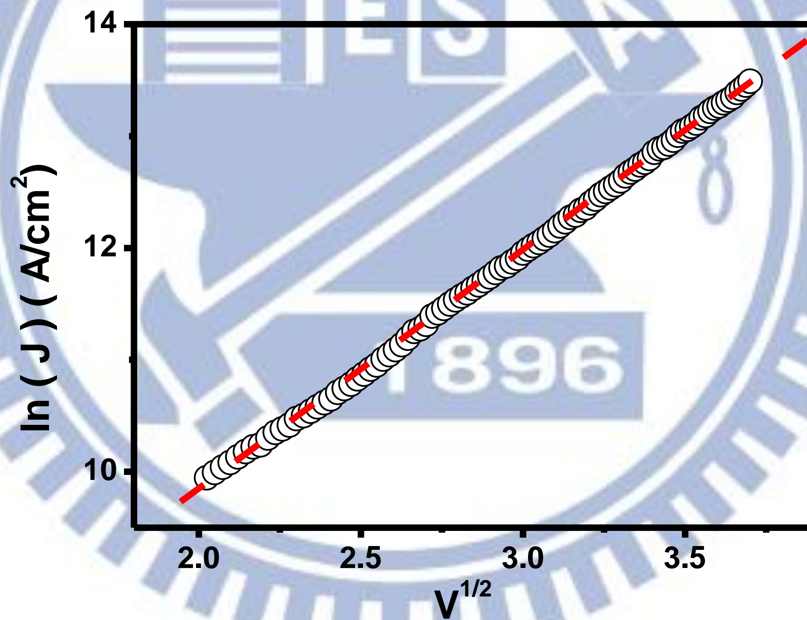

Figure 3-9. The typical electrical curve of Schottky emission.

3.2.3 The Poole-Frenkel Emission

Another common electrical transportation mechanism of RRAM is the Poole-Frenkel emission[47-49] and it also shows a non-linear I-V curve. This mechanism, which is attributed to the electrons, can move slowly through an insulator and these electrons are generally trapped in localized states. Moreover, the random thermal fluctuations or large electrical field will give the electrons enough energy to get out of its localized state and move to the conduction band. Figure 3-10 shows the energy band

diagram of the Poole-Frenkel emission.

Moreover, the transport mechanism is dependent on the barrier height and the dielectric constant, as is shown in Eq. (3-3).

$$J \propto E \exp(\frac{-q}{k_B T}[\phi_B - \sqrt{\frac{qE}{\pi\varepsilon}}]) \quad \text{......................(3-3)}$$

For Poole-Frenkel emission, the value of log(J/E) increases in the same amount with the square root of electrical field, and the typical Poole-Frenkel emission electrical curve[49] is shown in figure 3-11. The Poole-Frenkel emission characteristic appears in HRS of RRAM electrical transportation mechanism. Because the metal oxide film shows the insulator characteristic, the electrical curve of RRAM also shows the Poole-Frenkel emission behavior in HRS.

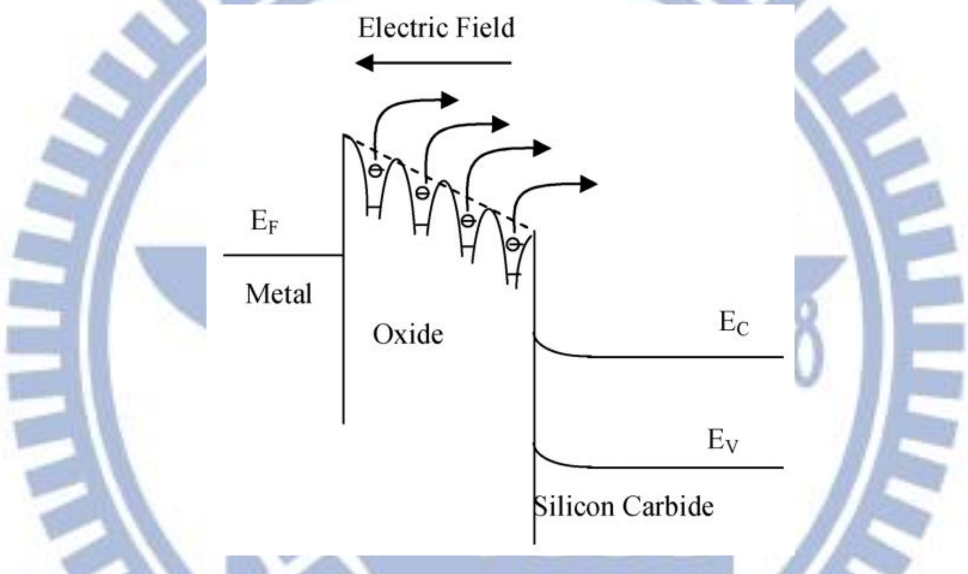

Figure 3-10. The energy band diagram of Poole-Frenkel emission[19].

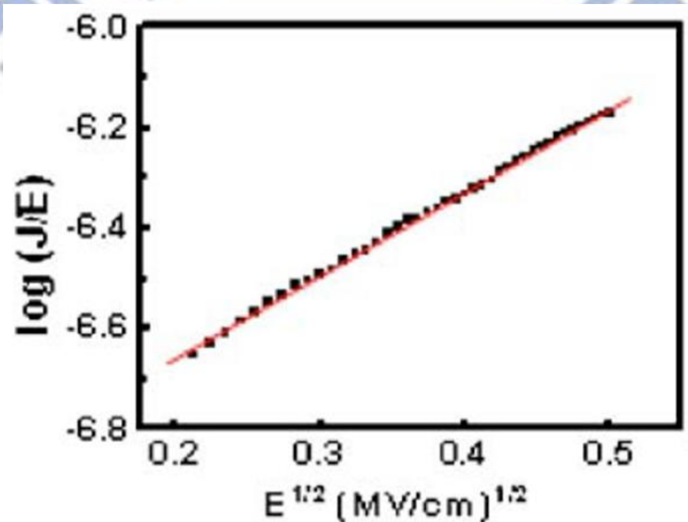

Figure 3-11. The typical electrical curve of Poole-Frenkel emission.

[19] Sanjeev K. Gupta, A. Azam, and J. Akhtar, J. Phys., vol.74, No.2, 327, (2010)

3.2.4 The Electron Hopping Transportation Mechanism

The electron hopping transportation[20] is another common electrical transportation of RRAM and it shows a non-linear I-V curve. The early researches indicated that this mechanism has low temperature conduction behavior in strongly disordered systems with localized states. Several researches reported the Mott variable range hopping (VRH) characteristics of RRAM materials. Figure 3-12 shows the band diagram of VRH. These gradation localized states is formed by the strongly disordered systems.

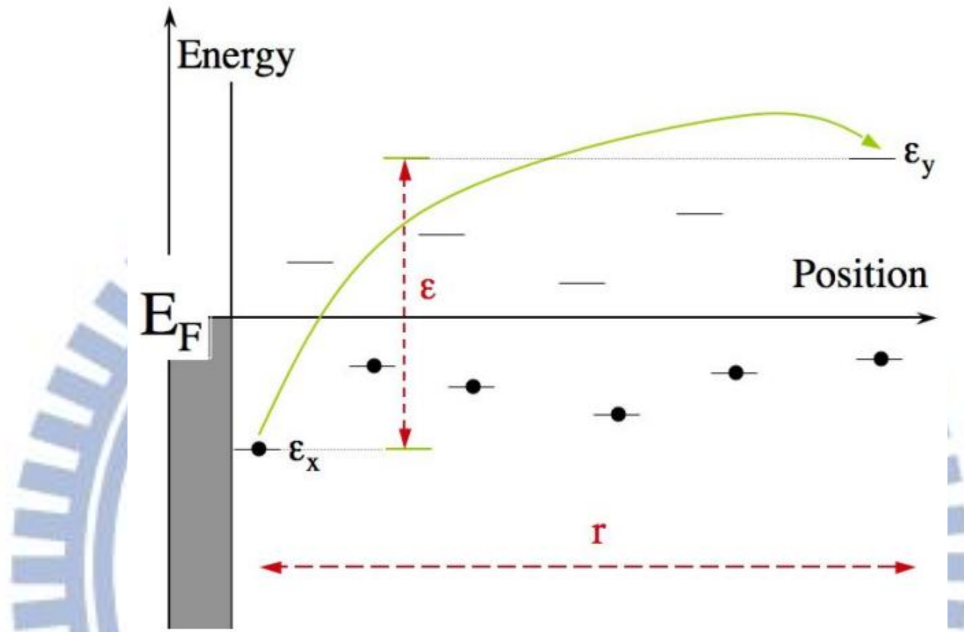

Figure 3-12. The band diagram of variable range hopping[20].

The VRH[62] transport mechanism is depicted by Eq. (3-4). Here, R is the hopping distance, $N(E_f)$ is the density of state, k is the Boltzman's constant, E is the electric field, α is the decay parameter of wave function, and ν_{ph} is dependent on the frequency of phonon.

$$J = A\exp(-BT^{-1/4})\sinh(\frac{eRF}{kT}) \text{ ....(3-4)}$$

$$A = 2eRkTN(E_F)\upsilon_{ph}\ ;\quad B = B_0\left\{\frac{\alpha^3}{kN(E_F)}\right\}^{1/4}\quad ;B_0 = 2\left(\frac{3}{2\pi}\right)^{1/4}$$

However, if eRF is much smaller than kT in a weak electric field, we can approximate the relation as $\sinh(\frac{eRF}{kT}) \Rightarrow \frac{eRF}{kT}$, and the function of VRH can described by the simplification equation. This simplification Mott VRH equation as shown by Eq. (3-5).

20 http://people.math.gatech.edu/~jeanbel/TalksE/mott09.pdf

$$J = A'\exp(-BT^{-1/4}) \text{ .....(3-5)}$$

Moreover, with the calculation of Origin software, we can obtain the value of (eRE/kt) with the hyperbolic sine fitting curve. Also, the hopping distance is calculated by the fitting value, and the relationship between this value and hopping distance is shown by Eq. (3-6).

$$\frac{eRF}{kT} = \frac{eRV}{kTd} = CV \text{ ......(3-6)}$$

The typical VRH electrical curve is shown in figure 3-13. The VRH electric characteristic appears both in LRS and HRS of RRAM electrical transportation mechanism. In several researches[20,29] of gradation oxidation systems, for example of WO_x-based RRAM, the week metal oxide film shows gradation WO_x system and the electron transportation characteristic follows the Mott VRH mechanism.

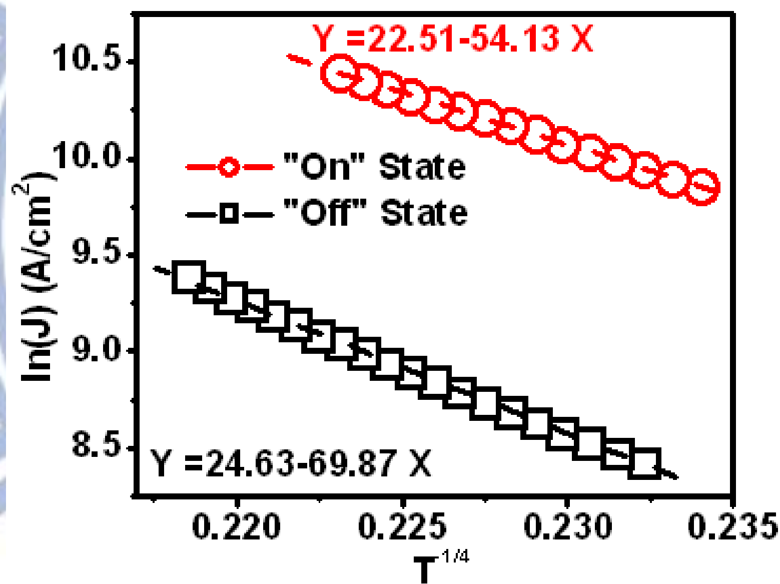

Figure 3-13. The electrical curve of Mott variable range hopping (VRH).

3.2.5 SCLC mechanism

Another electron transportation mechanism of RRAM is the SCLC[46]. This mechanism occurs before the charge injection when the charges accumulate at the interface and form a space charge cloud near the injecting electrode. The concentration of space charges rapidly dies out away from the electrode. The band diagram of the SCLC is shown in figure 3-14.

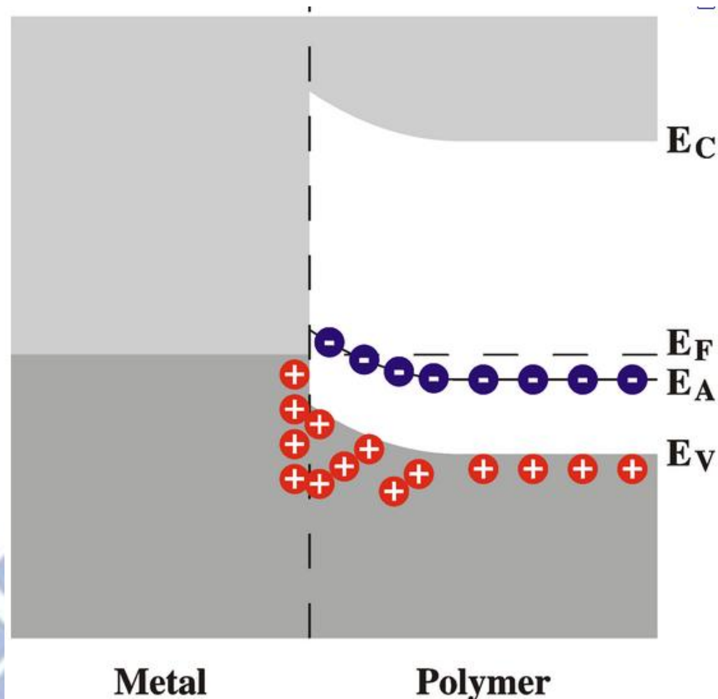

Figure 3-14. The band diagram of SCLC mechanism[21].

The SCLC transportation mechanism shows that the current proportionally increase with the square of the electric field relationship in electrical characteristic, which can be described by equation (3-7). Here, μ is mobility, and d is the thickness.

$$J = \frac{9\varepsilon_i \mu V^2}{8d^3} \quad \text{.....(3-7)}$$

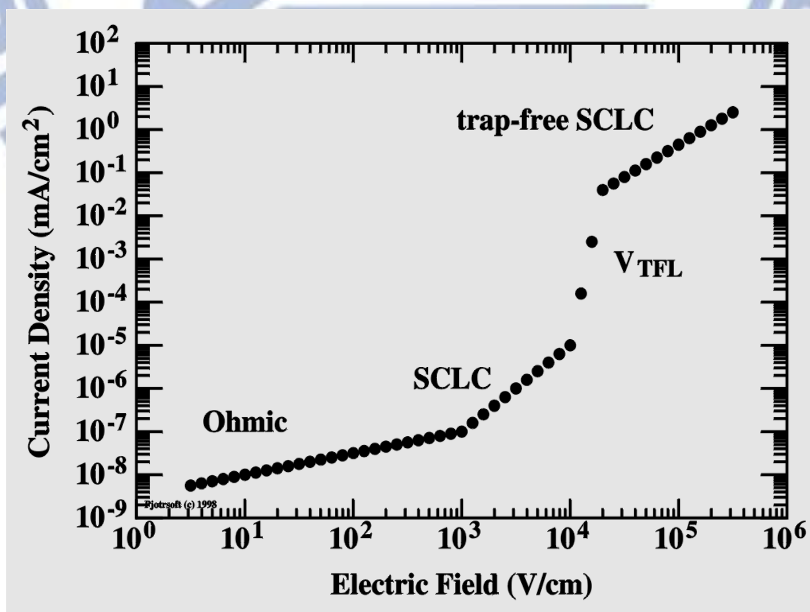

Figure 3-15. The electrical curve of SCLC[xxiv].

[21] http://ceot.ualg.pt/OptoEl/theory/2terminal/

Figure 3-15 shows the electrical characteristic of SCLC. This figure shows the linear I-V curve with metal ohm contact behavior when the applied electric field is below 1000 V/cm. Also, the electric characteristic displays the SCLC behavior when the applied electric field is between 1000 and 10000 V/cm. When the electric field applied is above 10000 V/cm, the electron transportation mechanism exchanges to another transportation mechanism, which is not discussed in this section. Similar to the band diagram of Schottky emission mechanism, the SCLC transportation mechanism of RRAM is attributed to the charge concentration near the injecting electrode with the metal-insulator interface. Moreover, the SCLC appears both in LRS and HRS in the RRAM transportation mechanism.

3.2.6 The TAT Mechanism

In the semiconductor technology, it is generally accepted that the origin of the stress induced leakage current (SILC) and the increase of the resulting gate current at low voltage in stress devices is resulted from the TAT mechanism. Such an electron transportation characteristic is also shown in previous report[50] of RRAM researches. Figure 3-16 shows the band diagram of TAT. This figure also shows the direct tunneling (DT) characteristic. It is obvious to see the difference between DT and TAT in this band diagram. The TAT phenomenon in insulator is attributed to the tunneling characteristic with charge trap influence, and it is divided into elastic and inelastic TAT phenomena (not discussed here).

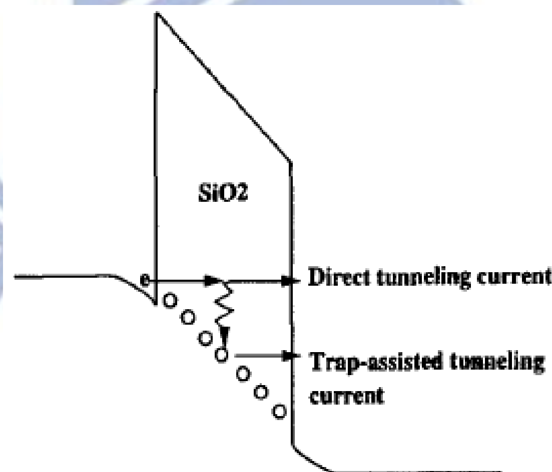

Figure 3-16. The band diagram of TAT mechanism[22].

Figure 3-17 shows the TAT electric characteristic in MOS device. The TAT mechanism also appears in the RRAM transportation characteristic. Figure 3-18 shows the TAT characteristic of RRAM[63]. The electric characteristic of metal-insulator-metal

[22] J. Wu, L. F. Register, and E. Rosenbaum, Annual International Reliability Physics Symposium, 389, (1999)

(MIM) structure combines with both TAT and DT curves, and it shows the similar SILC electric characteristic in the electric analysis. Moreover, the TAT mechanism always appears in the HRS.

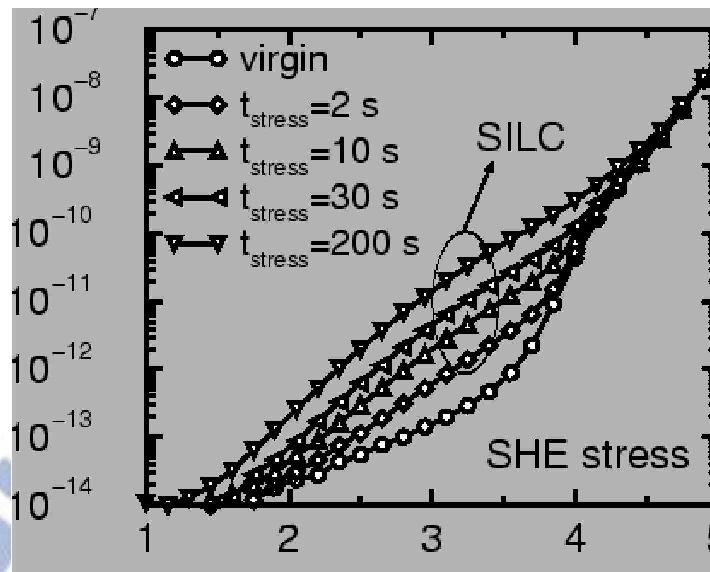

Figure 3-17. The electrical curve of TAT in MOS device[23].

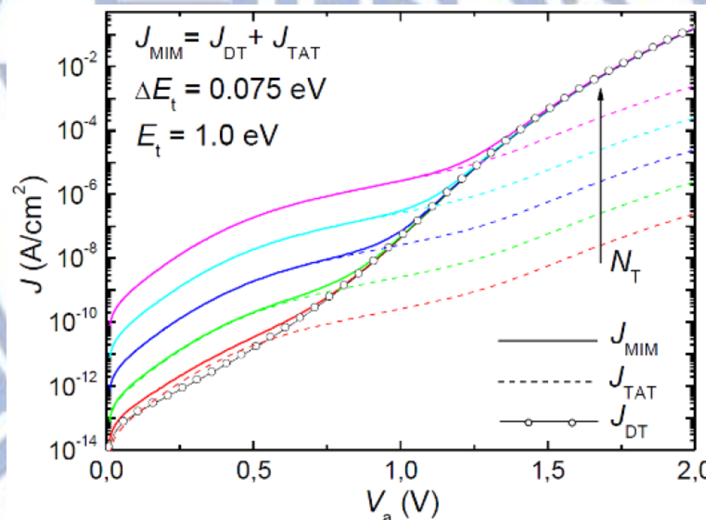

Figure 3-18. The electrical curve of TAT in RRAM.

In summary, most electron transportation mechanisms such as Poole-Frenkel emission, electron hopping transportation, and TAT mechanisms show the charge trapping phenomenon in the oxidation layer. This result indicates the oxide film of RRAM with imperfect insulator performance, and it could be attributed to the presence of defects. Most references correlated these defects with the oxygen vacancies, which provide the charge trapping. Also, these oxygen vacancies play an important role in the resistance switching characteristic.

[23] http://www.diegm.uniud.it/driussi/biografia/dottorato/node47.html

3.3 Resistance Switching Mechanisms

In recent years, there are many studies[64-74] proposed the resistive switching mechanism. Although the resistance switching theories in these reports show several different resistance switching mechanisms, most researches[51,54,55,75] reported that the oxygen vacancy in the oxidate film plays an important role in the resistance switching phenomenon. The electric characteristic exhibits the filament characteristic while the electrons pass through these oxygen vacancies. In this section, we discuss the conducting filament (CF) characteristic and the oxygen vacancy phenomenon for the explanation of resistance switching phenomenon in RRAM.

3.3.1 The Conducting Filament Characteristic

In the early research of RRAM, the resistance switching phenomenon of RRAM is attributed to the CF characteristic. Ryoo and Oh et al. [51] proposed that the filament mechanism of resistive switching characteristics. The electric characteristic exhibits a CF formed and ruptured behavior in the resistance switching process. Figure 3-19 shows the sketch of both set and reset processes. As shown in figure 3-19 (a), the CF was ruptured near the top-electrode region and the resistance state changes from LRS to HRS in the reset process. Also shown in figure 3-19(b), the CF formed and the resistance state recovered from HRS to LRS in set process. The CF model can be used to explain the resistive switching characteristic.

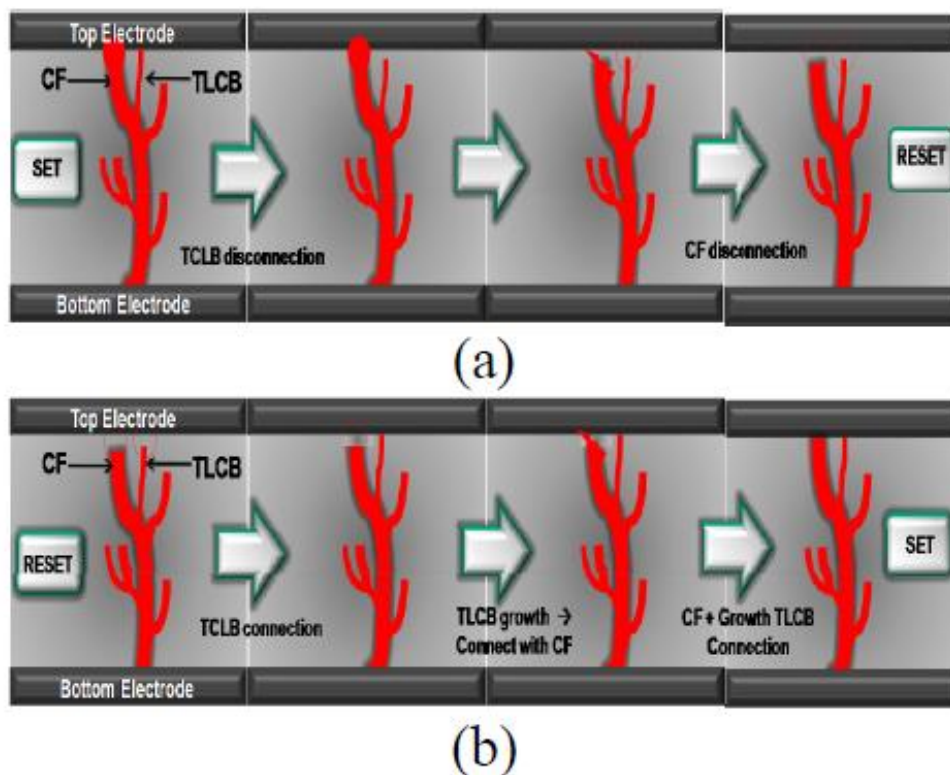

Figure 3-19. Sketch of (a) reset process (from LRS to HRS) and
(b) set process (from HRS to LRS)

Another study[52] also indicates the CF characteristic in their research. By means of the electron-beam-induced current (EBIC) image, we can clearly observe the CF image on the surface of oxide film and it shows the real CF image of the oxidation film. Figure 3-20 shows both EBIC image and I-V characteristic. Moreover, it also indicates the relation between these two factors. At the “initial” state, the resistance state is located at HRS, which is shown in figure 3-20 (a). When a negative voltage is applied, the resistance state switches from HRS to LRS, and the EBIC image observes several additional spots in figure 3-20 (b). Also, figure 3-20 (c) shows that several spots disappear in EBIC image when the resistance state switches back to HRS with a positive applied voltage. Figure 3-20 (d) shows more spots appear when the resistance state switches to LRS with another negative applied voltage. These spots of EBIC images indicate the existence of CF, and it also can be used to explain the resistance switching characteristics.

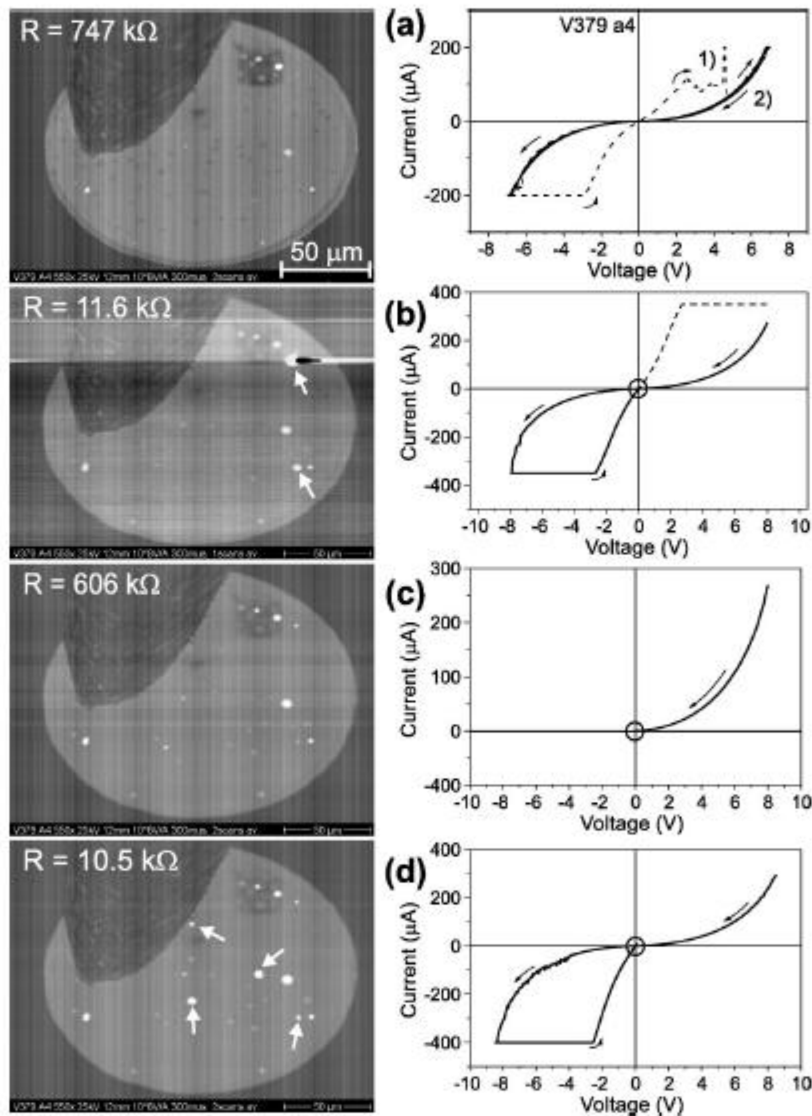

Figure 3-20. Sequence of EBIC image[52] and I-V characteristic (a) Initial state (b) Switch to LRS (c) Back to HRS (d) sweep to LRS.

Another image of CF can be observed with the conducting atom force microscopy (CAFM) system[53]. Figure 3-21 shows the CAFM image of ON and OFF state. It is clear to see the difference in both resistance states. Figure 3-21 (a) shows the CAFM image on HRS, and there are a few spots on the surface of oxidation film. It indicates that there are a few conducting channels in this oxide film. Also, the CAFM image of LRS shows many spots on the surface of oxidation film, which is shown in figure 3-21 (b). It indicates that there are many conducting channels in the oxide film.

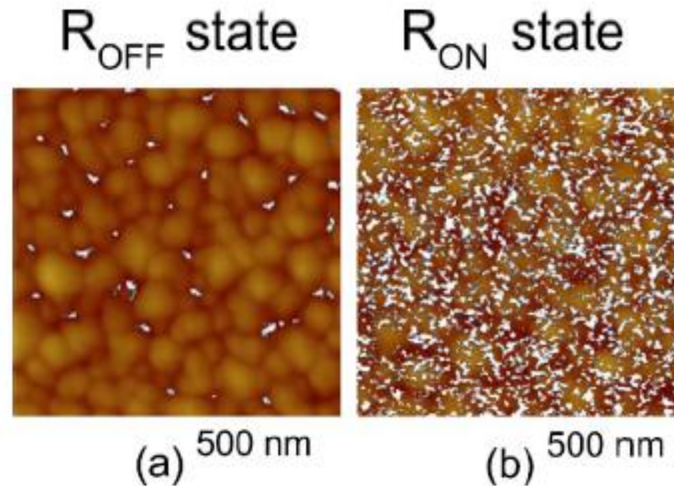

Figure 3-21. The conducting atom force microscopy (CAFM) of ON and OFF states[53].

3.3.2 The Oxygen Vacancy Phenomenon

In previous section, we discuss the CF theory for the resistance switching characteristic of RRAM. However, this theory can't explain the root cause of the resistance switching characteristics. It just depicts the phenomenon of resistance switching characteristics. In this section, we discuss delineate another theory to explain the resistance switching characteristic. This theory also illustrates the influence of resistance switching due to physical factors.

Gao proposed a unified physical theory for bipolar oxide-based resistive switching memory[54]. His study indicates that the oxygen vacancies can be generated by ionizing the oxygen atoms in lattice under a voltage bias. Xu et al.[55] also proposed that the oxygen vacancies and non-lattice oxygen ions play a critical role in the resistive switching device. Figure 3-22 shows the sketch of the carrier transport in both HRS and LRS.

In the set process, the oxygen ions are moved out from the lattice, and the oxygen vacancies appear at the same time. Also, the resistance state is switched from HRS to LRS because these oxygen vacancies appear in this resistance switching process. Figure 3-22 (a) shows the electron transportation in LRS. In this figure, the CF is formed by localized Vo and the conduction transportation is mainly due to electron hopping

transport among these Vo. Moreover, the charge-free of localized Vo^+ exhibits longer hopping distance than Vo.

In the reset process, the oxygen ions are recombined with electrons and the oxygen vacancies disappear. At the same time, resistance state is switched back to HRS. Figure 3-22 (b) shows the electron transportation in HRS. In this figure, the CF is ruptured by recombination of oxygen ions and the diminish of oxygen vacancies at the moment. The electrons can't conduct with hopping transportation due to the recombined oxygen ions. Since the hopping channel is destroyed, the electric characteristic switched to HRS.

By means of the theory of oxygen vacancy, we can explain the mechanism of resistive switching character. Combined with the CF theory, it can give readers much clear pictures in the RRAM film.

In summary, these theories can explain the bipolar operation resistance switching mechanism. But the unipolar operation resistance switching mechanism is still missing. Most references attribute the root cause of unipolar RRAM to the Joule heating effect. The research of unipolar operation resistance switching mechanism is still required.

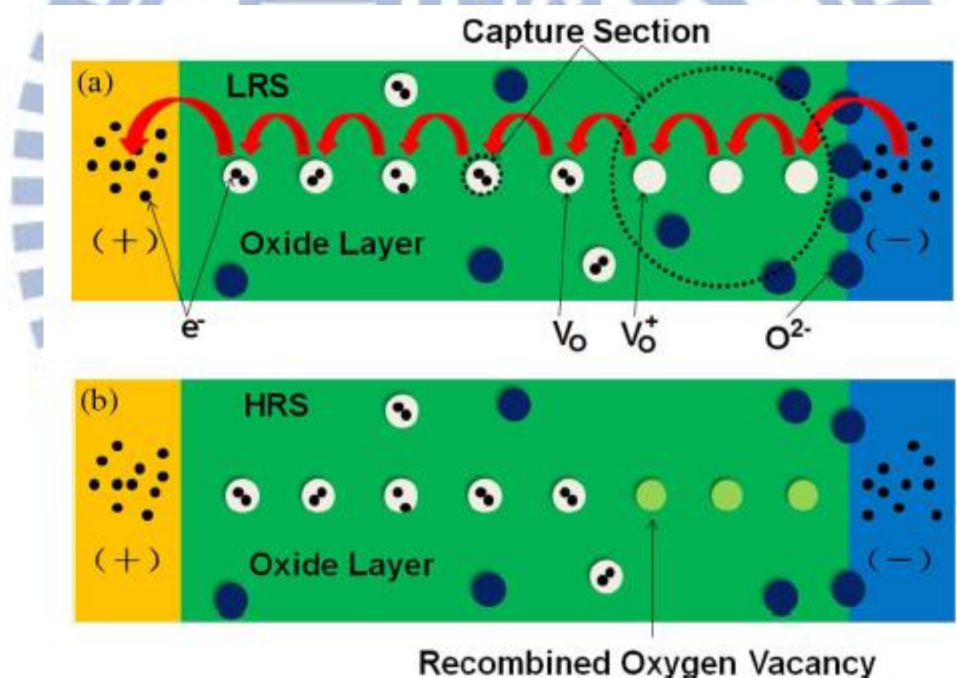

Figure 3-22. Schematic illustration of conduction transport in (a) LRS (b) HRS.

3.4 Resistance Switching Model

In recent years, many resistance switching models for RRAM has been proposed. These models are as follows: The stochastic model[56], two-variable resistor model[46,57], compact model[58], rupture ball model[38], thermal dissolution model[48,59], filament anodization model[76], numerical model[77] etc. In below, these models and discussed briefly.

3.4.1 The "Rupture Ball" Model

This model[38] is a blend of CF theory and oxygen vacancy theory. The electron transportation depends on the oxygen vacancy and the electric characteristic displays a CF phenomenon. Based on the results of previous researches, this model explains the relationship among "forming", "set", "reset", and "degradation" process. Figure 3-23 illustrates the schematic diagram of RRAM in above processes.

During the "forming" step, voltage is applied to the whole dielectrics as illustrated by figure 3-23 (b). After this process, the CFs can be formed by sufficient voltage. When further stress is applied to induce the "reset" process, CFs are ruptured by thermal effect depending on the applied power as illustrates by figure 3-23 (c). This "set" process resulting in the growth of Cfs as shown in figure 3-23 (d). However, with a continuous increase of the "reset" current, most of CFs can be destroyed due to the increased "reset" current, resulting in lowered current level as shown in figure 3-23 (e). These phenomena might cause irreversible degradation of dielectric films in the "over reset" process.

In this "rupture ball" model, it is shown that CFs are formed by the aggregation of oxygen vacancies through the "set" process. Also, the CFs are ruptured by deaggregation of oxygen vacancies through the "reset" process. In other words, the "rupture ball" might be formed by thermal diffusion of oxygen vacancies through the "reset" process, and the "rupture ball" might be destroyed with the diffusion of oxygen vacancies through the "set" process.

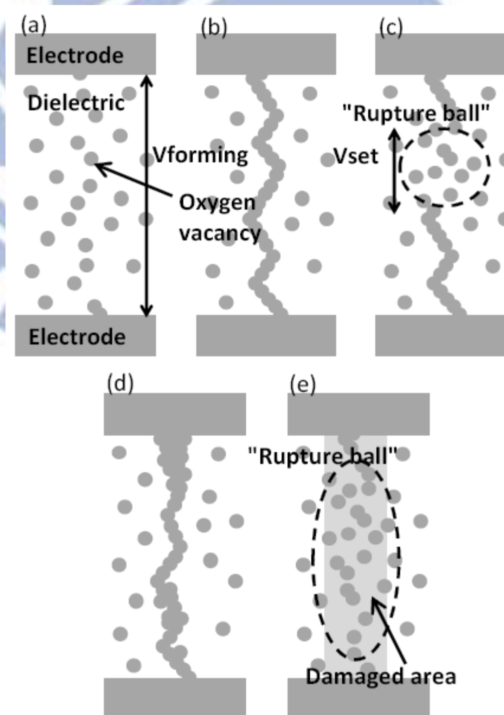

Figure 3-23. Schematic diagram[38] of dielectric status of RRAM at (a) fresh (b) after "forming" process, and (c) after "reset" process (d) after "set" process, and (e) after "over reset" process, respectively.

3.4.2 The Stochastic Model

In the stochastic model[56], the modeling of set/reset transitions is addressed by a statistical framework. The stochastic model for set and reset processes is developed by defining the probabilities for the cell to be in a set or reset state as P_{set} and P_{reset}, respectively. Assuming a Poisson statistics for set/reset, the time variation of P_{set} can be expressed by Eq. (3-8) where the average transition times are τ_{set} and τ_{reset} for set and reset, respectively.

$$\frac{dP_{set}}{dt} = -\frac{P_{set}}{\tau_{reset}} + \frac{P_{reset}}{\tau_{set}} \quad \text{.......(3-8)}$$

$$P_{set} = \frac{\tau_0}{\tau_{set}}\left(1 + \frac{\tau_{set}}{\tau_{reset}} e^{-\frac{t}{\tau_0}}\right), \quad P_{reset} = \frac{\tau_0}{\tau_{reset}}\left(1 - e^{-\frac{t}{\tau_0}}\right) \quad \text{.......(3-9)}$$

Solving equation (3-8) with condition $P_{set} + P_{reset}=1$, one obtains equation (3-9) with a characteristic transition time[56] $\tau_0 = \tau_{set}\tau_{reset} / (\tau_{set} + \tau_{reset})$. By defining the sweep rate $\beta = dV_{cell}/dt$, where V_{cell} is the voltage across the RRAM cell, the stochastic model calculates the set/reset time as shown in figure 3-24.

Figure 3-24 (a) shows the relationship between β and set/reset voltage. The “reset” voltage is smaller than the “set” one for small β. On the other hand, the set voltage is smaller than the reset one when the sweep rate is above 10^7 Vs^{-1}. In this case, the reset voltage increases quickly and it is ease to destroy the memory cell in the transition process. Figure 3-24 (b) shows the relationship between set/reset transition time and voltages. The crossover of τ_{set} and τ_{reset} is about 200 ns and V_{cell} is about 2.2 V. In this figure, the reset voltage shows sudden change when the transition time is below 200 ns. Also, the set voltage shows the characteristic of slow increasing characteristic when both β and transition times increased.

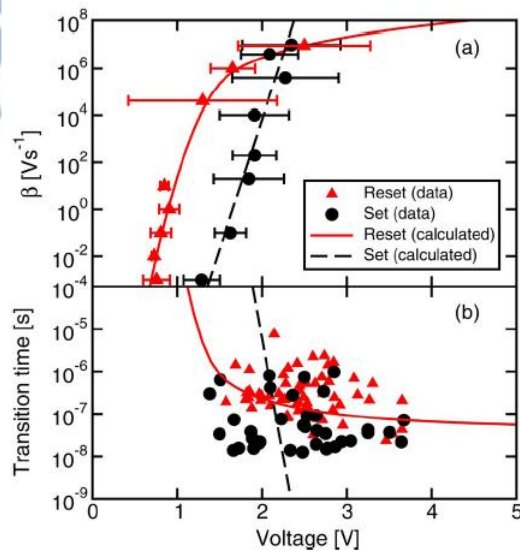

Figure 3-24. Measured and calculated relationships[56] of NiO film between the set/reset voltage and (a) the sweep rate or (b) the set/reset transition times.

To clarify the conditions for stable set/reset transitions, figure 3-25 shows the calculated I-V curves in set and reset states. Here, the reference assumes ohmic conduction with resistances from 1 to 50 kΩ for set and reset states, respectively. This curve shows the correspondence to the transition time according to the simulation results in figure 3-24. The dashing lines indicate the transition process at the same transition time. For example, at 100 ns transition time (open triangles), the reset voltage is smaller than the set voltage. It indicates that the probability of reset process is smaller than set process at 100 ns. On the other hand, at 10 us transition time (open squares), the set voltage is smaller than the reset voltage. It indicates that the probability of set process is smaller than reset process at 10 us.

In summary, it is shown that stable reset and set processes can take place above and below 200 ns, respectively.

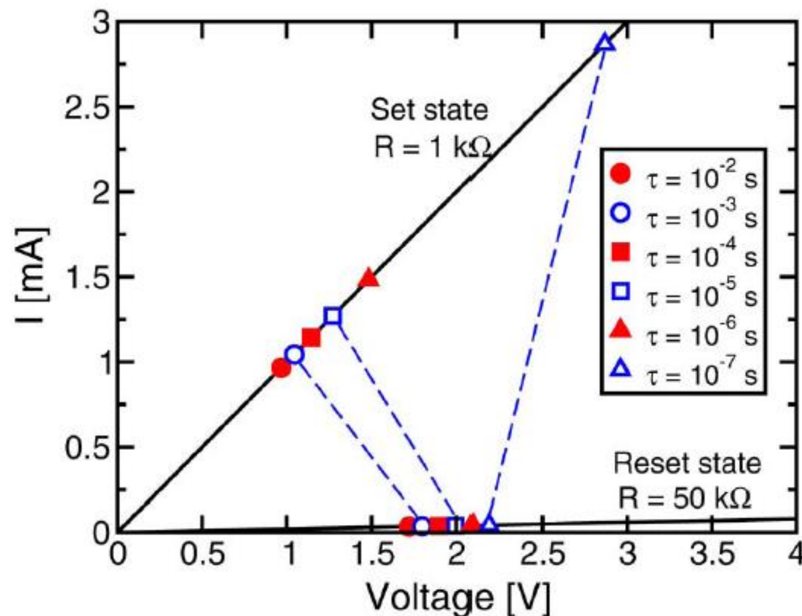

Figure 3-25. Calculated I-V curves for set and reset states[56]. The dashed lines connect transition point at equal transition times on two curves.

3.4.3 The Thermal Dissolution Model

The thermal dissolution model[48,59] is based on the CF theory and it can be used to explain resistance switching characteristic in the “reset” process. Figure 3-26 (a) shows the I-V curve of the CF based RRAM. It shows the characteristics of resistance increase when the applied voltage is increased. This result indicates the heating effect of the CFs. As shown in the inset in the figure, the temperature dependent relationship with resistance indicates the metals or doped semiconductors behavior. Moreover, Eq. (3-10) can be developed by this electric character. In this equation, the value of α is about 1.7×10^{-3}.

$$R(T) = R_0[1 + \alpha(T - T_0)] \ldots\ldots(3\text{-}10)$$

According to this equation, the resistance can be used as a thermometer for CF and can also be used to calculate the maximum temperature. Figure 3-26 (b) shows the relation between the temperature and the applied voltage. From this figure, the temperature increases with the increasing applied voltage. The critical temperature T_{crit} is about 550 K when reset process occurs.

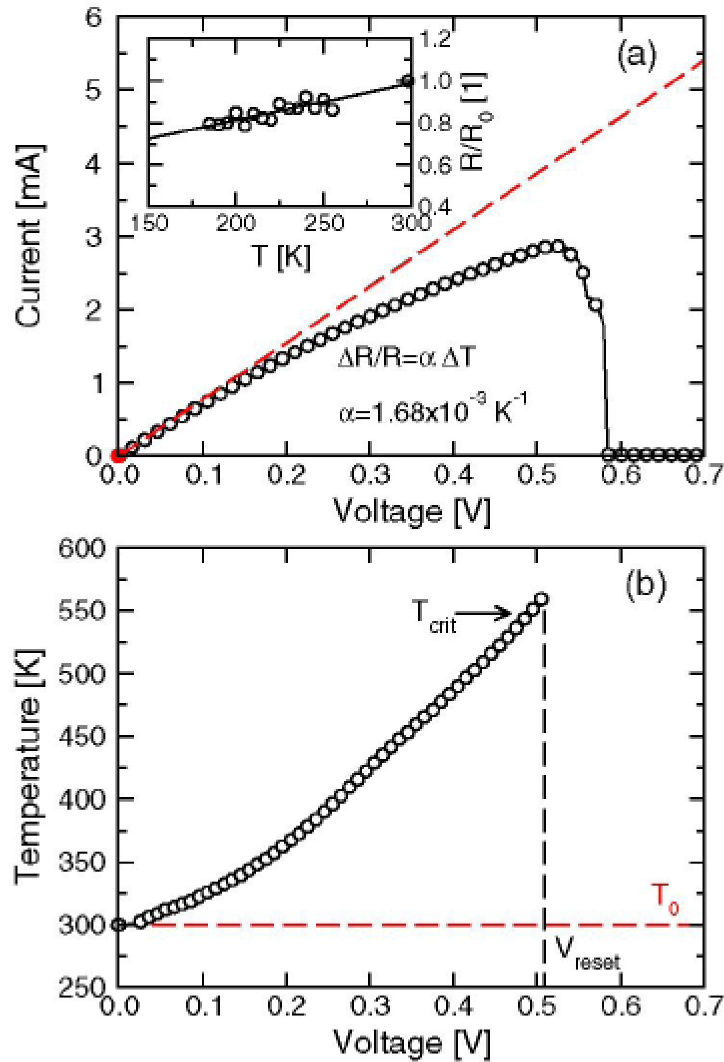

Figure 3-26. (a) The reset switching I-V curve and the temperature dependence relationship with resistance (inner) (b) Temperature has been evaluated from I-V curve[48].

Figure 3-27 shows the measured and calculated I-V curve during the reset process. Points A, B, C, and D correspond to the simulation results in figure 3-28, which is in the left region of CF. When the voltage is applied to the cell, a current flow will go through it, causing the CF temperature to increase as a consequence of Joule-heating. For a symmetric CF system, the temperature will be equal to room temperature at cell

electrodes, and it will reach a maximum temperature in the middle of the filament. In figure 3-27, points A and B show the I-V curve of cell without resistance switching phenomenon. Also, the first two pictures of figure 3-28 show the temperature relationship of these two points. Besides, point C shows the resistance switching phenomenon, and the third picture of figure 3-28 shows the simulation result of thermal dissolution. Finally, point D shows the HRS after the reset process, and the fourth picture of figure 3-28 shows the simulation result. It shows the CF is destroyed with the thermal dissolution and the temperature of this rupture CF is near the room temperature. The right picture of figure 3-28 shows the temperature profile along the symmetry axis in the cylindrical CF, representing the four bias points A-D in figure 3-27.

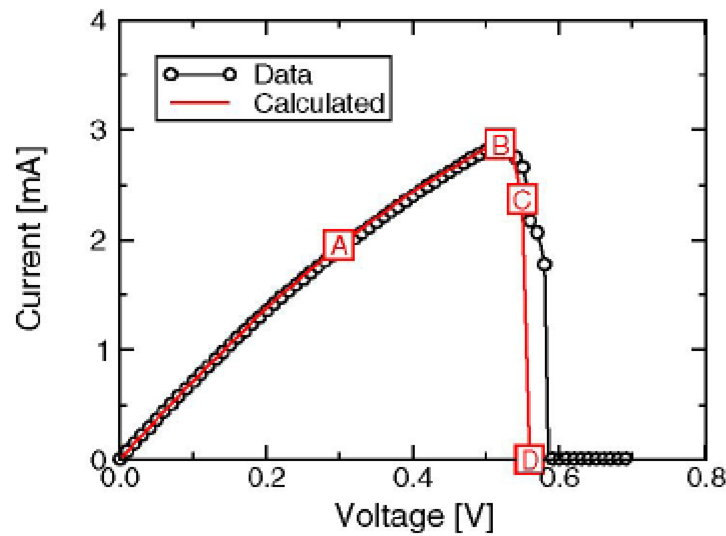

Figure 3-27. Measured and calculated I-V curve during reset process.

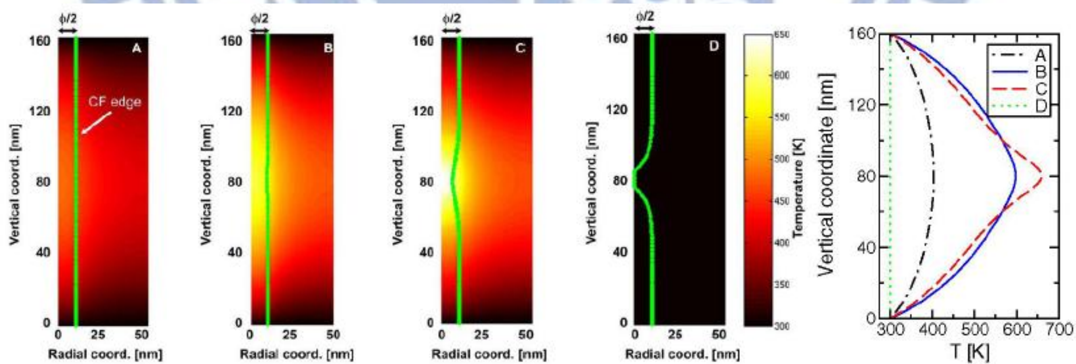

Figure 3-28. Simulation results for thermal dissolution of the CF[59]. The left four images show the four bias points A-D in figure 3-27 and the right image shows the temperature profile of A-D.

The thermal dissolution model indicates that the physical mechanisms underneath CF dissolution are diffusion of conductive particles or defects, resulting from the CF outward and their annealing or the reaction with other elements. This model can be used to explain the reset process of RRAM.

3.4.4 The Two-variable-resistor Model

The two-variable-resistor model[46,57] is based on the oxygen vacancy mechanism and can be used to explain the bipolar resistance switching. Figure 3-29 is the schematic illustration of this model. The structure of Al/TiO_x/Al is shown in the left part of figure 3-29 and this initial TiO_x film is in HRS (R_{off}). In this bipolar operation, the electrode β is ground, and the bias is applied to electrode α. The appearance of both positive and negative polarities of bias in this device can be understood if we use tow-variable-resistor model. The assumptions of this model are as follows. First, oxygen vacancies in TiO_x layer act as trap for electrons, and they are uniformly distributed in TiO_x layer. Second, the TiO_x layer is divided into two parts: a well conductive part (R_{on}) of thickness ω(t) and a less conductive part (R_{off}) of thickness D-ω(t). Third, the filled-trap region of TiO_x shows good conductivity (R_{on}). Finally, the unfilled-trap region of TiO_x shows poor conductivity (R_{off}). After applying bias, the total resistance of the TiO_x layer is determined by the two variable resistors in series, which consist of a low resistance resistor (R_{on}) and a high resistance resistor (R_{off}). Thus, the total resistance can be described by the following Eq. (3-11):

$$R_{total} = R_{on}\frac{\omega(t)}{D} + R_{off}\left(1-\frac{\omega(t)}{D}\right) \quad \text{.....(3-11)}$$

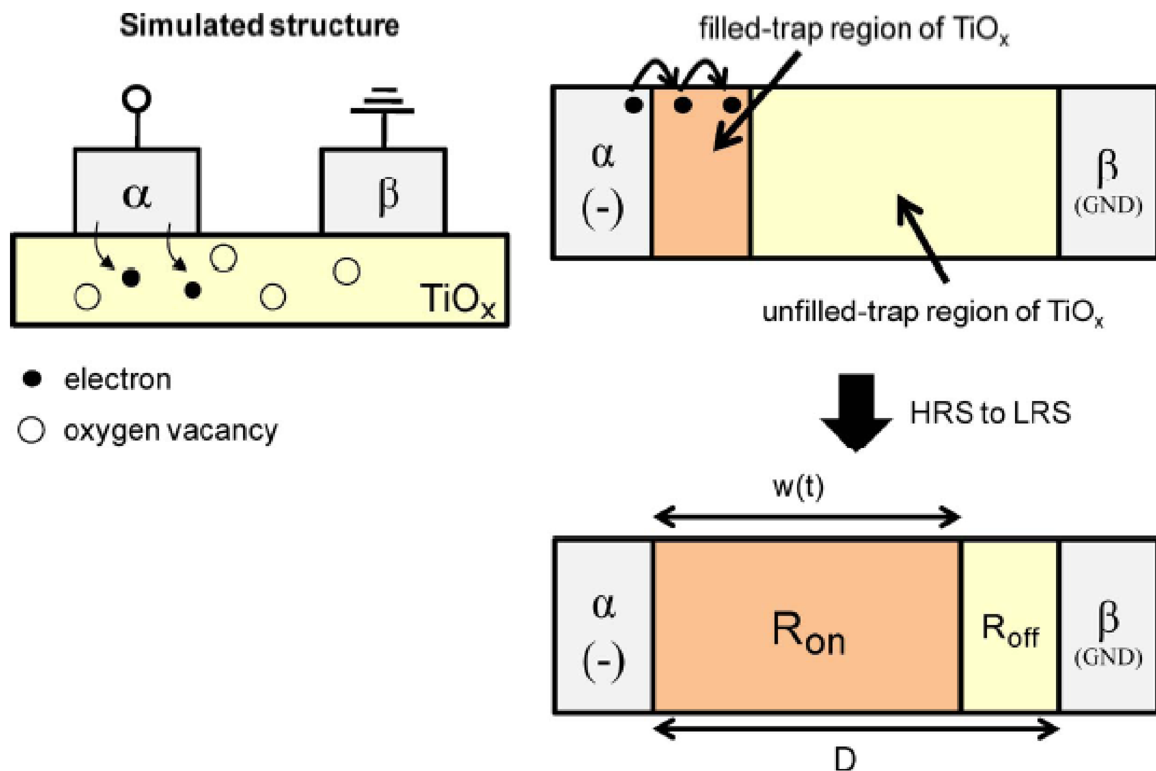

Figure 3-29. Schematics[57] to explain the resistive switching in the Al/TiO_x/Al structure considering the variation of the filled-trap region (R_{on}) of TiO_x by injected carrier.

In addition, D is the total thickness of TiO_x film. Moreover, the calculated I-V curve and the measured data of this device are shown in figure 3-30. It indicates that the result of calculated I-V curve is similar to the measured electric character.

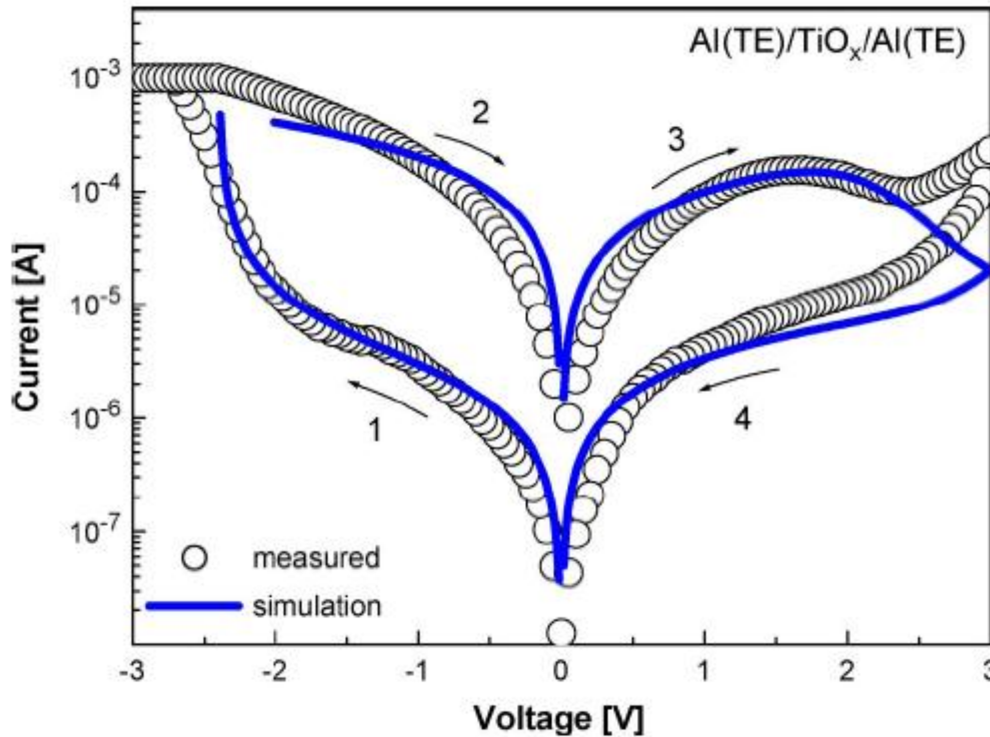

Figure 3-30. Calculated I-V curve of the $Al/TiO_x/Al$ device and the measured data[57].

In summary, the applying bias controls the filled-trap region of TiO_x film, and the electric character is dominated by this region. So, the two-variable-resistor model can be used to explain the phenomenon of the bipolar operation resistance switching of RRAM.

3.4.5 The Compact Model

The compact model[58] is based on the CF mechanism. That is, the resistive switching of RRAM is the formation and rupture of filament. In this model, the device of RRAM is divided into three parts: the series resistance of electrode (R_L), original resistance of resistive switching (RS) layer (R_H), and a resistive switching filament (R_f). Here, R_H is the maximum resistance and R_L is the minimum resistance. Figure 3-31 (a) shows the device scheme and figure 3-31 (b) shows the equivalent circuit of this RRAM device. The resistance of filament is based on its state ω, which can change from zero to infinity. The state is expressed by Eq. (3-12) and the resistance of filament is expressed by Eq. (3-13).

$$\omega = \omega_0 + f(I, V, t) \ \ldots.(3\text{-}12)$$

$$R_f = R_0 \omega^{1/b} \ldots\text{(3-13)}$$

Where ω_0 is original state, 1/b is saturation coefficient, and f(I,V,t) is function of current voltage and time influence on ω. Previous study[58] reported that the "set" process is controlled by current and the "reset" process is controlled by voltage. Hence the RS process could be represented as Eq. (3-14) and Eq. (3-15) in "set" and "reset" process, respectively. The R_0 and σ_0 are resistance coefficient, which is controlled by voltage or current on RS. The a_i and a_v are current, and voltage change parameters affect the RS speed. The *m* and ω are states of device.

$$1/R_f = \sigma_0 \omega^{1/b_i} \qquad \omega = \omega_0 + \int_{t2}^{t1} I(t)^{a_i}\, dt \ldots\text{(3-14)}$$

$$R_f = R_0 \omega^{1/b_v} \qquad m = m_0 + \int_{t2}^{t1} V(t)^{a_v}\, dt \ldots\text{(3-15)}$$

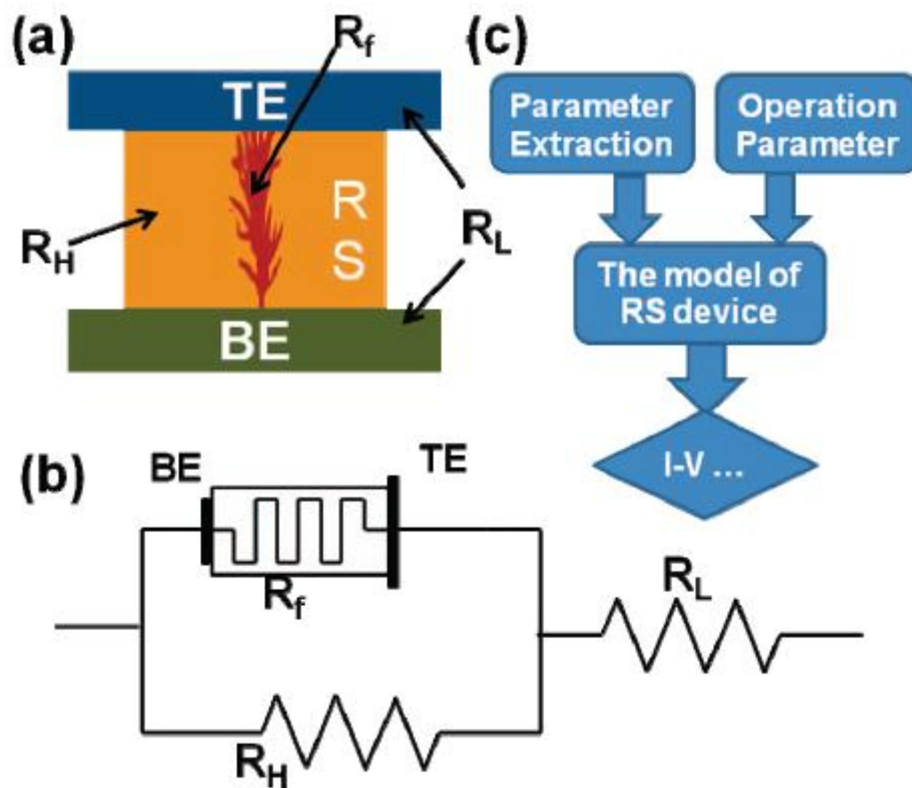

Figure 3-31. (a) the structure of RRAM and the filament is in the RS layer. (b) The equivalent circuit of RRAM device. (c) The flowchart of the model[58].

Figure 3-31 (c) shows the flowchart of the model parameter extraction, which can be used to obtain I-V curve and other behavior of the RS device. By using the Compact model, we obtain a typical I-V curve of bipolar RRAM, which is shown in figure 3-32. Another I-V curve of unipolar RRAM, which is shown in figure 3-33, can be obtained by using this model.

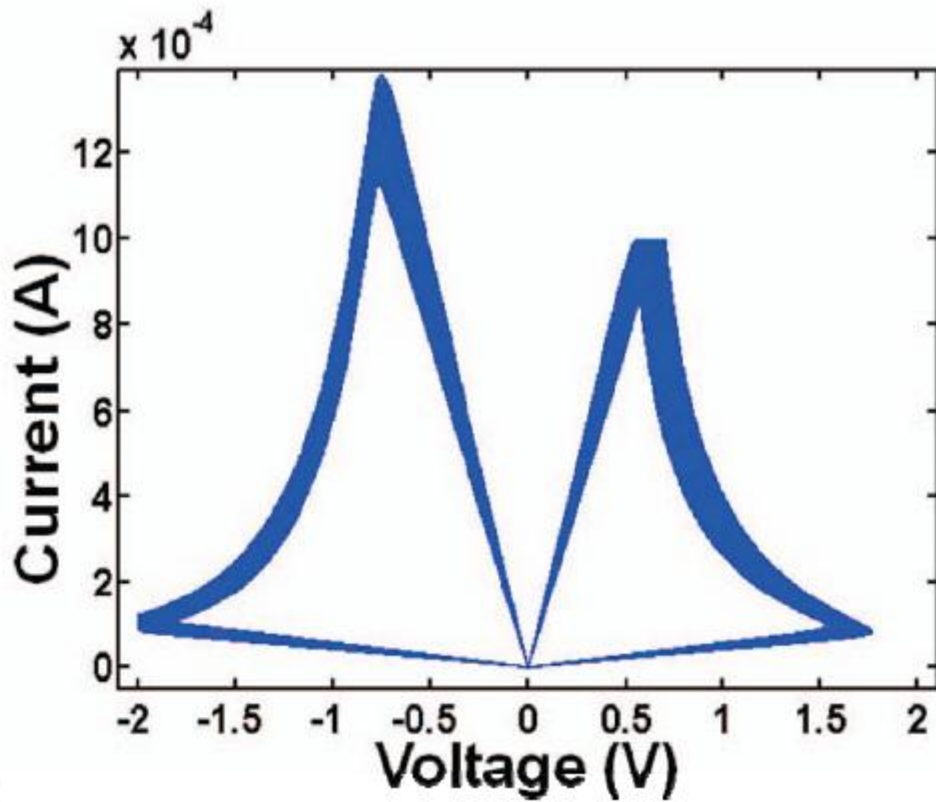

Figure 3-32. The simulated I-V curves of bipolar RRAM by compact model[58].

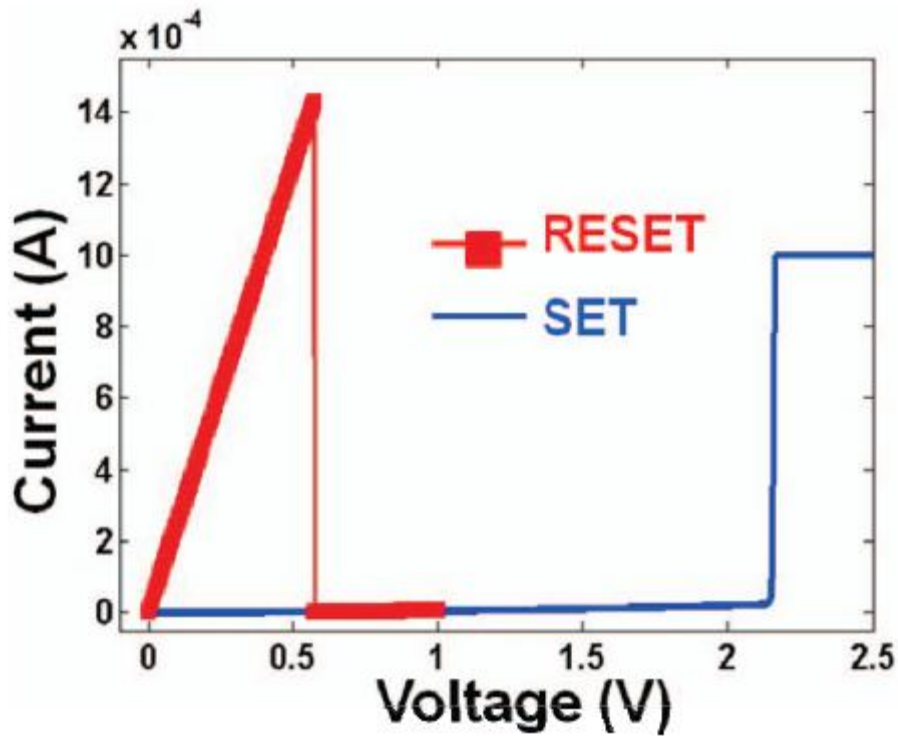

Figure 3-33. The simulated I-V curves of unipolar RRAM by compact model[58].

3.4.6 The Filament Anodization Model

Kinoshita[76] proposed a “filament anodization model” (FAM) for the resistance switching mechanism of RRAM. In his research, the anodic sides of filaments are anodized by the reset process, and the “set” process consisted of two steps. First, the dielectric breakdown (DB) occurs in the oxidation region of weakly anodized filaments. It means that some filaments are reconnected when DB occurs. Then, joule heating increases drastically and de-oxidizes neighboring filaments. From his experimental results, the weakly oxidation region of filaments plays an important role in resistance switching mechanism. The FAM model is described as follows. (1) In “forming” process, the top-electrode (TEL) and bottom-electrode (BEL) are connected by formed filaments, and the resistance state exhibits LRS. (2) In “reset” process, the edges of anodic sides of filaments are anodized, and the resistance exhibits HRS. (3) In “set” process, DB and joule heating cause reduction of filaments, and the resistance state returns to LRS. The schematic view of LRS and HRS is shown in figure 3-34, which can be used to explain the FAM model.

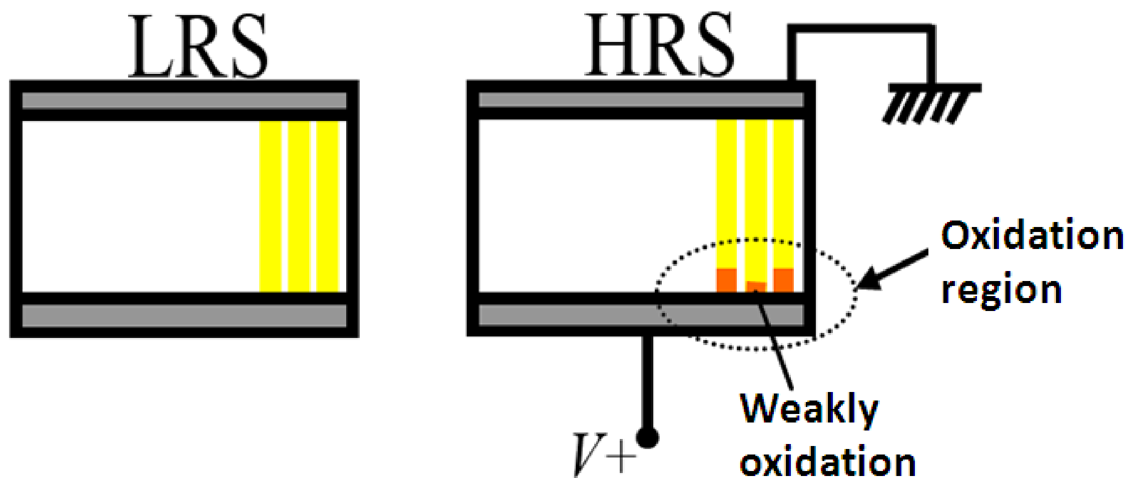

Figure 3-34. A schematic view of the condition of the filaments in LRS and HRS[76].

3.4.7 The Numerical Model

This model is based on the multiple states experiment of NiO RRAM[77]. In the multiple states experiment, the resistance states can be defined by multiple set/reset processes. Figure 3-35 shows the I-V curve of multiple “reset” process. In this figure, the first sweep is stopped at V_B about 0.65 V, and the resistance state is changed from R_A to R_B. A second sweep is applied to the R_B state and is interrupted at a slightly larger voltage V_C about 0.8 V. The resistance state is changed from R_B to R_C in this second sweep process. The third sweep is applied to the R_C state when the applied voltage is above V_C, and the resistance state is changed from R_C to HRS. In the numerical model, the multiple states can be interpreted as the result of a different size or composition of CF. Figure 3-36 is the schematic illustration of this model. Figure 3-36 (a) shows the

full set state, which corresponds to a metallic CF with relatively large diameter. Figure 3-36 (b) shows the partial reset state in a continuous CF with smaller diameter. Figure 3-36 (c) shows partial set state in a dispersed CF consisting of residual conductive elements. Finally, figure 3-36 (d) shows the full reset state, which consists of quasi-stoichiometric NiO with negligible concentration of localized states.

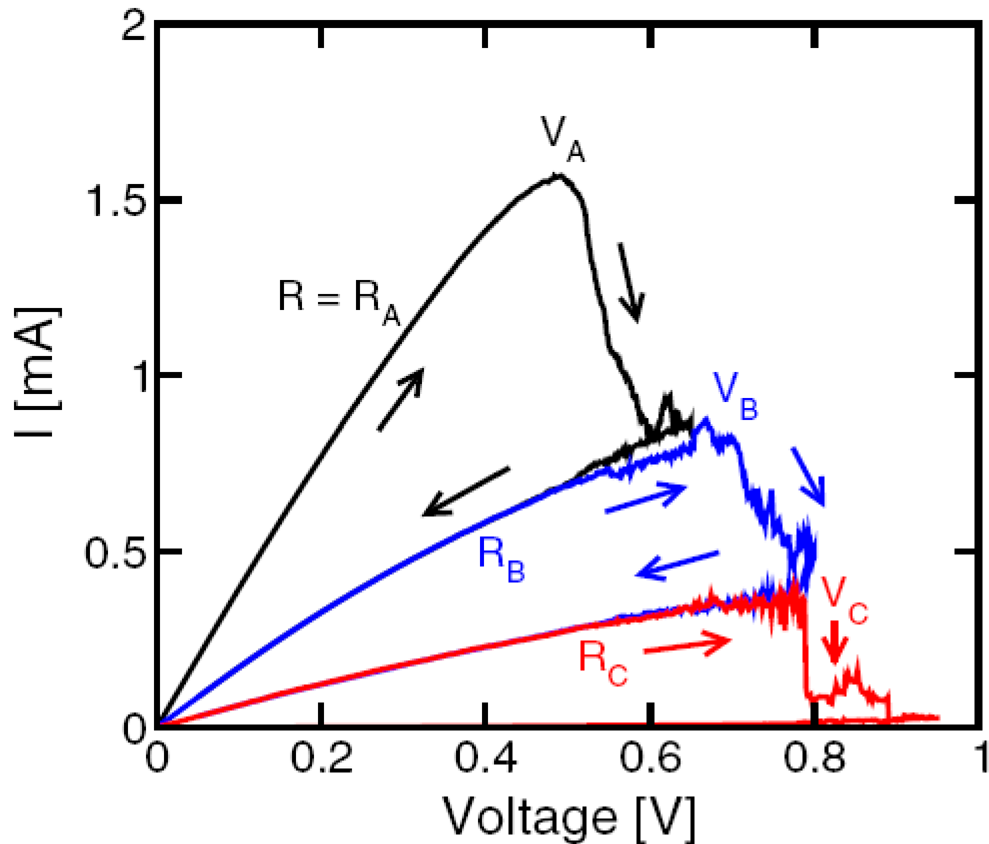

Figure 3-35. The I-V curve of multiple reset process[77].

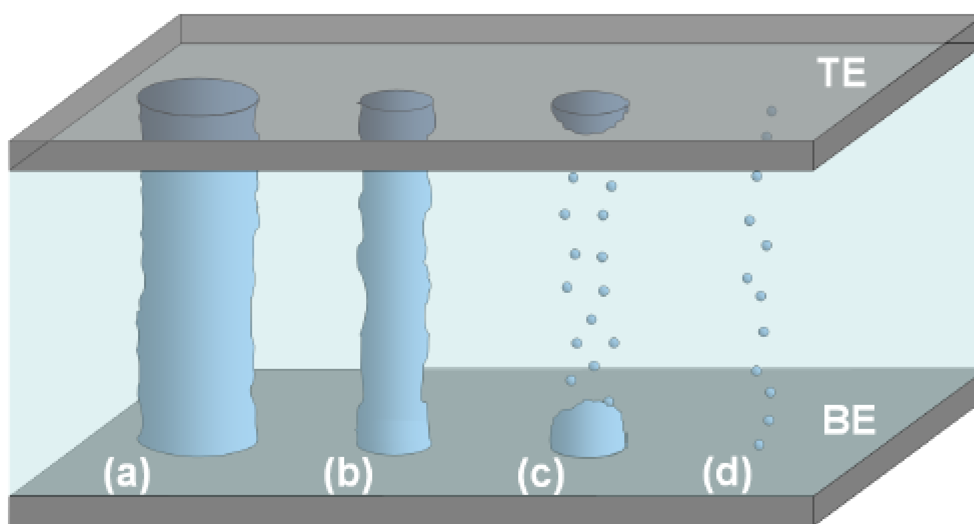

Figure 3-36. The schematic for multiple states[77]. (a) Full set state. (b) Intermediate state with small metallic CF. (c) Dispersed CF (d) Full reset state.

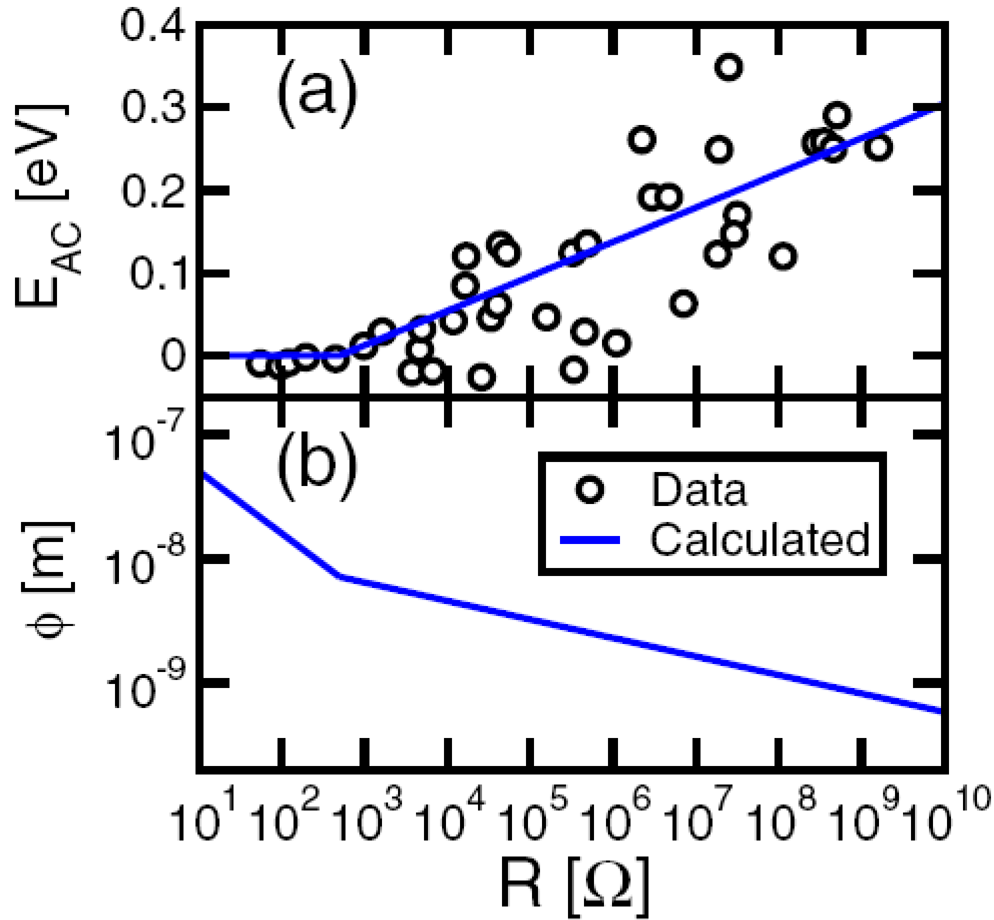

Figure 3-37. (a) The measured E_{AC} as function of resistance. (b) The calculated CF diameter as function of resistance.

From the slope of resistance in the Arrhenius plot, the activation energy (E_{AC}) can be collected for conduction. Figure 3-37 (a) shows the relation between E_{AC} and cell resistance. Moreover, the extracted E_{AC} can be applied to estimate the effective CF area A with the formula (3-16) :

$$R = \rho_0 \exp(\frac{E_{AC}}{kT}) \frac{t_{NiO}}{A} \quad \text{……(3-16)}$$

where k is the Boltzmann constant and ρ_0 is the pre-exponential constant for resistivity. The NiO layer thickness t_{NiO} is used to identify the CF length. Figure 3-37 (b) shows the relation between the CF diameter and the cell resistance.

In summary, the multiple states of RRAM depend on the diameter of CF. Different CF diameter exhibits different resistance state. With the calculation of equation (3-16), the diameter of CF can be obtained in this numerical model.

3.5 The Key Physical Parameters Influence RRAM Performance

In RRAM films, the temperature-dependence relation (with forming voltage, set voltage, reset voltage. etc) shows the domination of oxygen vacancy in the oxide film. The temperature-dependence relation can be attributed to the diffusion or migration of oxygen vacancies in oxidate film. First, the temperature-dependence characteristic is due to the movement of oxygen vacancies. Another temperature-independence characteristic is due to the drift of oxygen vacancies, and the resistance switching phenomenon shows the voltage-polarity-dependence characteristic. The temperature-dependence relation[78] in both HRS and LRS is shown in figure 3-38. Figure 3-38(a) shows the temperature-independence behavior in LRS and figure 3-38 (b) shows the temperature-dependence behavior in HRS. These results indicate that the electric characteristics are dominated by the diffusion and movement of oxygen vacancies, respectively.

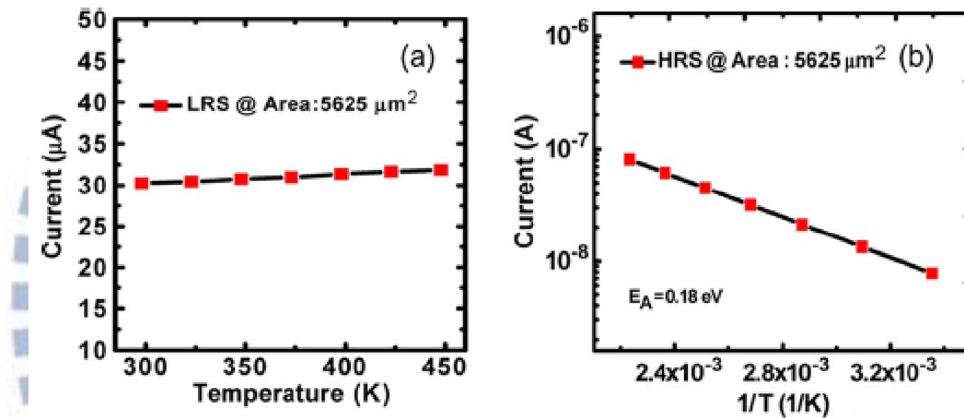

Figure 3-38. The temperature dependence relationship of (a) LRS (b) HRS.

Moreover, there are physics factors influence the resistance switching performance in RRAM. In this section, we discuss six physical parameters such as cell thickness, cell size, electrode, doping effect, density of oxygen vacancy, and electric field.

3.5.1 Thickness

In RRAM, the forming voltage shows the direction relationship with the cell thickness[38]. Figure 3-39 shows the “forming” and “set” voltage dependence on cell thickness. In this figure, the thinner the thickness is, the smaller the forming voltage will be. This result indicates that the thicker sample needs larger forming voltage to induce the resistance switching characteristics. However, the set voltage shows an independence relationship with cell thickness. Moreover, the “forming” voltage and “set” voltage could be the same value when the thickness is below 20 nm. It indicates that the forming free cell can be observed with thinner sample below 20 nm.

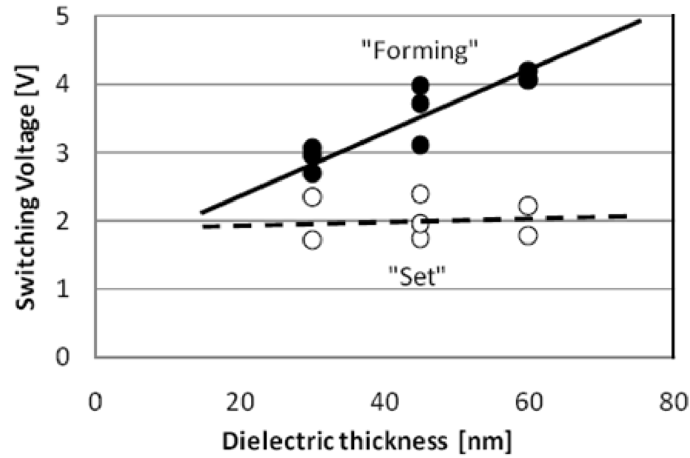

Figure 3-39. The “Forming” and “set” voltage dependence on TiO_2 thickness of $Pt/TiO_2/Pt$ RRAM.

3.5.2 Cell Size

The cell size (device area) is another parameter that affects RRAM performance. It can be understood in the HRS with the knowledge of physics. Due to the size effect, the HRS shows the direct relationship with device area. For plug structure, the smaller diameter sample shows larger resistance, and the larger diameter sample shows smaller resistance in HRS. This phenomenon is not clear in LRS. The relationship between device and resistance[39] is shown in figure 3-40 (a).

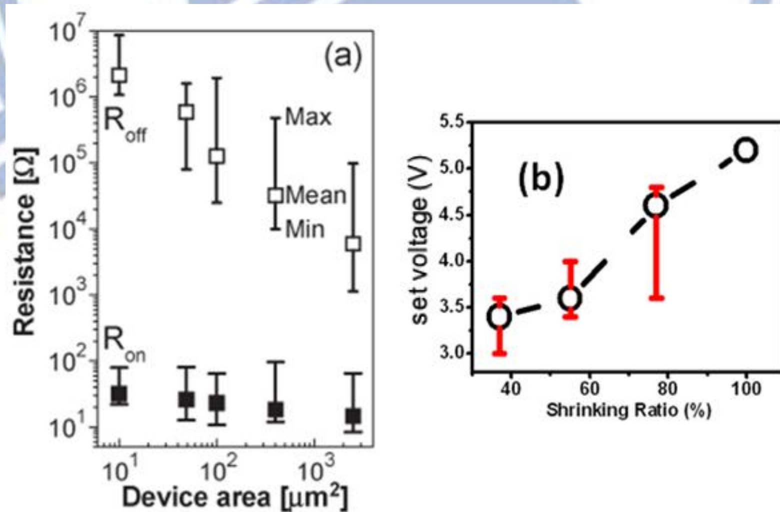

Figure 3-40. (a) The relationship between device area and resistance state. (b) The relationship between shrinking ratio and set voltage.

Moreover, this effect also influences the “set” voltage. In our research in tungsten based RRAM, the smaller area sample shows smaller “set” voltage. Figure 3-40 (b) shows the relationship between shrinking ratio and set voltage. It is clear to see the size effect in set voltage.

3.5.3 Electrode

Figure 3-41 shows the resistance characteristics of different cap layer in Pt/HfO_2/TiN system[41]. In this figure, it is clear to see that the resistance variation is large in HRS with different cap layers, yet the resistance variation of LRS is smaller than HRS. Also, the metal oxide cap layer sample shows higher resistance in HRS and the on/off ratio is larger than metal cap layer sample.

However, the sample with metal oxide cap layer doesn't show better on/off ratio with other electrode. Figure 3-42 shows the resistance characteristics of different cap layers in TiN/HfO_2/TiN system. In this figure, the resistance variation is still small in LRS and the HRS resistance becomes small in this system. Moreover, the on/off ratio data shows no difference in metal and metal oxide cap layer sample. These results indicate that the electrode plays an important role in the RRAM research, and this factor also influences the RRAM performance.

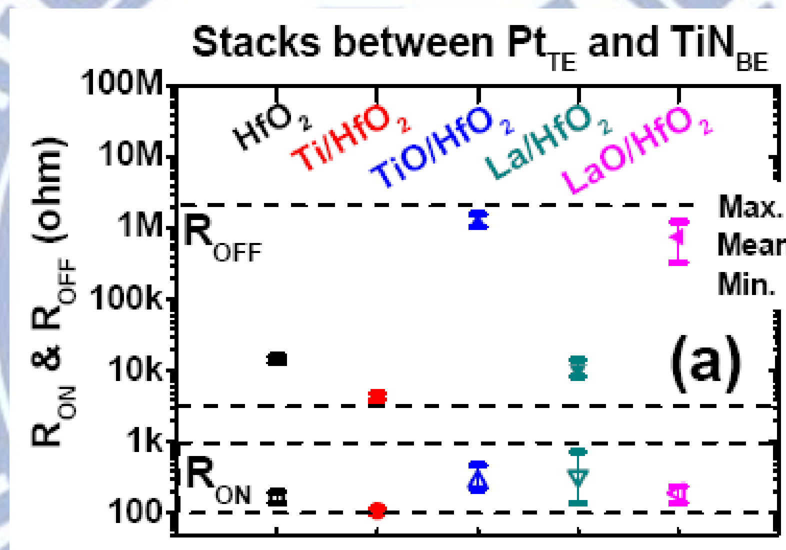

Figure 3-41. The resistance characteristics of different metal and metal oxide cap layers in Pt/HfO_2/TiN system.

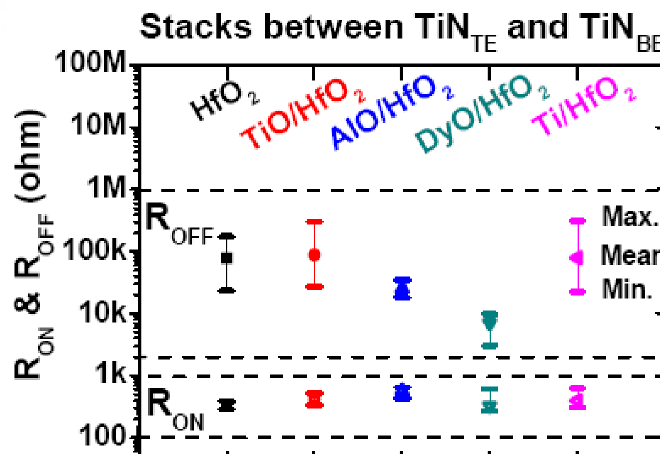

Figure 3-42. The resistance characteristics of different metal and metal oxide cap layers in TiN/HfO_2/TiN system.

3.5.4 Doping Effect

In the RRAM research, the doping effect also plays an important role in resistance switching behavior. Figure 3-43 shows the distribution of HRS in both doping and non-doping systems[40]. Figure 3-43 (a) shows the HRS distribution in non-doping system with different pulse width. The wide distribution of HRS can be clearly observed. However, the doping system shows better distribution in HRS. This result indicates the improvement of RRAM performance with the doping system.

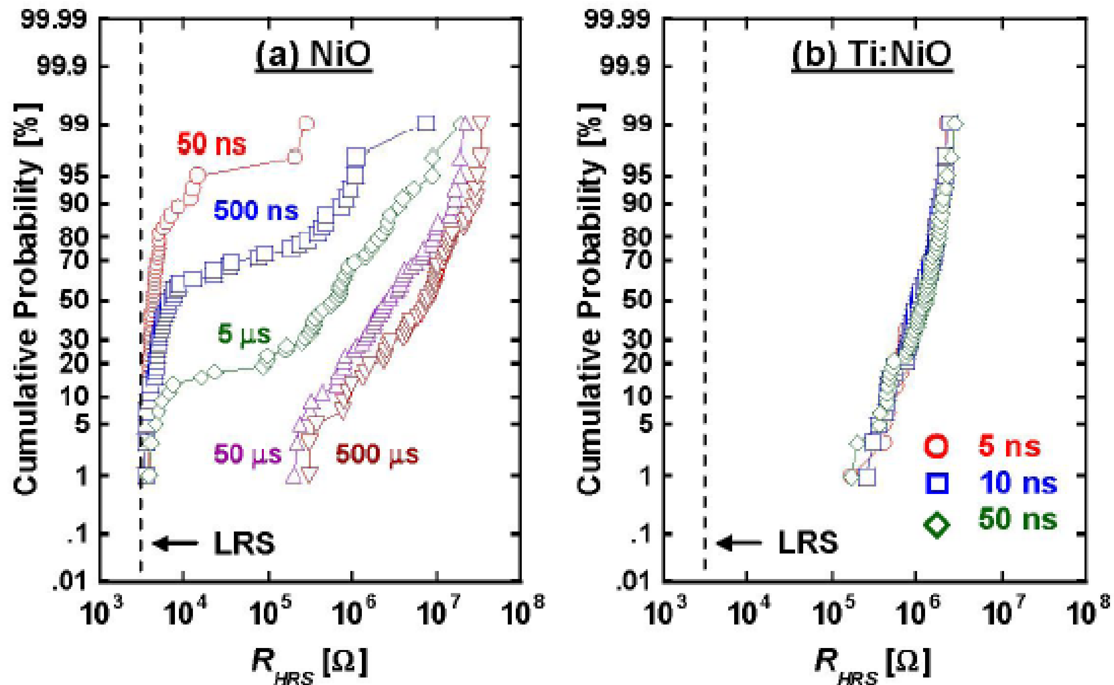

Figure 3-43. Distributions of the HRS in (a) NiO and (b) Ti:NiO as a function of the pulse width in the reset process.

3.5.5 Electric Field (Surrounding Environment and Dielectric Constant)

In RRAM, the resistance switching performance has much to do with the applied voltage. It also means that the electric field plays an important role in the resistance switching characteristics. Figure 3-44 shows of the influence of material surrounding environment on electric field[42]. The electric field enhancement structure is shown in the left region of figure 3-44. Also, the electric field distribution of 20 nm and 100 nm WO_x RRAM device is shown in the right region of this figure with the same applied voltage. In this figure, it is clear to see that the electric field of 20 nm device is higher than 100nm device. The forming voltage also shows the decreasing relation with the device cell in this experiment. This result indicates the electric field in RRAM material directly influences the RRAM performance.

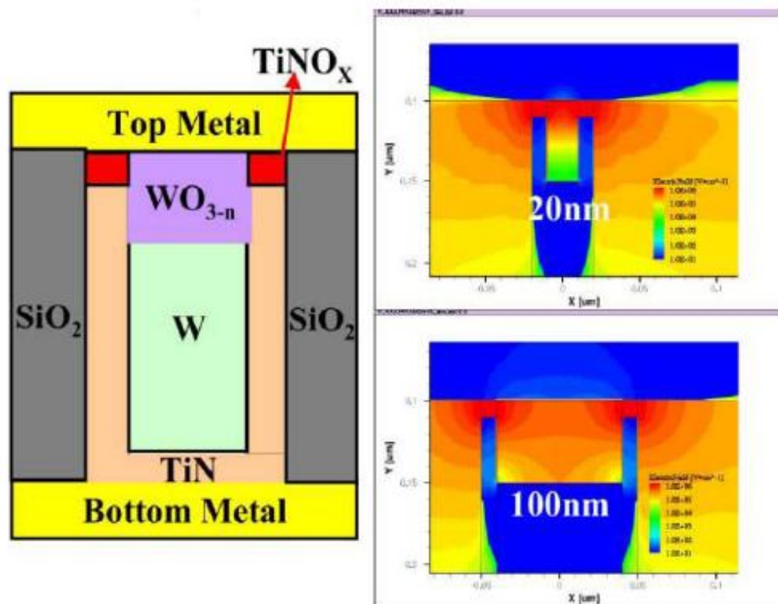

Figure 3-44. Electric enhancement structure (left) and the electric field distribution for 20nm (up-right) and 100nm (down-right) RRAM devices[42].

The dielectric constant of oxide layer also influences the electric field. Figure 3-45 shows the relationship between the forming voltage and dielectric constant[38]. In this figure, it is clearly shown that "forming" steps of RRAM can be regarded as soft-breakdown phenomenon of dielectric films controlled by applied electric field. Because different dielectric constant materials show different electric field in oxidation layer, the forming voltage also shows different values. In the previous results, the electric field in the oxidation layer plays an important role in the RRAM performance.

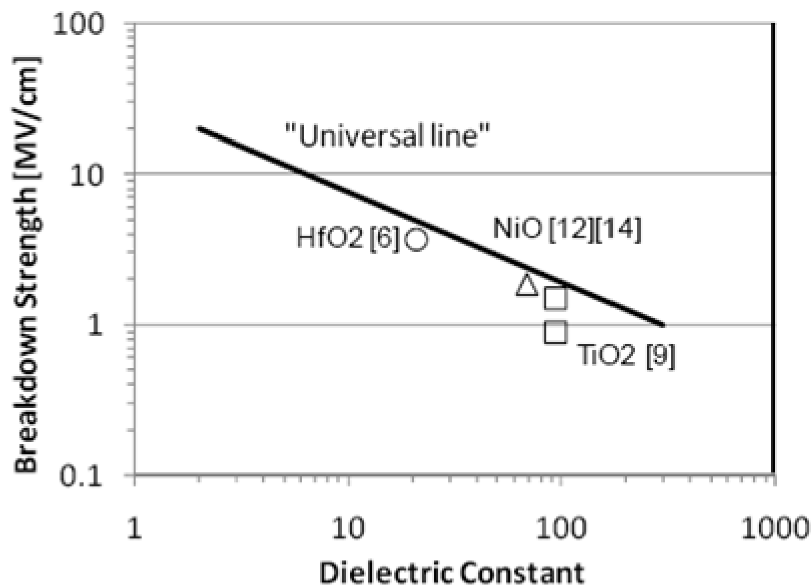

Figure 3-45. Forming voltage verse dielectric constant of RRAM[38].

3.5.6 Density of Oxygen Vacancies

Oxygen vacancy is a key element in the resistance switching mechanism, and many studies report that it also influences the RRAM performance. In our research of downstream plasma (DP) experiments, the initial resistance depends on the DP time, and oxygen vacancies depend on the DP time. Figure 3-46 shows the WO_x-based unipolar RRAM characteristic with different DP samples. Here, all the samples are forming-free and the initial resistance shows increasing relationship as DP increases. However, this WO_x-based RRAM with RTA oxidation process sample doesn't show the forming-free characteristic. These results indicate that the oxygen vacancy is an important element in the resistance switching performance.

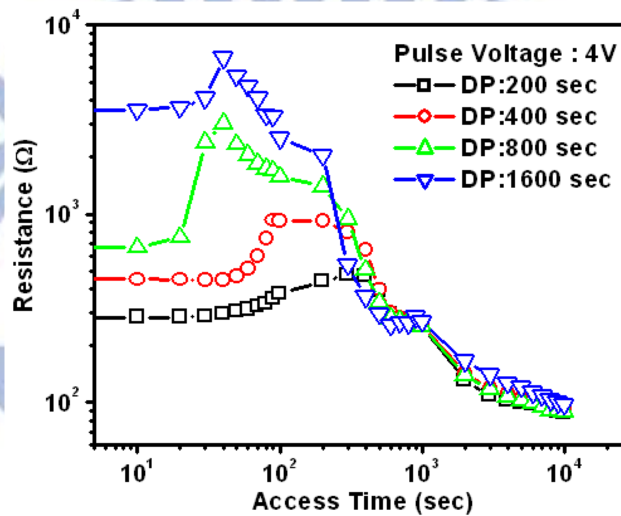

Figure 3-46. The unipolar operation character with different oxidation time.

Chapter 4 : Results and Discussion

In our experiments, we studied several materials such as nickel oxide (NiO_x), titanium oxide (TiO_x), and tungsten oxide (WO_x) for the RRAM. NiO_x, TiO_x and WO_x are suitable RRAM materials because they show stable resistive switching character. Moreover, due to the clear resistive switching character, simple structure, and CMOS fully compatible process of these three materials, presently many researchers still focus on these materials.

4.1 Outline of result

NiO_x, TiO_x and WO_x all exhibited bistable resistive switching character by the bipolar operation. The resistance ratio (also called on/off ratio), cycle endurance, and data retention were clearly observed in the reliability test. Moreover, the WO_x memory device was fully prepared by the semiconductor process, and it exhibits excellent performance in the reliability test. We believe that WO_x is promising to replace the present non-volatile memory.

The polycrystalline NiO_x RRAM showed bipolar resistive switching character, and electric character showed the relationship between thickness and oxygen content. The thicker thickness samples and higher oxygen content samples exhibit better performance in the reliability test. Also, the conduction mechanism can be well explained by Schottky emission and the resistive switching character shows the barrier high dependent relationship. Moreover, the dielectric constant of NiO_x shows the relationship with oxygen ratio and it also influences the efficiency of applied bias.

The TiO_x also showed bipolar resistive switching character and the conduction mechanism followed the Schottky emission. The electric character showed the barrier high dependence relationship. Moreover, the resistive switching behavior shows that thickness has little to do with trait. These results indicated the interface contribution in the resistive switching character. In addition, the TiO_x/SiO_2 hybrid system experiment indicated the interface contribution and this system exhibits better reliability performance.

For WO_x RRAM, the resistive switching behavior was observed not only by bipolar operation but also by unipolar operation. The electrical character of WO_x followed VRH in HRS and the electrical behavior of LRS is close to minimum-metal-conductivity (MMC). It also showed the barrier high dependent relationship with the resistance state. Its excellent performance includes high on/off ratio (>1000), good endurance (>1000), high thermal stability (>2000 hrs at 250℃), good read disturb (>1000 sec, at 1 V), high speed operation (<10 ns), small size (~9 nm), low current consumption (<10 uA), and so on. What's better, it can also be used in one-time programming (OTP) or multi-level cell (MLC) applications.

4.2 NiO_x-based RRAM

For NiO_x-based RRAM, there are three parts, including the material analysis, resistive switching character, and conduction mechanism analysis, which will be discussed in this section.

First, material analyses include the microstructure. Figure 4-1 shows the HRTEM image of our NiO_x film in the metal-insulator-metal (MIM) structure. According to this image, we can observe clearly (especially in the enlarge image of figure 4-2) that the polycrystalline NiO_x is everywhere in this film. Moreover, the SAED image (inset of figure 4-2) also shows the polycrystalline structure in NiO_x film. Several studies[79-81] also reported the polycrystalline structure in their NiO_x RRAM research.

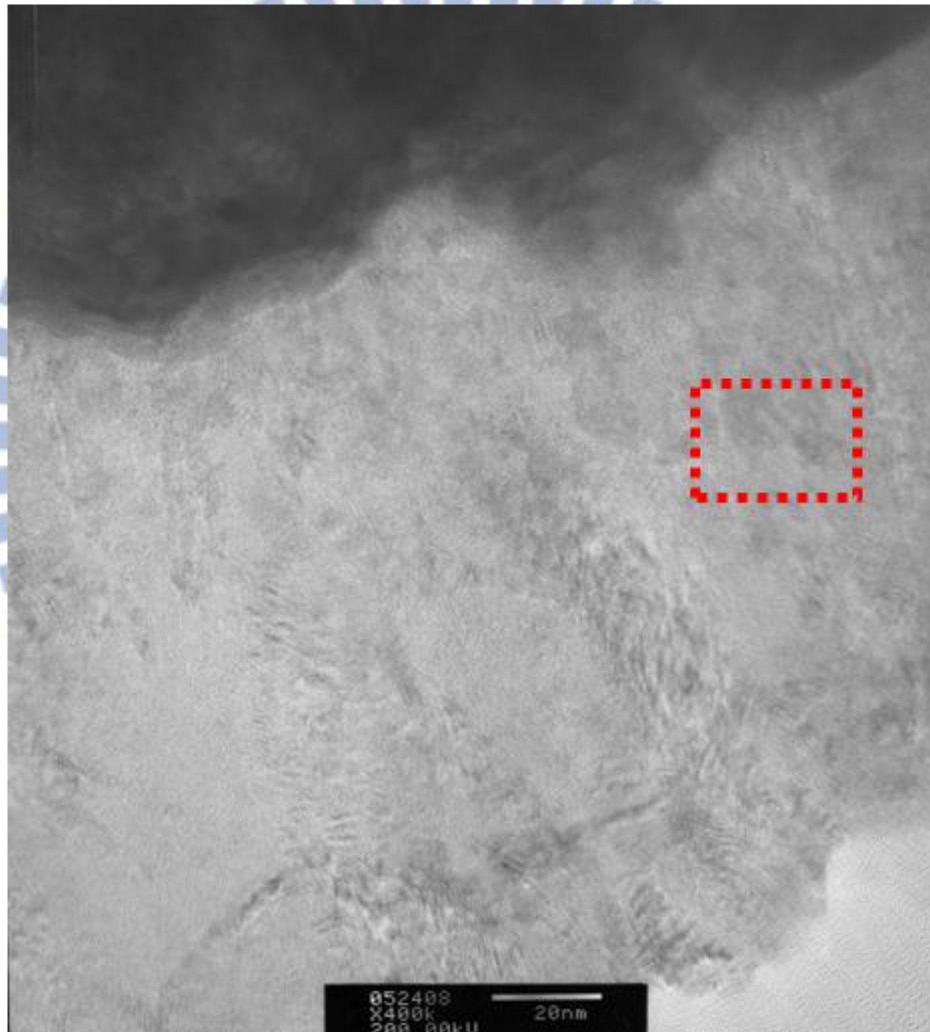

Figure 4-1. HRTEM image of polycrystalline NiO_x film

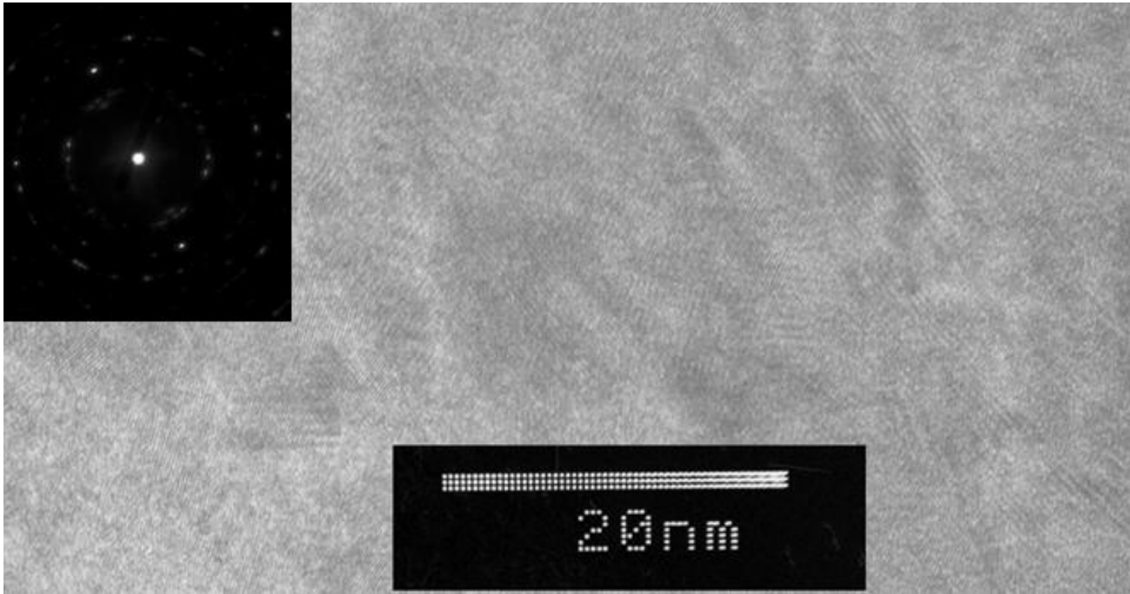

Figure 4-2. The enlarged part (dash mark in fig.4-1) of polycrystalline NiO_x film. Inset shows the SAED image.

Second, for resistive switching character, both unipolar and bipolar switching characters have been demonstrated in other studies[82-84]. These studies indicated the bistable resistive switching character in NiO_x film. For the bipolar resistive switching NiO_x RRAM, the resistance state is dependent on the direction of the applied voltage. The HRS and LRS is formed by opposite bias. For the unipolar resistive switching NiO_x RRAM, the resistance state is dependent on the amount of applied voltage. The LRS and HRS is formed by large and small applied voltage, respectively.

In this study, we only found the bipolar resistive switching character in NiO_x film. Figure 4-3 shows the thickness-dependent bipolar switching phenomenon of NiO_x films. In our experiment, the thickness above 30 nm was necessary because the bistable resistive switching phenomenon disappeared when the thickness was below 30 nm. With the increase of thickness, the more obvious resistive switching phenomenon was observed. Moreover, these thicker samples exhibited larger on/off ratio in the cycle endurance test. Accordingly, we defined the bistable states as high resistance state (HRS and low resistance state (LRS). In the programming operation, the resistance state is changed from HRS to LRS with an applied positive bias voltage. Similarly, the resistance state is changed from LRS to HRS by means of an applied negative bias voltage.

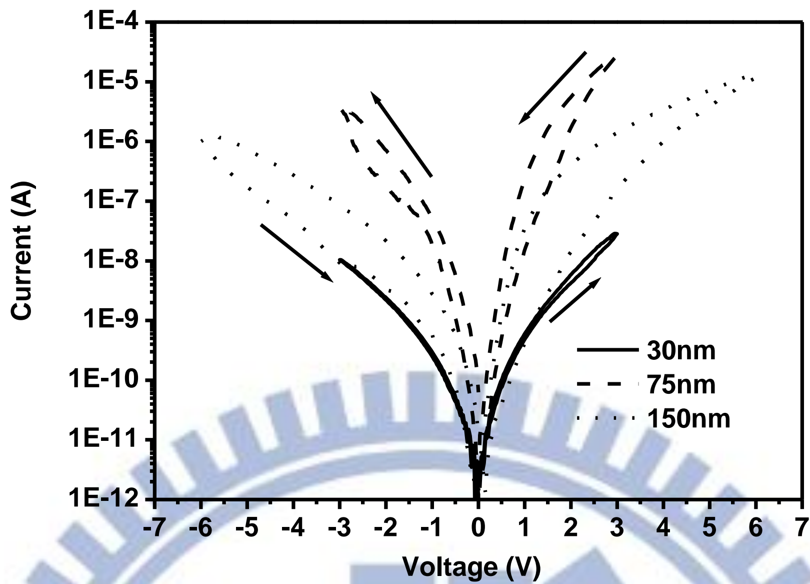

Figure 4-3. The resistive switching character of NiO_x films.

Figure 4-4 shows the relationship between sample thickness and the on/off ratio. The ratio shows the thickness effect in this figure. The on/off ratio is about 0.5 when the thickness is about 30 nm. As the thickness increases, the on/off ratio also increased. The on/off ratio is about 100 when the thickness increases to 150 nm. This result indicates the resistance switching performance dependent on the thickness of NiO_x.

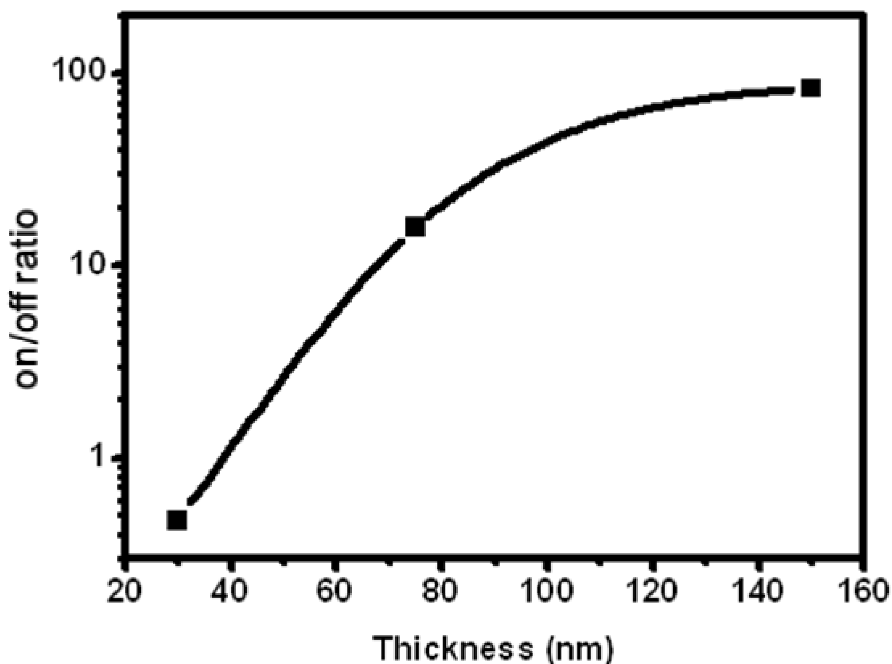

Figure 4-4. The relationship between sample thickness and on/off ratio.

Figure 4-5 shows more than 200 times of resistive switching processes of cycle endurance test of thick (75 nm and 150 nm) NiO_x films. In the endurance test, it was obvious that the resistive state is rising in this cycling process. It is attributed to the damage of the NiO_x film and this damage induced the rising of resistance state. This phenomenon was also reported by Rossel et al.[52] and it is attributed to the localized "burned" pits with create-like geometry. Therefore, the on/off ratio also showed a dropping in the endurance measurement. Figure 4-6 shows the on/off ratio dropping phenomenon and it indicates the on/off ratio dependence on the thickness of NiO_x.

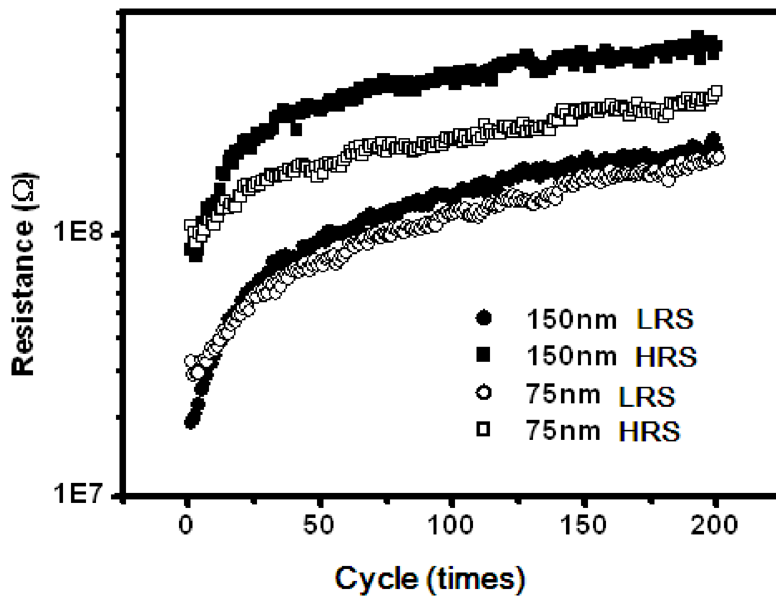

Figure 4-5. The endurance test of different thickness NiO_x films.

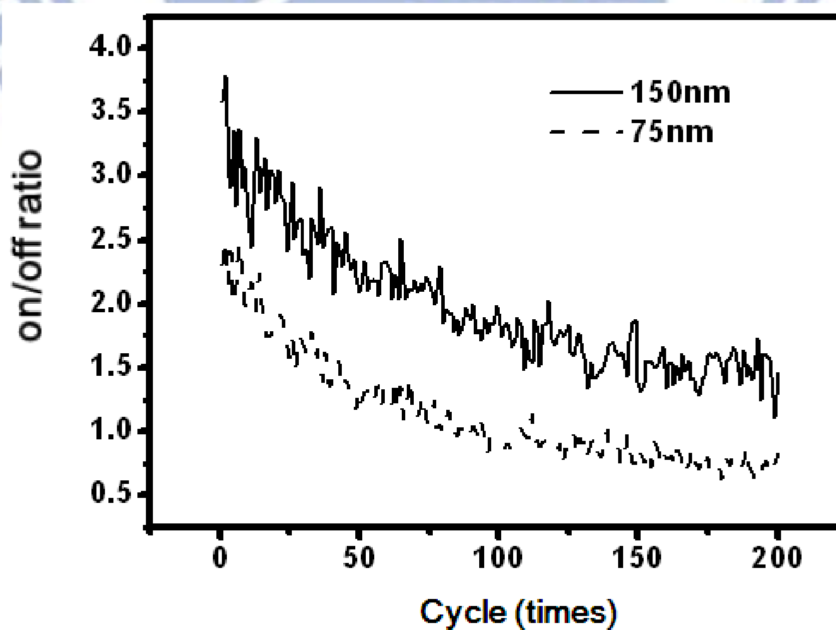

Figure 4-6. The on/off ratio of different thickness NiO_x films in the endurance measurement.

The oxygen content of NiO_x film is known to play an important role in resistive switching character. Figure 4-7 shows the resistive switching character (I-V curve) of 150 nm NiO_x film with various oxygen flow ratio. In this experiment, we defined $O_2/(Ar+O_2)$ as oxygen flow ratio and this ratio shows a strong relationship with on/off ratio. The relationship between oxygen flow ratio and the on/off ratio is shown in figure 4-8. It is clear to see that the on/off ratio dramatically increases from X3 to X100 as we increase oxygen flow ratio from 33% to 43%. In this figure, it indicates that the high oxygen flow ratio sample exhibits better performance.

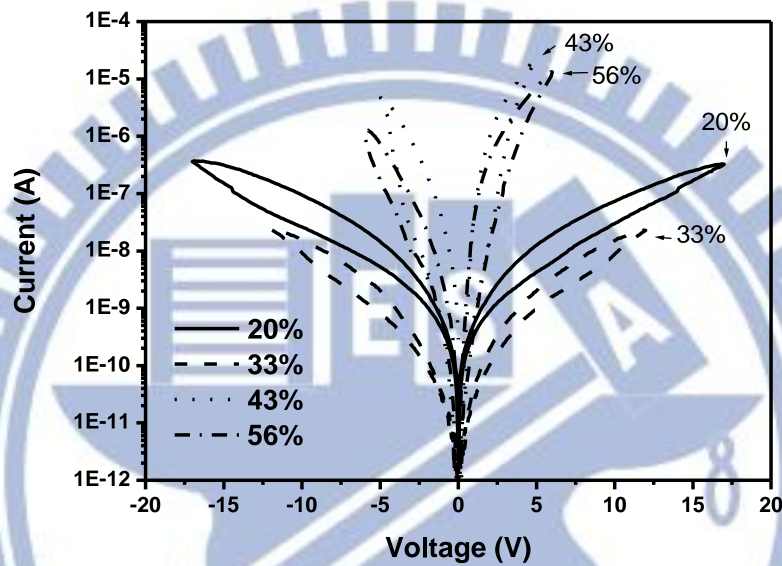

Figure 4-7. The resistive switching character of NiO_x film with different oxygen flow ratio.

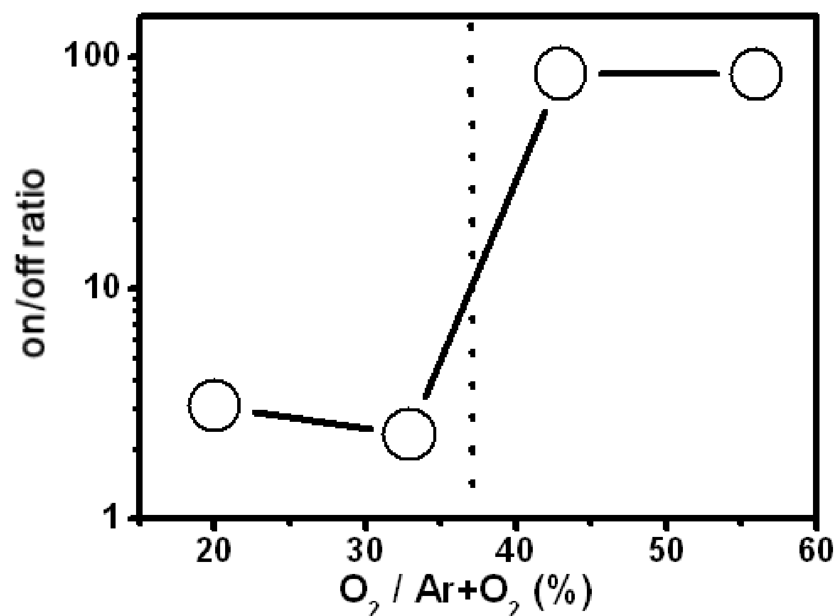

Figure 4-8. The relationship between on/off ratio and oxygen flow ratio.

Electrical analysis found the conduction mechanism was the Schottky emission in NiO_x. Figure 4-9 shows the Schottky emission fitting curve in our sample. The linear dependency indicates that the transport mechanism is strongly dependent on the barrier height and the dielectric constant, as is shown in Eq. (3-2). The calculation of dielectric constants and the $\delta(\phi_B)$, which was defined by the barrier high difference between HRS and LRS by fitting the Schottky emission, were summarized in figure 4-10. The trend of $\delta(\phi_B)$ is similar to the on/off ratio. It indicates the strong correlation between barrier high and on/off ratio. Several studies[85,86] also reported the relationship between barrier high and the resistive switching character. Moreover, a very high dielectric constant was obtained in the samples with oxygen flow ratio less than 33%, and the opposite case was observed in the sample with oxygen flow ratio higher than 43%. A sample with higher dielectric constant means it owns higher charge storage capability, which also influences the electric character in the resistive switching process.

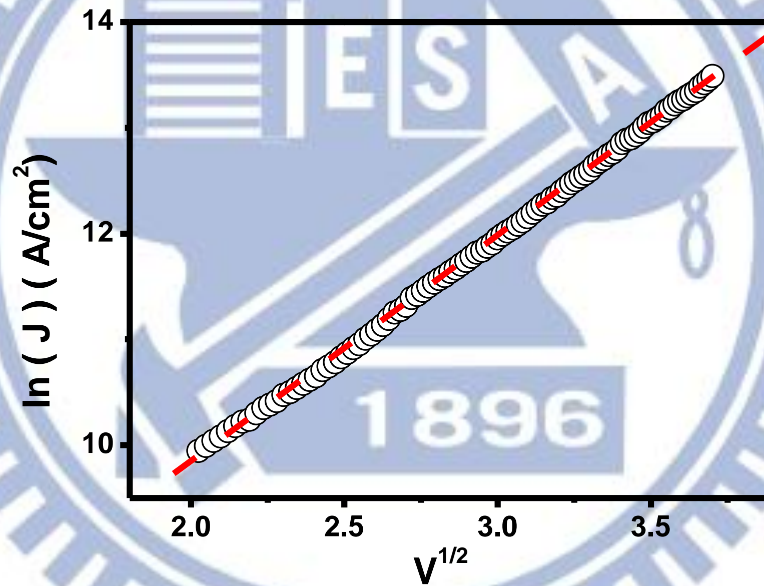

Figure 4-9. Schottky emission approximation of NiO_x film.

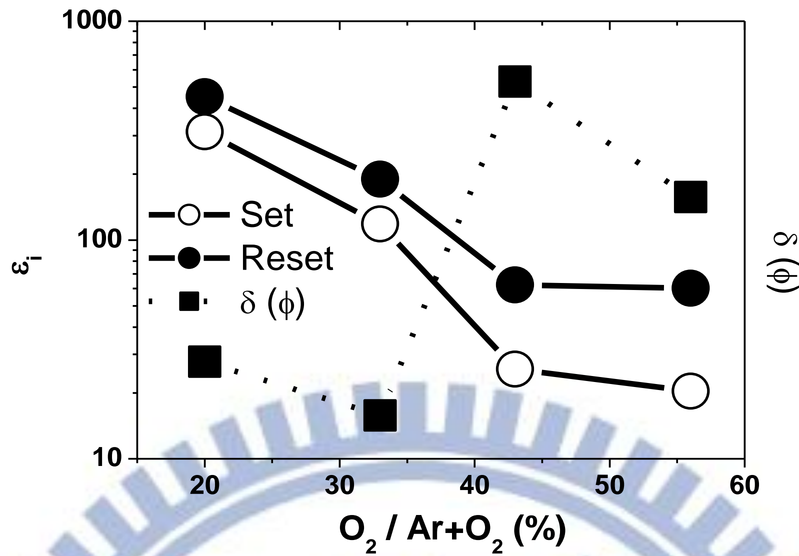

Figure 4-10. Dielectric constant and the barrier high change with various oxygen flow ratio.

Figure 4-11 illustrates how the internal electric field affects the resistive switching process for samples with various oxygen flow ratio. If we apply the same voltage in two different permittivity samples, the real voltage in those samples will be different. For the high permittivity sample, it can storage more charges in the interface and those charges form an opposite voltage in the insulator at the same time. Therefore, the real voltage in the sample is lower than the applied voltage. Similarly, there are small opposite voltage formed in the insulator of the low permittivity sample. This might be attributed to the fact that the samples with few oxygen ratios needed higher voltage to switch the resistance state.

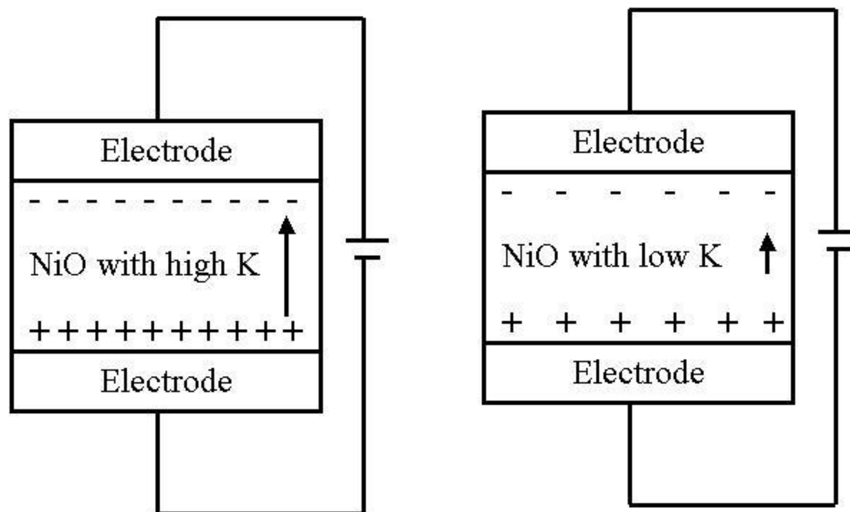

Figure 4-11. The influence of dielectric constant in the operation process.

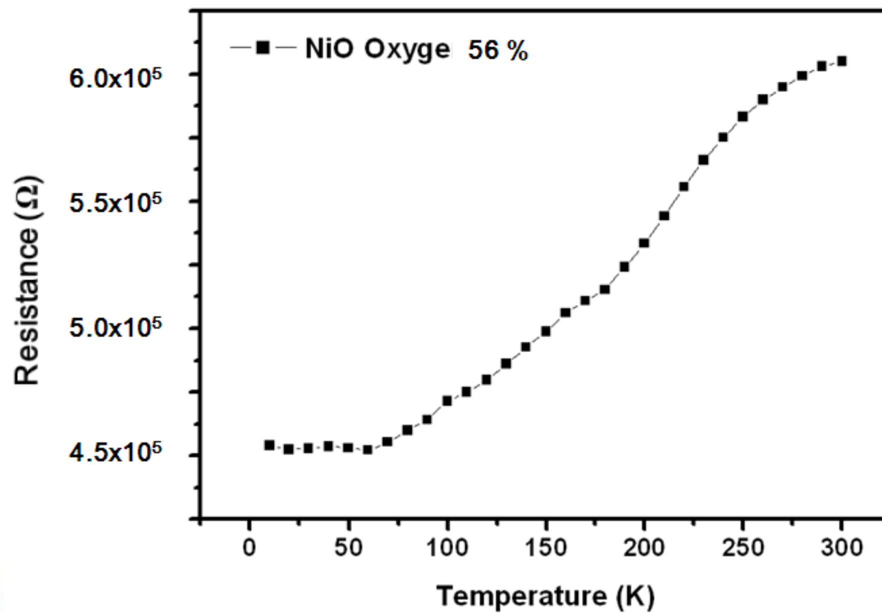

Figure 4-12. The temperature dependent electric character of NiO_x film.

Figure 4-12 shows the temperature-dependent electric character of NiO_x film. It is clear to see the resistance decreases when the temperature decreases from room-temperature to 4K. The resistance of NiO_x closes to linear decreasing trend when the temperature was above 60K. The minimum resistance appeared when the temperature was below 60K and it remained the same one. This result indicated a metal conduction character of our NiO_x film.

In summary, NiO_x shows the polycrystalline microstructure. The I-V curve shows clear bipolar resistive switching character. Both sample thickness and oxygen content influenced the bistable resistive switching phenomenon. The conduction mechanism follows the Schottky emission and the resistive switching character shows barrier high dependence relationship. Due to the temperature-dependent electric character, the NiO_x film showed a metal conduction character.

4.3 TiO_x-based RRAM

For TiO_x–based RRAM study in this section, we discuss three parts, including resistive switching character, conduction mechanism, and the interface contribution. Figure 4-13 shows the schematic core-section of TiO_x-based RRAM. The titanium oxide film is placed on the top of the 0.18 um diameter W-plug, and this W-plug is also called contact (CT) in the semiconductor fabrication. This CT is the connection between the memory cell and the source site, and the memory state is dependent on the resistance of titanium oxide.

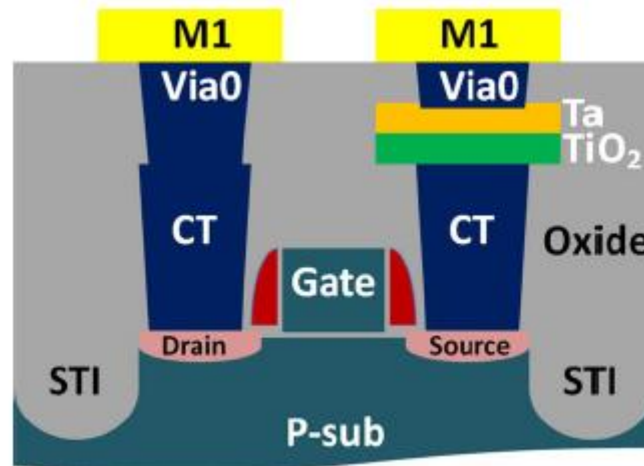

Figure 4-13. Cross-sectional view of TiO_x-based RRAM.

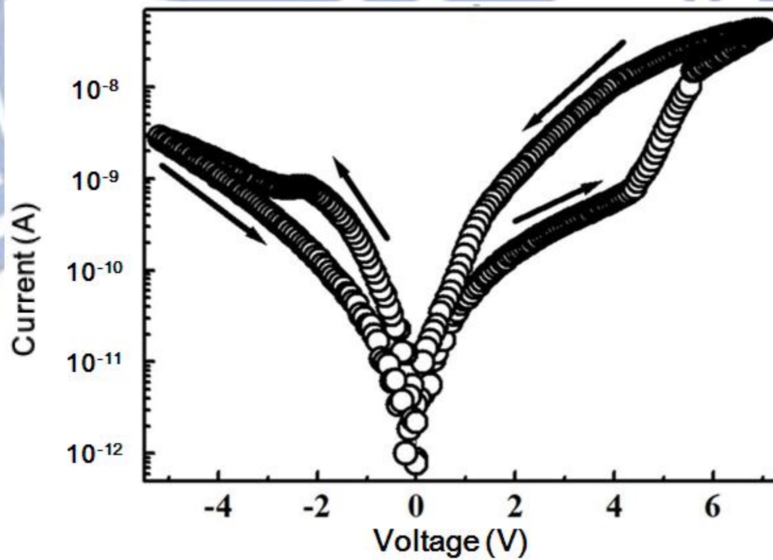

Figure 4-14. The bipolar resistive switching characterics of TiO_x film.

First, the electric character exhibits the bipolar resistive switching character, which is shown in figure 4-14. The positive switching voltage is about +5 V and the negatvie switching voltage is about -2 V. This asymmetrical resistive switching behavior is different with NiO_x film. Park et al.[87] also reported such an asymmetrical resistivite switching character in TiO_x film.

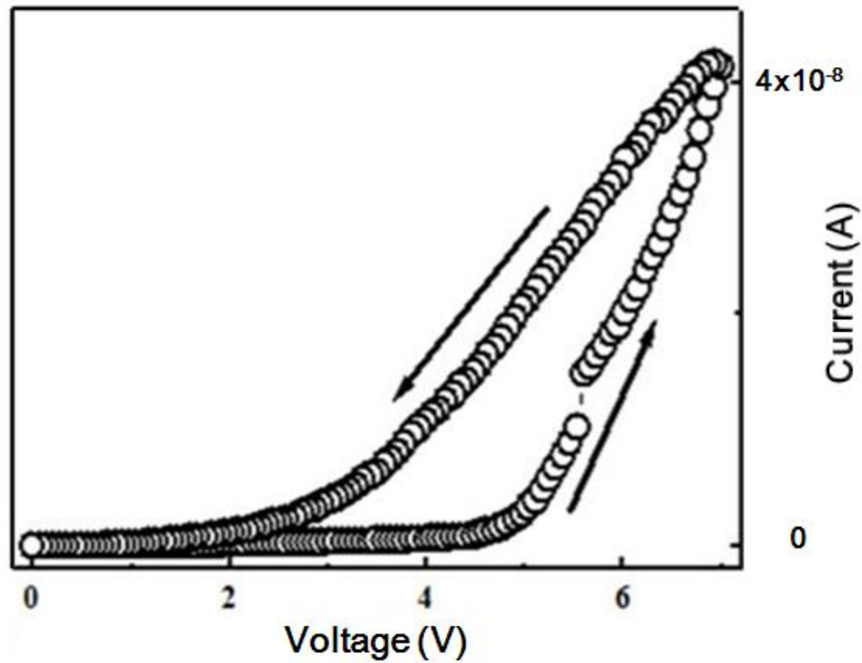

Figure 4-15. The resistive switching phenomenon from high resistance state to low resistance state.

Figure 4-15 shows the resistive switching phenomenon from HRS to LRS with linear scale of current. We can find a sudden rise at +5.5V in the rising curve and the CF is formed at the same time.

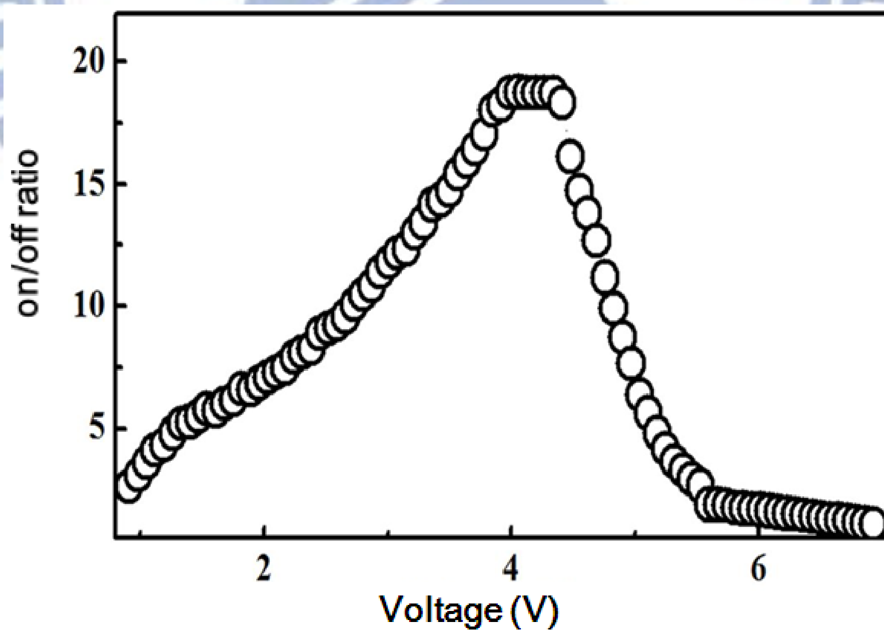

Figure 4-16. Voltage dependent on/off ratio.

Figure 4-16 shows the relationship between the applied voltage and on/off ratio. In this figure, we found the maximum on/off ratio is 20 at the applied voltage about 4 V. Also, we define this applied voltage as the transition voltage (V_T) and we can use this

parameter to observe the electric character. The reading voltage here must be below the V_T to avoid influencing the resistance stste.

Figure 4-17 shows resistive switching characters of TiO_x at various thicknesses. The electric characterstics indicate that these resistance switching behaviors are in thickness-indepentent relationship. All three I-V curves show similar resistive switching behavior and the resistance of these samples also shows thickness independent.

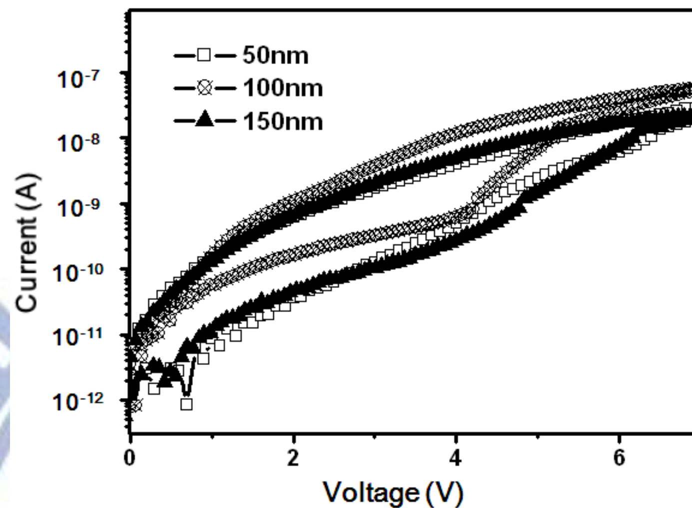

Figure 4-17. The resistive switching character of TiO_x film at various thicknesses.

Moreover, both on/off ratio and V_T are independent with sample thicknessas shown in figure 4-18. These results indicate the interface contribution of this TiO_x material.

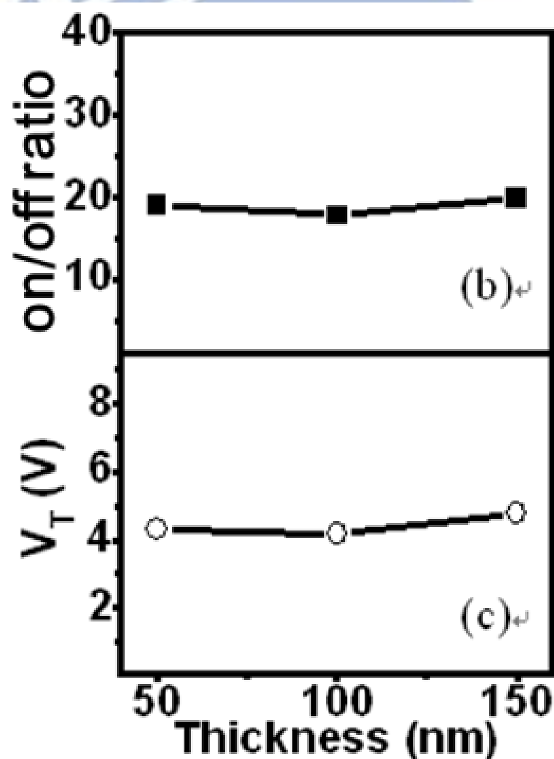

Figure 4-18. The thickness relationshop with transition voltage and the on/off ratio.

The curve fitting shown in figure 4-19 shows that all TiO_x films obey the Schottky emission mechanism. According to this result, we got one more proof of interface contribution in our TiO_x-based RRAM.

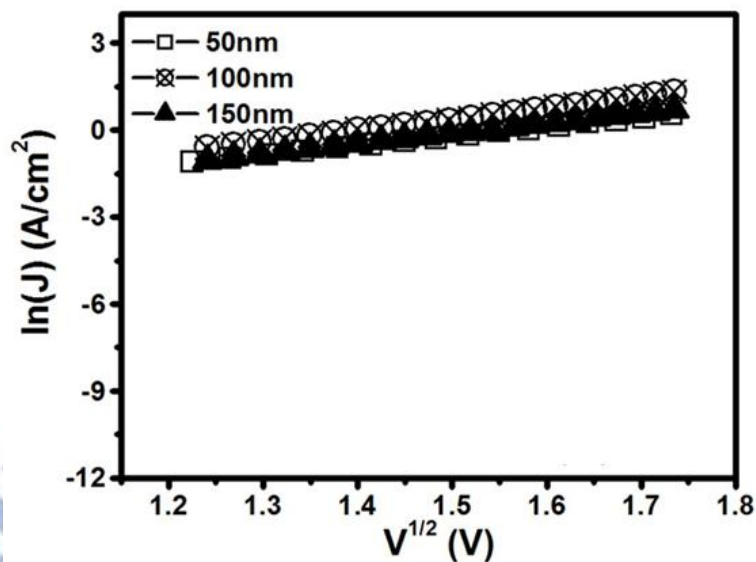

Figure 4-19. The curving fitting of I-V data for TiO_x atvarious thicknesses.

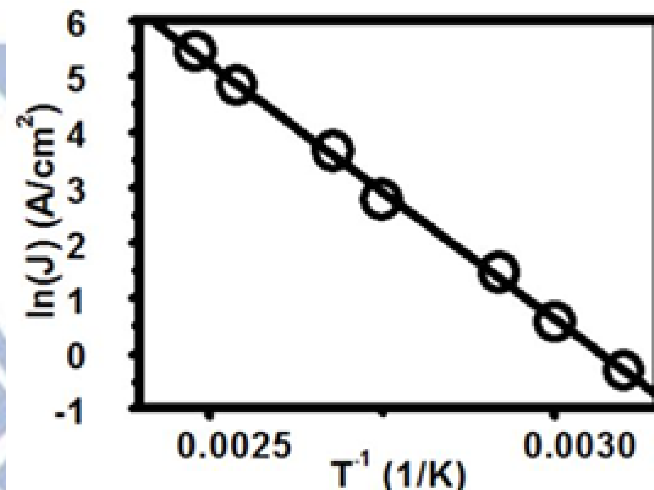

Figure 4-20. The temperature dependent electric characteristics of TiO_x film.

Figure 4-20 shows the temperature-dependent electric characteristics. In addition, according to the calculation of Schottky emission curve, we know the barrier high of HRS and LRS are about 0.6 eV and 0.73 eV, respectively.

In order to check this interface contribution, we prepared a hybrid sample with a 40 Å SiO_2 layer between TiO_x and bottom electrode. This hybrid sample (TiO_x-SiO_2) shows great improvement in the data retention test, and it also improves the on/off ratio. These improvements are shown in figure 4-21. In this figure, the LRS and HRS almost overlap, and the on/off ratio almost disappears after 100-sec retention test for TiO_x film. However, the on/off ratio always keeps at about 20 times for the hybrid sample.

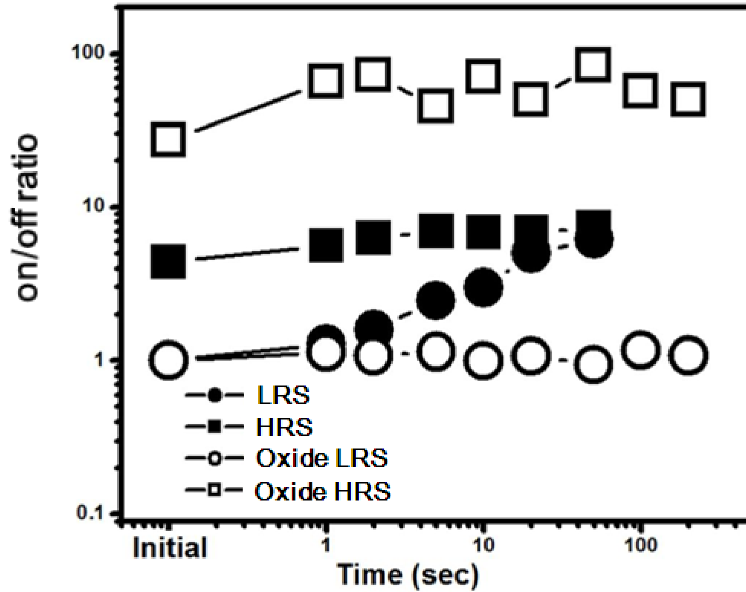

Figure 4-21. Data retention of TiO_x-based RRAM with/without SiO_2 hybrid system.

Figure 4-22 shows the cycle endurance test of TiO_x-based RRAM. In this figure, the resistance increases in the cycling test. It is attributed to the damage of the TiO_x film and this damage induces the rising of resistance. This result is similar to the NiO_x film. After 50 times of cycling operation, the LRS is close to the initial of HRS.

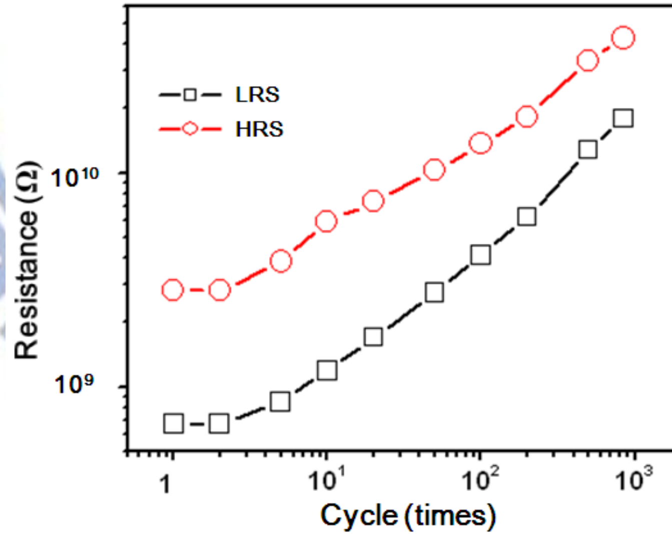

Figure 4-22. Cycle endurance test of TiO_x-based RRAM.

In hybrid system, the cycle endurance performance is also improved. Figure 4-23 shows the cycle endurance test of TiO_x-based RRAM with SiO_2 hybrid system. It is clear to see both LRS and HRS keep their resistance in the cycling operation test. This figure shows above 1000 times of cycle endurance performance of our hybrid system, and the on/off ration keeps at about 100X in this test. This hybrid system experiment also indicates the interface contribution of TiO_x RRAM.

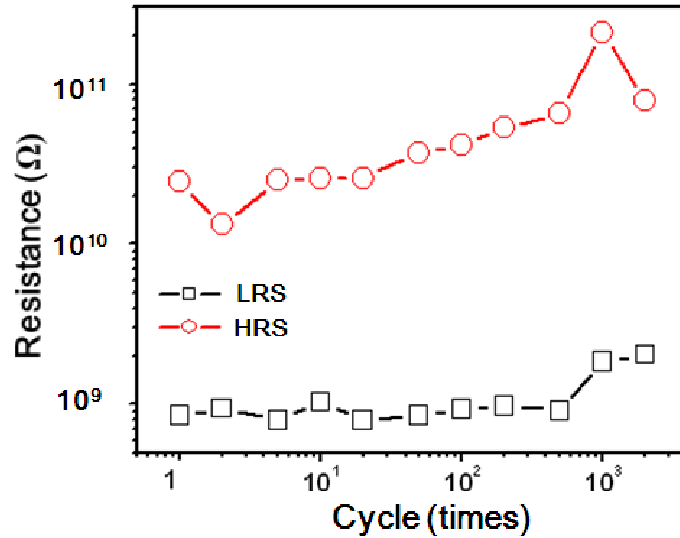

Figure 4-23. Cycle endurance test of TiO_x-based RRAM with SiO_2 hybrid system.

Figure 4-24 shows the read disturb test of the hybrid system. The reading voltage is only 50 mV to avoid damaging the memory cell. This figure indicates over 500 times read disturb performance of our hybrid system. Both LRS and HRS keep their resistance state, and the on/off ratio almost keeps at about 200X in this test. In this figure, the HRS decreases slowly in the read disturb test. It indicates that small reading voltage influences the HRS.

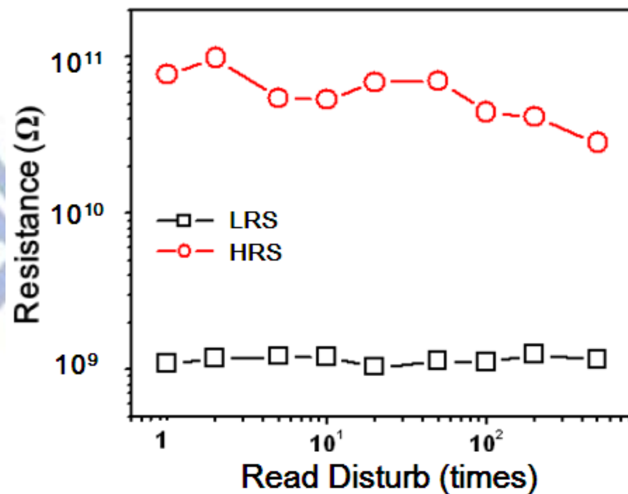

Figure 4-24. Read disturb test of TiO_x-based RRAM with SiO_2 hybrid system.

In summary, the TiO_x exhibits asymmetrical bipolar resistive switching character, and it shows interface contribution. The conduction mechanism follows the Schottky emission and the resistive switching character shows barrier high dependence relationship. The barrier high of LRA and HRS are about 0.6 and 0.73 eV, respectively. Moreover, the TiO_x-SiO_2 hybrid system also indicates the interface contribution, which improves the data retention cycle endurance and read disturb performance.

4.4 WO_x-based RRAM

WO_x-based RRAM has been studies by several research groups[24,28,88-91]. In the section, we discuss the process flow, microstructure, composition analysis, conduction mechanism, and the application for WO_x. Due to its better performance and widely applications, this material is promising for the next general nonvolatile memory applications.

Figure 4-25 shows the process flow of WO_x-based RRAM. First, we use a dummy wafer as the substrate and then deposit an inter metal dielectric (IMD1) for the isolation with Si wafer. Secondly, the TiN/AlSiCu/TiN was deposited for bottom electrode (ML1) and the SiO_2 was deposited for the second inter metal dielectric (IMD2). Thirdly, via pattern is defined by a photo lithography process and the via plug structure was created by via etching process. After the creation of via plug structure, an TiN adhesion layer was deposited and the W deposition was achieved by CVD process. After the W deposition, we used CMP process to make the surface smooth and form a W-plug structure at the same time. Finally, the oxidation process is formed by the down-stream plasma process and the top electrode (ML2) is defined by the second metal line process.

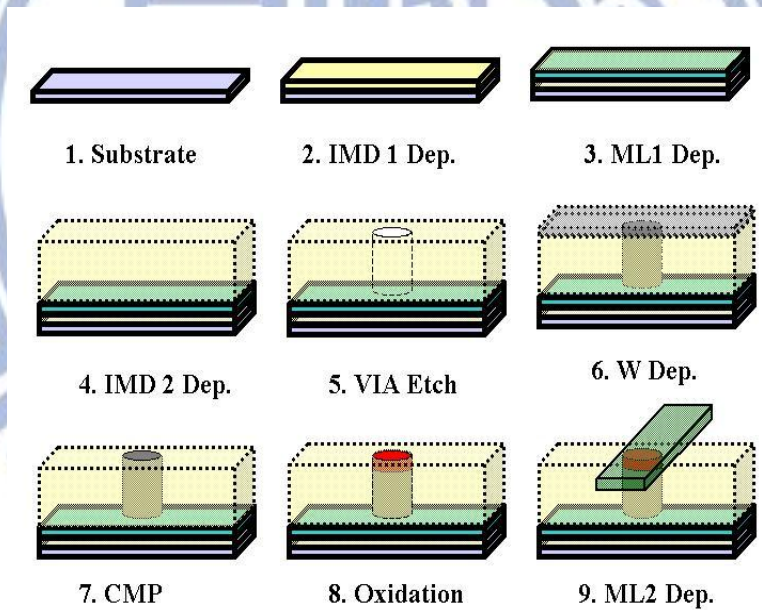

Figure 4-25. The WO_x base RRAM process flow

Figure. 4-26 shows the TEM image of WO_x film and the inset image shows the W-plug structure. The memory cell is placed on the top of the W-plug and it shows a uniform thickness about 120 Å of WO_x film. This image also indicates that our plasma oxidation is a uniform process and it can avoid the leakage of the short channel in the electrical measurement. Figure 4-27 shows the enlarged part of the WO_x layer. This image shows that the amorphous WO_x is everywhere in the memory cell.

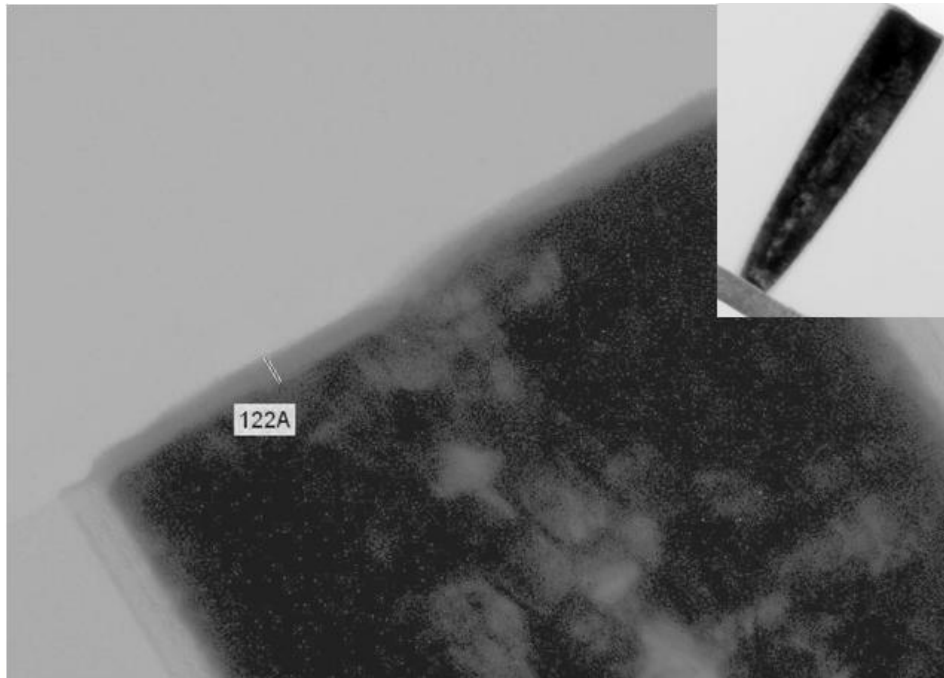

Figure 4-26. The TEM image of our WO_x film.

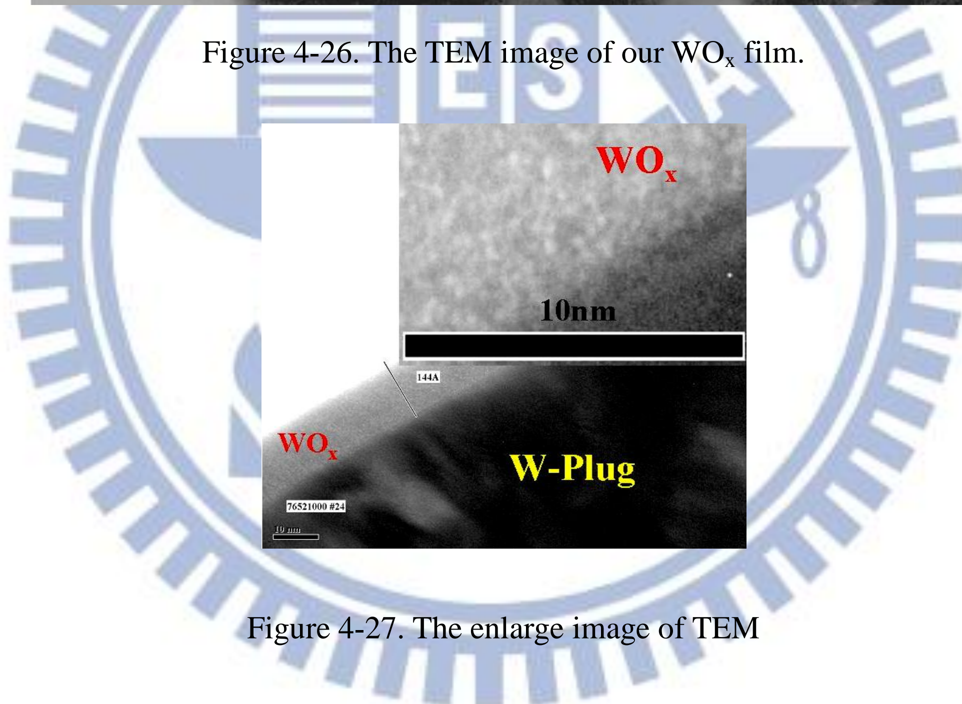

Figure 4-27. The enlarge image of TEM

Figure 4-28 shows the XPS data of WO_x film for O and W analysis. Figure 4-28 (a)~(d) shows the peak profile of the surface at the depth of 15Å, 70Å, and 140Å, respectively. In this figure, the WO_3 peak on the wafer surface (a) and the pure W peak is at the depth of 140Å (d). However, (b) and (c) do not show the clear peak profile in the XPS analysis because several peaks overlap in this region. XPS analysis indicated that the WO_3 dominates the top surface of WO_x and that mixed compounds are in deep regions, including WO_3, W_2O_5, WO_2, and so on.

Figure 4-29 shows the deconvolution of the XPS signal. This figure indicates the mixed compounds developed in deep regions, including WO_3, W_2O_5, WO_2, etc. The surface of memory device is WO_3 and about 140Å depth from surface is pure W. The

content of both W_2O_5 and WO_2 is below 40% in deep regions below 140Å. This deconvolution data shows the distribution of tungsten oxide and indicates the graded WO_x structure of WO_x RRAM device.

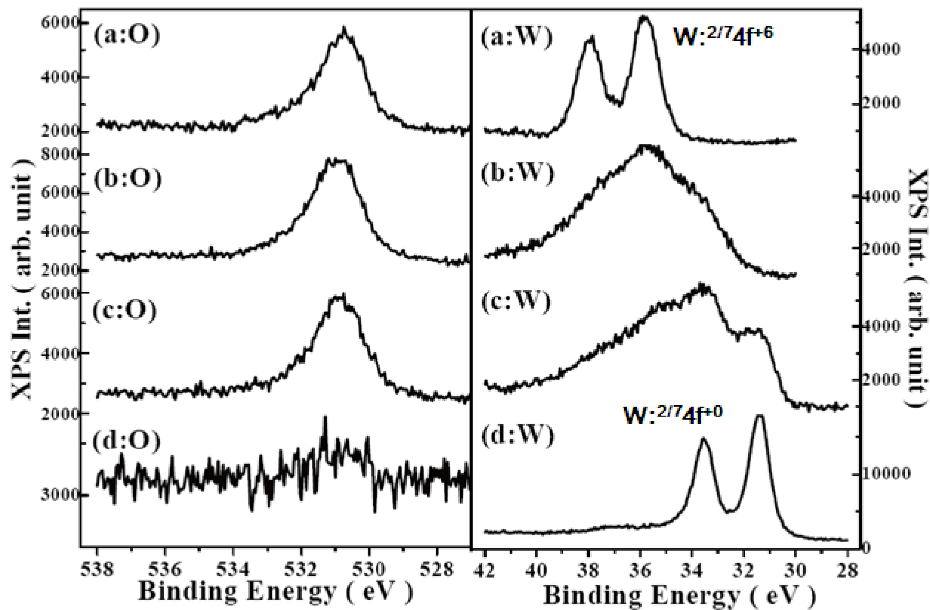

Figure 4-28. The XPS data of WO_x for O and W analysis. (a)~(d) are peak profile of at surface, depth of 15Å, depth of 70Å, and depth of 140Å.

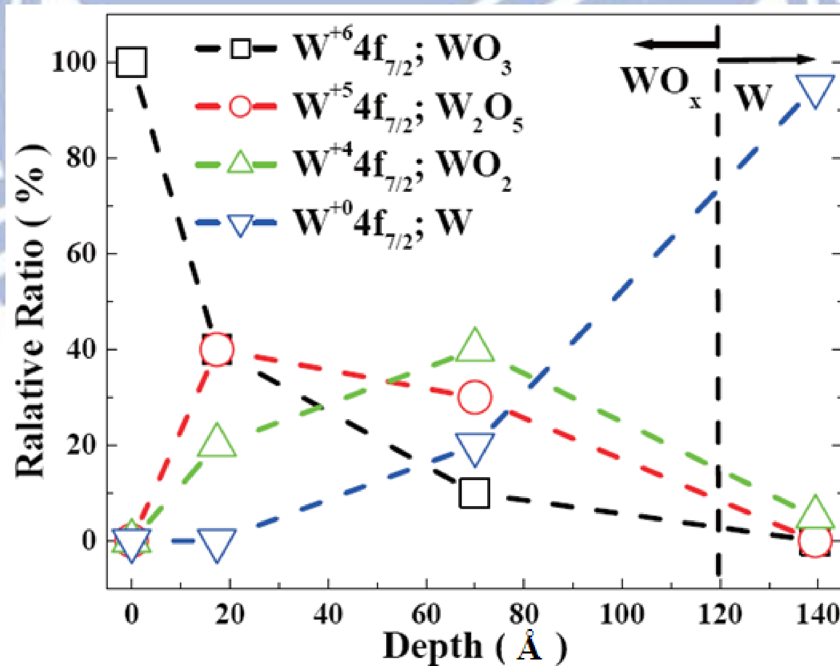

Figure 4-29. Vertical variation of W-ion that are analyzed by deconvolution of XPS.

Figure 4-30 shows the relationship of oxygen distribution. According to XPS data, the top surface of WO_x RRAM is WO_3, but the oxygen content decreases monotonically to <1 with depth. The XPS results suggest mixed compounds with different valence values of W^{+6}, W^{+5}, W^{+4}, and W^0. The oxygen content decreases with depth linearly. The thickness of graded WO_x structure is about 140Å.

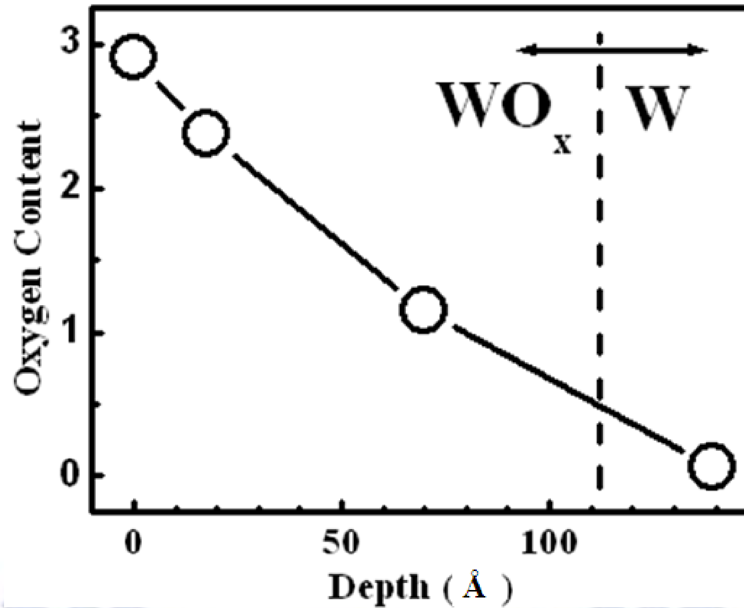

Figure 4-30. The distribution of oxygen content.

4.4.1 One-time-programming (OTP) RRAM

For the first tuning of the electrical character of our WO_x device, we tried several pulse conductions such as the combinations of pulse width and pulse voltage. We found the WO_x can be used for the one time programming (OTP) application. In our experiment, we found that there are two ways to be used in this OTP application. One is to use several pulse shots with constant voltage (5 V, 70 ns) to form the different resistance states. The resistance state is dependent on the numbers of pulse shot. Figure 4-31 shows the relation between the resistance state and the numbers of applied pulse shots. For example, the initial resistance state of our fresh sample is about 1 kΩ and this resistance state is defined as “01” state. However, the resistance state is reversed from this “01” state by one pulse shot and this reversed resistance state (“00” state ~ 20 kΩ) keeps about the same one if the number of shots is below N_{c1} (~60). When the number of shots is above N_{c1}, the resistance decreases from 20 kΩ to 100 Ω (“10” state) and it keeps at the same one if the number of shots is below N_{c2} (~120). Moreover, the lowest resistance of this WO_x film is about 30 Ω (“11” state) when the number of shots is above N_{c2}. With this kind of operation, we can easily program this two bits per cell (2 bits/cell) OTP resistance switching memory device.

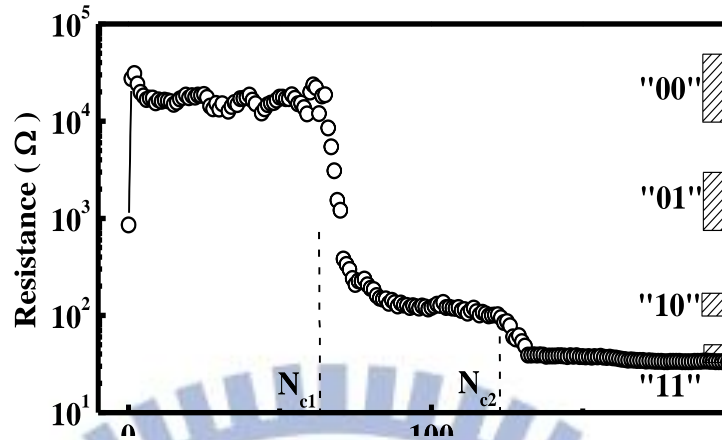

Figure 4-31. The resistance state verse the number of pulse shots.

However, these resistance states are very sensitive with the pulse width. Figure 4-32 shows the influence of the different pulse width on resistance switching character. For 100 ns pulse, the HRS ("00" state) was formed by only one shot. And the total number of shots at other two LRS ("10" and "11" states) is smaller than the number of shots by 70 ns pulse width. This result indicates the pulse width dependence relationship on the WO_x film.

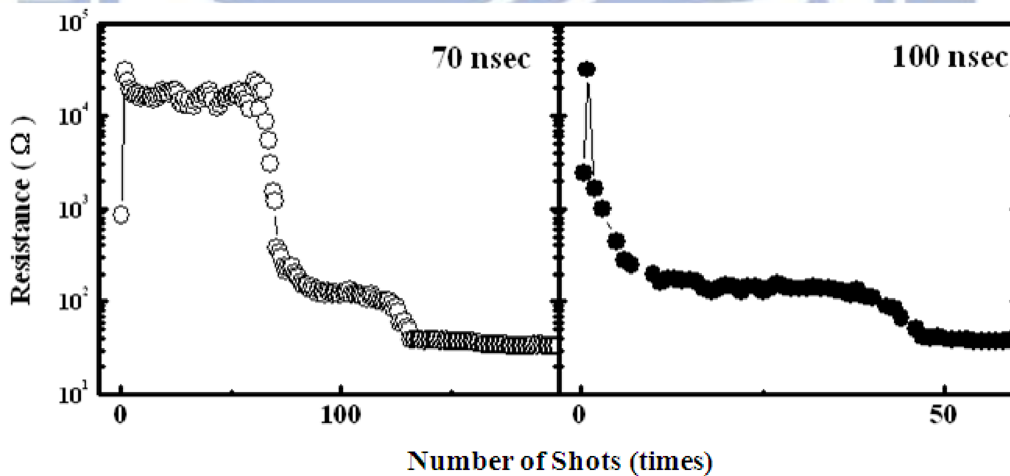

Figure 4-32. The resistance switching by 70 ns and 100 ns pulse width.

Another way to be used for the OTP operation is to change the pulse width with a fixed applied voltage. Figure 4-33 shows the relation between resistance state and the pulse width, with fixed the voltage at about 1.5V. The HRS ("00" state) can be programmed by a 60 ns pulse and the second HRS ("01" state) can be programmed by a 45 ns pulse. Moreover, the LRS ("11" state) can also be programmed by a 200 ns pulse applied. This method is more efficient for the OTP application because all the resistance state can be formed by only one shot. This one shot OTP operation not only increases the programming speed but also reduces the programming cost.

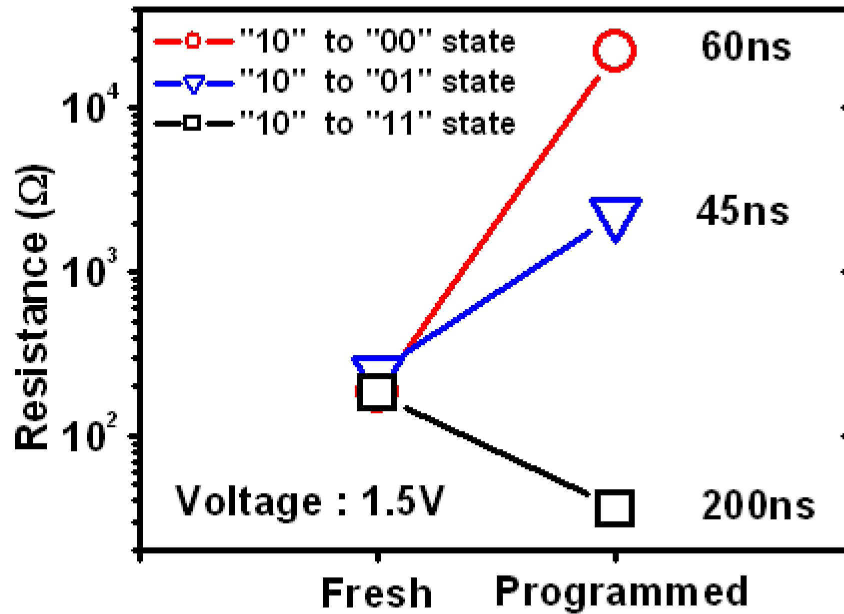

Figure 4-33. The one shot OTP operation character.

Figure 4-34 shows several shot programming operation with different pulse width. For 1.5V applied voltage, the initial resistance can't be reversed by applying a 10 ns pulse bias. It can be attributed to the fact that lower energy (too shorter pulse and low voltage) can't revise the resistance state. With the pulse width increasing (also means more power), the resistance state is reversed by the applied pulse shot. In this figure, the resistance state can be switched to HRS by 50 ns and 80 ns pulse shot. By the way, with the addition of pulse shots, the resistance state reverses slowly to the LRS. However, long pulse shot can switch the resistance state to the low resistance state. In this figure, the resistance switching behavior shows no difference between 1 us and 10 ms pulse shot. These LRS are created by the high energy pulse. Moreover, these LRS decreased slowly with more applied pulse.

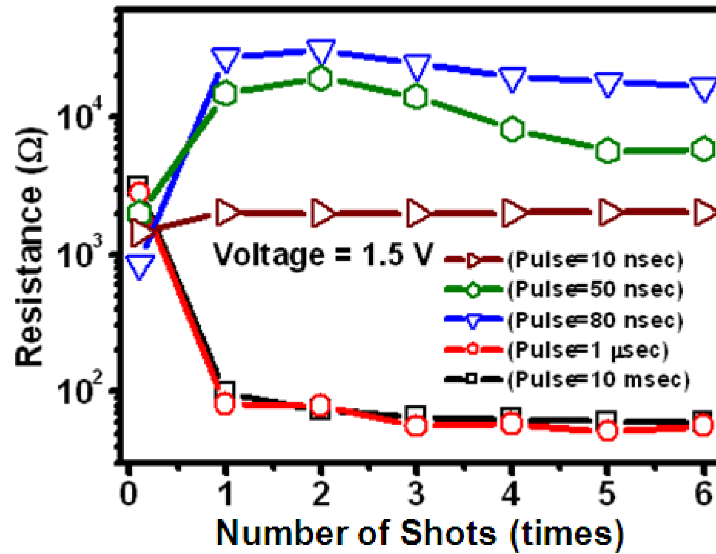

Figure 4-34. The influence of the pulse width with applied voltage about 1.5 V.

According to our previous experiments, it is easy to program these resistance states in the bi-stable 2 bits/cell device. Moreover, these states exhibit excellent read disturb performance. Figure 4-35 shows the read disturb character of our 2 bits/cell memory device. The applied reading voltage is about 10 mV and these resistance states still remain their resistance state after one thousand times of reading process.

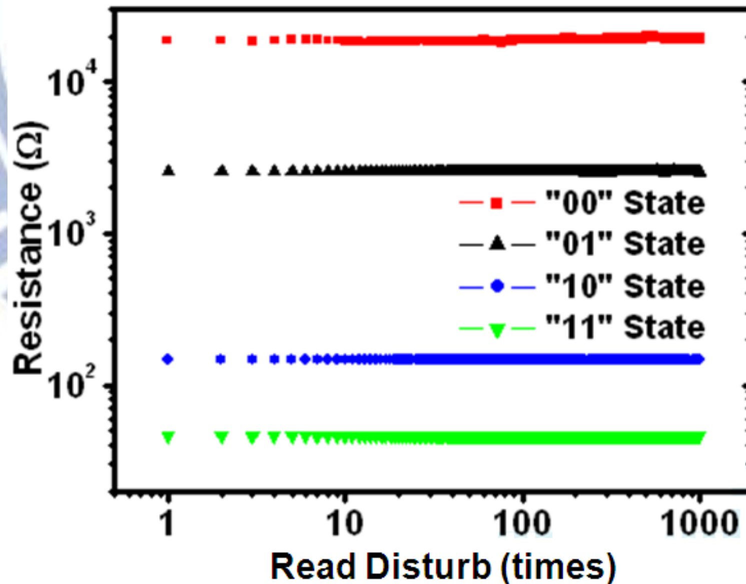

Figure 4-35. The 10mV read disturb of 2bits/cell WO_x film

These 2bits/cell resistance states also exhibited excellent data retention and thermal stability. The left of figure 4-36 shows data retention performance for more than 10^4 sec at room temperature, and the right of figure 4-36 shows thermal stability at 150℃ for more than several hundred hours. These results indicated that our OTP WO_x film is a suitable material for the OTP non-volatile memory application.

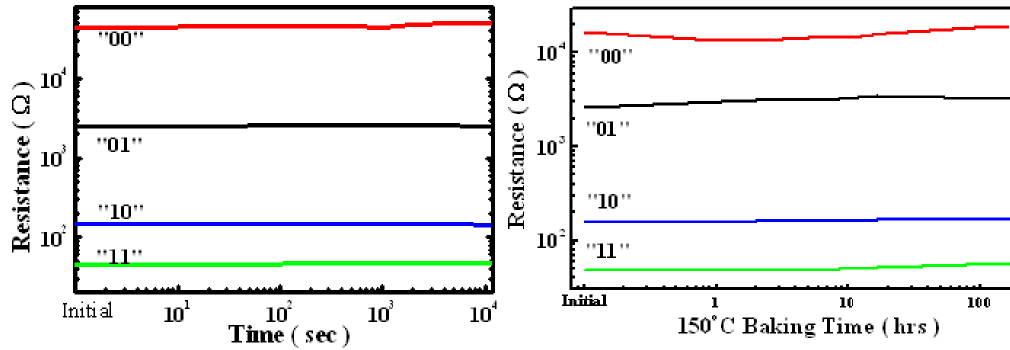

Figure 4-36. The data retention (left) and thermal stability (right) of 2bits/cell WO_x film

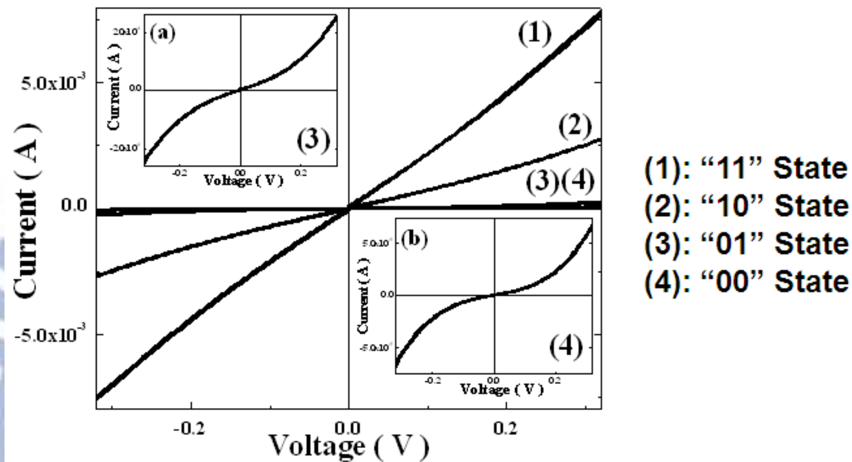

Figure 4-37. The electrical character of four resistance states.

Figure 4-37 shows the I-V curve of these four resistance states. These resistance states exhibit both linear and non-linear electrical behavior. The electrical character of LRS ("11" and "10" states) shows linear I-V curve and they follow the Ohm's law. It indicates the metal dominant behavior in these two low resistance states. However, the HRS ("01" and "00" states) shows non-linear I-V curve and these curves are well fitted by $T^{-1/4}$. It indicates that these electrical characters follow the VRH behavior.

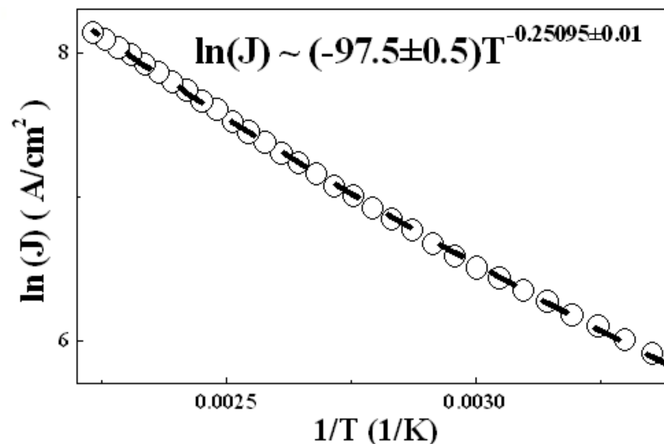

Figure 4-38. Temperature effect on "00" state. The dashed line is optimized fitting by power law.

Figure 4-38 shows the temperature effect on the current "00" state with applied voltage near zero. This figure indicates the VRH conduction mechanism as described by Eq. (3-4). If the voltage is close to zero, kT x sinh(CV/kT) becomes a temperature independent constant and Eq. 3-4 depends only on $\exp(T^{-1/4})$. We can simplify Eq. (3-4) to Eq. (4-1) and the important parameters are as followed:

$$I \sim \exp(-BT^{-1/4})CV \quad \ldots\ldots(4\text{-}1)$$

$$B = 1.66 \times \left\{ \frac{\alpha^3}{kN(E_F)} \right\}^{1/4}, \quad C = \frac{eR}{d}, \ N(E_F): \text{Density of state}$$

$$\text{Hopping distance}: R = \frac{3^{1/4}}{\{2\pi\alpha N(E_F)kT\}^{1/4}}, \ \text{Activation energy}: \ W = \frac{3}{4\pi R^3 N(E_F)}$$

With the hyperbolic-sin fitting on I-V curve, the hopping activation energy and the localized density of state can be calculated as 0.4 eV and 10^{20} $eV^{-1}cm^{-3}$, respectively. The average hopping distance for electrons is 15 Å .

4.4.2 Bipolar Multi-times-programming (MTP) RRAM

We found the WO_x film also exhibits bistable resistance switching behavior by a bipolar operation. In our experiment, the resistance state can be switched to HRS by applying a positive pulse voltage. On the other hand, the HRS can also be reserved to LRS by using a negative pulse voltage. The suitable pulse width is about 80 ns and the positive and negative voltage is +5 V and -4 V, respectively. By using this bipolar operation, it is easy to define the resistance state to LRS and HRS. Moreover, these two resistance states exhibit good performance on the reliability test, which will be described later in this section.

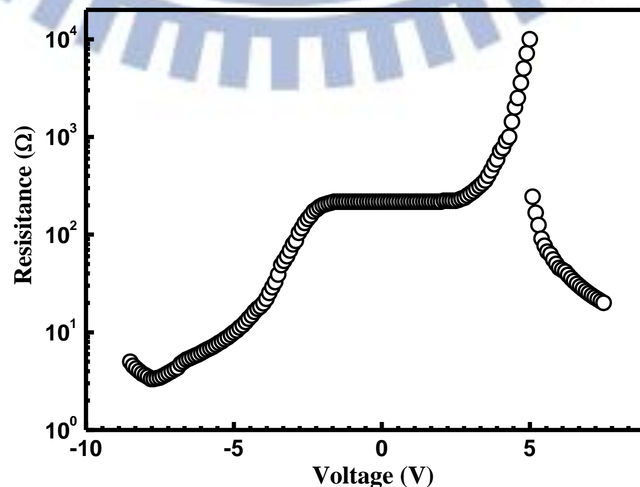

Figure 4-39. The resistance switching character by 80 ns pulse bipolar operation.

Figure 4-39 shows the resistance variation after an applied pulse (80ns). This WO_x film shows a typical bipolar resistive switching characteristic. With a positive applied voltage, we can clearly observe that the resistance increases when voltage is above 2.5V. The maximum resistance is about 10^4 Ω when the positive voltage reaches about +5V. Moreover, the resistance drops suddenly if the applied voltage is above the V_{th} (+5V), and the resistance becomes more unstable than before. In the meantime, the resistive switching character disappeared because the memory cell was destroyed when the applied voltage is above the V_{th}.

Oppositely, the resistance decreases when we apply a negative pulse voltage. When the applied negative bias reaches -4V, the resistance is about 20 Ω. This resistance is similar to the fail point when the applied positive bias is above V_{th}. In our experiment, this resistive memory exhibits good performance with these two operation conductions (+5V, -4V).

Figure 4-40 shows the cycle endurance test with this bipolar operation. It is clear to see that the on/off ratio keeps at about x10 during the cycle operation process for a thousand times. Both LRS and HRS exhibit small fluctuation in the cycle process and these two states never overlap in the cycle process.

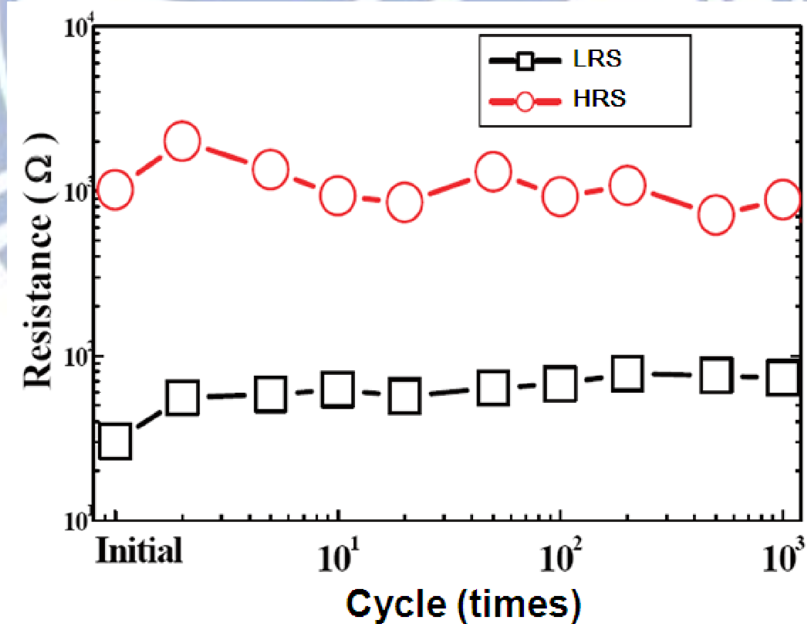

Figure 4-40. Above thousand cycle operation in the endurance test.

Figure 4-41 shows the thermal stability experiment. In this figure, it is clear to see that both LRS and HRS keep their resistance state and the on/off ratio keeps at about 100X for long time baking. Not only 150℃ but also 250℃ baking experiments indicated this WO_x film has excellent thermal stability.

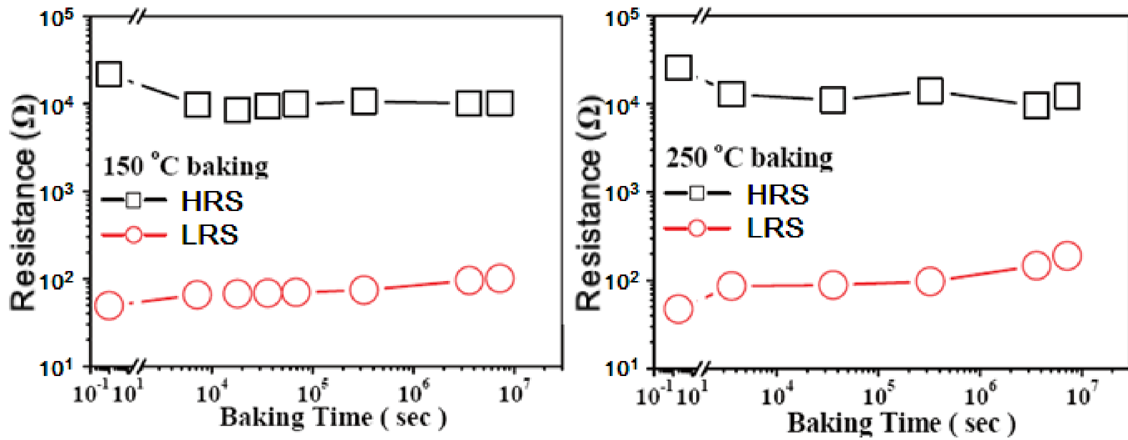

Figure 4-41. The thermal stability test at 150 (left) and 250℃ (right).

Figure 4-42 shows the influence of stress on the LRS. In this experiment, the LRS also shows good performance in the stress test. The low resistance keeps its resistance state over several thousand seconds in 200 mV stress environment. For the higher stress about 400 mV, the resistance state reduces to roughly 40% after a thousand seconds on the stress test. Moreover, in 1000 mV stress environment above 1000 sec, the resistance state still keeps at the LRS without overlapping with HRS.

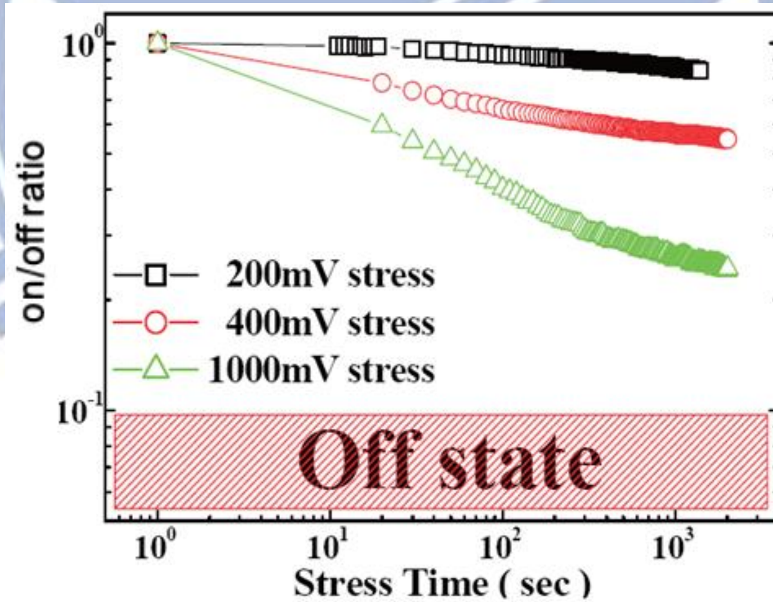

Figure 4-42. The stress test for LRS.

However, the width of applied pulse shot also plays an important role in the resistive switching character. Figure 4-43 shows the pulse width effect on the resistive switching character. We change pulse width from 9 ns to 80 ns to observe the influence on resistive switching behavior. Basically, the resistance switching behaviors are similar: first, the resistance increases and then suddenly drops after the threshold voltage (V_{th}). Next, the maximum resistance of those samples is in the range about 10^4~10^5 Ω and all

the breakdown resistance is below 100 Ω. In this figure, it is clear to observe that the V_{th} increases when we reduce the pulse width of applied voltage. The relationship of V_{th} and pulse width are also shown in figure 4-44.

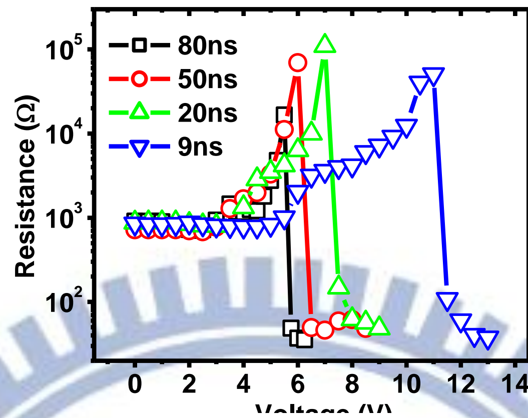

Figure 4-43. The resistive variation by applied bias with different pulse width.

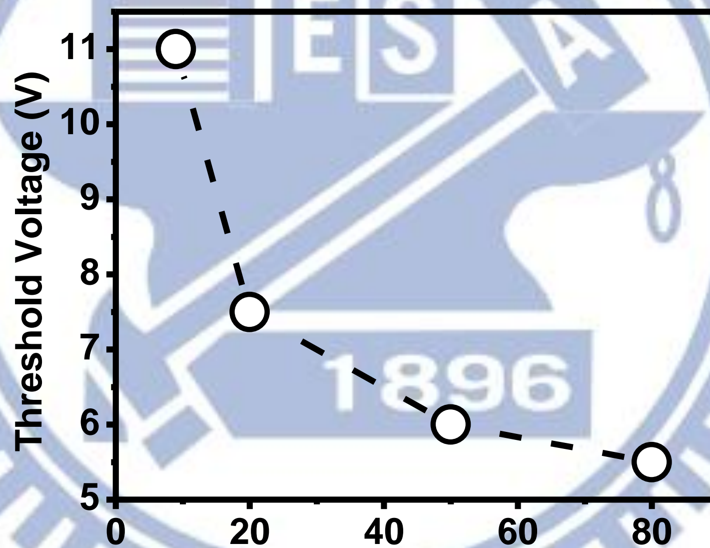

Figure 4-44. The relation between pulse width and threshold voltage.

The WO_x RRAM also shows the possibility of the multi-bits programmable. Figure 4-45 shows above 100 cycle endurance of 2 bits/cell operation. By fixing the pulse width (80ns) and changing applied voltage (from -4 to 5 V), it is easy to form four different resistance states. These four resistance states remain after 100 cycle operation. This result indicates that the WO_x RRAM is promising for multi-level-cell (MLC) application.

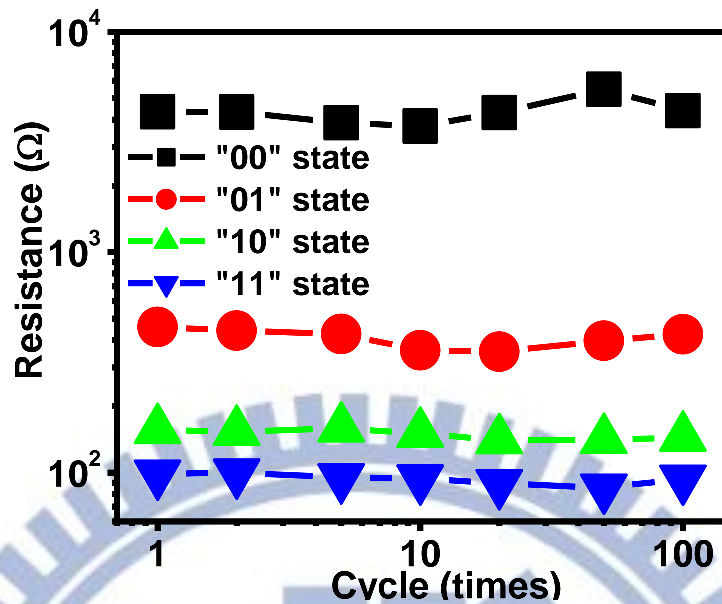

Figure 4-45. The endurance test of 2 bits/cell bipolar operation memory.

Figure 4-46 shows the electric character of LRS and HRS. This figure indicates the linear I-V curve of LRS. This metallic state is close to the minimum-metal-conductivity (MMC). However, the non-linear I-V curve of HRS follows the VRH conduction mechanism.

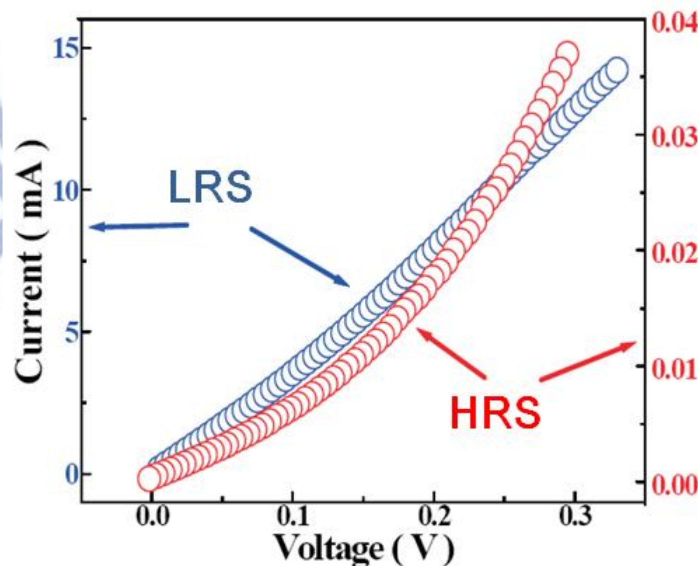

Figure 4-46. The I-V curve of LRS and HRS states.

Figure 4-47 shows the temperature effect on the HRS with current close to zero. Moreover, the good hyperbolic-sine fitting of the I-V curve (the inset of figure 4-47) further strengthens the VRH conduction mechanism. With the calculation of hyperbolic-sine fitting, we got the hopping distance about 15Å .

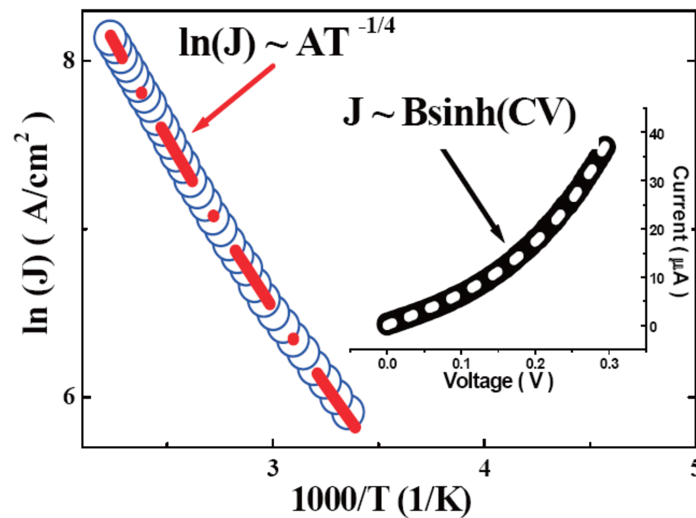

Figure 4-47. The temperature dependent electrical character and VRH fitting curve (inner) for high resistance state.

Figure 4-48 shows the temperature effect on LRS. The measurement range of temperature effect changes from room-temperature to 4K. It is clear to see that the resistance decreases when the temperature decreases. The temperature effect shows the same behavior both in low and high temperatures. The inset shows the resistance behavior which change from room-temperature to high temperature. These results indicate that the LRS follows the metal conduction mechanism.

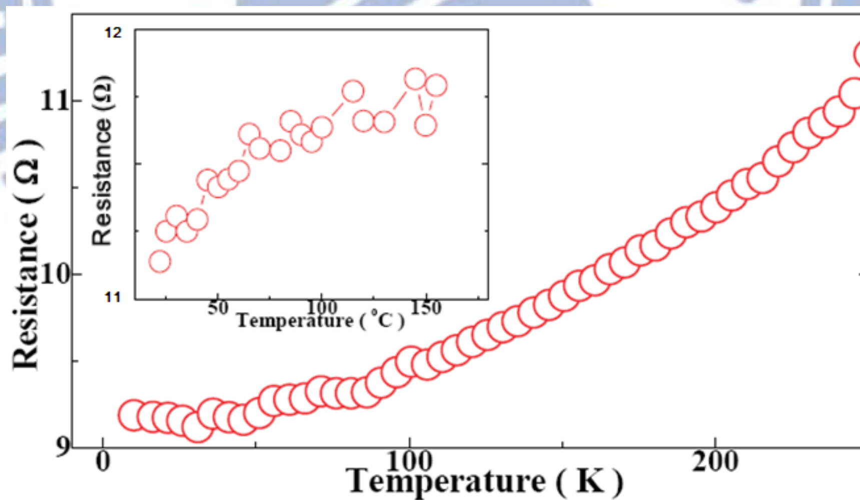

Figure 4-48. The temperature dependent electrical character for low resistance state.

Figure 4-49 shows the temperature effect on both HRS and LRS. The temperature dependent curve of HRS is different from LRS. It is clear to see that the resistance decreases when the temperature is increased. This result indicates the semiconductor behavior on HRS.

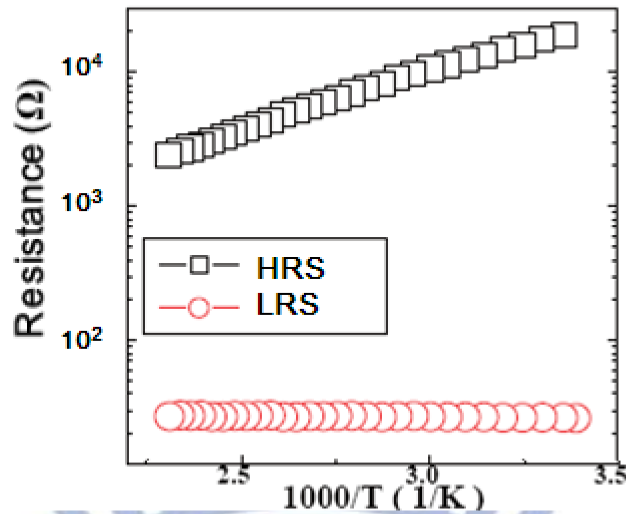

Figure 4-49. The temperature dependent electrical character of WO_x film.

4.4.3 Unipolar Multi-times-programming (MTP) RRAM

The graded WO_x RRAM also shows the potential of unipolar operation. It is clear to observe the unipolar operation when the positive voltage, is applied on top electrode. The HRS can be formed by a short pulse (~100 ns) voltage and LRS can be formed by a longer pulse (1000 ns) voltage. However, we can't observe the unipolar operation with applied negative voltage on top of electrode. Moreover, the oxidation time influences the WO_x thickness and it also influences the maximum value of HRS. For the unipolar WO_x RRAM, it also exhibited good performance of reliability test: cycle endurance above 1000, over 3000 hrs at 150℃ baking, 0.4 V stress above 1000 sec and 10x on/off ratio. Both HRS and LRS show the non-linear I-V curve and they follow the VRH conduction mechanism. With the calculation of VRH equation, we got the hopping distance about 24 and 16Å of HRS and LRS, respectively.

Figure 4-50 shows the resistive switching character by unipolar operation. The resistance state increases with the applied short pulse below 100 ns. When the applied pulse is above 100 ns, the resistance state switches from HRS to LRS. This unipolar operation of our system uses different pulse width (100 ns and 1000 ns for HRS and LRS programming, respectively) and fixes the positive applied voltage about 4V. With this kind of operation, it is easy to switch the resistance state.

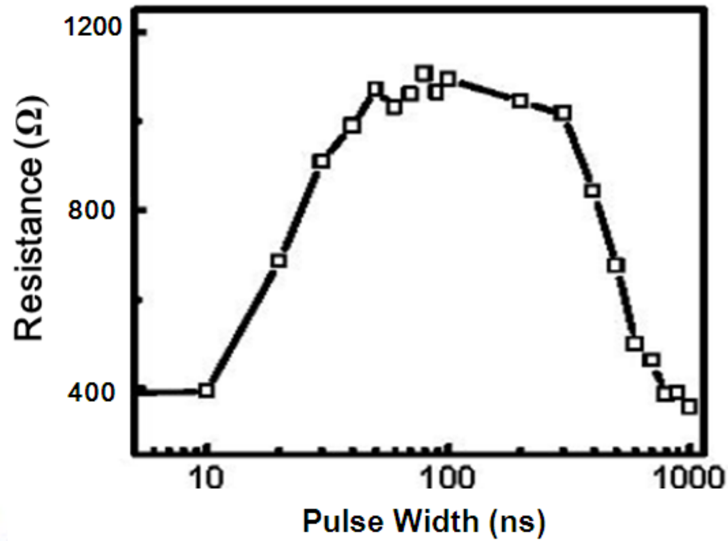

Figure 4-50. The pulse width influence of resistance state.

In our experiment, the oxidation layer is formed by down-stream-plasma process. The thickness of WO_x film is dependent on the oxidation time. Figure 4-51 shows the relationship between sample thickness and oxidation time. The thickness seems not linear dependent with the oxidation time. The thickness of WO_x film is about 90 and 140 Å by 200 and 1600 sec oxidation process, respectively.

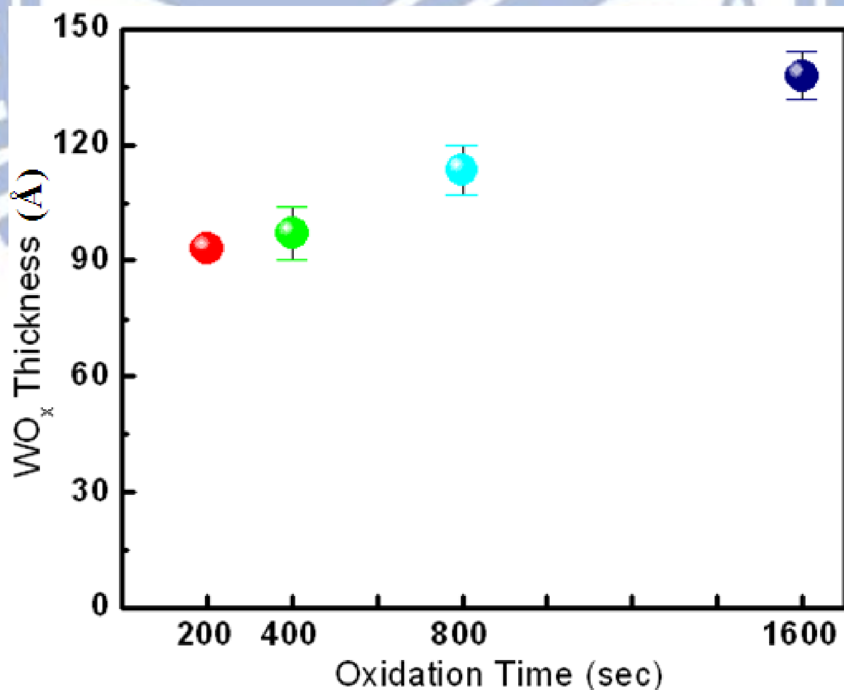

Figure 4-51. The WO_x thickness relationship with different oxidation time.

However, the oxidation time affects only the HRS. Figure 4-52 shows the unipolar resistive switching character with different oxidation time (OT). It is clear to see that a sample with longer oxidation time exhibits higher resistance state. This HRS can be

formed by a short pulse about 50~300 ns. Moreover, all the LRS keeps about 300 Ω by 1000 ns pulse applied. However, the resistive switching character will be damaged when the applied pulse width is over 1000ns.

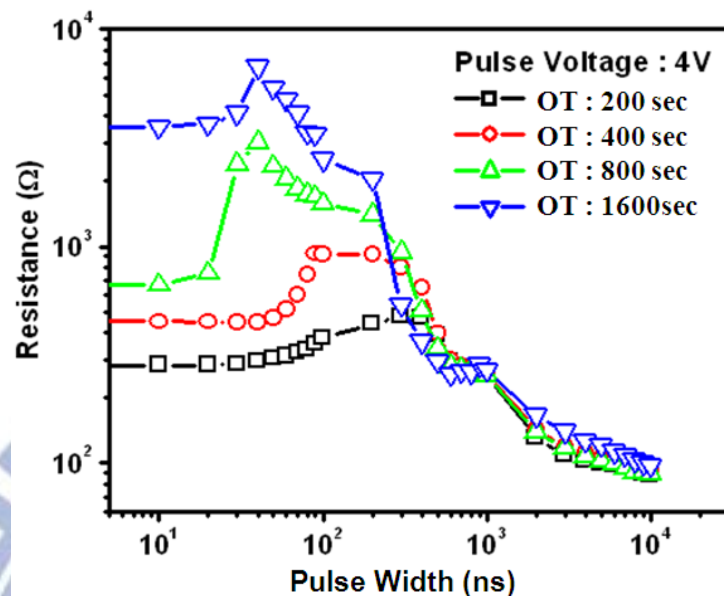

Figure 4-52. The unipolar operation character with different oxidation time.

The unipolar operation can't work out with a negative pulse applied. Figure 4-53 shows the resistance change by using a negative pulse. We can observe that the resistance state decreases when the applied negative voltage is above -3 V. Both short and long pulse can only reduce the resistance state. This result indicates the direction of our WO_x unipolar RRAM.

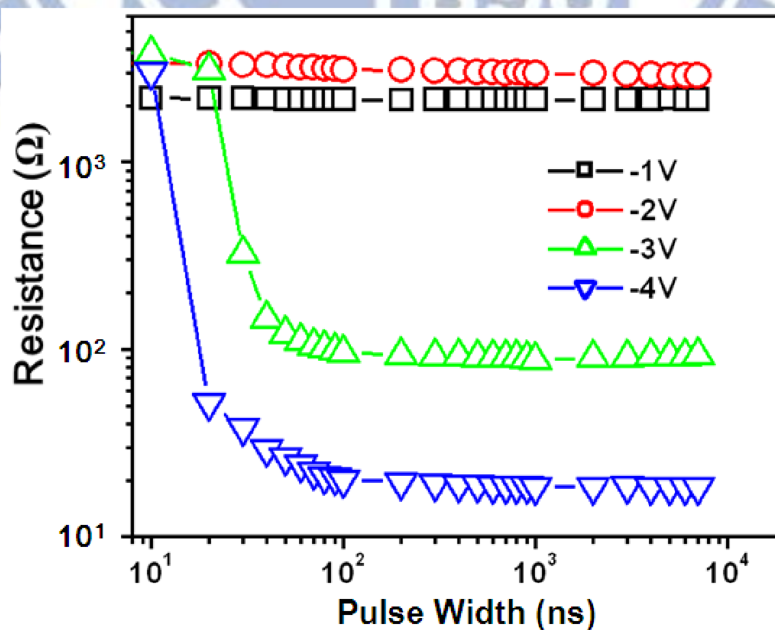

Figure 4-53. The resistance change by using negative voltage with varies pulse width

The unipolar operation RRAM also exhibits good cycle endurance performance. Figure 4-54 shows above 1000 times cycle operation. The on/off ratio is about 170x in the first cycle operation and it keeps about 3x after 1000 times of cycle operation. This result indicates that this unipolar RRAM is promising for non-volatile memory application.

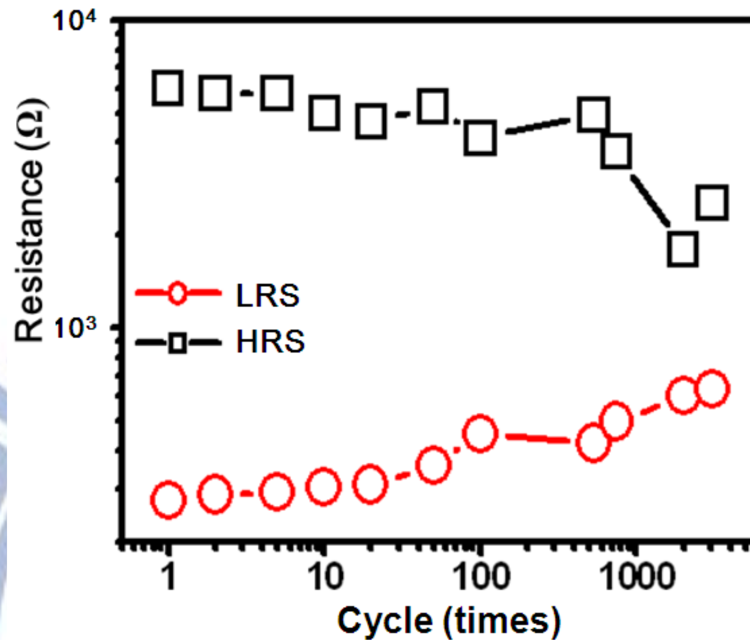

Figure 4-54. The cycle endurance test of unipolar operation

In the thermal stability experiment, the resistance states also exhibited good thermal stability by means of this unipolar operation shown in figure 4-55. Both LRS and HRS kept their resistance state above 3000 hrs at 150℃ baking environment. At higher baking environment about 250℃, those resistance states kept the resistance state above 500 hrs. Moreover, after the high temperature baking experiment at both 150℃ and 250℃, the on/off ratio kept about x10 for a long time.

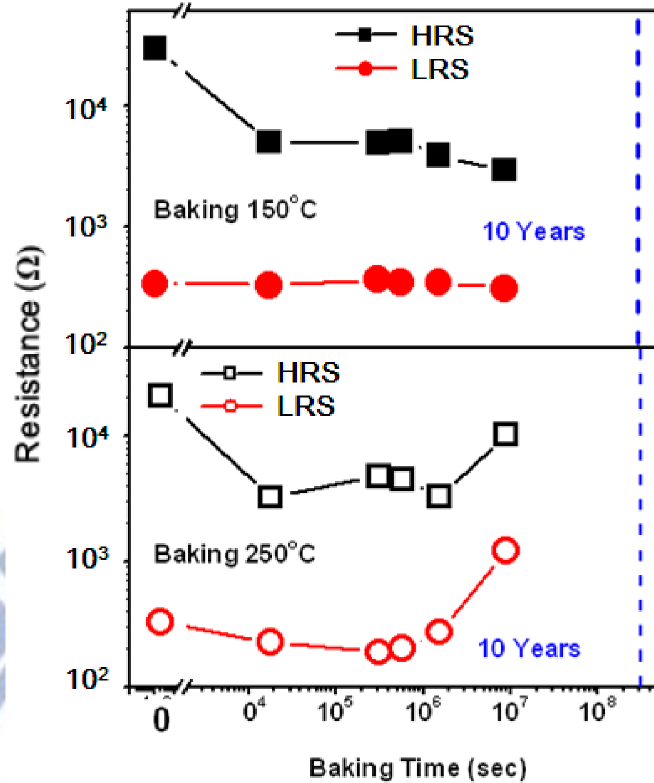

Figure 4-55. The thermal stability of unipolar operation at 150 and 250℃.

Figure 4-56 shows the stress influence on both LRS and HRS. It is clear to see that the HRS always keeps its resistance state when the stress voltage is below 0.6 V. For the LRS, it is clear to see that the resistance increases when the applied stress is above 0.6 V and the increase of resistance is linearly dependent on the stress time. This figure also indicates good stress performance at 0.2 V.

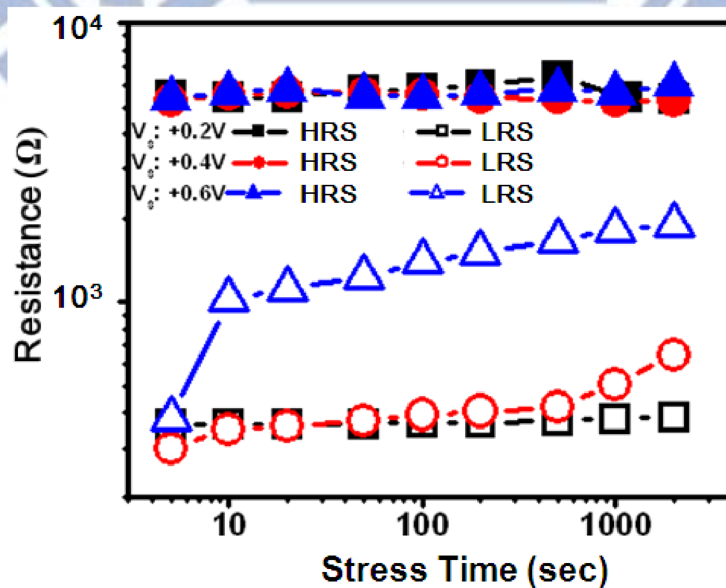

Figure 4-56. The stress influence of unipolar RRAM.

However, the higher stress above 0.6 V affected the HRS. Figure 4-57 shows the influence of HRS with stress voltage above 0.6 V. It is clear to see that the resistance of HRS decreases when the applied stress is above 1 V. Moreover, the resistance state switches to LRS immediately when the applied voltage is about 2 V. This figure also indicates that the HRS kept its memory state over 30 min in stress voltage about 1 V.

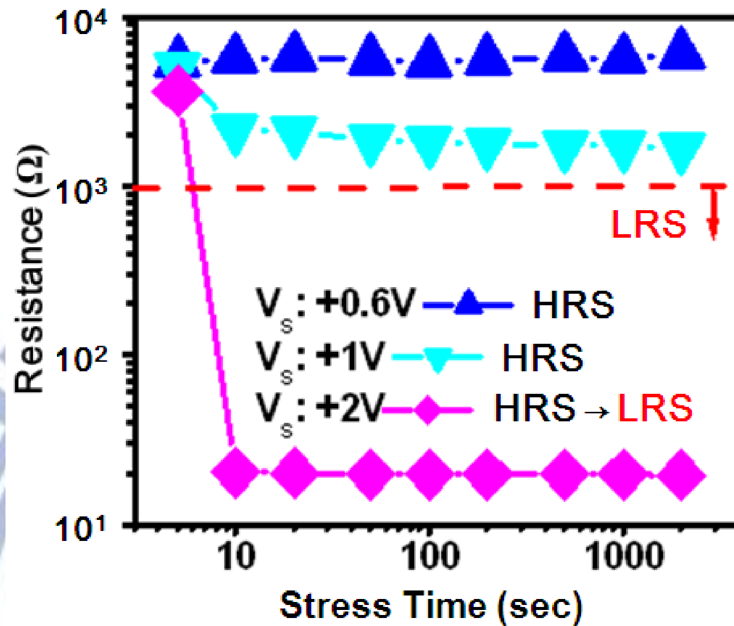

Figure 4-57. The stress test of high resistance state

In the unipolar operation, both LRS and HRS show non-linear I-V curve. Figure 4-58 shows the electric character of those states and the inset shows both I-V curves at the same current scale. Both LRS and HRS follows the VRH conduction mechanism in the unipolar operation. Figure 4-59 shows the temperature dependent on the resistance state. With the calculation of the VRH fitting curve, the hopping distance of LRS and HRS is about 16 and 24Å , respectively.

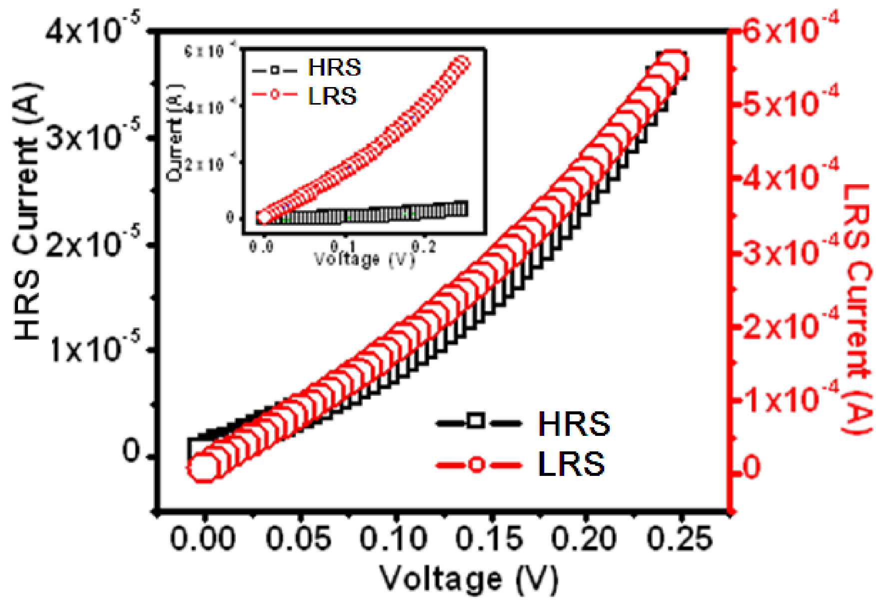

Figure 4-58. The electric character of LRS and HRS.

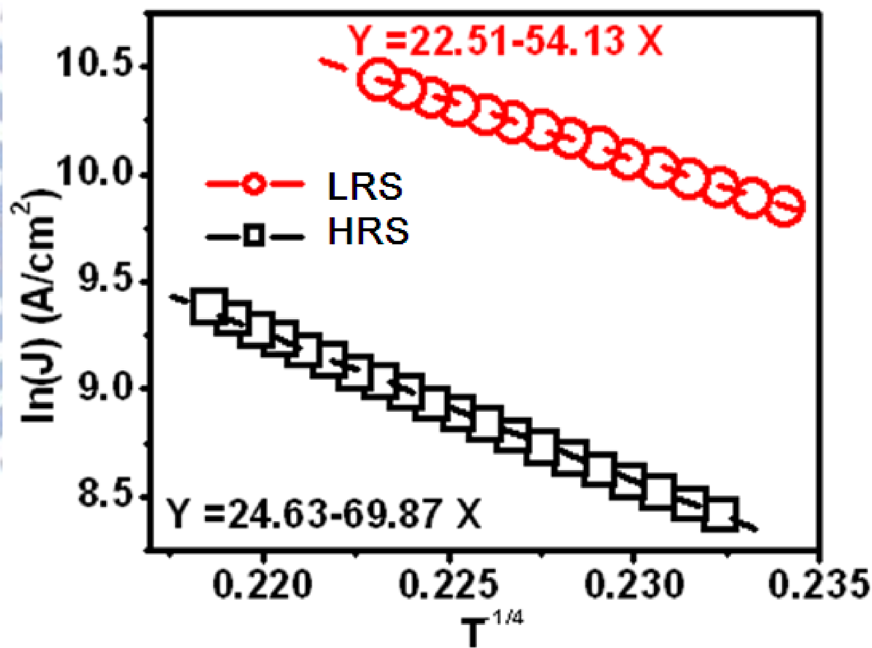

Figure 4-59. The VRH fitting curve of unipolar operation RRAM.

Figure 4-60 shows the change of the hopping distance in the cycle operation. The hopping distance of both states almost overlap after 3000 cycling operation. However, figure 4-54 doesn't show the overlap of both resistance states after 3000 times of cycling operation.

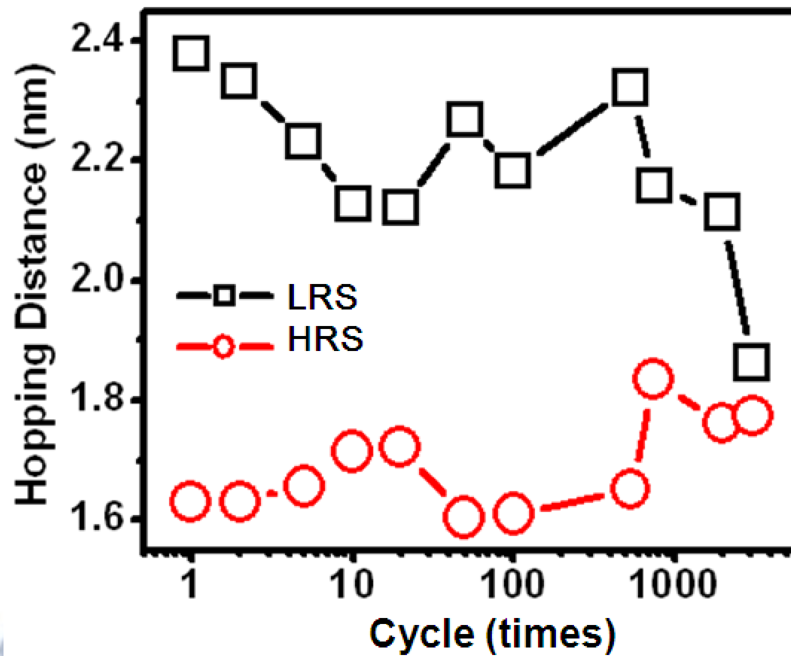

Figure 4-60. The hopping distance varies in the cycle endurance test.

4.4.4 Scaling Effect

In the scaling effect experiment, we used the spacer to shrink the active area on the top of W plug. By controlling the thickness of spacer, we prepared three samples with shrinking ratio from 77% to 37%. In the electric analysis, the V_{th} are dependent on the shrinking ratio. The smaller active area sample exhibited smaller threshold voltage behavior. In other words, the set voltage (switch memory state to HRS) decreases when the active area was reduced. Moreover, the hopping distance and density of state exhibited positive and negative relationship with the shrinking ratio. In the reliability test, the thermal stability was independent on the shrinking ratio. It still showed good performance at 150℃ for long time baking, yet the cycle endurance became poor when we shrinked the active area. It only shows above 50 times cycling performance in our experiment.

Figure 4-61 shows the sketch and TEM image of the scale-down sample. Before the spacer process, we must use the W-plug etching back skill to form a step profile on the top of W-plug. With the thickness control of spacer, we can define the active area on the top of W-plug. After this spacer process, the plasma oxidation is used to form the oxidation layer.

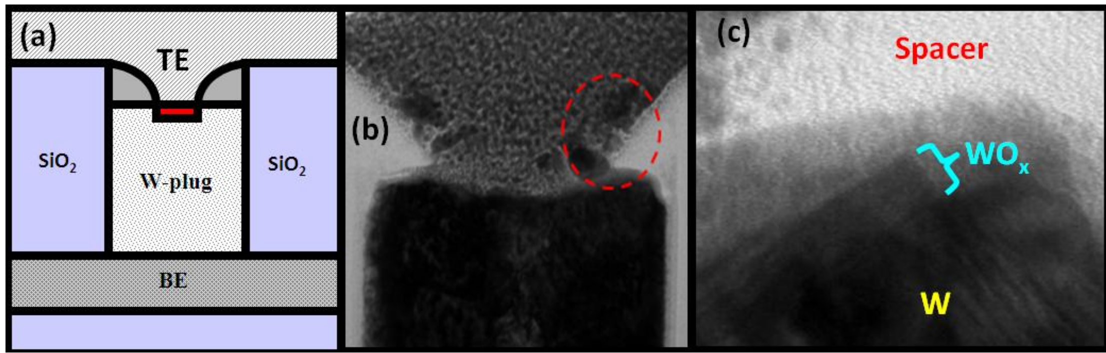

Figure 4-61. (a) the sketch of scaling reducing profile (b) TEM image of scaling reducing experiment (c) The enlarge part of WO_x film.

Figure 4-62 shows the V_{th} test for sample with different shrinking ratio. It is clear to observe that the V_{th} decreases from 5.4 to 3.5 V when the active area is shrinked from 100% to 37%. Moreover, the best conduction of set voltage (V_s) is dependent on this V_{th}. And the relationship between V_s and the shrinking ratio is shown in figure 4-63. This figure indicates that a larger active area sample needs larger applied voltage for switching to HRS.

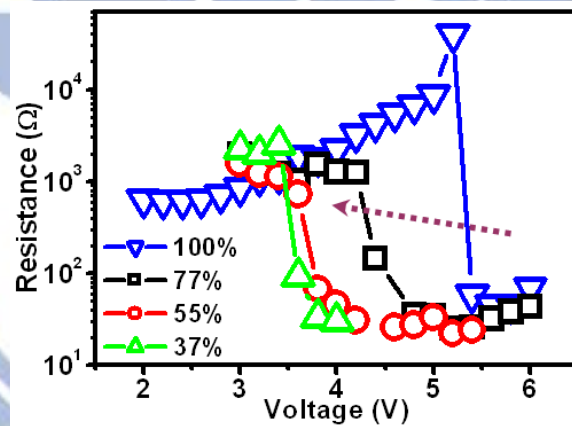

Figure 4-62. The threshold voltage varies with different reducing scale

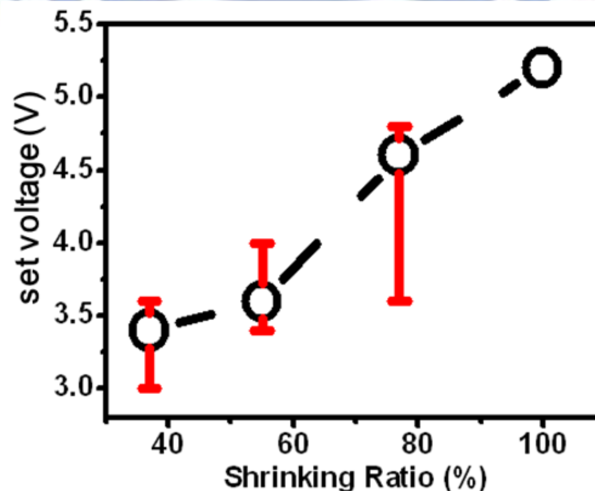

Figure 4-63. The relationship between shrinking ratio and set voltage.

With the calculation of VRH conduction function for HRS, we got the hopping distance and density of state relationship with shrinking ratio. Figure 4-64 shows the hopping distance increases when the active area decreases. However, the density of state (DOS) exhibits the opposite behavior with hopping distance. Due to several unknown parameter of VRH calculation, this figure only shows the trend of the DOS.

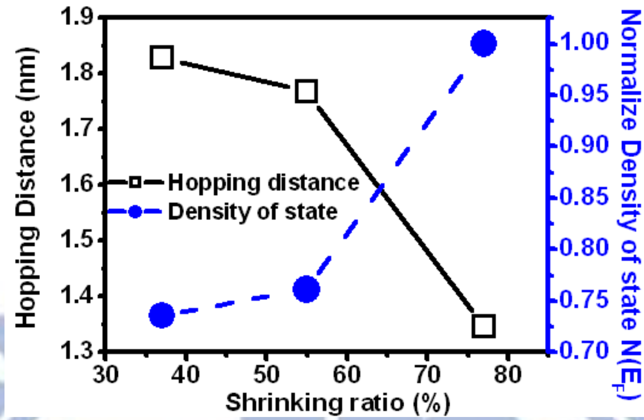

Figure 4-64. The shrinking ratio influence with hopping distance and density of state.

Figure 4-65 shows the thermal stability experiment at 150 ℃ for long time baking with different shrinking samples. In this figure, we found that the thermal stability is independent of the shrinking ratio. Both LRS and HRS kept their memory state at 150 ℃ for 100 hrs baking.

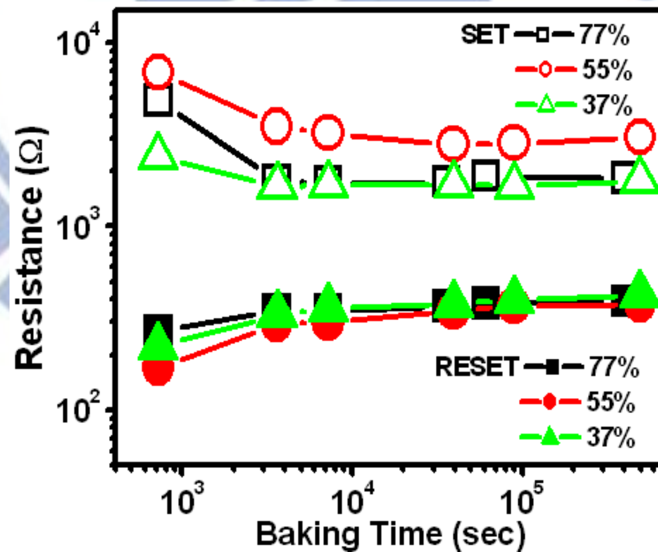

Figure 4-65. The thermal stability with different shrinking ratio.

However, the cycle endurance decreases when we shrink the active area. Figure 4-66 shows the cycle endurance test for those shrinking samples. It may be attributed to the poor programming conduction. With the shrinking of the active area, both “set” and “reset” programming conductions also change at the same time.

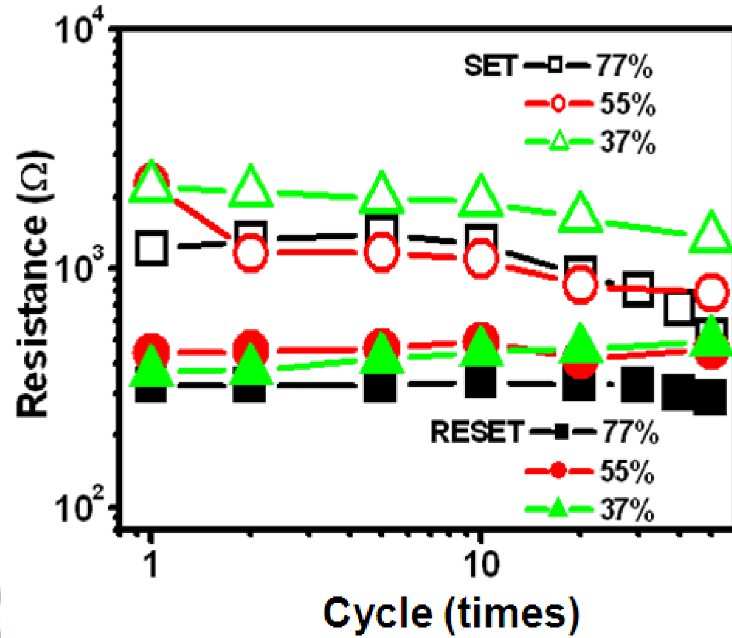

Figure 4-66. The cycle endurance test with different shrinking ratio sample.

4.5Metal-oxide RRAM organization

In the results of our metal-oxide RRAM experiments, three materials, including NiO_x, TiO_x, and WO_x, exhibit the resistive switching character. Both NiO_x and TiO_x exhibit the bipolar resistive switching behavior and their conduction mechanism follows the Schottky emission.

However, the WO_x shows the best RRAM performance in our experiment. Both bipolar and unipolar operation resistive switching character was found in this grade WO_x material. Moreover, this material can also be used for one-time-programming (OTP), multi-time-programming (MTP), and multi-level-cell (MLC) application. It also shows the shrinkable potential and the threshold voltage reducing with the shrinking ratio. Moreover, this WO_x RRAM shows good reliability performance, including better cycle endurance, good thermal stability, better stress performance, and good data retention. The conduction mechanism of high and low resistance state is variable-range-hopping (VRH) and the minimum-metal-conductivity (MMC), respectively.

Chapter 5 : Summary

We have demonstrated the CMOS fully compatible NiO_x, TiO_x, and WO_x based resistance random access memories successfully in this study. All three materials exhibit clear bistable resistive switching character and their resistive characters show the relationship between barrier high and on/off ratio.

Polycrystalline NiO_x shows the RRAM performance relationship between thin film and the oxygen content. Its conduction mechanism follows the Schottky emission, and the Schottky emission curve shows the relationship between dielectric constant and oxygen content. According to the calculation of this curve, samples with low oxygen content have a higher dielectric constant. This result explains that samples with low oxygen content need more applied voltage to countervail the inner opposite electric field in the resistive switching process.

Although TiO_x follows the Schottky emission, the electric character exhibits the interface contribution and thickness independence relationship. TiO_x / SiO_2 hybrid system also indicates that the interface contribution and the performance of data retention, cycle endurance, and read disturb can be improve by this hybrid system.

However, the WO_x based RRAM shows more potential than others in the non-volatile memory application such as one-time-programming (OTP), multi-times-programming (MTP), multi-level-cell (MLC), shrinkable memory cell, and the unipolar operation. The conduction mechanism of tungsten oxide follows variable-range-hopping (VRH) in high resistance state (HRS) and the electrical behavior of low resistance state (LRS) is close to minimum-metal-conductivity (MMC). Moreover, the good performance such as high on/off ratio (>1000), good cycle endurance (>1000), high thermal stability (>2000 hrs at 250℃), good read disturb (>1000 sec at 1V), high speed operation (<10ns), small cell size (~9nm), and low power consumption (<10uA) of tungsten oxide based RRAM shows highly potential for the next generation non-volatile memory applications.

According to the results of this study, all three NiO_x, TiO_x and WO_x are CMOS fully compatible materials without contamination risk. For the overall comparison of RRAM functionality, NiO_x or TiO_x cannot provide better characteristics than WO_x. The WO_x based RRAM could provide high potential for several commercial applications on electron devices, such as OTP, MTP, MLC, and unipolar operation as well. Therefore, we believe it is suitable for application in the next generation non-volatile memory device.

References

[1]. Yiran Chen, Wei Tian, Hai Li, Xiaobin Wang and Wenxhong Zhu, "PCMO Device With High Switching Stability", IEEE Electron Device Lett., vol.31, no.8, p.866,Aug. (2010).

[2]. S. Q. Liu, N. J. Wu and A. Ignatiev, "Electric-pulse-induced reversible resistance change effect in magnetoresistive film", Appl. Phys. Lett., vol.76, p.2749, (2000).

[3]. S. T. Hsu, W. W. Zhung, T. K. Li, W. Pan, A. Ignative, C. Papagianni and N. J. Wu, "RRAM Switching Mechanism", Symposium NonVolatile Memory Technology, p.121, (2005).

[4]. W. W. Zhuang, W. Pan, B. D. Ulrich, J. J. Lee, L. Stecker, A. Burmaster, D. R. Evans, S. T. Hsu, M. Tajiri, A. Shimaoka, K. Inoue, T. Naka, N. Awaya, K. Sakiyama, Y. Wang, S. Q. Liu, N. J. Wu and A. Ignatie, "Novell Crossal Magnetoresistive Thin Film Nonvolatile Resistance Random Access Memory", International Electron Devices Meeting (IEDM), p.193, (2002).

[5]. R. C. G. Naber, B. de Boer, P. W. Blom and D. M. de Leeuw, "Low-voltage polymer field-effect transistor for nonvolatile memories" Appl. Phys. Lett., vol.87, p.203509, (2005).

[6]. Ronald C. G. Naber, Cristina Tanase, Paul W. M. Blom, Gerwin H. Gelinck, Albert W. Marsman, Fred J. Touwslager, Aepas Setayesh and Dago M. De Leeuw, "High-performance solution-processed polymer ferroelectric field-effect transistors" Nature Mater., 4, p.243, (2005).

[7]. Ricky J. Tseng, Jiaxing Huang, Jianyong Ouyang, Richard B. Kaner and Yang Yang, "Polyaniline Nanofiber/Gold Nanoparticle Nonvolatile Memory" Nano Lett., vol.5, p.1077, (2005).

[8]. Qi-Dan Ling, Siew-Lay Lim, Yan Song, Chun-Xiang Zhu, Daniel Siu-Hhung Chan, En-Tang Kang and Koon-Gee Neoh, "Nonvolatile Polymer Memory Device Based on Bistable Electrical Switching in a Thin Film of Poly(N-vinylcarbazole) with Covalently Bonded C_{60}^{+}" J. Am. Chem. Soc. vol.23, p.312, (2007).

[9]. Qidan Ling, Yan Song, Shi J. Ding, Chunxiang Zhu, Daniel S. H. Chan, Dim-Lee Kwong, En-Tang Kang, and Koon-Gee Neoh, "Non-Volatile Polymer Memory Device Based on a Novel Copolymer of N-Vinylcarbazole and Eu-Complexed Vinylbenzoate", Adv. Mater., vol.17, p.455-459, (2005).

[10]. Michael Kund, Gerhard Beitel, Cay-Uwe Pinnow, Thmas Rohr, Jorg Schumann, Ralf Symanczyk, Klaus-Dieter Ufert and Gerhard Muller, "Conductive bridging RAM (CBRAM) An emerging non-volatile memory technology scalable to sub 20nm", International Electron Devices Meeting (IEDM), p.754, (2005).

[11]. Stefan Dietruch, Michael Angerbauer, Milena Ivanov, Dietmer Gogl, Hoenigshmid, Michael Kund, Corvin Liaw, Michael Markert, Ralf Symanczyk, Laith Altimime, Serge Bournat, and Gerhard Mueller, "A Nonvolatile 2-Mbit CBRAM Memory Core Fraturing Advanced Read and Program Control", IEEE J. Sol. Sat. Cir., vol.42, p.839, (2007).

[12]. Chakravarthy Gopalan, Yi Ma, Tony Gallo, Janet Wang, Ed Runnion, Juan Saenz, Foroozan Koushan, and Shane Hollmer, "Demonstration of Conductive Bridging Random Access Memory (CBRAM) in Logic CMOS Process", International Memory Workshop (IMW), (2010).

[13]. A. Beck, J. G. Bednorz, Ch Gerber, C. Rossel, and D. Widmer, "Reproducible switching effect in thin oxide films for memory applications" Appl. Phys. Lett., vol.77, p139, (2000).

[14]. S. B. Lee, A. Kim, J. S. Lee, S. H. Chang, H. K. Yoo, T. W. Noh, B. Kahng, M. –J. Lee, C. J. Kim, and B. S. Kang, "Reduction in high reset currents in unipolar resistance switching Pt/$SrTiO_x$/Pt capacitors using acceptor doping" Appl. Phys. Lett., vol.97, p093505, (2010).

[15]. M. Copel, J. D. Baniecki, P. R. Duncombe, D. Kotecki, R. Laibowitz, D. A. Neumayer, and T. M. Shaw, "Compensation doping of $Ba_{0.7}Sr_{0.3}TiO_3$ thin films" Appl. Phys. Lett., vol.73, p1832, (1998).

[16]. M. Meier, R. Rosezin, S. Gilles, A. Rudiger, C. Kugeler and R. Waser, "A multilayer RRAM nanoarchitecture with resistively switching Ag-doped spin-on glass", Ultimate Integration of Silicon (ULIS), p.143, (2009).

[17]. Haowei Zhang, Bin Gao, Shimeng Yu, Lin Lai, Lang Zeng, Bing Sun, Lifeng Liu, Xiaoyan Liu, Jing Lu, Ruqi Han and Jinfeng Kang, "Effects of Ionic Doping on the Behaviors of Oxygen Vacancies in HfO_2 and ZrO_2: A First Principles Study" Simulation of Semiconductor Processes and Devices (SISPAD), (2009).

[18]. Haowei Zhang, Bin Gao, Bing Sun, Guopeng Chen, Lang Zeng, Lifeng Liu, Xiaoyan Liu, Jing Lu, Ruqi Han, Jinfeng Kang, and Bin Yu, "Ionic doping effect in ZrO_2 resistive switching memory" Appl. Phys. Lett., vol.96, p123502, (2010).

[19]. Hyunjun Sim, Hyejung Choi, Dongsoo Lee, Man Chang, Dooho Choi, Yunik Son, Eun-Hong Lee, Wonjoo Kim, Yoondong Park, In-Kyeong Yoo and Hyunsang Hwang, "Excellent resistance switching characteristics of Pt/$SrTiO_3$ Schottky junction for multi-bit nonvolatile memory application", International Electron Devices Meeting (IEDM), p.758, (2005).

[20]. ChiaHua Ho, E. K. Lai, M. D. Lee, C. L. Pan, Y. D. Yao, K. Y. Hsieh, Rich Liu, and C. Y. Lu, "A Highly Reliable Self-Aligned Graded Oxide WO_x Resistance Memory: Conduction Mechanisms and Reliability", Symposium of VLSI Technology, p.228, (2007).

[21]. J. C. Bruyeye and B. K. Chakraverty, “Switching and negative resistance in thin films of nickel oxide”, Appl. Phys. Lett., vol.16, p40, (1970).
[22]. F. Argall, “Switching phenomena in titanium oxide thin films”, Solid-State Electron. vol.11, p.535, (1968).
[23]. C. H. Cheng, Albert Chin, and F. S. Yeh, “Novel Ultra-low power RRAM with good endurance and retention”, Symposium of VLSI Technology, p.85, (2010).
[24]. Wei-Chih Chien, Erh-Kun Lai, Kuo-Pin Chang, Chien-Hung Yeh, Ming-Hsiang Hsueh, Yeong-Der Yao, Tuung Luoh, Sheng-Hui Hsieh, T. H. Yang, K. C. Chen, Yi-Chou Chen, Kuang-Yeu Hsieh, Rich Liu, and Chih-Yuan Lu, “Unipolar Switching Characteristics for Self-Aligned WO_x Resistance RAM (R-RAM)”, International Symposium on VLSI Technology Systems and Applications (VLSI-TSA), p.144, (2008).
[25]. W. R. Hiatt and T. W. Hickmott., “Bistable switching in niobium oxide diodes” Appl. Phys. Lett., vol,6, p106, (1965).
[26]. K. L. Chopra, “Avalanche-Induced Negative Resistance Thin Oxide Films”, J. Appl. Phys., vol.36, p.184, (1965).
[27]. ChiaHua Ho, Cho-Lun Hsu, Chun-Chi Chen, Jan-Tsai Liu, Cheng-San Wu, Chien-Chao Huang, Chenming Hu, and Fu-Liang Yang, “9nm Half-Pitch Functional Resistive Memory Cell with <1uA Programming Current Using Thermally Oxidized Sub-Stoichiometric WO_x Film”, International Electron Devices Meeting (IEDM), 19.1, (2010).
[28]. W. C. Chien, Y. C. Chen, K. P. Chang, E. K. Lai, Y. D. Yao, P, Lin, J. Gong, S. C. Tsai, S. H. Hsieh, C. F. Chen, K. Y. Hsieh, R. Liu, and Chih-Yuan Lu, “Multi-Level Operation of Fully CMOS Compatible WO_x Resistive Random Access Memory (RRAM)”, International Memory Workshop (IMW), (2009).
[29]. ChiaHua Ho, Ming-Daou Lee, Chen-Ling Pan, Erh-Kun Lai, Yeong- Der Yao, Kuang-Yeu Hsieh, Rich Liu, and Chih-Yuan Lu, “A 2-bit/cell, Maskless, Self-Aligned Resistance Memory with Thermal Stability”, International Symposium on VLSI Technology Systems and Applications (VLSI-TSA), (2007).
[30]. K. Kahng and S. M. Sze, “A floating gate and its application to memory devices”, Solid-State Device Research Conference, vol.14, p.629, (1967).
[31]. Masukoa;Fujio, Iizuka; Hisakazu, “Semiconductor memory device and method for manufacturing the same”, US4531203
[32]. Yasuo Itoh, Masaki Momodom, Riichiro Shirota, Yoshihisa Iwata, Ryozo Nakayama, Ryouhei Kirisawa, Tomoharu Tanaka, Koichi Toita, Satoshi Inoue and Fujio Masuoka, “An Experimental 4Mb CMOS EEPROM with a NAND Structured Cell”, International Solid-State Circuits Conference (ISSCC), p.134, (1989).

[33]. Vicent Cros, Albert Fert, Pierre Seneor and Fredencric Petroff, “The 2007 Nobel Prize in Physics: Albert Fert and Petter Grunberg”, The Spin Progress in Mathematical Physics, vol.55, p.147, (2009).

[34]. T. Miyazaki and N. Tezuka, “Giant magnetic tunneling effect in Fe/Al_2O_3/Fe junction”, J. Magn. Magn. Mater., vol.139, p.L231 (1995).

[35]. J. F. Gibbons, and W. E. Beadle, ”Switching properties of NiO films” Solid-State Electron, vol.7, p.785, (1964).

[36]. W. C. Chien, Y. C. Chen, E. K. Lai, Y. D. Yao, P. Lin, S. F. Horng, J. Gong, T. H. Chou, H. M. Lin, M. N. Chang, Y. H. Shih, K. T. Hsieh, R. Liu, and Chih-Yuan Lu, “Unipolar Switching Behavior of WO_x RRAM”, IEEE Electron Device Lett., vol.31, no.2, p126, (2010).

[37]. Y. H. Tseng, C. E. Huang, C. –H. Kuo, Y. –D Chih, Y. C. King, and C. J. Lin, “A New High-Density and Ultrasmall-Cell-Size Contact RRAM (CR-RAM) With Fully CMOS-Logic-Compatible Technology and Circuits”, IEEE Trans. on Electron Devices, vol.58, p.53, (2011).

[38]. Keiji Hosotani, Seong-Geon Park, Yoshio Nishi, “Electric field dependent switching and degradation of Resistance Random Access Memory”, IEEE International Integrated Reliability Workshop (IRW) Final Report, p.11, (2009)

[39]. Sungho Kim, Hanul Moon, Dipti Gupta, Seunghyup Yoo, and Yang-Kyu Choi, “Resistive Switching Characteristics of Sol-Gel Zinc Oxide Films for Flexible Memory Applications”, IEEE Trans. on Electron Devices, vol.56, p.696, (2009).

[40]. K. Tsunoda, K. Kinoshita, H. Noshiro, Y. Yamazaki, T. Iizuka, Y. Ito, A. Takahashi, A. Okano, Y. Sato, T. Fukano, M. Aoki, and Y. Sugiyama, “Low Power and High Speed Switching of Ti-doped NiO ReRAM under the Unipolar Voltage Source of less than 3V”, International Electron Devices Meeting (IEDM), p.767, (2007).

[41]. X. P. Wang, Y. Y. Chen, L. Pantisano, L. Goux, M. Jurczak, G. Groeseneken, and D. J. Wouters, “Effect of anodic interface layers on the unipolar switching of HfO_2-based resistive RAM”, International Symposium on VLSI Technology Systems and Applications (VLSI-TSA), p.140, (2010).

[42]. W. C. Chien, Y. R. Chen, Y. C. Chen, Alfred T. H. Chuang, F. M. Lee, Y. Y. Lin, E. K. Lai, Y. H. Shih, K. Y. Hsieh, and Chih-Yuan Lu, “A forming-free WO_x resistive memory using a novel self-aligned field enhancement feature with excellent reliability and scalability”, International Electron Devices Meeting (IEDM), 19.2, (2010).

[43]. B. Chen, B. Gao, S. W. Sheng, L. F. Liu, X. Y. Liu, Y. S. Chen, Y. Wang, R. Q. Han, B. Yu, and J. F. Kang, “A Novel Operation Scheme for Oxide-Based Resistive-Switching Memory Devices to Achieve Controlled Switching Behaviors”, IEEE Electron Device Lett., vol.32, no.3, p282, (2011).

[44]. Jubong Park, Minseok Jo, Seungjae Jung, Joonmyoung Lee, Wootae Lee, Seonghyun Kim, Sangsu Park, Jungho Shin, and Hyunsang Hwang, "New Set/Reset Scheme for Excellent Uniformity in Bipolar Resistive Memory", IEEE Electron Device Lett., vol.32, no.3, p228, (2011).

[45]. M. D. Lee, C. H. Ho, C. K. Lo, T. Y. Peng, Y. D. Yao, "Effect of Oxygen Concentration on Characteristics of NiO-Based Resistance Random Access Memory", IEEE Trans. Magn., vol.43, p.939, (2007).

[46]. Linkai Wang, Ze Jia, and Tianling Ren, "Bipolar switching analysis and negative resistance phenomenon in TiO_x-based devices", IEEE International Conference of Electron Devices and Solid-Sate Circuits (EDSSC), (2010).

[47]. Ugo Russo, Carlo Cagli, "Filament Conduction and Reset Mechanism in NiO-Based Resistive-Switching Memory (RRAM) Devices", IEEE Trans. on Electron Devices, vol.56, p.186, (2009).

[48]. U. Russo, D. Ielmini, C. Cagli, A. Lacaita, S. Spiga, C. Wiemer, M. Perego, and Fanciulli, "Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM", International Electron Devices Meeting (IEDM), p.775, (2007).

[49]. Jung Won Seo, Jae-Woo Park, Keong Su Lim, Ji-Hwan Tang, and Sang Jung Kang, "Transparent resistive random access memory and its characteristics for nonvolatile resistive switching" Appl. Phys. Lett., vol.93, p223505, (2008).

[50]. Shimeng Yu, Ximeng Guan, and H. –S. Philip Wong, "Conduction mechanism of TiN/HfO_x/Pt resistive switching memory: A trap-assisted-tunneling model" Appl. Phys. Lett., vol.99, p063507, (2011).

[51]. Kyung-Chang Ryoo, Jeong-Hoon Oh, Hongsik Jeong, and Byung-Gook Park, "Irregular resistive switching characteristics and its mechanism based NiO unipolar switching resistive random access memory (RRAM)", Silicon Nanoelectronics Workshop (SNW), (2010).

[52]. C. Rossel, G. I. Meijer, D. Bremaud, and D. Widmer, "Electrical current distribution across a metal-insulator-metal structure during bistable switching", J. Appl. Phys., vol.90, p.2892, (2001).

[53]. J. Y. Son, and Y. –H Shin, "Direct observation of conducting filaments on resistive switching of NiO thin films" Appl. Phys. Lett., vol.92, p222106, (2008).

[54]. Bin Gao, Bing Sun, Haowei Zhang, Lifeng Liu, Xiaoyan Liu, Ruqi Han, Jinfeng Kang, and Bin Yu, "Unified Physical Model of Bipolar Oxide-Based Resistive Switching Memory", IEEE Electron Device Lett., vol.30, no.12, p1326, (2009).

[55]. Nuo Xu, Lifeng Liu, Xiao Sun, Xiaoyan Liu, Dedong Han, Yi Wang, Ruqi Han, Jinfeng Kang, and Bin Yu, "Characteristics and mechanism of conduction/set process in TiN/ZnO/Pt resistance switching random-access memories" Appl. Phys. Lett., vol.92, p232112, (2008).

[56]. Daniele Ielmini, "Reset-Set Instability in Unipolar Resistive-Switching Memory", IEEE Electron Device Lett., vol.31, no.6, p552, (2010).
[57]. Sungho Kim, and Yang-Kyu Choi, "A Comprehensive Study of the Resistive Switching Mechanism in Al/TiO_x/TiO_2/Al Structure RRAM", IEEE Trans. on Electron Devices, vol.56, p.3049, (2009).
[58]. B. Chen, Q. Y. Jun, B. Gao, F. F. Zhang, K. L. Wei, Y. S. Chen, L. F. Liu, X. Y. Liu, J. F. Kang, and R. Q. Han, "A compact model of resistive switching devices", IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), p.1829, (2010).
[59]. Ugo Russo, Carlo Cagli, "Self-Accelerated Thermal Dissolution Model for Reset Programming in Unipolar Resistive-Switching Memory (RRAM) Devices", IEEE Trans. on Electron Devices, vol.56, p.193, (2009).
[60]. Kyung-Chang Ryoo, Jeong-Hoon Oh, Sung-hun Jung, and Byung-Gook Park, "Resistive switching characteristics of novel Al-inserted resistive random access memory (RRAM)", IEEE Nanotechnology Materials and Devices Conference (NMDC), p.356, (2010).
[61]. O. Ginez, J. –M. Portal, and Ch. Muller, "Design and Test Challenges in Resistive Switching RAM (ReRAM): An Electrical Model for Defect Injections", IEEE European Test Symposium, p.61, (2009).
[62]. F. N. Mott, et al., Electronic Processes in Nan-Crystalline Materials, Oxford: Clarendon Press, pp 28-33, P.37, (1979).
[63]. Juraj Racko, Mlroslav Mlkolasek, Ralf Granzner, Juraj Breza, Danlel Donoval, Alena Grmanova, Ladlslav Harmatha, Frank Schwlerz, and Karol Frohlich, "Trap-assisted tunneling current in MIM structure", Central European Journal of Physics, 230, (2011)
[64]. D. Lee, D. –j. Seong, H. J. Choi, I. Jo, R. Dong, W. Xiang, S. Oh, M. Pyun, S. Seo, S. Heo, M. Jo, D. –K. Hwang, H. K. Park, M. Chang, and M. Hasan, "Excellent uniformity and reproducible resistive switching characteristics of doped binary metal oxide for non-volatile resistance memory applications", IEDM Tech. Dig., p.796 (2006).
[65]. D. S. Jeong, H. Schroeder, and R. Waser, "Impedance spectroscopy of TiO2 thin films switching resistive switching" Appl. Phys. Lett. vol.89, p082909, (2006).
[66]. B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg, and S. Tiedke, "Resistive switching mechanism of TiO_2 thin films grown by atomic-layer deposition", J. Appl. Phys. vol.98, p.033715, (2005).
[67]. A. Sawa, T. Fuji, M. Kawasaki, and Y. Tokura, "Hysteretic current-voltage characteristics and resistance switching at a rectifying Ti/$Pr_{0.7}Ca_{0.3}MnO_3$ interface" Appl. Phys. Lett. vol.85, p4073, (2004).

[68]. M. Fujimoto, H. Koyama, M. Konagai, Y. Hosoi, K. Ishihara, S. Ohnishi, and N. Awaya, “TiO_2 anatase nanolayer on TiN thin film exhibiting high-speed bipolar resistive switching” Appl. Phys. Lett. vol.89, p223509, (2006).

[69]. M. J. Rozenberg, I. H. Inoue, and M. J. Sanchez, “Nonvolatile Memory with Multilevel Switching: A Basic Model”, Phys. Rev. Lett. vol.92, p.178302, (2004).

[70]. D. C. Kim, S. Seo, S. E. Ahn, D. –S. Suh, M. J. Lee, B. –H. Park, I. K. Yoo, I. G. Baek, H. –J. Kim, E. K. Yim, J. E. Lee, S. O. Park, H. S. Kim, U. –I. Chung, J. T. Moon, and B. I. Ryu, “Electrical observations of filamentary conductions for the resistive memory switching in NiO films” Appl. Phys. Lett. vol.88, p202102, (2006).

[71]. W. Guan, S. Long, Q. Liu, M. Liu, and W. Wang, “Nonpolar Nonvolatile Resistive Switching in Cu Doped ZrO_2”, IEEE Electron Device Lett., vol.29, no.5, p434, (2008).

[72]. Ugo Russo, Carlo Cagli, and Andrea L. Lacaita, “Filament Conduction and Reset Mechanism in NiO-Based Resistive-Switching Memory (RRAM) Devices”, IEEE Trans. on Electron Devices, vol.56, p.186, (2009).

[73]. R. Fors, S. I. Khartsev, and A. M. Grishin, “Giant resistance switching in metal-insulator-magnetite junctions: Evidence for Mott transition”, Phys. Rev. B, vol.71, p.045305, (2005).

[74]. E. Y. Tsymbal and H. Kohlstedt, “Tunneling Across a Ferroelectric”, Science, vol.313, p.181, (2006).

[75]. B. Gao, H. W. Zhang, S. Yu, B. Sun, L. F. Liu, X. Y. Liu, Y. Wang, R. Q. Han, J. F. Kang, B. Yu, and Y. Y. Wang, “Oxide-based RRAM: Uniformity improvement using a new material-oriented methodology”, Symposium of VLSI Technology, p.30, (2009).

[76]. K. Kinoshita, T. Tamura, H. Aso, H. Noshiro, C. Yoshida, M. Aoki, Y. Sugiyama, and H. Tanaka, “New Model Proposed for Switching Mechanism of ReRAM”, Non-Volatile Semiconductor Memory Workshop (NVSMW), p.84, (2006).

[77]. D. Ielmini, F. Nardi, C. Cagli, and A. L. Lacaita, ”Trade-off between data retention and reset in NiO RRAMs”, International Reliability Physics Symposium (IRPS), p.620, (2010).

[78]. X. A. Tran, H. Y. Yu, Y. C. Yeo, L. Wu, W. J. Liu, Z. R. Wang, Z. Fanf, K. L. Pey, X. W. Sun, A. Y. Du, B. Y. Nguyen, and M. F. Li, “A High-Yield HfO_x-Based Unipolar Resistive RAM Employing Ni Electrode Compatible With Si-Diode Selector for Crossbar Integration”, IEEE Electron Device Lett., vol.32, no.3, p396, (2011).

[79]. Jong Yeog Son, Young-Han Shin, Hyungjun Kim, and Hyun M. Jang, “NiO Resistive Random Access Memory Nanocapacitor Array on Graphene”, ACS Nano, vol.4, p.2655, (2010).

[80]. S. H. Chang, S. C. Chae, S. B. Lee, C. Liu, T. W. Noh, J. S. Lee, B. Kahng, J. H. Jang, M. Y. Kim, D. –W. Kim, and C U. Jung, "Effects of heat dissipation on unipolar resistance switching in Pt/NiO/Pt capacitors" Appl. Phys. Lett., vol.92, p183507 (2008).

[81]. J. Y. Son, and Y. –H. Shin, "Direct observation of conducting filament on resistive switching of NiO thin films" Appl. Phys. Lett., vol.92, p222106, (2008).

[82]. Daniele Ielmini, Carlo Cagli, and Andrea L. Lacaita, v.31, no.4, 353, (2010).

[83]. I. G. Beak, M. S. Lee, S. Seo, M. J. Lee, D. H. Seo, D. –S. Suh, J. C. Park, S. O. Park, H. S. Kim, I. K. Yoo, U-In Chung, and J. T. Moon, "Highly scalable nonvolatile resistive memory using simple binary oxide driven by asymmetric unipolar voltage pulse", International Electron Devices Meeting (IEDM), p.587, (2004).

[84]. Kyung-Chang Ryoo, Silicon Nanoelectronics Workshop (SNW), the same with ref.51.

[85]. Y. S. Chen, B. Chen, B. Gao, F. F. Zhang, Y. J. Qiu, G. J. Lian, L. F. Liu, X. Y. Liu, R. Q. Han, and J. F. Kang, "Anticrosstalk characteristics correlated with the set process for α-Fe_2O_3/Nb-$SrTiO_3$ stack-based resistive switching device" Appl. Phys. Lett., vol.97, p262112, (2010).

[86]. B. Gao, S. Yu, N. Xu, L. F. Liu, B. Sun, X. Y. Liu, R. Q. Han, J. F. Kang, B. Yu, and Y. Y. Wang, "Oxide-based RRAM switching mechanism: Anew ion-transport-recombination model", International Electron Devices Meeting (IEDM), 22.8, (2008).

[87]. Jubong Park, K. P. Biju, Seungjae Jung, Wootae Lee, Joonmyoung Lee, Seonghyun Kim, Sangsu Park, Jungho Shin, and Hyunsang Hwang, "Multibit Operation of TiO_x-Based ReRAM by Schottky Barrier Height Engineering", IEEE Electron Device Lett., vol.32, no.4, p476,(2011).

[88]. W. C. Chien, Y. C. Chen, E. K. Lai, Y. D. Yoa, P. Lin, S. F. Horng, J. Gong, T. H. Chou, H. M. Lin, M. N. Chang, Y. H. Shih, K. Y. Hsieh, R. Liu, and Chih-Yuan Lu, "Unipolar Switching Behaviors of WO_x RRAM", IEEE Electron Device Lett., vol.31, no.2, p126, (2010).

[89]. Erh-Kun Lai, Wei-Chih Chien, Yi-Chou Chen, Tian-Jue Hong, Yu-Yu Lin, Kuo-Pin Chang, Yeong-Der Yao, Pang Lin, Sheng-Fu Horng, Jeng Gong, Shih-Chang Tsai, Ching-Hsiung Lee, Sheng-Hui Hsieh, Chun-Fu Chen, Yen-Hao Shih, Kuang-Yeu Hsieh, Rich Liu, and Chih-Yuan Lu, "Tungsten Oxide Resistive Memory Using Rapid Thermal Oxidation of Tungsten Plugs", Japanese J. of Appl. Phys., vol.49, p.04DD17, (2010).

[90]. Seonghyun Kim, Kuyyadi P. Biju, Minseok Jo, Seungjae Jung, Jubong Park, Joonmyoung Lee, Wootae Lee, Jungho Shin, Sangsu Park, and Hyunsang Hwang, "Effect of Scaling WO_x-Based RRAMs on Their Resistive Switching Characteristics", IEEE Electron Device Lett., vol.32, no.5, p671, (2011).

[91]. W. C. Chien, Y. C. Chen, E. K. Lai, F. M. Lee, Y. Y. Lin, Alfred T. H. Chuang, K. P. Chang, Y. D. Tao, T. H. Chou, H. M. Lin, M. H. Lee, Y. H. Shih, K. Y. Hsieh, Chih-Yuan Lu, Appl. Phys. A, 102, 901, (2011).

Publication List

Paper :

[1]. M. D. Lee, C. K. Lo, T. Y. Peng, S. Y. Chen, Y. D. Yao, "Endurance study of switching characteristics in NiO films", J. Magn. Magn. Mater. vol.310, p.e1030, (2007).

[2]. M. D. Lee, C. H. Ho, C. K. Lo, T. Y. Peng, Y. D. Yao, "Effect of Oxygen Concentration on Characteristics of NiO-Based Resistance Random Access Memory", IEEE Trans. Magn., vol.43, no.2, 939, (2007).

[3]. M. D. Lee, C. H. Ho, Y. D. Yao, "CMOS Fully Compatible Embedded Non-Volatile Memory System With TiO_2-SiO_2 Hybrid Resistive-Switching Material", IEEE Trans. Magn., vol.47, p.653, (2011).

[4]. M. D. Lee, C. K. Lo, T. Y. Peng, K. L. Yau, S. Y. Chen, Y. D. Yao, "Epitaxial layer of MgO (001) grown on Si (001) wafer by e-beam evaporation", J. Magn. Magn. Mater. vol.304, p.e44, (2006).

[5]. M. D. Lee, N. V. Nong, N. P. Thuy, Y. D. Yao, S. F. Lee, Y. Liou, Y. Y. Chen, C. R. Wang, "Temperature dependence of magnetic properties in Ni-Mn-Ga shape memory alloys", phys. stat. sol. (c), vol.1, p.3579, (2004).

[6]. C. H. Ho, E. K. Lai, M. D. Lee, C. L. Pan, Y. D. Yao, K. Y. Hsieh, R. Liu, C. Y. Lu, "A Highly Reliable Self-Aligned Graded Oxide WO_x Resistance Memory: Conduction Mechanisms and Reliability", Symposium of VLSI Technology, 12B-2, p.228, (2007).

[7]. C. H. Ho, M. D. Lee, C. L. Pan, E. K. Lai, Y. D. Yao, K. Y. Hsieh, R. Liu, C. Y. Lu, "A 2-bit/cell, Maskless, Self-Aligned Resistance Memory with High Thermal Stability", International Symposium on VLSI Technology Systems and Applications (VLSI-TSA), T66, (2007).

[8]. M. T. Lee, C. H. Ho, C. L. Hsu, W. C. Chiu, Y. D. Yao, "A Study of Nickel Oxide Resistive Random Access Memory for next Generation Application", Symposium on Nano Device Technology (SNDY), ND82, (2011).

Patent :

[1]. “具有梯度之金屬-氧化物電阻材料為基礎的半導體記憶裝置”,中華民國專利(申請號) : TW 098142995.
[2]. “一種以高密度電阻材料為主的半導體裝置”,中華民國專利 (申請號) : TW 097136747.
[3]. “電阻式隨機存取記憶體及其製造方法” ,中華民國專利(申請號) : TW 096146854.
[4]. “電阻式記憶體元件及其製造方法與操作方法” ,中華民國專利(申請號) : TW 096126592.
[5]. “記憶胞及其製程”,中華民國專利(申請號) : TW 096136900.
[6]. “電阻式儲存器元件及其製造方法與操作方法” ,中華人民共和國專利(公開號) : CN 101162760.
[7]. “儲存單元及其製程” ,中華人民共和國專利(公開號) : CN 101174672.
[8]. “電阻式隨機存取儲存器及其製造方法”,中華人民共和國專利(公開號) : CN 101388435.
[9]. “以高密度電阻材料為主的半導體儲存裝置及其製造方法”,中華人民共和國專利(公開號) : CN 101667588.
[10].“Resistive random acces memory and method for manufacturing the same”,美國專利號(申請號):US 7667293.
[11].“Resistance type memory device and fabricating method and operating method thereof”, 美國專利號(申請號):US 7524722.