國 立 交 通 大 學

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博 士 論 文

微污染與電漿製程對奈米電晶體元件特性影響之研究及其改善方法之研發

Study on the Effects of Microcontamination and Plasma Process to Nano-Device Characteristics and the Development of Improvement Methods

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摘 要

在超大型積體電路中，電晶體元件的尺寸必須持續微縮以降低成本及提升元件特性，在奈米世代元件的研發上，電晶體的重要製程，包括微污染、閘極氧化層、超淺接面及銅製程等，都是元件製作成敗的關鍵。本論文主要研究微污染防治及電漿製程兩大主題，分別就潔淨室中微污染及電漿製程對奈米電晶體元件特性的影響，並分別提出改良的新式製程。

在微污染防治方面，首先我們架設一組清洗工作台，在工作台內裝置可更換的濾網模組，分別使用新的鐵氟龍材質空氣濾網與傳統玻璃纖維空氣濾網，探討兩種濾網對微污染的控制能力。在定性與定量分析工作台內微污染的成分及含量後，發現兩種空氣濾網皆可有效控制包括無機離子、有機離子及金屬等微污染物，但是傳統玻璃纖維空氣濾網由於內含黏著劑，在循環迴風下，產生了相關的有機污染物。另外，我們製作了金氧半電容元件來評測暴露在不同濾網下，微污染對元件閘極氧化層的影響，結果發現鐵氟龍材質空氣濾網相較於傳統玻璃纖維空氣濾網，可有效改善元件特性。

接著，我們在工作台內使用氫氟酸氣體加速實驗來模擬潔淨室中酸性氣體的腐蝕過程，鐵氟龍與玻璃纖維材質的空氣濾網，分別安裝在工作台內進行實驗以分析兩種

空氣濾網的抗腐蝕能力，空氣採樣、晶片採樣及元件暴露實驗分別使用來探討兩種空氣濾網在腐蝕過程中所釋放污染物的成分及含量，以及這些污染物對元件特性的影響，結果證明鐵氟龍材質空氣濾網可有效抵抗潔淨室中酸性氣體的腐蝕，而傳統玻璃纖維材質的空氣濾網在氫氟酸氣體的腐蝕下，釋放了包括硼及有機離子等污染物，造成元件特性的退化。

在電漿製程研究方面，首先我們開發製作矽化鎳的製程，分別針對鎳金屬沉積厚度、快速熱退火溫度及製作於不同結晶的矽基板上等，尋找最佳化條件，發現在單晶矽及非晶狀複晶矽上，200Å 厚度的鎳在 400℃到 650℃快速熱退火下形成的矽化鎳，有較低且穩定的片電阻值。接著我們將矽化鎳製作於不同線寬的複晶矽閘極上，探討閘極線寬對矽化鎳阻值的影響，結果顯示矽化鎳的最佳製程溫度在 400℃到 550℃之間。然後，我們研究矽化鎳在第二次快速熱退火的熱穩定性，發現矽化鎳製作於單晶矽與非晶狀複晶矽有較佳的熱穩定性。

在矽化鎳製程最佳化後，我們將矽化鎳製程應用於超淺接面的製作，實驗發現接面二極體漏電流隨著矽化鎳製程溫度增加而減少，這是由於矽化鎳完全形成所致，另外，漏電流也會隨著矽化鎳厚度增加而增加，這是由於矽化鎳越來越接近接面二極體的空乏區。接著，我們使用新式選擇性液相沉積法來取代傳統活性離子蝕刻法製作接觸孔，研究二極體元件在電漿環境下元件特性退化的機制，結果發現利用選擇性液相沉積法製作接觸孔可以抑制電漿製程對接面深度 1000Å 以下元件造成的退化。

在本研究中，我們分別探討微污染及電漿製程對電晶體元件特性的影響，並提出改良製程，經實驗結果證實新式鐵氟龍材質空氣濾網及選擇性液相沉積法可有效改善元件特性，此兩項技術對應用於奈米世代元件製程，應該具有相當大的潛力。

Study on the Effects of Microcontamination and Plasma Process to Nano-Device Characteristics and the Development of Improvement Methods

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ABSTRACT

In ULSI, the dimension of device must be scaled down to reduce the cost and improve the device performance. For the development of nanometer generation devices, the important issues, including microcontamination, gate insulator, ultra-shallow junction, copper interconnection, etc., are the key processes to successfully fabricate devices. In this thesis, the microcontamination control and the plasma process of silicide shallow junction were the main topics. The influences of microcontamination and plasma process to device performance were studied and the new improvement methods were developed.

In the microcontamination control aspect, first the specially designed clean bench was set up in the cleanroom. The main filter of the clean bench was changeable and two kinds of air filter modules, including the PTFE and the glass-fiber ULPA filters, were used as the main filter, respectively. After the air sampling, wafer sampling and device exposure experiments, it was found that two kinds of air filters can effectively control the contaminants, including inorganic ions, organic ions and metals, in the cleanroom. The glass-fiber ULPA filter, however, presented some organic contaminants released from the binder of the filter in air recycling condition. Besides, the MOS capacitors were also used to investigate the effects of contaminations to gate insulator when the device were exposed under different ULPA filters. The results revealed that the PTFE ULPA filter can control the contamination and improve the device performance.

Next, the hydrofluoric acid (HF) vapor was used in the clean bench to simulate the acid vapor corrosion in the cleanroom. The PTFE and glass-fiber ULPA filters were used to investigate the corrosion-resistant ability, respectively. From the air sampling, wafer

sampling and device exposure experiments, the PTFE ULPA filter showed better resistance to HF vapor corrosion. On the contrary, the glass-fiber ULPA filter released organic ions and boron contaminants in the HF vapor environment and resulted in the degradation of device performance.

In the plasma process aspect, first the optimum process conditions of nickel silicide were developed according to the nickel film thickness, rapid thermal annealing (RTA) temperature and different crystallization substrates. The nickel silicide formed with the 200Å-thick nickel and the RTA temperature between 400℃ to 650℃ showed the low and stable sheet resistance when fabricated on the c-Si and apoly-Si substrates. The nickel silicide was also fabricated on the poly-gate with different linewidth and the results showed that the optimum process temperatures were between 400℃ to 550℃. Finally, the stability of nickel silicide processed with second RTA was studied and it was found that the nickel silicide formed on c-Si and apoly-Si substrates have the better thermal stability.

The optimum processes of nickel silicide were then used to fabricate on the ultra-shallow n^+/p junction. The leakage current of junction diode decreased with the increasing RTA temperature and this was due to the complete formation of nickel silicide. Besides, the leakage current of junction diode increased with the increasing nickel silicide thickness and this is because the silicide grew close to the junction depletion region. Finally, the selective liquid-phase deposition (S_LPD) method was used to replace the traditional reactive-ion etching (RIE) for the formation of contact holes. The degradation mechanism of diodes exposed under the plasma environment was investigated and the results displayed that diodes with the contact-holes formed by the S_LPD method can suppress the degradation of device with the junction depth shallower than 1000Å.

In this study, the influences of microcontamination and plasma process to device performance were investigated and the new improvement methods were also proposed. The experimental results revealed that the PTFE ULPA filter and the selective liquid-phase deposition method can effectively improve the device performance and they may become the potential technologies for the fabrication of nanometer generation devices.

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CHAPTER 1

Introduction and Thesis Organization

1.1 BACKGROUND AND MOTIVATIONS

In ULSI, the dimension of device must be scaled down to reduce the manufacturing cost and improve the circuit performance. As the device size is scaled down to nanometer generation, the development of advanced processes including wafer environment contamination control, gate insulator, ultra-shallow junction, interconnection, etc., become more and more crucial to fabricate nano-dimension devices. The recently developed technologies, including high-K gate insulator, metal gate, silicide, Cu damascene process, low K dielectric, etc., have been the inevitable trend for future device manufacturing. Table 1-1 shows the technology requirements predicted by ITRS 2003. Among these key processes, wafer environment contamination control and plasma process have been considered to be well-developed technologies and pay less attention on them. The impact of AMC and plasma process on device performance can only be expected to become more deleterious as device dimensions decrease to nanometer generation.

There is definitive consensus that as device geometries approach 90 nm and beyond, wafer isolation will prove to be an enabling technology. The percentage of process steps affected by non-particulate or molecular contamination is expected to increase. The use of copper and other novel materials in the process introduces other potential contaminants. Because of these trends, wafer isolation technology, integrated tool mini-environments and closed carriers (e.g., Front Opening Unified Pods (FOUPs)) are needed [1]. The wafer environment contamination control (WECC) technology requirements indicate target levels of

ambient acids, bases, condensables, dopants, and metals for specific process steps. Outgassing from materials of construction in the cleanroom, wafer processing equipment, and wafer environmental enclosures as well as fugitive emissions from chemicals used in wafer processing are the two main sources of Airborne Molecular Contamination (AMC). Oxygen and water vapor as well as low concentration atmospheric contaminants (e.g., CO) can also be considered as part of the AMC burden [2].

Acid vapors in the air come from the cleaning or etching process have been often seen during the wafer processing. These acid vapors may corrode the construction of cleanroom, releasing the boron, organic compounds and amines [3]. For example, the HF vapor makes the glass-fiber in HEPA filter degraded and the boron and organic compounds contained in HEPA filter will thus be released to the wafer surface [4]. Theses contamination will impact the device performance or DUV photoresists [5]. The impact of AMC on wafer processing can only be expected to become more deleterious as device dimensions decrease.

For the MOSFET device, the fabrication of source/drain (S/D) junction is an important process. With the scaling down of devices, the S/D junction depth must reduce to mitigate the punch-through phenomenon or other short-channel effects. The improvement of devices performance by the shrinking of devices size resulted in the increase of sheet resistance (R_S) and contact resistance (R_C). The increase of R_S and R_C will increase the resistance of junction area, causing the RC time delay. Since the reduction of junction area, junction depth and contact-hole size in an unsilicided device results in a high resistance junction area, it will degrade the transistor current drivability and increase the RC time delay, making the device fail to work properly. In order to reduce the parasitic resistance of the MOSFET device, the low resistivity silicide form on the junction region is required. Besides, the use of self-aligned silicide (salicide) process can selectively form silicide on the gate and the S/D region without

additional mask, which simultaneously reduced the gate and junction resistance. It is well known that the resistivity of commonly used titanium silicide ($TiSi_2$) increases as the gate linewidth reduces to submicron dimension. For the wide lines, the $TiSi_2$ is mainly the low resistivity C54 phase (10~15μΩ-cm), while for the narrow lines, the phase transformation process is limited and the high resistivity C49 phase (60~80μΩ-cm) is dominant. Besides, the high temperature (800~950℃) silicidation process is needed to make the C54 phase [6], [7]. However, as the thickness of Ti decreases, $TiSi_2$ agglomeration has been observed. This results in the high sheet resistance when thin $TiSi_2$ layers are used for the shallow junctions. For 0.18μm process or below, cobalt silicide ($CoSi_2$) is more preferred due to its lower linewidth dependence of sheet resistance. $CoSi_2$, however, consumes more silicon volume than $TiSi_2$ and it will limit the scaling of junction depth. Compared to $CoSi_2$, nickel silicide (NiSi) has the advantages: (1) less silicon consumption for the same sheet resistance, (2) low contact resistivity, (3) low process temperature and wide process window (400-600℃), (4) low stress, and (4) no creep-up phenomenon. According to the above mentioned, NiSi is a promising candidate silicide for next generation devices.

Reactive ion etching (RIE) is the most frequently used technology for contact-hole formation [8]. It is important to reduce the RIE damages on the surface of junction especially for ultra-shallow junction. It has been reported that the RIE process can induce some unwanted effects including radiation damage, surface amorphized layer and contaminated layer [8]-[11]. The radiation damage results from the energetic ions accelerated by DC bias. The surface amorphized layer comes from the ion bombardment damage to junction surface. And the contaminated layer is due to the fluorocarbon-containing based etching chemistries. This damage layer is around hundred of angstroms deep from the surface. Some technologies [8], [9] are used to eliminate this surface damage layer including high temperature annealing, surface etching, etc. But these methods may not suitable for silicide process and ultra-shallow

junction when manufacturing ULSI.

1.2 THESIS ORGANIZATION

In this thesis, the wafer environment contamination control and the plasma process of silicide shallow junction were the main topics. The influences of AMC and plasma process to device performance were studied and the new improvement methods were developed.

In chapter 2, a clean bench with different filter modules such as the NEUROFINE PTFE filter, the glass-fiber ULPA filter, and a combination of chemical filters with both of these was set up in the cleanroom. All elements in the air or on the wafer were analyzed through air sampling and wafer sampling inside the bench, to determine clearly the ability of each filter module to suppress AMC. The practical effects of AMC on device performance were also investigated by actually exposing a wafer to air in an especially controlled clean bench before gate oxidation.

In chapter 3, the performance of two ULPA filter modules - the PTFE and the glass-fiber was investigated. PTFE fiber is considered to be resistant to acid vapor corrosion and it is a good material from which to fabricate ULPA filters. The source of AMC and the effects of AMC on devices exposed in the clean bench in a HF vapor environment were examined to elucidate the impact of filter material. The results indicated that the PTFE ULPA filter can provide a better cleanroom environment than a commercial glass fiber ULPA filter.

In chapter 4, the optimum process condition of NiSi on different silicon substrates and the relation between sheet resistance and linewidth were investigated. In addition, the thermal stability of NiSi processed with second rapid thermal annealing (RTA) was also studied.

In chapter 5, a new selective liquid-phase deposition (S_LPD) process was proposed to overcome the RIE damage problems. S_LPD process is the selective deposition technology

which deposits silicon dioxide on silicide surface against photoresist. This technology was conduct under non-plasma environment and hence it will not induce the surface damaged and contaminated layer. The experimental results indicate that the new S_LPD process indeed has the superior of suppressing plasma damage on devices. Therefore, the new S_LPD process may become the candidate of non-plasma process for future advanced device manufacturing.

Finally, conclusions and recommendations for further research were summarized in Chapter 6.

TABLE 1-1
ITRS 2003 Technology Requirements

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		***hp90***			***hp65***		
MPU/ASIC ½ Pitch (nm)	***107***	***90***	***80***	***70***	***65***	***57***	***50***
MPU Printed Gate Length (nm)	***65***	***53***	***45***	***40***	***35***	***32***	***28***
MPU Physical Gate Length (nm)	***45***	***37***	***32***	***28***	***25***	***22***	***20***
Equivalent physical oxide thickness for MPU/ASIC T_{ox} (nm)	**1.3**	**1.2**	**1.1**	**1.0**	**0.9**	**0.8**	**0.8**
Drain extension X_j (nm)	**24.8**	**20.4**	**17.6**	**15.4**	**13.8**	**8.8**	**8.0**
Maximum drain extension sheet resistance (PMOS)(Ω /sq)	**545**	**663**	**767**	**833**	**884**	**1739**	**1800**
Maximum drain extension sheet resistance (NMOS) (Ω/sq)	**255**	**310**	**358**	**389**	**412**	**811**	**840**
Contact X_j (nm)	**49.5**	**40.7**	**35.2**	**30.8**	**27.5**	**NA**	**NA**
Maximum silicon consumption (nm)	**24.8**	**20.4**	**17.6**	**15.4**	**13.8**	**13.2**	**12**
Silicide thickness (nm)	**25**	**20**	**21**	**19**	**17**	**16**	**14**
Contact silicide sheet Rs (Ω/sq)	**6.5**	**7.9**	**7.5**	**8.6**	**9.6**	**10.0**	**11.1**
Contact maximum resistivity (Ω-cm^2)	**1.93E-07**	**1.62E-07**	**1.44E-07**	**1.20E-07**	**1.05E-07**	**0.87E-07**	**0.72E-07**
Airborne Molecular Contaminants in gas phase (pptM))							
Lithography—bases (as amine, amide, and NH_3)	**750**	**750**	**750**	**<750**	**<750**	**<750**	**<750**
Gate—metals (as Cu, $E=2\times10^{-5}$)	**0.15**	**0.1**	**0.1**	**0.07**	**<0.07**	**<0.07**	**<0.07**
Gate—organics (as molecular weight to 250, $E=1\times10^{-3}$)	**80**	**70**	**60**	**60**	**50**	**50**	**50**
Dopants	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Airborne Molecular Contaminants, Surface Deposition Limits (for Si Witness Wafer, 24-hour Exposure to Closed FOUP, Pod, Mini-environment or Air)							
SMC organics on wafers, ASTM 1982–99, ng/cm^2	**4**	**2**	**2**	**2**	**2**	**2**	**2**
Front-end processes, bare Si, total dopants added to 24-hour witness wafer, atoms/cm^2	**<2E12**	**<2E12**	**<2E12**	**1E12**	**1E12**	**1E12**	**1E12**
Front-end processes, bare Si, total metals added to witness wafer, atoms/cm^2	**<2E10**	**<2E10**	**<2E10**	**<2E10**	**<2E10**	**<2E10**	**<2E10**

SMC-Surface Molecular Condensable

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

CHAPTER 2

Investigation of Airborne Molecular Contamination in Cleanroom and Its Effects on Device Performance

2.1 INTRODUCTION

The cleanness of a cleanroom environment must be tightly controlled to achieve high-yield and high-performance ULSI manufacturing [12]-[15]. Recently, new developments of material and process have helped to shrink device geometry. The advanced contamination control of cleanrooms has also been indispensable in this regard [16]. So far, only particle contamination has been intensively studied [17], and recently developed filters, such as HEPA and ULPA, can already sufficiently suppress particles [18]. However, the controllability of airborne molecular contamination (AMC) by present cleanroom technologies has not yet been validated because AMC is a kind of atom or molecular-level gas-phase contamination like organic and inorganic ones. As the minimum feature size of devices is continuously scaled down to far below 0.1μm, AMC will gradually become crucial in ULSI manufacturing. In the near future, especially in the nanodevice era, contamination by organic compounds, inorganic ions, and trace doping impurities [19] in cleanroom air may also dominate the characteristics, reliability, and even yield of devices. Technologies for eliminating both particles and AMC from manufacturing environment must be considered to completely solve this problem.

To date, several investigations of AMC, and its effects on device performance, have been conducted. Most, however, have only paid attention to the experiments based on intentional contamination on devices [14], [20], [21]. Few studies have considered AMC absorbed from cleanroom air and its practical effects on the characteristics of devices.

In this work, a clean bench was specially equipped with different filter modules such as the NEUROFINE PTFE filter, the glass-fiber ULPA filter, and a combination of chemical filters with both of these. All elements in the air or on the wafer were analyzed through air sampling and wafer sampling inside the bench, to determine clearly the ability of each filter module to suppress AMC. The practical effects of AMC on device performance were also investigated by actually exposing a wafer to air in an especially controlled clean bench before gate oxidation.

2.2 EXPERIMENTS

A specially controlled and fabricated clean bench (CB) was set up in the cleanroom (CR) of class 10k in a laboratory. Figure 2-1 schematically depicts the CB. Cleanroom air, from the air inlet of the CB, was initially filtered with the filter module that included inorganic and organic ion chemical filters, before flowing through the main filter, which was designed to be changeable. The chemical filter is mainly composed of active carbon, and it can absorb ions. Two kinds of main filter were used, the NEUROFINE PTFE filter (PTFE) and the glass-fiber ULPA filter (GF). The air flow rate and turnover rate inside the CB were set to 0.4 m/s and 5 %, respectively. Before sampling, the CB was first operated for more than one week to stabilize environmental conditions.

2.2.1 Evaluation of AMC through Air Sampling

Figure 2-2 presents the air sampling tools, Impinger and TENAX, which were equipped with a flow meter and a pump. The flow rate and sampling time of Impinger were 2 L/min and 24-72 hrs while those of TENAX were 100 mL/min and 5 hrs. Impingers collected mainly both inorganic and metallic contamination elements. The former were analyzed by the ion chromatography (IC), while the latter were analyzed using an inductively coupled plasma mass spectrometer (ICP-MS). Organic substances were collected by a TENAX (a kind of

absorbent) tube, and quantitatively analyzed by gas chromatograph mass spectrometer (GC-MS). The air in the CR was also analyzed for comparison. Table 2-1 summarizes the air sampling experimental conditions.

2.2.2 Evaluation of AMC through Wafer Sampling

The AMC absorbed on the surfaces of actual 6" P-type (100) Si wafers was analyzed for each filter module. After standard RCA cleaning, wafers were divided into two parts, and exposed to the air in the CR and the CB for 24-72 hrs. The metal contamination on these wafer surfaces was analyzed using total reflection X-ray fluorescence (TRXRF), while the organic contamination was analyzed by thermal desorption system–atmospheric pressure ionized mass spectrum (TDS-APIMS). For comparison, the contamination of a wafer not exposed to any environment was evaluated as a control. Table 2-2 is the summary of wafer sampling experimental conditions.

2.2.3 Evaluation of AMC through Electrical Characterization

Metal oxide semiconductor (MOS) capacitors, with thermal oxide as the insulator, were prepared to study the effects of AMC on practical device characteristics. Figure 2-3 shows the process flow diagram for preparing a MOS capacitor. The active region was first defined on a 6" P-type (100) Si wafer by local oxidation of the silicon (LOCOS) process, and then a 40 nm-thick sacrificial oxide layer was formed by thermal oxidation. This sacrificial oxide was subsequently removed, and the wafers were further cleaned by RCA cleaning before exposure. After exposure in the CR or the CB for 4 hrs, a 5 nm-thick gate oxide layer was grown on each wafer by thermal oxidation, and finally an aluminum gate electrode was deposited and patterned. Unexposed blank samples were also prepared using the same procedure. Finally, for all samples, the electrical properties such as leakage current density vs. electrical field (J-E), breakdown field (E_{bd}), and charge to breakdown (Q_{bd}) were measured through the MOS

capacitor (200 μm × 200 μm) using the HP4156 semiconductor parameter analyzer.

2.3 RESULTS AND DISCUSSION

2.3.1 Air Sampling Results

First, the constituents of the air in the CR and the CB, equipped with only inlet chemical filters but no main filter, were evaluated. Figure 2-4 shows the IC results for inorganic ion concentrations of the air in the CR and the CB. The concentrations of inorganic ions such as NH_4^+, Cl^-, NO_2^-, NO_3^-, and SO_4^{2-} were found to be high in the CR. In contrast, the inorganic ions concentrations in the CB were obviously low, implying that the CB without a main filter but with chemical filters can still remove the inorganic contaminations, especially NH_4^+ ions. All the analysis data of inorganic ions were list in Table 2-3. Next, the PTFE filter was installed as main filter in the CB and the same sampling procedure was implemented. The result was very similar to that obtained only with the chemical filters. These experimental results suggest that chemical filters efficiently reduced inorganic ion contaminations [22].

Figure 2-5 presents the ICP-MS results of metals and boron concentrations in the air from the CR and the CB. And Table 2-4 shows the ICP-MS analysis data .The concentrations of K, Mg, and Al elements were all below the detection limit in the air from the CR and from the CB without main filter, but the concentrations of Na, Ca, and especially B were detected. However, for the CB with either PTFE or GF as the main filter, both the metal and the boron contamination levels were under the detection limit. In fact, the chemical filters do not remove boron or metal contamination. Boron and metal contamination can be reasonably considered to exist in complexes with particles, and are thus more efficiently eliminated when the main filter is used than when it is not.

The concentrations of organic compounds in the air from the CR and the CB were also

compared in Table 2-5. As shown in Fig. 2-6, the organic compounds can be mainly divided into Si-based and oil-based ones. The former included D3 ($C_6H_{18}O_3Si_3$), D4 ($C_6H_{24}O_4Si_4$), D5 ($C_{10}H_{30}O_5Si_5$), and D6 ($C_{12}H_{36}O_6Si_6$), while the latter included DEP ($C_{12}H_{14}O_4$), DBP ($C_{16}H_{22}O_4$), TEP ($C_8H_{15}O_4P$), TBP ($C_{12}H_{27}O_4P$), and BHT ($C_{15}H_{24}O$). The CR air included high quantities of both kinds of organic compounds, but they can be mostly removed when only chemical filters were used. Of course, the concentrations can be further reduced using a combination of chemical filters and the PTFE or the GF main filter. Notably, however, a high concentration of D6 remains in the CB with a GF filter, perhaps because this compound is present in the binder of the glass-fiber ULPA filter, or in some of the materials used to manufacture the filter. Figure 2-7 shows the essential difference between the fiber structure of the PTFE filter and that of the GF filter. The glass-fiber used as an intermediate in the GF filter is usually shorter than the PTFE-fiber used in the PTFE filter. Hence, it must be mixed with a binder to reduce the gaps and ensure that the filter can isolate particles. However the binder, which consists mainly of acrylic, is an organic contamination source of D6. Consequently, the total concentration of organic compounds present when a GF filter is used exceeds that obtained when a PTFE filter is used. The high organic contamination may degrade the characteristics of devices.

2.3.2 Wafer Sampling

Metal contamination on wafers exposed in the CR or the CB was quantified by TRXRF analysis. As shown in Fig. 2-8, the densities of metal on different wafers are compared and the detail data were shown in Table 2-6. The “BLANK” sample refers to a wafer treated only by RCA cleaning and unexposed to air before analysis. On each wafer, five points were analyzed and the averages of the results at these points were compared. The metal densities on the BLANK and the CB samples were all below the order of 10^{11} atoms/cm^2, but they were

distributed from 10^{11} to 10^{13} atoms/cm^2 on the CR samples, again showing that the CB sample when a main filter, PTFE or GF, is used indeed has the same concentration of metal as the BLANK sample. The results of TRXRF are rather consistent with those obtained by ICP-MS analysis, shown in Fig. 2-5. In PTFE or GF filter environments, the metal concentrations are the same, so the PTFE filter can replace the commercial glass fiber ULPA filter to meet the requirements of an advanced cleanroom.

Next, the intensity of organic contaminant species on the wafer surfaces, exposed or unexposed to air, were evaluated using TDS-APIMS. Figure 2-9 to Fig. 2-12 compares results for different samples. The concentrations of each specifies of organic contamination of the CR sample greatly exceeded that of the CB sample, revealing that the wafer surface exposed in the CR does absorb much organic contamination. Here, mass numbers m/z = 16, 45, 73, 99, 149 were chosen. Contamination peaks at m/z = 16, 45, 149 often come from the outgassing of oil based plasticizers, which are widely used in plastic products of the cleanroom, such as DEP and DBP. Peaks at m/z = 73, 99 are often associated with the absorption of Si-based siloxane, such as D5 and D6. For all the CB samples, the intensity of m/z = 99 for a GF filter exceeds that for a PTFE filter. The result is quite consistent with the air sampling results presented in Fig. 2-6. Overall, a combination of chemical and PTFE filters in a CB can provide an excellent environment with rather low concentrations of organic compounds for manufacturing advanced ULSI devices.

2.3.3 Electrical Characterization Using a MOS Capacitor

Figure 2-13 compares J-E curves of the samples exposed in the CB and the unexposed sample. Figure 2-13(a) reveals that the sample exposed under a PTFE filter has a similar leakage current density and breakdown field to the unexposed sample. The environment in the CB with the PTFE filter is excellent so the sample exposed even for 24 hrs

shows little degradation. On the contrary, as shown in Fig. 2-13(b), the sample under a GF filter reveals a large leakage current density and exhibits much earlier breakdown than the unexposed sample. Fig. 2-14 compares the distributions of the breakdown electrical fields for these three kinds of samples. The breakdown fields were 13-14 MV/cm for the unexposed samples, while they were spread over a wide range, but still mainly 12-13 MV/cm, for the PTFE samples. However, for the GF samples, the distribution was spread even more widely, and shifted to a low electrical field. The degradation of the leakage current and the breakdown field can be attributed to AMC, which, when adhering to the wafer surface may induce defects within the gate oxide. While the MOS device is operating, the intermediate oxide defects will result in electron tunneling, rapidly inducing more defects until defect clusters form a conductive path between the substrate and the gate.

Figure 2-15 plots the cumulative probabilities of leakage current densities for these three kinds of samples. In each case, the leakage current density was measured at 4 MV/cm. The PTFE samples perform similarly to the unexposed samples because the CB with the PTFE filter can create an excellent environment. In contrast, the GF samples still show a higher and less uniform leakage current density distribution than the PTFE and the unexposed samples. Figure 2-16 displays a Weibull plot of charge to breakdown (Q_{bd}) for different samples. The PTFE samples showed slight degradation in Q_{bd} compared to the unexposed samples, but the GF samples exhibited obvious degradation with low and non-uniform distribution. The above electrical results indicate that the PTFE filter is much better than the GF filter at creating an advanced clean environment for manufacturing devices.

2.4 SUMMARY

AMC in air and on the surfaces of wafers was quantitatively analyzed. Air sampling results reveal that a CB with chemical filters can only effectively remove inorganic ions,

while one further equipped with a PTFE main filter can eliminate not only organic contaminations but also boron and metal. A CB with a GF filter still has a high concentration of D6. Wafer sampling results also demonstrate that each filter can, indeed, reduce the metal concentration to a level that corresponds to no exposure to air. Wafers exposed under a PTFE filter have less organic contaminations than those in the CR, but a GF filter shows high contamination of silicon-based organic D6, because of the binder used in the GF filter. In summary, the results obtained by air and wafer sampling are highly consistent.

The effects of AMC on device performance were also investigated using a MOS capacitor. The samples exposed in the CB under the PTFE filter have nearly the same leakage current density and breakdown field distribution as the unexposed sample, implying that the exposed wafers have few defects and exhibit slight degradation of film quality. However, the samples in the CB under a GF filter suffer an obviously degraded breakdown field, leakage current density, and Q_{bd} because of high concentrations of organic compounds.

All these results reveal that AMC will become an important issue in future nanodevice fabrication. An AMC-free manufacturing environment must be seriously considered when manufacturing nanodevices. Advanced ULPA filters, like the NEUROFINE PTFE filter combined with chemical filters, are excellent candidates for creating advanced manufacturing environments.

TABLE 2-1
Summary of Air Sampling Experimental Conditions

Contamination Type	Sampling Equipments	Flow Rate	Sampling Time	Analysis Method
Organic Compounds	TENAX Tube	100 mL/min.	5 hrs	GC/MS (Gas Chromatograph Mass Spectrometer)
Inorganic Ions	Impinger	2 L/min.	24 hrs	IC (Ion Chromatography)
Metals & Boron	Impinger	2 L/min.	72 hrs	ICP-MS (Inductively Coupled Plasma Mass Spectrometer)

Bench Condition
Filter module: 1. PTFE ULPA filter + Chemical filter
2. Glass-Fiber ULPA filter + Chemical filter
Air flow rate: 0.4 m/s
Turnover rate: 5%
Temperature: 23 ℃

TABLE 2-2
Summary of Wafer Sampling Experimental Conditions

Contamination Type	Exposing Location	Exposing Time	Analysis Method	Elements
Organic Compounds	CR and CB	24 hrs	TDS-APIMS (Thermal Desorption System – Atmospheric Pressure Ionized Mass Spectrum)	D3, D4, D5, D6, DEP, DBP, TEP, TBP, BHT
Metals		72 hrs	TRXRF (Total Reflection X-Ray Fluorescence)	Na, K, Ca, Mg, Fe, Ti, V, Cr, Mn, Co, Ni, Cu, Zn

Bench Condition
Filter module: 1. PTFE ULPA filter + Chemical filter
2. Glass-Fiber ULPA filter + Chemical filter
Air flow rate: 0.4 m/s
Turnover rate: 5%
Temperature: 23 ℃

TABLE 2-3
Air Sampling Results of Inorganic Ions

Inorganic Ion ($\mu g/m^3$)	CR	Detection Limit	CB	Detection Limit
Inlet Filter Main Filter		- -	Chemical Filter -	
NH_4^+	7.4	0.07	0.33	0.07
Cl^-	0.13	0.02	0.038	0.02
NO_2^-	1.3	0.01	0.99	0.01
NO_3^-	0.68	0.05	0.05	0.05
SO_4^{2-}	0.2	0.04	< 0.03	0.03

TABLE 2-4
Air Sampling Results of Metals and Boron

Metals & Boron ($\mu g/m^3$)	CR	Detection Limit	CB	Detection Limit	CB_PTFE	Detection Limit	CB_GF	Detection Limit
Inlet Filter Main Filter		- -	Chemical Filter -		Chemical Filter PTFE Filter		Chemical Filter Glass-Fiber Filter	
Na	0.006	0.002	0.006	0.001	<0.008	0.008	<0.002	0.002
K	<0.01	0.01	<0.005	0.005	<0.006	0.006	<0.004	0.004
Ca	0.003	0.002	0.002	0.001	<0.003	0.003	<0.004	0.004
Mg	<0.002	0.002	<0.001	0.001	<0.003	0.003	<0.004	0.004
Al	<0.002	0.002	<0.001	0.001	<0.003	0.003	<0.004	0.004
Fe	<0.002	0.002	0.002	0.001	<0.003	0.003	<0.004	0.004
B	0.054	0.0003	0.063	0.0002	<0.0006	0.0006	<0.0007	0.0007

TABLE 2-5
Air Sampling Results of Organic Compounds

Organic Compounds ($\mu g/m^3$)	CR	Detection Limit	CB	Detection Limit	CB_PTFE	Detection Limit	CB_GF	Detection Limit
Inlet Filter Main Filter	- -		Chemical Filter -		Chemical Filter PTFE Filter		Chemical Filter Glass-Fiber Filter	
D3:$C_6H_{18}O_3Si_3$	0.13	0.1	<0.4	0.4	<0.1	0.1	<0.37	0.37
D4:$C_8H_{24}O_4Si_4$	0.29	0.25	<0.7	0.7	<0.25	0.25	<0.11	0.11
D5:$C_{10}H_{30}O_5Si_5$	<0.49	0.49	<0.3	0.3	<0.49	0.49	-	0.03
D6:$C_{12}H_{36}O_6Si_6$	<0.23	0.23	0.29	0.03	0.3	0.23	0.88	0.03
DEP:$C_{12}H_{14}O_4$	0.38	0.03	-	0.03	<0.03	0.03	-	0.03
DBP:$C_{16}H_{22}O_4$	0.2	0.09	0.11	0.03	<0.09	0.09	<0.14	0.14
TEP:$C_6H_{15}O_4P$	<0.03	0.03	<0.03	0.03	<0.03	0.03	<0.03	0.03
TBP:$C_{12}H_{27}O_4P$	0.24	0.03	<0.03	0.03	0.11	0.03	<0.03	0.03
BHT:$C_{15}H_{24}O$	<0.03	0.03	<0.03	0.03	<0.03	0.03	<0.03	0.03

TABLE 2-6
Wafer Sampling Results of Metals

Metals (10^{10} atoms/cm^2)	BLANK	CB_PTFE	CB_GF	CR
Inlet Filter Main Filter	- -	Chemical Filter PTFE Filter	Chemical Filter Glass-Fiber Filter	- -
Na	-	-	-	-
Mg	-	-	-	-
K	-	-	-	-
Ca	-	-	-	354.645
Ti	3.689	5.087	4.682667	20.963
V	5.391	4.069	3.407667	10.919
Cr	3.927	5.087	2.531667	74.97
Mn	2.374	3.899	2.126	8.72
Fe	-	-	-	122.129
Co	1.667	1.75	1.30266	15.493
Ni	-	-	-	12.677
Cu	1.076	1.018	0.8305	23.054
Zn	-	-	1.5683	10.426

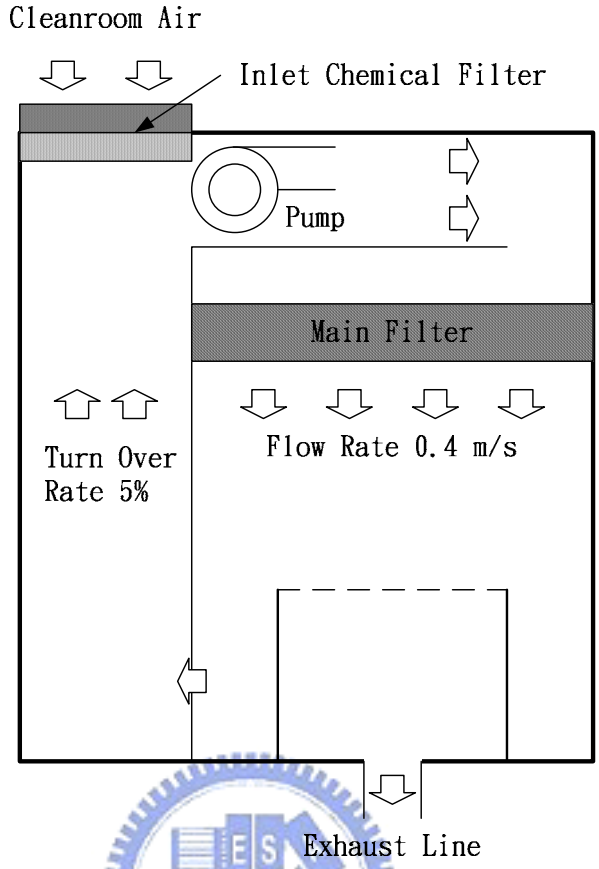


Fig. 2-1. Schematic diagram of specially designed clean bench.

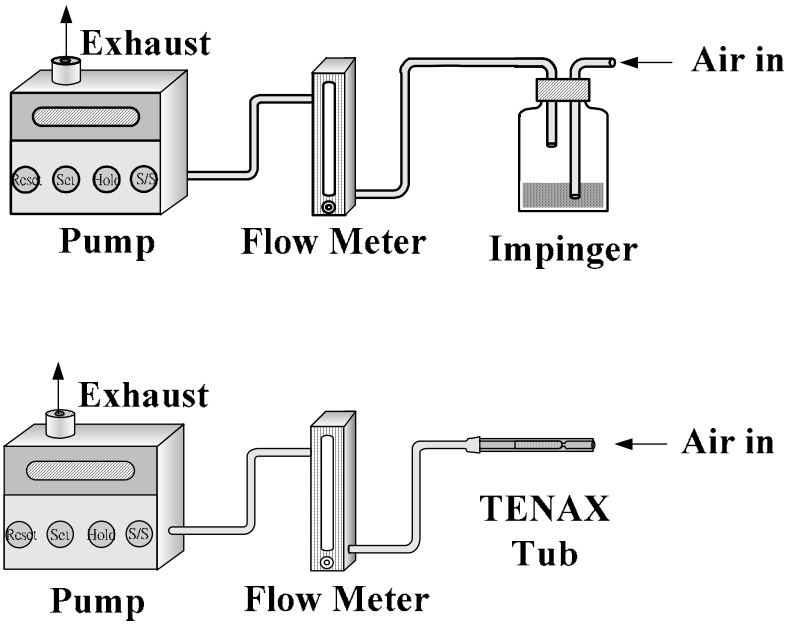


Fig. 2-2. Air sampling equipments used for evaluation of metals, inorganic and organic contaminations.

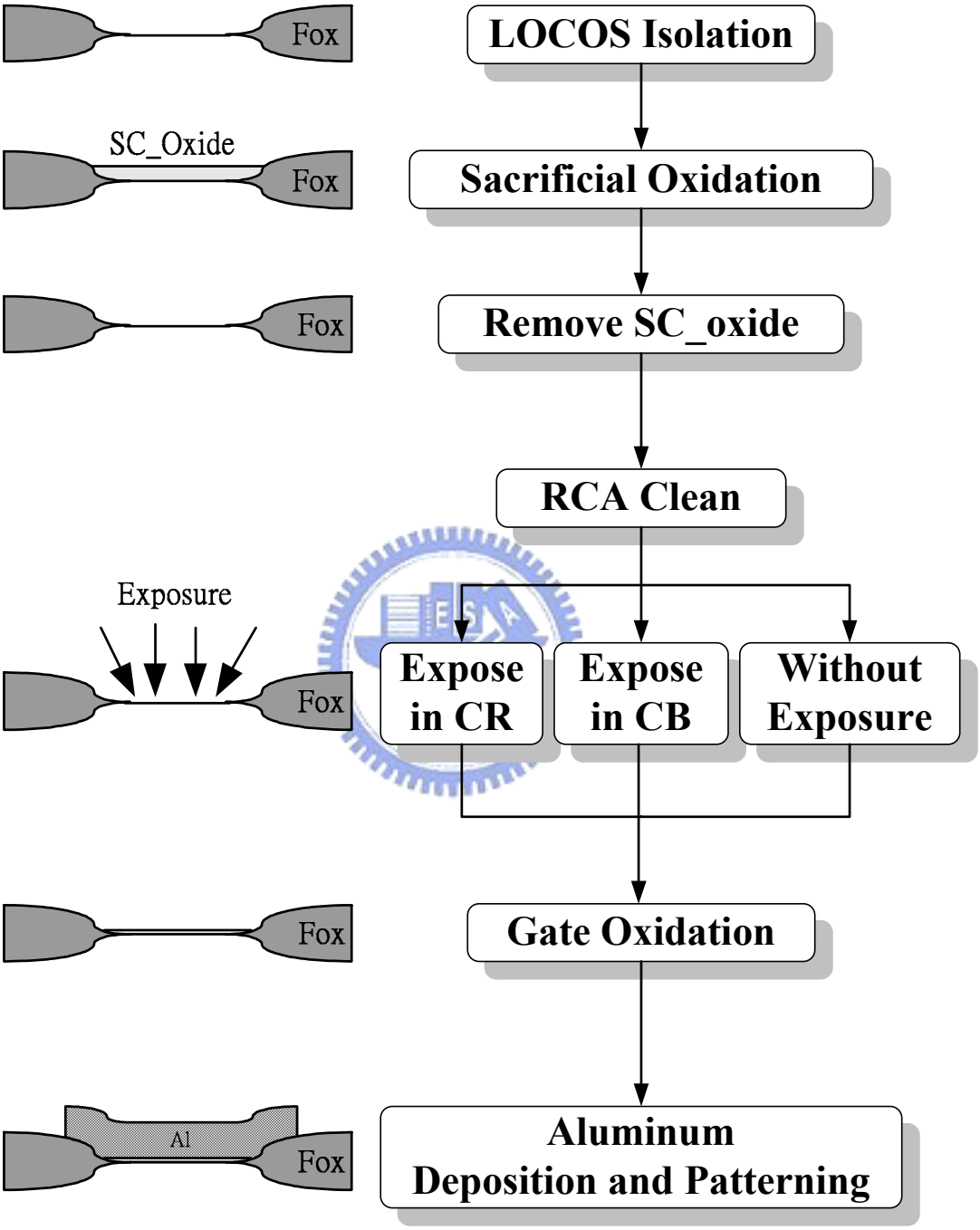


Fig. 2-3. Process flow of MOS capacitor exposure experiment.

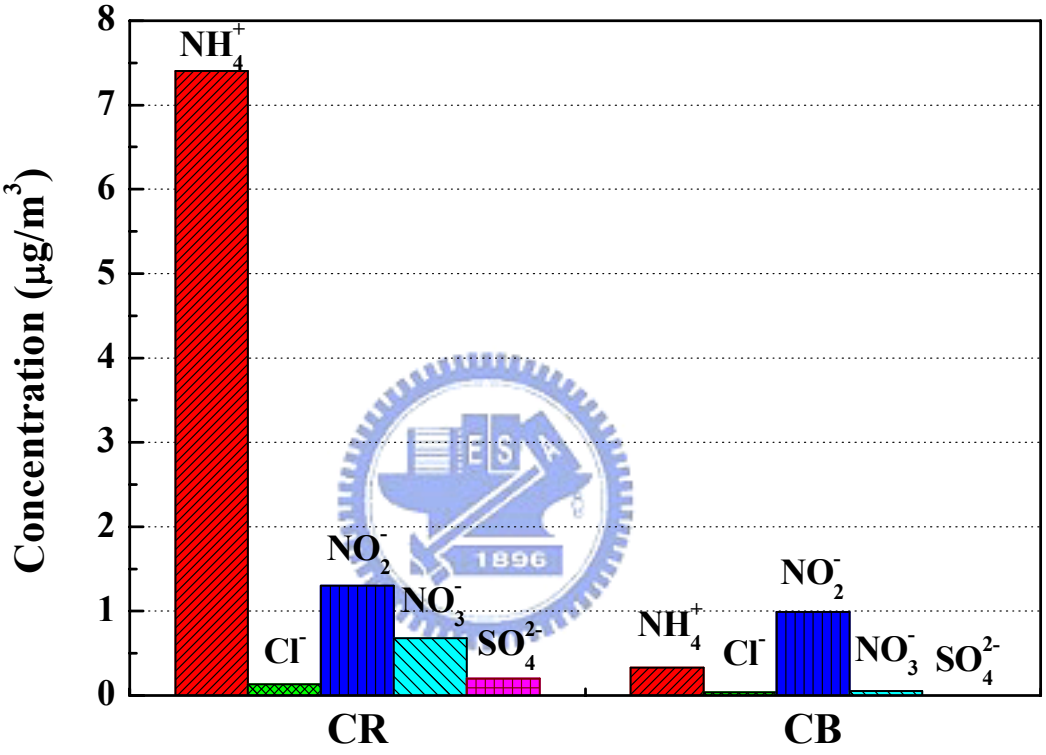


Fig. 2-4. Air sampling results of inorganic ions.

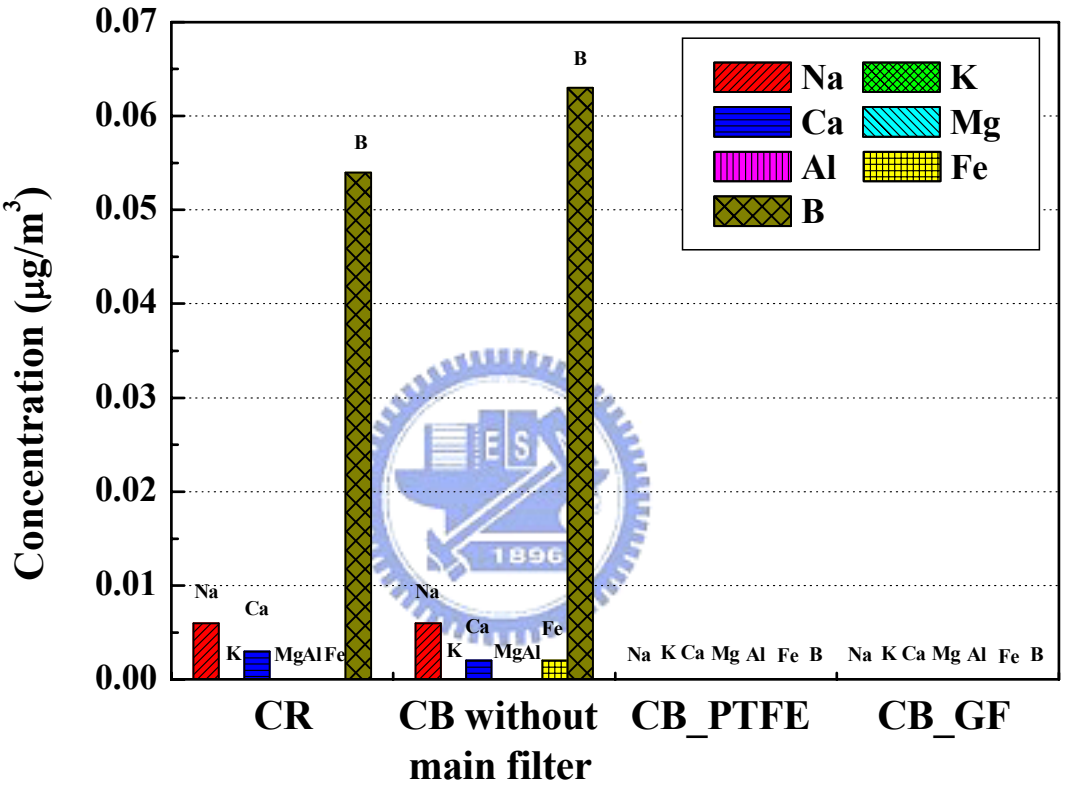


Fig. 2-5. Air sampling results of metals and boron.

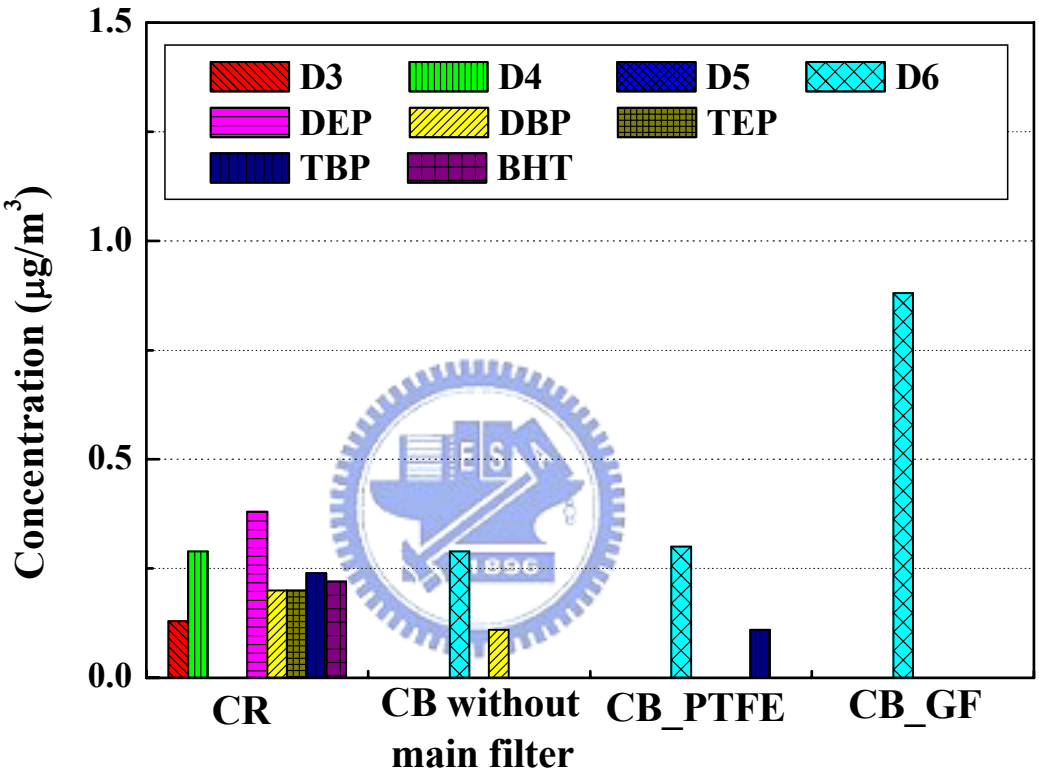
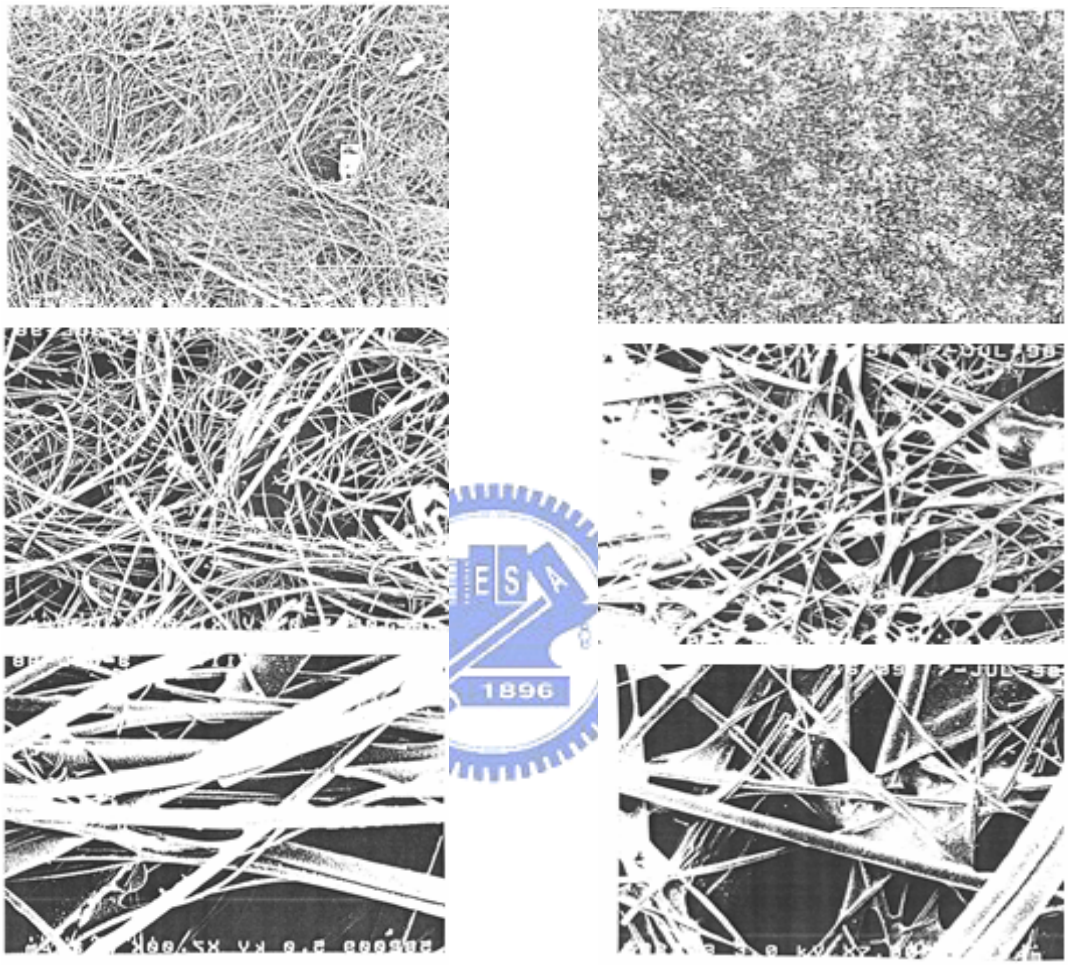


Fig. 2-6. Air sampling results of organic compounds.



(a) PTFE Fiber (b) Glass Fiber

Fig. 2-7. The fiber structure of (a) PTFE Fiber and (b) Glass Fiber.

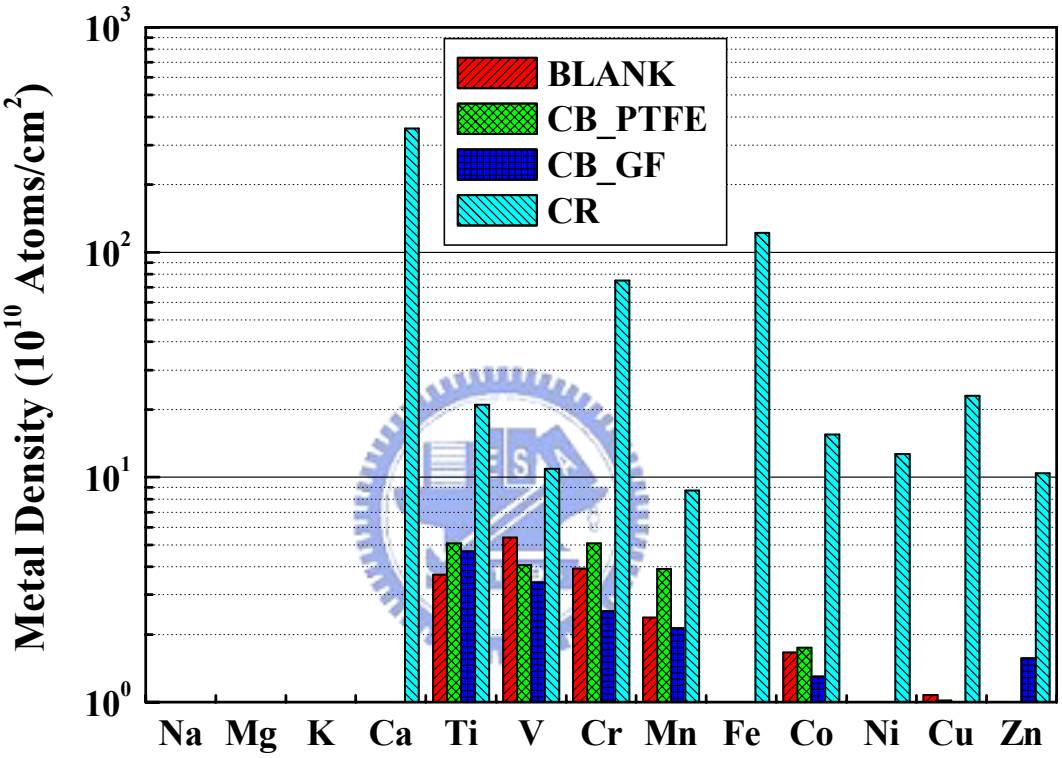
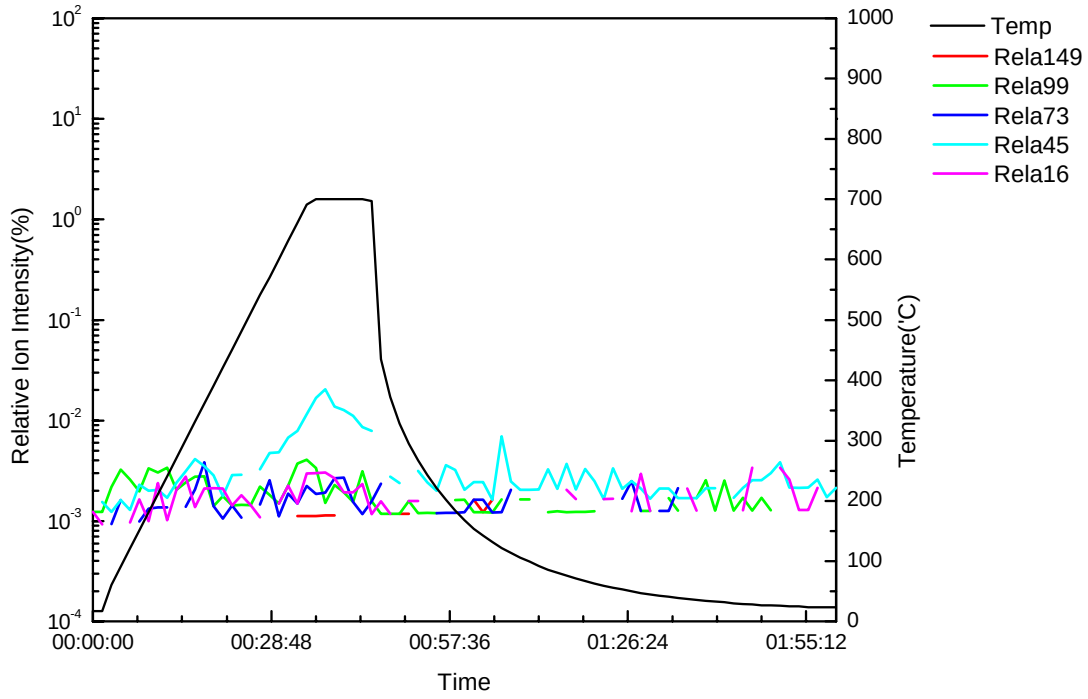
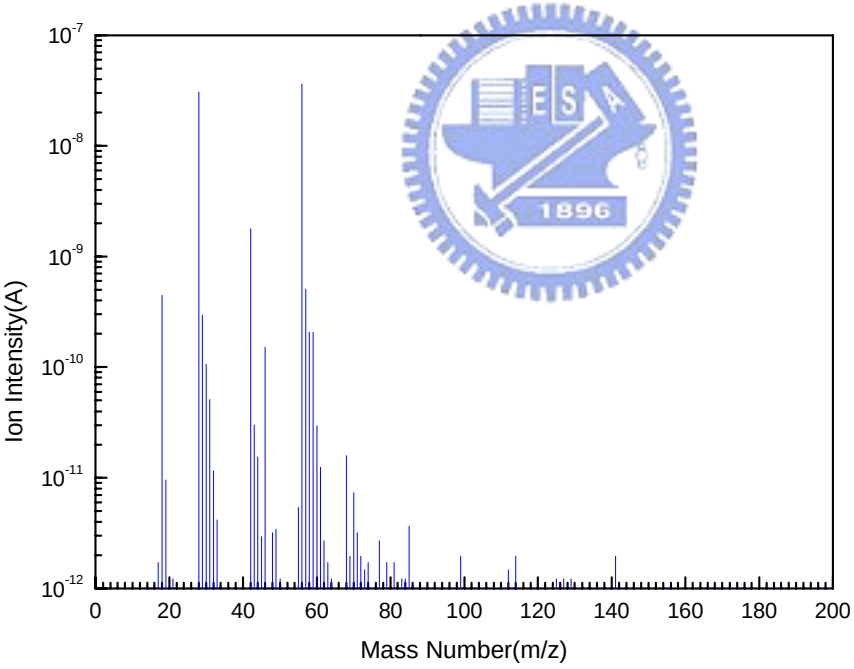


Fig. 2-8. Wafer sampling results of metals.

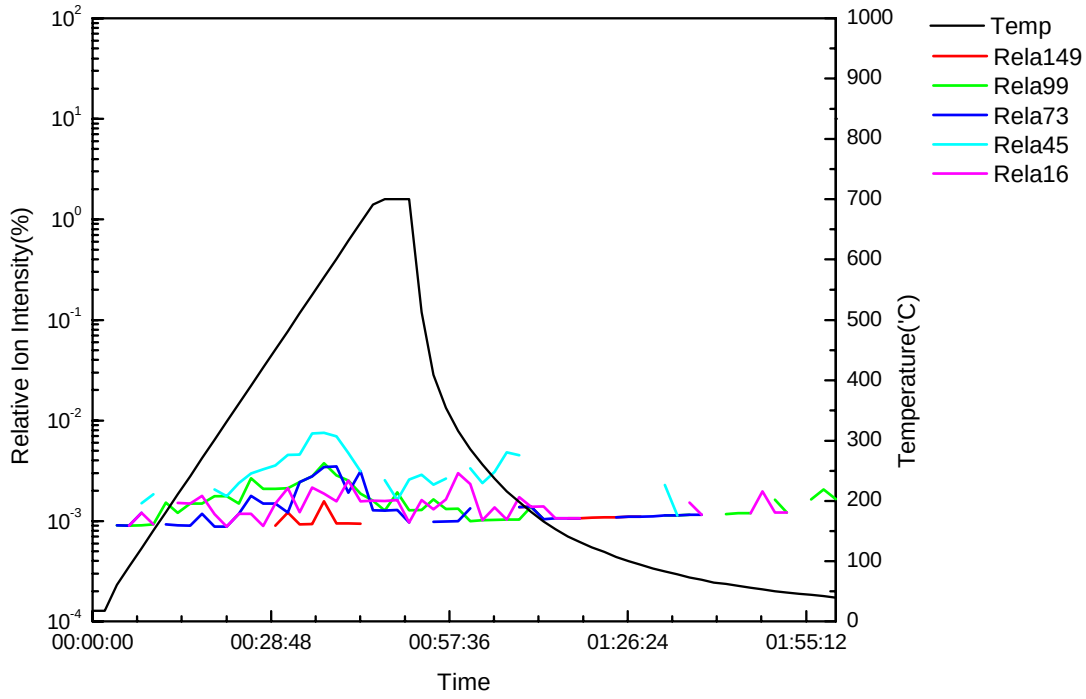


(a)

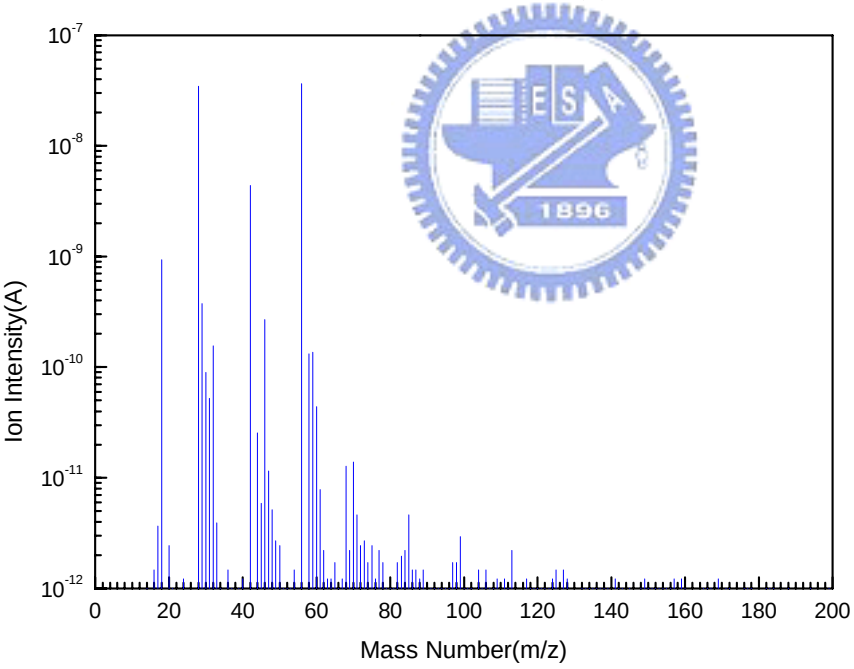


(b)

Fig. 2-9. TDS-APIMS analysis for unexposed sample: (a) Time depend ion intensity plot, (b) Mass spectrum at temperature = 336℃.

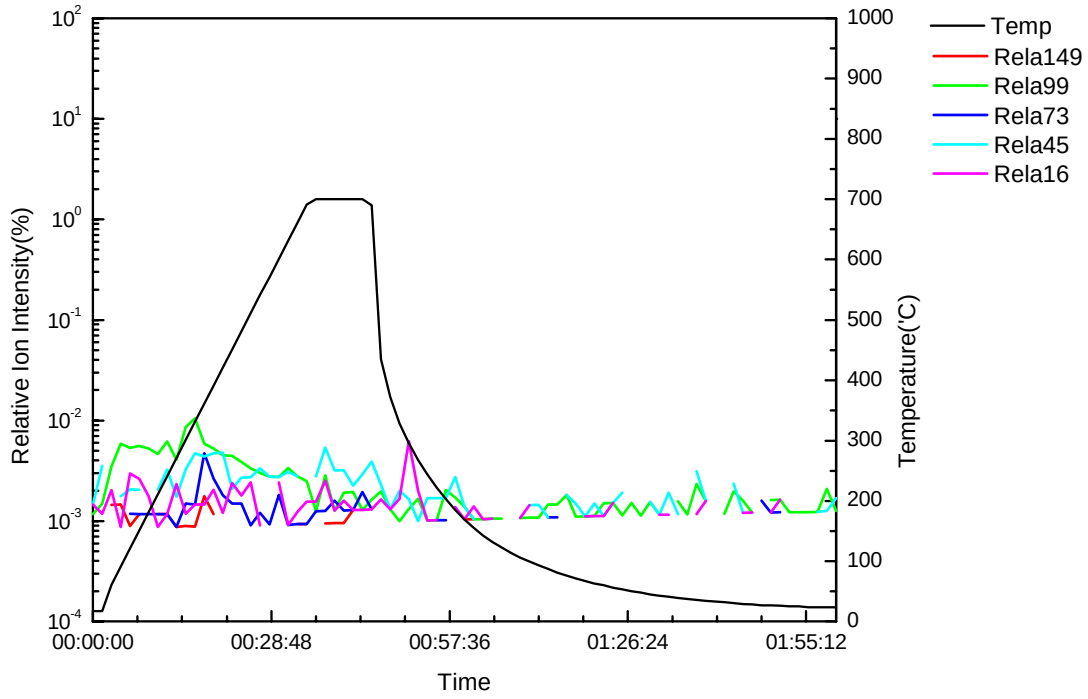


(a)

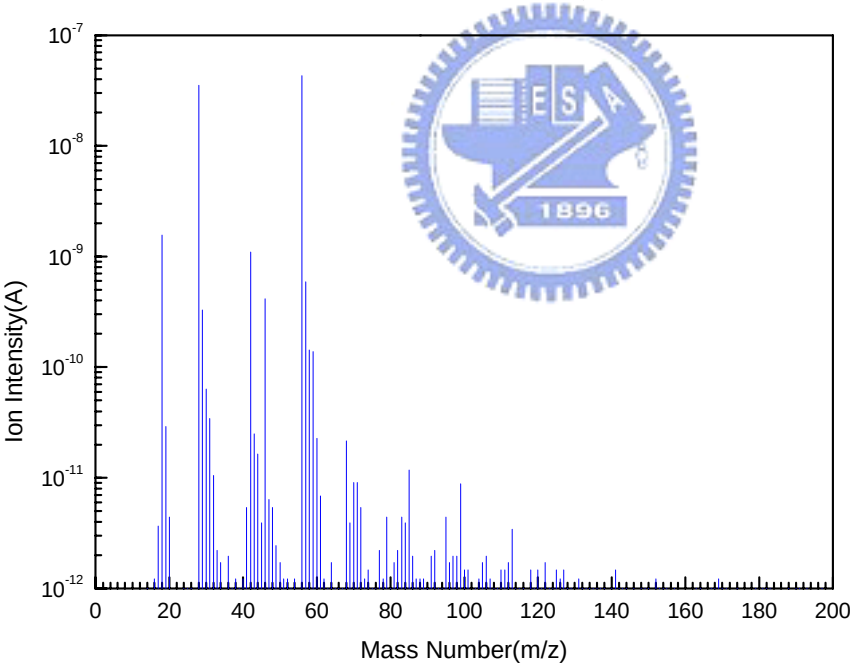


(b)

Fig. 2-10. TDS-APIMS analysis for CB_PTFE filter sample: (a) Time depend ion intensity plot, (b) Mass spectrum at temperature = 336℃.

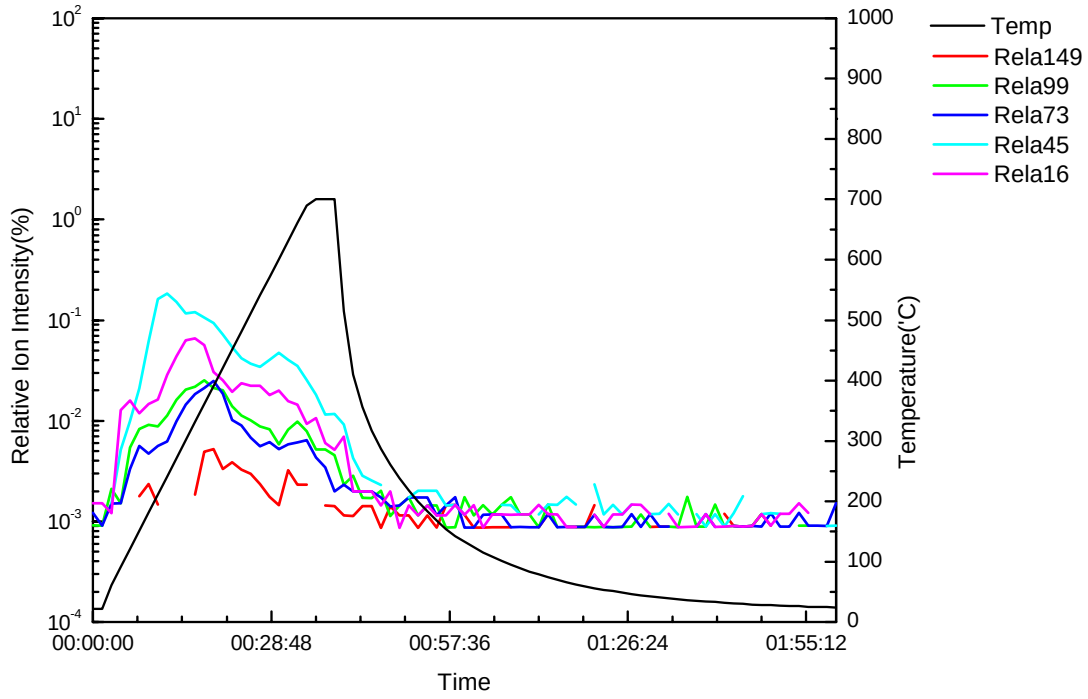


(a)

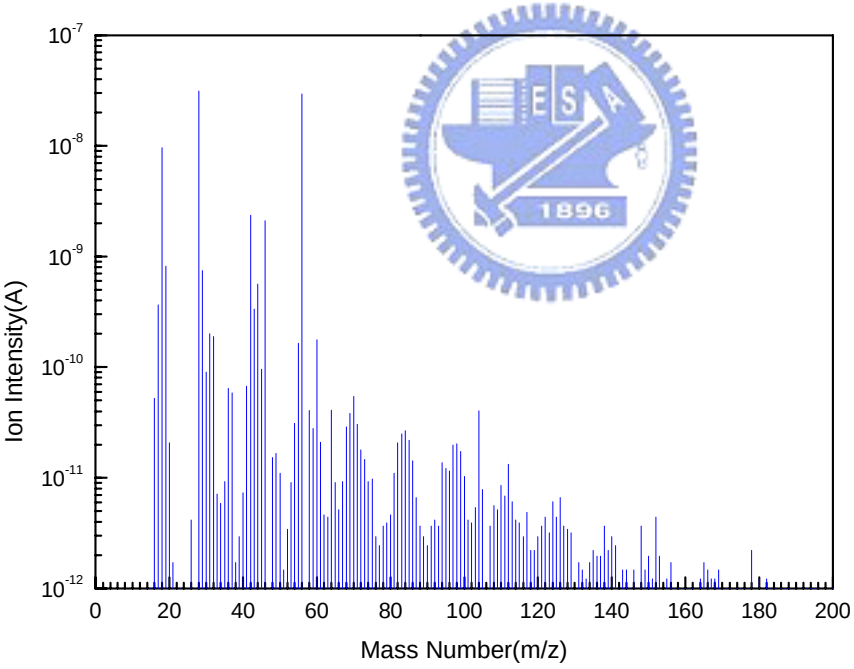


(b)

Fig. 2-11. TDS-APIMS analysis for CB_GF filter sample: (a) Time depend ion intensity plot, (b) Mass spectrum at temperature = 336℃.

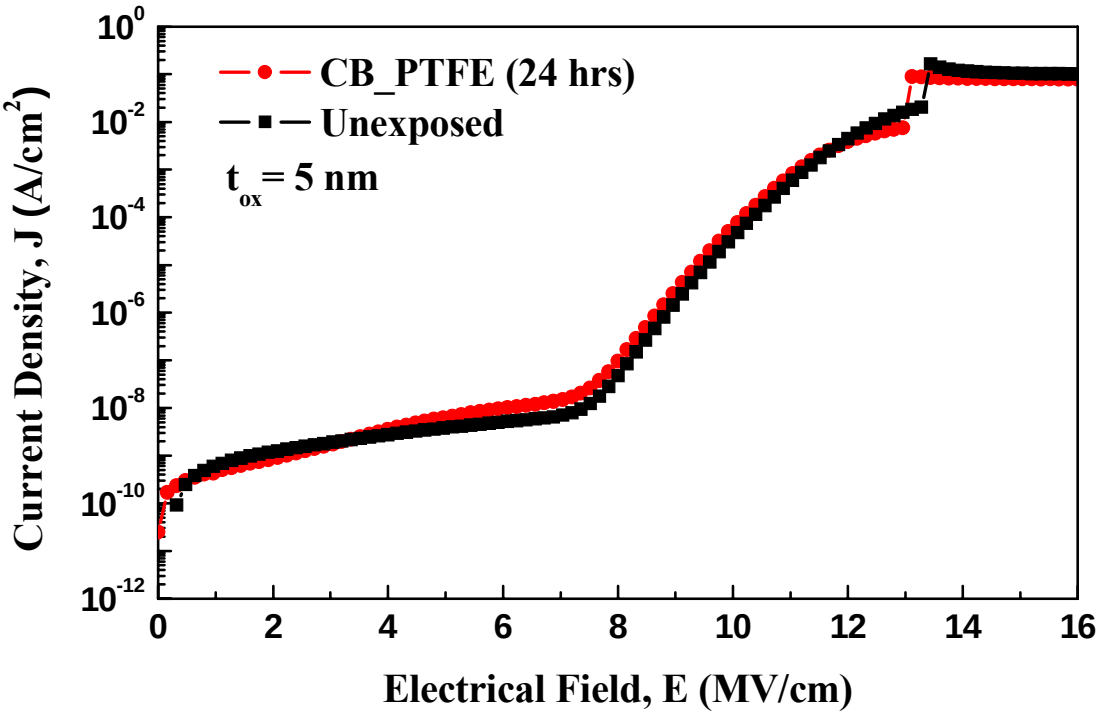


(a)

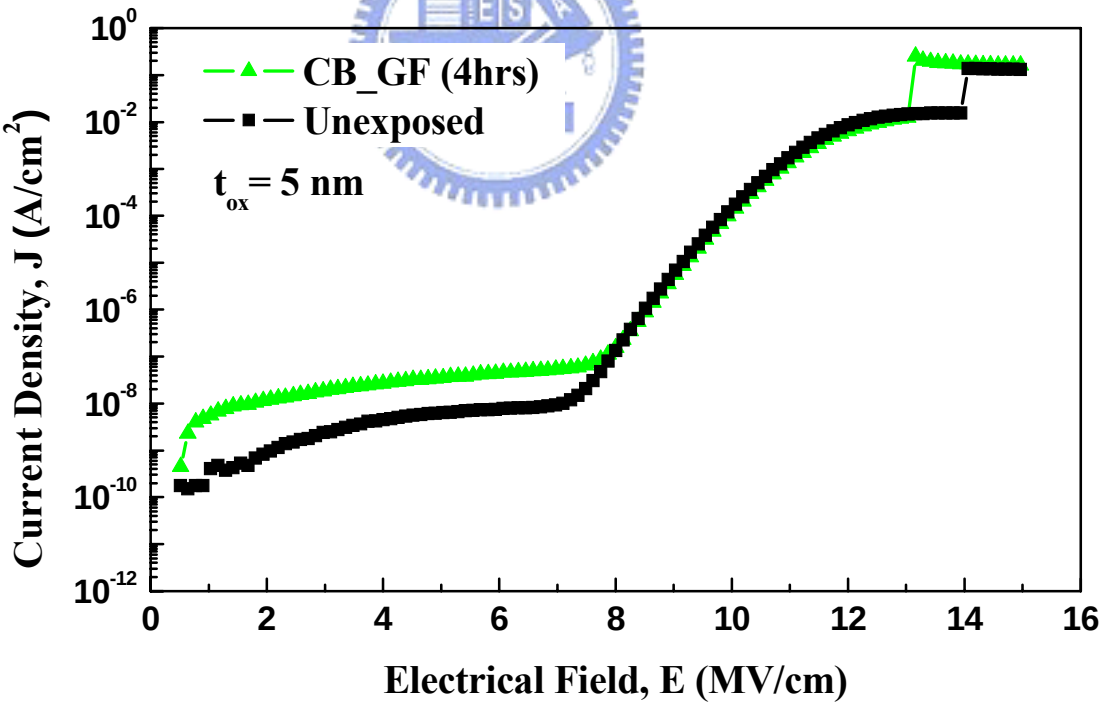


(b)

Fig. 2-12. TDS-APIMS analysis for CR sample: (a) Time depend ion intensity plot, (b) Mass spectrum at temperature = 336℃.

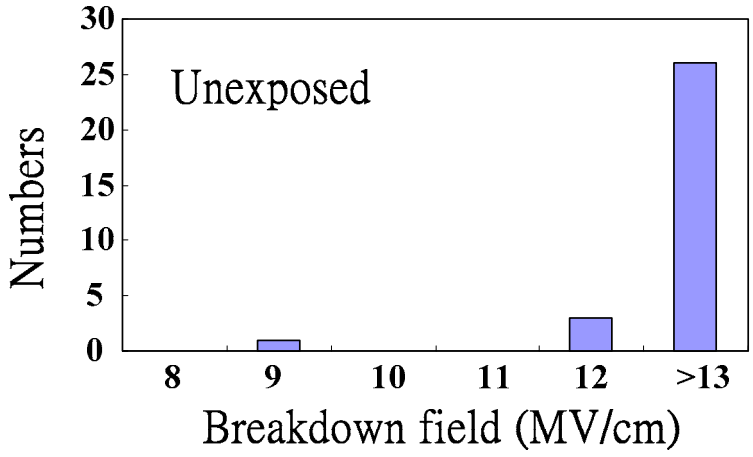


(a)

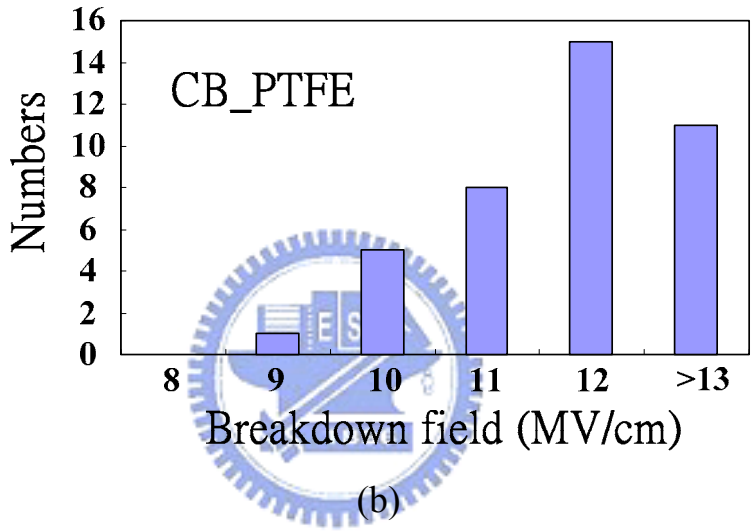


(b)

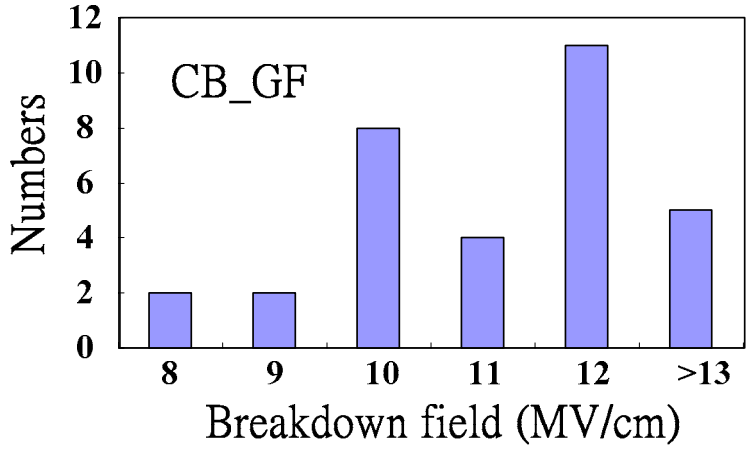
Fig. 2-13. J-E curves of MOS capacitors: (a) PTFE filter and (b) Glass-fiber filter.



(a)



(b)



(c)

Fig. 2-14. Breakdown field distribution of MOS capacitors: (a) Unexposed samples, (b) PTFE filter, and (c) Glass-fiber filter.

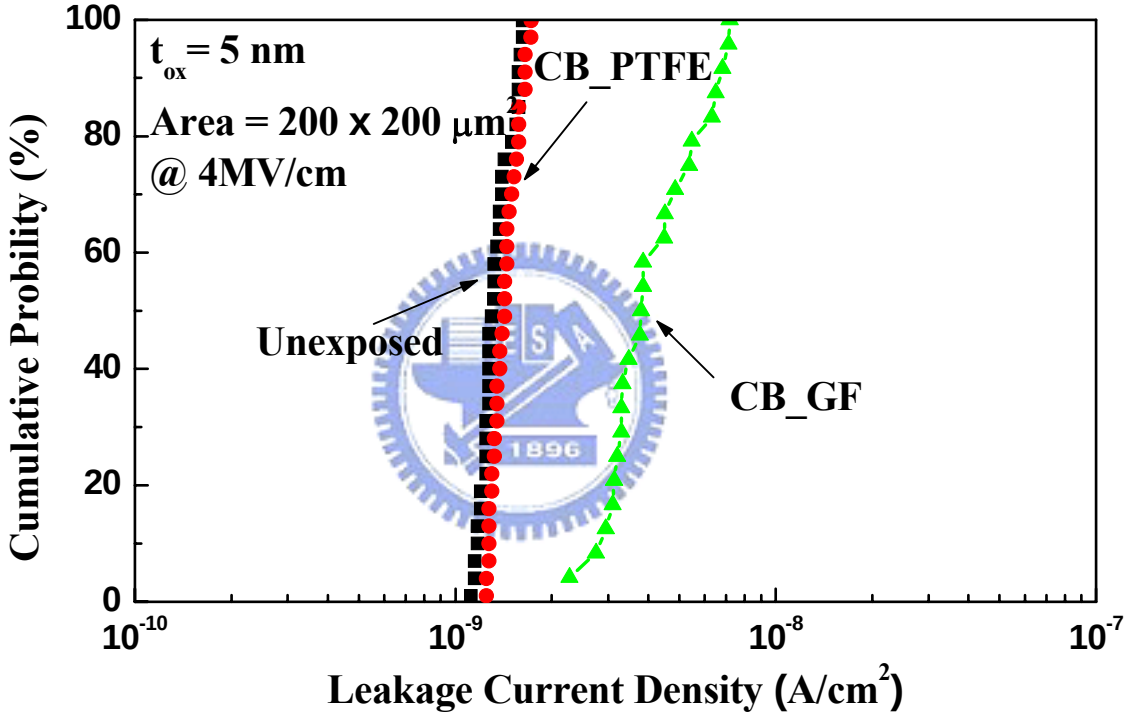


Fig. 2-15. Cumulative probability of leakage current density under different exposure environments.

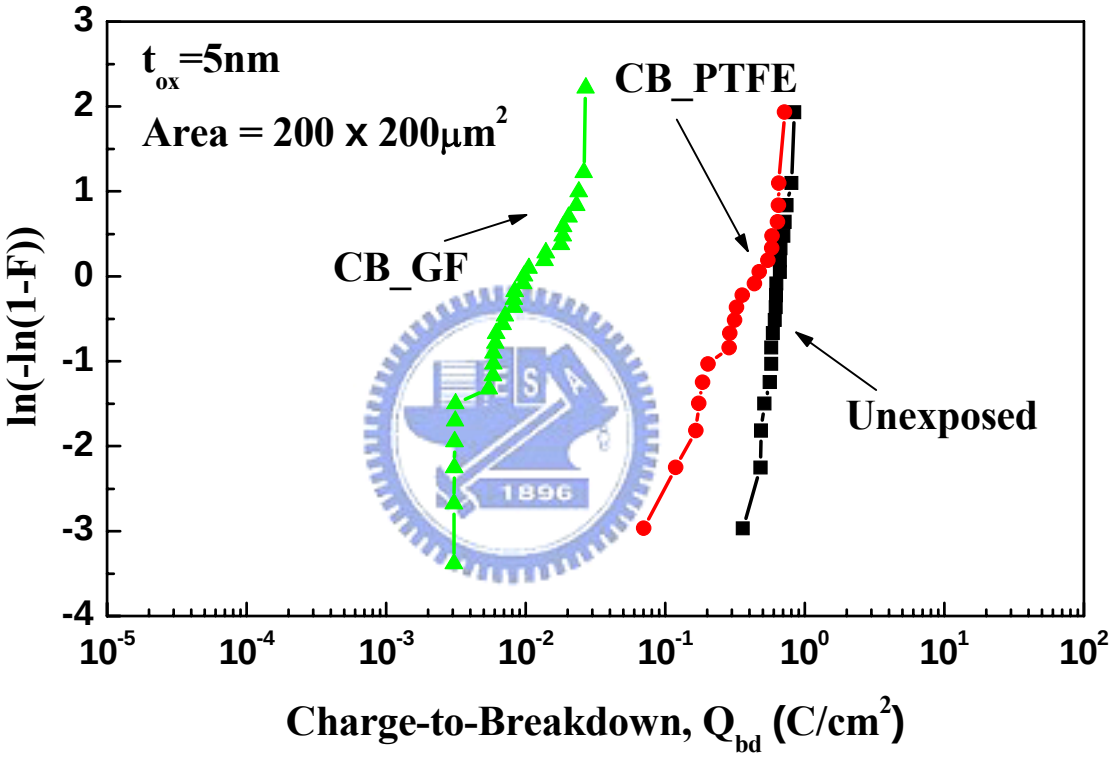


Fig. 2-16. Q_{bd} Weibull plot of MOS capacitors under different exposure environments.

CHAPTER 3

Study on the Degradation of Air Filter in Cleanroom with Acid Vapor Corrosion

3.1 INTRODUCTION

The cleanness of a cleanroom environment must be tightly controlled to achieve high-yield and high-performance ULSI manufacturing [23]-[26]. Recently developed filters, such as HEPA and ULPA filters, effectively eliminate traditional contamination [27]. However, the controllability of airborne molecular contamination (AMC) using present cleanroom technologies has not yet been validated because AMC is a kind of atomic or molecular level gas-phase contamination like organic and inorganic ones. In the near future, especially in the nanodevice era, contamination by organic compounds, inorganic ions and trace doping impurities in air in a cleanroom may dominate the characteristics, reliability, and even yield of devices [28], [29]. Acid vapor generated from the cleaning process is another important issue. Most commercial ULPA filters are made of glass-fiber, which may corroded in an acid vapor environment. Contaminants in a ULPA filter corroded by acid vapor will be released into the cleanroom air and adsorbed onto the surface of wafers, degrading the manufactured devices. Technologies for eliminating AMC from the manufacturing environment must be developed to solve these problems completely. Therefore, the development of a new filter material, which has minimal AMC and is resistant to acid vapor corrosion, is important to the fabrication of high-performance devices.

In this study, the performance of the PTFE and the glass-fiber ULPA filters in HF vapor

environment were investigated. PTFE fiber is considered to be resistant to acid vapor corrosion and it is a good material from which to fabricate ULPA filters. The kinds of AMC and the effects of AMC on devices exposed in the clean bench in a HF vapor environment were examined to elucidate the impact of filter material on device characteristics. The results indicated that the PTFE ULPA filter can provide a better cleanroom environment than a commercial glass-fiber ULPA filter.

3.2 EXPERIMENTS

A specially controlled and fabricated clean bench (CB) was set up in a cleanroom of class 10k. Figure 3-1 schematically depicts the CB. Cleanroom air, from the air inlet of the CB, was initially filtered through a filter module that included inorganic and organic ion chemical filters, before flowing through the main filter, which was designed to be changeable. Two main filters were used, the NEUROFINE PTFE filter (PTFE) and the glass-fiber ULPA filter (GF). The air flow rate and turnover rate inside the CB were set to 0.4 m/s and 5 %, respectively. The exposure experiments were conducted in a 1ppm HF vapor environment.

3.2.1 Evaluation of AMC through Air Sampling

Figure 3-2 presents the air sampling tools, Impinger and TENAX, which were equipped with a flow meter and a pump. The flow rate and sampling time of Impinger were 2 L/min and 24-72 hrs while those of TENAX were 100 mL/min and 5 hrs. Impingers collected mainly both metals and boron elements. These were analyzed using an inductively coupled plasma mass spectrometer (ICP-MS). Organic substances were collected by a TENAX (a kind of absorbent) tube, and quantitatively analyzed by gas chromatograph mass spectrometer (GC-MS). The air in the CR was also analyzed for comparison. Table 3-1 summarizes the air sampling experimental conditions.

3.2.2 Evaluation of AMC through Wafer Sampling

The AMC absorbed on the surfaces of actual 6" P-type (100) Si wafers was analyzed for each filter module. After standard RCA cleaning, wafers were divided into two parts, and exposed to the air in the CR and the CB for 24-72 hrs. The metal contaminants on these wafer surfaces were analyzed using total reflection X-ray fluorescence (TRXRF), while the organic contaminants were analyzed by thermal desorption system–atmospheric pressure ionized mass spectrum (TDS-APIMS). For comparison, the contamination of a wafer not exposed to any environment was evaluated as a control. Table 3-2 is the summary of wafer sampling experimental conditions.

3.2.3 Evaluation of AMC through Electrical Characterization

Metal oxide semiconductor (MOS) capacitors were prepared to investigate the effects of AMC on device characteristics. The active region was first defined on a 6" P-type (100) Si wafer by LOCOS process, and then a 40 nm-thick sacrificial oxide layer was formed by thermal oxidation. This sacrificial oxide layer was subsequently removed, and the wafers were further cleaned by RCA cleaning before exposure. After they had been exposed in the CB for 4-72 hours, a 5 nm-thick oxide layer was grown on each wafer by dry thermal oxidation, and an aluminum gate electrode was finally deposited and patterned. The process flow was shown in Fig. 3-3. These samples were used to evaluate the electrical characteristics. Other samples with the additional thermal annealing step after the exposure experiment were used to evaluate the surface doping concentration and the process flow was shown in Fig. 3-4. The Exposure experiments were conducted in a 1 ppm HF vapor environment. Unexposed control samples were also prepared using the same fabrication procedure. Finally, the electrical characteristics including leakage current density distribution, charge to breakdown (Q_{bd}) and doping concentration were measured through the MOS capacitor using a HP4156

semiconductor parameter analyzer.

3.3 RESULTS AND DISCUSSION

3.3.1 Pre- and Post-corroded Fiber Structure in HF Vapor Environment

Figure 3-5 shows the fiber structure of PTFE-fiber and glass-fiber after the HF vapor corrosion. The pre- and post-corroded fiber structure of PTFE did not reveal any difference and this meant the PTFE-fiber was resistive for HF vapor. On the contrary, the fiber structure of glass-fiber shown in Fig. 3-5(b) displayed the serious degradation in HF vapor environment. The glass-fiber was inevitable to be corroded due to the strong reduction of HF to glass. It is worthy to notice that the corrosion of glass-fiber may release the boron and organic contaminants contained in glass-fiber ULPA filter, thus causing the degradation of device characteristics. Therefore, the PTFE ULPA filter is suitable to be used in acid vapor environment.

3.3.2 Air Sampling Results in HF Vapor Environment

Figure 3-6 is the ICP-MS analysis results of metals and boron for different filter modules in HF vapor environment. The PTFE and the glass-fiber ULPA filter can effectively filter the metals including Na, K, Ca, Mg and Al. The CB with the PTFE and the GF ULPA filter, however, showed higher concentration of Fe ions than CR. It was suggested that the steel construction of clean bench corroded by HF vapor, releasing the Fe ions to air. Besides, the CB with GF filter showed large concentration of boron than the CB with PTFE filter. This may due to the corrosion of glass-fiber in HF vapor, releasing the boron atoms contained in glass-fiber as mentioned above. The detail analysis results of ICP-MS are listed in Table 3-3.

The organic compounds were considered to be another contamination the glass-fiber will release in HF vapor. Figure 3-7 shows the analysis results of GC/MS. It was found that all the

organic contaminants were removed in the CB with PTFE filter. But for the CB with GF filter, high concentration of organic contaminants appeared. According to our study in Chapter 2, these organic contaminants may come from the binder in GF ULPA filter. In HF vapor environment, the degradation of glass-fiber will release more organic contaminants as show in Fig. 3-7. Table 3-4 shows the detail analysis results of GC/MS.

3.3.3 Wafer Sampling Results in HF Vapor Environment

Metal contaminants on wafer surface exposed in the CB in HF vapor environment were quantified by TRXRF analysis. As shown in Fig. 3-8, the densities of metal on different wafers are compared and the detail data are shown in Table 3-5. The "Unexposed" sample refers to a wafer treated only by RCA cleaning and unexposed to air before analysis. On each wafer, five points were analyzed and the averages of the results at these points were compared. The wafer exposed in cleanroom showed higher metal density than the wafers exposed in CB with PTFE or GF filter. This result proved the better filtration efficiency of both PTFE and GF ULPA filter. The Fe ion was previously observed to have high concentration in air sampling; however, in the wafer sampling it showed low concentration. This might be the metals usually adhered to the particles and hence the low particle concentration in the CB with ULPA filter showed low concentration of metals.

Next, the intensity of organic contaminants on the wafer exposed in CB in HF vapor environment was evaluated using TDS-APIMS. Figure 3-9 to Fig. 3-12 compares results for different samples. The concentrations of each specifies of organic contamination of the CR sample greatly exceeded that of the CB sample, revealing that the wafer surface exposed in the CR does absorb much organic contamination. Here, mass numbers m/z = 16, 45, 73, 99, 149 were chosen. Contamination peaks at m/z = 16, 45, 149 often come from the outgassing of oil based plasticizers, which are widely used in plastic products of the cleanroom, such as

DEP and DBP. Peaks at m/z = 73, 99 are often associated with the absorption of Si-based siloxane, such as D5 and D6. As shown in Fig. 3-10 and Fig. 3-11 for the CB with the PTFE and the GF filter, the intensity of m/z > 99 of the GF filter exceeds that of the PTFE filter. The peak of m/z >99 usually represented the D5 and DBP. The result was quite consistent with the air sampling results presented in Fig. 3-7. The PTFE ULPA filter in a CB provided a high resistivity to HF vapor and hence with rather low concentrations of organic compounds than GF ULPA filter.

3.3.4 Electrical Characteristics of MOS Capacitors

In the cleanroom environment, the acid vapor generated from the cleaning process may accelerate the degradation of filters, releasing AMC to the processing environment. In this study, MOS capacitors with thin oxide as insulating layer were prepared to investigate the effect of AMC on device performance. The MOS capacitors were exposed in the CB for four hours before the insulating layer were formed. The PTFE and the glass-fiber ULPA filters were individually set in the CB. During exposure, the HF vapor was used to simulate acid vapor corrosion in the cleanroom. Figure 3-13 presents the leakage current density distribution of MOS capacitors in different ULPA filters. The devices in the CB that included a GF as the main filter had a larger leakage current than the unexposed control samples, while the PTFE samples showed a smaller leakage current. The devices may have been degraded by the corrosion of the GF filter in the HF vapor environment. Figure 3-5 illustrates the structures of glass-fiber and PTFE-fiber. Most glass fibers are short and so a binder must be used to combine the fibers in a dense network. Thus, the glass-fiber can be used to filter out the contamination. PTFE-fibers, however, are long and do not require a binder. It is important that the glass-fiber can be corroded in an acid vapor environment, especially in HF vapor. The boron in glass-fiber, which is used to soften the fiber and facilitate the fabrication of the filter,

may diffuse into the air in a cleanroom. The binder, which is mainly composed of organic compounds, can also be released [39]. As shown in Fig. 3-6 and Fig. 3-7, the GF filter released more organic compounds and boron atoms than PTFE filter under HF vapor corrosion. These contaminants may be adsorbed onto wafer surface and degrade the thin oxide layer. Accordingly, the experimental results reveal the poor electrical characteristics of devices exposed in the CB with a GF filter. However, resistivity to corrosion in HF vapor enables the devices in the CB with a PTFE filter to exhibit better characteristics, even close to those of the unexposed samples. Figure 3-14 shows the resulting Q_{bd} characteristics of the two kinds of filters. Similarly, the devices in the CB with a GF filter had the poorest characteristics of all the samples. The devices in the CB with a PTFE filter yielded almost the same results as the unexposed samples. These findings confirmed that the PTFE filter can resist the acid vapor corrosion and provide an optimum cleanroom environment, yielding devices with characteristics similar to those of unexposed devices.

3.3.5 Trace Doping of MOS Capacitors

In Fig. 3-6, the GF filter was suggested to release more boron contaminants in an environment of HF vapor. Boron contaminants adsorbed onto the surface of the wafer will over-dope or count-dope the silicon surface and change its electrical parameters (such as the threshold voltage). These changes will become severe when the device is shrunk to nanometer dimensions. In the experiment, two filters were compared to investigate the effect of boron contaminants on device performance. The experimental procedure was similar to that described above, except in that the exposure time was 72 hrs and the devices were annealed at 900 ℃ for 30 min. after exposure. The silicon wafers were epitaxial wafers whose doping concentrations varied by less than 2%. Figure 3-15 is the measured silicon surface doping concentration of MOS capacitors. The surface concentrations of unexposed control samples

were approximately 2×10^{15} /cm^3. Figure 3-15 indicates that the surface concentrations of devices exposed in the CB with a GF filter varied over a wide range, whose maximum was about twice the minimum. In contrast, the devices exposed in the CB with a PTFE filter showed a uniform distribution of surface concentrations, which were almost equal to that of the unexposed samples. The results imply that the HF vapor corroded the glass fiber, releasing the boron contaminants, causing over-doping of the silicon surface. The results also suggested that HF vapor only slightly corroded the PTFE filter.

3.5 SUMMARY

The qualitative and quantitative analyses of AMC in the CB with different filter module in HF vapor environment were investigated. The experimental results showed that the GF ULPA filter will release boron and organic contaminants in HF vapor environment, while the PTFE ULPA filter still maintained low concentration of contaminants. The effects of the materials from which air filters are made on device characteristics were also investigated. The glass-fiber ULPA filter released AMC when exposed in an HF vapor environment. These contaminants included organic compounds and boron trace dopants and degraded the device characteristics. In contrast, the HF vapor did not affect the PTFE ULPA filter. These results suggested that the PTFE fiber can be a good ULPA filter material for providing a very clean cleanroom environment.

TABLE 3-1
Summary of Air Sampling Experimental Conditions

Contamination Type	Sampling Equipments	Flow Rate	Sampling Time	Analysis Method
Organic Compounds	TENAX Tube	100 mL/min.	5 hrs	GC/MS (Gas Chromatograph Mass Spectrometer)
Metals & Boron	Impinger	2 L/min.	72 hrs	ICP-MS (Inductively Coupled Plasma Mass Spectrometer)

Bench Condition
Filter module: 1. PTFE ULPA filter + Chemical filter
2. Glass-Fiber ULPA filter + Chemical filter
Air flow rate: 0.4 m/s
Turnover rate: 5%
Temperature: 23 ℃
1ppm HF Vapor

TABLE 3-2
Summary of Wafer Sampling Experimental Conditions

Contamination Type	Exposing Location	Exposing Time	Analysis Method	Elements
Organic Compounds	CR and CB	24 hrs	TDS-APIMS (Thermal Desorption System – Atmospheric Pressure Ionized Mass Spectrum)	D3, D4, D5, D6, DEP, DBP, TEP, TBP, BHT
Metals		72 hrs	TRXRF (Total Reflection X-Ray Fluorescence)	Na, K, Ca, Mg, Fe, Ti, V, Cr, Mn, Co, Ni, Cu, Zn

Bench Condition
Filter module: 1. PTFE ULPA filter + Chemical filter
2. Glass-Fiber ULPA filter + Chemical filter
Air flow rate: 0.4 m/s
Turnover rate: 5%
Temperature: 23 ℃
1ppm HF Vapor

TABLE 3-3
Air Sampling Results of Metals and Boron in HF Vapor Environment

Metals & Boron ($\mu g/m^3$)	CR	Detection Limit	CB_PTFE	Detection Limit	CB_GF	Detection Limit
Inlet Filter	-		Chemical Filter		Chemical Filter	
Main Filter	-		PTFE Filter		Glass-Fiber Filter	
Na	0.25	0.002	<0.004	0.004	<0.002	0.002
K	0.006	0.004	<0.004	0.004	<0.004	0.004
Ca	0.004	0.004	<0.004	0.004	<0.004	0.004
Mg	<0.004	0.004	<0.004	0.004	<0.004	0.004
Al	<0.004	0.004	<0.004	0.004	<0.004	0.004
Fe	<0.004	0.004	0.008	0.004	0.05	0.004
B	0.024	0.0008	0.0036	0.0008	0.062	0.0009

TABLE 3-4
Air Sampling Results of Organic Compounds in HF Vapor Environment

Organic Compounds ($\mu g/m^3$)	CR	Detection Limit	CB_PTFE	Detection Limit	CB_GF	Detection Limit
Inlet Filter	-		Chemical Filter		Chemical Filter	
Main Filter	-		PTFE Filter		Glass-Fiber Filter	
D3:$C_6H_{18}O_3Si_3$	2.1	0.03	<0.03	0.03	*1	0.03
D4:$C_8H_{24}O_4Si_4$	<0.07	0.07	<0.07	0.07	0.11	0.07
D5:$C_{10}H_{30}O_5Si_5$	0.34	0.03	<0.03	0.03	0.14	0.03
D6:$C_{12}H_{36}O_6Si_6$	0.04	0.03	<0.03	0.03	0.14	0.03
DEP:$C_{12}H_{14}O_4$	<0.03	0.03	<0.03	0.03	0.27	0.03
DBP:$C_{16}H_{22}O_4$	0.27	0.22	<0.22	0.22	1.4	0.22
TEP:$C_6H_{15}O_4P$	<0.03	0.03	<0.03	0.03	<0.03	0.03
TBP:$C_{12}H_{27}O_4P$	<0.03	0.03	<0.03	0.03	<0.03	0.03
BHT:$C_{15}H_{24}O$	<0.03	0.03	<0.03	0.03	0.04	0.03

*1: Can not separate organic compounds peaks

TABLE 3-5

Wafer Sampling Results of Metals in HF Vapor Environment

Metals (10^{10} atoms/cm^2)	BLANK	CB_PTFE	CB_GF	CR
Inlet Filter	-	Chemical Filter	Chemical Filter	-
Main Filter	-	PTFE Filter	Glass-Fiber Filter	-
Na	-	-	-	-
Mg	-	-	-	-
K	56.7	57.5065	-	317.7524
Ca	-	-	-	468.67
Ti	-	-	4.319	43.2312
V	-	4.719	2.96	4.926
Cr	4.172	4.456667	3.062	9.6664
Mn	4.952	4.695	2.55	9.1372
Fe	-	-	1.441	262.6284
Co	-	1.943333	1.175	3.628667
Ni	-	-	-	-
Cu	3.014	2.276	-	4.5346
Zn	-	-	1.94	30.5904

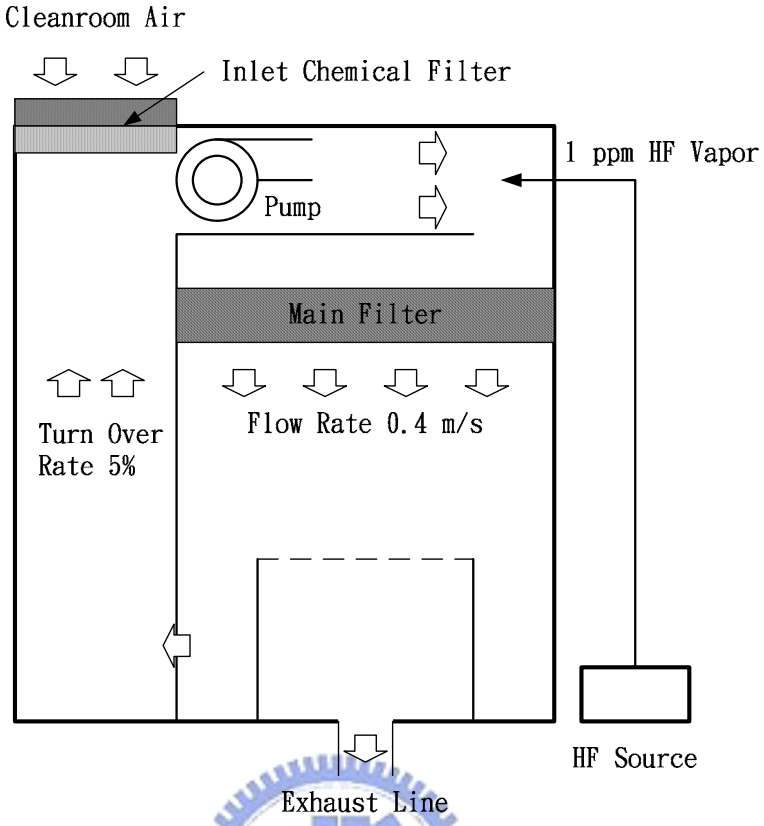


Fig. 3-1. Schematic diagram of specially designed clean bench with the HF vapor.

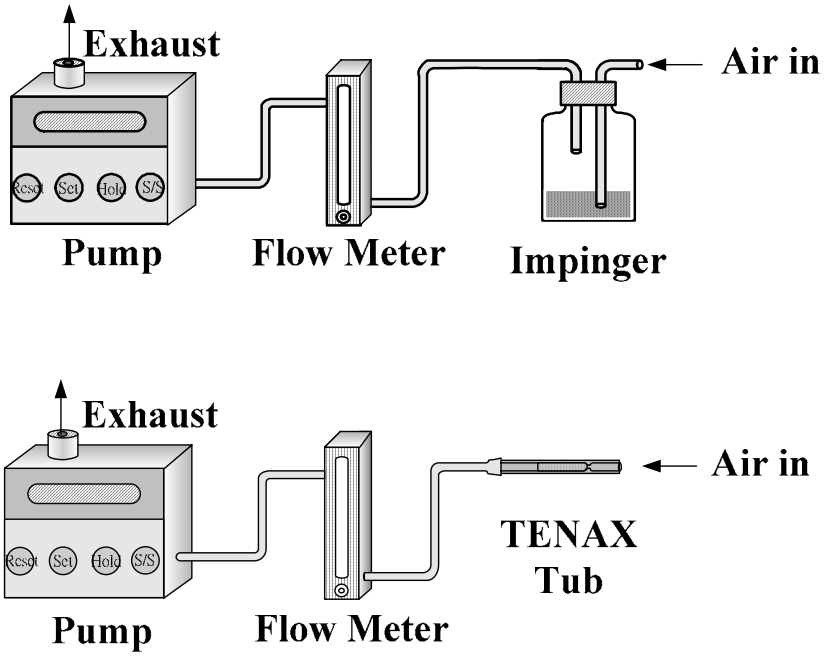


Fig. 3-2. Air sampling equipments used for the evaluation of metals and organic contaminations.

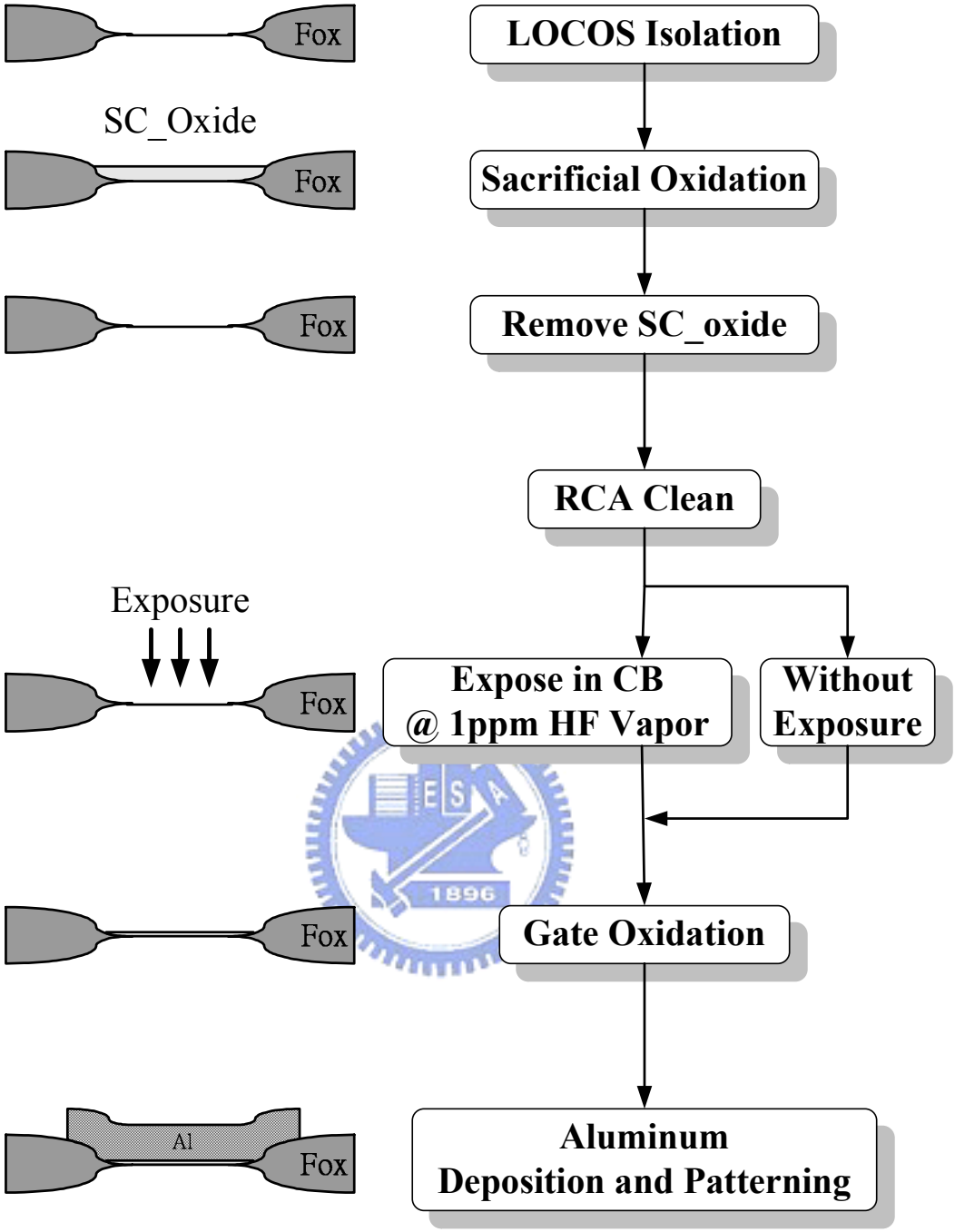


Fig. 3-3. Process flow of MOS capacitor exposure experiment used to evaluate the electrical characteristics.

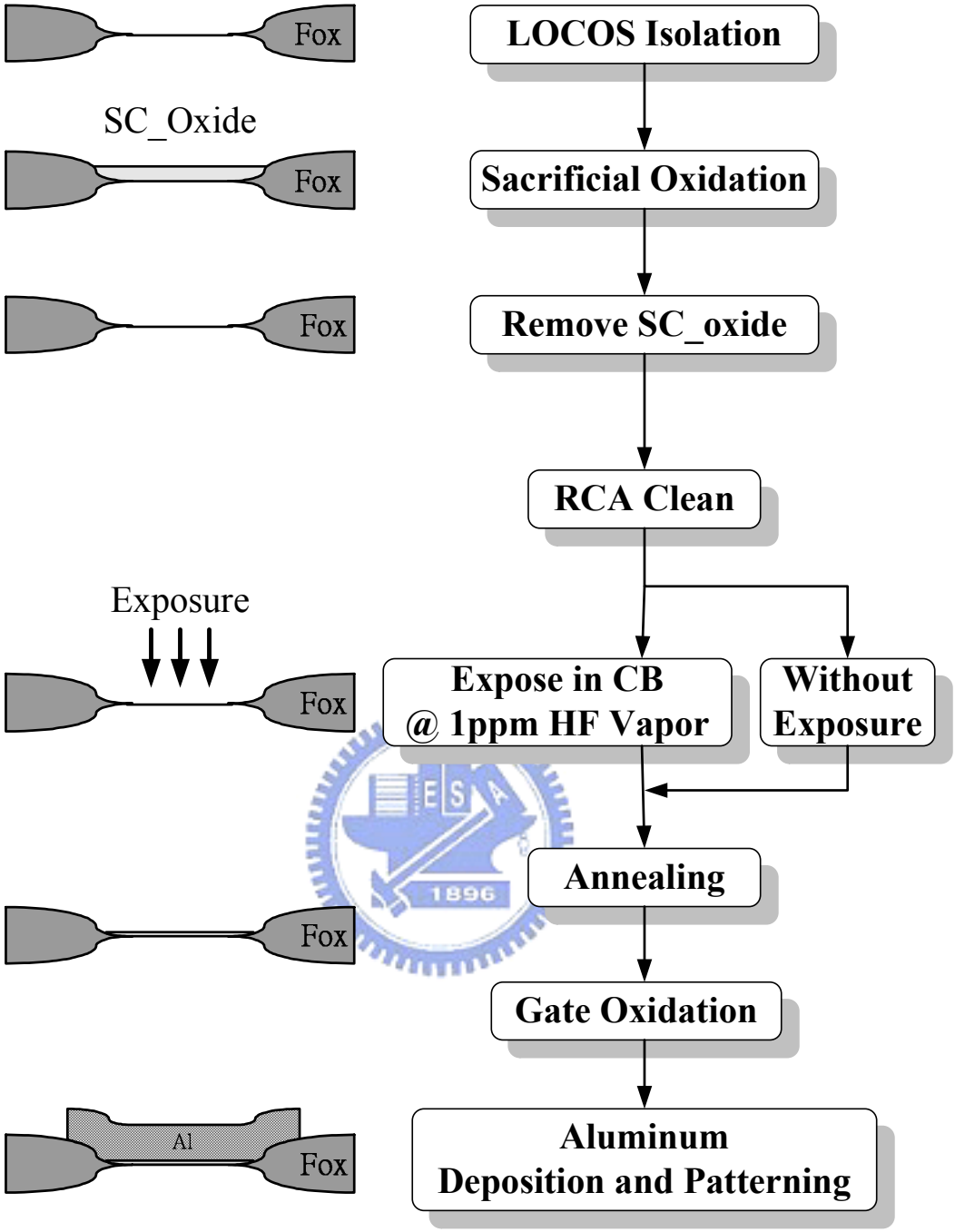
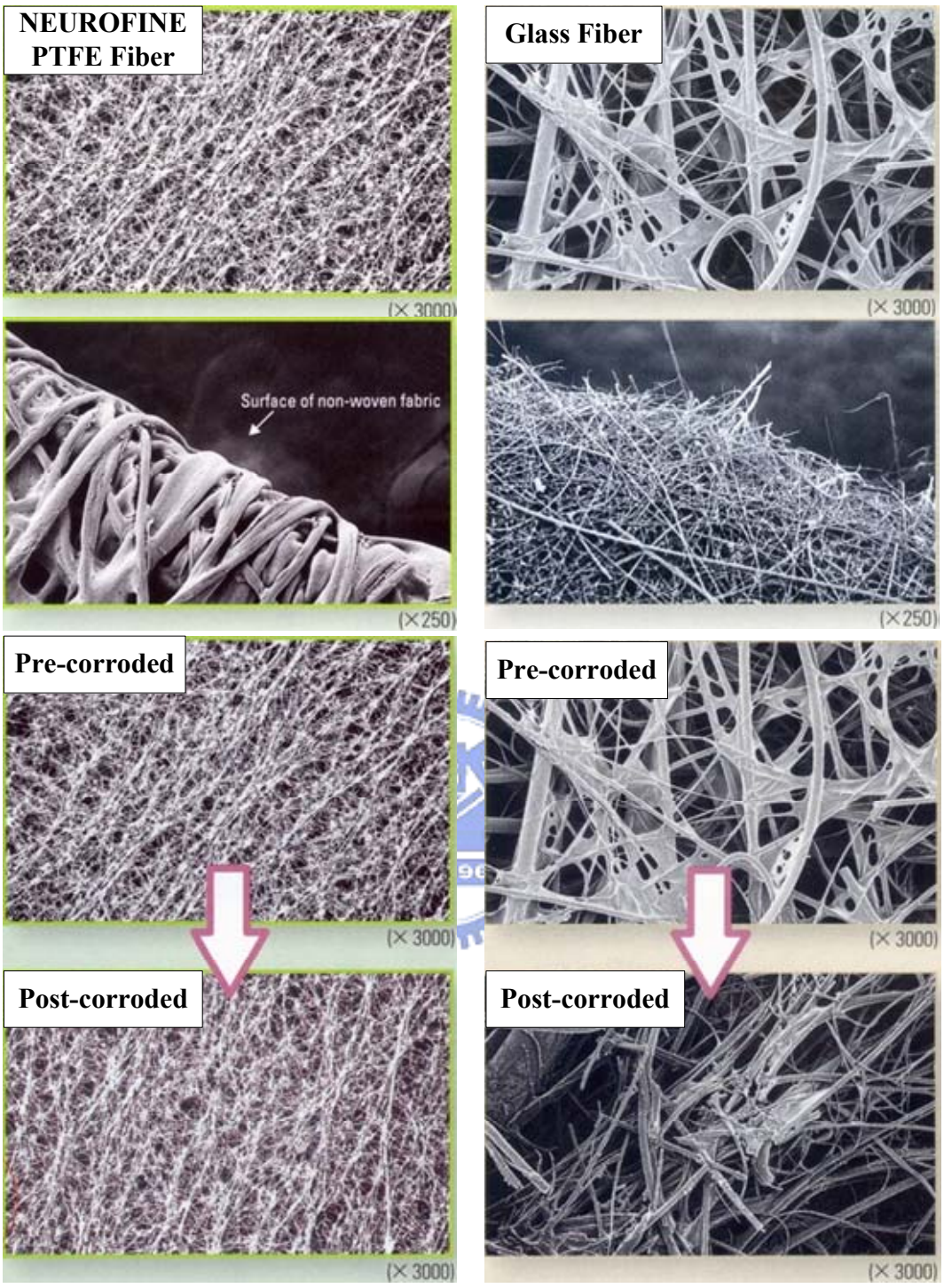


Fig. 3-4. Process flow of MOS capacitor exposure experiment used to evaluate the surface doping concentration.



(a) (b)

Fig. 3-5. The SEM photographs of (a) PTFE-fiber and (b) Glass-fiber structures.

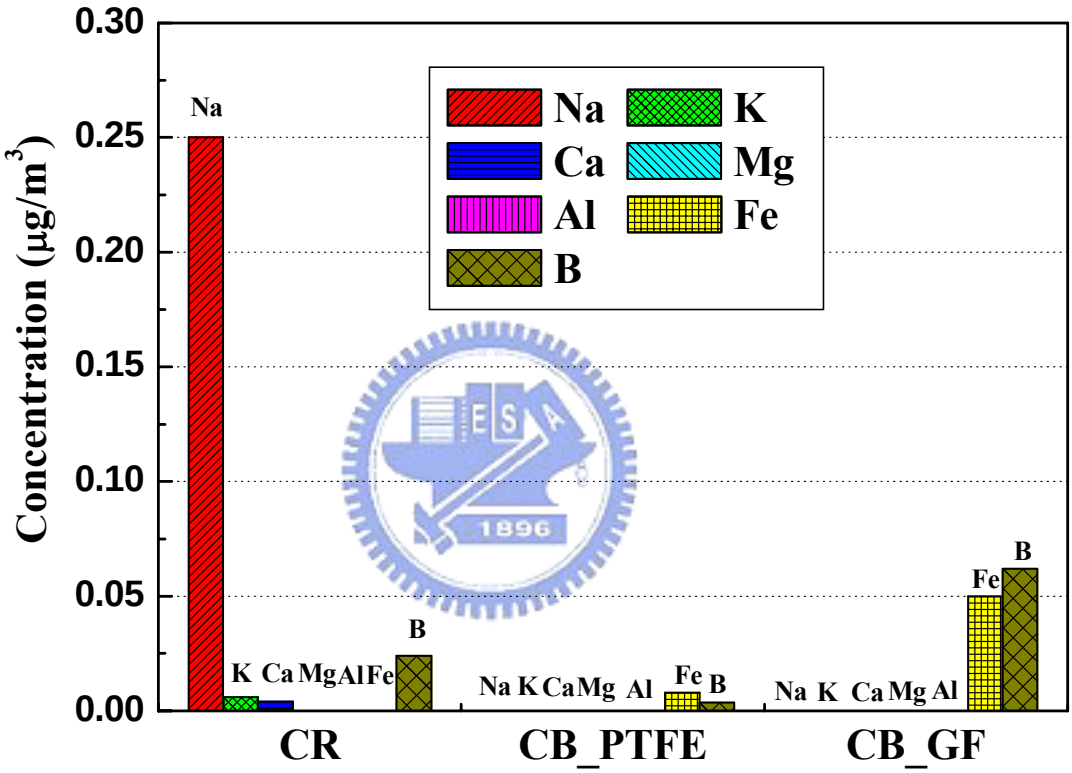


Fig. 3-6. Air sampling results of metals and boron in HF vapor environment.

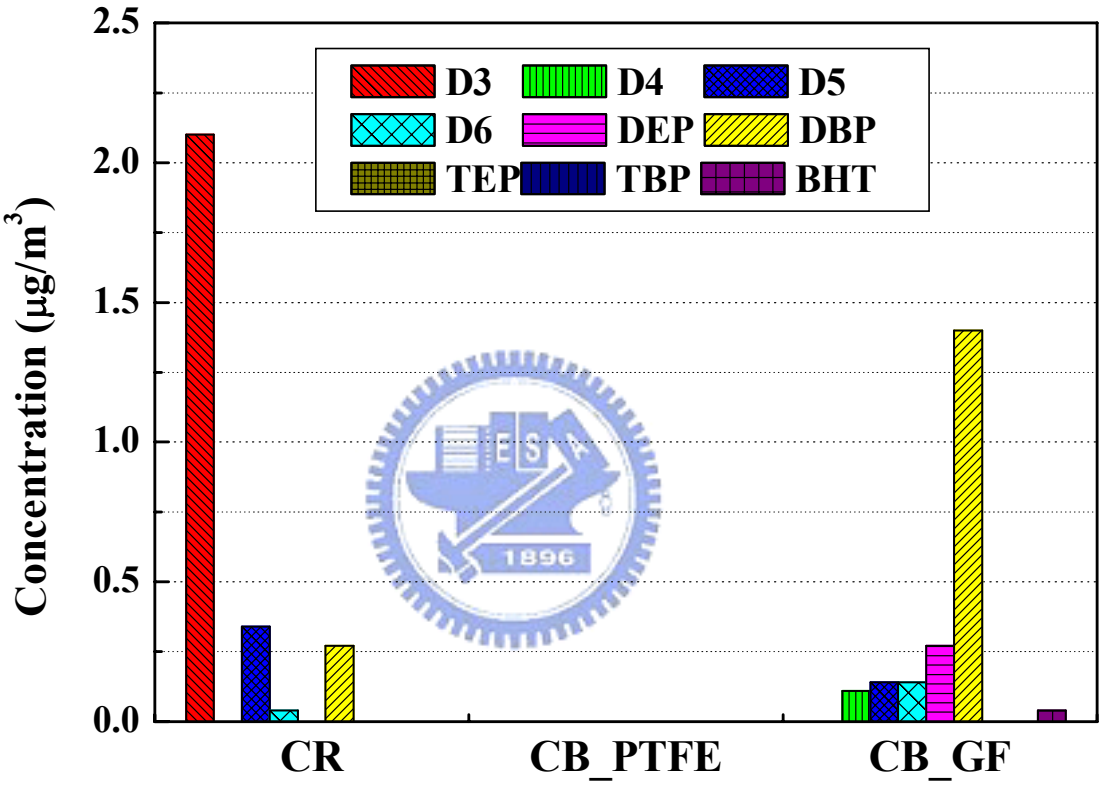


Fig. 3-7. Air sampling results of organic compounds in HF vapor environment.

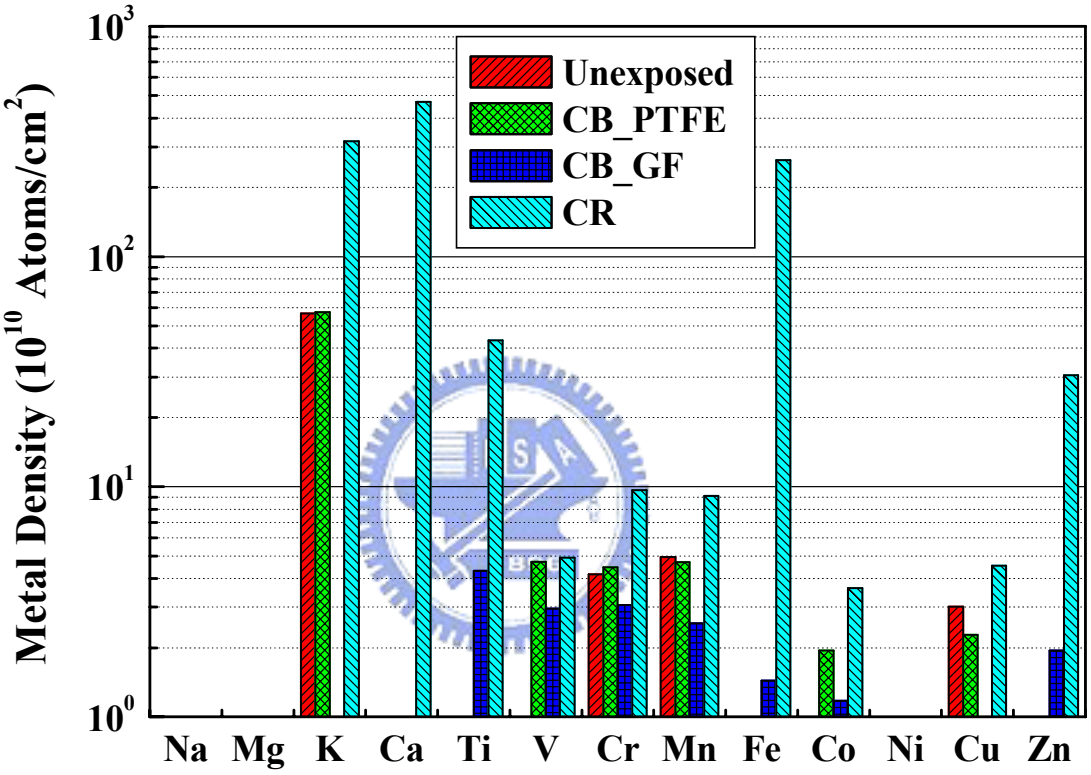
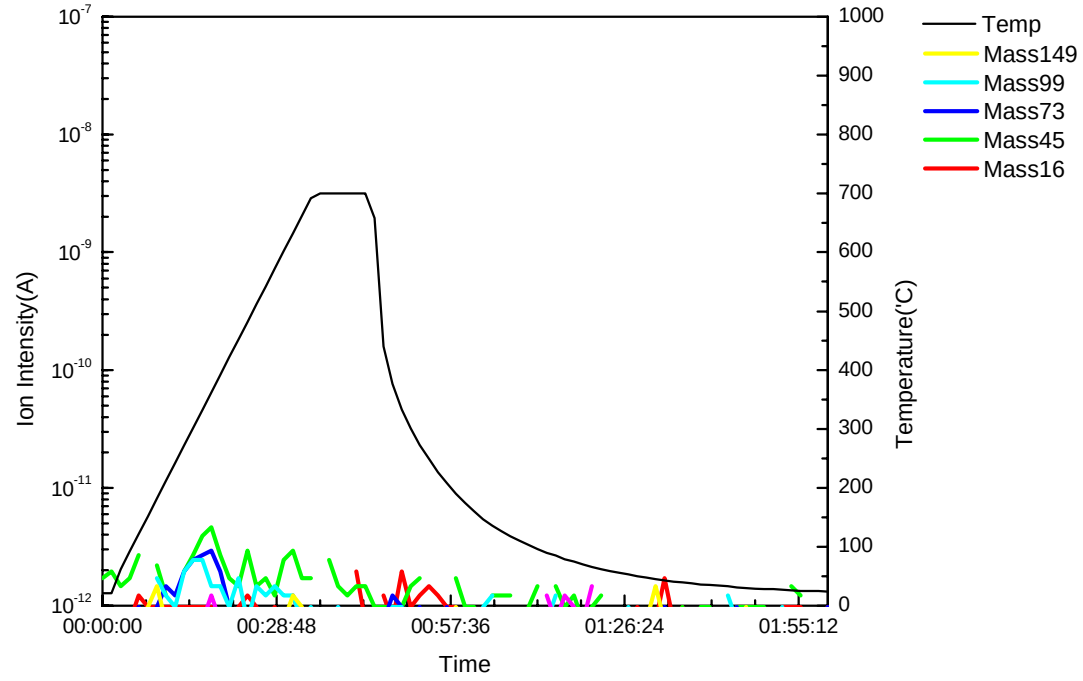
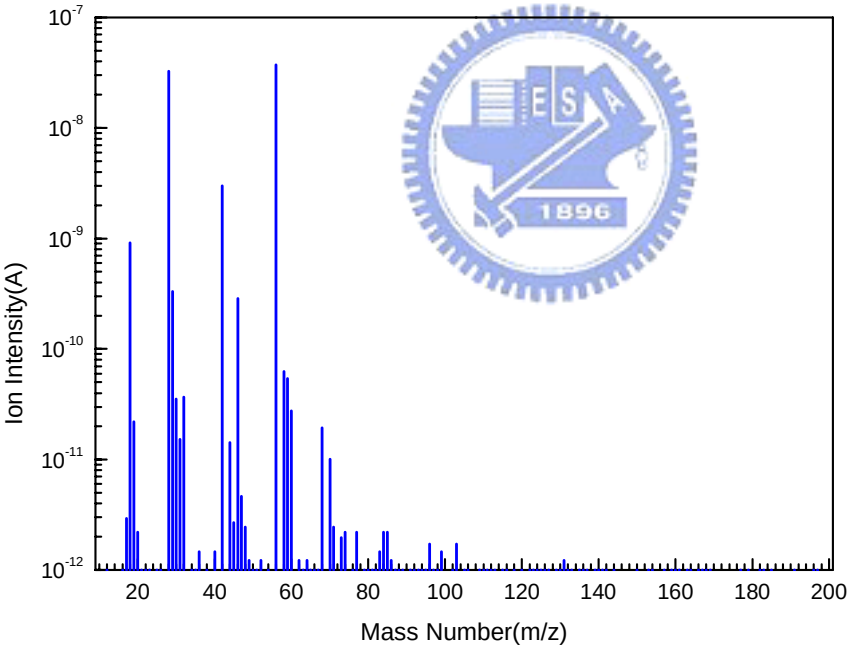


Fig. 3-8. Wafer sampling results of metals in HF vapor environment.

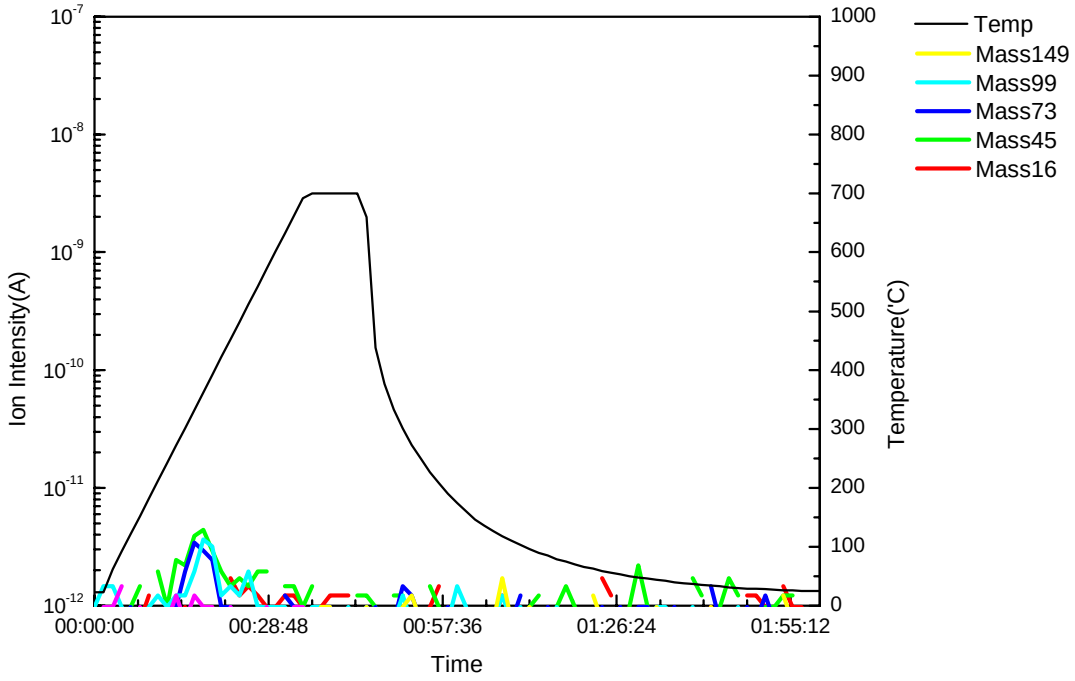


(a)

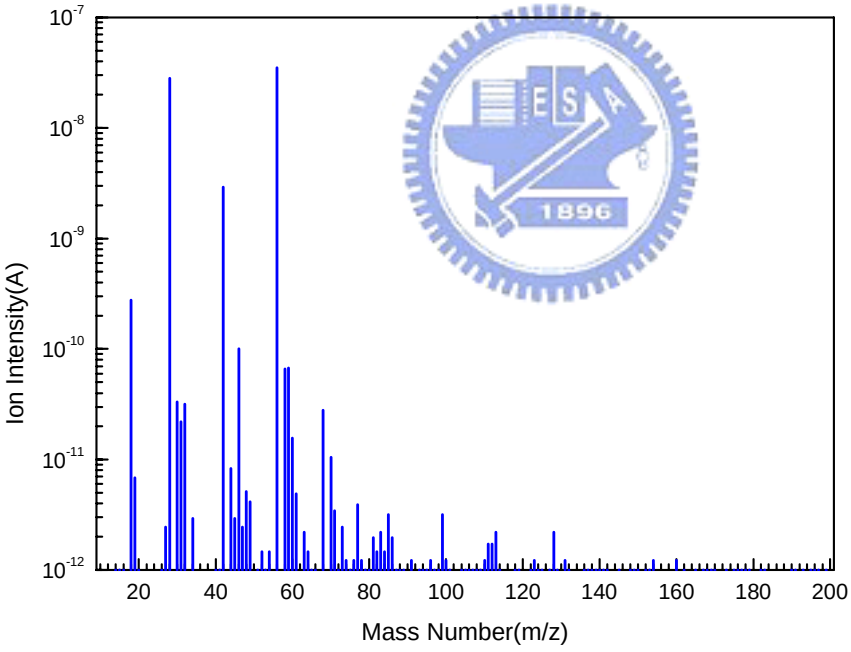


(b)

Fig. 3-9. TDS-APIMS analysis for unexposed sample: (a) Time depend ion intensity plot, (b) Mass spectrum at temperature = 400℃.

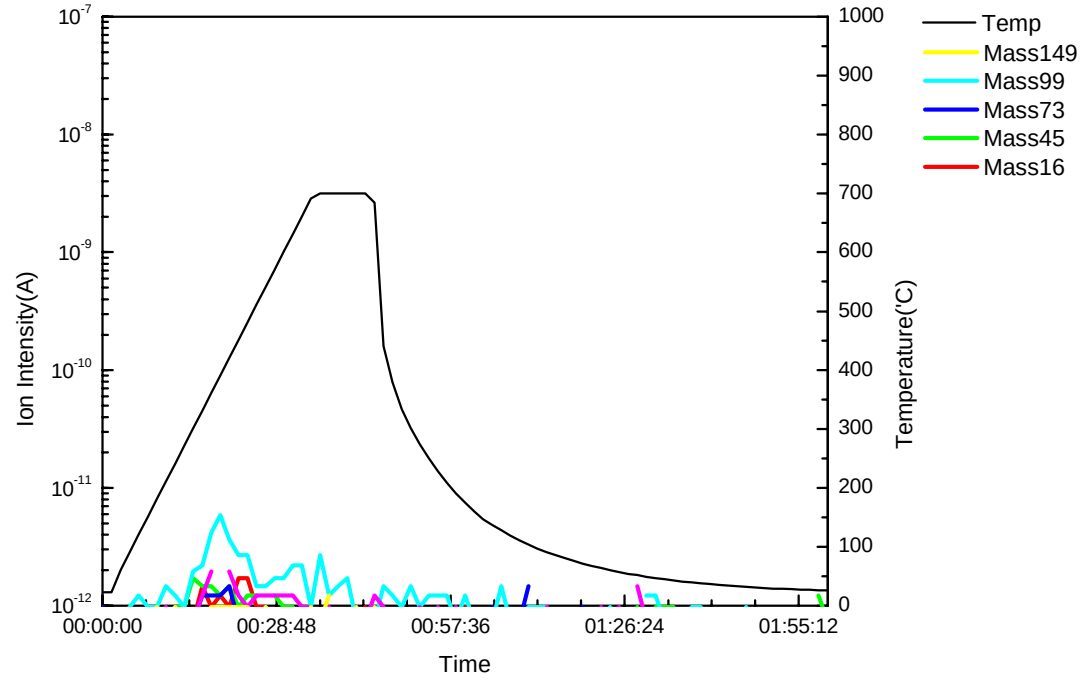


(a)

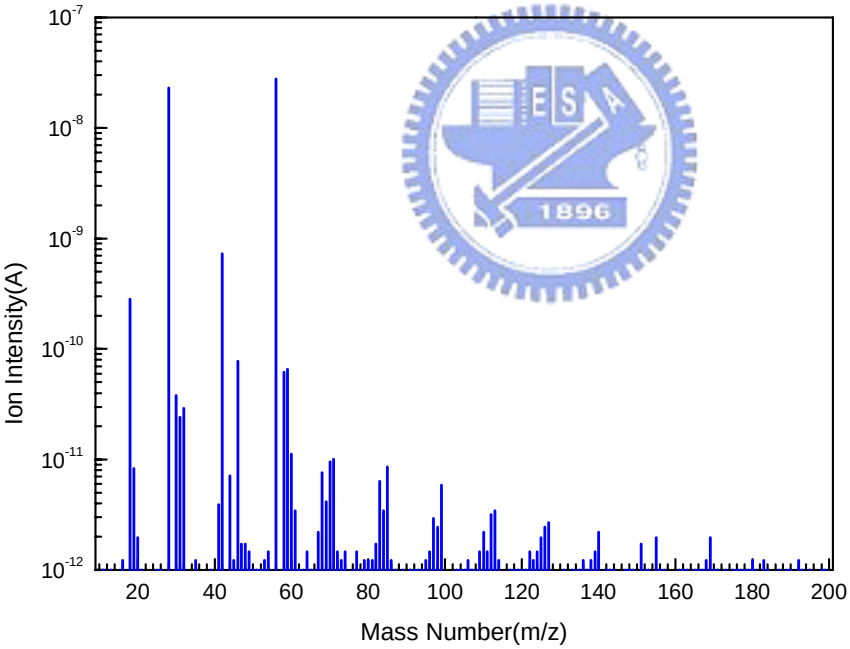


(b)

Fig. 3-10. TDS-APIMS analysis for CB_PTFE filter sample: (a) Time depend ion intensity plot, (b) Mass spectrum at temperature = 400℃.

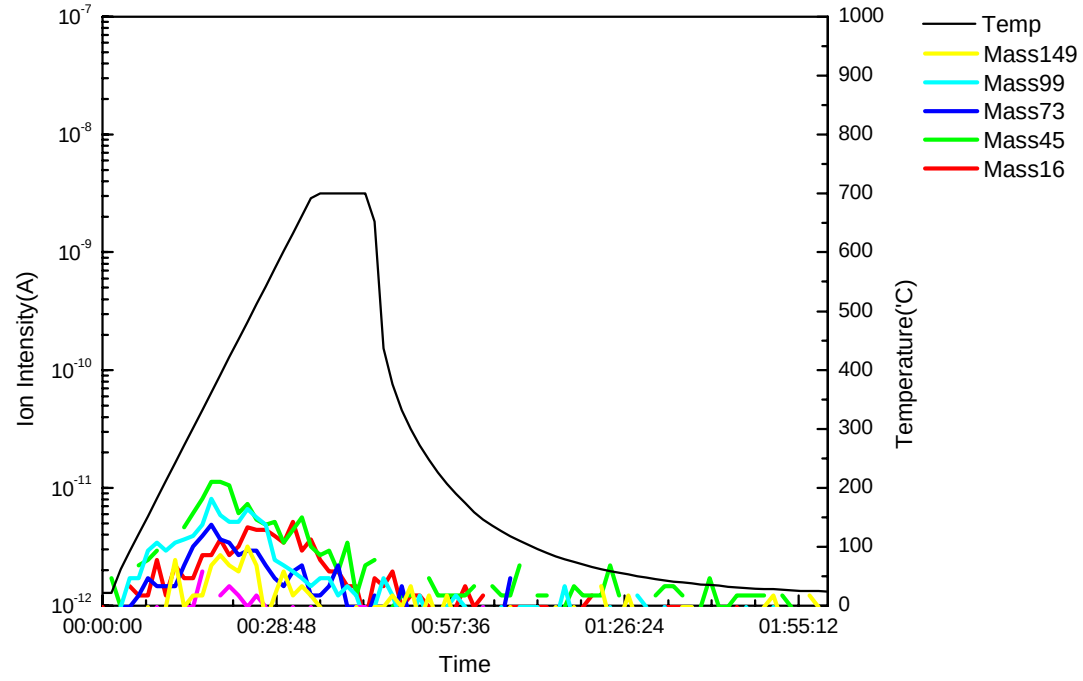


(a)

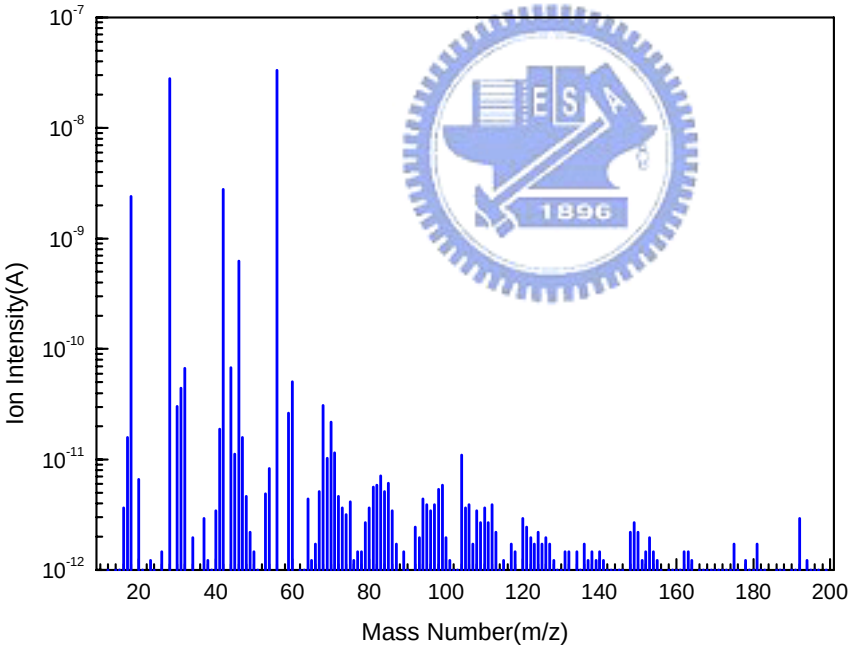


(b)

Fig. 3-11. TDS-APIMS analysis for CB_GF filter sample: (a) Time depend ion intensity plot, (b) Mass spectrum at temperature = 400℃.



(a)



(b)

Fig. 3-12. TDS-APIMS analysis for CR sample: (a) Time depend ion intensity plot, (b) Mass spectrum at temperature = 400℃.

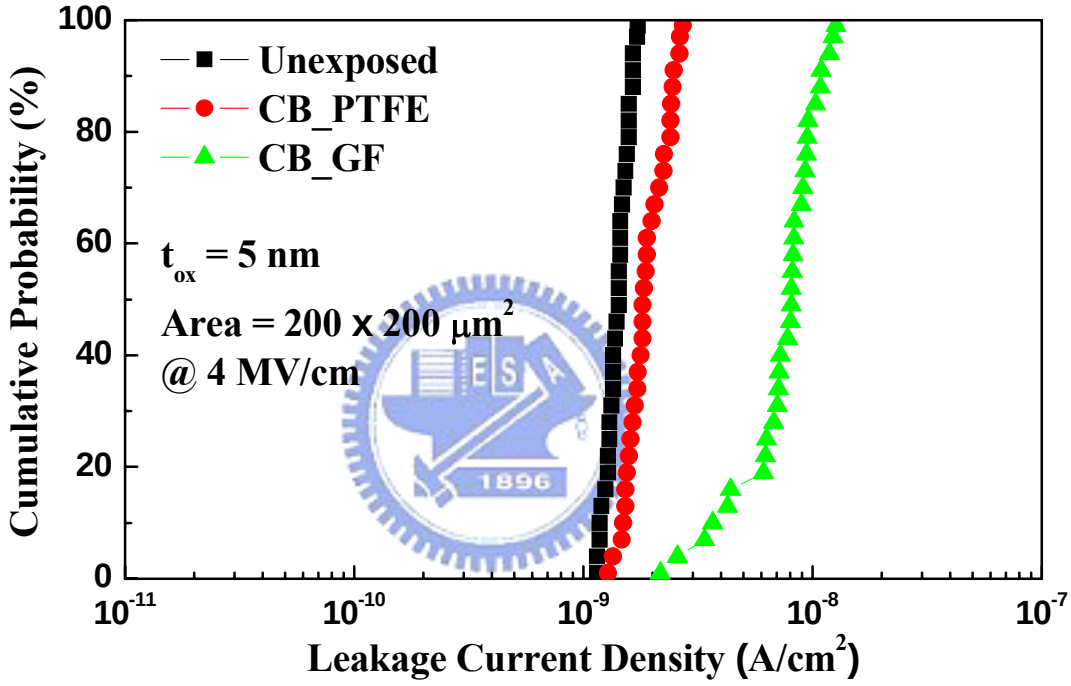


Fig. 3-13. The leakage current density distribution of MOS capacitors under different exposure environments.

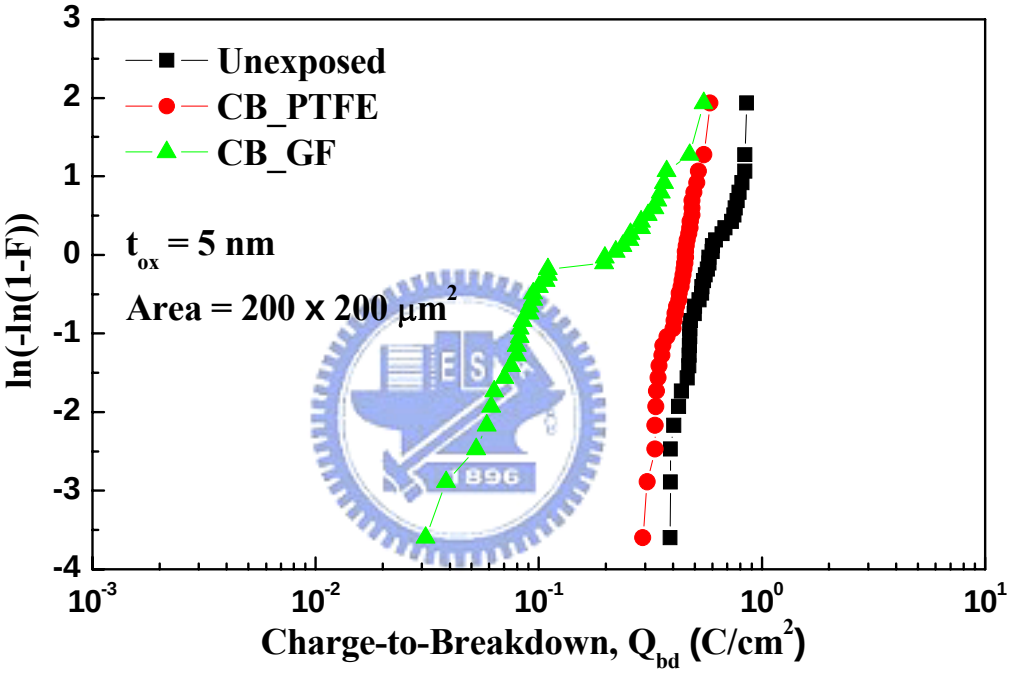


Fig. 3-14. Weibull plots of charge-to-breakdown (Q_{bd}) characteristics of MOS capacitors under different exposure environments.

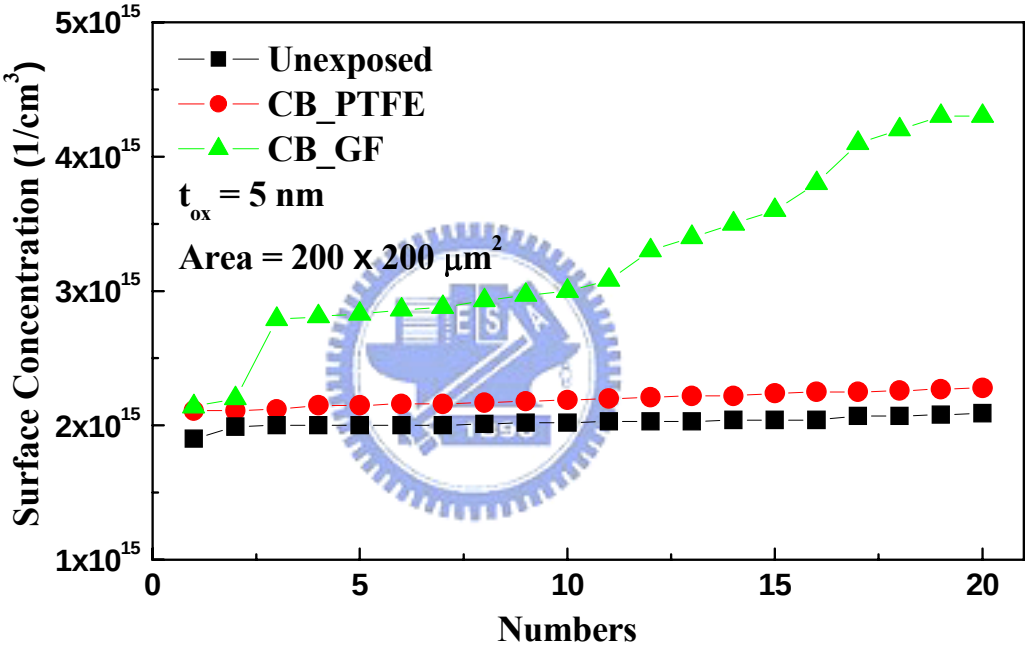


Fig. 3-15. Silicon surface doping concentration of MOS capacitors under different exposure environments.

CHAPTER 4

Development of the Nickel Silicide Process

4.1 INTRODUCTION

In ULSI regime, the dimension of the MOSFET device must scale down to the nanometer generation to fabricate high performance device characteristics. For the MOSFET device, the fabrication of source/drain (S/D) junction is an important process. With the scaling down of devices, the S/D junction depth must reduce to mitigate the punch-through phenomenon or other short-channel effects. The improvement of devices performance by the shrinking of devices size resulted in some problems. For example, when the device dimension is scaled down by a factor of k, the junction sheet resistance R_S (= ρ/t) is direct proportion to k, where ρ and t are the resistivity and the thickness of junction, respectively. For the contact resistance R_C (=ρ/A), it is direct proportion to k^2 because the contact area (A) is reduced by a factor of k^2. The increase of R_S and R_C will increase the resistance of junction area, causing the RC time delay. Since the reduction of junction area, junction depth and contact-hole size in an unsilicided device results in a high resistance junction area, it will degrade the transistor current drivability and increase the RC time delay, making the device fail to work properly. In order to reduce the parasitic resistance of the MOSFET device, the low resistivity silicide form on the junction region is required. Besides, the use of self-aligned silicide (Salicide) process can selectively form silicide on the gate and the source/drain region without additional mask, which simultaneously reduced the gate and junction resistance.

It is well known that the resistivity of commonly used titanium silicide ($TiSi_2$) increases as the gate linewidth reduces to submicron dimension. For the wide lines, the $TiSi_2$ is mainly

the low resistivity C54 phase (10~15μΩ-cm), while for the narrow lines, the phase transformation process is limited and the high resistivity C49 phase (60~80μΩ-cm) is dominant. Besides, the high temperature (800~950℃) silicidation process is needed to make the C54 phase [30], [31]. However, as the thickness of Ti decreases, $TiSi_2$ agglomeration has been observed. This results in the high sheet resistance when thin $TiSi_2$ layers are used for the shallow junctions. For 0.18μm process or below, cobalt silicide ($CoSi_2$) is more preferred due to its lower linewidth dependence of sheet resistance. $CoSi_2$, however, consumes more silicon volume than $TiSi_2$ and it will limit the scaling of junction depth. Compared to $CoSi_2$, NiSi has the advantages: (1) less silicon consumption for the same sheet resistance, (2) low contact resistivity, (3) low process temperature and wide process window (400~600℃), (4) low stress, and (4) no creep-up phenomenon. Table 4-1 shows the silicon consumption during silidation and the film stress for various silicides. According to the above mentioned, NiSi is a promising candidate silicide for next generation devices.

In this chapter, we investigated the process window of NiSi on different silicon substrates and the relation between sheet resistance and linewidth. In addition, we also investigated their thermal stability after 2nd rapid thermal annealing (RTA).

4.2 EXPERIMENTS

4.2.1 Fabrication Process of Nickel Silicide

To find out the optimum conditions of nickel silicide process, we conducted the experiments including different silicon substrate, rapid thermal annealing (RTA) temperature and as-deposited nickel thickness. As shown in Fig. 4-1, four different silicon substrates were prepared, including the P-type (100) single crystal silicon wafer (c-Si) with the bulk resistivity of 15-25 Ω-cm, the columnar poly silicon (poly-Si), the amorphous silicon (a-Si) and the non-columnar poly silicon (apoly-Si), which was formed by the 850℃, 30 minutes annealing

of the amorphous silicon in furnace. The poly-Si and a-Si samples were deposited by Low-Pressure Chemical-Vapor-Deposition (LP-CVD) at 620℃ and 550℃ on the 350Å thermally grown SiO_2 formed on silicon wafers, respectively.

After RCA cleaning, four different thickness nickel films (100Å, 150Å, 200Å, and 200Å with Ti 100Å capping) were deposited on c-Si, poly-Si, a-Si and a-poly Si substrates by sputter, respectively. The nickel silicide was formed by RTA at different temperatures (400℃~750℃, 50℃/step) for 30 seconds in N_2 ambient and then the residual nickel was removed in the SPM solution (H_2SO_4: H_2O_2=3:1). The sheet resistances of nickel silicide were measured by four-point probe.

In order to test the thermal stability of nickel silicide, the second RTA at the temperatures ranging from 500℃ to 800℃ for 30 seconds was performed. Then the sheet resistances of nickel silicide after second annealing were also measured.

4.2.2 Fabrication of Nickel Silicide with Different Linewidth

In order to investigate the linewidth effects of nickel silicide, poly-line with different linewidth were patterned and then the nickel silicide was formed on the poly-line to measure the sheet resistance. The fabrication process flow was illustrated in Fig. 4-2. After 5500Å wet oxide growth, three different Silicon films, including poly-Si, a-Si, and apoly-Si were prepared. These films were implanted by phosphorus at energy of 50keV to a dose of 3×10^{15} cm^{-2}, and followed by 1000℃, 30s RTA in N_2 ambient. After poly-line patterning, the poly-Si, a-Si, and apoly-Si films were etched by TCP poly-etcher and the photoresist was removed by fusion ozone and SPM solution. Then 5000Å oxide was deposited by LP-CVD at 700℃ after RCA cleaning. The oxide layer was subsequently etched by TEL5000 oxide-etcher to form the spacer. After RCA cleaning, a 200Å nickel film was deposited on the poly-line by sputter. After the RTA annealing (400℃~600℃, 30s), the nickel silicide was formed and then the

residual nickel was removed in SPM solution (H_2SO_4: H_2O_2=3:1). After the silicidation, 5000Å oxide passivation layer was deposited by PE-CVD. Following the contact hole pattering and etching, four metal layer (Ti/TiN/Al-Si-Cu/TiN = 400Å/1000Å/9000Å/400Å) was deposited. After pattering and etching the metal pad, the sheet resistances of the poly-lines were measured by HP4156C semiconductor parameter analyzer.

4.3 RESULTS AND DISCUSSION

4.3.1 Nickel Silicide Formed on c-Si, poly-Si, a-Si and apoly-Si

Table 4-3 shows the sheet resistance of as-deposited nickel film on different substrates. We found that the thicker as-deposited nickel film showed lower sheet resistance, and the nickel film with titanium film capping showed the lowest sheet resistance. In Fig. 4-3, the sheet resistances of NiSi formed on c-Si with four different Ni thicknesses (100Å, 150Å, 200Å and 200Å with Ti 100Å capping) were 10, 5.4, 4 and 4.2Ω/□ in average, respectively, after the 500℃ RTA for 30s. In the case of 200Å thick Ni, the sheet resistance of NiSi is stable between 400℃ and 700℃. As the thickness of Ni decreases to 150Å and 100Å, the sheet resistances obviously increase after 650℃ and 600℃ RTA, respectively. The high sheet resistance was due to the transition of the low resistivity NiSi phase to the high resistivity $NiSi_2$ phase.

As shown in Fig. 4-4, NiSi formed on columnar poly-Si showed less thermal stability. The sheet resistances of NiSi formed on poly-Si with four different Ni film thicknesses (100Å, 150Å, 200Å and 200Å with Ti 100Å capping) were 12.5, 6.5, 4.9 and 5.1Ω/□, respectively, after 500℃ RTA for 30s. The slightly higher sheet resistance may be due to the more grain-like microstructure of NiSi layer formed on poly-Si. For 100Å and 150Å thick Ni on poly-Si, the sheet resistance of NiSi increased high after above 600℃ RTA and the figure doesn't show out. Besides the formation of $NiSi_2$, the high increase in the resistivity may also

due to the growth of the poly-Si grains into the NiSi layer [32], [33].

In the case of NiSi formed on a-Si, as shown in Fig. 4-5, the sheet resistance is higher. For 100Å thick Ni, the sheet resistance is around 12.8Ω/□ after 400℃ RTA for 30s. As the RTA temperature increases to 500℃, the sheet resistance increases to 76Ω/□. If the temperature continuously increased to 600℃, the sheet resistance decreased to around 54.7Ω/□ on the contrary. Finally, the sheet resistance increases again after above 750℃ RTA. For the thicker Ni, this phenomenon is less obvious. Due to the higher diffusivity in a-Si, Ni may react with the entire a-Si to form various silicide phases even at the RTA temperature as low as 400℃ [34]. The $NiSi_2$ can promote the nucleation and growth of poly-Si grains and even cause layer reversal. $NiSi_2$ has been recently used as metal induced lateral crystallization (MILC) technology to obtain high mobility poly-Si TFT.

In order to simulate the silicidation on the gate of MOSFET, we prepared the apoly-Si substrate. As shown in Fig. 4-6, the sheet resistance of NiSi is stable between 450℃ and 650℃. Besides, these values are similar to those on poly-Si rather than on a-Si. This is due to the Si grain growth after annealing at 850℃ for 30 minutes in furnace. For 100Å and 150Å thick Ni on apoly-Si, the sheet resistances are lower after 400℃ RTA. The two apoly-Si substrates were processed with additional 1000℃ RTA for 30s after the annealing at 850℃ for 30 minutes in furnace. This process may induce the grain growth.

For MOSFET process, the process window of NiSi formed by 200Å Ni on c-Si and a-poly Si is between 400℃ and 650℃. And the thinner the Ni film thickness is, the narrower the process window. Then we also found that NiSi formed with Ti capping didn't show the lower sheet resistance.

4.3.2 Surface Morphology of Ni Silicide

As mentioned above, we know the variation of NiSi sheet resistance at different RTA temperature is mainly due to the silicide phase transition. But for NiSi on poly-Si, a-Si, and apoly-Si, the reason could be more complicated. Besides the phase transition, we must consider the effects of RTA temperature to the different substrates. In this section, the surface morphology of nickel silicide formed with 200Å thick Ni at different temperature was observed. Figure 4-7 shows the top view SEM micrographs of nickel silicide on poly-Si at different RTA temperature. As shown in Fig. 4-7(a), the surface morphology of NiSi at low RTA temperatures was more uniform grain-like microstructure than the others. Fig. 4-7(b) shows few dark spots or agglomeration occur in the first time when the RTA temperature was 550℃. As the RTA temperature increases, the dark spots seem to coalesce into larger ones. When the RTA temperature increases to 700℃, as shown in Fig. 4-7(e), the white region becomes fewer. Besides agglomeration, the transition of the low resistivity NiSi phase to the high resistivity $NiSi_2$ phase occurs. For the 750℃, the excess Ni moves via the grain boundary diffusion to form $NiSi_2$ [35]. As compared to Fig. 4-4, the sheet resistance of Ni silicide on poly-Si increases from 600℃. So we know the agglomeration of NiSi film and the phase transition of NiSi to $NiSi_2$ result in high sheet resistance.

Figure 4-8 shows the top view SEM micrographs of Ni silicide on a-Si at different RTA temperature. In order to observe the variation of the surface morphology of nickel silicide clearly, we magnified the ratio of SEM to 50k. We found the less dark spots than that on poly-Si, as shown in Fig. 4-8(a) to (f). As compared to Fig. 4-5, the sheet resistance of Ni-silicide on a-Si increases at 500℃ and becomes stable till 750℃. For 200Å thick Ni, we couldn't separate them from the surface morphology of nickel silicide.

Figure 4-9 shows the top view SEM micrographs of Ni silicide on apoly-Si at different

RTA temperature. The surface morphology of nickel silicide is different from that on poly-Si and a-Si. Fig. 4-9(a) to (b) show the uniform surface morphology and Fig. 4-9(c) shows few dark spots in the first time. From Fig. 4-9(d) to (f), the agglomeration of Ni silicide becomes more serious. Beside the agglomeration, the non-uniform microstructure of Ni silicide may also result from the transition of the low resistivity NiSi phase to the high resistivity $NiSi_2$ phase. As compared to Fig. 4-6, the sheet resistance of Ni silicide on apoly-Si increases from 650℃. So we know the agglomeration of NiSi film and the phase transition of NiSi to $NiSi_2$ result in high sheet resistance.

4.3.3 Measurement of NiSi Sheet Resistance with Different Linewidth

Figure 4-10 illustrates the bridge resistor structure. In the mask layout, the line length (L) is 500μm and the linewidth (W) are 0.5μm, 0.6μm, 0.7μm, 0.8μm, 0.9μm and 1.0μm, respectively. According to the relation of sheet resistance and measurement resistance which is described below, we can calculate the sheet resistance of NiSi with different linewidth.

$$Rs = \left(\frac{V_{12}}{I_{12}}\right) \times \left(\frac{W}{L}\right)$$

In this section, we tested the process window of NiSi RTA temperature ranging from 400℃ to 600℃ for 30s.

Figure 4-11 shows the measured sheet resistance of different linewidth NiSi formed on poly-Si. It shows the low sheet resistance after 400℃, 500℃ and 550℃ RTA. For 500℃ RTA, the sheet resistances range from 4.4 to 4.7Ω/□. Compared to the planer sheet resistance measured by four point probe, these values are slightly smaller than 4.9Ω/□. This is mainly due to the edge effects of NiSi formation. It means thicker NiSi formed at the edge of different linewidth. Edge effects would be more obvious with the narrower linewidth. In

addition, the poly-Si substrates were implanted by P at energy of 50keV to a dose of 3×10^{15} cm^{-2}, and followed by RTA at 1000℃ for 30s in N_2 ambient. Even so, the effects of implantation and dopant activation on poly-Si can be ignored as compared to the low sheet resistance of NiSi. For 600℃ RTA, it shows the increase of sheet resistance with the decrease of linwidth.

Figure 4-12 shows the measured sheet resistance of different linewidth NiSi formed on a-Si. It shows the lower resistances after 400℃, 500℃, and 550℃ RTA, which is similar to Fig. 4-11. For 500℃ RTA, the sheet resistances range from 5 to 6.3Ω/□. Compared to the planer sheet resistance measured by four point probe, these values are smaller than 10.7Ω/□. Besides the edge effects of Ni-silicide formation, the effect of dopant activation at 1000℃ for 30s RTA must be considered. The a-Si grain would enlarge after high temperature annealing and becomes similar to apoly-Si. So the growth of a-Si grain results in the obviously lower sheet resistance. For 600℃ RTA, it shows the increase of sheet resistance with the decrease of linwidth.

Figure 4-13 shows the measured sheet resistance of different linewidth NiSi formed on apoly-Si. It shows the lower resistances after 400°C, 500°C, and 550°C RTA. For 500℃ RTA, the sheet resistances range from 4.5 to 5.3Ω/□. Compared to the planer sheet resistance measured by four point probe, these values are slightly smaller than 5.2Ω/□ except for the 0.5μm one. The effect of dopant activation at 1000℃ for 30s RTA on apoly-Si is not as obvious as on a-Si. So the slightly lower sheet resistance is due to the edge effects of NiSi formation. For 600℃ RTA, it shows the increase of sheet resistance with the decrease of linwidth.

According to the discussion above, the linewidth effects would reduce the NiSi process window on poly-Si, a-Si, and apoly-Si to the range of 400℃ to 550℃. As the RTA

temperature increases above 600°C, the sheet resistance becomes much higher and unstable.

4.3.4 Thermal Stability of NiSi

In the MOSFET fabrication, some thermal processes were used after the silicidation process. Such as the PE-TEOS deposition, low K dielectric curing and aluminum sintering, etc. These process temperatures are usually below 800℃ to prevent the dopant redistribution. In this section, the thermal stability of NiSi was tested by the 2nd RTA at the temperatures ranging from 500℃ to 800℃ for 30s.

Figure 4-14 shows the sheet resistance of NiSi formed with 200Å thick Ni at different RTA-1 temperature. The samples with the RTA-1 temperature ranging from 400℃ to 600℃ were used to do the thermal stability tests.

For NiSi on c-Si, as shown in Fig. 4-15, the sheet resistances of NiSi formed at different RTA-1 temperature are stable after below 700℃ RTA-2 for 30s. The high temperature of 800℃ results in the relatively high sheet resistance with the transition of lower resistivity NiSi phase to higher $NiSi_2$ phase. Figure 4-16 shows the sheet resistance of NiSi on poly-Si at different RTA-2 temperature for 30s. We found the sheet resistances of NiSi formed at different RTA-1 temperature are still low after below 600℃ RTA-2, but become very high after above 700℃ RTA-2. Figure 4-17 shows the sheet resistance of NiSi on a-Si at different RTA-2 temperature for 30s. They are stable even after 800℃ RTA-2. Figure 4-18 shows the sheet resistance of NiSi on apoly-Si at different RTA-2 temperature for 30s. We could see the sheet resistances increase at 700℃ RTA-2 and become high at 800℃ RTA-2. After the thermal stability testing, Ni silicide on a-Si owns the best stability. But for NiSi on c-Si, Ni will continuous diffuse and increase the sheer resistance. Compared to the columnar poly silicon, the non-columnar poly silicon is more stable in the same thermal treatment.

4.4 SUMMARY

In this chapter, we investigated the sheet resistance behavior of Ni silicide on different substrates. We found the planer NiSi formed with 200Å thick Ni is stable and shows low sheet resistance between 400℃ and 650℃ RTA-1, and still stable after 700℃ RTA-2 for 30s on c-Si and apoly-Si. In the same experiment, the planer NiSi on poly-Si shows low sheet resistance below 600℃ RTA.

After the SEM micrographs observation, we found the different surface morphology of Ni silicide on poly-Si, a-Si, and apoly-Si. At the lower RTA temperature, the surface is more uniform. As the dark spots or agglomeration appear, the sheet resistance begins to increase. At the higher RTA temperature, the surface of Ni silicide on poly-Si and apoly-Si seem micro-crack or agglomeration which results in the higher sheet resistance.

As the research of the linewidth effects of NiSi sheet resistance on poly-Si, a-Si, and apoly-Si, we found the appearance of dark spots or agglomeration would affect the sheet resistance of Ni silicide seriously. For 600℃ RTA on poly-Si and apoly-Si, the sheet resistances of Ni silicide increase. Even so, it is more obvious with the narrower linewidth. We notice that behavior of NiSi sheet resistance at 600℃ RTA on a-Si is similar to that on apoly-Si. This is due to the effect of dopant activation at 1000℃ for 30s RTA. Due to the linewidth effects, the process window of NiSi RTA temperature is ranging from 400℃ to 550℃.

In the last section of this chapter, we tested thermal stability of Ni silicide by the 2nd RTA at the temperatures ranging from 500℃ to 800℃ for 30s. Ni silicide on a-Si owns the best stability. But for NiSi on c-Si, Ni will continuously diffuse and cause the sheet resistance to increase. Compared to the columnar poly silicon (poly-Si), the non-columnar poly silicon (apoly-Si) is more stable in the same thermal treatment.

TABLE 4-1
Silicon Consumption and Film Stress for Various Silicides

Silicide	Silicon Consumption	Silicidation Temperature(^oC)	Film Stress (dyn/cm^2)
NiSi	$0.82 \times T_{NiSi}$	350 ~ 750	6×10^9
$NiSi_2$	$1.02 \times T_{NiSi2}$	750 ~ 850	-
$TiSi_2$	$0.90 \times T_{TiSi2}$	800 ~ 950	1.5×10^{10}
CoSi	$0.91 \times T_{CoSi}$	375 ~ 500	-
$CoSi_2$	$1.04 \times T_{CoSi2}$	550 ~ 900	1.2×10^{10}

TABLE 4-2
Sheet Resistance of As-deposited Nickel on Different Substrates

Substrate	As-deposited nickel thickness			
	100Å	150Å	200Å	200Å/Ti cap100Å
c-Si	25.9	13.8	8.9	8.2
poly-Si	36.2	16.5	11.8	10.3
a-Si	30.4	14.3	10.3	9.3
apoly-Si	33.4	15.8	9.8	7.3

unit: Ω/□

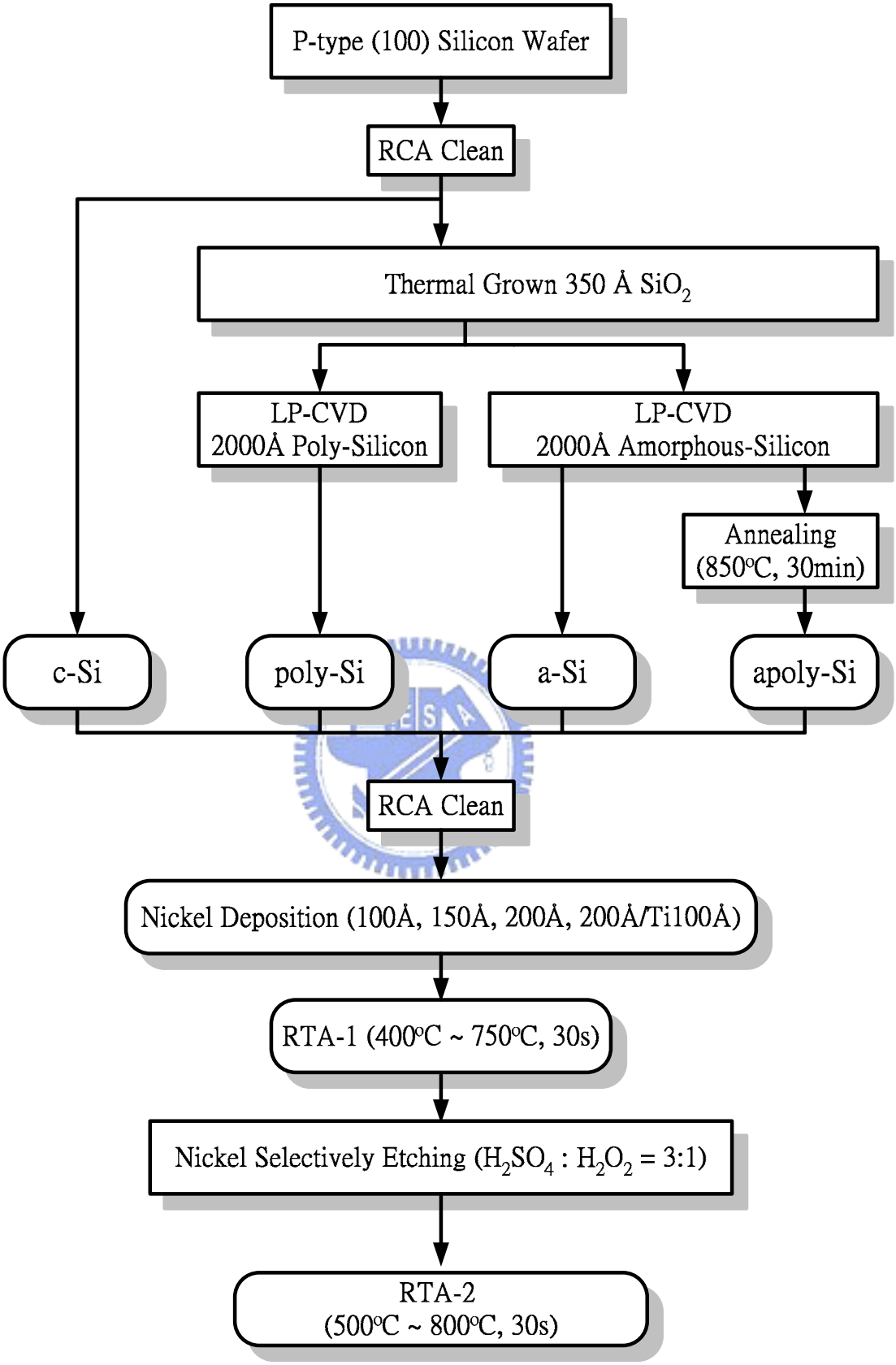
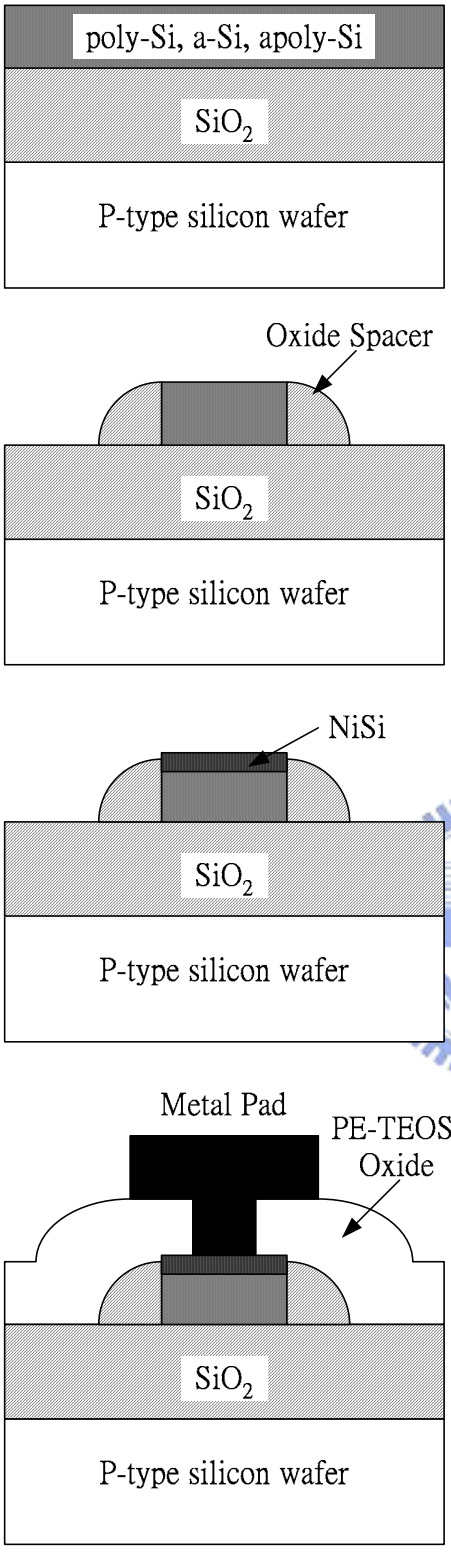


Fig. 4-1. Fabrication process flow of the of nickel silicide.



1. RCA clean
2. Wet oxide 5500Å
3. LP-CVD 2000Å (poly-Si, a-Si, apoly-Si)
4. Implant (Phosphorus 50 keV, 3E15)
5. RTA (1000°C, 30s)

6. Poly-line pattern define
7. Etch poly-Si
8. P. R. removal and RCA clean
9. LP-CVD oxide 5000Å
10. Etch oxide 5000Å

11. RCA clean
12. Deposit nickel 200Å
13. RTA (400°C ~ 600°C, 30s)
14. Nickel selectively etch (H_2SO_4+H_2O_2)

15. PE-CVD oxide 5000Å
16. Contact hole pattern define
17. Etch oxide 5000Å
18. Metal deposition (Ti/TiN/Al-Si-Cu/TiN)
19. Metal pad define
20. Etch Ti/TiN/Al-Si-Cu/TiN

Fig. 4-2. Fabrication process flow of poly-line with nickel silicide.

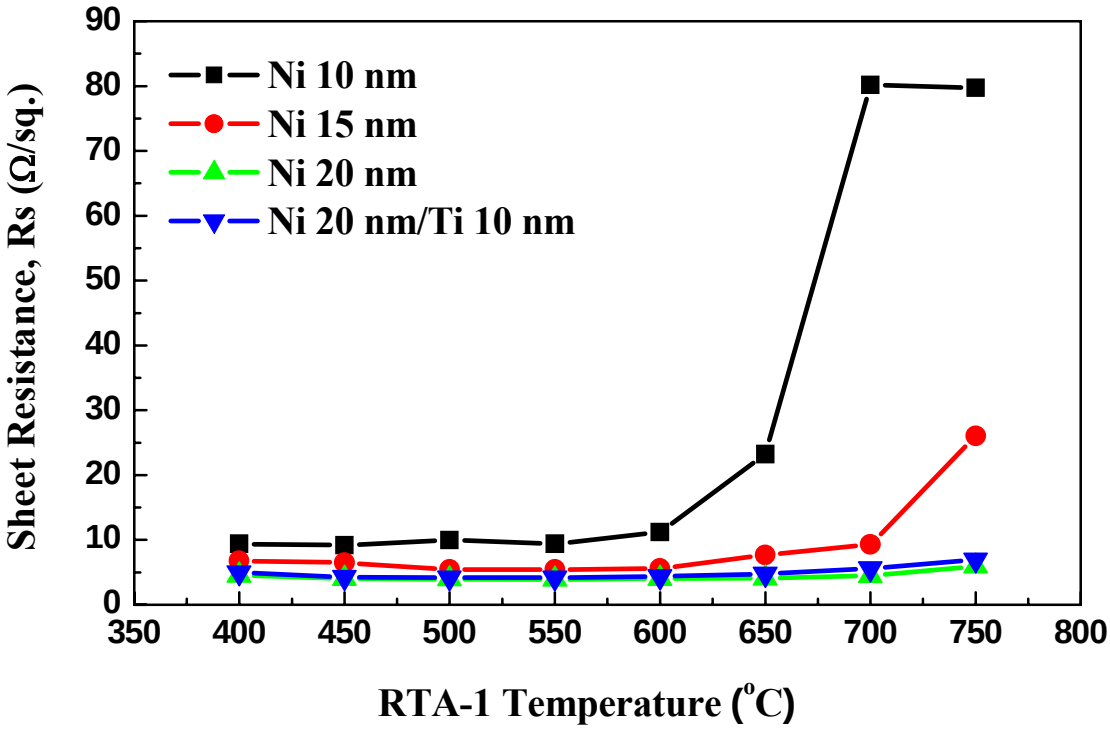


Fig. 4-3. Sheet resistance of NiSi formed on c-Si.

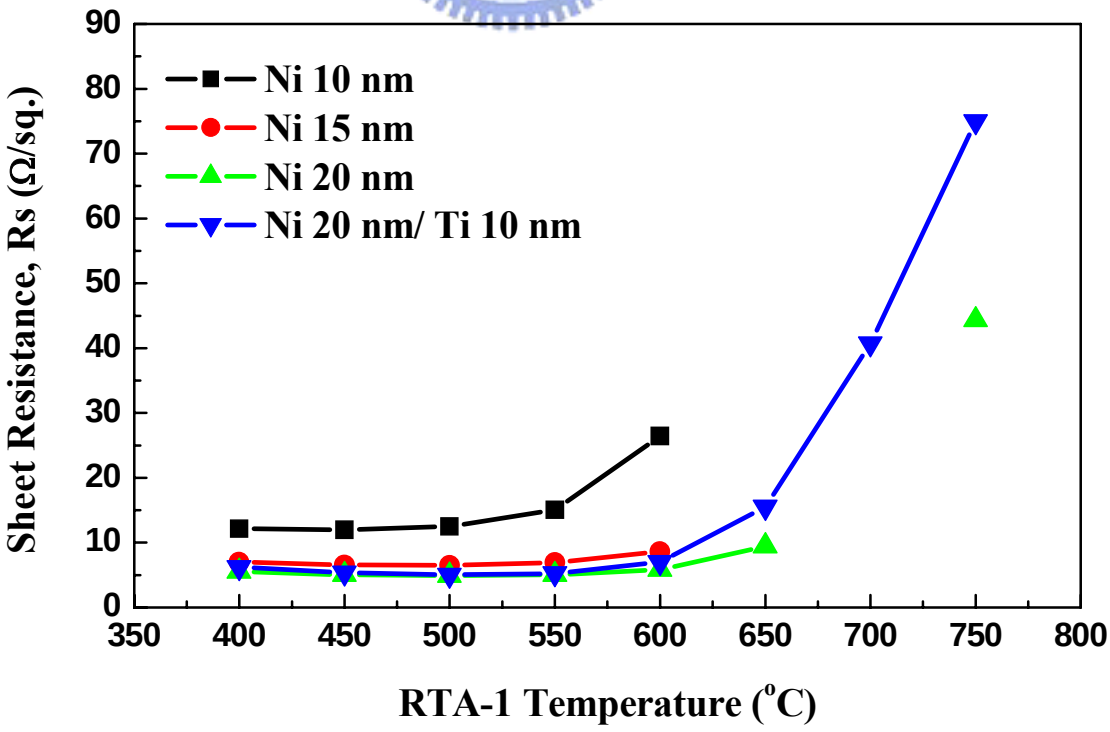


Fig. 4-4. Sheet resistance of NiSi formed on poly-Si.

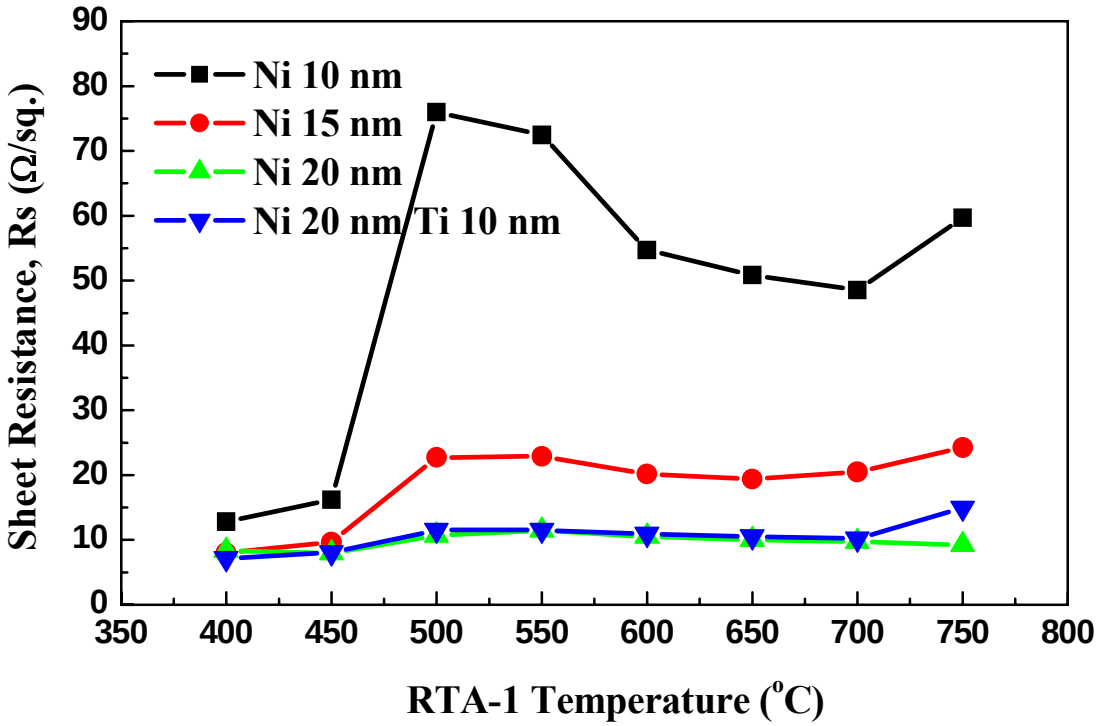


Fig. 4-5. Sheet resistance of NiSi formed on a-Si.

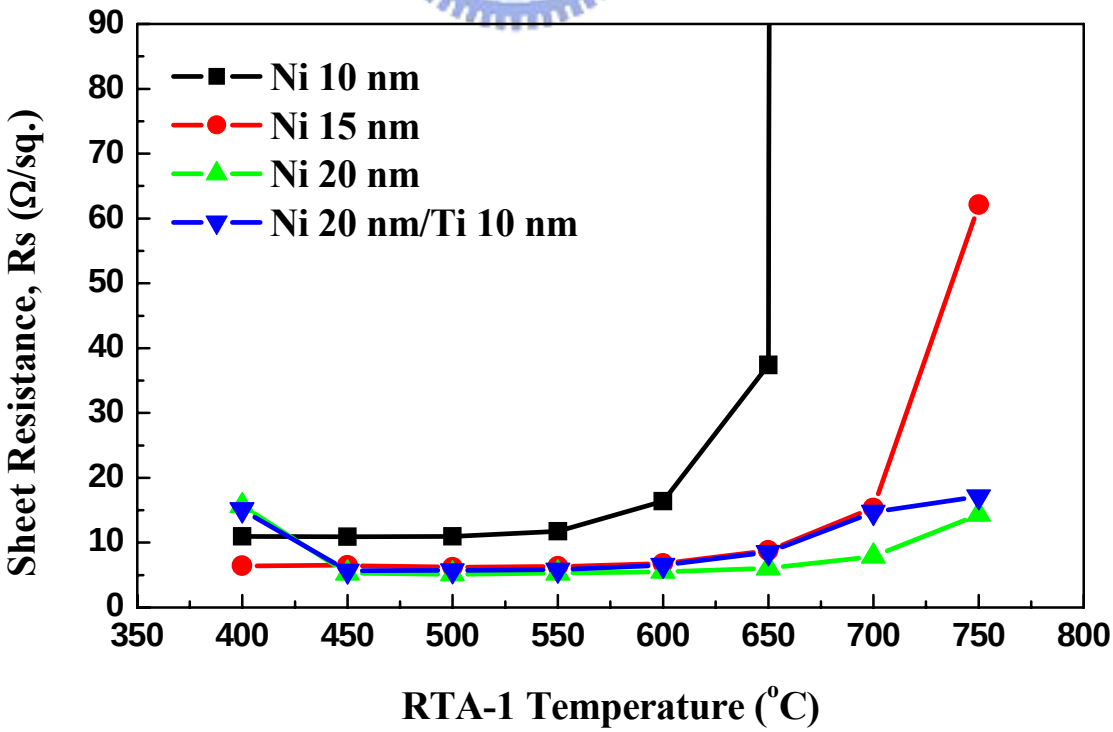
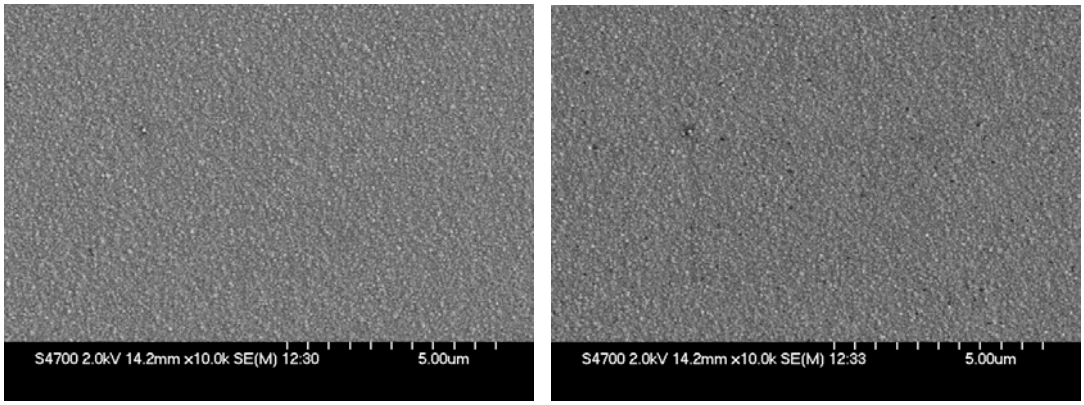
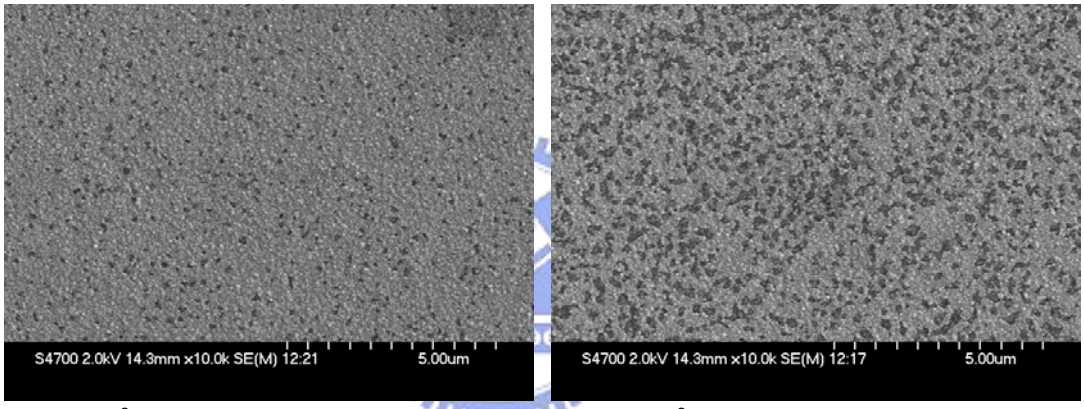


Fig. 4-6. Sheet resistance of NiSi formed on apoly-Si.

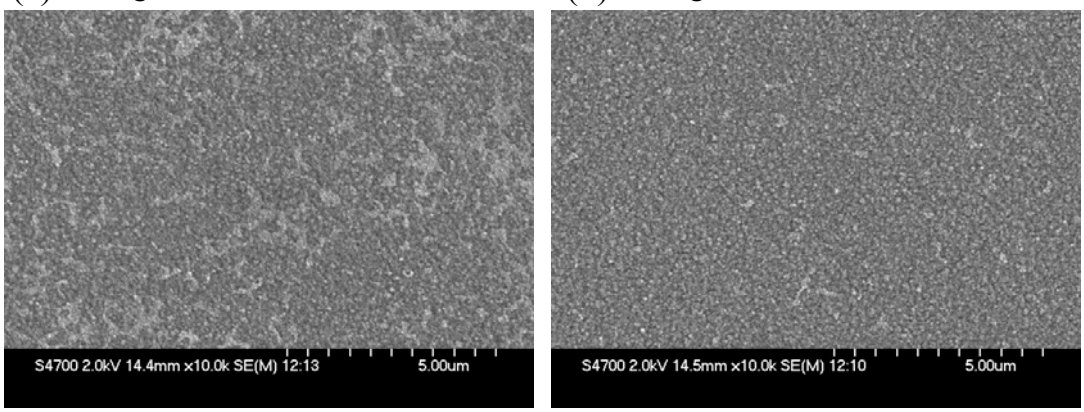


(a) 500℃

(b) 550℃

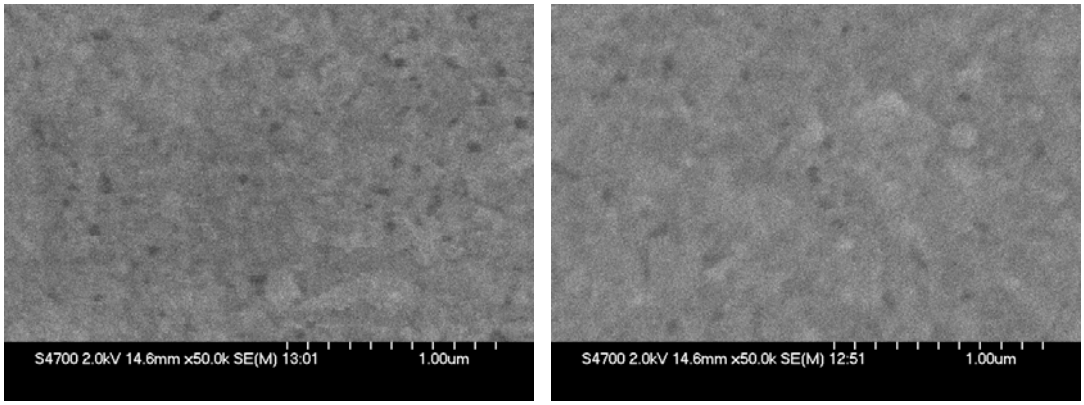


(c) 600℃ (d) 650℃

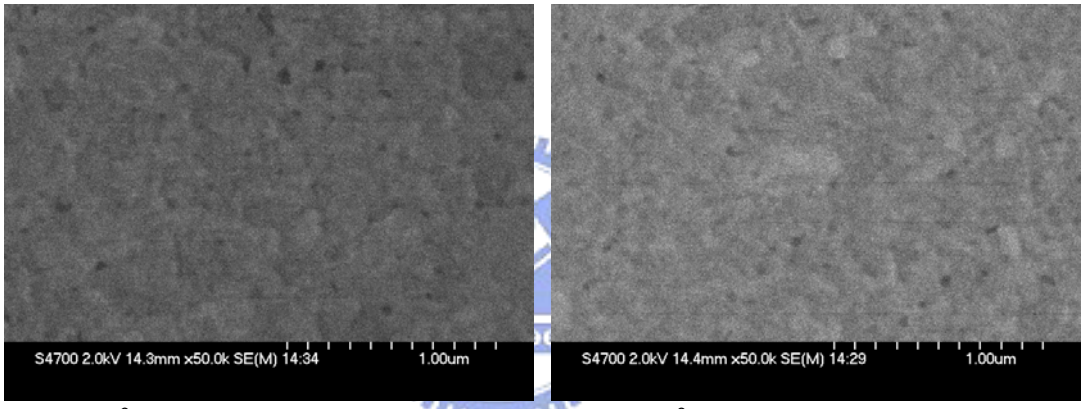


(e) 700℃ (f) 750℃

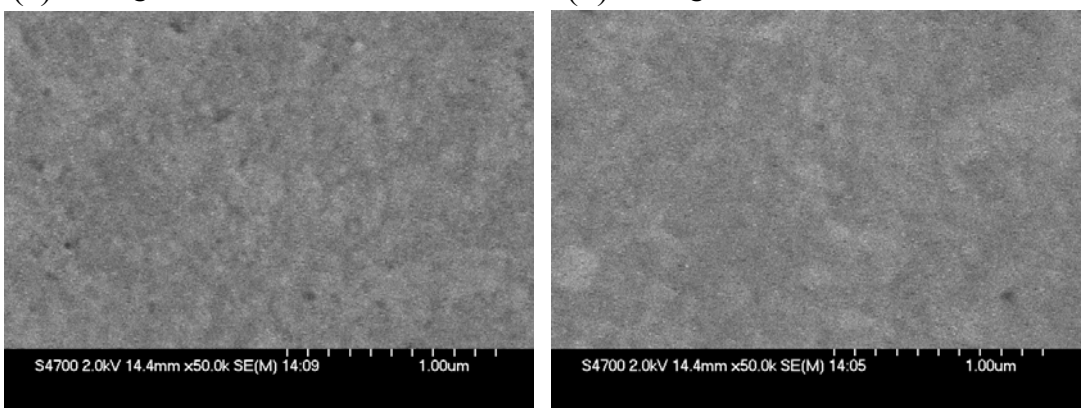
Fig. 4-7. Top view SEM micrographs of Ni-silicide on poly-Si at different RTA temperature.



(a) 500℃ (b) 550℃

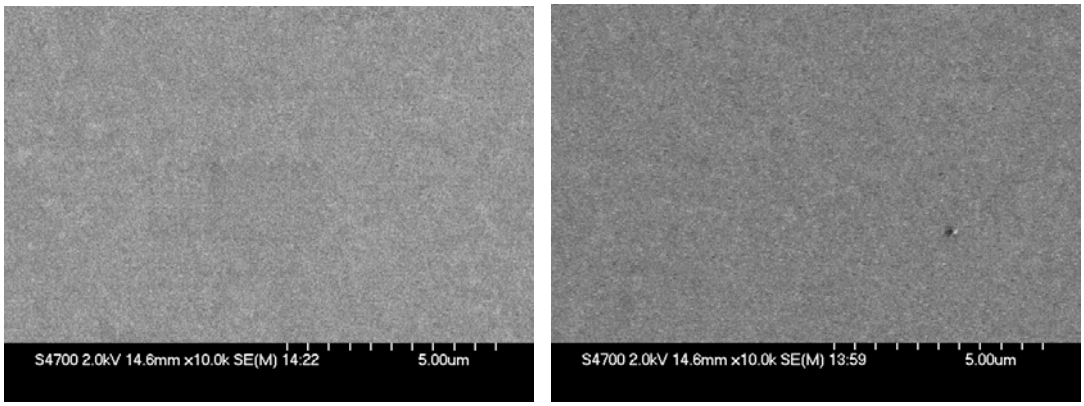


(c) 600℃ (d) 650℃

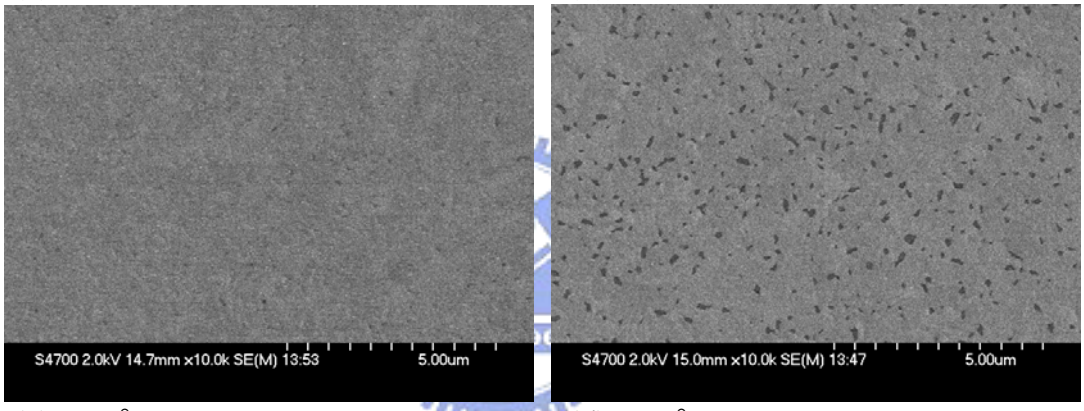


(e) 700℃ (f) 750℃

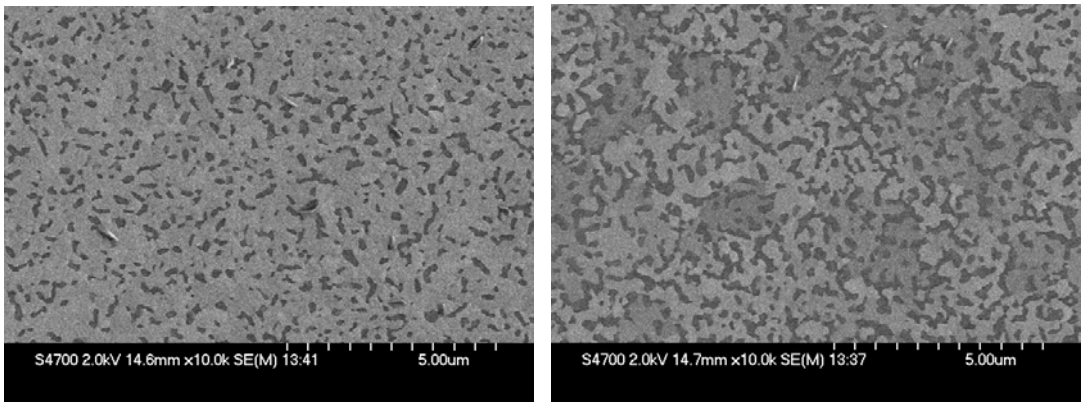
Fig. 4-8. Top view SEM micrographs of Ni-silicide on a-Si at different RTA temperature.



(a) 500℃ (b) 550℃



(c) 600℃ (d) 650℃



(e) 700℃ (f) 750℃

Fig. 4-9. Top view SEM micrographs of Ni-silicide on a-poly Si at different RTA temperature.

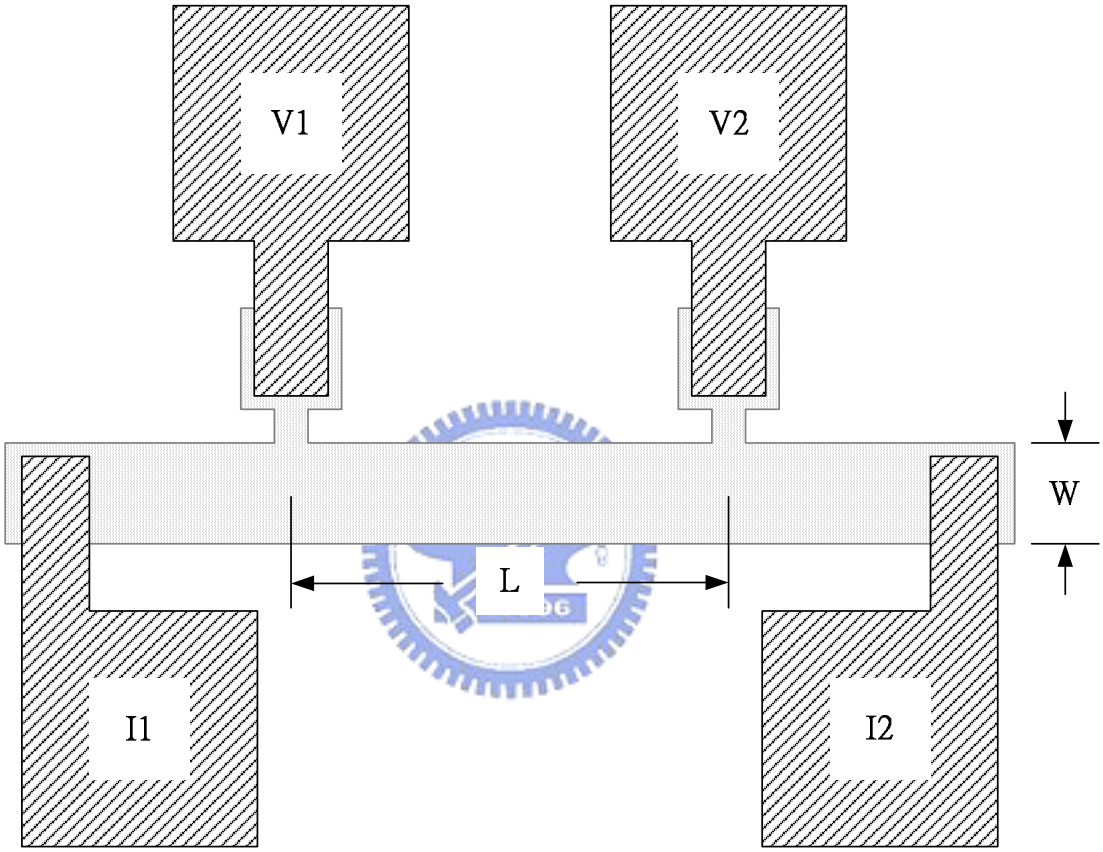


Fig. 4-10. Bridge resistor structure.

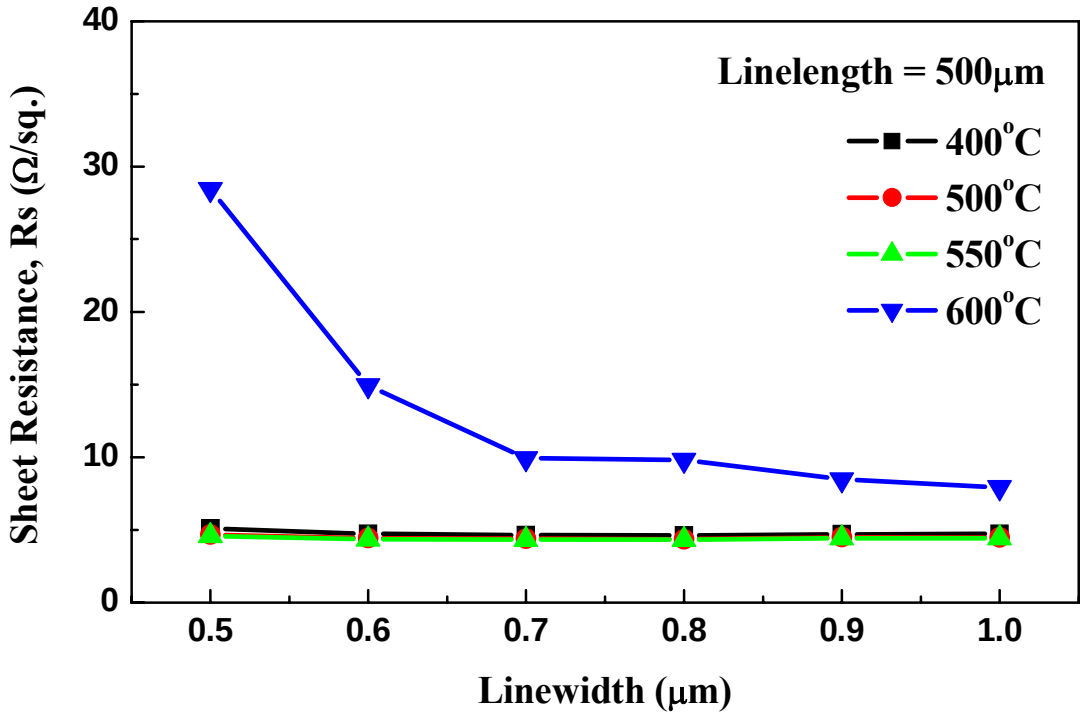


Fig. 4-11. Sheet resistance of different linewidth NiSi formed on poly-Si.

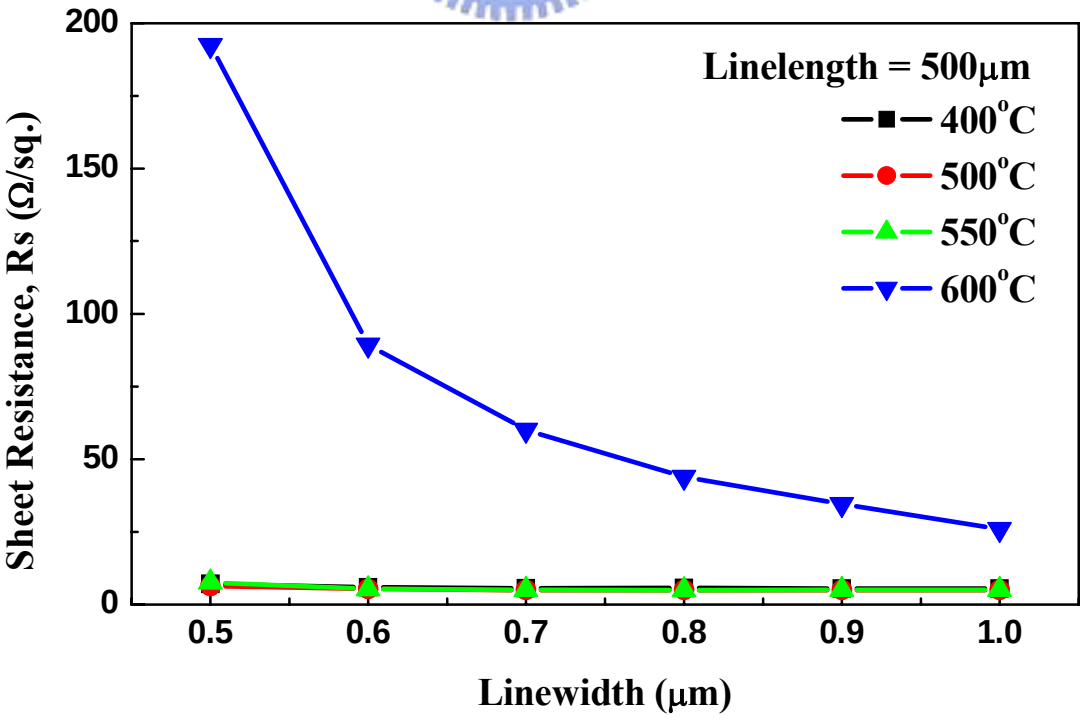


Fig. 4-12 Sheet resistance of different linewidth NiSi formed on a-Si.

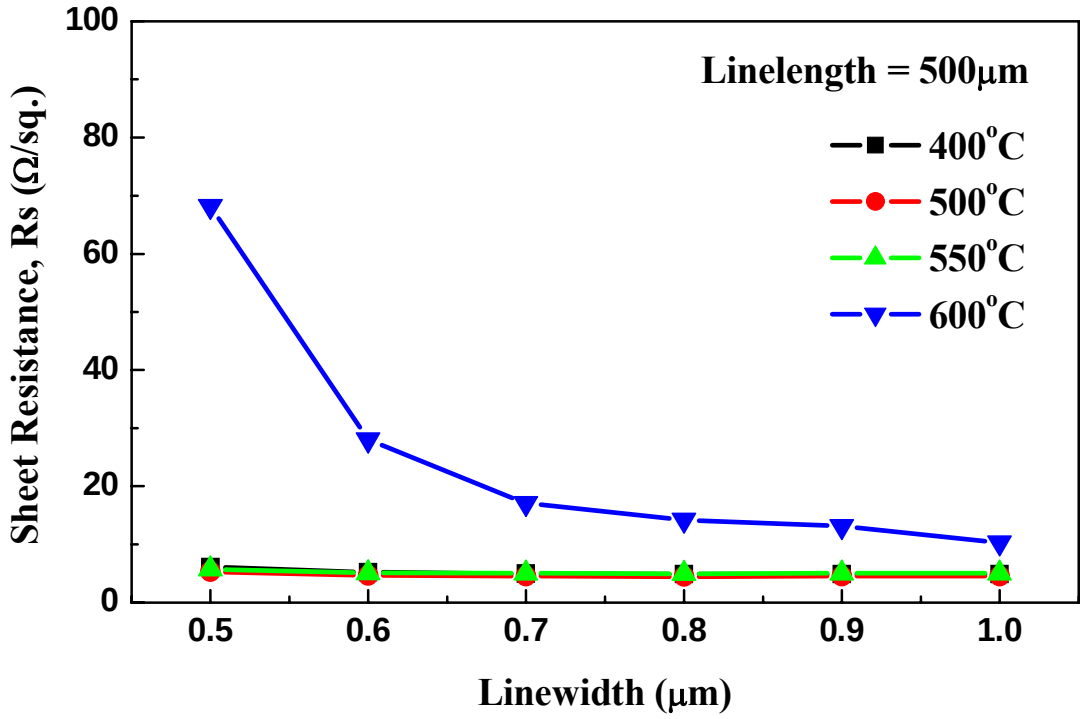


Fig. 4-13. Sheet resistance of different linewidth NiSi formed on apoly-Si.

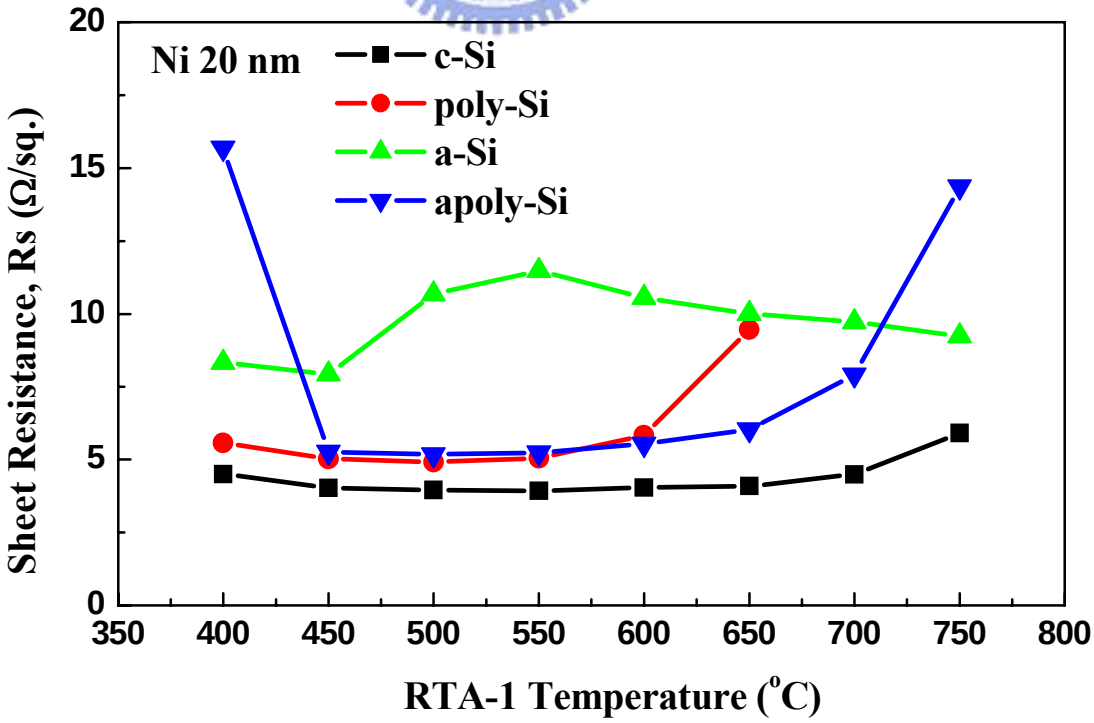


Fig. 4-14. Sheet resistance of NiSi formed with 200Å thick Ni.

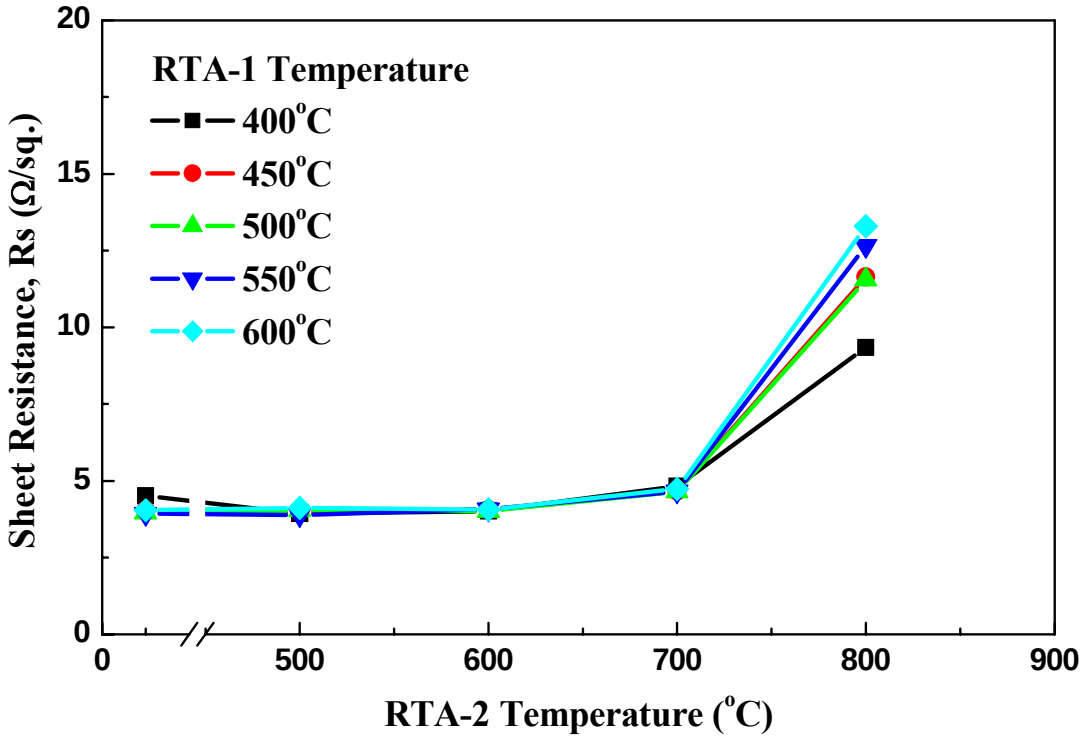


Fig. 4-15. Sheet resistance of NiSi on C-Si for RTA-2 annealing.

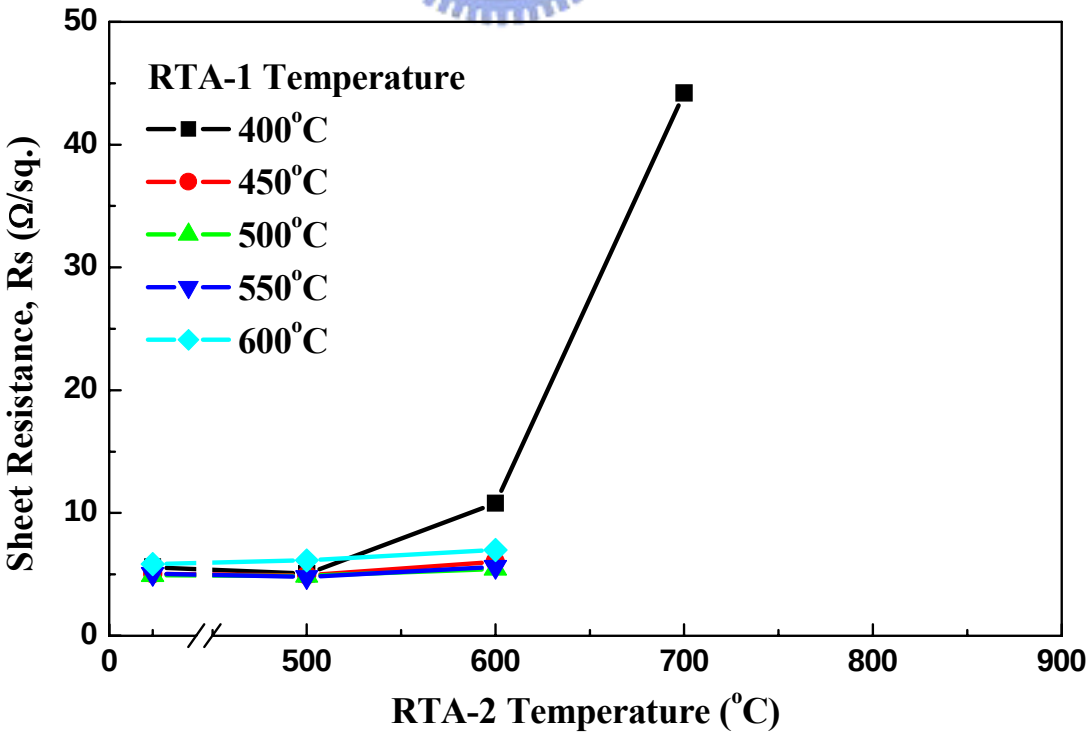


Fig. 4-16. Sheet resistance of NiSi on poly-Si for RTA-2 annealing.

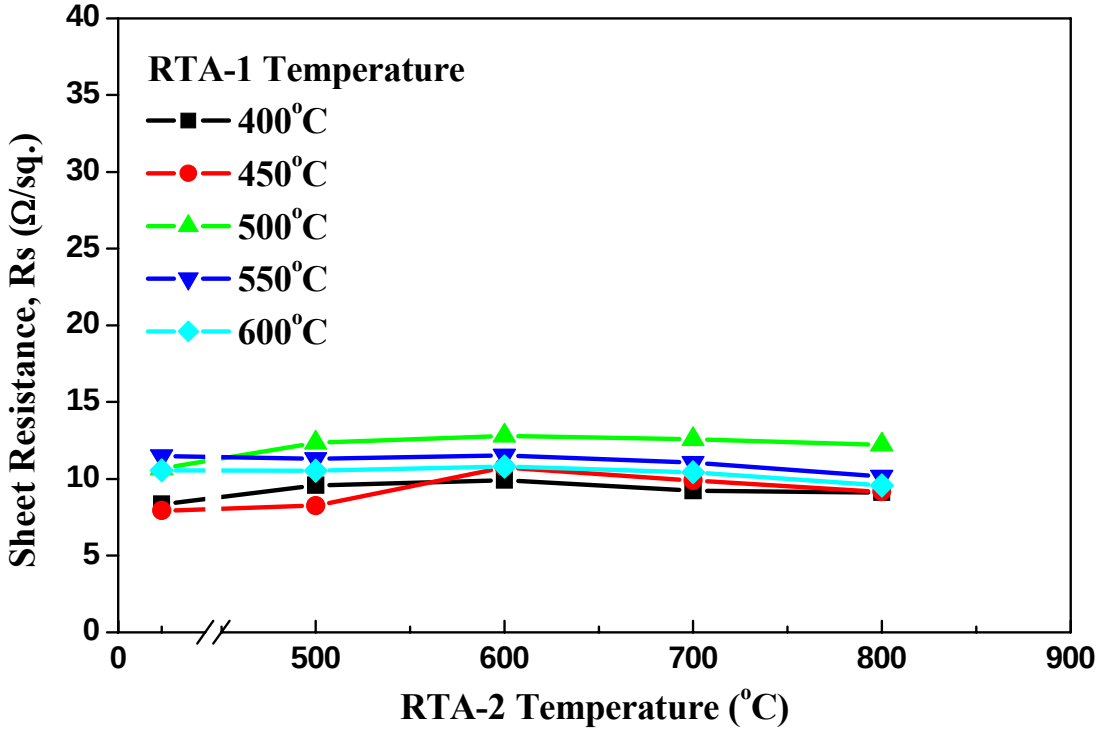


Fig. 4-17. Sheet resistance of NiSi on a-Si for RTA-2 annealing.

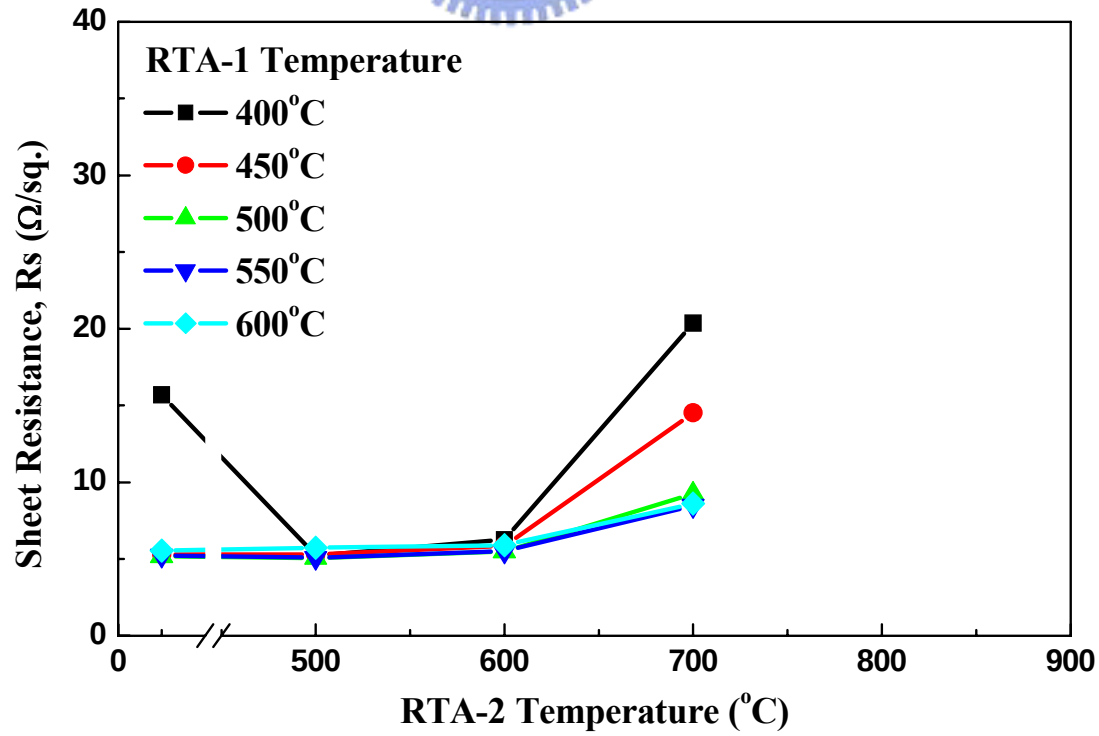


Fig. 4-18. Sheet resistance of NiSi on apoly-Si for RTA-2 annealing.

CHAPTER 5

Investigation of Plasma Damage-Free Selective Liquid-Phase Deposition to Contact-Hole Formation

5.1 INTRODUCTION

When device continuously scales down, the source/drain engineering becomes important and complex. With the MOSFET gate length scaling down to sub-100nm, the source/drain process almost reaches the limit. Many new technologies and materials have adopted to overcome these difficulties. Silicide is one key technology for solving these problems. As the gate length scales, the source/drain junction depth must shrink at the same time to decrease the short channel effects. Owing to the shallower junction depths than before, the resistance of junction becomes high. Silicide provides a new choice to lower the junction parasitic resistance. Titanium, cobalt and nickel are the popular materials to form silicide. Due to the line-width effect and thermal stability problems, titanium silicide is not suitable for future device manufacturing. Cobalt silicide is the most used material for sub-0.18μm technology. To reach the ultra-shallow junction, the high consumption of silicon to form cobalt silicide may be the weakness for further shrink device geometry. Nickel silicide is the promising material for future advanced device manufacturing because of its low silicon consumption, low resistivity and lack of line-width effect.

Reactive ion etching (RIE) is the most frequently used technology for contact-hole formation [36]. It is important to reduce the RIE damages on the surface of junction especially for ultra-shallow junction. It has been reported that the RIE process can induce some unwanted effects including radiation damage, surface amorphized layer and contaminated

layer [37]-[39]. The radiation damage results from the energetic ions accelerated by DC bias. The surface amorphized layer comes from the ion bombardment damage to junction surface. And the contaminated layer is due to the fluorocarbon-containing based etching chemistries. This damage layer is around hundred of angstroms deep from the surface. Some technologies [37], [38] are used to eliminate this surface damage layer including high temperature annealing, surface etching, etc. But these methods may not suitable for silicide process and ultra-shallow junction when manufacturing ULSI.

In our study, we proposed a novel selective liquid-phase deposition (S_LPD) process to overcome these problems. S_LPD process is the selective deposition technology which deposits oxide on silicide surface against contact-hole defined photoresist. This technology is conduct under non-plasma environment and hence it will not induce the surface damaged and contaminated layer. The experimental results indicate that the novel S_LPD process indeed has the superior of suppressing plasma damage on ultra-shallow junction. Therefore, the novel S_LPD process will become the candidate of non-plasma process for future advanced device manufacturing.

5.2 LIQUID-PHASE DEPOSITION (LPD) AND ITS SELECTIVITY

Figure 5-1 illustrates the schematic diagram of LPD apparatus used in this work. This system consists of two parts including an outer temperature-controlled cistern and an inner film deposition tank. The temperature-controlled cistern is connected with a refrigerated circulator to drive the temperature-controlled water flow and thereby keep the cistern and the film deposition tank at the desired temperature. The film deposition tank is filled with the chemical solution of LPD, and the sample wafers are immersed in the LPD solution to deposit LPD $SiO_{2-x}F_x$. The process flow of selective LPD (S_LPD) solution preparation is illustrated in Fig. 5-2. First, 80g of silica (SiO_2) powder with high purity of 99.99% was mixed into 1500

ml of hydrofluorosilicic acid (H_2SiF_6, 4mol/L). The solution became saturated with silicic acid ($Si(OH)_4$) after being stirred at 23℃ for 18 hours. The chemical reaction in the prepared solution can be represented by the following equilibrium equation:

$$5H_2SiF_6 + SiO_2 + 6H_2O \rightarrow 4SiF_6^{2-} + 2Si(OH)_4 + 6HF + 8H^+ \quad \text{.....(5.1)}$$

Before immersing the sample wafers, the prepared solution was filtered to remove the undissolved silica, and followed by adding deionized water into the saturated solution as it was stirred. The added deionized water enable the solution to become supersaturated with silicic acid $Si(OH)_4$. The corresponding process and mechanism of LPD have been proposed in our several literatures [40]-[42] in detail. In brief, we can write the net reaction of LPD for $SiO_{2-x}F_x$ deposition as following:

$$H_2SiF_6 + 2H_2O \rightarrow SiO_2 + 6HF \quad \text{.....(5.2)}$$

Figure 5-3 indicates that the process window of LPD is the function of silicic acid $Si(OH)_4$ concentration and solution temperature. Figure 5-4(a), 5-4(b) and 5-4(c) show the results of no-deposition, selective deposition and blanket deposition, respectively, by adequately controlling LPD solution in different conditions. In this work, we mainly perform the S_LPD in the solution condition of about 7.3×10^{-3} mol/L $Si(OH)_4$ concentration at 23 ℃. The SEM photograph in Fig. 5-4(b) shows the LPD oxide is selectively deposited against photoresist. It preliminarily reveals the absence of particles and indicates the feasibility of applying S_LPD to get sub-micron meter contact-holes. The photographs of Fig. 5-4(b) and 5-4(c) also reveals the conformal deposition of LPD SiO_2 and the capability to form the holes with high aspect-ratio.

5.3 EXPERIMENTS

In ULSI manufacturing, salicide and RIE processes are the commonly used technologies. Salicide is mainly used to reduce the parasitic resistance of MOSFET devices and RIE is used to etch the dielectric, metal, etc. In order to realize the influence of salicide and RIE processes on the MOSFET source/drain junction region, the following experiments were conducted to investigate the device degradation mechanism caused by these two processes.

5.3.1 Nickel Silicide Schottky Diode Using Different Contact-Hole Process

The Schottky diode was fabricated on the N-type (100) Si wafer with 2~7 Ω-cm bulk resistivity (10^{14}~$10^{15}$$cm^{-3}$). Conventional LOCOS process was adopted to isolate the individual device. Then, 200Å nickel was deposited on the wafer surface and the nickel silicide was formed by RTA (500℃, 30s). The contact-holes of Schottky diode were prepared by different technologies including S_LPD, RIE, and wet-etching. As shown in Fig. 5-5(a), for S_LPD sample, the inverse contact-hole mask made the photoresist on the area defined as the site of contact-hole keep intact. Next, the LPD oxide was selectively grown on the wafer against photoresist. After removing the photoresist, the contact-holes were automatically formed. For RIE and wet-etching samples, as shown in Fig. 5-5(b), PE-TEOS oxide or LPD oxide was globally deposited to cap the Schottky diodes. The PE-TEOS oxide was deposited by plasma-enhanced chemical-vapor-deposition (PECVD) under the following conditions: $TEOS/O_2$ = 10/200 (sccm), pressure = 300 (mtorr) and power = 200 (W). Then the contact-holes were defined through lithography, and etched using the RIE or the buffered oxide etching (BOE, NH_4F:HF = 6:1). RIE was performed under the following conditions: CHF_3/CF_4 = 40/80 (sccm), pressure = 5 mtorr and power/bias = 2300/900 (W). Before metallization, the samples were cleaned by H_2SO_4/H_2O_2 mixed solution. Four metal layers Ti/TiN/Ai-Si-Cu/TiN were then deposited as metal pad by PVD. After metallization, the

Schottky diodes were sintered at 400℃ for 30min in N_2. The detail process flows are list as follows:

1. LOCOS isolation.
2. RCA clean.
3. Nickel deposition: 200Å.
4. Rapid thermal annealing: 500℃, 30s.
5. Selectively etch remaining nickel: H_2SO_4/H_2O_2 (3:1).
6. Cleaning: H_2SO_4/H_2O_2 (3:1).
7. Contact-hole:
   (i) Selective liquid-phase deposition (S_LPD).
   (ii) LPD oxide with RIE etching (LPD_RIE).
   (iii) PE-TEOS oxide with RIE etching (TEOS_RIE).
   (iv) PE-TEOS oxide with BOE etching (TEOS_BOE).
8. Cleaning: H_2SO_4/H_2O_2 (3:1).
9. Metal deposition: Ti/TiN/Al-Si-Cu/TiN (400Å/1000Å/9000Å/400Å).
10. Metal pad etching.
11. Backside Al deposition.
12. Sintering: 400℃, 30 minutes in N_2.

Finally, the I-V characteristics, ideality factor and barrier height of Schottky diodes were measured by HP4156C semiconductor parameter analyzer.

5.3.2 Ultra-Shallow Junction n^+/p Diode with Nickel Silicide

The ultra-shallow junction n^+/p diode with nickel silicide was used to analysis the current-voltage (I-V) characteristics. As shown in Fig. 5-6(b), the n^+/p diode was fabricated on the P-type (100) Si wafer with 15~25 Ω-cm bulk resistivity ($10^{15}cm^{-3}$). Conventional LOCOS process was adopted to isolate the individual device. The n^+/p ultra-shallow junction was formed by the implantation of arsenic with the dose of 2×10^{15} cm^{-2} and the energy of 30 keV. After the ion implantation, the junction was activated by RTA (1000℃, 30s). Following the formation of ultra-shallow junction, nickel silicide was formed on the junction with different nickel thickness and RTA temperature. After the deposition of PE-TEOS oxide and

the contact-holes etching, metal pad was deposited and patterned. Then the wafers were sintered at 400℃ for 30mins in N_2 ambient. These detail process flows are list as follows:

1. LOCOS isolation.
2. RCA clean.
3. Ion implantation: As, 30keV, 2×10^{15} cm^{-2}.
4. RCA clean.
5. Rapid thermal annealing: 1000℃, 30 seconds.
6. RCA clean.
7. Nickel deposition: 100Å, 150Å, 200Å.
8. Rapid thermal annealing: 400℃ ~ 650℃, step = 50℃.
9. Selectively etch remaining nickel: H_2SO_4/H_2O_2 (3:1).
10. Cleaning: H_2SO_4/H_2O_2 (3:1).
11. Passivation layer: PE-TEOS, 5000Å.
12. Contact-holes etching: Reactive ion etching (RIE).
13. Cleaning: H_2SO_4/H_2O_2 (3:1).
14. Metal deposition: Ti/TiN/Al-Si-Cu/TiN (400Å/1000Å/9000Å/400Å).
15. Metal pad etching.
16. Backside Al deposition..
17. Sintering: 400℃, 30 minutes in N_2.

Finally, the I-V characteristics of silicide ultra-shallow junction were measured by HP4156C semiconductor parameter analyzer.

5.3.3 Silicide Ultra-Shallow Junction Using Different Contact-Hole Processes

The ultra-shallow junction n^+/p diode was fabricated on the P-type (100) Si wafer with 15~25 Ω-cm bulk resistivity. As shown in Fig. 5-6, conventional LOCOS process was adopted to isolate the individual device. The n^+/p ultra-shallow junction was formed by the implantation of arsenic with the dose of 2×10^{15} cm^{-2} and the energy of 30 keV. After the ion implantation, the junction was activated by RTA (1000℃, 30s). Then, the 200Å nickel was deposited on the wafer surface and the nickel silicide was formed by RTA (500℃, 30s). The contact-holes of n^+/p ultra-shallow junction diode were prepared by different technologies including S_LPD, RIE and wet-etching. As shown in Fig. 5-6(a), for S_LPD samples, the

inverse contact-hole mask made the photoresist on the area defined as the site of contact-hole keep intact. Next, the LPD oxide was selectively grown on the wafer against photoresist. After removing the photoresist, the contact-holes were automatically formed. For RIE and wet-etching samples, as shown in the Fig. 5-6(b), PE-TEOS oxide or LPD oxide was globally deposited to cap the n^+/p diode. The PE-TEOS oxide was deposited by PECVD under the following conditions: $TEOS/O_2$ = 10/200 (sccm), pressure = 300 (mtorr) and power = 200 (W). Then the contact-holes were defined through lithography, and etched by RIE and BOE. RIE was performed under the following conditions: CHF_3/CF_4 = 40/80 (sccm), pressure = 5 mtorr and power/bias = 2300/900 (W). Before metallization, the samples were cleaned by H_2SO_4/H_2O_2 mixed solution. Four metal layers Ti/TiN/Ai-Si-Cu/TiN were then deposited as metal pad by PVD. After metallization, the n^+/p diodes were sintered at 400℃ for 30mins in N_2. The detail process flows are list as follows:

1. LOCOS isolation.
2. RCA clean.
3. Ion implantation: As, 30keV, 2×10^{15} cm^{-2}.
4. RCA clean.
5. Rapid thermal annealing: 1000℃, 30s.
6. RCA clean.
7. Nickel deposition: 200Å.
8. Rapid thermal annealing: 500℃, 30s.
9. Selectively etch remaining nickel: H_2SO_4/H_2O_2 (3:1).
10. Cleaning: $H2SO_4/H_2O_2$ (3:1).
11. Contact-hole:
    (i) Selective liquid-phase deposition (S_LPD).
    (ii) LPD oxide with RIE etching (LPD_RIE).
    (iii) PE-TEOS oxide with RIE etching (TEOS_RIE).
    (iv) PE-TEOS oxide with BOE etching (TEOS_BOE).
12. Cleaning: H_2SO_4/H_2O_2 (3:1).
13. Metal deposition: Ti/TiN/Al-Si-Cu/TiN (400Å/1000Å/9000Å/400Å).
14. Metal pad etching.
15. Backside Al deposition.

16. Sintering: 400℃, 30 minutes in N_2.

Finally, the device parameter including the I-V characteristics, ideality factor and energy gap of n^+/p diode were measured by HP4156C semiconductor parameter analyzer.

5.4 RESULTS AND DISCUSSION

5.4.1 The Influences of LPD Solution and RIE Plasma Etching to Nickel Silicide

Figure 5-7 shows the sheet resistance variation of nickel silicide after the treatment of chemical solutions immersion and RIE plasma etching. LPD solution is the SiO_2 saturated H_2SiF_6 solution and it may have the similar property as HF and BOE solution. The immersion experiments were conducted to compare the influence of these three different solutions to nickel silicide. The fluorine ion is considered to replace the nickel and form the SiF_x compound, causing the increase of sheet resistance. From Fig. 5-7(a), it shows the degradation of silicide immersed in HF and BOE solutions. But the silicide immersed in LPD solution still retained the same value even after ten minutes immersion. This may due to the fluorine ions completely reacted with silicon dioxide and formed the SiO_2 saturated H_2SiF_6 solution. This result indicated that before the LPD oxide deposited on the silicide surface, the degradation of silicide is negligible.

In order to understand the difference between S_LPD and RIE processes. The effect of plasma etching on silicide sheet resistance was also investigated. Figure 5-7(b) is the results of nickel silicide exposed under plasma etching environment for different time. It showed that the nickel silicide will degraded after the plasma treatment, which is equal to the over-etching condition. According the results, it was found that S_LPD has the superior of non-etching and non-plasma damage to RIE.

5.4.2 Nickel Silicide Schottky Diode with Different Contact-hole Processes

Figure 5-8 is the current-voltage characteristics of Schottky diodes with different contact-hole process including S_LPD, LPD_RIE, TEOS_RIE and TEOS_BOE. The Schottky diode was fabricated using nickel silicide. From the figure, it showed good rectifying characteristic of Schottky diodes for these four contact-hole processes. The forward and reverse current of Schottky diodes with different contact-hole processes did not show obvious difference. To further investigate the effects of different process to the device characteristic, the ideality factor and barrier height of the Schottky diode were calculated to compare.

5.4.2.1 Ideality Factor of Schottky Diode

Figure 5-9 is the calculated ideality factor of Schottky diode with different contact-hole processes. Base on the current equation of Schottky barrier:

$$I = I_s\left(e^{\frac{qV}{nkT}} - 1\right)$$

$$\Rightarrow \quad I = I_s e^{\frac{qV}{nkT}} \qquad \text{as qV >> kT}$$

$$\Rightarrow \quad n = \frac{q}{kT}\frac{\partial V}{\partial(\ln I)} \qquad \text{.....(5.3)}$$

The ideality factor was calculated at V_F = 0.1-0.2V with the diode area of 1000×1000 μm^2. In Fig. 5-9(a), it was found that the contact-hole formation using the S_LPD technology showed the lowest ideality factor of 1.24, while the LPD_RIE, TEOS_RIE and TEOS_BOE were 1.33, 1.38 and 1.37, respectively. For LPD_RIE sample, the increase of ideality factor was due to the RIE because the difference between S_LPD and LPD_RIE was RIE process. As for TEOS_RIE sample, the ideality factor increased again due to another plasma process of PE-TEOS oxide deposition. If the RIE process was taken away, as for TEOS_BOE sample,

the ideality factor decreased as was considered. According to the results, the plasma process including RIE and PECVD both can degrade the ideality factor of Schottky diode. Besides, the uniformity of the TEOS_RIE and the TEOS_BOE samples were poor than the S_LPD and the LPD_RIE samples. It may due to the diode exposing area in RIE process was 25% of that in PECVD process. In order to study the area effect of plasma to device performance, the ideality factor of different diode area were measured. Figure 5-9(b) shows the ideality factor vs. diode area for different contact-hole processes. The ideality factor for all contact-hole processes increased with the increasing of diode area. This may due to that the large diode area has more surface states. Surface state will cause the increasing of ideality factor. From the ideality factor decreasing rate with area, it was found that S_LPD process showed the lowest slope, while the TEOS_RIE process showed the highest slope. Because the large diode area will experience more plasma damage, TEOS_RIE sample with both RIE and PECVD plasma processes displayed the quickest increasing rate with diode area. It was suggested that the degradation of ideality factor may due to the radicals in plasma environment diffused into the interface of silicide and silicon because the possible reason of ideality factor degradation in this experiment were surface state or defects in depletion region. Table 5-1 summarizes the ideality factor of Schottky diode with different contact-hole processes.

5.4.2.2 Barrier Height of Schottky Diode

Figure 5-10 reveals the results of barrier height for different contact-hole processes. Base on the current equation of Schottky barrier:

$$I = AA^{*}T^{2}\exp\left(\frac{-q\phi_{B}}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right)-1\right]$$

$$\Rightarrow \ \ln\left(I/T^{2}\right)=\ln\left(AA^{*}\right)-\frac{q\left(\phi_{B}-V/n\right)}{kT} \qquad \text{as qV >> kT}$$

$$\Rightarrow \quad \phi_B = \frac{V}{n} - \frac{k}{q}\frac{d\left[\ln\left(I/T^2\right)\right]}{d\left(1/T\right)} \qquad \text{.....(5.4)}$$

The barrier height of Schottky diode was calculated using the activation energy method, which the forward current was measured at the bias voltage of 0.1V and at the temperature from 30℃ to 110℃. Figure 5-10(a) is the Richardson plot of the results. It displayed that S_LPD sample showed the steepest slope, while TEOS_RIE sample showed lowest slope. After considering the ideality factor, the barrier height of Schottky diode was calculated. Figure 5-10(b) is the calculated result for different contact-hole processes. It indicated that the barrier height of S_LPD sample was the highest among these samples. The variation of barrier height may result from such causes as contamination in the interface, intervening insulating layer, edge leakage current, or deep impurity levels. According to the experimental conditions, deep impurity levels seemed to be the most possible factor. This can be explained that the radicals in plasma environment may diffuse into the interface and cause the surface state or defects in depletion region. TEOS_RIE sample revealed the lowest barrier height because it experience two plasma processes. Table 5-1 shows the barrier height for different processes.

5.4.3 I-V Characteristics of n^+/p Ultra-Shallow Junction with Nickel Silicide

5.4.3.1 Junction Depth for Different Ion Implantation Energy

Figure 5-11 is the secondary ion mass spectrometer (SIMS) depth profiles of arsenic with different ion implantation energy after 1000℃-30s RTA. The implantation energies were 10keV, 20keV and 30keV, respectively. The results showed that the junction depth was around 750Å for 10keV sample, 900Å for 20keV sample and 975Å for 30keV sample. These samples were implanted through 50Å screen oxide. But the experiments performed hereafter were no screen oxide, so the junction depth may be 50Å deeper than origin ones. So the junction depth would be about 1000Å for 30keV implantation and 1000℃-30s RTA.

5.4.3.2 n^+/p Junction Diodes with Different Silicide Thickness

Figure 5-12 indicates the typical I-V characteristics of n^+/p ultra-shallow junction diodes with different nickel thickness. The diode junction area was 1000×1000 μm^2 and the silicide was formed with 500℃, 30s RTA. Figure 5-13(a) and 5-13(b) show the reverse leakage current and forward current distribution of junction diodes, respectively. Figure 5-13(a) shows that the thicker the nickel thickness the higher the leakage current. This result was obvious since the thick silicide will approach the junction depletion region, causing the increase of metallic trap and hence the increase of leakage current. The nickel silicide formed with Ni 100Å, however, showed non-uniform distribution. This may due to the unstable deposition for thin metal film in our experiment. The forward current distribution shows in Fig. 5-13(b) displays the slightly high driving current of thick nickel silicide. This result comes from the low resistance of thick silicide. According to the TEM measurement of physical silicide thickness, the nickel silicide thickness is about 2.2 times the as-deposited nickel thickness. That is, as-deposited nickel film of 200Å will result in 440Å nickel silicide. Table 5-2 summarizes the diode characteristics including forward current, reverse current, J_{RA}, and J_{RP}. The formula used to extract these two components is showed as follows:

$$I = J_{RA}\ (A/cm^2) \times \text{areas} + J_{RP}\ (A/cm) \times \text{peripheral length} \quad \ldots\ldots(5.5)$$

J_{RA} represents the area component of junction leakage current while J_{RP} represents the periphery component of junction leakage current.

5.4.3.3 n^+/p Junction Diodes with Different Silicide Formation Temperature

Figure 5-14 is the typical I-V characteristics for silicide n^+/p ultra-shallow junction with different silicide formation temperature. The junction area was 1000×1000 μm^2 and the silicide was formed with 200Å nickel. Figure 5-15(a) and 5-15(b) show the reverse leakage

current and forward current distribution of nickel silicide n^+/p ultra-shallow junction with different silicide formation temperature, respectively. From Fig. 5-15(a), it was find that the leakage current decrease with increasing silicide formation temperature. The leakage current of silicide formation temperature 400℃ and 450℃ showed high leakage current. From our previous results, the low silicide formation temperature showed high value of sheet resistance and incomplete silicide formation. This phenomenon was also display in junction forward bias current distribution. From Fig. 5-15(b), it shows the non-uniform distribution and high forward current of junction diodes with low silicide formation temperature. The junction diodes I-V characteristics always showed high forward current along with high leakage current. Besides, it was discovered that the leakage current of junction diodes with 600℃ and 650℃ silicide formation temperature saturate and reach the lowest leakage current. This result may due to the complete formation of nickel silicide and the beginning of the transformation to nickel disilicide, which is the stable phase of nickel silicide. Owing to the stable property of nickel disilicide, the forward and reverse current distributions of junction diodes showed uniform distribution. According to our previous study, however, the nickel disilicide was not the proper phase to be used. Table 5-3 summarizes the diode characteristics including forward current, reverse current, J_{RA}, and J_{RP}. From this table, it was found that the abnormal behavior of junction leakage current with 400℃ and 450℃ silicide formation temperature, which was also found in I-V characteristics. This abnormal phenomenon resulted from the non-linear relation between J_{RA} and J_{RP} to I, which was caused by the low temperature silicide formation. Therefore the negative value of J_{RA} was extracted from the linear formula.

5.4.4 Electrical Characteristics of n^+/p Diode Using Different Contact-Hole Processes

5.4.4.1 Current-Voltage Characteristics

Figure 5-16 is the I-V characteristics of silicide ultra-shallow junction with four different

contact-hole processes. From Fig. 5-16, it did not show obvious difference between these four processes. The I-V characteristics, however, divided into two groups when the reverse bias voltage over 2V. In Fig. 5-17(a), the reverse current distribution at 3V clearly shows this phenomenon. Different contact-hole process did not obviously affect the leakage current, but the leakage current distribution divided into two groups according the dielectric deposition method, LPD and PECVD. Because the LPD oxide was deposited at room temperature, it may have poor dielectric characteristic than the PECVD oxide, which was deposited at higher temperature (300℃). Fig. 5-17(b) is the forward current distribution of these four different contact-hole processes. All processes have the nearly same current, so it can not distinguish their difference. According to the result, it was found that these different contact-hole processes showed not obviously effect on n^+/p ultra-shallow junction diode, but the different dielectric deposition methods divided these samples into two groups. Figure 5-18 is the leakage current density of different peripheral length to area ratio. The calculated J_{RA} and J_{RP} were list in Table 5-1. From the calculated values, it was found that the differences of leakage current of these four processes were mainly come from the peripheral leakage current.

5.4.4.2 Ideality Factor of Ultra-Shallow Junction n^+/p Diode with Silicide

Figure 5-19 is the ideality factor distribution of diodes for different contact-hole processes. The ideality factor was calculated from eq. 5.3 for the forward voltage of 0.1-0.3 V. From the results, the ideality factor can not be obviously distinguished for different contact-hole processes. It was suggested that the plasma damage may not influence the junction as deep as 1000Å. According the previous Schottky diode results, the plasma damage can affect the Schottky barrier of about 500Å. So the plasma damage may distribute at least 500Å, but less than 1000Å.

5.4.4.3 Effective Energy Gap

Figure 5-20 to Fig. 5-23 show the reverse and forward current-voltage characteristics of different temperature for different contact-hole processes. All the reverse characteristics for different contact-hole process showed voltage dependent at low temperature and voltage independent at high temperature. According to the reverse current equation:

$$I_{gen} = qAW \times \frac{n_i}{2\tau} \propto T^{\frac{3}{2}} e^{\frac{-E_g}{2kT}} \quad \text{.....(5.6)}$$

$$I_{diff} = qAD \times \frac{n_i^2}{N_b L_d} \propto T^3 e^{\frac{-E_g}{kT}} \quad \text{.....(5.7)}$$

At low temperature, I_{gen} dominates reverses reverse current and at high temperature, I_{diff} dominates reverse current. All four samples showed good electrical characteristics. Figure 5-24 shows the Arrhenius plot. From the plot of $\ln(I_R/T^3)$ versus 1/kT, the slop gives the effective energy gap. The calculated energy gaps are shown in Table 5-1. The energy gap at high temperature (>130℃) was about twice the energy gap at low temperature (<130℃). These results matched the prediction of reverse current equation. For the samples of different contact-hole processes, however, the energy gap did not show obvious difference. The results again revealed the same phenomenon as for ideality factor. That was, the plasma damage may only affected the diode of the junction depth less than 1000Å.

5.5 SUMMARY

The optimum process condition of ultra-shallow junction n^+/p diode with nickel silicide has been found out in work. It was found that the leakage current increases with the increasing of nickel thickness. This phenomenon resulted from the approach of nickel silicide to junction depletion region. It was also found that the leakage current decreases with the increasing silicide formation temperature. This is due to the complete formation of nickel

silicide.

The new S_LPD process for contact-hole formation was also developed in this study. This technology was performed under a non-plasma environment. From the experimental results, S_LPD technology showed the lowest ideality factor and highest barrier height for Schottky diode. On the contrary, TEOS_RIE with the PECVD oxide deposition and RIE etching showed the poorest characteristics. For the ultra-shallow junction n^+/p diode, the electrical characteristics including current-voltage curve, ideality factor and effective energy gap did not show obvious difference. From the results of Schottky diode and n^+/p diode, it was suggested that the plasma damage may influence the junction depth between 500Å to 1000Å. This indicated that the sub-100nm device with the junction depth below 1000Å may be affected by the plasma damage including PECVD, RIE and so on. According to above mentioned, it is believed the S_LPD technology will be the promising technology for future advanced device fabrication.

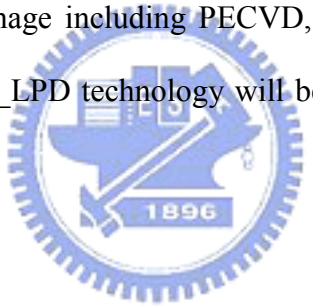


TABLE 5-1

Summary of Device Parameters for Different Contact-Hole Processes

	S_LPD	LPD_RIE	TEOS_RIE	TEOS_BOE
Schottky Diode				
Ideality Factor η (0.1 - 0.2V)				
1000×1000 μm^2	1.24	1.33	1.38	1.37
500×500 μm^2	1.20	1.26	1.31	1.29
200×200 μm^2	1.11	1.15	1.16	1.17
Barrier Height Φ_{Bn} (0.1V)				
1000×1000 μm^2 (V)	0.61	0.55	0.50	0.51
n^+/p Diode				
J_{RA}	5.40×10^{-8}	6.09×10^{-8}	3.49×10^{-8}	4.01×10^{-8}
J_{RP}	3.86×10^{-9}	8.01×10^{-9}	1.36×10^{-10}	4.08×10^{-10}
Ideality Factor η (0.1 - 0.3V)				
1000×1000 μm^2	1.11	1.13	1.09	1.12
Energy Gap Eg (1V)				
<130℃ (eV)	0.73	0.68	0.72	0.62
>130℃ (eV)	1.11	1.09	1.18	1.06

TABLE 5-2
Summary of Diode I-V Parameters with Different Nickel Thickness

Nickel Thickness	I_F (A)	I_R (A)	J_{RA} (A/cm^2)	J_{RP} (A/cm)
100Å	9.93×10^{-8}	7.34×10^{-12}	3.59×10^{-10}	9.39×10^{-12}
150Å	1.08×10^{-7}	2.17×10^{-10}	1.28×10^{-8}	2.22×10^{-10}
200Å	1.33×10^{-7}	3.37×10^{-10}	5.10×10^{-9}	7.15×10^{-10}

TABLE 5-3
Summary of Diode I-V Parameters
with Different Silicide Formation Temperature

RTA Temperature	I_F (A)	I_R (A)	J_{RA} (A/cm^2)	J_{RP} (A/cm)
400℃	2.90×10^{-7}	1.90×10^{-9}	-1.01×10^{-7}	7.29×10^{-9}
450℃	2.64×10^{-7}	1.20×10^{-9}	-4.90×10^{-8}	4.23×10^{-9}
500℃	1.33×10^{-7}	3.37×10^{-10}	5.10×10^{-9}	7.15×10^{-10}
550℃	1.34×10^{-7}	1.40×10^{-10}	5.70×10^{-9}	2.07×10^{-10}
600℃	1.01×10^{-7}	1.76×10^{-11}	3.40×10^{-10}	3.54×10^{-11}
650℃	1.14×10^{-7}	1.41×10^{-11}	1.87×10^{-10}	3.05×10^{-11}

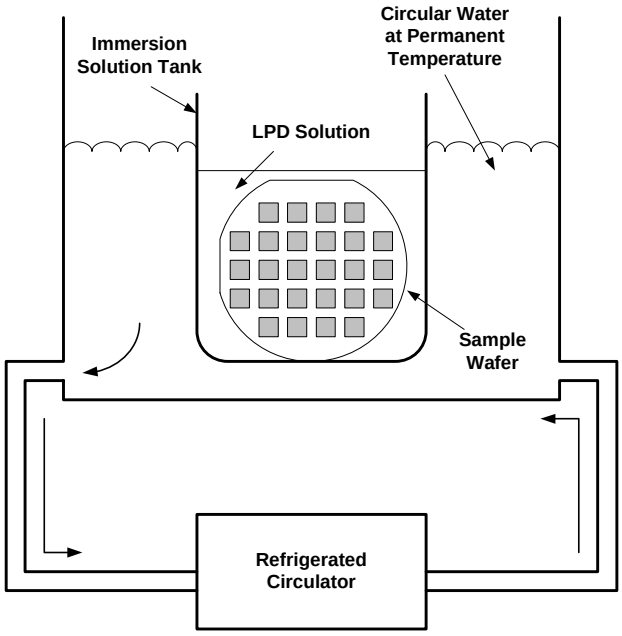


Fig. 5-1. The schematic diagram of LPD apparatus.

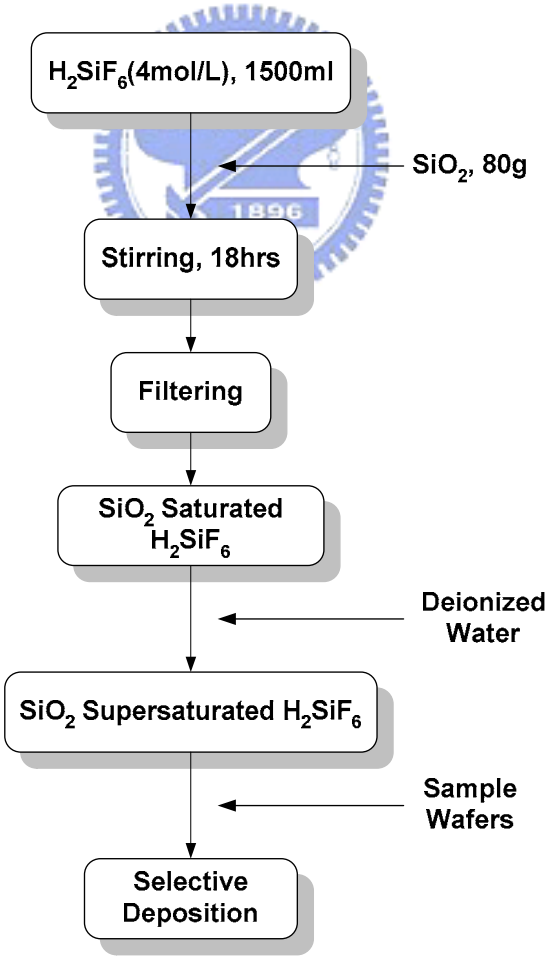


Fig. 5-2. The process flow of preparing S_LPD solution.

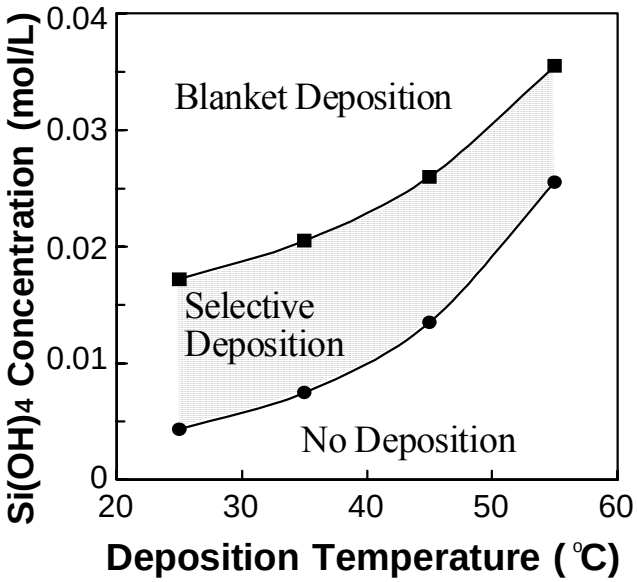


Fig. 5-3. The process window of S_LPD.

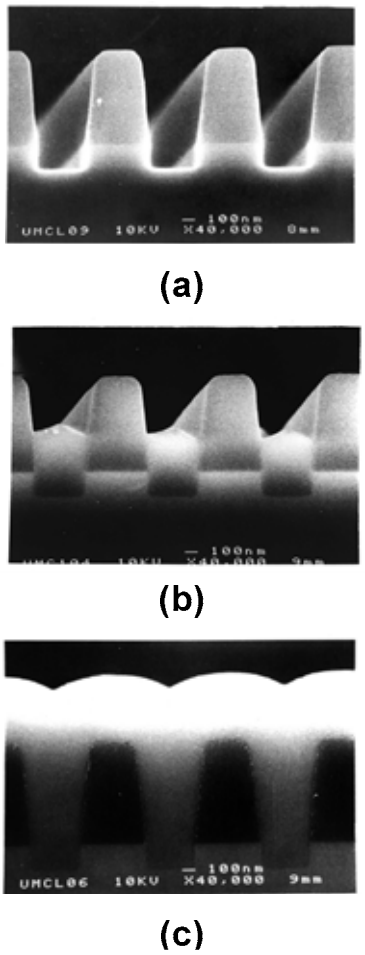


Fig. 5-4. SEM photographs of (a) No deposition, (b) Selective deposition and (c) Blanket deposition.

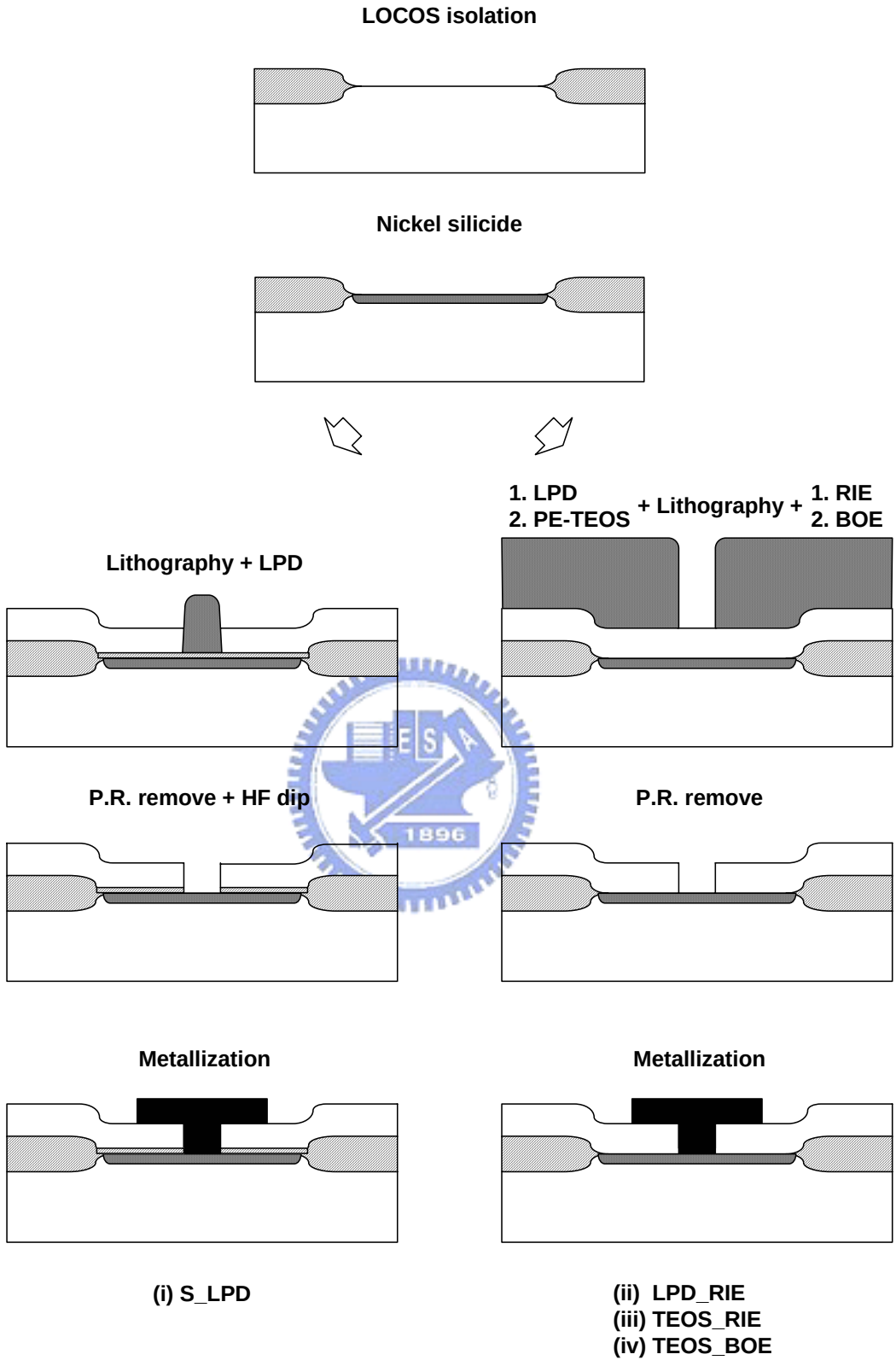


Fig. 5-5. Process flow of nickel silicide schottky diodes with contact-hole prepared by (a) S_LPD and (b) LPD_RIE, TEOS_RIE, and TEOS_BOE.

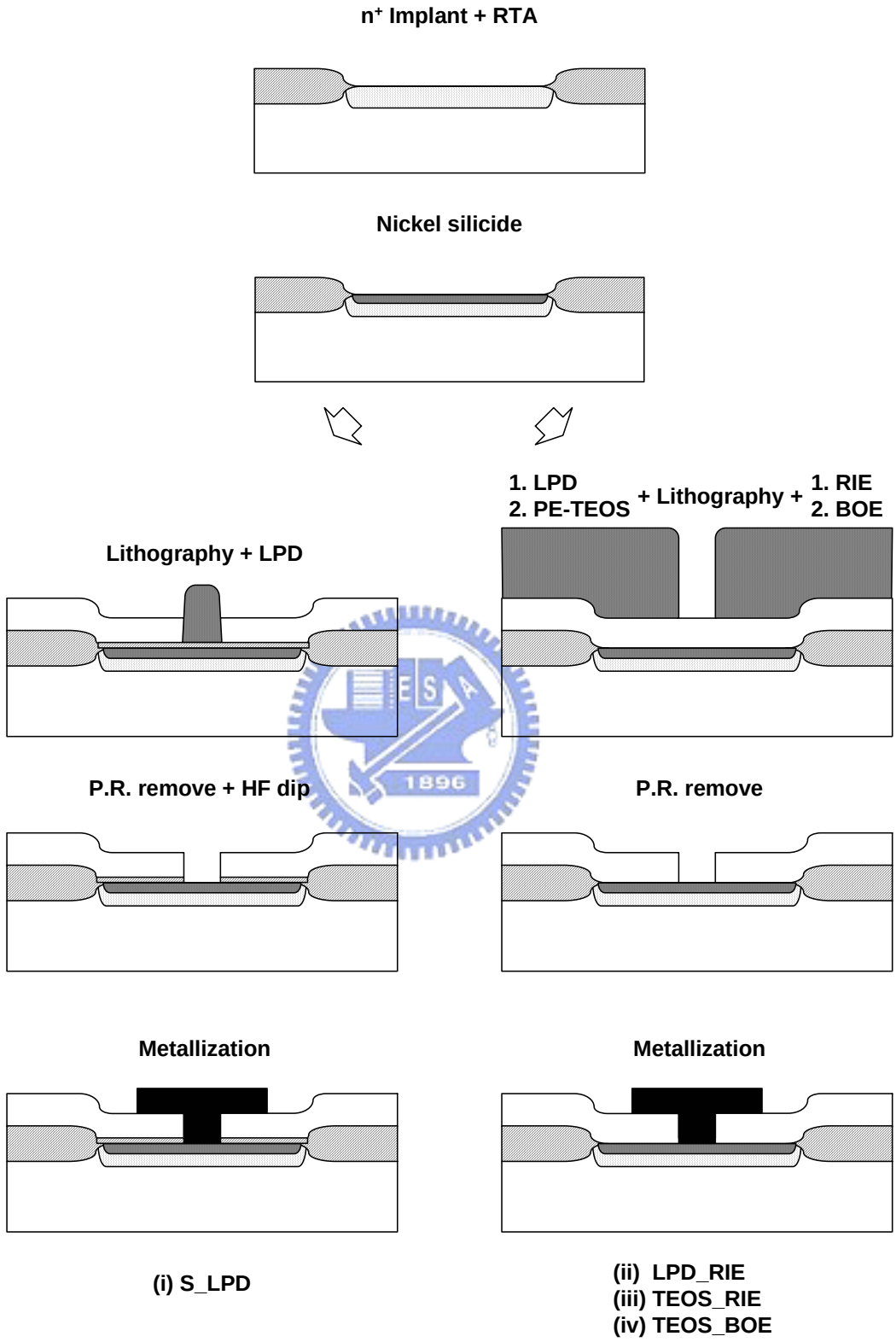
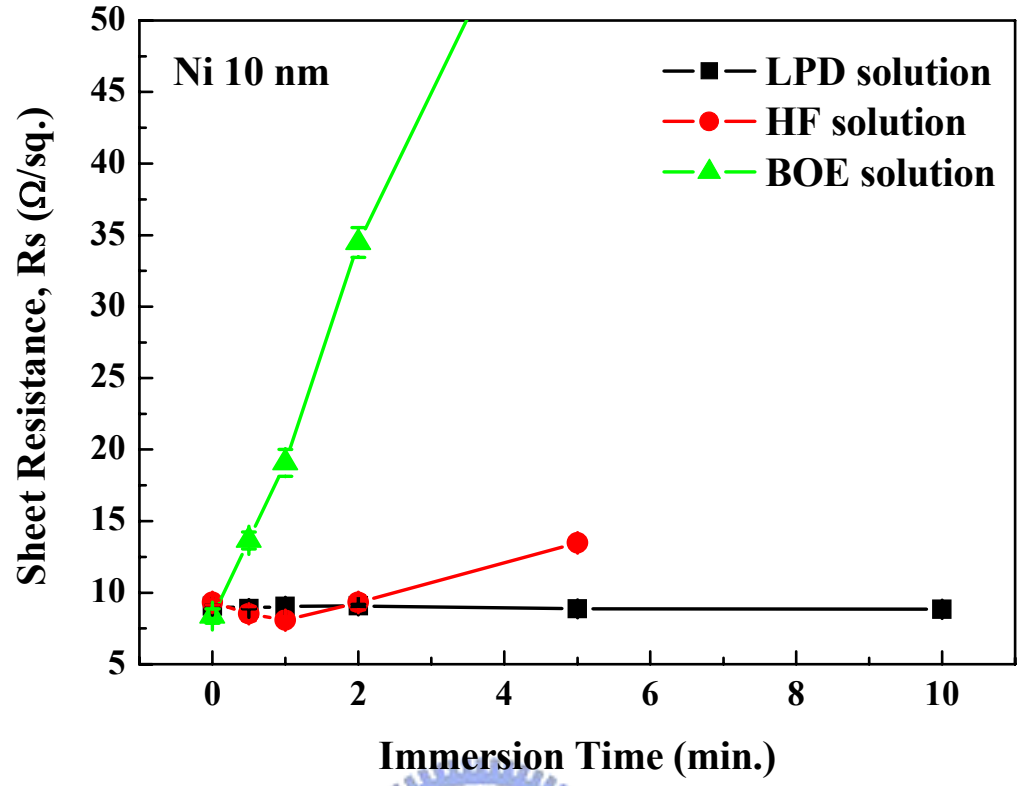
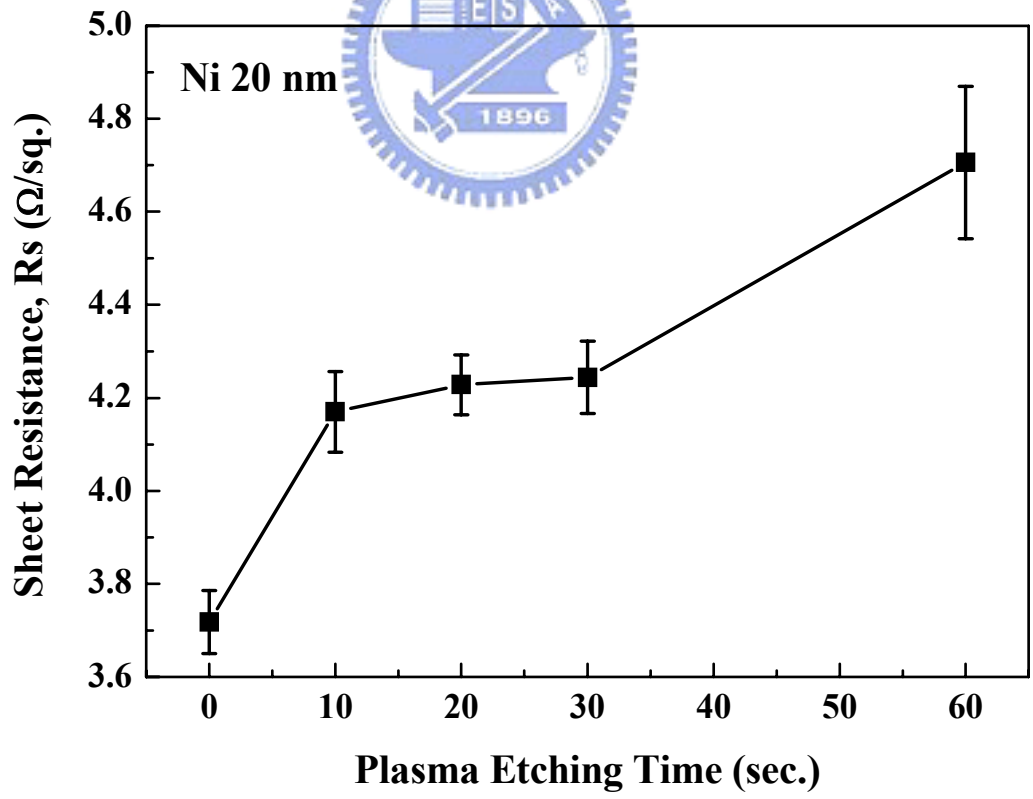


Fig. 5-6. Process flow of ultra-shallow junction n^+/p diodes with contact-hole prepared by (a) S_LPD and (b) LPD_RIE, TEOS_RIE, and TEOS_BOE.



(a)



(b)

Fig. 5-7. The sheet resistance variation of nickel silicide after the treatment of (a) Chemical solutions and (b) RIE plasma.

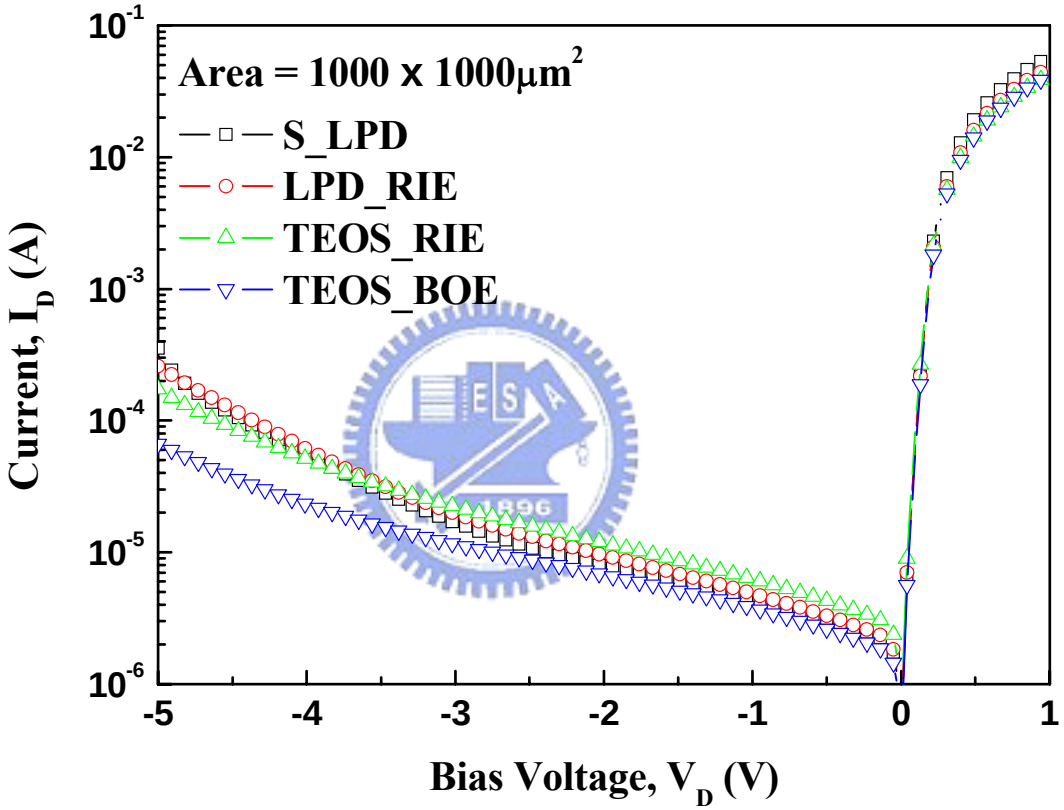
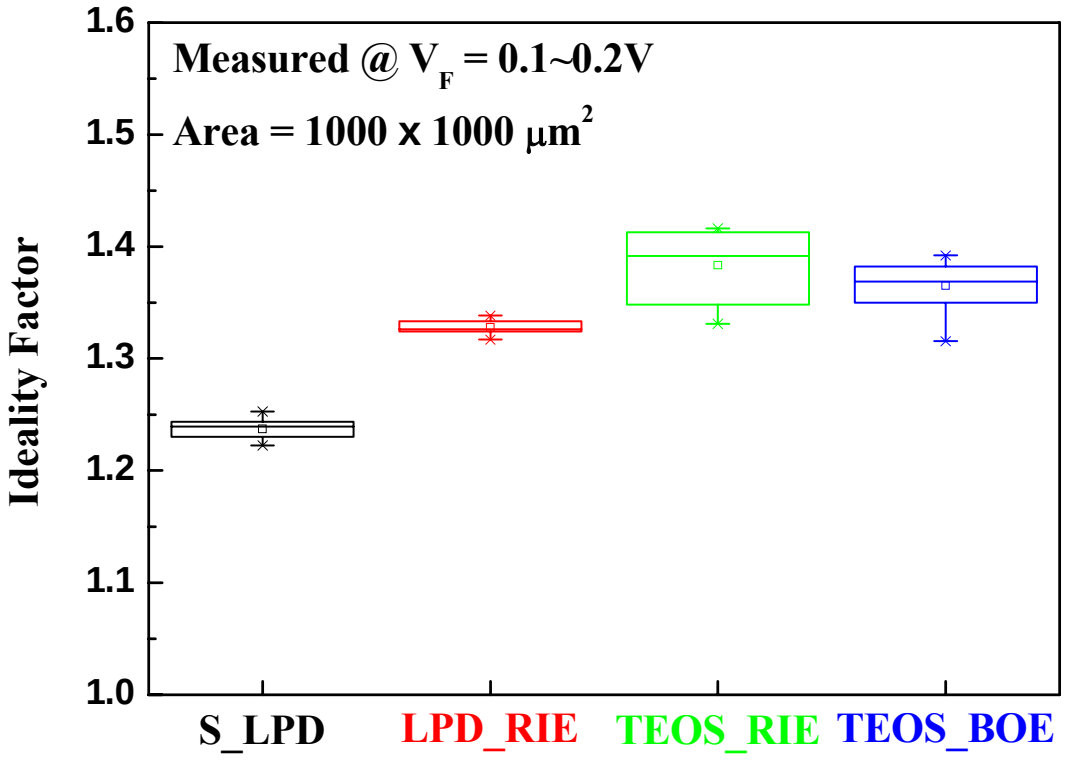
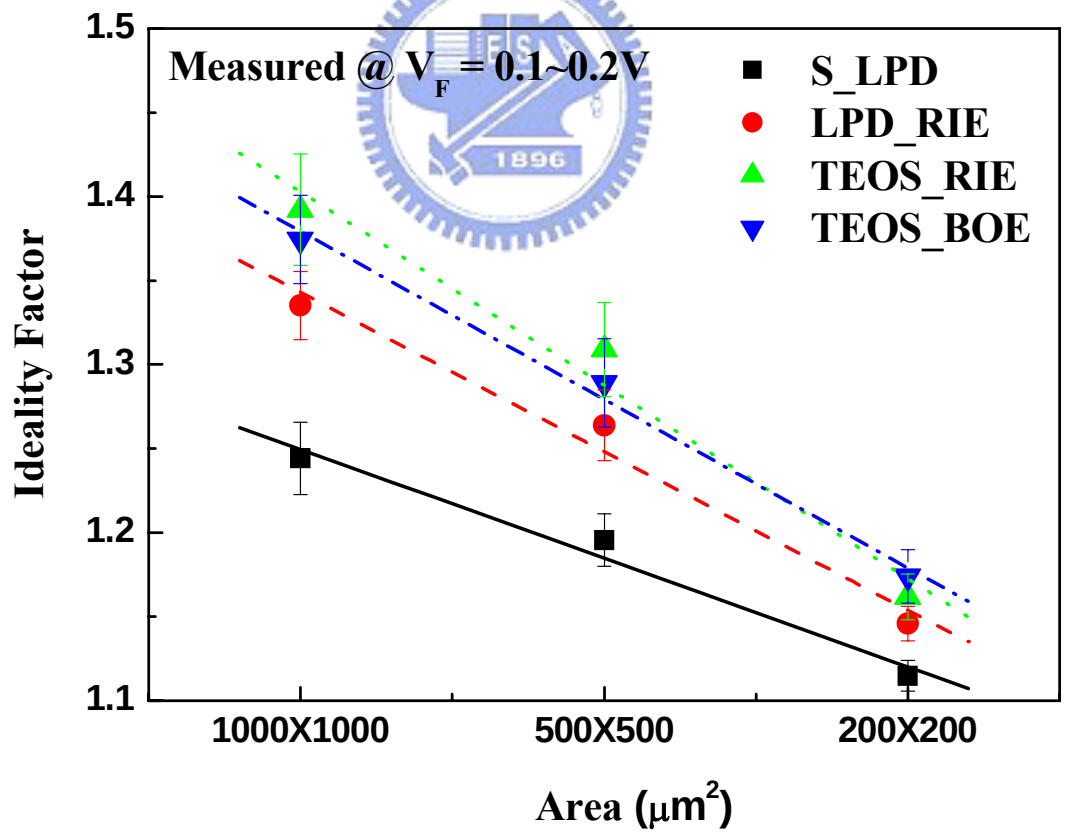


Fig. 5-8. The current-voltage characteristics of schottky diodes with different contact-hole processes.

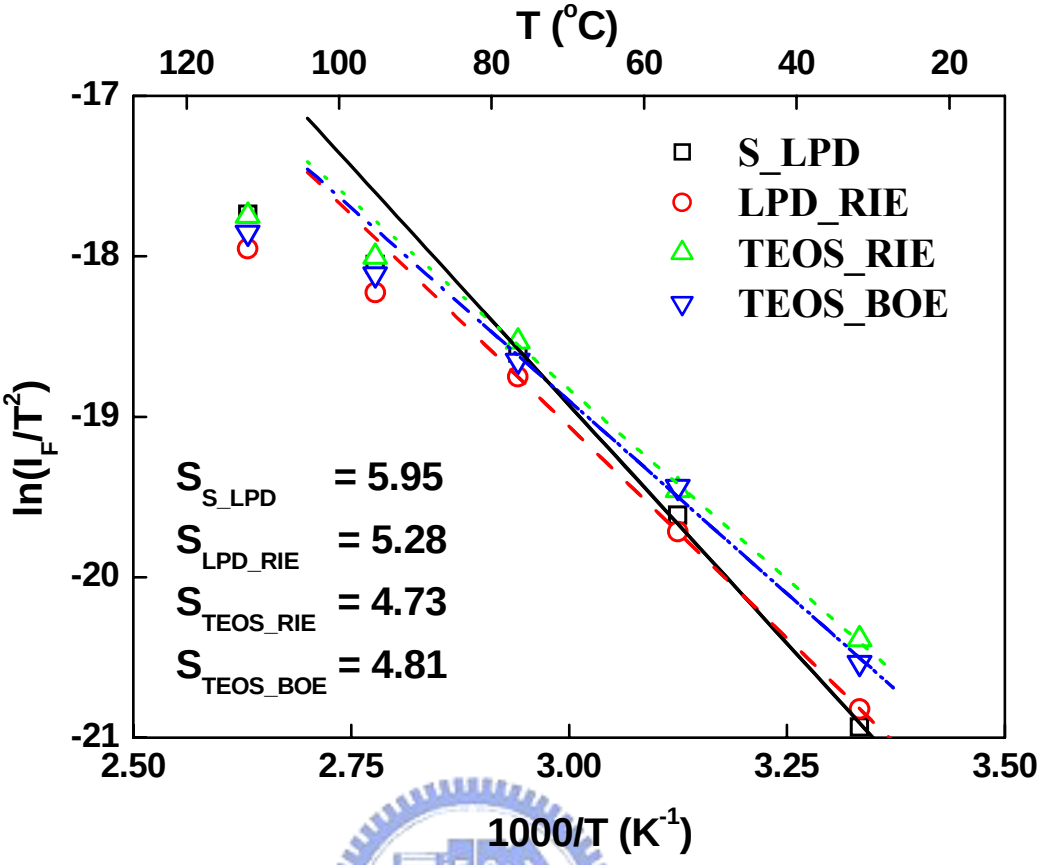


(a)

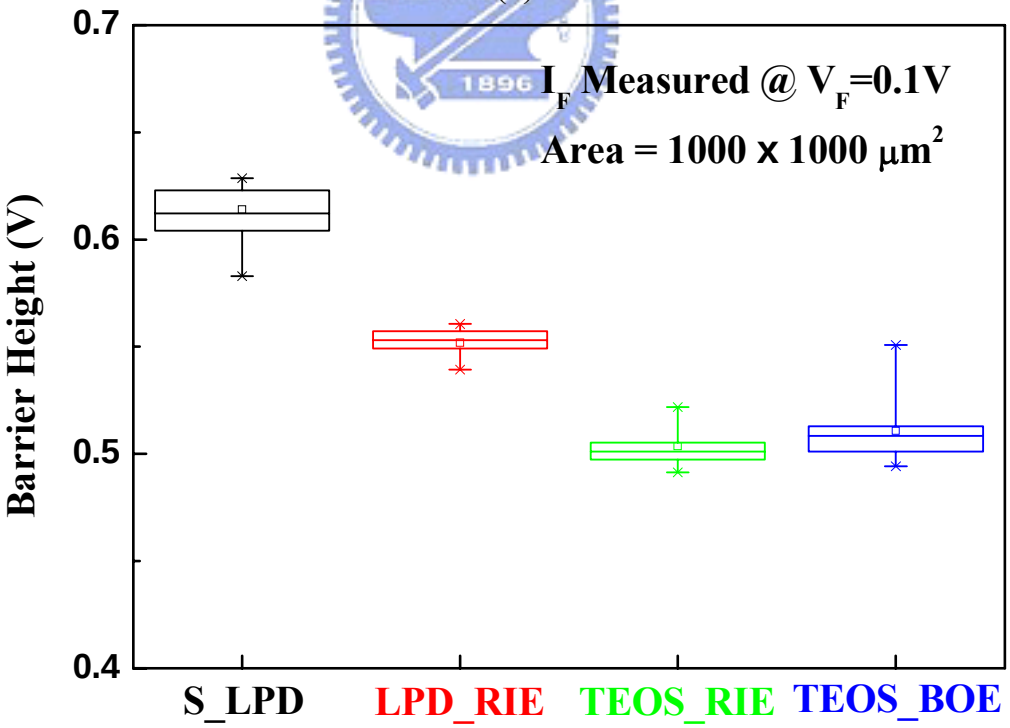


(b)

Fig. 5-9. The ideality factor variation of schottky diode with (a) Different contact-hole processes and (b) Different diode area.



(a)



(b)

Fig. 5-10. (a) Richardson plot and (b) Barrier height of different contact-hole processes.

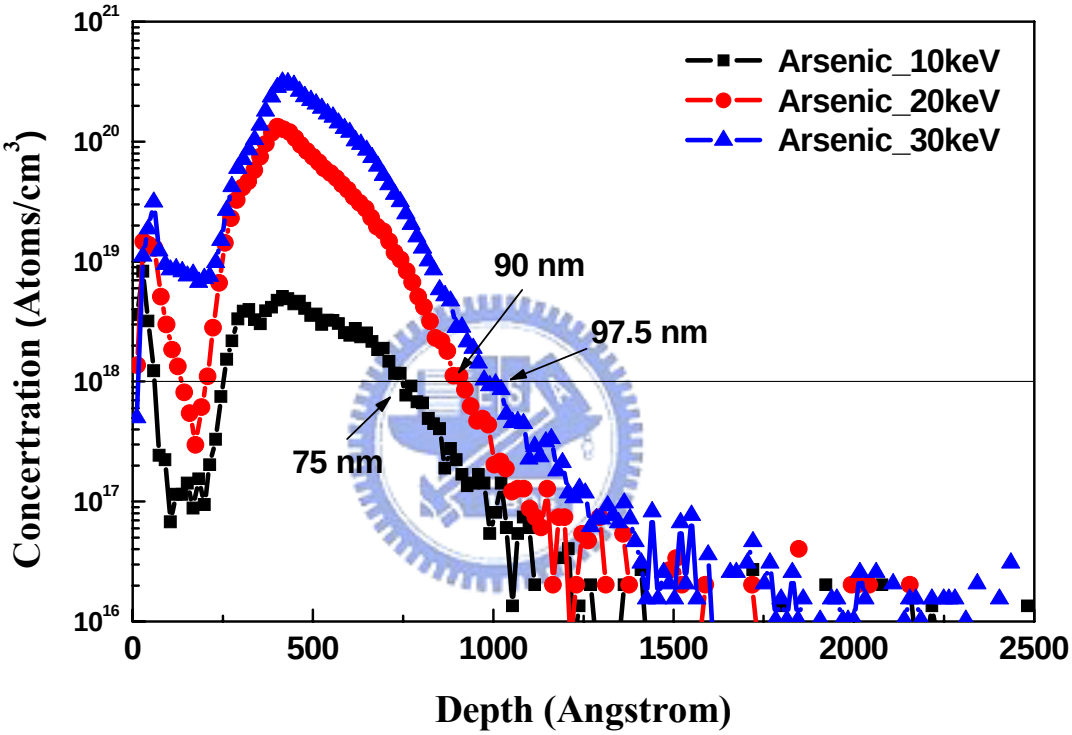


Fig. 5-11. SIMS depth profiles with different ion implantation energy.

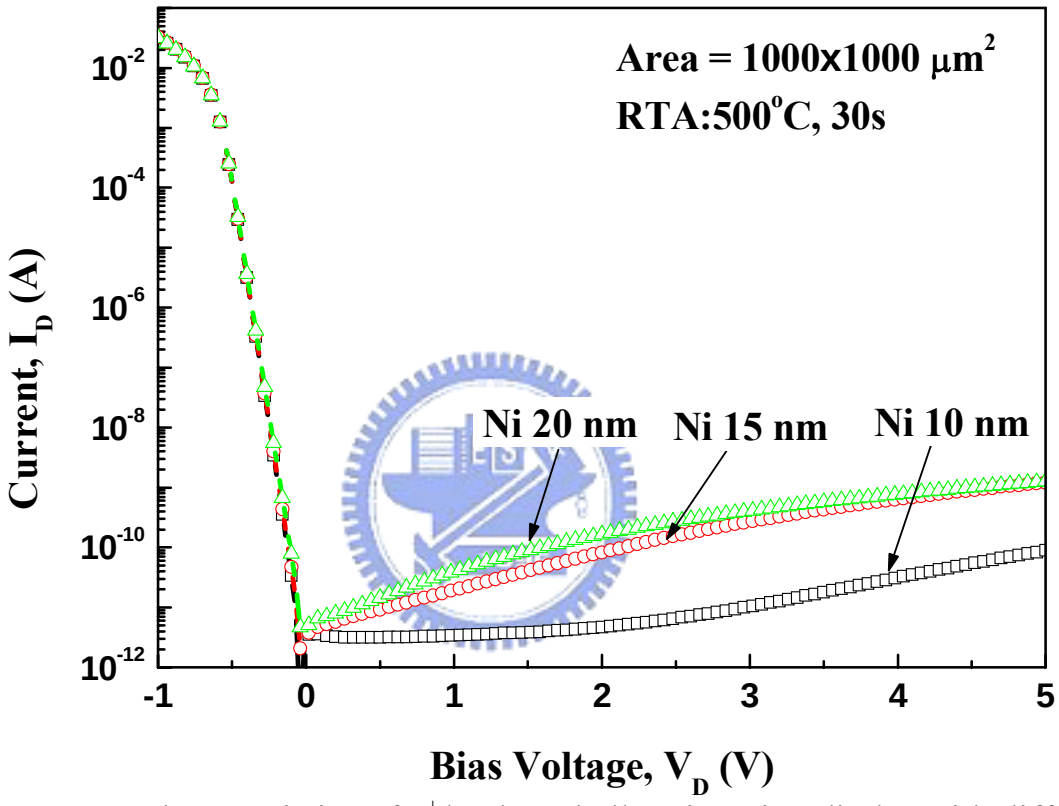
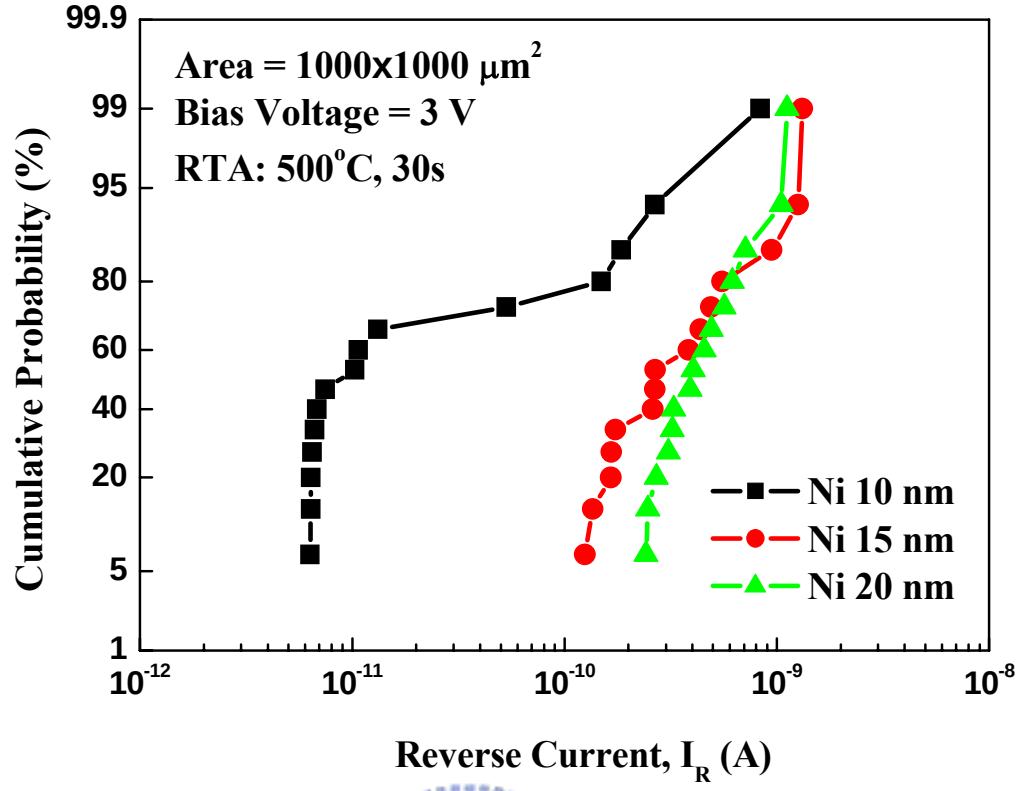
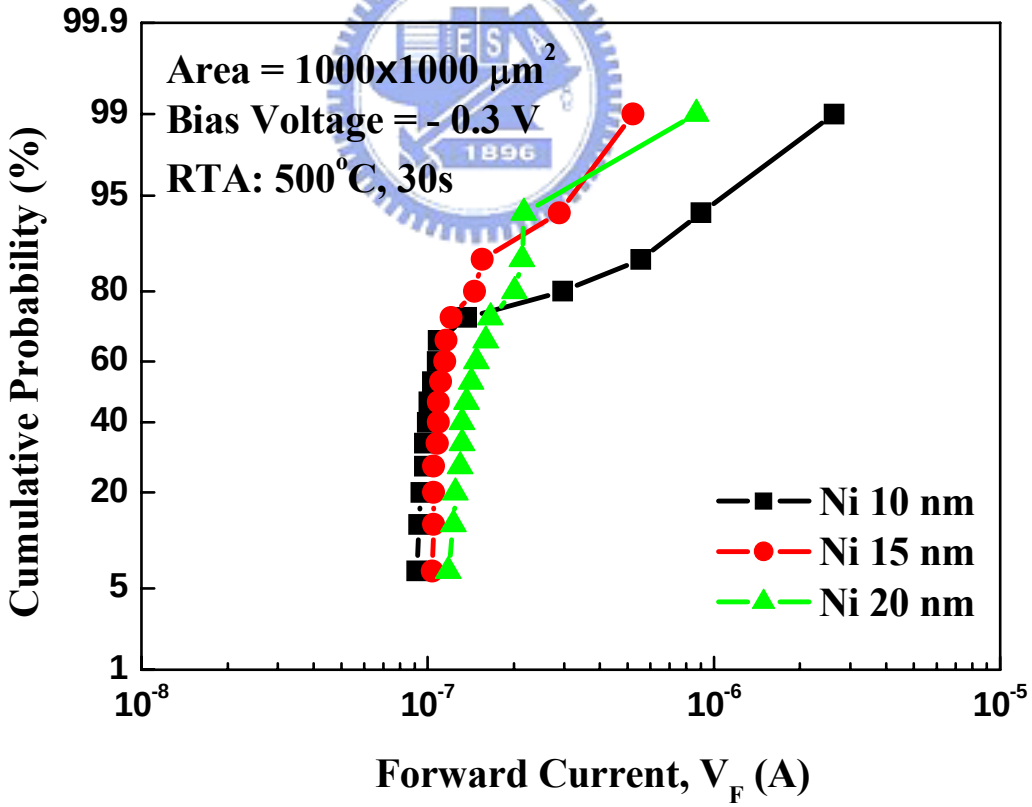


Fig. 5-12. I-V characteristics of n^+/p ultra-shallow junction diodes with different nickel thickness.



(a)



(b)

Fig. 5-13. (a)Reverse leakage current and (b) Forward current distribution of n^+/p ultra-shallow junction with different nickel thickness.

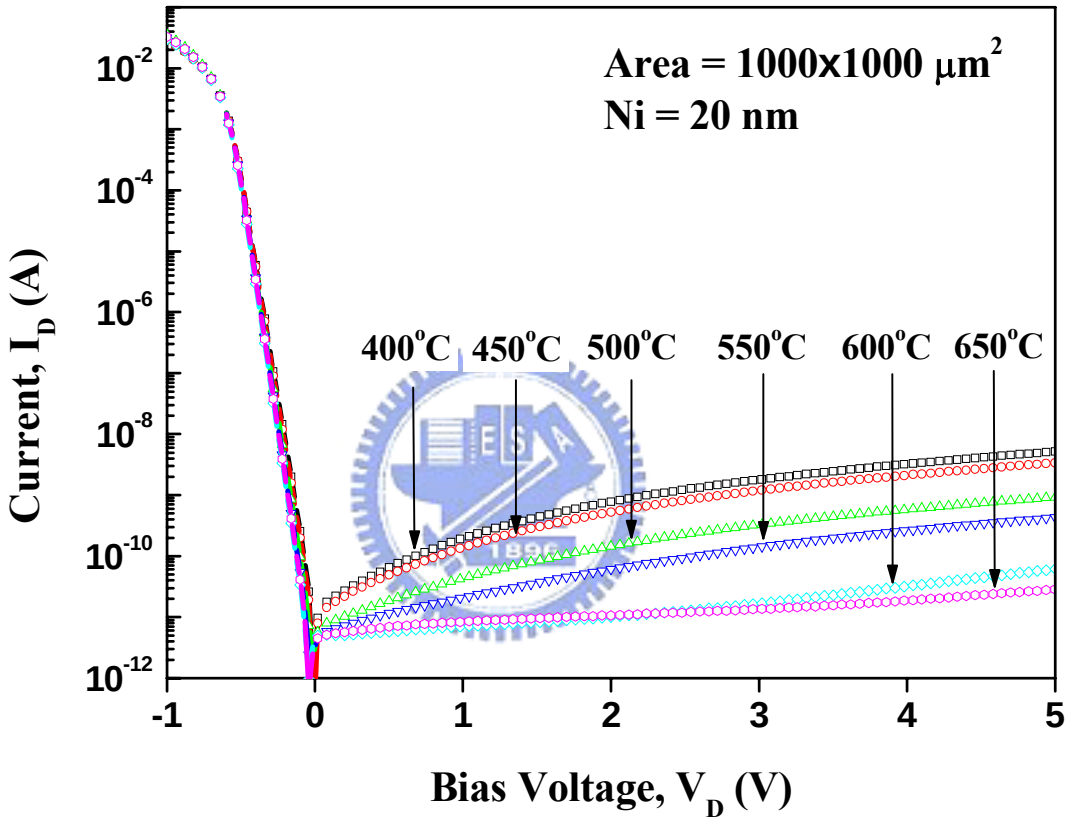
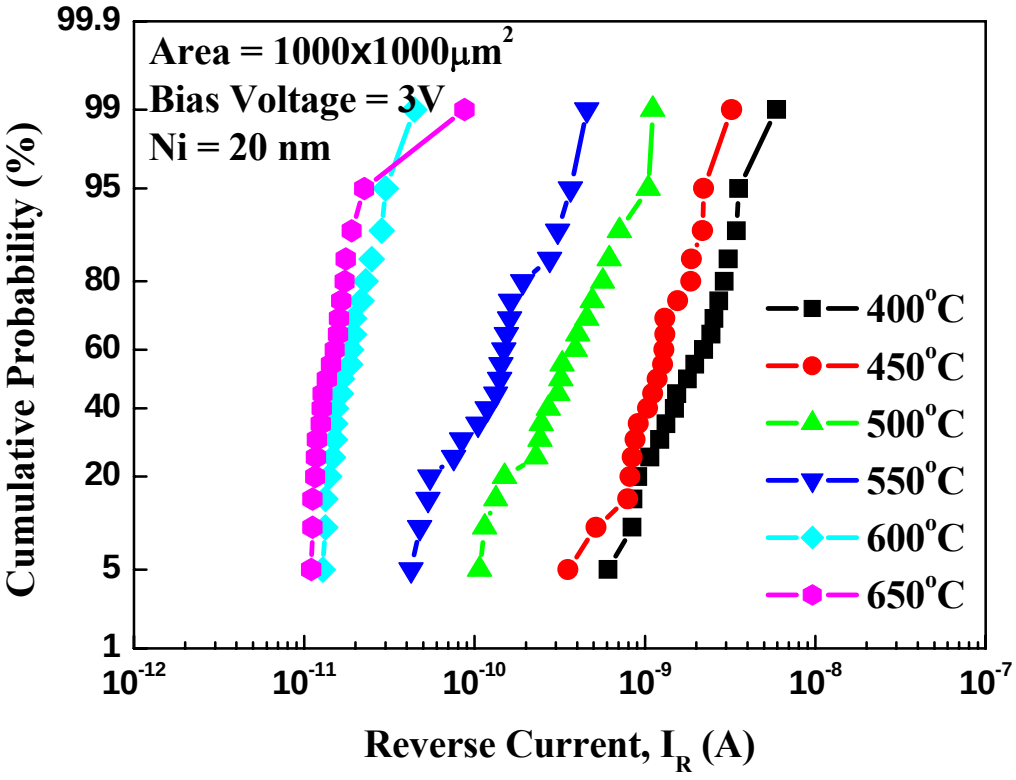
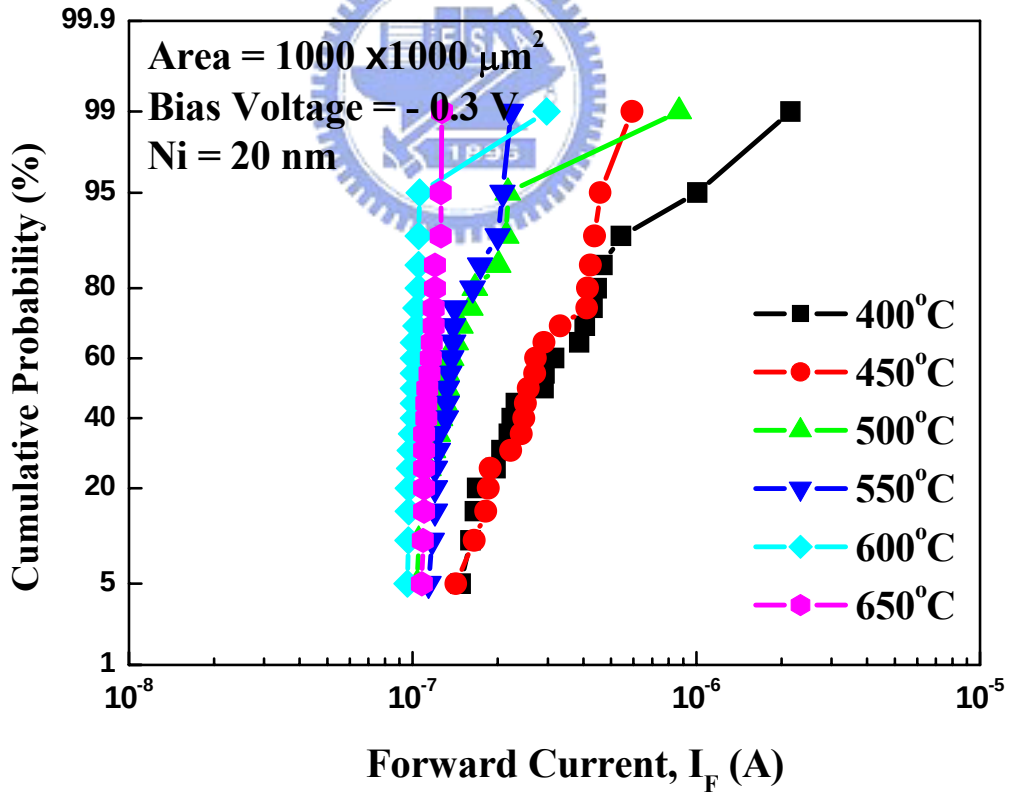


Fig. 5-14. I-V characteristics of n^+/p ultra-shallow junction diodes with different silicide formation temperature.



(a)



(b)

Fig. 5-15. (a) Reverse leakage current and (b) Forward current distribution of n^+/p ultra-shallow junction with different silicide formation temperature.

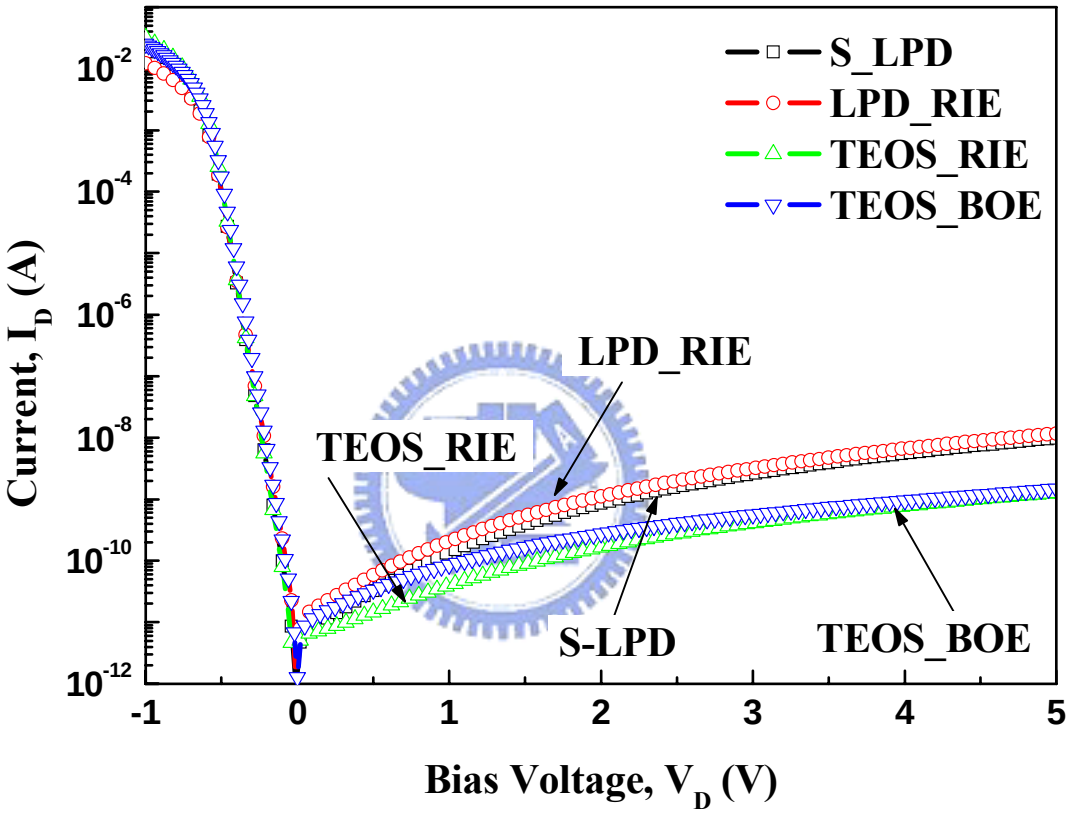
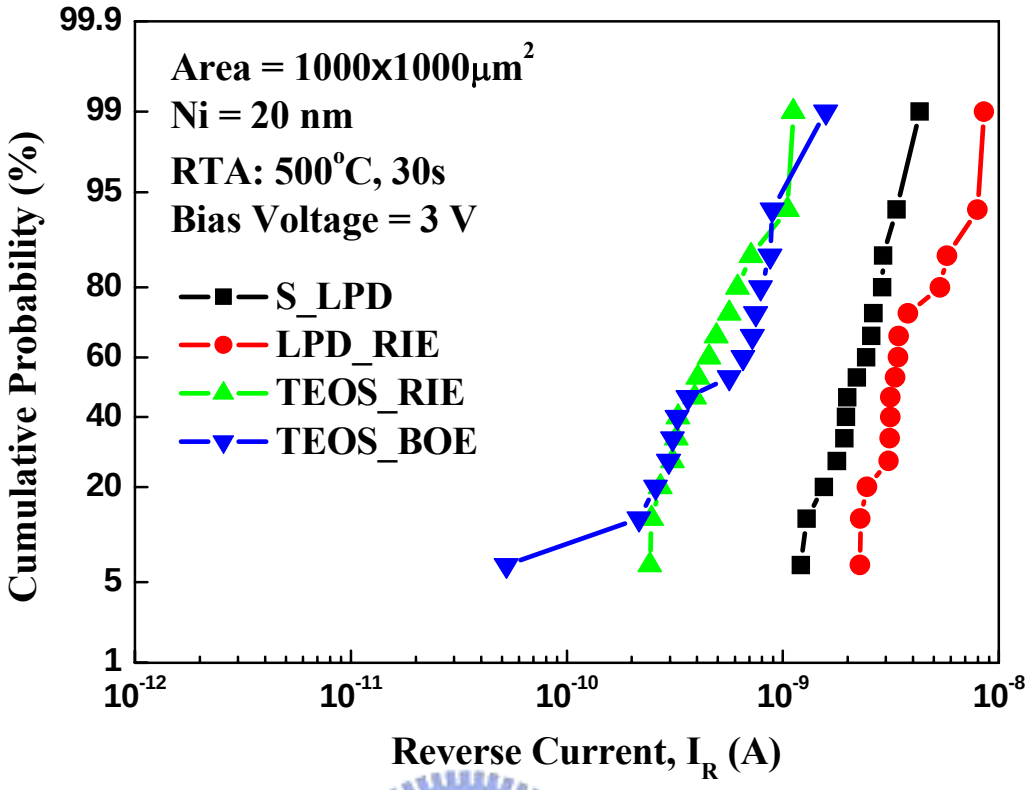
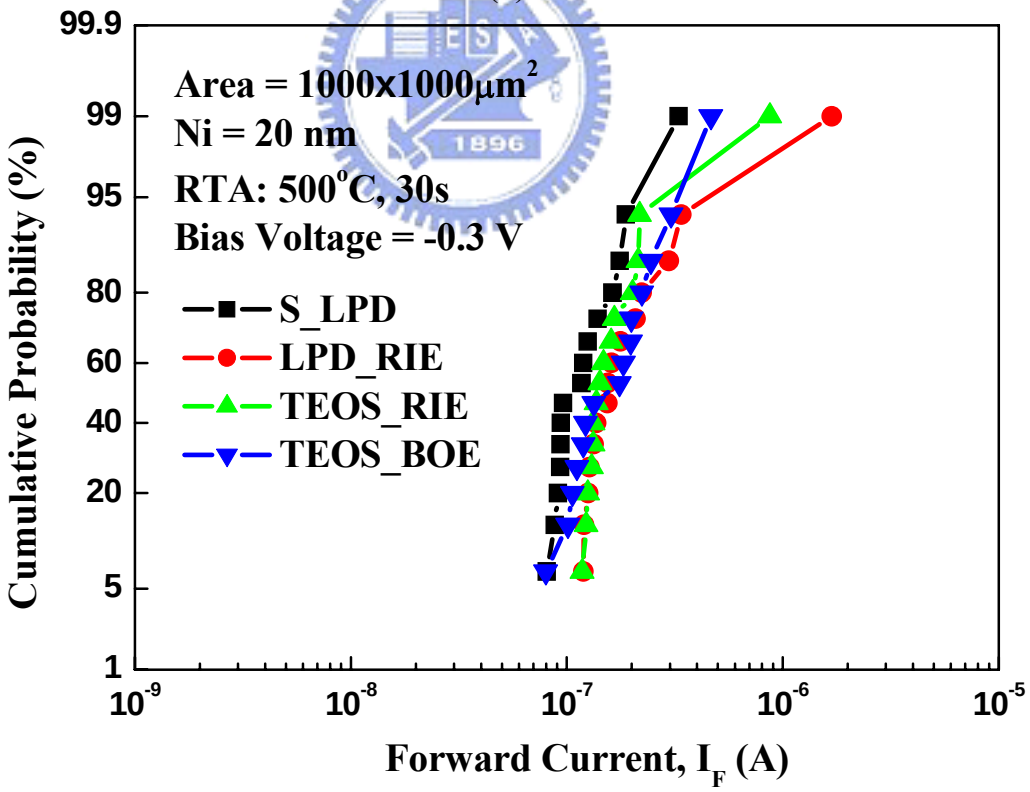


Fig. 5-16. I-V characteristics of silicide ultra-shallow junction with different contact-hole processes.



(a)



(b)

Fig. 5-17. (a) Reverse and (b) Forward current distribution of silicide ultra-shallow junction with different contact-hole processes.

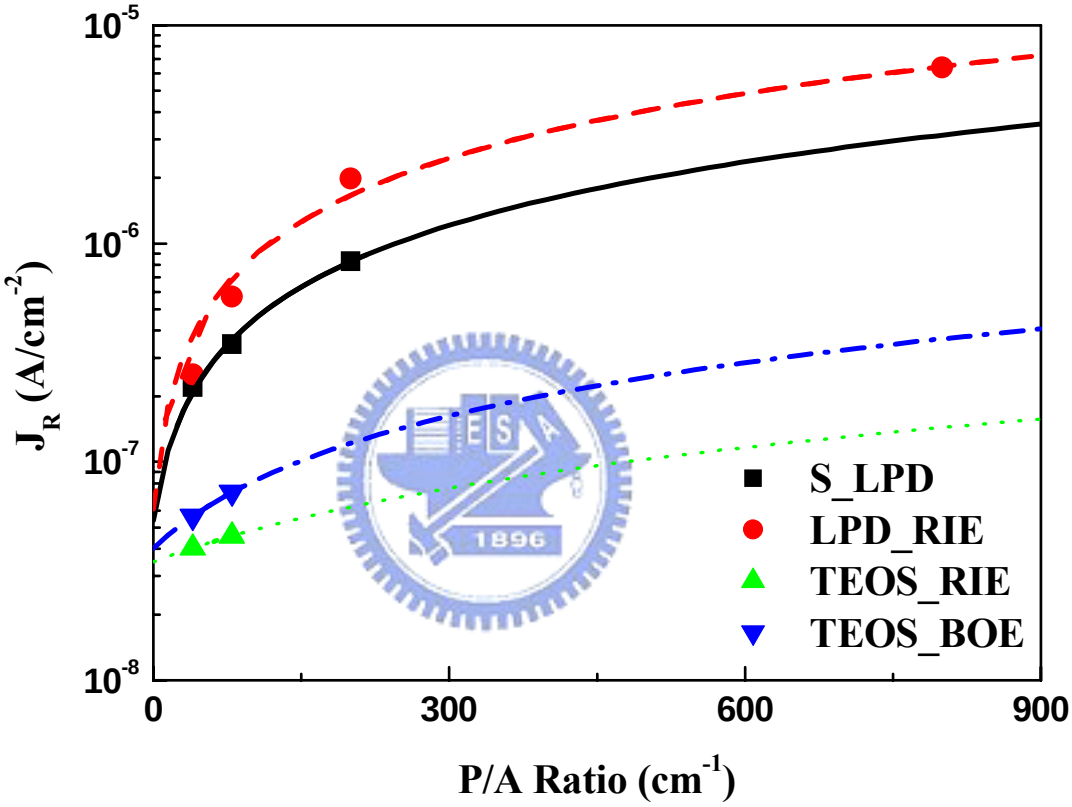


Fig. 5-18. The leakage current density of different peripheral length to area ratio.

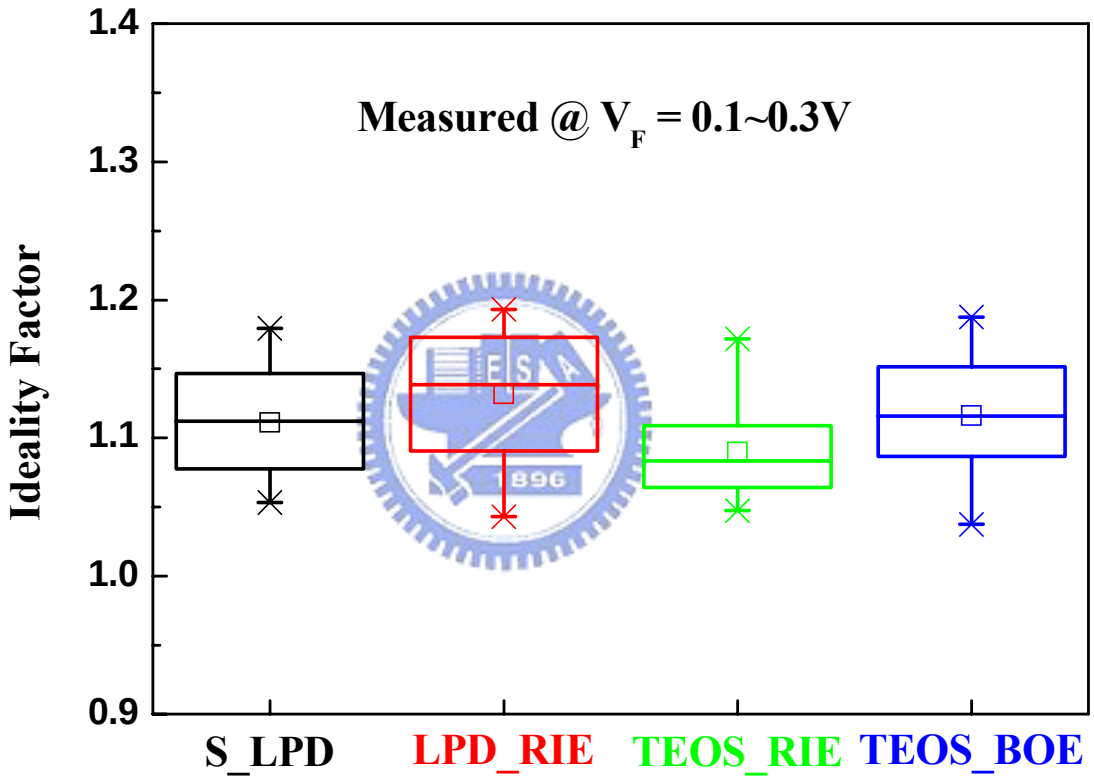
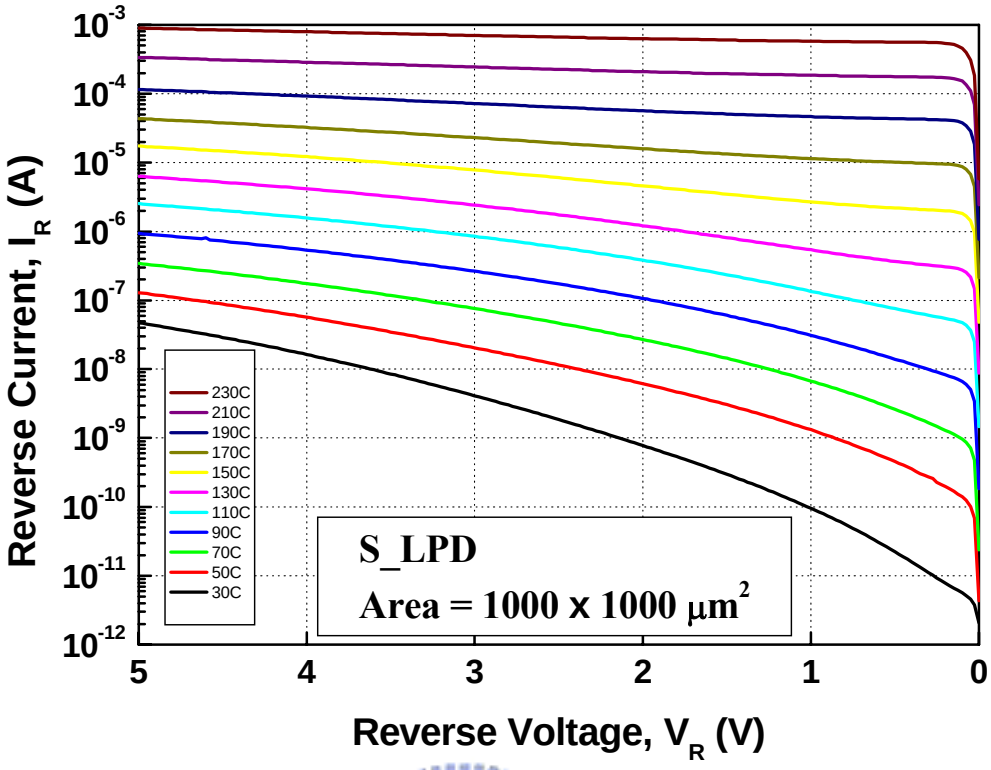
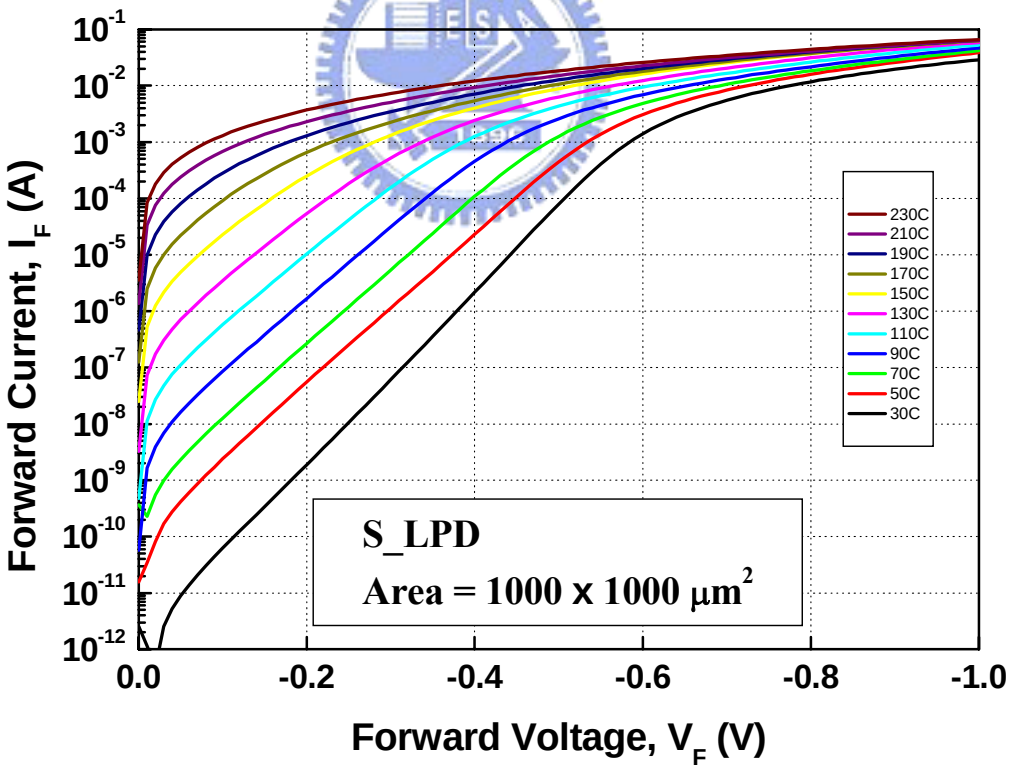


Fig. 5-19. The ideality factor distribution of n^+/p diodes for different contact-hole processes.

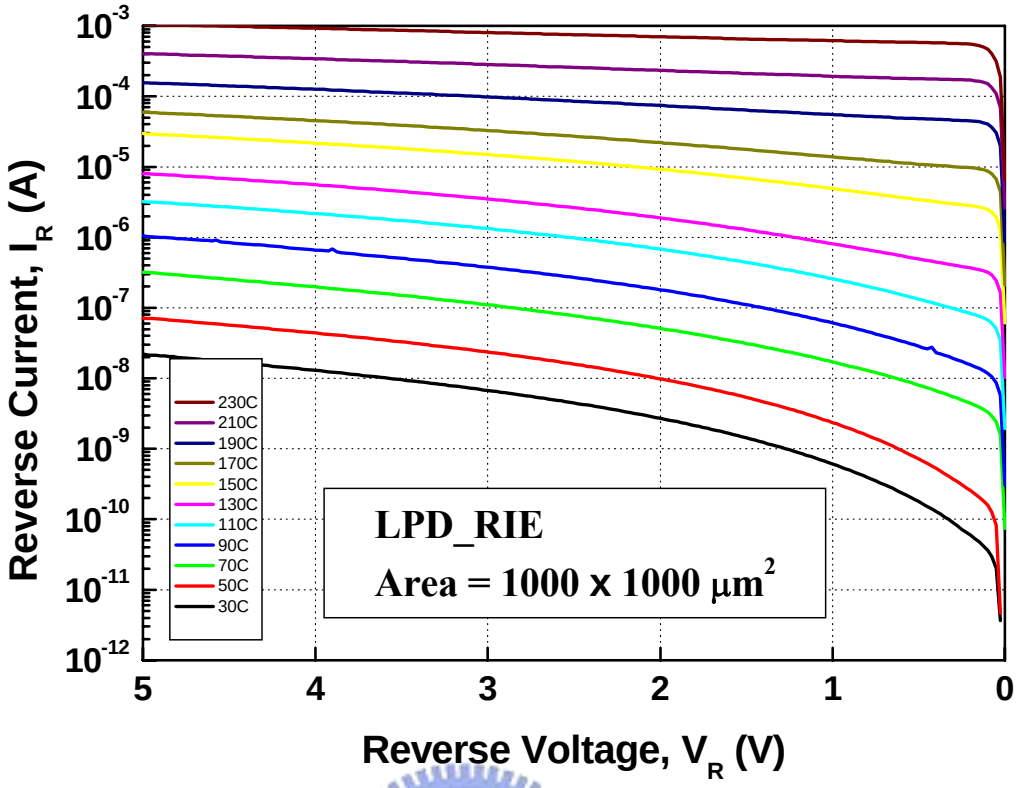


(a)

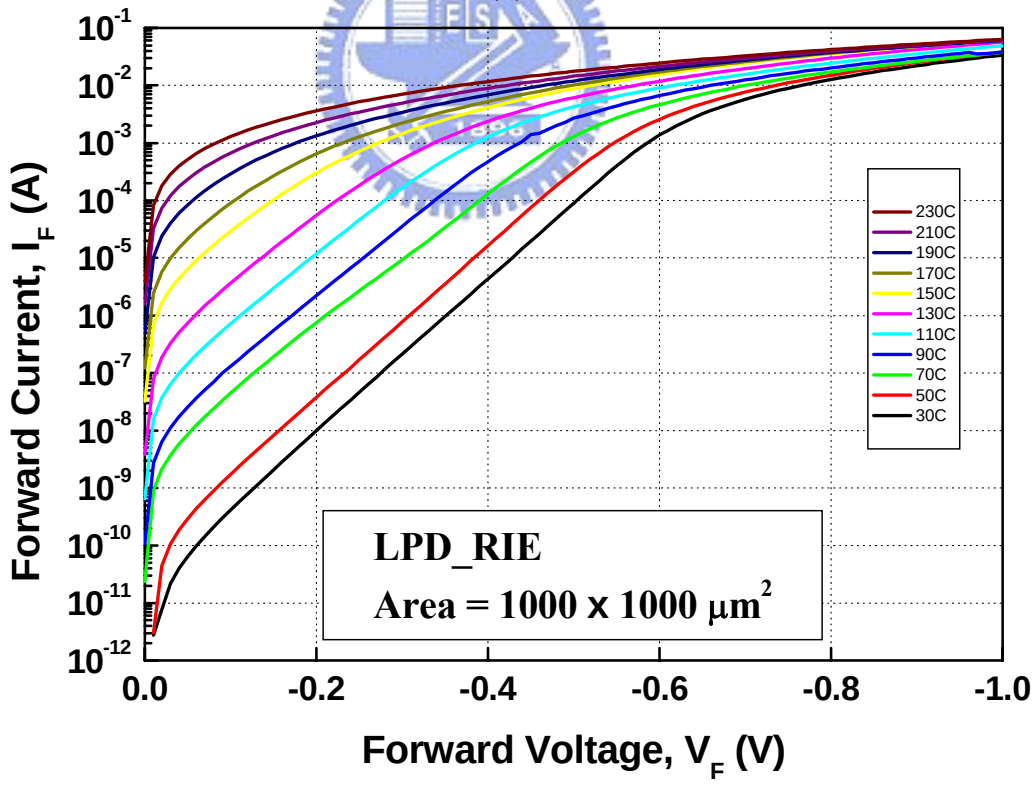


(b)

Fig. 5-20. The (a) Reverse and (b)Forward current-voltage characteristics of different temperature for S_LPD sample.

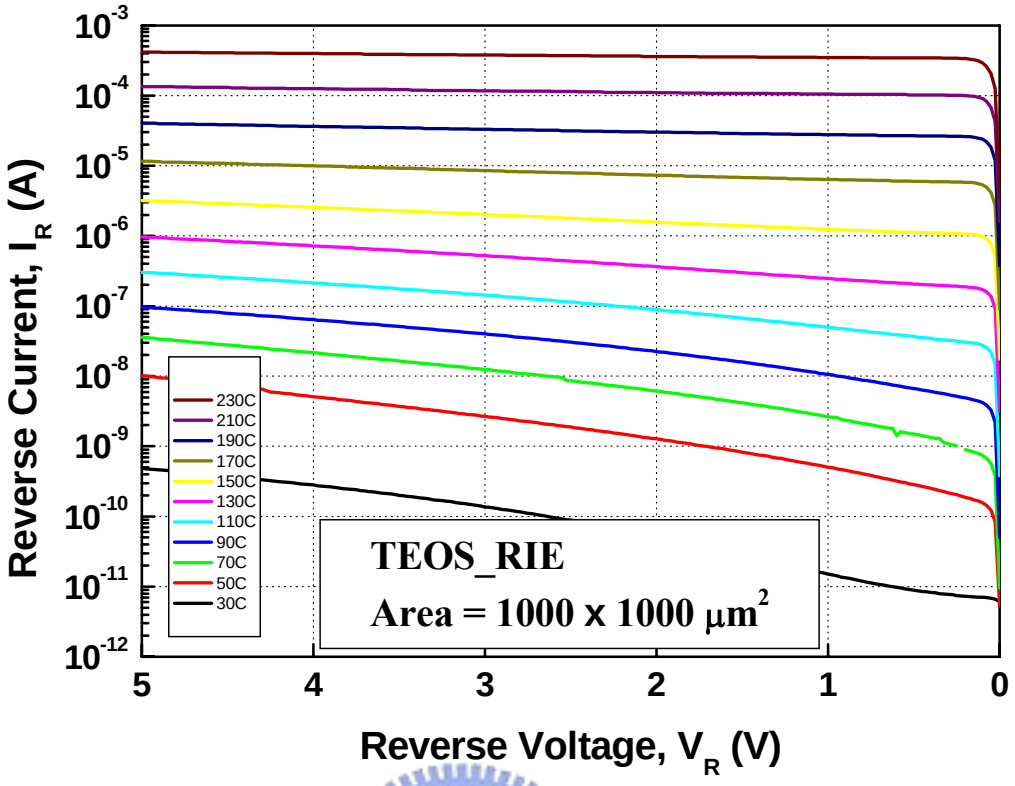


(a)

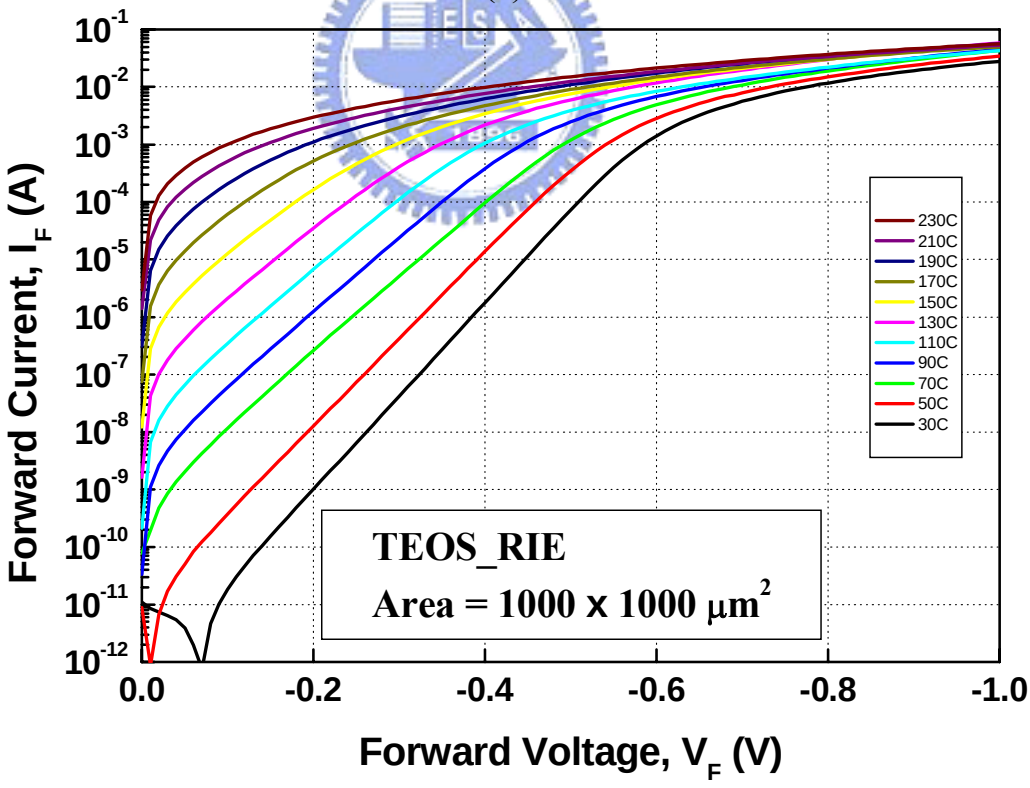


(b)

Fig. 5-21. The (a) Reverse and (b)Forward current-voltage characteristics of different temperature for LPD_RIE sample.

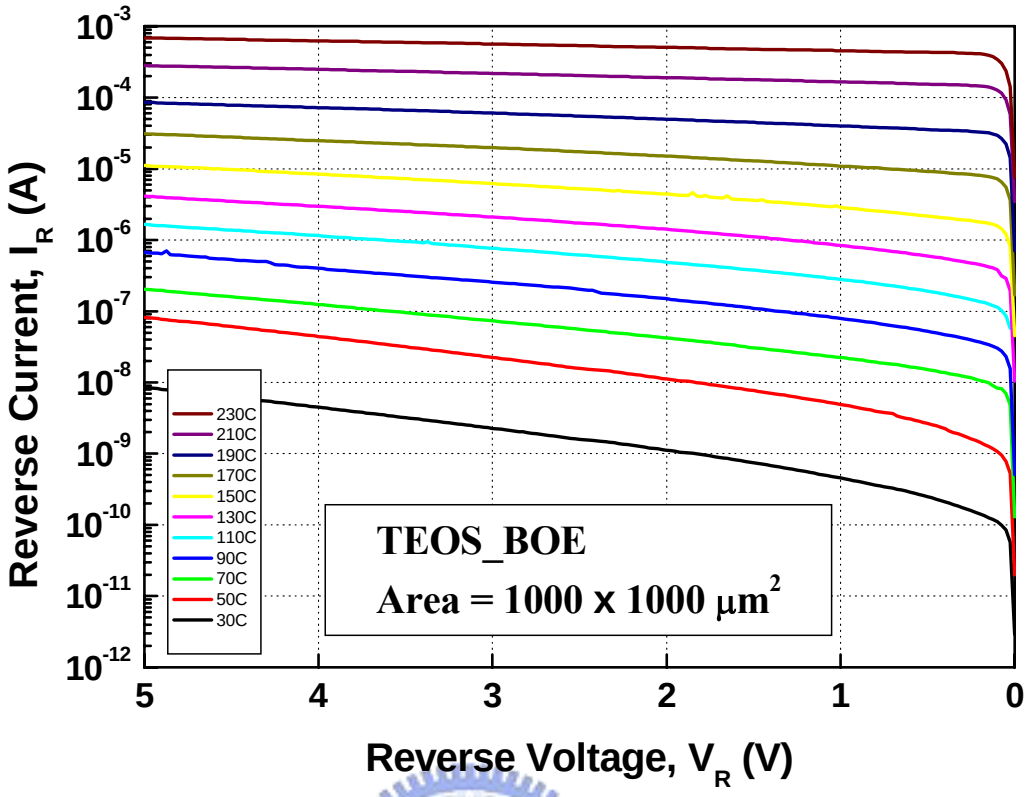


(a)

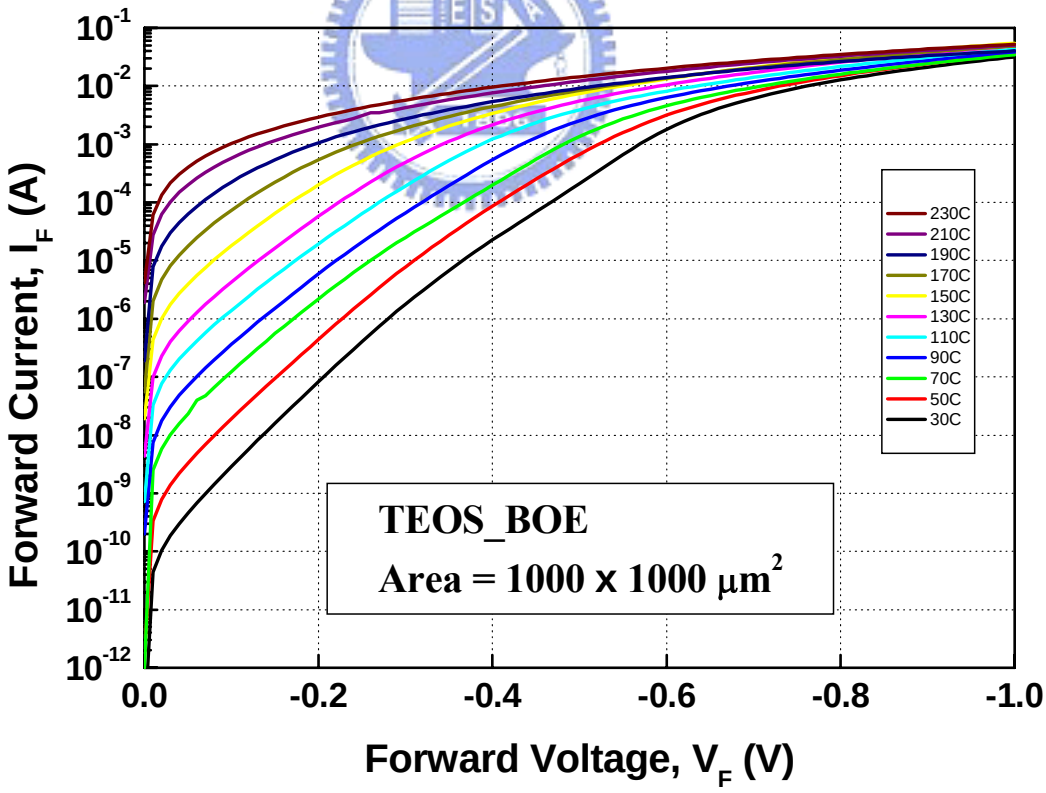


(b)

Fig. 5-22. The (a) Reverse and (b)Forward current-voltage characteristics of different temperature for TEOS_RIE sample.



(a)



(b)

Fig. 5-23. The (a) Reverse and (b)Forward current-voltage characteristics of different temperature for TEOS_BOE sample.

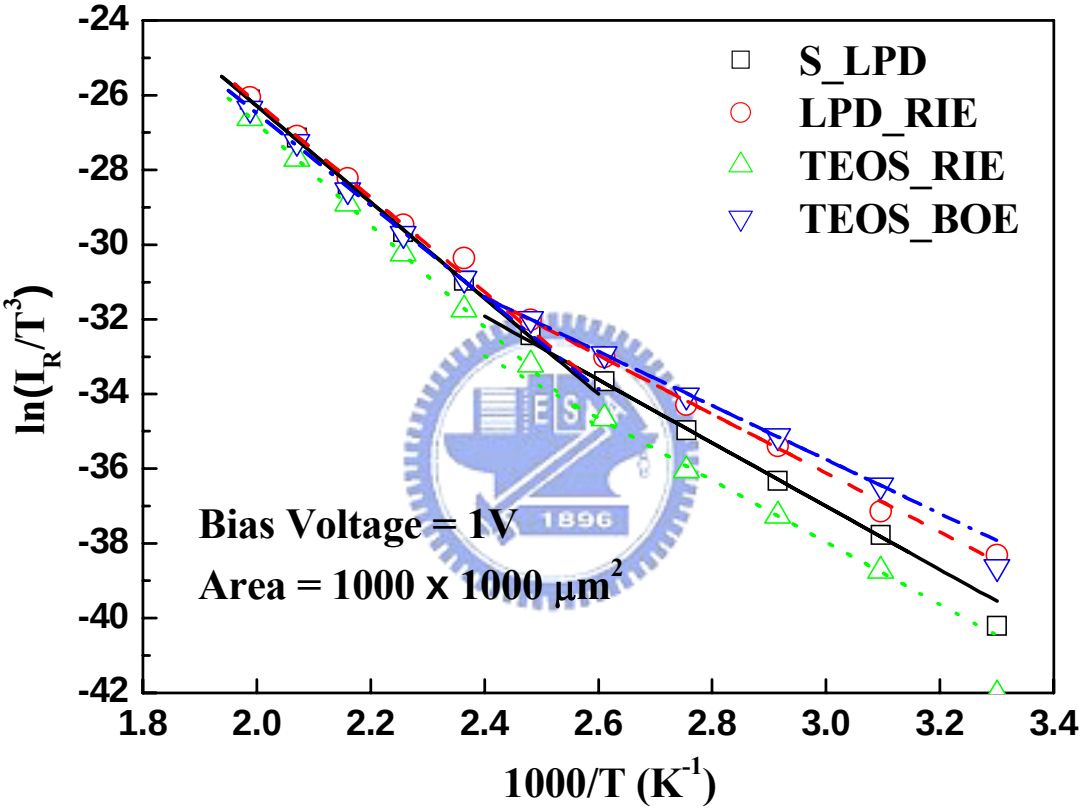


Fig. 5-24. The Arrhenius plot of diodes for different contact-hole processes.

CHAPTER 6

Conclusions and Future Works

6.1 CONCLUSIONS

In chapter 2, AMC in air and on the surfaces of wafers was quantitatively analyzed. Air sampling results reveal that a CB with chemical filters can only effectively remove inorganic ions, while one further equipped with a PTFE main filter can eliminate not only organic contaminations but also boron and metal. A CB with a GF filter still has a high concentration of D6. Wafer sampling results also demonstrate that each filter can, indeed, reduce the metal concentration to a level that corresponds to no exposure to air. Wafers exposed under a PTFE filter have less organic contaminations than those in the CR, but a GF filter shows high contamination of silicon-based organic D6, because of the binder used in the GF filter. In summary, the results obtained by air and wafer sampling are highly consistent. The effects of AMC on device performance were also investigated using a MOS capacitor. The samples exposed in the CB under the PTFE filter have nearly the same leakage current density and breakdown field distribution as the BLANK sample, implying that the exposed wafers have few defects and exhibit slight degradation of film quality. However, the samples in the CB under a GF filter suffer an obviously degraded breakdown field, leakage current density, and Q_{bd} because of high concentrations of organic compounds. All these results reveal that AMC will become an important issue in future nanodevice fabrication. An AMC-free manufacturing environment must be seriously considered when manufacturing nanodevices. Advanced ULPA filters, like the NEUROFINE PTFE filter combined with chemical filters, are excellent candidates for creating advanced manufacturing environments.

In chapter 3, the qualitative and quantitative analyses of AMC in the CB with different filter module in HF vapor environment were investigated. The experimental results showed that the GF ULPA filter will release boron and organic contaminants in HF vapor environment, while the PTFE ULPA filter still maintained low concentration of contaminants. The effects of the materials from which air filters are made on device characteristics were also investigated. The glass-fiber ULPA filter released AMC when exposed in an HF vapor environment. These contaminants included organic compounds and boron trace dopants and degraded the device characteristics. In contrast, the HF vapor did not affect the PTFE ULPA filter. These results suggested that the PTFE fiber can be a good ULPA filter material for providing a very clean cleanroom environment.

In chapter 4, the sheet resistances of NiSi on different silicon substrates were investigated. It was found that the NiSi formed with 200Å-thick nickel was stable and showed low sheet resistance between 400℃ and 650℃ RTA-1, and still stable after 700℃ RTA-2 for 30s on c-Si and apoly-Si. In the same experiment, the NiSi on poly-Si showed low sheet resistance below 600℃ RTA-1. After the SEM micrographs observation, the NiSi showed different surface morphology on poly-Si, a-Si, and apoly-Si. At the lower RTA temperature, the surface was uniform. As the dark spots or agglomeration appear with the increasing temperature, the sheet resistance of NiSi began to increase. At the higher RTA temperature, the micro-crack or agglomeration arose on the surface of NiSi on poly-Si and apoly-Si, which results in the higher sheet resistance. As for the research of the linewidth effects of NiSi sheet resistance on poly-Si, a-Si, and apoly-Si, it was found that the appearance of dark spots or agglomeration would affect the sheet resistance of NiSi seriously. For 600℃ RTA on poly-Si and apoly-Si, the sheet resistances of NiSi increase. Even so, it is more obvious with the narrower linewidth. It was observed that the behavior of NiSi sheet resistance at 600℃ RTA on a-Si is similar to that on apoly-Si. This is due to the effect of dopant activation at 1000℃

for 30s RTA. Due to the linewidth effects, the process window of NiSi RTA temperature was ranging from 400℃ to 550℃. In the last section of this chapter, the thermal stability of NiSi after the second RTA at the temperatures ranging from 500℃ to 800℃ for 30s was tested. NiSi on a-Si showed the best thermal stability. But for NiSi on c-Si, Ni will continuously diffuse and cause the sheet resistance to increase. Compared to the columnar poly silicon (poly-Si), the non-columnar poly silicon (apoly-Si) is more stable in the same thermal treatment.

In chapter 5, the optimum process condition of ultra-shallow junction n^+/p diode with nickel silicide has been found out in work. It was found that the leakage current increases with the increasing of nickel thickness. This phenomenon resulted from the approach of nickel silicide to junction depletion region. It was also found that the leakage current decreases with the increasing silicide formation temperature. This is due to the complete formation of nickel silicide. The new S_LPD process for contact-hole formation was also developed in this study. This technology was performed under a non-plasma environment. From the experimental results, S_LPD technology showed the lowest ideality factor and highest barrier height for Schottky diode. On the contrary, TEOS_RIE with the PECVD oxide deposition and RIE etching showed the poorest characteristics. For the ultra-shallow junction n^+/p diode, the electrical characteristics including current-voltage curve, ideality factor and effective energy gap did not show obvious difference. From the results of Schottky diode and n^+/p diode, it was suggested that the plasma damage may influence the junction depth between 500Å to 1000Å. This indicated that the sub-100nm device with the junction depth below 1000Å may be affected by the plasma damage including PECVD, RIE and so on. According to above mentioned, it is believed the S_LPD technology will be the promising technology for future advanced device fabrication.

6.2 SUGGESTIONS FOR FUTURE WORK

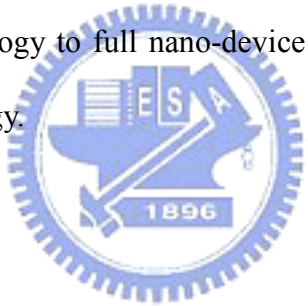
The effects of AMC and plasma process on the device performance have been studied. These studies, however, mainly focused on the individual process step. As for the development of nano-device, these studies should be considered in the complete device fabrication. Suggestions for future work are list as follows:

(1) Full nano-device processes are suggested to use for the complete study of AMC on device characteristics.

(2) The reliability study of nano-device influenced by the AMC.

(3) Physical and chemical studies of the effect of plasma process to nano-device.

(4) The use of S_LPD technology to full nano-device fabrication and the reliability test for this improvement technology.



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微污染與電漿製程對奈米電晶體元件特性影響之研究及其改善方法之研發

Study on the Effects of Microcontamination and Plasma Process to Nano-Device Characteristics and the Development of Improvement Methods

PUBLICATION LIST

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1. Ching-Fa Yeh, Chih-Wen Hsiao, Wen-Shan Lee, "Novel post CMP cleaning using buffered HF solution and ozone water," *Applied Surface Science*, Vol. 216, Issue: 1-4, pp. 46-53, Jun. 2003.
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