國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

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靜電放電防護電路設計

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摘要

隨著半導體製程的進步與發展，許多整合多功能的系統晶片已經成為各電子公司的產品研發主力，奈米電子時代的來臨提供積體電路更廣泛的設計平臺及更為前瞻的技術。許多積體電路產品已經使用奈米半導體製程技術進行量產，但其積體電路可靠度可能會成為奈米半導體製程中更需要考慮的問題，其中靜電放電(Electrostatic Discharge, ESD)防護已成為其中一個重要的可靠度指標。先進的奈米半導體製程雖然能有效地微縮元件尺寸進而提升電路運算效率，在半導體元件本身的特性卻會因尺寸過小產生許多微米製程中不需考慮之影響，如閘極透納電流(Gate Direct Tunneling Current)會產生嚴重的漏電而降低晶片的效能。因此在奈米製程中，全晶片靜電放電防護設計需達到高效率、高防護能力及低漏電流之特性。另一方面，由於晶片的操作電壓隨著製程演進持續下降以符合元件閘極氧化層可靠度及低功率消耗之需求，但是周邊電路的電壓卻未隨半導體製程的進步而降低，所以在扮演晶片輸入輸出媒介的混合電壓界面(Mixed-Voltage I/O Interface)上將會產生許多問題。因此要在此混合電壓電路加上其靜電放電保護電路，考量界面電壓轉換及可靠度等問題，如何仔細評估這些問題而設計出具有高的靜電放電防護能力的電路將是當今以及未來積體電路設計

上的重要課題，隨著半導體製程進入奈米級製程之後，對積體電路設計產業更加重要。另外，隨著高壓功率積體電路製程(Bipolar-CMOS-DMOS, BCD)在面版驅動電路、電源供應器及電源管理等使用的普及化，對於使用在這些應用的輸出端以及當作靜電放電保護元件的高壓電晶體來說，其高觸發電壓及低持有電壓的特性將使得高壓積體電路的靜電放電防護能力不足，並有可能產生閉鎖效應(Latchup)或類似閉鎖效應(Latchup-Like)的危險。因此如何開發有效的靜電放電防護設計，將是這些高壓積體電路設計上很重要的課題，這個主題也隨著這些產業應用上的多元化而更趨重要。所以本論文分別針對了奈米製程應用、混合電壓界面電路以及高壓功率積體製程應用上的限制與困難作討論，並進一步設計出有效的靜電放電防護電路以適用在各相關應用之積體電路晶片。

為了提供適用於奈米製程，具低漏電的全晶片靜電放電防護設計，本論文提出一新型靜電放電箝制電路，利用矽控整流器(Silicon Controlled Rectifier, SCR)作為靜電放電保護元件，及靜電放電偵測電路採取基體觸發(Substrate Triggered)技術來提昇其靜電放電防護能力。矽控整流器不具有閘極氧化層可有效避免閘極透納電流。且在考量閘極電流存在的操作情況下，此新型靜電放電偵測電路可在正常工作時有效地降低其漏電流，此靜電放電防護電路已在 65 奈米互補式金氧半製程中實際被製作與驗證。其人體放電模式(Human-Body-Model, HBM)及機器放電模式(Machine-Model, MM)的靜電放電耐受能力可以達到 7kV 及 325V，於室溫在 1V 工作電壓下，其漏電流僅 96nA。

為了提供有效的靜電放電防護電路於奈米製程下高低壓共容輸入輸出電路，本論文提出可耐高工作電壓之靜電放電箝制電路，用來保護可接受兩倍工作電壓訊號之共容輸出輸入電路。此可耐高工作電壓之靜電放電箝制電路利用低壓薄閘極氧化層元件來實現，並納入閘極電流作為低漏電流設計之重點。利用靜電放電匯流排及可耐高工作電壓之靜電放電箝制電路可有效地排放各種放電組合之靜電放電電流，以保護高低壓共容輸入輸出

電路。此適用於 1V/1.8V 高低壓共容輸入輸出電路新型電路已在 65 奈米互補式金氧半製程中實際被製作與驗證。

為了應用於高整合度之積體電路系統中，利用 N 型金氧半場效電晶體(NMOS)阻隔的技巧之高低壓共容輸入輸出電路被設計用來接受三倍、四倍甚至五倍的操作電壓，本論文提出兩個利用低電壓元件所實現的可耐受三倍工作電壓之靜電放電防護設計，透過不同的設計概念達到基體觸發之效用，提供有效的觸發電流，以提升防護元件之靜電放電耐受能力。本論文所提出應用在 1.2V/3.3V 高低壓共容輸出入界面之靜電放電防護設計已經在 130 奈米 1.2V 互補式金氧半製程下實現並已在 3.3V 的操作環境下驗證。

在高壓功率積體電路製程技術中，擴散式金氧半電晶體(DMOS)被廣泛地使用於靜電放電防護元件。本論文以擴散式金氧半電晶體為基礎提出新型的靜電放電防護電路以提升防護元件之導通效能及靜電放電耐受度。在正常電路操作時，擴散式金氧半電晶體可偏壓於 40V 而其 5V 閘極氧化層不會受到可靠度問題，另一方面此電路可進一步設計以避免高壓積體電路發生閉鎖效應或類似閉鎖效應的危險。此電路已在 0.35 微米 5-V/40-V 高壓功率積體電路製程中實際被製作與驗證。

本論文分別針對了奈米金氧半導體製程特性、混合電壓界面電路以及高壓功率積體電路製程應用上的限制與困難作討論，並設計出低漏電、高效能、並且在正常工作時不會受到閉鎖效應危險的靜電放電防護電路，所設計的靜電放電防護電路均已在實際晶片上成功驗證，並有相對應的國際期刊論文發表與專利申請。

LOW-LEAKAGE POWER-RAIL ESD PROTECTION DESIGNS IN CMOS INTEGRATED CIRCUITS

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Abstract

Continually scaling down the CMOS technologies into nanoscale generation imposes significant challenges in integrated circuit (IC) reliability, where electrostatic discharge (ESD) protection has become one of the major concerns. To meet such reliability specifications are necessary for IC product qualification. From the perspective of ESD, the similar gate oxide breakdown voltage and trigger voltage of MOSFET devices increased the design difficulty. Moreover, the secondary device characteristics of MOSFET have been considered in nanoscale CMOS generations. The most important impact for ESD is the gate direct tunneling current, which happens between the gate and silicon beneath the gate oxide, occurs while MOSFET implementing in a nanoscale CMOS process. Such gate tunneling current could induce a substantial fraction of overall leakage current in a chip. The traditional ESD protection circuit with a large gate oxide dimension suffers serious gate leakage issue. The on-chip ESD protection circuit in nanoscale CMOS process should be design with consideration of gate tunneling current to achieve a low standby leakage current during the normal circuit operation condition. During the ESD stress, the on-chip ESD protection circuit should provide efficient protection capability to assure the safety of the internal circuit which has a small gate oxide breakdown voltage in nanoscale CMOS process. For the mixed-voltage I/O interfaces with thin gate-oxide devices, the on-chip ESD protection

designs will meet design difficulties, such as gate-oxide reliability constraints and undesired leakage current paths. In high-voltage Bipolar-CMOS-DMOS (BCD) technology, high-voltage transistors have been widely used for display driver ICs, power supplies, and power management ICs. The high-trigger-voltage and low-holding-voltage characteristics of HV transistor have been found to cause latchup or latchup-like failure and insufficient ESD efficiency. Therefore, how to develop an efficient on-chip ESD protection design is an important challenge for high-voltage IC products. In this dissertation, the ESD design constraints in nanoscale CMOS process, mixed-voltage I/O interfaces, and high-voltage CDMOS technology are presented. Furthermore, the novel design solutions for on-chip ESD protection circuit have been developed to meet the design constraints in such technologies and applications.

To provide effective on-chip ESD protection with low standby leakage current in nanoscale CMOS technology, a new power-rail ESD clamp circuit by using the silicon controlled rectifier (SCR) device and ESD detection circuit with substrate-triggered technique is proposed. The SCR device without poly-gate structure has good immunity against the gate leakage current. The special ESD detection circuit is designed with consideration of gate current to reduce the standby leakage current. The new proposed design has been fabricated and verified in a 65nm fully-silicided CMOS process. The new proposed power-rail ESD clamp circuit can achieve 7kV in human-body-model (HBM) and 325V in machine-model (MM) ESD levels while consuming only a standby leakage current of 96nA at room temperature under 1-V bias.

In order to protect the mixed-voltage I/O interfaces in nanoscale CMOS technology, a new high-voltage-tolerant ESD clamp circuit is proposed to protect the mixed-voltage I/O circuits for receiving signals with 2×VDD voltage level. The devices used in the high-voltage-tolerant ESD protection design are all low-voltage thin gate-oxide devices. The gate current of each thin gate devices in the high-voltage-tolerant ESD detection circuit has also been considered. By using the ESD protection scheme with the ESD bus and the proposed high-voltage-tolerant ESD clamp circuit, the mixed-voltage I/O circuit can be well protected. The new proposed circuit has been fabricated in a 1-V 65-nm CMOS process for experimental verification.

In high integrated electronic system, the mixed-voltage I/O design with NMOS blocking technique is applied for receiving 3×VDD, 4×VDD, and even 5×VDD input signals without

the gate-oxide reliability issue. In this dissertation, two new ESD protection design by using only 1×VDD low-voltage devices for mixed-voltage I/O buffer with 3×VDD input tolerance are proposed. Two different special high-voltage-tolerant ESD detection circuits are designed with substrate-triggered technique to improve ESD protection efficiency of ESD clamp device. These two ESD detection circuits with different design concepts both have effective driving capability to trigger the ESD clamp device on. These ESD protection designs have been successfully verified in two different 130nm 1.2-V CMOS processes to provide excellent on-chip ESD protection for 1.2-V/3.3-V mixed-voltage I/O buffers.

In high voltage CDMOS technology, the high-voltage DMOS is widely used as on-chip ESD protection devices. The trigger voltage of the high-voltage devices is too high to protect the output buffer. Such characteristics will cause the high-voltage DMOS susceptible to the latchup or ESD danger in the practical applications. To greatly improve ESD performance of the high-voltage DMOS devices, gate-driven and substrate-triggered circuit techniques are applied. The proposed gate-driven and substrate-triggered ESD protection circuits have been successfully verified in a 0.35-μm 5V/40V bipolar CMOS DMOS (BCD) process. In addition, the power-rail ESD protection design can be also achieved with stacked structure to protect 40-V power pins without latchup issue in the smart power ICs.

In this dissertation, the novel ESD protection circuits have been developed for nanoscale CMOS process, mixed-voltage I/O interfaces and high-voltage BCD process with high ESD robustness. Each of the ESD protection circuits has been successfully verified in the testchips. The proposed ESD protection circuits in this dissertation can achieve the benefits of low standby leakage current, high ESD performance, and latchup-free characteristics for whole chip ESD design in CMOS ICs.

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王　暢　資
謹誌於竹塹交大
九十九年　五月

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Chapter 1

Introduction

In this chapter, the background of this dissertation is discussed. First, the gate direct tunneling current in nanoscale fully-silicided complementary metal-oxide-semiconductor (CMOS) processes are discussed. Then, the issue of electrostatic discharge (ESD) protection and mixed-voltage I/O interface realized in low-voltage CMOS process are introduced. Finally, the rest of this dissertation is organized.

1.1 Gate Direct Tunneling Current in Nanoscale CMOS

Improvement in circuit performance of operating frequency and density of the CMOS integrated circuits (IC) for aggressive device scaling with gate lengths down into nanoscale regime. Aggressive scaling of CMOS technology has reduced the SiO_2 gate dielectric thickness below 3nm. Major causes for concern in further reduction of oxide thickness include increased poly-silicon gate depletion, boron penetration into the channel region, and high direct tunneling gate leakage current which leads to questions regarding dielectric integrity, reliability, and standby power consumption. According to the International Technological Roadmap for Semiconductors (ITRS), gate oxide thicknesses of 1.2–1.5 nm have been required in 2004 for sub-100-nm CMOS. For such an ultrathin gate oxide, direct tunneling current will dominate the gate leakage current and the off-state power dissipation of the transistor [1]-[2]. For the transistors in conventional CMOS process, the dominant leakage mechanism is mainly due to short channel effects owing to drain-induced barrier lowering (DIBL). However, in the ultrathin gate oxide transistors, the gate leakage current could contribute to standby leakage current significantly, which may result in faulty circuit operation since designers may assume that there is no appreciable gate current.

1.1.1 Gate Current in N/P-Type MOSFET Devices

The gate current arises due to the finite probability of an electron directly tunneling through the insulating SiO_2 layer. The amount of the gate current is a strong exponential

function of the gate oxide thickness as well as the voltage potential across the gate oxide. A difference in gate oxide thickness of 0.2nm can result in an order of magnitude change in the gate current, making it the most sensitive parameter with respect to any physical dimensions. Even the gate oxides can be well controlled (within ±4% in general), as compared to other device dimensions (such as effective channel length or width of metal line), this significant sensitivity makes serious variation in the gate current among different dies in the same wafer. Another key point is that the gate current of a PMOS device is typically one order of magnitude smaller than that of an NMOS device, under the identical gate oxide thickness and voltage potential across the gate oxide[3]-[4]. This is due to the much higher energy required for hole tunneling in SiO_2 and the fact that there are very few electrons associated with a PMOS device. However, in alternate dielectric materials the energy required for electron and hole tunneling can be completely different. In the case of nitrided gate oxides, in use today in some processes, the gate current of the PMOS can actually exceed that of the NMOS depending on the nitrogen concentration (higher nitrogen content increases the gate current of the PMOS relative to the NMOS) [5]-[6].

1.1.2 Modeling of Gate Direct Tunneling Current

Direct tunneling of the conduction band electron from inversion or accumulation layers has been extensively studied [7]-[9]. As for p+ polysilicon gate p-MOSFETs, direct tunneling hole was found to dominate the gate current under channel inversion conditions [10]-[11]. The direct tunneling current appearing between the source–drain extension (SDE) and the gate overlap, so-called the edge direct tunneling (EDT), dominates off-state drive current, especially in very short channel devices [12], [13].

Gate direct tunneling current is produced by the quantum-mechanical wave function of a charged carrier through the gate oxide potential barrier into the gate, which depends not only on the device structure but also bias conditions. The various gate tunneling components in a scaled NMOSFET are illustrated in Fig. 1.1. The gate-to-channel current (*Igc*), the gate-to-bulk current (*Igb*), and the EDT currents (*Igs* and *Igd*) are shown. In long-channel devices, *Igs* and *Igd* are less important than *Igc* because the gate overlap length is small compared to the channel length. In very short channel devices, the portion of the gate overlap compared to the total gate length becomes larger.

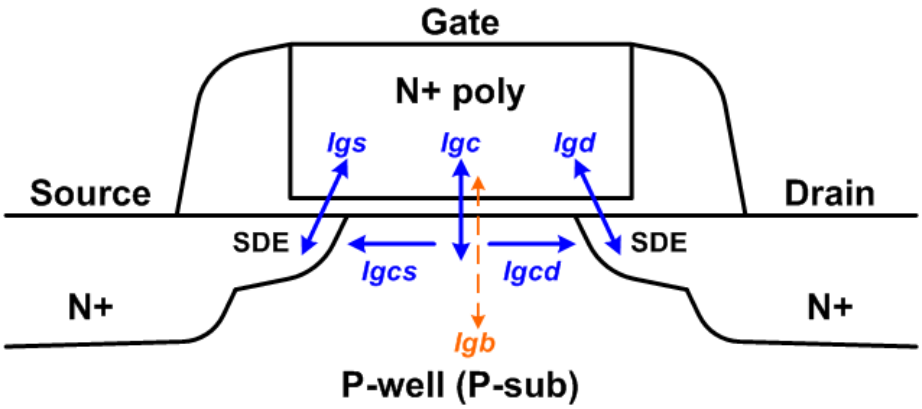


Fig. 1.1 Illustration of gate direct tunneling components of a very short-channel NMOSFET. (*Igs* and *Igd* are EDT currents)

Fig. 1.2 illustrates the band diagrams and electron tunneling directions along the gate-to-channel and gate-to-SDE directions for a highly doped drain (HDD) NMOSFET. For Vg > 0V, the gate-to-channel tunneling current (*Igc*) is the dominant current component, since a higher gate oxide voltage (V_{ox}) appears between the gate and the channel, as shown in Fig. 1.2(a). Here, the V_{fb} of an NMOSFET with an n-type polysilicon gate (i.e., n+ poly/SiO2 /p-substrate) is approximately -1V, while the V_{fb} along the gate-to-SDE (i.e., n+ poly/SiO2 /n+ SDE) is approximately 0 V. On the contrary, the EDT currents (*Igs* and *Igd*) can become dominant for bias conditions of V_{fb} < Vg < 0V. For the gate-to-SDE case, electrons accumulated in the n+ poly gate tunnel to the SDE region can lead to an appreciable off-state current. Meanwhile, operating in the depletion mode along the n+ poly/SiO2/p-substrate surface, few electrons are present in the channel that can in turn tunnel into the gate, as shown in Fig. 1.2(b). Such gate currents in ultrathin oxide transistors have been modeled in BSIM4 MOSFET model [14].

In BSIM4 model, the oxide voltage V_{ox} is written as

$$V_{ox} = V_{oxacc} + V_{oxdepinv}, \tag{1.1}$$

$$V_{oxacc} = V_{fbzb} + V_{FBeff}, \tag{1.2}$$

$$V_{oxdepinv} = K_{1ox}\sqrt{\Phi_s} + V_{gsteff}, \tag{1.3}$$

where V_{oxacc} and $V_{oxdepinv}$ are the oxide voltages in accumulation and in inversion (depletion), respectively. The components of gate tunneling current include the tunneling current between gate and bulk (*Igb*), the current between gate and channel (*Igc*), and the current between gate

and source/drain diffusion regions (*Igs* and *Igd*). The gate-to-bulk current is partitioned into two components for the MOSFET in accumulation (*Igbacc*) and in inversion (*Igbinv*). *Igbacc* and *Igbinv* are given by

$$Igbacc = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gb} \cdot V_{aux\_Igbacc} \cdot \exp\left[-B \cdot TOXE(AIGBACC - BIGBACC \cdot V_{oxacc}) \cdot (1 + CIGBACC \cdot V_{oxacc})\right], \text{ and} \quad (1.4)$$

$$Igbinv = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gb} \cdot V_{aux\_Igbinv} \cdot \exp\left[-B \cdot TOXE(AIGBINV - BIGBINV \cdot V_{oxdepinv}) \cdot (1 + CIGBINV \cdot V_{oxdepinv})\right]. \quad (1.5)$$

The current between gate-to-source/drain diffusion regions are given by

$$Igs = W_{eff} DLCIG \cdot A \cdot T_{oxRatioEdge} \cdot V_{gs} \cdot V_{gs}' \cdot \exp\left[-B \cdot TOXE \cdot POXEDGE(AIGSD - BIGSD \cdot V_{gs}') \cdot (1 + CIGSD \cdot V_{gs}')\right], \text{ and} \quad (1.6)$$

$$Igd = W_{eff} DLCIG \cdot A \cdot T_{oxRatioEdge} \cdot V_{gd} \cdot V_{gd}' \cdot \exp\left[-B \cdot TOXE \cdot POXEDGE(AIGSD - BIGSD \cdot V_{gd}') \cdot (1 + CIGSD \cdot V_{gd}')\right]. \quad (1.7)$$

The gate-to-channel current is formulated as

$$Igc = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gse} \cdot V_{aux\_Igc} \cdot \exp\left[-B \cdot TOXE(AIGC - BIGC \cdot V_{oxdepinv}) \cdot (1 + CIGC \cdot V_{oxdepinv})\right]. \quad (1.8)$$

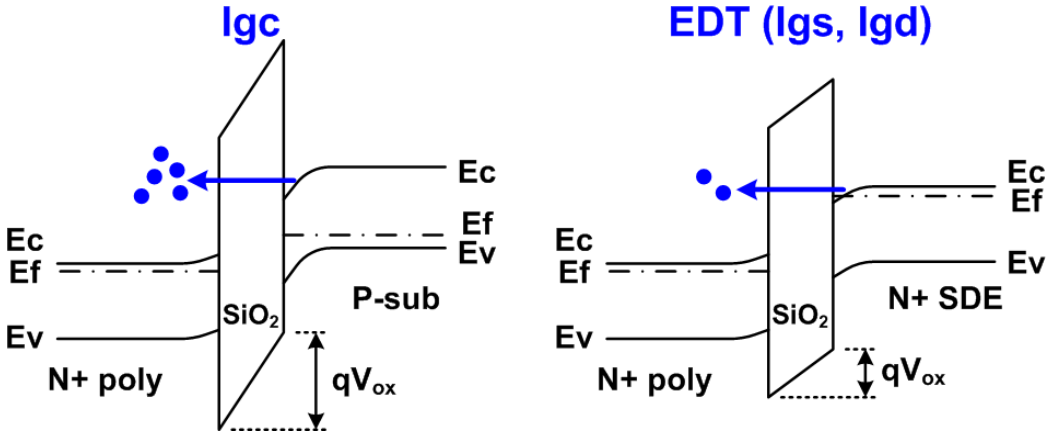
With consideration of drain bias effect, *Igc* has been partitioned into two parts as *Igcs* and *Igcd*, which are expressed as

$$Igcs = Igc0 \cdot \frac{PIGCD \cdot V_{dseff} + \exp(-PIGCD \cdot V_{dseff}) - 1 + 1 \times 10^{-4}}{PIGCD^2 \cdot V_{dseff}^{\ 2} + 2 \times 10^{-4}}, \text{ and} \quad (1.9)$$

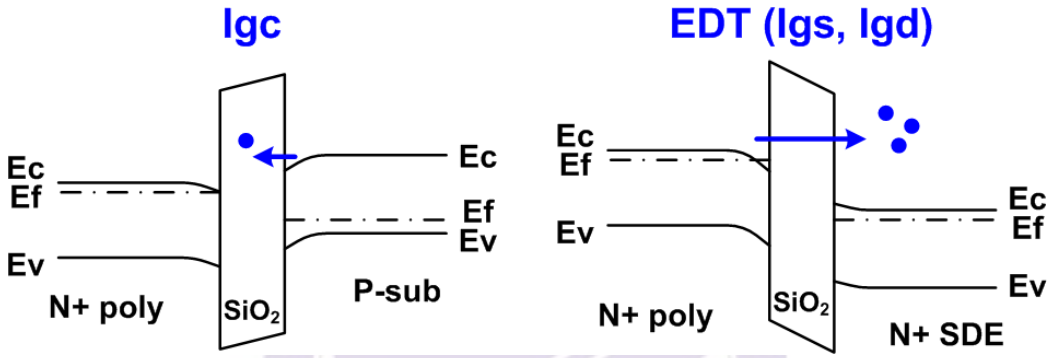
$$Igcd = Igc0 \cdot \frac{1 - (PIGCD \cdot V_{dseff} + 1) \cdot \exp(-PIGCD \cdot V_{dseff}) + 1 \times 10^{-4}}{PIGCD^2 \cdot V_{dseff}^{\ 2} + 2 \times 10^{-4}}, \quad (1.10)$$

where *Igc*0 equals *Igc* at *Vds* of 0V.

From equations (1.4)-(1.8), the main parameters of a MOSFET that dominate the gate current include the effective channel width, channel length, and the voltage difference between the gate and the other terminals.



(a) Vg > 0 V



(b) V_{fb} < Vg < 0 V

Fig. 1.2 Gate bias dependent band diagrams and electron tunneling in the channel (Igc) and the gate edge (Igs and Igd). (a) Vg > 0 V (inversion mode). (b) V_{fb} < Vg < 0 V (depletion mode).

1.2 Background of ESD Protection

ESD failure has become the main reliability concern on semiconductor products, especially for the system-on-a-chip (SOC) implementation in nanoscale CMOS processes. Common ESD failures are destructive, leading to immediate malfunction of ICs caused by either thermal breakdown in silicon and/or metal interconnects due to high-current transient or dielectric breakdown in gate oxide due to high-voltage overstress [15]. To sustain reasonable ESD robustness in nanoscale CMOS IC's, on-chip ESD protection circuits must be added into the chips. ESD specification of commercial IC products are required to be higher than 2kV in human-body-model (HBM) and 200V in machine-model (MM) ESD stress [16], [17]. According to the SESD standards, the ESD stress can be applied to any pin with another pin grounded in an IC. Therefore, on-chip ESD protection circuits have to be

designed and placed around the input, output, and power pads to provide efficient ESD protection in CMOS ICs against unexpected ESD damages in the internal circuits of CMOS ICs [18]–[24]. ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode), as shown in Figs. 1.3(a) ~ 1.3(d), respectively. For comprehensive ESD verification, the positive and negative VDD-to-VSS ESD stresses had also been specified to verify the whole-chip ESD robustness, which are shown in Figs. 1.4(a) and 1.4(b).

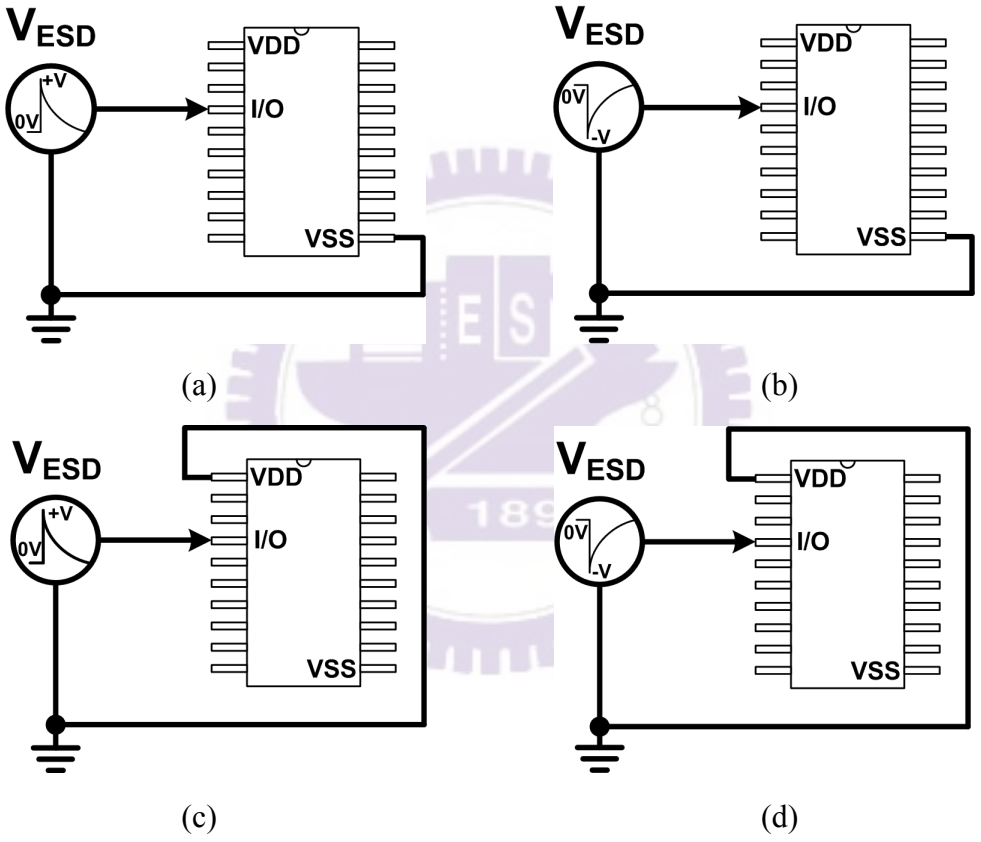
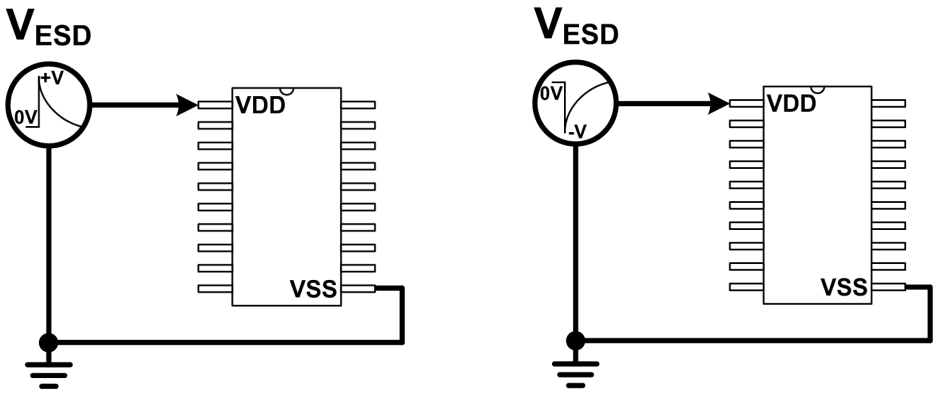


Fig. 1.3. The four pin-combination modes for ESD test on an IC product: (a) positive-to-VSS (PS-mode), (b) negative-to-VSS (NS-mode), (c) positive-to-VDD (PD-mode), and (d) negative-to-VDD (ND-mode).



(a) (b)

Fig. 1.4. VDD-to-VSS ESD tests: (a) positive mode, and (b) negative mode.

The typical design of on-chip ESD protection configuration, with efficient power-rail ESD clamp circuit between VDD and VSS power lines, in a CMOS IC is illustrated in Fig. 1.5 [24]. Such ESD protection scheme can be designed to meet the requirements for circuit operation of general purpose I/O while providing ESD immunity to the necessary ESD levels. The power-rail ESD clamp circuit is implemented by ESD clamp device (M_{ESD}) and a RC-based ESD detection circuit. The clamp device (M_{ESD}) can either operate in snapback or can be sized to conduct the ESD current through the channel. The elements R and C can be shared by numerous power-rail ESD clamp circuits in the whole-chip ESD protection design..

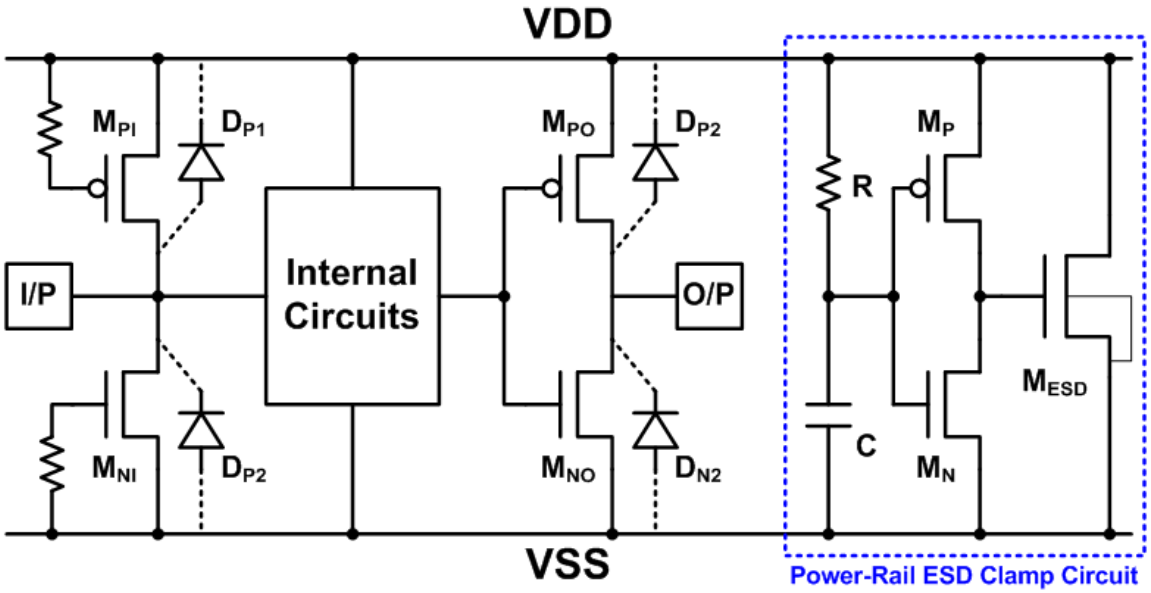


Fig. 1.5. Typical on-chip ESD protection scheme with power-rail ESD clamp circuit in a CMOS IC.

1.2.1 Issue of Mixed-Voltage I/O Interface

With the scaled-down device dimension in advanced CMOS technology, the power supply voltage is also scaled down to reduce the power consumption and to meet the gate-oxide reliability. Therefore, chip design quickly migrates to the lower voltage level with the advancement of the nanoscale CMOS technology. However, some peripheral components or other ICs in a microelectronic system are still operated at the higher voltage levels. In other words, an electronic system could have chips operated at different voltage levels. From the perspective of circuit design for whole system integration, the I/O buffers may drive or receive high-voltage signals to communicate with other ICs. Thus, some circuits must be design in low-voltage process, but still operated in the high-voltage or mixed-voltage (high-voltage and low-voltage) environments. Several problems arise in the I/O interface between these ICs, such as the gate-oxide breakdown [25]-[27] and the undesirable leakage current paths [28]. Fig. 1.6 shows the input and output stage of the traditional CMOS I/O buffer with VDD of 1V and 1-V gate oxide MOSFETs. When an external 1.8-V signal is applied to the I/O pad, the conducted channel of the pull-up PMOS and the parasitic drain-to-well junction diode in the pull-up PMOS will cause the leakage current paths from I/O pad to VDD, as the dashed lines shown in Fig. 1.6. Besides, the 1-V gate oxides of the pull-down NMOS in the output stage and the inverter in the input stage will be over-stressed by the 1.8-V input signal and then suffer the gate-oxide reliability problem.

To solve the gate-oxide reliability issue without using the additional thick gate-oxide process (called dual gate oxide in some CMOS processes), the stacked-NMOS configuration had been widely used in the mixed-voltage I/O buffer to reduce the process complexity and fabrication cost of the chip [29]–[35]. The typical 2×VDD-tolerant mixed-voltage I/O circuit (e.g. 1V/1.8V mixed-voltage I/O interface) is shown in Fig. 1.7. The gate of top NMOS in the stacked-NMOS device is biased at VDD (e.g. 1V in a 1V/1.8V mixed-voltage I/O interface), and the gate of bottom NMOS is biased by the pre-driver circuit. The independent control on the top and bottom gates of stacked-NMOS device allows the devices to meet reliability limitations during normal circuit operation with an input signals with 2×VDD voltage level (e.g. 1.8V in a 1V/1.8V mixed-voltage I/O interface). The gate tracking circuits and the N-well self-biased circuits are designed to ensure that the pull-up PMOS, between the I/O pad and the VDD power line, does not conduct current when the 1.8-V input signals enter the I/O pad. In such mixed-voltage I/O circuits, the on-chip ESD protection circuits will meet more design constraints and difficulty.

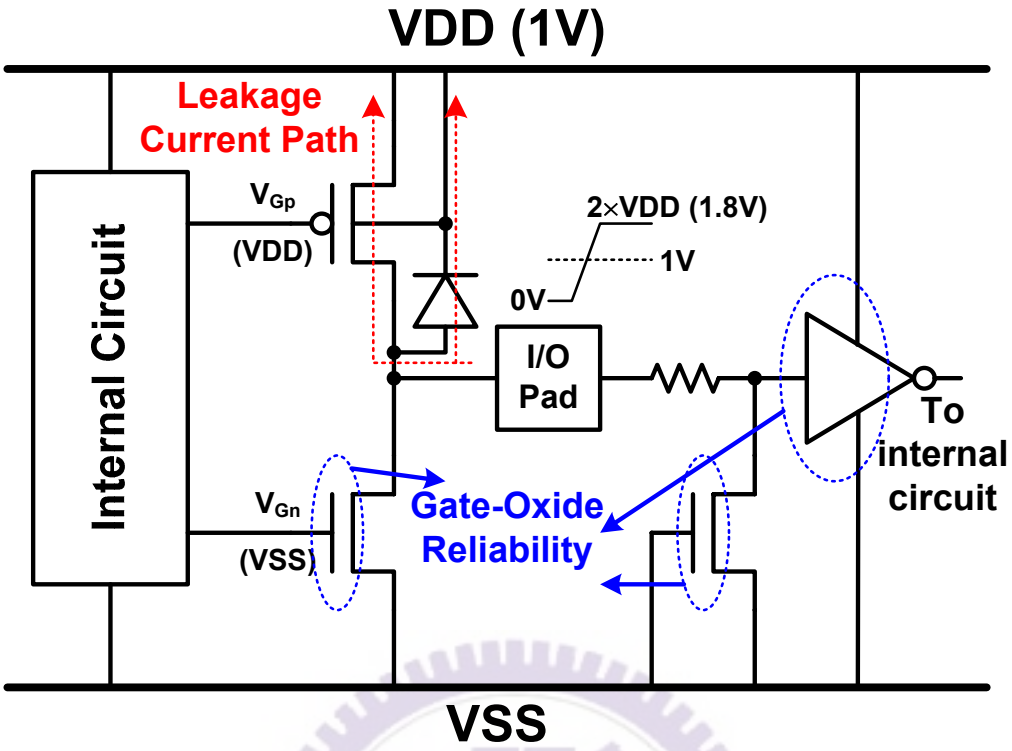


Fig. 1.6. Typical circuit diagrams for the traditional CMOS I/O buffer. The leakage current and the gate-oxide reliability appear while I/O pad receives 2×VDD input signals.

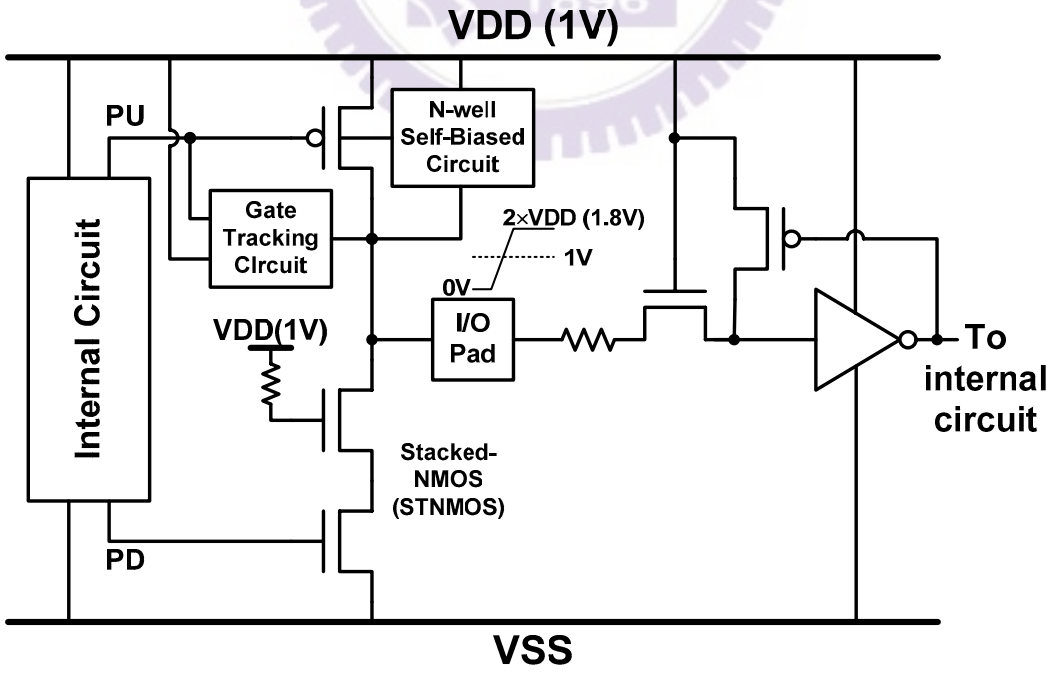
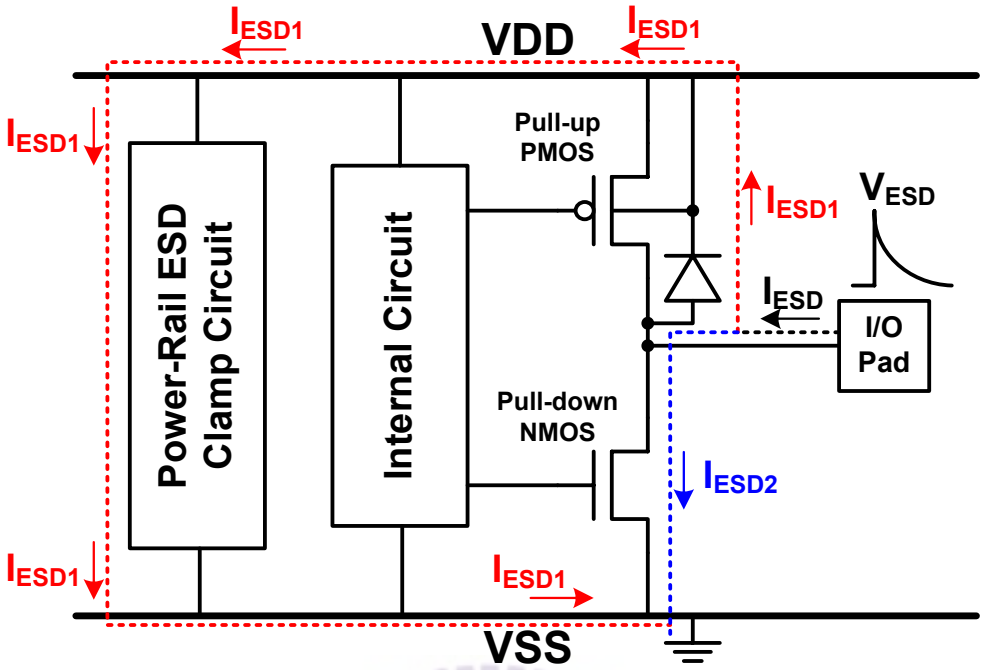
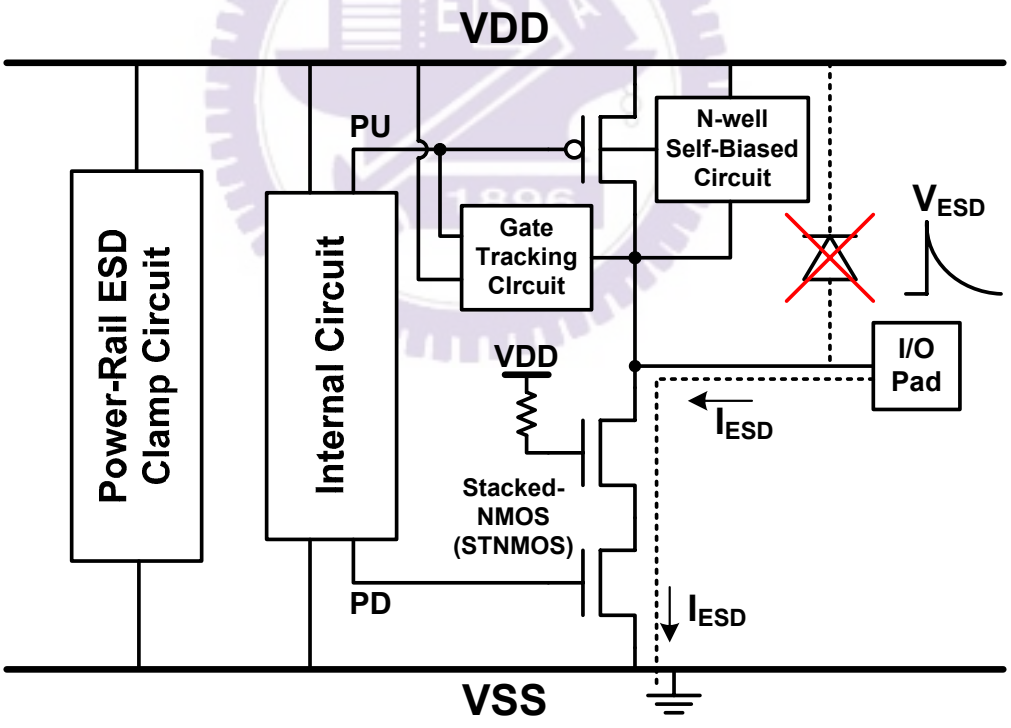


Fig. 1.7. Typical circuit diagrams for the mixed-voltage I/O circuits with the stacked NMOS and the N-well self-biased PMOS.

The ESD protection design of I/O pad cooperating with power-rail ESD clamp circuit for traditional I/O circuit and 2×VDD-tolerant mixed-voltage I/O circuit are shown in Fig. 1.8(a) and 1.8(b), where a PS-mode ESD pulse is applied to the I/O pad. In the traditional I/O circuit, the PS-mode ESD pulse can be discharged via two effective paths, as shown in Fig. 1.8(a). The one is through the NMOS in the output buffer by snapback breakdown. The other is through the parasitic diode of PMOS from I/O pad to VDD and power-rail ESD clamp circuit to VSS grounded. However, due to the leakage current issue in the mixed-voltage I/O circuits, there is no diode connected from the I/O pad to VDD power line in the mixed-voltage I/O circuits, as shown in Fig. 1.8(b). Without such diode connected from the I/O pad to VDD in the mixed-voltage I/O circuits, the ESD current at I/O pad under PS-mode ESD stress cannot be discharged from the I/O pad to VDD power line, and cannot be discharged through the additional VDD-to-VSS ESD clamp circuit. Therefore, the power-rail ESD clamp circuit did not help to pull up ESD level of the mixed-voltage I/O pad under the PS-mode ESD stress. In this situation, the ESD current at the I/O pad is mainly discharged through the stacked-NMOS by snapback breakdown. Besides, comparing the single NMOS and the stacked-NMOS in the high-current snapback region, the stacked-NMOS will have a higher trigger voltage, a higher snapback holding voltage, slower turn-on speed, and a lower secondary breakdown current. Therefore, such mixed-voltage I/O circuits with stacked-NMOS often have much lower ESD level under the PS-mode ESD stress, as compared to the traditional I/O circuits with a single NMOS [36], [37]. In addition, without the diode connected from the I/O pad to VDD, the mixed-voltage I/O circuit also has a lower ESD level for I/O pad under PD-mode ESD stress. The absence of the diode between I/O pad and VDD power line in the mixed-voltage I/O circuits will seriously degrade ESD performance of the I/O pad under the PS-mode and PD-mode ESD stresses. By using extra process modification such as ESD implantation, the ESD robustness of stacked-NMOS device can be further improved [38], [39], but the process complexity and fabrication cost are increased. In addition, the induced high voltage on the gate of top NMOS transistor under ESD stress will cause high-current crowding effect in the channel region to seriously degrade ESD robustness of stacked-NMOS device in the mixed-voltage I/O circuits [40]. Therefore, effective ESD protection design without increasing process complexity is strongly requested by the mixed-voltage I/O circuits in the scaled-down CMOS processes.



(a)



(b)

Fig. 1.8. The ESD current paths of (a) the traditional I/O pad with power-rail ESD clamp circuit, and (b) the mixed-voltage I/O pad with power-rail ESD clamp circuit, under the positive-to-VSS (PS-mode) ESD stress. The ESD current paths are indicated by the dashed lines.

1.2.2 Issue of High Voltage BCD ICs

High-voltage Bipolar-CMOS-DMOS (BCD) technology has been widely used in LCD driver circuits, telecommunication, power switch, motor control systems, etc [41]. In the smart-power technology, bipolar junction transistor, high-voltage CMOS, high-voltage lateral DMOS, and silicon controlled rectifier (SCR) device were used as on-chip ESD protection devices [42]–[50]. Some ESD protection designs used the lateral or vertical bipolar transistors as ESD protection devices in smart power technology [48]. However, fabrication cost and process complexity are increased by adding vertical bipolar modules into a high-voltage BCD process without epitaxial layer. With a thick gate oxide of several hundred angstroms, the high-voltage CMOS device, which can sustain high-voltage, was often used as the ESD protection device because it can work as both of output driver and ESD protection device simultaneously in the high-voltage ICs. With an ultra-high operating voltage, the ESD robustness of high-voltage CMOS device is quite weaker than that of low-voltage MOSFET. Moreover, the high-voltage lateral DMOS device with a thin gate oxide to gain the small turn-on resistance and driving capability was usually implemented with several hundred thousand micrometers as the large-sized output buffer in some applications, such as DC-DC converters, and class-D amplifier. In this case, an additional efficient ESD protection device should be placed in parallel with the output buffer. Besides, such ESD protection device must be designed with not only a robust ESD capability but also the fast turn-on speed in case the output buffer was damaged before the ESD protection device turned on. To increase ESD robustness, the conventional design with large device dimension still suffers the non-uniform current distribution among the device. The high-voltage NMOS has the extremely strong snapback phenomenon during ESD stress, which often results in non-uniform turn-on variation among the multi-fingers of high-voltage NMOS [51]. Moreover, the holding voltage of the high-voltage devices in snapback breakdown condition has been found to be much smaller than the power supply voltage. Such characteristics will cause the high-voltage ICs susceptible to the latchup or latchup-like danger in the practical system applications, especially while these devices are used in the power-rail ESD clamp circuit. To overcome the problem of non-uniform turn-on phenomenon, the gate-coupling technique was applied to the HV NMOS [45], [52]. However, the gate of HV NMOS must be in series with a large resistor, which occupies a large layout area. Hence, how to improve the ESD robustness of the high-voltage NMOS with a reasonable silicon area is indeed an important reliability issue in

the high-voltage BCD technology. In this dissertation, the gate-driven and substrate-triggered ESD protection designs realized with the high-voltage lateral DMOS with consideration of latchup issue is proposed.

1.3 ESD Protection Design for Mixed-Voltage I/O Interface

1.3.1 Stacked-NMOS Device with Substrate-Triggered Technique

To improve the turn-on uniformity among the multiple fingers of CMOS output buffer, the substrate-triggered designs [53]-[56] have been reported to increase ESD robustness of the large-device-dimension nMOS. The substrate-triggered circuit for providing the trigger current should be designed to avoid electrical overstress on the gate oxide and to prevent the undesired leakage current paths during normal circuit operating condition. During ESD stress condition, the substrate-triggered circuit should generate large enough current to effectively improve the turn-on efficiency of parasitic n-p-n BJT in stacked NMOS device. The substrate-triggered circuit should meet above constraints for providing effective ESD protection to the mixed-voltage I/O interfaces. By using this substrate-triggered design, the gates of stacked NMOS in the mixed-voltage I/O circuits can be fully controlled by the pre-driver of I/O circuits without conflict to the ESD protection circuits. Therefore, the ESD robustness of mixed-voltage I/O circuits can be effectively improved without occupying extra silicon area to realize the additional stand-alone ESD protection device into the I/O cells.

1.3.2 Additional ESD Protection Circuit between I/O pad and Power Pad

To improve ESD level of the mixed-voltage I/O circuits, the additional ESD protection circuit was added between I/O pad and VSS power pad [57], [58]. Under the PS-mode ESD stress, the ESD current at the I/O pad is designed to be directly discharged through such additional ESD protection circuit to the grounded VSS. Under the PD-mode ESD stress, the ESD current at the I/O pad can be discharged through the additional ESD protection circuit to VSS power line, and then through the parasitic diode of power-rail ESD clamp circuit to the grounded VDD. The substrate-triggered lateral n-p-n BJT device [57] and the stacked NMOS triggered SCR (SNTSCR) [56], have been verified to protect the mixed-voltage I/O circuits. On the other hand, the additional ESD protection circuit can also be added between I/O pad and VDD power pad to improve the ESD robustness [59]-[61]. Under the PD-mode ESD

stress, the ESD current at the I/O pad is designed to be directly discharged through such additional ESD protection circuit to the grounded VDD. Under the PS-mode ESD stress, the ESD current at the I/O pad can be discharged through the additional ESD protection circuit to VDD power line, and then through the power-rail ESD clamp circuit to the grounded VSS. The diode string, which can sustain high ESD current in forward-biased condition, has been used for protecting the mixed-voltage I/O circuits [59], [60]. The number of diodes in the diode string is determined by the voltage difference between the maximum input voltage at the I/O pad and the VDD supply voltage. The area of such diodes must be scaled up by the number of the diodes to keep the low turn-on resistance from I/O pad to VDD during the ESD stress event. The additional ESD protection device connected between I/O pad the VDD pad can also be implemented by the gate p-n-p BJT, which has been verified to protect the mixed-voltage I/O circuits [59]. In this design, the gated p-n-p BJT can effectively clamp the overstress ESD pulse during the ESD stress event, and meet the gate-oxide reliability constraints without leakage current path during the normal operation.

1.3.3 ESD Protection Design with ESD Bus

The whole-chip ESD protection scheme with the additional ESD bus for the 2×VDD-tolerant and 3×VDD-tolerant mixed-voltage I/O interfaces are proposed in Chapter 3 and Chapter 4 in this dissertation. The additional ESD bus line is realized by a wide metal line in CMOS IC [62]. The ESD bus is not directly connected to an external power pin, but biased via a diode to VDD. The diode connected between the VDD power line and ESD bus is also used to block the leakage current path from the I/O pad to VDD during normal circuit operating condition with a high-voltage input signal. The ESD protection scheme with ESD bus and the circuit operation are discussed in detail in Chapter 3 in this dissertation. With the turn-on-efficient power-rail ESD clamp circuits, high ESD level for the mixed-voltage I/O circuits can be achieved by this ESD protection scheme with ESD bus.

1.4 Organization of This Dissertation

To overcome the ESD design constraints in nanoscale CMOS process, mixed-voltage I/O interfaces and high-voltage BCD process, the novel ESD protection circuits have been developed and verified in this dissertation. This dissertation contains six chapters. Chapter 1 presents an introduction of the gate direct tunneling current in the thin gate-oxide MOS transistor while implemented in nanoscale CMOS technology and an overview on the design

concept and circuit implementations of the ESD protection designs for mixed-voltage I/O interfaces without using the additional thick gate-oxide process. To improve ESD level of the mixed-voltage I/O circuits, the ESD protection design without increasing the process complexity is strongly requested by the mixed-voltage I/O circuits in consumer IC products. Such ESD protection design in the mixed-voltage I/O circuits still meets the gate-oxide reliability constraints, and needs to prevent the undesired leakage current paths during normal circuit operating condition. Under ESD stress condition, the ESD protection circuit should be quickly triggered on to discharge ESD current.

In chapter 2, a new power-rail ESD clamp circuit with low standby leakage current for nanoscale IC product is proposed. The low-leakage power-rail ESD clamp circuit is composed of substrate-triggered SCR device and special ESD detection circuit. The traditional RC-based ESD protection design with consideration of gate current issue is discussed. Compared with the traditional large-sized MOSFET as ESD clamp device, the SCR device without poly-gate structure has good immunity against the gate leakage current. The special ESD detection circuit is designed with consideration of gate current to reduce the standby leakage current. By controlling the gate current of the devices in the ESD detection circuit under a specified bias condition, the whole power-rail ESD clamp circuit can achieve a low standby leakage current. Without using additional low-leakage or thick gate-oxide devices (which need extra mask layers and process flows), the new proposed design has been fabricated and verified in a 1-V 65nm fully-silicided standard CMOS process.

In chapter 3, a new high-voltage-tolerant ESD clamp circuit is proposed to protect the mixed-voltage I/O circuits for receiving signals with 2×VDD voltage level. The devices used in the high-voltage-tolerant ESD protection design are all 1V low-voltage thin gate-oxide NMOS/PMOS devices which can be safely operated under the 1.8V bias conditions without suffering from the gate-oxide reliability issue. The gate current of each thin gate devices in the high-voltage-tolerant ESD detection circuit has also been considered. By using the ESD protection scheme with the ESD bus and the proposed high-voltage-tolerant ESD clamp circuit, the mixed-voltage I/O circuit can be well protected. The four mode (PS, NS, PD, and ND) ESD stresses on the mixed-voltage I/O circuits can be effectively discharged. The new proposed circuit has been fabricated in a 1-V 65-nm standard CMOS process for experimental verification.

In chapter 4, two new ESD protection design by using only 1×VDD low-voltage devices for mixed-voltage I/O buffer with 3×VDD input tolerance are proposed. Two different special

high-voltage-tolerant ESD detection circuits are designed with substrate-triggered technique to improve ESD protection efficiency of ESD clamp device. These two ESD detection circuits with different design concepts both have effective driving capability to trigger the ESD clamp device on. These ESD protection designs have been successfully verified in two different 130nm 1.2-V standard CMOS processes to provide excellent on-chip ESD protection for 1.2-V/3.3-V mixed-voltage I/O buffers.

In chapter 5, the ESD protection design for smart power applications with lateral double-diffused MOS (LDMOS) transistor is investigated. With the gate-driven and substrate-triggered circuit techniques, the n-channel LDMOS can be quickly turned on to protect the output drivers during ESD stress event. From the experimental results, the high-voltage lateral DMOS with the proposed ESD detection circuit has better TLP-measured It2, ESD robustness, and turn-on efficiency than the stand-alone lateral DMOS. The proposed gate-driven and substrate-triggered ESD protection circuits have been successfully verified in a 0.35-μm 5V/40V bipolar CMOS DMOS (BCD) process.

Finally, the main results of this dissertation are summarized in chapter 6. Some suggestions for the future works are also addressed in this chapter.

Chapter 2

Low Leakage ESD Protection Design for Nanoscale CMOS Process

In this chapter, a new power-rail ESD clamp circuit with low standby leakage current for nanoscale IC product is proposed. The low-leakage power-rail ESD clamp circuit is composed of substrate-triggered SCR device and ESD detection circuit. The SCR device without poly-gate structure has good immunity against the gate leakage current. The new proposed ESD clamp circuit has an efficient ESD detection circuit to improve the turn-on efficiency of the ESD clamping device. By using the new proposed circuit solution with only thin gate-oxide devices, the standby leakage current of the proposed power-rail ESD clamp circuit can be successfully reduced under the normal circuit operating condition. The proposed power-rail ESD clamp circuit has been successfully verified in a 1-V 65-nm CMOS process. [63].

2.1 Background

With the decrease of the power supply voltage for low power applications, the thickness of the gate oxide has been also scaled down in the nanometer CMOS technologies. However, such a thin gate oxide of only ~2nm in advanced CMOS technology has been reported to result in a substantial fraction of the overall leakage current in the chip due to its gate leakage current [64]. In 45-nm generation and beyond, the metal gate technology is therefore applied to reduce the gate leakage current [65]. Nevertheless, the gate leakage issue still exists in the 90-nm and 65-nm CMOS technologies which are currently used in production without the high-k metal gate structure. The gate current has been modeled in BSIM4 MOSFET model, and the foundries have also provided the corresponding SPICE models of nanometer CMOS processes to circuit designers. Recently, some work has been reported on how to reduce the gate leakage current for digital circuits in advanced CMOS processes [66]-[68].

2.1.1 Influence of Gate Current on ESD Protection Circuit

From the perspective on commercial IC products, to achieve the electrostatic discharge (ESD) specification is necessary for product qualification. The power-rail ESD clamp circuit to effectively protect the core circuits is traditionally implemented by RC-based ESD protection structure with a large-sized ESD clamping MOSFET [chap1]. Such a traditional RC-based ESD clamp circuit is shown in Fig. 2.1. However, the gate leakage current caused from the large-sized MOSFET (M_{ESD}) and the MOS capacitor (Mc) in the traditional power-rail ESD clamp circuit becomes serious in nanoscale CMOS processes. Such gate current through the MOS capacitor could influence the function of the traditional ESD protection circuit seriously. With such a leakage current in the MOS capacitor, the ESD clamping MOSFET (M_{ESD}) cannot be completely turned off under the power-on condition due to the malfunction of the ESD detection circuit caused by gate leakage current and in turn to induce extra large leakage current through M_{ESD}. Such a leaky ESD protection circuit is barely tolerable in portable products with low power requirements. To solve the problem of malfunction in the traditional RC-based ESD detection circuit, the modified ESD clamp circuit with the timer level restorer was ever reported as that re-drawn in Fig. 2.2 [69]. But, the experimental result in that work still showed a high standby leakage current in the order of several micro-amperes in a 130-nm CMOS process at a high temperature of 125°C [69]. New designs of the power-rail ESD clamp circuit need to be developed to further reduce such standby leakage current in nanometer CMOS processes.

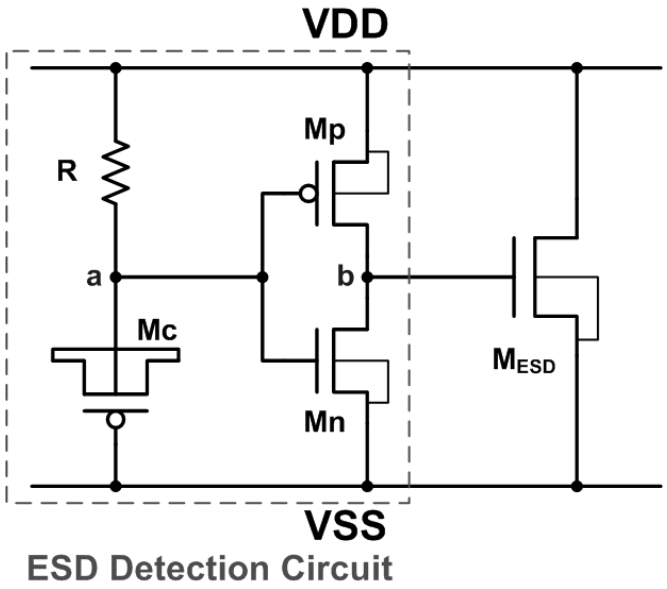


Fig. 2.1. The traditional RC-based power-rail ESD clamp circuit.

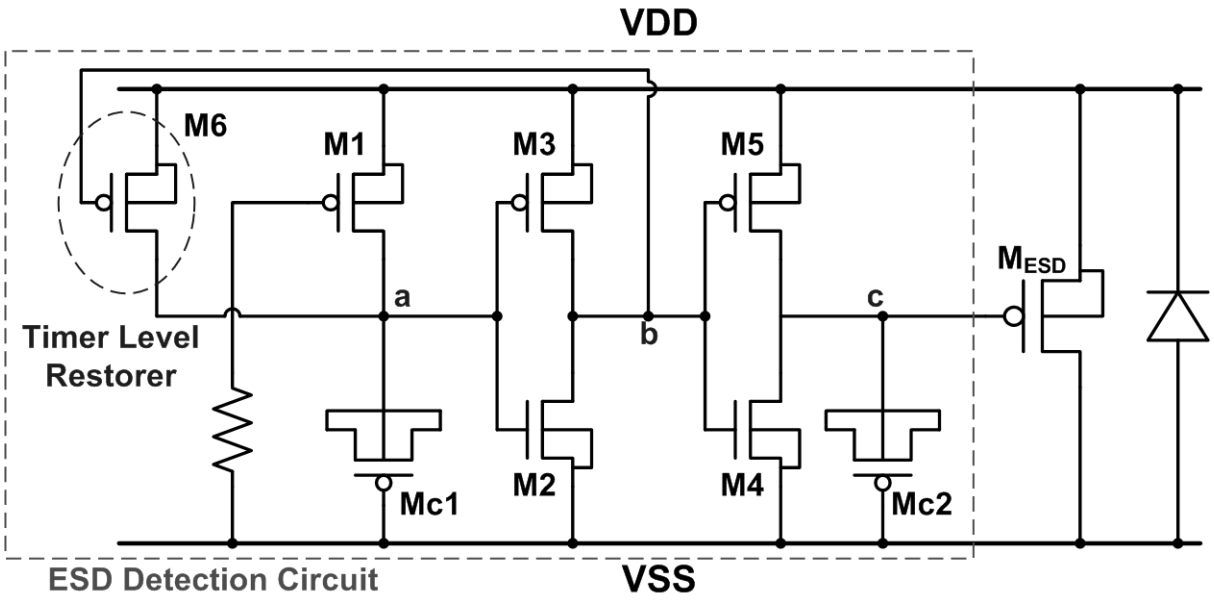


Fig. 2.2. The modified power-rail ESD clamp circuit with timer level restorer.

2.1.2 Gate Current through MOS Capacitor

The gate leakage current cannot be neglected when the gate oxide thickness is scaled down to 3nm and below. The oxide thickness and the total gate current across the gate-oxide of N/P MOSFET with W/L of 1μm/1μm under 1-V bias in 90-nm, 65-nm, and 45-nm CMOS processes are compared in Table 2.1. In BSIM4 model [14], the components of gate tunneling current include the tunneling current between gate and bulk (*Igb*), the current between gate and channel (*Igc*), and the current between gate and source/drain diffusion regions (*Igs* and *Igd*).

Table 2.1

Oxide Thickness and Gate Current of Gate-Oxide of N/P MOSFET under 1-V Bias in Different CMOS Technologies

Generation	MOS Type	Oxide Thickness	Gate Leakage @ 1V Bias (W/L = 1μm/1μm)
90nm	NMOSFET	~2.3nm	~11nA
	PMOSFET	~2.5nm	~3nA
65nm	NMOSFET	~2.0nm	~140nA
	PMOSFET	~2.2nm	~80nA
45nm	NMOSFET	~1.9nm	~260nA
	PMOSFET	~2.1nm	~95nA

For a MOS capacitor, the source, drain, and bulk terminals are connected to the same node. Therefore the total gate-to-source current (*Igcs*+*Igs*), the total gate-to-drain current (*Igcd*+*Igd*), and the gate-to-bulk current (*Igb*) of a MOS capacitor with W/L of 5μm/5μm can be simulated with foundry provided SPICE parameters. The corresponding currents are 1.02μA, 1.02μA, and 89pA, respectively, in a 65-nm CMOS process under 1-V bias. Compared with gate-to-source current and gate-to-drain current, the component of gate-to-bulk current in a MOS capacitor is quite small in comparison to the simulated results. The simulated total gate current of the MOS capacitor with W/L of 5μm/5μm and 10μm/10μm in 65-nm and 90-nm CMOS processes are shown in Fig. 2.3. From Fig. 2.3, the gate current of a MOS capacitor is directly dependent on the area of the poly gate structure. Besides, the gate leakage problem in 65-nm CMOS process is more serious than that in 90-nm CMOS process.

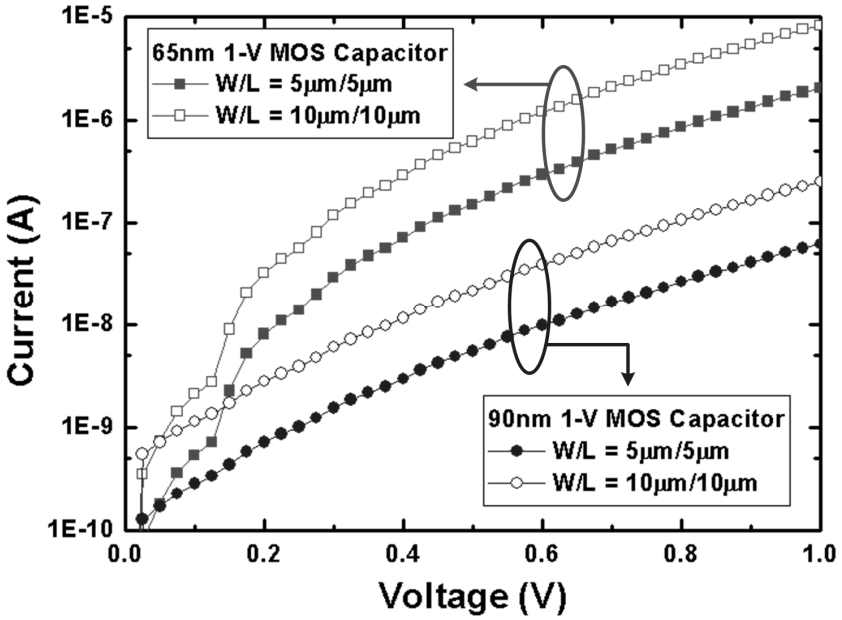


Fig. 2.3. The gate current of the MOS capacitor in different CMOS technologies.

2.2 ESD Protection Design with Consideration of Gate Current

2.2.1 Traditional RC-based ESD Clamp Circuit with Gate Current Consideration

The traditional RC-based ESD clamp circuit is shown in Fig. 2.1. Based on BSIM4 gate

current model, the MOS capacitor with a large-sized gate oxide will induce a large amount of gate current from node a to VSS under the normal circuit operating condition. Such gate current causes a voltage drop across the resistor R, and therefore the PMOS Mp in the ESD detection circuit can not be completely turned off. With a non-turned-off PMOS, node b is charged up to some voltage level higher than VSS, and that in turn causes the main ESD clamping MOSFET (M_{ESD}) operating in sub-threshold region under the normal circuit operating condition. The ESD clamping MOSFET (M_{ESD}) drawn with large device dimension in sub-threshold region further generates a large amount of standby leakage current.

Fig. 2.4 shows the HSPICE-simulated voltages on the nodes of the ESD detection circuit and the gate current of the MOS capacitor Mc under the normal power-on condition with a rise time of 1ms in a 65-nm CMOS process. The dimensions of R, Mc, Mp, and Mn are 60kΩ, 5μm/5μm, 80μm/0.12μm, and 5μm/0.12μm. When the VDD reaches 1V, the gate current of Mc is as large as 1290nA, so that the voltage level at node a cannot reach 1V due to the voltage drop across R. The PMOS Mp with a Vsg of ~0.1V cannot be fully turned off and in turn a leakage current path is generated from VDD through the inverter (Mp and Mn) to VSS. The ESD clamping MOSFET with several hundred micro-meters device width in sub-threshold region will cause a considerable leakage current of several micro-Amperes under the normal circuit operating condition with VDD of 1V in a 65-nm CMOS process.

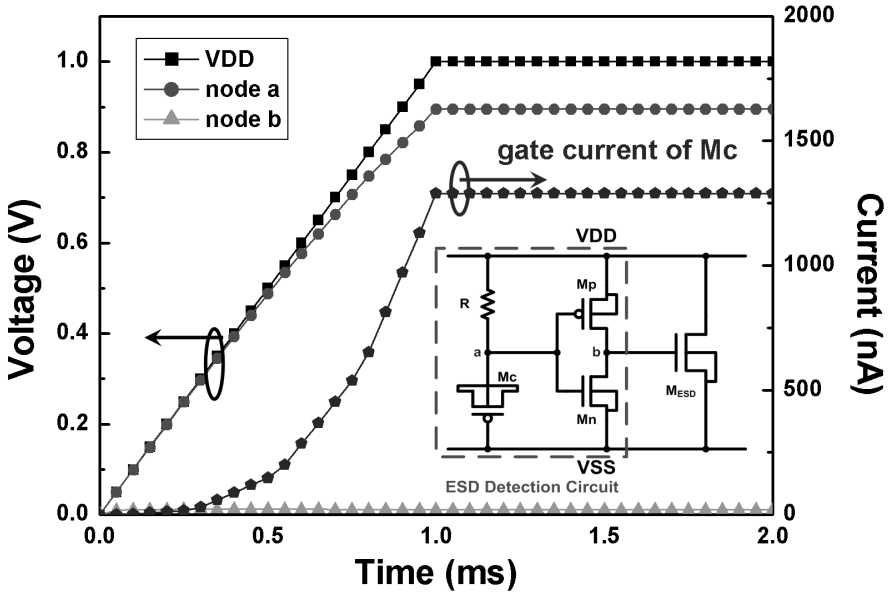


Fig. 2.4. HSPICE-simulated voltage on the nodes of the ESD detection circuit and the gate current flow through the MOS capacitor Mc in the traditional RC-based power-rail ESD clamp circuit under the normal power-on condition with VDD of 1V in a 65-nm CMOS process.

2.2.2 Modified ESD Clamp Circuit with Gate Current Consideration

To solve the malfunction of the ESD detection circuit that results in a large amount of leakage current from the ESD clamping MOSFET (M_{ESD}) in sub-threshold region, one modified design with the additional timer level restorer was reported in Fig. 2.2 [69]. Under the normal power-on condition, node a is initially pulled high by the turned-on PMOS M1. However, with a leaky gate MOS capacitor Mc1, node a cannot be pulled to a full VDD voltage level. Afterward node b is pulled down to VSS by NMOS M2 and in turn the timer level restorer can be turned on, pulling node a to a full VDD voltage level. Therefore, the function of the ESD detection circuit is guaranteed to keep the main ESD clamping MOSFET (M_{ESD}) in off state under the normal circuit operating condition. However, node a in this ESD detection circuit is kept at the voltage level of VDD, so that the voltage difference between the gate and bulk of MOS capacitor Mc1 still causes a significant leakage current path from VDD through M1 and Mc1 to VSS in nanoscale CMOS process.

From HSPICE simulation result based on BSIM4 model, under the normal operating condition with VDD of 1V, the standby leakage current in the ESD detection circuit of Fig. 2.2 is around 1.5μA at 25°C in a 65-nm CMOS process, where the dimensions of devices are chosen appropriately and listed in Table 2.2. The simulation result excludes the leaky large-sized ESD clamping MOSFET (M_{ESD}). Even if the timer level restorer can solve the malfunction problem in the ESD detection circuit, the standby leakage current of such modified power-rail ESD clamp circuit is still too large for portable application with low-power requirements.

To overcome the gate leakage current in the thin gate oxide, one solution is to use the thick gate-oxide device to implement the MOS capacitor in the ESD detection circuit. In this work, a power-rail ESD clamp circuit designed with only thin gate-oxide devices to achieve ultra-low standby leakage current is proposed. By using the new proposed circuit solution with only thin gate-oxide devices, the standby leakage current of the power-rail ESD clamp circuit can be successfully reduced under the normal circuit operating condition.

Table 2.2

Dimensions of Devices in the ESD detection Circuit of the Modified ESD Clamp Circuit with Timer Level Restorer for HSPICE Simulation

Devices	Dimension (W/L)
Mc1	5μm/5μm
Mc2	5μm/5μm
M1	0.3μm/20μm
M2	5μm/0.12μm
M3	10μm/0.12μm
M4	20μm/0.12μm
M5	5μm/0.12μm
M6	0.3μm/20μm

2.3 Ultra Low-Leakage Power-Rail ESD Clamp Circuit

The proposed ultra-low-leakage power-rail ESD clamp circuit is shown in Fig. 2.5. The p-type substrate-triggered silicon-controlled rectifier (SCR) device is used as the main ESD clamping device [70]-[73]. The SCR device, which is composed of cross-coupled n-p-n and p-n-p BJTs with regenerative feedback loop, with a low holding voltage can sustain a high ESD level within a small silicon area in CMOS process. Moreover, the SCR device without poly gate structure has good immunity against the gate leakage problem. However, there are some disadvantages of using the SCR device as the ESD clamp device, such as the slow turn-on speed and the high triggered voltage. Therefore, the ESD detection circuit is used to improve the turn-on speed of the SCR device with substrate-triggered design. The new ESD detection circuit is designed with consideration of the gate current in this work. Utilizing the gate current to bias the ESD detection circuit and to reduce the voltage difference across the gates of the MOS capacitors, the gate leakage current through the MOS capacitor under the normal circuit operating condition can be further reduced. The total leakage current resulted from the MOS capacitor in the ESD detection circuit can be minimized. Therefore, the leakage currents through the ESD clamping device and the ESD detection circuit can be well controlled and minimized by this new proposed design.

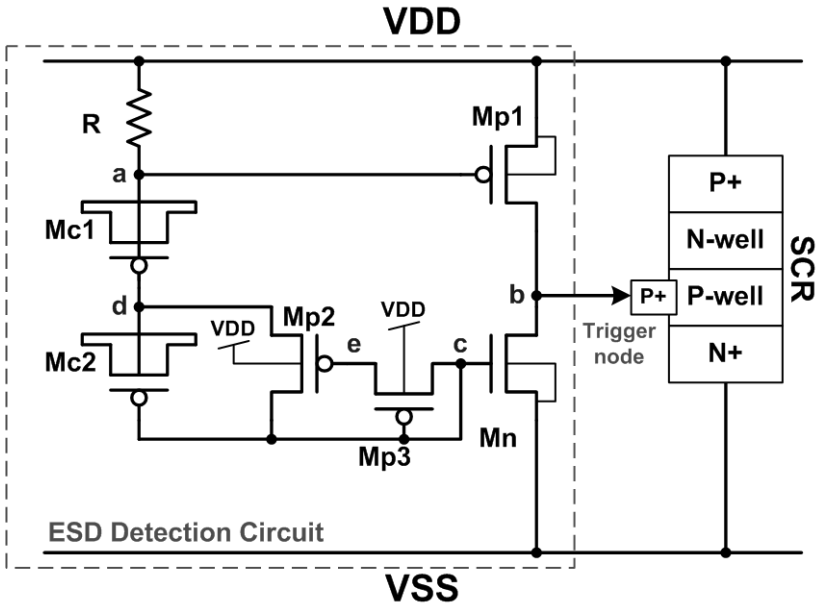


Fig. 2.5. The proposed ultra-low-leakage power-rail ESD clamp circuit with p-type substrate-triggered SCR device as ESD clamp device, where the ESD detection circuit is designed with consideration of gate leakage current.

In the proposed ESD detection circuit, the PMOS Mp1 is used as substrate driver to generate the substrate-triggered current into the trigger node of the SCR device during the ESD stress event, but Mp1 is kept off under the normal circuit operating condition. The NMOS Mn is used to keep the voltage level at the trigger node (node b in Fig. 2.5) at VSS, so the ESD clamping device (SCR) is guaranteed to be turned off during the normal circuit operating condition. The RC time constant from R, Mc1, Mc2, and the parasitic gate capacitance of Mn is designed around the order of ~μs to distinguish ESD stress event from the normal power-on condition. The diode-connected Mp2 and Mp3 are acted as a start-up circuit with initial gate-to-bulk current from VDD into the ESD detection circuit, and in turn to conduct some gate current of Mc1 to bias the nodes c, d, and e. After that, the voltage level at node d will be biased at a voltage level to reduce the voltage difference across the gate of Mc1 and to minimize the gate leakage current through the MOS capacitors.

2.3.1 Design Procedure

The gate voltage of Mn should be designed higher than its threshold voltage under the normal circuit operating condition. Realized in a 65-nm CMOS process with VDD of 1V, the voltage level at node c is chosen as 0.45V to keep Mn in turned-on state but without

generating too much gate leakage current from node c to VSS under the normal circuit operating condition. While designing the dimensions of the devices in the ESD detection circuit, the voltage levels at node a and node b are assumed to be kept at VDD and VSS, respectively, under the normal circuit operating condition. With consideration of the RC time constant, Mc1 and Mc2 are designed with the same device dimension, so that the voltage level at the node d is chosen as 0.7V. The gate current of Mc1 will be slightly larger than that of Mc2, and the different parts of the gate current can be conducted by Mp2. From Kirchhoff's Current Law, the current equation at the node c, d, and e can be expressed as

$$Igd_{Mn} + Igs_{Mn} = Isg_{Mc2} + Idg_{Mc2} + Id_{Mp2} + Igd_{Mp2} + Id_{Mp3} + Isg_{Mp3}, \quad (2.1)$$

$$Isg_{Mc1} + Idg_{Mc1} = Isg_{Mc2} + Idg_{Mc2} + Id_{Mp2} + Isg_{Mp2}, \text{ and} \quad (2.2)$$

$$Isg_{Mp2} = Id_{Mp3} + Isg_{Mp3}, \quad (2.3)$$

where Igd_{Mn} means the total gate-to-drain current of Mn including *Igcd* and *Igd* defined in [14]. The total gate current of Mc1 is equal to the total gate current through the oxide of Mn, which can be derived as

$$Isg_{Mc1} + Idg_{Mc1} = Igd_{Mn} + Igs_{Mn}. \quad (2.4)$$

The voltage differences between the source and drain (*Vds*) of both Mc1 and Mn are 0V, so that the gate-to-drain current and the gate-to-source current should be the same. Therefore, equation (2.4) can be simplified to the component of only gate-to-source current for Mc1 and Mn, which can be derived as

$$Isg_{Mc1} = Igs_{Mn}. \quad (2.5)$$

The total gate-to-source current of Mc1 (Isg_{Mc1}) in the equation (2.5) can be solved by the given voltage Vsg_{Mc1} of 0.3V with the device parameters provided from foundry, which can be roughly calculated as

$$Isg_{Mc1} \approx W_{eff} \cdot (L_{eff} \cdot 492 + 3 \times 10^{-5}) \text{ (A)}. \quad (2.6)$$

With consideration of the RC time constant, the W/L of MOS capacitor Mc1 is chosen as 5μm/5μm, and the total gate-to-source current of Mc1 can be determined by equation (2.6). Therefore, the device dimension of Mn can also be determined by equation (2.5). Likewise, the dimension of each device in the proposed ESD detection circuit can be derived through the equations (2.1)-(2.3). With fine tuning on the voltage level at the nodes c, d, and e to achieve a minimized overall standby leakage current, the final dimension for each device in the proposed ESD detection circuit implemented in a given 65-nm CMOS process is shown in Table 2.3, where the device dimension of Mp1 can be adjusted with different triggering

current capability to turn on the main ESD clamping device (SCR). With a large device dimension of Mp1, the substrate-triggered current generated by Mp1 can be increased to accelerate the turn-on speed of the SCR device during ESD event. The discussion on the design flexibility is described in Section 2.4.

Table 2.3

Dimensions of Devices in the ESD detection Circuit of The Proposed Power-Rail ESD Clamp Circuit

Devices	Dimension (W/L)
Mc1	5μm/5μm
Mc2	5μm/5μm
Mn	5μm/1μm
Mp1	80μm/0.12μm
Mp2	0.2μm/10μm
Mp3	0.2μm/10μm

2.3.2 Operation under Normal Circuit Operating Condition

Under the normal power-on condition with VDD of 1V and grounded VSS, the gate voltage of Mp1 is biased at around 1V through the resistor R with a low gate current of MOS capacitor Mc1 in the new proposed ESD detection circuit, so that Mp1 can be kept off and no trigger current is generated from the ESD detection circuit to the SCR device. In addition, node c in Fig. 2.5 is biased at some voltage level (~0.45V) to turn on Mn which in turn keeps the trigger node of SCR grounded. Fig. 2.6 shows the HSPICE-simulated voltage waveforms on the nodes of the proposed ESD detection circuit and the gate current through the MOS capacitor Mc1 under the normal power-on condition with a rise time of 1ms and VDD of 1V (VSS of 0V). The gate current of Mc1 is only around 23nA and the voltage level at node a is almost kept at 1V (overlapped with VDD in Fig. 2.6), so that Mp1 is kept in off state.

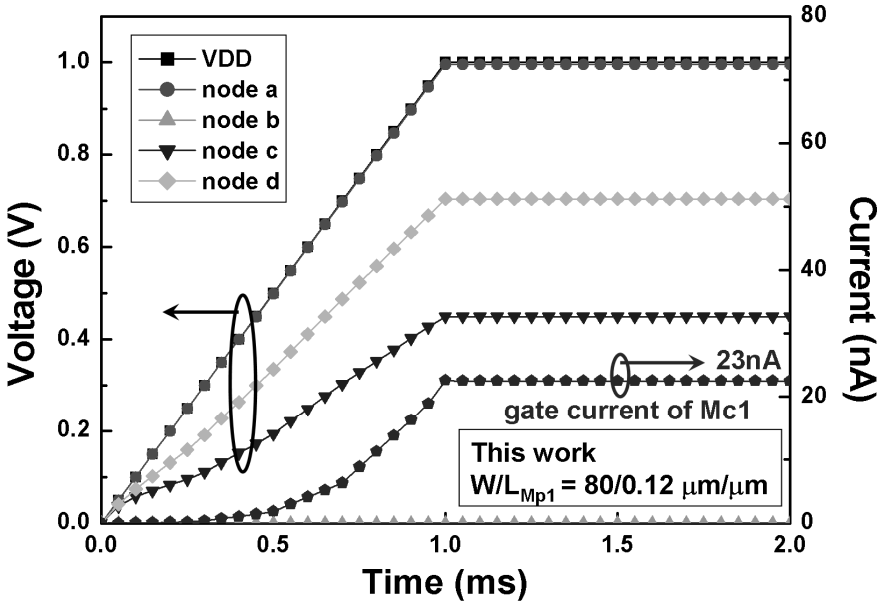


Fig. 2.6. HSPICE-simulated voltage on the nodes of the ESD detection circuit and the gate current flow through the MOS capacitor Mc1 in the proposed ultra-low leakage ESD clamp circuit in a 65-nm CMOS process under the normal power-on condition.

2.3.3 Operation under ESD Transient Event

When a positive fast-transient ESD voltage is applied to VDD with VSS grounded, the RC delay in the ESD detection circuit keeps the gate of Mp1 at a relatively low voltage level compared to the fast rising voltage level at VDD. The Mp1 can be quickly turned on by the ESD energy to generate the substrate-triggered current into the trigger node (node b) of the SCR device. Finally, the SCR device can be fully turned on into holding state to discharge ESD current from VDD to VSS. In order to simulate the fast transient voltage of HBM ESD event, a 0-to-5V voltage pulse with a rise time of 10ns is applied to VDD as "ESD-like transient pulse" in HSPICE simulation. Fig. 2.7 shows the simulated voltage and substrate-triggered current of the new proposed ESD detection circuit under the ESD transition, where a 0-to-5V voltage pulse with a rise time of 10ns is applied to VDD to simulate the fast transient voltage of human-body-model (HBM) ESD event. With a limited voltage height of 5V in the voltage pulse, the voltage transition on each node in the ESD detection circuit can be simulated to check the desired circuit function before device breakdown. With the proposed ESD detection circuit, the SCR device should be triggered on before device breakdown.

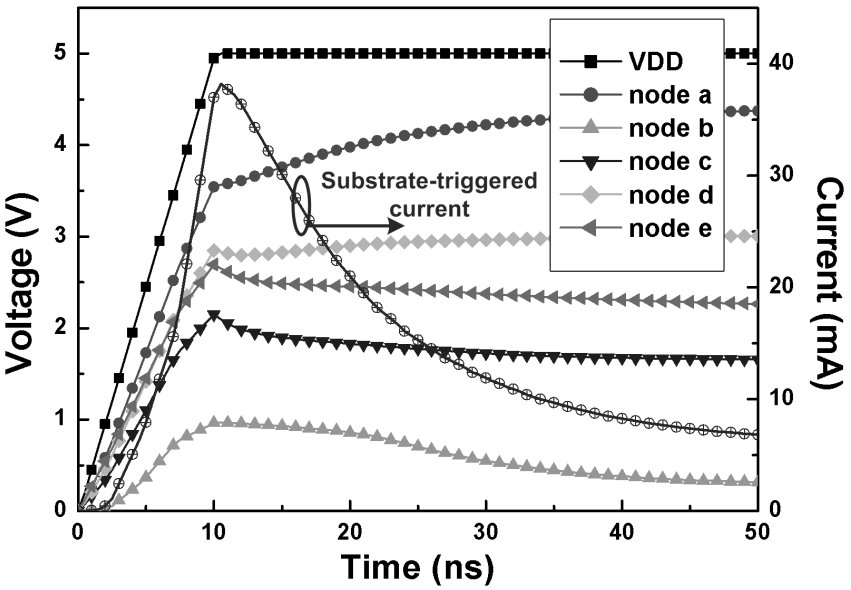


Fig. 2.7. HSPICE-simulated voltages on the nodes of the ESD detection circuit and the substrate-triggered current which flows into the SCR device under 0-to-5V ESD-like transition on VDD.

2.4 Experimental Results

The new proposed power-rail ESD clamp circuit has been fabricated in a 65-nm CMOS process. All devices used in this design are 1-V fully-silicided devices, including the SCR device. The active area of the whole ESD clamp circuit (including the SCR width of 45 μm) is only 49μm×21μm, and the layout view is shown in Fig. 2.8.

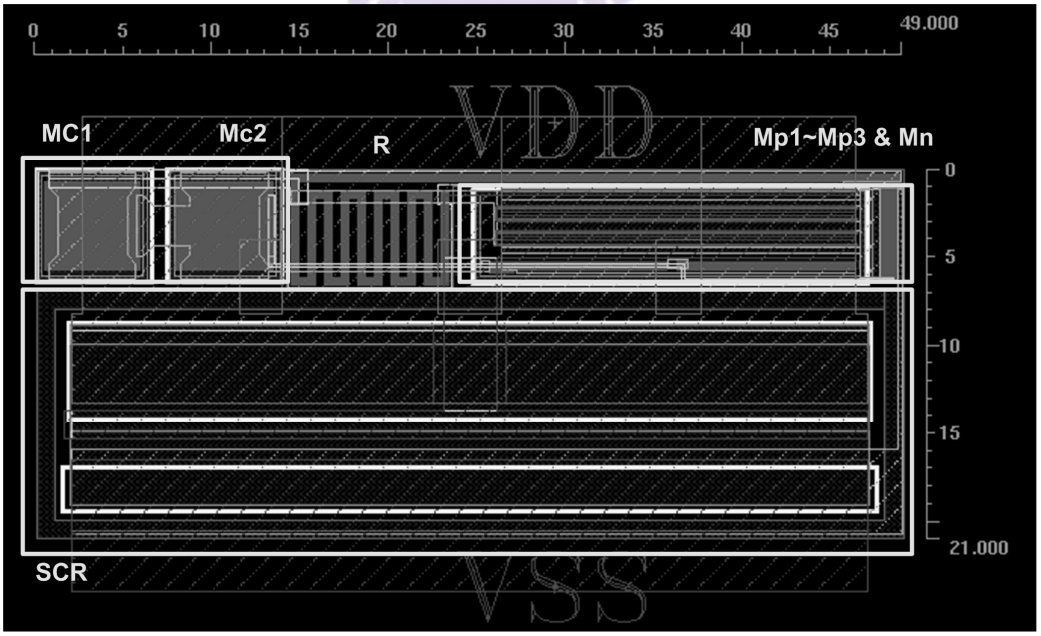


Fig. 2.8. Layout view of the proposed power-rail ESD clamp circuit.

The widths of SCR device as ESD clamping device are varied in 30μm, 45μm, 60μm, and 90μm in the test chip to verify the corresponding ESD robustness. The chip photograph of the test patterns of the proposed power-rail ESD clamp circuit is shown in Fig. 2.9.

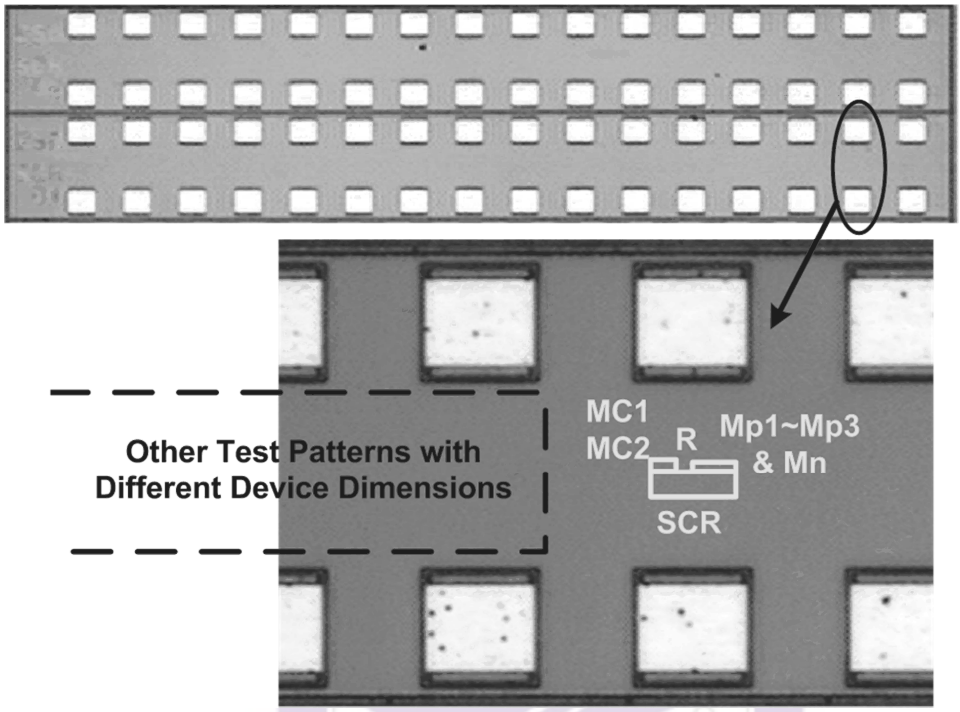


Fig. 2.9. Chip photograph of the test patterns of the proposed power-rail ESD clamp circuit. The chip has been fabricated in a 65-nm CMOS process with 1-V devices.

2.4.1 Turn-on Verification

The turn-on behavior of SCR devices is an important index for ESD protection, which had been evaluated in the literature [74]-[76]. To verify the turn-on efficiency of the proposed ultra-low-leakage ESD clamp circuit, a square-type voltage pulse with a rise time of ~10ns and a pulse height of 5V is used to simulate the rising edge of a positive-to-VSS HBM ESD pulse. When the positive voltage pulse is applied to VDD of the proposed ESD clamp circuit with VSS grounded, the sharp-rising edge of the ESD-like voltage pulse will start the ESD detection circuit to generate the substrate-triggered current to trigger on the SCR device, and in turn to provide a low-impedance path between VDD and VSS. The voltage waveform clamped by the ESD clamp circuit on the VDD pad is shown in Fig. 2.10, where the voltage waveform of the applied ESD-like 0-to-5V pulse is measured into an open to show its original pulse shape. The applied 5-V voltage pulse is clamped down quickly to a stable low

voltage level (~2V) by the proposed ESD clamp circuit with a SCR device width of 45μm. From the measured voltage waveform, the excellent turn-on efficiency of the proposed ESD clamp circuit during the ESD stress event has been successfully verified.

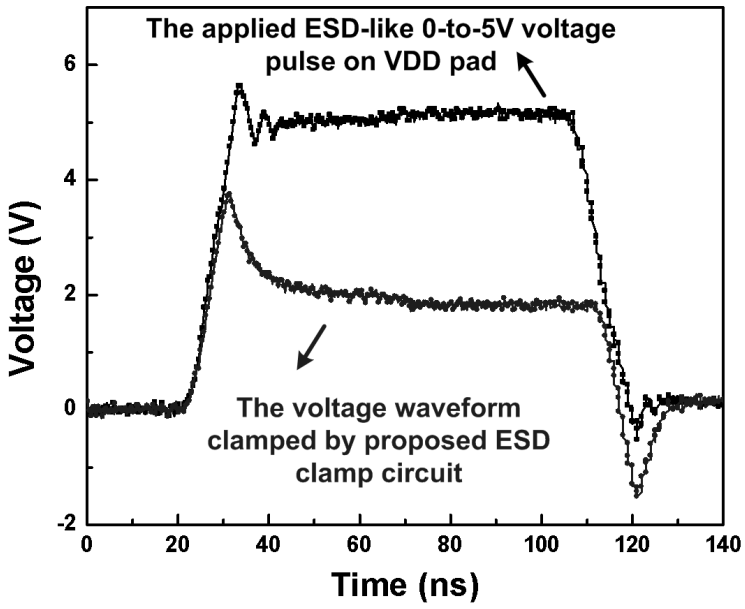


Fig. 2.10 The measured voltage waveforms clamped by the proposed ESD clamp circuit by applying a 0-to-5V voltage pulse to VDD pad.

2.4.2 ESD Robustness

To investigate the turn-on behavior of the ESD clamping device with ESD detection circuit during the ESD stress event, transmission line pulse (TLP) generator with a pulse width of 100ns and a rise time of ~10ns is used to measure the second breakdown current (It2) of the ESD clamp circuit. The TLP-measured I-V characteristics of the ESD clamp circuit with SCR device of different widths are shown in Fig. 2.11, where the device dimension of the substrate driver Mp1 is kept at 80μm/0.12μm. The ESD clamp circuit with SCR widths of 45μm, 60μm, and 90μm can achieve It2 of 4.54A, 6.03A, and 9.24A, respectively. Without any triggered current, the original trigger voltage of the SCR device is as high as 11.5V, as shown in Fig. 2.11. However, with the proposed ESD detection circuit in this work, the trigger voltage of the SCR device is reduced to only around 3 to 4V. Therefore, the low trigger voltage and high It2 value of the ESD clamp circuit can ensure the effective ESD protection capability. The holding voltage of the SCR device is around 1.6V. Such holding

voltage is higher than the voltage level of VDD (1V) under the normal circuit operating condition. Even if the SCR device is mis-triggered due to the noise disturbance, it will automatically recover to the normal condition after the noise source is removed. Therefore, the new proposed power-rail ESD clamp circuit is free from latchup issues. The turn-on resistance of the ESD protection circuit with SCR width of 45μm is ~1.6Ω, where ~0.5Ω is contributed by the metal connections between pads. By using the ESD protection circuit with SCR width of 45μm to protect the internal circuit with breakdown voltage of 6V, the parasitic resistance of the metal connection should be designed with lower than 1.5Ω to bypass 2kV HBM ESD current (1.33A). With a larger dimension of SCR width, the larger resistance of metal connection can be allowed.

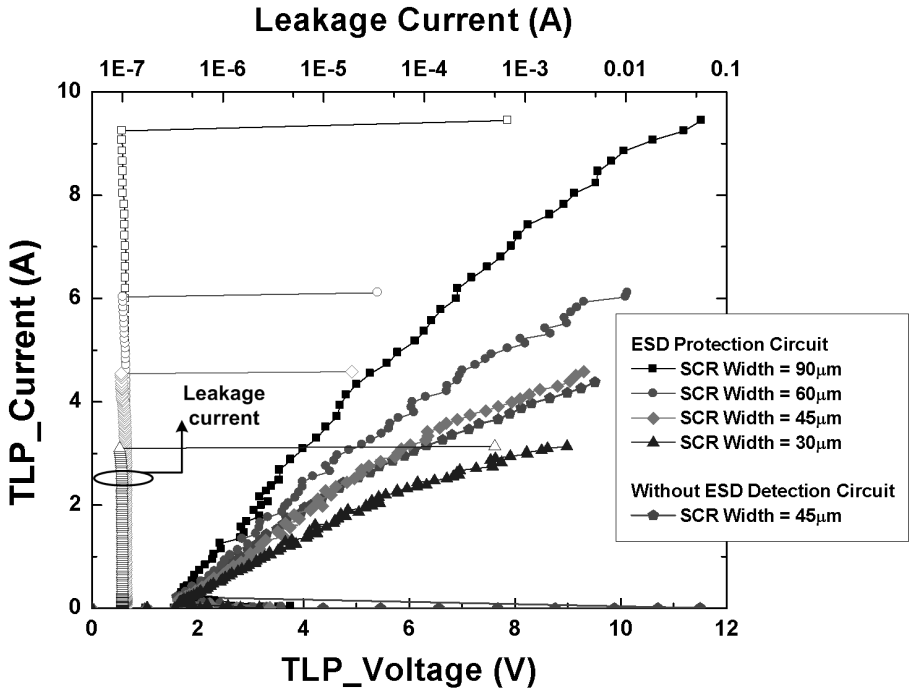


Fig. 2.11. The TLP-measured I-V characteristics of the proposed power-rail ESD clamp circuit with SCR device of different widths under positive-to-VSS ESD stress. The TLP-measured I-V curve of the stand-alone SCR device without ESD detection circuit is also included in this figure.

To evaluate the effectiveness of the proposed ESD protection circuit in faster ESD-transient events, the TLP-measured I-V characteristics of the ESD protection circuit with SCR width of 45μm under the TLP rise times of 10ns, 2ns, and 200ps are compared in Fig. 2.12. There is no obvious difference in the TLP-measured I-V characteristics under different TLP rise times. The proposed ESD detection circuit is fast enough to turn on the SCR device even under a fast-transient pulse with only 200-ps rise time.

The human-body-model (HBM) ESD levels and machine-model (MM) ESD levels of the proposed ESD clamp circuit with SCR of different widths under positive-to-VSS ESD stress are listed in Table 2.4. The corresponding second breakdown current (It2) measured by TLP is also listed in Table 2.4. The failure criterion is defined as the I-V characteristic curve shifting over 20% from its original curve after three continuous ESD zaps at every ESD test level. The HBM and MM ESD levels of the proposed ESD clamp circuit with SCR width of only 45μm can achieve 7kV and 325V, respectively, in a 65-nm CMOS process.

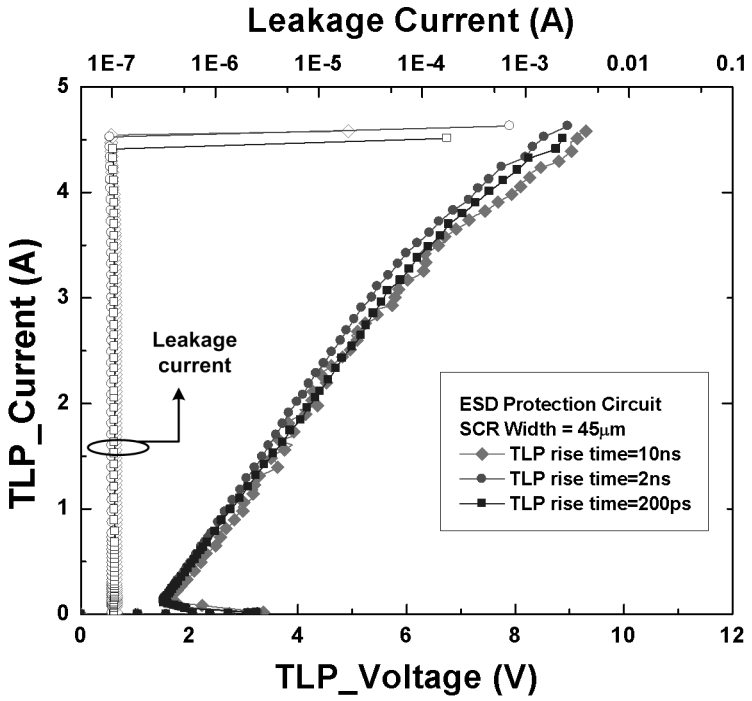


Fig. 2.12. The TLP-measured I-V characteristics of the proposed power-rail ESD clamp circuit with SCR device of 45μm under different TLP rise times of 10ns, 2ns, and 200ps.

Table 2.4

ESD Robustness of the Proposed Power-Rail ESD Clamp Circuit with SCR Device of Different Widths

SCR Width (μm)	It2 (A)	HBM ESD Level (V)	MM ESD Level (V)
30	3.10	4750	225
45	4.54	7000	325
60	6.03	> 8000	400
90	9.24	> 8000	525

The dependence of It2 and MM ESD levels on SCR widths is shown in Fig. 2.13. From Fig. 2.13, the It2 performance of the SCR with different widths is almost a straight line, so that the turn-on uniformity of the SCR device can be verified. However, there is some degradation of the MM ESD level compared with the expected dash line when SCR width increases to 90μm. With a limited driving capability from the same dimension of substrate driver (Mp1) in the ESD detection circuit, the SCR device with a larger device width might be not turned on as efficiently as that with a smaller device width under a faster rising MM ESD stress.

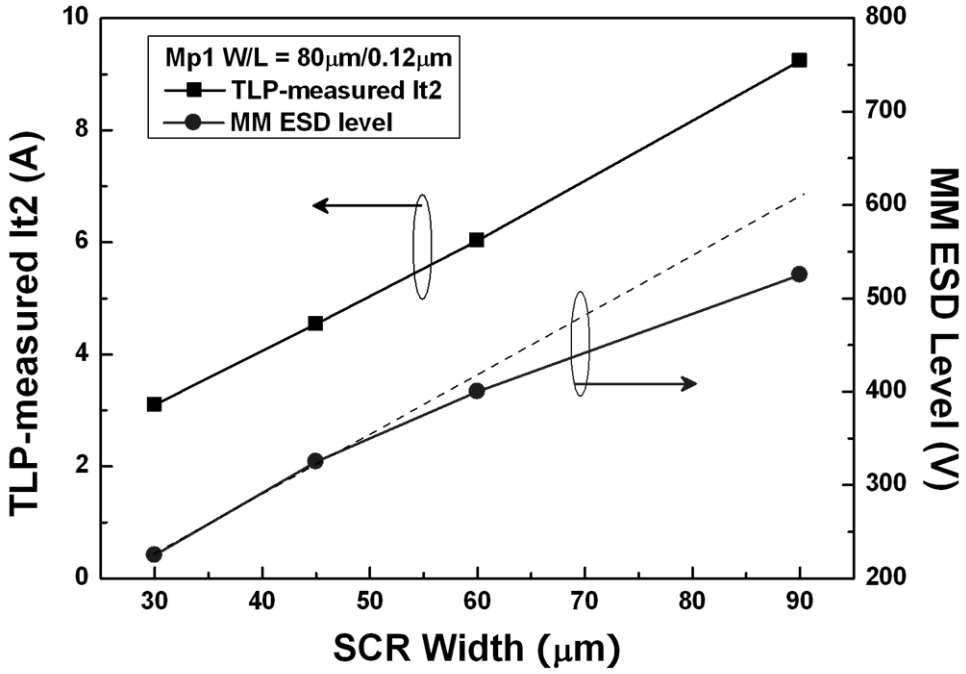


Fig. 2.13. The dependence of TLP-measured It2 and MM ESD levels on SCR device of different widths.

2.4.3 Standby Leakage and Design Flexibility

The standby leakage current under 1-V bias of the whole ESD clamp circuit with SCR of 45μm is only 96nA at 25°C. The standby leakage current of the proposed ESD clamp circuit is dominated by Mp1 in the ESD detection circuit while the leakage current contributed by the MOS capacitor is only ~23nA from simulation result. Increasing the device dimension of Mp1 can improve the turn-on speed of the SCR device with a reduced

trigger voltage, but it results in a larger standby leakage current under the normal circuit operating condition. The measured results of the standby leakage current and the trigger voltage of the proposed power-rail ESD clamp circuit with different dimensions for Mp1 and the SCR device are shown in Figs. 2.14 and 2.15. From Fig. 2.14, the standby leakage currents of the proposed power-rail ESD clamp circuit with SCR of 45μm and 90μm are similar, because there is a quite small leakage current (less than 1nA at 25°C) generated from the SCR device. While the device dimension of Mp1 increases from 80μm/0.12μm to 100μm/0.12μm, the standby leakage current of the whole power-rail ESD clamp circuit increases from 96nA to 115nA at 25°C (1.02μA to 1.28μA at 125°C) under 1-V bias, as shown in Fig. 2.14. However, the corresponding trigger voltage of the SCR of 45μm can be reduced from 3.7V to 3.1V when the dimension of Mp1 is increased, as shown in Fig. 2.15. Therefore, the standby leakage current of the whole ESD clamp circuit and the turn-on speed of the SCR device can be adjusted to meet different application requirements.

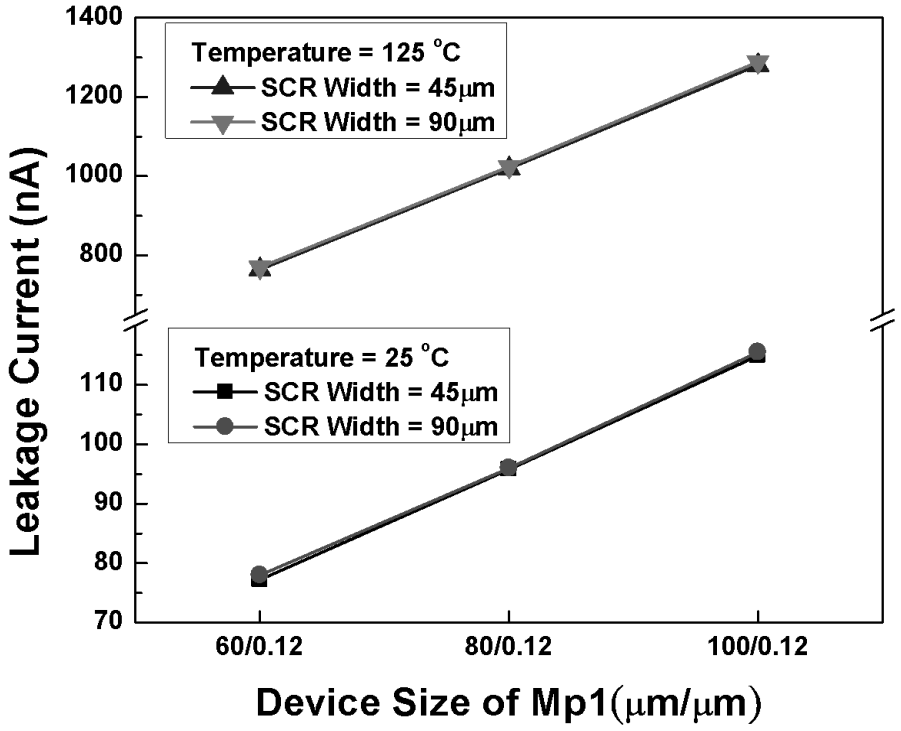


Fig. 2.14. The dependence of the standby leakage current under 1-V bias of the whole ESD clamp circuit at different temperatures.

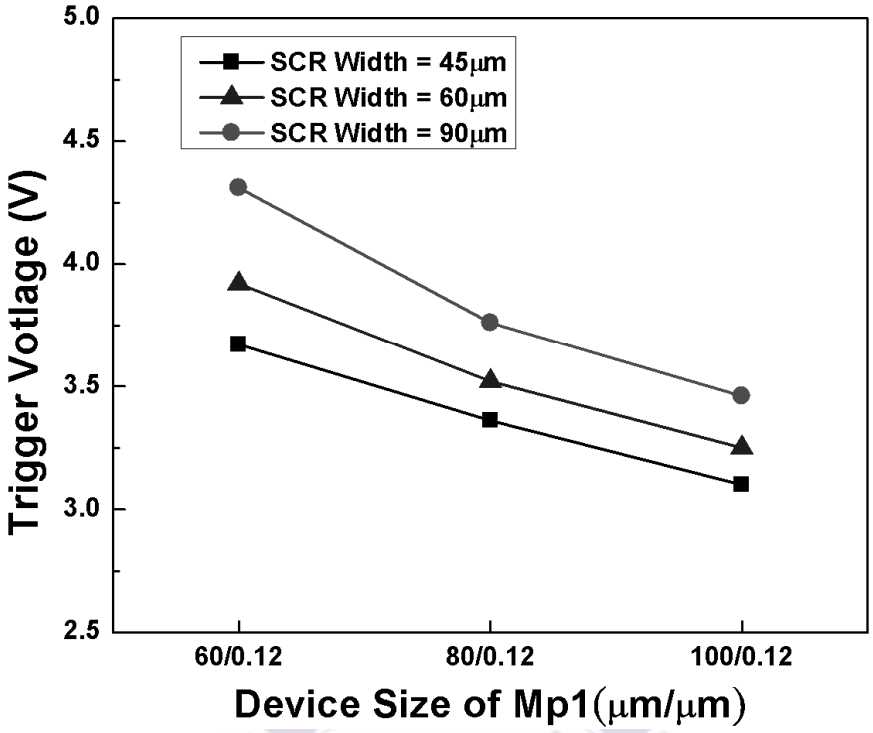


Fig. 2.15. The TLP-measured trigger voltage of the SCR device, on the device size of Mp1 under SCR device of different widths.

2.4.4 Discussion

From the simulation, the ratios of gate leakage current to sub-threshold leakage current in the ESD detection circuit of the traditional RC based ESD protection circuit and this work are 3.0:1 and 0.34:1 under VDD of 1V at 25°C, respectively. Both the total amount of leakage current and the component of gate leakage current are reduced by the proposed design. Table 2.5 shows the performance comparison among the traditional RC-based power-rail ESD clamp circuit, the modified ESD clamp circuit with timer level restorer, and the new proposed design of this work. The traditional RC-based power-rail ESD clamp circuit was also fabricated in the same 65-nm CMOS process. The standby leakage currents under 1-V bias of the traditional RC-based ESD clamp circuit with the ESD clamping MOSFET (M_{ESD}) of W/L = 400μm/0.12μm at 25°C and 125°C are as large as 3.74μA and 44.8μA, respectively. Even if the leaky ESD clamping MOSFET (M_{ESD}) is excluded, the standby leakage current of the stand-alone ESD detection circuit is still as large as 26.9μA at 125°C. The standby leakage current of the modified ESD detection circuit of Fig. 2.1(b) is simulated as around 1.5μA with the appropriate device dimensions shown in Table 2.2 under the same bias condition

(VDD of 1V with VSS grounded) at 25°C. Since the high temperature models from the foundry might not be accurate enough, the standby leakage current of the modified ESD detection circuit at 125°C is not available by simulation. The standby leakage currents under 1-V bias of the proposed ESD clamp circuit with SCR of 45μm and Mp1 of 80μm/0.12μm at 25°C and 125°C are only 96nA and 1.02μA, respectively. The HBM ESD level of the traditional RC-based ESD clamp circuit with the ESD clamping MOSFET (M_{ESD}) of W/L = 400μm/0.12μm is 3.25kV. However, the HBM ESD level of the proposed ESD clamp circuit with SCR width of 45μm in this work can achieve 7kV. With consideration of ESD robustness and standby leakage current, the new proposed ESD clamp circuit of this work has provided an excellent ESD solution in advanced nanoscale CMOS technologies.

Table 2.5

Comparison among the Proposed Power-Rail ESD Clamp Circuit and Prior Works

	Traditional RC-based ESD protection (Fig. 2.1)		Modified ESD clamp circuit with timer level restorer (Fig. 2.2)	This work (Fig. 2.5)
	ESD Detection Circuit Only	With M_{ESD} W = 400μm L = 0.12μm	ESD Detection Circuit Only	W_{Mp1} = 80μm W_{SCR} = 45μm
Standby leakage current under 1-V bias at 25°C	2.33 μA	3.74 μA	~1.5 μA (simulation)	96 nA
Standby leakage current under 1-V bias at 125°C	26.9 μA	44.8 μA	n/a	1.02 μA
HBM ESD level	n/a	3250 V	n/a	7000 V
Function of ESD detection circuit	poor		good	good
Overall performance	poor		middle	excellent

2.5 Summary

A power-rail ESD clamp circuit with ultra-low standby leakage current and high robust ESD performance has been successfully verified in a 65-nm CMOS process. The proposed

ESD detection circuit designed with consideration of gate leakage current has been verified with a standby leakage current of only 96nA under 1-V bias at 25°C. Compared with the traditional power-rail ESD clamp circuit, the new proposed power-rail ESD clamp circuit achieves high ESD robustness in a small layout area with an ultra-low standby leakage current and is an excellent circuit solution for on-chip ESD protection design in nanometer CMOS technologies.

Chapter 3

Low Leakage ESD Protection Design for 2×VDD Mixed-Voltage I/O Circuits

In this chapter, a new high-voltage-tolerant ESD clamp circuit is proposed to protect the mixed-voltage I/O circuits for receiving signals with 2×VDD voltage level. The devices used in the high-voltage-tolerant ESD protection design are all 1V low-voltage thin gate-oxide NMOS/PMOS devices which can be safely operated under the 1.8V bias conditions without suffering from the gate-oxide reliability issue. The gate current of each thin gate devices in the high-voltage-tolerant ESD detection circuit has also been considered. By using the ESD protection scheme with the ESD bus and the proposed high-voltage-tolerant ESD clamp circuit, the mixed-voltage I/O circuit can be well protected. The four mode (PS, NS, PD, and ND) ESD stresses on the mixed-voltage I/O circuits can be effectively discharged. The new proposed circuit has been fabricated in a 1-V 65-nm CMOS process for protecting 1-V/1.8-V mixed-voltage I/O circuit.

3.1 Background

The ESD protection schemes with only 1×VDD thin gate-oxide devices for the mixed-voltage I/O interfaces to drive or receive 2×VDD high-voltage signals, with power supply voltage of 2×VDD is shown in Fig. 3.1. From Fig. 3.1, the ESD protection scheme can be implemented by placing diode from I/O pad to the power pad of 2×VDD with an efficient 2×VDD-tolerant ESD clamp circuit between 2×VDD and VSS. However, this protection scheme can not be applied if the power supply voltage is only VDD due to the leakage current path across the top-side diode Dp. The ESD bus (realized by wide metal line in CMOS process) is applied to solve this problem. The ESD protection schemes with only 1×VDD thin gate-oxide devices for the 2×VDD-tolerant mixed-voltage I/O interfaces with power supply voltage of VDD is shown in Fig. 3.2. The ESD bus is not directly connected to

an external power pad, but is initially biased at VDD through the diode D1 after the chip has been powered on. When the 2×VDD input signals reach to the I/O pad (Fig. 3.2), the ESD bus line will be charged up to 2×VDD through Dp. Therefore, the ESD clamp circuit between ESD bus and VSS should be also designed to tolerant 2×VDD supply voltage during normal circuit operating conditions.

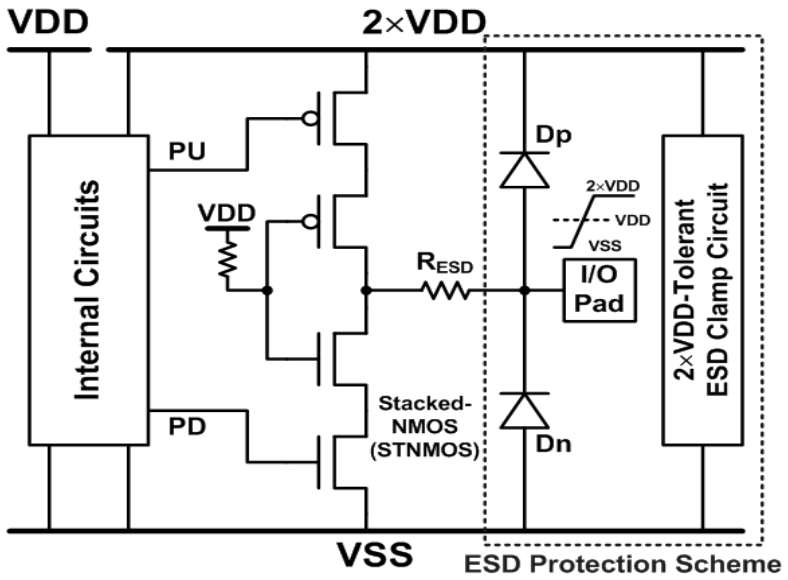


Fig. 3.1. ESD protection schemes for mixed-voltage I/O interface with 2×VDD-tolerant ESD clamp circuit, where the power supply is powered by voltage level of 2×VDD.

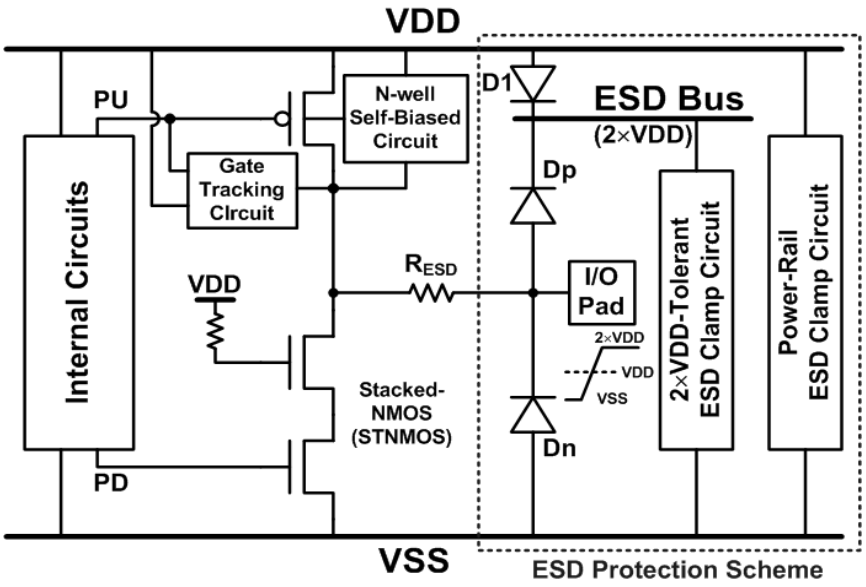


Fig. 3.2. ESD protection schemes for mixed-voltage I/O interface with ESD bus and 2×VDD-tolerant ESD clamp circuit, where the power supply is powered by voltage level of VDD.

Both ESD protection schemes (Fig. 3.1 and Fig. 3.2) need a 2×VDD-tolerant ESD clamp circuit to protect the stacked-NMOS in the mixed-voltage I/O buffer. The R_{ESD} is used to avoid damage on the stacked-NMOS before the ESD current is discharged through this ESD protection scheme. The diode D1 connected between the VDD and ESD bus is used to block the leakage current path from the I/O pad to VDD.

For the ESD protection scheme with ESD bus, under positive-to-VSS (PS-mode) ESD stress on I/O pad, the ESD current can be discharged through the diode Dp to the ESD bus and then through the 2×VDD-tolerant ESD clamp circuit to the grounded VSS, instead of through stacked NMOS in the I/O buffer to ground. Under positive-to-VDD (PD-mode) ESD stress on I/O pad, the ESD current can be discharged through Dp, ESD bus, and the 2×VDD-tolerant ESD clamp circuit to VSS power line, and then through the power-rail ESD clamp circuit between VDD and VSS to the grounded VDD. Under negative-to-VSS (NS-mode) ESD stress on I/O pad, the negative ESD current can be discharged through the diode Dn in forward-biased condition to the grounded VSS. Under negative-to-VDD (ND-mode) ESD stress on I/O pad, the negative ESD current can be discharged through Dn to the floating VSS power line, and then through the power-rail ESD clamp circuit between VDD and VSS to the grounded VDD. These four modes of ESD stresses on the mixed-voltage I/O pad to VDD or VSS have the corresponding well-designed ESD discharging paths in the ESD protection scheme with ESD bus.

3.2 Review on High-Voltage-Tolerant ESD Power-Rail ESD Clamp Circuit with Consideration of Gate Current

Recently, an ESD protection design with on-chip ESD Bus and high-voltage-tolerant ESD clamp circuit with only thin gate-oxide devices has been successfully verified in 0.13-μm CMOS process [77]. However, the prior designs did not consider the effect of gate leakage current if such circuits are further implemented in nanometer CMOS processes. New designs on the high-voltage-tolerant power-rail ESD clamp circuit for mixed-voltage I/O interfaces need to be developed to further reduce such standby leakage current in nanometer CMOS processes.

The prior work of the 2×VDD-tolerant ESD clamp circuit used to protect the mixed-voltage I/O buffers is redrawn and shown in Fig. 3.3. Based on BSIM4 model, the STNMOS in Fig. 3.3 with large device size as ESD clamp device generates some leakage

current from VDD_H to VDD via the gate of Mn1. Furthermore, the sub-threshold leakage current of the STNMOS in a nanoscale CMOS technology is also large. In the ESD detection circuit, the MOS capacitor with gate oxide of large area will induce a large amount of gate current from node a to VDD under the normal circuit operating condition. Therefore, the leakage current path exists from VDD_H through R1, Mc1, and R to VDD. Such gate current causes a voltage drop across the resistor R1, and therefore the PMOS Mp1 in the ESD detection circuit can not be completely turned off. With a non-turned-off PMOS, node d could be charged up to some voltage level higher than VSS, and that in turn provides some triggered current into the substrate of STNMOS under the normal circuit operating condition. The STNMOS with weak triggered current could further induce extra leakage current. Both the ESD detection circuit and STNMOS in this prior work suffer serious leakage current issue when this ESD clamp circuit is implemented in a nanoscale CMOS technology. By simulation with 65-nm SPICE parameters provided by foundry, the leakage current of STNMOS with W/L of 320μm/0.12μm under the bias conditions of VDD_H of 1.8V and VDD of 1V is higher than 1μA. The standby leakage current of the prior work of whole ESD clamp circuit will cause a considerable leakage current of several micro-Amperes under the normal circuit operating condition with VDD_H of 1.8V and VDD of 1V in a 65-nm CMOS process. Such a leaky ESD protection circuit is barely tolerable for low power requirements.

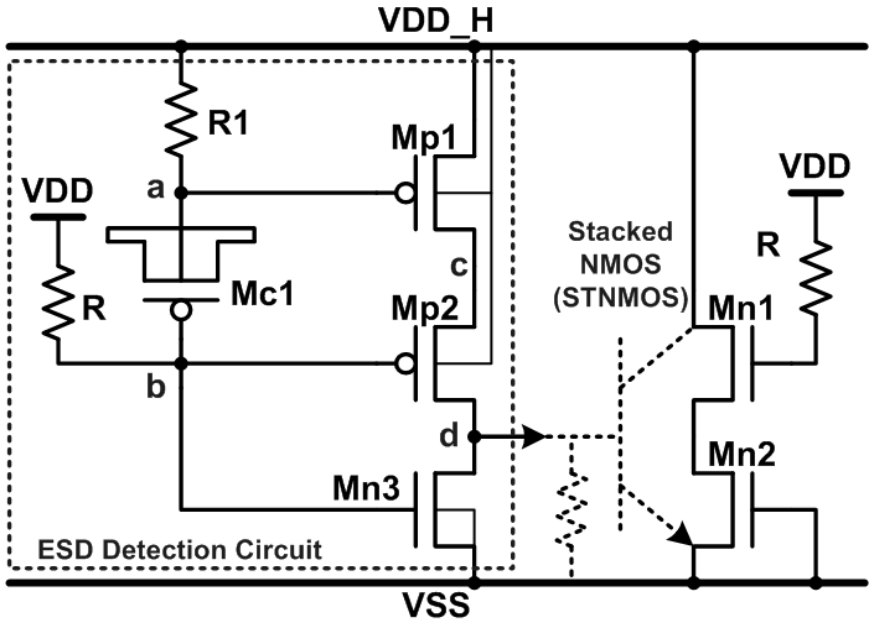


Fig. 3.3. The prior work of the 2×VDD-tolerant power-rail ESD clamp circuit used to protect the mixed-voltage I/O buffers [77].

To overcome the gate leakage current in the MOSFET with thin gate oxide, one solution is to use the thick gate-oxide device (realized with additional mask and process steps) to implement the MOS capacitor in the ESD detection circuit. The new 2×VDD-tolerant power-rail ESD clamp circuit designed with only thin gate-oxide (1×VDD) devices to achieve low standby leakage current is proposed. By using the new proposed circuit solution with only thin gate-oxide devices, the standby leakage current of the 2×VDD-tolerant power-rail ESD clamp circuit can be successfully reduced under the normal circuit operating condition.

3.3 Low-Leakage 2×VDD-Tolerant Power-Rail ESD Clamp Circuit

The proposed low-leakage 2×VDD-tolerant power-rail ESD clamp circuit is shown in Fig. 3.4. The new proposed ESD clamp circuit is realized with only 1-V thin oxide devices to operate under 1.8-V VDD_H without suffering the gate-oxide reliability issue. The whole ESD clamp circuit is composed of two parts, the ESD detection circuit and the ESD clamp device. The p-type substrate-triggered SCR device is used as the main ESD clamp device. The ESD detection circuit is used to improve the turn-on speed of the SCR device with substrate-triggered mechanism. Recently, a dual-base triggered SCR with trigger circuit have been reported to achieve low leakage current and adjustable trigger voltage. Nevertheless, the ESD protection design was not considered to apply for a 2×VDD-tolerant mixed-voltage I/O buffer. The new ESD detection circuit with only 1-V thin oxide devices is designed with consideration of the gate current and gate-oxide reliability in this work. By utilizing the gate current to bias the ESD detection circuit and optimizing the voltage difference across the gates of the MOS capacitors, the gate leakage current through the MOS capacitor under the normal circuit operating condition can be reduced. The total leakage current resulted from the MOS capacitor in the ESD detection circuit can be minimized. Therefore, the leakage currents through the ESD clamp device (SCR) and the ESD detection circuit can be well controlled and minimized by this new proposed design.

In the proposed ESD detection circuit, the PMOS Mp1 and Mp2 are used as substrate driver to generate the substrate-triggered current into the trigger node of the SCR device during ESD stress event, but the substrate driver is kept off under the normal circuit operating

condition. The NMOS Mn is used to keep the trigger node (node d in Fig. 3.4) at VSS, so the ESD clamping device (SCR) is guaranteed to be turned off during the normal circuit operating condition. The RC time constant from R1, Mc1, Mc2, and the parasitic gate capacitance of Mn is designed around the order of ~μs to distinguish ESD stress event from the normal power-on condition. The diode-connected Mp3 and Mp4 are acted as a start-up circuit with initial gate-to-bulk current from VDD_H into the ESD detection circuit, and in turn to conduct some gate current of Mc1 to bias the nodes e and f. After that, the voltage level at node e will be biased at a specified voltage level to reduce the voltage difference across the gate of Mc1 and to minimize the gate leakage current through the MOS capacitors.

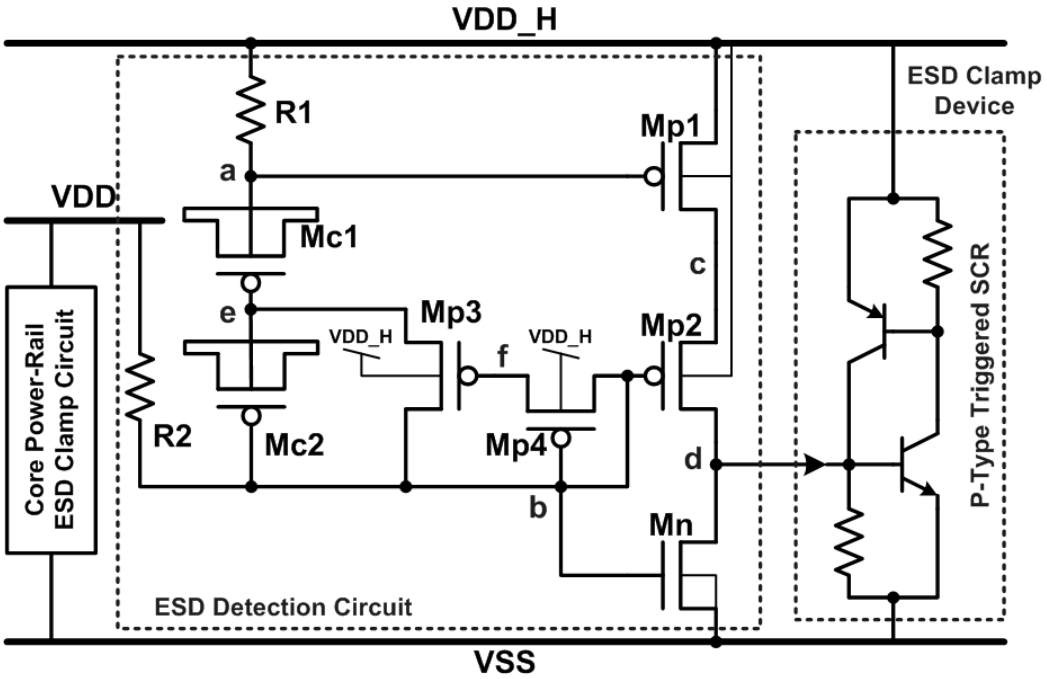


Fig. 3.4. The proposed low-leakage 2×VDD-tolerant power-rail ESD clamp circuit with p-type substrate-triggered SCR device as ESD clamp device, where the ESD detection circuit is designed with consideration of gate leakage current.

3.3.1 Design Procedure

The ESD detection circuit is implemented in a 65-nm CMOS process with VDD_H of 1.8V and VDD of 1V. While designing the dimensions of the devices in the ESD detection circuit, the voltage levels at node a, node b, and node d are assumed to be biased at VDD_H, VDD, and VSS, respectively, under the normal circuit operating condition. The gate-to-bulk current of the devices in the ESD detection circuit is also neglected because that is much

smaller than other current components. With consideration of the RC time constant, Mc1 and Mc2 are designed with the same device dimension, so that the voltage level at the node d is chosen at around 1.4V. The gate current of Mc1 is designed to be slightly larger than that of Mc2, and the different parts of the gate current can be conducted by Mp3.

The total gate current of Mc1 is equal to the total gate current through the gate oxide of Mn and Mp2, which can be derived as

$$Isg_{Mc1} + Idg_{Mc1} = Igd_{Mn} + Igs_{Mn} + Igs_{Mp2} + Igd_{Mp2}, \tag{3.1}$$

where Igd_{Mn} means the total gate-to-drain current of Mn including *Igcd* and *Igd* defined in [14], and the other current components are follow the same definition as Igd_{Mn}. The voltage differences between the source and drain (*Vds*) of both Mc1 and Mn are 0V, so that the gate-to-drain current and the gate-to-source current should be the same. Therefore, equation (1) can be simplified to the component of only gate-to-source current for Mc1 and Mn, which can be derived as

$$2 \cdot Isg_{Mc1} = 2 \cdot Igs_{Mn} + Igs_{Mp2} + Igd_{Mp2}. \tag{3.2}$$

The current flow from Mp1 to Mp2 is resulted from the gate-to-drain current of Mp1, which can be derived as

$$Igd_{Mp1} = Isg_{Mp2} + Id_{Mp2}, \tag{3.3}$$

where the drain current of Mp1 in off-state is neglected. The W/L of Mp1 and Mp2 are chosen as 80μm/0.12μm for enough driving capability to trigger on the SCR device during the ESD stress event. While voltage levels at the node a, b, and d are given, the voltage level of node c can be solved by equation (3.3) with the device parameters provided from foundry. Therefore, the total gate-to-source current of Mc1 (Isg_{Mc1}) in the equation (3.2) can be solved by the given voltage Vsg_{Mc1} of 0.4V. With consideration of the RC time constant, the W/L of MOS capacitor Mc1 is chosen as 5μm/5μm, and the total gate-to-source current of Mc1 can be determined. The device dimension of Mn can also be determined by equation (3.2). From Kirchhoff's Current Law, the current equation at the node b, e, and f can be expressed as

$$Igd_{Mn} + Igs_{Mn} = Isg_{Mc2} + Idg_{Mc2} + Id_{Mp3} + Igd_{Mp3} + Id_{Mp4} + Isg_{Mp4} + Isg_{Mp2} + Idg_{Mp2}, \tag{3.4}$$

$$Isg_{Mc1} + Idg_{Mc1} = Isg_{Mc2} + Idg_{Mc2} + Id_{Mp3} + Isg_{Mp3}, \text{ and} \tag{3.5}$$

$$Isg_{Mp3} = Id_{Mp4} + Isg_{Mp4}. \tag{3.6}$$

Likewise, the dimension of each device in the proposed ESD detection circuit can be derived through the equations (3.4)-(3.6). With fine tuning on the voltage level at the nodes e and f to achieve a minimized overall standby leakage current, the final dimension for each

device in the proposed ESD detection circuit implemented in a given 65-nm CMOS process is shown in Table 3.1. By adjusting the device dimensions of Mp1 and Mp2, the substrate-triggered current generated by the ESD detection circuit can be adjusted to accelerate the turn-on speed of the SCR device during ESD event.

Table 3.1

Dimensions of Devices in the ESD Detection Circuit of the New Proposed 2×VDD-Tolerant Power-Rail ESD Clamp Circuit

Devices	Dimension
Mc1	5μm/5μm
Mc2	5μm/5μm
Mn	5μm/0.8μm
Mp1	80μm/0.12μm
Mp2	80μm/0.12μm
Mp3	0.3μm/20μm
Mp4	0.3μm/20μm
R1	80kΩ
R2	1kΩ

3.3.2 Operation under Normal Circuit Operating Condition

During the normal circuit operating condition with VDD_H of 1.8V, VDD of 1V, and grounded VSS, the gate voltage (node a) of Mp1 is biased at around 1.8V through the resistor R1 with a low gate current of MOS capacitor Mc1 in the new proposed ESD detection circuit, so that Mp1 can be kept off and no trigger current is generated from the ESD detection circuit to the SCR device. In addition, the node b is biased at 1V through the 1-kΩ resistor of R2 to turn on Mn which in turn keeps the trigger node (node d) of the SCR device grounded. Due to the off-state Mp1, no current flows from VDD_H though Mp1 and Mp2 to VSS, so the Mp2 is also kept in off state. The source-to-gate voltage of Mp2 is less than the threshold voltage of a 1-V PMOS transistor, and therefore the node c is kept between 1V and (1V+|Vtp|). The node e is biased at ~1.4V and the node f is biased at some voltage level between that at node b (1V) and node e (~1.4V). Under such a bias condition, all 1-V devices in the proposed ESD

detection circuit are free from gate-oxide reliability issue under normal circuit operating condition. The HSPICE-simulated voltage waveforms at the nodes of the proposed ESD detection circuit during and after the normal power-on transition are shown in Fig. 3.5. VDD_H and VDD are powered on to 1.8V and 1V, respectively, with a simultaneous rise time of 1ms. From the simulation results, the voltage differences across the gate-to-drain, gate-to-source, and gate-to-bulk terminals of all devices in the proposed ESD detection circuit do not exceed the process limitation (1.1V for 1-V devices in a 65-nm CMOS process). Therefore, the ESD detection circuit can be ensured against gate-oxide reliability issue under the normal circuit operating condition.

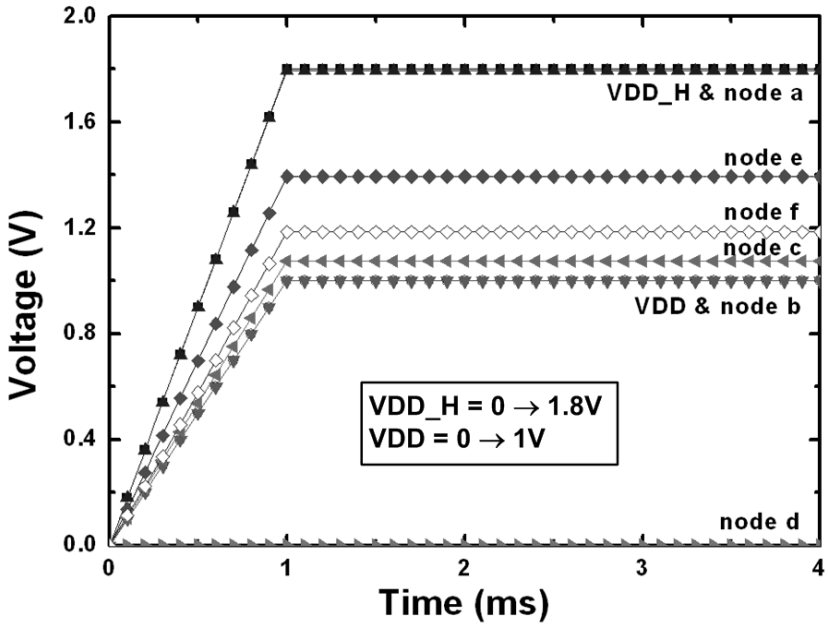


Fig. 3.5. HSPICE-simulated voltage on the nodes of the ESD detection circuit in a 65-nm CMOS process under the normal power-on condition with VDD_H of 1.8V and VDD of 1V.

3.3.3 Operation under ESD Transient Event

When a positive fast-transient ESD voltage is applied to VDD_H with VSS relatively grounded and VDD floating, the RC delay in the ESD detection circuit keeps the gate of Mp1 (node a) at a relatively low voltage level compared to the fast rising voltage level at VDD_H. The node b is initially floating via VDD with a voltage level of around 0V and charged up slowly due to the RC delay, too. The Mp1 and Mp2, whose initial gate voltages are at relatively low voltage levels compared to their source voltages, can be quickly turned on by the ESD energy to generate the substrate-triggered current into the trigger node (node d) of

the SCR device. Finally, the SCR device can be fully turned on into holding state to discharge the ESD current from VDD_H to VSS. Fig. 3.6 shows the simulated voltage and substrate-triggered current of the new proposed ESD detection circuit during the ESD transition, where a 0-to-5V voltage pulse with a rise time of 10ns is applied to VDD_H to simulate the fast transient voltage of HBM ESD event. With a limited voltage height of 5V in the voltage pulse, the voltage transition on each node in the ESD detection circuit can be simulated to check the desired circuit function before device breakdown. From the simulated results, the source-to-gate voltages of Mp1 and Mp2 are around 1.5V, which is much higher than their threshold voltage, and the substrate-triggered peak current generated from substrate driver is higher than 30mA during the ESD transition. With the proposed ESD detection circuit, the SCR device can be triggered on by the adequate substrate-triggered current before device breakdown during the ESD stress event.

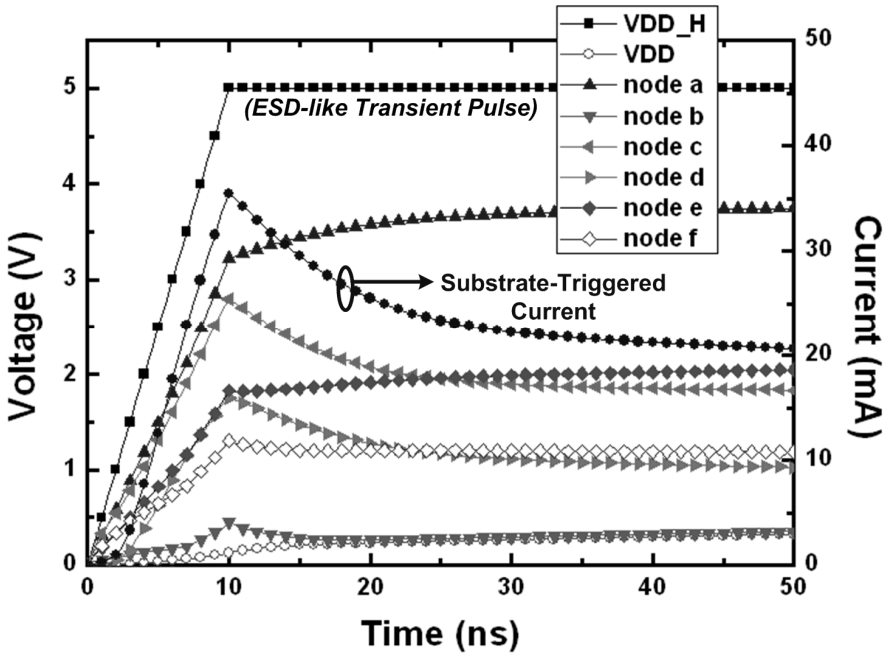


Fig. 3.6. HSPICE-simulated voltages on the nodes of the ESD detection circuit and the substrate-triggered current which flows into the SCR device under 0-to-5V ESD-like transition on VDD_H.

3.4 Experimental Results

The new proposed 2×VDD-tolerant power-rail ESD clamp circuit has been fabricated in a 65-nm CMOS process. All devices used in this design are 1-V fully-silicided devices, including the p-type substrate-triggered SCR device. The layout view of the proposed ESD

clamp circuit is shown in Fig. 3.7. The widths of SCR device as ESD clamping device are varied in 30μm, 45μm, and 60μm in the test chip to verify the corresponding ESD robustness. The prior work shown in Fig. 2 has also been fabricated in the same 65-nm CMOS process to compare the standby leakage current and ESD performance, where the dimension of the STNMOS and the devices in the ESD detection circuit is listed in Table 3.2.

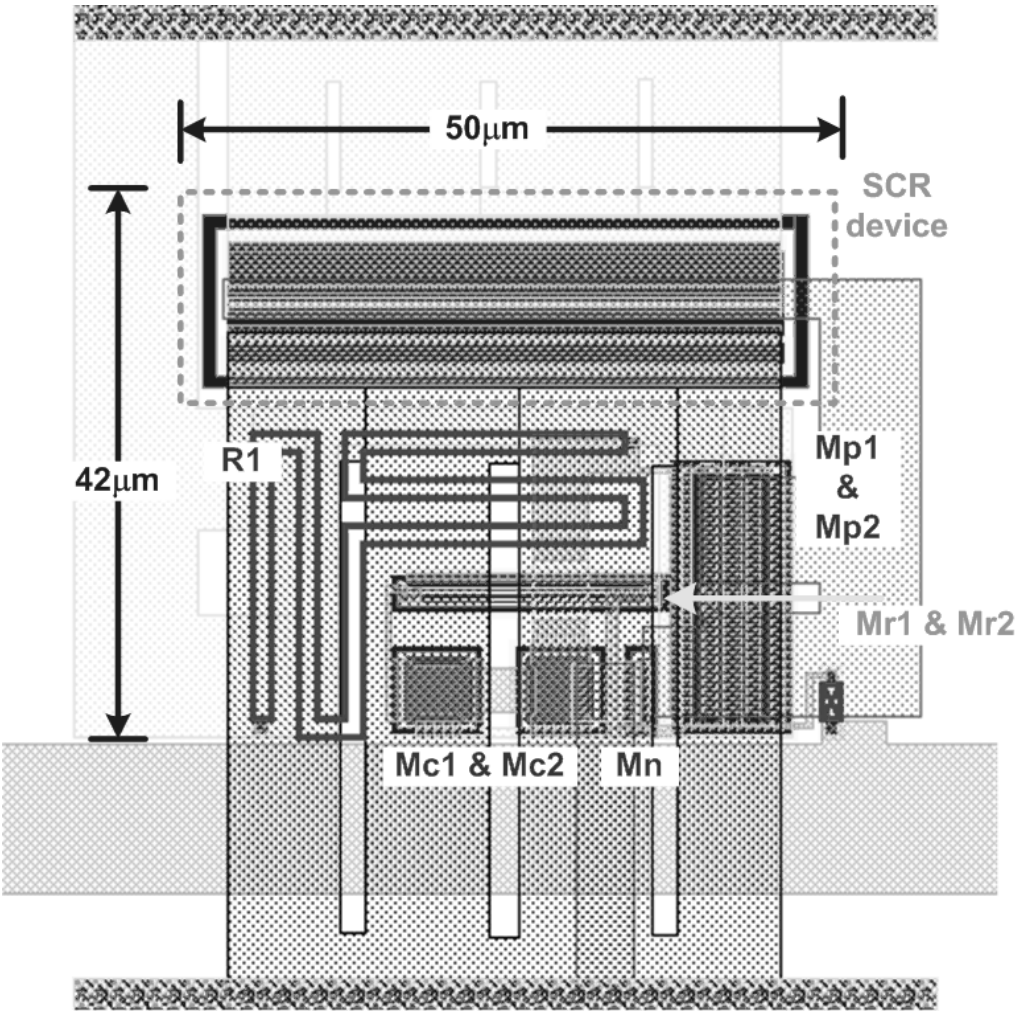


Fig. 3.7. Layout view of the proposed 2×VDD-tolerant power-rail ESD clamp circuit. The chip has been fabricated in a 65-nm CMOS process with 1-V devices.

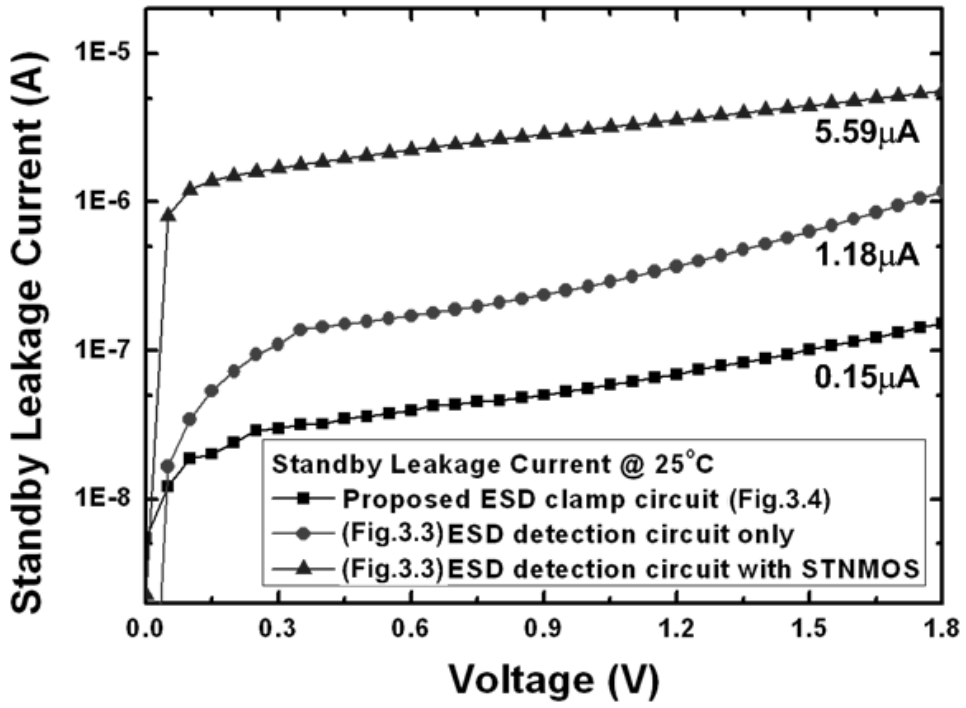
Table 3.2

Dimensions of Devices in the ESD Detection Circuit of the Previous 2×VDD-Tolerant Power-Rail ESD Clamp Circuit (Fig. 3.3)

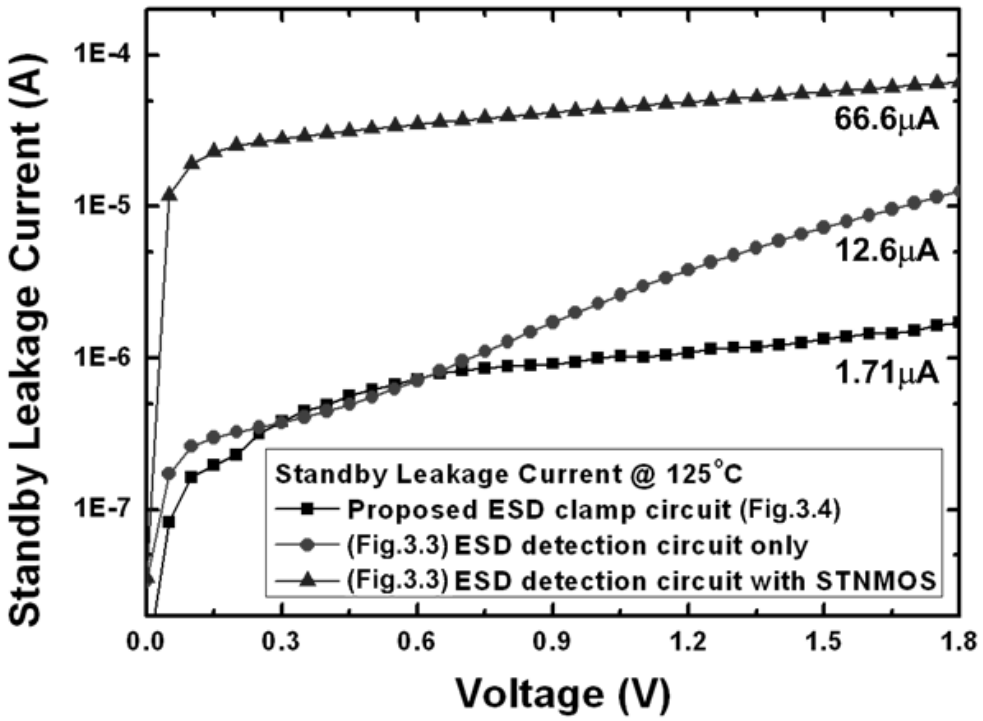
Devices	Dimension
Mc1	5μm/5μm
Mp1	80μm/0.12μm
Mp2	80μm/0.12μm
Mn1	320μm/0.12μm
Mn2	320μm/0.12μm
Mn3	5μm/0.8μm
R1	80kΩ
R	1kΩ

3.4.1 Standby Leakage Current

The measured standby leakage current of the fabricated 2×VDD-tolerant power-rail ESD clamp circuit under different temperatures are shown in Figs. 3.8(a) and 3.8(b), where the width of the SCR device is 45μm. The standby leakage current is measured by increasing the voltage of VDD_H from 0V to 1.8V and VDD from 0V to 1V simultaneously. The standby leakage current of the prior work (shown in Fig. 3.3) is measured under the same bias condition, and the results are also shown in Fig. 3.8. From the measured results, the standby leakage current of the proposed ESD clamp circuit is only 0.15μA under the temperature of 25^{o}C and 1.71 μA under the temperature of 125^{o}C. However, the standby leakage current of the ESD detection circuit in the prior work is as high as 1.18μA under the temperature of 25^{o}C and 12.6 μA under the temperature of 125^{o}C. With the STNMOS, the standby leakage current of the prior work increases to even 5.59μA under the temperature of 25^{o}C and 66.6 μA under the temperature of 125^{o}C. The standby leakage current of both the ESD detection circuit and the ESD clamp device (SCR) in this work are much smaller than that in the prior work. The proposed 2×VDD-tolerant ESD clamp circuit can achieve a low standby leakage current compared with the prior work. With such a low leakage current, the proposed ESD clamp circuit is suitable for portable or low-power applications, especially when chips are powered by small batteries.



(a)



(b)

Fig. 3.8. The standby leakage current of the proposed ESD clamp circuit and the prior work of ESD detection circuit with and without STNMOS in Fig. 2 at (a) 25°C and (b) 125 °C.

3.4.2 Turn-on Verification

The turn-on behavior of SCR device used as ESD clamp device is an important index for ESD protection. To verify the turn-on efficiency of the proposed ESD clamp circuit, a square-type voltage pulse with a rise time of ~10ns and a pulse height of 5V is used to simulate the rising edge of a positive-to-VSS HBM ESD pulse. When the positive voltage pulse is applied to VDD_H of the proposed 2×VDD-tolerant ESD clamp circuit with VSS grounded and VDD floating, the ESD-like voltage pulse will start the ESD detection circuit to trigger on the SCR device, and in turn to provide a low-impedance path from VDD_H to VSS. The voltage waveform on the VDD_H pin clamped by the ESD clamp circuit is shown in Fig. 3.9. The applied 5-V voltage pulse is clamped down quickly to a low voltage level (~2V) by the proposed ESD clamp circuit with a SCR device width of 45μm. The turn-on time is ~15ns, as observed from the maximum voltage peak to the clamped low voltage level in Fig. 3.9. From the measured voltage waveform, the excellent turn-on efficiency of the proposed ESD clamp circuit during the ESD stress event has been successfully verified.

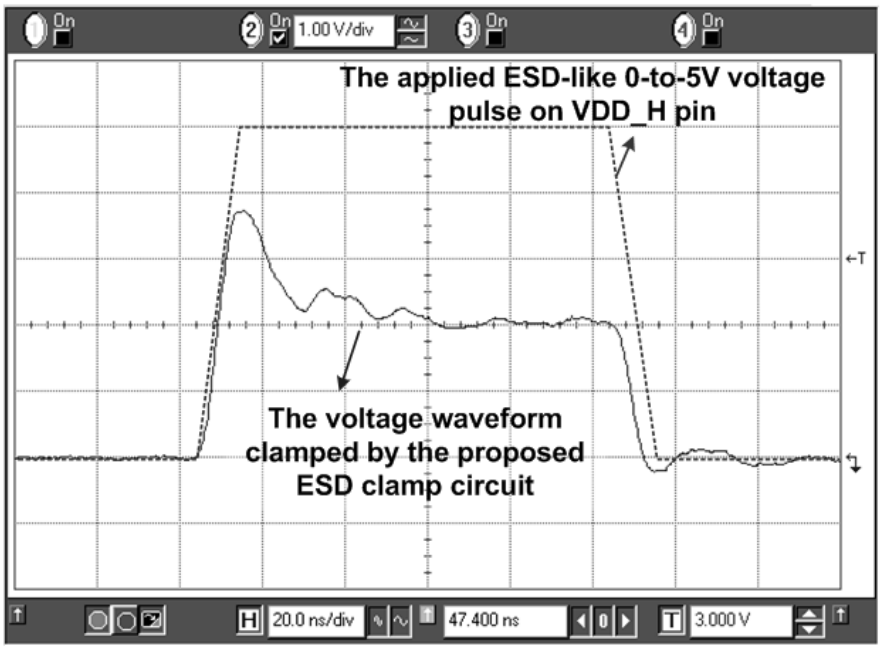


Fig. 3.9. The measured voltage waveforms clamped by the proposed 2×VDD-tolerant ESD clamp circuit by applying a 0-to-5V voltage pulse to VDD_H of the proposed ESD clamp circuit with VSS grounded and VDD floating. (Y axis: 1V/div.; X axis: 20ns/div.)

3.4.3 ESD Robustness

To investigate the turn-on behavior of the ESD clamping device with ESD detection circuit during the ESD stress event, TLP generator with a pulse width of 100ns and a rise time of ~2ns is used to measure the It2 of the proposed 2×VDD-tolerant ESD clamp circuit. The TLP-measured I-V characteristics of the ESD clamp circuit with SCR device of different widths are shown in Fig. 3.10. The ESD clamp circuit with SCR widths of 30μm, 45μm, and 60μm can achieve It2 of 3.15A, 4,71A, and 6.17A, respectively. Without any triggered mechanism, the original trigger voltage of the stand alone SCR device is as high as ~11.5V. However, with the proposed ESD detection circuit in this work, the trigger voltage of the SCR device is reduced to only around 3 to 4V, depending on the SCR width. Therefore, the low trigger voltage and high It2 value of the 2×VDD-tolerant ESD clamp circuit can ensure the effective ESD protection capability. The It2 level measured by TLP is proportional to the SCR device width, so the turn-on uniformity of the SCR device has been verified. By increasing the SCR device width, the higher It2 level can be achieved. The holding voltage of the 2×VDD-tolerant ESD clamp circuit is around 2V. Such a holding voltage is higher than the voltage level of VDD_H (1.8V) under the normal circuit operating condition. Even if the SCR device is mis-triggered due to any noise disturbance from the environment of applications, it will be automatically turned off after the noise source is removed. Therefore, the new proposed 2×VDD-tolerant power-rail ESD clamp circuit is free from latchup issue in this design with VDD_H of 1.8V. Once a higher holding voltage is needed for save guardband to prevent latchup issue, the stacked diode structure can be added in series with SCR to increase its overall holding voltage.

The TLP-measured I-V curve of the stacked NMOS in the mixed-voltage I/O buffer (fabricated in the same CMOS process) is shown in Fig. 3.11. The trigger voltage of the stacked NMOS in the mixed-voltage I/O buffer is around 6V, which is much higher than the trigger voltage (~4V) of the proposed ESD protection circuit, as shown in Fig. 3.10. Therefore, the proposed ESD protection circuit can be turned on before the drain junction breakdown of the stacked NMOS in the mixed-voltage I/O buffers.

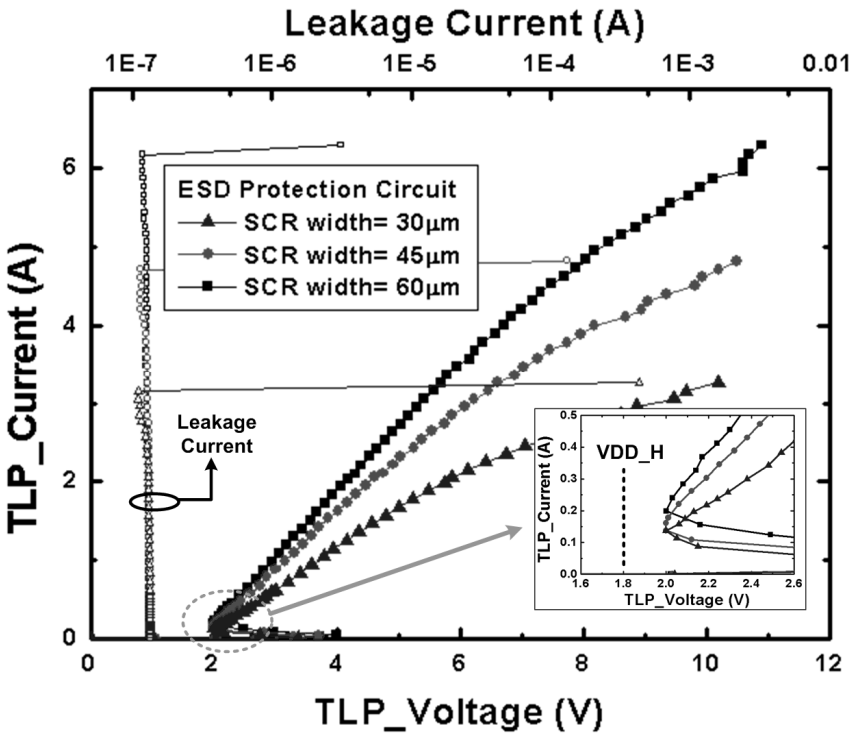


Fig. 3.10. The TLP-measured I-V characteristics of the proposed power-rail ESD clamp circuit with SCR device of different widths under positive VDD_H-to-VSS ESD stress. The TLP pulse used in this measurement is with pulse width of 100ns and rise time of ~2ns. The inset figure showed the room-in view on the snapback holding point, where the holding voltage is ~2V.

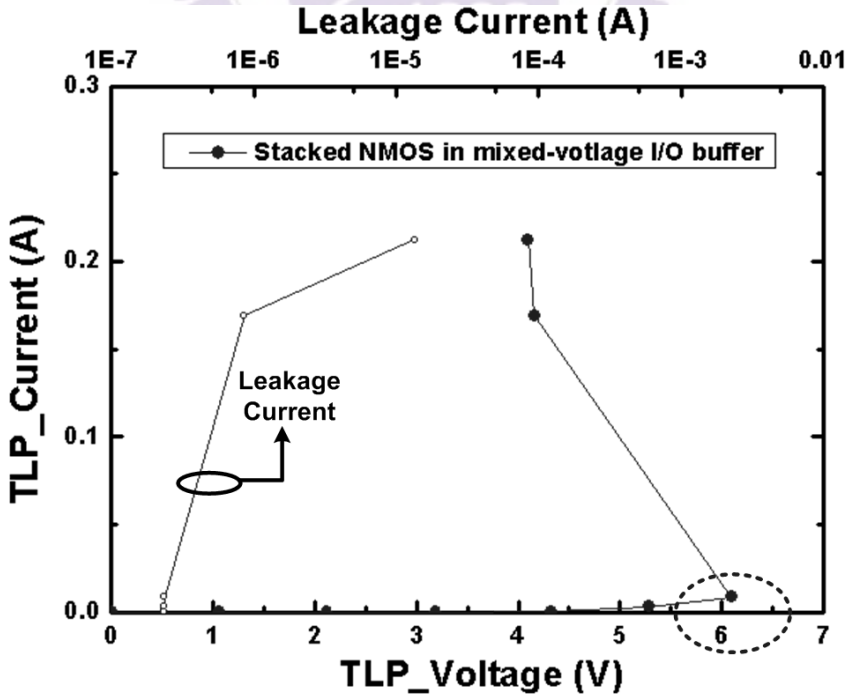


Fig. 3.11. The TLP-measured I-V curve of the stacked NMOS in the mixed-voltage I/O buffer. The trigger voltage of the stacked NMOS in the mixed-voltage I/O buffer is around 6V.

The HBM ESD levels and MMESD levels of the proposed 2×VDD-tolerant power-rail ESD clamp circuit with SCR of different widths under positive VDD_H-to-VSS ESD stress are listed in Table 3.3. The failure criterion is defined as the I-V characteristic curve shifting over 20% from its original curve after three continuous ESD zaps at every ESD test voltage level. The HBM ESD levels of the ESD clamp circuit with SCR width of 30μm, 45μm, and 60μm are 4.25kV, 6.5kV, and larger than 8kV, respectively. Besides, the MM ESD levels of the ESD clamp circuit with SCR width of 30μm, 45μm, and 60μm are 225V, 350V, and 450V, respectively, in a 65-nm CMOS process. The corresponding It2 measured by TLP is also listed in Table 3.3.

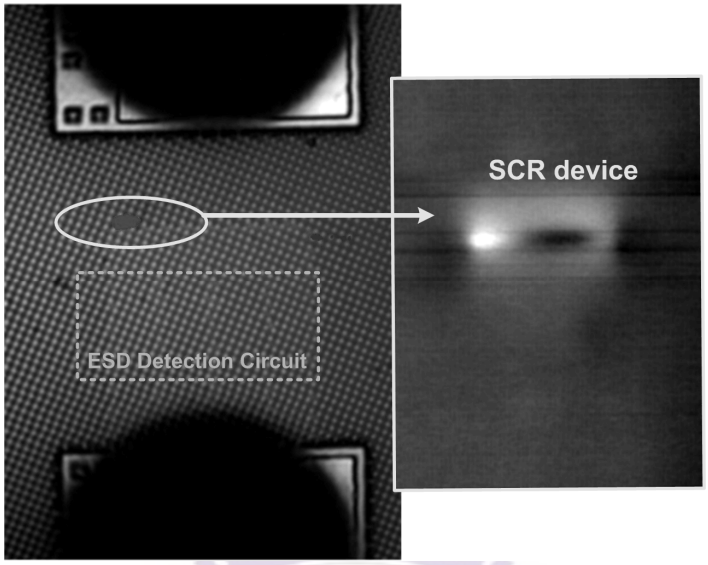
Table 3.3
ESD Robustness of the Proposed Power-Rail ESD Clamp Circuit with SCR Device of Different Widths

SCR Width	It2	HBM ESD Level	MM ESD Level
30μm	3.15A	4.25kV	225V
45μm	4.71A	6.5kV	350V
60μm	6.17A	> 8kV	450V

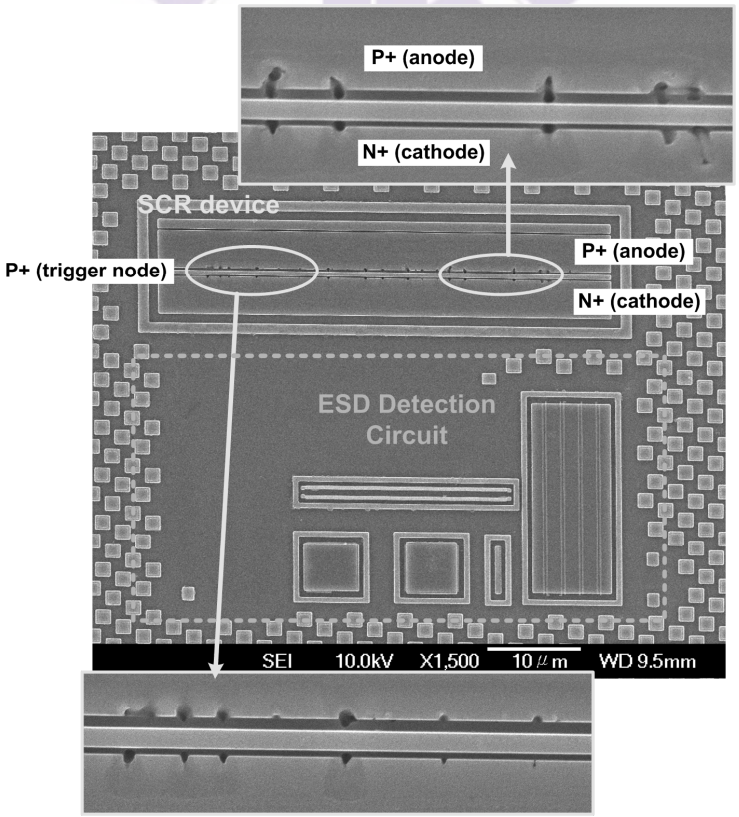
3.4.4 Failure Analysis

The experimental results have shown that the turn-on speed of SCR device can be substantially improved by the proposed ESD detection circuit. Failure analyses carried out by OBIRCH [78] and SEM [79] images provide the visual evidence for that the SCR device can be triggered on uniformly by the ESD detection circuit. Fig. 3.12 shows the ESD failure location of the proposed ESD clamp circuit with SCR width of 45μm after 6.75kV VDD_H-to-VSS HBM ESD stress. When ESD transient events occur, the ESD detection circuit conducts some initial ESD current to trigger on the SCR device. After the SCR device is turned on, it provides a path with low impendence to conduct ESD current to VSS, so that most of ESD current is discharged through the SCR device. The electrical abnormal region of the ESD clamp circuit after ESD stress locates on the SCR device instead of the ESD detection circuit, as the OBIRCH image shown in Fig. 3.12(a). The SEM image of this ESD-damaged SCR device with ESD detection circuit is shown in Fig. 3.12(b). The failure

spots were found at the anode-to-cathode path along the entire width of SCR device, indicating that the SCR device can be uniformly turned on through the design of ESD detection circuit in this work.



(a)



(b)

Fig. 3.12. (a) After 6.75kV VDD_H-to-VSS HBM ESD stress, the electrical abnormal region of the ESD clamp circuit was located at the SCR device. (b) The failure spots were found at the anode-to-cathode path of the SCR device.

3.4.5 Discussion

From the simulation, the ratios of gate leakage current to sub-threshold leakage current in the ESD detection circuit of the prior work and this work are 9.9:1 and 3.1:1 under VDD_H of 1.8V and VDD of 1V at 25°C, respectively. Both the total amount of leakage current and the component of gate leakage current are reduced by the proposed design. The performance comparison between the prior work and the new proposed design of this work is shown in Table 3.4. Even the STNMOS with the leaky poly structure is excluded, the standby leakage currents of the ESD detection circuit in the prior work under VDD_H of 1.8V and VDD of 1V at 25°C and 125°C are still as large as 1.18μA and 12.6μA, respectively. The standby leakage currents of the proposed ESD clamp circuit with SCR of 45μm under VDD_H of 1.8V and VDD of 1V at 25°C and 125°C are only 0.15μA and 1.71μA, respectively. The HBM (MM) ESD level of the prior work with STNMOS of W/L = 320μm/0.12μm is 4kV (250V). However, the HBM (MM) ESD level of the proposed ESD clamp circuit with SCR width of 45μm in this work can achieve 6.5kV (350V). With consideration of ESD robustness and standby leakage current, the new proposed 2×VDD-tolerant ESD clamp circuit in this work has provided an excellent ESD solution for mixed-voltage I/O interfaces in advanced nanoscale CMOS technologies.

Table 3.4

Comparison between the Proposed Power-Rail ESD Clamp Circuit and Prior Work

	Prior work (Fig. 3.2)		This work (Fig. 3.3)
	ESD Detection Circuit Only	With STNMOS W = 320μm L = 0.12μm	ESD Detection Circuit + SCR W_{SCR} = 45μm
Standby leakage current at 25°C	1.18μA	5.59μA	0.15μA
Standby leakage current at 125°C	12.6μA	66.6μA	1.71μA
HBM ESD Level	n/a	4kV	6.5kV
MM ESD Level	n/a	250V	350V

3.5 Summary

A new 2×VDD-tolerant power-rail ESD clamp circuit with low standby leakage current

and high robust ESD performance has been successfully verified in a 65-nm CMOS process. The proposed 2×VDD-tolerant power-rail ESD clamp circuits realized with only low-voltage (1×VDD) devices can effectively protect the mixed-voltage I/O buffers without gate-oxide reliability issue under the normal circuit operating conditions. The proposed ESD detection circuit, designed with consideration of gate leakage current, has been verified with a very small standby leakage current of only 0.15μA under 1.8-V bias at 25°C, and has also shown the effectiveness on reducing the trigger voltage of the SCR device. Compared with the prior work, the new proposed power-rail ESD clamp circuit with advantages of low standby leakage current, high ESD robustness, and no gate-oxide reliability issue is an excellent circuit solution for on-chip ESD protection design for mixed-voltage I/O buffers in nanometer CMOS technologies.

Chapter 4

3×VDD-Tolerant Power-Rail ESD Clamp Circuit

In this chapter, two new ESD protection design by using only 1×VDD low-voltage devices for mixed-voltage I/O buffer with 3×VDD input tolerance are proposed. Two different special high-voltage-tolerant ESD detection circuits are designed with substrate-triggered technique to improve ESD protection efficiency of ESD clamp device. These two ESD detection circuits with different design concepts both have effective driving capability to trigger the ESD clamp device on. These ESD protection designs have been successfully verified in two different 130nm 1.2-V CMOS processes to provide excellent on-chip ESD protection for 1.2-V/3.3-V mixed-voltage I/O buffers [80]-[82].

4.1 Background

The mixed-voltage I/O design with NMOS blocking technique is applied for receiving 3×VDD, 4×VDD, and even 5×VDD input signals without the gate-oxide reliability issue. The mixed-voltage I/O buffer to receive 3×VDD input signals by using only 1×VDD low-voltage devices without suffering gate-oxide reliability issue has been proposed [83]. Nevertheless, the ESD protection design for such a 3×VDD-tolerant mixed-voltage I/O buffer was not considered. To achieve a good whole-chip ESD protection scheme for the 3×VDD-tolerant mixed-voltage I/O interface, it is required to design the low leakage power-rail ESD clamp circuit with only low-voltage devices that can sustain the high power-supply voltage (3×VDD) without suffering gate-oxide reliability. Recently, the ESD protection scheme for the 3.3-V mixed-voltage I/O buffers with 1-V/2.5-V dual gate low-voltage devices has been successfully verified in 0.13μm CMOS process [84]. However, this prior design still needs extra mask-set to implement the thick gate-oxide devices (2.5V devices). Therefore, how to design an effective ESD protection circuit with only low-voltage devices without suffering gate-oxide reliability for mixed-voltage I/O buffer with 3×VDD input tolerance is a significant challenge.

4.2 ESD Protection Scheme for 3×VDD-Tolerant Mixed-Voltage I/O Buffer

To improve ESD robustness of the mixed-voltage I/O interfaces, an ESD protection concept by using the on-chip ESD bus had been reported. However, in this prior art, the gate-oxide reliability was not considered in its circuit implementation. With consideration on the gate-oxide reliability, the new ESD protection scheme for mixed-voltage I/O buffer with 3×VDD input tolerance is shown in Fig. 4.1. The circuit design for 3×VDD-tolerant I/O buffer realized with only 1×VDD devices has been reported in [83]. In the 3×VDD I/O buffer, the dynamic gate-bias circuit controls the gate voltages of the stacked NMOS as shown in Fig. 4.1. When the I/O buffer receives a logic high (3×VDD), the gate voltages of the stacked NMOS are biased at VDD and 2×VDD from left to right, respectively. When operating at other receiving or transmitting modes, the stacked NMOS can also be well biased by the dynamic gate-bias circuit. Therefore, the 3×VDD I/O buffer can tolerate 3×VDD input signals without gate-oxide reliability issue. The detailed circuit implantation to realize such dynamic gate-bias circuit, which can trace the voltage level at the I/O pad, can be found in [83].

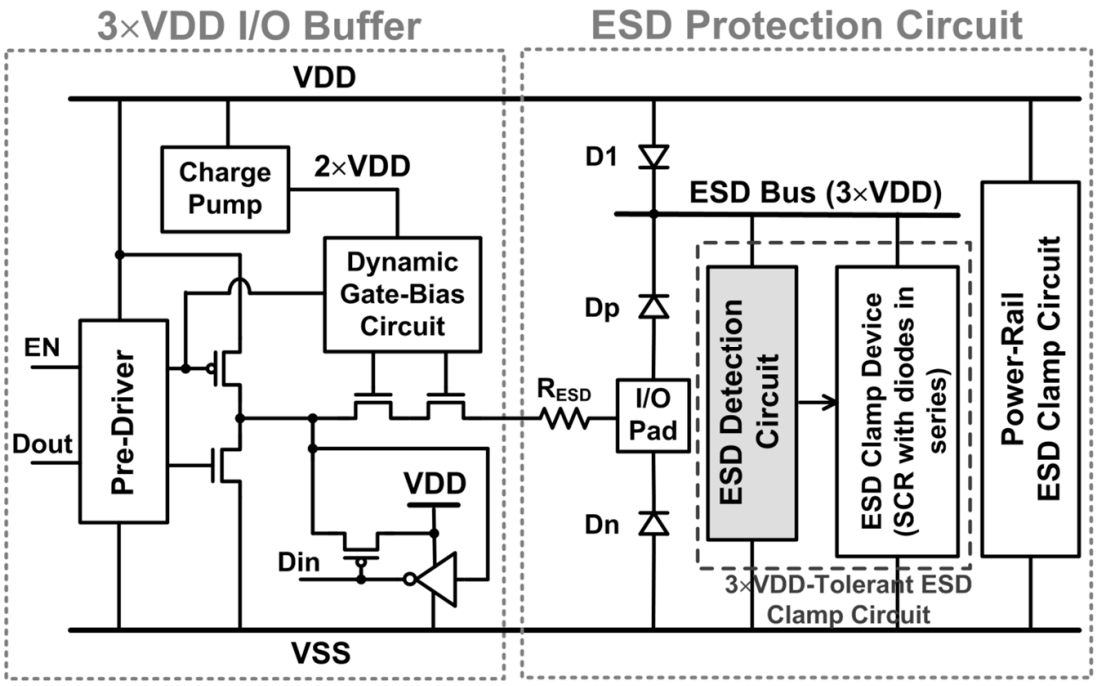


Fig. 4.1 The proposed ESD protection scheme for mixed-voltage I/O buffer with 3×VDD input tolerance realized with only 1×VDD devices.

To receive the input signals with 3.3-V voltage level, the traditional ESD protection with direct diode connection from I/O pad to VDD of 1.2V is forbidden. Therefore, the ESD protection circuit is realized with diodes Dp, Dn, D1, ESD bus, ESD detection circuit, ESD clamp device, and the power-rail ESD clamp circuit between VDD and VSS, as shown in Fig. 4.1.

Under positive-to-VSS (PS-mode) ESD stress on I/O pad, the ESD current can be discharged through the diode Dp to the ESD bus and then through the ESD clamp device (SCR) to the grounded VSS, instead of through stacked NMOS in the I/O buffer to ground. Under positive-to-VDD (PD-mode) ESD stress on I/O pad, the ESD current can be discharged through Dp, ESD bus, and the ESD clamp device to VSS power line, and then through the power-rail ESD clamp circuit between VDD and VSS to the grounded VDD. Under negative-to-VSS (NS-mode) ESD stress on I/O pad, the negative ESD current can be discharged through the diode Dn in forward-biased condition to the grounded VSS. Under negative-to-VDD (ND-mode) ESD stress on I/O pad, the negative ESD current can be discharged through Dn to the floating VSS power line, and then through the power-rail ESD clamp circuit between VDD and VSS to the grounded VDD. The four modes of ESD stresses on the mixed-voltage I/O pad to VDD or VSS have the corresponding well-designed ESD discharging paths in the proposed ESD protection scheme.

When an ESD stress is applied to the I/O pad, the transient voltage-limiting criteria of the 3×VDD tolerant I/O buffer can be expressed as

$$V_{\max} = I_{ESD} \times R_{ESD} + V_{BD\_NMOS}, \quad (1)$$

where $V_{\max}$ is the maximum transient voltage that the 3×VDD I/O buffer can sustain, I_{ESD} is the ESD current, and the V_{BD_NMOS} is the transient breakdown voltage of the stacked NMOS between the R_{ESD} and VSS in Fig. 4.1. Under the ESD stress event, all nodes in the 3×VDD I/O buffer are floating initially. The transient breakdown voltage V_{BD_NMOS} is given by the drain breakdown voltage of the stacked NMOS in the 3×VDD I/O buffer. In order to prevent the ESD current from injecting into the 3×VDD I/O buffer, the trigger voltage and the clamp voltage of the 3×VDD-tolerant ESD clamp circuit should be less than $V_{\max}$. The clamp voltage of the 3×VDD-tolerant ESD clamp circuit can be expressed as

$$V_{clamp} = V_D + V_{hold} + I_{ESD} \times R_{on}, \quad (2)$$

where V_D is the voltage drop across the diode Dp, V_{hold} is the holding voltage of the 3×VDD-tolerant ESD clamp circuit, and R_{on} is the equivalent turn-on resistance of the diode Dp, parasitic routing resistance, and the 3×VDD-tolerant ESD clamp circuit. Therefore, R_{ESD}

should be designed to be slightly greater than some critical value to make sure that V_{clamp} is less than V_{max}. The criterion of R_{ESD} can be found as

$$R_{ESD} > R_{on} + \frac{V_D + V_{hold} - V_{BD\_NMOS}}{I_{ESD}}. \quad (3)$$

In this work, V_{BD_NMOS} of ~7.5V is measured from the breakdown voltage of the stacked NMOS. For a V_D of 0.7V, V_{hold} of 3.3V, and R_{on} of 3 ohm, the resistance R_{ESD} should be greater than 0.4 ohm and 1.7 ohm for 2kV (I_{ESD} of 1.33A) and 4kV (I_{ESD} of 2.66A) HBM ESD levels, respectively. Under these criteria, the ESD current is discharged through the proposed ESD protection circuit rather than the 3×VDD I/O buffer under ESD stress, so that the stacked NMOS in the 3×VDD I/O buffer can be safely protected by the proposed ESD protection scheme in Fig. 4.1.

The power-rail ESD clamp circuit between VDD and VSS can be realized by the traditional RC-based ESD detection circuit. To solve the latch-up issue, several diodes are added in series with SCR as the ESD clamp device to increase its overall holding voltage for such (3.3-V) mixed-voltage I/O buffer. Because these two ESD protection design were implemented in two different foundries, the electrical characteristic of SCR devices used as ESD clamp device were quite different. The holding voltage of SCR device is dominated by the doping profiles correlated with the process of each foundry, and therefore the numbers of diodes added in series with SCR for two ESD clamp circuit are different to avoid the latch-up issue. In this work, three (two) diodes are added with SCR in series to increase its overall holding voltage to approximately 4V for such 3.3-V tolerant ESD clamp circuit A (B). The holding voltage a little higher than 3.3V is used to overcome overshooting supply voltage. The device structure of the ESD clamp device used in these work is shown in Fig. 4.2. The purpose of the additional N-well region under the N+ diffusion at the cathode of the SCR device with the substrate-triggered technique is to further enhance the turn-on speed of the SCR device for better turn-on efficiency, because that can increase the equivalent substrate resistance (R_{sub}) in this device structure.

To avoid the ESD damage on I/O buffer before ESD clamp device is turned on, the substrate-triggered technique is used to quickly trigger on the ESD clamp device. Because ESD bus line will be biased at 3.3V through the diode Dp when 3.3-V input signals reach to the I/O pad, the ESD detection circuit connected between ESD bus and VSS must sustain the high-voltage (3.3V) stress during normal circuit operating condition. Some ESD detection circuits proposed to increase the turn-on speed of SCR device will suffer gate-oxide

reliability issue under 3.3-V bias with only 1.2-V low-voltage devices. Therefore, how to design a turn-on-efficient ESD detection circuit with only 1.2-V devices to sustain 3.3-V bias becomes a quite significant challenge to this 1.2/3.3-V mixed-voltage I/O buffer.

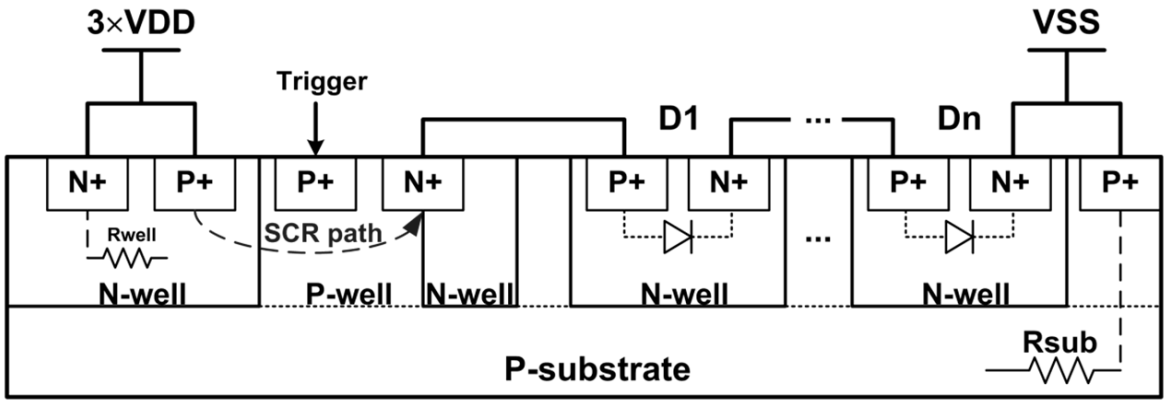


Fig. 4.2 Device structure of the ESD clamp device composed of substrate- triggered SCR device with diodes in series.

4.3 3×VDD-Tolerant ESD Clamp Circuit A

During normal circuit operating condition with 1.2-V VDD power supply and grounded VSS, when a 3×VDD (3.3-V) input signal is applied to the I/O pad, the voltage level at the internal ESD bus will be charged up to 3.3V through the diode Dp connected between I/O pad and ESD bus. For the convenience of easily describing the circuit operation of the 3×VDD-tolerant ESD clamp circuit with HSPICE simulations, the ESD bus is treated as an external 3.3V power supply in this section.

The ESD clamp circuit that can be operated under 3.3-V bias with only 1.2-V low-voltage devices is shown in Fig. 4.3. Under normal circuit operating condition, the diode-connected PMOS (Mp1~Mp3) are used as the voltage divider to bias the substrate driver (Mn1, Mp4, and Mp5) of the ESD detection circuit, where a deep N-well is used in Mn1 to avoid the gate-oxide overstress between gate and bulk. The NMOS (Mn2) is used to keep the voltage level of the trigger node at VSS, so the ESD clamp device is guaranteed to be kept off in the normal circuit operating condition. Here, the RC time constant of R1 and Mp7 should be designed around the order of ~1μs to distinguish the normal circuit operating condition from the ESD transition.

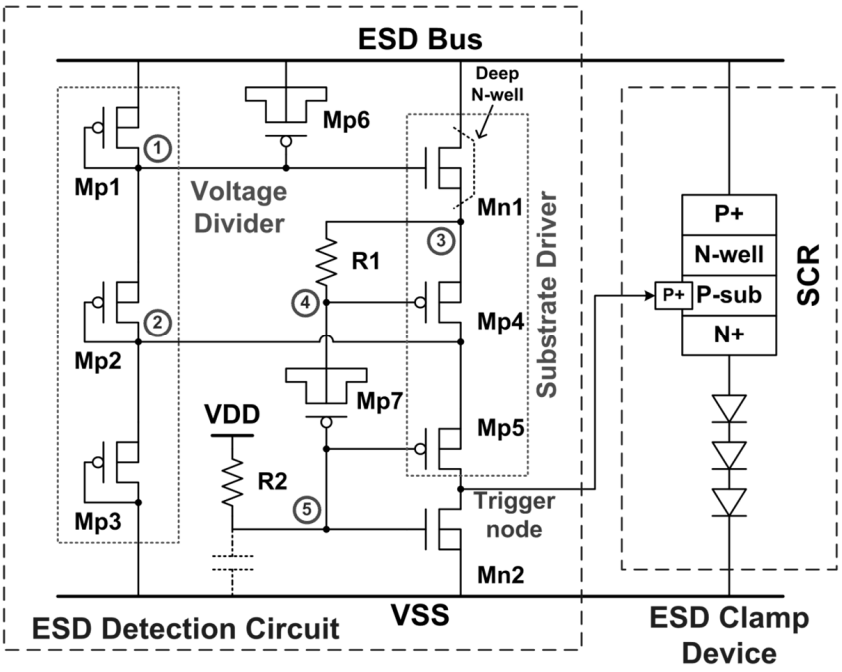


Fig. 4.3 Circuit implementation of the 3×VDD-tolerant ESD clamp circuit A realized with 1×VDD devices.

4.3.1 Operation under Normal Circuit Operating Condition

During normal circuit operating condition, the node 1 and node 2 in the ESD detection circuit will be biased at 2.2V and 1.1V, respectively. The node 5 is biased at 1.2V through the 1kΩ resistor of R2 to VDD, so that Mp5 is turned off. There is no trigger current generated from the ESD detection circuit into the ESD clamp device. In addition, the Mn2 in the turned-on state, whose gate is connected to VDD through the resistor of R2, can increase the noise margin of the ESD detection circuit to guarantee the ESD clamp device against false triggering during the normal circuit operating conditions. All devices in the proposed ESD detection circuit with 1.2-V gate oxide can be free from gate-oxide reliability issue under the ESD bus of 3.3V.

In this ESD detection circuit, the drain-to-gate voltage of Mn1 is (3.3V-2.2V), where Mn1 is working at inversion region under the normal circuit operating conditions. But, the induced channel region of Mn1 could be insufficient to shade the strength of the electric field across the gate and bulk if its bulk region is grounded. There is somewhat gate-oxide reliability concern on Mn1 if its bulk is grounded. Therefore, to avoid this possible issue, the bulk of Mn1 is connected to its own source node. To avoid the leakage current path through

the bulk (p-well) of Mn1 to the grounded p-substrate, the bulk (p-well) of Mn1 is isolated by the deep N-well with 3.3-V bias from the common p-substrate, as the diagram shown in Fig. 4.4. Fig. 4.4 also marks with the Spice-simulated voltages at the nodes of the ESD detection circuit during normal circuit operating condition. From these simulated voltages, the voltages between each two adjacent nodes of devices do not exceed their voltage limitation (1.32V for 1.2-V devices). Therefore, the ESD detection circuit is free from the gate-oxide reliability issue.

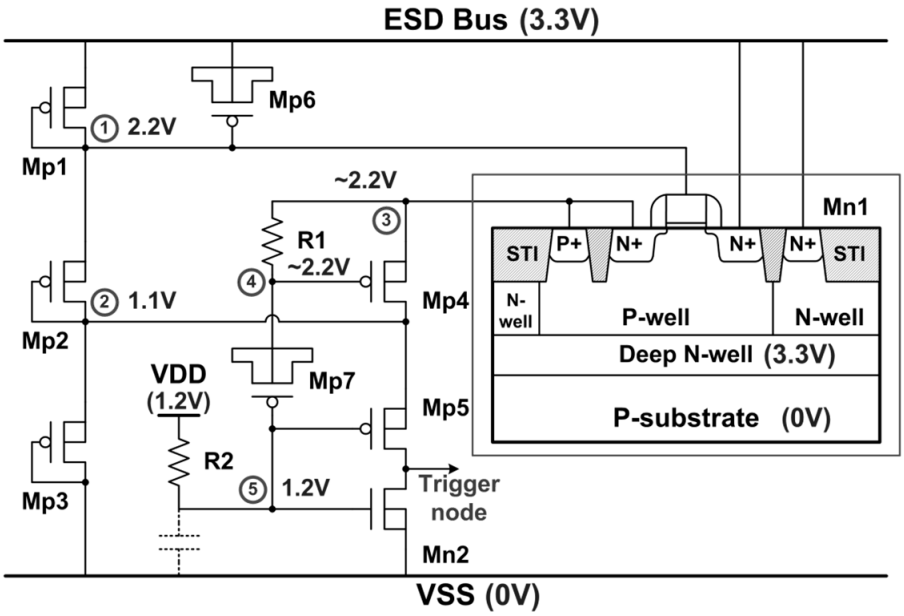


Fig. 4.4 Cross-sectional view of the NMOS Mn1 and the HSPICE-simulated voltages at the nodes of ESD detection circuit under the normal circuit operating condition.

4.3.2 Operation under ESD Transition

When ESD voltage is applied to the I/O pad with VSS relatively grounded, such ESD transient voltage will be conducted into ESD bus through the Dp diode in forward-biased condition. Therefore, the ESD bus will have a fast rising-up ESD voltage. The capacitor (Mp6) will couple some ESD transient voltage to the node 1 to turn on Mn1 and to pull up the node 3. The RC delay from R1 and Mp7 in the ESD detection circuit will keep the gate of Mp4 (node 4) at a relatively lower voltage level (compared to the node 3) for a long time. The VDD is initially floating with an initial voltage level of 0V during a PS-mode ESD stress at I/O pad. Some ESD transient voltage would be coupled to VDD through the parasitic

capacitance during ESD zapping, but the R2 and the parasitic capacitance at the gates of Mp5 and Mn2 will hold the gate of Mp5 at a low voltage level for a long time to keep Mp5 in on state. Therefore, Mp4 and Mp5**,** whose initial gate voltages are at low voltage level, can be quickly turned on by ESD energy to generate the substrate-triggered current into the substrate of SCR. Then, the ESD clamp device can be quickly triggered on to discharge ESD current from ESD bus to VSS.

Fig. 4.5 shows the HSPICE-simulated voltages and the substrate-triggered current of the ESD detection circuit under ESD transition. A 0-to-6V ESD-like voltage pulse with a rise time of 10ns is applied to the ESD bus to simulate the ESD transient voltage. The Spice-simulated results show that the gate voltage of Mn1 (node 1) is quickly pulled high through Mp6, whereas the gate voltage of Mp4 (node 4) is kept low due to the RC time delay from R1 and Mp7. Therefore, the ESD clamp device can be triggered on to discharge ESD current from ESD bus to VSS. The substrate driver can provide the substrate-triggered current larger than 35mA within 10ns when the 0-to-6V transient voltage is applied to ESD bus, as shown in Fig. 4.5. By selecting the suitable device dimensions of R1, Mp7, and the substrate driver (Mn1, Mp4, and Mp5), the peak current and the period of the substrate-triggered current can be adjusted to meet different applications or specifications.

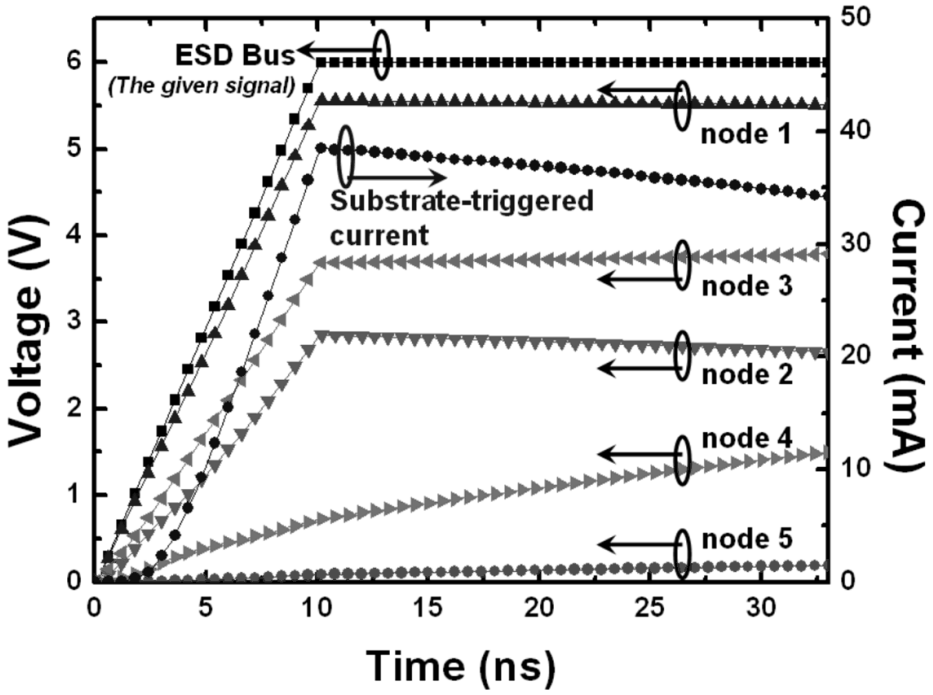


Fig. 4.5 HSPICE-simulated voltages on the nodes of ESD detection circuit and the substrate-triggered current through Mp5 under 0-to-6V ESD-like transition on ESD bus.

4.4 3×VDD-Tolerant ESD Clamp Circuit B

The other 3×VDD-tolerant power-rail ESD clamp circuit, which contains ESD clamp device and ESD detection circuit with additional control, is shown in Fig. 4.6, where the ESD clamp device is realized by a substrate-triggered SCR with two diodes in series. The new proposed 3×VDD-tolerant power-rail ESD clamp circuit is also realized with only 1.2-V low-voltage devices to operate at 3.3-V power supply (3×VDD) without the risk of gate-oxide reliability.

Under normal circuit operating condition, the diode-connected PMOS (Md1~Md6) are used as the voltage divider to bias the substrate driver (Mp1, Mp2, and Mp3) and the control circuit (M1~M6, Mp4 and Mp5) of the ESD detection circuit. Here, the RC time constant of R1 and Mc1 should be designed around the order of ~1μs to distinguish ESD stress event from the normal circuit operating conditions. Furthermore, the special control circuit can further enhance the substrate-triggered current generated by substrate driver in ESD detection circuit.

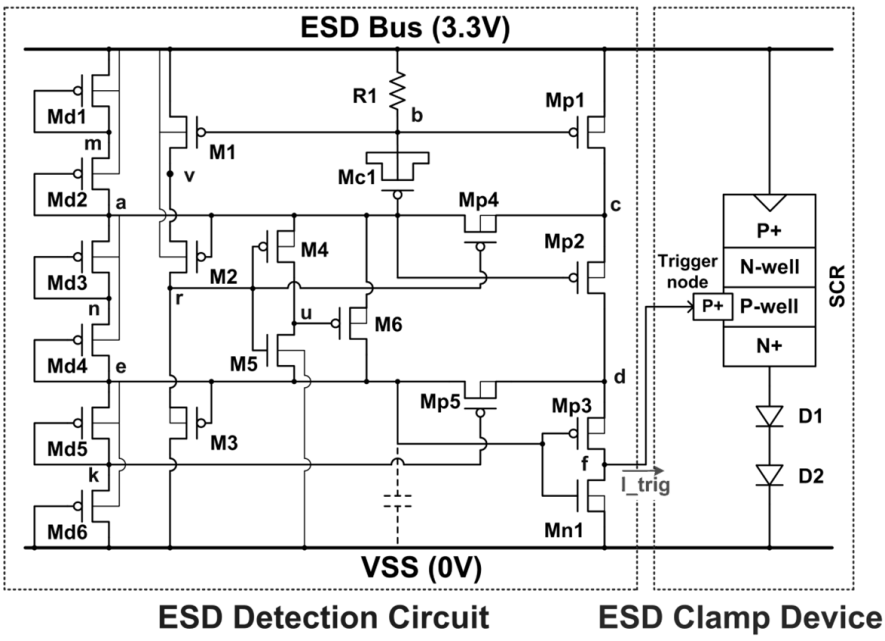


Fig. 4.6 Circuit implementation of the 3×VDD-tolerant ESD clamp circuit B realized with 1×VDD devices.

4.4.1 Operation under Normal Circuit Operating Condition

During the normal circuit operating condition, the node a and node e in the ESD detection circuit are biased at 2.2V and 1.1V, respectively. The gate voltage (node k) of Mp5 will be biased at 0.6V due to the body effect of Md6, so that Mp5 is turned on and the node d is

biased at 1.1V. The gate-to-source voltage of Mp3 is 0V, and therefore Mp3 is turned off. There is no trigger current generated from the ESD detection circuit into the ESD clamp device. In the ESD detection circuit, the gate voltage of Mp1 and M1 is biased at 3.3V through the resistor R1. Therefore, the Mp1 and M1 are kept in off state. Owing to the turned-off M1, there is no current path from ESD bus line through the PMOS M1, M2, and M3 to VSS, so that M2 is kept in off state. Therefore, the source-to-gate voltage of M2 is less than the threshold voltage of the 1.2-V PMOS transistor (|Vtp|), so the voltage level of node v is kept between 2.2V (node a) and (2.2V+|Vtp|). With the same reason, M3 is also kept in off state, and the gate voltage (node r) of M4 and Mp4 is kept between 1.1V and (1.1V+|Vtp|), so that M4 and Mp4 are both in on state, and therefore the voltage level of node c and node u are biased at 2.2V. The gate-to-source voltages of M5, M6, and Mp2 are nearly 0V, so these transistors are all in off state. In this situation, all 1.2-V devices are free from gate-oxide reliability issue under normal circuit operating condition with 3×VDD line of 3.3V.

Fig. 4.7 shows the HSPICE-simulated voltages on the nodes of the proposed ESD detection circuit. In this simulation, the ESD bus line is powered-on to 3.3V with a rise time of 1ms. In addition, with consideration to the voltage variation in ESD bus line, the HSPICE-simulated voltages on nodes of the ESD detection under normal circuit operating conditions with 10% variation in supply voltage of 3×VDD (3V to 3.6V) are shown in Fig. 4.8. From the simulation results in Figs. 4.7 and 4.8, the voltages across the gate-to-drain, gate-to-source, and gate-to-bulk terminals of every device in Fig. 4.6 do not exceed the process limitation (1.32V for 1.2-V devices in 0.13μm CMOS process), even if 10% voltage variation exists in ESD bus line. Therefore, the ESD detection circuit can be ensured against gate-oxide reliability issue.

4.4.2 Operation under ESD Transition

When ESD voltage is conducted to the ESD bus line with VSS relatively grounded, the RC delay of R1 and Mc1 in the ESD detection circuit keep the gates of Mp1 and M1 (node b) at a relatively low voltage level, compared with the ESD bus line for a long time. M1 and Mp1 can be turned on and therefore the voltage levels at node c and node v rise rapidly. The voltage levels at node a and node e are initially floating with a voltage level of ~0V, so that M2 and Mp2 can be turned on, and the voltage levels at node r and node d also rise as the voltage levels at node v and node c. Mp5, whose gate voltage (node k) is relatively lower

than its source voltage (node d), is in on state, and the voltage level at node e should rise with the voltage level at node d. However, the RC delay of the turn-on resistance of Mp5 and the parasitic capacitance of Mn1 keep the node e in a low voltage level to ensure that Mp3 is in the turned-on state during ESD stress event. Moreover, the gate voltage (node r) of M5 is higher than its source voltage (node e). So, M5 is turned on to keep the voltage level at node u in a low voltage level as that at node e. Therefore, the gate-to-drain voltage of M6 is nearly zero to keep the voltage level at node a around the voltage level at node e plus a threshold voltage of M6, when the voltage level at node a is one threshold voltage higher than the voltage level at node u. Furthermore, the gate voltage (node r) of Mp4 is as high as its source voltage (node c), so that Mp4 is in off state to ensure that the voltage level at node a can be kept in a low voltage level compared with node c. Therefore, the substrate driver of Mp1, Mp2, and Mp3, whose gates are at relatively low voltage levels, can be quickly turned on by ESD energy to generate the substrate-triggered current into the trigger node (node f) of the SCR.

Fig. 4.9 shows the HSPICE-simulated voltages of the ESD detection circuit under ESD stress event. A 0-to-6V ESD-like pulse with a rise time of 10ns is applied to the ESD bus line to simulate the ESD transient voltage. From the simulation results, such low voltage levels at node a, node b, and node e guarantee that Mp1, Mp2, and Mp3 can be turned on during ESD stress event. Therefore, the substrate-triggered current can be generated by the substrate driver into the trigger node of SCR to trigger on the ESD clamp device to discharge ESD current from the 3×VDD line to VSS.

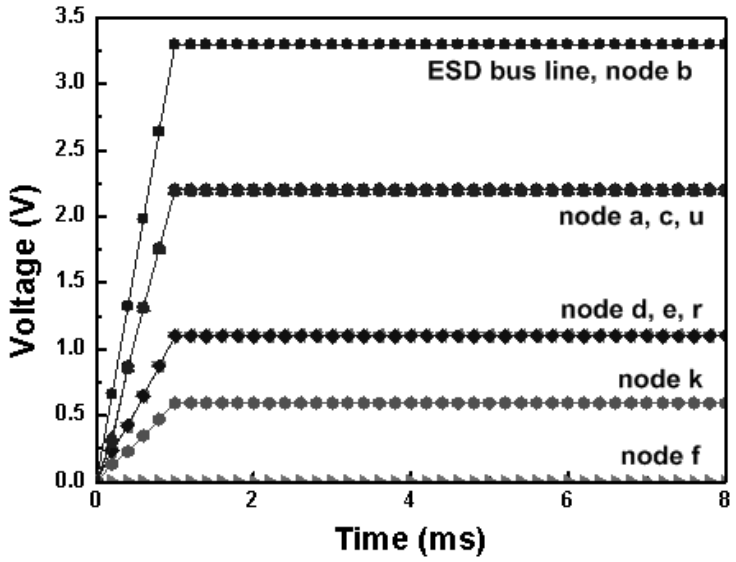


Fig. 4.7 HSPICE-simulated voltages on the nodes of the proposed ESD detection circuit under normal power-on transition with a rise time of 1ms.

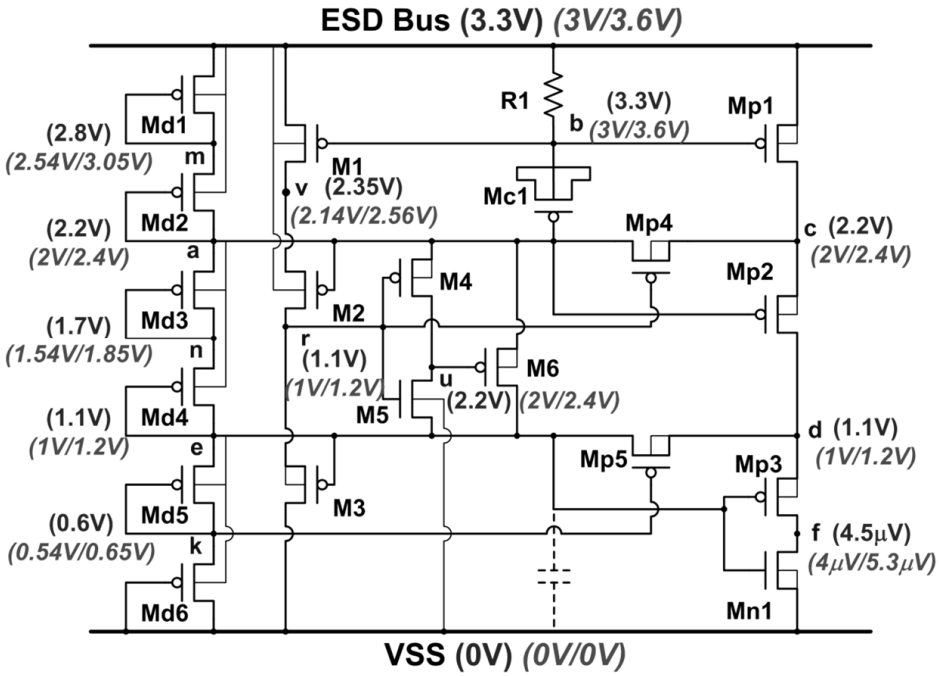


Fig. 4.8 HSPICE-simulated voltages on nodes of the ESD detection circuit under normal circuit operating conditions with 10% voltage variation in the ESD bus line.

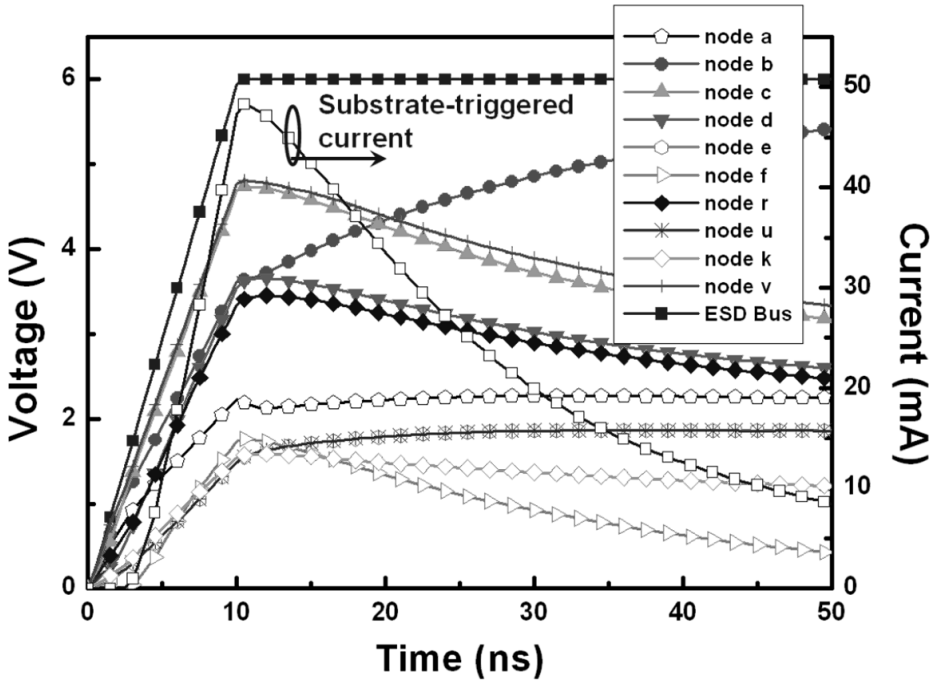


Fig. 4.9 HSPICE-simulated voltages on the nodes of ESD detection circuit under 0-to-6V ESD-like transition on ESD bus line (the line for node e overlaps with the line for node u).

4.5 Discussion on 3×VDD-Tolerant ESD Clamp Circuits

The 3×VDD-tolerant ESD clamp circuit A seems to be easily implemented, however it needs extra mask and process steps for deep N-well formation with the additional bias connection of 1×VDD supply. If 1×VDD supply does not power on simultaneously with 3×VDD supply by several micro-seconds or even mini-seconds, the ESD detection circuit may malfunction to generate large leakage current or be damaged due to gate-oxide overstress during power-on transition. Although the 3×VDD-tolerant ESD clamp circuit B is more complicated as compared with circuit A, it needs only conventional twin-well CMOS process to implement. Besides, it needs only 3×VDD supply to eliminate the malfunction and gate-oxide reliability issue due to non-simultaneous power-on transition. Furthermore, the ESD detection circuit with additional control in the 3×VDD-tolerant ESD clamp circuit B can further enhance the detection function to ESD events rather than only using the function of RC delay.

The substrate driver in the ESD detection circuit is guaranteed to be kept in off state under the normal circuit operating condition. In this situation, the P/V/T variation could only affect the leakage current of the ESD detection circuit rather than the circuit operation. During the ESD event, any process variation might affect the triggered current generated by the substrate driver. The amount of triggered current that can trigger the SCR device on is around several mA, which will be shown in the next section with measured data from silicon chip. By adjusting the device dimension in the substrate driver, the triggered current can be over designed greater than the minimum required current. Therefore, the circuit operation of ESD detection circuit can still function well under reasonable P/V/T variation in CMOS processes.

4.6 Experimental Results

The proposed ESD protection circuits have been fabricated in two different 0.13-μm silicided CMOS process with only 1.2-V devices. In these proposed ESD protection circuits, the ESD detection circuits and ESD clamp devices are fully-silicided. In 3×VDD-tolerant ESD clamp circuit A, the widths of SCR in ESD clamp device are varied in 45μm and 90μm. On the other hand, the widths of SCR in ESD clamp device are varied in 30μm, 45μm, and 60μm in 3×VDD-tolerant ESD clamp device B.

4.6.1 DC I-V Characteristics of ESD Clamp Device

The dc I-V characteristics of the ESD clamp device (SCR with two diodes in series) in 3×VDD-tolerant ESD clamp circuit B is measured by using Tek370 curve tracer.

To avoid the issue of false triggering and latchup, the holding voltage of the SCR-based ESD clamp device with diodes in stacked configuration must be designed to be greater than the maximum voltage level of 3×VDD (3.3V in 0.13-μm CMOS process) under the normal circuit operating condition. The measured dc I-V characteristics of the ESD clamp device under different temperatures are shown in Fig. 4.10. The inset in Fig. 4.10 is the enlarged view around the holding points of one SCR with 2 stacked diodes in series (SCR+2D). The holding voltages of the ESD clamp device are 3.98V, 3.82V, and 3.64V under the temperatures of 25°C, 75°C, and 125°C, respectively. These holding voltages are higher than the voltage level of 3×VDD (3.3V) under the normal circuit operating conditions. Even if the ESD clamp device was mis-triggered due to noise disturbance, it can be recovered to the normal condition after the noise source is removed. Therefore, the SCR-based ESD clamp device with a suitable number of stacked diodes in series can be safely applied in 3×VDD-tolerant ESD clamp circuit without any latchup issue.

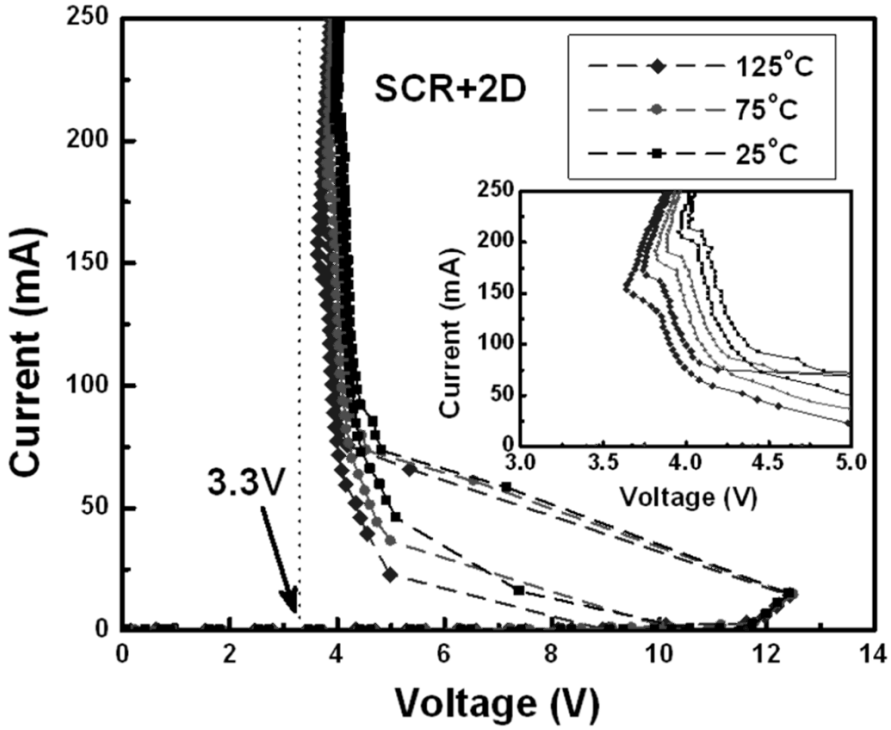


Fig. 4.10 The measured dc I-V characteristics of the ESD clamp device (SCR with 2 diodes in series) under different temperatures.

The measured dc I-V characteristics of the ESD clamp device under different substrate-triggered currents (I_trig) into the p+ trigger node are shown in Fig. 4.11. The measurement setup is also illustrated as the inset in Fig. 4.11. When the SCR-based ESD clamp device has no substrate-triggered current (I_trig=0mA), the SCR is essentially triggered on by junction avalanche breakdown. As shown in Fig. 4.11, the trigger voltage of the fabricated SCR-based ESD clamp device without the substrate-triggered current is as high as ~12.4V, which is higher than the breakdown voltage of the stacked NMOS with R_{ESD} in mixed-voltage I/O buffers. But the trigger voltage of the ESD clamp device is reduced to 8V when the substrate-trigger current is 8mA. Moreover, the trigger voltage of the ESD clamp device is reduced to only 4.2V, which almost equals to the holding voltage of the ESD clamp device, when the substrate-triggered current is increased to 10mA. The trigger voltage of the ESD clamp device is decreased while the substrate-triggered current is increased. ESD clamp device with low trigger voltage can be turned on more quickly to discharge ESD current to provide more effective protection for mixed-voltage I/O interfaces.

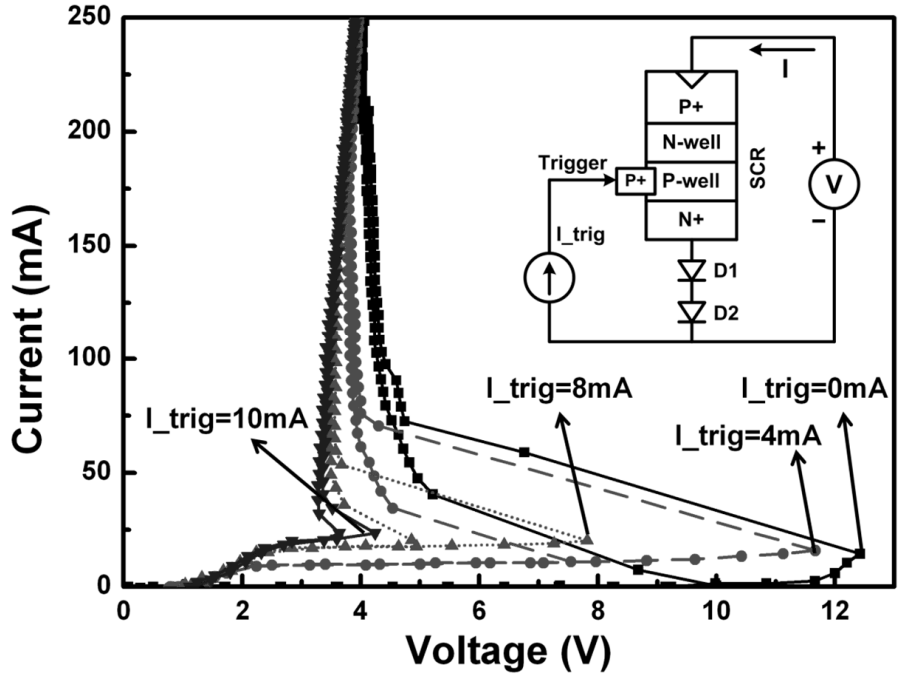


Fig. 4.11 The measured dc I-V characteristics of the ESD clamp device (SCR with 2 diodes in series) under different substrate-triggered currents (I_trig).

4.6.2 Turn-on Verification

The turn-on behavior of SCR devices is one of important factors for ESD protection, and it has been evaluated in some recent works. To verify the turn-on efficiency of the proposed 3×VDD-tolerant ESD clamp circuits, an experimental setup is shown as the inset in Fig. 4.12,

where a voltage pulse generated from a pulse generator is used to simulate the rising edge of a PS-mode HBM ESD pulse. The voltage pulse generated from the pulse generator initially has a square-type voltage waveform with a rise time about ~10ns and a pulse height of 6V, as shown in Fig. 4.12. When the positive voltage pulse is applied to the I/O pad of the proposed ESD protection circuit with VSS grounded, the sharp-rising edge of the ESD-like voltage pulse will start the ESD detection to generate substrate-triggered current to trigger ESD clamp device on, and provide a low-impedance path between the I/O pad and VSS. The voltage waveform on the I/O pad is therefore clamped by the turned-on ESD clamp device. The voltage waveforms, clamped by 3×VDD-tolerant ESD clamp circuit A and B, on the I/O pad are also shown in Fig. 4.12. The voltage waveforms on the I/O pad are clamped by the Dp and ESD clamp device to ~4V, which is lower than the breakdown voltage of the stacked NMOS in the mixed-voltage I/O buffer. The time to clamp the 0-to-6V voltage pulse to the holding voltage level (~4V) by the ESD clamp device is about ~20ns. From the measured voltage waveforms, the excellent turn-on efficiency in ESD-stress condition has been successfully verified in the proposed ESD protection circuits.

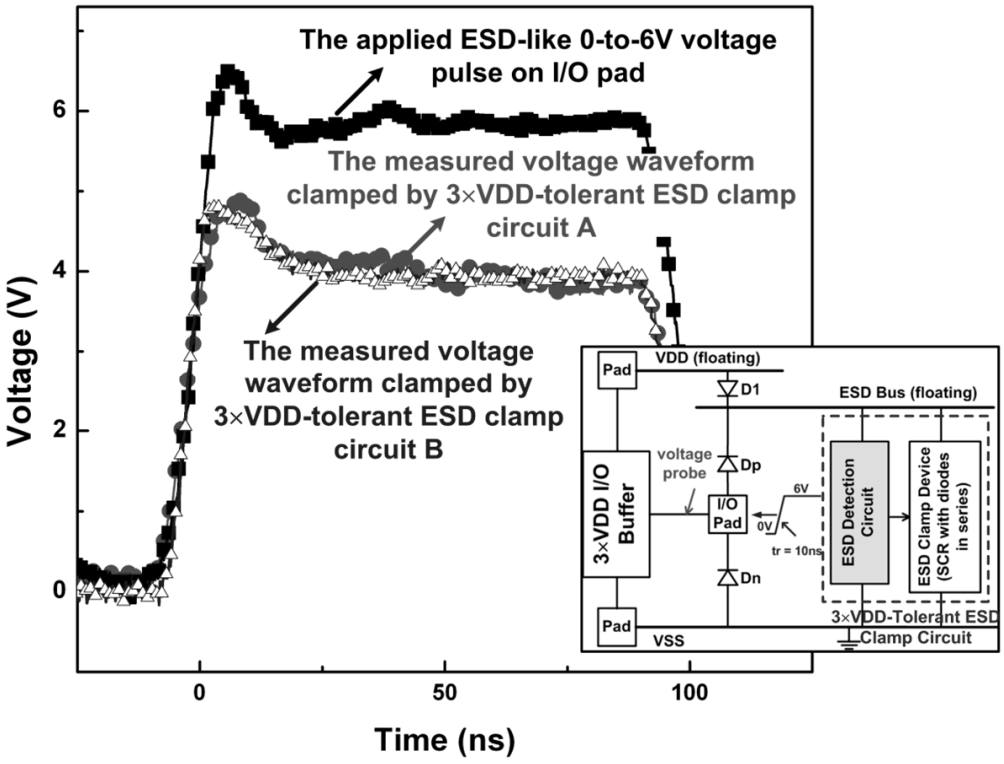


Fig. 4.12 The measured voltage waveforms, clamped by 3×VDD-tolerant ESD clamp circuit A and B, on the I/O pad when a 0-to-6V voltage pulse is applying to I/O pad under the PS-mode ESD stress (VDD floating and VSS grounded).

4.6.3 TLP Characteristics and ESD Robustness of ESD Protection Design With 3×VDD-Tolerant ESD Clamp Circuit A

The TLP-measured second breakdown current and HBM ESD level of the I/O buffer with and without the proposed ESD protection design with 3×VDD-tolerant ESD clamp circuit A under PS-mode ESD stress are compared in Table 4.1. When the width of SCR device in ESD clamp device is 45μm, the secondary breakdown current of the I/O buffer with the proposed ESD protection design and 3×VDD-tolerant ESD clamp circuit A can be increased from 0.2A to 4A, as comparing with the I/O buffer without ESD protection. In addition, the HBM ESD level of the I/O buffer with the proposed ESD protection design can be improved from 500V to 6kV. When the width of SCR device in ESD clamp device is increased to 90μm, the second breakdown current and HBM ESD level of the I/O buffer with the proposed ESD protection scheme can be further increased larger than 6A and 8kV, respectively. The proposed ESD protection design can significantly improve the second breakdown current and HBM ESD level of the 3×VDD-tolerant I/O buffer.

Table 4.1
ESD robustness of I/O buffer with or without ESD protection circuit with ESD clamp circuit A

3×VDD-Tolerant I/O Buffer	It2	HBM ESD Level
I/O Buffer without ESD Protection Circuit	0.2A	<500V
I/O Buffer with ESD Protection Circuit A (SCR Width = 45μm)	4A	6kV
I/O Buffer with ESD Protection Circuit A (SCR Width = 90μm)	>6A	>8kV

4.6.4 TLP Characteristics and ESD Robustness of ESD Protection Design With 3×VDD-Tolerant ESD Clamp Circuit B

The TLP-measured I-V characteristics of the ESD clamp device with or without ESD detection circuit of 3×VDD-tolerant ESD clamp circuit B under PS-mode ESD stress are

shown in Fig. 4.13, where the width of the SCR in ESD clamp device is 60μm. From the measured results, the trigger voltage of ESD clamp device without ESD detection circuit is 12.7V, whereas the trigger voltage of ESD clamp device can be reduced to only 4.6V by ESD detection circuit without involving the junction avalanche breakdown. Therefore, the trigger voltage of ESD clamp device can be significantly reduced by the proposed ESD detection circuit to ensure effective ESD protection.

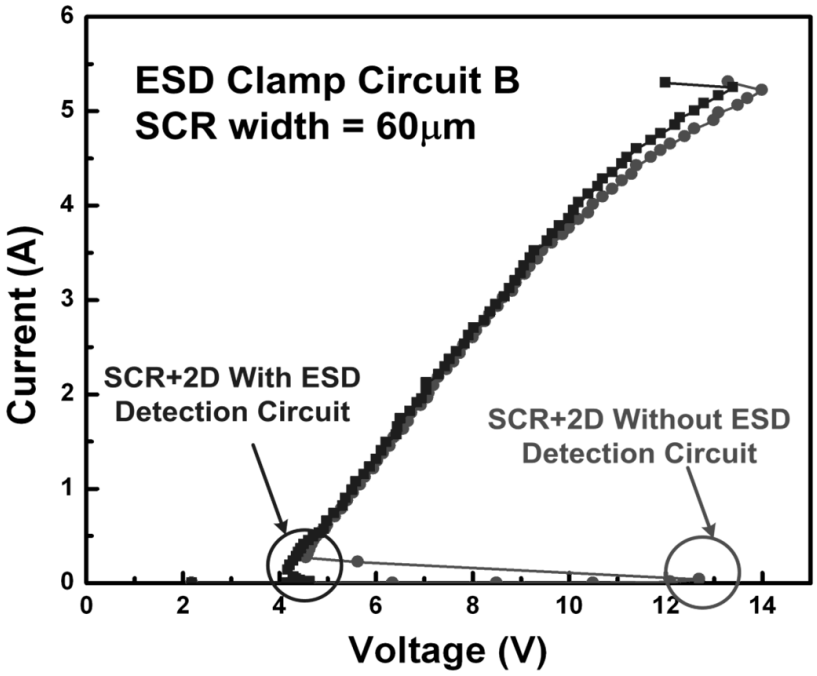


Fig. 4.13 The measured TLP I-V characteristics of the ESD clamp device in the 3×VDD-tolerant ESD clamp circuit B with or without ESD detection circuit under PS-mode ESD stress.

The second breakdown current and the turn-on resistance of the ESD protection circuit with a 60μm-wide SCR and two diodes in series is 5.31A and ~1.9Ω, respectively. The standby leakage current under 3.3-V bias of the whole ESD protection circuit is only 83nA. By adjusting the width of the ESD clamp device and the size of the substrate driver in ESD detection circuit, the second breakdown current, turn-on resistance, and the trigger voltage of the ESD protection circuit can be modified to satisfy the specification of different mixed-voltage I/O circuits. The HBM ESD levels and MM ESD levels of the proposed ESD protection circuit with 3×VDD-tolerant ESD clamp circuit B with various widths of SCR-based ESD clamp devices under PS-mode ESD stress are listed in Table 4.2. The HBM ESD levels of ESD protection circuit under ESD clamp device width of 30μm, 45μm, and 60μm are 4kV, 6.2kV, and larger than 8kV, respectively. Besides, the MM ESD levels of

ESD protection circuit under ESD clamp device width of 30μm, 45μm, and 60μm are 260V, 380V, and 440V, respectively. The corresponding second breakdown current measured by TLP is also listed in Table 4.2.

The CDM ESD robustness of the proposed ESD protection circuits are also verified by KeyTek RCDM tester. The 3×VDD-tolerant I/O buffer protected by the proposed ESD protection circuits in this work (both 3×VDD-tolerant ESD clamp circuits A and B) can achieve a CDM ESD level of greater than ±1kV.

Table 4.2

ESD robustness of the proposed ESD protection circuit with ESD clamp circuit B with various widths of ESD clamp devices

ESD clamp device width (μm)	HBM ESD Level	MM ESD Level	It2
30	4kV	260V	2.56A
45	6.2kV	380V	3.82A
60	>8kV	440V	5.31A

4.7 Pin-to-Pin ESD Protection

In the whole chip ESD protection design, the proposed 3×VDD-tolerant ESD protection circuit can be shared with other 3×VDD-tolerant I/O buffers by connecting ESD bus to each other to achieve pin-to-pin ESD protection, as shown in Fig. 4.14. During the pin-to-pin ESD test, the ESD stress is applied to one I/O pad with other I/O pad grounded, where the VDD and VSS are initially floating. The ESD current will flow from one I/O pad through the forward diode Dp, ESD bus line, and then through the proposed 3×VDD-tolerant ESD clamp circuit to the VSS line, finally from the VSS line through the forward diode Dn to the other grounded I/O pad. Therefore, the pin-to-pin ESD protection can be achieved by using this ESD protection scheme with the proposed 3×VDD-tolerant ESD clamp circuit for 3×VDD-tolerant mixed-voltage I/O buffers.

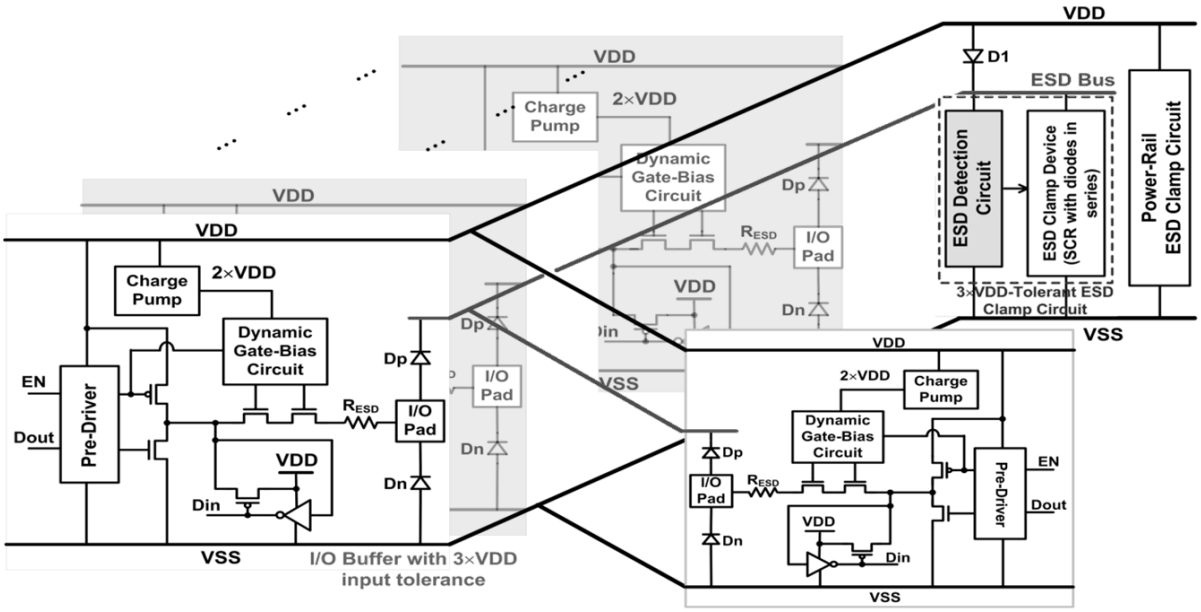


Fig. 4.14 The shared ESD bus and 3×VDD-tolerant ESD clamp circuit for whole set of I/O buffers to achieve pin-to-pin ESD protection.

4.8 Summary

Two novel circuit solutions on ESD protection design, realized with 1×VDD devices for mixed-voltage I/O buffer with 3×VDD input tolerance, have been successfully verified in two different 0.13-μm 1.2-V CMOS process. The four-mode (PS, NS, PD, and ND) ESD stresses and pin-to-pin ESD stresses on the 1.2/3.3-V mixed-voltage I/O buffer can be effectively discharged by the ESD protection scheme, with the proposed 3×VDD-tolerant power-rail ESD clamp circuits. The proposed 3×VDD-tolerant power-rail ESD clamp circuits operates without gate-oxide reliability issue under the normal circuit operating conditions. By using the special control circuit in the 3×VDD-tolerant ESD clamp circuit B, the device sizes of the resistor, capacitor, and the substrate driver can be reduced. Therefore, the active area and the standby leakage current of the ESD detection circuit in 3×VDD-tolerant ESD clamp circuit B can be further reduced. In addition, the ESD detection circuit has also shown significant help on reducing the trigger voltage of ESD clamp device. The turn-on behaviors of the ESD clamp device have been measured to verify the effectiveness of the ESD detection circuit for both two 3×VDD-tolerant ESD clamp circuits. The experimental results have also confirmed that the ESD robustness of the 3×VDD mixed-voltage I/O buffer can be significantly

increased up to 8kV with the proposed ESD protection designs. These two proposed power-rail ESD clamp circuit with the advantages of low leakage current, high ESD robustness, and no gate-oxide reliability issue are the excellent ESD protection solutions to the mixed-voltage I/O interfaces with high-voltage input/output signals.

Chapter 5

ESD Protection Design for 5-V/40-V High-Voltage BCD Technology

In this chapter, the ESD protection design for smart power applications with lateral double-diffused MOS (LDMOS) transistor is investigated. With the gate-driven and substrate-triggered circuit techniques, the n-channel LDMOS can be quickly turned on to protect the output drivers during ESD stress event. From the experimental results, the high-voltage lateral DMOS with the proposed ESD detection circuit has better TLP-measured It2, ESD robustness, and turn-on efficiency than the stand-alone lateral DMOS. The proposed gate-driven and substrate-triggered ESD protection circuits have been successfully verified in a 0.35-μm 5V/40V bipolar CMOS DMOS (BCD) process.

5.1 Background

DMOS power transistors have been commonly used as output driver in the smart power technologies [85], [86], including the automotive ICs. Such high-voltage transistor is often self protecting against ESD stress. The DMOS devices were employed for ESD protection of high-voltage pins by channel current under gate biasing condition [87], [88]. However, the high-voltage device with a large amount of finger numbers did not have high ESD robustness after entering the snapback breakdown region. Such device exhibits random and unconstrained failures during the snapback breakdown before reaching its intrinsic limitation [89]. The medium sized drivers are usually not robust enough to pass the typical industrial ESD specifications. This is attributed to the current crowding effect among the multiple fingers and then inducing inhomogeneous triggering of the parasitic BJT to cause the non-uniform turn-on issue [90], [91]. Therefore, additional ESD protection design is needed to protect such output drivers in the high-voltage technologies [92]. In some power applications, the ESD ballast resistor of several hundred Ohms is forbidden to be placed between the output pad and the output driver which was often designed with a specification

of small turn-on resistance in applications. In such a case, the additional ESD protection circuit is placed in parallel with the output driver from the pad to ground. For example, the circuit diagram of ESD protection scheme for LED driver and DC-DC converter are shown in Figs. 5.1(a) and 5.1(b). If the additional ESD protection circuit was not turned on quickly enough, the output driver would be damaged during ESD stress event. To improve the turn-on speed of MOS transistors for ESD protection, RC-based ESD protection design (with a MOS capacitor) has been widely used in advanced CMOS processes. However, no MOS capacitor is available to sustain high-voltage operation due to the thin gate-oxide structure of the lateral DMOS transistor (e.g. Vd = 40V and Vg = 5V) in such a high-voltage technology studied in this work. If the MOS capacitor is implemented by such thin gate oxide and biased at high voltage level, the overstress voltage will damage the thin gate oxide.

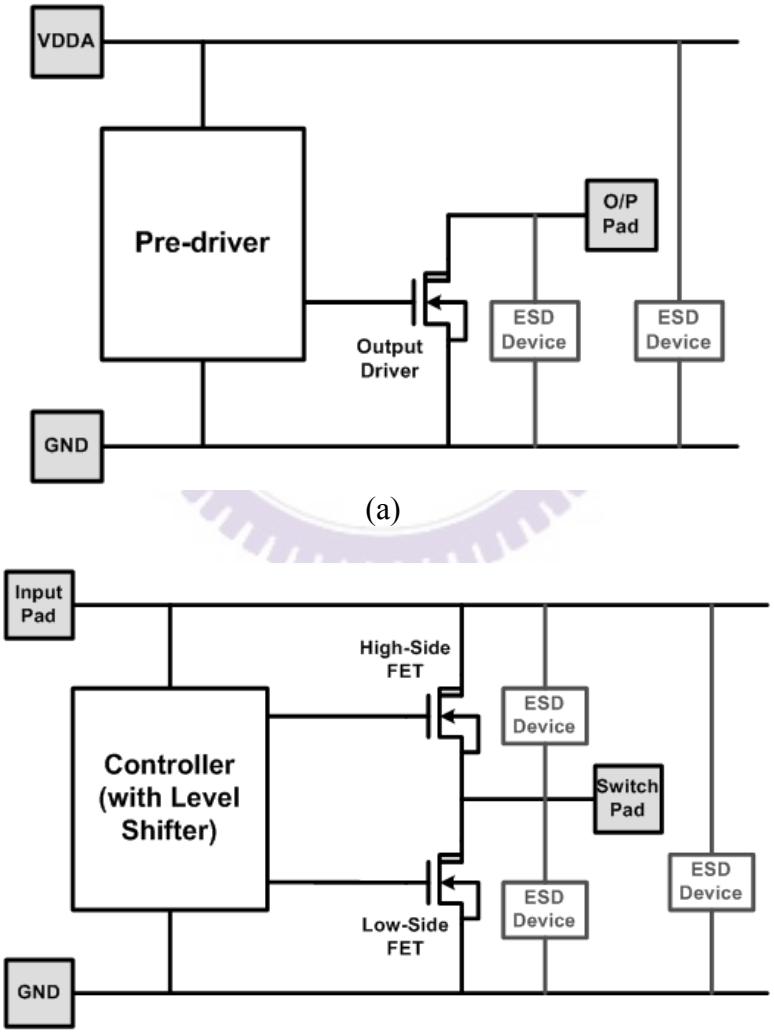
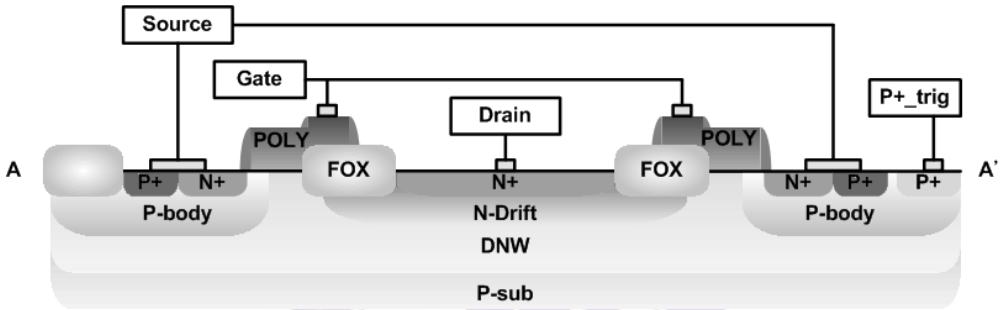


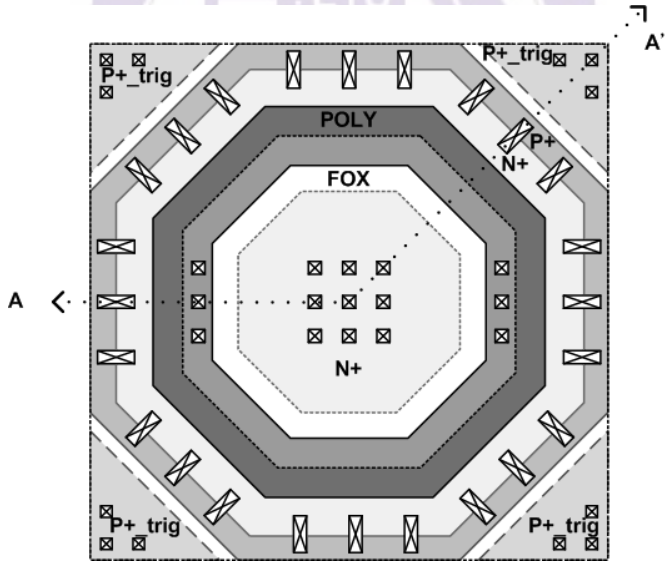
Fig. 5.1. ESD protection design for applications of (a) output pad of LED driver and (b) DC-DC converter. The resistor R_{ESD} in advanced CMOS process is not allowed in such applications.

5.2 Characteristics of LDNMOS with Gate-Biased and Substrate-Triggered Effect

The device cross-sectional view and the layout top view of the n-channel LDMOS (LDNMOS) with a field oxide (FOX) located at the drain region in a 0.35-μm 5V/40V BCD process are shown in Figs. 5.2(a) and 5.2(b), respectively. The gate-oxide thickness of such device is only 14nm, limiting the maximum applicable gate voltage to 5V. The N-Drift and the P-Body layers in Fig. 5.2(a) are lightly doped regions. The device is completely surrounded by the deep n-well (DNW) structure.



(a)



(b)

Fig. 5.2. (a) The device cross-sectional view, and (b) the layout top view, of the octagonal unit cell of the n-channel LDMOS with 5-V gate oxide and 40-V drain-to-source operating voltage in a 0.35-μm 5V/40V BCD process.

The LDNMOS used as the ESD clamp device in the ESD protection circuit is drawn in multiple octagonal cells, as shown in Fig. 5.2(b). The side length of the octagon is 10μm (the channel length of each side), and therefore the perimeter of each cell is 80μm. The P+_trig

regions at the four corners are drawn as the trigger nodes for implementation of the substrate-triggered technique. In the traditional multiple-fingers structure, the P-Body regions of all fingers are fully separated by FOX, and the individual P-Body regions could worsen the non-uniform turn-on behavior of the LDNMOS device.

Fig. 5.3 shows the ESD failure location of the gate-grounded LDNMOS device drawn by traditional multiple-fingers structure after 3kV HBM ESD stress. Only a few contacts were damaged at the drain diffusion during the ESD stress event. Therefore, the non-uniform turn-on phenomenon among the multiple fingers of the LDNMOS device is easily observed, and the ESD robustness is hard to be improved by only increasing the device dimension. On the other hand, the P-Body regions at the source side are connected to each other if the LDNMOS is constructed by multiple octagonal cells with the P+_trig regions located around the LDNMOS. The LDNMOS can be assembled by multiple cells of row number and column number to reach a larger total device width for higher current conducting capability. In this work, the LDNMOS is built up by 2 × 2 octagonal cells, and the equivalent total device width is 320μm, as shown in Fig. 5.4. Moreover, such octagonal structure can be applied for gate-biased technique or substrate-triggered technique (which is widely used in CMOS process) by connecting the gate node or the P+_trig node to the bias/trigger circuits. The active layout area of such LDNMOS is 63μm × 63μm.To clarify the effectiveness of the gate-biased and substrate-triggered techniques on a HV LDNMOS device, the TCAD simulation study is performed in the following.

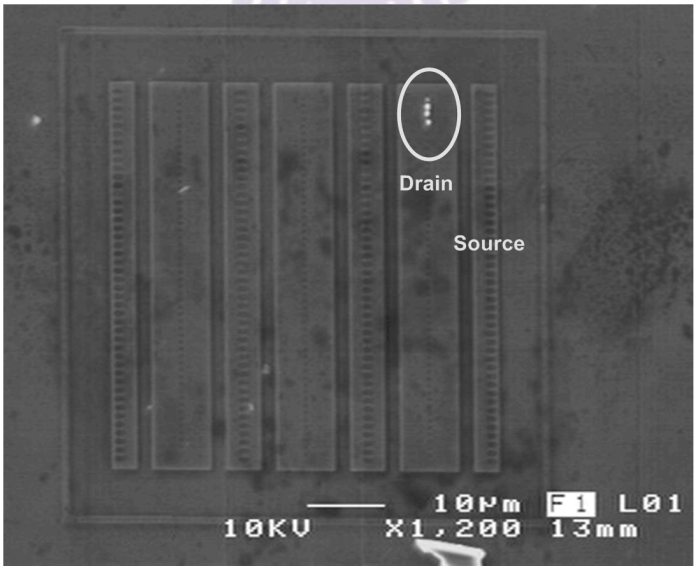


Fig. 5.3. After 3kV HBM ESD stress, the failure spot were found at only a few contacts at the drain side of the LDNMOS drawn with multiple finger structure.

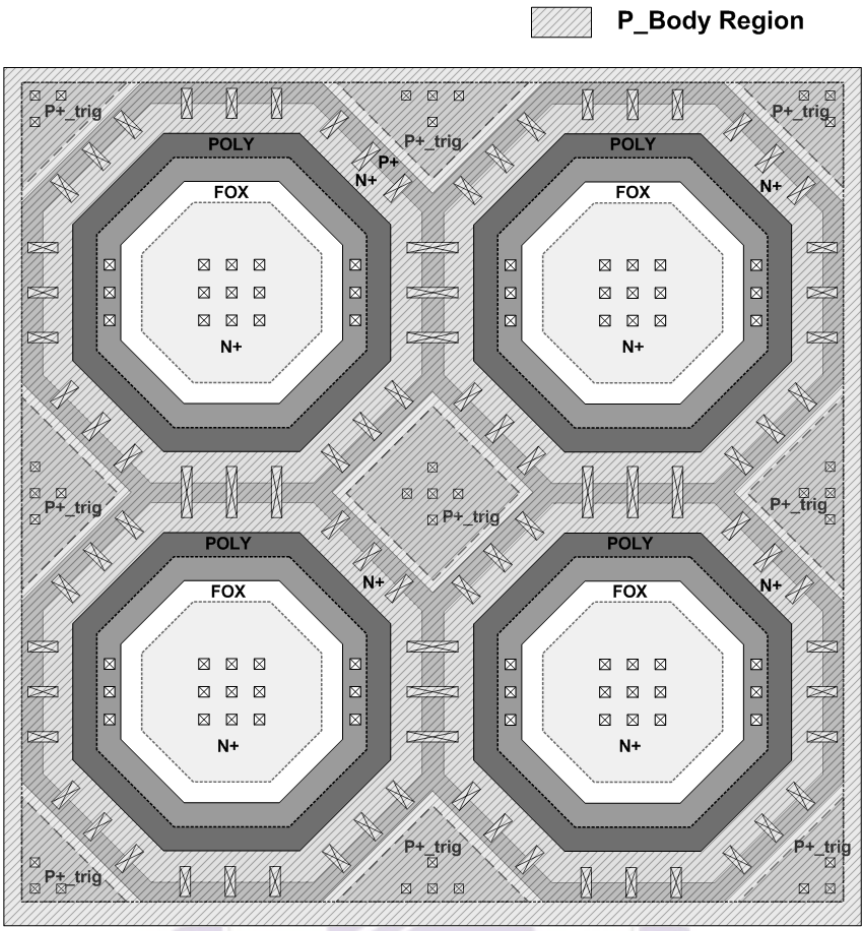


Fig. 5.4. The layout top view of a LDNMOS which is constructed by 2 × 2 octagonal cells. In this structure, the P_Body regions of all the cells are connected to each other.

5.2.1. LDNMOS with Gate-Biased Technique

The TCAD simulated I-V curves of the LDNMOS with different gate-biased conditions are shown in Fig. 5.5. Without the bias voltage on the gate terminal (Vg=0V), the trigger voltage of the LDNMOS is around 58V. When the bias voltage is increased, the channel current is generated to improve the turn-on speed of the parasitic NPN BJT (DNW/P_Body/N+), and then the trigger voltage of the LDNMOS can be reduced. The trigger voltage can be reduced to 47V when a 5V bias is applied at the gate of the LDNMOS. To compare the difference between the LDNMOS device with and without gate bias, the I-V curves of the LDNMOS with Vg of 0V and Vg of 5V are re-plotted in full scale and shown in Fig. 5.6(a). Points a, b, c, and d are marked on the curves to compare the corresponding electric field distribution under VDS of 10V and 47V (the trigger voltage of LDNMOS with Vg of 5V). The electric field distribution of the LDNMOS with Vg of 0V at the points a and b

of the I-V curve are shown in Fig. 5.6 (b). Without gate bias voltage, the electric field distribution localizes at the FOX edge, and no turn-on phenomenon appears even if the VDS is increased to 47V. On the other hand, the electric field distribution of the LDNMOS with Vg of 5V at the points c and d of the I-V curve are shown in Fig. 5.6 (c). With gate bias of 5V, the channel current along the surface can release the amplitude of the electric field and accelerate the turned-on speed of the parasitic NPN BJT in LDNMOS. When the VDS is increased to 47V, the LDNMOS is going to enter the snapback region, and the localization of electric field distribution is shifting from the FOX edge to the N_Drift region at the drain side. From the simulation, the gate-biased technique can improve the turn-on behavior of the LDNMOS device.

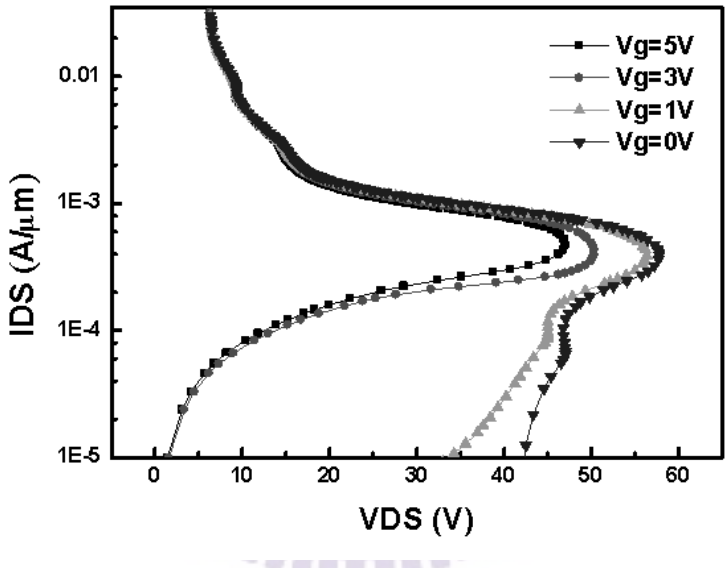
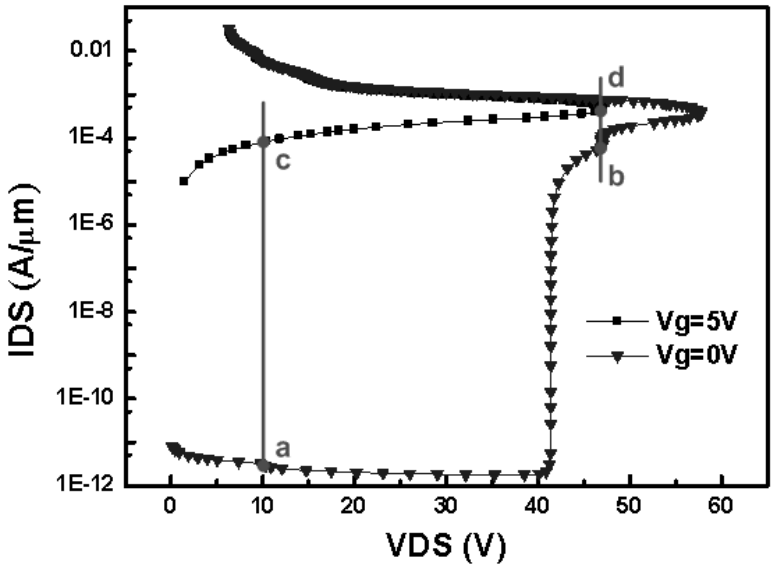
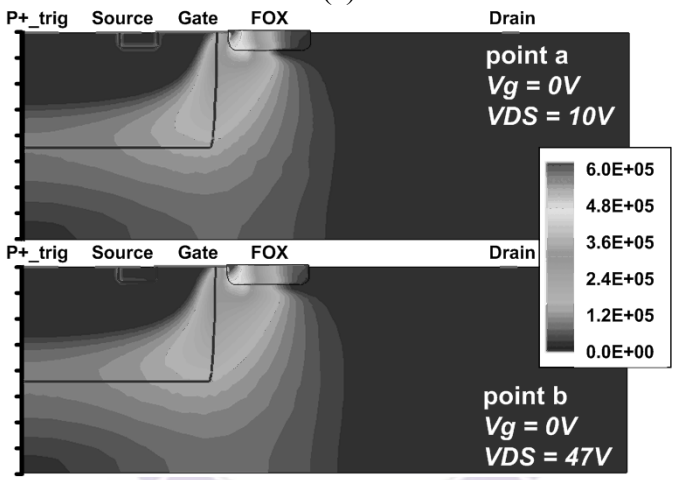


Fig. 5.5. The TCAD simulated I-V curves (IDS-VDS) of the LDNMOS device with different gate biases.



(a)



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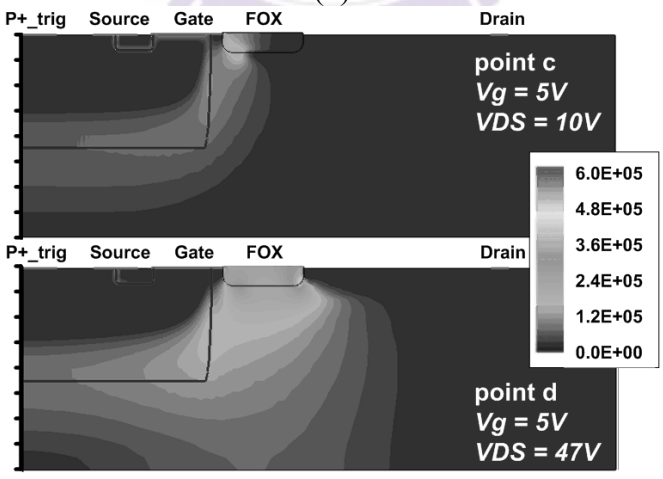
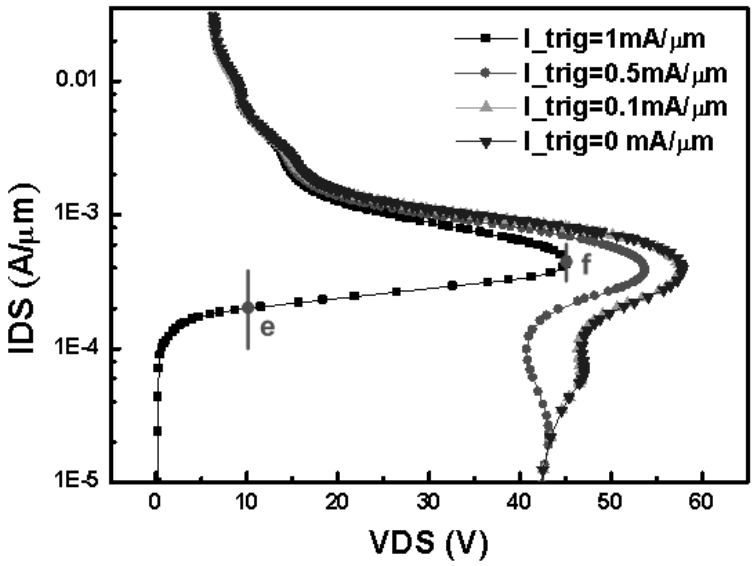


(c)

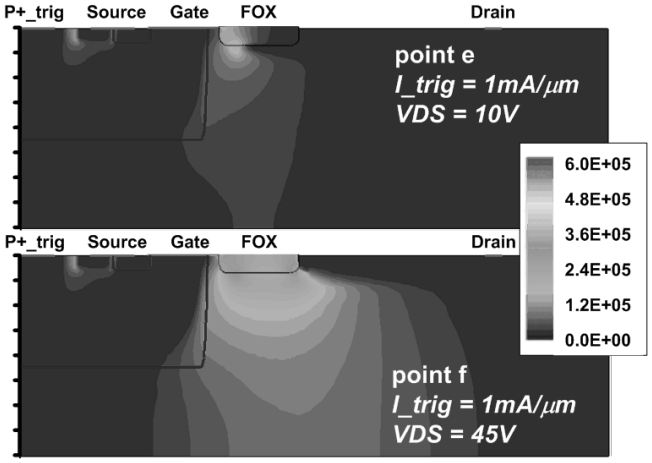
Fig. 5.6 (a) The TCAD simulated I-V curves of the LDNMOS device, and the corresponding electric field distribution of the LDNMOS device with (b) Vg of 0V and (c) Vg of 5V under VDS of 10V and VDS of 47V.

5.2.2. LDNMOS with Substrate-Triggered Technique

The TCAD simulated I-V curves of the LDNMOS with different substrate-triggered currents (I_trig) are shown in Fig. 5.7(a). The substrate-triggered current flowing from P_trig to N+ region at the source side will provide the base current of the parasitic NPN BJT to trigger it on. When the substrate-triggered current is higher than 0.5mA/μm, the trigger voltage of the LDNMOS will be reduced. With I_trig of 1mA/μm, the trigger voltage is reduced to 45V. The electric field distribution of the LDNMOS with I_trig of 1mA/μm at the point e (under VDS of 10V), and the point f (under VDS of 45V) of the I-V curve are shown in Fig. 5.7 (b).



(a)



(b)

Fig. 5.7. (a) The TCAD simulated I-V curves of the LDNMOS device with different substrate-triggered currents (I_trig), and (b) the electric field distribution at VDS of 10V and VDS of 45V under I_trig of 1mA/μm.

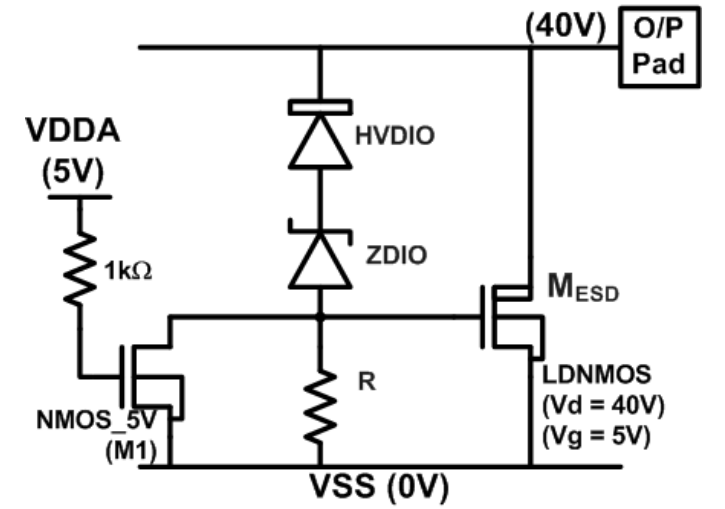
In the simulation, the substrate-triggered current flowing from the P_trig to N+ region is obvious, and it generates a voltage difference between the base and emitter of the parasitic NPN BJT to trigger on the LDNMOS. Therefore, the substrate-triggered technique is also a useful method for accelerating the turn-on speed of the LDNMOS device for ESD protection.

5.3 Implementation of ESD Protection Circuit with LDNMOS

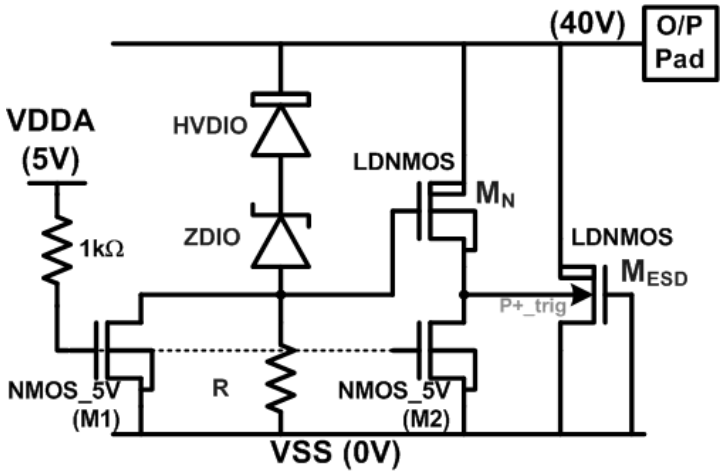
The proposed ESD protection designs with gate-driven ESD detection circuit (gate-biased technique) and substrate-triggered ESD detection circuit are shown in Figs. 5.8(a) and 5.8(b), respectively, which are named as the gate-driven ESD protection circuit and the substrate-triggered ESD protection circuit in this work. The ESD clamp device (M_{ESD}) is implemented by LDNMOS with 2 × 2 octagonal cells, as discussed in Section II. In Fig. 5.8(a), the gate-driven ESD detection circuit is composed of a 40-V HV diode (HVDIO), a 7-V zener diode (ZDIO), a 10-kΩ resistor (R), and a 5-V NMOS device (M1). The reverse-biased HV diode and zener diode are connected in series to sustain the high-voltage (40V) applications on the output pad (O/P) during the normal circuit operating condition. The margin of 7V from the total breakdown voltage of the diodes to the operating voltage is used to avoid mis-triggering on the LDNMOS, even if a 10% overshooting voltage happens to the pad. Therefore, the gate-driven ESD protection circuit can be ensured against gate-oxide overstress issue under the normal circuit operating condition. The gate of M1 is connected to the low-voltage power supply (VDDA). The turned-on NMOS (M1) keeps the gate of the LDNMOS at VSS, so the ESD clamp device (M_{ESD}) is guaranteed to be kept off during the normal operating condition. When a positive fast-transient ESD voltage is applied to the output pad with VSS grounded and VDDA floating, the HV diode and the zener diode will enter the breakdown mode to conduct some of ESD current across the resistor R to generate bias voltage to the gate of M_{ESD}. Therefore, the gate voltage of M_{ESD} can be quickly pulled up to turn itself on by the gate-biased technique during ESD stress. After that, the ESD clamp device enters the snapback region to discharge ESD current from the output pad to VSS. The VDDA is initially floating with an initial voltage level of ~0V during ESD stress event, so M1 is kept in off state without influence on the operation of ESD clamp device.

In Fig. 5.8(b), the substrate-triggered ESD protection circuit includes not only the HVDIO, ZDIO, R, and M1 (which are used in gate-driven ESD detection circuit), but also an additional LDNMOS (M_N) as driving element and a 5-V NMOS device (M2). The gates of M1 and M2 are connected to VDDA to keep the voltage levels at the gate of M_N and the

P+_trig node of the ESD clamp device (M_{ESD}) at VSS. During the ESD transient event, the driving element M_N is turned on by the gate-biased effect from the diodes in breakdown mode, and then generates some channel current through M_N into the P+_trig node of the ESD clamp device (M_{ESD}). The substrate-triggered effect can be accomplished to accelerate the turn-on speed of the ESD clamp device.



(a)



(b)

Fig. 5.8. The proposed ESD protection circuits with (a) gate-driven, and (b) substrate-triggered, ESD detection circuits.

5.4 Experimental Results

The proposed ESD protection circuits have been fabricated in a 0.35-μm 5V/40V BCD

process. No any additional mask layer is needed to fabricate the proposed ESD protection circuits. The typical gate-coupled LDNMOS by connecting a resistor from its gate to VSS has been also fabricated in the same wafer for comparison with the proposed gate-driven and substrate-triggered ESD protection circuits. The gate-coupled LDNMOS is drawn by multiple finger structure with each finger width of 75μm, and the total device width is 300μm. On the other hand, the ESD clamp device in the proposed ESD protection circuits are drawn by 2 × 2 octagonal cells with equivalent total device width of 320μm. To investigate the device behavior during ESD stress, the transmission line pulsing (TLP) technique has been widely used to measure the trigger voltage (Vt1) and the secondary breakdown current (It2) of ESD devices. The TLP generator (TLPG) with a pulse width of 100 ns and a rise time of 10 ns is used in this work to find the Vt1 and It2 of the LDNMOS with gate-biased or substrate-triggered technique. The HBM ESD levels and MM ESD levels of the ESD protection circuits are measured by KeyTek ZapMaster and the failure criterion is defined as the I-V characteristic curve shifting over 20% from its original curve after three continuous ESD zaps at every ESD test level.

5.4.1. TLP Characteristics of Stand-Alone LDNMOS with Gate-Biased or Substrate-Triggered Effects

The TLP-measured I-V characteristics of the LDNMOS device drawn by 2 × 2 octagonal cells with equivalent total device width of 320μm under different gate-biased voltages (Vg) are shown in Fig. 5.9. Without any gate-biased voltage, the Vt1 of the LDNMOS device is ~60V. When the gate-biased voltage is increased to 1V, 3V, and 5V, the Vt1 of the LDNMOS device is reduced to around 57V, 50.5V, and 48V, respectively. With the gate-biased voltage of 8V and 10V, the Vt1 of the LDNMOS device can be reduced to ~40V. The TLP-measured I-V characteristics of the LDNMOS device drawn by 2 × 2 octagonal cells with equivalent total device width of 320μm under different substrate-triggered currents (I_trig) are shown in Fig. 5.10. When the applied substrate-triggered current is higher than 130mA (equivalent to 0.4mA/μm), the parasitic NPN BJT in the LDNMOS device starts to be turned on, and the Vt1 of the LDNMOS device is reduced. When the I_trig is increased to 0.5mA/μm and 0.55mA/μm, the Vt1 can be reduced to 45V and 23V, respectively. When the I_trig is higher than 0.6mA/μm, the LDNMOS can be turned on rapidly to enter the snapback region without the breakdown mechanism, so the Vt1 is observed as ~11V. From the experimental results of the TLP characteristics of the LDNMOS device with gate-biased

voltage and substrate-triggered current, the acceleration to the turn-on speed of LDNMOS device can be achieved by the gate-biased or substrate-triggered techniques.

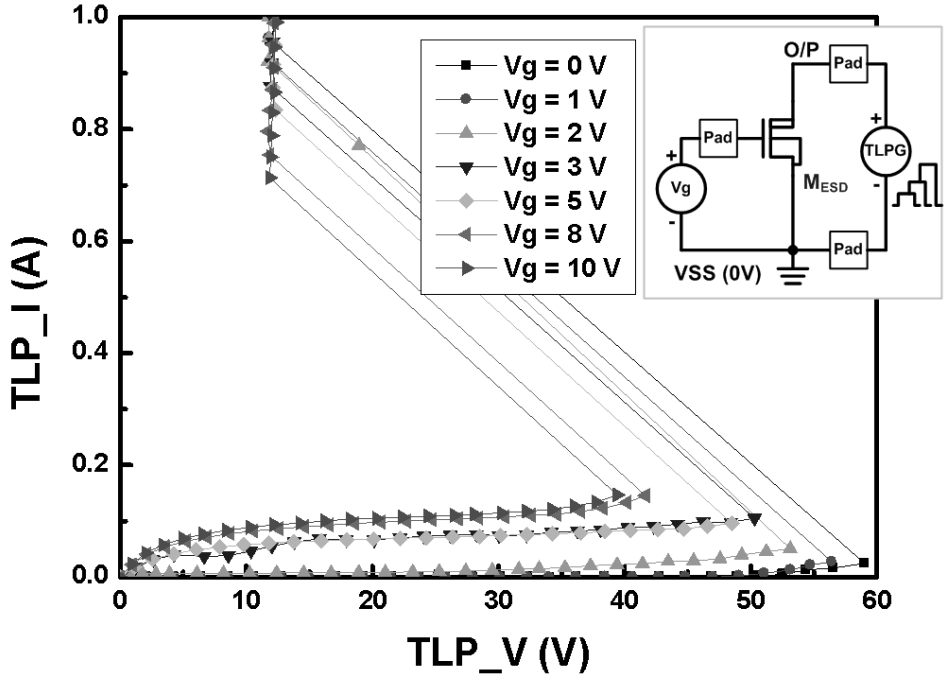


Fig. 5.9. TLP-measured I–V curves of the LDNMOS device drawn by 2 × 2 octagonal cells with device width of 320μm under different gate-biased voltages (Vg).

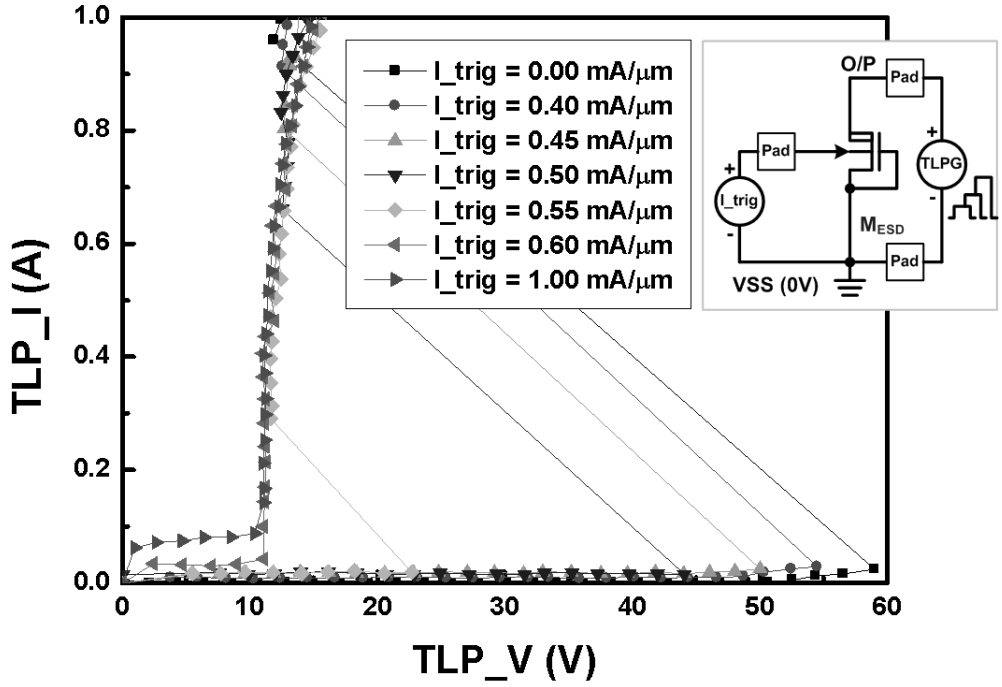


Fig. 5.10. TLP-measured I–V curves of the LDNMOS device by with 2 × 2 octagonal cells with device width of 320μm under different substrate-triggered currents (I_trig).

5.4.2. ESD Performance of LDNMOS with Gate-Coupled Design

The TLP-measured I-V characteristics of the gate-coupled LDNMOS with the resistor of 10kΩ and 50kΩ are shown in Fig. 5.11. The trigger voltage of the gate-coupled LDNMOS with device width of 300μm is still ~60V which is the same as the Vt1 of the standalone gate-grounded LDNMOS with the same device width. Moreover, there is no obvious difference between these two conditions with resistors of 10kΩ and 50kΩ, because the parasitic capacitance from gate to drain of the LDNMOS device is too small to couple sufficient transient voltage to the gate for triggering on the LDNMOS device.

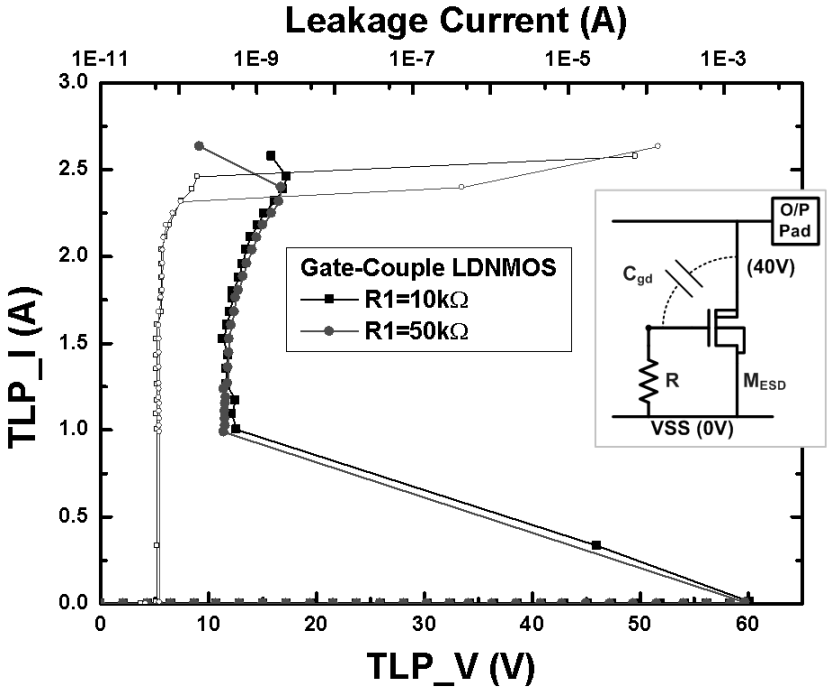


Fig. 5.11. The TLP-measured I-V characteristics of the gate-coupled LDNMOS (drawn by multiple-finger structure with width of 300μm) with resistors of 10kΩ and 50kΩ connected from gate to source.

5.4.3. ESD Performance of LDNMOS with Gate-Driven and Substrate-Triggered ESD Detection Circuits

The TLP-measured I-V characteristics of the gate-driven ESD protection circuit and the substrate-triggered ESD protection circuit are shown in Fig. 5.12, where the I-V characteristic of the gate-coupled LDNMOS with resistor of 10kΩ is also plotted into the figure for comparison. As seen in Fig. 11, the LDNMOS starts to be turned on by the gate-driven or

substrate-triggered ESD detection circuit when the applied voltage is higher than 47V. The Vt1 of the LDNMOS with the gate-driven ESD detection circuit and substrate-triggered ESD detection circuit can be reduced to ~55V and ~51V, respectively. From the TLP measured I-V curves, both gate-driven and substrate-triggered ESD detection circuits are effective in triggering on the LDNMOS device, where the substrate-triggered ESD detection circuit gains more benefit to reduce the Vt1. However, it needs an additional device M_N as the driving element which will occupy some layout area. The leakage current of the gate-coupled LDNMOS was obviously increased when the TLP current is higher than 2.1A. The failure criterion for the It2 measurement is determined by leakage current increasing 30% compared to that of fresh samples in this work. Therefore, the It2 level of the gate-coupled LDNMOS is determined as 2.1A. However, the It2 of the LDNMOS drawn by 2 × 2 octagonal cells with the gate-driven and substrate-triggered ESD detection circuits can be improved up to 2.6A and 2.7A, respectively.

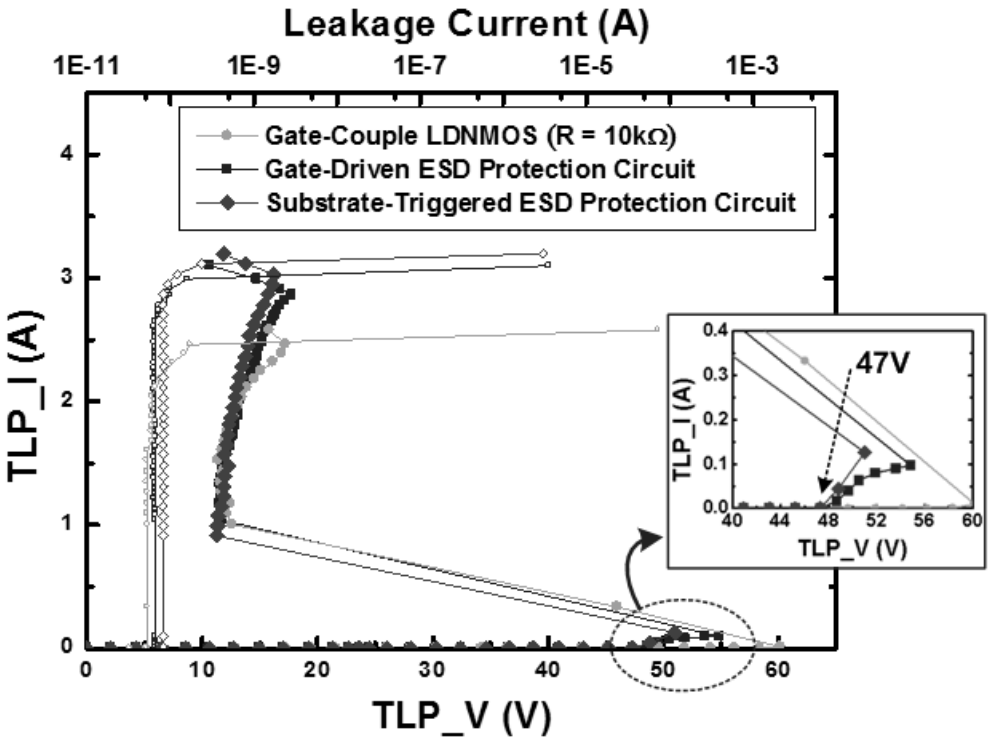


Fig. 5.12. The TLP-measured I-V characteristics of the LDNMOS with the proposed ESD detection circuits and the gate-coupled LDNMOS.

The HBM and MM ESD levels of the gate-coupled LDNMOS, the gate-driven ESD protection circuit, and the substrate-triggered ESD protection circuit are listed in Table 5.1. The gate-coupled LDNMOS has ESD levels of 3kV in HBM and 200V in MM ESD tests. With the gate-driven ESD detection circuit, the HBM and MM ESD levels of LDNMOS can

be improved to 4.4kV and 275V, respectively. With the substrate-triggered ESD protection circuit, the HBM and MM ESD levels of LDNMOS are 4.2kV and 275V, respectively. No obvious difference in ESD robustness of the LDNMOS device with these two ESD detection circuits, because each octagonal cell of the LDNMOS device can be turned on uniformly. If a higher ESD level is desired, the number of the octagonal cells in LDNMOS should be increased to sustain the ESD stress.

Table 5.1

Comparison of ESD Robustness among the Gate-Coupled LDNMOS, Gate-Driven ESD Protection Circuit, and Substrate-Triggered ESD Protection Circuit

	Layout Type of M_{ESD}	Width of M_{ESD}	HBM ESD Level	MM ESD Level	It2 (TLP)
Gate-Coupled LDNMOS	Multiple-Finger	300μm	3kV	200V	2.1A
Gate-Driven ESD Protection Circuit	Octagonal Cells	320μm	4.4kV	275V	2.6A
Substrate-Triggered ESD Protection Circuit	Octagonal Cells	320μm	4.2kV	275V	2.7A

5.4.4. Failure Analysis

The experimental results have shown that the trigger voltage of the LDNMOS device can be substantially reduced by the gate-driven and substrate-triggered ESD detection circuits. Failure analyses carried by SEM images provide the visual evidence to the LDNMOS device drawn in multiple octagonal cells which can be triggered on uniformly by the ESD detection circuit. Fig. 5.13 shows the ESD failure locations on the proposed gate-driven ESD protection circuit after 4.6-kV positive-to-VSS HBM ESD stress. The failure spots were found at the drain contacts in each cell of the LDNMOS device, indicating that the LDNMOS device has been uniformly turned on by the proposed gate-driven ESD detection circuit.

5.5. Power-Rail ESD Protection Design

From the TLP-measured I-V characteristic in Fig. 5.12, the snapback holding voltage of LDNMOS with the gate-driven or substrate-triggered ESD detection circuit is ~12V, which is smaller than the HV power supply voltage (VDD_HV) of 40V. Such an ESD element used in

the power-rail ESD protection circuit may be mis-triggered on by the system-level ESD transient pulse to cause latchup failure [93], [94]. To overcome the latchup issue between the power rails, the stacked-LDNMOS structure is used to increase the total holding voltage. With the gate-driven ESD detection circuit, the trigger voltage of the stacked LDNMOS structure can be still kept the same as that of the design in Fig. 5.8(a). The circuit diagram of the stacked-LDNMOS structure (four LDNMOS devices in series, where each LDNMOS is drawn by multiple finger structure with width of 300μm) with the gate-driven ESD detection circuit is shown in Fig. 5.14(a). The corresponding TLP-measured I-V characteristic is shown in Fig. 5.14(b). During ESD stress, the stacked LDNMOS can be triggered into snapback region to discharge ESD current. With a total holding voltage of ~50V, the latchup issue can be successfully overcome for 40-V applications [95]. Therefore, the latchup-free power-rail ESD protection circuit can be safely applied in IC products with high-voltage power supply voltage of 40V. The It2 level is still kept at ~2.5A, so the ESD performance of the stacked-LDNMOS structure with gate-driven ESD detection circuit can be kept as good as that of a single LDNMOS device. Of course the stacked-LDNMOS can be also implemented with the layout of octagonal cells in the power-rail ESD protection circuit.

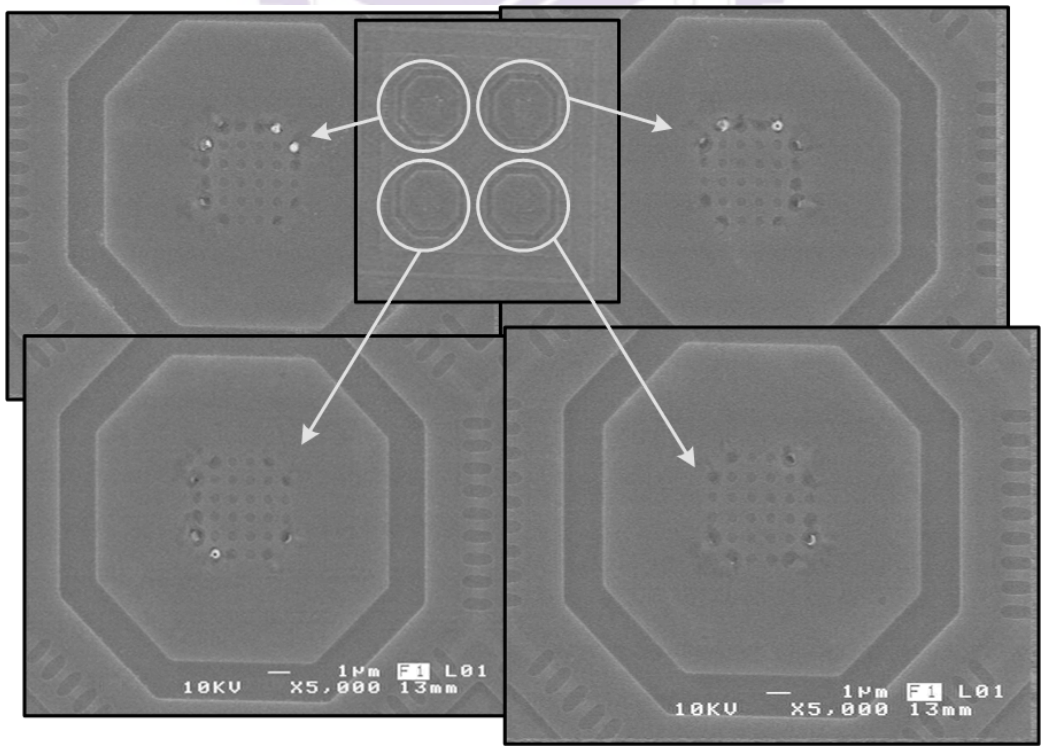
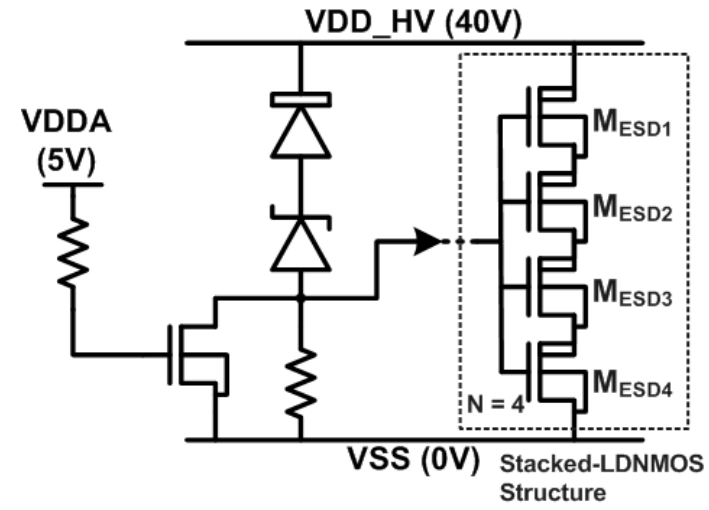


Fig. 5.13. After 4.6-kV HBM ESD stress, the failure spots were found at the drain contacts of each unit cell of the LDNMOS device with the gate-driven ESD protection circuit.



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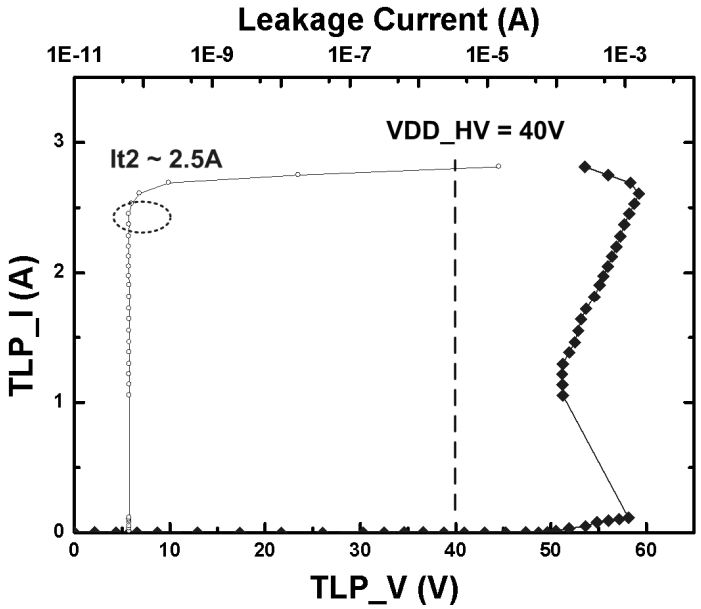

(b)

Fig. 5.14. (a) The latchup-free ESD protection circuit realized with four stacked-LDNMOS devices and the gate-driven ESD detection circuit for 40-V power pins, and (b) the corresponding TLP-measured I-V characteristics.

5.6. Summary

The device characteristics of the LDNMOS with gate-biased and substrate-triggered effects have been investigated in details by TCAD simulation and TLP measurement. Based

on such device behaviors, two ESD protection circuits cooperated with LDNMOS for 40-V output pad have been successfully verified in a 0.35-μm 5V/40V BCD process. The proposed ESD protection circuits with gate-driven and substrate-triggered techniques have performed the efficient turn-on uniformity with robust ESD levels, which are excellent design solutions to protect the high-voltage output drivers for smart power applications. By using the stacked-LDNMOS structure with the gate-driven ESD detection circuit, the latchup-free ESD protection circuit can be achieved for protecting the high-voltage power pins.

Chapter 6

Conclusions and Future Works

This chapter summarizes the main results and contributions of this dissertation. Suggestions for future research topics in the fields of low-leakage ESD protection designs for whole-chip ESD protection and mixed-voltage I/O interfaces in fully silicided low-voltage CMOS process are also provided in this chapter.

6.1 Main Results of This Dissertation

In this dissertation, the novel ESD protection circuits have been developed for nanoscale CMOS process, mixed-voltage I/O interfaces and high-voltage BCD process with high ESD robustness. The low-leakage and latchup-free ESD protection circuits are proposed for different generations and high-voltage-tolerant applications. Each of the ESD protection circuits has been successfully verified in the testchips.

In chapter 2, to provide effective on-chip ESD protection with low standby leakage current in nanoscale CMOS technology, a new power-rail ESD clamp circuit with low standby leakage current for nanoscale IC product has been proposed and verified. The new power-rail ESD clamp circuit is implemented by using the silicon controlled rectifier (SCR) device and ESD detection circuit with substrate-triggered technique. The special ESD detection circuit is designed with consideration of gate current to reduce the standby leakage current. By controlling the gate current of the devices in the ESD detection circuit under a specified bias condition, the whole power-rail ESD clamp circuit can achieve an ultra-low standby leakage current. The new proposed design has been fabricated and verified in a 65nm fully-silicided CMOS process. The new proposed power-rail ESD clamp circuit can achieve 7kV in HBM and 325V in MM ESD levels while consuming only a standby leakage current of 96nA at room temperature under 1-V bias and occupying an active area of only 49μm×21μm.

In chapter 3, to protect the mixed-voltage I/O interfaces in nanoscale CMOS technology, a new high-voltage-tolerant ESD clamp circuit has been proposed and verified to protect the

mixed-voltage I/O circuits for receiving signals with 2×VDD voltage level. The devices used in the high-voltage-tolerant ESD protection design are all 1V low-voltage thin gate-oxide NMOS/PMOS devices which can be safely operated under the 1.8V bias conditions without suffering from the gate-oxide reliability issue. The gate current of each thin gate devices in the high-voltage-tolerant ESD detection circuit has also been considered. The proposed ESD detection circuit, designed with consideration of gate leakage current, has been verified with a very small standby leakage current of only 0.15μA under 1.8-V bias at 25°C, and has also shown the effectiveness on reducing the trigger voltage of the SCR device. Compared with the prior work, the new proposed power-rail ESD clamp circuit with advantages of low standby leakage current, high ESD robustness, and no gate-oxide reliability issue is an excellent circuit solution for on-chip ESD protection design for mixed-voltage I/O buffers in nanometer CMOS technologies. The new proposed circuit can achieve 6.5kV in HBM and 350V in MM ESD levels.

In chapter 4, to protect the 3×VDD-tolerant I/O buffer without using any extra mask sets, two new ESD protection design by using only 1×VDD low-voltage devices for mixed-voltage I/O buffer with 3×VDD input tolerance have been proposed and verified. Two different special high-voltage-tolerant ESD detection circuits are designed with substrate-triggered technique to improve ESD protection efficiency of ESD clamp device. These two ESD detection circuits with different design concepts both have effective driving capability to trigger the ESD clamp device on. With ESD bus, the four modes of ESD stresses on the mixed-voltage I/O pad to VDD or VSS have the corresponding well-designed ESD discharging paths in the proposed ESD protection scheme. These ESD protection designs have been successfully verified in two different 130nm 1.2-V CMOS processes to provide excellent on-chip ESD protection for 1.2-V/3.3-V mixed-voltage I/O buffers. The new proposed 3×VDD-tolerant power-rail ESD clamp circuits can achieve higher than 8kV in HBM and 440V in MM ESD levels.

In chapter 5, the device characteristics of the LDNMOS with gate-biased and substrate-triggered effects have been investigated in details by TCAD simulation and TLP measurement. The proposed ESD protection circuits with gate-driven and substrate-triggered techniques have performed the efficient turn-on uniformity with robust ESD levels, which are excellent design solutions to protect the high-voltage output drivers for smart power applications. The proposed ESD protection design can well bias the lateral DMOS (with 5V gate-oxide but 40V operating voltage at drain side) without gate-oxide reliability under the

normal condition. The ESD protection design has been successfully verified in a 0.35-μm 5-V/40-V BCD process. The proposed ESD protection circuits can achieve 4.2kV in HBM and 275V in MM ESD levels.

6.2 Future Works

In mixed-voltage I/O interfaces, the effective ESD protection circuits with consideration of gate current for nanoscale have been proposed and verified in this dissertation. But, the whole-chip ESD protection design for a real IC product with more complex circuits and power domains should be considered in nanoscale CMOS technology. The cross power domain ESD protection design should be verified with proposed low-leakage ESD protection designs. The design criterion of the power bus, ESD bus, and the device dimension of low-leakage ESD protection designs could be developed for a real IC product. Moreover, in nanoscale CMOS technology, the ESD protection circuits should be designed for CDM ESD event, which will be a serious challenge to protect ultra-thin gate-oxide, especially for the SoC applications with a large chip area. In high-voltage BCD technology, the ESD robustness and turn-on speed of the ESD protection design with has been improved and verified in this dissertation. In addition, the holding voltage of the stacked-device structure can be designed higher than the supply voltage to avoid the latchup or latchup-like issues in high-voltage BCD ICs. But the layout area of the stacked-device structure will increase as compared to that of the single device, especially for high ESD robustness requirement. The design of new device with the characteristics of both high holding voltage and efficient turn-on speed from the structure design or process modification will be a useful solution. For example, the SCR device or FOX device with high-holding behavior might be a good approach. By adjusting the well profiles of each junction, a non-snapback ESD device might be achieved. Such ESD topics will be the continual future works for research.

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Low-Leakage Power-Rail ESD Protection Designs in CMOS Integrated Circuits

Publication List

(A) Referred Journal Papers:

[1] M.-D. Ker and **Chang-Tzu Wang**, "Design of high-voltage-tolerant ESD protection circuit in low-voltage CMOS processes," *IEEE Trans. on Device and Materials Reliability*, vol. 9, no. 1, pp. 49-58, Mar. 2009.

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(D) Local Conference Papers:

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[2] **王暢資**、唐天浩、蘇冠丞、柯明道, "65奈米金氧半製程中具低漏電流之靜電防護電路設計," 2009年台灣靜電放電防護技術研討會.

(E) Patents:

[1] **Chang-Tzu Wang** and M.-D. Ker, "ESD detection circuit," **US Patent 7586721**, Sep. 2009 and TW patent pending.

[2] M.-D. Ker, C.-Y. Lin, and **Chang-Tzu Wang**, "Silicon controlled rectifier," **US Patent 7582916**, Sep. 2009.

[3] M.-D. Ker, C.-Y. Lin, and **Chang-Tzu Wang**, "ESD protection circuitry with multi-finger SCRs," US, CN, and TW Patent pending.

[4] M.-D. Ker, Y.-W. Hsiao, and **Chang-Tzu Wang**, "Electrostatic discharge protection device and related circuit," US Patent pending.

[5] M.-D. Ker, C.-Y. Lin, and **Chang-Tzu Wang**, "Electrostatic discharge protection circuit," US Patent pending.

[6] M.-D. Ker, **Chang-Tzu Wang**, and C.-C. Wang, "2×VDD-tolerant power-rail ESD clamp circuit with ultra-low standby leakage current," US and TW Patent pending.