國立交通大學

電子工程學系 電子研究所

博 士 論 文

單軸應變矽奈米尺寸金氧半場效電晶體對於載子遷移率之各種散射機制的實驗性研究

Experimental Investigation of Carrier Mobility considering Various Scattering Mechanisms for Uniaxial Strained MOSFETs

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摘要

此研究針對單軸應變對於載子遷移率中不同散射機制的影響做一個全面性的探討。首先，我們引進一個以柏克萊短通道 IGFET 模型(BSIM)的寄生電阻萃取方法。這個方法比傳統的通道電阻法還有偏移比例法(Shift & Ratio Method)還要準確，因為它考慮了因為單軸應變跟水平方向非均勻通道摻雜所導致的遷移率變化. 我們利用了各種不同的製程條件來驗證這個方法而且跟實驗數據都能夠一致性的吻合。這個以柏克萊短通道 IGFET 模型為基礎的寄生電阻萃取方法也透過半導體工藝模擬以及器件模擬工具(Technology Computer Aided Design)得到驗證。

除此之外，我們利用分離式電容電壓量測 (Split-CV Method) 的方式萃取短通道載子遷移率進而探討單軸應變對短通道載子遷移率的影響。接著對於 N 型及 P 型金氧半場效電晶體，我們在不同溫度下針對庫倫散射遷移率與應力之間的關係作實驗性的探討。我們的研究結果發現應力對於庫倫散射遷移率的敏感度跟溫度呈現顯著關係，這是因為基板電荷跟介面電荷散射機制互相抗衡的結果。因此，為了要將應力對於庫倫散射遷移率的效益極佳化 ，必須要將介面電荷加以抑

制。

除此之外，透過低溫系統量測，我們也探討了單軸應變對於P型金氧半場效電晶體表面粗糙散射遷移率的影響。我們更進一步比較了應力對於表面粗糙散射遷移率跟聲子散射遷移率的敏感度。我們量測數據指出應力很明顯的提升表面粗糙散射遷移率，同時表面粗糙散射遷移率的敏感度比聲子散射遷移率的敏感度還要高。我們的實驗結果證實了之前發表過的模擬結果。除此之外，本文也從波函數穿透的觀點來解釋應力改變表面粗糙散射遷移率的可能原因。

此外， 我們在奈米尺寸 P 型金氧半場效電晶體實驗性地評估單軸應變對於載子遷移率的溫度效應。研究結果指出電洞遷移率對於應力的改變量隨著溫度增加而減少，這個結果跟之前利用單軸機械彎曲實驗研究結果一致. 此現象是因為溫度增加的時候，更少的電洞會聚集在能使等效載子質量變輕的能帶邊緣，進而使得應力效率降低。同時，藉由低溫量測系統分開萃取表面粗糙散射遷移率跟聲子散射遷移率, 我們更進一步在P型金氧半場效電晶體探討應力對於聲子散射遷移率的溫度效應。而從萃取出的表面粗糙散射遷移率跟聲子散射遷移率數據中，它們跟垂直電場以及溫度的關係跟已經發表文獻的數據也是一致的。而聲子散射遷移率跟溫度的關係會因為壓縮單軸應力的增加而變強，其原因是因為壓縮單軸應力增加會使得光熱子能量增加，進而增加了聲子散射遷移率對於溫度的敏感度，而這新發現也可以解釋為何汲極電流的溫度效應在單軸應變金氧半場效電晶體會變的更加敏感。

關鍵字: 金氧半場效電晶體， 單軸應變， 庫倫散射， 表面粗糙散射， 聲子散射， 外部寄生電阻， 遷移率

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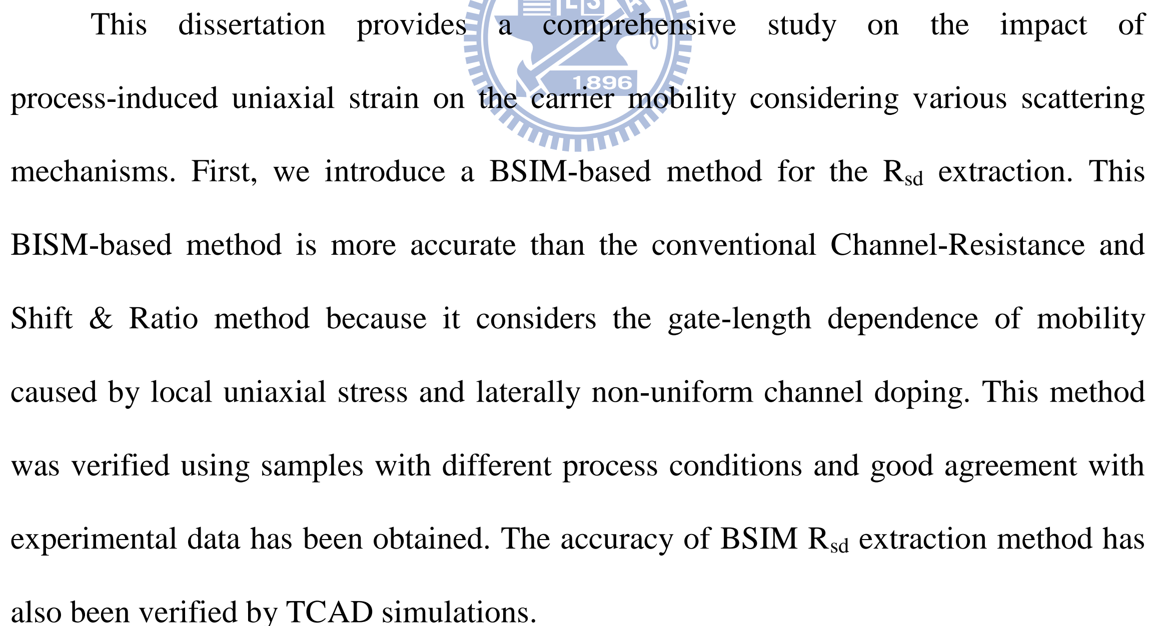
Abstract



This dissertation provides a comprehensive study on the impact of process-induced uniaxial strain on the carrier mobility considering various scattering mechanisms. First, we introduce a BSIM-based method for the R_{sd} extraction. This BISM-based method is more accurate than the conventional Channel-Resistance and Shift & Ratio method because it considers the gate-length dependence of mobility caused by local uniaxial stress and laterally non-uniform channel doping. This method was verified using samples with different process conditions and good agreement with experimental data has been obtained. The accuracy of BSIM R_{sd} extraction method has also been verified by TCAD simulations.

In addition, the short channel mobility extraction method by using split-CV is introduced to investigate the strain impact on short channel mobility. Then the uniaxial strain dependence of Coulomb mobility extracted by Matthiessen's rule is experimentally investigated for both nMOSFETs and pMOSFETs under various

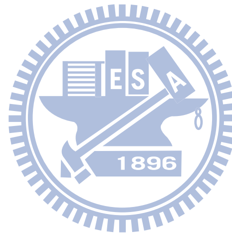
temperatures. Our study indicates that the stress sensitivity of the Coulomb mobility shows strong temperature dependence. It is due to the competition result of the stress sensitivity between bulk charge scattering and interface charge (N_{it}) scattering. Therefore, in order to optimize the strain efficiency on Coulomb mobility, it is necessary to suppress the formation of N_{it}.

Besides, through He-based low temperature measurement, the uniaxial strain dependence on surface roughness mobility (μ_{SR}) of pMOSFETs is also studied. Moreover, we compare the strain sensitivity between μ_{PH} and μ_{SR}. Our measured data indicates that μ_{SR} can be significantly enhanced by the uniaxial compressive strain. Furthermore, the μ_{SR} has higher strain dependence μ_{PH}. Our experimental results confirm the previously reported simulation results. In addition, a wavefunction penetration perspective is proposed to explain the possible physical origin of the uniaxial strain dependence of μ_{SR}.

Moreover, we experimentally assess the impact of process-induced uniaxial strain on the temperature dependency of carrier mobility in nanoscale pMOSFETs. Our study indicates that the strain sensitivity of hole mobility becomes less with increasing temperature and it is consistent with previous uniaxial mechanical bending result. It is because the less hole repopulations at energy band edge induce less strain sensitivity as temperature increases. Furthermore, through decoupling μ_{SR} and $\mu_{PH,}$ we investigate the impact of uniaxial strain on the temperature dependence of phonon-scattering limited mobility in nanoscale PMOSFETs. The vertical electric field dependence (E_{EFF}) and temperature dependence of the extracted μ_{SR} and μ_{PH} are consistent with the reported data in the literature. The temperature sensitivity of the extracted phonon mobility becomes higher when compressive strain is applied. It is contributed by the higher optical phonon energy induced by uniaxially-compressive strain. Our new findings also

explain the higher temperature sensitivity of drain current presented in uniaxial strain PMOSFETs.

Keywords: MOSFET, Uniaxial strain, Coulomb, Surface roughness, Phonon, External series resistance, mobility



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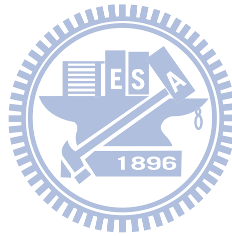

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Fig. 5.11 Schematic plot of E-k energy band diagram under uniaxial compressive stressor in PFET. Optical phonon energy ($\hbar\omega_o$) may increase when compressive uniaxial strain is applied.…………………………………133

Chapter 1

Introduction

1.1 Background and Motivation

For the past 50 years, the geometry scaling of silicon complementary metal-oxide semiconductor (CMOS) continues keep Moore's law effective by increasing in circuit integration density and also boosting transistor performance. In order to maintain Moore's law in nanoscale regime, the optimizations on the parasitic external resistance reduction and carrier mobility enhancement becomes more critical for the transistor design. For the past 25 years, global biaxial tensile strain technology has been widely developed to boost transistor mobility for both NMOSFET and PMOSFET [1]. This global biaxial strain technology is using a wafer-based approach of a thin strained Si layer on a thick relaxed Silicon-Gemanium (SiGe) virtual substrate. It is known that strain can improve phonon scattering limited mobility (μ_{PH}) by reducing inter-valley phonon scatterings and effective conduction mass [2]. However, the benefits of mobility enhancement only occur at low electric field and high stress level by this global strain [2]. Furthermore, the junction leakage induced by the lattice mismatch from silicon (Si) and gemanium (Ge) is also a barrier to implement the technique into mass production.

Recently, local uniaxial strained-Si technology becomes the preferred method to boost transistor mobility in nanoscale CMOS development and has been considered as a key process knob beyond 90nm technology [2-4]. The uniaxial strain process has the following advantages comparing with biaxial strain process: (a) Uniaxial strain provides more flexibility from the perspective of CMOS integration process since it may apply different strain polarity for NMOSFET and PMOSFET separately. (b) Uniaxial strain has no same junction leakage issue with biaxial strain. (c) Uniaxial strain provides

significant mobility enhancement at both high field and low field region. (d) The uniaxial strain results in significantly smaller stress-induced threshold shift due to less bandgap narrowing. (e) Uniaxial strain provides better mobility enhancement than biaxial strain due to different band engineering mechanism and high stress levels.

Nevertheless, since the series resistance (R_{sd}) may counteract the actual mobility enhancement in these strained devices, an accurate R_{sd} value has to be used in the extraction of intrinsic effective mobility (μ_{eff}). The most popular methods in the determination of R_{sd} are the conventional Channel-Resistance method [5] and Shift & Ratio method [6]. However, both methods are no longer suitable to nano-scale strained-silicon MOSFETs with halo implants because the laterally non-uniform halo doping as well as the uniaxial stress may result in a total resistance (R_{tot}) which does not scale linearly with gate length [7,8]. It is difficult to determine R_{sd} accurately from the non-linear R_{tot} vs. gate length characteristics. Therefore, an adequate method that may accurately determine R_{sd} for nano-scale strained-silicon MOSFETs with halo implants is sorely necessary.

It is known that uniaxial strain can improve phonon scattering limited mobility (μ_{PH}) from band engineering and carrier repopulations [2]. However, because Coulomb mobility ($\mu_{Coulomb}$) and surface roughness mobility (μ_{SR}) dominate at low and high vertical electric field (E_{EFF}) respectively, whether uniaxial strain can improve $\mu_{Coulomb}$ and μ_{SR} is still not clear and merits of further investigation.

Recently, several studies [9-12] reported degraded carrier mobility for short channel devices and pointed out the increasing importance of Coulomb scatterings due to halo implantations. Although Gamiz et al. [11] and Nayfeh et al. [10] have shown that Coulomb mobility is not enhanced in strained-Si nMOSFETs, Weber and Takagi [9] have demonstrated that the mobility limited by substrate impurity scattering is still

enhanced in long-channel strained devices (L=10μm). These findings seem to be inconsistent for biaxial strained MOSFETs, and further examination on $\mu_{Coulomb}$ is needed, especially for state of the art uniaxial strained MOSFETs.

Recently, the biaxial strain dependence of μ_{SR} has been examined by Bonno *et al.* [13] and Zhao *et al.* [14]. These studies show μ_{SR} has strong strain sensitivity for both nMOSFETs and pMOSFETs with biaxial strain. However, the observed μ_{SR} data by Zhao *et al.* [14] showed opposite trend between NFET and PFET and cannot be easily explained by the micro-roughness of Si/SiO_2 interface. Furthermore, the uniaxial strain dependence of μ_{SR} has not been studied until now.

Besides, the temperature effect on strain-enhanced mobility is of special importance because it may provide insights for the underlying mechanisms responsible for the performance enhancement. Several studies have investigated the temperature effect on strain-enhanced mobility in the past [15-18]. For NMOS, the temperature effect of process-induced biaxial strain [15,16], uniaxial strain [15] and mechanical uniaxial strain [17] applied on devices has been experimentally studied. The results all indicated less strain sensitivity in carrier mobility with decreasing temperature due to less contribution of the intra valley scatterings in the 4-fold valleys. For PMOS, the temperature effect of process-induced biaxial strain [16] and mechanical uniaxial strain [18] has also been investigated. The results showed higher strain sensitivity in carrier mobility with decreasing temperature due to lighter effective conduction mass, i.e., the opposite trend with NMOS. However, the temperature effect of process-induced uniaxial strain in nanoscale PMOS devices is still not reported and merits investigation.

Furthermore, the temperature sensitivity of drain current for the compressively-strained PFET is larger than that of the unstrained counterpart. Our new

finding in this work [19], the strain-enhanced temperature sensitivity of μ_{PH}, has unveiled the underlying mechanism responsible for these observations.

1.2 Organization

This dissertation includes six chapters.

In Chapter 1, the background and the motivation of this thesis are discussed.

In Chapter 2, we introduce the BSIM-based method for the R_{sd} extraction [20]. Using this method, R_{sd} can be well extracted in nano-scale strained devices. We have verified this method using samples with different process conditions and good agreement with experimental data has been obtained. This BSIM-based method is also verified by TCAD simulated current-voltage (IV) characteristics [21]. The extracted R_{sd} will be used in the following chapters for the extraction of carrier mobility.

In Chapter 3, by using the split-CV method [22], the channel mobility in the short channel devices can be extracted by calibrating the extracted R_{sd} values from Chapter 2, as a shown in Fig. 1.1. Then we assessed the impact of process-induced uniaxial strain on Coulomb mobility in short-channel nMOSFETs and pMOSFETs under various temperatures [23,24]. We also utilized the four-point mechanical bending technique on both short and long channel devices in PMOSFETs. Our study indicates that the stress sensitivity of the Coulomb mobility shows strong temperature dependence due to the competition result of the stress sensitivity between bulk charge scattering and interface charge scattering [9,25]. In order to improve the strain efficiency on Coulomb mobility, it is necessary to suppress the formation of interface charges (N_{it}).

In Chapter 4, we examined the impact of strain on surface roughness mobility (μ_{SR}) of pMOSFETs by process-induced uniaxial strain with He-based low temperature system and compare the strain sensitivity between μ_{PH} and μ_{SR} [26]. Our measured data indicates that μ_{SR} can be significantly enhanced by the uniaxial compressive strain.

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Furthermore, the μ_{SR} has higher strain dependence than the phonon scattering limited mobility (μ_{PH}). Our experimental results confirm the previously reported results based on simulations [27,28] In addition, a wavefunction penetration perspective [29,30] is proposed to explain the possible physical origin of the uniaxial strain dependence of μ_{SR}.

In Chapter 5, we conduct an experimental assessment for the impact of process-induced uniaxial strain on the temperature dependency of carrier mobility in nanoscale pMOSFETs [31]. Furthermore, through cryogenic temperature measurement from Chapter 4, we investigate the impact of uniaxial strain on the temperature dependence of phonon-scattering limited mobility in nanoscale PMOSFETs [19]. The E_{EFF} and temperature dependence of the extracted μ_{SR} and μ_{PH} will be discussed and benchmarked with published data [32,33]. Our study indicates that the strain sensitivity of hole mobility becomes less with increasing temperature and it is consistent with previous uniaxial mechanical bending result [18]. The temperature sensitivity of phonon mobility becomes higher when compressive strain is applied. It can be explained by the higher optical phonon energy induced by uniaxially-compressive strain. Our new findings also explain the higher temperature sensitivity of drain current presented in uniaxial strain PMOSFETs.

In Chapter 6, we summarize the key research results and the contribution of this thesis.

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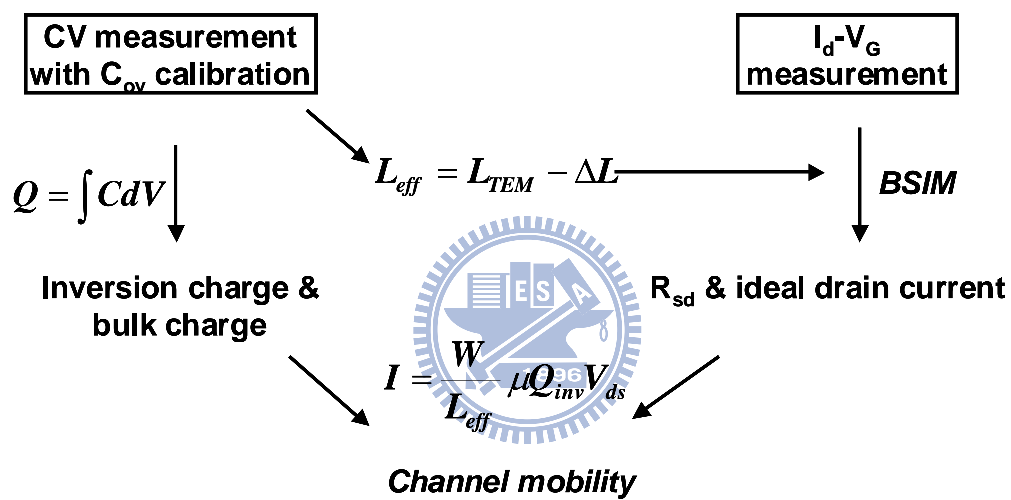

Figure 1.1. The flowchart of the short channel mobility extraction.

Chapter 2

A New Series Resistance Extraction Method for Nanoscale MOSFETs

2.1 Introduction

As strained-silicon and USJ (Ultra Shallow Junction) techniques are widely used to optimize the carrier velocity and parasitic resistances in the MOSFET, an accurate determination of the parasitic source/drain series resistance (R_{sd}) for these nano-scale MOSFETs becomes a crucial issue. Since the series resistance may counteract the mobility enhancement in these strained devices, an accurate R_{sd} value has to be used in the extraction of intrinsic effective mobility (μ_{eff}) during process development. Furthermore, the R_{sd} parameter is critical to evaluate the performance of USJ engineering works.

Among several studies regarding the R_{sd} extraction in the past [1]-[4], Kim et al. [1] proposed an integrated methodology to separate R_{sd} components and utilized the conventional Channel-Resistance method in the determination of R_{sd}. Although the Channel-Resistance method has been widely used [1]-[2], it is no longer suitable to nano-scale strained-silicon MOSFETs with halo implants because the laterally non-uniform channel doping as well as the uniaxial stress may result in a total resistance (R_{tot}) which does not scale linearly with gate length (L_{TEM}) [5]. It is difficult to determine R_{sd} accurately from the non-linear R_{tot} vs. L_{TEM} characteristics.

Another popular method, Shift & Ratio, is also unsatisfactory because its basic assumption that μ_{eff} is independent of L_{TEM} is no longer valid [3]. The uni-axial stress that may increase as L_{TEM} decreases tends to increase the mobility of short-channel devices, while the halo overlapping profile may degrade the mobility of short-channel

devices [6]. Therefore, an adequate method that may accurately determine R_{sd} for nano-scale strained-silicon MOSFETs with halo implants is sorely needed.

In this work, we tackle this problem by a BSIM-based method [7]. Using this method, R_{sd} can be well extracted in nano-scale strained devices. The extracted R_{sd} will be used in the following chapters for the extraction of carrier mobility.

2.2 Devices and Experimental Setup

The devices used in this experiment were fabricated by state-of-the art IC manufacturing technology [10], which provides transistors with gate lengths ranging from 4μm down to 41nm with same channel width (W = 1μm) on 300mm bulk substrate. A 1.2nm nitrided gate oxide was used as a gate dielectric. Processes with ultra low HDE (Highly Doped Extension) energy and unique Spike Rapid Thermal Annealing condition were used to maintain good SCE (Short Channel Effect) control and high activation rate simultaneously. In this study, devices with different extension dosage and various stressors (Tensile/Compressive/Neutral) in NMOS were adopted to verify this extraction methodology. The testkeys constituted by the transistor arrays and calibration patterns are designed for CV measurement. Transistor arrays with Source/Drain tied together can provide enough area to characterize the capacitance in nano-scale devices. Moreover, we have used a high frequency probing system to improve the accuracy and stability of CV characterization results.

2.3 Methodology and Discussion

Fig. 2.1 shows the main procedure of our proposed BSIM-based R_{sd} and μ_{eff} extraction methodology. Table 2.1 provides the related information for key parameters. Please note A_{bulk} is one parameter in BSIM3 which is used to take into account bulk charge effect. As the drain bias is large or the channel length is long, the depletion width is not uniform. This will cause a non-uniform distribution of the threshold voltage along

the channel. This effect is so called bulk charge effect. A_{bulk} is very close to 1 if the channel length is short. Since the effective channel length (L_{eff}) plays a crucial role in the extraction of R_{sd}, it needs to be adequately determined first. L_{eff} can be calculated by (L_{TEM} - $2L_{ov}$) as depicted in Fig. 2.2 L_{TEM} may be obtained from the in-line SEM (Scanning Electron Microscopy) measurement (with accuracy within ± 2nm) at poly patterned stage and the etching-induced length bias(ΔL). L_{ov} represents the overlap distance between source/drain and gate and can be extracted from CV (Capacitance-Voltage) measurement [11,12]. Fig. 2.3 shows the CV curves of different L_{TEM} in NMOS. C_{gc} and C_{ov} can be extracted at gate bias equal to 1.0V and –0.5V respectively [11]. The gate length dependency of extracted C_{gc} and C_{ov} is shown in Fig. 2.4. L_{ov} can be easily obtained from the intercept of C_{gc} and C_{ov} [11,12].

Since the conventional R_{sd} extraction methods, which do not consider the gate length dependency of μ_{eff}, need to conduct the R_{sd} extraction using devices with gate length ranging from short to long channel, their extraction errors are significant. Therefore, in this work, we carried out the R_{sd} extraction based on the nano-scale devices with L_{TEM} from 50nm to 83nm.

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For these short-channel devices, the impact of R_{sd} on the drain current (I_d) in the linear region (V_d = 20mV) can be modeled by Eq. (1):

$$I_d = \mu_{eff} C_{ox} \frac{W}{L_{eff}} \frac{(V_g - V_{th} - V_d/2)V_d}{1 + R_{sd}\mu_{eff} C_{ox} \frac{W}{L_{eff}} (V_g - V_{th} - V_d/2)} \quad (1)$$

Note that Eq. (1) can be derived from the BSIM drain current model [7] under the assumption that the carrier velocity saturation and the bulk-charge effect are negligible. The effective mobility (μ_{eff}) in Eq. (1) can be modeled by [7]

$$\mu_{eff} = \frac{\mu_0}{1+\left(E_{eff}/E_0\right)^{v}} \tag{2}$$

where μ_0, E_0 and v are model fitting parameters. E_{eff} represents the average electric field experienced by the carriers in the inversion layer and is given by $(V_g + V_{th}) / 6T_{ox}$ for an NMOS transistor with n-type poly-silicon gate.

Since the accuracy of Eq. (1) in fitting the experimental data strongly depends on R_{sd}, we propose to determine R_{sd} by the following objective function:

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$$\delta_{\min}(\mu_0',E_0',\upsilon',R_{sd}') = \sum_{L_{TEM}=50\sim 83nm} \left\{ \left| \frac{\left[Id_{Si}(L_{TEM}) - Id_{\text{model}}\left(L_{TEM},\mu_0',E_0',\upsilon',R_{sd}'\right)\right]}{Id_{\text{model}}\left(L_{TEM},\mu_0',E_0',\upsilon',R_{sd}'\right)} \right| \right\} \tag{3}$$

where Id_{si} and Id_{model} represent the measured drain current and the calculated I_d by Eq. (1), respectively. μ_0', E_0' and υ' are the optimized model parameters that may result in a minimum model-hardware discrepancy (δ_{min}) for a given R_{sd}'. The correlation of δ_{min} and R_{sd}' shown in Fig. 2.5 indicates that δ_{min} is sensitive to the change in R_{sd}' and we may therefore determine the true R_{sd} value by finding the local minimum, i.e., $\frac{\partial \delta_{\min}(R_{sd}')}{\partial R_{sd}'} = 0$. For our NMOS devices, the extracted R_{sd} value based on this method is ~165 Ω*μm, which follows the ITRS projection for this technology generation [13].

Note that if the R_{sd} value is not accurate, the drain current ratio of devices with different L_{TEM} will not be correct, as shown in Fig. 2.6. Fig. 2.7 provides the R_{sd} sensitivity with variations on different key parameters, where R_{sd} is the most sensitive to L_{eff} but this can be overcome by careful in-line measurement. It is worth noting that the variation in μ_{eff} has to be limited to within ± 5% if ± 4% R_{sd} variation is the maximum tolerance level. In this work, we carried out the R_{sd} extraction based on the devices with L_{TEM} from 50nm to 83nm, where the variation of μ_{eff} is within ± 5%.

To test our R_{sd} extraction methodology, NMOS and PMOS transistors with various extension conditions have been used. Fig. 2.8 shows the relationship between R_{sd} and the measured overlap capacitance (C_{ov}) for these devices. It can be seen that when we increase the extension dose and hence the overlap distance (L_{ov}), the extracted R_{sd} indeed decreases as C_{ov} increases. R_{sd} values of PMOS are around two times of NMOS.

We assume R_{sd} is independent of L_{TEM} due to the following observations: (i) In Fig. 2.8, R_{sd} is very sensitive to overlap capacitance (C_{ov}). However, Fig. 2.4 shows that C_{ov} is independent of L_{TEM}. (ii) Based on our Tsuprem4 simulation results incorporated with halo implants, the L_{ov} (Extension overlap distance under the poly) is independent on L_{TEM}, as shown in Fig. 2.9.

Once R_{sd} is accurately determined, the intrinsic μ_{eff} may be obtained using Eq. (1). Fig. 2.10 shows the gate-length dependency of mobility ($\mu_{eff}(L_{TEM})$) in our NMOS devices with various stressors. Although the extracted R_{sd} values for both tensile and compressive stressors are almost identical to the sample with zero stress (difference < 10Ω*μm), the local tensile stressor enhances the mobility as L_{TEM} decreases, while the compressive stressor degrades the mobility. For devices with L_{TEM} shorter than 90nm, however, the mobility shows significant degradation with L_{TEM} for all of the stressors.

Several explanations regarding the mobility degradation behavior in the short channel regime were proposed in the past, including halo implants and quasi-ballistic transport characteristics performed in these nano-scale devices [2,14,15]. This issue, nevertheless, deserves further study in the future. Using the extracted μ_{eff} (L_{TEM}) in Eq. (1), good agreement with the silicon data over a wide range of L_{TEM} (41nm to 4μm) can be seen, as shown in Fig. 2.11.

Please note μ_{eff} extracted here is based on the charge density (Q_{inv}) approximated by $C_{ox}\times(V_g-V_{th})$. However, some channel charge still exists in the sub-threshold region. The better approach to obtain the Q_{inv} result is a direct measurement of Q_{inv} (split-CV method) from capacitance measurement, with the mobile channel charge density determined from the gate-to-channel capacitance (C_{gc}), as shown in Eq. (4):

$$Q_{inv} = \int_{V_{fb}}^{V_{gs}} C_{gc} dV_{gs} \tag{4}$$

We will leave it for the detail discussions in chapter 3.

2.4 Verification by TCAD Simulation

To verify the proposed BSIM R_{sd} extraction method, we extract R_{sd} from simulated I_d-V_g curves by Medici simulator [16] and compare with R_{sd} obtained from the ohmic drop in the source region of the simulated device structures. The drain bias condition is set to 50mV. Three values of specific resistivity (7×10^{-8}, 1×10^{-7} and $1.3\times10^{-7}\Omega*cm^2$) are input to modify R_{sd} values and then the related I_d-V_g characteristics are generated for BSIM fitting method.

The inset of Fig. 2.12 shows simulated device structure with potential contour. The voltage drop in the source region is extracted directly from point A on the silicide region (V_A) and point B on the extension boundary (V_B). By using Ohm's law, Rsd can be easily obtained and R_{sd} offset (ΔR_{sd}) in different specific resistivity values can be

extracted directly. ΔR_{sd} here is defined as R_{sd} (ρ_c)- R_{sd} (ρ_c=1x10^{-7}Ω*cm^2). As shown in Fig. 2.12, ΔR_{sd} extracted from potential contour with different specific resistivity values shows the consistent trend with ΔR_{sd} extracted by BSIM fitting method. It indicates that the proposed BSIM method can accurately quantify the difference of R_{sd} and be a suitable monitor tool for USJ (Ultra Shallow Junction) and strained process development.

2.5 Conclusion

We have proposed a BSIM-based method for R_{sd} and μ_{eff} extraction which applies to nano-scale strained-silicon MOSFETs with halo implants. This R_{sd} extraction method may serve as a suitable process monitor tool for USJ (Ultra Shallow Junction) and strained process development. This method is more accurate than the conventional Channel-Resistance and Shift & Ratio method because it considers the gate-length dependence of mobility caused by local uniaxial stress and laterally non-uniform channel doping. We have verified this method using samples with different stressor/doping conditions and good agreement with experimental data has been obtained. Significant mobility degradation in short channel regime has been observed for various uniaxial stressors. The accuracy of BSIM R_{sd} extraction method is also verified by simulated IV characteristics with different external resistant values in short channel region. Therefore, this method may serve as a suitable process monitor tool for USJ and strained process development. The extracted R_{sd} will be used in the following chapters for the carrier mobility extraction.

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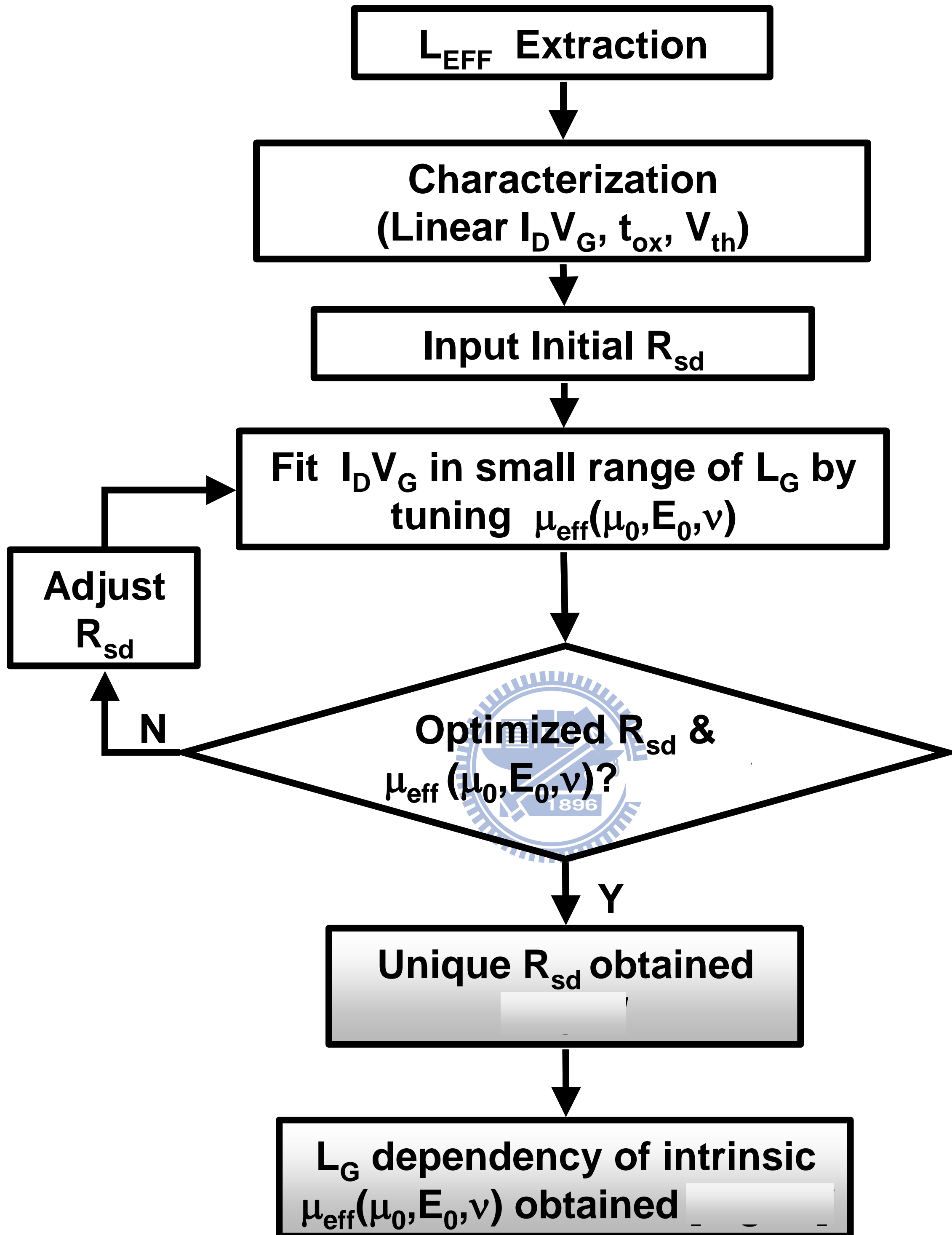

Figure 2.1. Flow chart of the BSIM-based R_{sd} & μ_{eff} extraction method.

Parameter Table	Symbol	Definition
Input Parameter	I_D	*Drain current in linear region*
	C_{gc}	*Gate oxide capacitance*
	L_{ov}	*Gate-extension overlap distance; extracted from C_{gc} and C_{ov}*
	L_{TEM}	*Obtained from L_{SEM} - Δ L. L_{SEM} is from in-line measurement.* *Δ L is a constant offset between L_{TEM} and L_{SEM}*
	L_{eff}	*L_{TEM} -2*L_{ov}*
	μ_{eff}	*Effective mobility; Need to calibrate with R_{sd} by iterations*
	V_{th}	*Threshold voltage from measurement*
	A_{bulk}	*Bulk charge parameter; A_{bulk} ~1 in short channel region*
	E_{sat}	*Saturation electrical field; Set $E_{sat} \sim \infty$ so that $V_{ds}/E_{sat} * L_{eff} \ll 1$*
Fitting Parameter	μ_0	*Mobility fitting parameter*
	E_0	
	ν	
	R_{sd}	*Source/Drain series resistance*

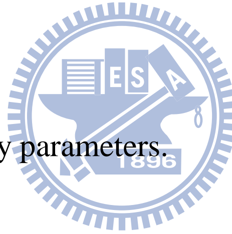

Table 2.1. Definition table of key parameters.

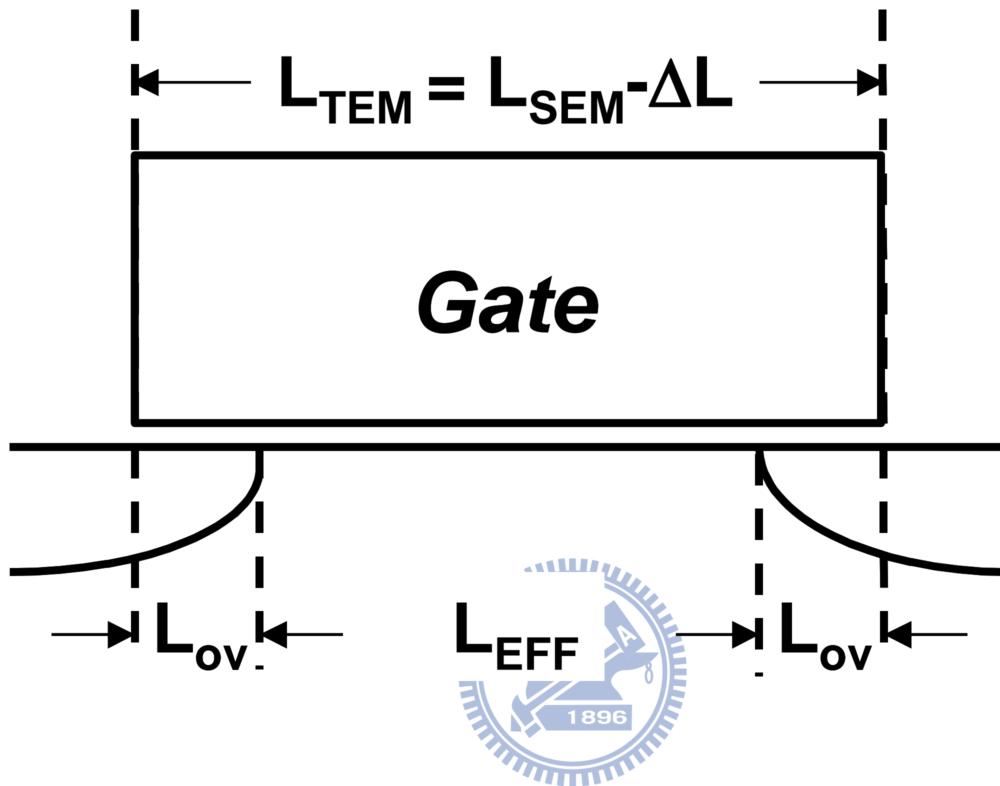

Figure 2.2. Schematic profile of MOSFET. L_{eff} can be obtained by (L_{TEM} – 2*L_{ov}).

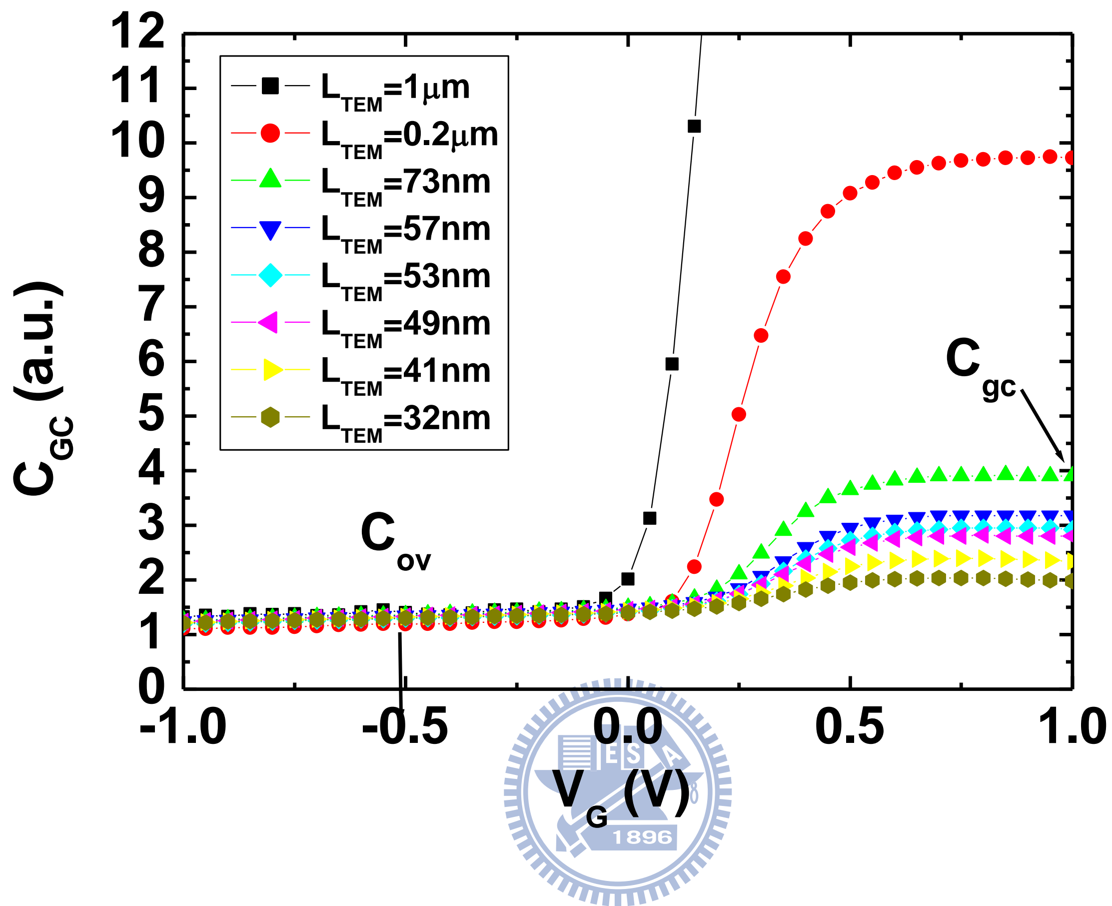

Figure 2.3. The measured CV curves in NMOS with various L_{TEM}. C_{gc} & C_{ov} are extracted at V_G equal to 1.0V and -0.5V respectively.

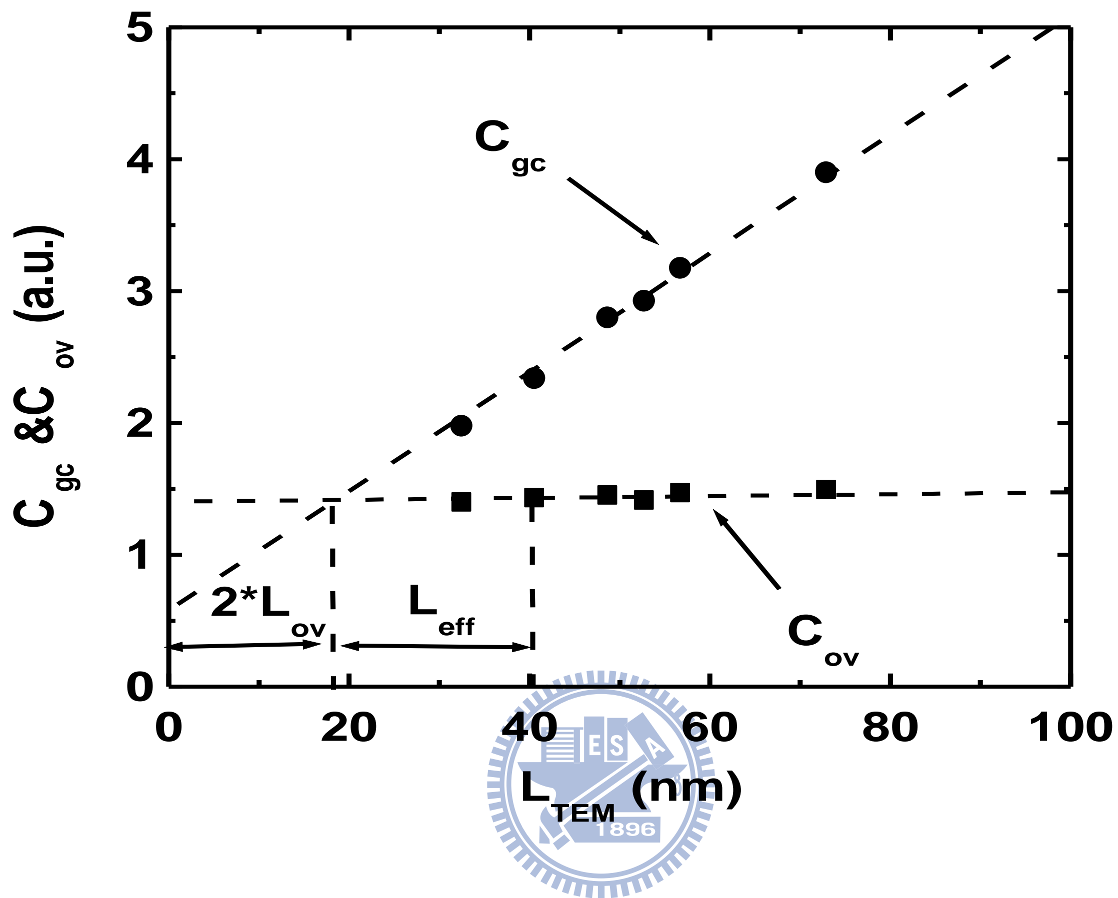

Figure 2.4. Plot of C_{gc} & C_{ov} versus various L_{TEM}. L_{ov} and L_{eff} can be obtained from the intercept points from C_{gc} & C_{ov}.

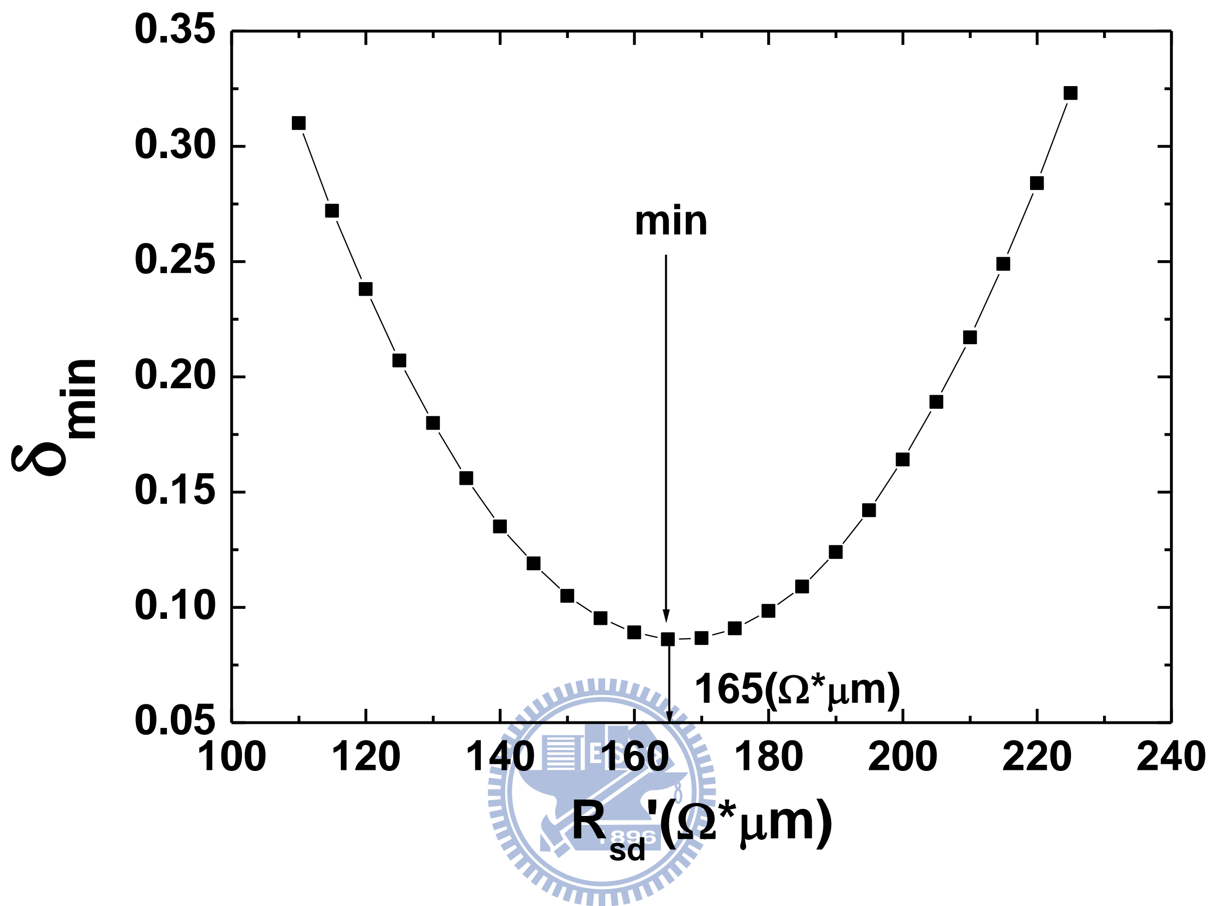

Figure 2.5. The objective function, δ_{min}, versus R_{sd}'. Optimized R_{sd} (165 Ω*μm) can be obtained from the minimum of δ_{min}.

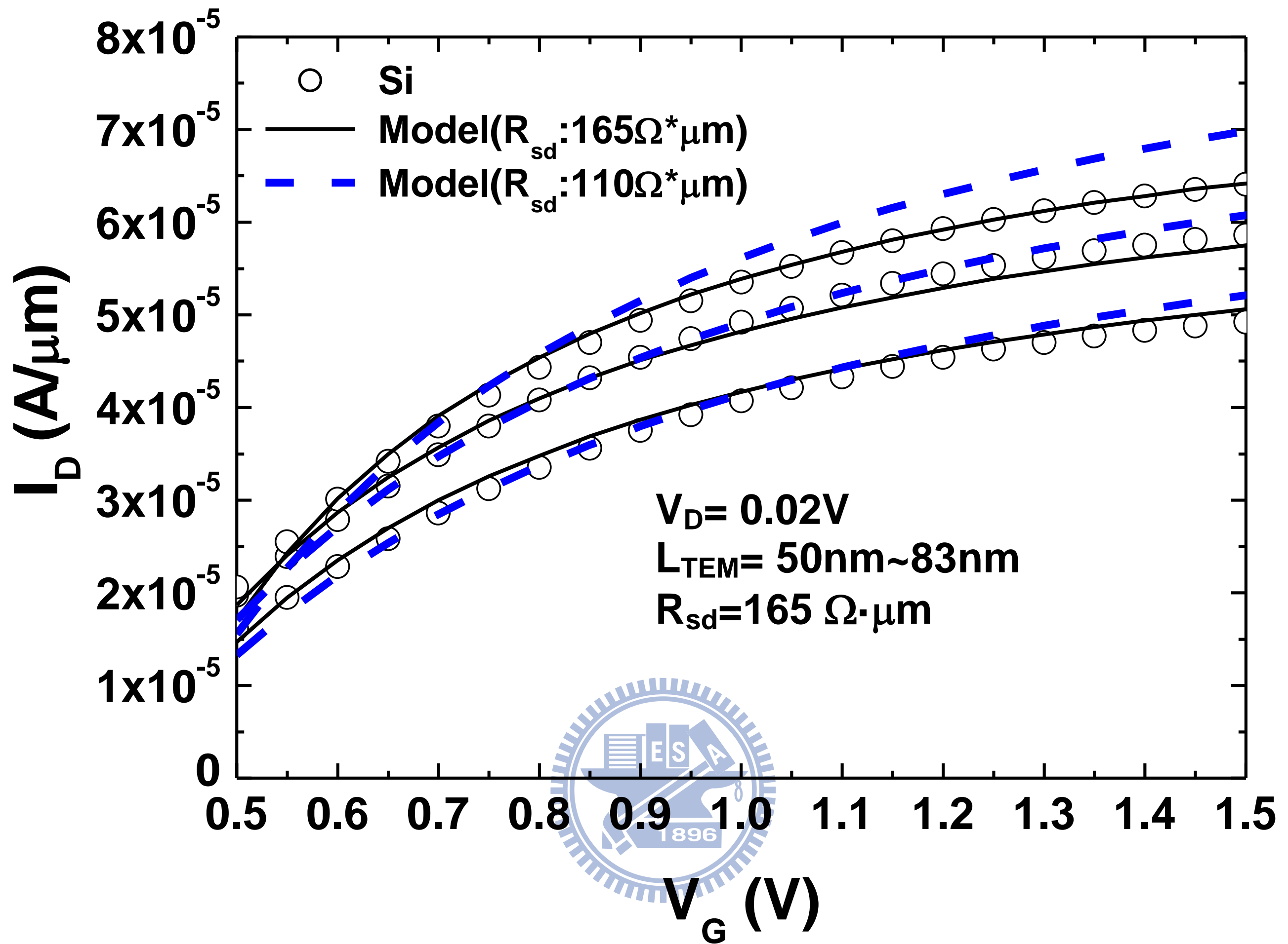

Figure 2.6. I_d-V_g modeling results using various R_{sd} values. The three groups of curves correspond to different gate length ranging from 50nm to 83nm. If the R_{sd} value in the model is not accurate (e.g., R_{sd} = 110 Ω*μm), the drain current ratio of devices with different L_{TEM} will not be correct.

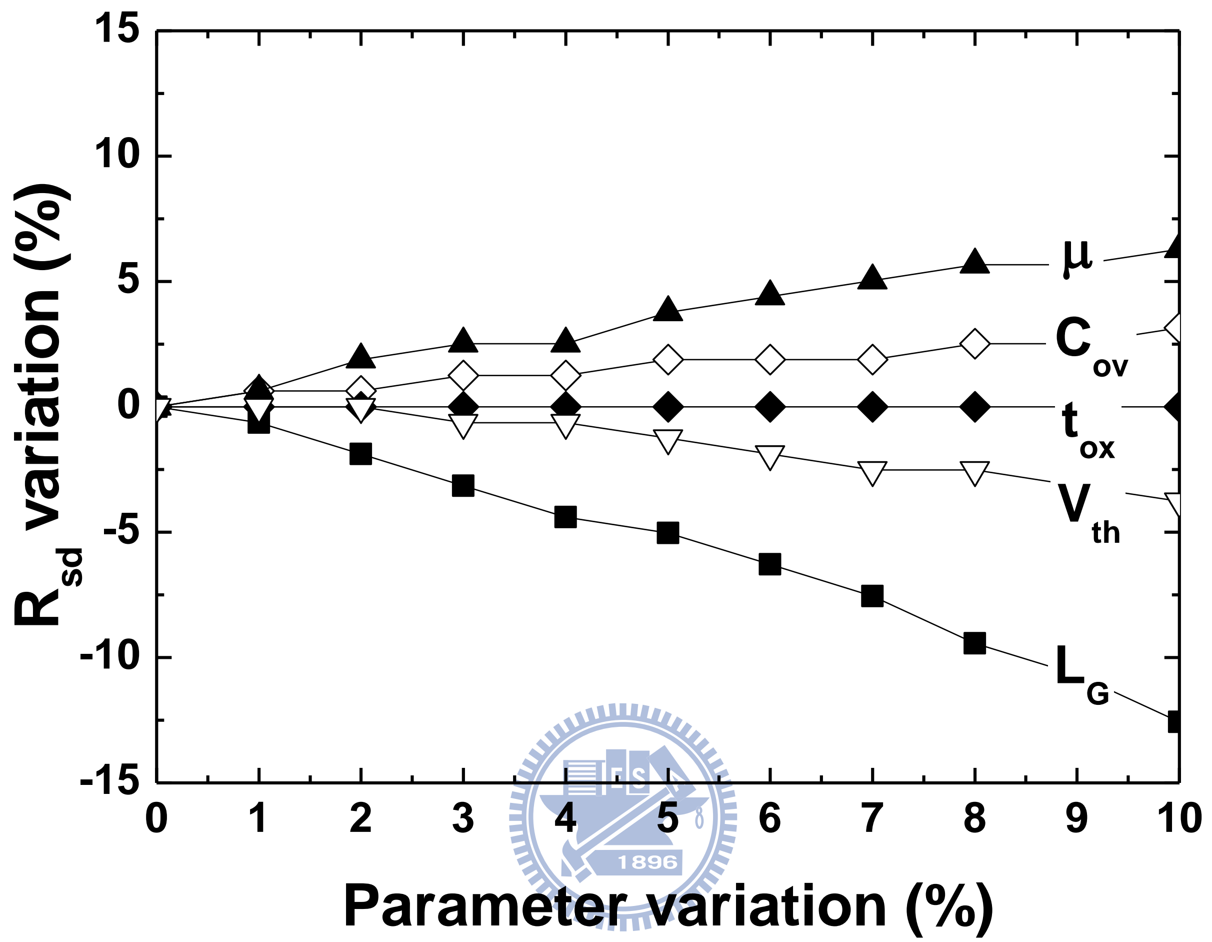

Figure 2.7. R_{sd} sensitivity plot with different key parameters.

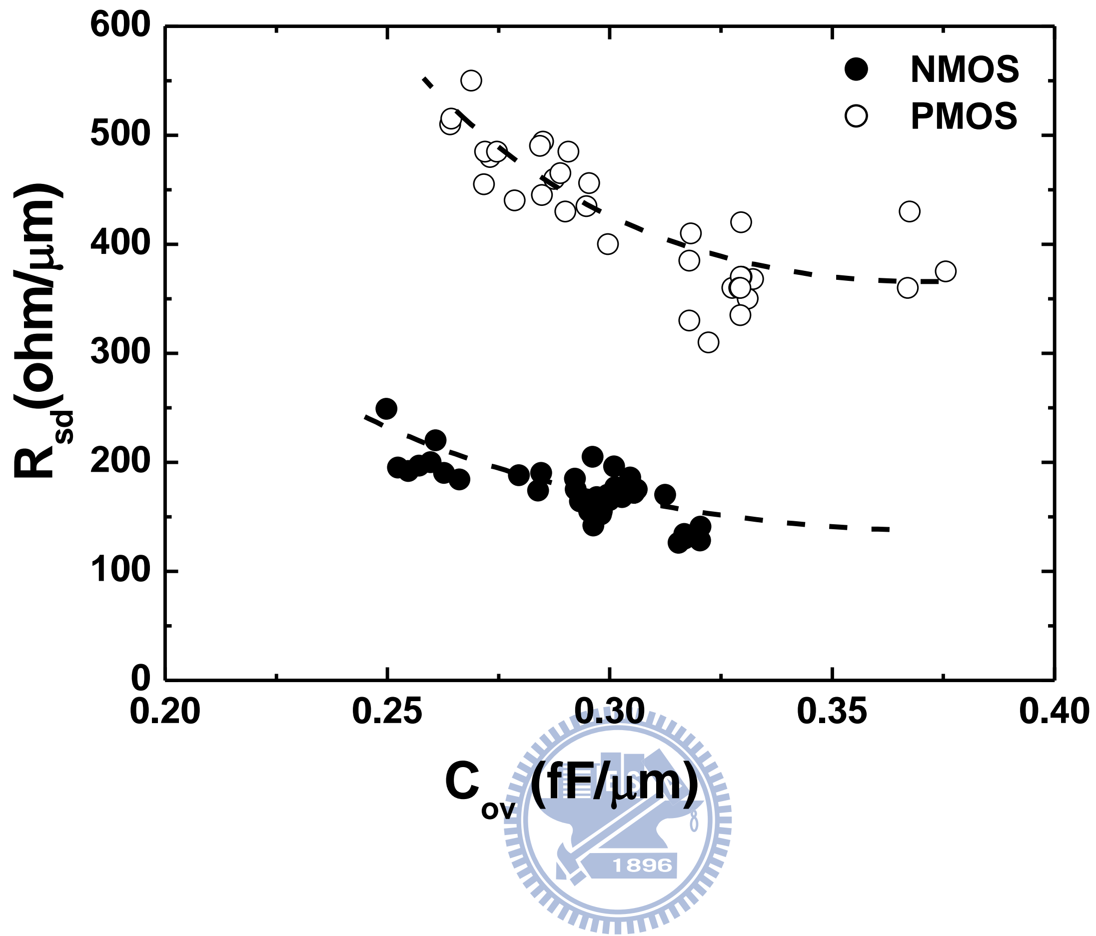

Figure 2.8. Relationship between R_{sd} and overlap capacitance (C_{ov}).

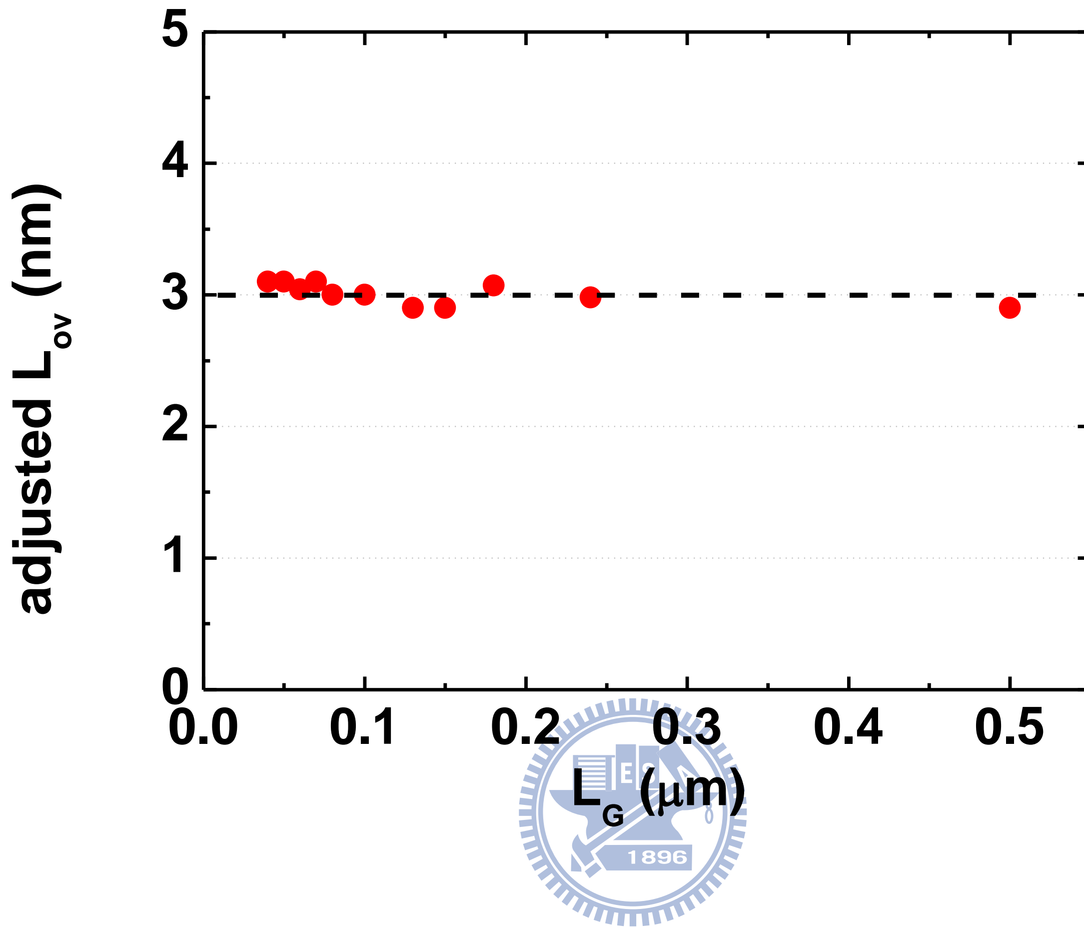

Figure 2.9. L_{ov} (Extension overlap distance under poly) versus L_G from Tsuprem4 structure simulation. The L_{ov} is subtracted by a positive value for adjusted purpose.

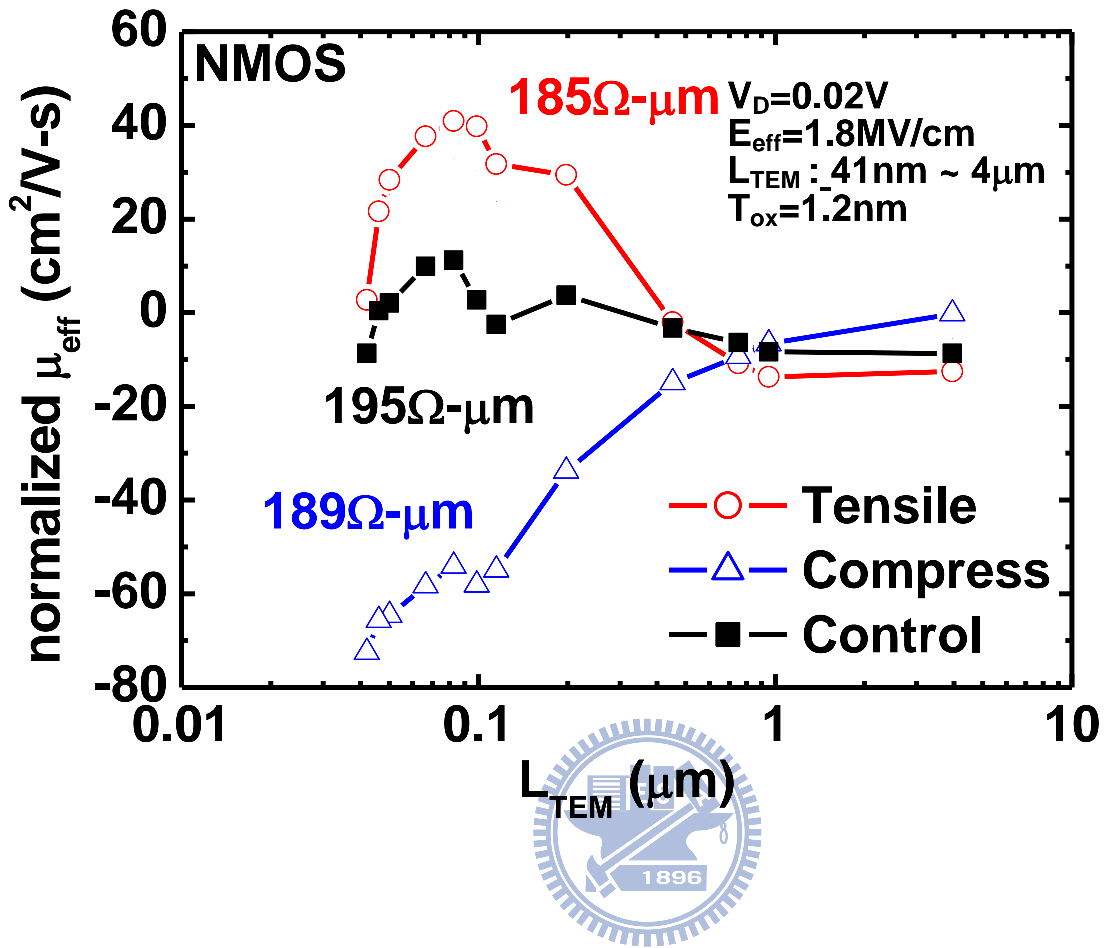

Figure 2.10. $\mu_{eff}(L_{TEM})$ for NMOS devices with halo implants and various stressors (Tensile/0 stress/Compressive). The mobility is subtracted by a positive constant for normalization purpose.

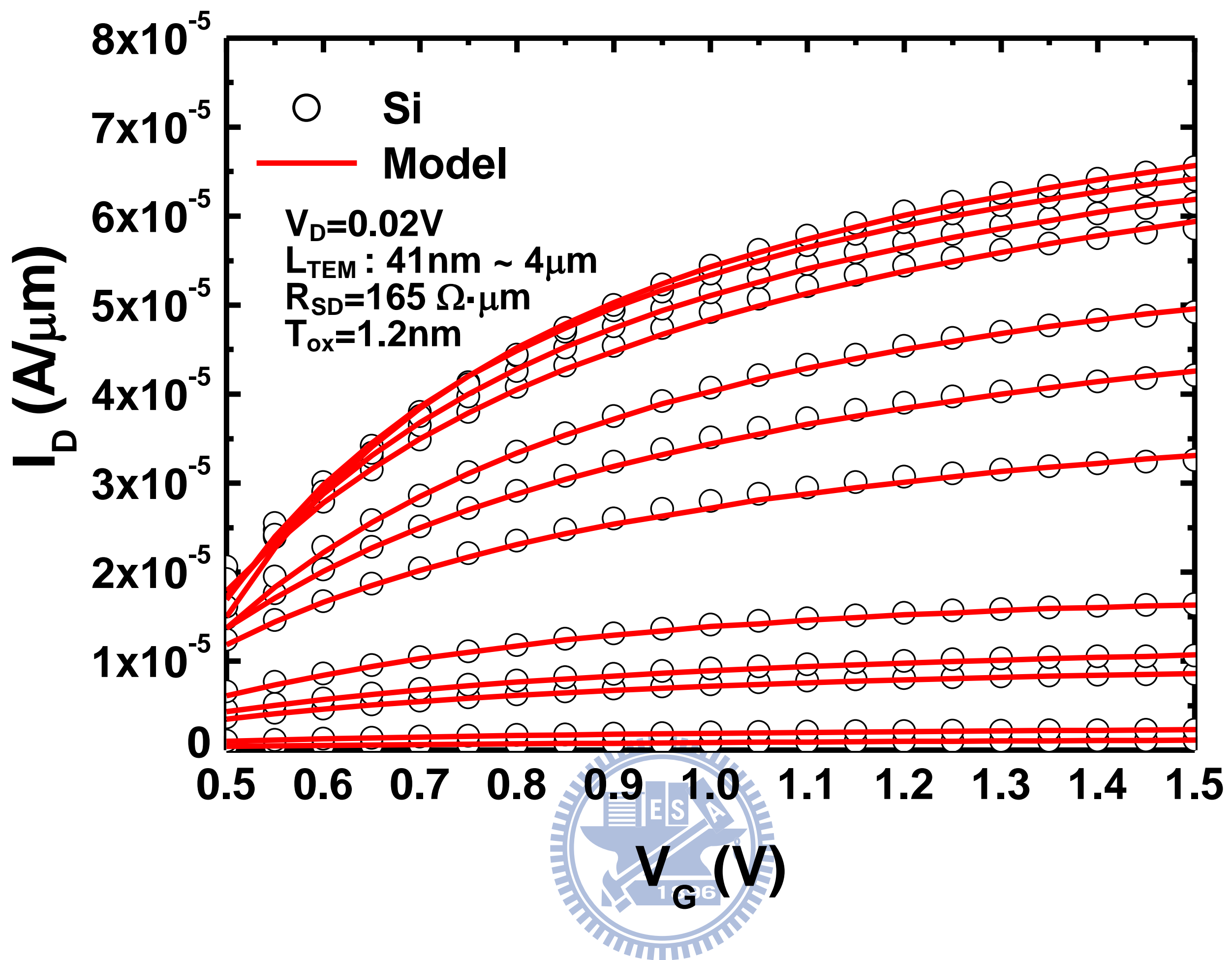

Figure 2.11. I_d-V_g modeling results for a wide range of L_{TEM} using the extracted μ_{eff} (L_{TEM}).

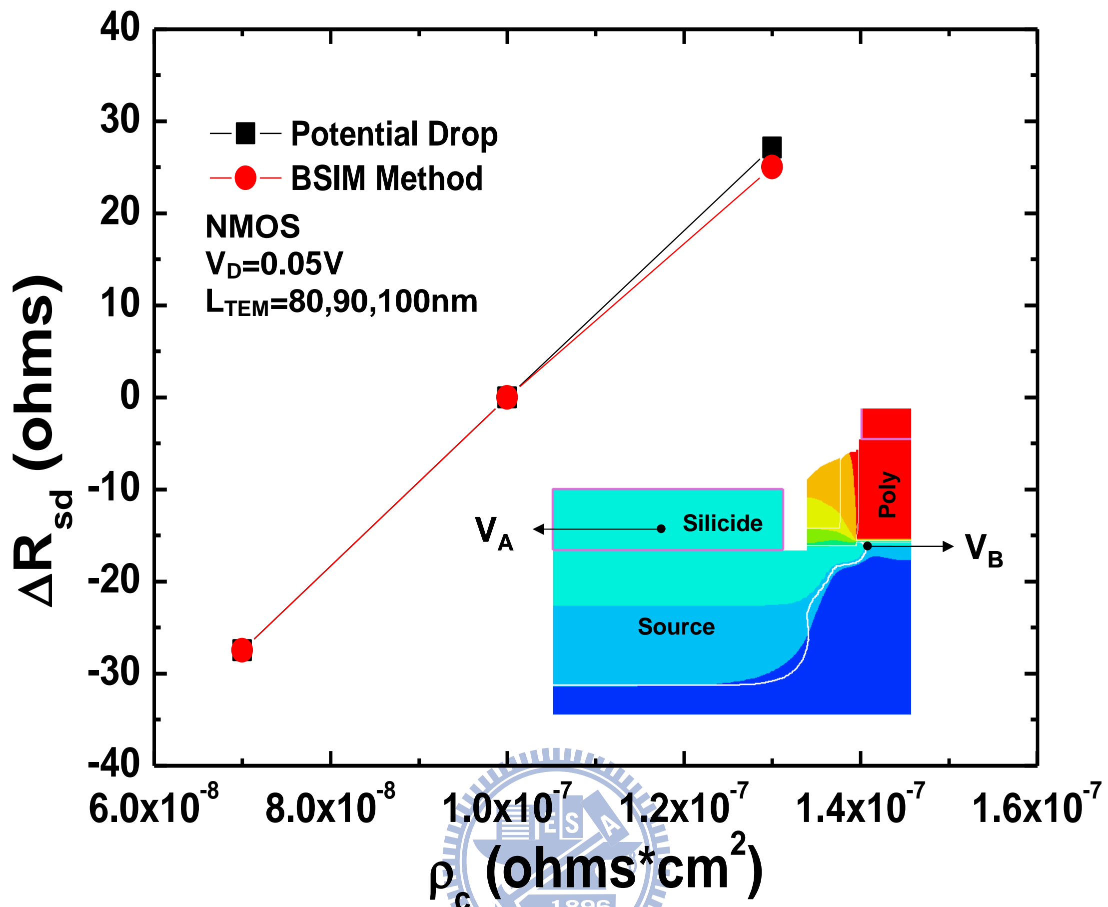

Figure 2.12. A comparison plot of ΔR_{sd} versus ρ_c (specific resistivity) with two R_{sd} extraction methods - BSIM fitting method and Medici potential contour method. ΔR_{sd} equals to R_{sd} (ρ_c)- R_{sd} (ρ_c=1x10$^{-7}\Omega$*cm^2). (Inset: potential contour of simulation MOSFET profile, R_{sd} is extracted by Ohm's law: (V_A-V_B)/I_d).

Chapter 3

Investigation of Coulomb Mobility in Nanoscale Strained MOSFETs

3.1 Introduction

Uniaxial strained-Si technology is critical to transistor performance in nanoscale CMOS development [1-2]. The improvement of current drive shows strong correlation with the low-field mobility enhancement by uniaxial strain [3]. However, in order to suppress the short channel effect for device scaling, halo implantation is widely used. With shrinking gate length, halo profiles begin to merge and result in higher effective bulk concentration. Recently, several studies [4-9] reported degraded carrier mobility for short channel devices and pointed out the increasing importance of Coulomb scatterings. Whether or not the Coulomb scattering mobility can be enhanced by process-induced strain is crucial to device design and merits investigation.

Although Gamiz et al. [6] and Nayfeh et al. [5] have shown that Coulomb mobility is not enhanced in strained-Si nMOSFETs, Weber and Takagi [4] have demonstrated that the mobility limited by substrate impurity scattering is still enhanced in long-channel strained devices (L=10μm). These findings seem to be inconsistent, and further examination on Coulomb mobility is needed. Furthermore, similar studies have not been performed in PMOSFET, especially for short channel devices. Therefore, further examination on Coulomb mobility is needed for PMOSFET.

In this work, we tackle the problem using advanced short-channel strained devices [10-13]. By accurate mobility extraction under various temperatures, we assess the impact of process-induced uniaxial strain on Coulomb mobility in short-channel

nMOSFETs and pMOSFETs. The Coulomb mobility in the short channel region under compressive and neutral uniaxial local stress conditions is carefully characterized by split C-V (Capacitance-Voltage) method and Matthiessen's rule. In order to further verify our experimental results, we have also utilized the four-point mechanical bending technique on both short and long channel devices in PMOSFETs.

3.2 Devices and Experimental

For comparison purpose, N-channel and P-channel MOSFETs with channel direction <110> with neutral and compressive uniaxial Contact Etch Stop Layer (CESL) were manufactured based on state-of-the-art CMOS technology on 300mm (100) silicon substrate, as shown in Fig. 3.1. The compressive film may transfer significant compressive stress to the channel region, modulating silicon subbands and carrier populations, and altering carrier mobility [14]. In Fig. 3.2 (a) and (b), the device on-off performance is boosted –36% and +35% by compressive uniaxial stressors in the short channel region for NMOSFETs & PMOSFETs, respectively.

The devices with neutral and compressive CESL films were implanted by the same pocket conditions. Shallow Trench Isolation (STI) was patterned to define the active region. Then an ultra thin oxide was grown on the surface of wafer. The poly gate was implanted with heavily doped N/P type species after poly deposition and post annealed to increase gate activation rates. Then ultra shallow HDD (Highly Doped Drain) implant, spacer formation, source and drain implant, post implantation annealing, and back-end process were implemented sequentially.

The devices with effective channel length (L_{EFF}) ranging from 975 nm to 90 nm were examined for NMOSFETs and 950nm to 45nm for PMOSFETs with gate width equal to 1μm. Special transistor arrays were designed to provide sufficient area for split C-V measurement. In addition, it is known that parasitic capacitance components play

an important role in short channel devices and affect the accuracy of the extraction result. Therefore, calibration test keys were also designed to exclude the parasitic effects.

In order to reproduce the stress environment by local compressive stressors, a four-point mechanical bending tool was used to apply external stress on both long and short channel devices in PMOSFETs. The compressive stress level is around -230MPa based on the meter reading.

3.3 Mobility Extraction

In order to extract the short channel mobility, 3 types of special transistor testkeys were designed. The first type of testkey is MOSFET array. The purpose of MOSFET array is for Capacitance-Voltage (C-V) characterizations. Because the gate capacitance of short channel single MOSFET cannot meet the measurement resolutions of HP4284, the array type of MOSFET are necessary to provide sufficient gate area for CV characterizations. The second type of testkey is calibration array. The purpose of calibration array is for the calibrations of inter-metal parasitic capacitance. This testkeys has exactly the same layout with the MOSFET arrays but the Active Region Layer (OD layer) is excluded. The third type of testkey is a single MOSFET designed for Current-Voltage (I-V) characterizations. Please note 3 types of testkeys are designed for each dimension.

In chapter 2, we have mentioned that the μ_{eff} extracted by the BSIM method is based on the charge density (Q_{inv}) approximated by $C_{ox}\times(V_g-V_{th})$. However, some channel charges still exist in the sub-threshold region. The better approach to obtain the Q_{inv} result is a direct measurement of Q_{inv} (by split-CV method) from capacitance measurement, with the mobile channel charge density determined from the gate-to-channel capacitance (C_{gc}), as shown in Eq. (1):

$$Q_{inv} = \int_{V_{fb}}^{V_{gs}} (C_{gc} - C_{ov}) dV_{gs} \tag{1}$$

Moreover, in order to calculate the vertical effective field, the inversion charge density (Q_{inv}) and bulk charge density (Q_b) are also crucial for each dimension. Therefore, this work used split C-V measurement [15-17] to characterize the Q_{inv} and Q_b, respectively, for long and short channel devices.

First, the extracted capacitance from MOSFET arrays needs to be calibrated by the MOSFET calibration arrays. In Fig. 3.3, it shows the contribution of inter-metal parasitic capacitance on Gate-to-Channel capacitance (C_{gc}) is significant. Then the characterized Gate-to-Channel capacitance with floating bulk terminal (C_{gc}) is calibrated by considering the parasitic components such as overlap capacitance (C_{ov}) and fringing capacitance (C_{of}) [15,18,19], as shown in Fig. 3.4. Fig. 3.5 (a) & (b) show the C_{gc} characteristic by C_{ov} and C_{of} calibrations. In Fig. 3.5(a), it shows C_{ov} and C_{of} are independent of gate length and considered as parasitic capacitance. Moreover, it is worth noting that the inner fringing capacitance (C_{inov}) in Fig. 3.5(b) shows significant dependency on V_G, which is consistent with [18]. The Gate-to-Channel capacitance with source/drain/bulk tied together (C_{gg}) is also calibrated using the same calibration procedure with C_{gc}. After C_{gc} and C_{gg} were obtained, the Q_{inv} and Q_b can be obtained by integrating the whole C_{gc} and (C_{gg}-C_{gc}) from flat-band voltage by Eq. (1) and Eq. (2), as shown in Fig. 3.6.

$$Q_b = \int_{V_{fb}}^{V_{gs}} (C_{gg} - C_{gc}) dV_{gs} \tag{2}$$

Fig. 3.7 shows the extracted Q_{inv} and Q_b and Q_{total}(=Q_{inv}+ Q_b) versus gate bias. It shows

that Q_{inv} becomes dominate in Q_{total} when $V_G>V_{th}$ and strong dependency on V_G. Furthermore, the Q_b becomes constant above the threshold voltage because the depletion width is saturated in strong inversion region.

By using split-CV method, the effective vertical electric field (E_{EFF}) can be calculated by Eq. (3):

$$E_{eff} = \frac{Q_b + \eta \cdot Q_{inv}}{\varepsilon_{si}} \tag{3}$$

Where η are 1/2 and 1/3 for NFET and PFET, respectively [19], ε_{Si} is the permittivity of Si.

The effective bulk doping concentration (N_a) from long to short channel is extracted by the NCSU fitting program [20]. In order to exclude the parasitic source/drain series resistance (R_{sd}) effect, the BSIM R_{sd} extraction method in Chapter 2 is adopted [21,22]. After R_{sd} is obtained, ideal drain current can be derived from Eq. (4):

$$I_d(int) = \frac{I_d(ext)}{1 - I_d(ext) \times \frac{R_{sd}}{V_d}} \tag{4}$$

where $I_d(int)$ represents the intrinsic drain current, $I_d(ext)$ represents the extrinsic drain current which includes the R_{sd} effect, and R_{sd} is the parasitic source/drain series resistance.

Fig. 3.8 shows the drain current versus gate voltage with R_{sd} calibrations. It shows that the Rsd is crucial to extract intrinsic drain current, especially for short channel devices because R_{sd} becomes more important in this regime. Fig. 3.9 shows the drain current enhancement vs L_g by considering R_{sd} calibrations. It shows that the drain current enhancement may be underestimated if R_{sd} effect is not calibrated in short

channel devices.

The physical poly gate length (L_{phy}) can be obtained from the in-line SEM (Scanning Electron Microscopy) measurement (with accuracy within ± 2nm) at poly patterned stage and the etching-induced length bias(ΔL), as shown in Eq. (5):

$$L_{phy} = L_{SEM} - \Delta L \tag{5}$$

The overlap distance between poly and LDD region (L_{ov}) is extracted by split CV method [15,16], as shown in Fig. 3.10. Then the effective channel length (L_{EFF}) can be derived by subtracting L_{ov} from L_{phy}. Finally, the total mobility can be extracted by Eq. (6):

$$\mu = \frac{I_d(int) \cdot L_{EFF}}{W \cdot Q_{inv} \cdot V_d} \tag{6}$$

W represents the device width. Eq. (6) represents the total mobility and Coulomb mobility is extracted from it by using Matthiessens's rule. It is worth noting that the total mobility is inversely proportional to Q_{inv} at high vertical field region where the surface roughness scattering mechanism dominates.

Fig. 3.11 shows the extracted mobility by considering asymmetry spatial distribution of Q_{inv} due to V_D bias [23]. Because V_D is 5mV only, the impact on mobility caused by the asymmetry spatial distribution at low Q_{inv} region is negligible.

3.4 Stress Simulation

In order to explain how CESL stressor transfer stress to the channel region, two dimensional stress profiles induced by strained CESL were determined by TCAD stress simulation. In order to accurately reconstruct the device scheme, all major front-end processes from the shallow trench isolation to the rapid thermal annealing were included. The thermal budget and temperature profiles during processing have been well calibrated. The corresponding simulation geometries were also calibrated from TEM

cross-section images. The layout effects (e.g. Poly Spacing Effect) have been considered in this simulation. In order to investigate the stress dependence on device geometry, MOSFET schemes at different gate lengths have been constructed.

The compressive CESL induces stronger compressive stress along the silicon channel direction as gate length becomes shorter. This is mainly attributed to the corner and the direct CESL effect [24]. The corner effect is due to the interaction of the lateral-CESL and the bottom-CESL, resulting in compressive stress along the channel direction. The direct CESL effect is dominated by the bottom-CESL effect. Both corner and direct CESL effect have higher stress efficiency on shorter channel devices. Note that the stress level represents the average stress over the volume of the silicon channel (depth = 10A and length = gate length).

For PMOSFETs, Fig. 3.12 (a) and (b) show the simulated stress contours with intrinsic and compressive CESL films respectively. The gate length for both devices is 54nm. The average stress levels along the channel direction (Sxx) are -0.153GPa and -0.662GPa for neutral and compressive CESL nitride films, respectively. The Sxx of neutral CESL is mainly contributed by the STI effect instead of the CESL effect. For compressive CESL, the corner effect and the direct CESL effect are responsible for Sxx in the short channel device [24].

Fig. 3.13 (a) and (b) show the stress level (Sxx and Syy, as shown in the inset of Fig. 3.13(a)) between long and short channel devices. In Fig. 3.13 (a), the compressive CESL induces stronger compressive stress (Sxx) in the Si channel as gate length becomes shorter. It is mainly attributed to the corner and the direct CESL effect [24]. The corner effect is due to the interaction of the lateral-CESL and the bottom-CESL, resulting in compressive stress along the channel direction. The direct CESL effect is dominated by the bottom-CESL effect. In Fig. 3.13 (b), the compressive CESL induces

stronger tensile stress (Syy) vertical to the Si surface as gate length becomes shorter. It is mainly due to the indirect CESL effect [24]. For long channel devices, the indirect effect arises from the top-CESL; for short channel devices, 49% of the total stress amount comes from the lateral-CESL, 29% from the top-CESL and 21% from the bottom-CESL [24].

For NMOSFETs, based on TCAD stress simulation, the average stress levels for L_G=90nm along the channel direction are -0.165GPa and -0.599Gpa ("-" means compressive stress) for neutral and compressive CESL nitride films, respectively. The average stress levels vertical to the silicon surface are -0.079GPa and 4.120GPa for neutral and compressive CESL nitride films, respectively. The average stress levels along the width direction are -0.684GPa and -0.522GPa for neutral and compressive CESL nitride films, respectively. The ways to control the stress level of CESL films are to modify film compositions or thickness by different deposition parameters. In general, stronger compressive CESL film or thicker compressive CESL film means stronger compressive stress applied along the silicon channel.

S. Thompson et al. [14] have shown that the mobility of PMOSFET with <110> channel direction on (001) wafer prefers compressive Sxx (Longitudinal) and tensile Syy (Out-of-Plane) based on piezoresistance, and vice versa for NMOSFETs. The simulation results of Fig. 3.12 and Fig. 3.13 can explain how the compressive CESL affects on hole and electron mobility.

3.5 Results and Discussion

3.5.1 NMOSFETs

Fig. 3.14 shows the extracted mobility of long and short channel devices versus the vertical electrical field (E_{EFF}). It can be seen that the short channel mobility significantly depends on the stress level. Fig. 3.15 shows the temperature dependence of the mobility

at E_{EFF}=1.2MV/cm. As gate length decreases, the temperature sensitivity of the mobility changes. It has been known that the importance of Coulomb mobility also increases as gate length decreases [4-9].

To extract the Coulomb mobility, we use the Matthiessen's rule and assume that the universal mobility curve (UMC) follows the measurement data in the high-field region [5]. In order to verify the accuracy of the extracted Coulomb mobility, we have compared the extracted Coulomb mobility under various UMC (±10%) as shown in Fig. 3.16. It can be seen that the extracted Coulomb mobility curves remain almost the same when Q_{inv} is smaller than 5×10^{12} cm^{-2}, at which V_G is about 1.1 V.

Fig. 3.17 shows the Coulomb mobility for the short-channel devices with different stressors under various temperatures. It can be seen that in the low vertical field region, the Coulomb mobility decreases with temperature. This is because slower electrons are more susceptible to Coulomb scattering [25]. Moreover, the Coulomb mobility shows significant stress dependency. In other words, the strain engineering can still be employed to modulate the Coulomb scattering mobility of short-channel nMOSFETs. It is worth noting that our result is inconsistent with the results in [5] and [6].

Fig. 3.18 shows the stress sensitivity of the short-channel Coulomb mobility at various temperatures. It can be seen that in the low vertical field region, the stress sensitivity decreases as temperature increases. It is plausible that two competing mechanisms, bulk impurity scattering and interface scattering, are responsible for our observation. As pointed out in [4], the mobility limited by bulk impurity scattering (μ_b) shows opposite stress sensitivity to the mobility limited by interface scattering (μ_{it}). Although the bulk impurity scattering of the short-channel nFET increases under the compressive stress, the interface scattering becomes less because there are more electrons in the 4-fold valley. These two mechanisms counteract each other and

determine the overall stress dependency of Coulomb mobility. As temperature increases, the importance of interface scattering increases [25]. As a result, the stress dependency of the overall Coulomb mobility decreases.

Fig. 3.19 shows the fitting result of $\mu_{Coulomb}$ data [23] with first principle 2-D model. Eq. (7) represents the Coulomb mobility model that includes screened and unscreened effect [26]:

$$\mu_{screened} = \frac{\pi\mu_{unscreened}}{F(\alpha)} \cdot \frac{Z_{sub}}{Z_{inv}}, \mu_{unscreened} = \frac{640\pi^3 h\varepsilon_{si}^2\varepsilon_0^2 k_b T_L}{G(P)m^* e^3 N_a Z_{sub}} \quad (7)$$

Where F(a) and G(P) represent the screening function and the correction factor for repulsive Coulombic potential respectively. Fig. 3.20 shows the enhancement of screened and unscreened $\mu_{Coulomb}$ when m* is reduced 20% by applying tensile stress along <110> channel direction on NFETs. The screened $\Delta\mu_{Coulomb}$ is +13% higher than the unscreened $\Delta\mu_{Coulomb}$. This means the bulk screening effect also has strain dependency. It is plausible that the strained device has thinner inversion thickness due to subband splitting effect [4] and better bulk screening effect caused by higher Q_{inv}, as explained in the inset of Fig. 3.21. Fig. 3.21 shows that +13% $\mu_{Coulomb}$ is enhanced by +10% Q_{inv} due to higher V_G bias and better screening effect. Our Si data also shows that Q_{inv} is increased +7% at the same V_G bias when 14% m is enhanced by tensile stress. The finding supports our hypothesis of the stress dependence of the bulk screening effect.

Table 3.1 shows the summary table of stress dependence of Coulomb mobility limited by different mechanisms and scattering sources with compressive stress applied along <110> channel direction: (a) N_a scattering limited $\mu_{Coulomb}$ shows degradation due to heavier effective mass (m*) [4] (b) N_{it} scattering limited $\mu_{Coulomb}$ shows enhancement

due to thicker inversion layer thickness (Z_{inv}) [4] (c) N_a screening limited $\mu_{Coulomb}$ shows degradation due to lower electron density (This work) (d) N_{it} screening limited $\mu_{Coulomb}$ shows no stress sensitivity on $\mu_{Coulomb}$ due to the Quantization effect caused by high Na [6].

3.5.2 PMOSFETs

Fig. 3.22 shows the characterized mobility with neutral stressors at room temperature where L_{EFF} equals to 950nm, 190nm, 45nm, respectively. It can be seen that the high vertical field mobility is degraded as L_{EFF} shrinks. The abnormal behavior can be explained by halo pile-up, interface states, oxide charges, neutral defects, and remote Coulomb scattering [4-9].

Fig. 3.23 shows the temperature dependence of the total mobility when the effective vertical field is equal to 0.8MV/cm. When temperature is decreased, the thermal velocity of carriers becomes reduced. Therefore, the interaction time between moving carriers and ionized impurity charges becomes longer. This means higher Coulomb scattering probability and lower Coulomb mobility. As gate length shrinks, the temperature sensitivity of the mobility increases, indicating that the Coulomb mobility plays a critical role in the short channel region.

In order to extract the Coulomb mobility, we assume that the universal mobility curve follows the measurement data in the high-field region [5] from long to short channel lengths. Matthiessen's rule can then be used to extract the Coulomb mobility [5]. The extracted PMOS Coulomb mobility versus Q_{inv} is shown in Fig. 3.24. It can be seen that the Coulomb mobility decreases with channel length. The length dependence of Coulomb mobility comes from the non-uniform halo profiles. As channel length becomes shorter, the effective bulk charges increases and the Coulomb mobility decreases because of halo merge effect. To verify our mobility data, we fit it using the

equation $\mu_{coulomb} = AQ_{inv}^{\alpha}N_{a}^{-\beta}$ [5], where A is a constant, α and β are both equal to 1, and N_a is extracted from NCSU fitting programs. The result shows a fairly good fit between the data and the Coulomb mobility model.

Fig. 3.25 (a) shows that the long channel total mobility with L_{EFF}=950nm agrees with the model equation. Since the uniaxial stressor is only effective for short channel devices, the long channel mobility is almost the same between neutral and compressive stressors. Weber and Takagi used SiGe strained material under the silicon substrate and the stress is effective from both long to short channel devices because of global stress effect [4]. Fig. 3.25 (b) shows that for the short channel device with L_{EFF} =45nm, our extracted total mobility agrees with the model. The 71% mobility enhancement for the compressive stressor in the high vertical field region is mainly due to the uniaxial stress effect [14].

Fig. 3.26 shows the total mobility versus Q_{inv}. It is observed that the PMOS mobility in the high vertical field region shows strong stress dependence. However, very little stress dependence is observed in the low vertical field region. The inset of Fig. 3.26 shows the extracted Coulomb mobility for neutral and compressive stressors using Matthiessen's rule. It indicates that the Coulomb mobility has almost no stress dependence at room temperature.

To further verify our observation, we have also utilized the four-point wafer bending measurement. The advantage of this method is that it can provide the same global stress level to devices with various dimensions. Based on the extracted mobility data under varying mechanical stress, we can determine whether the Coulomb mobility shows stress dependency and verify the result obtained from the local stressors. The inset of Fig. 3.27 shows the schematic of the mechanical bending tool. In this case, 230MPa compressive stress is applied to the test device based on instrument reading.

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Fig. 3.27 shows the mobility versus effective vertical field for devices under global compressive bending stress. Unlike the behavior of local stressors, significant mobility improvement can be observed in long and short channel devices in the high vertical field region because of the global stress effect. It should be noted that R_{sd} has been well calibrated during mobility extraction.

Fig. 3.28 shows the total mobility enhancement percentage from long channel to short channel devices in the wafer bending experiment. In the high vertical field region, the mobility enhancement is around 15% and is independent of the channel length. It indicates that devices with various dimensions have similar stress level under the global stress and that phonon scattering mechanism still dominates in this higher vertical field region. However, the total mobility enhancement decreases with Q_{inv}. Moreover, the total mobility enhancement decreases with the channel length for a fixed Q_{inv}. It indicates that the Coulomb mobility has less stress dependence. In Fig. 3.29, the extracted Coulomb mobility indeed shows negligible stress dependency for either long channel or short channel devices, verifying our previous observation in Fig. 3.28. According Takagi's explanation [4], it is plausible that it is due to the competition result of the stress sensitivity between bulk charge scattering and interface charge scattering for our PMOSFET samples.

In order to support previous assumption for PFET, we extract the temperature dependency of strain impact on Coulomb mobility, as shown in Fig. 30. It shows that no strain sensitivity of Coulomb mobility at T=25C. However, the compressive uniaxial strain may further degrade Coulomb mobility as temperature increased. Similar with NFET, although the bulk impurity Coulomb scattering of the short-channel PFET decreases under the compressive stress, the interface Coulomb scattering rate becomes higher because there are more holes occupied in the lower subband. These two

mechanisms counteract each other and determine the overall stress dependency of Coulomb mobility. As temperature increases, the importance of interface scattering increases [25]. As a result, the Coulomb mobility degraded under uniaxial compressive strain.

3.6 Conclusion

By using the split-CV method and careful calibration of parasitic components on the short channel devices with local stressor, we have examined the impact of process-induced uniaxial strain on Coulomb mobility for short-channel nMOSFETs and pMOSFETs. For nMOSFETs, our study indicates that the Coulomb mobility has significant stress dependency. Moreover, the stress sensitivity of the Coulomb mobility shows strong temperature dependence. Since it is the interface scattering that counteracts the stress sensitivity of the bulk impurity limited mobility, further reducing the interface charges will be crucial to future mobility scaling.

For pMOSFETs, we have observed that the Coulomb mobility in PMOS shows almost no stress dependency at room temperature. This observation has also been verified by the four-point wafer bending measurement. However, the strain sensitivity of the Coulomb mobility shows strong temperature dependence, similar with NFET's result. It is due to the competition result of the stress sensitivity between bulk charge scattering and interface charge scattering for our PMOSFET samples. Therefore, in order to boost Coulomb mobility by strain technology, it is necessary to suppress the formations of interface charges (N_{it}).

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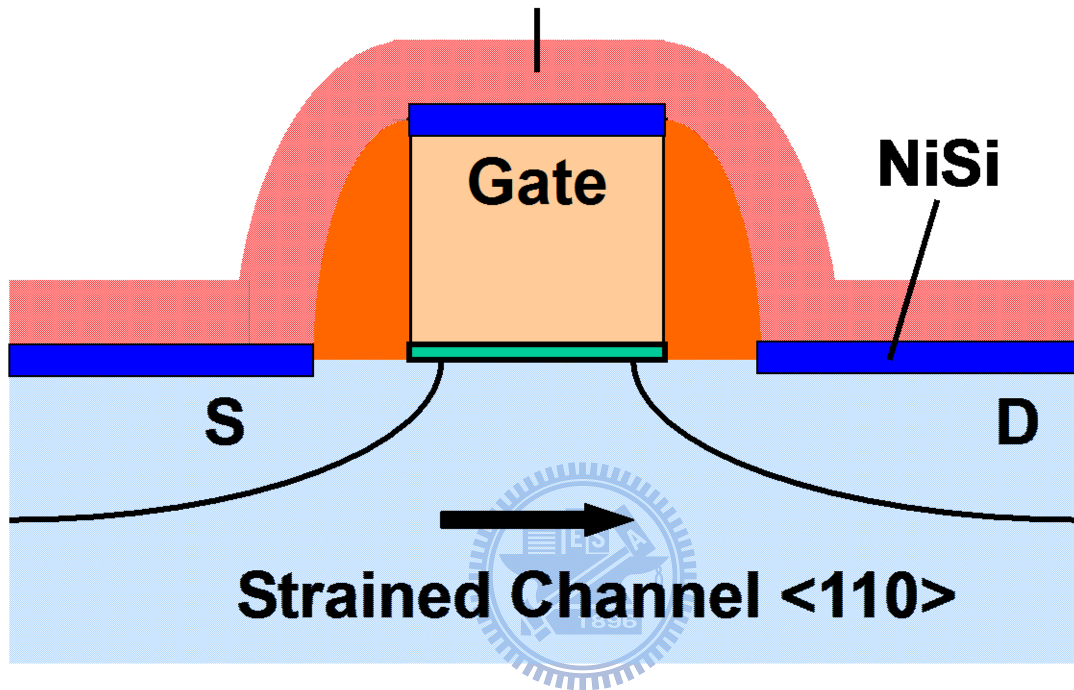
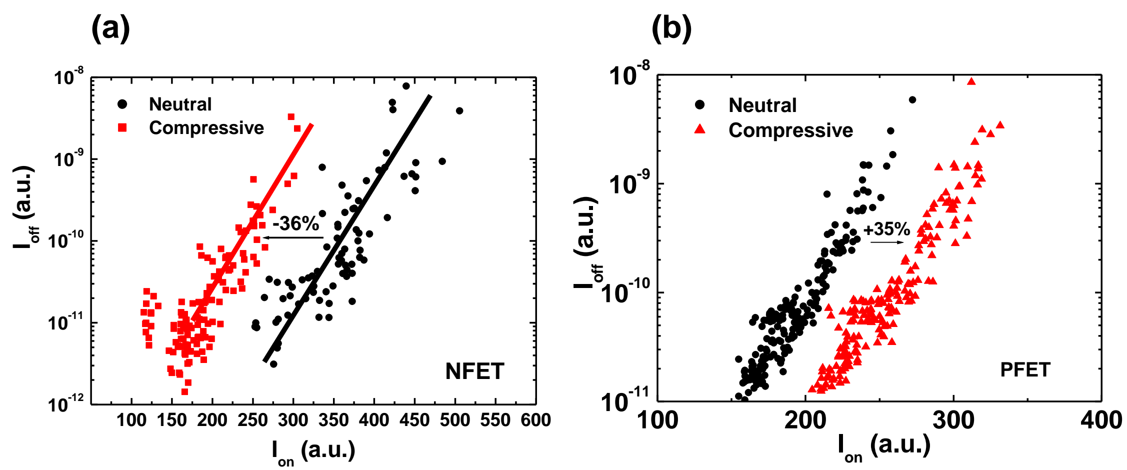


Figure 3.1. MOSFET schematic with neutral and compressive stressor.



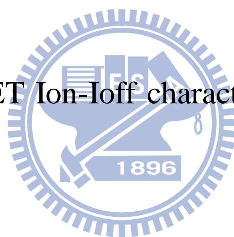
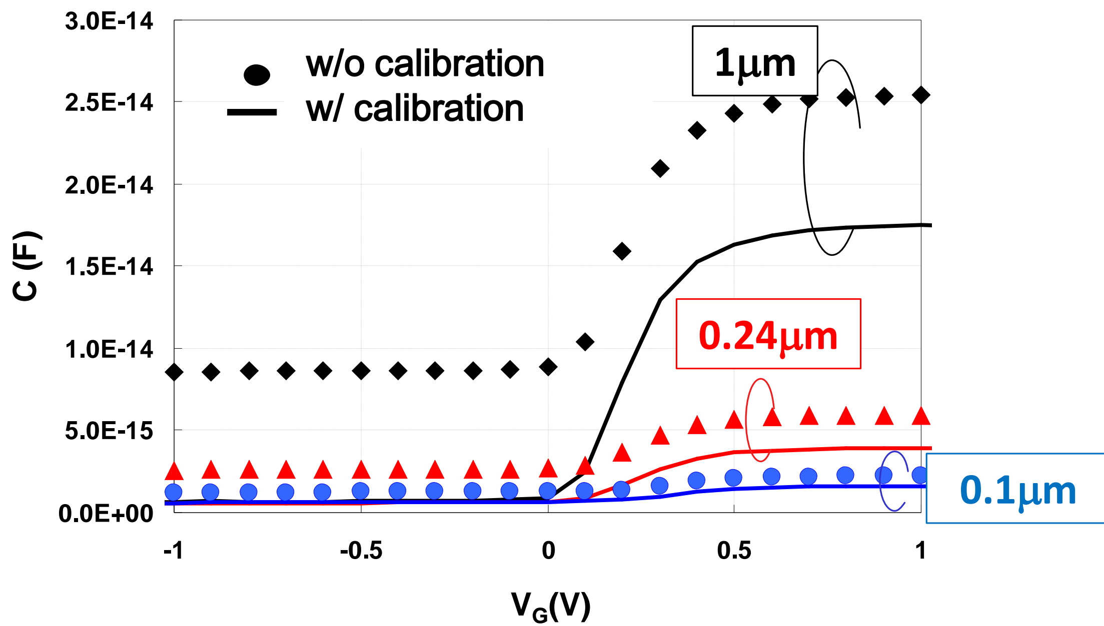


Figure. 3.2. (a) NFET (b) PFET Ion-Ioff characteristic with neutral and compressive stressor.



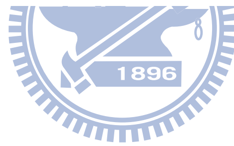
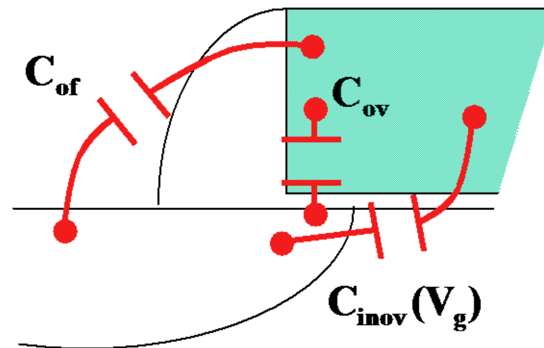


Figure 3.3. Capacitance calibrated with inter-metal parasitic capacitance.



$$C_{gc}(V_g, L) = C_{ov} + C_{inov}(V_g) + C_{of} + C_{gc0}(V_g, L)$$

Figure 3.4. Direct overlap capacitance (C_{ov}) and outer fringing capacitance (C_{of}) .

These parasitic capacitance needs to be calibrated for Q_{inv} extraction.

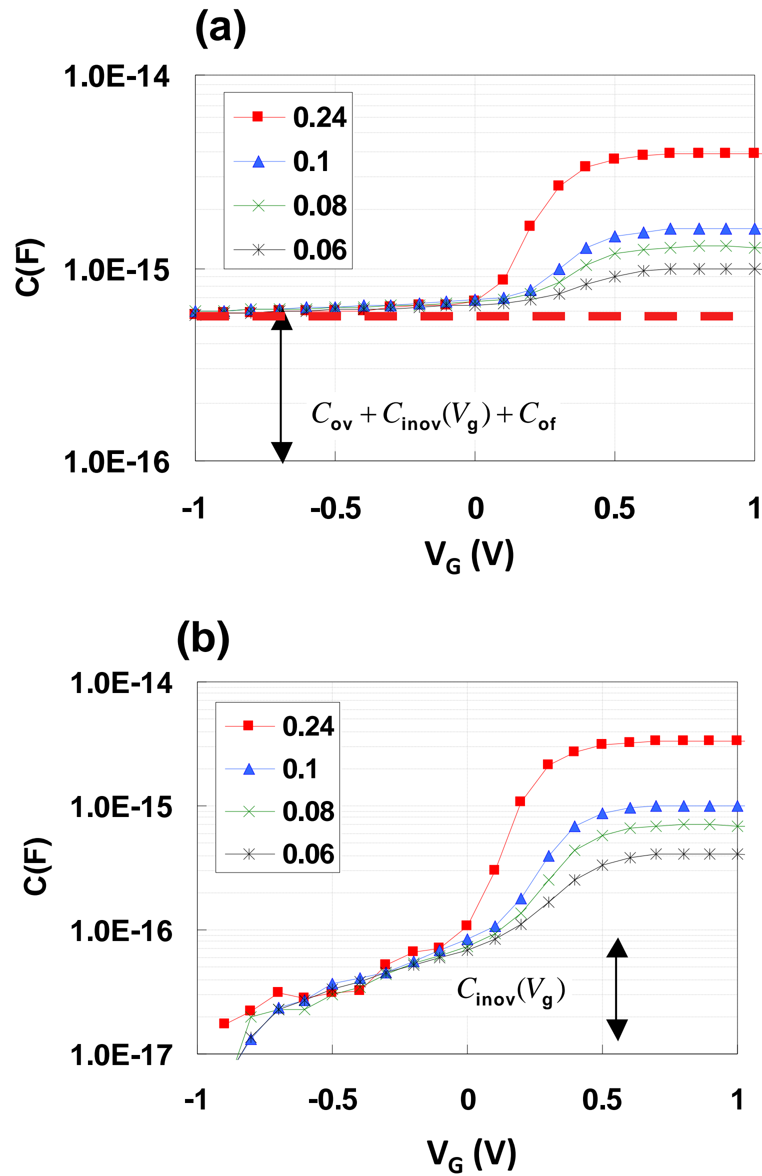


Figure 3.5. (a) Direct overlap capacitance (C_{ov}) and outer fringing capacitance (C_{of}). These parasitic capacitance needs to be calibrated for Q_{inv} extraction. (b) C_{gc} characteristic after C_{ov}/C_{of} calibrations. C_{inov} shows strong Vg dependence, consistent with [18].

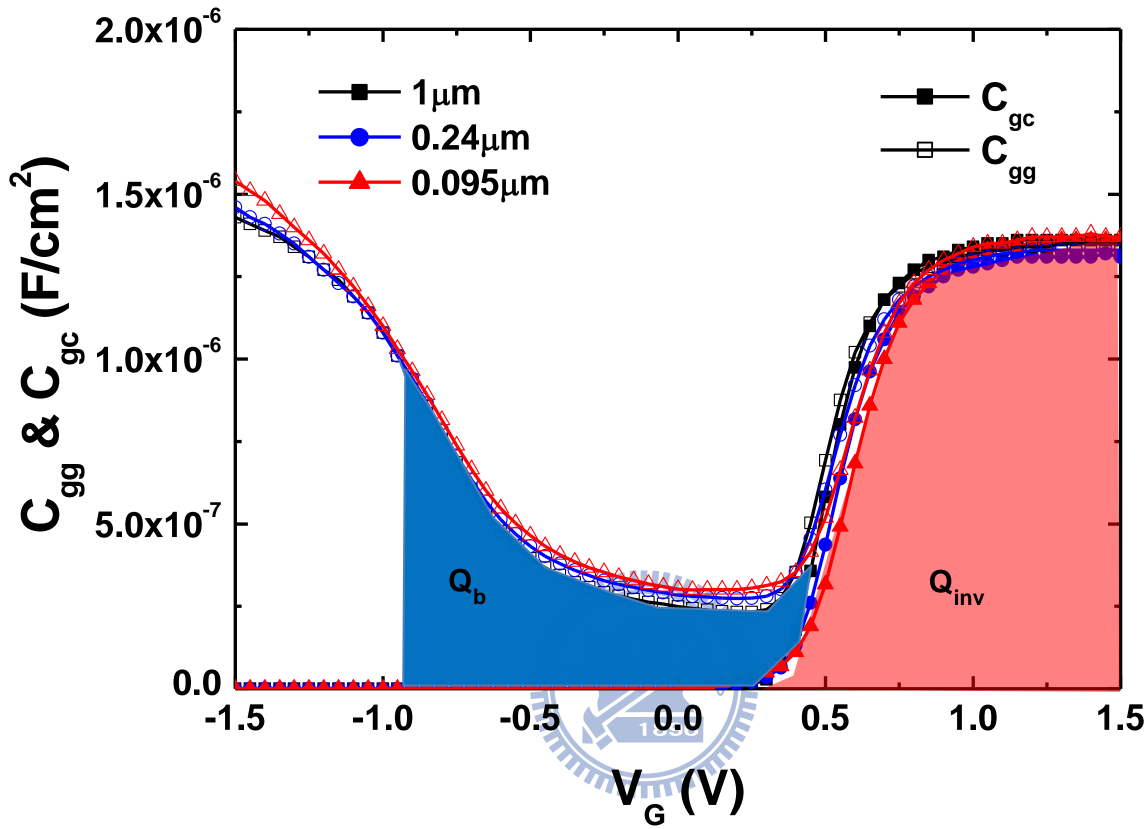


Figure 3.6. Q_{inv} and Q_b are obtained by integrating the whole C_{gc} and C_{gg} curve from flat-band voltage.

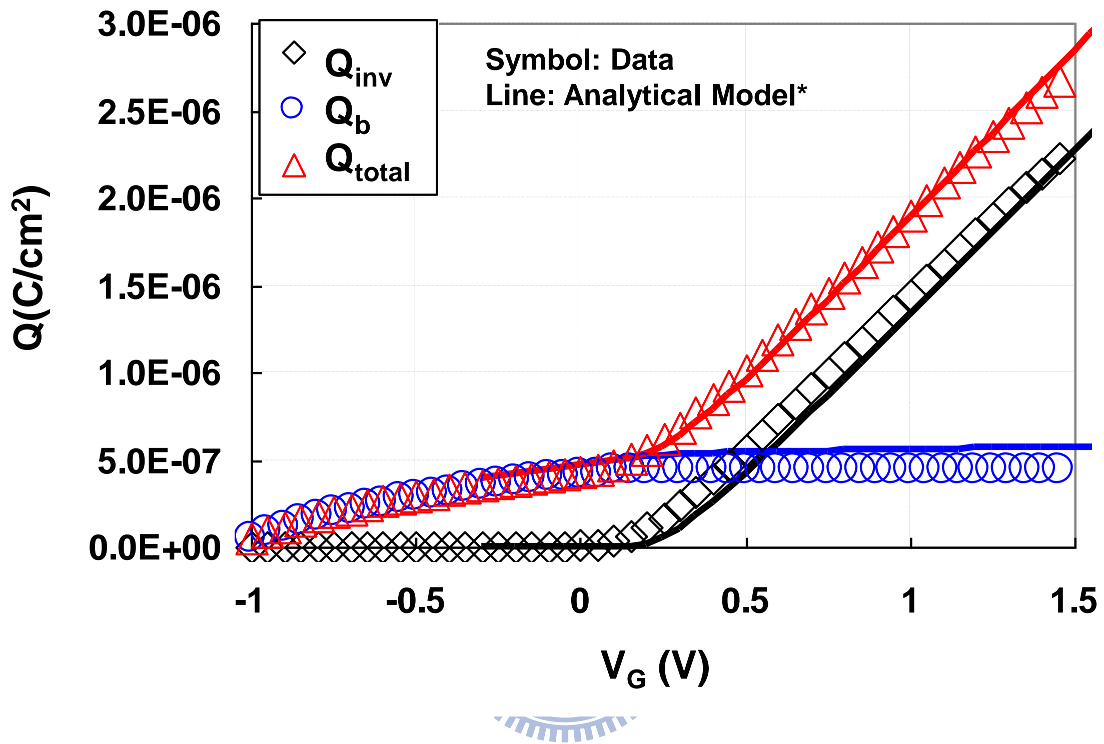


Figure 3.7. Extracted Q_{inv} and Q_b and Q_{total}(=Q_{inv}+ Q_b) versus gate bias.

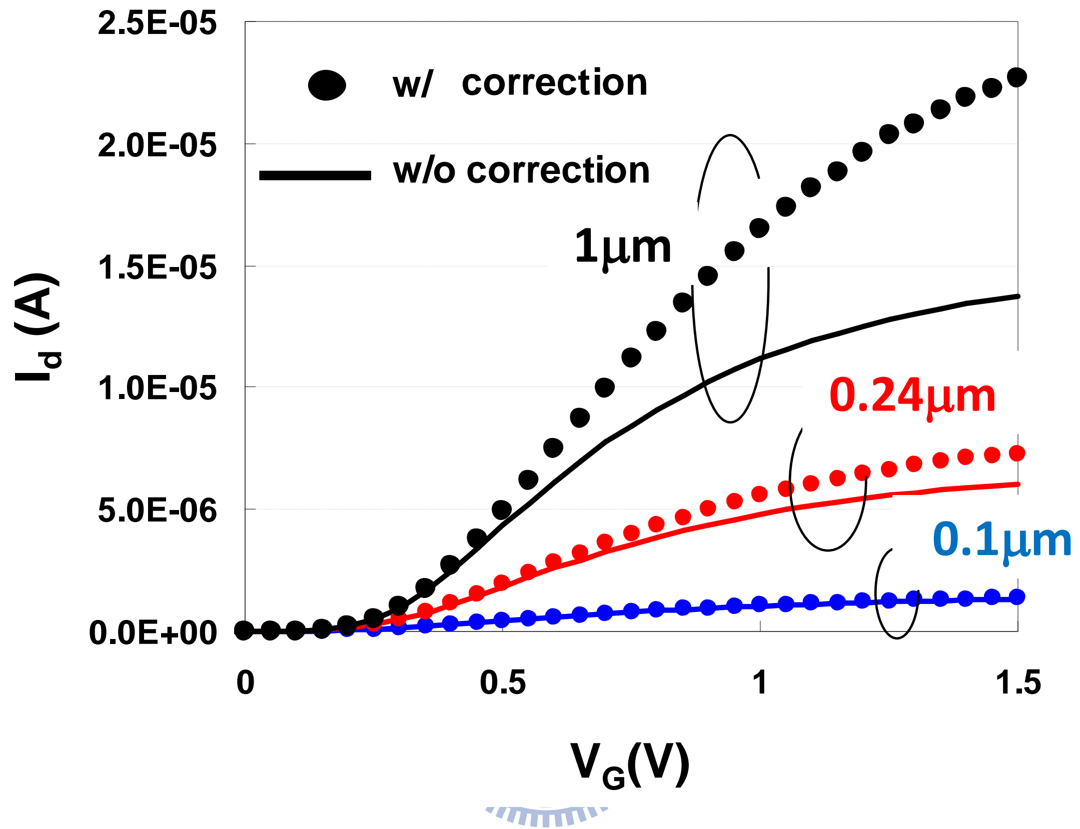


Figure 3.8. The drain current versus gate voltage with R_{sd} calibrations. It shows the R_{sd} is crucial to extract intrinsic drain current.

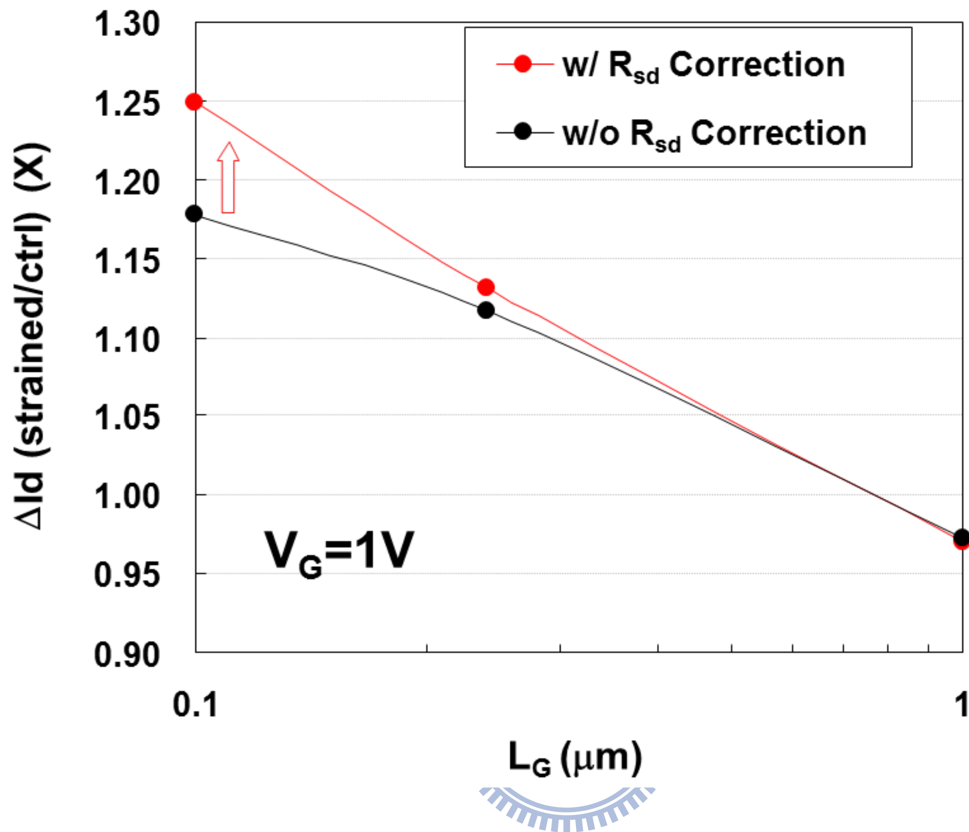


Figure 3.9. The drain current enhancement vs L_g by considering R_{sd} calibrations. It shows that the drain current enhancement can be underestimated if R_{sd} effect was not calibrated.

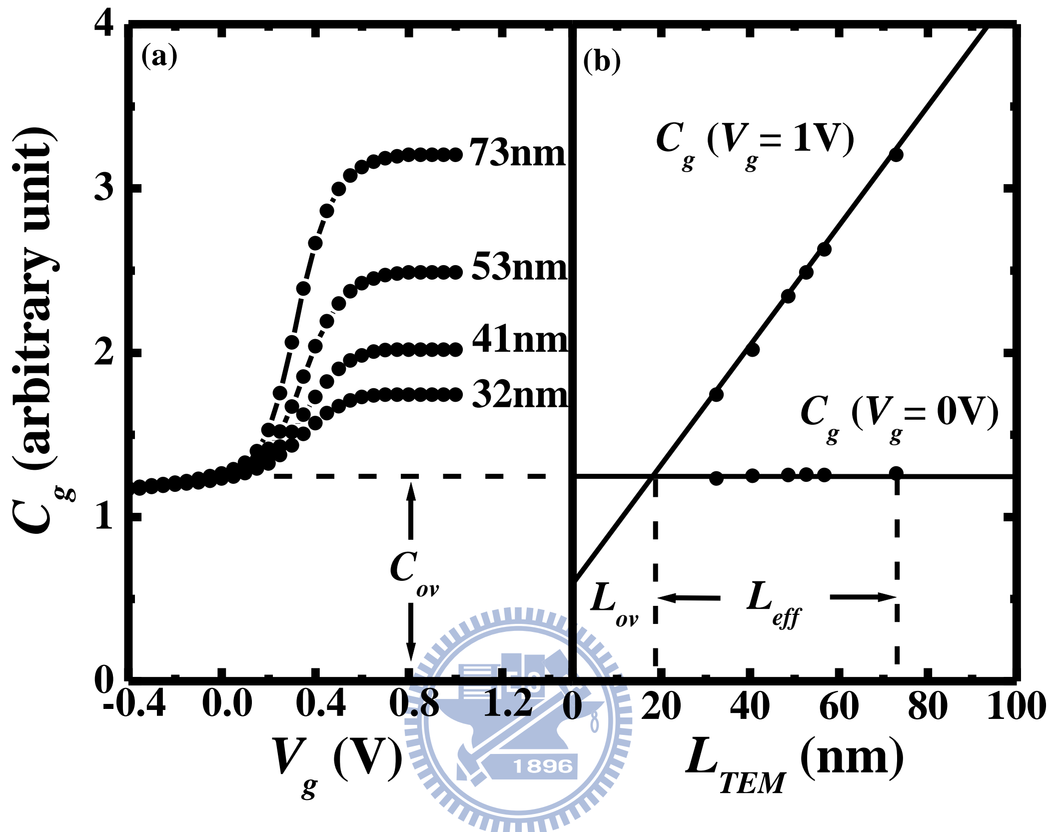


Figure 3.10. The L_{OV} and L_{EFF} can be extracted from Cgc curve with different Lg.

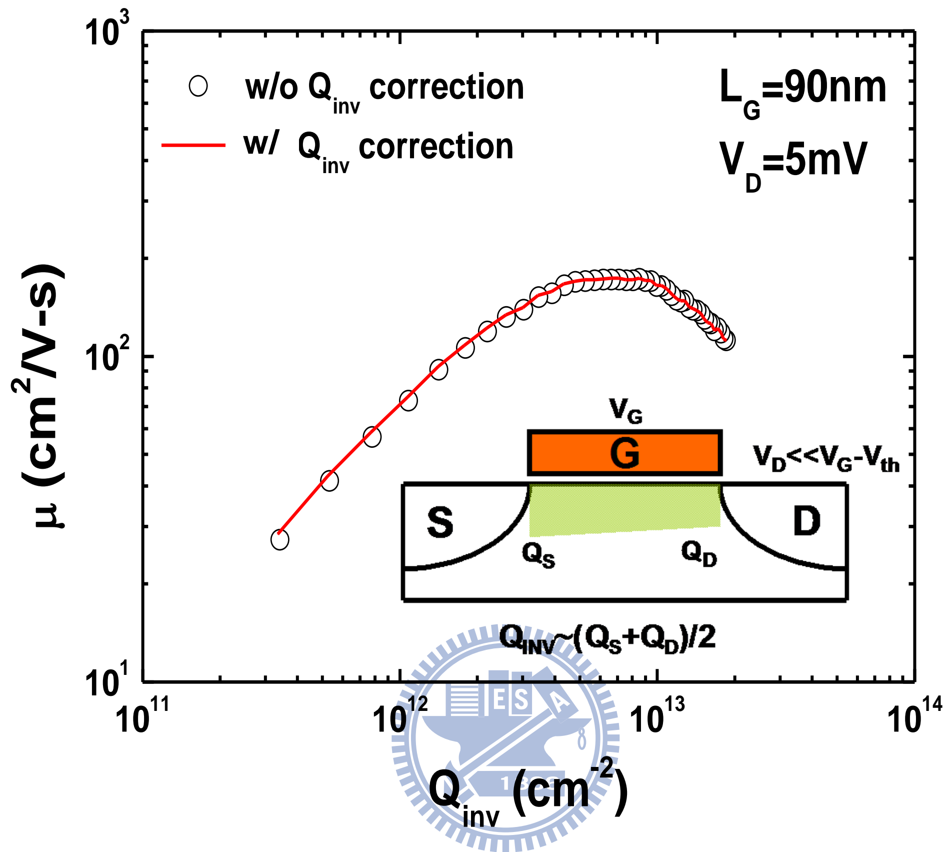


Figure 3.11. Extracted mobility by considering spatial distributions of Q_{inv}. (Inset: Spatial distribution due to V_D)

(a) Neutral CESL **(b) Compressive CESL**

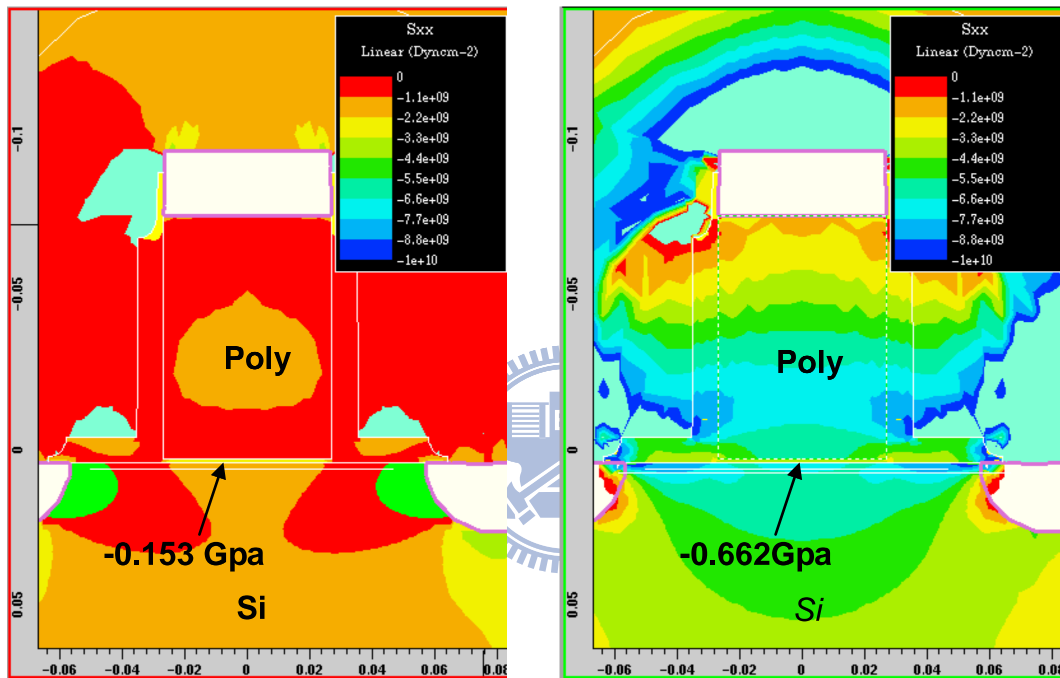
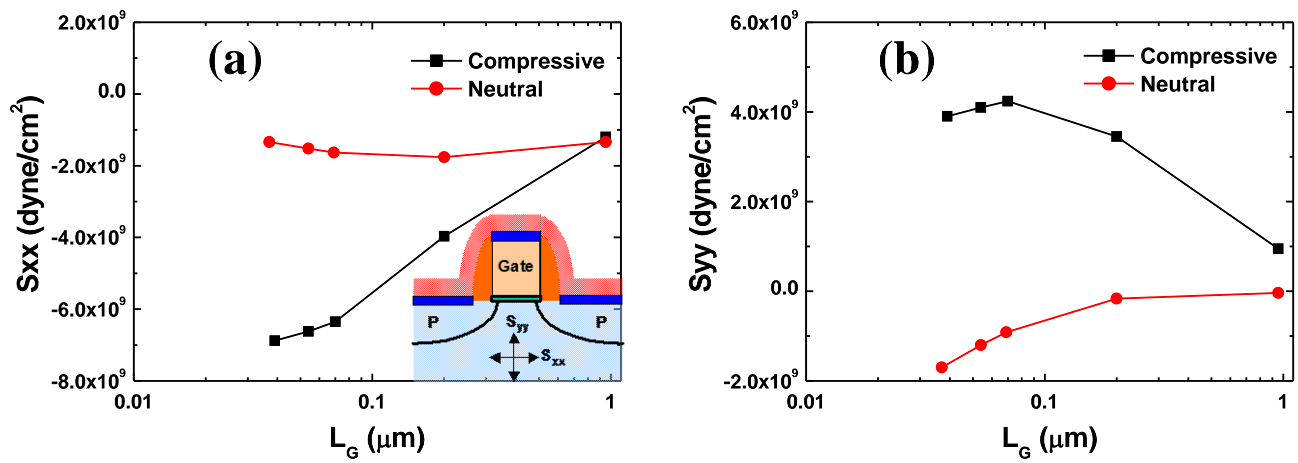


Figure 3.12. Stress contours by TCAD simulation: (a) Neutral CESL (b) Compressive CESL. The gate length equals 54nm. Average stress levels along the channel direction are –0.153 GPa and –0.662 GPa for (a) and (b) respectively.



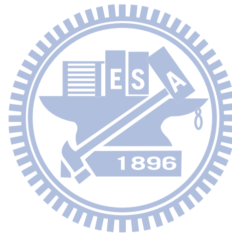


Figure 3.13. Gate length dependence of (a) Sxx and (b) Syy show compressive CESL contributes stronger compressive Sxx and stronger tensile Syy as L_G becomes shorter.

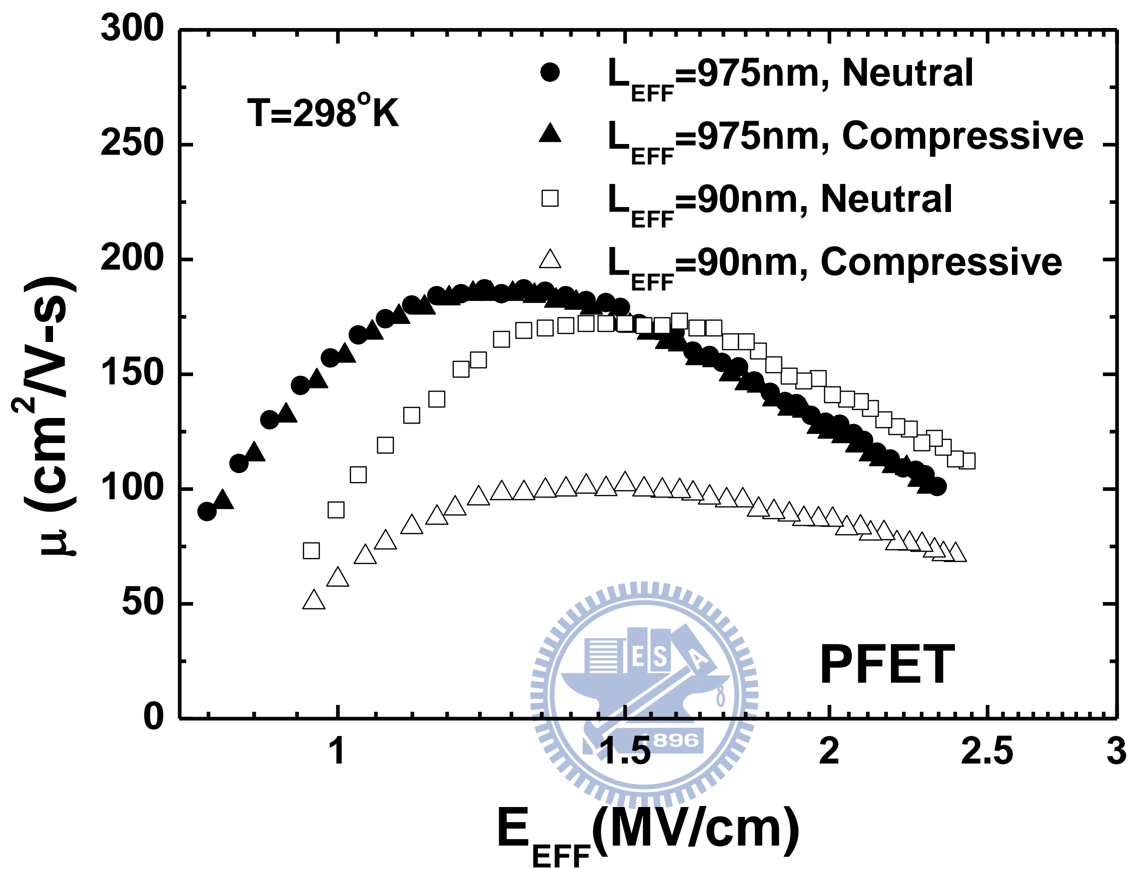


Figure 3.14. Our extracted short-channel mobility shows significant dependence on the uniaxial stressor applied.

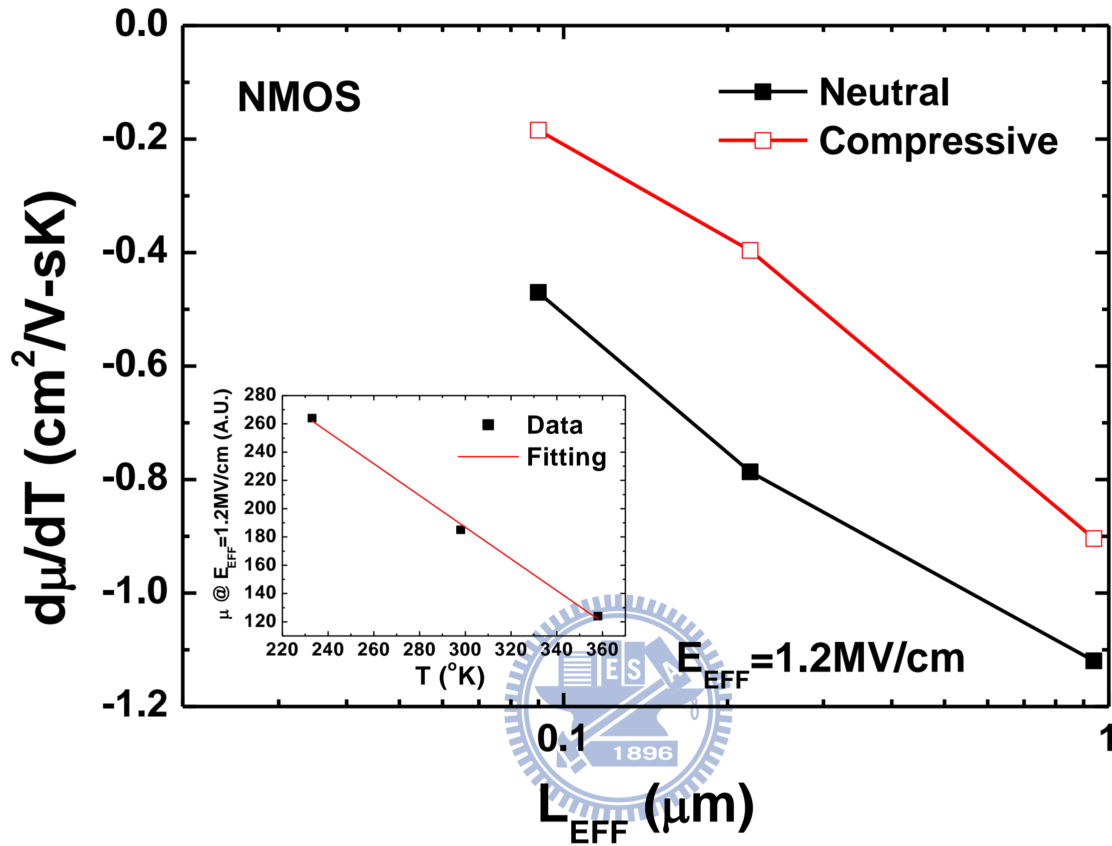


Figure 3.15. Temperature dependence of the mobility at (E_{EFF}=1.2MV/cm) versus L_{EFF}. [Inset: dμ/dT is extracted in the temperature range from 233K to 358K]

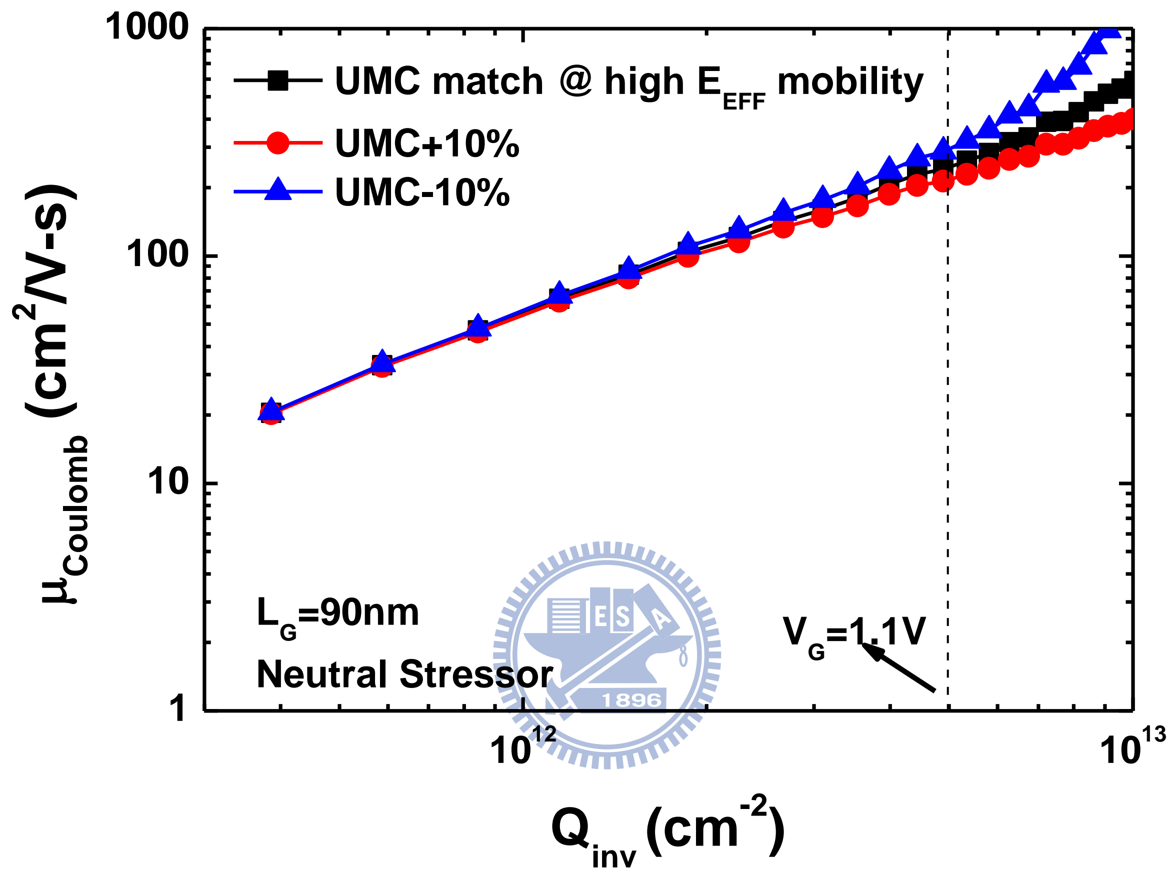


Figure 3.16. We have varied the UMC (Universal Mobility Curve) by ±10% to verify the accuracy of our extracted Coulomb mobility.

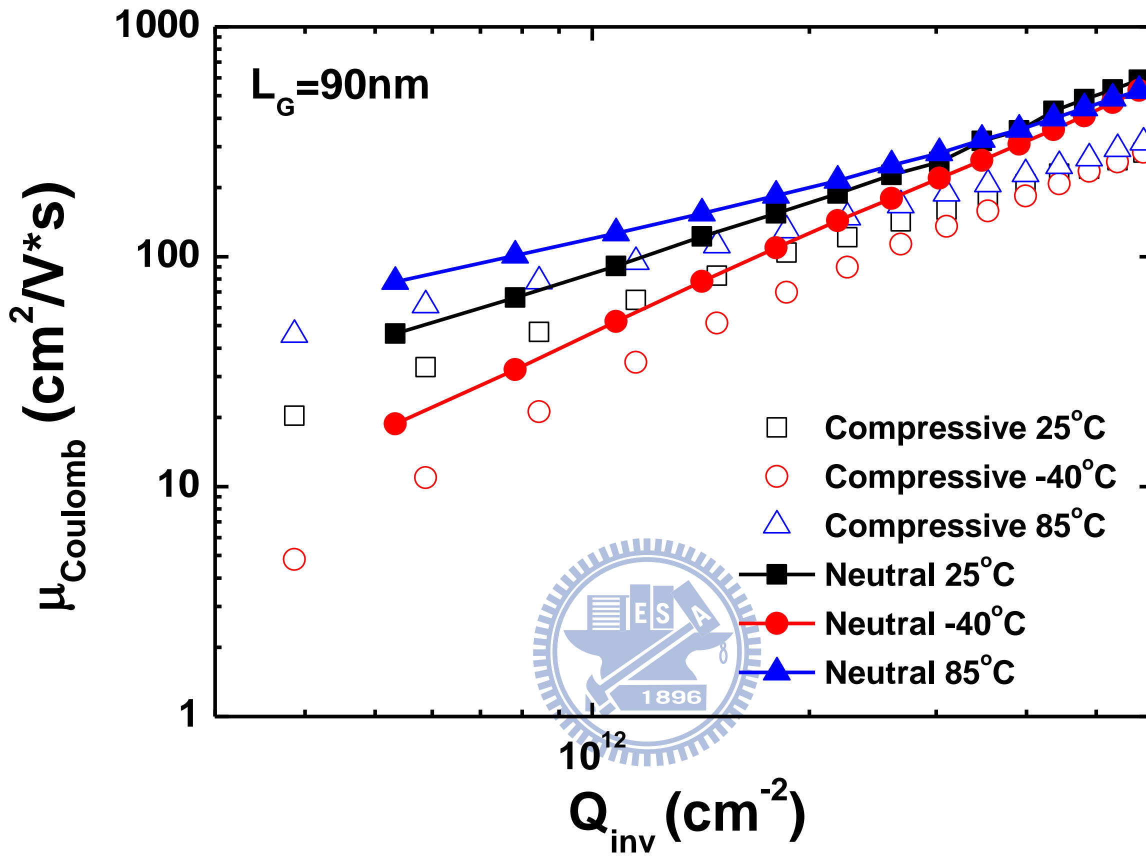


Figure 3.17. NFET Coulomb mobility for short-channel devices with different stressors under various temperatures.

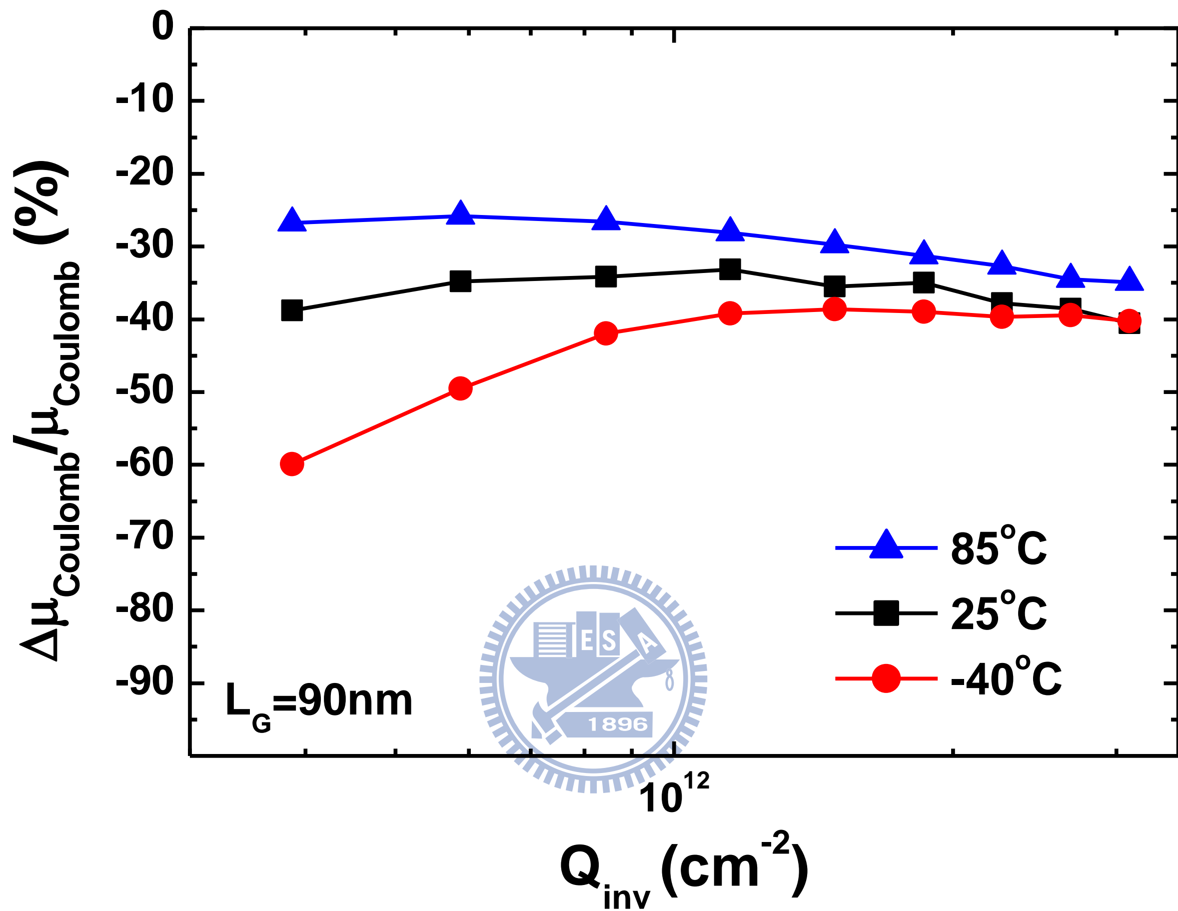


Figure 3.18. The stress sensitivity of Coulomb mobility under various temperatures. The $\Delta\mu_{Coulomb}$ represents $\mu_{Coulomb_strain}$- $\mu_{Coulomb_neutral}$.

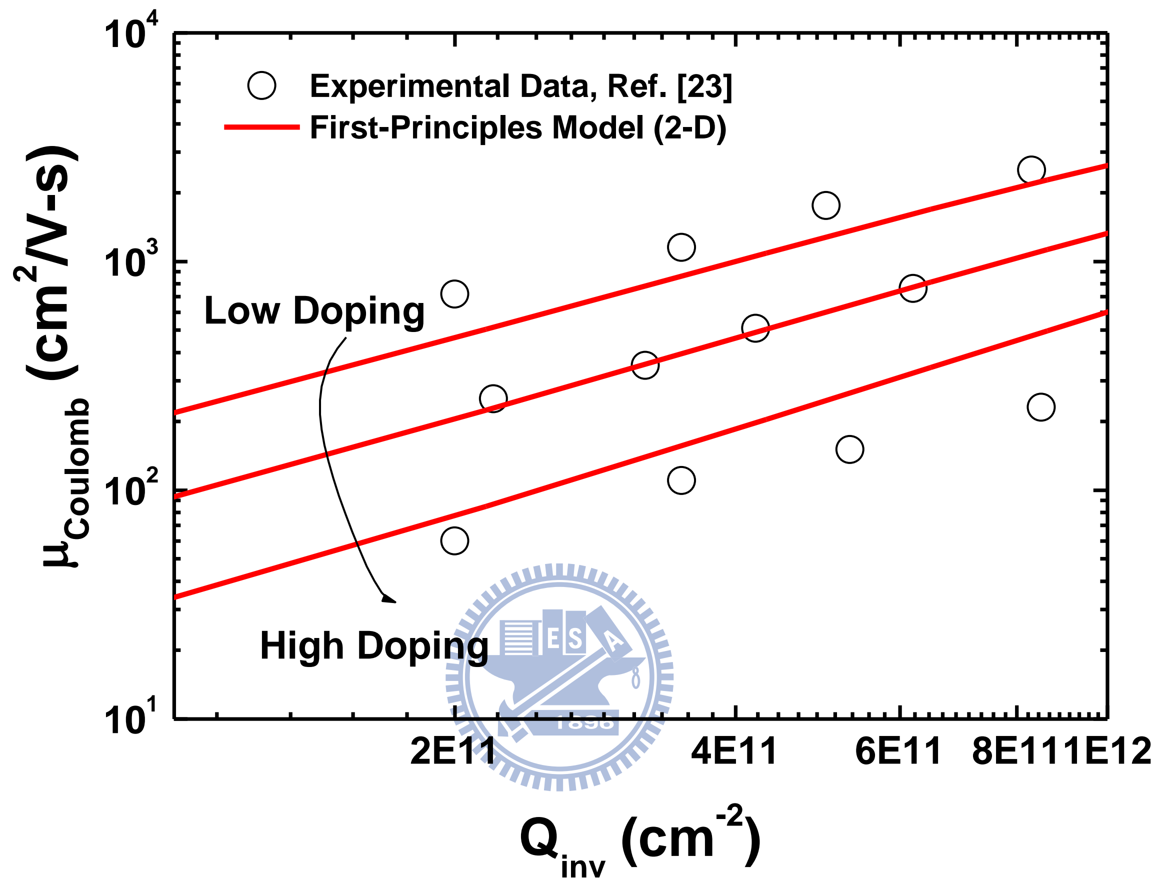


Figure 3.19. Coulomb mobility versus Q_{inv} with different bulk concentrations. It shows model fits well with published data [23]. Both screened and unscreened Coulomb scattering effects are included in this model.

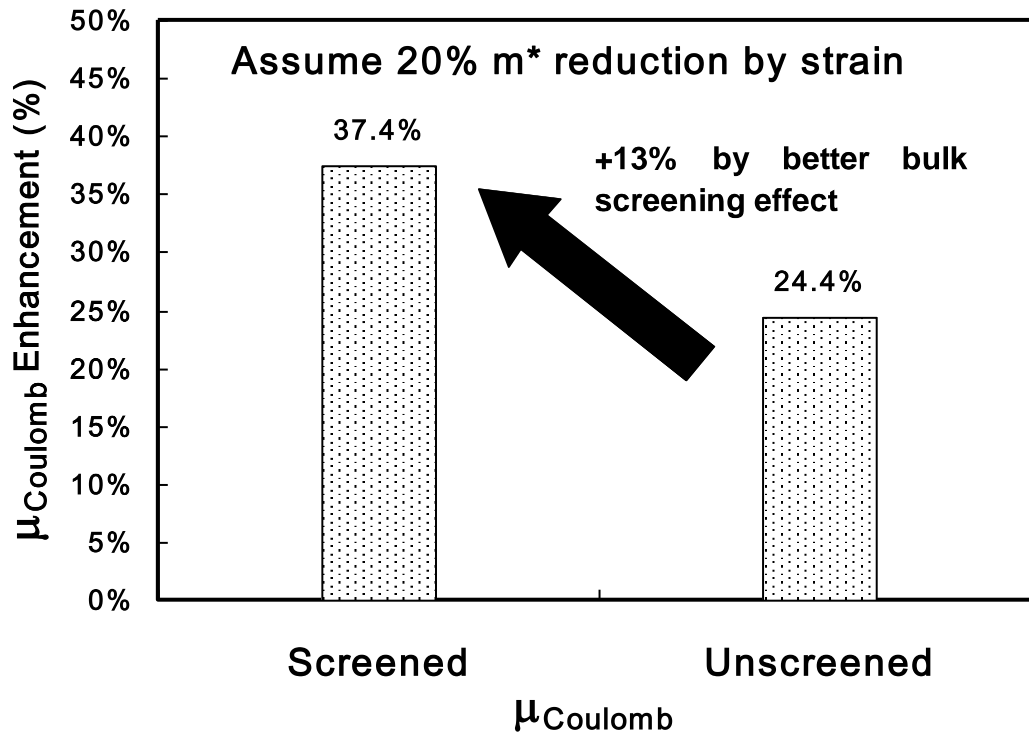


Figure 3.20. Screened and unscreened $\mu_{Coulomb}$ enhancement after 20% m* reduction. The prior one shows +13% better than the latter one because of better screening effect by strain.

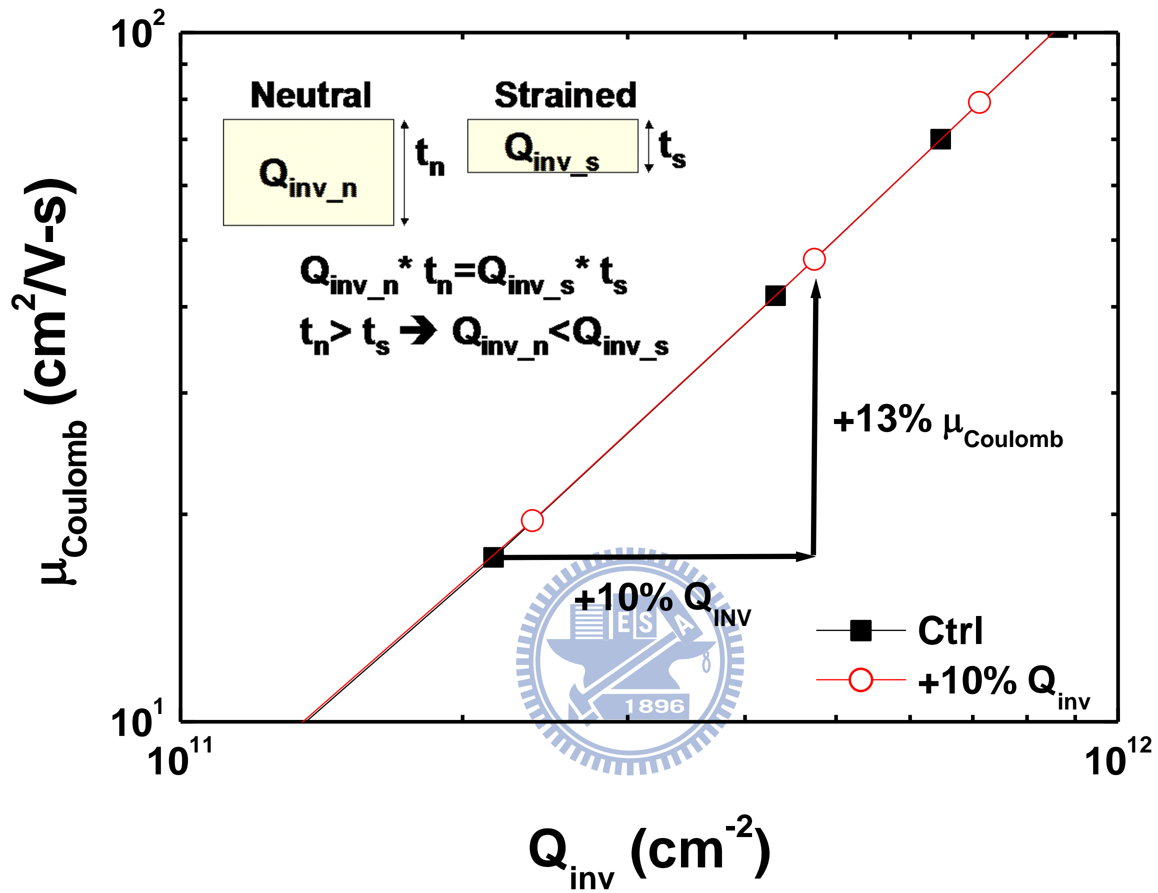


Figure 3.21. Coulomb mobility versus Q_{inv}. 10% higher Q_{inv} improves 13% $\mu_{Coulomb}$ due to better bulk screening effect. (Inset: Strain caused thinner inversion layer and then higher Q_{inv})

$\Delta\mu_{Coulomb}$ (Compressive vs Neutral)	+:Enhancement -:Degradation =:No sensitivity	
Mechanism/Scatterning Source	N_a (Bulk Charge)	N_{it} (Interface Charge)
Scatterning Effect	- (a), m* ↑	+ (b), Z_{inv} ↑
Screening Effect	- (c), Q_{inv} ↓	= (d) , no effect @ High N_a

NFET <110> Channel Direction; $\Delta\mu_{Coulomb}=\mu_{Coulomb_Compressive}-\mu_{Coulomb_Neutral}$

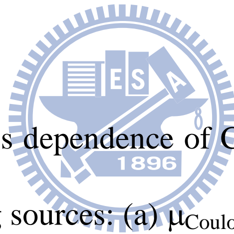


Table 3.1. Summary table of stress dependence of Coulomb mobility limited by different mechanisms and scattering sources: (a) $\mu_{Coulomb}$ degradation due to higher effective mass (m*) (b) $\mu_{Coulomb}$ enhancement due to thicker inversion layer thickness (Z_{inv}) (c) $\mu_{Coulomb}$ degradation due to lower electron density (d) Minor stress sensitivity on $\mu_{Coulomb}$ due to Quantization effect caused by high N_a.

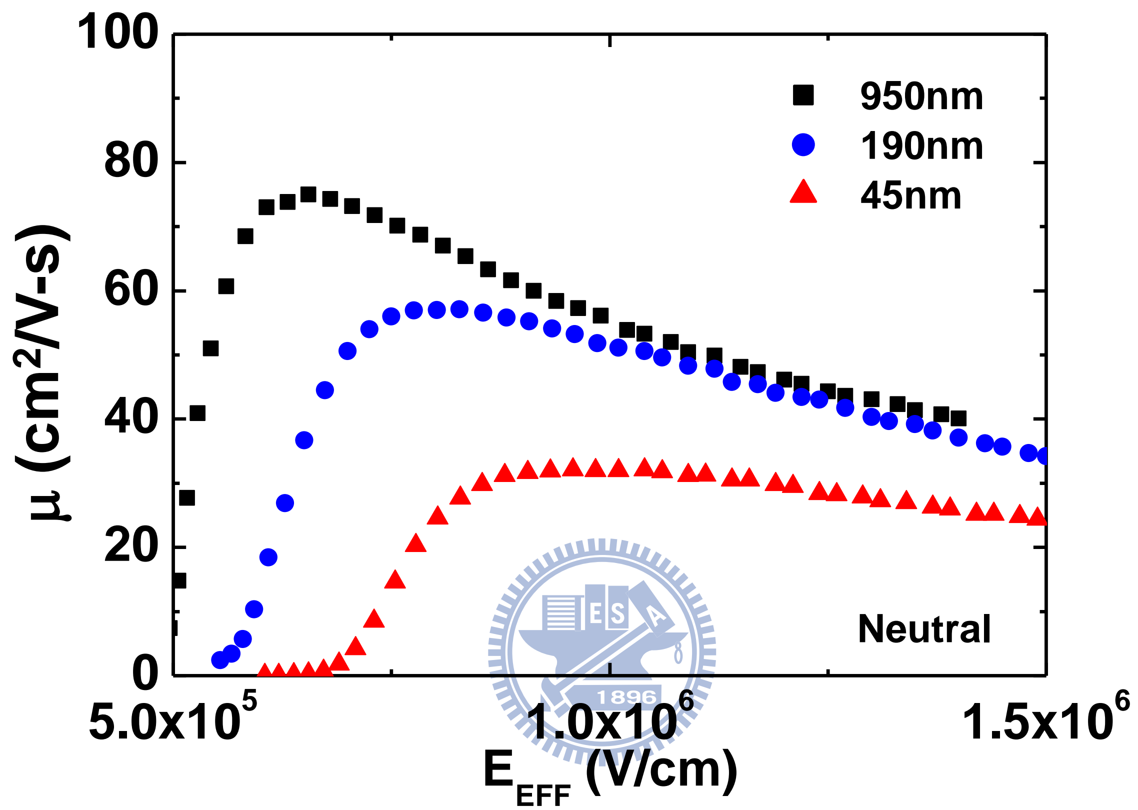


Figure 3.22. PFET low field mobility versus the vertical electric field at different L_{EFF} with neutral stressor.

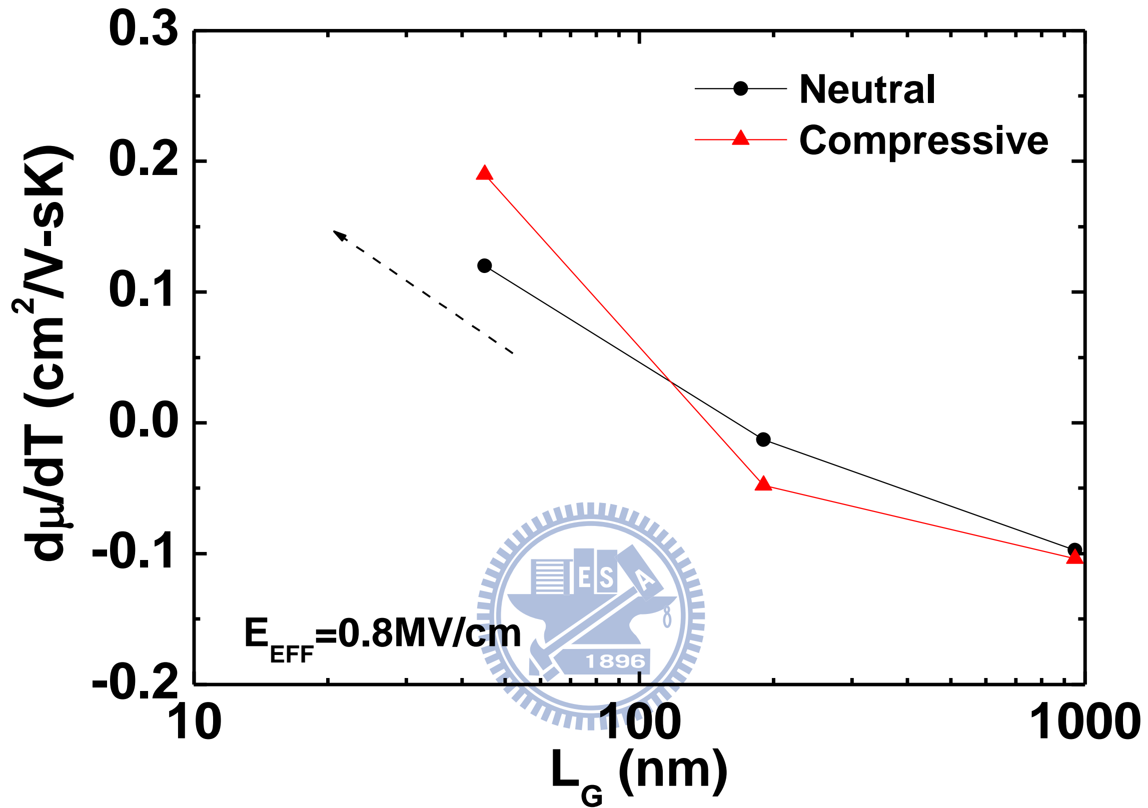


Figure 3.23. Vertical field mobility sensitivity to temperature (E_{EFF}=0.8MV/cm) versus L_{EFF} in PMOS. It shows that Coulomb mobility plays an important role in the short channel region. When temperature is increased, the thermal velocity of carriers becomes faster. It means Coulomb scattering probability becomes lower and causes higher Coulomb mobility.

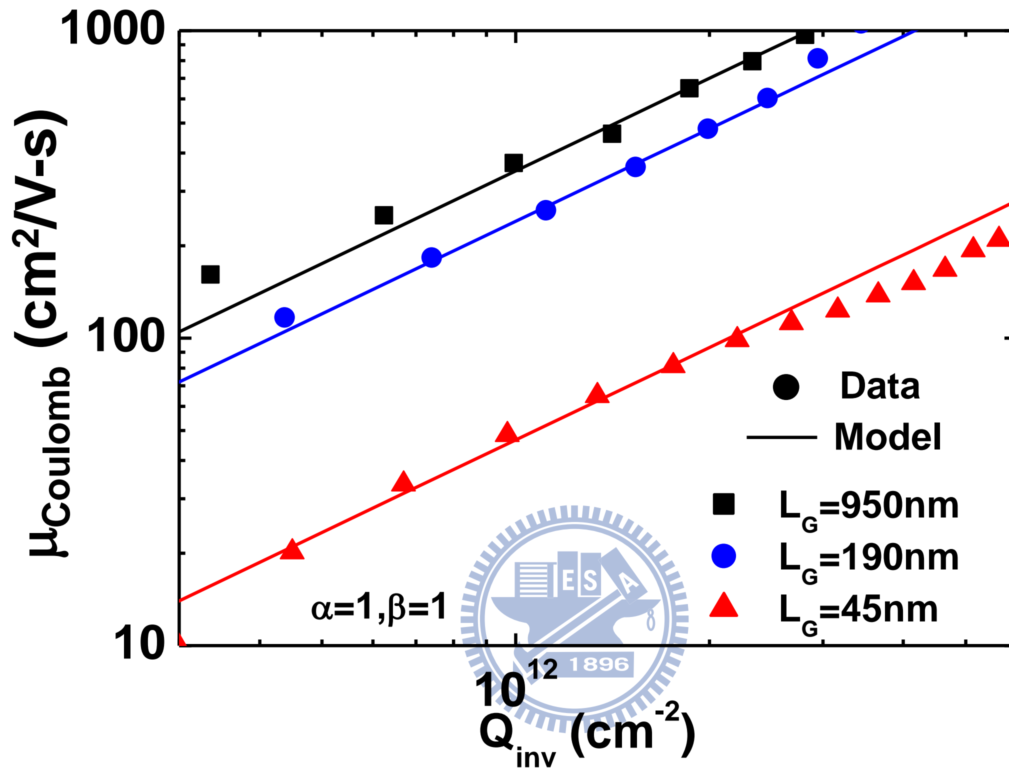


Figure 3.24. Coulomb mobility data versus model in PMOS for long and short channel regions. Coulomb mobility becomes smaller as L_{EFF} shrinks because of higher N_a. *A* is a constant, α and β are both equal to 1, N_a is extracted from NCSU fitting programs.

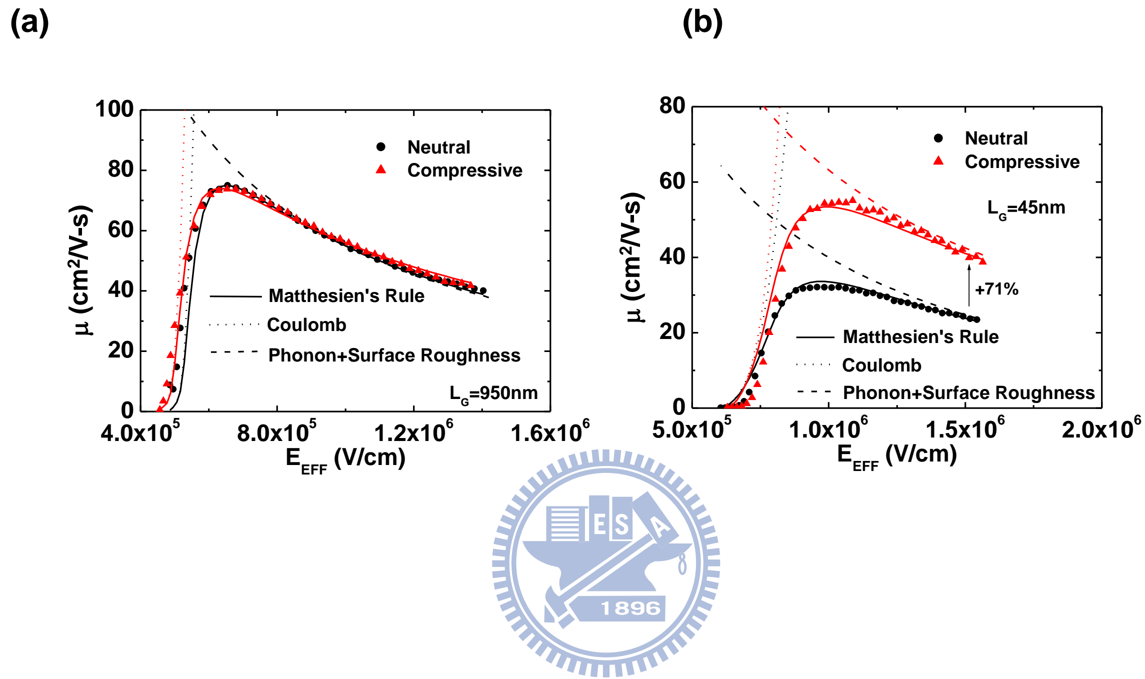


Figure 3.25. (a) PFET long channel mobility (L_{EFF}=950nm) with neutral and compressive CESL stressors. The mobility model matches with silicon data very well. Since the uniaxial stressor is only effective for short channel devices, the long channel mobility is almost the same under different neutral and compressive stressors. (b) PFET short channel mobility (L_{EFF}=45nm) with neutral and compressive CESL stressors. The extracted total mobility agrees with the model quite well. The 71% mobility enhancement for compressive stressor in the high vertical field region is mainly due to the uniaxial local compressive stress.

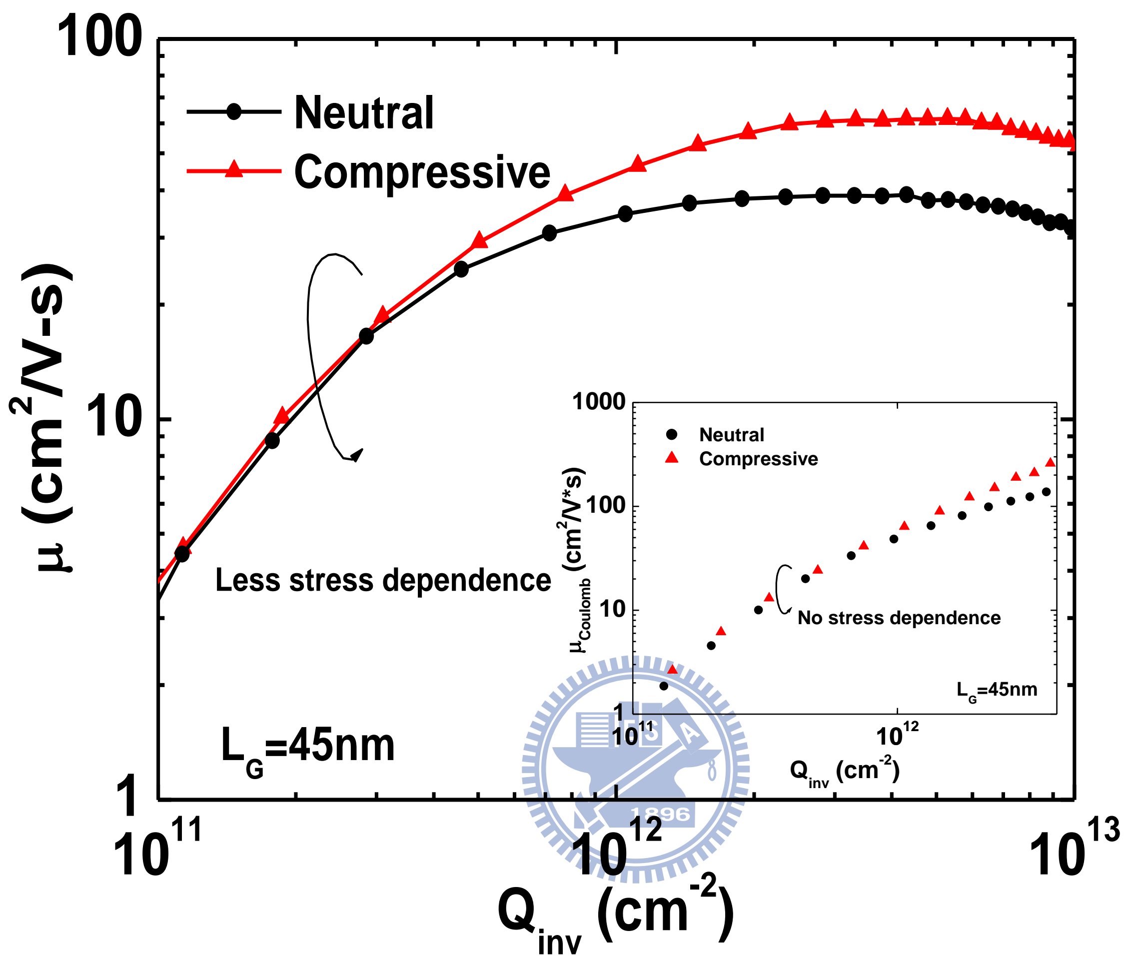


Figure 3.26. PFET total mobility at low vertical field versus Q_{inv} under various stressors. Very little stress dependence is observed in the low field region, where Coulomb scattering mechanism dominates. (Inset: PFET Coulomb mobility extracted by Matthiessen's rule between neutral and compressive stressors. No stress dependence is observed in short channel region at room temperature.)

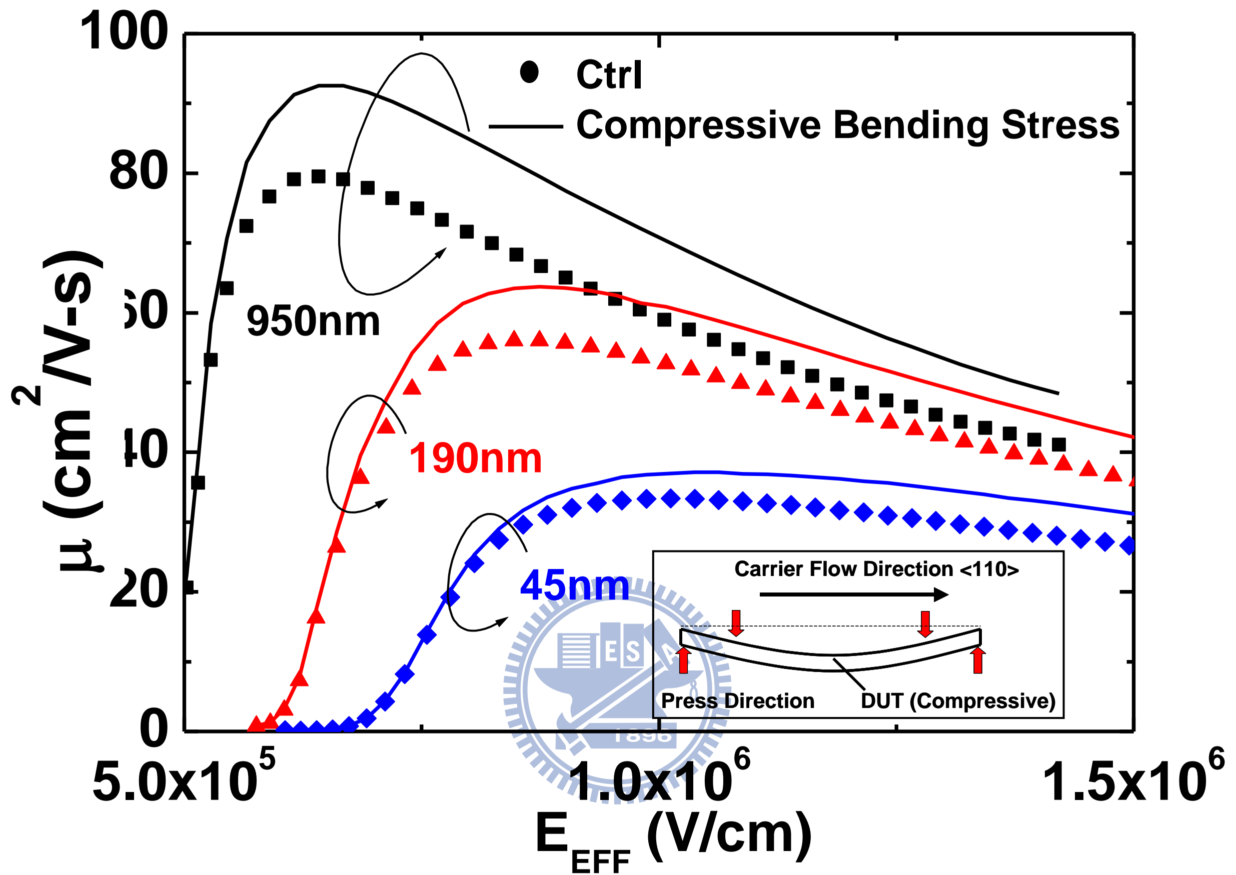


Figure 3.27. PFET total mobility versus E_{EFF} after applying 230Mpa compressive bending stress on devices with different L_{EFF}. Unlike the behavior of local stressors, significant mobility improvement can be observed from long to short channel devices in the high vertical field region because of global stress effect. (Inset: The schematic of the mechanical bending tool)

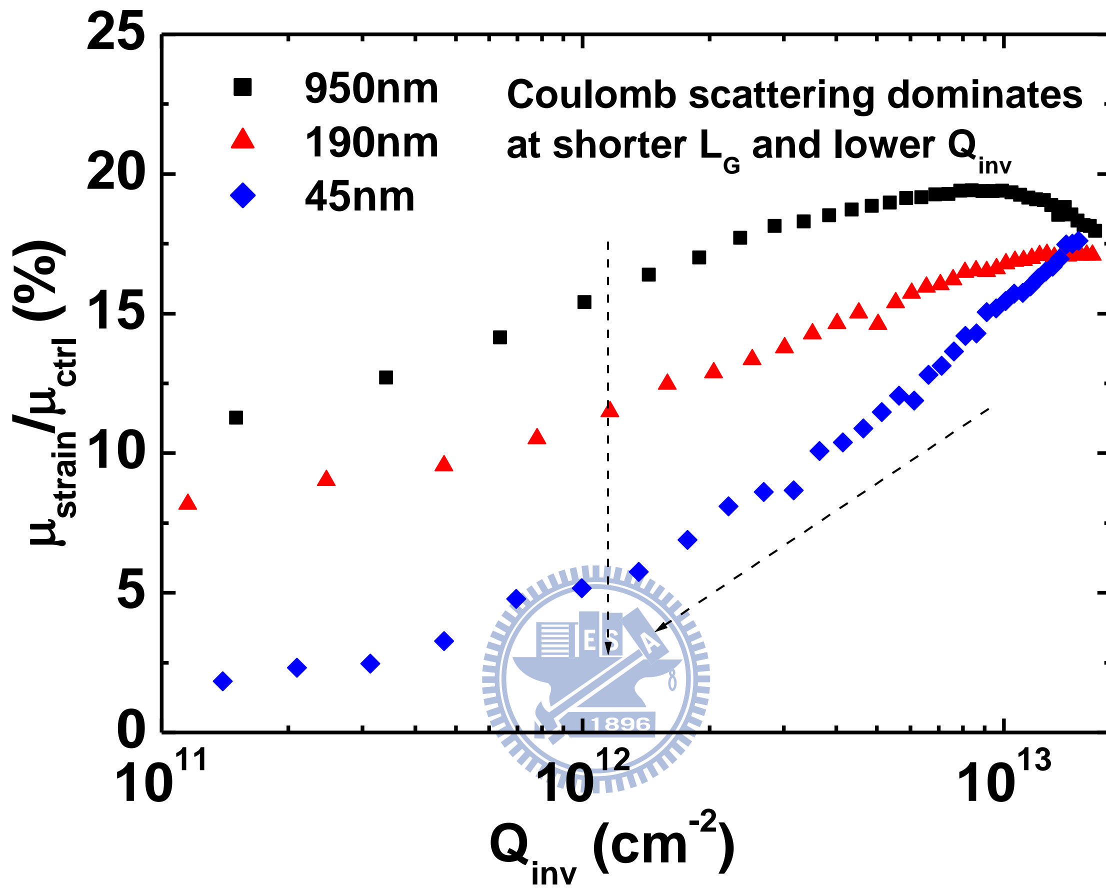


Figure 3.28. PFET total mobility enhancement versus Q_{inv} by applying compressive mechanical stress on the devices with different L_{EFF}.

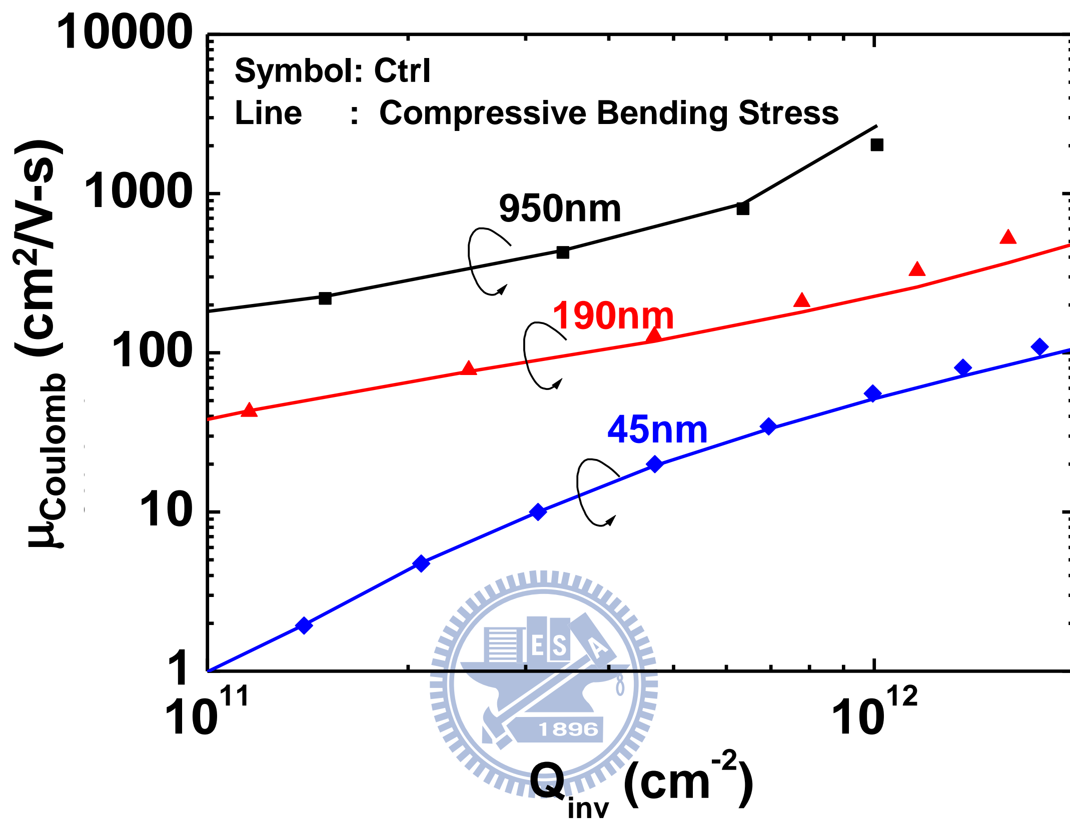


Figure 3.29. PFET Coulomb mobility versus Q_{inv} by applying compressive mechanical stress on the devices with different L_{EFF}. No stress dependence is observed for both long and short channel Coulomb mobility, which is consistent with the findings from local stressors.

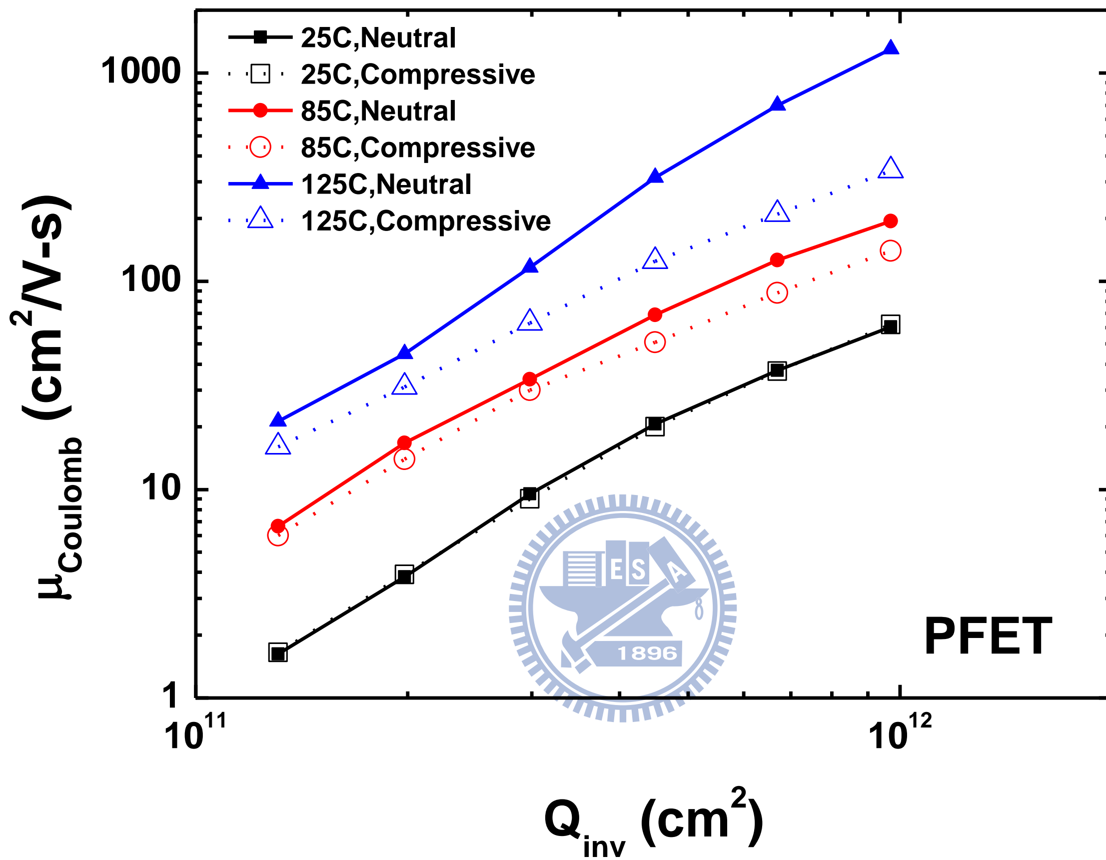


Figure 3.30. PFET Coulomb mobility for short-channel devices with different stressors under various temperatures.

Chapter 4

Impact of Uniaxial Strain on the Surface Roughness Scattering Limited Mobility in Nanoscale p-MOSFETs

4.1 Introduction

Strain technology has been considered as a key process knob beyond 90nm technology [1,2]. It is known that strain can improve phonon scattering limited mobility (μ_{PH}) by reducing inter-valley phonon scatterings and effective conduction mass [2]. Whether strain can improve the surface roughness limited mobility (μ_{SR}) is still not clear and demands more experimental investigations.

Recently, the biaxial strain dependence of μ_{SR} has been examined by Bonno *et al.* [3] and Zhao *et al.* [4]. These studies show μ_{SR} has strong strain sensitivity for both NFETs and PFETs with biaxial strain. However, the observed μ_{SR} data by Zhao *et al.* [3,4] showed opposite trend between NFET and PFET and cannot be easily explained by the micro-roughness of Si/SiO_2 interface. The temperature dependences of hole mobility by mechanical uniaxial strain [5] and process-induced uniaxial strain [6] have also been studied experimentally. However, the temperature range was higher than 87K and the phonon scattering mechanism was not fully suppressed. To investigate the uniaxial strain dependence of surface roughness mobility, it is necessary to extract mobility with temperature down to 20 K to suppress the phonon scattering mechanism.

In this work, we examine the impact of strain on μ_{SR} of pMOSFETs by process-induced uniaxial strain with He-based low temperature system and compare the strain sensitivity between μ_{PH} and μ_{SR} [7,8]. In addition, a wavefunction penetration perspective [8,9] is proposed to explain the possible physical origin of the uniaxial

strain dependence of μ_{SR}.

4.2 Experimental Setup

pMOSFETs with channel direction <110> under neutral, tensile and compressive uniaxial Contact Etch-Stop Layer (CESL) [8] were investigated. In this study, the carrier mobility of PMOS devices with L_{EFF} =95nm and conventional silicon oxynitride gate was examined. The equivalent oxide thickness is about 17Å. The estimated stress is -2.8GPa for compressive film and +1.6GPa for tensile film [10]. The drain bias condition is -5mV.

Split C-V measurement [11,12] was used to characterize the inversion charge density (Q_{inv}). After the gate-to-channel capacitance with floating bulk terminal (C_{gc}) was calibrated by considering the parasitic components such as overlap capacitance and fringing capacitance [13,14], Q_{inv} was obtained by integrating the entire C_{gc} curve from flat-band voltage [15].

Since external resistance (R_{sd}) is crucial to the mobility extraction for short-channel devices [16,17], the intrinsic drain current (I_d) was calibrated by considering the series-resistance effect using the methodology introduced in Chapter 2. The R_{sd} values considered constant as a function of temperature are 201, 208 and 185 ohms-μm, respectively, for neutral, compressive and tensile stressors. The physical poly gate length (L_{PHY}) was obtained by inline SEM measurement. The LDD overlap region under the gate (L_{OV}) was extracted by the split-CV method [19]. The effective channel length (L_{EFF}) can then be derived by subtracting L_{OV} from L_{PHY}. Finally, the carrier mobility can be extracted [6].

In order to extract the surface roughness mobility μ_{SR}, cryogenic temperature measurements were carried out using liquid He as cooling source. The measurement temperature ranges from 10K to 300K. HP4156 and HP4285 were adopted to measure

the IV and CV characteristics.

Fig. 4.1 shows the drain current with constant voltage overdrive 1V with 21 samples for PFET. The drain current with constant voltage overdrive can exclude the variations of threshold voltage of the samples. It shows that the variations of constant overdrive drain current are <4% for neutral, compressive and tensile stressors respectively. Sample #7 was chosen for the following surface roughness mobility extraction at cryogenic temperature.

4.3 Impact of Uniaxial Strain on the Surface Roughness Mobility

Fig. 4.2 shows the drain current versus gate voltage at various temperatures for PFETs with neutral stressor. It can be seen that the drain current increases with decreasing temperature. Fig. 4.3 shows the characteristic of capacitance versus gate voltage (CV) with various temperatures. It shows that CV characteristic are almost independent of temperatures. Fig. 4.4 shows the corresponding carrier mobility versus vertical electric field (E_{EFF}) with various temperatures. It can be seen that under high E_{EFF}, the mobility tends to increase as temperature decreases due to suppressed phonon scattering. At temperature lower than 60K, the mobility at high E_{EFF} saturates because the phonon scattering mechanism is fully suppressed. In other words, the mobility at high E_{EFF} within this temperature range can be viewed as the surface roughness limited mobility.

Fig. 4.5 shows the extracted carrier mobility versus temperature at E_{EFF}=1.6MV/cm for various stressors. It can be seen that the compressive uniaxial strain results in significant mobility enhancement due to band engineering and carrier repopulations [2]. In addition, μ_{SR} dominates the total mobility for temperature <60K for all kinds of stressors. Fig. 4.6 shows the mobility enhancement percentage ($\Delta\mu/\mu$) versus temperature with compressive and tensile stressors. As temperature decreases, it

can be observed that the mobility enhancement increases and saturates at temperature <60K where surface roughness scattering dominates. It indicates that μ_{SR} has stronger stress sensitivity than μ_{PH}. Furthermore, the surface roughness mobility enhancement tends to saturate and shows little sensitivity to temperature. It is worth noting that our experimental results are consistent with the reported results by Monte-Carlo simulations [20,21]. Specifically, it was reported in [20] that the scattering rate with interfacial roughness can be reduced by smoother interfaces in biaxial strained NFET. In addition, the atomic scale model in [21] also indicates weaker surface scattering potential in strained Si due to the nature of primitive defects. For the uniaxially strained PFET case, it is plausible that the lighter effective conduction mass [5] induced by compressive strain may result in μ_{SR} enhancement. Besides, the strain dependence of μ_{SR} may also be explained from the perspective of the carrier wavefunction penetration model. We will keep this part for detail discussions in Chap 4.4 later.

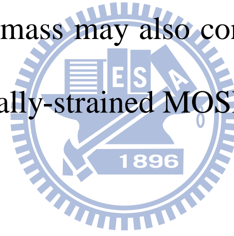
Fig. 4.7 shows the extracted carrier mobility versus effective vertical electric field (E_{EFF}) for neutral and compressive stressors at 20K. Within this temperature range, both the Coulomb scattering and surface-roughness scattering mechanisms are crucial in the determination of the overall carrier mobility. It can be seen that the mobility is dominated by the surface roughness scattering mechanism for E_{EFF} higher than 1.2MV/cm. The inset of Fig. 4.7 shows that μ_{SR} enhancement increases with E_{EFF} in the high E_{EFF} regime, where the carrier mobility is dominated by surface roughness scatterings. Based on the assumption that μ_{SR} is independent of temperature [22], we adopt Matthessien's rule ($\frac{1}{\mu_{PH}(T)} = \frac{1}{\mu_{total}(T)} - \frac{1}{\mu_{SR}(<60K)}$) to extract μ_{PH} and decouple the μ_{SR} and μ_{PH} enhancement with different temperatures, as shown in Fig. 4.8. Please note $\Delta\mu_{PH}$ with T<140K is not reliable because μ_{SR} is quite close to μ_{total}. It

shows the strain dependence of μ_{SR} indeed is stronger than μ_{PH} at E_{EFF}=1.6MV/cm from experimental data.

4.4 Discussion – A Wavefunction Penetration Perspective

In order to explain the observed strain dependence of surface roughness mobility, the possible root causes are list in the followings:

1. It is known that the scattering rate with interfacial roughness is reduced for smoother interfaces in biaxial strained MOSFET [3,4]. Therefore, better surface roughness morphology may contribute to the higher surface roughness mobility.
2. The atomic scale model in [21] indicates weaker surface scattering potential in strained Si due to the nature of primitive defects. Uniaxial strain Si should also show the same behavior.
3. Lighter conduction effective mass may also contribute to better surface roughness limited mobility [5] in uniaxially-strained MOSFETs.



Besides, a wavefunction penetration picture previously proposed by Polishchuk and Hu [9] is shown in Fig. 4.9. The penetration level depends on carrier attenuation length (λ) [9] and can be modeled as (1) [23]:

$$\lambda = \sqrt{\frac{\hbar^2}{2m_z\phi_b}} \quad (1)$$

with ħ the reduced Planck's constant, m_z the out-of plane effective mass, Φ_b the Si/SiO_2 potential barrier height. Since longer λ causes more roughness scatterings [9], the stress sensitivity of μ_{SR} ($\Delta\mu_{SR}/\mu_{SR}$) is determined by the strain engineering on m_z and Φ_b. The model was originally proposed to explain the impact of gate stack on the surface roughness mobility. Here we would like to extend the model to explain the impact of

strain on the surface roughness scattering mechanism.

From the angle of the wavefunction penetration perspective, compressive uniaxial strain on <110> pMOSFETs contributes heavier out-of-plane effective mass (m_z) and higher barrier height (Φ_b) [24-27], which cause shorter electron attenuation length and then lower surface roughness scattering rates. Therefore, lower surface scattering rates should be responsible for μ_{SR} enhancement in uniaxial pMOSFETs.

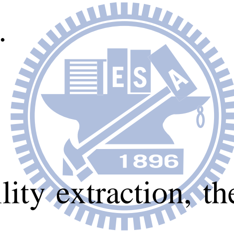
The wavefunction penetration model may also explain previous works on biaxial strain dependence of μ_{SR} [3,4,28]. Fig. 4.10 shows the $\Delta\mu_{SR}/\mu_{SR}$ of NFET and PFET extracted from [3,4,28] under biaxial tensile strain.

For NFET with biaxial tensile strain, Fig. 4.11 shows most electrons repopulate into the D2 valley under biaxial stress, which may result in higher Φ_b [24-27], heavier m_z [24-27], shorter λ and thus higher μ_{SR}. For NFET with uniaxial tensile strain, Fig. 4.12 shows most electrons repopulate into the D4' and D4'' valleys under uniaxial tensile stress, which may also result in higher Φ_b [24-27], heavier m_z [24-27], shorter λ and thus higher μ_{SR}, too.

For PFET, the biaxial strain dependence on μ_{SR} is quite different with the uniaxial strain case. In order to explain the different behaviors, the uniaxial and biaxial strain dependence on energy band diagram and m_z of each subband are referred to [24], as shown in Fig. 4.13. It can be seen that uniaxial compressive and biaxial tensile present different subband splitting behavior. Fig. 4.14 shows the PFET energy band diagram [2,24] and hole repopulations with uniaxial compressive stress and biaxial tensile stress, respectively. Both types of stressor result in higher Φ_b but opposite trend for m_z. Uniaxial compressive stress increases m_z, decreases λ, and consequently improves μ_{SR}. For biaxial tensile stress, λ is initially increased by the strain-reduced m_z, but is then decreased with increasing strain due to the strain-increased Φ_b. Both the strain-reduced

m_z and strain-increased Φ_b compete with each other. This explains the PFET non-monotonic behavior of $\Delta\mu_{SR}/\mu_{SR}$ versus strain level in Fig. 4.10.

Table 4.1 summarizes the polarities of stress sensitivity for m_z [24-27], Φ_b [24-27], λ and μ_{SR} respectively. In order to verify the strain dependence on wavefunction penetration level, a 1D QM Sivalco simulator [29] is modified to examine the polarities in Table 4.1. Fig. 4.15 shows the electron wavefunction penetration into gate dielectric from the exact solution, where m_z=0.3m_0, V_g=1.4V and T_{ox}=50Å. In Fig. 4.16, higher Φ_b and heavier m_z show lower fraction *f* of carrier penetration [9] from 1D QM simulations. The definition of *f* is the ratios of the carriers penetrating into dielectric. Typically lower *f* means less wavefunction penetrations, which means shorter λ and lower surface roughness scattering rates [9]. The result is consistent for the case of uniaxial NFET shown in Table 4.1.



4.5 Conclusion

By accurate split C-V mobility extraction, the strain dependence of μ_{SR} in short channel pMOSFETs is investigated under cryogenic temperatures. Our measured data indicates that μ_{SR} can be significantly enhanced by the uniaxial compressive strain. Furthermore, the μ_{SR} has higher strain dependence than the phonon scattering limited mobility (μ_{PH}). Our experimental results confirm the previously reported results based on simulations [20,21]. Furthermore, from the angle of the wavefunction penetration, compressive uniaxial strain results in shorter electron attenuation length and thus lower surface roughness scattering rates. In addition, the wavefunction penetration model also successfully explains the strain dependence of μ_{SR} for both uniaxial and biaxial strain silicon.

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Constant Overdrive Current	Compressive	Tensile	Neutral
sigma/med (21 DUTs)	2.90%	3.68%	3.26%

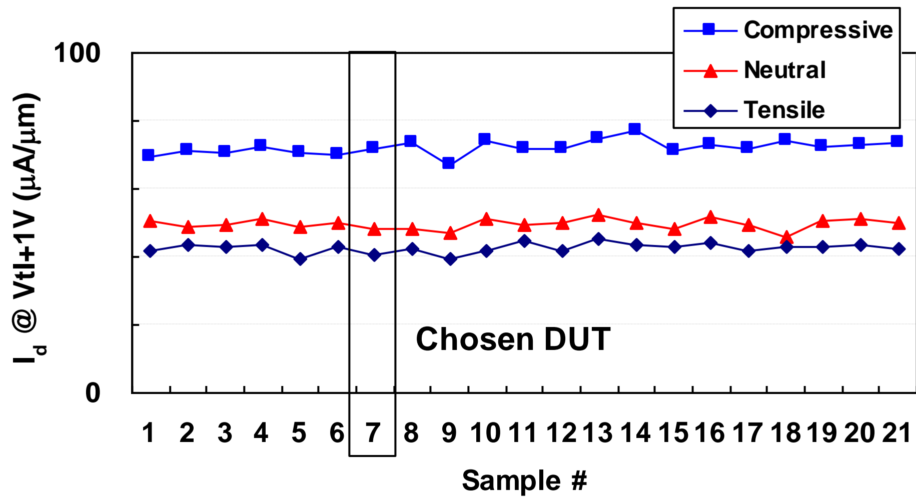


Figure 4.1. Drain current with constant overdrive 1V with 21 samples for PFET.

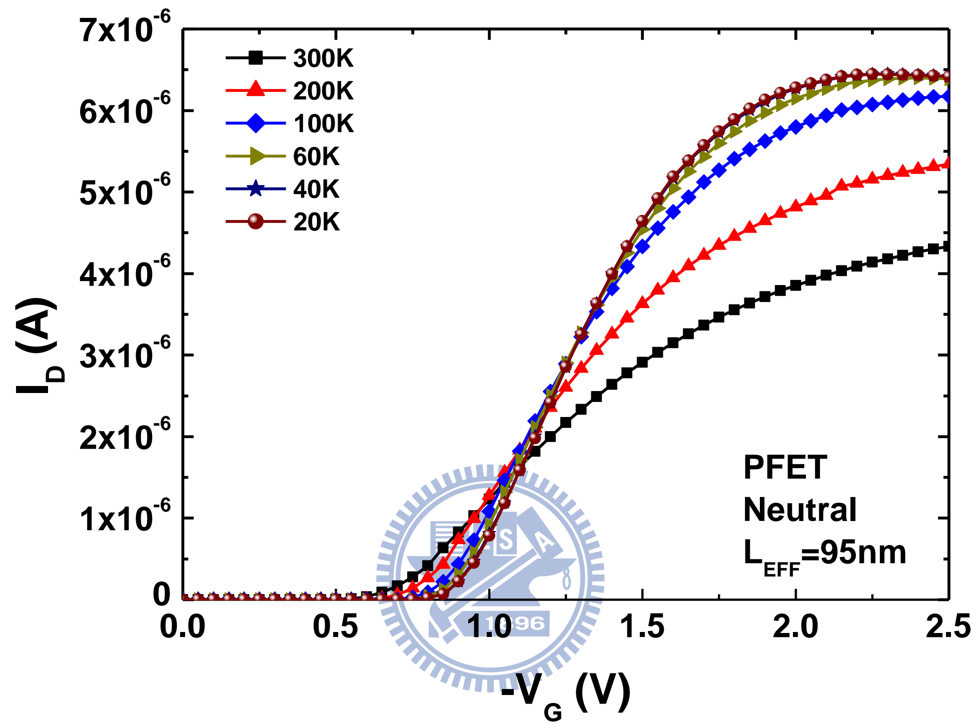


Figure 4.2. Drain current versus gate voltage at various temperatures for PFET with neutral stressor.

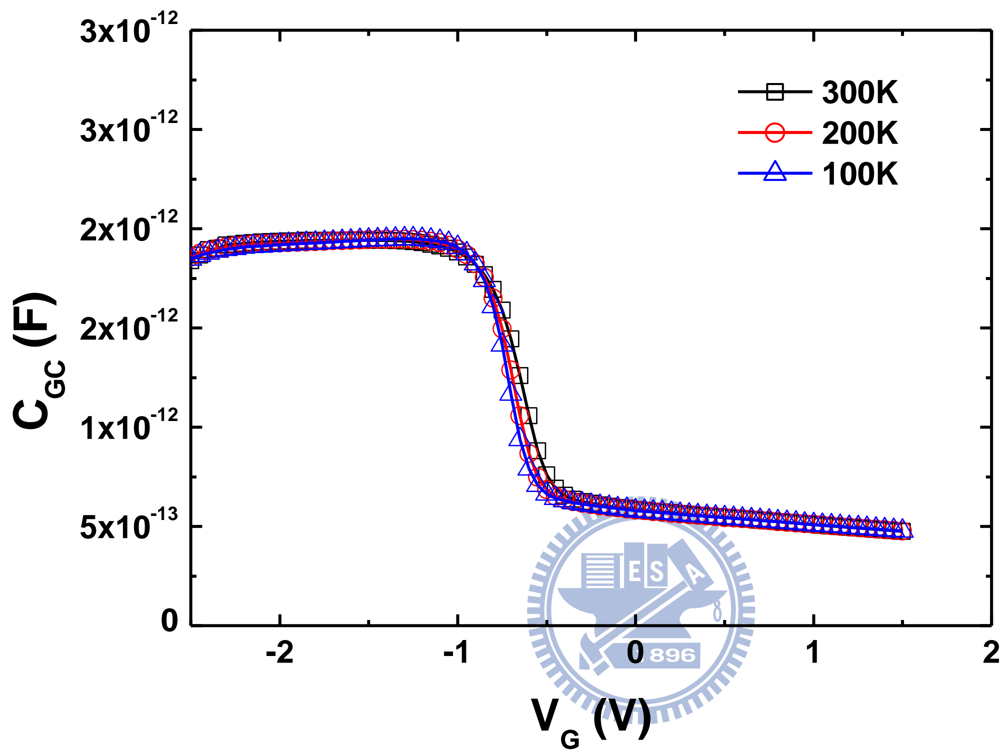


Figure 4.3. The characteristic of capacitance versus V_G with various temperatures. The CV curves are almost independent of temperature.

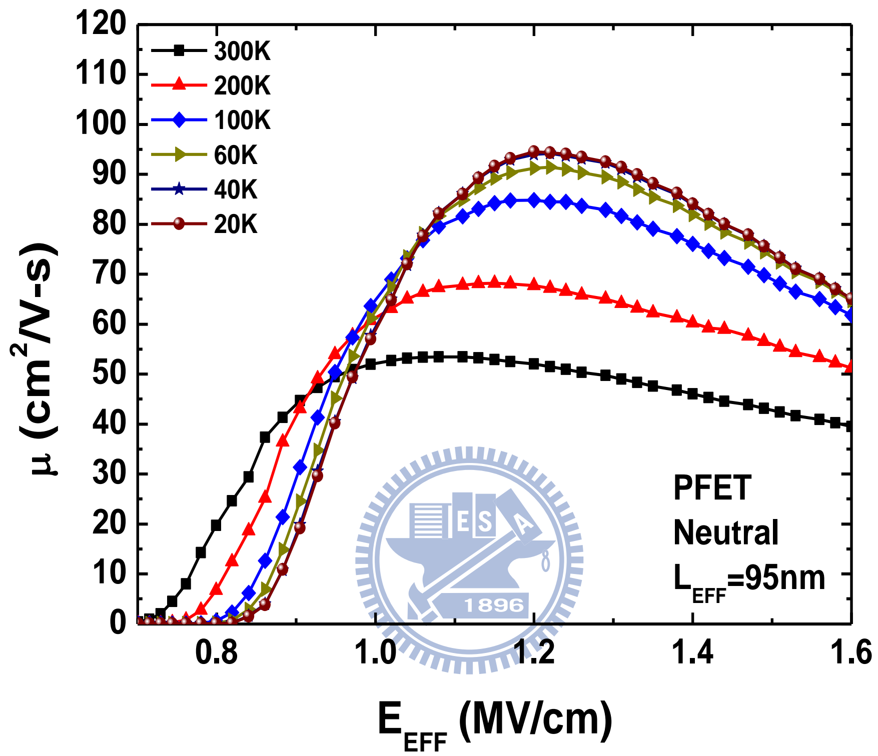


Figure 4.4. Extracted carrier mobility versus vertical electric field under various temperatures.

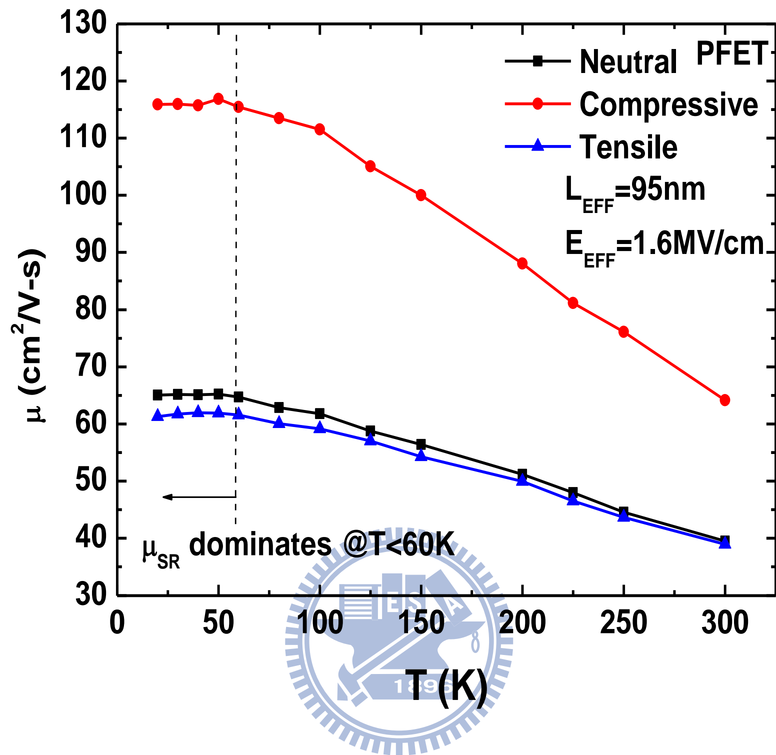


Figure 4.5. Extracted carrier mobility at E_{EFF}=1.6MV/cm with various stressors. μ_{SR} dominates the total mobility for temperature <60K.

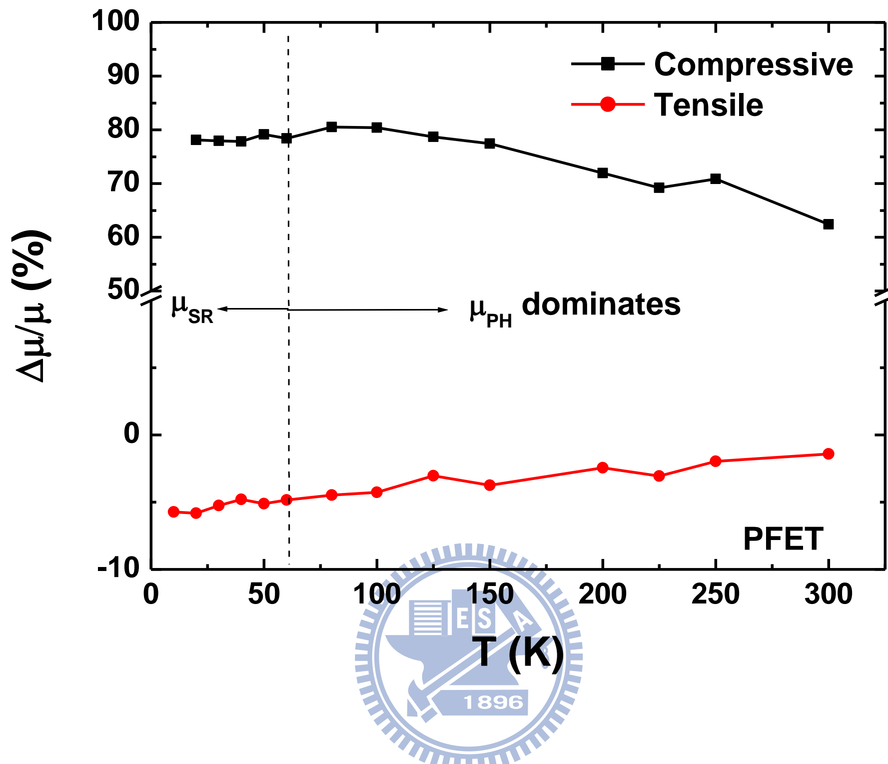


Figure 4.6. Mobility enhancement percentage ($\Delta\mu/\mu$) versus temperature with compressive and tensile stressors.

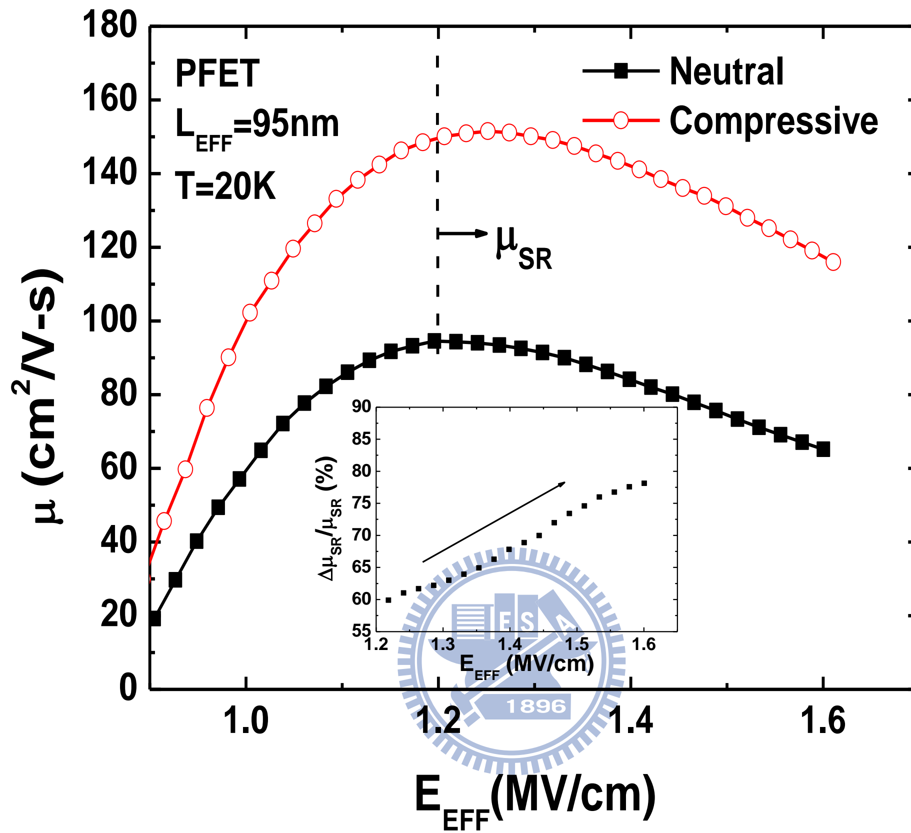


Figure 4.7. Extracted carrier mobility versus vertical electric field at 20K for the neutral and compressive stressors. Inset: The surface roughness mobility enhancement increases as E_{EFF} increases.

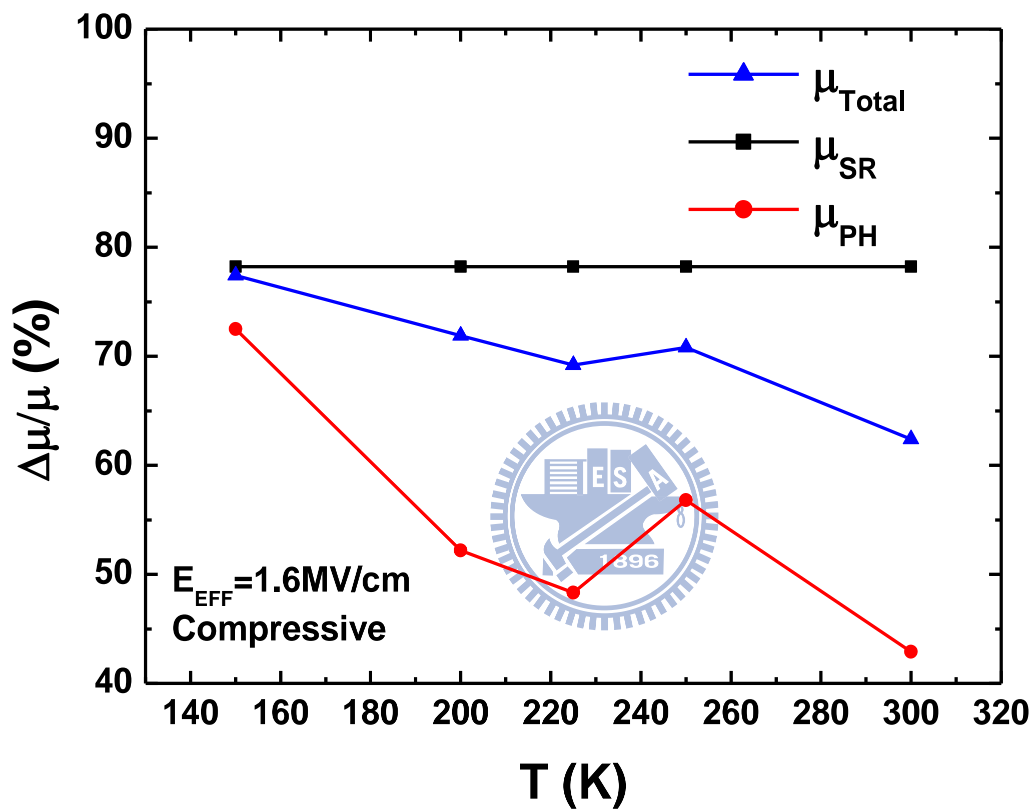


Figure 4.8. The dissection of mobility enhancement versus temperature with different scattering mechanisms.

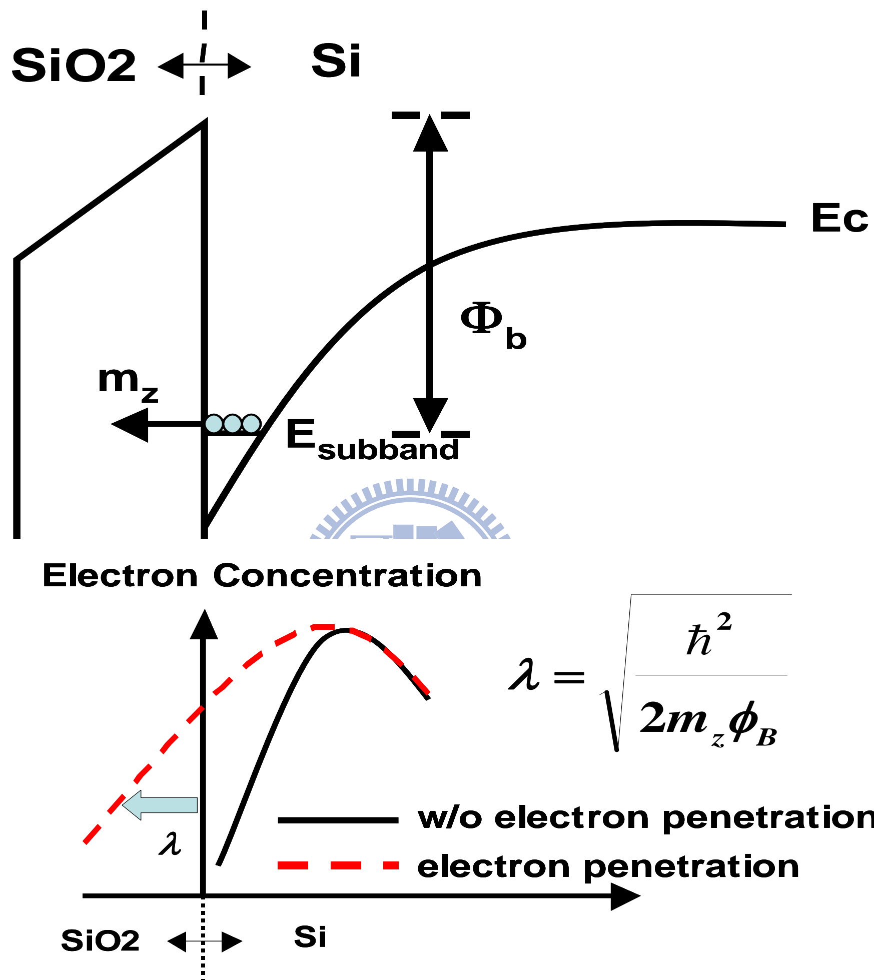


Figure 4.9. Electron wavefunction penetration into gate dielectric. m_z is out-of plane effective mass; Φ_b is Si/SiO_2 potential barrier height; λ is electron attenuation length. Longer λ causes more surface roughness scattering. [9]

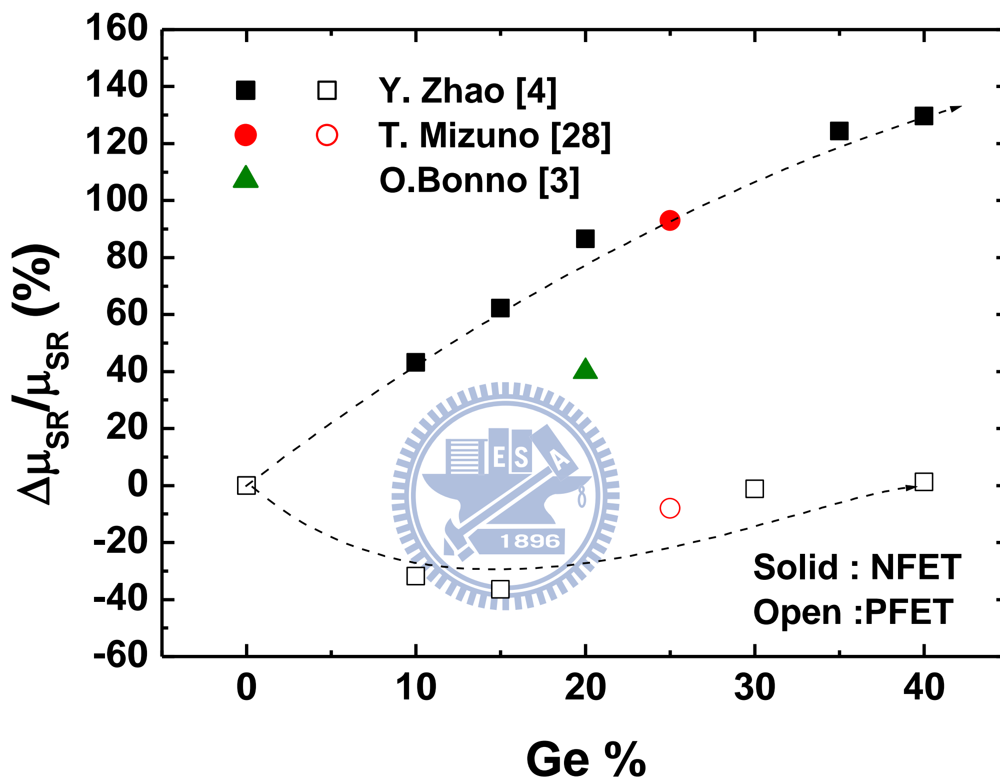


Figure 4.10. $\Delta\mu_{SR}/\mu_{SR}$ by biaxial strain extracted from the literature [3,4,28].

NFET
Biaxial

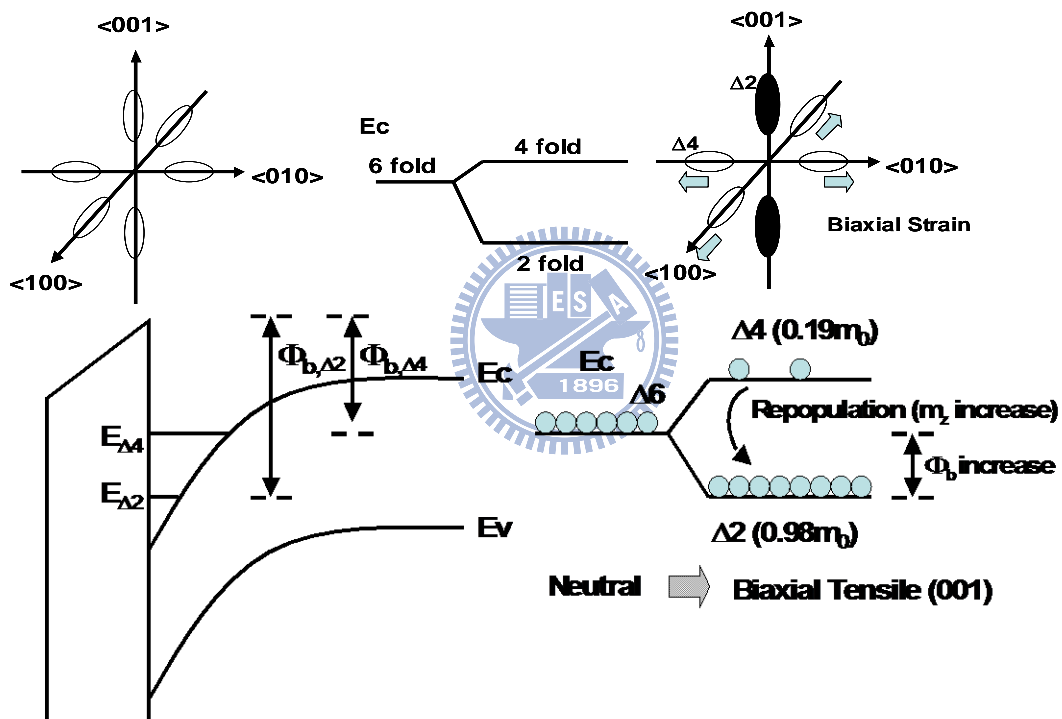


Figure 4.11. NFET energy band diagram and electron repopulations showing that most electrons repopulate into Δ2 valley under biaxial tensile stress. It may result in higher Φ_b [24-27], heavier m_z [24-27], shorter λ and thus larger μ_{SR} .

NFET
Uniaxial

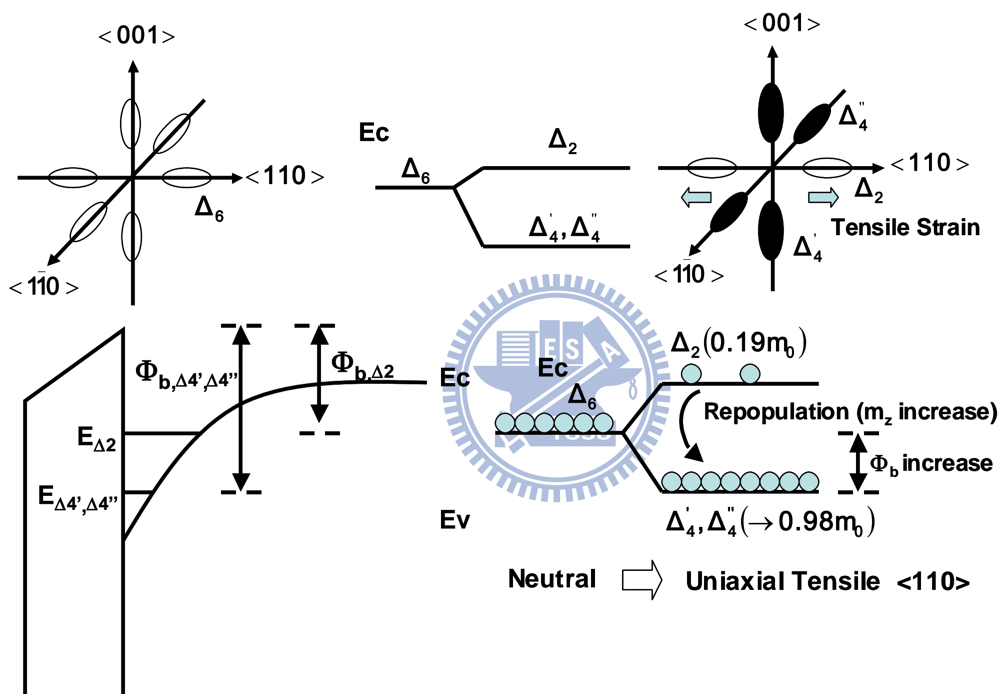


Figure 4.12. NFET energy band diagram and electron repopulations showing that most electrons repopulate into Δ4' and Δ4" valley under uniaxial tensile stress. It may result in higher Φ_b, heavier m_z, shorter λ and thus larger μ_{SR} .

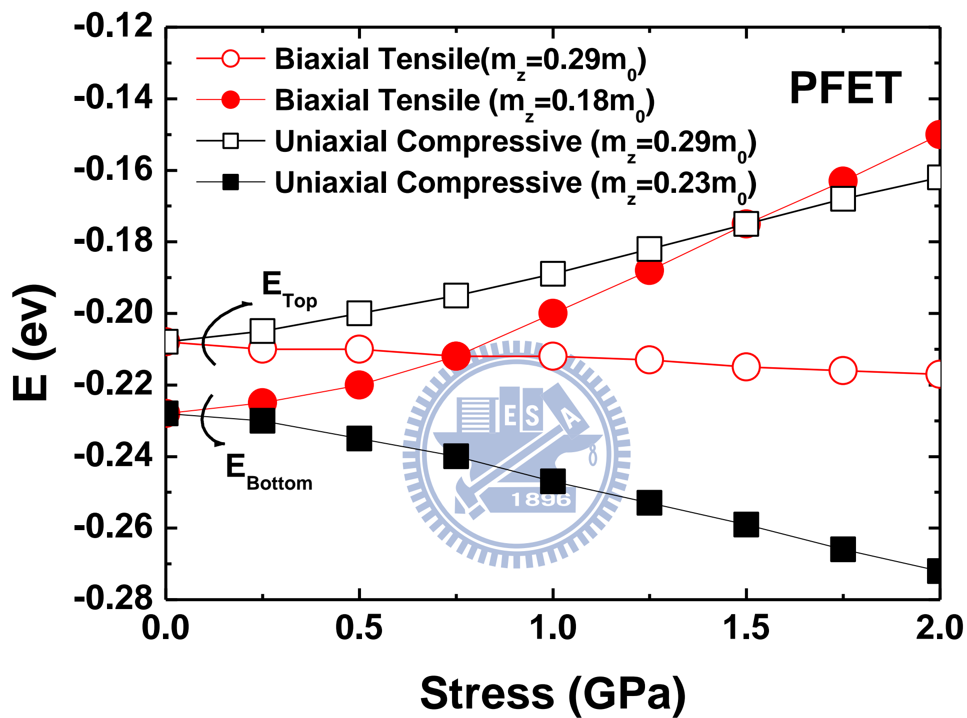


Figure 4.13. Hole subband versus different stress levels [2,24]. Uniaxial compressive and biaxial tensile have different subband splitting behavior. Zero energy represents the band edge of valence band.

PFET
Uniaxial vs Biaxial

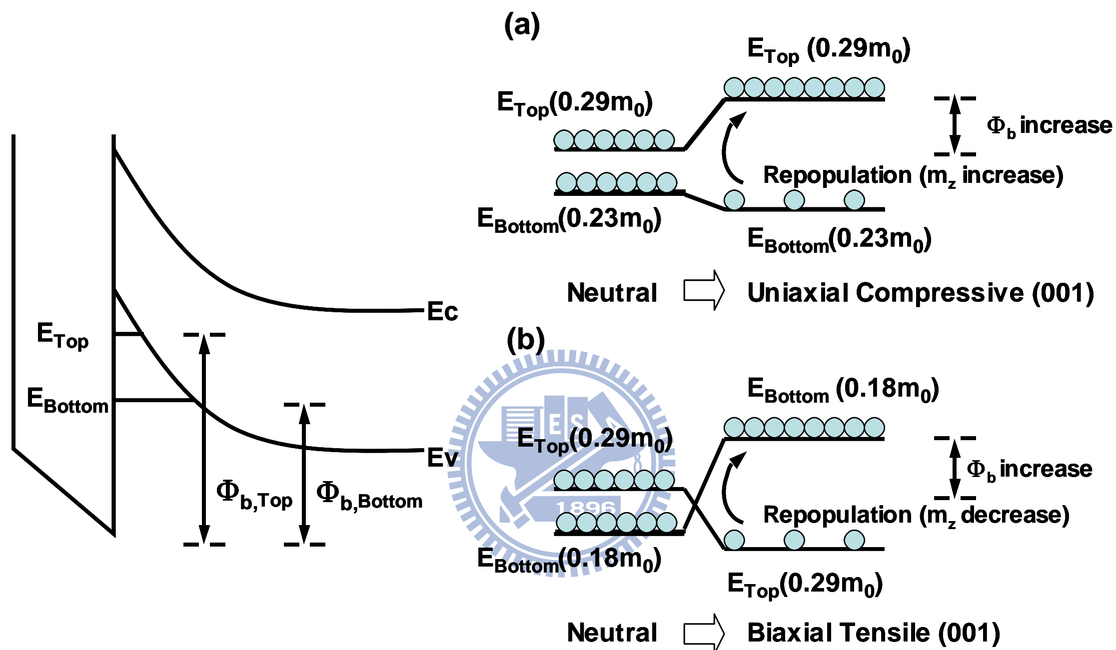


Figure 4.14. PFET energy band diagram and hole repopulations with uniaxial compressive stress and biaxial tensile stress. Subband energy levels are engineered with different stress types and most of hole carriers repopulate into the lower subband. (a) Uniaxial compressive stress increases m_z and Φ_b. Both factors improve λ and then μ_{SR}. (b) In the case of biaxial tensile stress, when the Ge percentage is increased, the λ is initially increased by lighter m_z but soon recovered due to higher Φ_b at high stress levels.

Stressor	Index	NFET	PFET
Biaxial-Tensile [3,4]	m_z	↗	↘
	Φ_b	↗	↗
	λ	↘	lower σ : ↗ stronger σ : ↘
	μ_{SR}	↗	lower σ : ↘ stronger σ : ↗
Uniaxial-Tensile	m_z	↗	↘
	Φ_b	↗	↘
	λ	↘	↗
	μ_{SR}	↗	↘
Uniaxial-Compressive [This work]	m_z	↘	↗
	Φ_b	↘	↗
	λ	↗	↘
	μ_{SR}	↘	↗

Table 4.1. Summary of stress sensitivity to out-of-plane effective mass (m_z) [8-12], barrier height (Φ_b) [8-12], electron attenuation length (λ) and surface roughness scattering limited mobility (μ_{SR}).

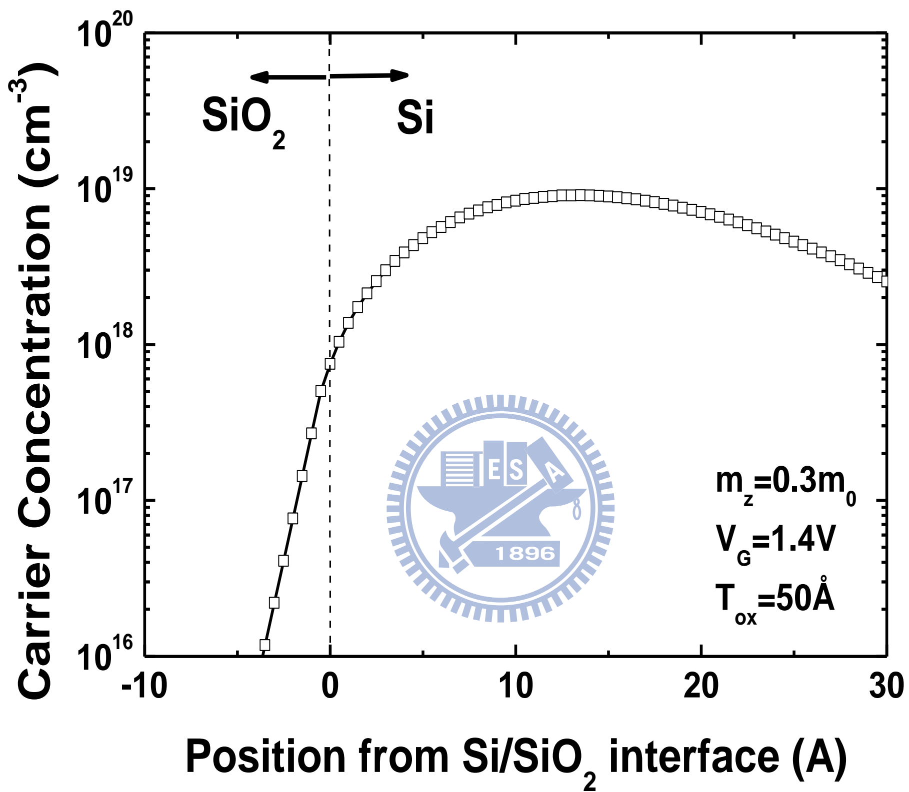


Figure 4.15. Wavefunction penetration into gate dielectric.

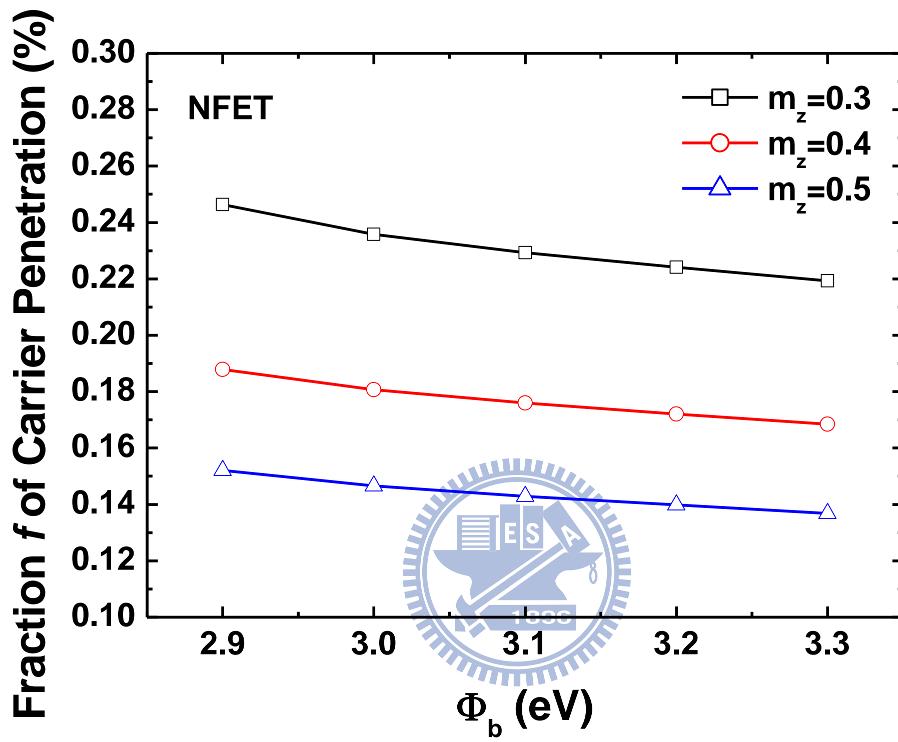


Figure 4.16. Higher Φ_b and heavier m_z show lower fraction f of carrier penetration from 1D QM simulations. It is consistent with uniaxial-Tensile NFET in Table 4.1.

Chapter 5

Impact of Uniaxial Strain on the Temperature Dependence of Carrier Mobility in Nanoscale p-MOSFETs

5.1 Introduction

Uniaxial strained-Si technology is crucial to transistor performance in state-of-the-art CMOS development [1-3]. The temperature effect on strain-enhanced mobility is of special importance because it may provide insights for the underlying mechanisms responsible for the performance enhancement. Several studies have investigated the temperature effect on strain-enhanced mobility in the past [4-7]. For NMOS, the temperature effect of process-induced biaxial strain [4,5], uniaxial strain [4] and mechanical uniaxial strain [6] applied on devices has been experimentally studied. The results all indicated less strain sensitivity in carrier mobility with decreasing temperature. For PMOS, the temperature effect of process-induced biaxial strain [5] and mechanical uniaxial strain [7] has also been investigated. The results showed higher strain sensitivity in carrier mobility with decreasing temperature, i.e., the opposite trend with NMOS. However, the temperature effect of process-induced uniaxial strain in nanoscale PMOS devices is still not reported and merits investigation. Moreover, recently several studies have reported that the temperature sensitivity of drain current for PMOSFETs increases by uniaxially-compressive strain [8-9,20-22]. In addition, the carrier scattering mechanism in the strained PMOS devices becomes more phonon-limited [8-9,20-22]. However, the underlying mechanism is still no clear and merits investigation.

In this work, we conduct an experimental assessment for the impact of process-induced uniaxial strain on the temperature dependency of carrier mobility in nanoscale pMOSFETs [8]. Furthermore, through cryogenic temperature measurement to decouple the surface roughness limited mobility (μ_{SR}) and the phonon-scattering limited mobility (μ_{PH}), we investigate the impact of uniaxial strain on the temperature dependence of phonon-scattering limited mobility in nanoscale PMOSFETs [9].

5.2 Experimental Setup

PMOSFETs with channel direction <110> with neutral, tensile and compressive uniaxial Contact Etch Stop Layer (CESL) were manufactured based on state-of-the-art CMOS technology on 300mm (100) silicon substrate [10,11]. Shallow Trench Isolation (STI) was patterned to define the active region. A uniform channel doping was implanted to define the PMOS devices and maintain reasonable threshold voltage. Then an ultra thin nitride oxide was grown on the surface of wafer. The poly gate was implanted with heavily doped P+ species and post annealed to increase the gate activation rates. Then the ultra shallow HDD (Highly Doped Drain) implant, spacer formation, source and drain implant, post implantation annealing, and back-end process were implemented sequentially. The effective channel doping is around 2×10^{18} cm^{-3} for short channel devices based on TCAD simulation. The equivalent oxide thickness is about 17Å . For comparison purpose, nitride films with neutral, compressive and tensile stress were deposited on pMOSFETs at the CESL deposition stage.

Since external resistance (R_{sd}) is crucial to the short channel mobility extraction [12,13], the intrinsic drain current (I_D) was calibrated by considering the series-resistance effect [14]. The physical poly gate length (L_{phy}) was obtained using in-line SEM measurement. The LDD overlap region under the gate (L_{ov}) was extracted by the split CV method [15]. The effective channel length (L_{EFF}) can then be derived by

subtracting L_{ov} from L_{phy}. Finally, the mobility for short channel devices can be determined [10]. In order to decouple the surface roughness mobility (μ_{SR}) and the phonon scattering limited mobility (μ_{PH}), cryogenic temperature measurements were carried out using liquid He as cooling source. The measurement temperature ranged from 20K to 300K. HP4156 and HP4285 were adopted to measure the transistor IV and CV characteristics.

5.3 Results and Discussion

Fig. 5.1 shows the drain current (I_D) versus gate voltage characteristics at various temperatures for the PMOS devices under test. The drain current shows strong correlation with stressor types, and can be explained by the extracted carrier mobility as shown in Fig. 5.2. It can be seen from Fig. 5.2 that the short-channel mobility in PMOS (L_{EFF}=95nm) shows significant dependence on the uniaxial strain. The PMOS mobility prefers compressive stress because of the strain-reduced conductivity effective mass [11].

Also shown in Fig. 5.2 is that the mobility is degraded when temperature increases in the high vertical field region, where phonon scattering is important [16,17]. Moreover, the temperature dependence of mobility shows strong sensitivity to strain. In other words, as the mobility is enhanced by compressive strain, its temperature dependence also increases. The root cause will be discussed later.

Fig. 5.3 shows the temperature sensitivity ($\log\mu/\log T$) of hole mobility versus the vertical effective electric field (E_{EFF}). For a given stressor, it can be seen that the temperature sensitivity increases (i.e., more negative) and then saturates as E_{EFF} increases. More importantly, the $\log\mu/\log T$ for the PFET under compressive strain is the highest in absolute value among the three stressors. In other words, the scattering mechanism of PMOS device becomes more phonon-limited [16,17] under compressive

strain. This also explains why the temperature sensitivity of drain current for the compressively-strained PFET is the largest among the three stressors, as shown in Fig. 5.1.

Fig. 5.4 shows the hole mobility enhancement ($\Delta\mu/\mu$) versus temperature at E_{EFF}=1.5MV/cm. It shows that for both compressive and tensile stressors, the magnitude of $\Delta\mu/\mu$ decreases as temperature increases. Our result from process-induced uniaxial stressors is consistent with the study in [7], in which an external compressive uniaxial mechanical stress was applied.

Based on the model proposed in [7], it is plausible that as temperature increases, the compressively-strained PFET has less holes to populate states near the band edge where the conductivity effective mass along the channel direction is smaller. Therefore, the observed mobility enhancement decreases with increasing temperature.

In order to explain why the scattering mechanism of PMOS device becomes more phonon-limited under compressive strain, cryogenic temperature measurements were carried out to decouple μ_{PH} and μ_{SR}. Fig. 5.5 shows the measured carrier mobility under compressive and neutral uniaxial strain with temperature ranging from 20K to 60K. It is known that the phonon scattering mechanism is fully suppressed and the surface roughness scattering mechanism may dominate within this temperature range (especially for E_{EFF}>1.3MV/cm). It can be seen that the μ_{SR} shows little temperature dependence, which is consistent with the reported data in the past [17,18].

In order to extract the phonon scattering limited mobility (μ_{PH}), it is assumed that the μ_{SR} is independent of temperature [17,18], and then the Matthiessen's rule can be adopted:

$$\mu_{PH}^{-1}(T) = \mu_{Total}^{-1}(T) - \mu_{SR}^{-1}(T = 20K) \quad (1)$$

where μ_{Total} is the total mobility including Coulomb, phonon, and surface roughness scattering mechanisms, and μ_{SR} (20K) is the surface roughness mobility at E_{EFF} larger than 1.3MV/cm. Fig. 5.6 shows the extracted μ_{PH} at 300K, 250K and 225K for neutral stressors. It can be seen that the μ_{PH} increases when temperature is decreased because of decreased phonon scattering rate [17].

Fig. 5.7 and Fig. 5.8 show the E_{EFF} dependence of μ_{SR} and μ_{PH}. The extracted μ_{SR} and μ_{PH} are proportional to $E_{EFF}^{-1.3}$ and $E_{EFF}^{-0.3}$, respectively, which is consistent with the reported data in the past [17,18]. Fig. 5.9 shows the temperature dependences of μ_{PH} ($\mu_{PH} \propto T^{-\alpha}$) versus E_{EFF} for neutral and compressive stressors. It can be seen that the α is close to 1.75 for the neutral stressor, which is consistent with the reported data in the literature [17]. It also shows that, with compressive uniaxial strain, the temperature sensitivity of μ_{PH} is increased ($\alpha \approx 2.3$).

Note that although the α is determined by both acoustic and optical phonon scattering mechanisms, the impact of uniaxial strain lies mainly in the optical phonon scattering [11]. Fig. 5.10 (a) and (b) show the empirical temperature dependence of acoustic and optical phonon scattering mobility for both NFET and PFET, respectively [19]. Phonon temperature sensitivity should range from –1.5 to –3.13 for NFET and from –1.5 to –3.25 for PFET [19]. Moreover, Fig. 5.10 (a) and (b) both show that optical phonon mobility dominates in the total phonon mobility at room temperature. Therefore, it is reasonable to investigate the strain impact on the temperature dependence of phonon mobility from the optical phonon scattering mechanism. To explain the strain dependence of α in Fig. 5.9, the optical-phonon limited mobility can be expressed as Eq. (2) [19]:

$$\mu_o = A_o T^{-\frac{1}{2}} e^{\frac{\hbar\omega_o}{kT}} \tag{2}$$

where μ_o is the optical phonon mobility, A_o is a constant, T is the temperature, k is the Boltzmann constant; and $\hbar\omega_o$ represents the optical phonon energy. Eq. (2) indicates that the temperature sensitivity of the optical phonon mobility depends on the optical phonon energy ($\hbar\omega_o$).

In order to derive the formula of the temperature dependence of optical phonon mobility, the logarithm of μ_o needs to be obtained as Eq. (3):

$$\log \mu_o = \log\left(A_o T^{-\frac{1}{2}} e^{\frac{\hbar\omega_o}{kT}} \right) = \log A_o - \frac{1}{2}\log T + \frac{\hbar\omega_o}{kT}\log(e) \tag{3}$$

Then take the differentiation of Eq. (3) with respect to temperature as Eq. (4):

$$\frac{\delta \log \mu_o}{\delta \log T} = -\frac{1}{2} + \frac{\hbar\omega_o}{k}\log(e) \times \frac{\delta(T^{-1})}{\delta \log T} = -\frac{1}{2} + \frac{\hbar\omega_o}{k}\log(e) \times \frac{\delta(T^{-1})}{\delta T} \times \frac{\delta T}{\delta \log T} \tag{4}$$

Set x=log T and based on the derivative of Exponential function ($\frac{\partial}{\partial x} a^x = \ln(a) a^x$), then Eq. (5) is obtained:

$$\frac{\delta T}{\delta \log T} = \frac{\delta 10^x}{\delta x} = \ln(10) \times 10^x = \ln(10) \times T \tag{5}$$

Feedback the result of Eq. (5) into Eq. (4) and Eq. (6) is derived:

$$\frac{\delta \log \mu_o}{\delta \log T} = -0.5 + \frac{\hbar\omega_o}{k}\log(e) \times (-)T^{-2} \times \ln(10) \times T = -0.5 - \frac{\hbar\omega_o}{kT} \tag{6}$$

From Eq. (6), it shows that the temperature sensitivity depends on the optical phonon energy ($\hbar\omega_o$). Higher $\hbar\omega_o$ shows stronger temperature sensitivity of optical phonon scattering limited mobility.

The schematic plot of E-k band diagram in Fig. 5.11 shows the impact of uniaxial compressive strain on $\hbar\omega_o$. The strain induces the light-hole (LH) and heavy hole (HH) band-split and most of the holes repopulate into the light hole band [11]. In other words, the $\hbar\omega_o$ is increased due to band splitting as the compressive strain is applied. Therefore the α value is increased (Fig. 5.9) for the compressively-strained PMOSFETs.

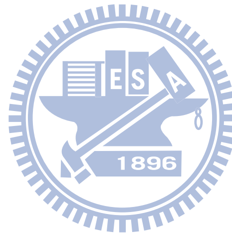
From previous reports [8,20-22], it has been found that the temperature sensitivity of drain current for the compressively-strained PFET is larger than that of the unstrained counterpart. Furthermore, the scattering mechanism in PMOS devices is more phonon-limited [8,20-22] under compressive strain. Our new finding in this work [9], the strain-enhanced temperature sensitivity of μ_{PH}, has unveiled the underlying mechanism responsible for these observations. It also provides insights for future mobility scaling using advanced strain technologies.

5.4 Conclusion

We have investigated the temperature dependency of mobility for advanced short-channel strained PMOS devices. By accurate split-CV mobility extraction under various temperatures, we examine the impact of process-induced uniaxial strain on the temperature dependence of mobility and mobility enhancement in nanoscale pMOSFETs. Our study indicates that the strain sensitivity of hole mobility becomes less with increasing temperature and it is consistent with previous uniaxial mechanical bending result. It is because the hole repopulations at energy band edge induce less strain sensitivity as temperature increases. Furthermore, the carrier scattering mechanism for the PMOSFET under uniaxial compressive strain tends to be more

phonon-limited at a given vertical electric field, which explains the larger drain current sensitivity to temperature present in the compressively-strained PFET.

Through cryogenic temperature measurement, the extracted μ_{SR} and μ_{PH} are proportional to $E_{EFF}^{-1.3}$ and $E_{EFF}^{-0.3}$, respectively, which is consistent with the reported data in the literature. The temperature sensitivity of phonon mobility is proportional to $T^{-1.75}$ for neutral stressor and becomes higher when compressive strain is applied. It can be explained by the higher optical phonon energy induced by uniaxially-compressive strain. Our new findings also explain the higher temperature sensitivity of drain current presented in uniaxial strain PMOSFETs.



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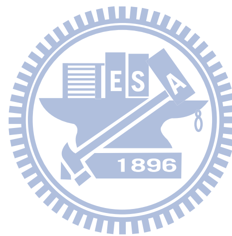


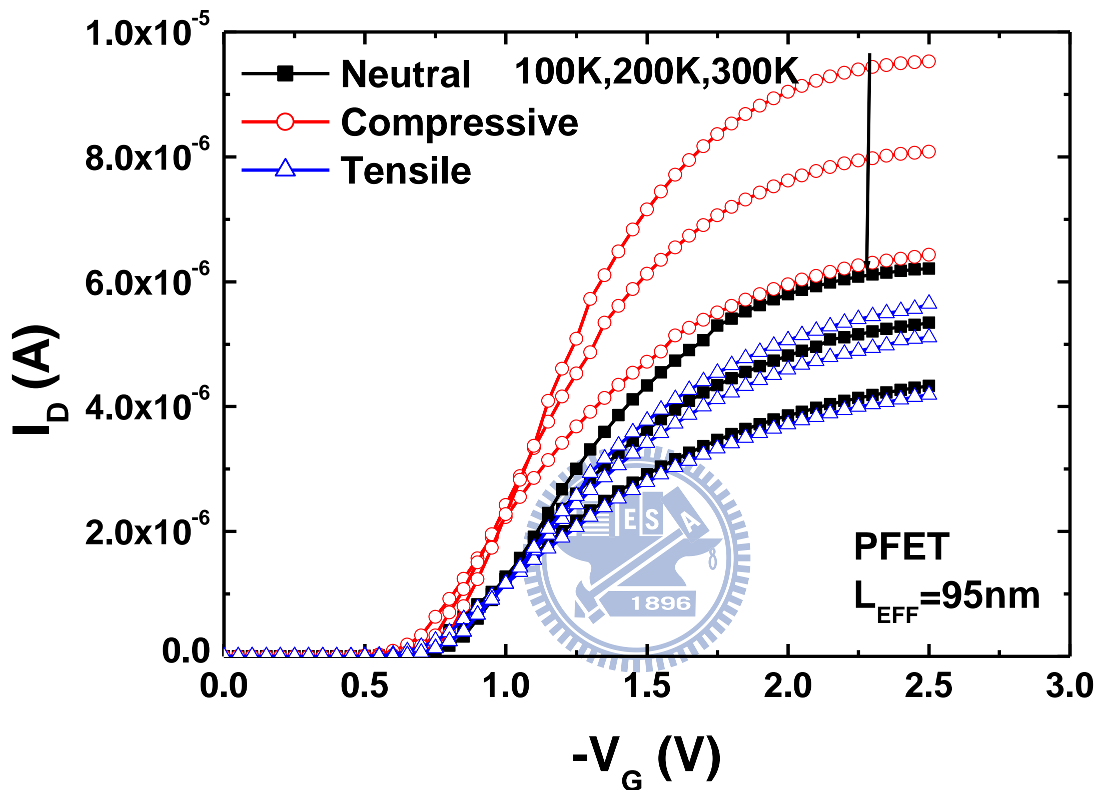


Figure 5.1. Drain current versus gate voltage at various temperatures for PFETs with various stressors. The drain bias (V_{DS}) is –5mV. The temperature dependence of drain current shows strong correlation with stressor types.

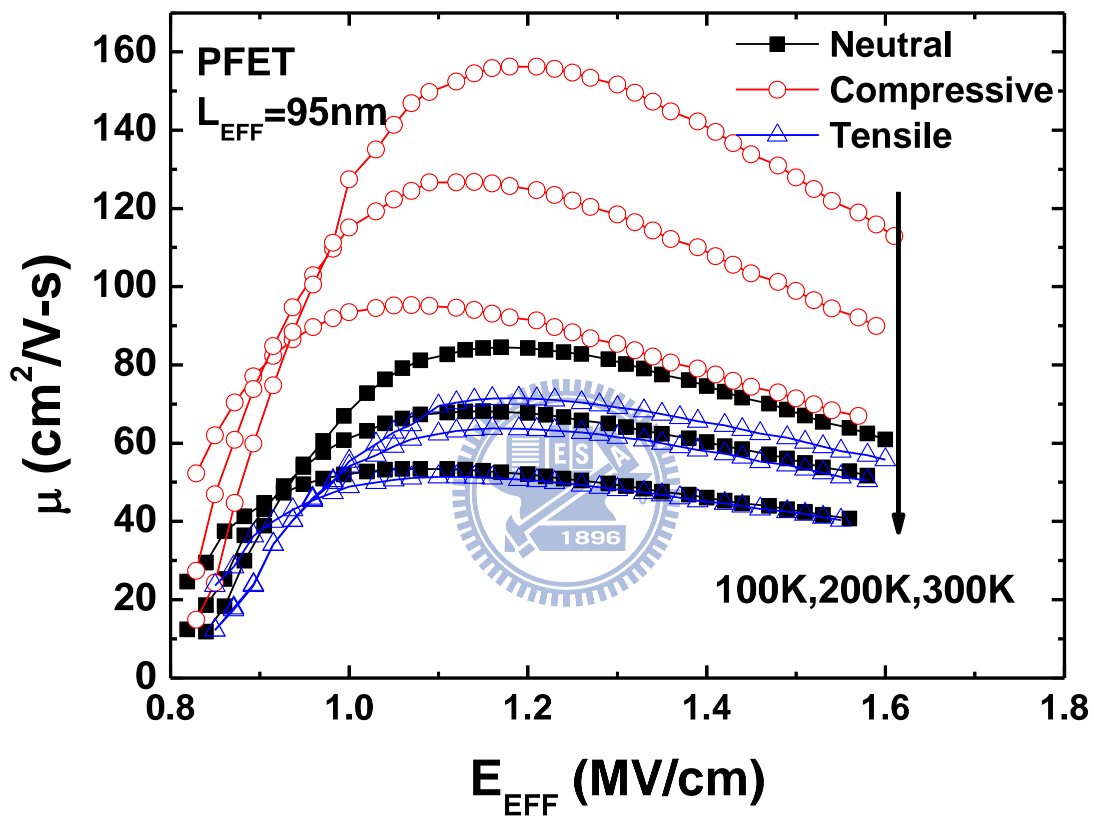


Figure 5.2. The extracted carrier mobility shows significant dependence on the uniaxial stressor.

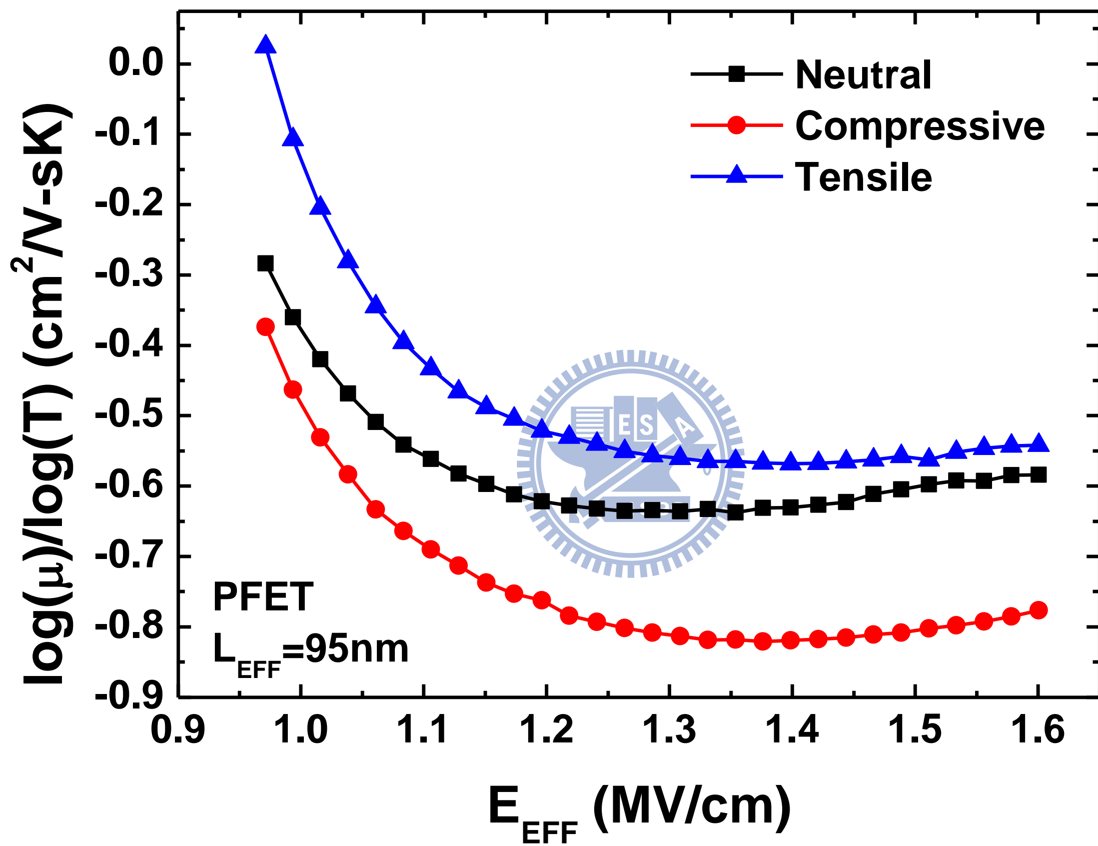


Figure 5.3. Temperature sensitivity of hole mobility vs. the vertical field for various uniaxial stressors.

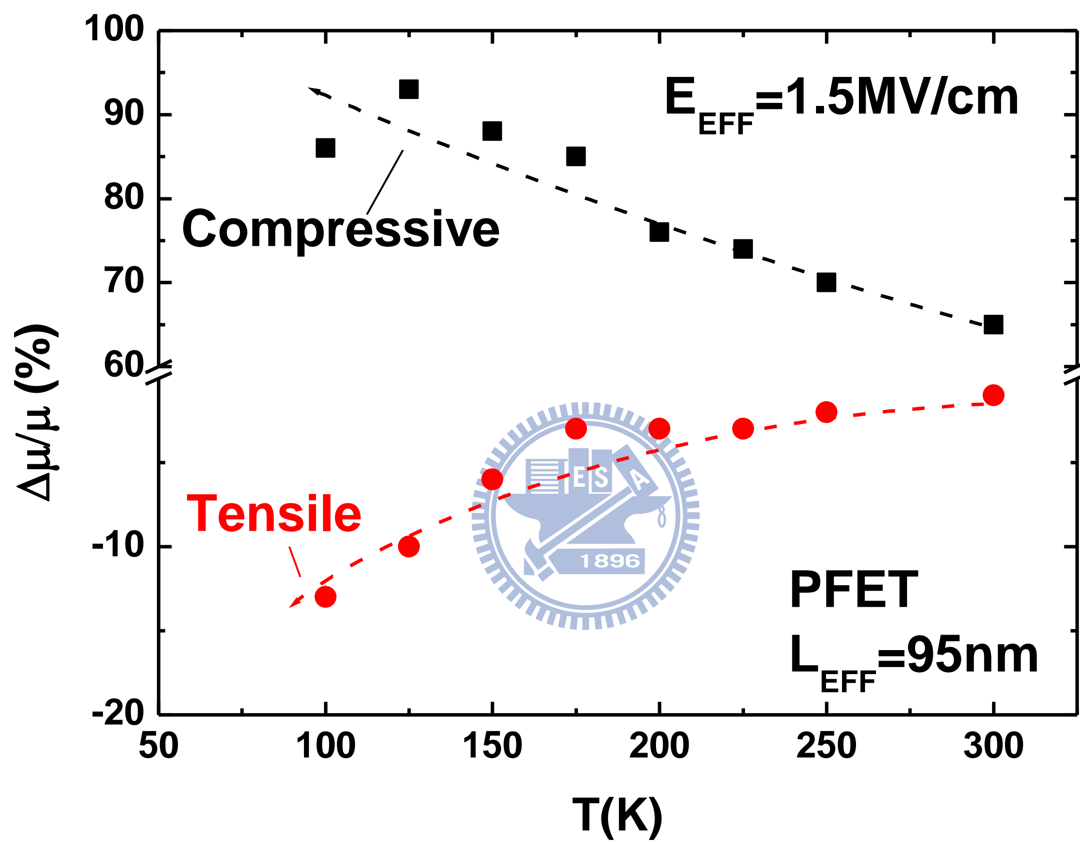


Figure 5.4. Hole mobility enhancement versus temperature at E_{EFF}=1.5MV/cm for PMOS devices with various stressors.

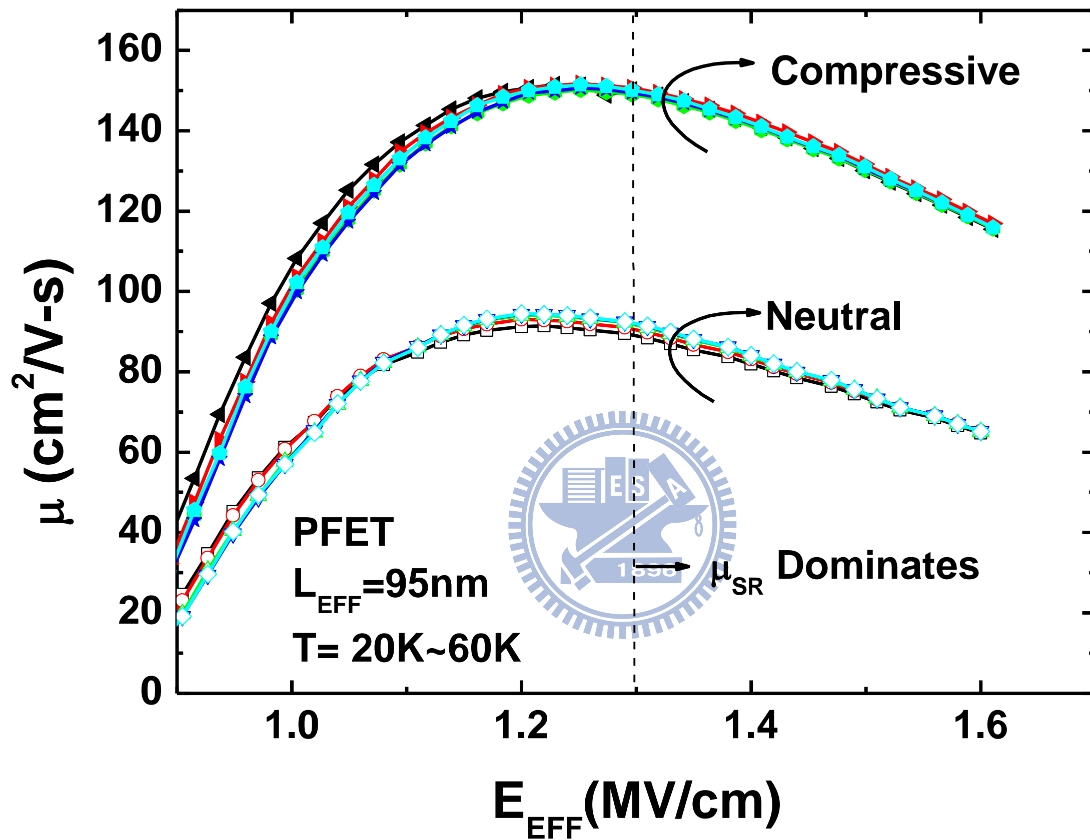


Figure 5.5. The measured total mobility with temperature ranging from 20K to 60K for neutral and compressive uniaxial stressors. The surface roughness mobility (μ_{SR}) tends to dominate as E_{EFF}>1.3MV/cm and is independent of temperature.

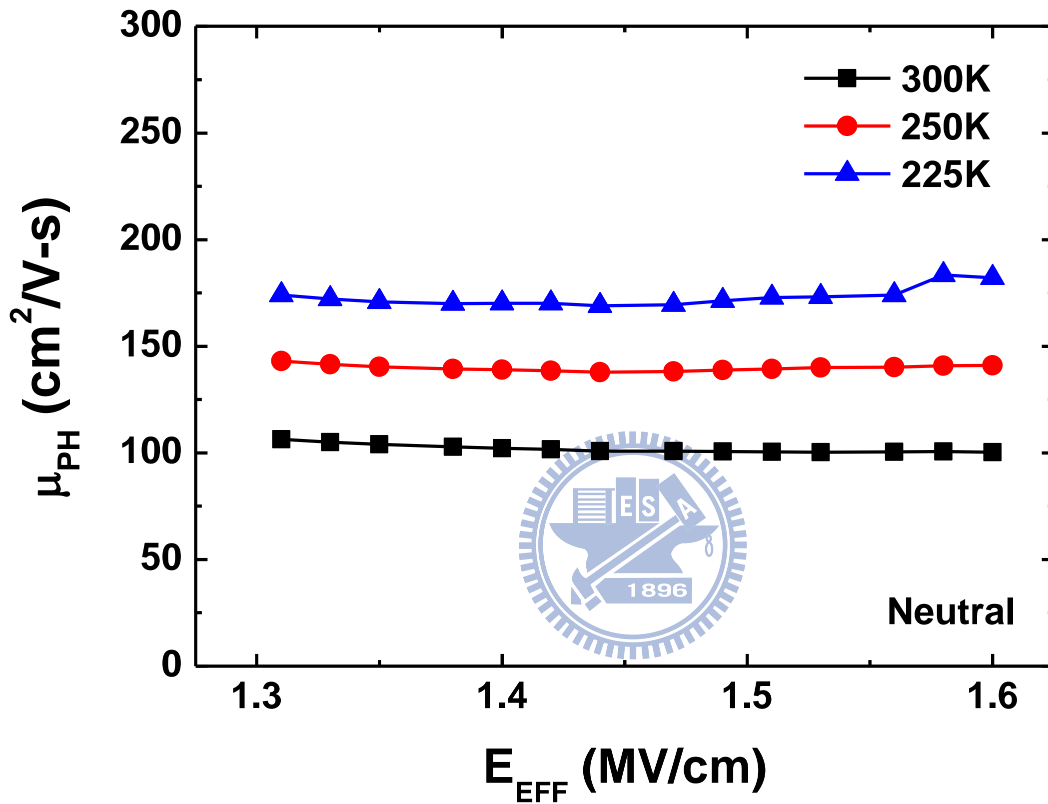


Figure 5.6. The extracted phonon scattering limited mobility for neutral and compressive stressors at T=225K, 250K and 300K, respectively.

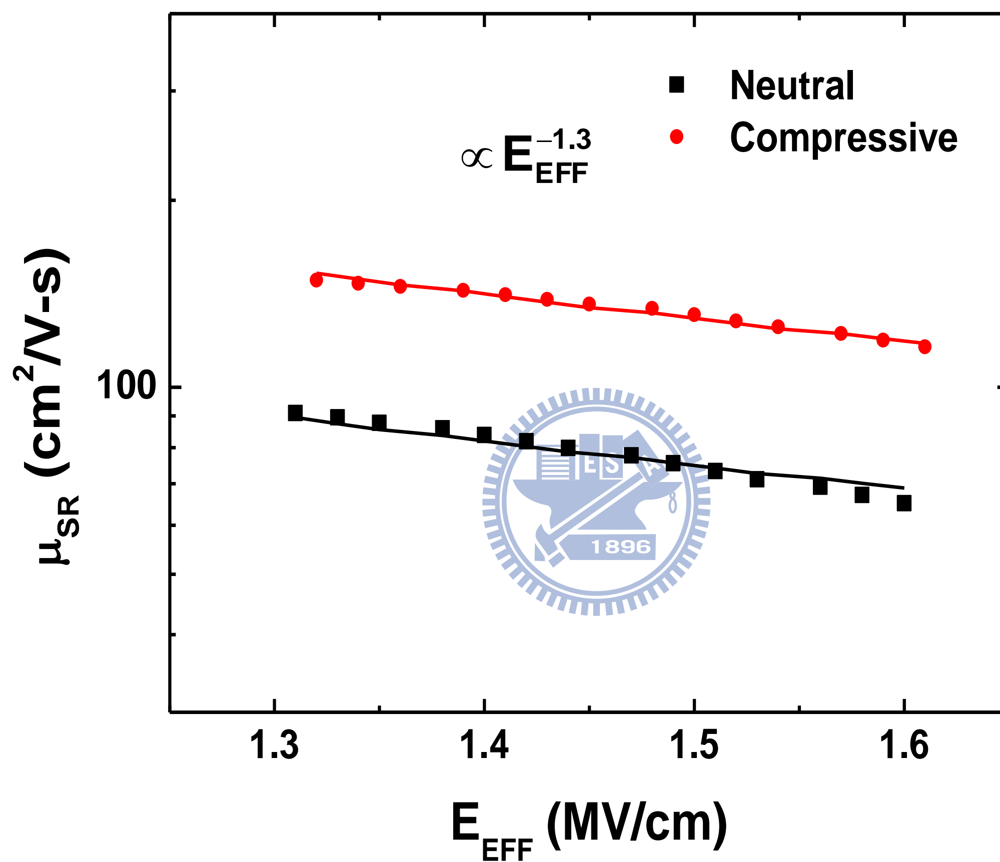


Figure 5.7. The E_{EFF} dependence of μ_{SR}. The extracted μ_{SR} is proportional to $E_{EFF}^{-1.3}$.

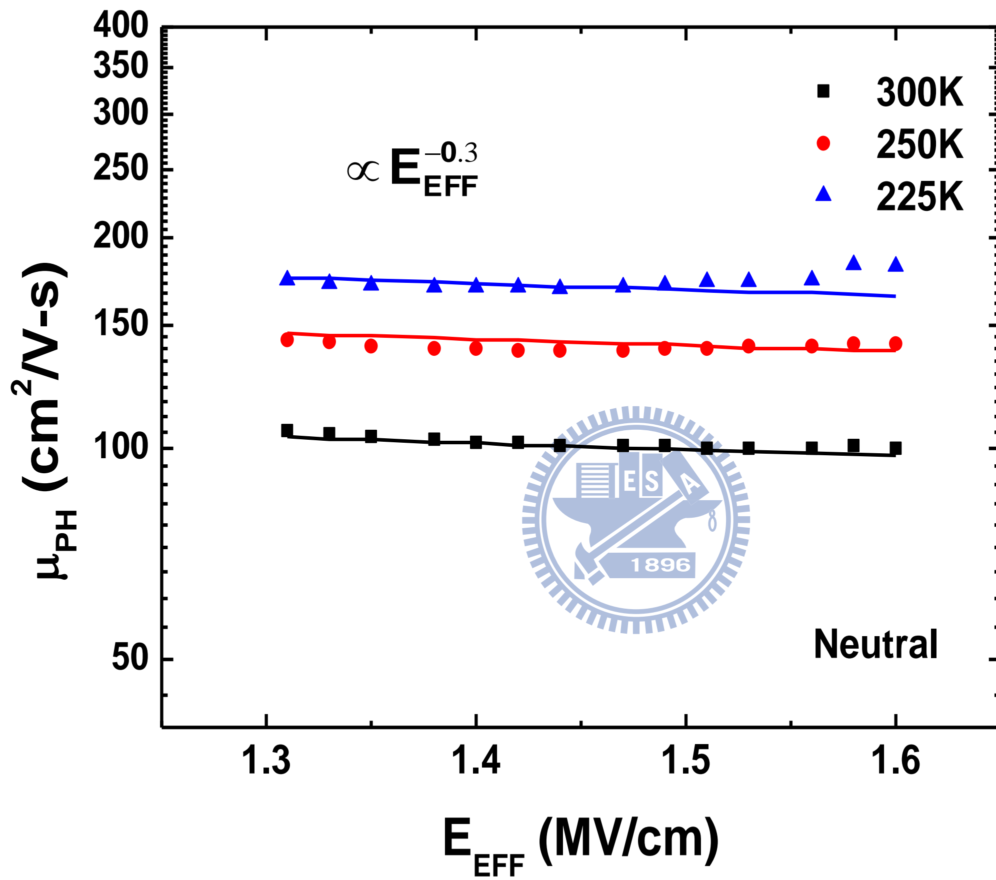


Figure 5.8. The E_{EFF} dependence of μ_{PH}. The extracted μ_{PH} is proportional to $E_{EFF}^{-0.3}$.

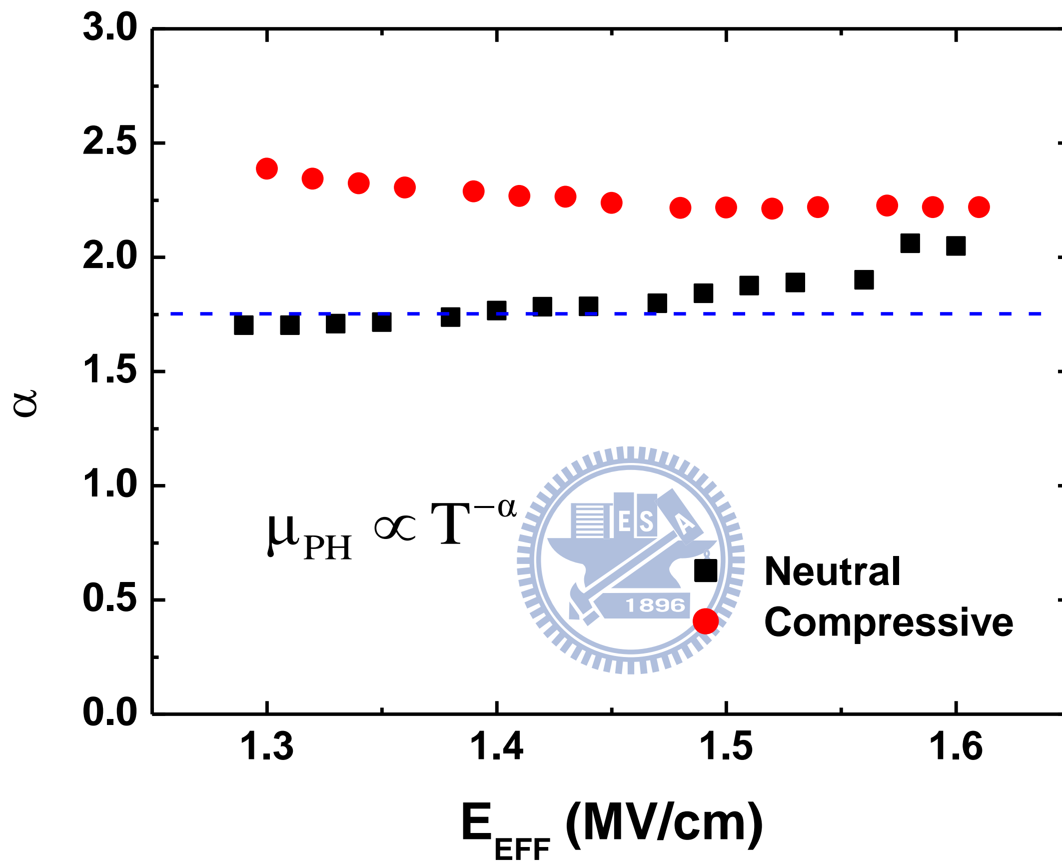
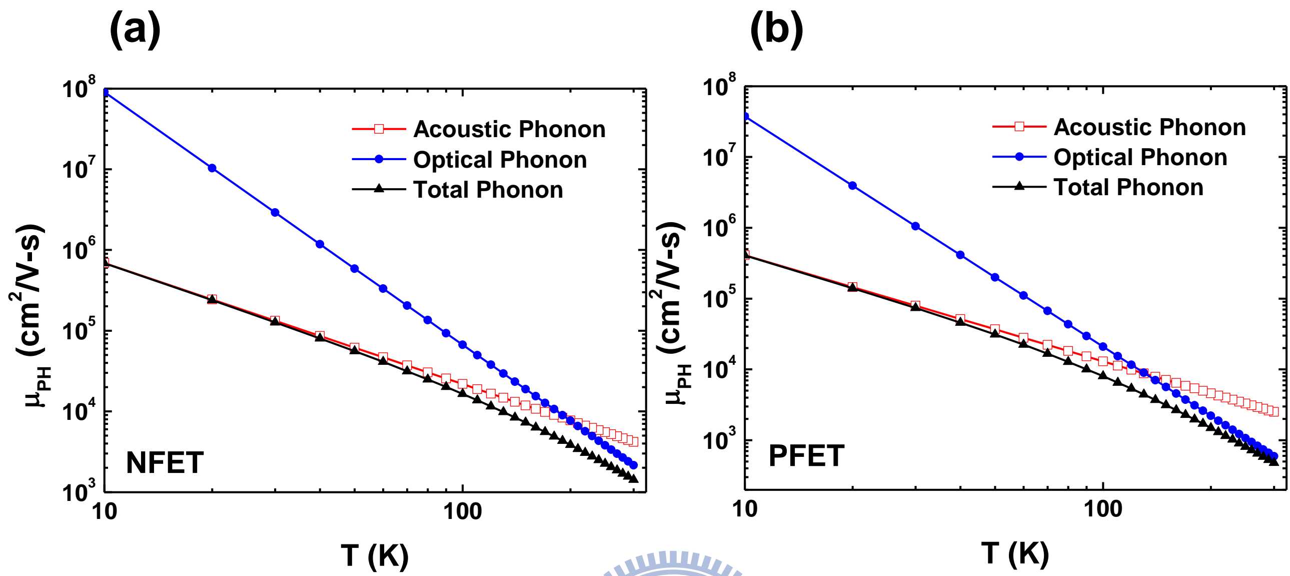


Figure 5.9. Temperature dependence of μ_{PH} ($T^{-\alpha}$) for neutral and compressive stressors. The α of neutral stressor is close to 1.75 [17], while the compressive stressor may further enhance the α value to around 2.3.



	Electrons	Holes
μ_A	$2.18\text{x}10^{7}T^{-1.5}$	$1.30\text{x}10^{7}T^{-1.5}$
μ_O	$1.22\text{x}10^{11}T^{-3.13}$	$6.64\text{x}10^{10}T^{-3.25}$

Figure 5.10. Phonon temperature sensitivity should range from –1.5 to –3.13 for NFET and from –1.5 to –3.25 for PFET from empirical number [19]. Optical Phonon mobility dominates in the total phonon mobility at room temperature.

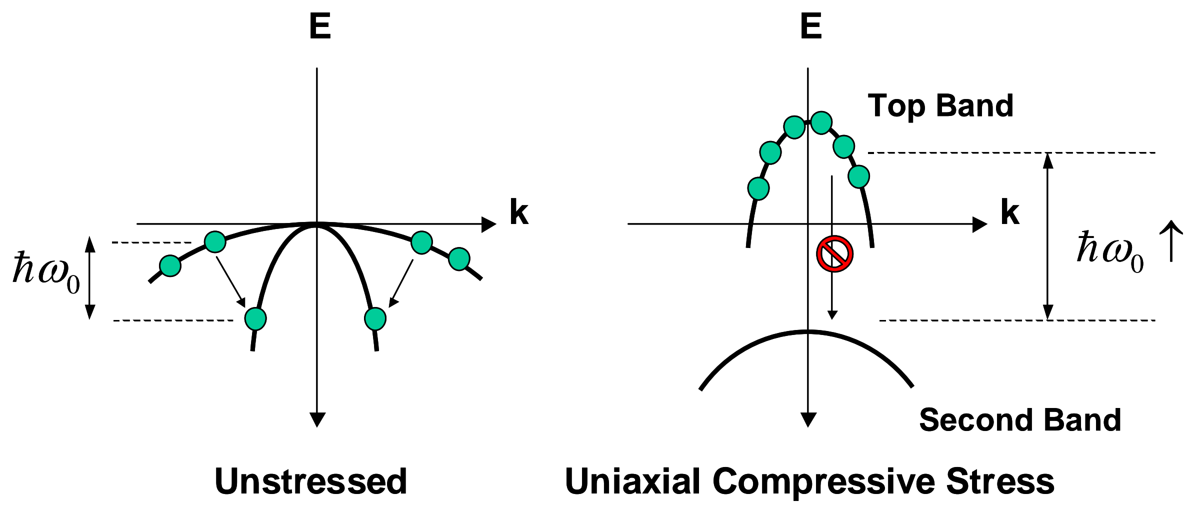


Figure 5.11. Schematic plot of E-k energy band diagram under uniaxial compressive stressor in PFET. Optical phonon energy ($\hbar\omega_o$) may increase when compressive uniaxial strain is applied.

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Chapter 6

Conclusion

In this dissertation, we systematically investigate the impact of process-induced uniaxial strain on the carrier mobility considering various scattering mechanisms. First, we introduce a BSIM-based R_{sd} extraction method and split CV method to extract short channel mobility [1,2]. Then the uniaxial strain dependence of Coulomb mobility is experimentally investigated for both nMOSFETs and pMOSFETs [3-4]. In addition, through cryogenic temperature measurement, the uniaxial strain dependence of surface roughness mobility (μ_{SR}) for pMOSFETs is also studied [5]. By decoupling μ_{SR} and phonon scattering limited mobility (μ_{PH}), we examine the impact of uniaxial strain on the temperature dependence of μ_{PH} [6,7].

Several important results have been obtained and summarized as follows:

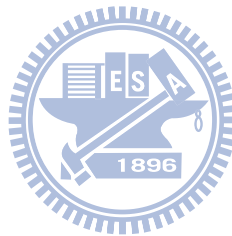
1. In Chapter 2, the BSIM-based method is introduced for the R_{sd} extraction. This BISM-based method is more accurate than the conventional Channel-Resistance and Shift & Ratio method because it considers the gate-length dependence of mobility caused by local uniaxial stress and laterally non-uniform channel doping. This method has been verified using samples with different process conditions and good agreement with experimental data has been obtained. The accuracy of BSIM R_{sd} extraction method has also been verified by TCAD simulations.
2. In Chapter 3, the short channel mobility extraction method by using split-CV is introduced to investigate the strain impact on short channel mobility. Then the impact of process-induced uniaxial strain on Coulomb mobility in short-channel nMOSFETs and pMOSFETs is investigated under various temperatures. Our study indicates that the stress sensitivity of the Coulomb mobility shows strong

temperature dependence. It results from the competition between bulk charge scattering and interface charge scattering. Therefore, in order to optimize the strain efficiency on Coulomb mobility, it is necessary to suppress the formation of interface charges (N_{it}).

3. In Chapter 4, we examine the impact of strain on surface roughness mobility (μ_{SR}) of pMOSFETs by process-induced uniaxial strain with He-based low temperature system. Moreover, we compare the strain sensitivity between μ_{PH} and μ_{SR}. Our measured data indicates that μ_{SR} can be significantly enhanced by the uniaxial compressive strain. Furthermore, the μ_{SR} has higher strain dependence than the phonon scattering limited mobility (μ_{PH}). Our experimental results confirm the previously reported results based on simulations. In addition, a wavefunction penetration perspective is proposed to explain the possible physical origin of the uniaxial strain dependence of μ_{SR}.

4. In Chapter 5, we conduct an experimental assessment for the impact of process-induced uniaxial strain on the temperature dependency of carrier mobility in nanoscale pMOSFETs. Furthermore, through decoupling μ_{SR} and $\mu_{PH,}$ we investigate the impact of uniaxial strain on the temperature dependence of phonon-scattering limited mobility in nanoscale PMOSFETs. Our study indicates that the strain sensitivity of hole mobility becomes less with increasing temperature and it is consistent with previous uniaxial mechanical bending result. It is because the less hole repopulations at energy band edge induce less strain sensitivity as temperature increases. The extracted μ_{SR} and μ_{PH} are proportional to $E_{EFF}^{-1.3}$ and $E_{EFF}^{-0.3}$, respectively, which is consistent with the reported data in the literature [8]. The temperature sensitivity of the extracted phonon mobility is proportional to $T^{-1.75}$ [12] for neutral stressor and becomes higher when compressive strain is

applied. It can be explained by the higher optical phonon energy induced by uniaxially-compressive strain. Our new findings also explain the higher temperature sensitivity of drain current presented in uniaxial strain PMOSFETs.



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博士論文題目：

單軸應變矽奈米尺寸金氧半場效電晶體對於載子遷移率之各種散射機制的實驗性研究

Experimental Investigation of Carrier Mobility considering Various Scattering Mechanisms for Uniaxial Strained MOSFETs

著作目錄

A. International Journal

1. **<u>W. P. -N. Chen</u>**, J. J.-Y. Kuo, and P. Su, "Impact of Process-Induced Uniaxial Strain on the Temperature Dependence of Carrier Mobility in Nanoscale pMOSFETs," *IEEE Electron Device Letters*, vol. 31(**5**), pp. 414-416, May. 2010. (A 類期刊-**SCI**)

2. **<u>W. P. -N. Chen</u>**, J. J.-Y. Kuo, and P. Su, "Experimental Investigation of Surface Roughness Limited Mobility in Uniaxial Strained pMOSFETs," *IEEE Electron Device Letters*, in press. (A 類期刊-**SCI**)

3. **<u>W. P. -N. Chen</u>**, P. Su, K. Goto, "Impact of Process-Induced Strain on Coulomb Scattering Mobility in Short-Channel n-MOSFETs," *IEEE Electron Device Letters*, vol. 29(**7**), pp. 468-470, July 2008. (A 類期刊-**SCI**)

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C. Patents

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