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博 士 論 文

先進金氧半場效電晶體考慮溫度相依之高頻小訊號及雜訊特性分析

High-Frequency Small-Signal and Noise Characterization for Advanced MOSFETs Considering Temperature Dependence

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摘要

本篇論文對於現今各種的平面金氧半場效電晶體(MOSFET)作了完整的高頻小訊號及雜訊特性分析和模型化工作，這些元件包括傳統 MOSFET(bulk MOSFET)、絕緣層上矽 MOSFET(SOI MOSFET)、絕緣層上矽動態起始電壓 MOSFET(SOI DT MOSFET)和應變 MOSFET(strained MOSFET)等。建立於傳統 MOSFET 架構下的等效射頻小訊號電路模型將被適當地修改以考量存在於各別元件的寄生效應，並藉由在適當的位置擺入各雜訊源，我們便可以建立各元件對應的高頻雜訊模型。此外，本篇論文也首次探討到各元件在溫度變化下的高頻行為表現。

部分空乏 SOI MOSFET 中性體區(neutral-body)的寄生效應，會影響到元件的輸出特性，其影響甚至可到數個 GHz 的操作頻率。由於通道電導高溫時減小，造成了 bulk MOSFET 和 SOI MOSFET 的通道雜訊都呈現具負溫度係數的特性。此外，SOI 元件中的自發熱效性(self-heating effect)和浮體效應(floating-body effect)會使得其雜訊因子(noise factor)高於傳統 MOSFET。不利於高頻雜訊的浮體效應(在低閘電壓下較明顯)可藉由升溫加以抑制，而自發熱效應則因為高閘極電壓伴隨的低電導而可抵掉一部分效應。

SOI DT MOSFET 的基底寄生元件和串聯電阻對最大震盪頻率(f_{max})的影響比對截止頻率(f_t)來的大。此外，在一般操作所使用的低閘極和低汲極偏壓(VDD)下，由於轉導(g_m)會隨溫度上升而上升，造成 f_t 和 f_{max} 都和溫度成正相依關係。實驗結果顯示當 DT MOSFET 的偏壓朝弱反轉方向減小，由於轉導平方項的正溫度相依情形相對於通道

雜訊來得大，我們發現其等效熱雜訊電阻 R_n 將具有負的溫度係數。進一步的研究發現，基底的連接電阻 R_b 所產成的雜訊會不利於最低雜訊指數 $NF_{\min}$，且低 VDD 偏壓下的較大 R_b 對於 $NF_{\min}$ 的溫度相依情形反而影響不大。

舒張形變 n 型 MOSFET(tensile-strained nMOSFET)因為擁有較大載子移動率及和傳統 MOSFET 相近的飽和電壓，所以以相同的偏壓條件來說，會有較大的通道雜訊。然而，實驗結果顯示對於相同的功率消耗條件來說，其較大的轉導會使得 tensile-strained nMOSFET 在 f_t、$f_{\max}$、$NF_{\min}$ 和 R_n 的表現上都會比傳統 MOSFET 來的優異。

最後，本論文探討 65 奈米 MOSFET 應用於毫米波時的雜訊表現。實驗結果顯示，持續上升的通道雜訊對整體毫米波雜訊模型化工作和特性分析的影響愈來愈重要。除此之外，以寄生效應來看，閘極電阻對毫米波的雜訊影響程度比基板電阻來的大。

關鍵字：動態起始電壓金氧半場效電晶體, 毫米波, 雜訊因子, 雜訊參數, 射頻, 絕緣層上矽金氧半場效電晶體, 小訊號, 溫度相依, 應變

High-Frequency Small-Signal and Noise Characterization for Advanced MOSFETs Considering Temperature Dependence

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Abstract

This dissertation provides a comprehensive high-frequency small-signal and noise characterization and modeling for various kinds of modern planar MOSFET devices, including the bulk MOSFET, silicon-on-insulator (SOI) MOSFET, partially-depleted SOI dynamic threshold voltage (DT) MOSFET, and strained MOSFET. The traditional RF small-signal equivalent circuit for the bulk MOFET will be modified to include existing parasitic components present in each kind of MOSFETs. Based on each tailored small-signal model, the corresponding high-frequency noise model can be built by adding the noise sources in place. For the first time, the temperature dependence of the high-frequency performance will also be discussed.

The SOI MOSFET has the inherent neutral-body effect, which will be found to influence the output characteristic even in GHz applications. The channel noise S_{id} has been shown to have a negative temperature coefficient for both the bulk and SOI MOSFETs due to the lowered channel conductance at high temperature. Besides, the self-heating effect (SHE) and the floating-body effect (FBE) of the SOI MOSFET would make its noise factor higher than the bulk MOSFET. It shows that the FBE, which dominates at low V_{GS} regime, can be suppressed by elevating the ambient temperature, while the SHE, obvious at high V_{GS}, would

be partly counterbalanced by the lowered channel conductance at high temperature.

The body-related parasitics and the series resistance of the SOI DT MOSFET are found to have more impact on $f_{\max}$ (maximum oscillation frequency) than f_t (cut-off frequency). Besides, in the normal bias condition - low gate and drain voltage (low VDD) regime, both f_t and $f_{\max}$ have positive temperature coefficients due to the increased g_m (trans-conductance) at high temperature. We also show that the DT MOSFET would get a negative temperature coefficient for equivalent noise resistance R_n towards the weaker inversion region due to the much higher g_m^2 than S_{id} with increasing temperature. Furthermore, our research results show the noise arising from the body resistance R_b can degrade the minimum noise figure $NF_{\min}$, and the larger R_b encountered in the low VDD regime would have less impact on the temperature dependence of $NF_{\min}$.

The tensile-strained nMOSFET presents larger S_{id} than the control device due to its enhanced mobility and nearly the same saturation voltage for a given bias point, and has the same temperature dependence of S_{id} as the control device. However, our measured data indicates that the enhanced carrier trans-conductance in the tensile nMOSFET would contribute to better f_t , $f_{\max}$, $NF_{\min}$ and R_n than the control device for a given DC power consumption.

Finally, for the emerging millimeter-wave applications, we examine the millimeter wave noise behavior of 65nm MOSFETs. The experimental results show that the continually increasing S_{id} makes it play a more and more important role in the millimeter-wave noise modeling and characterization. Besides, compared to the substrate resistance, the gate resistance has more impact on the noise parameters in the millimeter-wave frequency.

Keywords: DT MOSFET, millimeter-wave, noise factor, noise parameters, RF, SOI MOSFET, small-signal, temperature dependence, tensile-strained

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Chapter 1

Introduction

With the advantages of low cost, low power, high integration capability, and easy access to technology [1][2], CMOS technology has become an attractive choice for RF applications. Specifically, the continuous downscaling of CMOS processes beyond the deep sub-micron generation has led to the improved cut-off frequency (f_t) and minimum noise figure ($NF_{\min}$) of MOSFETs [3]-[5].

To save time to market and reduce the design cycle, the demand for accurately modeling the RF characteristics is strong and has attracted a bunch of studies. Recently, a lot of investigations on the RF small-signal characterization and modeling for the traditional bulk MOSFET have been reported. The equivalent circuit used to analyze and model the RF small-signal behaviors for bulk MOSFETs is well-built, and the parameter extraction methodology has been well-developed, either for the intrinsic or extrinsic components [6]-[10]. Based on this mature equivalent circuit, many reports on RF noise characterization and modeling have been presented accordingly. They have shown that both the channel noise and noise factor would increase with decreasing channel length [11][12], and this can harm the RF noise performance. Besides, the impact of parasitics associated with the probing pad and substrate has been examined [13][14]. The temperature dependent noise behavior for the bulk MOSFET, however, has rarely been discussed.

The emerging silicon-on-insulator (SOI) technology has shown the features of low junction capacitance, high process capability with the traditional bulk silicon process, low cross-talk [15][16]. Therefore, it has become an alternative to the traditional bulk MOSFET technology. Due to the low-pass filter nature, its inherent floating body has been shown to have significant effect either on the ac output characteristics [17] or the flicker noise performance [18]. Hence, the parasitic neutral body region is usually assumed to be negligible

to the above mega-hertz application [19]. In fact, we will show that the coupling path through the quasi-neutral body region may still play an important role in the RF SOI modeling in several GHz. Besides, several studies have considered the self-heating effect to capture the noise behavior for the SOI MOSFETs [20][21]. Nevertheless, the direct comparison of RF noise performance between the bulk and SOI MOSFETs in terms of noise parameters and white-γ noise factor has not been widely reported.

Another novel device formed by connecting the gate and body terminal together is the dynamic-threshold voltage MOSFET (DT MOSFET). The DT MOSFET, which can be fabricated using the SOI process, has the advantages of larger current driving ability and low leakage current [22]. Hence, it is also attractive for RF application [23]. To give a comprehensive discussion, we will cover the study on the temperature effect of body-related parasitics and series resistances on f_t and $f_{\max}$. The RF noise behavior and its temperature dependence will be addressed as well.

To maintain the scaling trends of CMOS devices while bypassing the other physical and technological issues, strain-engineering technology has become a popular way to fabricate devices. Recently, the strained CMOS technology has demonstrated its excellent RF performance with a high cut-off frequency (f_t) [24]. However, the effects of the highly tensile stressors on the high frequency noise characteristics have rarely been unveiled. Hence, it is necessary to investigate and analyze the high frequency noise characteristics of tensile-strained nMOSFETs.

Besides, with the continuous downscaling of channel length toward deca-nanometer regime, RF MOSFETs have entered the field of millimeter-wave applications [25]. The previous works have discussed the RF noise behavior for deep sub-micron MOSFETs operating mainly in several GHz, and the experimental results for the millimeter-wave noise characterization and its corresponding modeling are deficient. We will use an external tuner-based method to demonstrate a complete millimeter-wave noise characterization and modeling up to 60GHz for 65nm MOSFETs. Since the gate resistance and substrate loss have

been reported to be main issues to degrade the RF noise performance, these effects will be considered in this thesis.

This dissertation is organized as follows. Chapter 2 presents small-signal modeling for RF SOI MOSFETs. Especially, we have incorporated the neutral-body effect in our RF SOI model. This effect can not be ignored in both RF extrinsic and intrinsic modeling stages. In addition, we have developed a physically-accurate parameter extraction method based on our analytical expressions. Our modeling results agree well with the measured data and can capture the frequency dependences of both output conductance and capacitance in the GHz frequency region. The anomalous S_{22} and S_{21} behaviors as well as the output conductance rising effect observed in our measurements can be predicted and described using the proposed model.

In chapter 3, we experimentally study the temperature dependence of the power spectrum densities (PSDs) of the intrinsic noise sources for both the RF bulk and SOI MOSFETs. The popular van der Ziel's model is used to check its applicability at different temperatures. The power spectral density (PSD) for the channel noise current is found to decline as temperature increased due to the decreased channel conductance. Along with the extracted small-signal and van der Ziel's model parameters, their temperature dependences can be well described. For completeness, their temperature-dependent noise parameters are demonstrated as well. Besides, for SOI MOSFETs, our experimental results reveal that the significant floating body effect and the self-heating effect may contribute to the higher noise factor compared to the bulk counterparts.

In Chapter 4, temperature-dependent RF small-signal and noise characteristics of SOI dynamic threshold voltage (DT) MOSFETs are experimentally examined. In the low voltage regime, both the cut-off and maximum oscillation frequencies (f_t and $f_{\max}$) tend to increase with temperature. In addition, the inherent body-related parasitics and the series resistance have much more impact on $f_{\max}$ than f_t. Besides, we found that the noise stemmed from the body resistance (R_b) would contribute to the output noise current, and degrade the

minimum noise figure ($NF_{\min}$). Our study may provide insights for RF circuit design using advanced SOI DT MOSFETs.

The high-frequency noise behavior of tensile-strained nMOSFETs, including its temperature dependency, is experimentally examined in Chapter 6. Our experimental results indicate that with similar saturation voltages, the strained nFET is found to have a larger channel noise than the control device at the same bias point. For a given DC power consumption, however, due to enhanced trans-conductance, the strained nFET has better small signal behaviors (higher f_t and $f_{\max}$) and noise characteristics (smaller $NF_{\min}$ and R_n) than the control device.

Using an external tuner-based method, Chapter 6 demonstrates a complete millimeter-wave noise characterization and modeling up to 60GHz for 65nm MOSFETs for the first time. Due to channel length modulation, the channel noise continues to increase and remains the most important noise source in the millimeter-wave band. Our experimental results further show that, with the downscaling of channel length, the gate resistance has more serious impact on the high frequency noise parameters than the substrate resistance even in the millimeter-wave frequency.

Chapter 7 concludes the experimental results of this dissertation.

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Chapter 2

RF Small-Signal Modeling and Characterization for SOI MOSFETs

2.1 Introduction

Due to its highly integrated nature and good scaling capabilities, CMOS technology has become an excellent choice for RF applications. SOI CMOS is especially a promising candidate for the RF system-on-chip integration because of its low source and drain parasitic capacitances, high process capability with the traditional bulk Si process, reduction in cross-talk between RF and digital circuits, and easy integration of high quality passive elements [1][2]. With the penetration of SOI CMOS into RF applications [3][4], RF SOI small-signal modeling has become a crucial design issue.

Although several investigations [5]-[8] regarding the RF SOI small-signal modeling have been carried out in the past, it was assumed that the RF small-signal equivalent circuit of the SOI MOSFET is essentially identical to that of the bulk counterpart. Moreover, Lederer *et al.* proposed a SOI model suitable for body-tied devices without considering the neutral-body region underneath the gate oxide layer [6]. However, we will show that the coupling path between the source and drain terminals through the quasi-neutral body region may play an important role in the RF SOI modeling [9].

In this chapter, we will present a comprehensive RF SOI small-signal model considering this neutral-body path [10]. Based on this model, the methods suitable for RF extrinsic and intrinsic parameter extractions will also be demonstrated. Finally, the neutral-body effect on the output characteristics will be investigated as well [11].

2.2 Devices and Experiments

The RF SOI MOSFETs used in this work were fabricated using UMC 0.13 μm SOI technology. The thicknesses for gate oxide, SOI layer and buried oxide are 1.4nm, 40nm, and 200nm, respectively. These RF devices were laid out in the multi-finger and multi-group structure with the following denotations: L for channel length, W_F for finger length, N_F for the number of fingers, and N_G for the number of groups (*i.e.* total gate width $W = W_F \times N_F \times N_G$). The presence of current kinks in Fig. 2-1 shows that the devices under study are partially depleted (PD).

On-wafer 2-port common-source S parameters were measured using network analyzers with microwave probes. To eliminate the inevitable parasitic accompanied with the probing pads, the S parameters of devices' corresponding open dummy ware measured and then used to perform the de-embedding procedure. After that, the de-embedded S parameters of the devices will be transformed to Z parameters to participate in the following extraction of the extrinsic terminal resistances.

To further minimize possible substrate resistive loss through the buried oxide layer [12], a bias-network connected to the chuck of the probe station was used to provide the substrate DC ground (*i.e.* back-gate voltage $V_{ES} = 0$) with RF floating.

2.3 Neutral-Body Effect on the Resistance Extraction

The extraction of extrinsic resistances is essential to RF CMOS modeling. References [13]-[15] have presented extrinsic resistance extraction methodologies for SOI MOSFETs. Among these approaches, the zero method developed under the zero condition (*i.e.* $V_{GS} = V_{DS} = 0$) is attractive because it can simplify the corresponding equivalent circuit and avoid the extraction error caused by the non-quasi-static (NQS) effect [15].

Based on the equivalent circuit built for bulk MOSFETs under the zero condition as shown in Fig. 2-2 [16], the following frequency-independent resistance expressions have been

derived to directly determine R_s, R_d, and R_g, respectively.

$$\mathrm{Re}(Z_{21}) = \mathrm{Re}(Z_{12}) = R_s \tag{2-1}$$

$$\mathrm{Re}(Z_{22} - Z_{12}) = R_d \tag{2-2}$$

$$\mathrm{Re}(Z_{11} - Z_{12}) = R_g \tag{2-3}$$

Figure 2-3 compares the resistance curves versus frequency characteristics under the zero condition for PD SOI MOSFET and its bulk counterpart with identical layout structure and geometry. All of these curves more or less are frequency-dependent. The poor shapes for the bulk MOSFET can be attributed to the complicated and significant substrate resistive loss [17][18]. For the SOI MOSFET, however, the substrate loss may not be responsible for this frequency-dependent behavior because the thick buried oxide layer in the SOI transistor has provided good isolation from the substrate.

We turn to consider the neutral-body parasitics beneath the channel of the SOI MOSFET. Figure 2-4(a) shows its cross-sectional view under the zero condition. The neutral-body coupling path is constituted by source- and drain-side junction capacitances ($C_{j,sb}$ and $C_{j,db}$), and body resistances (R_b). Its corresponding equivalent circuit is depicted in Fig. 2-4(b). Here the neutral-body coupling path is represented by a lumped junction capacitance C_b [$= \left(C_{j,sb}^{-1} + C_{j,db}^{-1}\right)^{-1}$] and a body resistance R_b. Based on this equivalent circuit, the following more general resistance expressions regarding R_s, R_d, and R_g can be derived:

$$\mathrm{Re}(Z_{21}) = \mathrm{Re}(Z_{12}) = R_s + \frac{A}{\omega^2 + B} \tag{2-4}$$

$$\mathrm{Re}(Z_{22}) - \mathrm{Re}(Z_{12}) = R_d + \alpha \cdot \frac{A}{\omega^2 + B} \tag{2-5}$$

$$\mathrm{Re}(Z_{11}) - \mathrm{Re}(Z_{12}) = R_g - \frac{\alpha}{1+\alpha} \cdot \frac{A}{\omega^2 + B} \tag{2-6}$$

where

$$A = \left[C_{gd}\left(C_{gs}+C_{gd}\right)C_b^2\right]\cdot R_b^{-1}\cdot\beta^{-1}, \tag{2-7}$$

$$\begin{aligned} B = \{&2C_{gs}C_{gd}\left[C_b\left(C_{gs}+C_{gd}+C_b\right)+C_{ds}\left(C_{gs}+C_{gd}+C_{ds}\right)\right] \\ &+2C_{ds}C_b\left(C_{gs}^2+C_{gd}^2\right)+\left(C_{gs}^2+C_{gd}^2\right)\left(C_b^2+C_{ds}^2\right) \\ &+C_{gs}^2C_{gd}^2+4C_{gs}C_{gd}C_{ds}C_b\}\cdot R_b^{-2}\cdot\beta^{-1} \end{aligned}, \tag{2-8}$$

$$\alpha = \frac{C_{gs}}{C_{gd}}, \tag{2-9}$$

and

$$\beta = C_{gs}C_{gd}^2C_b^2\left(C_{gs}+2C_{ds}\right)+C_{gd}C_{ds}^2C_b^2\left(C_{gd}+2C_{gs}\right)+C_{ds}C_{gs}^2C_b^2\left(C_{ds}+2C_{gd}\right). \tag{2-10}$$

The frequency independent parameters, A, B, α and β, are all constants involved with intrinsic parameters under the zero condition. Besides, as shown in Fig. 2-3, whether the substrate RF ground is provided or not, the resistance curves are almost unchanged. This indicates that the substrate effect is negligible in our experiments. Therefore, to simplify the equivalent circuit, any substrate parasitic through the buried oxide has been omitted here.

According to Equs. (2-4) to (2-6), it is obvious that these resistance expressions are frequency dependent, and the extrinsic resistances are equal to their high frequency asymptotes. In practice, although we cannot rely on the very high frequency measurement to directly obtain these resistance values, they can be obtained by fitting the resistance expressions with their corresponding measured data. The achieved model-data comparison for the extraction of R_s, R_d, and R_g are shown in Fig. 2-5. It can be seen that the measured curves are indeed frequency dependent, and can be well fitted by Equs. (2-4) to (2-6). For clarity, the model parameters and extracted resistance values (or equally the high frequency asymptotes) are also shown in the figure. The low gate resistance ($R_g = 0.4\,\Omega$) is physically expected due to the multi-finger structure [19], and non-equal R_s and R_d results from the fact that the RF devices were laid out in the multi-finger and multi-group structure. The multi-source regions were out-connected at two ends of each finger, while the multi-drain

regions were out-connected at only one side. In addition, the interconnection between each group can provide additional resistance for the drain terminal and result in discrepancy between R_s and R_d. Also note that the nearly unity α implies $C_{gs} \approx C_{gd}$, which is reasonable for multi-finger structures and has been widely used under the zero condition [15].

The good agreements between the modeled and measured data for the resistance curves with various layout geometries can be found in Fig. 2-6 ($\alpha = 1$). Besides, according to Equs. (2-4) to (2-6), $\mathrm{Re}(Z_{22} - Z_{12})$, $\mathrm{Re}(Z_{12})$, and $\mathrm{Re}(Z_{11} - Z_{12})$ are mutually correlated [14] by:

$$\mathrm{Re}(Z_{22} - Z_{12}) = \mathrm{Re}(Z_{12}) + R_{d-s} \tag{2-11}$$

$$\mathrm{Re}(Z_{11} - Z_{12}) = -0.5 \times \mathrm{Re}(Z_{12}) + R_{g-s} \tag{2-12}$$

$$\mathrm{Re}(Z_{11} - Z_{12}) = -0.5 \times \mathrm{Re}(Z_{22} - Z_{12}) + R_{g-d} \tag{2-13}$$

where $R_{d-s} = R_d - R_s$, $R_{g-s} = R_g + 0.5 \times R_s$, and $R_{g-d} = R_g + 0.5 \times R_d$. Equations (2-11) to (2-13) have been verified in Fig. 2-7.

The extracted extrinsic resistances and model parameters A, B, R_{d-s}, R_{g-s}, and R_{g-d} for each SOI device are listed in Table 2-1. Besides, since all the involved device conductance and capacitances in Equs. (2-4) to (2-6) are proportional to the total gate width W, the parameter A should increase as W decreases. As indicated in Fig. 2-6, the resistance curves for the device with smaller W indeed have a larger deviation from its high-frequency asymptote in the lower frequency regime. Therefore, one can minimize the extraction error resulted from the SOI neutral-body effect by using the wide device.

2.4 Neutral-Body Effect on the Intrinsic Modeling

After extracting $R_s / R_d / R_g$, we can obtain the intrinsic Z parameters (Z_i) of the devices by exploiting the following expression [16]:

$$\begin{bmatrix} Z_{i,11} & Z_{i,12} \\ Z_{i,21} & Z_{i,22} \end{bmatrix} = \begin{bmatrix} Z_{11} - (R_g + R_s) & Z_{12} - R_s \\ Z_{21} - R_s & Z_{22} - (R_d + R_s) \end{bmatrix}. \tag{2-14}$$

Then, the intrinsic Y parameters (Y_i) can be obtained directly from the Z-to-Y parameter transformation of Z_i.

Based on the equivalent circuit proposed in [20], Figure 2-8 shows the intrinsic small-signal equivalent circuit for SOI devices under the active operation, where the neutral-body parasitic is represented by a series combination of two junction capacitances, $C_{j,sb}$ and $C_{j,db}$, and a body resistance R_b along with the body trans-conductance g_{mb}. It is worth noting that, instead of the particular access resistance introduced via the external body contacts in body-tied or dynamic-threshold SOI MOSFETs [6][7], R_b may represent the un-depleted body resistance for all kinds of SOI MOSFETs. In addition, to simplify the following derivations, some modifications have been made to this circuit. First, the junction related conductances are neglected in the equivalent circuit because the junction capacitances would dominate the entire junction admittances at high frequency. Second, the conductance caused by the body potential through the impact ionization is also omitted due to its low pass nature [20]. Finally, the intrinsic body node is assigned to be located just next to the source-body junction as usually done in bulk MOSFET models.

Since the major impact of the neutral-body effect on the equivalent circuit lies in the output admittance Y_{out}, which is equal to $Y_{i,22} + Y_{i,12}$ and defined by the dashed box shown in Fig. 2-8, this means that except those model components relating to Y_{out}, the others can be directly determined by those equations originally derived for bulk MOSFETs [16]:

$$C_{gs} = \frac{\mathrm{Im}(Y_{i,11} + Y_{i,12})}{\omega} \tag{2-15}$$

$$C_{gd} = -\frac{\mathrm{Im}(Y_{i,12})}{\omega} \tag{2-16}$$

$$g_m = |Y_{i,21} - Y_{i,12}| \tag{2-17}$$

Figure 2-9 shows these extraction results, and their frequency independences also reveal the accuracy of the resistance extraction method presented in the previous section. Note that for our devices with cut-off frequency larger than 90 GHz, the delay time constant τ can be neglected for the operating frequency not exceeding 10 GHz.

To extract Y_{out}-related components, however, the following analytical equations must be used.

$$G_{out} \equiv \mathrm{Re}(Y_{out}) = \frac{1}{R_{ds}} \times \left[1 + \frac{\omega^2 C_{j,sb}^2 C_{j,db}^2 R_b R_{ds} + g_{mb} C_{j,db} R_{ds} \left(C_{j,db} + C_{j,sb}\right)}{\omega^2 C_{j,sb}^2 C_{j,db}^2 R_b^2 + \left(C_{j,sb} + C_{j,db}\right)^2}\right] \tag{2-18}$$

$$C_{out} \equiv \frac{\mathrm{Im}(Y_{out})}{\omega} = C_{ds} \times \left[1 + \frac{C_{j,sb} C_{j,db} \left(C_{j,sb} + C_{j,db} - g_{mb} C_{j,db} R_b\right)}{C_{ds}\left[\omega^2 C_{j,sb}^2 C_{j,db}^2 R_b^2 + \left(C_{j,sb} + C_{j,db}\right)^2\right]}\right] \tag{2-19}$$

One can find that Equs. (2-18) and (2-19) will tend to saturate at $R_{ds}^{-1} + R_b^{-1}$ and C_{ds}, respectively at very high frequency. This is because the short-circuited junction capacitances at high frequencies (both the junction impedances $\left(j\omega C_{j,sb}\right)^{-1}$ and $\left(j\omega C_{j,db}\right)^{-1}$ approach 0) cause the residual body resistance to be parallel with the channel resistance, and makes no other capacitance except C_{ds} left. Therefore, RF output conductance (denoted as g_{RF}) extracted from the high frequency asymptote of G_{out} would be the parallel combination of channel conductance and body conductance ($= R_{ds}^{-1} + R_b^{-1}$) and is larger than sole channel conductance R_{ds}^{-1}, which can be extracted from the DC current-voltage (IV) measurement (denoted as g_{DC}).

The modeling results of G_{out} and C_{out} for various drain bias conditions with gate bias 1.2V are shown in Figs. 2-10(a) and (b), respectively, where the frequency dependence natures of both G_{out} and C_{out} can be described by our model (Equs. (2-18) and (2-19)). Here, R_{ds}^{-1} is directly extracted from g_{DC}, R_b^{-1} from $g_{RF} - g_{DC}$, and C_{ds} from the high frequency asymptote of C_{out}, and for clarity, all the extracted component values are listed in

Table 2-2. These figures show that the neutral-body effect would play an important role mostly in the low GHz region. To be more completed, the good modeling results of S parameters considering the neutral-body effect (NBE) have been verified and are shown in Fig. 2-11.

It is also worth noting that, for SOI MOSFETs, our model can predict the occurrence of anomalous behaviors in the S parameters. In Fig. 2-12(a), two abnormal phenomena in S_{22} can be observed - the inductance-like behavior for Bias A condition and the kink behavior for Bias B. Also, the abnormal S_{21} behaviors can be observed in Fig. 2-12(b). The modeling results for their magnitude and phase versus frequency characteristics can also be found in Fig. 2-13. In these figures, only the proposed model considering the neutral-body effect can capture these abnormal phenomena prominent in lower frequency region. This also indicates the need of considering the neutral-body effect when it comes to the RF SOI modeling especially below several GHz.

2.5 Neutral-Body Effect on the Output Characteristics

We have shown how the SOI-specific neutral-body affects the small-signal model structure and the parameter extraction for both extrinsic and intrinsic parts of RF SOI MOSFETs. For RFIC designers, it is also important to evaluate the significance of the neutral-body effect on the increase of the RF output conductance, which may dominate the circuit performance.

To assess the importance of the neutral-body effect on the RF performance, we define the fractional factor η:

$$\eta \equiv \frac{R_{ds}}{R_b} = \frac{g_{RF} - g_{DC}}{g_{DC}} = \frac{g_b}{g_{ds}}. \tag{2-20}$$

According to this definition, it is obvious that the higher the factor is, the more significant R_b would be. Figure 2-14 shows g_{DC} $(=R_{ds}^{-1})$ and g_b $(=R_b^{-1})$ versus drain bias with different gate bias conditions, and their corresponding η's are shown in Fig. 2-15. Both

figures show that the body conductance g_b has the chance to be comparable with or even larger than the channel conductance g_{DC}. Therefore, the neutral-body effect can influence the RF performance to a great extent.

2.6 Summary

The SOI neutral-body coupling effect should be considered for the characterization and modeling of SOI MOSFETs, although the thick buried oxide can block the complicated substrate network. An equivalent circuit including the neutral-body parasitics has been proposed, and a new set of model equations capturing the frequency dependence of extrinsic resistances and output characteristics has been derived accordingly. After taking into account the impact of quasi-neutral body, we have completed a physically accurate RF small-signal characterization and modeling for SOI MOSFETs.

The neutral-body parasitics predict and explain the existence of anomalous S_{22} and S_{21} behaviors, and they can influence the RF output characteristics of SOI MOSFETs.

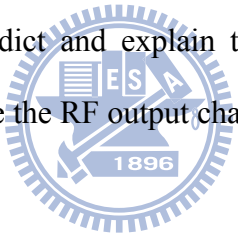

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Table 2-1 Extracted model parameters for the extrinsic resistances. The values of $L/W_F/N_F/N_G$ for FET1, FET2 and FET3 are 0.12μm/2.4μm/16/3, 0.12μm/1.8μm/2/18, and 0.12μm/3.6μm/11/4, respectively.

	W (μm)	A ($10^{21}F^{-1}s^{-1}$)	B ($10^{20}s^{-2}$)	R_{d-s} (Ω)	R_{g-s} (Ω)	R_{g-d} (Ω)	R_s (Ω)	R_d (Ω)	R_g (Ω)
FET1	115.2	4.9	7.2	1.4	1.45	2.15	0.1	1.5	1.4
FET2	64.8	6.4	6.4	2.9	1.35	2.8	0.1	3	1.3
FET3	158.4	3.5	7.4	0.9	1.55	2	0.1	1	1.5

Table 2-2 Extracted model parameters for the intrinsic modeling. ($V_{GS} = 1.2V$)

V_{DS} (V)	C_{gs} (fF)	C_{gd} (fF)	g_m (mS)	C_{ds} (fF)	R_{ds} (Ω)	R_b (Ω)	$C_{j,sb}$ (pF)	$C_{j,db}$ (pF)	g_{mb} (mS)
0.8	109	56	96	14	119	63	61	50	32
1	109	53	96	24	156	73	64	58	25
1.2	109	51	96	29	167	88	74	20	53

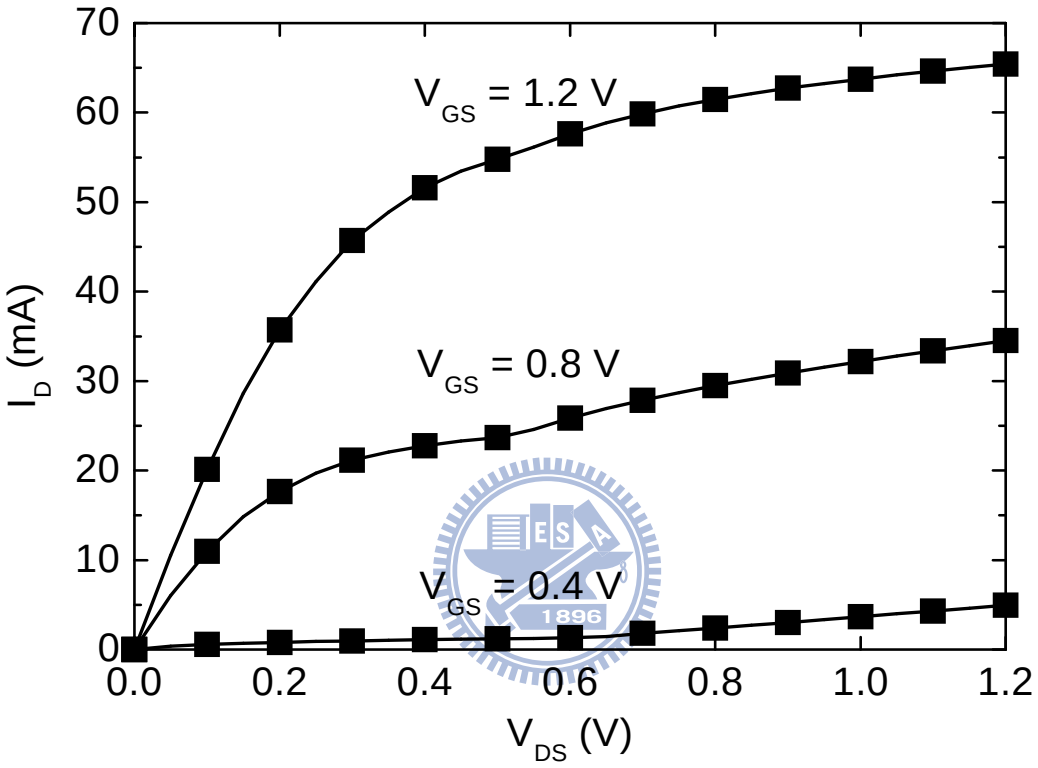


Figure 2-1 I_D versus V_{DS} curves for the RF SOI MOSFETs showing their properties of being partially depleted. ($L/W_F/N_F/N_G$ = 0.12μm/2.4μm/16/3)

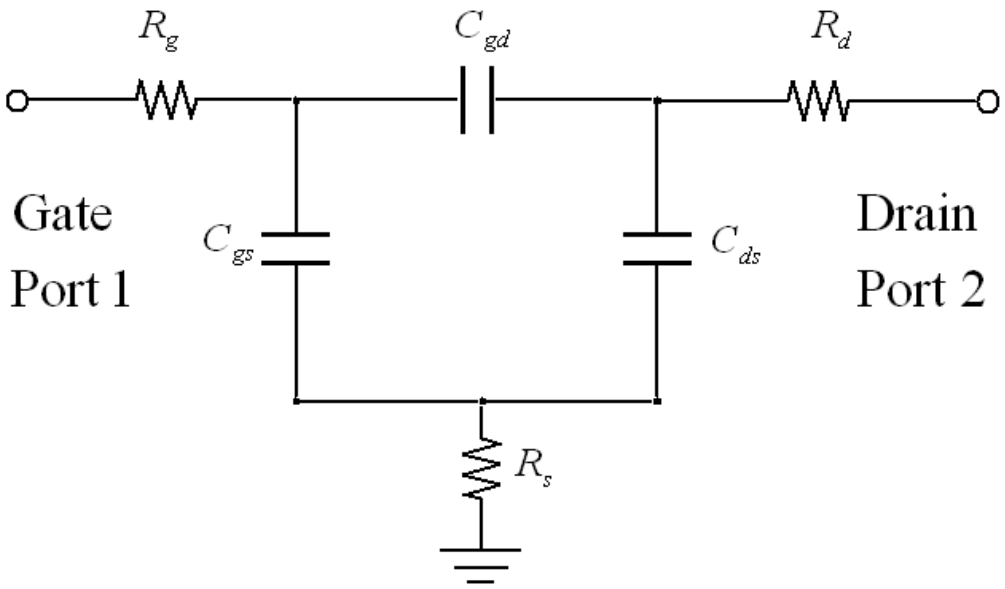


Figure 2-2 Traditional equivalent circuit for the bulk MOSFET under the zero condition.

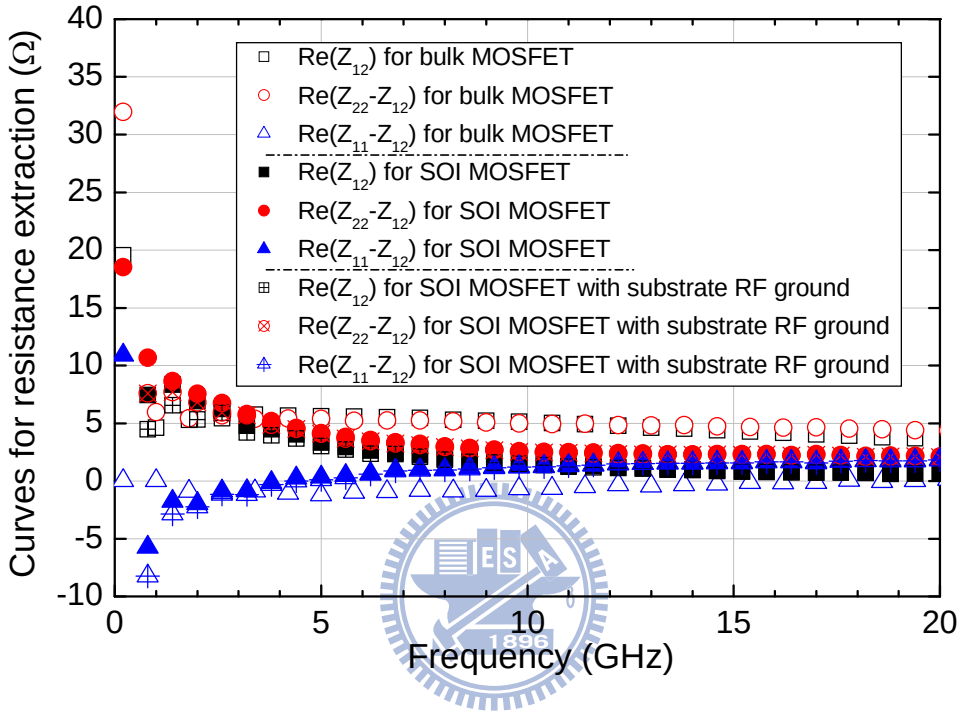


Figure 2-3 Resistance curves for the bulk and PD SOI MOSFETs. ($L/W_F/N_F/N_G$ = 0.12μm/2.4μm/16/3)

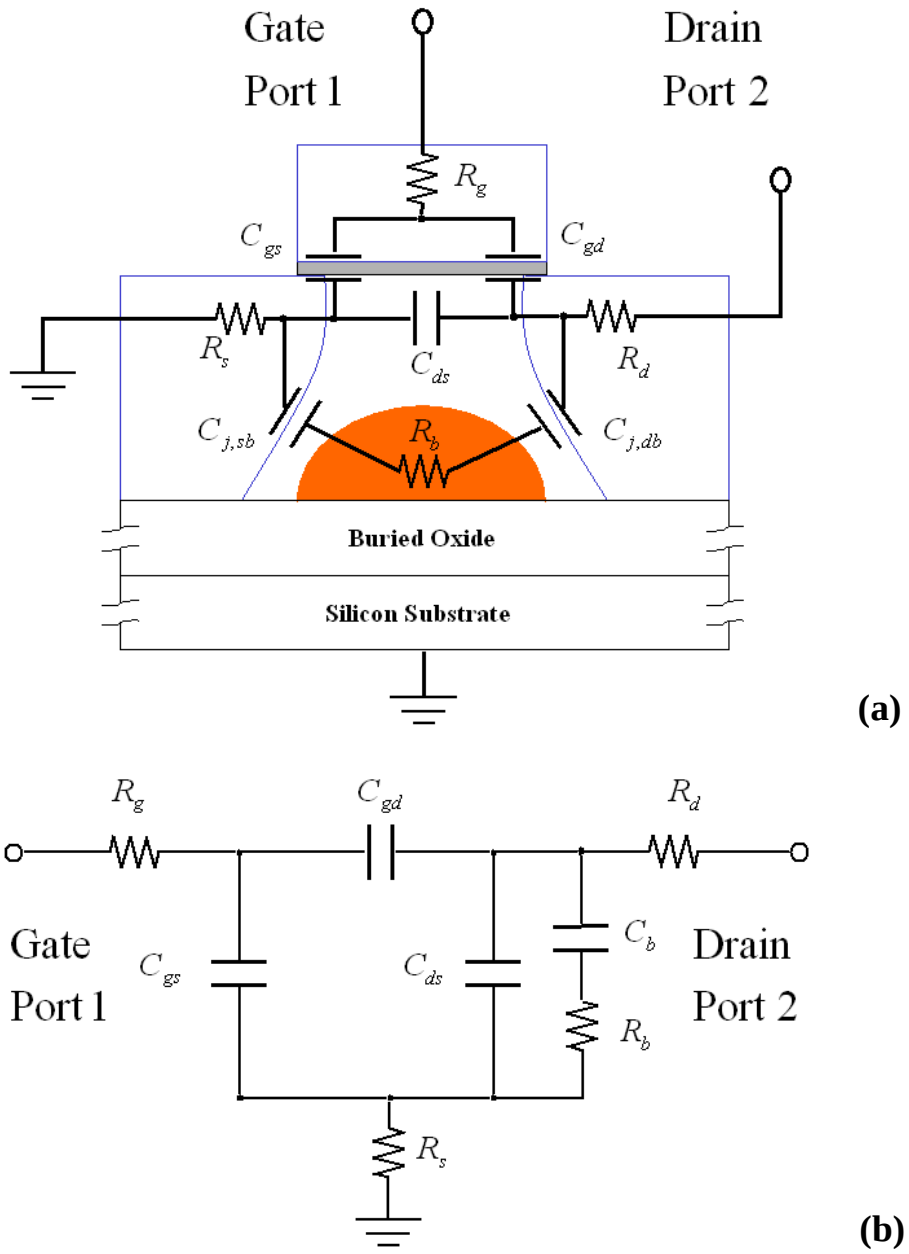


Figure 2-4 (a) Cross-sectional view of the SOI MOSFET under the zero condition, and (b) its corresponding equivalent circuit.

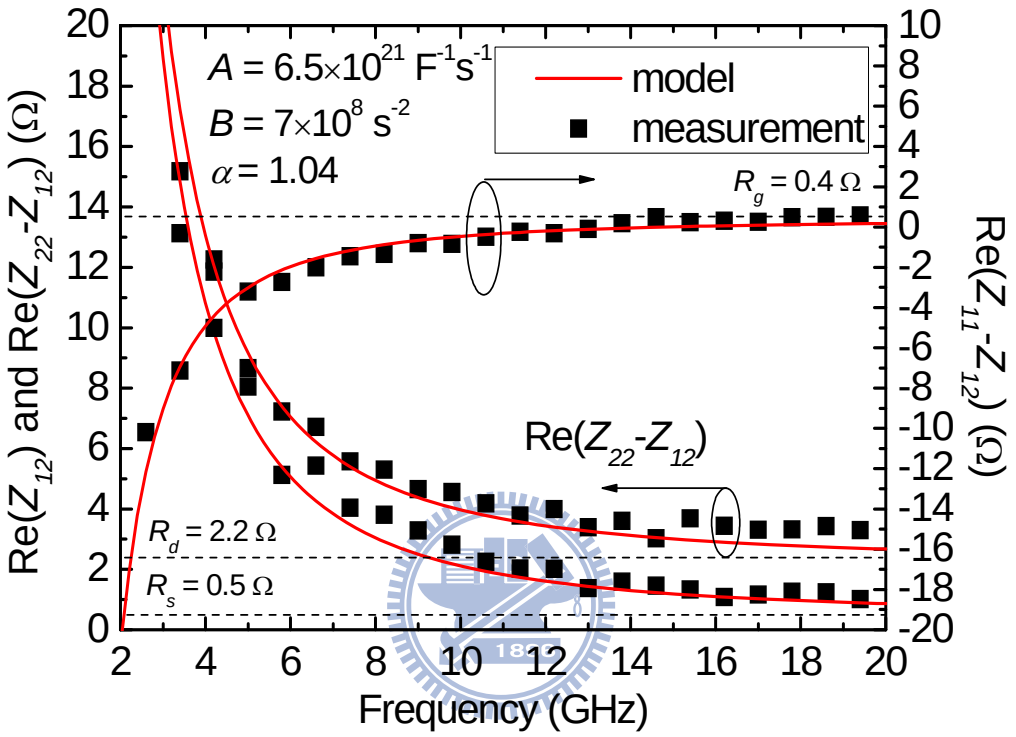


Figure 2-5 Model-data comparison for the extraction of extrinsic resistances. ($L/W_F/N_F/N_G$ = 0.18μm/2.4μm/16/3)

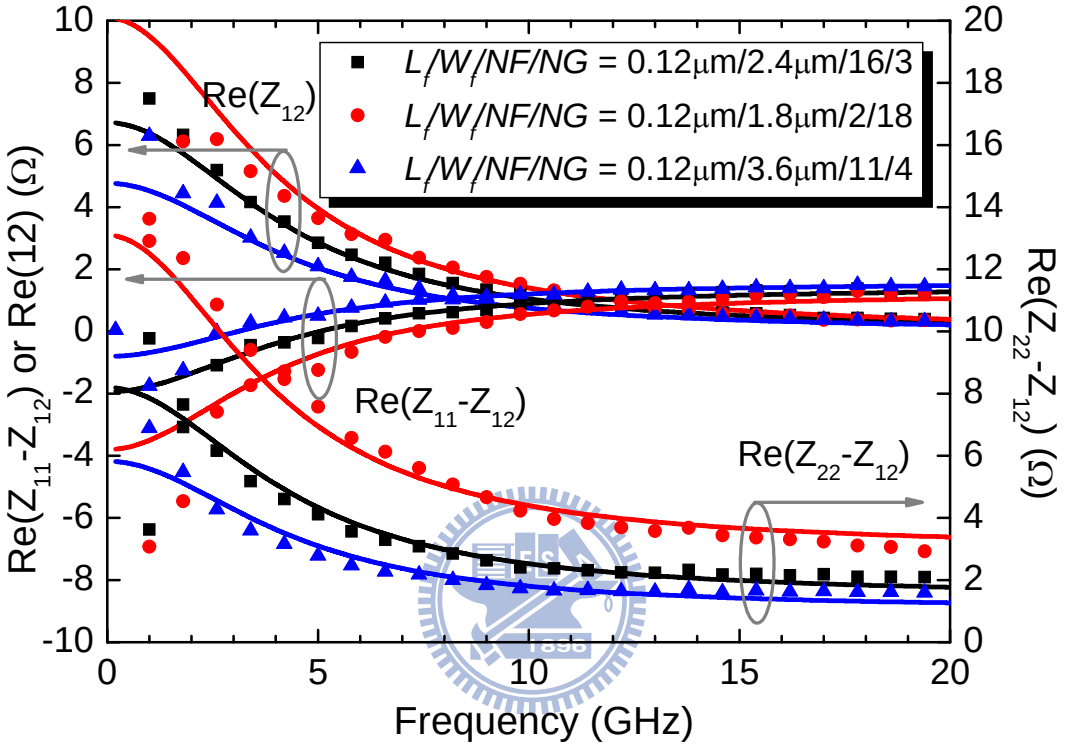


Figure 2-6 Modeling results for extrinsic resistance extraction considering the neutral-body effect. (symbols: measured data; lines: models)

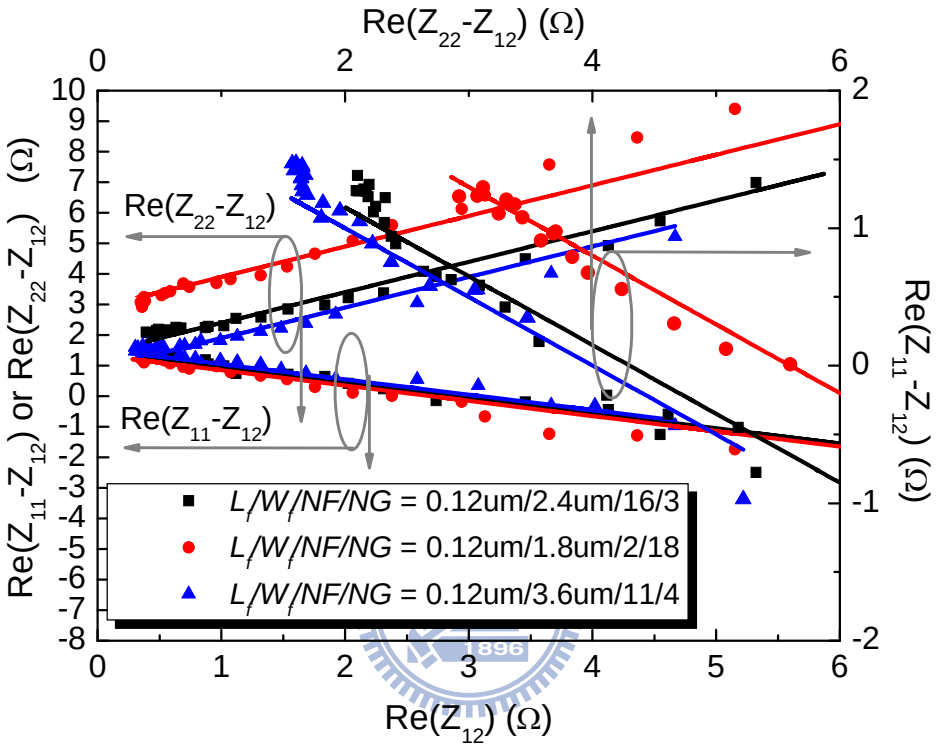


Figure 2-7 Correlation between $\mathrm{Re}(Z_{22}-Z_{12})$, $\mathrm{Re}(Z_{12})$, and $\mathrm{Re}(Z_{11}-Z_{12})$. (symbols: measured data; lines: models)

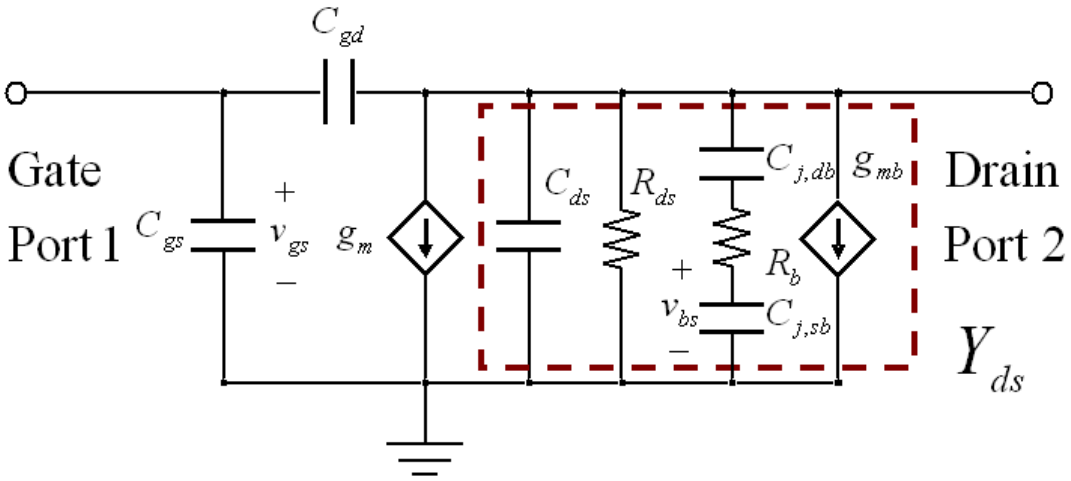


Figure 2-8 Intrinsic small-signal model considering the neutral-body effect for the SOI MOSFET.

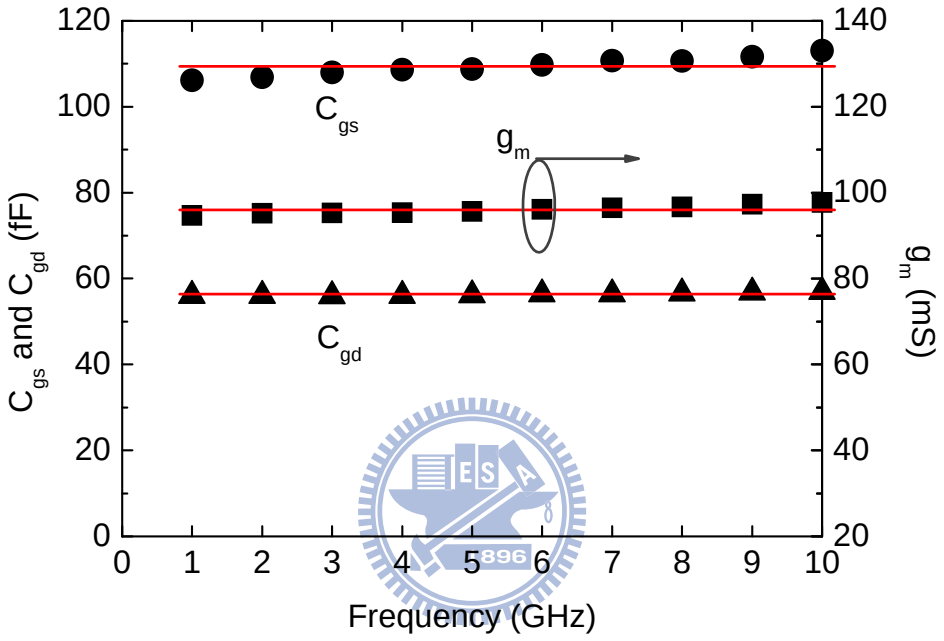
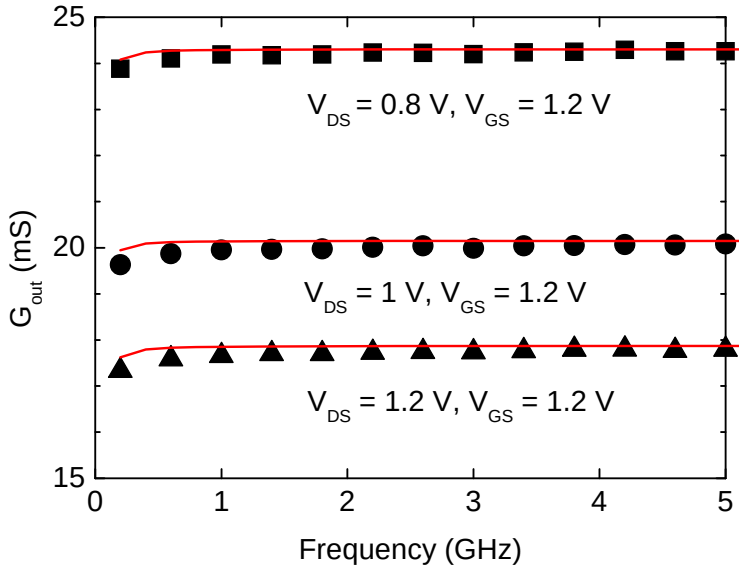
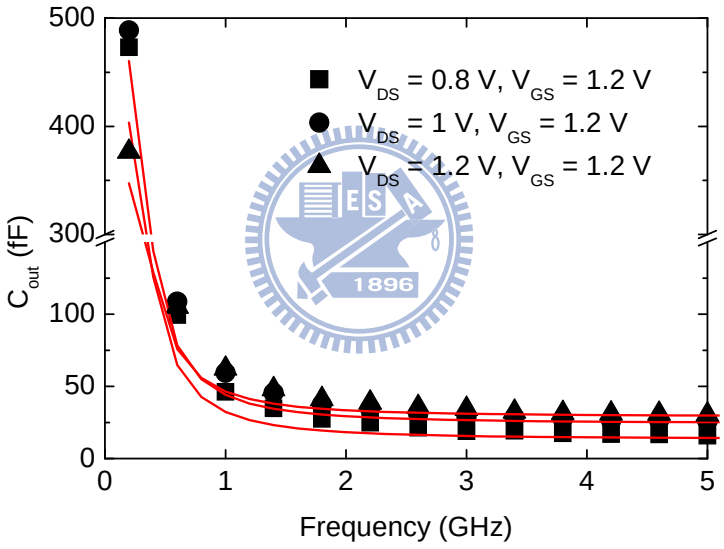


Figure 2-9 Modeling results of C_{gs}, C_{gd} and g_m. (symbols for measured data, lines for models, and $L/W_F/N_F/N_G = 0.12\mu m/3.6\mu m/16/2$)

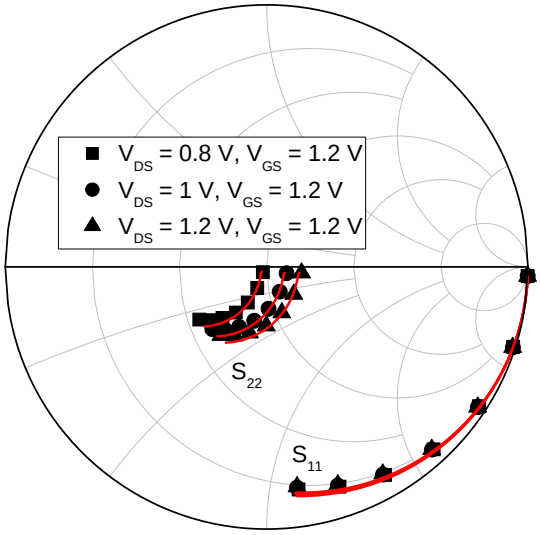


(a)

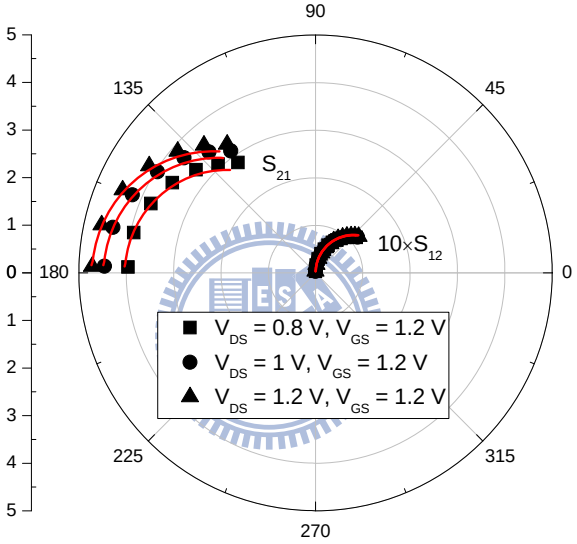


(b)

Figure 2-10 Modeling results of (a) G_{out}, and (b) C_{out}. (symbols for measured data, lines for models, and $L/W_F/N_F/N_G = 0.12\mu m/3.6\mu m/16/2$)

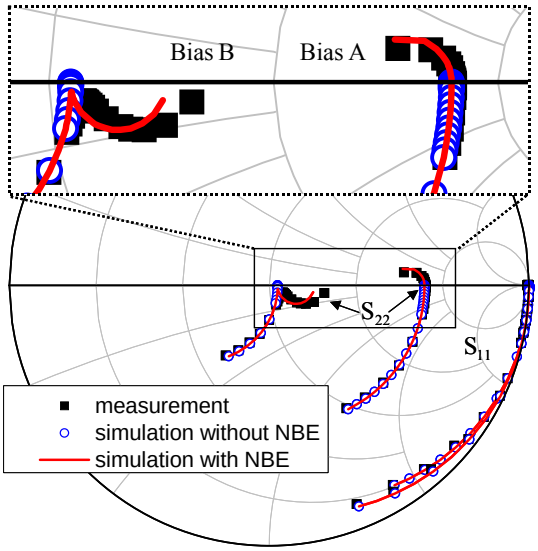


(a)

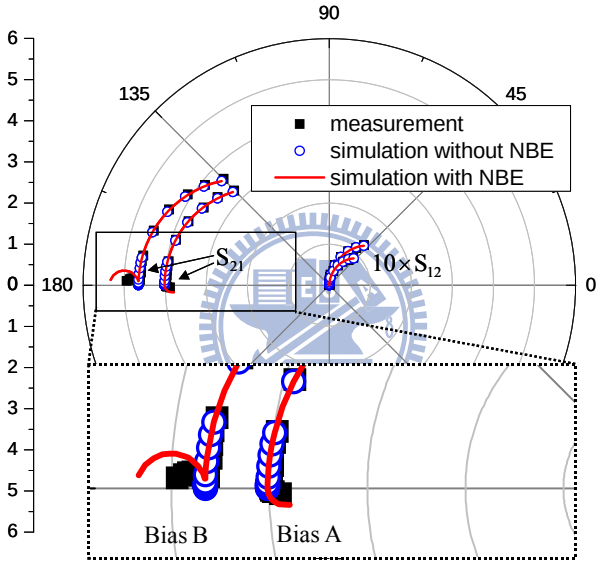


(b)

Figure 2-11 Modeling results of (a) S_{11} and S_{22}, and (b) S_{21} and S_{12}. (frequency: 0.2 ~ 10GHz, symbols for measured data, lines for models, and $L/W_F/N_F/N_G$ = 0.12μm/3.6μm/16/2)



(a)



(b)

Figure 2-12 Modeling results of (a) S_{11} and S_{22}, and (b) S_{21} and S_{12} with and without considering the neutral-body effect (NBE). The anomalous behaviors are highlighted, and the bias conditions for Bias A and B are $V_{GS}=0.4\,\mathrm{V}$, $V_{DS}=1.2\,\mathrm{V}$ and $V_{GS}=1.2\,\mathrm{V}$, $V_{DS}=1.2\,\mathrm{V}$, respectively. (frequency: 1MHz ~ 6GHz, and $L/W_F/N_F/N_G$ = 0.12μm/2.4μm/16/3)

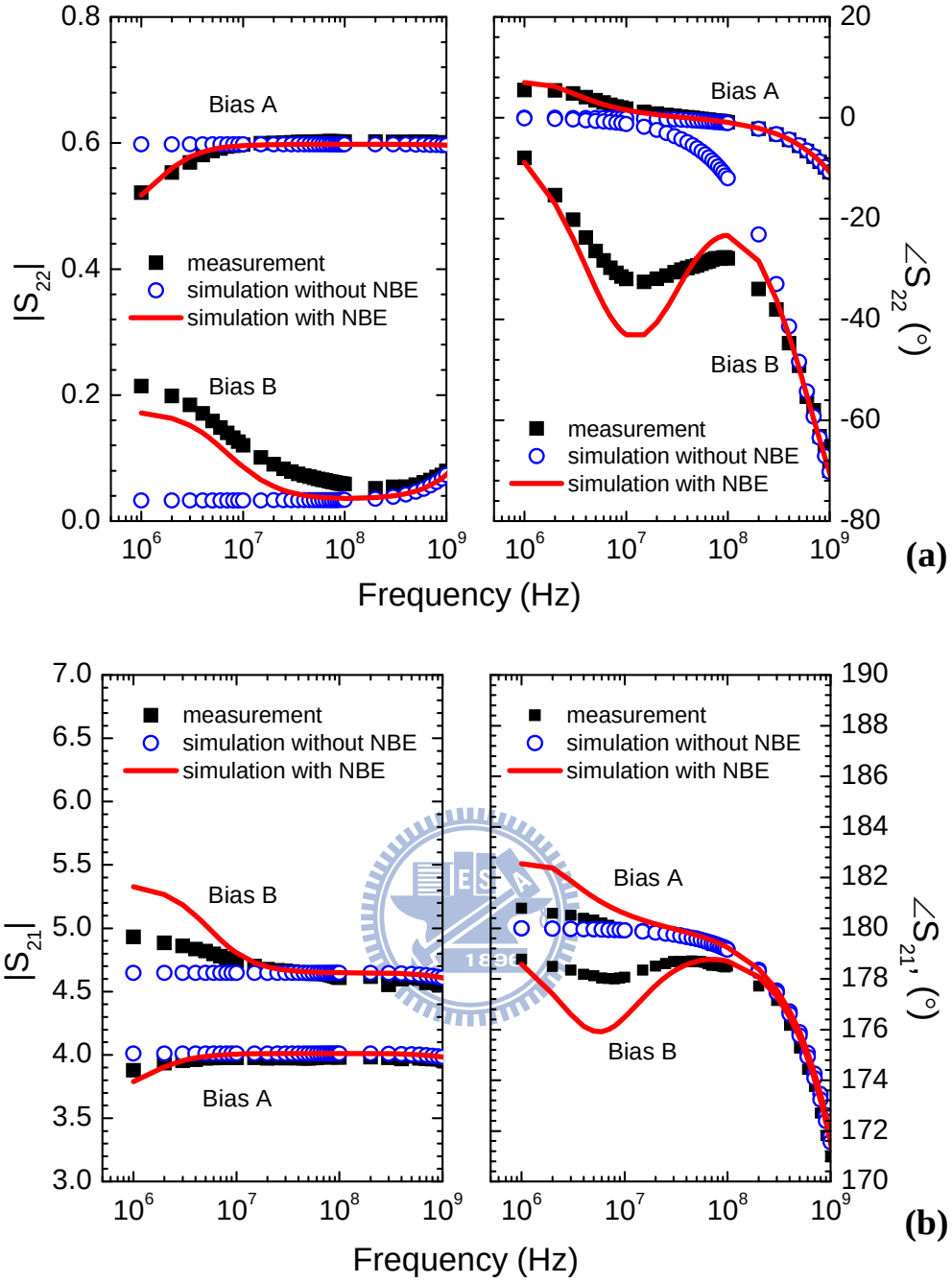


Figure 2-13 Modeling results of (a) $|S_{22}|$ and $\angle S_{22}$, and (b) $|S_{21}|$ and $\angle S_{21}$ with and without considering the neutral-body effect (NBE). The bias conditions for Bias A and B are $V_{GS} = 0.4\,\mathrm{V}$, $V_{DS} = 1.2\,\mathrm{V}$ and $V_{GS} = 1.2\,\mathrm{V}$, $V_{DS} = 1.2\,\mathrm{V}$, respectively. ($L/W_F/N_F/N_G$ = 0.12μm/2.4μm/16/3)

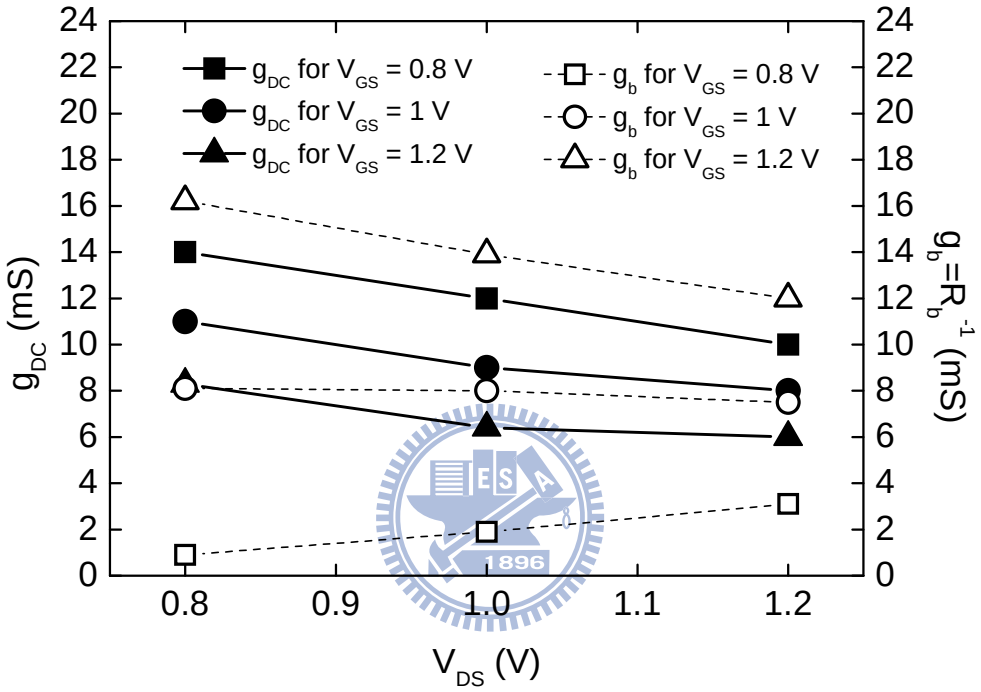


Figure 2-14 g_{DC} and g_b versus V_{DS} for different V_{GS}.

($L/W_F/N_F/N_G$ = 0.12μm/3.6μm/16/2)

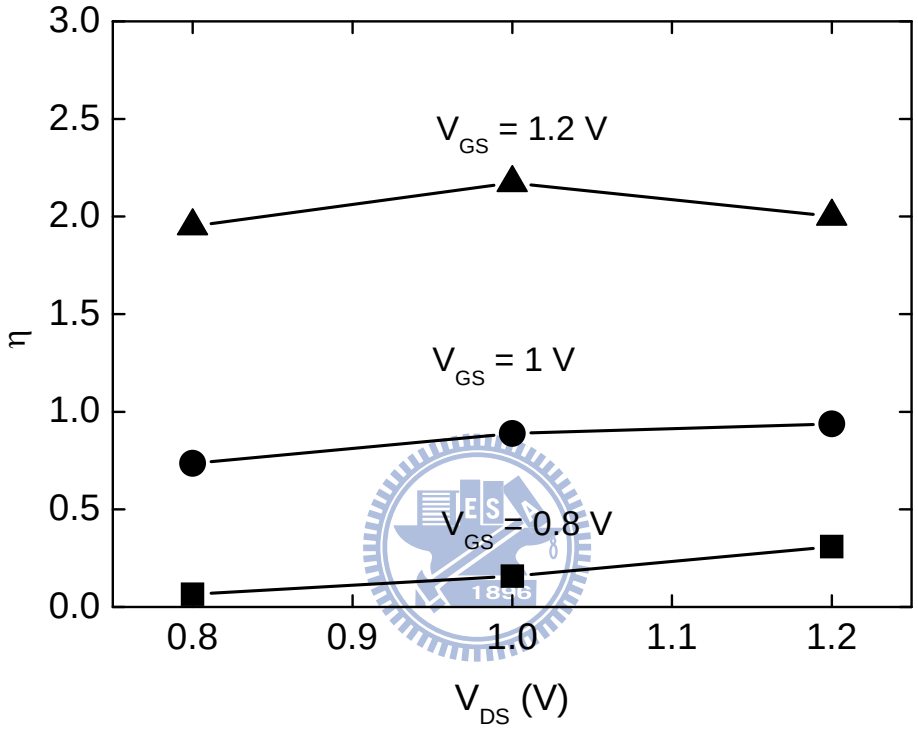


Figure 2-15 η versus V_{DS} for different V_{GS}.

($L/W_F/N_F/N_G$ = 0.12μm/3.6μm/16/2)

Chapter 3

RF Noise Characterization for Bulk and SOI MOSFETs

3.1 Introduction

The noise performance of RF MOSFETs is critical to RF applications, especially to the design of low noise amplifiers, resulting in a need for the accurate noise modeling [1]. Besides, it is well known that both the small-signal circuit parameters and noise sources play important roles in RF noise modeling. There have been many studies on the RF noise characterization and modeling for both bulk and SOI MOSFETs [1]-[9], and the temperature dependence of their small-signal performances has also been widely discussed [10]-[12]. However, the study on the temperature dependence of their RF noise sources and noise parameters was deficient. Therefore, for the purpose of temperature modeling and understanding the underlying physics, the temperature dependence of RF noise behaviors demands investigation.

Pascht *et al.* have presented the temperature noise model by exploiting the circuit simulator [2]. However, only the noise source for the bulk MOSFET has been discussed, and its temperature dependence was not clear. In this chapter, we will experimentally study the temperature dependence of the power spectrum densities (PSDs) of the intrinsic noise sources for both the RF bulk and SOI MOSFETs. The applicability of the popular van der Ziel's model is also checked at different temperatures. Along with the extracted small-signal and noise factor, their temperature dependences can be well described.

3.2 Devices and Experiments

The RF MOSFETs used in this study were fabricated using UMC 0.13 μm bulk and SOI technologies, respectively. All the transistor's finger length, finger number and group number

are fixed to 3.6 μm , 16 and 2, respectively. For SOI MOSFETs, the thicknesses for gate oxide, SOI layer and buried oxide are 1.4 nm, 40 nm, and 200 nm, respectively.

The noise parameters of the device under different temperatures were measured using ATN NP5B noise parameter measurement system. The pads and series parasitics were de-embedded to obtain the intrinsic noise parameters. Then, the intrinsic noise current sources can be extracted by following the approach presented in [3], which is based on the noise matrix manipulation derived from the two-port noise theorem.

3.3 RF Noise Characterization for Bulk MOSFETs

3.3.1 RF Noise Characteristics for Medium-Long Devices

In this sub-section, we will first discuss the RF noise behaviors for the medium-long device ($L = 0.36$ μm) [13].

The van der Ziel's model widely adopted to characterize the PSDs for the drain-induced gate noise (S_{ig}), channel noise (S_{id}), their correlation noise (S_{igd^*}) can be expressed as follows [7][14].

$$S_{ig} = \frac{\overline{i_g i_g^*}}{\Delta f} = \delta 4k_B T \frac{\omega^2 C_0^2}{g_{d0}} \tag{3-1}$$

$$S_{id} = \frac{\overline{i_d i_d^*}}{\Delta f} = \gamma 4k_B T g_{d0} \tag{3-2}$$

$$S_{igd^*} = \frac{\overline{i_g i_d^*}}{\Delta f} = j\varepsilon 4k_B T \omega C_0 \tag{3-3}$$

where C_0 is the intrinsic gate capacitance ($\approx 3C_{gs}/2$), g_{d0} is the channel conductance at zero drain bias, $k_B \approx 1.38\times10^{-23}$ J/K is Boltzmann constant, and T is the ambient temperature in Kelvin. A fairly good data-model comparison of S_{ig}, S_{id} and S_{igd^*} for $L = 0.36$ μm device biased at $V_{GS} = V_{DS} = 1.2$V can be obtained and are shown in Figs. 3-1

to 3-3, respectively.

In these figures, one can find that S_{ig} and S_{igd^*} would become larger for higher ambient temperature. For S_{id}, however, it tends to decrease with increasing temperature. To explain these different trends, Table 3-1 lists the extracted C_0, g_{d0} and their normalizations with respect to their cases at $-40℃$. Besides, the extracted model parameters δ, γ and ε for different temperatures are also shown in Fig. 3-4. It is also worth noting that the van der Ziel's model was originally derived for long channel devices, and the model parameters should be $\delta_{sat} = 16/135$, $\gamma_{sat} = 2/3$, and $\varepsilon_{sat} = 1/9$ in the saturation region. It is no surprise that for the short channel device as in our study, the parameters could deviate from these theoretical values [3]-[5].

The small variations for δ, γ and ε shown in Fig. 3-4 reveal that they are less temperature-dependent, and may not be the main contribution to the temperature dependence of these three PSDs. In addition, C_0 in Table 3-1 is shown to be insensitive to temperature. Therefore, for a given operating frequency, the following approximations can be achieved.

$$S_{ig} \propto \frac{T}{g_{d0}} \tag{3-4}$$

$$S_{id} \propto T g_{d0} \tag{3-5}$$

$$S_{igd^*} \propto T \tag{3-6}$$

Equation (3-6) directly captures the positive temperature coefficient observed for S_{igd^*}.

On the other hand, as temperature increases, the channel mobility would decline [10], causing g_{d0} to decrease with increasing temperature as shown in Table 3-1. This explains the positive temperature coefficient for S_{ig} (Equ. (3-4)). Moreover, since the decrease of g_{d0} overwhelms the increase of ambient temperature in Kelvin (Table 3-1), S_{id} would have negative temperature coefficient (Equ. (3-5)). Besides, the correlation coefficient between noise currents $\overline{i_g}$ and $\overline{i_d}$ (denoted as c) can be expressed as

$$c \equiv \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g i_g^*} \cdot \overline{i_d i_d^*}}} = j\frac{\varepsilon}{\sqrt{\delta\gamma}} \quad . \tag{3-7}$$

Since δ, γ and ε are shown to be less temperature-dependent, the temperature dependence of c shown in Fig. 3-4 is also weak.

Finally, the extracted values for the model parameters and the correlation coefficient for various gate and drain biases are shown in Figs. 3-5 (a)~(d). It suggests that in the wide temperature range between -40℃ and 200℃, δ, ε, and c/j have a larger temperature dependence at higher V_{GS}, while γ has a larger temperature dependence only for a lower V_{GS}.

3.3.2 RF Noise Characteristics for Deep-Submicron Devices

We now turn to investigate the RF noise behaviors for deep-submicron MOSFETs. Since compared to the channel noise, both the drain-induced gate noise and the correlation noise between them have been shown to play an insignificant role in determining the high-frequency noise behaviors for devices down-scaled into/beyond deep-submicron regime [15], we will limit our studies on the channel noise source only.

Figure 3-6 shows the temperature dependence of noise factor γ for devices with different channel lengths. One can see that the temperature dependence is weak even for $L = 0.12\mu m$ device biased at high V_{GS}. This indicates that g_{d0}'s temperature dependence is still the major factor determining the temperature dependence of channel noise S_{id} as suggested by Equ. (3-5). For $L = 0.12\mu m$ device, since g_{d0} does not decrease with temperature as much as that for both $L = 0.24\mu m$ and $L = 0.36\mu m$ devices (shown in Fig. 3-7), instead of decreasing with temperature, the channel noise relatively remains constant over the whole temperature range as shown in Fig. 3-8.

The minimum noise figure ($NF_{\min}$) and the equivalent noise resistance (R_n) are two important figures of merit (FOM) used to judge the noise performance of a device, and can be respectively written as [15][16]:

$$NF_{\min} \approx 1 + \frac{2}{g_m^2}\sqrt{(R_s + R_g)\frac{S_{id}}{4kT_0}} \times \left\{ \omega C_{gg} g_m + \omega^2 C_{gg}^2 R_g \sqrt{\frac{S_{id}}{4kT_0}} \right\} \quad (3\text{-}8)$$

$$R_n \approx \frac{T}{T_0}(R_g + R_s) + \frac{S_{id}}{4k_B T_0 g_m^2} \quad (3\text{-}9)$$

Note that in the above derivation, we have neglected the contribution from S_{ig} and S_{igd}.

From Equs. (3-8) and (3-9), we can see that except S_{id}, the trans-conductance g_m would play an important role in determining both intrinsic $NF_{\min}$ and R_n. The temperature dependence of g_m for devices with different channel lengths is shown in Fig. 3-9. It suggests that g_m decreases with temperature at a rate larger than that for S_{id}. Therefore, according to Equs. (3-8) and (3-9), both $NF_{\min}$ and R_n would tend to degrade and become larger with increasing temperature as shown in Figs. 3-10 (a) and (b), respectively.

3.4 RF Noise Characterization for SOI MOSFETs

Figure 3-11 shows the noise factor γ for both the bulk and SOI devices. It shows that, in the medium-long channel devices ($L = 0.36\mu m$), γ seems to remain the same for both SOI and bulk devices. However, the SOI devices would have an increasing γ as the channel length shrinks. Two mechanisms may contribute to this phenomenon: floating body effect (FBE) and self-heating effect (SHE) [20]. Due to the floating body structure of the SOI nMOSFET, there is a potential barrier between the source and the body region. Therefore, the holes generated by impact ionization [19] at high drain bias condition can be easily trapped in the body volume, and the body potential can rise [17][20]. The elevated body potential would in turn lower the effective threshold voltage, and accordingly increase the gate overdrive voltage ($V_{GT} = V_{GS} - V_T$). Then, a more conductive channel and hence larger S_{id} can be expected. According to van der Ziel's model (Equ. (3-2)), a larger γ can be obtained using lower g_{d0} extracted at zero drain bias, where FBE is negligible. Besides, due to the more substantial impact ionization current induced by the larger maximum channel electric field

[19] at lower V_{GS} ($\approx V_{dd}/2$), FBE would have a larger impact on the excess noise at lower V_{GS}.

On the other hand, as V_{GS} increases, the DC power and therefore the temperature of the SOI MOSFET increases due to the so-called self-heating effect [18][19]. This effect is caused by poor thermal conductivity of the buried oxide, which is about two orders of magnitude less than that of the silicon [18][19], and the lattice temperature would play an important role in determining the SOI MOSFET noise characteristics [8]. Besides, the noise arising from the neutral-body resistance should be enhanced by the elevated lattice temperature and its contribution to the channel noise S_{id} may have to be considered. However, since the effective mobility and hence channel conductance should be decreased accordingly, the excess noise caused by SHE would partly counterbalanced by the reduction of channel conductance. This captures the slight increase of γ at high V_{GS} (see Equ. (3-2)). It is worth noting that since the SHE may reduce the body potential by inducing more diode leakage [20], the excess noise caused by FBE at high V_{GS} could be further alleviated.

Figure 3-12 shows the temperature dependence of γ for both SOI and bulk devices. Since the FBE can be eliminated at high temperature [17], the channel suffering less FBE would have decreasing γ with increasing temperature. This is especially obvious at low V_{GS}, where FBE dominates the excess channel noise behavior. For bulk devices, since they suffer neither FBE nor SHE, they have the similar γ over the whole temperature region.

Finally, we compare $NF_{\min}$ and R_n for the SOI and bulk devices for a given DC power consumption. Figure 3-13(a) and (b) respectively show the comparison of S_{id} and g_m versus current for a given drain voltage ($V_{DS} = 1.0\text{V}$). Because SOI device has larger S_{id} and lower g_m than the bulk counterparts in our experiments, referring to Equs. (3-8) and (3-9), it is expected that it would has worse $NF_{\min}$ and R_n as shown in Fig. 3-14(a) and (b), respectively. It is worth noting that the extrinsic parameters, such as gate capacitance and terminal resistances would not significantly contribute to the deviations, since both devices

have been checked to have similar C_{gg} (see Fig. 3-13(c)) and terminal resistances (shown in Table 3-2) for each temperature.

It should be noted that we have neglected the neutral-body effect on the RF characterization in this section. This is because the previous chapter has demonstrated the insignificant neutral-body effect on the RF small-signal characteristics of SOI MOSFETs except the output admittance. Besides, the body trans-conductance and drain leakage current have been presented to have significant effect mostly on the low frequency noise behavior due to its low-pass nature [21]. Note that at the very high frequency, the neutral-body resistance R_b would be equivalently parallel to the channel resistance and can contribute to the output noise current associated with the drain terminal. However, its thermal noise contribution is at the level of about $4k_BT/R_b \approx 1.66\times10^{-22}\,\mathrm{A^2/Hz}$ (for $R_b \approx 100\Omega$), and can be neglected compared with the extracted S_{id} (see Fig. 3-13(a)).

3.5 Summary

We have investigated the temperature dependence of S_{ig}, S_{id} and S_{igd*} for the medium-long RF MOSFET. S_{ig} and S_{igd*} are found to have positive correlation with ambient temperature, while S_{id} has negative one due to much lower channel conductance at higher temperature. For $L = 0.12\mu\mathrm{m}$ device, however, since g_{d0} does not decrease with temperature as much as that for both $L = 0.24\mu\mathrm{m}$ and $L = 0.36\mu\mathrm{m}$ devices, S_{id} relatively remains constant over a large temperature range.

For SOI MOSFETs, the FBE and SHE may contribute to the higher noise factors compared to the bulk counterparts. The FBE dominates at low V_{GS} regime, and can be suppressed by elevating the temperature. At high V_{GS} regime, where the SHE is significant, the excess noise contribution from the elevated lattice temperature would be partly counterbalanced by the lowered channel conductance. Therefore, compared to the FBE, its

contribution to S_{id} may not be significant.

Finally, since the trans-conductance decreases with temperature in a rate higher than that for S_{id}, both $NF_{\min}$ and R_n would increase accordingly. Our experiment also shows that the SOI device has worse $NF_{\min}$ and R_n due to the larger S_{id} and lower g_m than the bulk counterpart.

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Table 3-1 Extracted g_{d0}, C_0 and their normalizations with respect to cases at -40℃ for the bulk MOSFET. ($L = 0.36$ μm)

	$T(\mathrm{K})$	$\|T(\mathrm{K})\|$	$g_{d0}(\mathrm{mS})$	$\|g_{d0}\|$	$C_0(\mathrm{fF})$	$\|C_0\|$
$T = -40$ ℃	233	× 1	112.4	× 1	520	× 1
$T = 0$ ℃	273	× 1.17	96	× 0.85	517	× 0.99
$T = 100$ ℃	373	× 1.60	66	× 0.59	508	× 0.98
$T = 200$ ℃	473	× 2.03	51	× 0.45	506	× 0.97

Table 3-2 Extracted R_s, R_d, and R_g for both the SOI and bulk devices. ($L = 0.12$ μm)

	SOI			BULK		
	$R_s(\Omega)$	$R_d(\Omega)$	$R_g(\Omega)$	$R_s(\Omega)$	$R_d(\Omega)$	$R_g(\Omega)$
$T = 23$ ℃	0.1	1.7	1.9	0.1	1.5	2.0
$T = 100$ ℃	0.1	1.8	2.2	0.1	1.8	2.2
$T = 200$ ℃	0.1	2.2	2.3	0.1	2.0	2.5

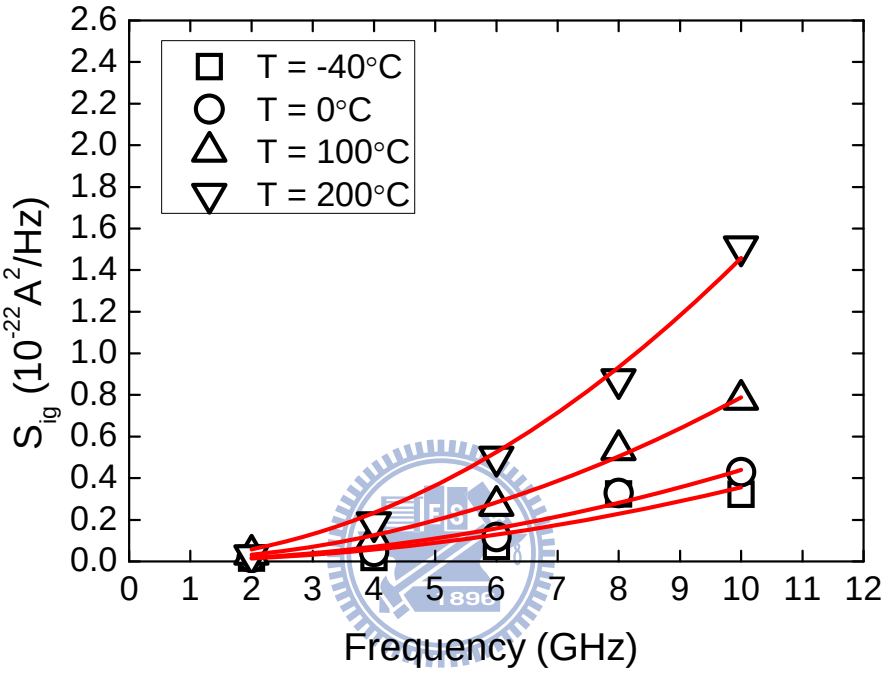


Figure 3-1 Induced gate noise (S_{ig}) versus frequency for the bulk MOSFET under different temperatures. ($L = 0.36$ μm , and $V_{GS} = V_{DS} = 1.2\text{V}$)

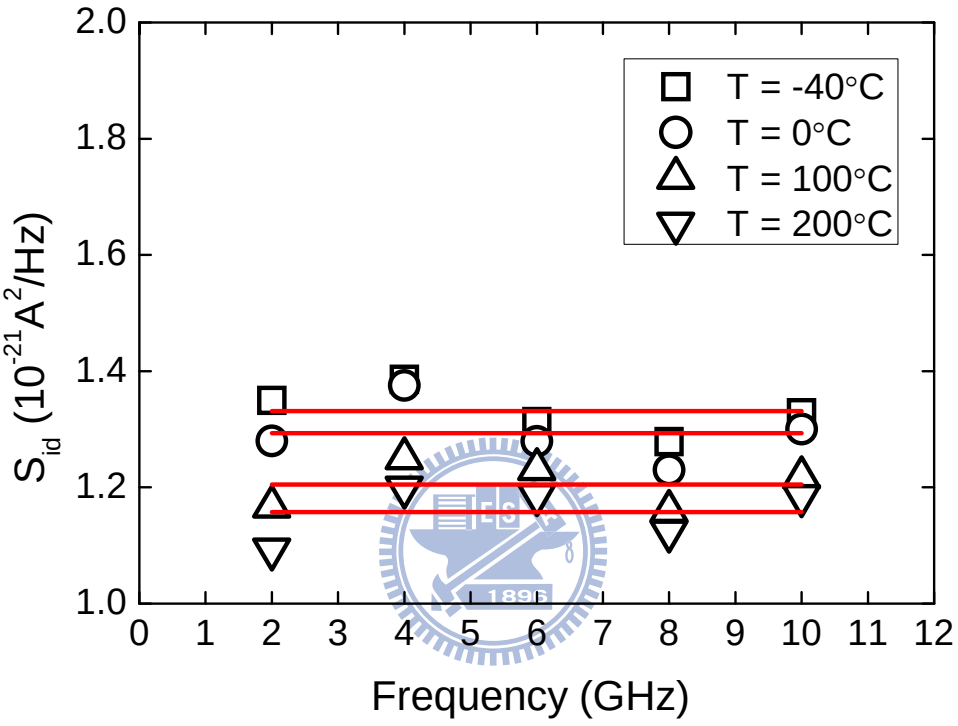


Figure 3-2 Channel noise (S_{id}) versus frequency for the bulk MOSFET under different temperatures. ($L = 0.36$ μm, and $V_{GS} = V_{DS} = 1.2\text{V}$)

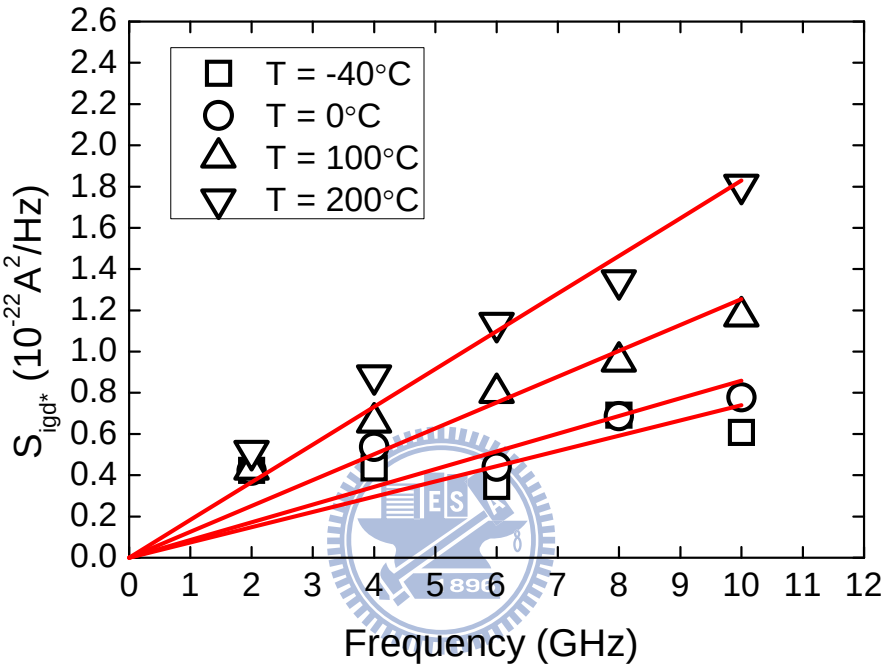


Figure 3-3 Correlation noise (S_{igd^*}) versus frequency for bulk MOSFET under different temperatures. ($L = 0.36$ μm, and $V_{GS} = V_{DS} = 1.2\text{V}$)

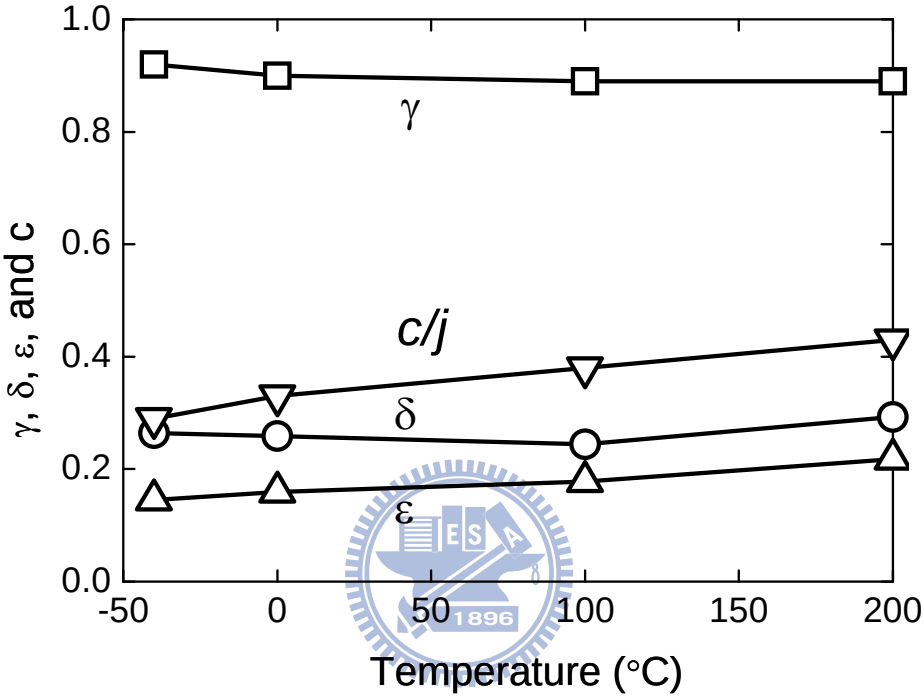


Figure 3-4 Model parameters δ, γ, ε and correlation coefficient c versus temperature for the bulk MOSFET. ($L = 0.36$ μm, and $V_{GS} = V_{DS} = 1.2\text{V}$)

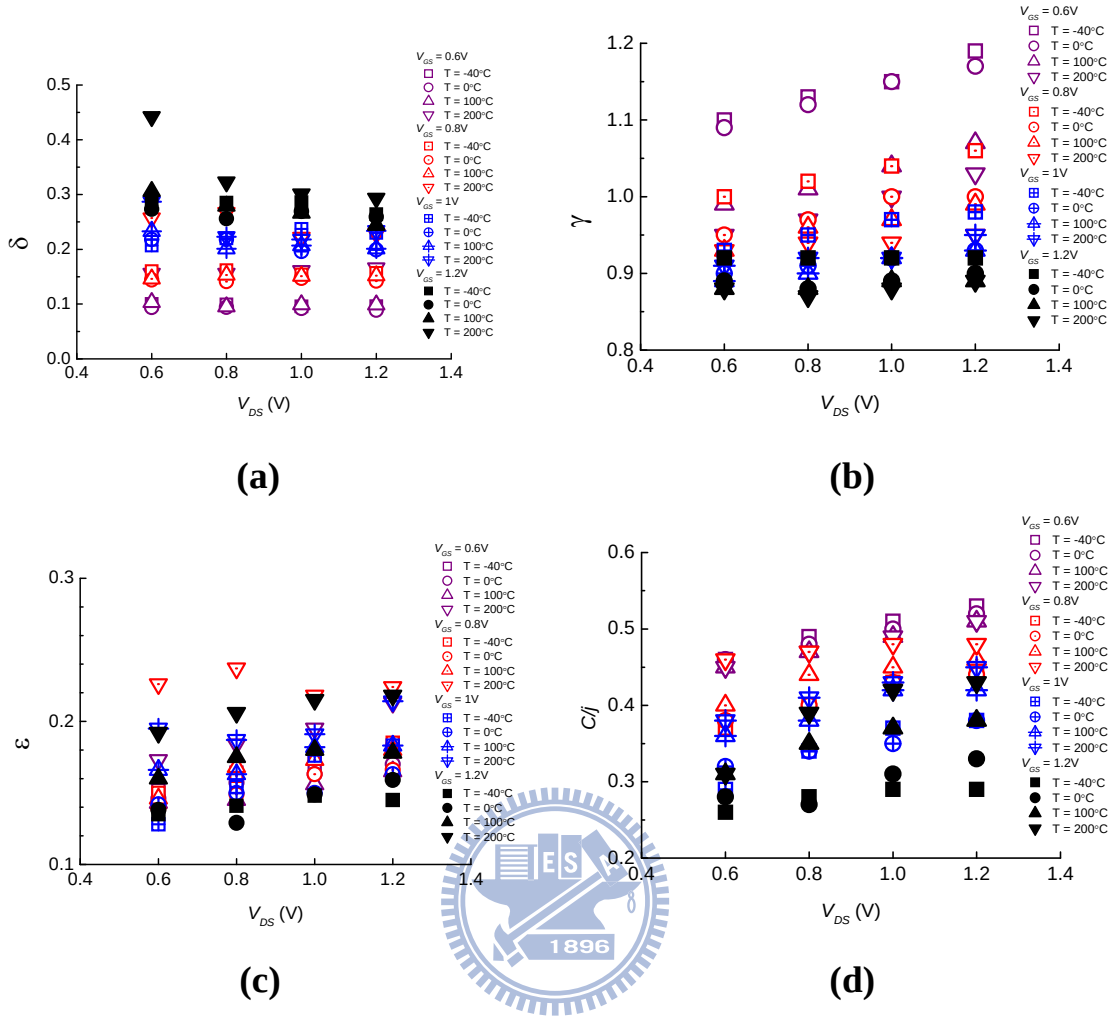


Figure 3-5 Noise model parameters (a) δ, (b) γ, (c) ε, and (d) c/j versus drain bias for different temperature and gate bias conditions for the bulk MOSFET. ($L = 0.36$ μm)

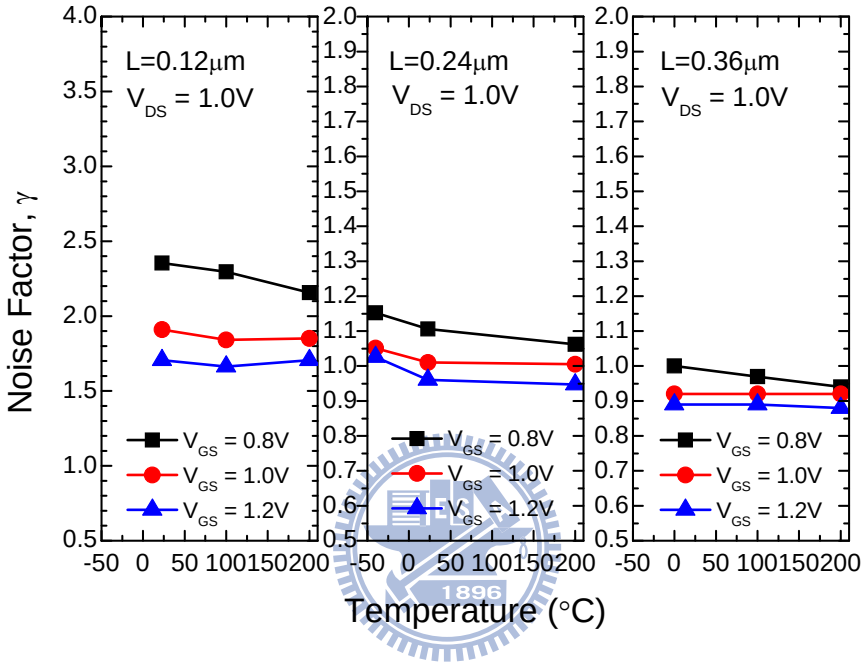


Figure 3-6 Temperature dependence of γ for bulk devices with different channel lengths.

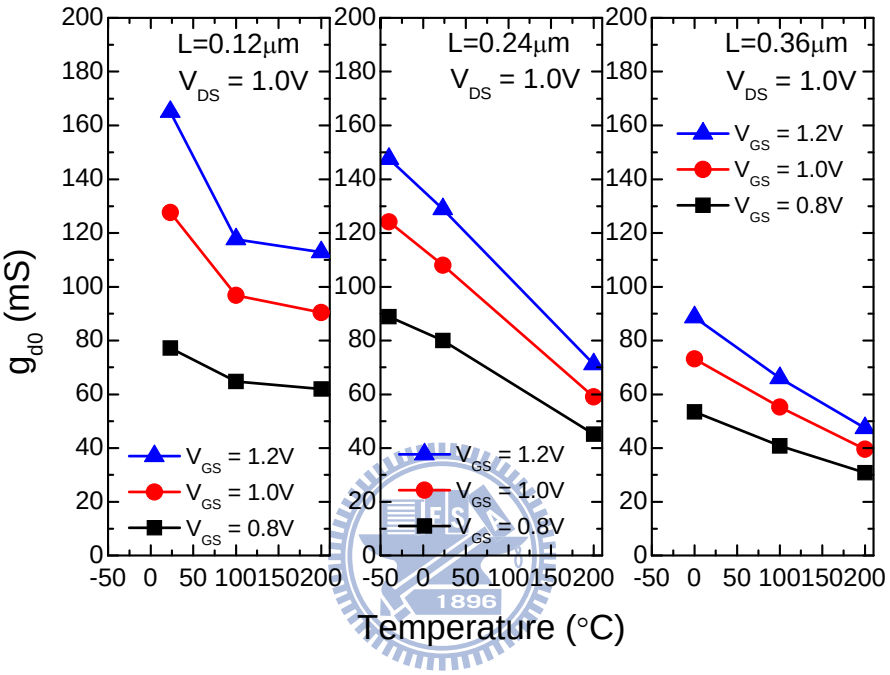


Figure 3-7 Temperature dependence of g_{d0} for bulk devices with different channel lengths.

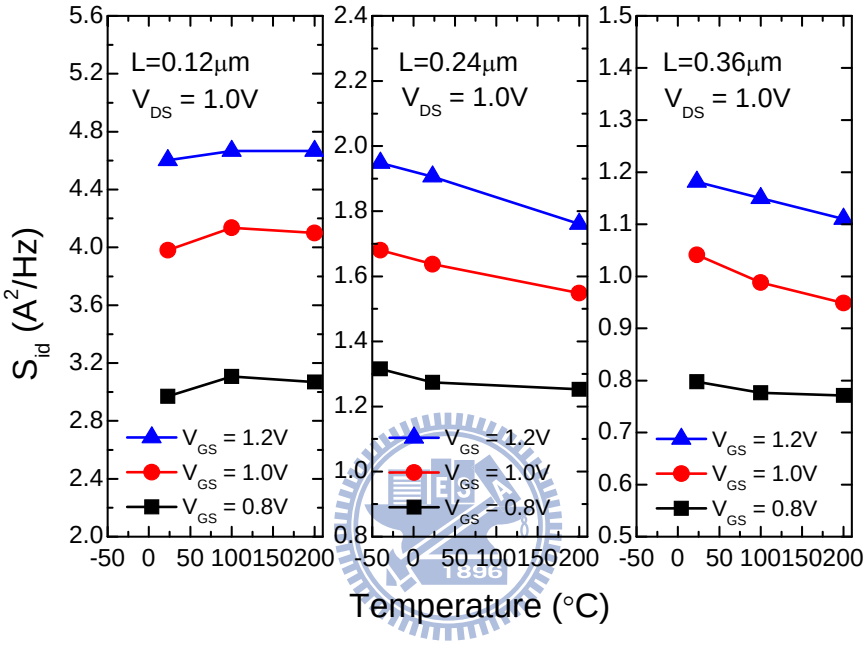


Figure 3-8 Temperature dependence of S_{id} for bulk devices with different channel lengths.

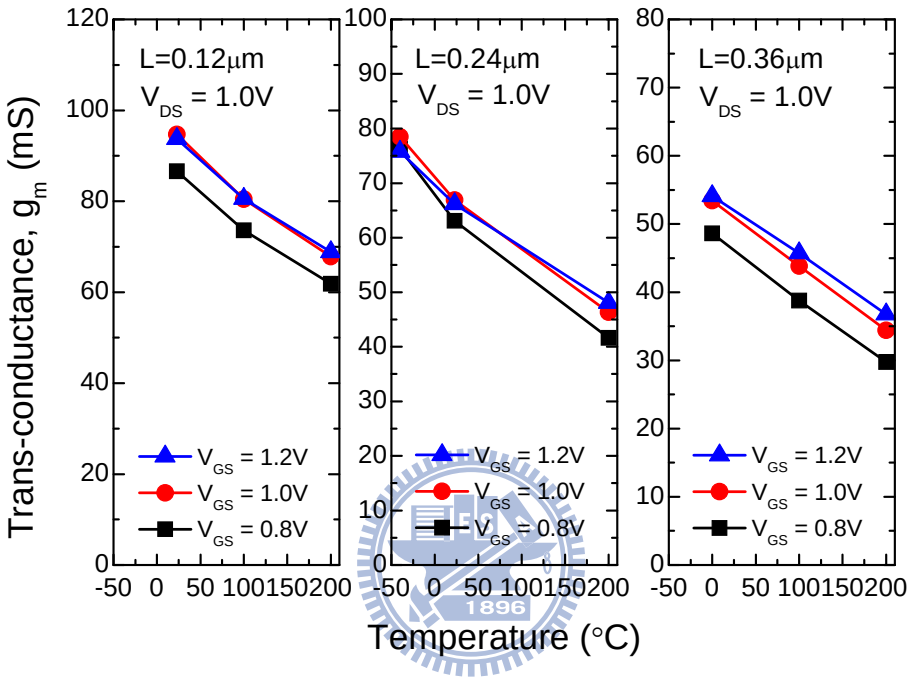
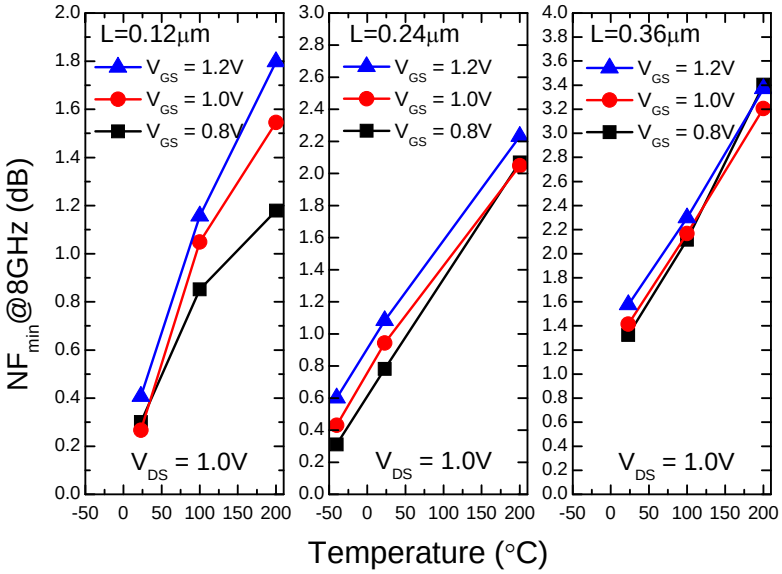
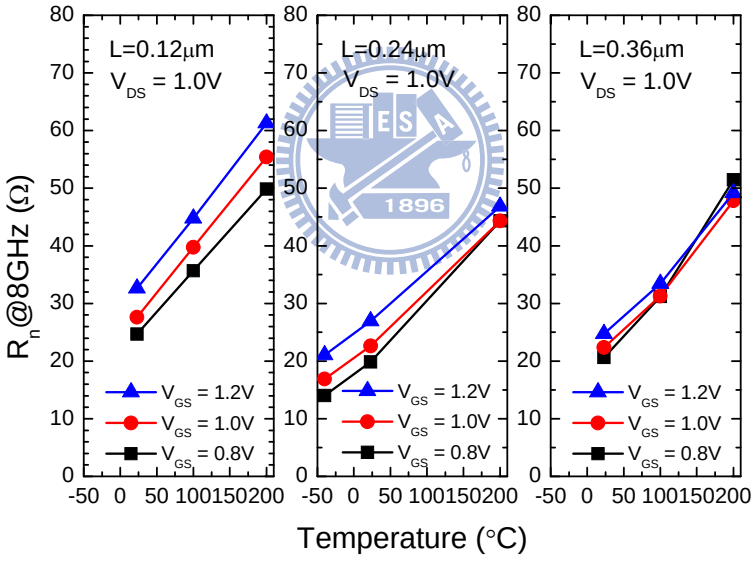


Figure 3-9 Temperature dependence of g_m for bulk devices with different channel lengths.



(a)



(b)

Figure 3-10 Temperature dependence of (a) $NF_{\min}$ and (b) R_n for bulk devices with different channel lengths.

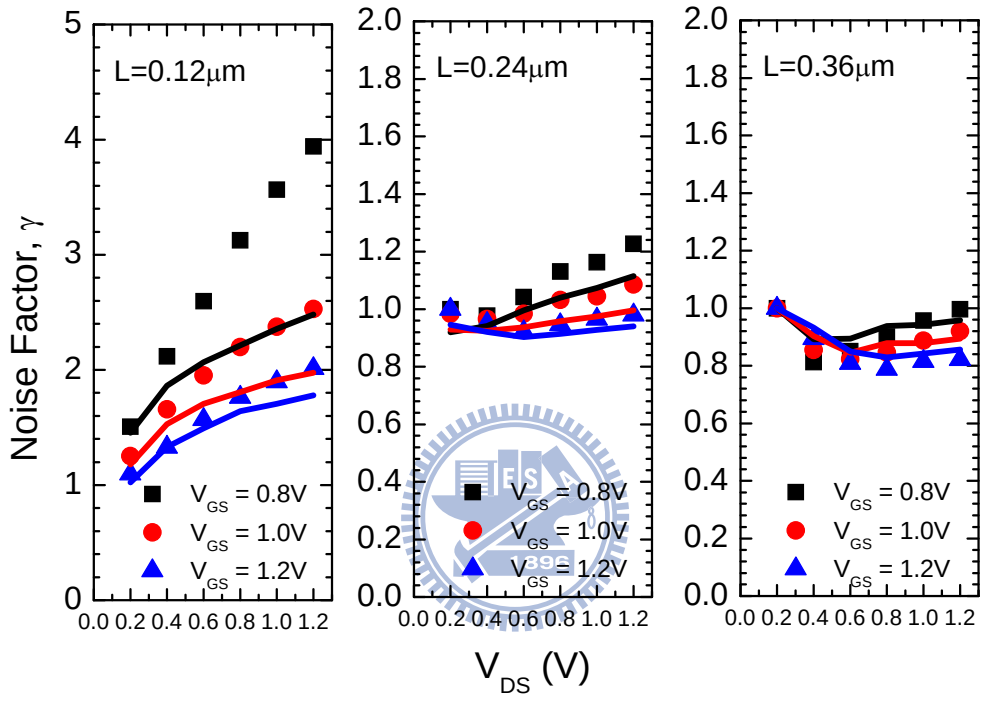


Figure 3-11 Noise factor γ for both SOI (symbols) and bulk (lines) devices with different channel lengths.

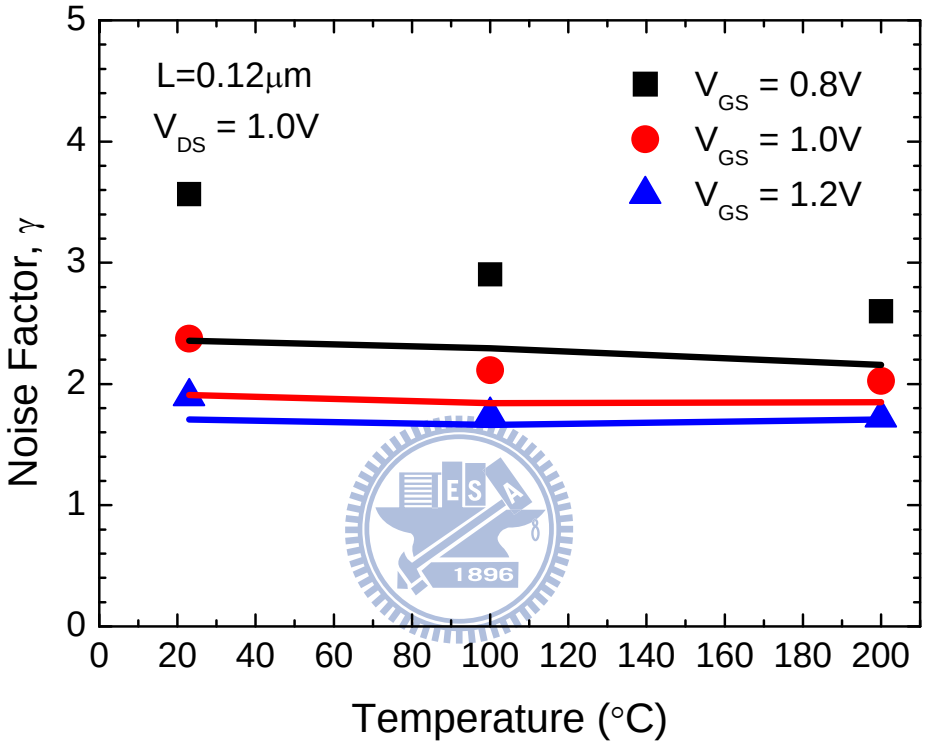
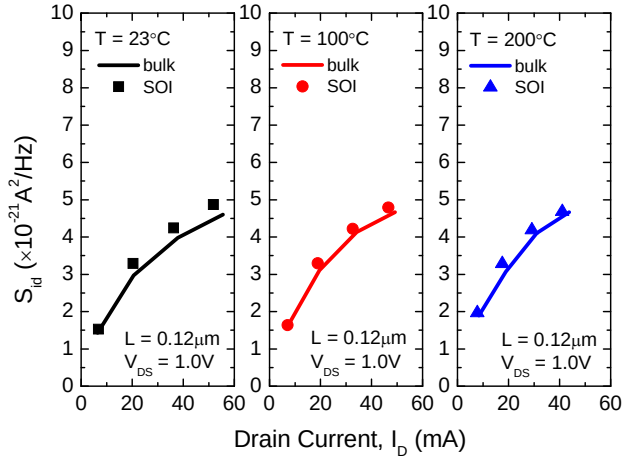
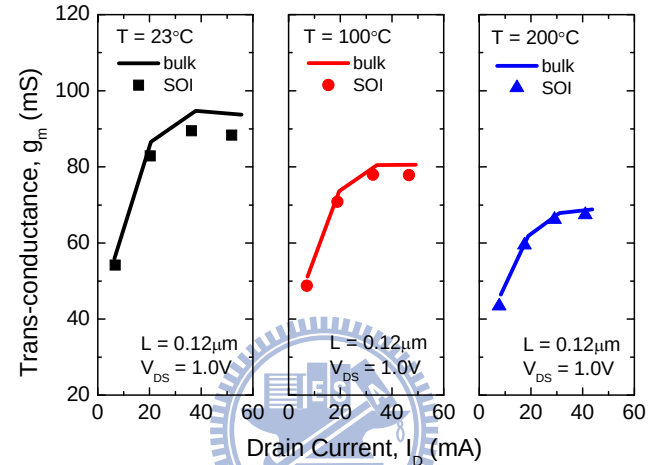


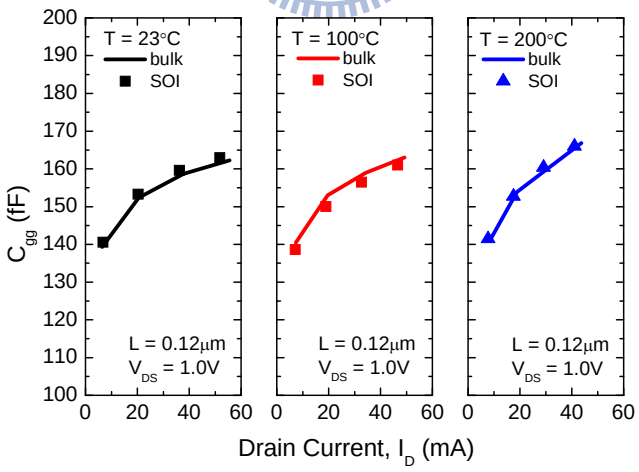
Figure 3-12 Temperature dependence of noise factor γ for both SOI (symbols) and bulk (lines) devices.



(a)

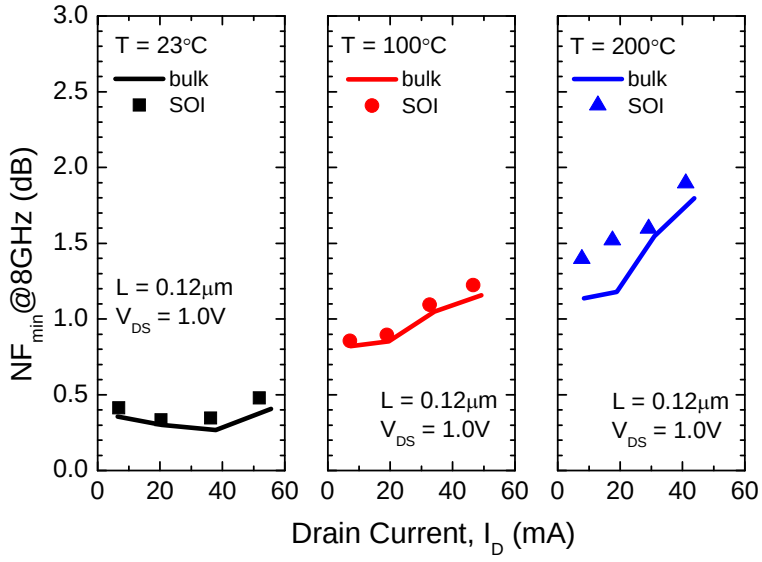


(b)

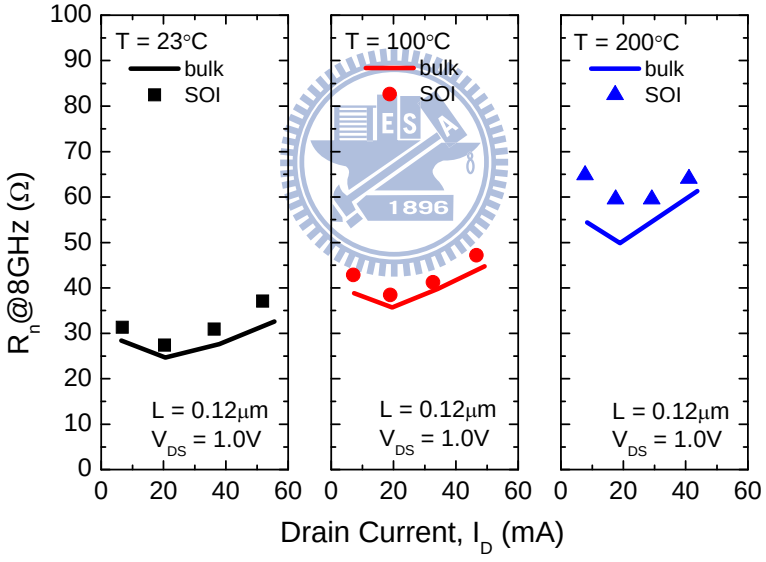


(c)

Figure 3-13 The comparison of (a) S_{id}, (b) g_m, and (c) C_{gg} versus drain current between the bulk and SOI MOSFETs. (V_{DS} = 1.0V)



(a)



(b)

Figure 3-14 The comparison of (a) $NF_{\min}$, and (b) R_n versus drain current between the bulk and SOI MOSFETs. ($V_{DS} = 1.0\text{V}$)

Chapter 4

RF Noise Modeling and Characterization for SOI Dynamic Threshold Voltage MOSFETs

4.1 Introduction

Due to its larger current driving ability with low leakage current, the dynamic threshold voltage (DT) MOSFET is attractive for low power applications [1]. Hence, the DC characteristics and modeling of the DT MOSFET have been widely studied since its introduction [2]-[4]. Moreover, the temperature effect on its DC characteristic has also been well investigated [4].

Several optimized SOI- or bulk-based DT MOS fabrication processes with improved performance have been demonstrated [5][6], and its ability of radio-frequency (RF) applications with high cut-off frequency (f_t) and maximum oscillation frequency ($f_{\max}$) has been reported as well [7]-[9]. However, the temperature effect on the RF characteristics of DT MOSFETs is rarely known.

In this chapter, we will first conduct RF small-signal modeling for the SOI DT MOSFET and demonstrate a practical extraction method to facilitate the extraction work with physical accuracy. Based on the small-signal model structure, the RF noise model for the DT MOSFET will be built, and this model is shown to well capture its RF noise behavior. Besides, the accuracy of some important model parameters will be examined by comparing them to those of the standard conventional devices with different channel lengths at various bias conditions. Finally, we will give an experimental investigation on the RF small-signal and noise characteristics of SOI DT MOSFETs, including their temperature dependences [10]. To avoid a large leakage current flowing through the source-body junction, a DT MOSFET is usually biased in the low gate overdrive (V_{GT}) region. Therefore, we will be dedicated to examining the RF small-signal and noise characteristics under this regime.

4.2 Devices and Experiments

The RF SOI DT MOSFETs used in this work were fabricated using UMC 65nm SOI technology. These RF devices were laid out in the multi-finger and multi-group structure with the following denotations: L for channel length, W_F for finger length, N_F for the number of fingers, and N_G for the number of groups (total gate width $W = W_F \times N_F \times N_G$).

On-wafer 2-port common-source high frequency S and noise parameters were measured using ATN NP5B noise measurement system with Cascade microwave probes. Besides, to eliminate the inevitable parasitic accompanied with the probing pads, the S parameters of devices' corresponding open dummy were measured and then used to perform the S and noise parameters de-embedding procedure.

Figure 4-1 shows the temperature dependences of threshold voltage (V_T) extracted by the constant current ($I_{th} \equiv 50\,\text{nA} \times W/L$) method. Due to the negative temperature coefficient of the device's Fermi potential [4], V_T has the negative temperature dependence for devices with different channel lengths.

4.3 RF Small-Signal and Noise Modeling

The RF small-signal and noise equivalent circuit suitable for the DT MOSFET modeling and characterization will be described in this section. Then, a set of simple and analytic expressions of Y parameters beneficial to the model parameter extraction will be presented accordingly [11].

4.3.1 Equivalent Circuit and Model Parameter Extraction

The small-signal equivalent circuit for SOI DT MOSFETs is depicted in Fig. 4-2 [12]. The series resistances were determined using the proposed zero method [13], and the good extraction results can be found in Fig. 4-3. For simplification, the neutral-body resistance between the two junction capacitances is ignored [14]. Based on this circuit, its simple and

analytic two-port admittance (Y) parameters can be derived when the effect of series resistances compared to access body resistance (R_b) can be neglected. Following especially shows the expressions benefiting the parameter extraction:

$$\mathrm{Re}(Y_{11}) \approx \frac{(R_b + R_{j,sb}) + \omega^2 \Delta^2 / R_b}{den} \tag{4-1}$$

$$\frac{\mathrm{Im}(Y_{11})}{\omega} \approx (C_{gs} + C_{gd}) + \frac{\Delta^2 / [R_b^2 (C_{j,sb} + C_{j,db})]}{den} \tag{4-2}$$

$$\mathrm{Re}(Y_{gain}) \approx \mathrm{Re}(Y_{21} - Y_{12}) = g_m + \frac{g_{mb} \Delta (R_b + R_{j,sb}) / [R_b (C_{j,sb} + C_{j,db})]}{den} \tag{4-3}$$

$$\frac{\mathrm{Im}(Y_{gain})}{\omega} \approx \frac{\mathrm{Im}(Y_{21} - Y_{12})}{\omega} = -g_m \tau - \frac{g_{mb} \Delta^2 / [R_b (C_{j,sb} + C_{j,db})]}{den} \tag{4-4}$$

$$\mathrm{Re}(Y_{22}) \approx \frac{1}{R_{ds}} + \frac{\omega^2 \Delta C_{j,db} [g_{mb} \Delta + C_{j,db} (R_b + R_{j,sb})] / (C_{j,sb} + C_{j,db})}{den} \tag{4-5}$$

$$\begin{aligned} \frac{\mathrm{Im}(Y_{22})}{\omega} \approx{}& (C_{gd} + C_{ds}) + \frac{C_{j,db} (R_b + R_{j,sb}) [(R_b + R_{j,sb}) + g_{mb} \Delta / (C_{j,sb} + C_{j,db})]}{den} \\ &+ \frac{\omega^2 \Delta^2 C_{j,db} [(C_{j,sb} + C_{j,db}) - C_{j,db}] / (C_{j,db} + C_{j,db})}{den} \end{aligned} \tag{4-6}$$

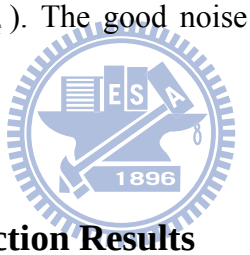
$$\frac{\mathrm{Im}(Y_{12})}{\omega} \approx -C_{gd} - \frac{C_{j,db} \Delta (R_b + R_{j,sb}) / [R_b (C_{j,sb} + C_{j,db})]}{den} \tag{4-7}$$

where $den \equiv (R_b + R_{j,sb})^2 + \omega^2 \Delta^2$ and $\Delta \equiv R_b R_{j,sb} (C_{j,sb} + C_{j,bd})$. A practical extraction procedure shown in Fig. 4-4 is then proposed. Compared to the method proposed in reference [12], which needs some parameters determined from DC characteristics, our extraction method relies only on local optimizations using definite RF fitting targets to obtain all model parameters, so the excellent modeling results with less than 10% relative root-mean-square errors for each real and imaginary part of Y parameters, as shown in Fig. 4-5, can be expected. For the reader's reference, the extracted model parameters are listed in Table 4-1.

Besides, as shown in Fig. 4-6, based on the RF small-signal equivalent circuit, the RF noise equivalent circuit can be built by adding the corresponding noise current sources. In this noise equivalent circuit, $\overline{i_d}$ stands for the intrinsic channel noise current, and the assumption

that the high-frequency prominent drain-induced gate noise can be neglected is adopted. This assumption had been shown to be reasonable especially for deep sub-micrometer devices [15], and its validity will also be examined in Chapter 6. Furthermore, the noise current sources related to series resistances and access body resistance are considered as thermal noise current sources ($\bar{i} = \sqrt{4kT/R}$, R : resistance value). Finally, the inherent shot noise current caused by the source-side junction current is estimated using shot noise current formula ($\overline{i_{j,sb}} = \sqrt{2qI_b} \approx \sqrt{2qI_g}$).

The only one unknown model parameter $\overline{i_d}$ can be directly obtained by optimizing the four measured high-frequency noise parameters (minimum noise figure $NF_{\min}$, equivalent noise resistance R_n, magnitude of the optimum reflection coefficient $|\Gamma_{opt}|$, and phase of the optimum reflection coefficient $\angle\Gamma_{opt}$). The good noise modeling results are shown in Fig. 4-7.



4.3.2 Verification of the Extraction Results

To further examine the accuracy of the modeling results, some important model parameters versus VDD for different channel lengths are examined. Note that we let $V_{GS}(=V_{BS}) = V_{DS} \equiv VDD$ to keep the device operating in the saturation region. Figure 4-8(a) shows that compared to the standard device, the DT device has larger trans-conductance (g_m) due to its lower threshold voltage (V_T) and higher mobility. The enhanced carrier mobility can result from the lower effective normal field in the channel caused by the reduction of the body charge [1]. Hence, this phenomenon could be more obvious at larger VDD. Besides, lower V_T and higher mobility can also help to decrease the channel resistance. However, in the saturation region, the DT devices may have smaller channel length modulation (CLM) than the standard devices, which in turn tends to increase the channel resistance as reported in [16]. This effect is more prominent for shorter DT devices, and it explains the smaller difference in

channel resistance (R_{ds}) for shorter channel devices in Fig. 4-8(b).

Besides, lower threshold voltage also increases the channel charge, and hence increases the intrinsic capacitance [1]. Therefore, as shown in Fig. 4-8(c), the DT device would have larger gate-to-source capacitance (C_{gs}) than the standard one. Figure 4-9(a) shows that the body trans-conductance (g_{mb}) tends to increase with VDD. However, in the low-voltage regime where the DT device normally operates, compared to g_m, its value is small and hence its contribution to the total device performance could be negligible.

Finally, the source- and drain-side junction capacitances ($C_{j,sb}$ and $C_{j,db}$) as well as access body resistance (R_b) versus VDD are examined. In Fig. 4-9(b), $C_{j,sb}$ tends to exponentially increase as VDD increases due to the nature of its forward-biased diffusion capacitance, while $C_{j,db}$ shows less bias dependence. Besides, decreasing channel length can help decrease $C_{j,sb}$, but increase $C_{j,db}$. Figure 4-9(c) shows that R_b may decrease with increasing VDD, which results from the abundant positive charge supplied by the external DC source through the body contact. This figure also supports that because the shorter device has a smaller cross-section for current flowing into the body, it has larger R_b. Note that all the channel length dependences for $C_{j,sb}$, $C_{j,db}$, and R_b become weak for channel length below 0.12 μm.

4.4 RF Small-Signal Characterization

In this section, using the extraction methodology proposed in the previous section, we will study the temperature dependences of the extracted small-signal parameters for the RF SOI DT MOSFET.

4.4.1 Temperature Dependences of Small-Signal Parameters

Figure 4-10 shows the temperature dependences of gate-to-source capacitance C_{gs}, channel resistance R_{ds}, and trans-conductance g_m for the DT MOSFET. Lower threshold voltage at higher temperature can induce more charges in the channel and hence larger C_{gs} [1] and lower R_{ds} as shown in Figs. 4-10(a) and (b), respectively. This also results in positive temperature dependence for g_m in the low VDD regime as shown in Fig. 4-10(c) [4]. At high VDD, however, the lower mobility at higher temperature would degrade g_m, so g_m tends to decrease with increasing temperature in the high VDD regime [4][17]. Also note that at all bias conditions where saturation holds, C_{gs} shows much less temperature dependence than g_m.

The temperature dependences of inherent body-related parasitics of the DT MOSFET are shown in Fig. 4-11. Due to the more leaky behavior encountered in source-to-body junction at higher temperature, the source-to-body junction capacitance $C_{j,sb}$ would increase with temperature. On the other hand, compared to $C_{j,sb}$, the drain-to-body junction capacitance $C_{j,db}$ shows less temperature dependence (see Fig. 4-11(a)). Besides, at higher temperature and larger VDD (and hence, larger V_{BS}), more charge would be injected into the body region through source-to-body junction, and this could contribute to the observation that the body resistance R_b tends to decrease with increasing temperature and VDD as shown in Fig. 4-11(b). Finally, the more leaky source-to-body junction at higher temperature and larger VDD could result in more sever body effect and this would in turn increase the body trans-conductance g_{mb} as shown in Fig. 4-11(c).

4.4.2 Temperature Dependences of f_t and $f_{\max}$

The cut-off frequency (f_t) and maximum oscillation frequency ($f_{\max}$) are two common

figures of merit used to characterize the RF performance of a device. To derive out simple and analytical equations for analysis, the series resistances have been omitted at the moment, and also de-embeded from the maseured data for model comparison. Based on the equivalent circuit shown in Fig. 4-6 without considering series resistances R_s, R_d, and R_g, the f_t and $f_{\max}$ for the DT MOSFET biased in the low VDD regime can be approximately expressed as the following equations [18].

$$f_t \approx \frac{g_m}{2\pi\sqrt{C_{gs}\left(C_{gs}+2C_{gd}\right)}} \approx \frac{g_m}{2\pi C_{gs}} \tag{4-8}$$

$$f_{\max} \approx f_{\max 0}\left\{1+g_{mb}R_{ds}\frac{C_{j,db}}{C_j}\right\}^{-0.5} \equiv f_{\max 0}\cdot\alpha_{DT} \tag{4-9}$$

In Equs. (4-8) and (4-9), $C_j = C_{j,sb} + C_{j,db}$,

$$f_{\max 0} \approx \frac{f_t}{2}\sqrt{\frac{R_{ds}}{R_i}}, \tag{4-10}$$

R_i is the input resistance, which can be extracted by optimizing $\mathrm{Re}(Z_{11})$, and

$$\alpha_{DT} = \left\{1+g_{mb}R_{ds}\frac{C_{j,db}}{C_j}\right\}^{-0.5}. \tag{4-11}$$

The approximation in Equs. (4-8) and (4-9) holds in the low VDD regime, where $g_m/g_{mb} >> 1$, $R_b/R_i >> 1$, $g_{mb}R_b >> C_{j,db}/C_j$, and $\omega R_b C_j >> 1$ around $f_{\max}$, and the good modeling results for f_t and $f_{\max}$ in the low VDD regime are shown in Figs. 4-12(a) and (b), respectively.

Equation (4-8) implies that the inherent body-related parasitics of the DT MOSFET would have little influence on f_t. In the low VDD regime, since g_m tends to increase with temperature, f_t would have a positive temperature coefficient as shown in Fig. 4-13(a) for VDD below 0.4 V.

On the other hand, Equation (4-9) implies that the body-related parasitics would degrade

$f_{\max}$ through the degradation factor α_{DT}, which is about 3/4 and almost bias and temperature independent as shown in Fig. 4-14. In addition, due to the less temperature dependent behavior of $\sqrt{R_{ds}/R_i}$ (also shown in Fig. 4-14), $f_{\max}$ tends to have the same temperature dependence as f_t (see Fig. 4-13(b)). That is, in the low VDD regime, both $f_{\max}$ and f_t would tend to become larger at higher temperature.

4.4.3 Series Resistance Effect

In the previous sub-section, we have focused on the 'inner' device performance without considering the series resistance effect. To judge the series resistance effect on the overall performance and complete the characterization, this effect will be considered in this sub-section. Besides, to facilitate the examination of the temperature effect, we have normalized the related parameters with respect to their corresponding values at $T = 25°C$ in the following discussions.

Figure 4-15 shows that the series resistance has much more significant effect on the unilateral power gain U (or $f_{\max}$) than the short-circuit current gain $|H_{21}|$ (or f_t) at $VDD = 0.3\text{V}$. Compared to the series resistance, the much larger input and output impedance in the low VDD regime would dominate $|H_{21}|$, and hence, f_t. The little series resistance effect on f_t can be also deduced in Fig. 4-16(a) and (b), where f_t has nearly the same temperature coefficient as g_m for each channel length device. This coincides with the implication in Equ. (4-8), which has assumed the series resistance is insignificant.

The input and output impedance matching for maximum available power gain, or equivalently $f_{\max}$, however, can be greatly influenced by the series resistance. Moreover, since the degradation factor α_{DT} is found to be nearly temperature independent for each channel length device as shown in Fig. 4-17(a), the $f_{\max}$ with degraded temperature dependence shown in Fig. 4-17(b) would be the results mostly caused by the series resistance effect. That is, the larger series resistance at higher temperature would more severely degrade

$f_{\max}$.

4.5 RF Noise Characterization

4.5.1 Channel Noise and Equivalent Noise Resistance

The extracted power spectral density for the channel noise current i_d (denoted as S_{id}) is shown in Fig. 4-18, and usually expressed as follows [19].

$$S_{id} = 4k_B T \gamma g_{d0} \tag{4-12}$$

where $k_B \approx 1.38\times10^{-23}$ J/K is Boltzmann constant, T is the ambient temperature in Kelvin, g_{d0} is the channel conductance at zero drain-source voltage, and γ is noise factor. Besides, reference [20] has shown that γ has the weak temperature dependence, and the temperature dependence of S_{id} is dominated by that of g_{d0} and T.

Figure 4-19(a) and (b) respectively show the temperature dependences of S_{id} and g_{d0}. In the low VDD regime, since g_{d0} tends to increase with temperature [18], S_{id} would increase accordingly as predicted by Equ. (4-12). Note that Equ. (4-12) was originally derived for the device operating in the strong inversion region. However, in our experiments, the consistent prediction results for the temperature dependence of S_{id} shows that it seems to remain valid even for the medium or weak inversion applications.

The channel noise has significant effect on the equivalent noise resistance R_n for conventional MOSFETs. In fact, by neglecting the body trans-conductance, the R_n for DT MOSFETs would be approximately the same as that for conventional MOSFETs as expressed in the following.

$$R_n \approx \frac{S_{id}}{4k_B T_0 g_m^2} + \frac{T}{T_0} R_g \tag{4-13}$$

where $T_0 = 290K$ is the reference temperature. Note that Equ. (4-13) indicates that in the low VDD regime, the body-related parasitics would have little influence on R_n.

Figure 4-20(a) shows R_n versus temperature curves for each channel length device. Since V_T for $L = 60\text{nm}$ device is about 0.1V higher than those for $L = 120\text{nm}$ and $L = 240\text{nm}$ devices in the whole temperature range (see Fig. 4-1), we first consider $VDD = 0.3\text{V}$ for $L = 120\text{nm}$ and $L = 240\text{nm}$ devices, and $VDD = 0.4\text{V}$ for $L = 60\text{nm}$ device to keep approximately the same gate overdrive voltage. In this case, one can compare the temperature dependence for S_{id} in Fig. 4-19(a) and that for g_m^2 in Fig. 4-20(b). Since S_{id} tends to have the similar temperature coefficient as g_m^2, according to Equ. (4-13), R_n tends to increase with temperature mainly due to the increase of R_g and T.

For $L = 60\text{nm}$ device operating at weaker bias condition, that is, $VDD = 0.3\text{V}$, however, g_m^2 tends to more deeply increase with increasing temperature than S_{id}. This could compete with or even overwhelm the contribution from "hot" R_g. Therefore, R_n tends to decrease with increasing temperature. This also shows the existence of the zero temperature coefficient for R_n, which occurs between $VDD = 0.3\text{V}$ and $VDD = 0.4\text{V}$ for $L = 60\text{nm}$ device.

4.5.2 Output Noise Current and Minimum Noise Figure

Unlike R_n, the minimum noise figure $NF_{\min}$ may be strongly influenced by R_b. Although the analytical expression for $NF_{\min}$ is not easily derived, the noise contribution arising from R_b to the output noise current flowing into the drain terminal can be analyzed and regarded as an important factor determining $NF_{\min}$.

The noise power spectral density arising from R_b (denoted as S_{iRb}) is considered as thermal noise, and can be expressed as below.

$$S_{iRb} = 4k_B T / R_b \tag{4-14}$$

The extracted R_b values and their corresponding S_{iRb} contribution with respect to S_{id}

counterpart to the output noise current and are shown in Fig. 4-21(a) and (b), respectively. We found that larger R_b in the low VDD regime would have less S_{iRb} noise contribution for each length device. This figure also shows that the shorter device with larger R_b would have more S_{iRb} contribution. It is worth noting that the smaller body cross-section area seen in the direction perpendicular to the channel current flow can account for the larger R_b present in the shorter device.

Through the sensitivity analysis of the variation of R_b to its noise contribution as shown in Fig. 4-22, we can see that its noise contribution could be reduced with increasing R_b. In fact, the noise equivalent circuit for DT MOSFETs would be equivalent to that for conventional MOSFETs when R_b approaches infinity and can be removed in the equivalent circuit. Therefore, the larger R_b would play an insignificant role in determining $NF_{\min}$.

The minimum noise figure $NF_{\min}$ versus VDD is shown in Fig. 4-23. The $NF_{\min}$ is sharply increased towards the weak inversion region, and this trend is consistent with that for the conventional bulk MOSFET [21]. Moreover, our experimental results show that $NF_{\min}$ has less temperature dependence in the low VDD regime. As shown in Fig. 4-22, in the low VDD regime, since the noise contribution of S_{iRb} to the output noise current for each temperature is not significant, R_b would have little effect on the temperature dependence of $NF_{\min}$.

4.6 Summary

We have demonstrated the RF small-signal and noise modeling for SOI DT MOSFETs. Based on a set of simple and analytic expressions of Y parameters, model parameters can be physically extracted, and the model has been shown to be valid up to 12 GHz.

The temperature dependences of RF small-signal and noise behaviors for the DT MOSFET have been investigated. In the low VDD regime, since g_m tends to increase with temperature, f_t would have a positive temperature coefficient. On the other hand, due to the

less temperature dependent behavior of α_{DT} and $\sqrt{R_{ds}/R_i}$, $f_{\max}$ is found to increase with temperature as well. Moreover, the body-related parasitics and the series resistances are found to have more impact on $f_{\max}$ than f_t.

In the low VDD regime, the channel noise S_{id} has a positive temperature coefficient due to larger g_{d0} at higher temperature. In addition, compared to S_{id}, the much higher g_m^2 towards the weaker inversion region can cause R_n to have a negative temperature coefficient. Finally, it shows that, in the low VDD regime, the large R_b would have little impact on the temperature dependence of $NF_{\min}$.

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Table 4-1 Extracted model parameters for bias condition $V_{GS} = 0.8\,\text{V}, \text{and}\, V_{DS} = 1\,\text{V}$. ($L/W_F/N_F/N_G = 0.24\mu\text{m}/1\mu\text{m}/8/16$)

g_m (mS)	R_{ds} (Ω)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	τ (ps)	g_{mb} (mS)	R_b (Ω)	$R_{j,sb}$ (Ω)	$C_{j,sb}$ (fF)	$C_{j,db}$ (fF)	$\overline{i_d}$ ($\text{pA}/\sqrt{\text{Hz}}$)
127	93	550	79	1.3	1.6	38	597	2083	246	20	60

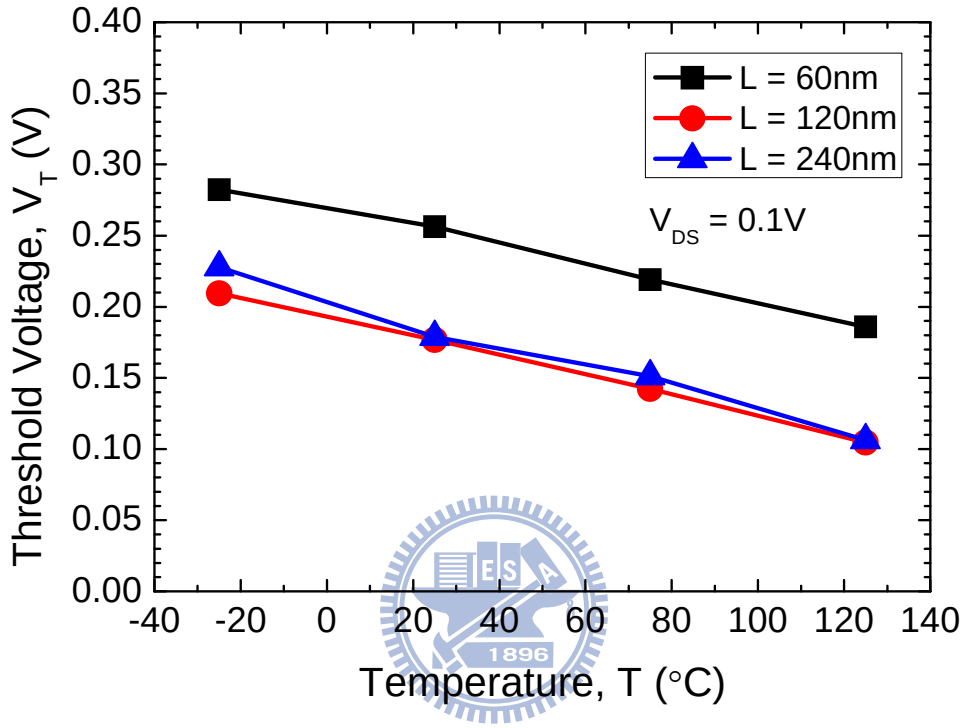


Figure 4-1 Temperature dependence of the threshold voltage for SOI DT MOSFETs.

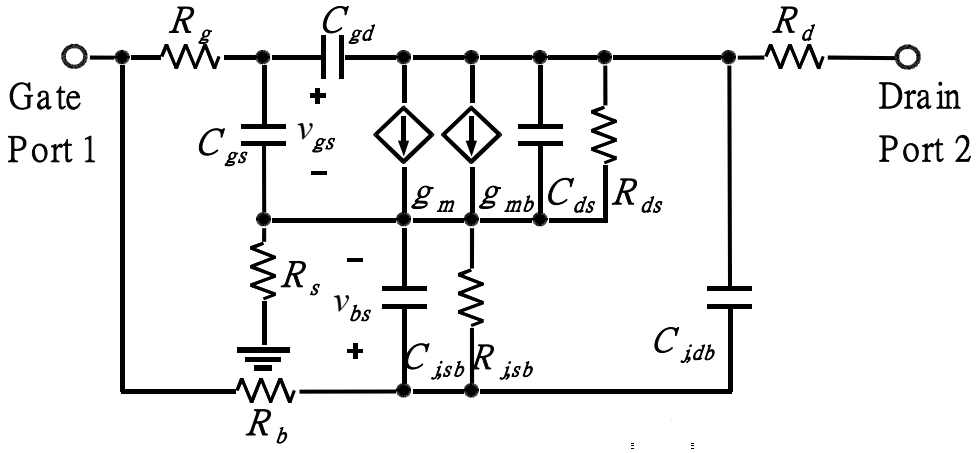


Figure 4-2 RF small-signal equivalent circuit for the SOI DT MOSFET.

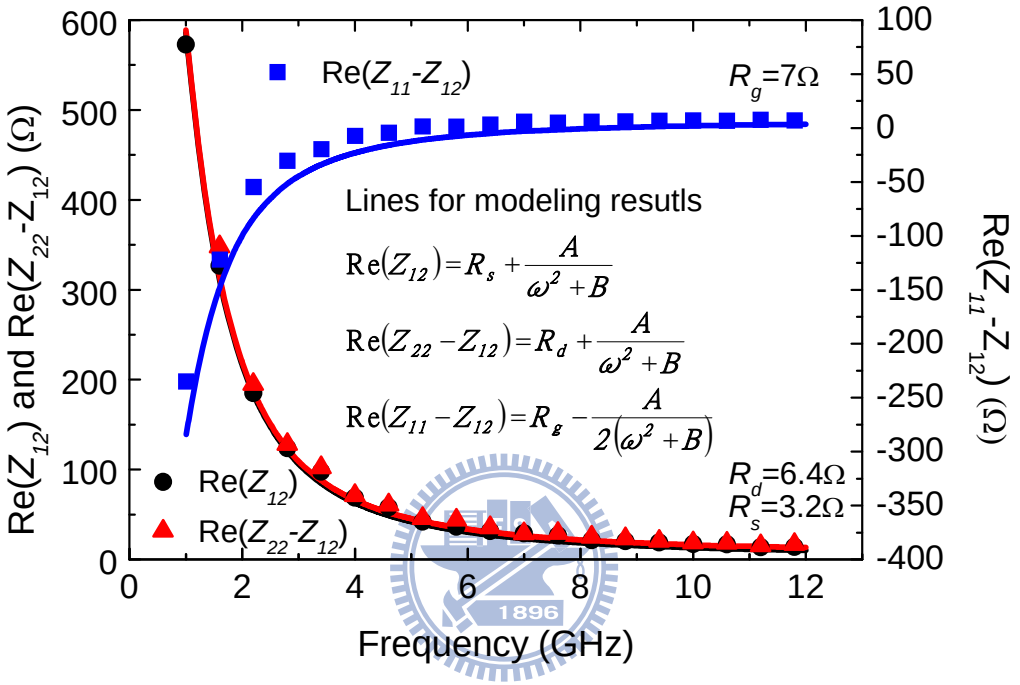


Figure 4-3 Model-data comparison for the extraction of series resistances using zero method. ($L/W_F/N_F/N_G = 0.24\mu m/1\mu m/8/16$, and $V_{GS} = V_{DS} = 0V$)

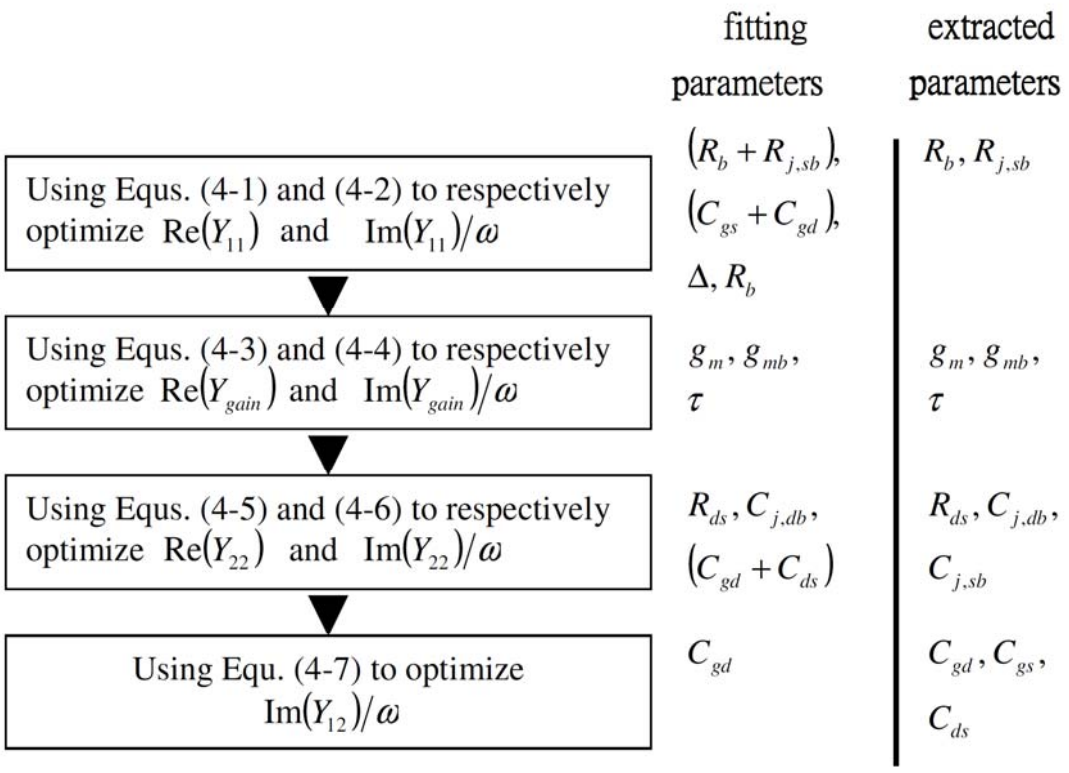
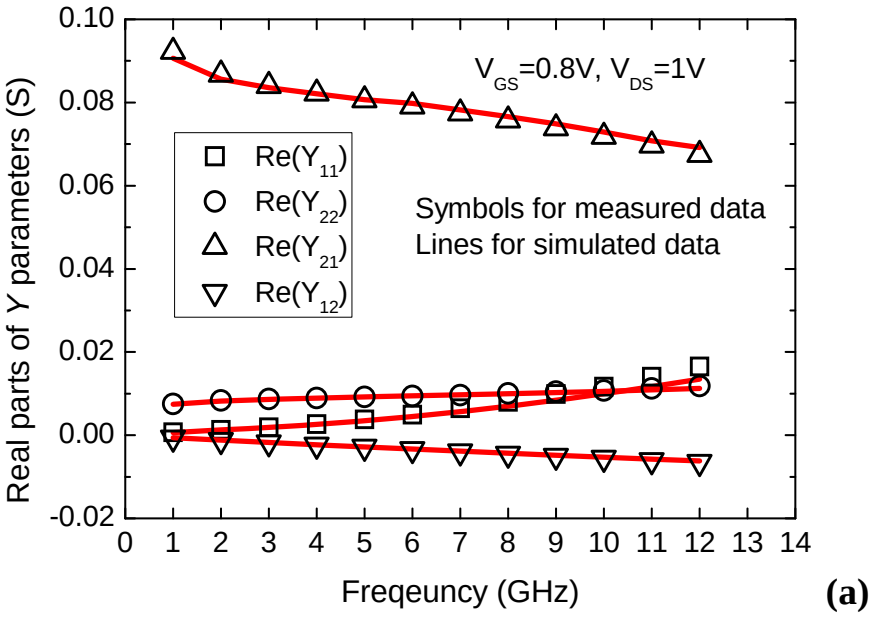


Figure 4-4 Proposed parameter extraction flow.



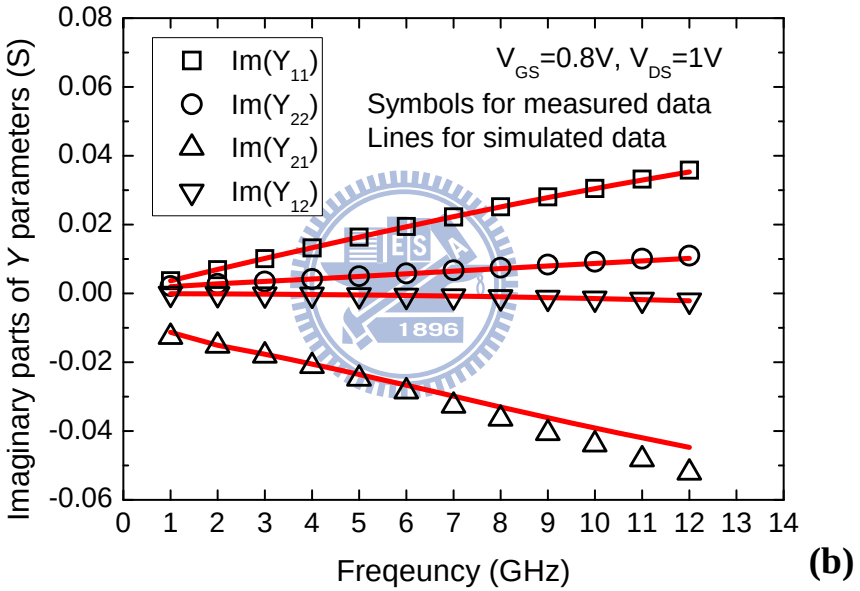


Figure 4-5 Modeling results for (a) $\mathrm{Re}(Y)$ and (b) $\mathrm{Im}(Y)$.

($L/W_F/N_F/N_G = 0.24\mu\mathrm{m}/1\mu\mathrm{m}/8/16$).

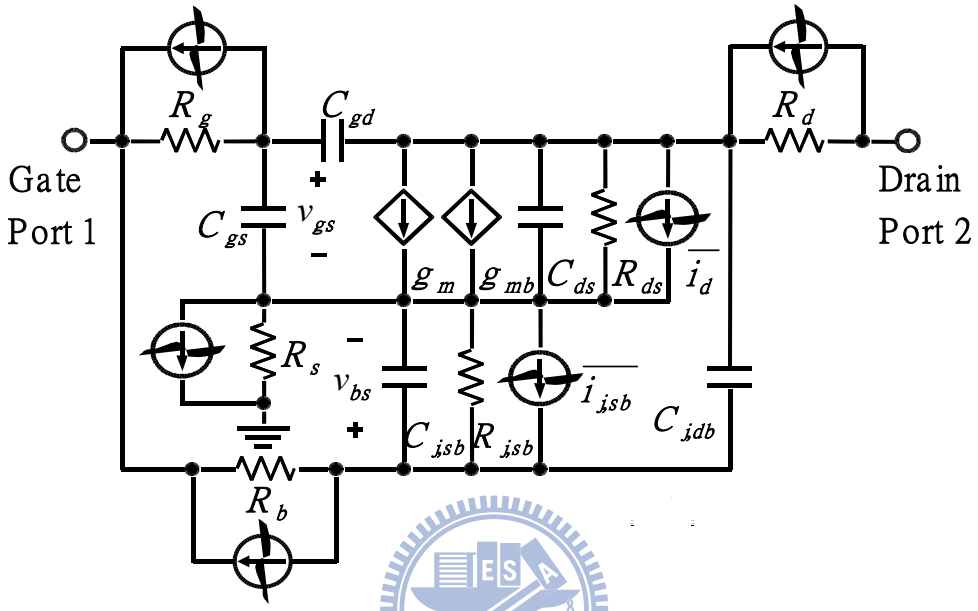
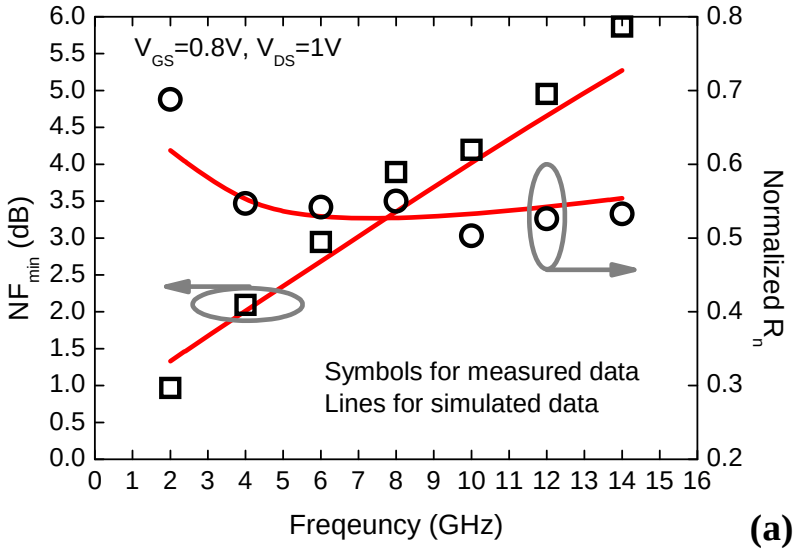
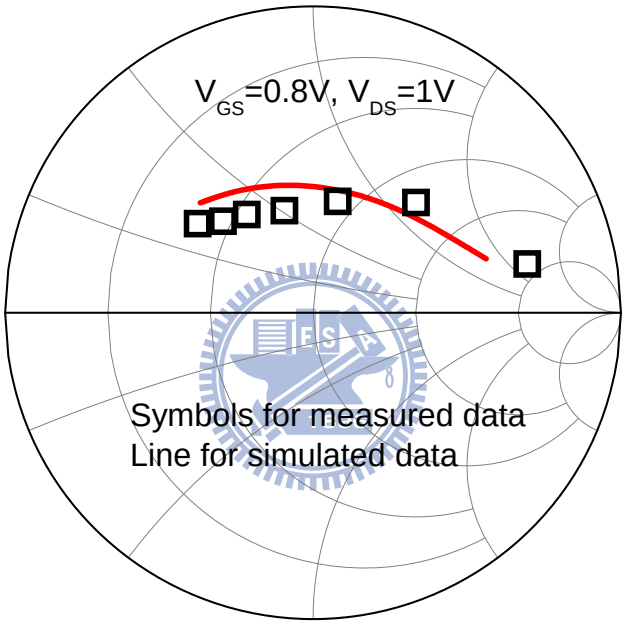


Figure 4-6 RF small-signal and noise equivalent circuit for the SOI DT MOSFET.



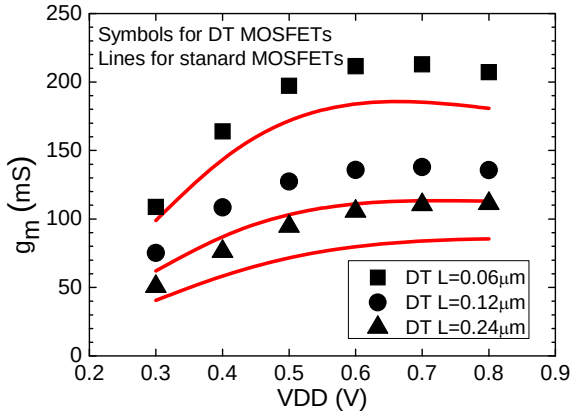
(a)



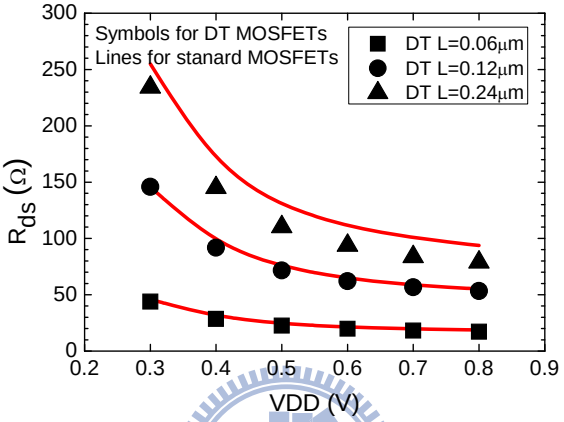
(b)

Figure 4-7 Noise modeling results for (a) $NF_{\min}$, R_n, and (b) Γ_{opt}.

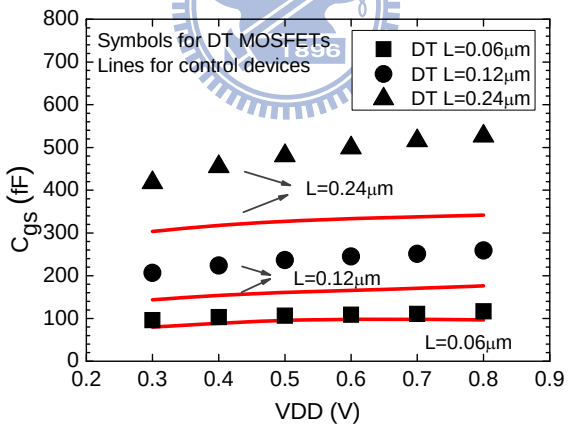
($\overline{i_d}$ = 60 pA/$\sqrt{\text{Hz}}$, and $L/W_F/N_F/N_G = 0.24\mu\text{m}/1\mu\text{m}/8/16$)



(a)

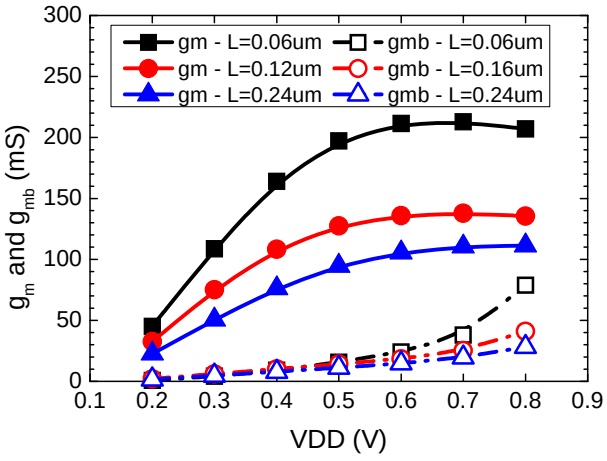


(b)

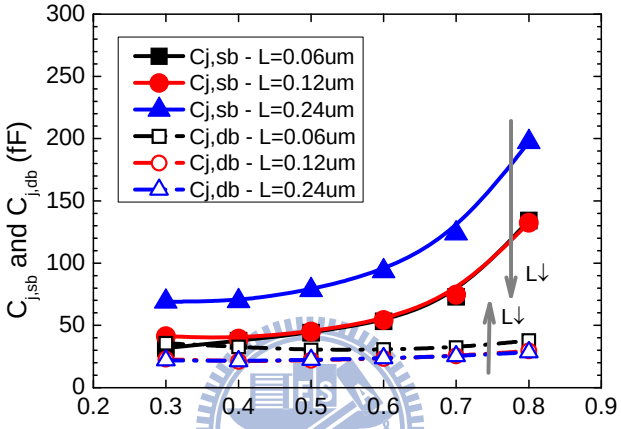


(c)

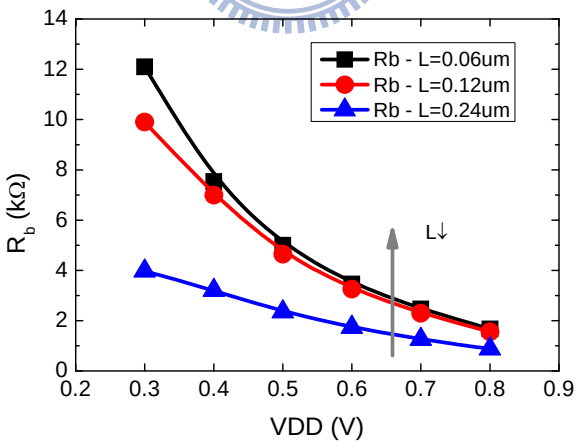
Figure 4-8 (a) g_m, (b) R_{ds}, and (c) C_{gs} versus VDD characteristics for DT and standard MOSFETs with different channel lengths. ($W_F / N_F / N_G$=1μm/8/16)



(a)



(b)



(c)

Figure 4-9 (a) g_{mb} and g_m, (b) $C_{j,sb}$ and $C_{j,db}$, and (c) R_b versus *VDD* characteristics for DT MOSFETs with different channel lengths. (W_F / N_F / N_G =1μm/8/16)

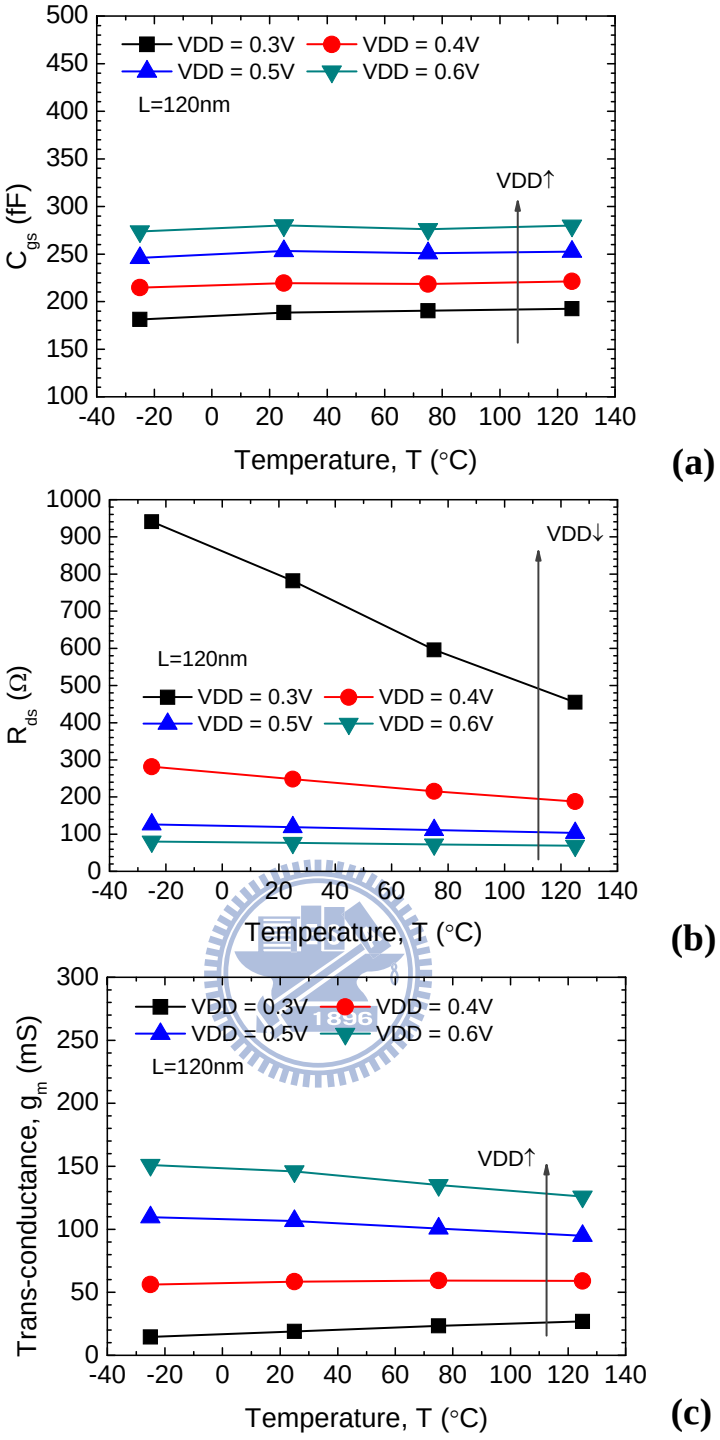


Figure 4-10 Temperature dependences of (a) C_{gs}, (b) R_{ds}, and (c) g_m for SOI DT MOSFETs. ($L/W_F/N_F/N_G$=0.12μm/1μm/8/16)

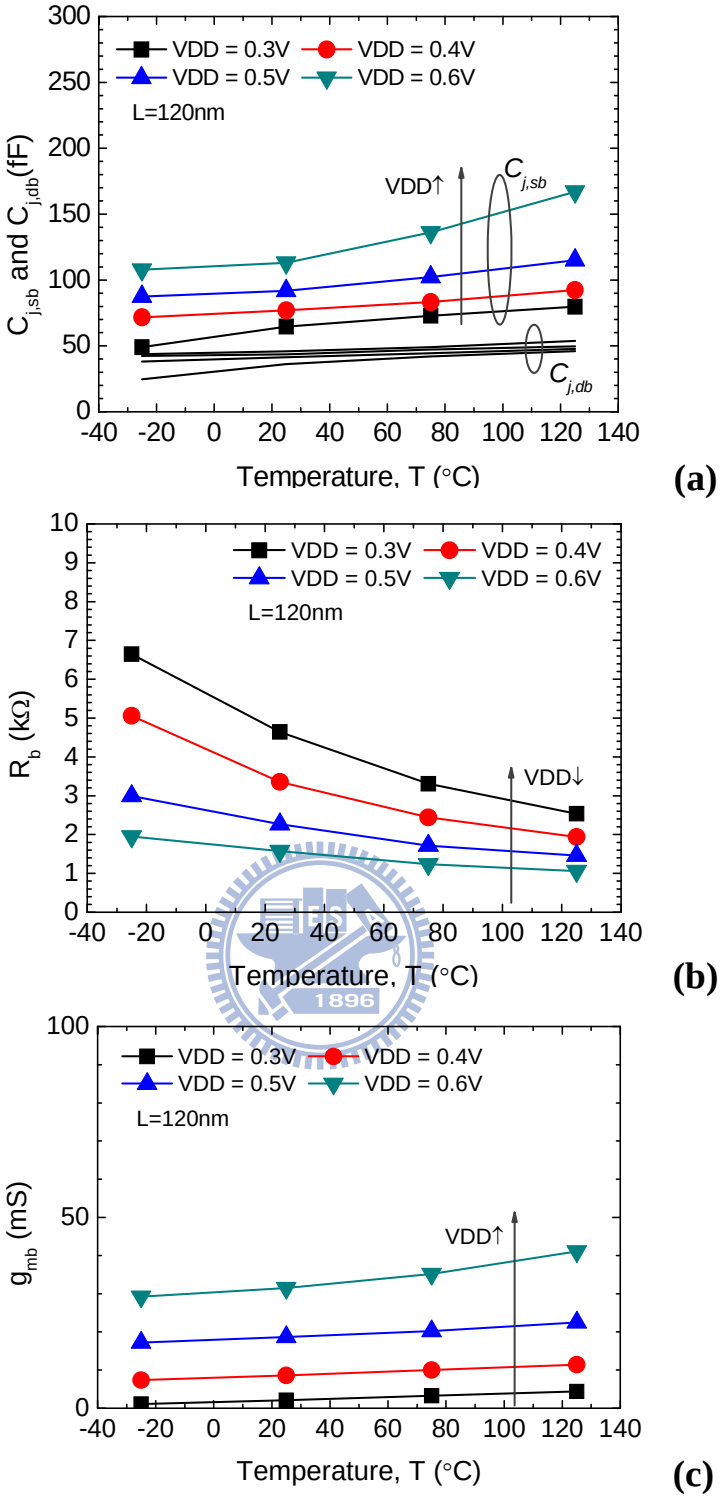


Figure 4-11 Temperature dependences of (a) $C_{j,sb}$ and $C_{j,db}$, (b) R_b, and (c) g_{mb} for the SOI DT MOSFET. ($L/W_F/N_F/N_G = 0.12\mu m/1\mu m/8/16$)

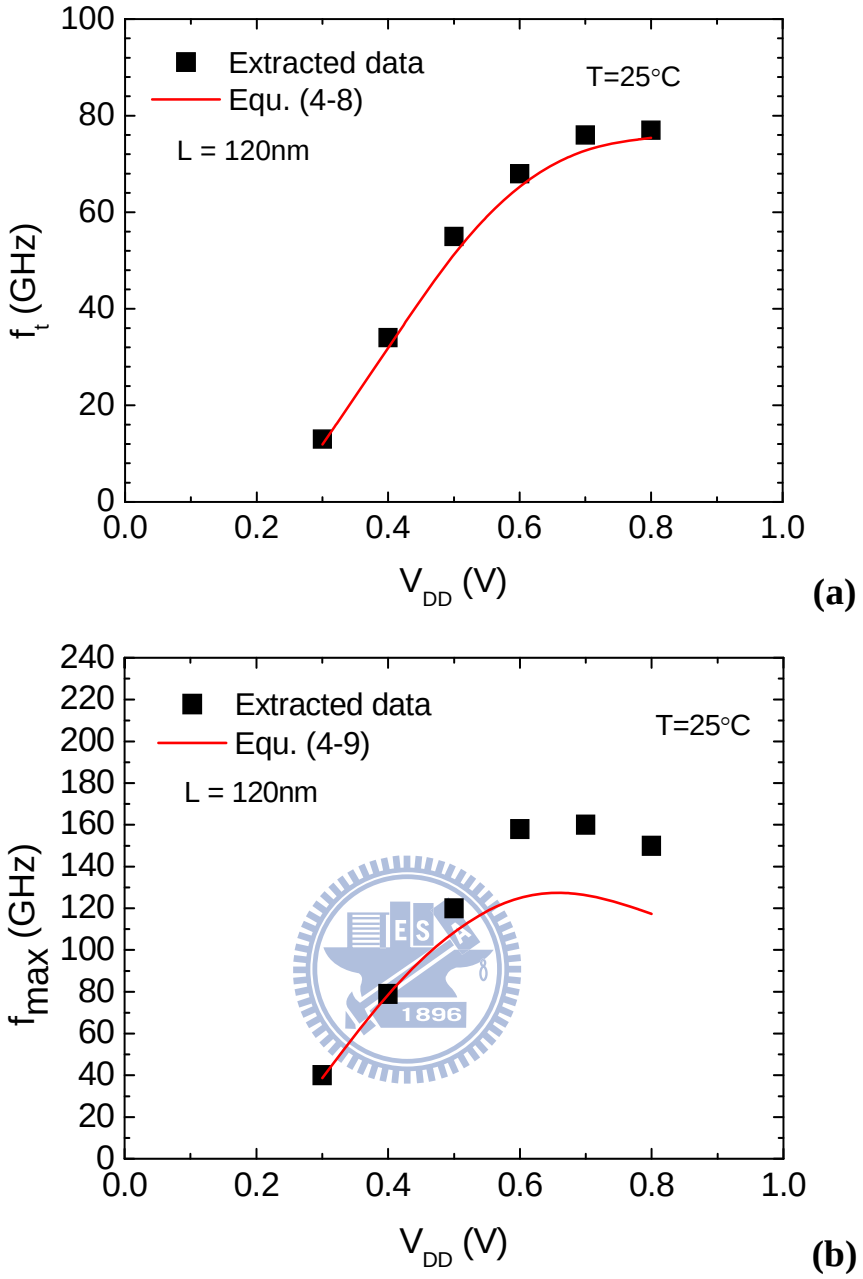


Figure 4-12 (a) Model-data comparison for (a) f_t, and (b) f_{max}.

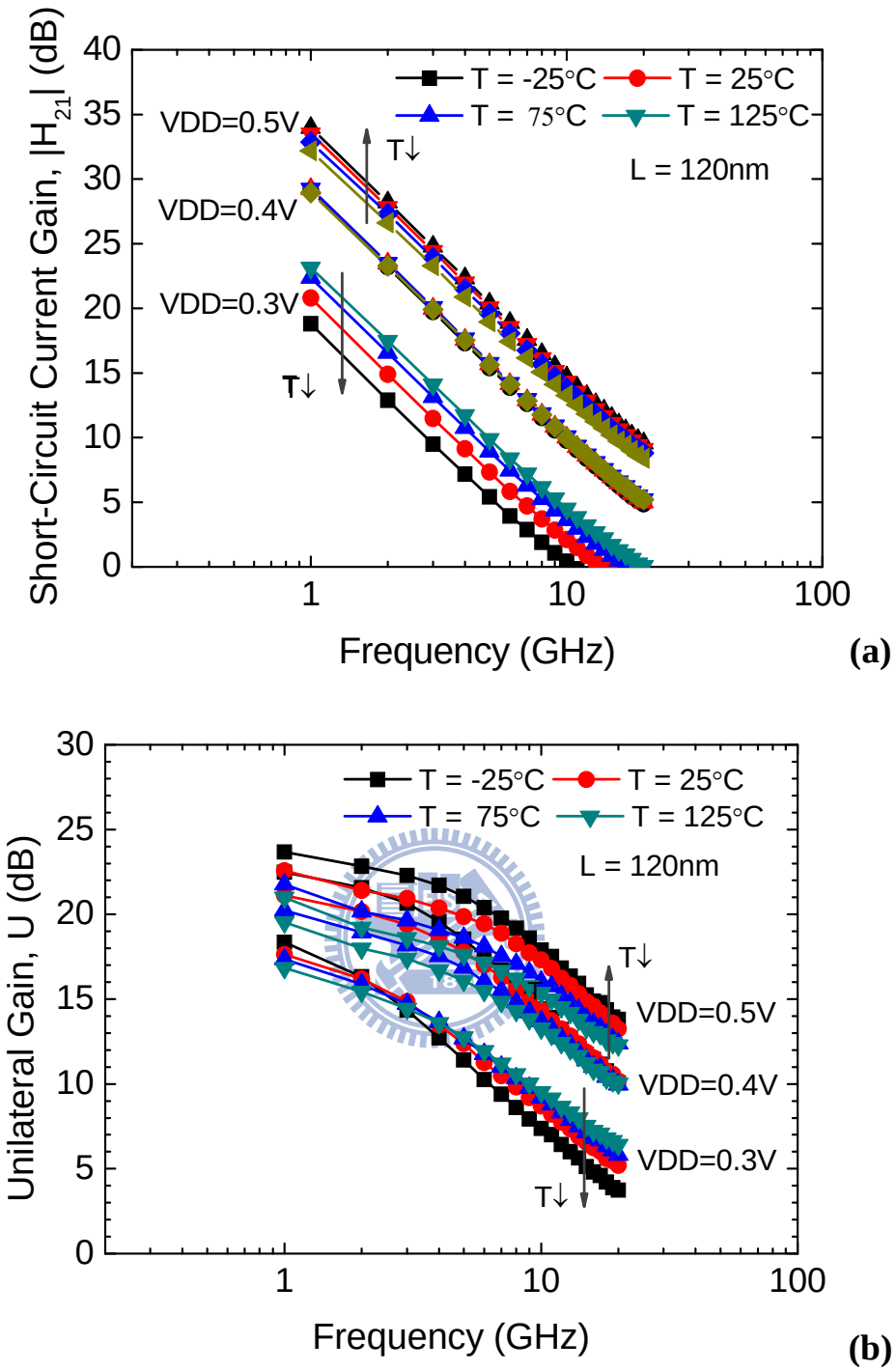


Figure 4-13 Temperature dependences of (a) $|H_{21}|$ and (b) U for the SOI DT MOSFET.

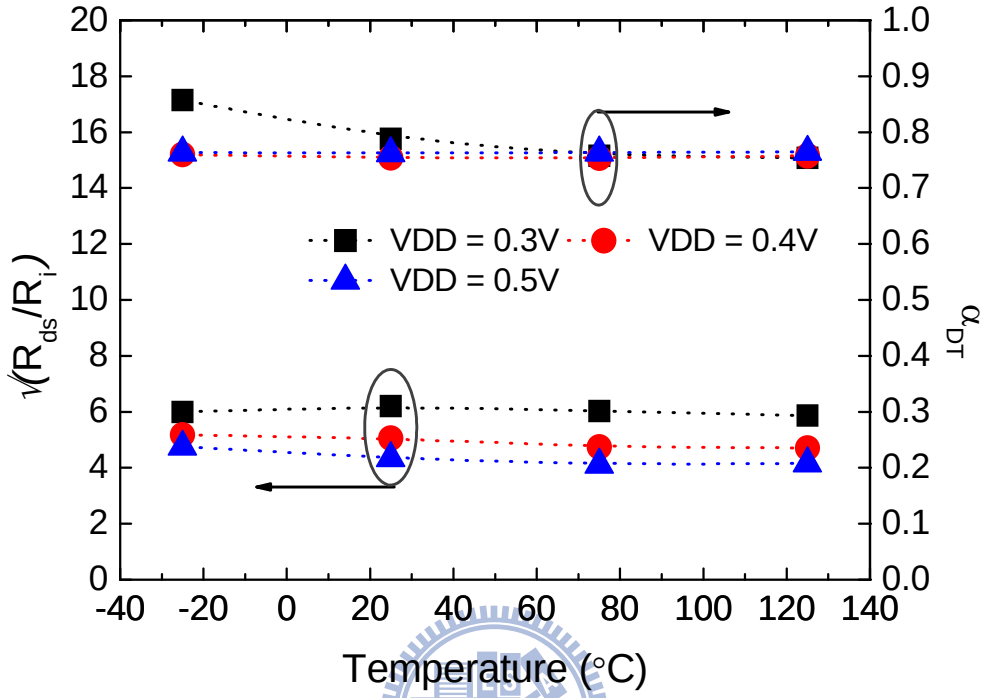
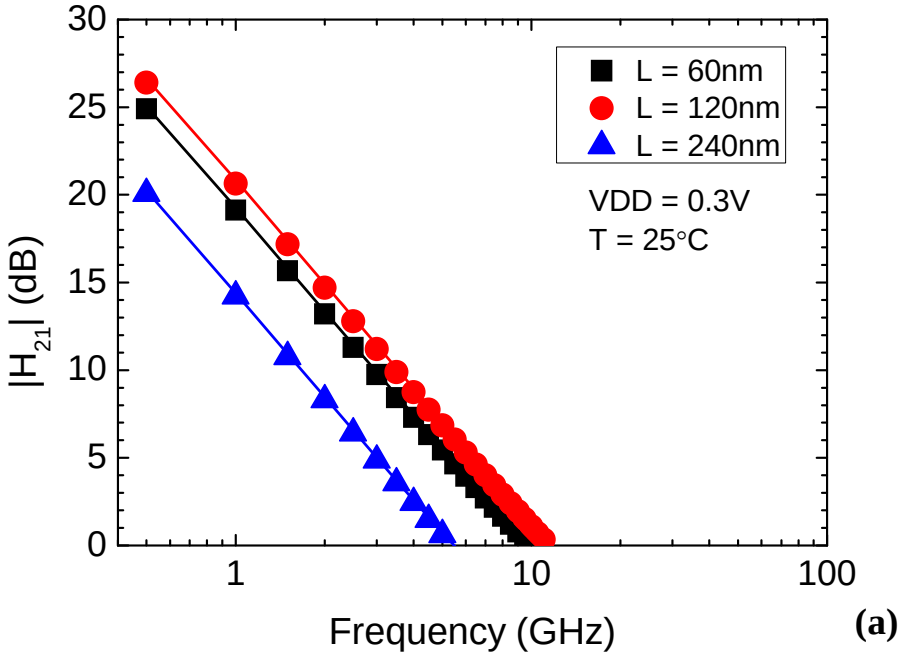


Figure 4-14 Temperature dependences of $\sqrt{R_{ds}/R_i}$ and α_{DT}.



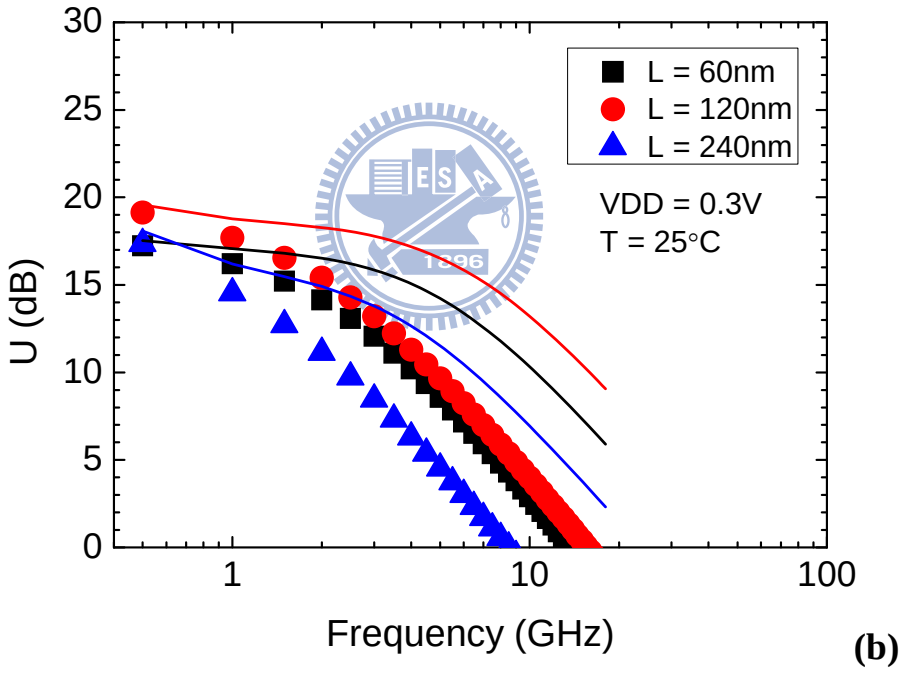
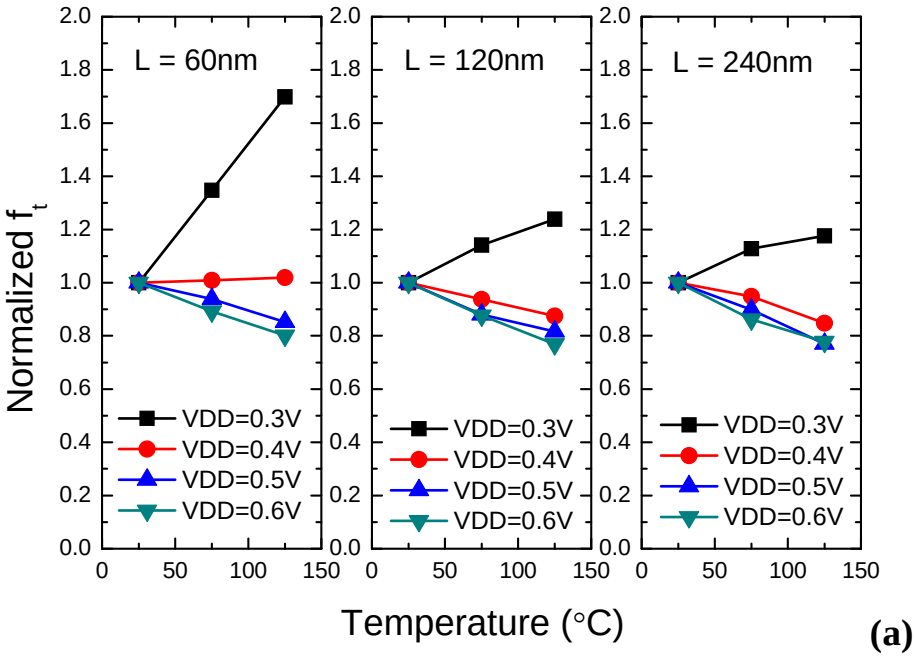


Figure 4-15 (a) The short-circuit current gain $|H_{21}|$ with (symbols) and without (lines) considering the series resistance effect. (b) The unilateral power gain U with (symbols) and without (lines) considering the series resistance effect.



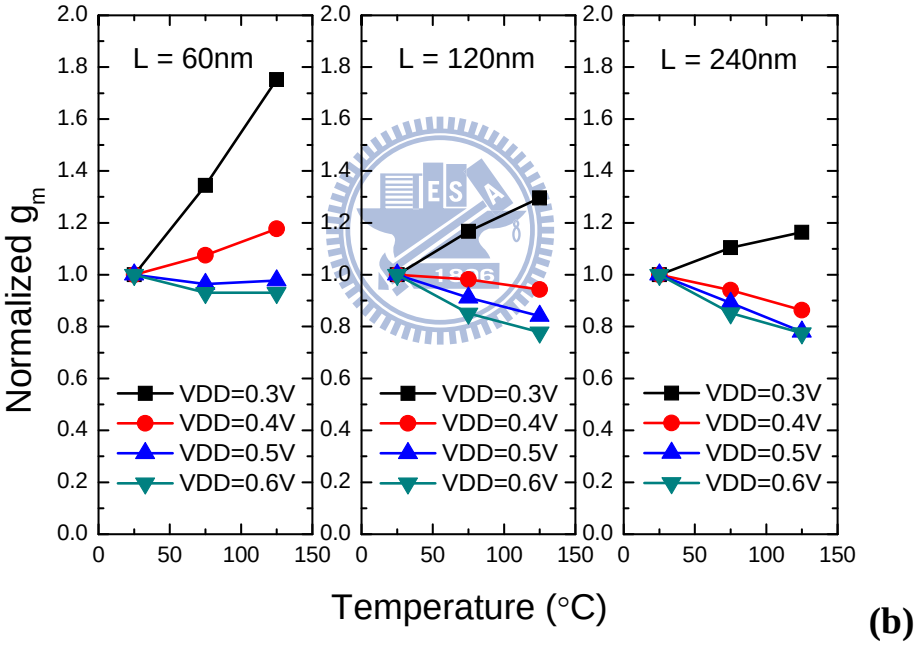
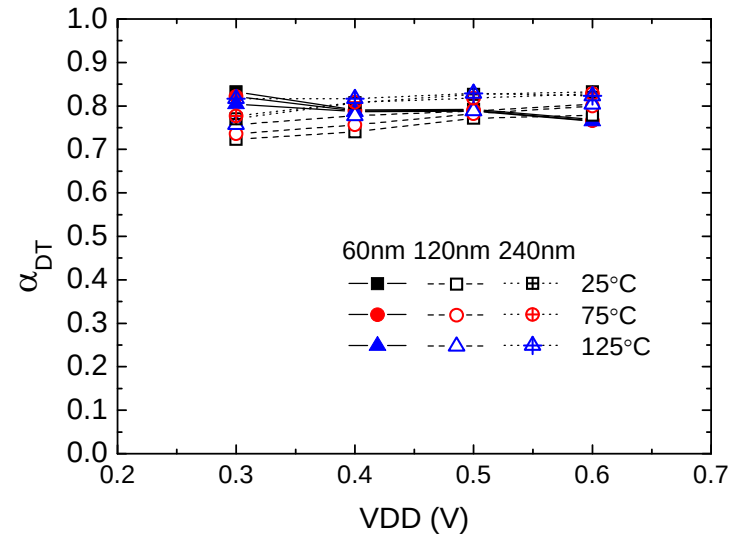
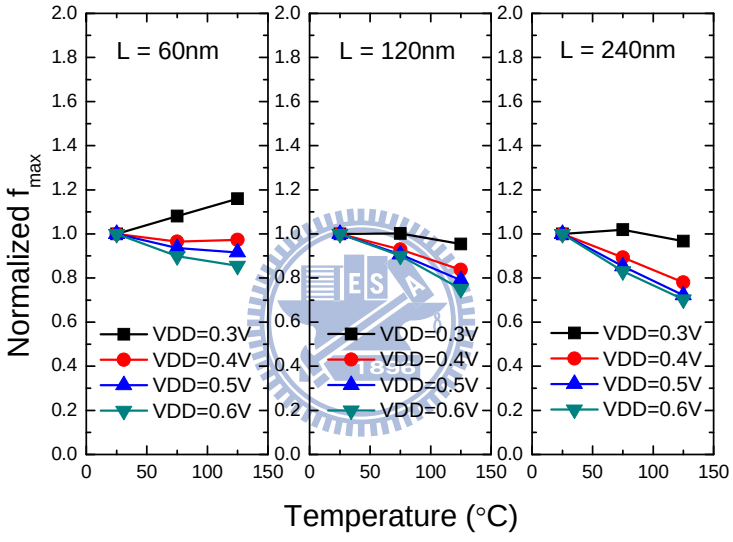


Figure 4-16 Temperature dependences for (a) f_t and (b) g_m.



(a)



(b)

Figure 4-17 (a) The bias dependence for α_{DT} and (b) the temperature dependence for $f_{\max}$.

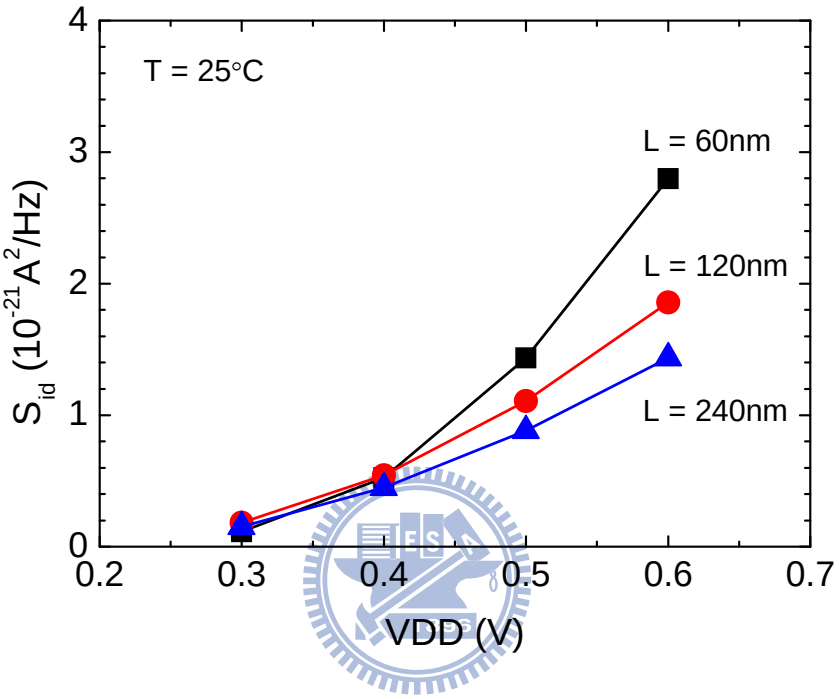
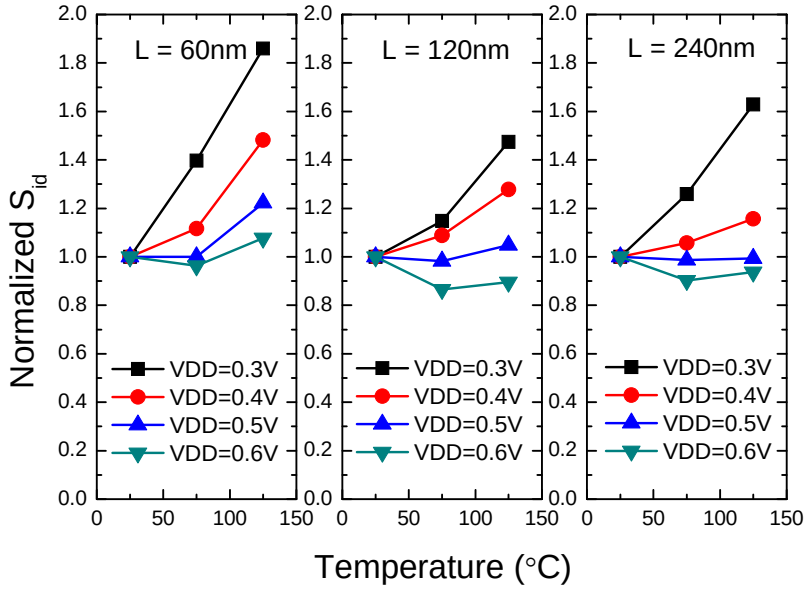


Figure 4-18 Channel noise versus VDD. (W_F / N_F / N_G = 1μm/8/16)



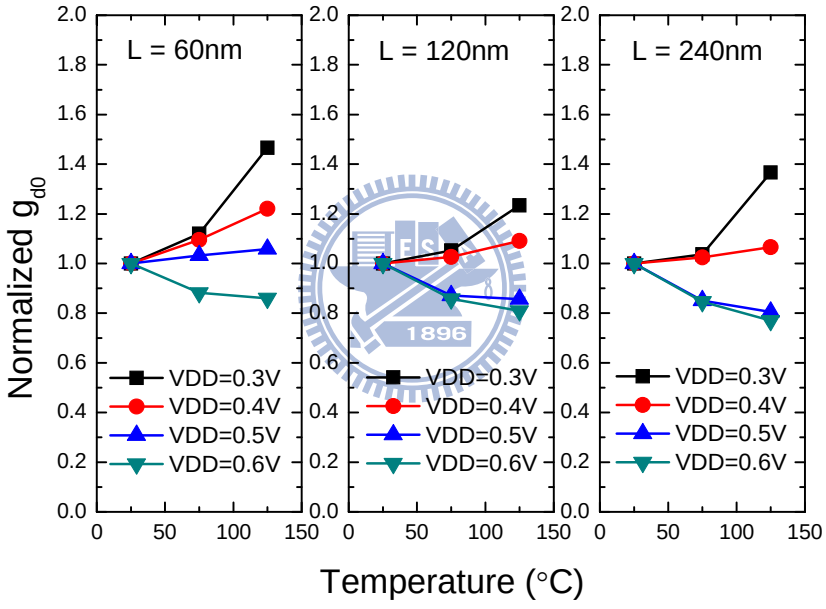


Figure 4-19 The temperature dependences for (a) S_{id}, and (b) g_{d0}.

(W_F / N_F / N_G =1μm/8/16)

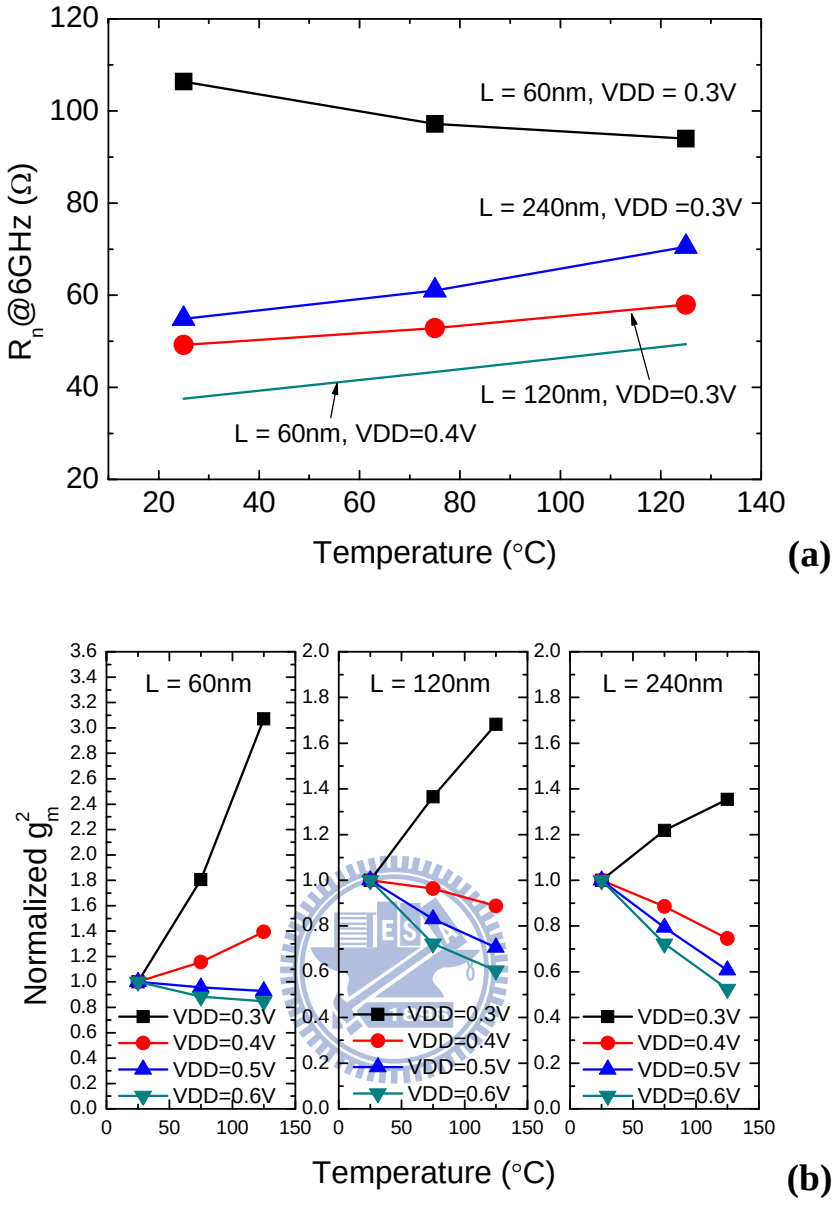
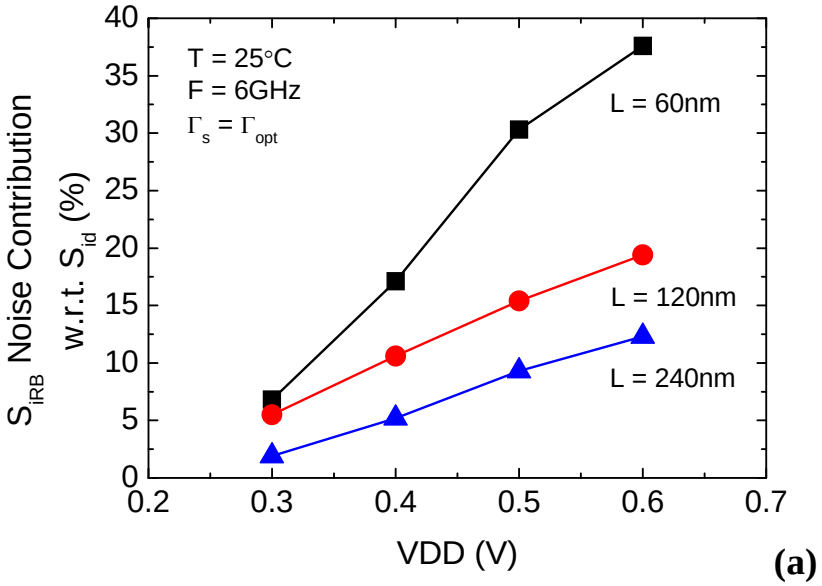


Figure 4-20 The temperature dependences for (a) R_n , and (b) g_m^2 . (W_F / N_F / N_G =1μm/8/16)



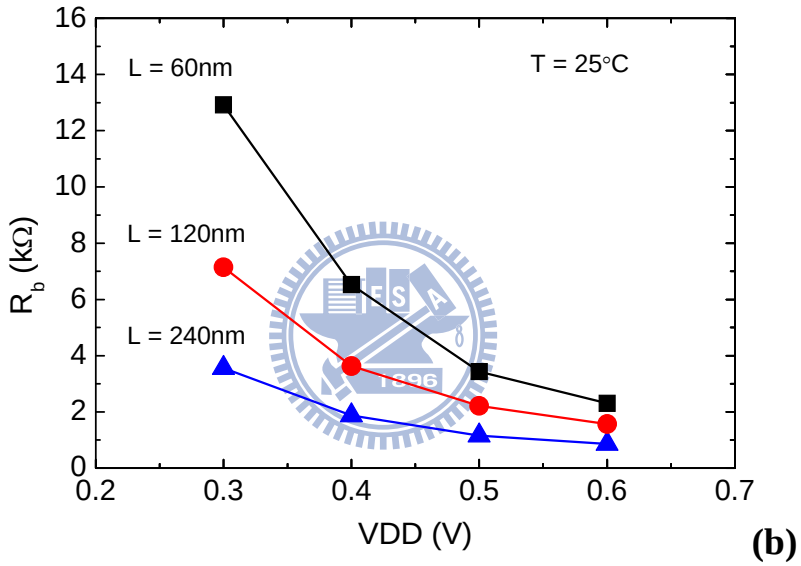


Figure 4-21 (a) The noise contribution from the body noise to the output noise current with respect to that from the channel noise. (b) The extracted body resistance as a function of VDD. (W_F / N_F / N_G =1μm/8/16)

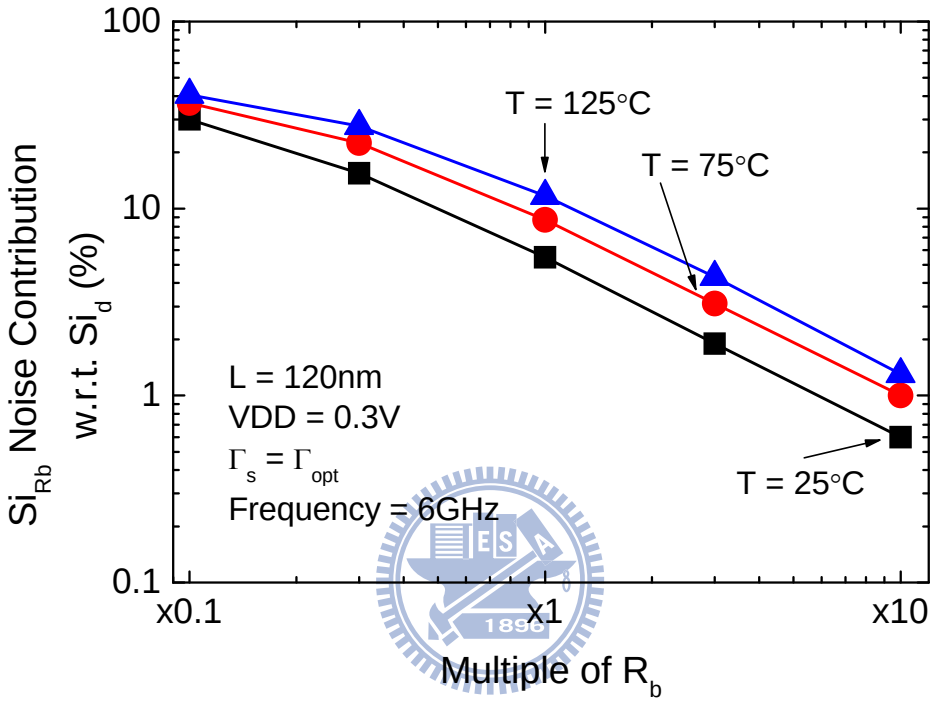


Figure 4-22 Sensitivity analysis of the variation of R_b to its noise contribution. (W_F / N_F / N_G =1μm/8/16)

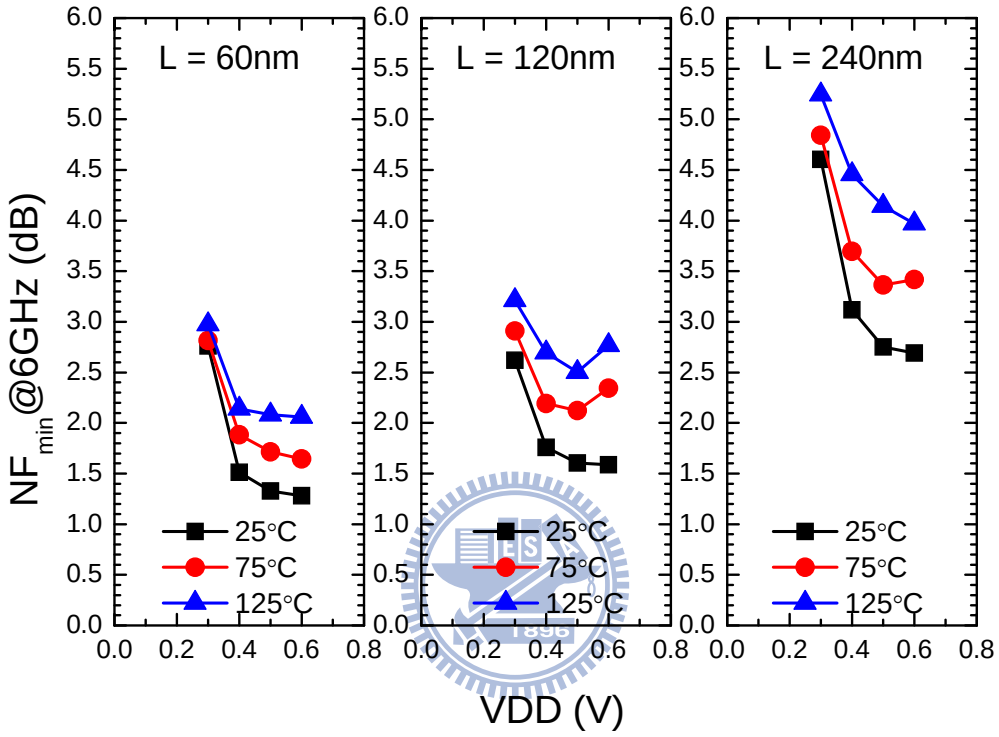


Figure 4-23 $NF_{\min}$ as a function of VDD at different temperatures for various channel length devices. ($W_F / N_F / N_G = 1\mu m/8/16$)

Chapter 5

RF Noise Characterization for the Tensile-Strained nMOSFET

5.1 Introduction

As the gate length of CMOS transistors is down-scaled to decananometer regime, device scaling is becoming extremely difficult due to many physical and technological problems [1]. Strain-engineering technology is one way to maintain the scaling trends of CMOS devices. It is well known that the strained-channel MOSFETs have larger carrier mobility and drain current than the unstrained counterparts [2]-[6]. It is expected that the improved DC performances can also enhance the RF performances.

Recently, CMOS technologies with the incorporation of high-tensile contact etch stop layer (CESL) stressors have been demonstrated for RF applications and a very high cut-off frequency (f_t) has been reported [7][8]. There have been many studies on the high frequency noise characterization and modeling for the conventional MOSFET devices [9]-[17]. However, the effects of the highly tensile stressors on the high-frequency noise characteristics have rarely been known. In this chapter, the high-frequency noise characteristics of tensile-strained nMOSFETs including their temperature dependences will be investigated and analyzed for the first time [18].

5.2 Devices and Measurements

Multi-finger CMOS transistors were fabricated using UMC 65nm-generation technology with <100>-channel orientation on (100) wafer. For enhancing the electron mobility of the channel, an 850-Å-thick SiNx CESL layer was grown as a high-tensile stressing layer. As indicated in Fig. 5-1, this eventually applied a lateral-tensile stress of 1.5 GPa along the channel of the devices. Besides, for the control device, a low-tensile-strength (SiNx=360Å)

CESL layer was used.

The gate length of the test devices varies from 60nm to 240nm, and the total gate width of the test devices is 128 μm (4 μm by 32 gate fingers). The noise parameters of the MOSFET under different temperatures were measured using Auriga scattering and noise parameter measurement system. The dummy OPEN and SHORT de-embedding technique was used to eliminate the parasitic contributions from the probing pads and metal interconnections [12]. Finally, the intrinsic channel noise current was extracted following the approach presented in [13].

Figure 5-2 compares the DC characteristics of the tensile-strained and control devices. The strained device presents larger drain current than the control one for each ambient temperature because of its enhanced carrier mobility, which can also help to boost the cut-off frequency (f_t) and maximum oscillation frequency ($f_{\max}$) as shown in Fig. 5-3.

Figure 5-4 compares the noise measurement results in terms of the minimum noise figure ($NF_{\min}$) and equivalent noise resistance (R_n) for the strained and control devices. The strained device shows the better high-frequency noise performance than the control one. The good match between the measured and modeled results based on the equivalent circuit in [14] (or refer to Fig. 6-2, Chapter 6) also indicates the validity of the extracted noise parameters shown in this chapter.

5.3 Channel Noise Characterization

The extracted power spectral density of channel noise (S_{id}) is shown in Fig. 5-5. It shows that the strained device has larger S_{id} than the control one for a given bias point. This phenomenon can be explained by the following model equation developed by Asgaran *et al.* [15]:

$$S_{id} = 4k_B T I_D \left(\frac{1}{V_{D,sat}} + \frac{\alpha^2 V_{D,sat}}{3V_{GT}^2} \right) \approx \frac{4k_B T I_D}{V_{D,sat}} \tag{5-1}$$

where $k_B \approx 1.38 \times 10^{-23}$ J/K is Boltzmann constant, T is the ambient temperature in Kelvin,

$V_{D,sat}$ is the drain saturation voltage, $V_{GT} = V_{GS} - V_T$ is the gate overdrive voltage, and α is the bulk charge coefficient.

This model indicates that in the saturation region, channel length modulation is the main mechanism responsible for the excess channel noise. Since the impact of tensile strain on $V_{D,sat}$ of the strained nFET is negligible as shown in Fig. 5-6(a), the larger drain current (I_D) present in the strained device is responsible for the larger S_{id}. The validity of Asgaran model has also been confirmed in Fig. 5-6(b).

On the other hand, the well-known van der Ziel's model [11], which uses the white-noise gamma factor to characterize S_{id}, can be written as:

$$S_{id} = \gamma 4k_B T g_{d0} \tag{5-2}$$

where g_{d0} is the channel conductance at zero drain bias, and γ is the noise factor. For long channel devices, γ would approach 2/3 in the saturation region. For short channel devices, however, it would be larger than 2/3, and can be considered as a figure of merit used to assess the excess channel noise.

Figure 5-7(a) shows the extracted g_{d0} versus temperature. The larger g_{d0} for the strained device results from its higher mobility. In addition, two different temperature dependences can be observed. At lower V_{GS}, the lowered threshold voltage at higher temperature contributes to the positive temperature coefficient of g_{d0}. At higher V_{GS}, however, the degraded carrier mobility overwhelms the effect of lowered threshold voltage at higher temperature, causing g_{d0} to decrease with increasing temperature.

Figure 5-7(b) shows both the strained and control devices have nearly the same noise factor γ, which means they suffer approximately the same short channel effect on the high frequency noise performance. Besides, since both S_{id} and I_D (or g_{d0}) scale with mobility, the result of similar γ for both the strained and control devices can be expected as indicated by Equ. (5-1). For completeness, the plot of noise factor versus channel length for different ambient temperatures is shown in Fig. 5-8. It shows that both strained and control devices

indeed have similar noise factors, which remain to increase with channel length scaling for the 65nm technology node.

It is worth noting that S_{id} tends to decrease with increasing temperature at high V_{GS} (see Fig. 5-5). This is consistent with the result for the medium-long channel device ($L = 0.36\mu m$) [16] due to the severe decrease of g_{d0} counterbalancing the increase of temperature (see Equ. (5-2)). However, the temperature dependence is not so significant for the 65nm technology under this study.

5.4 Noise Parameters Characterization

The minimum noise figure ($NF_{\min}$) and equivalent noise resistance (R_n) can be approximately expressed by the following equations [14][17].

$$NF_{\min} \approx 1 + \frac{2}{g_m^2}\sqrt{(R_s + R_g)\frac{S_{id}}{4kT_0}} \times \left\{ \omega C_{gg} g_m + \omega^2 C_{gg}^2 R_g \sqrt{\frac{S_{id}}{4kT_0}} \right\} \tag{5-3}$$

$$R_n \approx \frac{T}{T_0}(R_g + R_s) + \frac{S_{id}}{4k_B T_0 g_m^2} \tag{5-4}$$

where $T_0 = 290K$ is the reference temperature, and $C_{gg} = C_{gs} + C_{gd}$ is the gate capacitance. Note that since the induced gate noise current has been found to be insignificant at 65nm node even in the millimeter-wave application [14], it has been neglected in the above derivation.

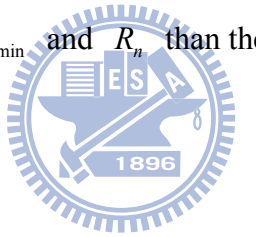
For a given DC power consumption, compared with the control device, since the strained device exhibits larger trans-conductance and comparable S_{id} as shown in Figs. 5-9 and 5-10, respectively, Equations (5-3) and (5-4) implies that the strained device would have smaller $NF_{\min}$ and R_n as shown in Figs. 5-11(a) and (b), respectively. Besides, the magnitude and phase of the optimum source reflection coefficient ($|\Gamma_{opt}|$ and $\angle\Gamma_{opt}$) for a given drain current are respectively depicted in Figs. 5-11(c) and (d) for the reader's reference, although the effect of the tensile strain on them is not significant.

Finally, it should be noted that the similar access resistances and gate capacitances

shown in Fig. 5-12 and the insets of Fig. 5-9, respectively, indicate the negligible impact of tensile strain on them for the two different fabrication processes. Therefore, they can not be attributed to the discrepancy of the high-frequency small-signal and noise performance between the strained and control devices.

5.5 Summary

In this chapter, we have investigated the high frequency noise behaviors of the tensile-strained nMOSFET. With nearly the same saturation voltages and noise factors, the strained device presents larger S_{id} than the control device due to its enhanced mobility for a given bias point. Besides, both the strained and control devices share the same temperature dependence of S_{id}. Finally, for a given DC power consumption, due to the enhanced trans-conductance, our experimental results show that, in addition to the better f_t and $f_{\max}$, the strained device has the better $NF_{\min}$ and R_n than the control device.



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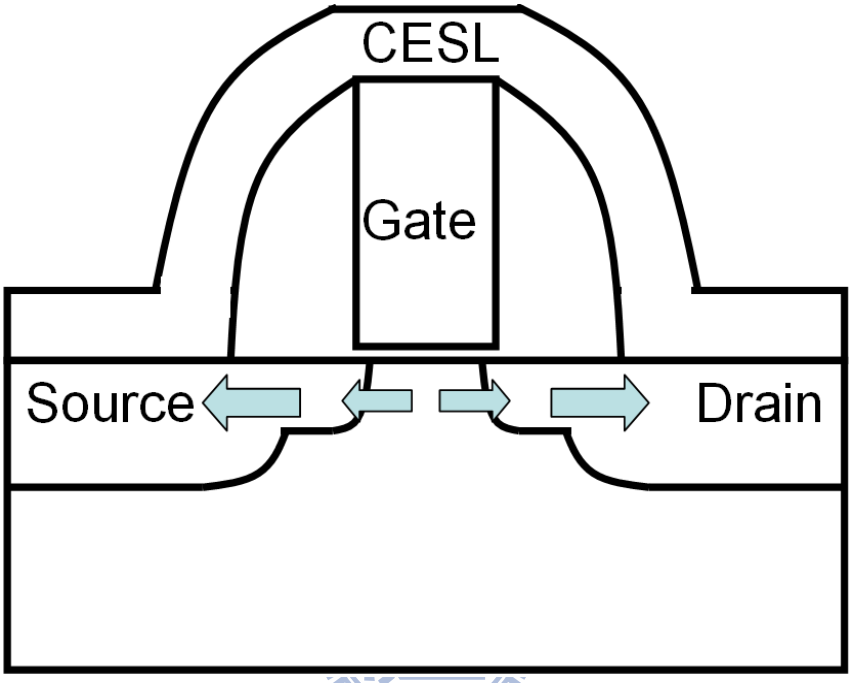

Figure 5-1 Tensile stress in the channel of a high-strained nMOSFET.

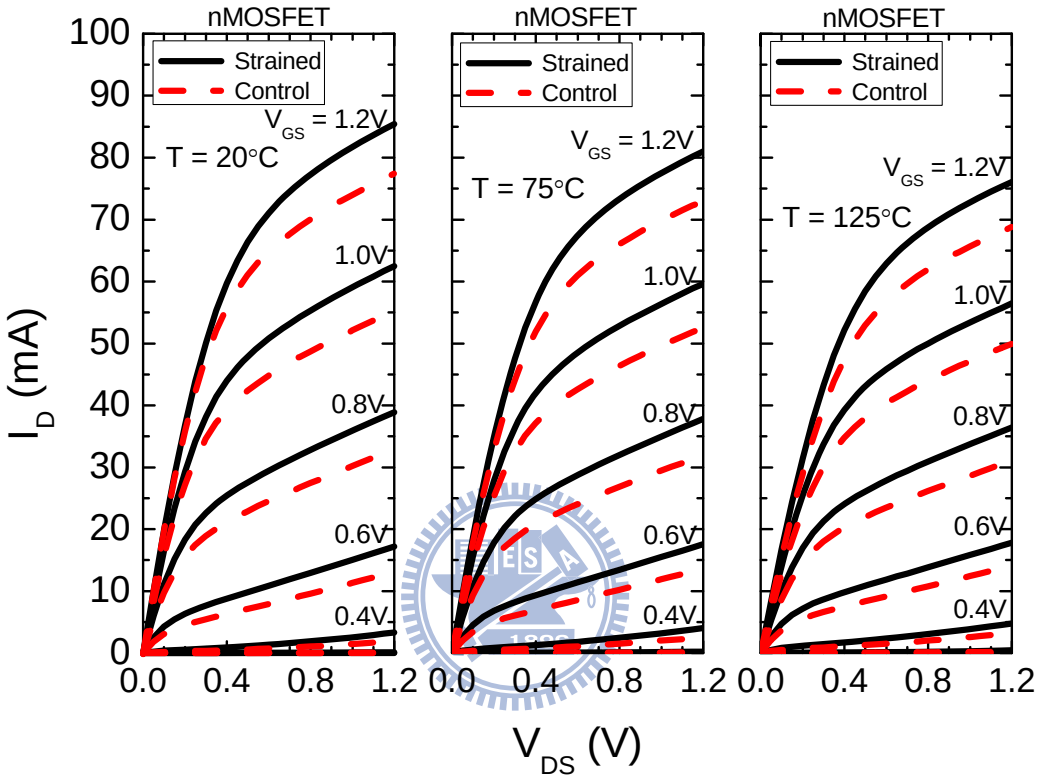

Figure 5-2 I-V characteristics for the strained and control devices. ($L = 60$nm)

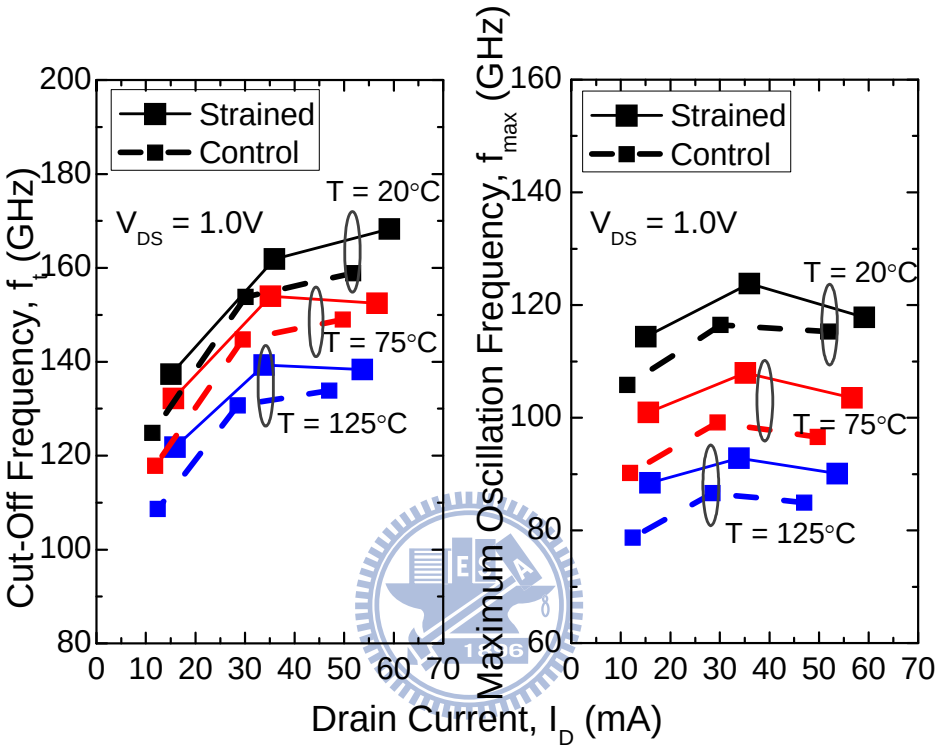

Figure 5-3 f_t and $f_{\max}$ versus drain current for the strained and control devices. ($L = 60$nm)

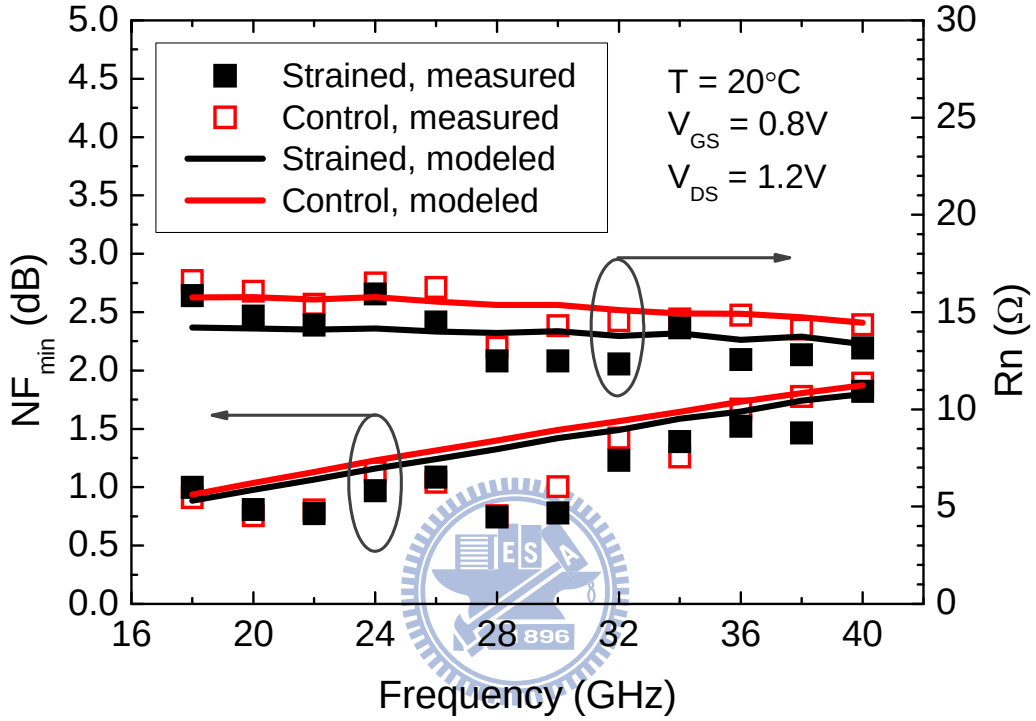

Figure 5-4 The measured and modeled results for $NF_{\min}$ and R_n. ($L = 60\text{nm}$)

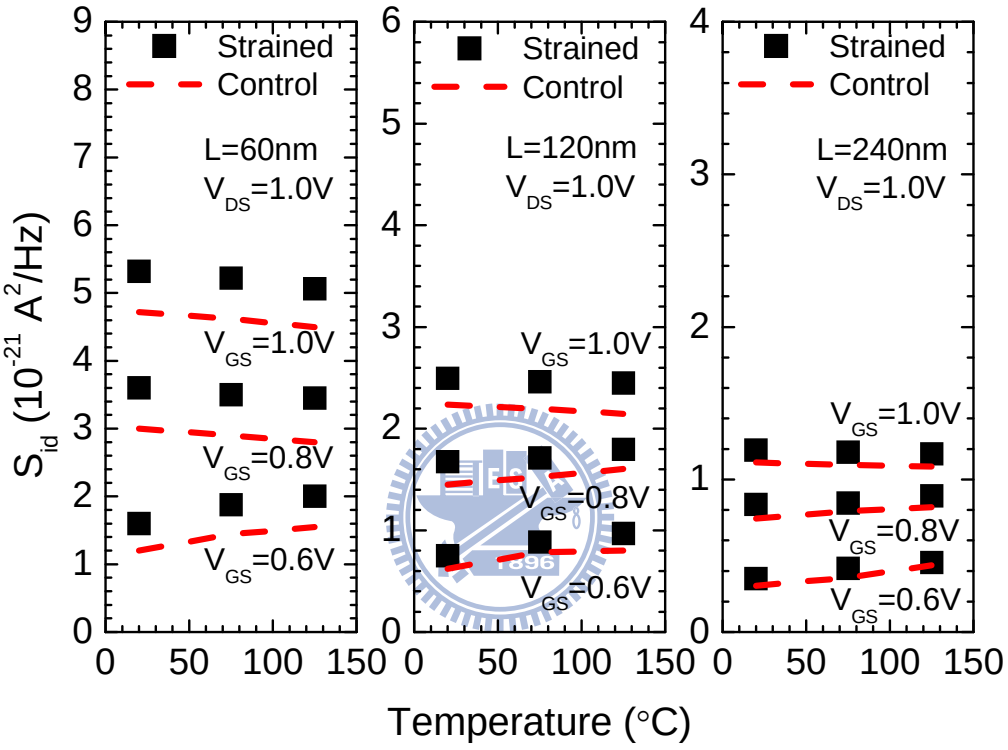

Figure 5-5 Power spectrum density of the channel noise (S_{id}) versus temperature for the strained and control devices.

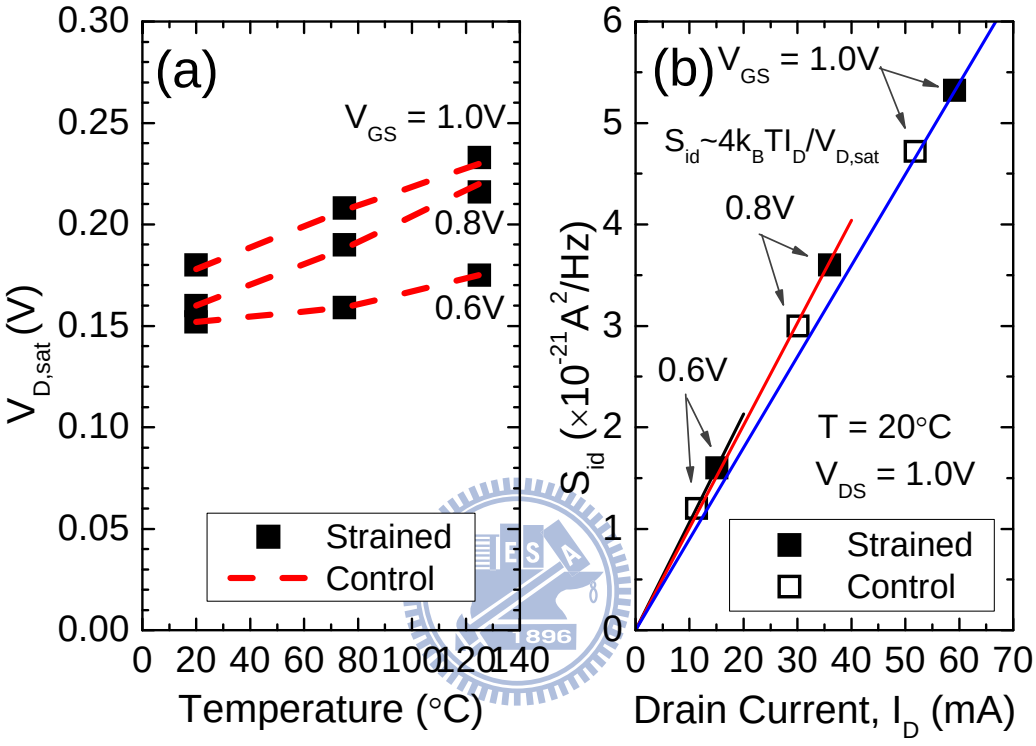

Figure 5-6 (a) Similar drain saturation voltage ($V_{D,sat}$) for the strained and control devices at each temperature, and (b) the good match between the measured S_{id} and Asgaran model (Equ. (5-1)). ($L = 60$nm)

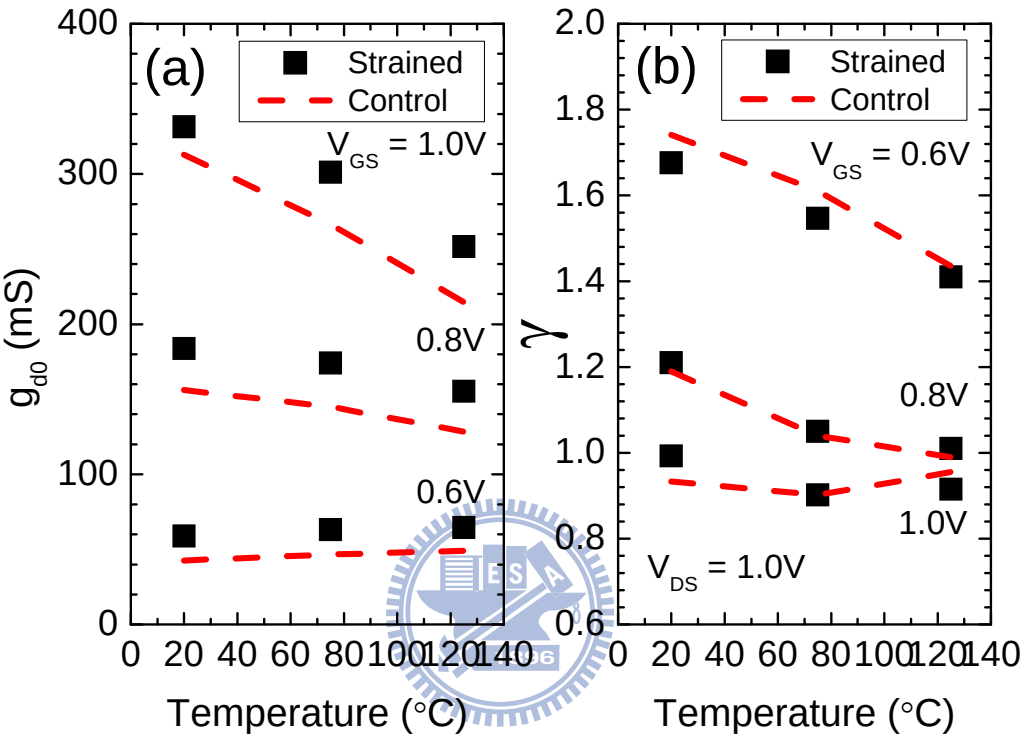

Figure 5-7 (a) Channel conductance at zero drain bias (g_{d0}) and (b) noise factor (γ) versus temperature. ($L = 60$nm)

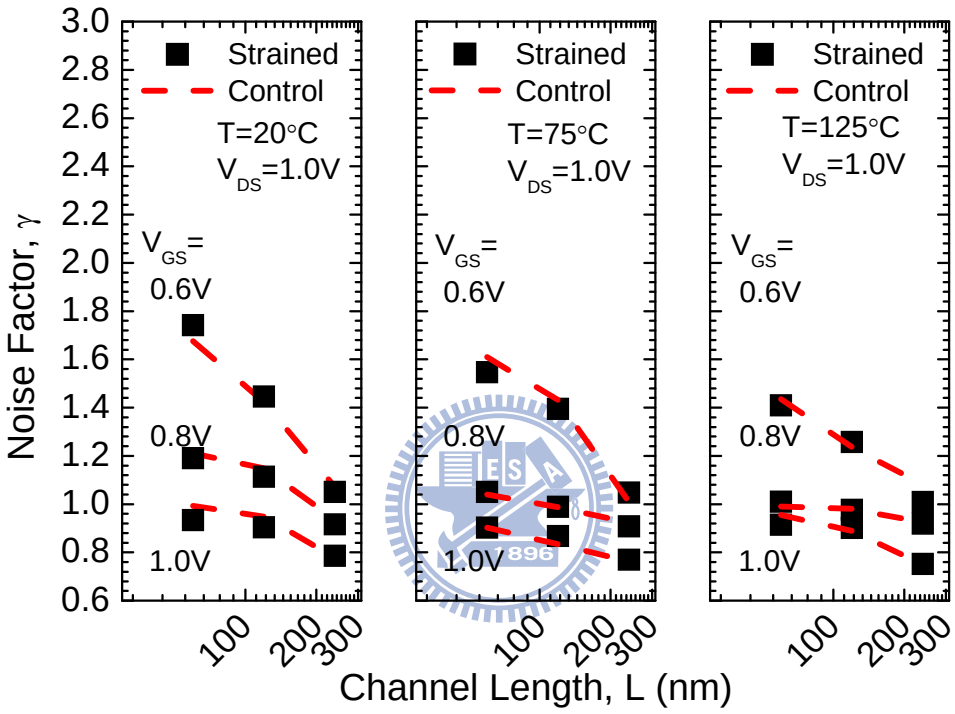

Figure 5-8 Noise factor versus channel length for different ambient temperatures.

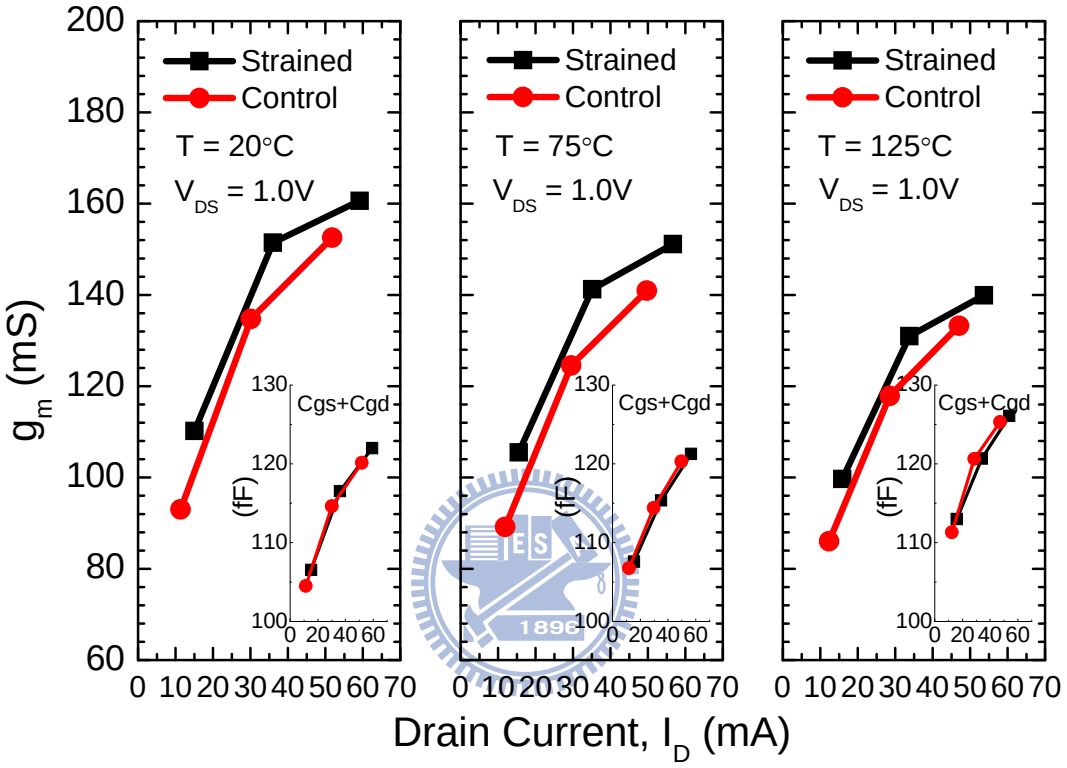

Figure 5-9 Trans-conductance (g_m) versus drain current for the strained and control devices. The insets show the gate capacitance versus drain current. ($L = 60$nm)

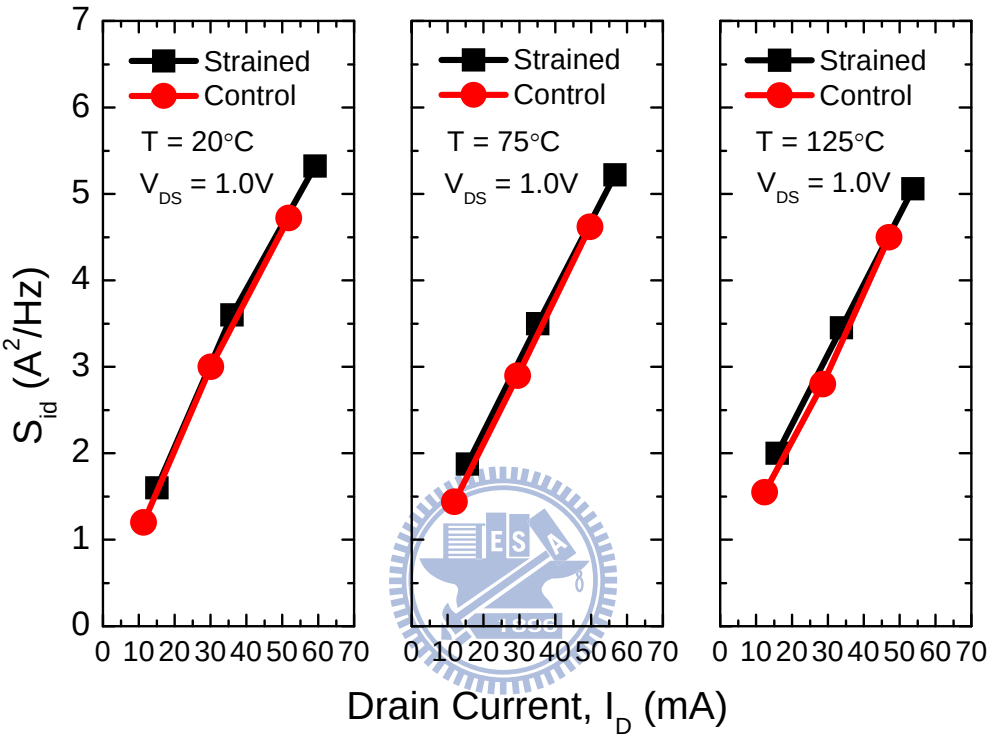

Figure 5-10 S_{id} versus drain current for the strained and control devices. ($L = 60$nm)

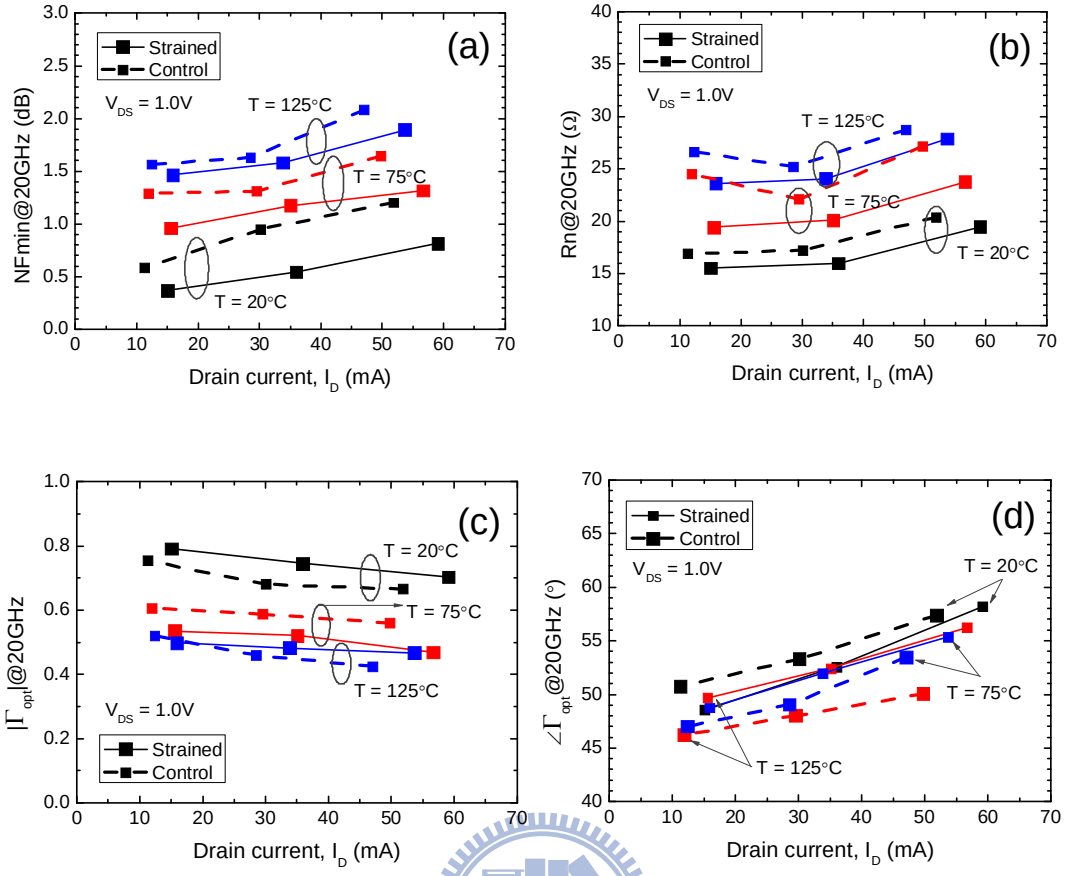

Figure 5-11 (a) $NF_{\min}$, (b) R_n, (c) $|\Gamma_{opt}|$, and (d) $\angle\Gamma_{opt}$ versus drain current for the strained and control devices. ($L = 60$nm)

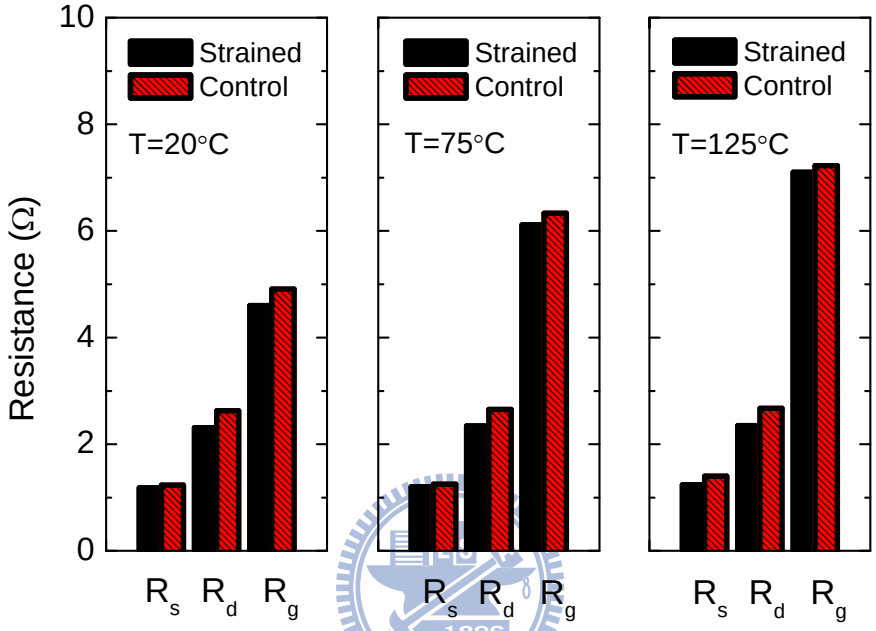

Figure 5-12 Access resistances for the strained and control devices. R_s, R_d, and R_g are access resistances associated with the source, drain and gate terminals, respectively. ($L = 60\text{nm}$)

Chapter 6

Millimeter-Wave Noise Characterization

6.1 Introduction

With the downscaling of channel length into decananometer regime, RF MOSFETs have become good choices for millimeter-wave applications [1]. Although RF noise characterization and modeling for deep sub-micron MOSFETs have been widely studied, the operating frequencies were mostly limited to several GHz and should be extended to fit the need for millimeter-wave applications. Therefore, there is an urgent need to characterize and model the noise behaviors up to millimeter-wave frequencies. Although Waldhoff *et al.* [2] have shown noise parameters covering the millimeter-wave regime, their results were based on the F50 method [3] that may not be accurate enough due to its approximations for noise parameter extraction.

In this chapter, to more accurately obtain and model the millimeter-wave noise behaviors, the tuner-based method is used instead [4]. With the help of tuner-based Auriga scattering and noise parameter measurement system [5], a complete millimeter-wave noise characterization and modeling for MOSFETs fabricated in 65nm technology can be achieved. Note that contrary to the in-situ tuner based technique [6][7], the Auriga measurement system uses an external tuner to avoid the pre-design, characterization and de-embedding of the on-die tuner, and maintains reasonable measurement results.

6.2 Devices and Experiments

The bulk devices used in this chapter were fabricated using UMC 65nm technology process and laid out in multi-fingers and multi-groups structure with two-sided gate access. The number of fingers and groups are 8 and 4, respectively, and finger length is 4 μm, which might not be optimized for millimeter-wave applications. The scattering (S) and noise

parameters (minimum noise figure $NF_{\min}$, equivalent noise resistance R_n, magnitude of optimum source reflection coefficient $|\Gamma_{opt}|$, and phase of optimum source reflection coefficient $\angle\Gamma_{opt}$) from 18 to 60GHz were measured using Auriga scattering and noise parameter measurement system, and the dummy OPEN and SHORT de-embedding technique was used to eliminate the parasitic contributions from the probing pads and metal interconnections [8]. The Auriga system was carefully calibrated and the accuracy of measurement results were confirmed by the widely used 18GHz ATN scattering and noise parameter measurement system as shown in Fig. 6-1. The good agreement between the extracted channel noise and its theoretical value for a cold device shown in Fig. 6-1(c) also validates measurement reliability.

The equivalent circuit shown in Fig. 6-2 was used to characterize devices' noise behaviors, and its small-signal model elements were carefully extracted using the approach presented in [9]. In this figure, the input resistance R_i and phase delay τ are essential in describing the intrinsic small signal behaviors when operating frequencies approach cut-off frequency (f_t), and the junction capacitance $C_{j,db}$ along with substrate resistance R_b are used to model the RF substrate loss. In addition, the series inductances (L_s, L_d, and L_g) are pronounced for the high-frequency operation. Therefore, these elements must be considered when it comes to millimeter-wave characterization and modeling. Table 6-1 shows the intrinsic small-signal parameters that can benefit the characterization of the noise parameters. Besides, since the gate current is about or smaller than $1\,\text{nA}$, its associated incremental resistance ($>100\,\text{M}\Omega$) and resulting shot noise ($\approx 10^{-28}\ \text{A}^2/\text{Hz}$) are neglected in this model.

6.3 Channel Noise Source Characterization and Modeling

Figure 3 shows the extracted power spectral density (PSD) for channel noise i_d, induced gate noise i_g, and their correlation noise (denoted as S_{id}, S_{ig}, and S_{igd^*}, respectively). To

obtain these intrinsic PSDs, the noise contributions from the parasitic series and substrate components were eliminated following the approach presented in [10]. S_{id} is shown to be frequency independent, and S_{ig} and S_{igd^*} to be proportional to f^2 and f, respectively. These relations agree with the van der Ziel model [11]. Besides, our extracted results coincide with the previous findings that with the channel length scaling, S_{id} are expected to increase, while S_{ig} and S_{igd^*} are expected to decrease [10][12] due to the smaller oxide capacitance coupling [13]. Note that due to the smaller power gain and hence the larger inaccuracy in noise measurement, the upper measurement frequency is limited to 40GHz for $L = 0.24$ μm device. The short-circuit current gain ($|H_{21}|$) and unilateral power gain (U) versus frequency are also shown in Fig. 6-4 for the reader's reference.

Traditionally, S_{id} can be expressed as [11][13]:

$$S_{id} = 4k_B T \gamma g_{d0} \tag{6-1}$$

where $k_B \approx 1.38 \times 10^{-23}$ J/K is Boltzmann constant, T is the ambient temperature in Kelvin, g_{d0} is the channel conductance at zero drain-source voltage, and γ is noise factor. The extracted noise factor versus channel length is depicted in Fig. 6-5, which shows that γ continues to increase with decreasing channel length.

Asgaran *et al.* [14] have developed an analytical expression for S_{id} based on the classical thermal noise theory with taking the channel length modulation into account.

$$S_{id} = 4k_B T I_D \left(\frac{1}{V_{D,sat}} + \frac{\alpha^2 V_{D,sat}}{3V_{GT}^2} \right) \approx \frac{4k_B T I_D}{V_{D,sat}} \tag{6-2}$$

where $V_{D,sat}$ is the drain saturation voltage, at which the carriers start to travel with their saturation velocity, V_{GT} is the gate overdrive voltage, and α is the bulk charge coefficient. The approximation is especially valid for shorter devices with smaller $V_{D,sat}$. The extracted and modeled S_{id} versus drain current I_D for different channel lengths are shown in Fig.

6-6. In our experiments, the values for $V_{D,sat}$ under a given gate bias V_{GS} were extracted by linear extrapolation in the output resistance versus drain bias plot [15], and the $V_{D,sat}$ extraction results are also shown in Fig. 6-7.

According to this model [14], devices with smaller $V_{D,sat}$, which means suffering more serious channel length modulation in the channel, would exhibit larger channel noise. As shown in Fig. 6-7, since $V_{D,sat}$ continuously decreases with downscaling channel length, one can expect that S_{id} would continue to increase as shown in Fig. 6-6. Since Equ. (6-2) was a purely thermal noise based model, the good channel noise modeling results also imply that the shot noise is not significant at 65 nm technology node, which agrees with the results shown in [16]. This also explains the increase of noise factor γ with the downscaling of the channel length.

6.4 Noise Parameter Characterization and Modeling

Based on the equivalent circuit shown in Fig. 6-2, and the channel noises extracted in the previous section, the noise parameters were simulated using Agilent ADS. Note that the noise sources associated with series resistances (R_g, R_s, and R_d) and substrate resistance (R_b) are considered as thermal noise, and their PSDs can be expressed as $4k_BT/R$, where R is the resistance value. In addition, for simplification, we have neglected S_{ig} and S_{igid^*} as in [17]. To validate the assumption for millimeter-wave modeling, both the modeling results with and without considering S_{ig} are shown in Fig. 6-8 for comparison. This figure shows that without considering S_{ig}, the errors are still within acceptable range especially for $L = 0.12$ μm and $L = 0.06$ μm devices, and this supports the approximation we used in the millimeter-wave modeling. Besides, since the $L = 0.24$ μm device is not suitable for millimetre-wave application due to its low cut-off frequency f_t and maximum oscillation

frequency $f_{\max}$ as implied in Fig. 6-4, the larger errors in $NF_{\min}$ and G_{opt} for this device may not be a concern for millimeter-wave applications.

6.4.1 Intrinsic Noise Parameters

Neglecting S_{ig} and S_{igid^*}, the intrinsic noise parameters can be expressed as follows.

$$R_{n,\text{int}} = \frac{S_{id}}{4k_B T_0 \left(g_m^2 + \omega^2 C_{gd}^2\right)} \tag{6-3}$$

$$G_{opt,\text{int}} = \text{Re}\left(\frac{1-\Gamma_{opt,\text{int}}}{1+\Gamma_{opt,\text{int}}}\right) \approx \frac{\omega^2 C_{gs}^2 R_i}{1+\omega^2 C_{gs}^2 R_i^2} \tag{6-4}$$

$$B_{opt,\text{int}} = \text{Im}\left(\frac{1-\Gamma_{opt,\text{int}}}{1+\Gamma_{opt,\text{int}}}\right) \approx -\omega\left(C_{gs}+C_{gd}\right) \tag{6-5}$$

$$NF_{\min,\text{int}} \approx 1 + 4R_{n,\text{int}} G_{opt,\text{int}} \approx 1 + \frac{S_{id}}{k_B T_0 \left(g_m^2 + \omega^2 C_{gd}^2\right)} \frac{\omega^2 C_{gs}^2 R_i}{1+\omega^2 C_{gs}^2 R_i^2} \tag{6-6}$$

where the subscript 'int' means the intrinsic part, and $T_0 = 290\text{K}$ is the reference temperature.

A good figure of merit (FOM) to judge the intrinsic noise performance is $S_{id}/\left(g_m^2 + \omega^2 C_{gd}^2\right) \approx S_{id}/g_m^2$. According to Equ. (6-3), lower S_{id}/g_m^2 can lead to smaller $R_{n,\text{int}}$, which can benefit the input matching for circuit design. Figure 6-9 depicts S_{id} and $R_{n,\text{int}}$ versus g_m^2 for different channel lengths. It shows that with length scaling down, the increase of the channel noise tends to overwhelm the increase of g_m^2, and in turn degrades $R_{n,\text{int}}$.

6.4.2 The Impact of Gate Resistance on Noise Parameters

It has been shown that the gate resistance has significant impact on the noise parameters

and can not be ignored in deep sub-micron noise modeling [17][18]. In fact, as the gate resistance exists, the total expressions for noise parameters have the following relations to the intrinsic ones.

$$R_n \approx R_{n,\text{int}} + \frac{T}{T_0} R_g \tag{6-7}$$

$$B_{opt} \approx \frac{R_{n,\text{int}}}{R_n} B_{opt.\text{int}} \tag{6-8}$$

$$G_{opt} \approx \sqrt{\left(\frac{R_{n,\text{int}}}{R_n}\right)\left(G_{opt,\text{int}}^2 + B_{opt,\text{int}}^2\right) - \left(\frac{R_{n,\text{int}}}{R_n}\right)^2 B_{opt,\text{int}}^2} \tag{6-9}$$

$$NF_{\min} \approx 1 + 2R_n G_{opt} + 2R_g R_{n,\text{int}}\left(G_{opt,\text{int}}^2 + B_{opt,\text{int}}^2\right) \tag{6-10}$$

These equations suggest that the gate resistance would highly increase equivalent noise resistance and minimum noise figure. In addition, since the gate resistance is significant in shorter devices as shown in Fig. 6-10, its impact on their noise parameters is expected to be more serious. This is also confirmed in Fig. 6-8, where larger error can occur in the shorter device without considering the gate resistance.

Note that for cases where R_s is comparable or even larger than R_g as in [17], more accurate equations can be obtained by replacing R_g with $R_g + R_s$ in Equs. (6-7) to (6-10). Besides, the value of R_g can be changed as a function of the gate materials, the number of gate fingers, and the gate layout geometry. Therefore, the effect of R_g on the noise parameters can be greatly varied at different cases.

6.4.3 The Impact of Substrate Resistance on Noise Parameters

Reference [19] has considered the effect of substrate resistance (R_b) on high-frequency noise modeling. The modeling results without considering the substrate resistance are also shown in Fig. 6-8. This figure shows, however, as compared to R_g, the substrate resistance

R_b has much smaller influence on noise parameters. To explain this, one can find that at very high frequency, the drain-side noise current's PSD can be approximated by $S_{id} + S_{ib}$, where $S_{ib} = 4k_B T / R_b$ is the noise current PSD for the substrate resistance. As shown in Fig. 6-11, based on the extracted values of R_b, S_{ib} is about 1/10 of S_{id} at the very high frequency and can be ignored. That is, in millimeter wave frequencies, the overall noise performance would be mainly dominated by S_{id} and R_g.

6.5 Summary

We have demonstrated the millimeter-wave noise characterization and modeling for 65nm MOSFETs based on the tuner method for the first time. Our experimental results show that with the continuous down scaling of channel length, the channel noise S_{id} would remain the dominant noise source in the intrinsic part of the device due to the serious channel length modulation, and can be predicted by the traditional thermal noise theory. The sharply increased S_{id} also degrades R_n.

Finally, the millimeter-wave noise modeling is achieved. With the help of circuit simulation, the impact of R_g and R_b on the noise parameters has been examined. Compared to R_b, R_g is shown to have more serious influence on the noise parameters, and should be included in the millimeter-wave noise modeling.

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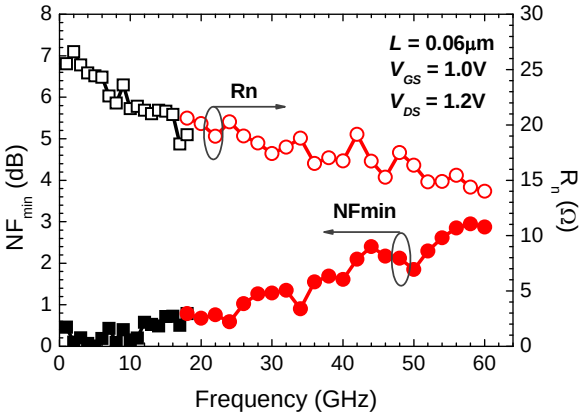
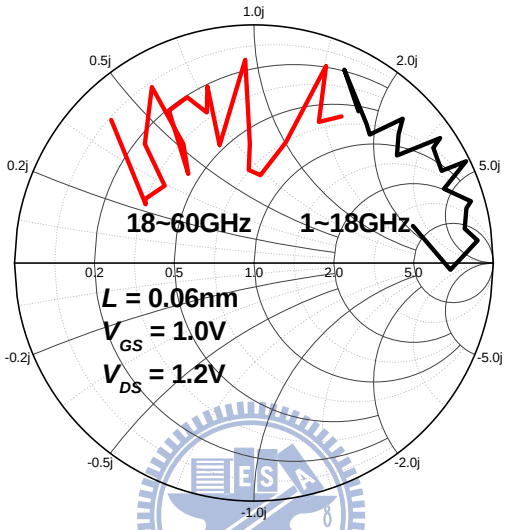
Table 6-1 Extracted intrinsic small-signal parameters that can benefit the characterization of the noise parameters. ($V_{GS}=1.0\text{V}$, $V_{DS}=1.2\text{V}$)

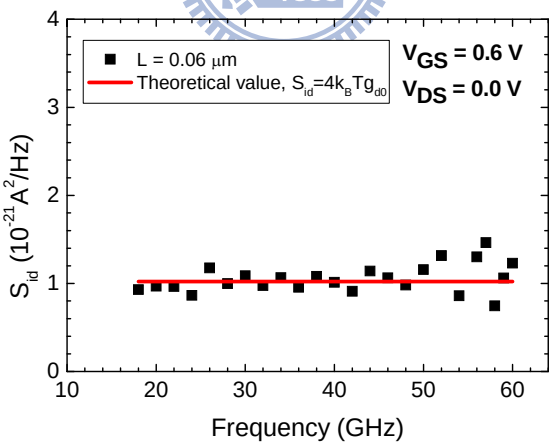
$L(\mu\text{m})$	$R_i(\Omega)$	$g_m(\text{mS})$	$C_{gs}(\text{fF})$	$C_{gd}(\text{fF})$	$\tau(ps)$
0.06	6.8	151.8	71.3	36.4	0.2
0.12	3.4	106.9	146.3	42.4	0.7
0.24	3	74.8	317.2	`47.6	1.2



(a)



(b)



(c)

Figure 6-1 Broadband (1 to 60GHz) noise parameters. (a) $NF_{\min}$ and R_n versus frequency plot, and (b) Γ_{opt} in Smith Chart. The data below 18GHz were measured by ATN system, while above were measured by Auriga system. (c) Good agreements between extracted channel noise and its theoretical value for a cold device.

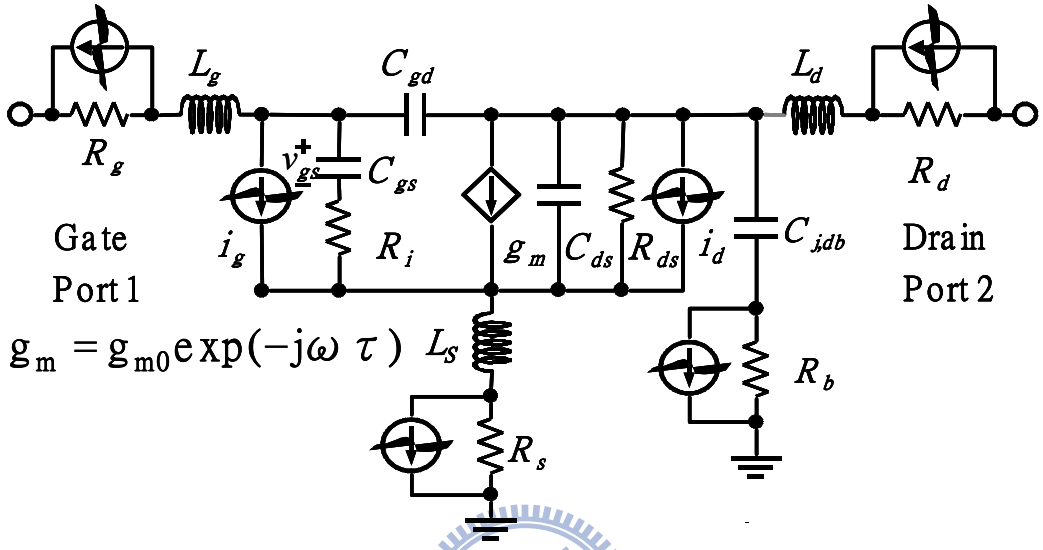
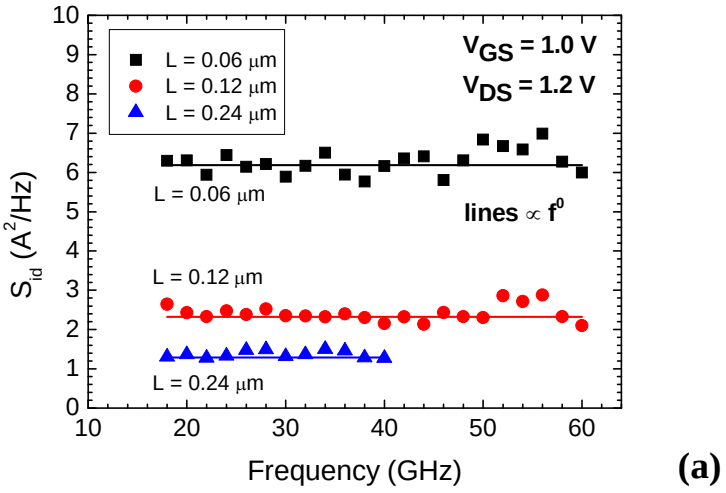
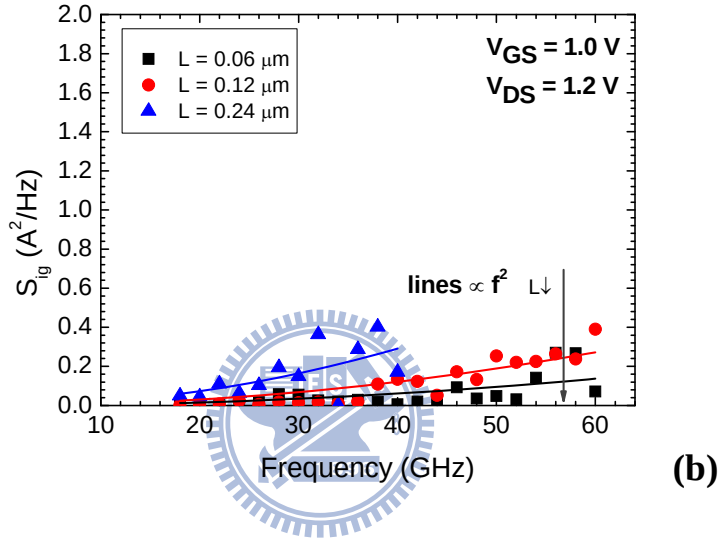


Figure 6-2 RF noise equivalent circuit for the bulk MOSFET.





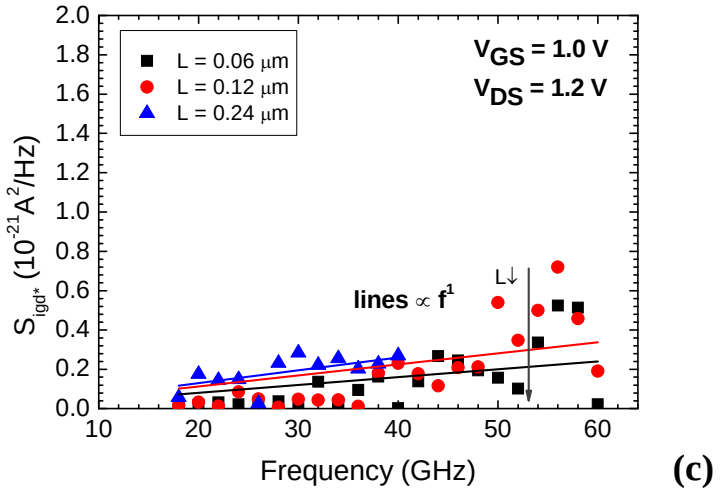


Figure 6-3 Extracted (a) S_{id}, (b) S_{ig}, and (c) S_{igd^*} versus frequency. The solid lines show the frequency dependence.

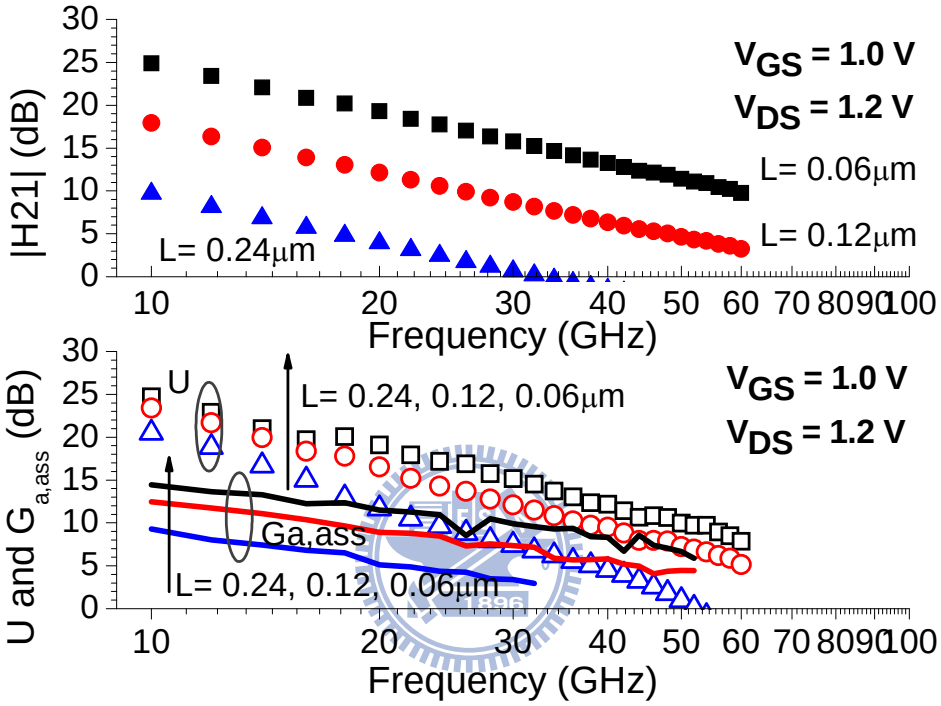


Figure 6-4 Short-circuit current gain ($|H_{21}|$), unilateral power gain (U), and associated gain ($G_{a,ass}$) versus frequency.

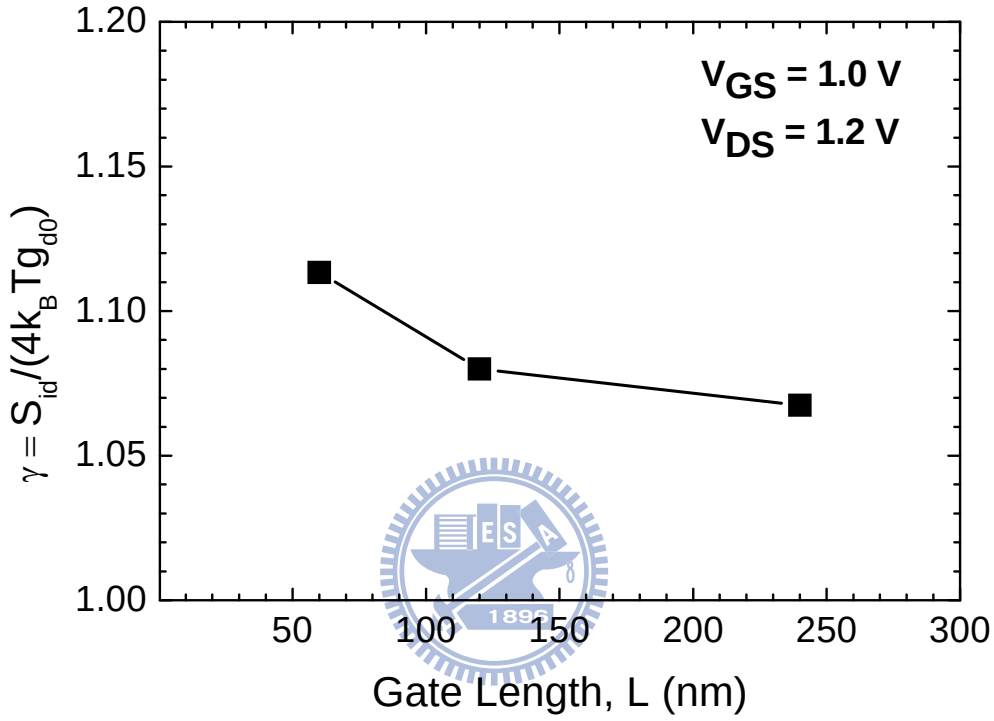


Figure 6-5 Noise factor γ versus gate length.

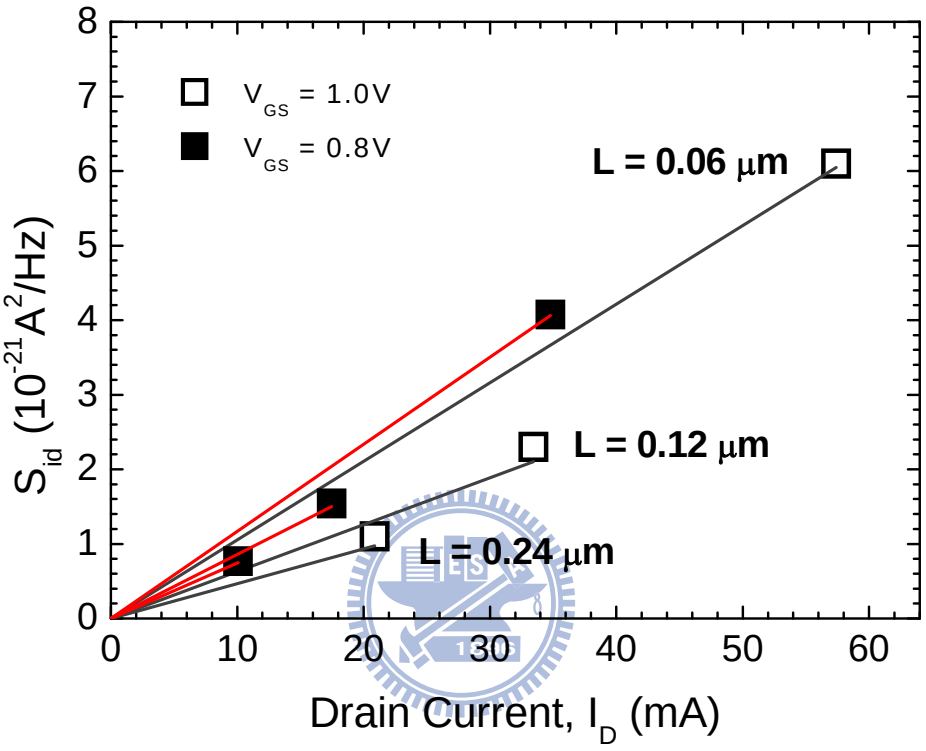


Figure 6-6 Extracted channel noises (symbols) and their theoretical values (lines) calculated using Equ. (6-2) versus drain current.

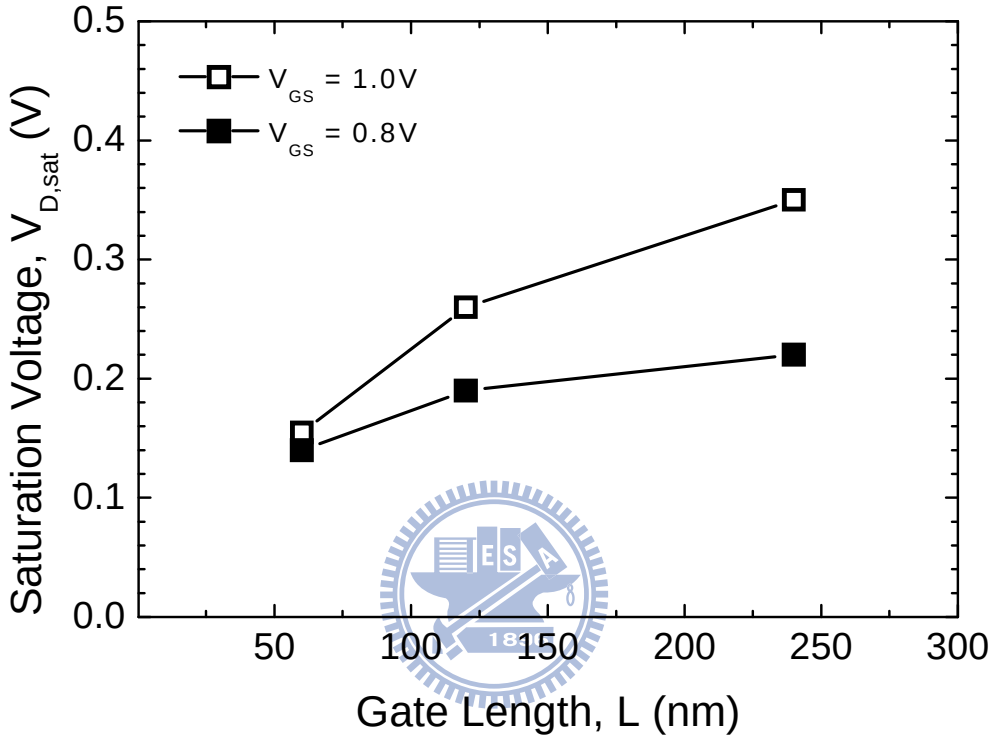


Figure 6-7 Saturation voltage versus channel length.

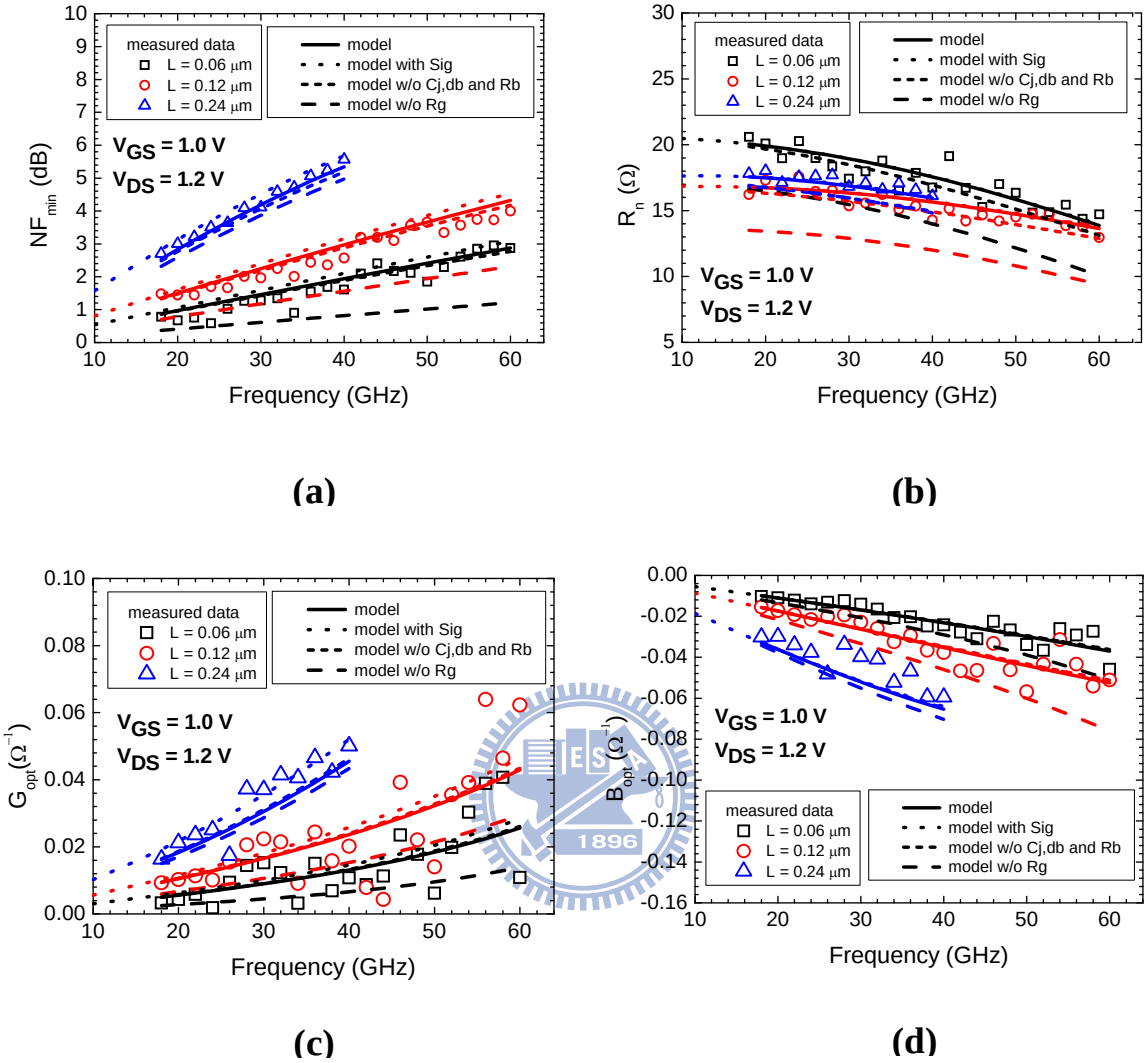


Figure 6-8 Modeled (a) $NF_{\min}$, (b) R_n, (c) G_{opt}, and (d) B_{opt} versus frequency. The impact of S_{ig}, the gate resistance and the substrate resistance on these noise parameters are also shown.

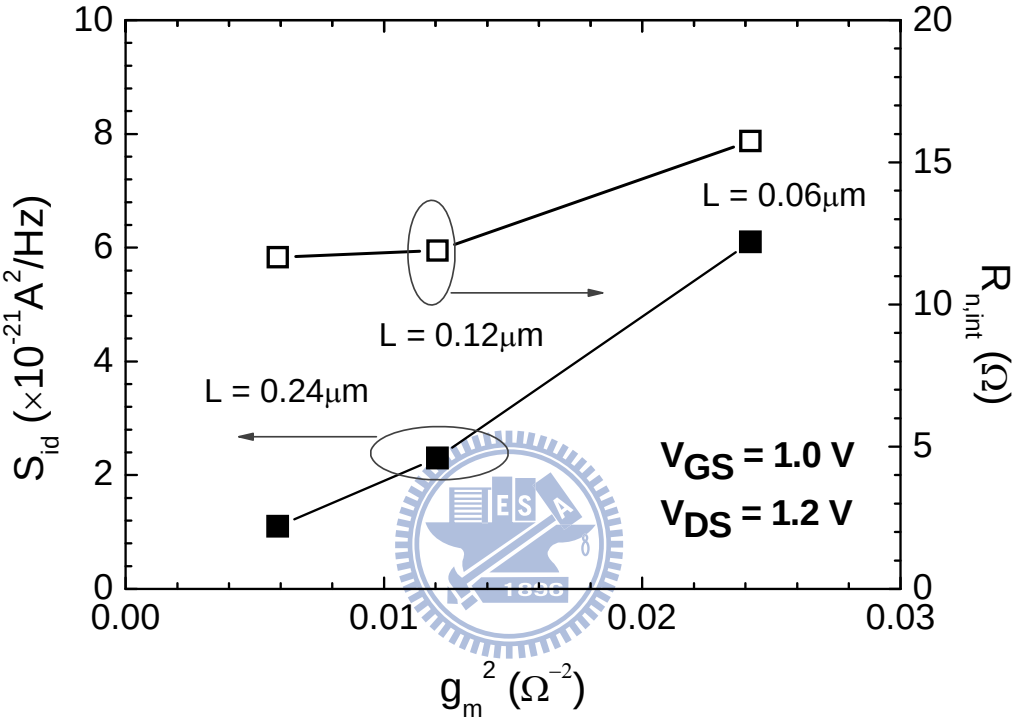


Figure 6-9 S_{id} and $R_{n,\text{int}}$ versus g_m^2.

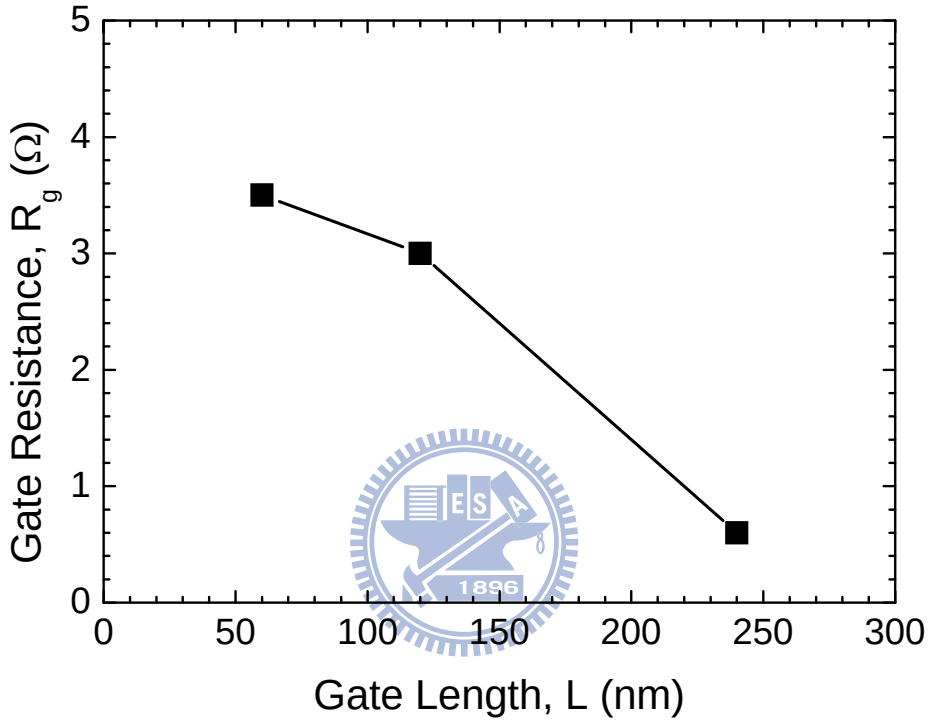


Figure 6-10 Extracted gate resistance (R_g) versus channel length.

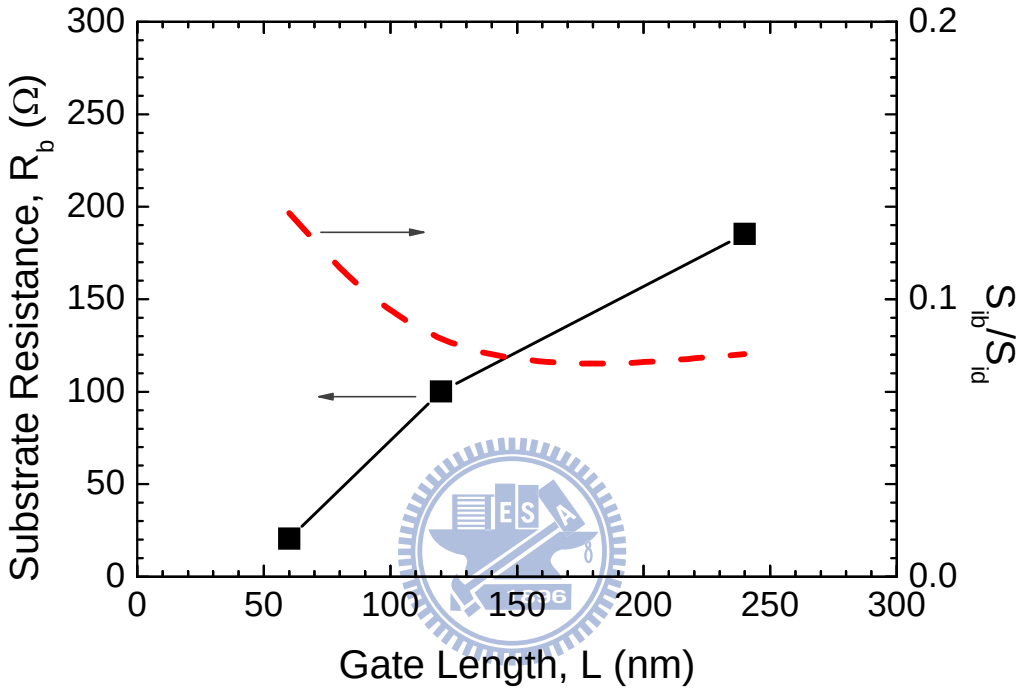


Figure 6-11 R_b and S_{ib}/S_{id} versus gate length.

Chapter 7

Conclusion

In this dissertation, based on the traditional RF small-signal and noise framework, we have comprehensively investigated the RF noise characteristics for various kinds of MOSFETs fabricated in contemporary advanced process technologies. These devices include bulk MOSFETs, SOI MOSFETs [1][2], SOI DT MOSFETs [3][4], and tensile-strained MOSFETs [5]. To achieve this goal, we have tailored the traditional small-signal equivalent circuit to take into account the specific effects present in respective MOSFET devices. The corresponding approaches to the extraction of small-signal and noise parameters have also been well developed. For the first time, the temperature effect on the RF noise behaviors for each device has been investigated as well [6].

In Chapter 2, the need of considering the neutral-body effect on the RF SOI small-signal modeling has been demonstrated. Due to this SOI-specific effect, the traditional equivalent circuit for bulk MOSFETs and its corresponding parameter extraction methods have to be modified accordingly both in the extrinsic and intrinsic parts. Our measurement results have shown that the neutral-body effect may influence the output characteristics of RF SOI MOSFETs in the GHz regime. The anomalous S_{22} and S_{21} behaviors can also be predicted and captured using our proposed model.

In Chapter 3, we have investigated the noise characteristics for both the bulk and SOI MOSFETs. The channel noise S_{id} is found to decrease with increasing temperature due to lower channel conductance at higher temperature. However, this trend is not obvious for devices with channel length below $0.12\mu m$. Compared to the bulk MOSFETs, the SOI devices own the larger noise factors. The inherent floating-body effect and self-heating effect may contribute to this phenomenon. Our experimental results also show that the SOI device has worse $NF_{\min}$ and R_n than the bulk counterpart due to its larger S_{id} and lower g_m.

In Chapter 4, the temperature dependences of RF small-signal and noise behaviors for the SOI DT MOSFET have been studied. In the attractive low VDD regime, g_m tends to increase with increasing temperature, and hence causes both f_t and $f_{\max}$ to have positive temperature coefficients. Besides, due to larger g_{d0} at higher temperature, the channel noise S_{id} also has a positive temperature coefficient in the low VDD regime. In addition, compared to S_{id}, the much higher g_m^2 towards the weaker inversion region can cause R_n to have a negative temperature coefficient. Our study also indicates that in the low VDD regime, the large R_b has little impact on the temperature dependence of $NF_{\min}$ for the SOI DT MOSFET.

In Chapter 5, the high frequency noise behavior of the tensile-strained nMOSFET has been examined. The strained device presents larger S_{id} than the control device due to its enhanced mobility for a given bias point, while both the strained and control devices have the same temperature dependence of S_{id}. However, for a given DC power consumption, due to the enhanced trans-conductance, our experimental results show that the strained device has better $NF_{\min}$ and R_n than the control one.

In Chapter 6, we have demonstrated the millimeter-wave noise characterization and modeling for 65nm MOSFETs based on the external tuner method for the first time [7]. In the millimeter-wave frequency band, the channel noise S_{id} remains the dominant noise source in the intrinsic part of the device, and can still be well predicted by the traditional thermal noise theory. We also show that compared to the substrate resistance R_b, the gate terminal resistance R_g has more serious influence on the millimeter-wave noise parameters.

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High-Frequency Small-Signal and Noise Characterization for Advanced MOSFETs Considering Temperature Dependence

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