國立交通大學

電子工程學系 電子研究所

博 士 論 文

應用於行動電視標準之射頻電路及系統

RF Circuits and Systems for Mobile TV Applications

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中 華 民 國 九 十 九 年 七 月

應 用 於 行 動 電 視 標 準 之 射 頻 電 路 及 系 統

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博 士 論 文

A Dissertation
Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering

July 2010
Hsinchu, Taiwan, Republic of China

中華民國九十九年七月

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摘要

本篇論文主要探討手持式行動射頻調諧器於系統層級及電路層級，實現考量之解決方案。本文針對詳細之設計流程(以地面/手持式數位視訊廣播(DVB-T/H)標準為例)，從標準規格研讀、轉換成射頻接收機規範之考量及推導、再切分成細部電路方塊之實現要求，做一完整呈現。三個高整合性射頻調諧器已實現於先進 CMOS 製程以驗證系統設計概念之完善程度。三個實驗晶片皆採用直接降頻架構，以期達成最高之整合性及硬體共享程度。

第一個高整合性調諧器晶片設計實現於 0.13μm CMOS 製程。此射頻調諧器包含射頻前端電路、類比基頻電路、及頻率合成器，並支援雙頻帶之操作。射頻前端電路包含一創新之單端轉雙端之低雜訊放大器，及一電流切換模式之可變增益技巧，以期可達成最佳之訊號－雜訊/干擾比。為了實現一低電壓操作、低功率消耗、及高整合性之射頻調諧器設計，許多電路設計技巧被巧妙使用、並於本文中仔細討論描述。此接收機在單一 1.2 伏特操作下，可達成 -96.7dBm 之接收敏感度，連續操作模式下整體電路功耗為 114 毫瓦。

第二個高整合性調諧器晶片設計實現於 65nm CMOS 製程。此射頻調諧器整合一創新之可支援單端及雙端輸入之低雜訊放大器，以適合發展單端輸入(低成本,RF 單晶片)或雙端輸入(高抗雜訊干擾,適用系統單晶片)之解決方案，

並降低晶片研發過程再投片的風險。此部分研究同時探討當製程從 0.13μm 轉換至 65nm 製程時，RF 電路設計必要之考量及挑戰。晶片系統性能驗證流程（含數位解調器）及結果，也詳盡描述於本文中。此接收機在單一 1.2 伏特操作下，達成-97.3dBm 之接收敏感度，連續操作模式下整體電路功耗僅為 88 毫安培。

RF Circuits and Systems for Mobile TV Applications

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Abstract

This dissertation is focused on system-level and building-block-level solutions in realization of mobile TV tuners. Detailed design procedures starting from standard specifications to receiver specifications to building block requirements is presented, with an emphasis on the DVB-T/H standard. To demonstrate the design aspects, three fully integrated RF tuner prototypes were realized in advanced CMOS technologies. Direct-conversion architecture was used to achieve maximum-level of integration and block sharing.

The first prototype was designed and implemented in 0.13μm CMOS technology to meet the specifications of DVB-T/H standard. The tuner supports dual-band operation and includes RF front-end, analog baseband, and frequency synthesizer. The front-end comprises a novel single-to-differential low noise amplifier (LNA) and a novel variable-gain technique to maintain the maximum signal-to-noise-and-interference ratio (SNIR). Techniques to enable low-voltage, low-power, and high-integration tuners are discussed in more details. The receiver achieves a sensitivity level of -96.7dBm and dissipates 114mW from a 1.2 V supply.

The second prototype was designed and implemented in 65nm CMOS technology, based on the same architecture. A wideband LNA compatible for differential and single-ended inputs was integrated to meet the requirements either on RF-alone or system-on-a-chip (SoC) developments and to reduce the risks of design re-spin. The description in the second implementation is mainly focused on the specific challenges related to the 65nm CMOS technology. Detailed chip verification is presented, including system-level using a digital demodulator. The receiver achieves a sensitivity level of -97.3dBm and dissipates 88mA from a 1.2 V supply.

誌謝

得以順利完成博士論文，首先要感謝我的指導教授－郭建男博士，老師多年來的悉心指導，尤其論文撰寫上對我提出許多懇切的建議與指導，讓我穫益良多。感謝呂良鴻教授、呂學士教授、孟慶宗教授、徐碩鴻教授、溫瓌岸教授、劉深淵教授、鍾世忠教授(以上依中文姓氏筆劃排列)，於百忙之中撥空擔任我的論文口試委員，並對本論文提出許多寶貴的意見，使其更臻完善。

在此要特別感謝一些學弟及同事: 小文、志宏、宜興、仕豪、家洪。沒有小文的類比基頻電路及志宏的頻率合成器設計，就無法順利將系統規劃設計做完整硬體驗證，也不可能有 0.13 微米高整合度射頻調諧器的整體研究成果；也感謝宜興、仕豪、家洪的接續，一起完成 65 奈米調諧器的研究開發，也因此有機會讓整個技術研究探討更為完整；另外，感謝廖素琴女士在打線上不厭其煩的給予協助。除此之外也要感謝我在職場上的好長官，感謝許峻銘博士在我前幾年職場生涯上所給予的指導與協助，從他身上學習到很多做事的態度及方法。感謝楊子毅組長多年來的支持與包容，提供我們充分的空間去挑戰前瞻技術，也讓我能在工作與學業上取得平衡。另外，要感謝台積電提供 65 奈米先進製程，得以進行 65 奈米調諧器之下線驗證。

感謝實驗室的學長、學弟妹們，特別感謝俊興、燕霖、博一幫忙處理博士口試準備事項。

最後，要特別感謝我的家人，因為有他們的全力支持，讓我得以專心致力於自我的發展。

謹以此論文獻給每一個關心我、愛我的人。

郭明清

2010/09

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Abbreviations

4G	4th Generation
ABB	Analog Baseband
ADC	Analog-to-Digital Converter
AFC	Adaptive Frequency Calibration
AGC	Automatic Gain Control
ATT	Attenuation
AWGN	Additive White Gaussian Noise
BBP	Baseband Processor
BCC	Bulk Cross-Coupling
BER	Bit Error Rate
BOM	Bills of Material
BW	Bandwidth
C/N	Carrier-to-Noise
CCC	Capacitor Cross-Coupling
CD	Common Drain
CG	Common Gate
CML	Current-Mode Logic
CMMB	China Mobile Multimedia Broadcasting
CMOS	Complementary Metal-Oxide Semiconductor
CMR	Common-Mode Rejecting
CMRR	Common-Mode Rejection Ratio
COB	Chip on a Board
CR	Coding Rate
CS	Common Source
CW	Continuous Wave
dB	Decibel
dBv	Decibel Volt (peak)
DC	Direct Current
DCC	Dual Cross-Coupling
DCOC	DC Offset Cancellation
DR	Dynamic Range
DSB	Double Side Band

DSP	Digital Signal Processing
DVB-H	Digital Video Broadcasting–Handheld
DVB-T	Digital Video Broadcasting–Terrestrial
ESD	Electrostatic Discharge
ETSI	European Telecommunications Standards Institute
EVM	Error Vector Magnitude
F	Noise Factor
ft	Transit frequency
GSM	Global System for Mobile communications
I/Q	In-phase/quadrature
I2C	Inter-Integrated Circuit
IF	Intermediate Frequency
IIP2	2nd-order Input Referred Intercept Point
IIP3	3rd-order Input Referred Intercept Point
IM2	2nd-order Intermodulation
IM3	3rd-order Intermodulation
IMD	Intermodulation Distortion
IMRR	Image Rejection Ratio
ISDB-T	Integrated Services Digital Broadcasting – Terrestrial
k	Boltzmann constant
LDO	Low-Dropout Regulator
LG	Low-Gain
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LTE	Long Time Evolution
MBRAI	Mobile and portable DVB-T/H Radio Access Interface
MediaFLO	Media Forward Link Only
MER	Modulation Error Ratio
MIM	Metal-Insulator-Metal Capacitor
MMIC	Monolithic Microwave Integrated Circuit
NF	Noise Figure
NMOS	N-Channel Metal-Oxide Semiconductor
OFDM	Orthogonal Frequency-Division Multiplexing
PAL	Phase Alternate Line
PAPR	Peak to Average Power Ratio
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase-Locked Loop
PMOS	P-Channel Metal-Oxide Semiconductor

PVT	Process, Voltage, Temperature
QAM	Quadrature Amplitude Modulation
QFN	Quad Flat Non-leaded package
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RFC	RF Chock
RFE	RF Front-End
RFIC	Radio Frequency Integrated Circuit
RSSI	Received Signal Strength Indicator
Rx	Receiver
SAW	Surface Acoustic Wave
SMA	SubMiniature version A
SNIR	Signal-to-Noise- and-Interference Ratio
SNR	Signal-to-Noise Ratio
SoC	System-on-a-Chip
T	Absolute temperature
T-DMB	Terrestrial Digital Multimedia Broadcasting
TIA	Transimpedance Amplifier
U/D	Unwanted-to-Desired power ratio
UHF	Ultra-High Frequency
VCO	Voltage Control Oscillator
VDD	Power Supply Voltage
VGA	Variable Gain Amplifier
VGCF	Variable-Gain low-pass Channel Filter
VGLNA	Variable-Gain LNA
VHF	Very High Frequency
VSA	Vector Signal Analyzer
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	Wireless Local Area Network

Chapter 1

Introduction

1.1 Background

In recent years, television broadcasting systems all over the world have been gradually switching over from analog to digital. These digital broadcasting technologies bring several advantages in bandwidth efficiency, robustness, and signal quality. Currently, technological developments have introduced mobile TV, making it possible to efficiently receive TV channels and other high bit-rate services in handheld devices. In order to support these new applications, the existing broadcast TV standards are augmented to meet the more demanding requirements on mobile receptions. This chapter provides an overview of mobile TV standards.

1.2 Overview of Mobile TV Standards

There exist several mobile TV standards being developed and emerging around the world. Each of them dominates the mobile TV technology in different parts of the world and till date there is no single globally accepted standard. Below listed are main dominant mobile TV standards along with their brief profiles.

Digital Video Broadcasting–Handheld (DVB-H) [1] is a standard proposed by the DVB Group for the delivery of digital multimedia content to mobile, handheld devices. The physical layer of DVB-H systems essentially conforms to the DVB-T specification, with a limited number of extensions. The new features make it possible

to efficiently receive high data-rate services in battery-powered devices. To increase power saving, each service is transmitted in bursts with a typical 1:10 on/off ratio using the whole available bandwidth. As claimed in the DVB-H standard, this time slicing technique can reduce the power consumption up 90 percent with respect to a non-time-sliced transmission. On the other hand, the Multi-Protocol Encapsulation–Forward Error Correction (MPE-FEC) technique is introduced to increase the carrier-to-noise (C/N) and Doppler performance in mobile channels.

The DVB-H system is fully compatible with the DVB-T network and system, allowing for the use of the existing DVB-T equipments. It utilizes a part of the frequency range for DVB-T, including VHF III and UHF bands with a channel bandwidth of 6/7/8MHz. In addition, a 5MHz channel in L-band (1670-1675MHz) has been allocated for the DVB-H operation in the United States. In Europe, the additional usage of 1450-1490MHz L-band is also discussed.

Terrestrial Digital Multimedia Broadcasting (T-DMB) [2] was developed in South Korea, and its physical parameters are identical to the European DAB (Digital Audio Broadcasting) standard. T-DMB uses OFDM technology and operates with a 1.536MHz bandwidth. For the mobile reception, its frequency band is allocated at VHF III and 1450-1492MHz bands. It offers 1.06 Mbits/s – 2.3 Mbits/s data rate.

Integrated Services Digital Broadcasting – Terrestrial (ISDB-T) [3] was developed in Japan since 1999, and also adopted as Brazil's standard in 2006. ISDB-T uses a COFDM multicarrier system as in DVB-T, but is more complex and robust. The 6 MHz-wide channel can be subdivided into 13 segments. One segment has a width of 430 kHz with a guard band of about 200 kHz each for the upper and lower adjacent channels. The allocated spectrum is VHF and L-band.

MediaFLO (Media Forward Link Only) [4] was developed by Qualcomm to effectively address key challenges involved in the wireless delivery of multimedia content to mass consumers. It utilizes OFDM modulation schemes and supports frequency bandwidths of 5/6/7/8 MHz. In a 6 MHz channel, the FLO physical layer can achieve up to 11.2 Mbps at this bandwidth. In USA, the FCC assigned licenses for 698-746 MHz in 6 MHz blocks for advanced mobile services.

China Mobile Multimedia Broadcasting (CMMB) [5] is a mobile TV and multimedia standard developed and specified in China since 2006. The CMMB system is a mixed satellite and terrestrial wireless broadcasting system, which utilizes

two S-band satellites to cover the digital video broadcasting (DVB) over a wide area, while the cellular base stations in the populated metropolitan areas. The service operates in both S-band (2635-2660MHz) and U-band (470-860MHz). The channel bandwidth can be either 2 or 8 MHz, depending on the data rate.

Summarized in Table 1.1, these standards have some common characteristics such as OFDM modulation and frequency allocations among VHF III, UHF, and L-band. The global fragmentation of mobile TV standards will ultimately lead to strong demands for multi-standard mobile TV solutions. It is also a fact that two or more standards begin to coexist within one country.

In general, mobile TV subsystems are divided into two main parts: RF tuner and digital demodulator. The tuner receives the desired TV channel and converts it to the baseband for further signal processing in the demodulator. The demodulated signal is then decoded and displayed on the LCD panel. To achieve high-performance high-quality signal receiving, the tuner is a critical part. This dissertation attempts to address the tuner design for such mobile devices in advanced CMOS technologies. Although this research mainly targets for the DVB-H standard that appears to be the most popular in more countries, many design aspects could be generalized to most other standards.

Table 1.1 Overview of several mobile TV standards

Standard	DVB-T/H	T-DMB	ISDB-T	MediaFLO	CMMB
Area	EU	Korea	Japan	USA	China
RF Spectrum (MHz)	470-862 174-240 1670-1675 1452-1492	- 174-240 - 1452-1492	470-770 90-222 - -	696-746 - 2605-2655 -	470-798 - 2635-2660 -
Channel Bandwidth	5 / 6 / 7 / 8	1.536	0.43-1.29	6	8
Modulation	COFDM 4-64 QAM	COFDM DQPSK	COFDM 4-16 QAM	COFDM 4-16 QAM	COFDM
Data rate (Mbps)	4.98—21.11	1.06—2.3	0.28—1.79 (per seg.)	2.8—11.2	—16.24
Required C/N	~25	~7	~12	~12	~25

1.3 Dissertation Organization

Chapter 2 discusses how to obtain RF specifications from the system specifications. Based on the DVB-T/H standard, RF specifications such as voltage gain, noise figure (NF), input third-order intercept point (IIP3), and phase noise can be calculated from the system standard that specifies sensitivity, selectivity, and linearity test patterns.

Chapter 3 deals with distributing the building block specifications from the derived RF specifications. Based on analytical expressions, spread-sheet tables are constructed to distribute the requirements among the receiver blocks. Link budget analysis and system design verification are also discussed for a complete design procedure.

Chapter 4 presents a single-stage wideband low-noise amplifier (LNA) with a differential output, but a reconfigurable single-ended or differential input. The proposed common-mode rejecting (CMR) buffer significantly improves noise figure (NF) and linearity, making it possible to support a dual-mode operation. The LNA realized in 0.13μm CMOS technology achieves 23dB voltage gain, 0dBm IIP3, and 2.5dB NF in either differential or single-ended receiving mode, while consuming only 3mW.

Chapter 5 presents a fully integrated dual-band DVB-H tuner implemented in 0.13μm CMOS technology. The subsystem design includes the RF front-end, the analog baseband, and the frequency synthesizer. Considerations on RF integration design are also illustrated. With a single-ended input configuration, the tuner achieves a sensitivity level of -96.6dBm and dissipates 114mW from a 1.2 V supply.

Chapter 6 illustrates design considerations as the technology scales from 0.13μm to 65nm. The LNA is used as an example to evaluate the performance at the sub-GHz band in 65nm design compared to 0.13μm case. Two integrated receiver prototypes were realized in 65nm CMOS. The first receiver was implemented to demonstrate even higher levels of noise immunity. The proposed LNA compatible for differential and single-ended inputs was integrated for system-level evaluations. The second receiver was implemented to demonstrate even better sensitivity performance with an asymmetric LNA, achieving an NF less than 3.5dB across the band of interest. The performance verification of the tuner is described in detail.

Chapter 7 concludes this dissertation and discusses the future research directions for mobile TV technologies.

Chapter 2

Receiver Architectures and Specifications

The specifications for the DVB-T/H tuner are contained in the mobile and portable DVB-T/H radio access interface (MBRAI) document [6], [7]. MBRAI details radio specifications in terms of modulation formats, bit error rates (BER), carrier-to-noise (C/N) requirements, sensitivity, and selectivity/ linearity patterns. Although these parameters are commonly seen in wireless standards, it is not straightforward to be used for RF/analog design. In this chapter, we will describe how to translate these system specifications into the RF specifications such as noise figure (NF), third-order intercept point (IP3), second-order intercept point (IP2), and phase noise [8].

2.1 Receiver Architecture

2.1.1 Classical Receiver Architectures

Traditional analog and digital TV tuners have a wide bandwidth from 48 to 864MHz, imposing stringent requirements on the tuner performance characteristics such as harmonics and image rejections [9]. Fig. 2.1(a) and (b) illustrate the problems of harmonics and image mixing. Due to the wide bandwidth spanning several octaves,

unwanted signals located around the harmonics of LO must be supressed to avoid down-conversion into the band of interest, otherwise it would deteriorate signal quality. Similarly, the unwanted image signal which is twice the IF away from the desired channel must be attenuated sufficiently to mitigate SNR degradation.

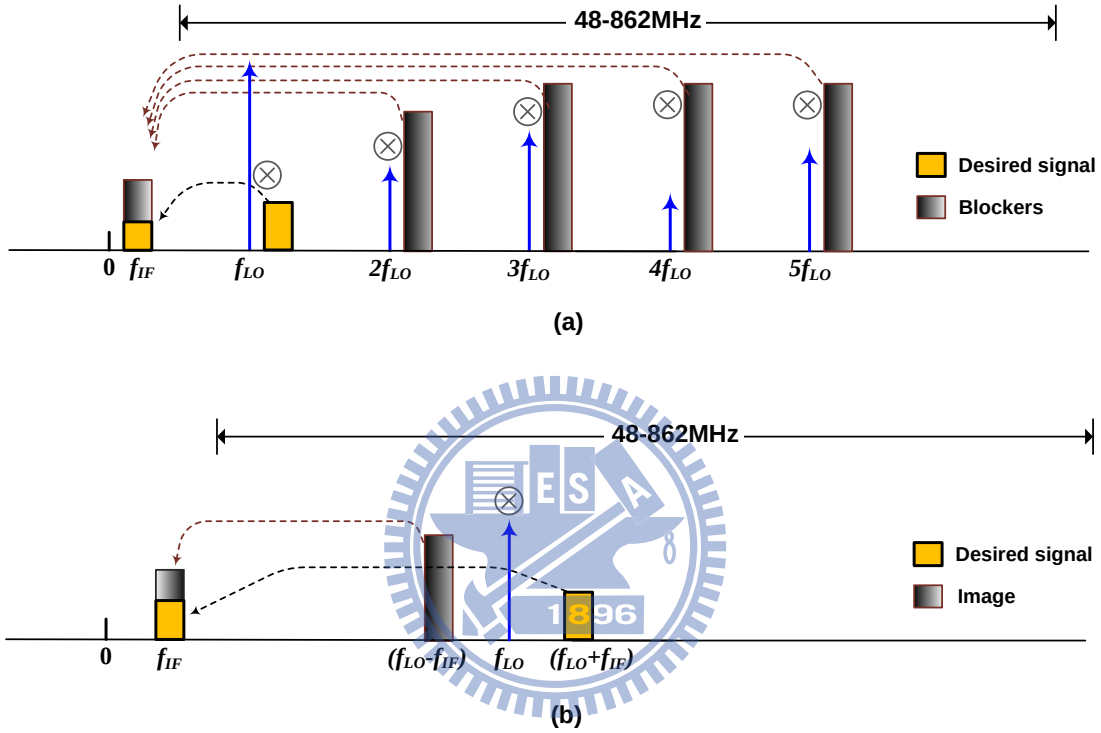


Fig. 2.1 Deterioration mechanisms due to: (a) harmonics and (b) image mixing.

In order to solve these problems, several different techniques have been proposed [10]-[14]. Conventional superheterodyne tuners are classical architectures, shown in Fig. 2.2 (a), which utilizes a bulky tunable tracking filter to filter out the higher band channels as well as the image channel. However, this architecture is not easy to implent monolithically because the RF tracking filter must have a high-Q factor and need external high control voltages to tune its selection frequency.

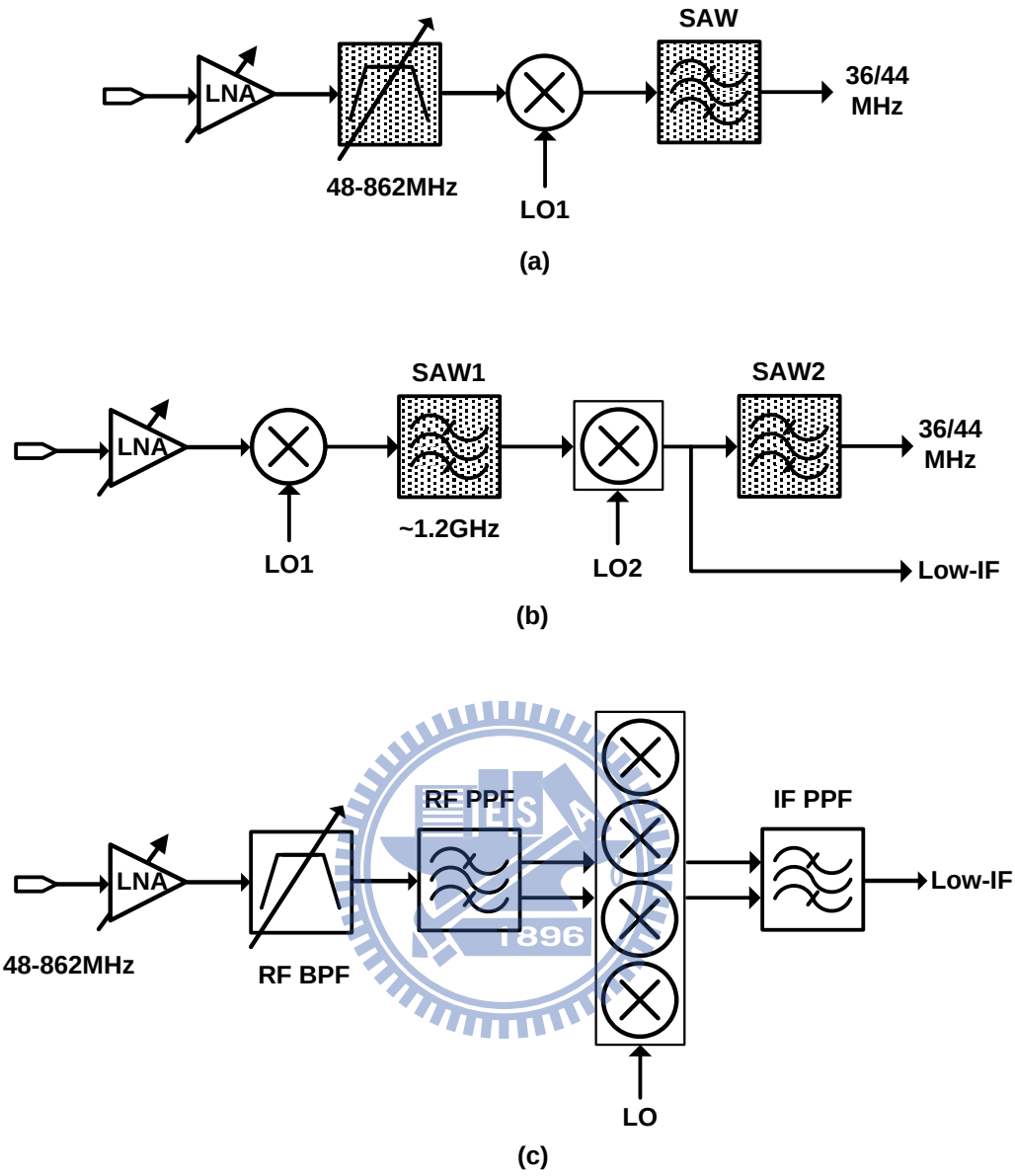


Fig. 2.2 Classical receiver architectures for DVB-T: (a) superheterodyne; (b) up-down dual conversion; (c) single down-conversion low-IF.

To eliminate the tunable high-Q tracking filter, an up/down dual-conversion architecture as shown in Fig. 2.2 (b) was proposed [11], [12]. A higher first intermediate frequency (IF) around 1.2GHz is chose to alleviate the problem of harmonics/image mixing by pulling the harmonics of the LO and image channels out of the TV band. However, an external surface acoustic wave (SAW) filter is still needed to select the desired channel at the fixed first IF. Prior to the second down-conversion to a lower second IF at 36/44MHz for standard TV demodulation,

the first-IF SAW filter msut provide an image rejection of 30-40dB. To achieve a required image rejection up to 60dB totally in system considerations, therefore, the remaining 30dB of image rejection can be done by using an image rejection mixer (IRM) in the second down-conversion. The drawback of this architecture is the need for an external SAW filter, which limits the level of integration and raises the power dissipation.

Compared with the dual-conversion architectures, [13], [14] employs a single down-conversion low-IF architecture to increase the level of integration, shown in Fig. 2-2 (c). This topology relaxes the requirements of RF filters. Unwanted signals at and above 5 times the wanted signal frequency should be supressed; as a result, RF filters can be integrated on chip. In addition, a double quadrature mixer [15] is implemented to obtain an image suppression better than 60dB at the cost of higher system complexity.

2.1.2 Direct-Conversion Receiver Architectures

As mentioned earlier, classical TV tuners consume much power of 0.5-1W to overcome the technical bottlenecks and generally need external tracking and SAW filters which are expensive and bulky for channel selection as well as image rejection. Obviously, such solutions are not appropriate in mobile TV applications. In the battery-powered handheld devices, the constraints of low power consumption and small form factor demand a simplified tuner architecture that differ from classical architectures.

Since only a part of classical TV broadcast band (48-864MHz) has been allocated to mobile TV spectrum, the problem of hamonics and image mixings is much relaxed. More specifically, most mobile TV standards target on the use of VHF III (174-230MHz), UHF- (470-862MHz), and L-bands (1452-1492MHz and 1670-1675MHz). For battery-powered handheld devices, thus, a direct conversion receiver (DCR) architecture seems to be a promising architecture in realizing a low cost, small form factor, low power consumption highly integrated DVB-T/H receiver..

As shown in Fig. 2.3, two configurations can be selected to implement the tuner architecture. In [16]–[18], state-of-the-art solutions generally utilize dedicated LNA or front-end circuits for each band as shown in Fig. 2.3 (a), where seperate LNAs is

shown as the example. Such solutions eliminate the need for an external switch and facilitates the connections to seperate RF band-selection filters. Most of all, seperate RF circuits can be optimized for each band with reduced power consumption.

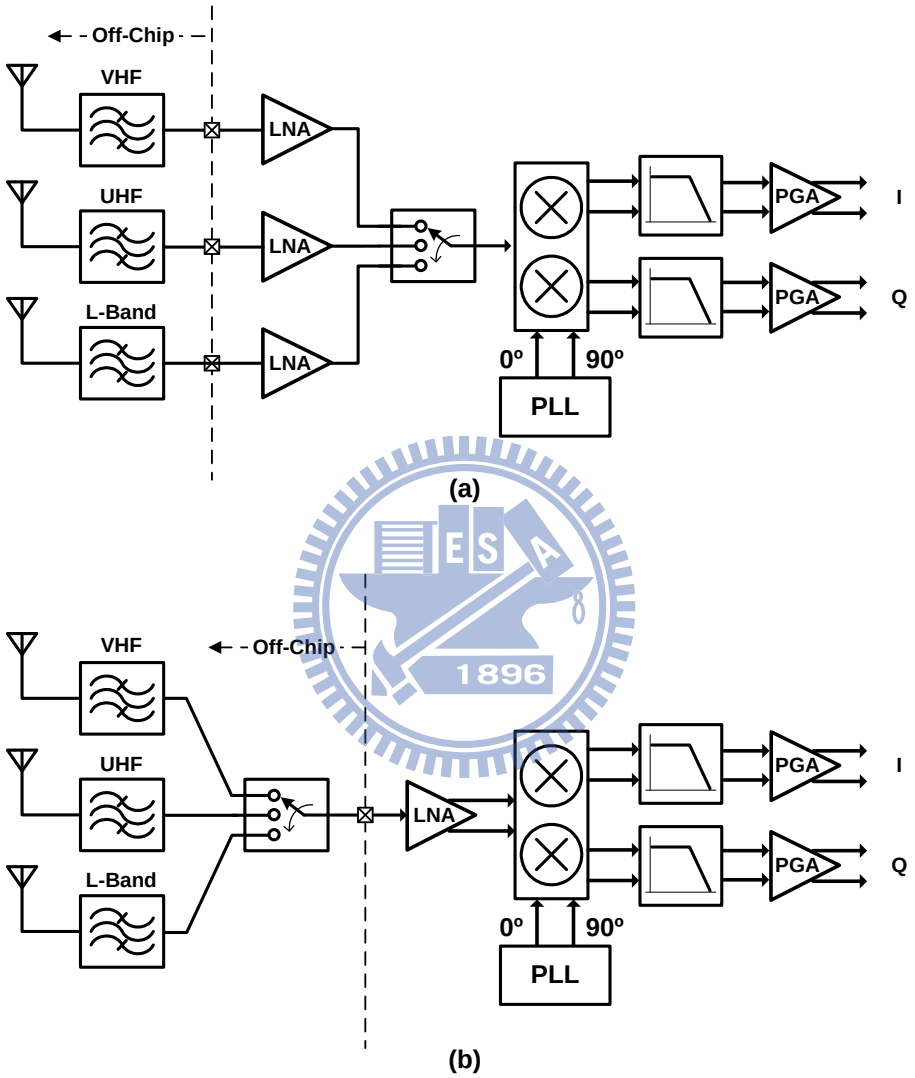


Fig. 2.3 Block diagram of dierect conversion receiver with: (a) dedicated LNAs for each band, and (b) a broadband LNA.

Another technique is utilizing wideband techniques to cover multi-band operations as shown in Fig. 2.3 (b). This architecture requires a wideband front-end to support full band of mobile-TV services from 170 to 1700 MHz [19]. Wideband

reception can minimize the hardware requirement on front-ends, but an external RF switch is needed to enable band selection in conjunction with seperate RF filters and antennas. Requirements on such external components typically limit the use of this architecture in manufactures, especially the need for external wideband balun if differential LNAs are adopted.

2.2 RF Specifications

Fig. 2.4 depicts the block partition of a DVB-T/H system. The defined requirements are referred to the RF reference point at the input of the tuner. All the RF specifications in this thesis are derived based on an 8MHz channel bandwidth for the portable or hand-held convergence terminals (terminal category b2 or c), unless otherwise stated.

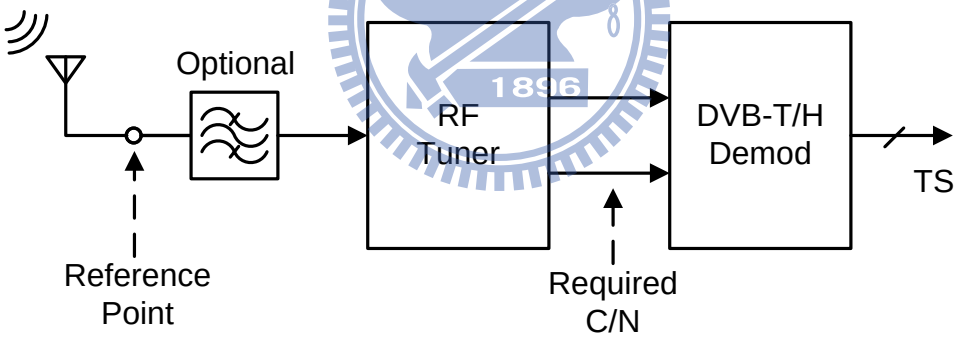


Fig. 2.4 Block diagram of a DVB-T/H system.

2.2.1 Frequencies and Channel Bandwidths

The European Telecommunications Standards Institute (ETSI) initially allocates the frequency bands covering UHF IV and V for the terminal category b2 or c. The receiver should be able to support 6/7/8MHz channel bandwidths, depending on the region. Table 2.1 illustrates the centre frequencies for various channel bandwidths, in which flexible offset frequencies of $\pm n \times 1/6$ MHz and $n \in \{1, 2, ...\}$ should be

guaranteed. The frequency range is 470-862MHz for category b2, while limited to 754MHz in a TV-GSM co-integrated terminal (category c).

Since GSM uplink at 880MHz is close to the TV spectrum, a GSM rejection filter is needed at the receiver input to avoid nonlinear distortions and reciprocal mixing issues due to strong GSM interferers. Together with the coupling losses between antennas (~10dB) [20], the filter must provide high attenuation (~50dB) to suppress the GSM transmitted power from +33dBm to -28dBm, which is the maximum allowed signal level at the receiver input for DVB-H. Under the case with a GSM rejection filter, the overall noise figure can be up to 6 dB [6].

Table 2.1 Channel bandwidth and centre frequencies in MBRAI

Channel BW [MHz]	System Noise BW [MHz]	Channel Centre Frequencies [MHz]
8	7.61	$474+(N-21)\times 8+f_{offset},\ N=\{21,\ldots,69\}$
7	6.65	$474+(N-21)\times 8+f_{offset},\ N=\{14,\ldots,83\}$
6	5.71	$473+(N-14)\times 6+f_{offset},\ N=\{14,\ldots,83\}$

2.2.2 C/N Requirement

In *MBRAI*, the *C/N* performance is calculated based on the noise model as illustrated in Fig. 2.5. Assume that the incoming signal is amplified and down-converted by a front-end stage which has an overall noise factor F_{RX} and perfect automatic gain control (AGC). The relative excess noise P_x denotes several impairments such as phase noise, quantization noise, etc. For giving the reference *BER* (2×10^{-4}), the carrier-to-noise ratio (*C/N* ratio) at the demodulator input can be derived for a particular modulation scheme. The main *C/N* requirements for different modulation schemes are listed in Table 2.2.

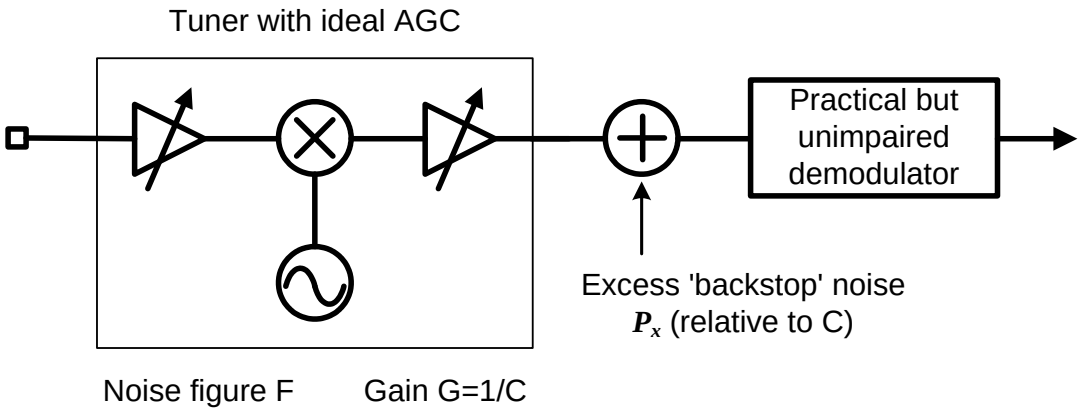


Fig. 2.5 Noise model for calculating C/N performance.

Table 2.2 C/N requirements versus modulation schemes

Modulation Scheme	C/N Requirement in Gaussian Channel	C/N Requirement in Portable outdoor channel
QPSK 1/2 code rate	4.6	10.5
16-QAM 2/3 code rate	12.7	19.5
64-QAM 3/4 code rate	19.9	27.5

2.2.3 Minimum Input Levels

The receiver sensitivity, defined as the minimum signal input level that a receiver can detect and maintain a target *BER*, is given by

$$S_{\min}(dBm) = 10 \cdot \log_{10}(kT) + 10 \cdot \log_{10}(BW) + NF_{RX} + \frac{C}{N} \qquad (2.1)$$

where k=1.38×10^{-23} J/°K is Boltzmann constant, T=290 ° K is ambient temperature, BW is signal bandwidth, NF_{RX} is overall receiver noise figure, and C/N is the minimum required signal-to-noise ratio. Since *MBRAI* 2.0 requires a NF below 4dB at the sensitivity level, the sensitivity target for 8MHz channel bandwidth shall be lower than -96.6dBm for *QPSK 1/2* modulation scheme, where 7.61 MHz of effective bandwidth and 4.6dB of SNR requirement are specified.

2.2.4 Dynamic Gain Range

In the absence of any interference, the maximum desired signal level at the tuner input is specified to be -28dBm. Since the minimum sensitivity level is -96.6dBm, the tuner has to provide at least 68.6dB gain range. Assume that the maximum rail-to-rail voltage swing at the tuner output from a supply of 1.2V is $2V_{p-p}$ differentially, i.e., 10dBm referred to 50Ω resistance. As a peak-to-average power ratio (PAPR) of 15dB is taken into account, a reasonable power level at the tuner output would be maintained at -5dBm for all input power levels and gain settings. As a result, the tuner should provide a gain range from 22.6 to 91.6dB at least.

2.2.5 Interference Test Patterns

The wide frequency spectrum of DVB-T/H causes the issue that the desired signal usually comes with multiple in-band interferers. This issue becomes important when the desired signal is weak and adjacent-channel interferers are strong at the receiver input. Several types of interference tests are specified in the *MBRAI* document to characterize reception conditions in the presence of other interfering TV channels. They can be divided into two categories: 1) receiver selectivity testing with a single analog or digital interferer, and 2) receiver linearity testing with two analog and/or digital TV interferers. Table 2.3 and Table 2.4 respectively illustrate these test patterns, where D represents desired channel signal power and U is unwanted interferer signal power.

Table 2.3 Selectivity test patterns

Selectivity Pattern	Modulation of interferer	Interferer location	U/D Ratio [dBc]	U [dBm]
S1	analog	N±1	38	-35
		N±*k* (*k*>1)	48	-28
S2	digital	N±1	29	-35
		N±*k* (*k*>1)	40	-28

Table 2.4 Linearity test patterns

Linearity Pattern	Modulation of interferer	Interferer location	U/D Ratio [dBc]	U [dBm]
L1	Digital and analog	N+2 (digital)	40	-35
		N+4 (analog)	45	
L2	analog	N+2, N+4	45	-35
L3	digital	N+2, N+4	40	-35

The selectivity patterns measure a receiver's ability to receive a desired signal in the presence of an unwanted interferer at an adjacent/alternate channel close to or away from the desired channel. In general, this test item is mainly concerned with three performance parameters: 1) the attenuation ratio of the channel selection filter to the adjacent/alternate interferers, 2) the phase noise and spurs of the synthesized LOs.

The linearity patterns are mainly utilized to evaluate the corruption of the desired signal due to the third-order intermodulation (IM_3) of two nearby interferers. If a weak desired signal along with two strong interferers enter a nonlinear circuit and experience the third-order nonlinearity in that circuit, then one of the IM_3 might fall in the band of interest and corrupts the desired signal. Third-order distortion is specified in terms of an input referred third-order intercept point IIP3.

2.2.6 Phase Noise and LO Spurs

Ideally the synthesizer's output spectrum should be a Dirac impulse at the desired frequency. But practical signal sources usually have sidelobes in the frequency spectrum due to the disturbance of several kinds of noise sources. To this nonideal effect, there are two main mechanisms that create distortion and noise components on the desired channel.

First, the close-in phase noise of the LO causes the loss of orthogonality on the subcarriers due to the inter-subcarrier interference [21]. This mechanism degrades the modulation accuracy of desired signal, i.e., EVM, and is reflected in the requirement of integrated phase noise within the signal bandwidth or maximum tolerable rms

phase error. To minimize this influence, *MBRAI* specifies the excess noise to be 33 dB lower than the LO signal level. In fact, 37dB at least should be guaranteed to allow for the presence of other impairments such as quadrature mismatch.

Second, the reciprocal mixing of the LO phase noise with the adjacent/alternate channel interferers may also result in in-band interference [22]. This mechanism is depicted in Fig. 2.6. In order not to deteriorate the signal quality much, the phase noise requirements at different offset frequencies from carrier can be determined by

$$L(\Delta f) = -\left(\frac{U}{D}\right) - \left(\frac{C}{N}\right) - 10\log(BW) - 10\log(\%) \tag{2.2}$$

where U/D represents unwanted/desired power ratio in test scenario, C/N is the minimum required signal-to-noise ratio, *BW* is signal bandwidth, and the last term (%) denotes the contribution ratio to the overall impairments.

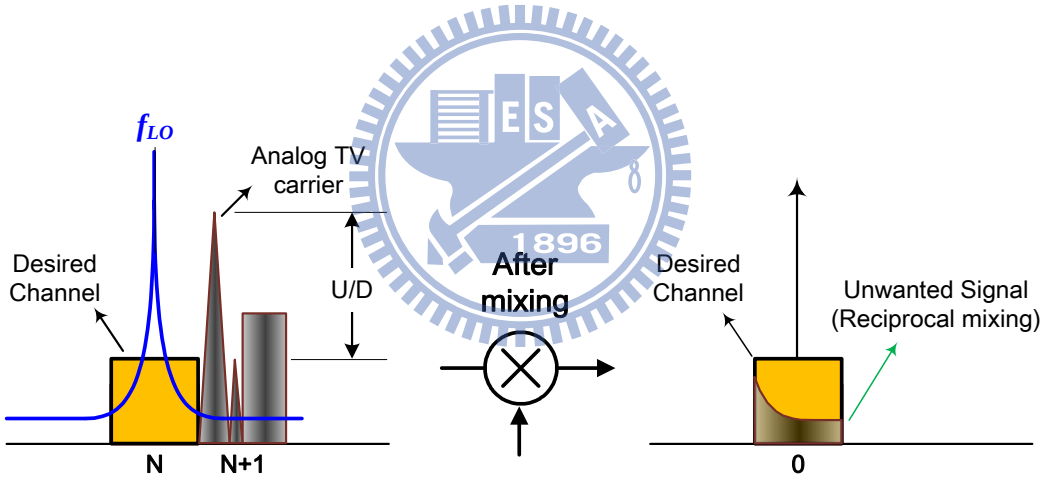


Fig. 2.6 Impact of phase noise on reciprocal mixing.

According to S1 pattern in MBRAI2.0, analog TV (PAL/SECAM) interference at N+1 adjacent channel is up to 35 dB stronger than the wanted 64-QAM signal. From PAL signal definitions, its signal power is concentrated at the picture carrier, which is 1.25 MHz away from the boundary as shown in Fig. 2.6. This implies that the picture carrier is only 5.25 MHz away from the center of the wanted channel. For this demodulation, the minimum required SNR is 20dB and the signal bandwidth is 7.61MHz. Thus, the integrated phase noise from 1.45 to 9.05 MHz offset from the LO

can be calculated.

$$\int_{LO+1.45MHz}^{LO+9.05MHz} L(\Delta f) < -\left(\frac{U}{D}\right) - \left(\frac{C}{N}\right) - 10\log(\%) \tag{2.3}$$

$$\int_{LO+1.45MHz}^{LO+9.05MHz} L(\Delta f) < -35 - 20 - 5 = -60dBc \tag{2.4}$$

The calculation shows that integrated phase noise from 1.45 to 9.05MHz offset should be less than –60dBc with a 5dB margin. Assume a rectangular phase-noise distribution within the channel. This translates to a phase-noise requirement of -129dBc/Hz at 1.45MHz away from the center. Actually, this assumption overestimates the requirement at 1.45MHz, which ensures that the phase noise profile can meet all the requirements with sufficient margins.

With respect to the (N+2) adjacent interferer, two channels away from the desired signal in S1 pattern, analog TV interference may be 43dB higher than the wanted 64-QAM signal. This requires that the integrated phase noise from 9.45 to 17.05 MHz offset from the LO should be less than –68dBc. Similarly, this translates to a phase-noise requirement of -137dBc/Hz at 9.45MHz offset from the LO.

The influence of frequency spurs acts very similarly to phase noise. They reciprocal-mix the adjacent/alternate channel interferers down into signal bands and contribute distinct terms in integrated phase noise. To evaluate this impact, the integrated phase noise across the frequencies of interest should include the power of LO spurs within this bandwidth.

2.2.7 Filter Response

Another IC specification relative to the selectivity patterns is concerned with the rejection ratio of the channel selection filter to the adjacent/alternate interferers. Since the received signal contains not only the desired channel but some neighboring interference channels, baseband filters are needed to separate the desired channel from unwanted interference channels. In general, the filtering can be done either in the analog or digital domain. Theoretically it is preferable to realize as much filtering as possible in the digital domain because digital filters has high accuracy against process,

voltage, temperature (PVT) variations and do not require tuning circuitry. However, pushing more filtering into the digital domain increases the required dynamic range and resolution in the ADC. Unfortunately, this significantly increases power consumption since the power of Nyquist rate ADC is proportional 2^N where N is number of bits [23]. From a power dissipation and area perspective, as a result, some combination of analog and digital filtering will be an optimal choice.

There is a tradeoff among the filter's out-of-band attenuation, the maximum VGA gain and the dynamic range of the ADC. The residual adjacent channel power after the analog channel-select filter increases the required dynamic range in the ADC. In order not to saturate the ADC, the maximum signal magnitude at the receiver output should not exceed the allowable full swing of the ADC. Fig. 2.7 shows the SNR and SNDR requirement of the ADC, which is constrained mainly by the required adjacent channel immunity.

$$SNR = (U/D) + (C/N) + \text{PAPR} - \text{ATT} + \text{Margin} \quad (\text{in dB}) \tag{2.5}$$

where U/D represents the unwanted-to-desired signal ratio, C/N is the minimum required carrier-to-noise ratio for a specific modulation scheme; PAPR is the peak-to-average power ratio of the unwanted OFDM signal; ATT represents the out-of-band attenuation of the filter.

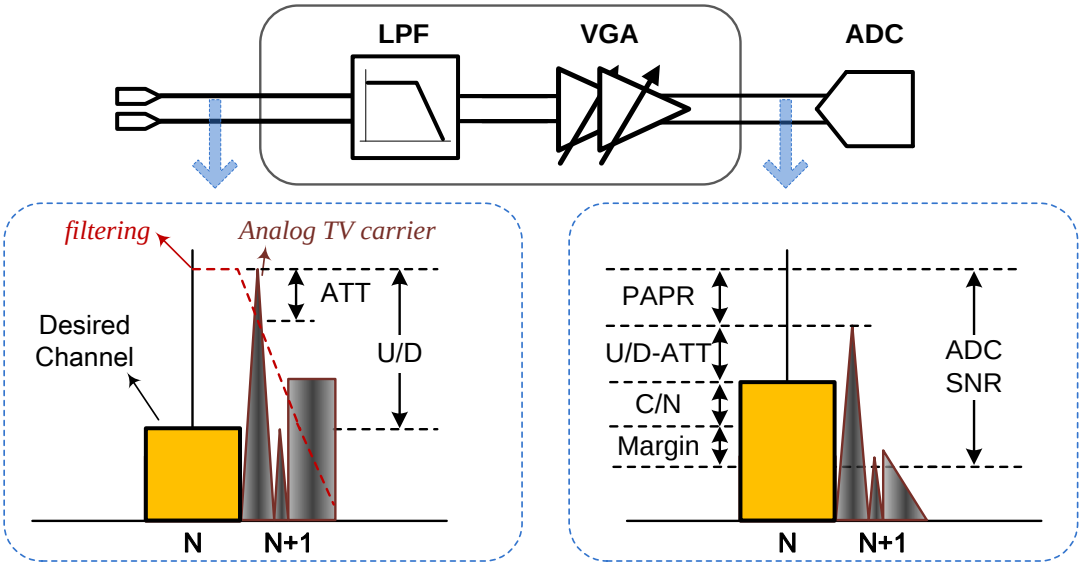


Fig. 2.7 Design trade-offs between the ABB filtering and ADC SNR.

According to S2 pattern in *MBRAI 2.0*, digital TV (DVB-T) interference at N+1 adjacent channel is up to 29 dB stronger than the wanted 64-QAM signal. To maintain a minimum 20dB C/N requirement, 15 dB PAPR, 14dB margin, the SNR requirement of the ADC is calculated as (79-ATT) in dB. In order to conform to most of commercial demodulator ICs which own different ADC specifications, the target SNDR of the ADC is expected to be as low as 48dB (~8bits). This implies that the analog filter must provide at least 30dB of attenuation at 5.25MHz offset from the center frequency. Here, 5.25MHz refers to the carrier frequency of analog TV interference at the adjacent channel (N+1).

2.2.8 IIP2 requirement

In a direct conversion receiver, two nearby interferers can directly mix with each other and produce the IM2 component ($f_1 - f_2$). It is important to note that digital interferers can create broadband baseband interference due to the interactions among sub-carriers of the OFDM blocker in frequency domain. The interfering product would fall in the band of interest and degrade the performance of the receiver as shown in Fig. 2.8. In order to maintain the minimum SNR requirement, such a product must be suppressed, which could be approximated by an IM2 analysis using two-tone power series expansions. Calculation of the in-band interference can be expressed as

$$P_{IMD2} = 2 \cdot (P_{N+m} - 3) - IIP2 < P_{sig} - \left(\frac{C}{N}\right) - 10\log(\%) \qquad (2.6)$$

where P_{N+m} represents the total power of the digital interferers which is m channels away from the desired channel. Since the interferer is approximated by two tones with the same power, half the total power each, i.e., 3dB lower, should be considered for calculations. Moreover, total noise and interference power P_{N+I} should be distributed (%) since several different interfering products, such as IM3, phase noise, etc., are created simultaneously.

Thus, the minimum IIP2 is given by

$$IIP2 > 2P_{N+m} - P_{sig} + \left(\frac{C}{N}\right) + 10\log(\%) - 6 \tag{2.7}$$

Since the standard defines the digital TV interference 2 channels away at –28 dBm and the wanted 64-QAM signal at –68 dBm, assuming 10% noise power contribution and 20 dB SNR_{min}, it can be easily found that the required IIP2 at the input is higher than +36 dBm under the S2 pattern test.

Normally the IIP2 of a receiver is dominated by the mixer due to the high gain of the LNA and AC coupling between LNA output and mixer output. Thus, much attention on the input transconductance stage of the mixer for a symmetric design and layout should be paid to ensure a high IIP2.

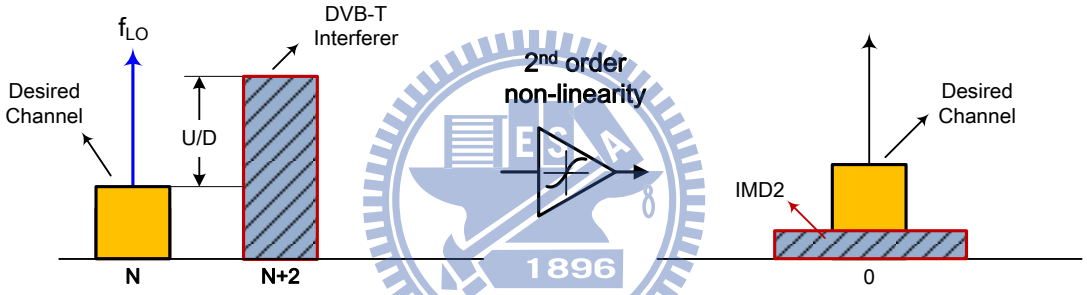


Fig. 2.8 Impact of second-order intermodulation distortion.

2.2.9 IIP3 requirement

As shown in Fig. 2.9, two unwanted interferers may create intermodulation products which fall in the desired channel due to the third-order nonlinearity of the receiver. To achieve enough SNR, the IM3 product should be limited, which can be approximated corresponding to the traditional formula based on two-tone analysis [8]. The required input referred IM3 product is derived as

$$P_{IMD3} = 2P_{N+2} + P_{N+4} - 2IIP3 < P_{sig} - \left(\frac{C}{N}\right) - 10\log(\%) \tag{2.8}$$

where P_{N+2} and P_{N+4} respectively represents interferer signal power at N+2 and N+4

channel.

According to L3 test pattern, two digital TV interferers located at two and four channels away from the deisred channel will produce an IM3 product which falls into the desired channel. Since the power level of both two interferers is -35dBm with a requirement of unwanted-to-desired power ratio (U/D) higher than 40dB, the maximum allowable noise plus interference power level must be –87.7dBm to ensure a minimum SNR of 12.7dB for 16-QAM 2/3 modulation. Assume that the IMD3 interference contributes 50% of the total noise plus interference power, i.e., –87.7dBm–3dB =–90.7dBm. Hence, the IIP3 must be better than –7.15dBm

$$IIP3 > P_{N+2} + \frac{1}{2}\left(\frac{U}{D} + \frac{C}{N} + 10\log(\%)\right) \tag{2.9}$$

$$IIP3 > -35 + \frac{1}{2}(40 + 12.7 + 3) \tag{2.10}$$

Along with an IIP3 requirement of -7dBm, an NF less than 9.5dB is required to meet L1 and L2 tests simultaneously.

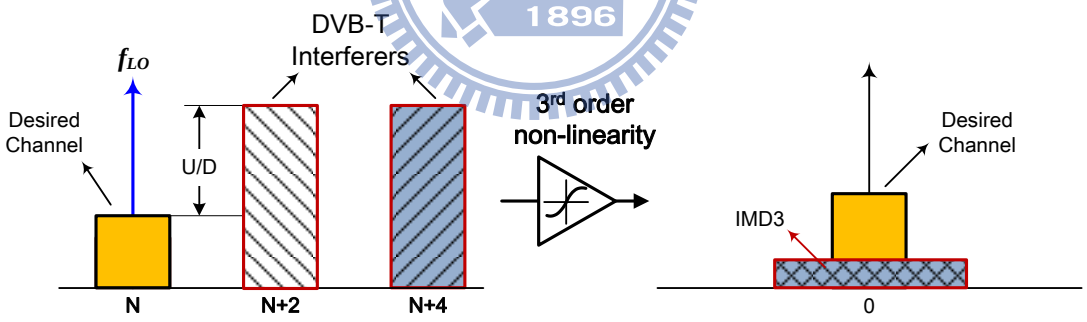


Fig. 2.9 Impact of third-order intermodulation distortion.

2.2.10 Image Rejection

In a direct-conversion receiver, the LO frequency is equal to the center frequency of the desired channel. Since the desired signal spectrum is spanned on both sides of the LO, the image of the desired channel is the desired channel itself. In order to maximize spectral efficiency, OFDM techniques are quickly becoming a popular

method for advanced communications networks, including DVB-H. Since OFDM signals have asymmetrical spectrum, i.e., the upper sideband are uncorrelated to its lower sideband, the problem of image mixing should be concerned. In general, the quadrature down-conversion can be utilized to achieve a basic requirement on image rejection. As shown in Fig. 2.10, the overall quadrature imbalance can be referred to the LO path and modeled as a leakage component in the negative LO frequency. Similar to the low-IF architecture, the $-f_{LO}$ mixes with the positive component of the desired signal and generates unwanted image component, which distorts the OFDM constellation. In general, the requirement of image rejection depends on the specific modulation scheme. According to *MBRAI 2.0*, the most stringent requirement on image rejection refers to the use of 64-QAM. To maintain a reasonable EVM, an image rejection of better than -37dBc would be desirable, referring to an amplitude mismatch of 1.5% and phase error of 1.5 degree [24].

Note that the constant I/Q mismatch errors may be corrected by DSP in the demodulator [25], but frequency-dependent errors have to be minimised by careful circuit design and layout.

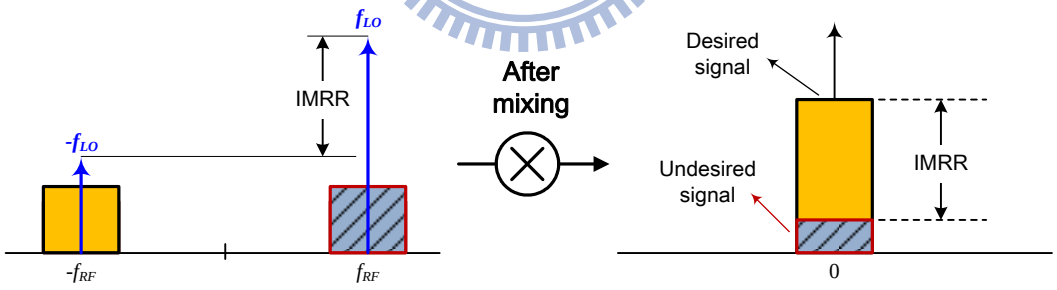
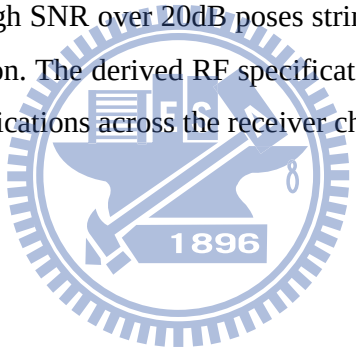


Fig. 2.10 Impact of quadrature imbalance in a direct-conversion receiver.

2.3 Conclusion

In this chapter, the RF specifications for DVB-T/H tuners have been calculated, which are based on MBRAI system specifications. The RF specifications consist of noise figure, voltage gain, phase noise, filtering, IIP2, IIP3, and image rejection specifications. As mentioned earlier, they are calculated based on the system specifications which are expressed as test scenarios for which the receiver system should pass with a specific minimum performance. This chapter gives an overview of the most important test patterns and where possible these test patterns are translated to receiver RF specifications. The overall NF is directly related to the sensitivity requirement of a receiver. The channel filtering characteristics, the LO phase noise and IIP2 are determined by selectivity test patterns. The linearity requirement of IIP3 is mainly dominated by linearity test patterns. Duo to the use of 64-QAM modulation scheme, the requirement of high SNR over 20dB poses stringent requirements on close-in phase noise and image rejection. The derived RF specifications will be further distributed into the building blocks specifications across the receiver chain in the next chapter.



Chapter 3

Receiver System Analysis and Design

In the previous chapter, we have translated the DVB-T/H radio standard, MBRAI2.0, into receiver system specifications. In this chapter, we will discuss the receiver system design and verification by distributing the system specifications into individual building blocks specifications. One major task of the receiver system design is to properly select building block topologies and to define their specifications. To achieve this, we must be familiar with the basic specifications of various building blocks as well as their possible performance based on the present technology. Once building block specifications have been defined, system performance should be verified by cascading the receiver blocks and evaluating the cascaded SNR. It is noted that all impairments should be taken into account to evaluate the SNR degradation as real as possible. Typically, the receiver system design is a rather iterative procedure.

3.1 Distributing Building Block Specifications

This section details the building block specifications, derived from analytical expressions spread-sheet tables. Design requirements and considerations on each circuit block are also described. Recommended specifications on each block are illustrated as the basis for the selection of building block topologies and to evaluate the feasibility in the early stage of the receiver design.

3.1.1 RF Font-end

RF front-end composed of LNA and mixer is the most critical block in the receiver chain. Its performance typically dominates the overall NF and linearity of the system. To achieve an overall NF below 4dB in the sensitivity level, the LNA gain is expected as high as possible. However, this trades off with the overall linearity which is typically dominated by the mixer input stage. To alleviate linearity contraints and to reduce *intermodulation distortions (IMD)*, programmable gain switching should be implemented in the front-end of the receiver. As the desired signal has a power level much higher than the sensitivity level, a lower gain can be set in the front-end to avoid saturation and generation of interfering IMDs in the receiver chain.

In the case of our particular receiver, a received signal strength indicator (RSSI) circuit is utilized to sense the input signal power which includes all the desired and unwanted signals within the band of interest. When the total received power is in excess of a certain threshold, the RF AGC loop will back off the RF gain to avoid SNR degradation due to nonlinearity distortions. It is noted that the received power may be significantly dominated by strong interferers in conjuction with a weak desired signal. Thus, it is important to define the NF specifications at different input conditions. To conform to all reception conditions, the RF gain back-off and its corresponding NF and IIP3 is illustrated in Fig. 3.1 and also listed in Table 3.1. The front-end block provides ten steps of gain back-off with a gain range from 0 to 36dB. In the sensitivity level, the RF front-end provides a maximum gain of 36dB, an NF of 3.5dB, and an IIP3 of -13dBm. As the signal power reaches -40dBm, the front-end starts to back-off its gain setting in 2dB/step until -29dBm. Then, a low-gain (LG) mode is dedicated to support the range from -28dBm to -21dBm. After that, an extra low-gain (ELG) mode is allocated to the range from -20dBm to -15dBm. As the signal power is larger than -14dBm, the RF front-end is switched to the minimum gain (MIN) mode.

In addition to the gain, NF and IIP3, other performance such as input return loss and IMRR should be highly concerned in the front-end design. Detailed specifications of the RF front-end is given in Table 3.2.

Table 3.1 RF front-end gain distribution and their corresponding NF/IIP3

Pin (dBm)											
	Max	-98	-40	-38	-36	-34	-32	-30	-28	-20	-14
	Min	-41	-39	-37	-35	-33	-31	-29	-21	-15	0
Gain Mode		Max	-	-	-	Mid	-	-	LG	ELG	Min
Gain Back-off (dB)		0	2	4	6	8	10	12	15	20	36
Voltage Gain (dB)		36	34	32	30	28	26	24	21	16	0
NF (dB)		3.5	4.3	4.8	5.5	6.5	7.5	9	10	14	36
IIP3 (dBm)		-13	-11	-10	-8	-6	-4	-2	+5	+6	+10

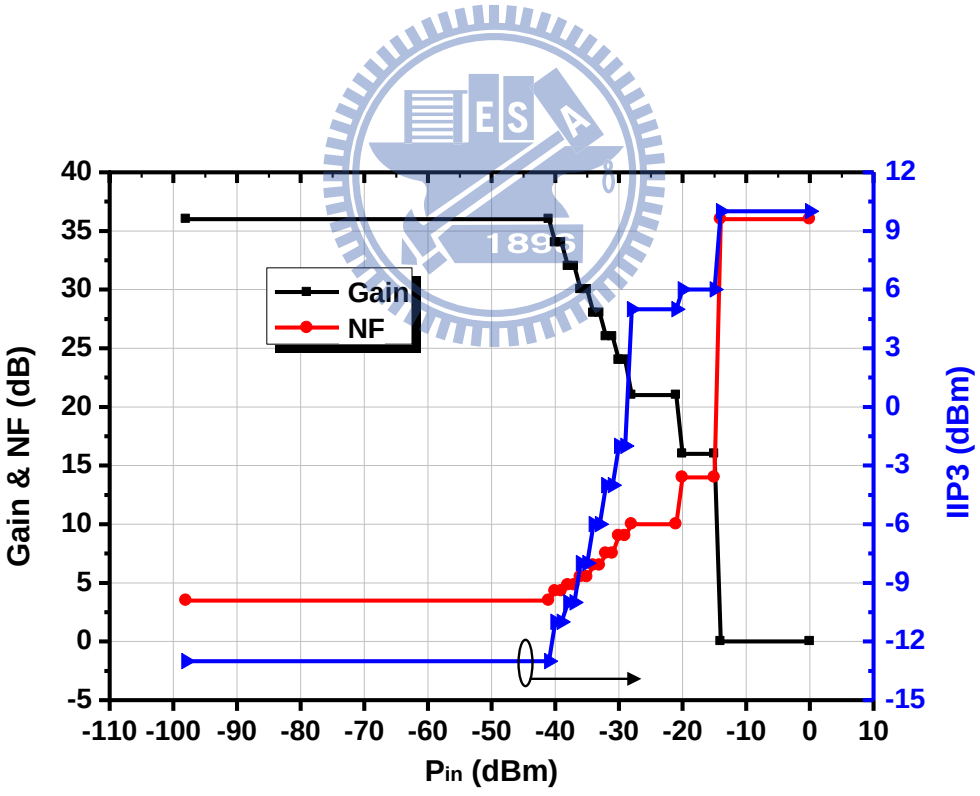
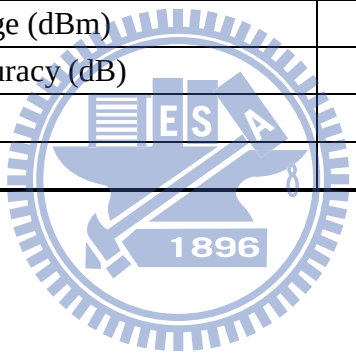


Fig. 3.1 RF front-end gain settings versus input power levels.

Table 3.2 Recommended RF front-end specifications

Vdd (V)		1.2
Input Return Loss (dB)		-10
Gain Range (dB)		36－0
Max Gain	NF (dB)	3.5
	IIP3 (dBm) @N+2, N+4	-13
	IIP2 (dBm) @N+2	+30
Low Gain	NF (dB)	10
	IIP3 (dBm) @N+2, N+4	+5
	IIP2 (dBm) @N+2	+50
Gain mismatch (dB)		0.1
Phase imbalance (°)		1.3
IMRR (dB)		-37
RSSI	Range (dBm)	-40－-10
	Accuracy (dB)	±2
DC offset (mV)		<5
Output DC (V)		0.6



3.1.2 Analog Baseband

The analog baseband performs three kinds of analog signal processing functions: 1) low-pass filtering (LPF); 2) programmable-gain amplification (PGA), and 3) DC offset cancellation (DCOC).

3.1.2.1 PGA

In order to achieve the overall dynamic range specifications, two AGC loops controlled by the digital demodulator are utilized in the RF and analog baseband, respectively. The analog baseband provides programmable-gain ability to keep almost constant signal level at the ADC input. As derived in Ch 2.2.4, the overall receiver gain of 92－23dB is required. Since the RF front-end provides a gain range of 36－0dB, the analog baseband should achieve a gain range of 56－23dB at least. To ensure

a reliable operation with a maximum SNR, however, a wider gain range from 60 to -6dB would be preferred. The extended gain range towards 0dB retains a potential to switch RF gain back-off later, alleviating a sudden SNR degradation when RF gain is changed from 15dB to 0dB. In addition, an accuracy of 0.5dB steps is specified to minimize the SNR degradation from gain changes during data reception under fading conditions [26].

3.1.2.2 Filter

To implement an analog filter for channel selection filtering, there are three important parameters that should be determined first: 1) filter prototype function; 2) 3-dB corner frequency; and 3) filter order. From DVB-T/H standard, the analog baseband must deal with 5/6/7/8 MHz channel bandwidth, i.e., 2.5/3/3.5/4 MHz cut-off frequency low-pass filtering. In addition, the selectivity pattern requires an attenuation of 30dB at 1.25MHz offset as derived in Ch 2.2.7. As a result, in this design a seventh order Chebyshev I filter is selected in a leap-frog configuration. This filter topology results in the sharpest stop-band attenuation, but contains the largest group delay. In order to compensate the group delay of the overall system, a first order all-pass filter is utilized in the analog baseband. Since the analog filter is sensitive to the process, voltage, and temperature variations, an auto-calibration circuit is needed to guarantee cut-off frequency accuracy within ±3%.

3.1.2.3 DCOC

Since direct conversion receivers down-convert the desired channel to the zero frequency, offset voltages at DC can corrupt the signal and saturate the following stages after the mixer [23]. As a result, in the analog baseband one important task to deal with is to eliminate or minimize the DC offset.

In genreal, there are two mechanisms to generate the offset voltages. The first one involves the finite matching performance of the devices in the mixer and the following stages. The mismatches of transistors and passive components will result in DC offset, which is almost constant. In order to minimize this source of DC offset, increasing the matching performance by using larger transistor size and symmetric

layout would be helpful.

The second one involves the finite isolation between the LO and RF port of the mixer, which causes the self-mixing effect to create the DC offset as shown in Fig. 3.2 (a) and (b). The leakage of LO signal to the input of the mixers may mix with itself to generate a constant DC offset. On the other hand, the strong interferers from the input may also leak to the LO port, but this self-mixing effect will generate a time-varying DC offset. In order to minimize this source of DC offset, improving the port isolation is helpful, which can be achieved by incorporating some shielding techniques and reducing the undesired coupling in circuit layout.

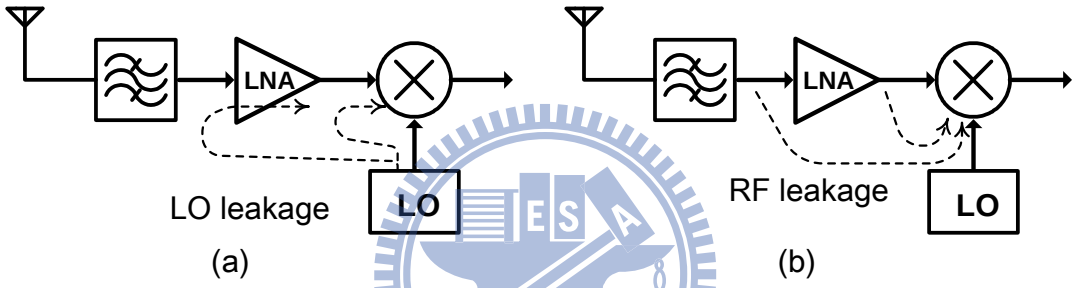


Fig. 3.2 LO/RF leakage and generation of DC offsets.

In addition to minimizing the sources of DC offset, an offset canceling technique is required to remove the DC offset. In general, high-pass filtering by means of AC blocking capacitors is the simplest method to remove the DC components. In order not to destroy the signal around DC, however, the cutoff frequency of the high-pass filter must be very low. This means that the required blocking capacitors will be very large and diffcult to implement on chip. On the contrary, DC servo loop is a good candidate for the purpose of high integration. As shown in Fig. 3.3, a low-pass filtering circuit which is placed between the input and output of the baseband amplifier can feedback the output DC components to the input. By subtracting these components from the input signal, a high-pass filtering can be realized. Compared with the method using the blocking capacitors, the required capacitors used in the DC servo loop is much reduced at the cost of extra power consumption. In this work, the DC servo loop has a cutoff frequency less than 1 kHz to ensure sub-carriers around DC

are not affected too much.

Detailed analog baseband specification is given in Table 3.3.

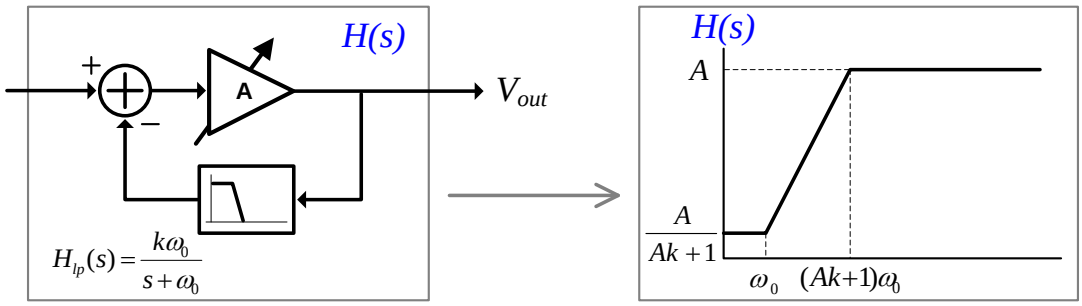


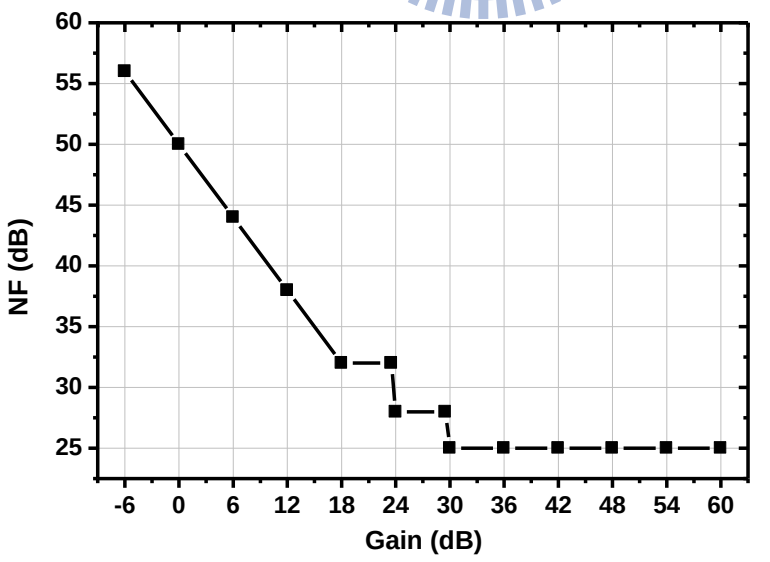
Fig. 3.3 Servo loop for DC offset cancellations.

3.1.2.4 Noise/Linearity Trade-off

One of the main issues to address when designing the analog baseband is how to arrange the distribution of filtering attenuations and amplifications. If the amplifications are performed prior to the attenuations, the analog baseband can achieve the best noise performance but have the most stringent linearity requirement. If the attenuations are performed prior to the amplifications, on the contrary, the linearity requirement is much relaxed at the expense of poor noise performance. To comprise the noise and linearity trade-off, the amplification and filtering procedures are repeated through the combined filter/PGA topology in the case of our particular receiver. A programmable gain of 48dB in 6dB steps is merged into the seventh-order Chebyshev filter, which is arranged as the preceding block of the ABB. The remaining variable gain range including a stage of 6dB fine gain tuning in 0.5dB steps is implemented in the latter stage of the ABB. Such arrangement ensures that the gain switching can be done from the last stage towards the front stage. Therefore, the noise figure in higher gain settings can be maintained almost in the minimum value since the gain of the preceding stages is not changed. Fig. 3.4 shows the recommended noise performance at different gain settings. The noise figure is almost constant, as pointed out earlier, less than 22dB as the gain is higher than 30dB. Then, the noise grows rapidly because the gain in the preceding stages is switched down.

Table 3.3 Recommended analog baseband specifications

Supply voltage (V)		1.2
Channel Bandwidth (MHz)		2－5
Passband ripple (dB)		0.5
Attenuation (dB)	5.25MHz	-30
	13.25MHz	-90
	29.25MHz	-130
Gain range (dB)		60－-6
Gain step (dB)		0.5
Gain accuracy (dB)		±0.25
Output Swing (Vp-p) @ single-ended		1
Noise Figure (dB) @max. gain		25
IIP3 (dBm) @(N+2, N+4), max. gain		+18
DC offset (mV)		<10
Common-mode DC		0.6
Group delay (μs)		150



Gain(dB)	NF(dB)
-6	56
0	50
6	44
12	38
18	32
24	28
30	25
36	25
42	25
48	25
54	25

Fig. 3.4 NF versus gain settings in the analog baseband.

3.1.3 Frequency Synthesizer

As derived in Ch 2.2, the design of LO generation is much challenging due to the stringent requirements on large frequency range (470-862MHz at least), low phase noise (-37dBc rms), low spur level (-60dBc), as well as fast settling time and low power consumption. Since DVB-T/H standard requires a step size as low as 166.67 kHz, a ΔΣ fractional-N synthesizer is used for LO generation. In an integer-N frequency synthesizer design, it is supposed to lower the reference frequency to have fine step size, leading to high division ratio and high in-band phase noise. Moreover, it also causes small loop bandwidth which is usually limited to less than one tenth of the reference frequency for stability, resulting in long settling time. On the contrary, a fractional-N frequency synthesizer can operate with a high reference frequency since its division ratio could be noninteger. This is helpful in reducing the division ratio and widening the loop bandwidth. A low division ratio reduces the noise contribution of reference crystal, dividers and charge pump. Moreover, a large loop bandwidth can help supress the contribution of VCO phase noise. Thus, the in-band phase noise can be supressed and fast settling can be achieved simultaneously. In addition, fractional synthesis also allows sharing the same crystal with the existing platform applications such as cellular phone RF transceivers. Even though the fractional-N synthesizers have so many advantages, the noise disturbance from the digital circuits such as the delta-sigma modulator is much severe.

Since the LO signal is generated using a divide-by-N divider from the PLL output, the phase noise mask of the LO would be 20xlog(N) dB lower than that of the PLL output. Fig. 3.5 illustrates the recommended mask requirements of phase noise at the PLL and LO output, respectively. This recommended phase noise profile refers to an integrated phase noise of -37dBc from 1kHz to 3.8MHz at the LO output.

Recommended circuit specifications are given in Table 3.4.

Table 3.4 Recommended frequency synthesizer specifications

Supply voltage (V)		1.2
VCO tuning range (GHz)		2.4－3.6
PLL resolution (Hz)		100
PLL Phase Noise (dBc)	10kHz	-70
	100kHz	-78
	1MHz	-118
RMS phase noise (°) @ 400－4MHz		2
Spurious tones		< -53
Settling time (μs)		300
Reference Clock (MHz)		10－40
LO Output (through Divide_by_N)		
LO range (MHz)		470－862
RMS phase noise (°) @ 400－4MHz		0.5
LO Spurs (dBc)		< -65

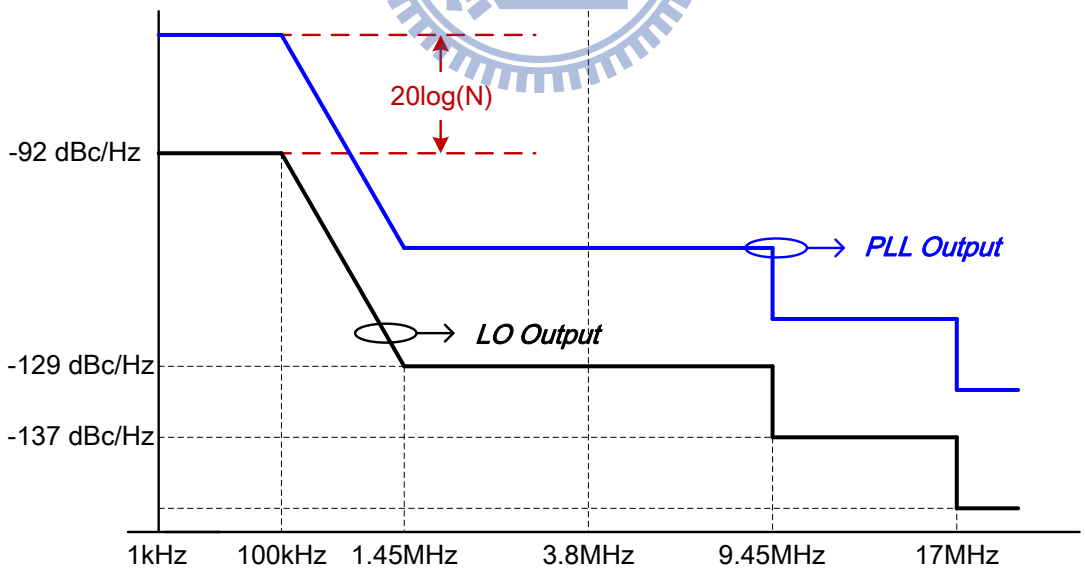


Fig. 3.5 Recommended LO/PLL phase noise mask.

3.2 Link Budget Analysis

The purpose of link budget analysis is to verify whether the distributed noise and distortion performance of the system meets the design specifications. By cascading the specifications of building blocks in the receiver chain, link budget analysis can provide an insight into the system performance. It would be very helpful to understand when and where each building block dominates the others and limits the system performance. The key performance factors such as noise figure and IP3 are described in this section.

3.2.1 Cascaded Noise Analysis

For a chain of circuit blocks, the overall NF of a cascaded system can be calculated using the Friis equation [28]:

$$F_{tot} = 1 + (F_1 - 1) + \frac{F_2 - 1}{A_1^2} + \frac{F_3 - 1}{A_1^2 A_2^2} + \cdots + \frac{F_m - 1}{A_1^2 A_2^2 \cdots A_{m-1}^2}, \tag{3.1}$$

where F_i and A_i are the noise factor and gain of the i^{th} stage. In the case of our particular receiver, the LNA is the first stage, followed by the mixer and the analog baseband. Table 3.5 lists the NF of the building blocks in the sensitivity level. This leads to an overall NF of 3.65dB by (3.1). Percentage contribution of the three blocks to the overall system NF is shown in the pie diagrams in Fig. 3.6. As can be found, the LNA contributes a significant part.

Table 3.5 NF and IIP3 distribution in the maximum gain mode

Block	LNA	Mixer	ABB	System
Gain (*dB*)	21	15	55	91
NF (*dB*)	3	15	25	3.65
IIP3 (*dBm*)	0	9	33*	-12.7

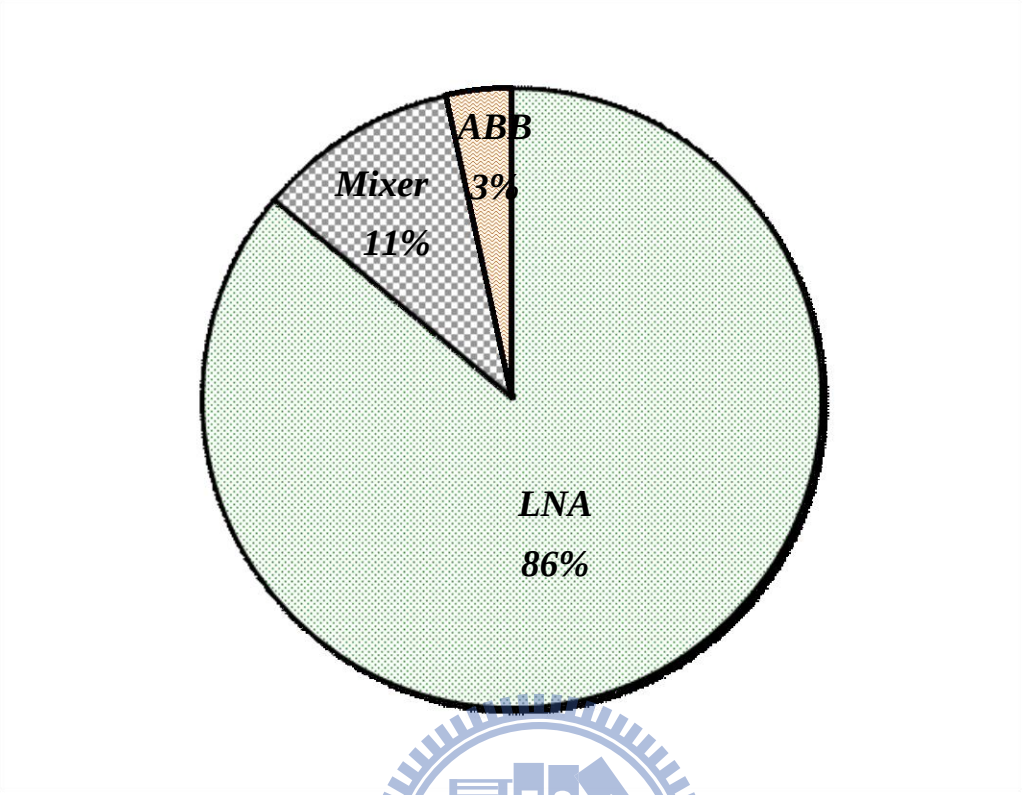


Fig. 3.6 Noise contributions from different blocks in the maximum gain mode.

3.2.2 Cascaded intermodulation-distortion analysis

When cascading several nonlinear stages, the overall system IIP_3 can be calculated using the following formula,

$$\frac{1}{A_{IIP3_{tot}}^2} = \frac{1}{A_{IIP3_1}^2} + \frac{A_1^2}{A_{IIP3_2}^2} + \frac{A_1^2 A_2^2}{A_{IIP3_3}^2} + \cdots + \frac{A_1^2 A_2^2 \cdots A_{m-1}^2}{A_{IIP3_m}^2}, \tag{3.2}$$

where A_{IIP3i} and A_i are the input referred IIP3 (in volts) and the voltage gain of the i^{th} stage, respectively.

From the formula above, it can be found that the overall linearity can be significantly dominated by one limiting block. In the receiver chain, the mixer typically is the bottleneck of linearity. Under this condition, there is no improvement achievable if attention is paid on improving the linearity of the other components such as the LNA. In fact, to make this true, the contribution of IMD3 from the analog baseband should be suppressed sufficiently. This can be done by placing a real pole at

the output of the mixer to pre-filter the out-of-channel interference. As the nonlinearity of the mixer is limited by its input transconductance stage, which is typical in most design cases, this added pole cannot improve the IIP3 of the mixer itself. From the view of overall system, however, this added pole indeed relaxes the IIP3 requirements of the following stages. In other words, for the link budget calculation, some revisions should be made to reflect this effect, which is explained as follows.

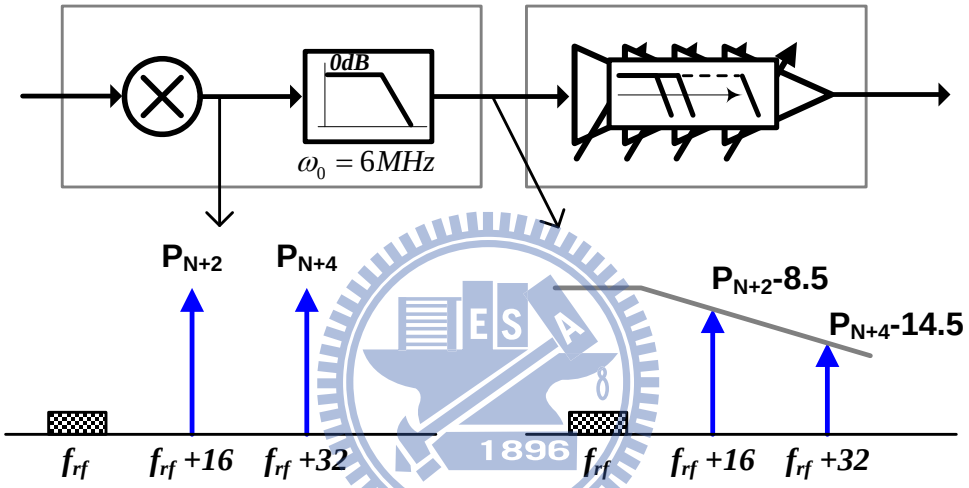


Fig. 3.7 Pre-filtering effect at the mixer output.

As shown in Fig. 3.7, the desired signal along with two interferers which are two and four channels (16MHz and 32MHz) away from the desired channel is amplified and down-converted to the baseband at the mixer output. If no pole is placed at the mixer output, the level of the interferers would be P_{N+2} and P_{N+4}, respectively. As a pole at 6MHz is added at the mixer output, two interferers would have extra attenuation of 8.5dB and 14.5dB, respectively. Here, one real-pole system is assumed for the calculation. Assume the analog baseband has an IIP3 denoted as $P_{IIP3,ABB}$. From (2.8), the contribution of third-order intermodulation distortion (IMD3) which is referred to the ABB input would be suppressed due to this extra pole and expressed as

$$P_{IMD3} = 2(P_{N+2} - 8.5) + (P_{N+4} - 14.5) - 2P_{IIP3,ABB},$$

$$P_{IMD3} = 2P_{N+2} + P_{N+4} - 2(P_{IIP3,ABB} + 15.75). \quad (3.3)$$

The derivation shows that an equivalent improvement of 15.75dB can be added into the IIP3 performance of ABB for the link budget analysis to reflect the benefit from the extra pole at the mixer output. As the analog baseband achieves an IIP3 of +18dBm, an IIP3 of +33.75dBm can be taken for the link analysis.

According to Table 3.5, where the IIP3 of the building blocks in the maximum gain mode are listed, contribution of the three blocks to the system IIP3 is depicted in Fig. 3.8. As can be found, the mixer significantly dominates the overall IIP3.

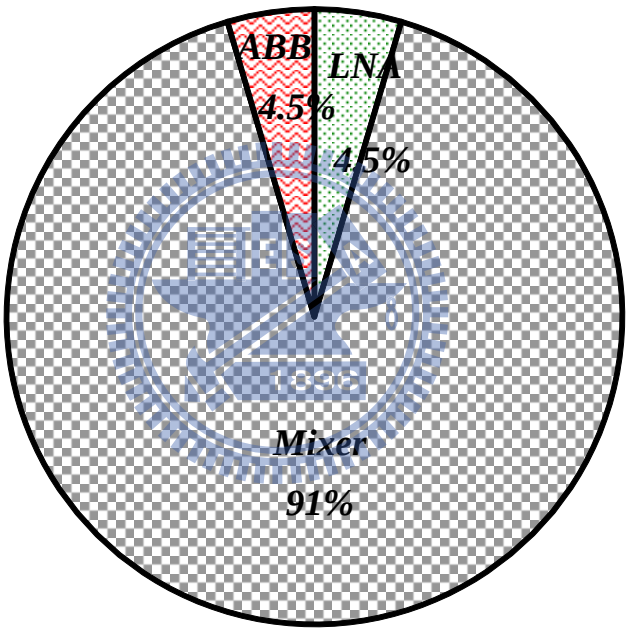


Fig. 3.8 IIP3 contributions from different blocks in the maximum gain mode.

3.3 System Design Verification

In real radio systems there are various analog/RF impairments which contribute to the impact on the system performance. These impairments such as nonlinearity, I/Q mismatch, phase noise can be viewed as additive noise sources, which contribute to the noise floor and degrade the signal-to-noise ratio (SNR). It is noted that SNR is

sometimes modified to include the interference and described as the signal-to-noise-and-interference ratio (SNIR). Whether SNR or SNIR, they can be used to predict bit error rate (BER) performance of a receiver. In this section, we will explore the impact of various noise-like impairments in different reception scenarios.

3.3.1 Sensitivity and Dynamic Range

Sensitivity and dynamic range are two main performance parameters in a receiver system. Sensitivity defines the minimum input signal level that must be detected and demodulated by the receiver with acceptable quality, and the dynamic range defines the entire range of input signal level from the sensitivity threshold up to the maximum tolerable strength.

In addition to the thermal noise most concerned in the conventional formula, various noise-like impairments are taken into account to observe the system performance across the dynamic range. To evaluate the level of noise floor, several dominant noise-like components are summed and given by

$$P_{\mathrm{N},tot} = P_{\mathrm{N},thermal} + (P_{\mathrm{N},IMD} + P_{\mathrm{N},PN} + P_{\mathrm{N},IMRR}). \tag{3.4}$$

where $P_{N,thermal}$ represents the thermal noise of the circuit blocks, $P_{N,IMD}$ represents the intermodulation distortion components due to the circuit nonlinearity, and $P_{N,PN}$ denotes the contribution from LO phase noise, and $P_{N,IMRR}$ counts the impairment of quadrature inaccuracy. As normalized to the signal power, the formula can be rewritten as

$$\frac{1}{SNR_{total}} = \frac{1}{SNR_{thermal}} + \left[\frac{1}{SNR_{IMD}} + \frac{1}{SNR_{PN}} + \frac{1}{SNR_{IMRR}}\right]. \tag{3.5}$$

In the case of dynamic range evaluation, only the desired signal is taken into account, i.e., no other interferers are received. For a given receiver system, therefore, SNR_{PN} and SNR_{IMRR} are almost constant across the dynamic range, while $SNR_{thermal}$ and SNR_{IMD} are highly dependent on the strength of input signal.

$$SNR_{thermal} = P_{sig} - (kTB + NF) = P_{sig} - (-105.2 + NF). \tag{3.6}$$

$$SNR_{IMD} = P_{sig} - P_{N,IMD} = 2 \times (IIP3 - P_{sig}). \quad (3.7)$$

Here, the effect of intermodulation distortion considers only the third-order nonlinear component, which dominates the others in the evaluation of dynamic range.

Table 3.6 shows the spreadsheets containing the gain settings for different input level. The corresponding NF and IIP3 are also listed for the dynamic range evaluation. By substituting the data in this table into (3.6) and (3.7), $SNR_{thermal}$ and SNR_{IMD} at various input power level can be calculated. Assume that the system has a 41dB of SNR_{PN} and a 37dB of SNR_{IMRR}, i.e., the in-band phase noise should be less than 0.5 degree rms and the I/Q accuracy should be better than -37dBc. Based on these performance parameters, the overall SNR across the dynamic range can be calculated from (3.5) and plotted in Fig. 3.9. As can be seen, the thermal noise dominates the noise floor when the signal level is at the threshould of sensitivity. As soon as the signal level becomes larger, the noise contribution from phase noise and I/Q impairments can dominate the thermal noise and limit the maximum achievable SNR. As the signal level exceeds -10dBm, the contribution from IMD3 significantly affects the received signal quality.

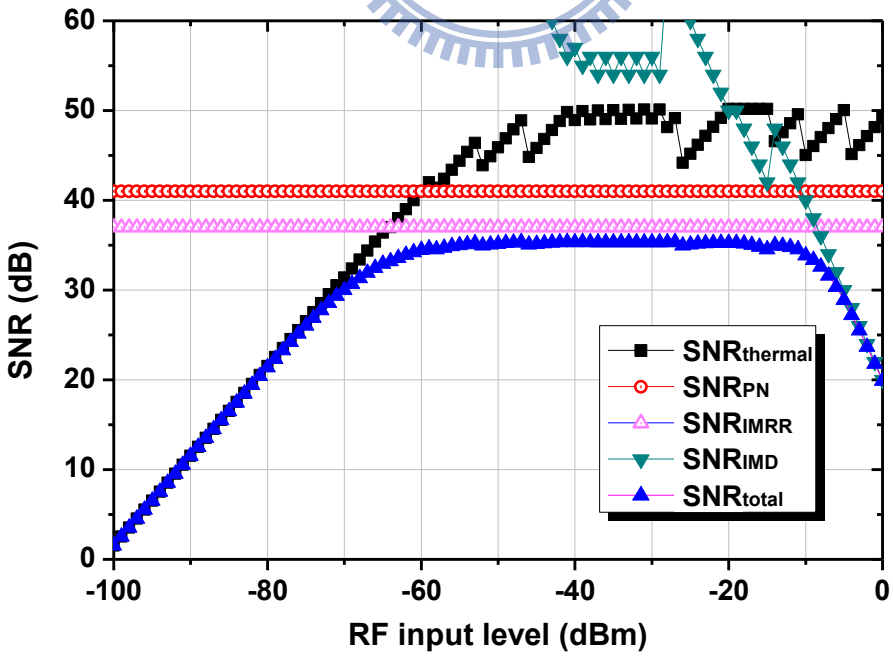


Fig. 3.9 SNR versus RF Input power level in sensitivity test.

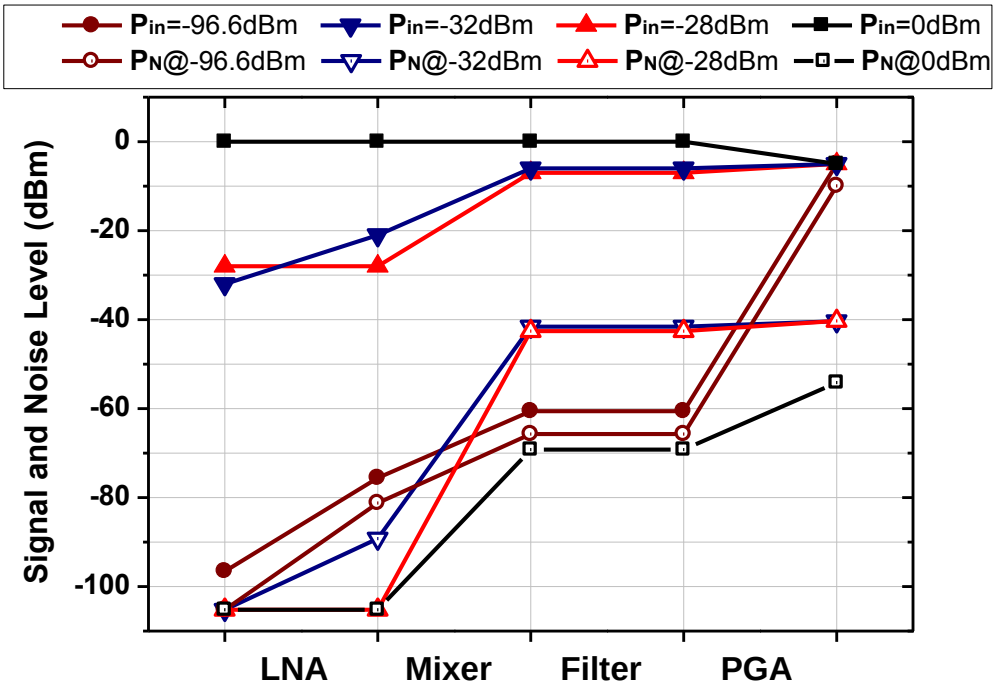


Fig. 3.10 Signal and noise levels along the receiver chain in DR test.

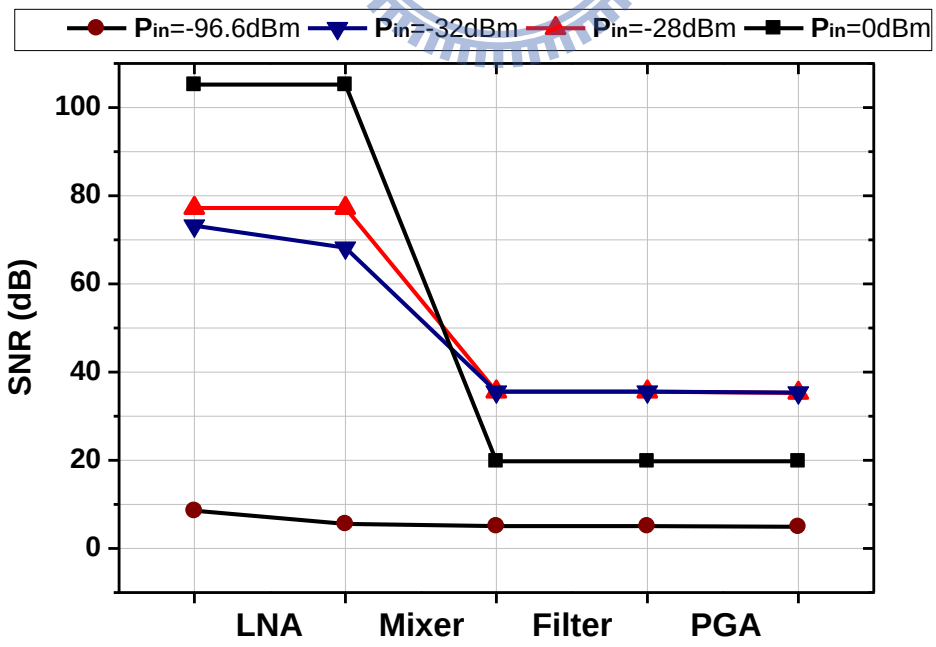


Fig. 3.11 SNR degradation along the receiver chain in DR test.

Table 3.6 Gain settings versus input level in dynamic range test

	Front-end		ABB		Cascaded	Cascaded
Pin(dBm)	Gain	NF	Gain	NF	NF (dB)	IIP3 (dBm)
-97 to -95	36	3.5	56 to 54	25	3.65	-13
-94 to -89	36	3.5	53 to 48	25	3.65	-13
-88 to -83	36	3.5	47 to 42	25	3.65	-13
-82 to -77	36	3.5	41 to 36	25	3.65	-13
-76 to -71	36	3.5	35 to 30	25	3.80	-13
-70 to -65	36	3.5	29 to 24	28	4.21	-13
-64 to -59	36	3.5	23 to 18	32	5.82	-13
-58 to -53	36	3.5	17 to 12	38	9.32	-13
-52 to -47	36	3.5	11 to 6	44	14.4	-13
-46 to -41	36	3.5	5 to 0	50	14.4	-13
-40 to -39	34	4.3	1 to 0	50	16.3	-11.5
-38 to -37	32	4.8	1 to 0	50	18.2	-10
-36 to -35	30	5.5	1 to 0	50	20.2	-8
-34 to -33	28	6.4	1 to 0	50	22.1	-6
-32 to -31	26	7.5	1 to 0	50	24.1	-4
-30 to -29	24	9.0	1 to 0	50	26.1	-2
-28 to -27	21	10	2 to 1	50	29.1	5
-26 to -21	21	10	0 to -5	50	35.0	5
-20 to -15	15	14	0 to -5	50	35.0	7
-14 to -11	0	36	9 to 6	44	44.6	10
-10 to -5	0	36	5 to 0	50	50.2	10
-4 to 0	0	36	-1 to -5	56	56.0	10

Fig. 3.10 illustrates the signal and noise levels along the receiver chain in the dynamic range (DR) test, where four levels of input power are shown as the examples. Here, only the thermal noise component is shown. By taking the other impairments into account, their corresponding SNR plots are also in Fig. 3.11. As the input signal level is at -96.6dBm, a target sensitivity level, the receiver chain provides 91.5dB of gain and amplifies the signal level to -5.1dBm along with a noise level of -10.04dBm. The output SNR is 4.94dB, well above the required minimum SNR of 4.6dB for QPSK demodulation. This result conforms to a cascaded NF of 3.65dB as pointed out

earlier. As the input level is up to -32dBm or -28dBm, the output SNR is bounded at 35dB due to the constraints of phase noise and IMRR.

It is noted that in the case of our targeted receiver the LNA stage is assumed to be bypassed and combined into the mixer, implying that the LNA contributes no impact to the system in this performance evaluation. As the input signal has a level up to 0dBm, the RF front-end is set at a minimum gain of 0dB and the analog baseband has a gain attenuation of -5dB. The output signal level is -5dBm with a SNR of 19.8dB, while over 50dB if only AWGN is considered as shown in Fig. 3.10. As mentioned earlier, the SNR degrades much in the mixer stage due to the effect of third-order nonlinearity.

3.3.2 Selectivity Test

According to S2 test pattern, one digital interferer at two channels away from the desired channel have -28dBm of power level and an U/D ratio of 40dB. To ensure a minimum SNR requirement of 20dB for 64-QAM 3/4 CR scheme, the input referred maximum acceptable noise plus interference power within the desired signal channel is

$$P_{N+I(acceptable)} = -28dBm - 40dB - 20dB = -88dBm\,. \qquad (3.13)$$

Because in this test scenario there are several interfering products created, the allowable interference power (referred to the input of the receiver) must be distributed. The assumed power distribution is as follows,

Thermal noise power	30% (-5.2dB)	$\Rightarrow$ -93.2dBm
Second-order intermodulation products:	20% (-7dB)	$\Rightarrow$ -95dBm
LO spurs @ 16MHz	50% (-3dB)	$\Rightarrow$ -91dBm
LO integrated phase noise:	5% (-13dB)	$\Rightarrow$ -101dBm
I/Q mismatch:	5% (-13dB)	$\Rightarrow$ -101dBm

The thermal noise power corresponds to an NF of 12dB from (2.1). The IMD2 product determines the required IIP2 of +33Bm from (2.7). The interfering product due to the reciprocal mixing effect requires LO spurs less than -63dBc from (2.3). The

other two impairment contributions imply that both LO integrated phase noise and I/Q mismatch should be less than -33*dBc*. It should be noted that this assumption is used to determine the specifications of the receiver, which can provide information about feasibility evaluation in the early stage of the front-end design. The distribution can be made arbitrary as long as the sum of the distributions is equal to 100%. For example, if we distribute more power to LO spurs and less power to IMD_2 products, the LO spurs requirement will be relaxed but the receiver IIP2 requirement becomes more stringent.

Above-mentioned performance parameters are derived based on the minimum performance requirements. In fact, system design should retain certain margins for high yield. There is no unique way to define the value of design margins since they always compromise with other targets such as power consumption, cost, and size. With the performance parameters listed in Table 3.1 to 3.6, the signal, interference, and noise levels along the receiver chain can be calculated to evaluate the performance margins. It should be noted that in this test scenario the interference level dominates the input signal power, which is around -28dBm. Thus, the RF front-end is switched into LG mode with a gain back-off of 15dB according to Table 3.1.

Fig. 3.12 illustrates all signal levels including the desired signal (P_{sig}), the adjacent channel interference ($P_{interference}$), the thermal noise contribution ($P_{N,thermal}$), and the overall noise plus interference power ($P_{N,tot}$). The evaluation shows that the recommended specifications can achieve an output SNR of 22.3dB, which is 2.3dB well above the minimum requirement. As depicted in Fig. 3.13, an alternate evaluation shows that the recommended specifications can tolerate the desired signal level as low as -70.4dBm while maintaining an output SNR of 20dB in the presence of -28dBm interference. The result means that the recommended specifications can retain a margin of 2.4dB in the S2 (N+2) test.

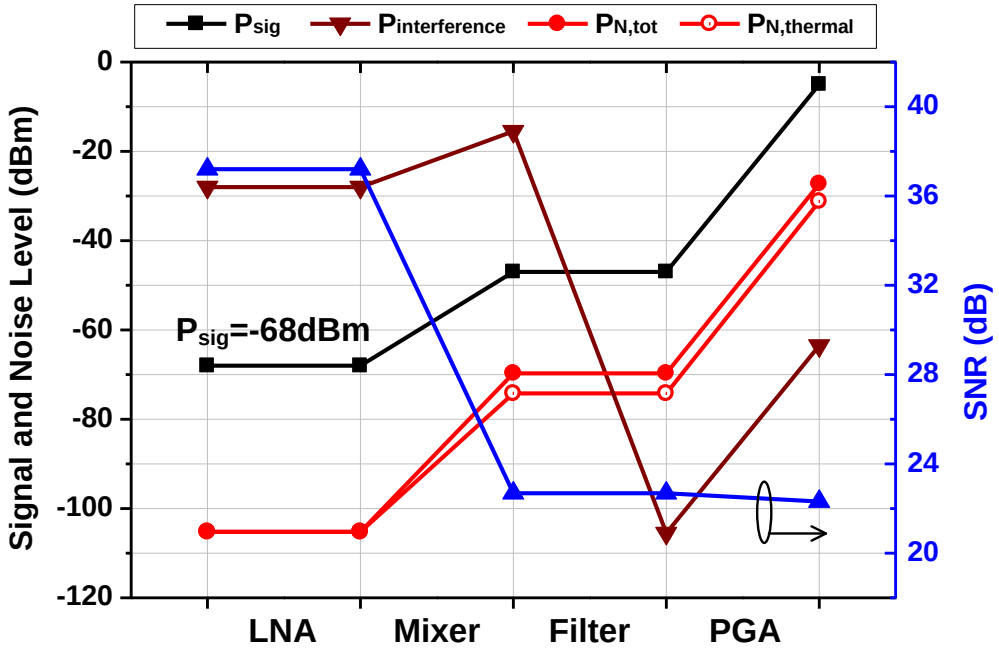


Fig. 3.12 Signal and noise levels along the receiver chain in S2 test.

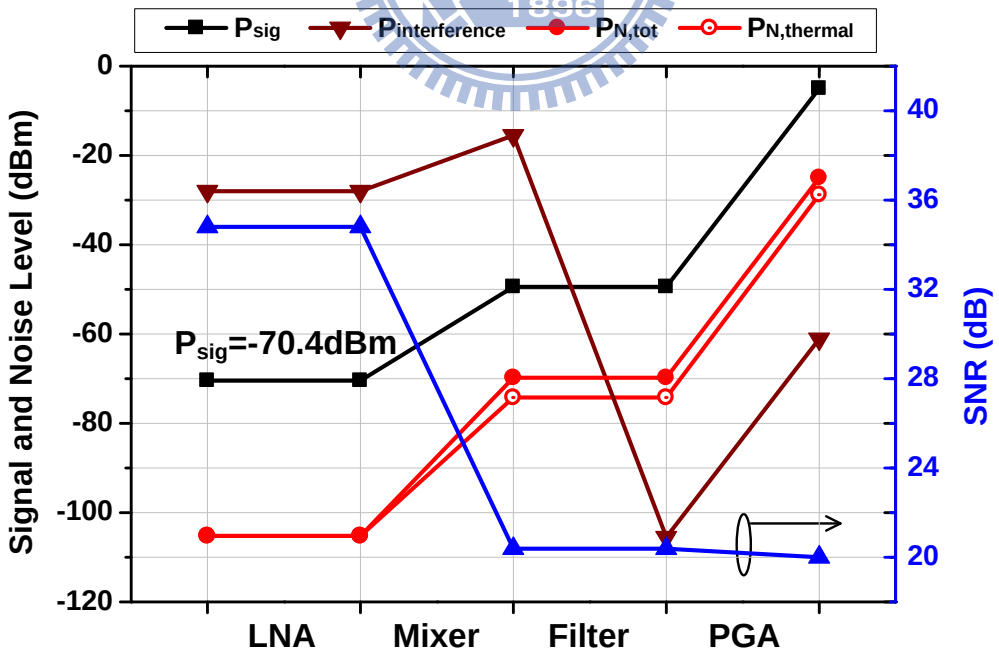


Fig. 3.13 Margined signal and noise levels along the receiver chain in S2 test.

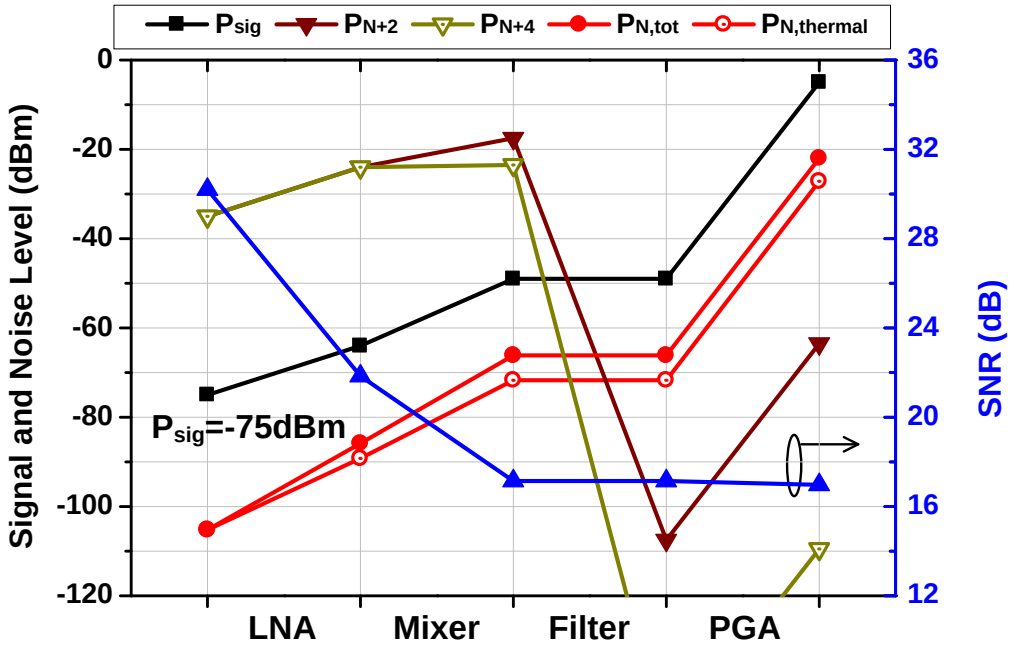


Fig. 3.14 Signal and noise levels along the receiver chain in L3 test.

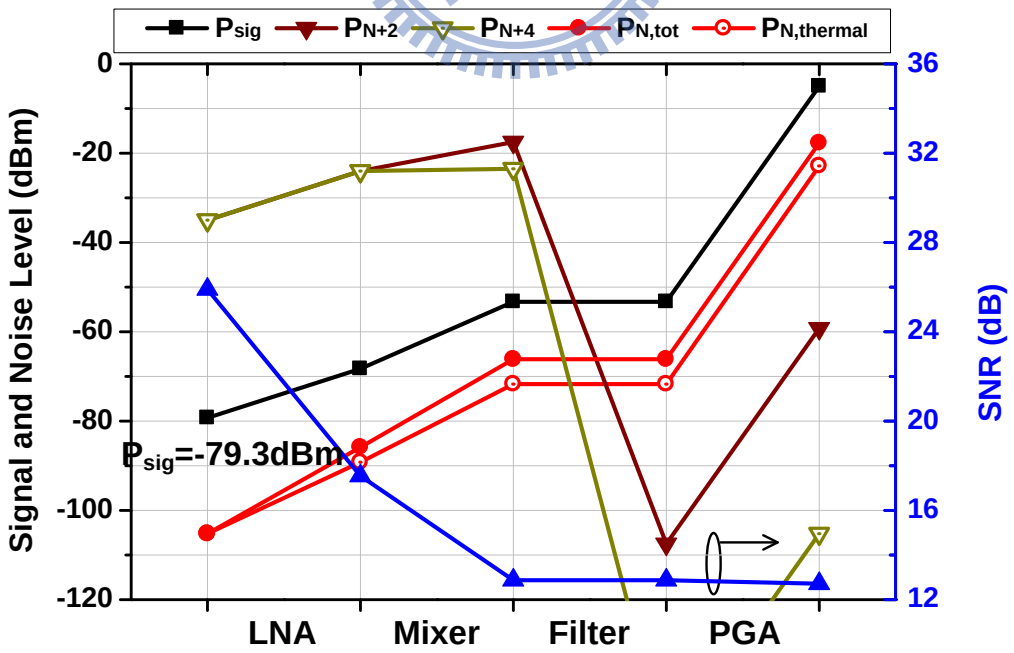


Fig. 3.15 Margined signal and noise levels along the receiver chain in L3 test.

3.3.3 Linearity Test

According to L3 test pattern, two digital interferers at two and four channels away from the desired channel have a power level of -35dBm and U/D ratio of 40dB. To ensure a minimum SNR requirement of 12.7dB for 16-QAM 2/3 CR scheme, the input referred maximum acceptable noise plus interference power in the desired signal channel is

$$P_{N+I(acceptable)} = -35dBm - 40dB - 12.7dB = -87.7dBm\,. \tag{3.13}$$

Similarly, the noise and interference power must be distributed and is assumed as follows,

Thermal noise power	14% (-8.5dB)	$\Rightarrow$ -96.2*dBm*
Third-order intermodulation products:	60% (-2.3*dB*)	$\Rightarrow$ -90*dBm*
Second-order intermodulation products:	6% (-12.3*dB*)	$\Rightarrow$ -100*dBm*
LO spurs @ 16MHz&32MHz:	18% (-7.5*dB*)	$\Rightarrow$ -95.2*dBm*
LO integrated phase noise:	1% (-20*dB*)	$\Rightarrow$ -107.7*dBm*
I/Q mismatch:	1% (-20*dB*)	$\Rightarrow$ -107.7*dBm*

From (2.1), the thermal noise power corresponds to an NF of 9dB. From (2.9), the IMD3 product determines an IIP3 requirement of -7.5dBm. Moreover, the IMD2 product determines the required IIP2 of +27dBm from (2.7). The interfering product due to the reciprocal mixing effect requires LO spurs less than -59.7dBc from (2.3). The other two impairment contributions also imply that both LO integrated phase noise and I/Q mismatch should be less than -32.7dBc.

As the receiver has the same performance parameters as the recommended specifications, the signal levels along the receiver chain is evaluated. Fig. 3.14 shows the signal levels including the desired signal (P_{sig}), the adjacent channel interference at N+2 channel (P_{N+2}) and N+4 channel (P_{N+4}), the thermal noise contribution ($P_{N,thermal}$), and the overall noise plus interference power ($P_{N,tot}$). Since the two interferers respectively has a power level of -35dBm and the desired signal has a power level of -75dBm, the total input power level will be around -32dBm. Thus, the RF front-end should have a gain back-off of 10dB according to Table 3.1 to tolerate this input signal level. The evaluation shows that the recommended specifications can achieve

an output SNR of 17dB, which is 4.3dB well above the minimum requirement. As depicted in Fig. 3.15, an alternate evaluation shows that the recommended specifications can tolerate the desired signal level as low as -79.3dBm while maintaining an output SNR of 12.7dB in L3 test scenario. The result shows that the recommended specifications can retain a margin of 4.3dB in the L3 (N+2, N+4) test.

3.4 Conclusion

In this chapter, we focus on the design considerations in distributing the overall receiver specifications into individual building block specifications. Furthermore, link budget analysis and system design verification are also discussed for a complete design procedure. Initially, a reasonable distribution of specifications across the building blocks must be set, either based on previous experience or some intuition. An excessive requirement on a specific block should be avoided, which would raise the risks to fail. Then, the overall system specifications should be verified by cascading the building blocks and calculating overall performance. By applying all kinds of standard tests to the receiver, from time to time, the overall system can be verified to check if it operates properly to meet all requirements. It is noted that this conversion is a rather iterative procedure since the distributions can be made arbitrary as long as the sum of the distributions equals to 100%.

The building block specifications obtained in this way could be used as starting point for the circuit level design, but still should be optimized by iterations. The main goal is to find the distribution that guarantees minimal power consumption as well as cost-effective chip area, in addition to compliance with the standard. This chapter provides recommended specifications of each circuit block, which are used as the initial reference specifications in realization of a direct-conversion receiver in CMOS technology as shown in the next chapter.

Chapter 4

LNA Compatible for Differential and Single-Ended Inputs

A single-stage noise-canceling LNA with a differential output, but a reconfigurable single-ended or differential input has been realized in 0.13μm CMOS technology. The LNA can flexibly operate as either differential or single-ended by adjusting external components without any change inside the chip. Moreover, it achieves good performance in noise figure, gain, input matching and differential balance, irrespective of the differential or single-ended configuration. The LNA is designed for sub 1-GHz applications. It provides 22.5dB voltage gain, +1dBm IIP3, and 2.5dB NF in the differential configuration, while achieving 23dB voltage gain, -0.5dBm IIP3, and 2.65dB NF in the single-ended mode. The LNA core circuit draws 2.5mA from a 1.2V supply voltage, and occupies a small chip area of 0.06mm^2.

4.1 Motivation

A low noise amplifier (LNA) is a sensitive block in an RF chip, and the LNA architecture involves the system plan. The determination of LNA input configuration depends not only on the level of system integration but on the operating environments. In a highly integrated system-on-a-chip (SoC) or a noisy environment, one more robust LNA design is necessary. More specifically, in a SoC solution, a sensitive RF front-end

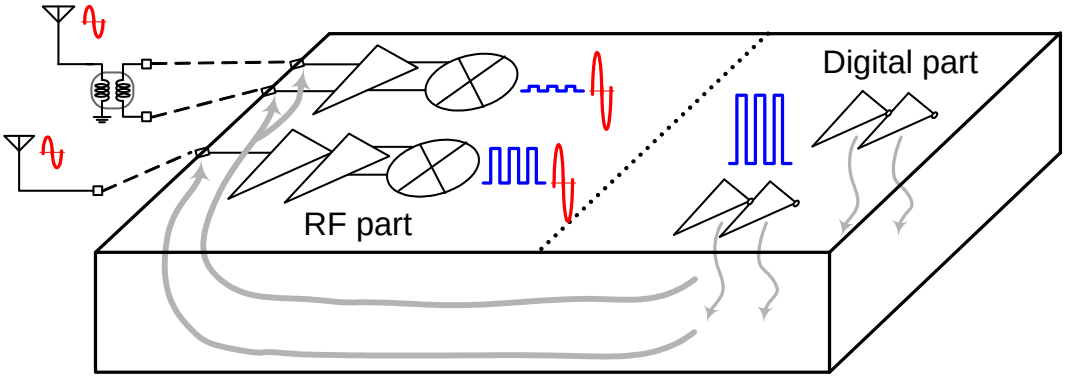


Fig. 4.1 Illustration of substrate noise coupling from a digital back-end to an LNA.

is integrated with a noisy digital back-end on the same die such that it inevitably suffers from the troublesome substrate noise and spurs leakage [28]. Take 802.11g WLAN SoC for an example. The 61st harmonic of the 40-MHz reference clock, which falls into the desired RF channel at 2440 MHz, would desensitize the receiver [29]. Thus, the use of a differential LNA is needed to alleviate this problem. As shown in Fig. 4.1, any noise coupled from the digital back-end arrives at not only the positive but the negative input nodes of a differential LNA and eventually appears as a common-mode signal, which can be cancelled by taking the output differentially [30]. Unfortunately, this mechanism does not exist in a single-ended input LNA. A single-ended LNA is prone to performance degradation due to the coupling noise/interference. Nevertheless, a single-ended LNA presents its superiority in a lower level of integration or a price-orientation solution. Although a differential LNA is popular due to its high immunity to noise, it generally requires an external balance-to-unbalance (balun) converter, which produces loss, degrades gain flatness, and raises cost. On the contrary, a single-ended input LNA presents lower noise figure and reduced bill-of-material (BOM) due to no need for an off-chip balun.

Differential and single-ended LNAs have their respective advantages in specific applications or operating environments. Accordingly, there exists the need for a reconfigurable LNA to flexibly operate as either a differential or single-ended configuration. Supporting both differential and single-ended configurations in LNAs is not common in literature. The difficulty lies in the constraint that the LNA must

simultaneously meet the specification requirements based on the link budget analysis, regardless of the differential or single-ended operation. One possible scheme was demonstrated in a 65nm CMOS tuner [[31], Fig. 4(a)]. It achieves similar gain, matched input impedance, sufficient linearity, and low NF in both configurations. However, an on-chip transformer is needed to perform single-to-differential transformation in the single-ended operation, which consumes a large chip area as well as production cost.

This chapter presents a reconfigurable LNA capable of receiving either a differential or a single-ended input, while providing a differential output. The LNA changes its input configurations simply by adjusting external components. No change inside the chip is needed. The LNA also achieves comparable performance between the two configurations. In particular, the LNA carries out the balun function under the single-ended configuration so that it needs no bulky transformer and only occupies a small chip area, well suitable for highly integrated receiver implementations.

4.2 Review of Existing CG-Based LNAs

4.2.1 CCC-CG LNA

Common-Gate (CG) LNA is attractive for its superior broadband input match, but suffers from a high noise factor of $1+\gamma/\alpha$ [32]. By inserting an inverting amplifier between the source and gate terminals of the CG amplifier, the transconductance of the CG transistor increases by a factor of $(1+A)$. Thus, the noise contribution from the CG transistor decreases by the factor $(1+A)$. This is known as the g_m-boosting technique [33]. As the inserted amplifier is noiseless, the noise factor is reduced to $1+(\gamma/\alpha)/(1+A)$. Based on this principle of operation, the capacitor cross-coupled (CCC) CG-LNA shown in Fig. 4.2 was proposed [34]-[36]. The cross-coupled capacitors realize the feed-forward amplification in a fully differential configuration. From the view of an equivalent half-circuit, it achieves an inserted amplification of -1 assuming $C_c >> C_{gs}$. As a result, the input transconductance is doubled without consuming extra DC current. The noise factor is hence reduced to $1+(\gamma/\alpha)/2$ since the capacitors contribute no additional noise. If an ideal wideband balun of $1:1$ is applied, the differential input impedance is transform into single-ended one approximately as

$$Z_{in} \approx (\frac{1}{G_{m1}} + \frac{1}{G_{m2}}) = \frac{1}{g_{mi}} \tag{4.1}$$

Here, a symmetric design is applied, i.e., $G_{m1}=G_{m2}=2g_{mi}$. The differential output voltage gain can be derived as

$$A_v = \kappa \cdot 2 \cdot g_{mi} R_L \tag{4.2}$$

where the factor κ equals to $2Z_{in}/(R_s+Z_{in})$, which is unity under a perfect input match condition.

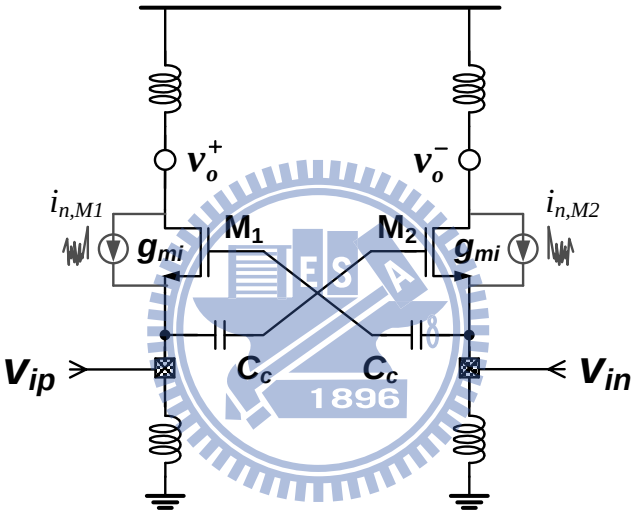


Fig. 4.2 Capacitor Cross-Coupled CG-LNA configuration.

4.2.2 CG-CS Balun LNA

Balun LNA is an attractive circuit topology with a noise-canceling technique [37]-[40]. As shown in Fig. 4.3, it utilizes a common-gate and a common-source amplifier as the input stage to realize single-to-differential conversion. The CG amplifier can provide a broadband impedance match with $Z_{in}=1/g_{m1}$. On the other hand, the CS amplifier makes the noise/distortion from the CG transistor appear as a common-mode source, which can be canceled at a differential output. As the CG and CS amplifiers provide the same gain, i.e., $g_{m1}R_{L1}=g_{m2}R_{L2}$, a balanced voltage output is

obtained. As $1/g_{m1}=R_s$, moreover, broadband impedance match can be achieved. Accordingly, this balun LNA provides a voltage gain of $2R_{L1}/R_s$. This implies that a resistor load of only 250Ω leads to a voltage gain of 20dB. Even though the noise from the CG amplifier can be canceled due to the parallel CS amplifier, the overall NF may be too high due to the significant contribution from the CS amplifier. Assume only the thermal noise of transistors and resistors are taken into account. If the effect of transistors' finite conductance is neglected, the noise factor of the entire LNA can be approximated by

$$F = 1 + \frac{1}{g_{m2}R_s}\frac{\gamma}{\alpha} + \frac{2}{A_v}\left(1 + \frac{1}{g_{m2}R_s}\right) \tag{4.3}$$

where γ/α represents the transistor's excess noise factor and A_v represents the voltage gain. In (4.3), the second term is contributed by CS transistor thermal noise, and the last term denotes the contribution due to the load resistors R_{L1} and R_{L2}. It indicates that a significant improvement to the noise factor can be obtained by increasing g_{m2}. In [38]-[40], a g_{m2} larger than four times of g_{m1} is chosen to achieve a better NF, while at the expense of more current consumption.

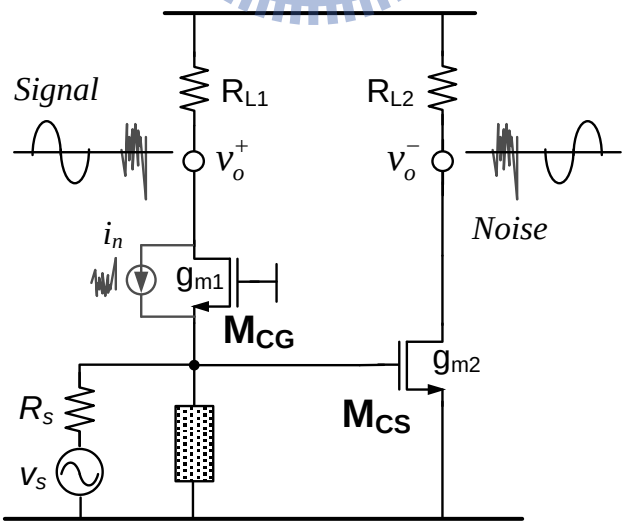


Fig. 4.3 Noise-canceling Balun LNA configuration.

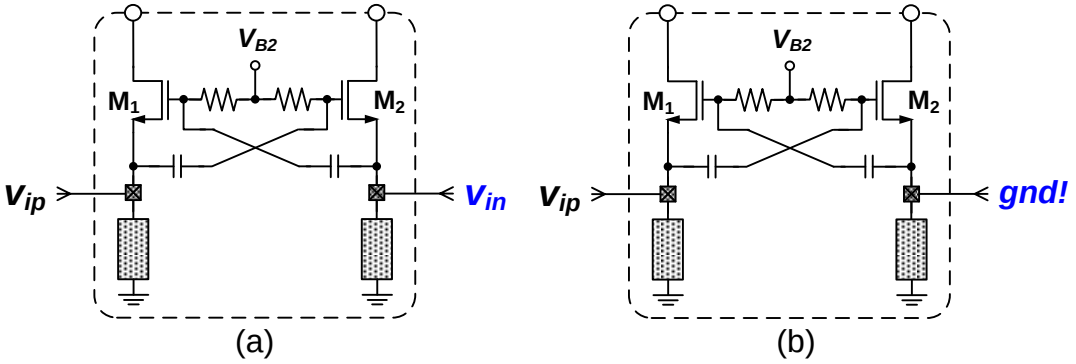


Fig. 4.4 LNA configured as either (a) differential input CCC-CG LNA, or (b) single-ended input Balun LNA.

4.3 Design of Reconfigurable LNA

The previous section reviewed two existing CG-based LNAs. Interestingly, re-configuring these two circuit topologies is feasible if properly arranged. As found in Fig. 4.4, the CCC-CG LNA can be re-configured as the balun LNA by merely coupling its negative input to the ground. Comparing Fig. 4.4 (a) and (b), M_1 is always constructed as a CG amplifier, but M_2 is changed from a CG amplifier to a CS amplifier. Recalling the discussions in the previous section, the CCC-CG LNA and the balun LNA can achieve the same performance in terms of input impedance match and voltage gain. This greatly enhances attraction to realize a reconfigurable-input LNA based on this characteristic. Before that, however, the noise issue must be addressed first. To be compatible with the differential operation mode, a symmetric design with equally sized devices and bias is required. Unfortunately, such a design will result in a poor NF in the single-ended mode of operation. From (4.3), the noise figure is as high as 3.8dB, assuming $(\gamma/\alpha)=1$, R_L =250Ω, and $1/g_{m1}=R_s$.

To alleviate this noise issue, this work proposes a *common-mode rejecting (CMR)* buffer to improve the NF performance, especially under the single-ended operation. As will be shown later, the cascode CMR buffer results in a feed-forward path to reduce the noise contribution of the CS transistor without need to increase $g_{m,CS}$ as commonly used in literature. Circuit balance is therefore sustained, making the design of reconfigurable operations more reliable.

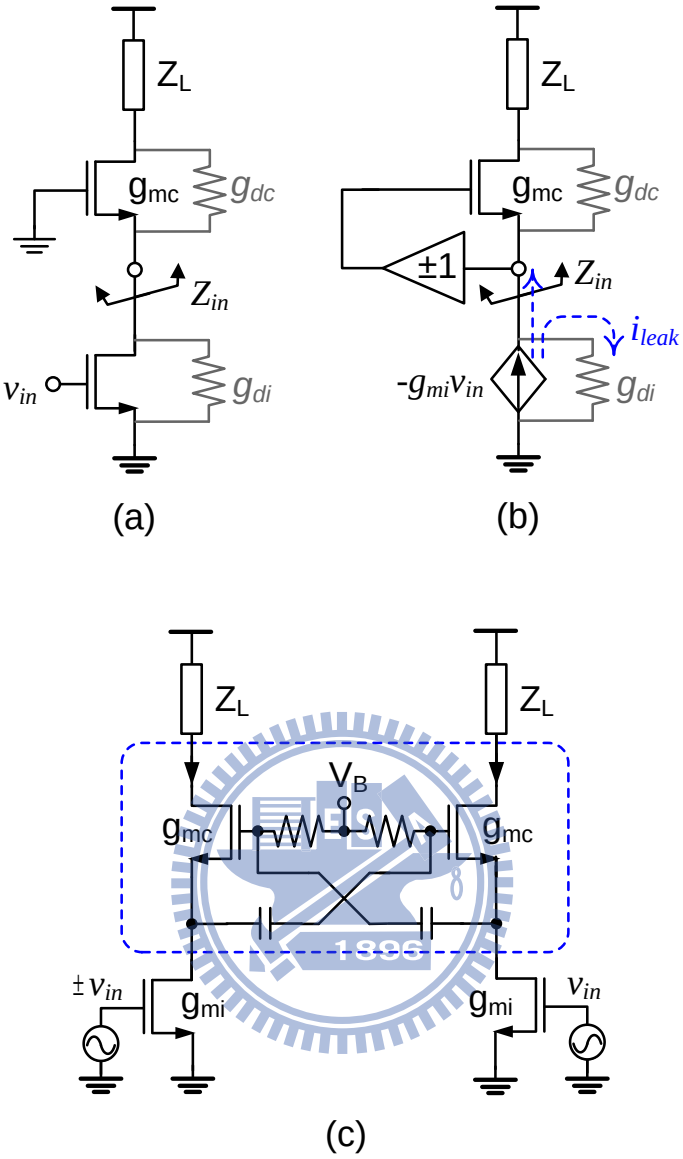


Fig. 4.5 Cascode current buffer (a) conventional CG buffer, (b) Gm-boosting technique with a feed-forward gain of +1 or -1, (c) the proposed CMR buffer.

4.3.1 Proposed CMR Buffer

In general, a CG transistor is in cascode as a current buffer to increase input/output isolation and to alleviate the Miller's effect. The CG current buffer provides a current gain approximate to unity for any input current. In contrast to this, a CMR buffer is proposed in this paper, which presents a higher current gain, but a

lower gain corresponding to a differential or a common-mode signal, respectively. This mechanism can be explained and illustrated in Fig. 4.5.

Fig. 4.5(a) depicts a cascode amplifier, where the finite transistor output conductances g_{di} and g_{dc} are taken into account. In order to steer the input signal current as much as possible to the output, this cascode CG buffer must present a low input impedance, $Z_{in} = (1+g_{dc}Z_L)/(g_{mc}+g_{dc})$. By the principle of current division, this buffer provides a current gain of $1/(1+g_{di}|Z_{in}|)$. The lower $g_{di}|Z_{in}|$ is, the higher the gain is. Utilizing the principle of g_m-*boosting* technique, Z_{in} can be effectively scaled down or up corresponding to the feed-forward gain response. As shown in Fig. 4.5(b), if the gate to source terminal exhibits a gain response of *-1*, Z_{in} will decrease nearly by a half as $(1+g_{dc}Z_L)/(2g_{mc}+g_{dc})$. Accordingly the current gain becomes higher. If the gain response is *+1*, on the other hand, Z_{in} will boost to $(1+g_{dc}Z_L)/g_{dc}$. This causes much current to leak through g_{di}, leading to a lower current gain of $g_{dc}/(g_{dc}+g_{di})$.

From the above discussions, it will be highly attractive to take advantage of these two impedance transfer characteristics to simultaneously process desired and undesired signals. Fortunately, this mechanism can be reflected in a differential configuration by a pair of capacitors which cross-couple the gate-source terminals of the cascode CG buffers as shown in Fig. 4.5(c). For the desired differential signal, there exists a gain response of *-1* between the gate and source terminals, increasing the desired signal gain. For the undesired common-mode signal, however, the featured gain response is *+1*. Thus, the boosted impedance strengths the leakage effect for the undesired signal. The respective current gain can be derived as

$$A_{I,dm} = \frac{2g_{mc}+g_{dc}}{2g_{mc}+g_{dc}+g_{di}+g_{di}g_{dc}Z_L} \approx 1-\frac{g_{di}}{2g_{mc}} \quad , \tag{4.4}$$

$$A_{I,cm} = \frac{g_{dc}}{g_{dc}+g_{di}+g_{di}g_{dc}Z_L} \quad . \tag{4.5}$$

Therefore, the CMRR is enhanced by a ratio of about $(1+g_{di}/g_{dc})$ in contrast to a conventional CG buffer that features a constant current gain of about $(1-g_{di}/g_{mc})$ irrespective of differential or common-mode signal.

Although this proposed CMR buffer appears to be similar to the input stage of the CCC CG-LNA in [34]-[36], the characteristic of CMRR enhancement was not mentioned. When used as a cascode current buffer, the enhanced CMRR can

compensate for the mismatch prior to this buffer. It exhibits great advantages as combined into a pseudo-differential amplifier which eliminates the constant current source for higher linearity, but at the expense of poor CMRR [41]. It could help suppress even-order harmonic distortions, improving the IIP2.

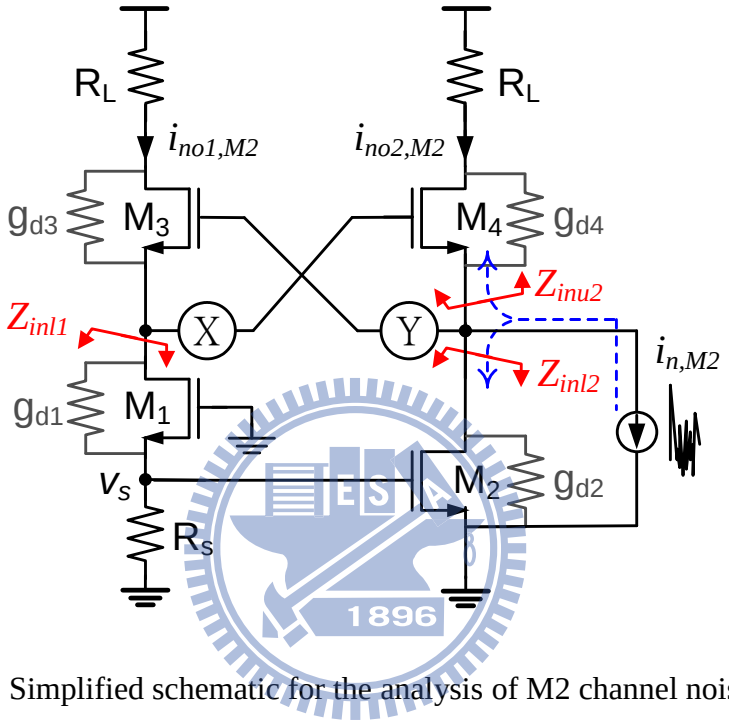


Fig. 4.6 Simplified schematic for the analysis of M2 channel noise.

4.3.2 Noise Reduction in Single-Ended Configuration

As the CMR buffer is in cascode of the CG-CS input stage, the coupling configuration results in a feed-forward path to suppress the dominant noise contributor $i_{n,M2}$, improving the overall NF. This effect can be analyzed from the simplified schematic as shown in Fig. 4.6.

By using the impedance ratio based upon the current division principle at node X, the output noise current $i_{no2,M2}$ due to $i_{n,M2}$ can be determined. On the other hand, the output noise current $i_{no1,M2}$ can be calculated by treating M_3 as a CS amplifier with a degenerative resistance Z_{inl1}. M_3 senses the noise voltage at node X, and generates the output noise current $i_{no1,M2}$. Therefore, the two output noise current

$i_{no2,M2}$ and $i_{no1,M2}$, can be expressed, respectively, as

$$i_{no2,M2} = \frac{Z_{inl2}}{Z_{inl2} + Z_{inu2}} \cdot i_{n,M2}, \tag{4.6}$$

$$i_{no1,M2} \approx -\frac{g_{m3}}{1 + g_{m3} \cdot Z_{inl1}} \cdot \left(Z_{inu2} \| Z_{inl2}\right) \cdot i_{n,M2}. \tag{4.7}$$

And the differential output noise current is approximate as

$$i_{no,M2} = i_{no1,M2} - i_{no2,M2} \approx -\frac{1 + Z_{inl2}/Z_{inl1}}{1 + Z_{inu2}/Z_{inl2}} \cdot i_{n,M2} \quad . \tag{4.8}$$

As aforementioned, Z_{inu2} is boosted due to the g_m-boosting technique with an inserted amplifier having a positive gain of K. Here, K denotes the conversion gain from node Y to X, which is close to unity. As a result, Z_{inu2} has an order of magnitude close to $1/g_{d4}$. On the other hand, Z_{inl2} is reduced by a factor smaller than $1/g_{d2}$ due to the shunt feedback through the path from M_3, then M_1, to the gate of M_2. As to Z_{inl1}, it is enlarged by a factor larger than two due to the series feedback by the source resistance R_s. Performing *Kirchhoff's Current Low* at nodes X and Y, we obtain the three terminal impedances as,

$$Z_{inu2} = \frac{1 + g_{ds4} R_{L2}}{(1 - K) \cdot g_{m4} + g_{ds4}}, \tag{4.9}$$

$$K = \frac{1}{1 + \frac{g_{ds3}}{g_{m3}} + \frac{g_{ds1}}{g_{m3}} \left(\frac{1 + g_{ds3} R_{L1}}{1 + (g_{m1} + g_{ds1}) R_s} \right)}. \tag{4.10}$$

$$Z_{inl2} = \frac{1}{g_{ds2}} \frac{1}{1 + \frac{g_{ds1}}{g_{ds2}} \left(\frac{g_{m1} R_s}{1 + g_{m1} R_s} \right)}, \tag{4.11}$$

$$Z_{inl1} = \frac{1}{g_{ds1}} \cdot \left[1 + (g_{m1} + g_{ds1}) \cdot R_s\right]. \tag{4.12}$$

By hand calculations, we get that Z_{inu2} is close to Z_{inl2}, and Z_{inl1} is about four times of Z_{inl2} in this design. This leads to the noise current gain, $i_{no,M2}/i_{n,M2}$, about 0.63 from (4.8). As a result, the noise factor contributed by M_2 is reduced by a factor of 0.4 as compared to the conventional balun LNA without the CMR buffer.

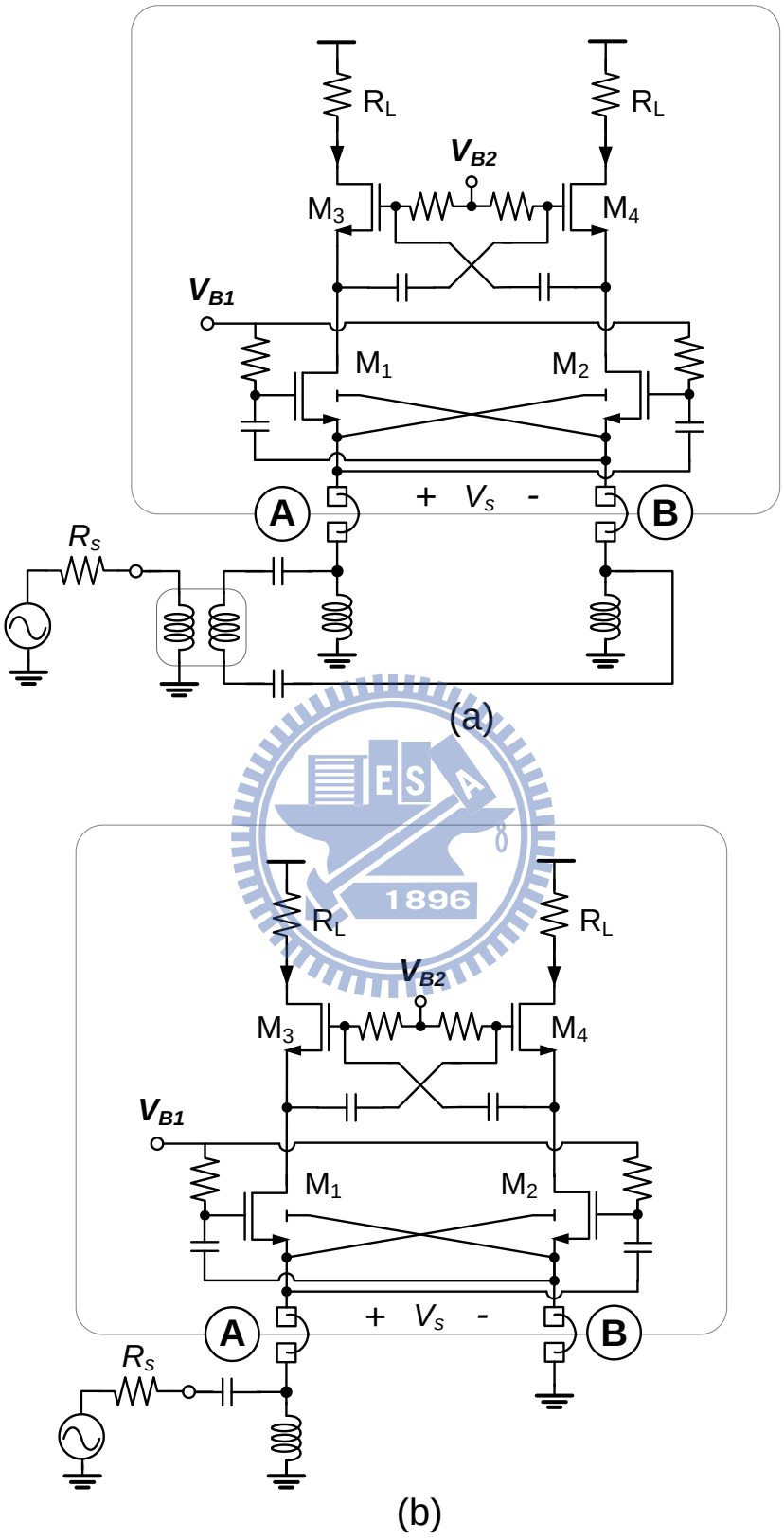


Fig. 4.7 The proposed LNA configurations: (a) in the differential receiving mode; (b) in the single-ended receiving mode.

4.4 Circuit Implementation

The schematic of the proposed LNA core is shown within the dashed box in Fig. 4.7. It is realized with a symmetric structure, using identical device dimensions as well as bias conditions between the two branches. Different from the conventional topology, an extra *bulk cross-coupling (BCC)* technique is applied to the input stage, in addition to the cascode CMR buffer. The body source cross-coupled configuration successfully incorporates an extra bulk-driven transconductor [42] into the conventional gate-driven one. The input transconductance thus boosts from g_{m1} to $g_{m1}+g_{mb1}$ without consuming extra dc current. An extra 20% increase is thus obtained due to the BCC in this design. Actually, the increase of voltage gain without relying on more current dissipation or larger load resistors helps mitigate the problem of insufficient voltage headroom. Most of all, the boosted input transconductance can increase voltage gain and reduce noise figure.

4.4.1 Differential Receiving Mode

As the LNA selectively operates in the differential receiving mode, both the source nodes of M_1 and M_2 are connected to the ground through external RF chock (RFC) inductors for DC current sink as shown in Fig. 4.7(a). Also, the source nodes of M_1 and M_2 as the input ports receive a differential signal from an off-chip balun. This circuit has a basic operation similar to the CCC CG-LNA. The voltage gain and input impedance are the same as respectively given in (4.1) and (4.2), in which g_{m1} should be replaced with $g_{m1}+g_{mb1}$ due to the BCC technique. Similarly, the overall noise factor can be derived as

$$F = 1 + \frac{2}{G_m R_s} \cdot \frac{g_m}{G_m} \cdot \frac{\gamma}{\alpha} + \left(\frac{1}{G_m R_s} + \frac{1}{2} \right)^2 \cdot \frac{2R_s}{R_L} \quad . \tag{4.13}$$

where g_m represents the transconductance of M_1/M_2, and G_m is equal to $2(g_{m1}+g_{mb1})$. In (4.13), the second term denotes the contribution from M_1/M_2, and the final term represents the contribution of the load resistors. Beneficial from the BCC, the noise factor contributed by M_1/M_2 is reduced by a factor of $g_m/(g_m+g_{mb})$, or 18% in this design if compared to that of the existing CCC CG-LNA. As can be found in

(4.13), the higher the G_m is, the lower the NF is. However, this might cause significant input impedance mismatch if the G_m is too high. In this work G_m of 50mS, i.e., g_m=20mS and g_{mb}=5mS, is chosen to trade-off the NF and the input return loss. This achieves an NF of 1.9dB while maintaining an S_{11} under -19dB, assuming $\gamma/\alpha=1$ and R_L=400Ω. As to the CMRR in this configuration, it can be expressed by $A_{I,dm}/A_{I,cm}$ from (4.4) and (4.5), in which g_{di} should be replaced with $g_{d1}/(1+g_{m1}R_S)$ due to the effect of Rs degeneration at M1 source node.

4.4.2 Single-ended receiving mode

As the LNA selectively operates in the single-ended receiving mode, the complete circuit configuration is shown in Fig. 4.7(b). As can be seen, M_1 constructs a CG amplifier by connecting its source node to ground through an external RFC inductor. On the other hand, M_2 constructs a common-source (CS) amplifier by shortening its source node to the ground. The LNA has a basic operation similar to the conventional Balun LNA. It also features a voltage gain and input impedance as respectively given in (4.1) and (4.2), in which g_{m1} should be substituted with $g_{m1}+g_{mb1}$ due to the BCC as well. Nevertheless, the cascode CMR buffer increases common-mode signal rejection and strengths the reverse isolation. It not only reserves primary advantages but also further improves performance in terms of NF, linearity, and differential balance.

NF derivation of the complete circuit is much complicated than that of the conventional Balun LNA due to the cross-coupling configuration of the CMR buffer. Assume only the thermal noise of transistors and resistors are taken into account and denote $\overline{i_{n,M}^2}$ and $\overline{i_{n,R}^2}$ with $4kT(\gamma/\alpha)g_m$ and $4kT/R$. The overall noise factor can be calculated by the ratio of the total output noise power referring to the source noise power, and given by

$$F = 1 + \frac{g_{m1}R_s}{\left|T_{i,R_s}\right|^2}\left\{\left(\frac{\gamma}{\alpha}\right)\cdot\left[\left(\left|T_{i,M1}\right|^2 + \left|T_{i,M2}\right|^2\right) + \frac{g_{m3}}{g_{m1}}\left(\left|T_{i,M3}\right|^2 + \left|T_{i,M4}\right|^2\right)\right] + \frac{2}{g_{m1}R_L}\right\} \quad . \tag{4.14}$$

where $T_{i,M1}$–$T_{i,M4}$ denote the current transfer gain in the differential output due to

M_1–M_4 transistor noise current, respectively, and $T_{i,Rs}$ represents the transfer gain of R_s noise current.

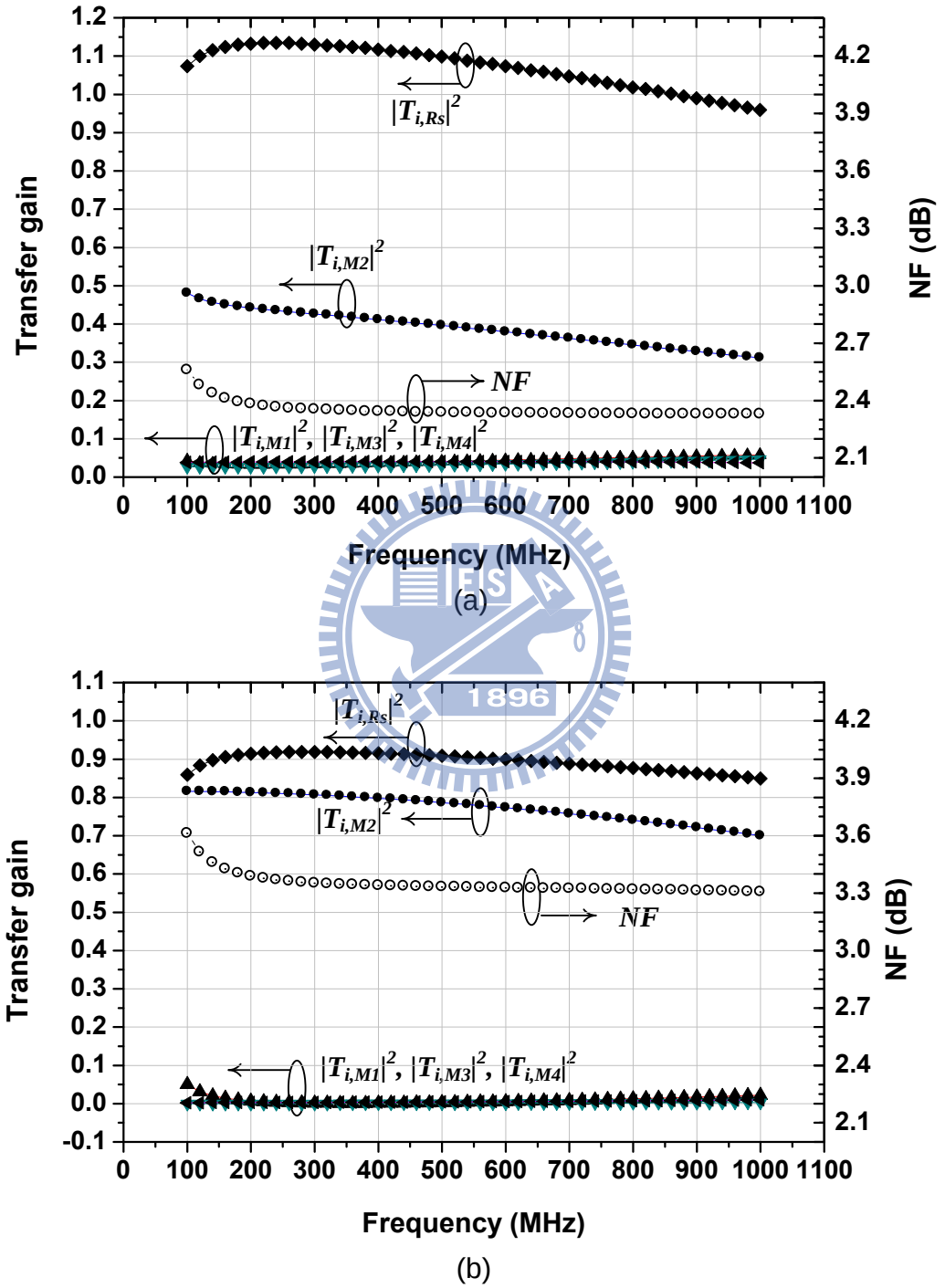


Fig. 4.8 Simulated noise transfer gain and overall NF in (a) the proposed LNA, (b) the conventional Balun LNA.

Fig. 4.8 illustrates the simulated transfer gain of main noise sources as well as the overall noise figure in our designed LNA with no simplification. The conventional balun LNA without the BCC and CMR is also explored for comparison. As can be seen, the proposed LNA has a higher gain with a higher $|T_{i,Rs}|^2$, while a much lower noise contribution from M_2. This leads to a better NF, 1dB lower than the conventional LNA.

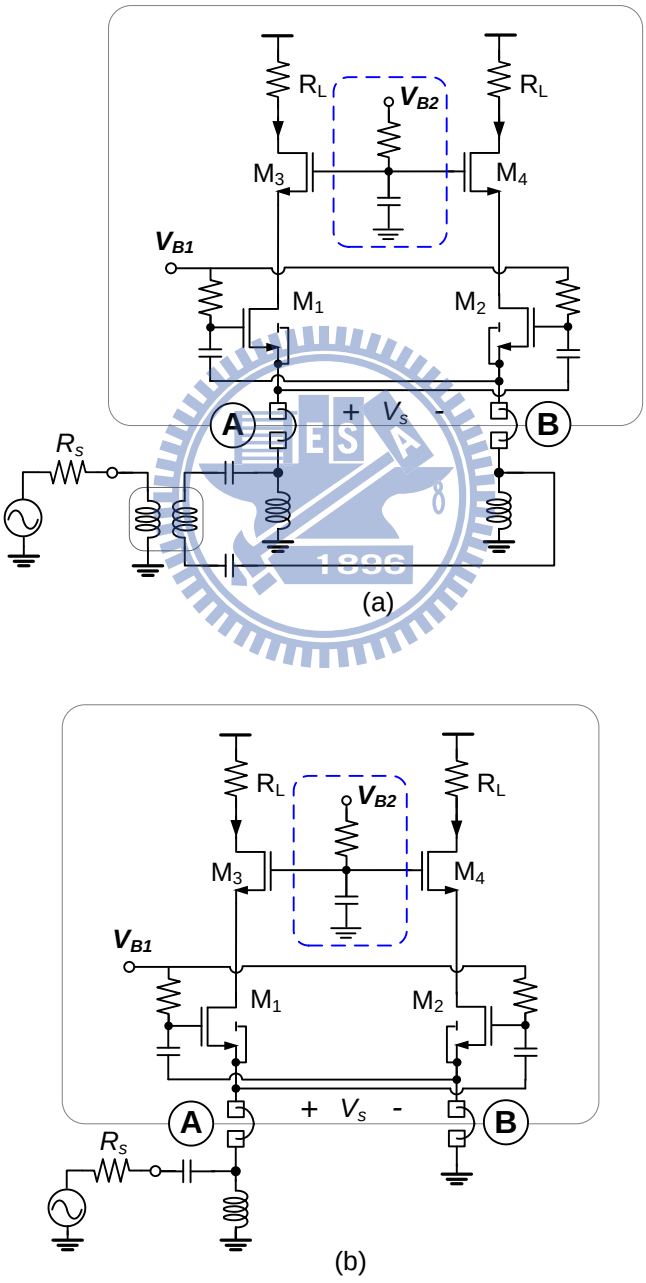


Fig. 4.9 The conventional LNA configurations: (a) in the differential receiving mode; (b) in the single-ended receiving mode

4.5 Measurement Results

The proposed reconfigurable LNA topology was implemented in a 0.13μm CMOS technology for sub 1-GHz applications such as DVB-T/H. To validate the effect of the proposed CMR buffer and BCC technique, five test-kits were implemented for comparison. As shown in Fig. 4.9, the conventional LNA utilizes a CG current buffer and has no bulk cross-coupling configuration. All test-kits duplicate identical device sizes and bias conditions for a fairly comparable basis. The die microphotograph is shown in Fig. 4.10. Each test-kit occupies an area of 300 × 700 μm^2, but the LNA core excluding the test buffer is only 200 × 300 μm^2 including the MIM capacitors.

The measurement of the LNA chip is performed by bonding the chip on a board. External RFC inductors of 100nH are used for DC bias in both configurations as shown in Fig. 4.11. Since the test buffer is difficult to de-embed accurately, all the measurement results include the effect of the test buffer except the item of voltage gain.

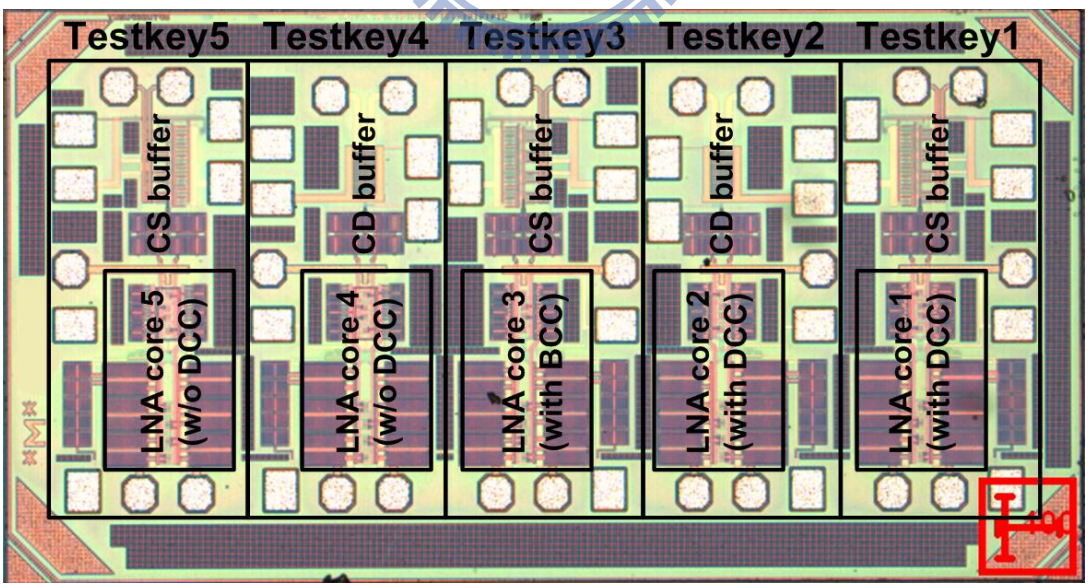


Fig. 4.10 Die micrograph of the fabricated LNA.

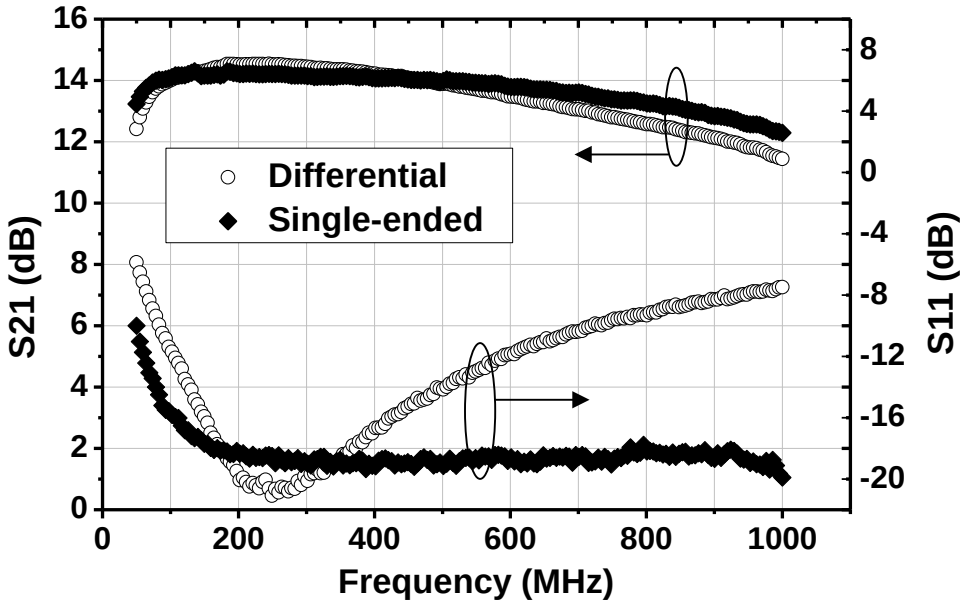


Fig. 4.11 The measured S-parameters in the differential and signle-ended configurations.

The S-parameters are measured using a 4-port network analyzer. In the differential configuration, an external balun with a turn ratio of *1:1* is required to match the input port to 50Ω. In other words, the same test setup with a single-ended input to a differential output is performed for the S-parameters measurement, regardless of differential or single-ended configuration. As shown in Fig. 10, the S_{11} is below -16 dB from 100 MHz to 1 GHz in single-ended mode, while -8 dB in differential mode due to the effect of the non-ideal external balun. The measured single-ended input to differential output S-parameter gain S_{ds21} is 14.3-12.3 dB in single-ended mode, while 14.5-11.5 dB after subtracting the balun loss in differential mode. These results respectively refer to voltage gain of 23±1 dB and 22.5±1.5 dB after de-embedding the effect of the test buffers based on the simulation results. The gain roll-off at lower frequencies is caused by the load effect of the input source inductance, while at higher frequencies due to the capacitive parasitics at the output loads of the LNA core.

The measured NF is illustrated in Fig. 4.12. Across the band of interests, the proposed LNA achieves an average NF of 2.65dB in single-ended mode, while 2.5dB

in differential mode. Without the CMR buffer and the BCC technique, the conventional LNA has an average NF of 3.9dB in single-ended mode, while 3.1dB in differential mode. The measurement results show that the proposed techniques improve the overall NF by 1.2dB and 0.6dB in the single-ended and differential configuration, respectively.

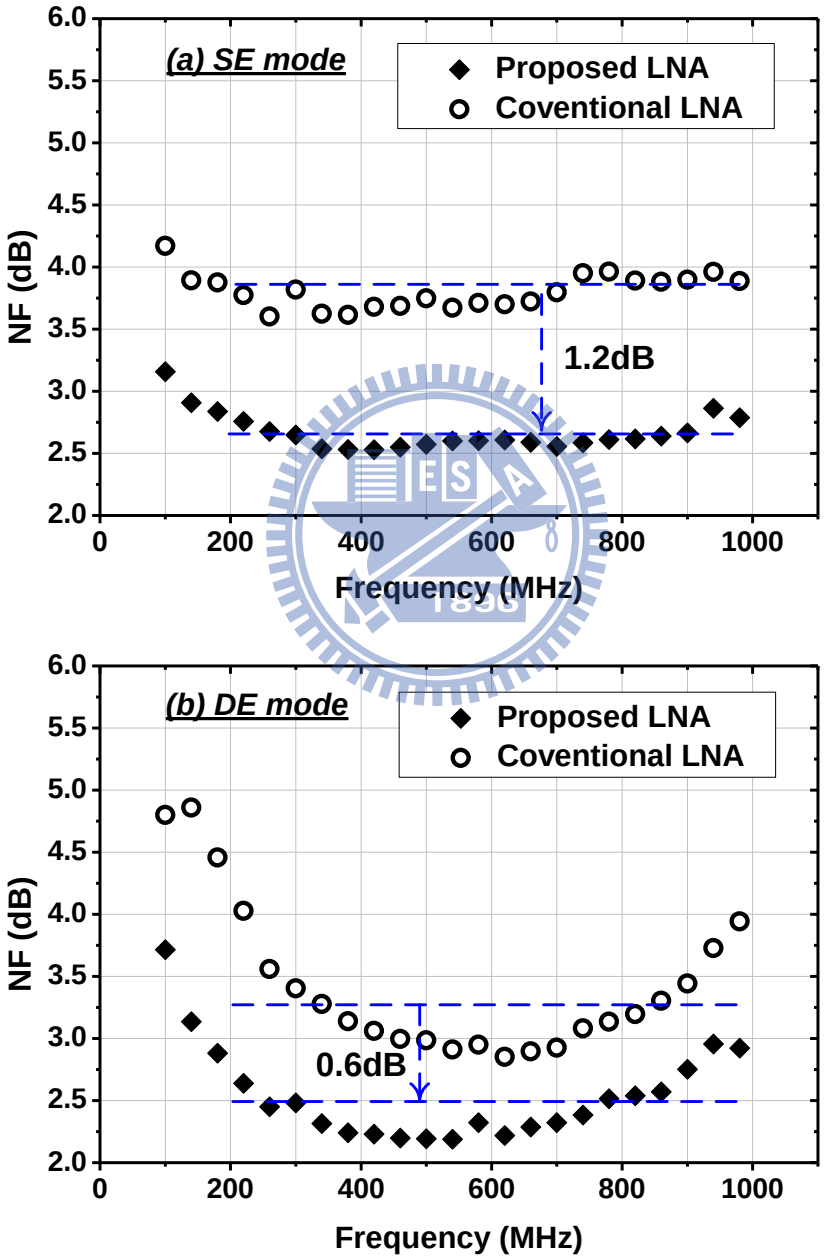


Fig. 4.12 The measured NF of the proposed LNA and of the conventional LNA in (a) the single-ended (SE) configuration, and (b) the differential (DE) configuration.

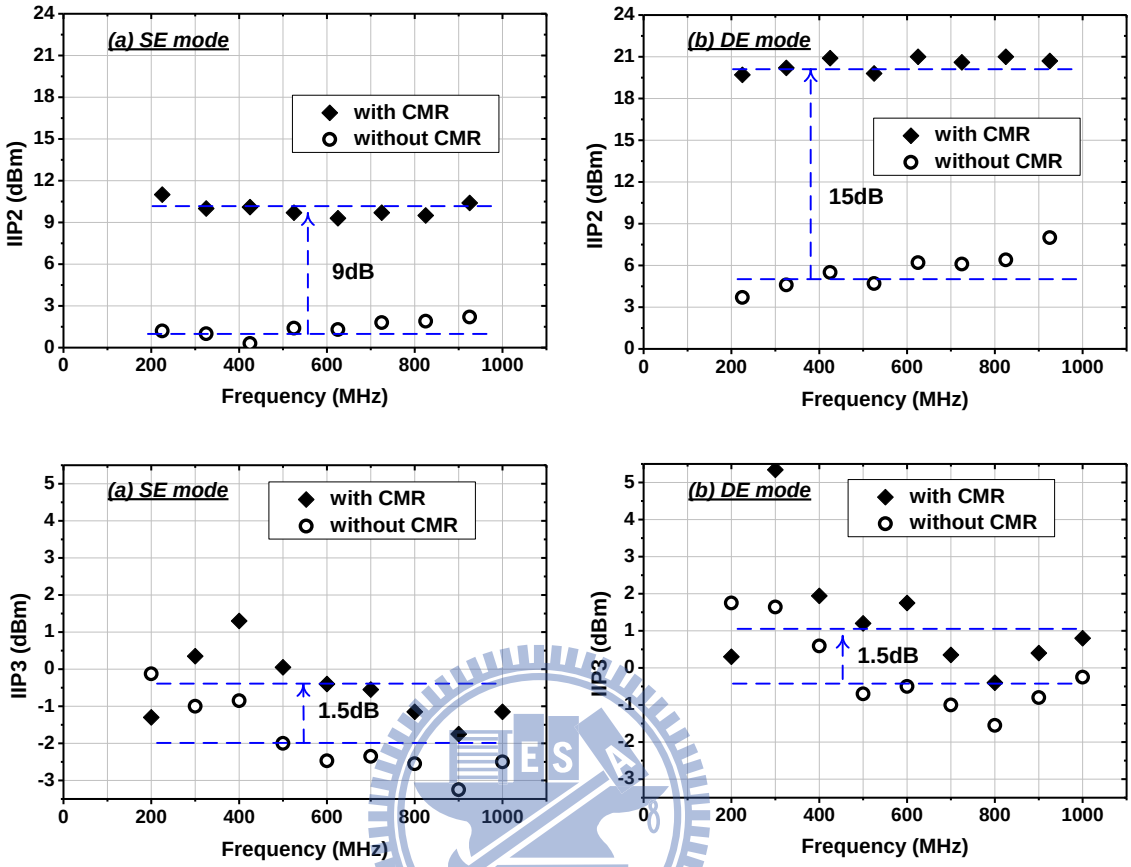


Fig. 4.13 The measured IIP2 and IIP3 of the proposed LNA and of the conventional LNA in (a) the single-ended (SE) configuration, and (b) the differential (DE) configuration.

Fig. 4.13 shows the measured IIP2 and IIP3. The IIP2 was measured by applying two tones with 210 MHz spacing and measuring the spur at their difference frequency. The measurement results show that the proposed LNA achieves an IIP2 of +10dBm and +20dBm, respectively, in the single-ended and differential configuration. On the other hand, the LNA using a conventional CG buffer rather than the CMR buffer has an IIP2 of +1dBm/+5dBm in the single-ended/differential configuration, respectively. As expected, the proposed CMR buffer benefits the second-order harmonic rejection and improves IIP2 over 9dB. As to the IIP3, it was measured by applying two tones with 2-MHz spacing. As can be seen, the proposed LNA achieves an IIP3 of -0.5dBm/+1dBm in the single-ended/differential

configuration. Without the proposed CMR buffer, nevertheless, the respectively measured IIP3 is -2dBm/-0.5dBm. The measurement shows that an extra improvement of 1.5dB IIP3 is achieved due to the CMR buffer.

Table 4.1 summarizes the measured performance of the proposed LNA. The summary table also presents the comparisons with the recently reported wideband noise-canceling LNAs [43], [44]. It is shown that the implemented LNA has the features: low power consumption, high voltage gain, low noise figure, moderate linearity, and small chip area, irrespective of single-ended or differential configuration.

Table 4.1 PERFORMANCE COMPARISON

Ref.	This Work		[14] JSSC '08	[12] JSSC '04	[18] ISSCC '09	[19] JSSC '09
Architecture	Balun	Differential	Balun	SE	Differential	SE
Freq. [GHz]	0.1—1	0.1—1	0.2—5.2	0.2—2	0.3—0.92	0.05—1
A_v Gain [dB]	22—24	22—23.5	13—15.6	10—14	18—21	N/A
S21 [dB]	14.3	14.5	6.6	10-14	N/A	14
NF [dB]	2.5—2.9	2.2—2.9	2.8—3.5	1.9—2.4	3 *	3.0—3.3
IIP3 [dBm]	-0.5	+1	0	0	-3.2	+3
S11 [dB]	< -10	< -8	< -10	-8	-10	< -9
Supply [V]	1.2	1.2	1.2	2.5	1.8	2.2
Power [mW]	3	3	14	35	3.6	35
Technology	0.13µm	0.13µm	65nm	0.25µm	0.18µm	0.18µm
Area [mm^2]	0.06	0.06	0.009	0.075	0.33 **	0.16

4.6 Conclusion

A wideband LNA which can operate as either a differential or single-ended configuration is introduced. The input re-configurability provides high flexibility in developing different positioning products, possibly sensitive to low cost/area or high performance. The applied BCC technique enhances the effective transconductance without consuming extra current consumption, achieving higher gain and lower NF. In addition, the proposed CMR buffer effectively improves circuit's CMRR, suppressing the second-order harmonic distortion. A better IIP2, IIP3, and NF are thus obtained. Overall, the LNA achieves wideband impedance match, high voltage gain, and low NF with low power consumption, regardless whether the input stage is selected to operate in the differential or single-ended configuration.

4.7 Appendix I – Circuit Analysis

The proposed CMR buffer in Fig. 4.5(c) can be analyzed from its simplified equivalent schematic as shown in Fig. 4.14. By modeling each input transconductor as a current source in parallel to its equivalent output impedance, the input and output currents can be related by a transfer matrix:

$$\begin{bmatrix} i_{o1} \\ i_{o2} \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \frac{1}{I} \cdot \begin{bmatrix} I_{11} & I_{12} \\ I_{21} & I_{22} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \tag{4.15}$$

where T_{ij} denotes the current transfer function from the *j-th* input (i_j) to the *i-th* output (i_{oi}), and is derived as

$$I_{11} = (1 + g_{d4}R_{L2} + g_{d4}r_{o2})(g_{m3}r_{o1} + g_{d3}r_{o1}) + g_{m4}g_{d3}r_{o1}r_{o2}. \tag{4.16}$$

$$I_{12} = -g_{m3}r_{o2}(1 + g_{d4}R_{L2}). \tag{4.17}$$

$$I_{21} = -g_{m4}r_{o1}(1 + g_{d3}R_{L1}). \tag{4.18}$$

$$I_{22} = (1 + g_{d3}R_{L1} + g_{d3}r_{o1})(g_{m4}r_{o2} + g_{d4}r_{o2}) + g_{m3}g_{d4}r_{o1}r_{o2}. \tag{4.19}$$

$$I = (1 + g_{d4}R_{L2} + g_{d4}r_{o2})(1 + g_{d3}R_{L1} + g_{d3}r_{o1} + g_{m3}r_{o1}) + g_{m4}r_{o2}(1 + g_{d3}R_{L1} + g_{d3}r_{o1}). \tag{4.20}$$

In this case, r_{o1} and r_{o2} are equal to $1/g_{d1}$ and $1/g_{d2}$, respectively. As can be seen, the cascode CMR buffer transfers each input current to both of the output branches with opposite signs. Consider the case of a symmetric structure, e.g., $g_{m1}=g_{m2}=g_{mi}$, $r_{o1}=r_{o2}=1/g_{di}$, $g_{m3}=g_{m4}=g_{mc}$, $g_{d3}=g_{d4}=g_{dc}$, and $R_{L1}=R_{L2}=Z_L$. The CMR buffer then carries out a symmetric transfer function, i.e., $T_{11}=T_{22}$, and $T_{12}=T_{21}$.

As a differential signal is applied, i_{o1} and i_{o2} can be obtained from (4.15) by replacing i_1 and i_2 with $g_{mi}v_{in}$ and $-g_{mi}v_{in}$, respectively, leading to

$$\frac{i_{o1}}{g_{mi}v_{in}} = \frac{-i_{o2}}{g_{mi}v_{in}} = T_{11} + |T_{12}| = \frac{2g_{mc} + g_{dc}}{2g_{mc} + g_{dc} + g_{di} + g_{di}g_{dc}Z_L} \approx 1 - \frac{g_{di}}{2g_{mc}}. \tag{4.21}$$

The current gain is balanced and close to unity, similar to that using a conventional CG current buffer but with double transconductance.

If the input signal is in the common-mode, on the other hand, the current in the two output branches is largely decreased, both expressed as

$$\frac{i_{o1}}{g_{mi}v_{in}} = \frac{i_{o2}}{g_{mi}v_{in}} = T_{11} - |T_{12}| = \frac{g_{dc}}{g_{dc} + g_{di} + g_{di}g_{dc}Z_L}. \tag{4.22}$$

The CMR buffer achieves a smaller current gain than the conventional CG buffer. According to (4.21) and (4.22), the CMRR is enhanced by a factor of $(g_{dc}+g_{di})/g_{dc}$ if $g_{dc}Z_L<<1$. This characteristic benefits in differential balancing and common-mode signal rejection such as the second-order harmonic distortion due to input transistor nonlinearity.

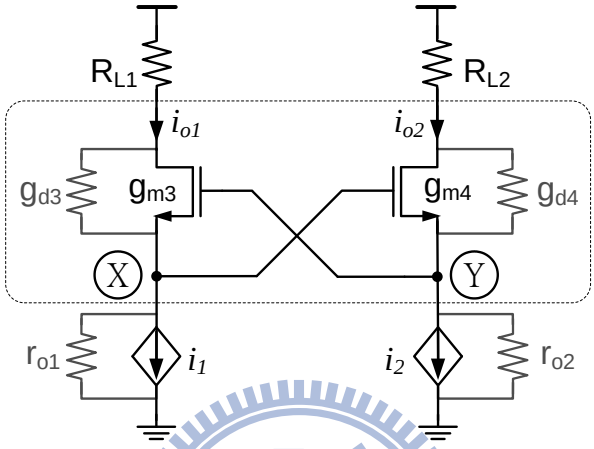


Fig. 4.14 Simplified equivalent circuit for the analysis of the proposed CMR buffer.

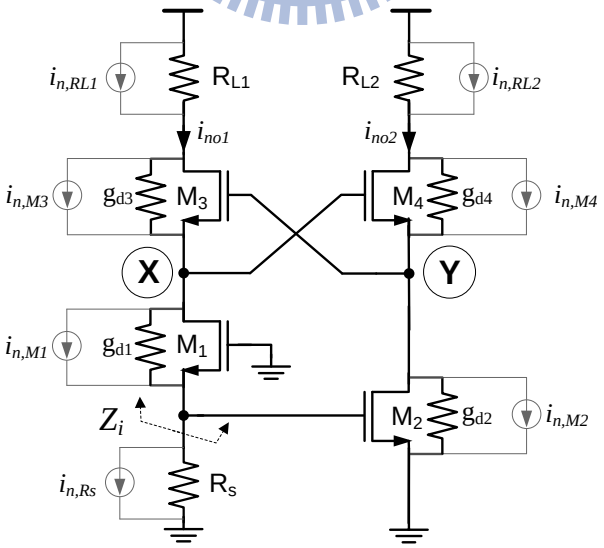


Fig. 4.15 The equivalent circuit for the analysis of the CG-CS amplifier in cascode with the CMR buffer, including the noise sources from each device.

4.7.1 CG-CS Amplifier in Cascode with a CMR Buffer

As mentioned earlier, the CMR buffer achieves an enhanced CMRR in the differential topology utilizing two CS amplifiers as the input stage. This buffer also appears to be effective to the hybrid CG-CS input stage that presents non-equal output impedance, i.e., $r_{o1} \neq r_{o2}$, as shown in Fig. 4.15. In this section, it will be shown that the CMR buffer benefits differential balancing, noise canceling, and distortions canceling in a CG-CS amplifier. The derivation assumes that the CG and CS branches have symmetric devices and bias, e.g., $g_{m1}=g_{m2}$ and $g_{m3}=g_{m4}$. For the purpose of numerical analysis, the design parameters listed as follows are used. The transistors in use have an intrinsic gain around 22.5, i.e., $g_{m1}/g_{d1}=g_{m3}/g_{d3}=22.5$. The other parameters are $g_{m3}=0.8\times g_{m1}$, and $R_{L1}=R_{L2}=400\Omega$.

4.7.1.1 Differential Balancing

The significance of the CMR buffer is examined numerically. First we inspect signal balance by (4.15) in the case of the same input currents ($i_1=i_2$) but non-equal transconductor output impedances ($r_{o1} \neq r_{o2}$). With aforementioned design parameters and making $g_{m3}=g_{m4}$ =20mS, the two output currents i_{o1} and i_{o2} are calculated and normalized, and plotted as the functions of r_{o1} and r_{o2} in the contour plots shown in Fig. 4.16. As can be seen, the normalized output currents in the two branches are still almost balanced and close to unity even though r_{o1} is significantly different from r_{o2}. Also, the differential current gain in this case is similar to that in a conventional case using a conventional CG current buffer with a double transconductance.

Next we examine the case with additional imbalance from the drain currents i_1 and i_2. By replacing i_1 and i_2 with $1\angle 0^\circ$ and $(1+\varepsilon)\angle(180+\theta)^\circ$, where ε and θ represent the input differential amplitude and phase mismatch, respectively, we can verify differential balance improvement in this asymmetric configuration by (4.15). Fig. 4.17 plots the current mismatch between i_{o1} and i_{o2} by sweeping r_{o1} and r_{o2}. Fig. 4.17(a) and Fig. 4.17(b) respectively depicts the contour plot of output amplitude and phase mismatch by introducing an input mismatch of ε=0.2 and θ=20°. The results show that the CMR buffer still benefits the differential balance even though the circuit topology is not fully symmetric. The smaller the r_{o1} and r_{o2} are, the better the

differential balancing is. However, this benefit comes from the tradeoff to the gain loss.

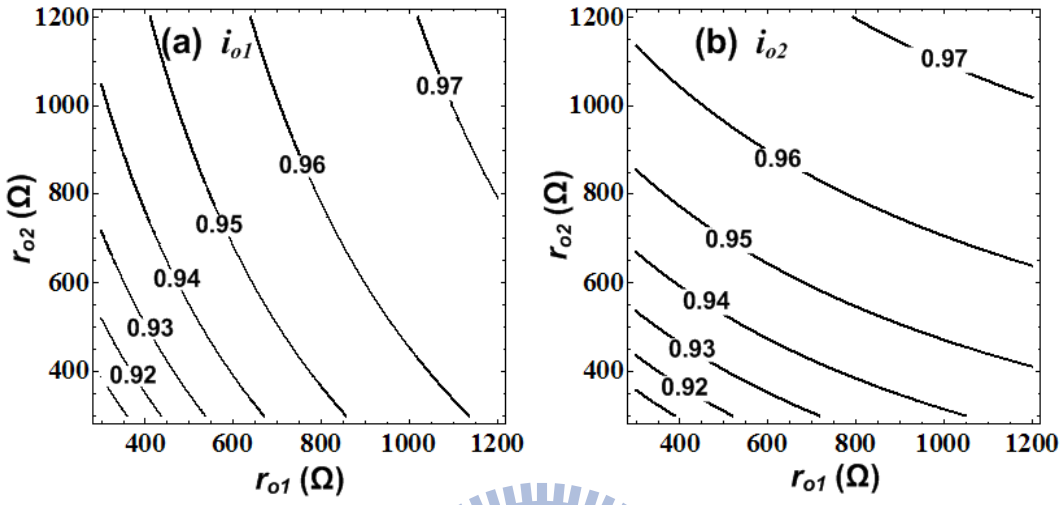


Fig. 4.16 Contour plots of normalized (a) i_{o1} and (b) i_{o2} as the functions of r_{o1} and r_{o2}.

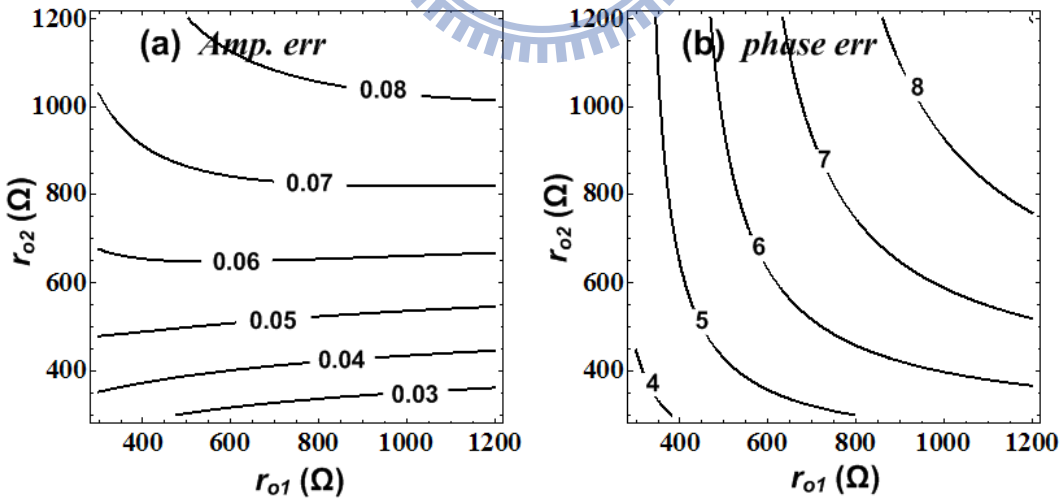


Fig. 4.17 Contour plot of differential output mismatch by sweeping r_{o1} and r_{o2} with input mismatch of ε=0.2 and θ=20°: (a) amplitude mismatch, and (b) phase mismatch.

4.7.1.2 Noise Canceling

As the CMR buffer is in cascode of the CG-CS input stage, the coupling configuration results in a negative feed-forward path to improve NF performance. This advantage can be analyzed form the simplified schematic as shown in Fig. 4.15. All transistor noise sources such as the channel thermal noise and the gate induced noise are modeled as a noise current source across the drain-source terminals of the transistor.

The overall noise factor can be calculated by the ratio of the total output noise power referring to the source noise power, and given by

$$F = 1 + \frac{\overline{i_{n,M1}^2}\left|T_{i,M1}\right|^2 + \overline{i_{n,M2}^2}\left|T_{i,M2}\right|^2 + \overline{i_{n,M3}^2}\left|T_{i,M3}\right|^2 + \overline{i_{n,M4}^2}\left|T_{i,M4}\right|^2 + \overline{i_{n,RL1}{}^2} + \overline{i_{n,RL2}{}^2}}{\overline{i_{n,Rs}^2}\left|T_{i,Rs}\right|^2}. \quad (4.23)$$

In (4.23), $T_{i,M1}-T_{i,M4}$ denote the current transfer gain in the differential output due to M_1-M_4 transistor noise current, respectively, and $T_{i,Rs}$ represents the transfer gain of R_s noise current. To simplify the calculation, only the thermal noise of the transistors and of the resistors is taken into account assuming that M_1-M_4 have an identical excess noise factor, (γ/α). Substituting $\overline{i_{n,M}^2}$ and $\overline{i_{n,R}^2}$ with $4kT(\gamma/\alpha)g_m$ and $4kT/R$ into (4.23), the overall noise factor is rewritten as

$$F = 1 + \frac{1}{\left|T_{i,R_s}\right|^2}\left\{\left(\frac{\gamma}{\alpha}\right)\cdot\left[g_{m1}R_s\left(\left|T_{i,M1}\right|^2 + \left|T_{i,M2}\right|^2\right) + g_{m3}R_s\left(\left|T_{i,M3}\right|^2 + \left|T_{i,M4}\right|^2\right)\right] + \frac{2R_s}{R_L}\right\}. \quad (4.24)$$

For the derivation of $T_{i,Rs}$, it is obvious that the noise current $i_{n,Rs}$ generates differential output at X and Y nodes. The impedance looking into the CMR buffer therefore responds to this differential noise current to be low, and the effect of g_{d1} is negligible. The transfer function of $i_{n,Rs}$ is thus derived as

$$T_{i,Rs} = A_{I1}\cdot\frac{g_{m1}R_s}{1+g_{m1}R_s} + A_{I2}\cdot\frac{g_{m2}R_s}{1+g_{m1}R_s}. \quad (4.25)$$

where A_{I1} and A_{I2} represent the contributions from each input current to the differential output current, equal to $(T_{11}-T_{21})$ and $(T_{22}-T_{12})$, respectively, referring to (4.15).

As to $T_{i,M1}-T_{i,M4}$, the derivation is more complicated because all noise sources

$i_{n,M1\text{-}4}$ effectively generate noise currents containing the common-mode significantly driving into the CMR buffer. In general, Kirchhoff's Law can be performed to obtain all four transfer gains, but the derived expressions are too complex to give direct insights for LNA design. Instead, the output impedance r_{o1} and r_{o2} are pursued. Theoretically the values of r_{o1} and r_{o2} are not all the same in each noise source analysis due to the coupling between M_1 and M_2. Fortunately, in response to these four noise sources, r_{o1} and r_{o2} can be approximately expressed, respectively, as

$$r_{o1} \approx \frac{1}{g_{d1}} \cdot \left[1 + g_{m1} R_s\right]. \tag{4.26}$$

$$r_{o2} \approx \frac{1}{g_{d2}} \cdot \frac{1}{1 + \frac{g_{d1}}{g_{d2}} \left(\frac{g_{m2} R_s}{1 + g_{m1} R_s} \right)}. \tag{4.27}$$

Note that the ratio of r_{o1} to r_{o2} is approximate to $1+2g_{m1}R_s$ if the two branches have symmetric devices and bias.

The transfer gains for $i_{n,M1}$ and $i_{n,M2}$ can be derived by the transfer matrix function in (4.15) with effective input current as follows. The noise current $i_{n,M2}$ of M_2 results in effective current of the same amount as i_2 driving to the buffer, referring to Fig. 4.14. The transfer gain $T_{i,M2}$ is thus obtained from (4.15) by replacing i_1 and i_2 with 0 and $i_{n,M2}$, respectively, leading to

$$T_{i,M2} = \frac{i_{o1} - i_{o2}}{i_{n,M2}} = A_{I2} = T_{22} - T_{12}. \tag{4.28}$$

Differently, M_1 channel noise $i_{n,M1}$ results in the noise currents i_{nd1} and i_{nd2} at the drain ports of M_1 and M_2, respectively, derived as

$$i_{nd1} = \frac{1}{1 + g_{m1} R_s} \cdot i_{n,M1}. \tag{4.29}$$

$$i_{nd2} = g_{m2} \cdot i_{nd1} R_s = \frac{g_{m2} R_s}{1 + g_{m1} R_s} \cdot i_{n,M1}. \tag{4.30}$$

Note that these two currents are of the same sign. Thus, the transfer function of $i_{n,M1}$ can be derived from (4.15) by replacing i_1 and i_2 with i_{nd1} and i_{nd2}, respectively, as (4.31)

$$T_{i,M1} = \frac{i_{o1} - i_{o2}}{i_{n,M1}} = A_{I1} \cdot \frac{1}{1 + g_{m1} R_s} - A_{I2} \cdot \frac{g_{m2} R_s}{1 + g_{m1} R_s}. \tag{4.31}$$

Similarly, the transfer gains of $i_{n,M3}$ and $i_{n,M4}$ can be derived as

$$T_{id,M3} = \frac{(1+g_{m4}r_{o2}+g_{d4}r_{o2}+g_{d4}R_{L2})-g_{m4}r_{o1}}{I}. \tag{4.32}$$

$$T_{id,M4} = \frac{(1+g_{m3}r_{o1}+g_{d3}r_{o1}+g_{d3}R_{L1})-g_{m3}r_{o2}}{I}. \tag{4.33}$$

where I is a shorthand notation as in (4.20).

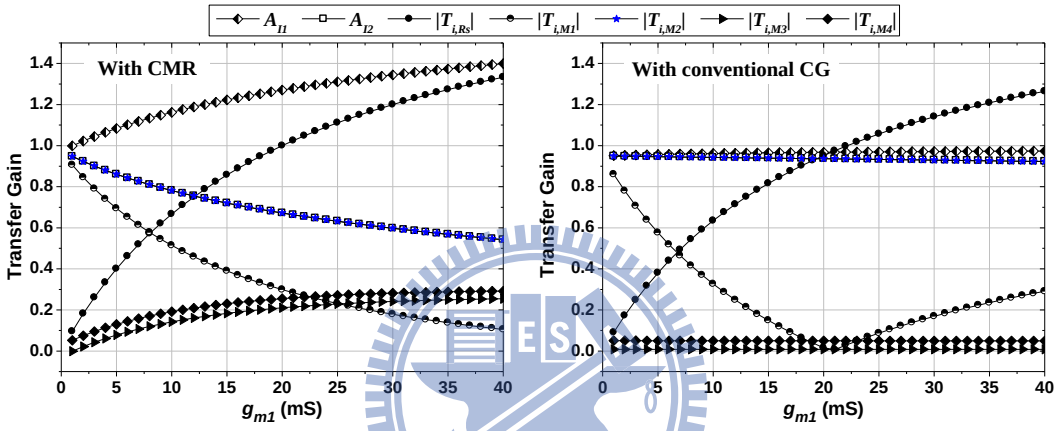


Fig. 4.18 A_{I1}/A_{I2} and transfer gains of M_1—M_4 channel noise and R_s noise currents by sweeping g_{m1} for two cases with the CMR or the conventional CG buffer.

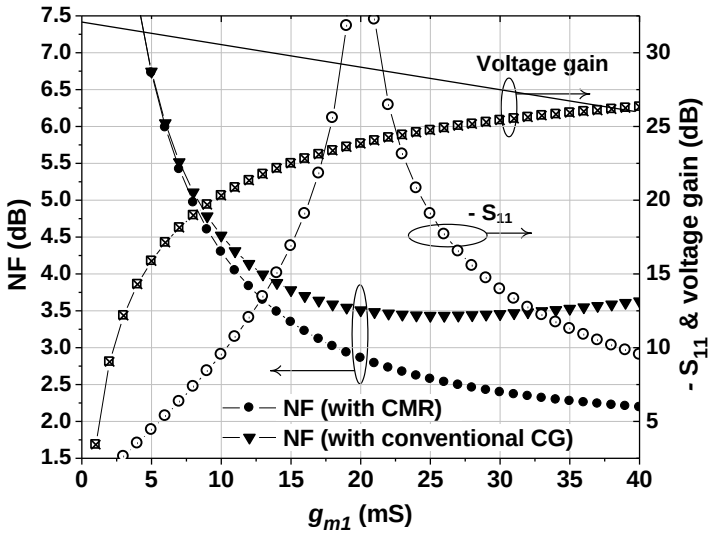


Fig. 4.19 The calculated NF, voltage gain, and S_{11} versus g_{m1}.

Fig. 4.18 illustrates all the noise transfer gains and A_{I1}/A_{I2} versus g_{m1}. Two circuits with the same design parameters but respectively using the CMR or the conventional CG buffer are explored for comparison. The design parameters in use are the same as that listed in the beginning of Section III. In the case using the CMR buffer, the higher the g_{m1} is, the higher the ratio of r_{o1} to r_{o2} is. Then A_{I1} becomes much larger than A_{I2}. Also both $T_{i,M1}$ and $T_{i,M2}$ decrease, while both $T_{i,M3}$ and $T_{i,M4}$ increase. However, in the case using the conventional CG buffer, $T_{i,M1}$, approaches to a minimum of zero at g_{m1} of 20mS, while $T_{i,M2}$ keeps approximately at unity. Moreover, A_{I1} and A_{I2} are almost identical and close to unity, irrespective of g_{m1}. Comparing these two cases, we can find that at g_{m1} of 30mS the CMR case has $T_{i,M2}$ of 0.6, decreased by a ratio of 0.6 opposite to the conventional CG case. This indicates a considerable decrease of M_2 noise contribution by a ratio of 0.36. Fig. 4.19 illustrates the NF, voltage gain, and S_{11} sweep versus g_{m1} for the CMR case. The NF is calculated by (4.24) with $(\gamma/\alpha)=1$. At the same time, the NF for the conventional CG case is also plotted for comparison. As can be seen, the CMR case achieves a lower NF with a larger g_{m1}. However, this might degrade input impedance matching if the effective g_{m1} is too high. It is well known that the common-gate input amplifier constitute an input impedance of $1/g_{m1}$. If g_{m1} of 30mS is chosen, the LNA can achieve an NF of 2.4dB and a voltage gain of 25dB, while maintaining a safe margin on S_{11} below -13dB. The NF is reduced by 1dB due to the CMR buffer, in large part due to a considerable decrease of $T_{i,M2.}$

4.7.1.3 Distortion Canceling

Typically the linearity performance of a single-stage amplifier is limited by the input transconductor nonlinearity. For small signal operation, the drain-source currents of the CG and CS transconductors can be expressed as a power series in terms of the gate-source voltage. Since the LNA uses symmetric devices and bias in the two branches, both the CG and CS transconductors have almost the same transconductance coefficients. Thus, we can get

$$i_{ds,CG}(v_s) = g_m(-v_s) + \frac{g'_m}{2!}(-v_s)^2 + \frac{g''_m}{3!}(-v_s)^3. \quad (4.34)$$

$$i_{ds,CS}(v_s) = g_m(v_s) + \frac{g'_m}{2!}(v_s)^2 + \frac{g''_m}{3!}(v_s)^3. \quad (4.35)$$

where the weakly nonlinear behavior is assumed such that the nonlinearities of the order higher than three are negligible. Therefore, the small-signal nonlinear equivalent circuit of the input stage for distortion analysis is illustrated in Fig. 4.20, where i_{hd2} and i_{hd3} denote the second- and third-order distortion terms, respectively.

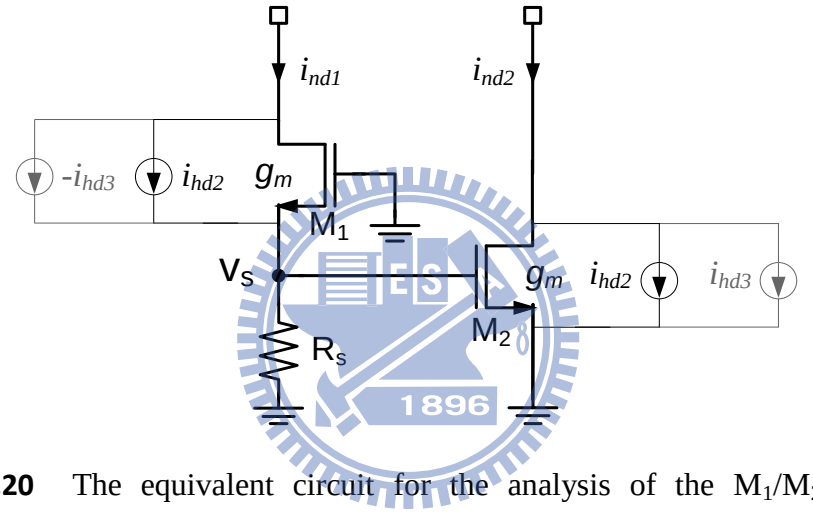


Fig. 4.20 The equivalent circuit for the analysis of the M_1/M_2 distortion currents.

Since the second-order distortion current generated by the CG and CS amplifiers are of the same sign, according to (4.29) – (4.31), its transfer function can be given by

$$T_{i,hd2} = A_{I1} \cdot \frac{1}{1+g_{m1}R_s} - A_{I2} \cdot \left(\frac{g_{m2}R_s}{1+g_{m1}R_s} + 1\right). \quad (4.36)$$

Nevertheless, the third-order distortion currents generated by the CG and CS amplifiers have opposite signs. The transfer function thus is given by

$$T_{i,hd3} = A_{I1} \cdot \frac{1}{1+g_{m1}R_s} - A_{I2} \cdot \left(\frac{g_{m2}R_s}{1+g_{m1}R_s} - 1\right). \quad (4.37)$$

Fig. 4.21 illustrates the transfer gains of the second- and the third-order distortion currents versus g_{m1}. As compared with the case using the conventional CG buffer, the CMR buffer greatly improves the second-order linearity performance but shows no effect on the third-order. As g_{m1} is 30mS, the transfer gain $T_{i,hd2}$ is suppressed from 1.2 to 0.42. This translates to an IIP2 improvement of 9dB based on the two-tone analysis.

It is worth mentioning that the second-order nonlinearity in a wideband amplifier is an important issue. The issue can be addressed in twofold. The second-order nonlinearity may directly cause any two interferers intermodulating and creating spurs at their sum and difference frequencies [45]. Once falling into the desired channel, the spurs will degrade the signal-to-noise level. Furthermore, in a two-stage cascaded amplifier the incoming fundamental and second-order harmonic tones which are generated by the first stage might be mixed via the second-order nonlinearity of the second stage, producing an extra third-order nonlinear product to the output [46], [47]. This cascade interaction may raise the third-order intermodulation distortion (IMD3), and deteriorate the overall IIP3.

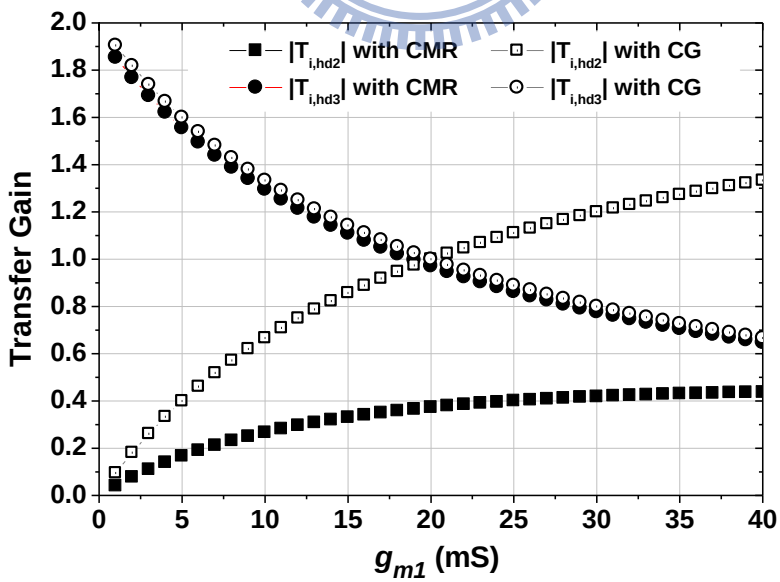


Fig. 4.21 The transfer gains of harmonic distortion currents with the CMR buffer or the conventional CG buffer.

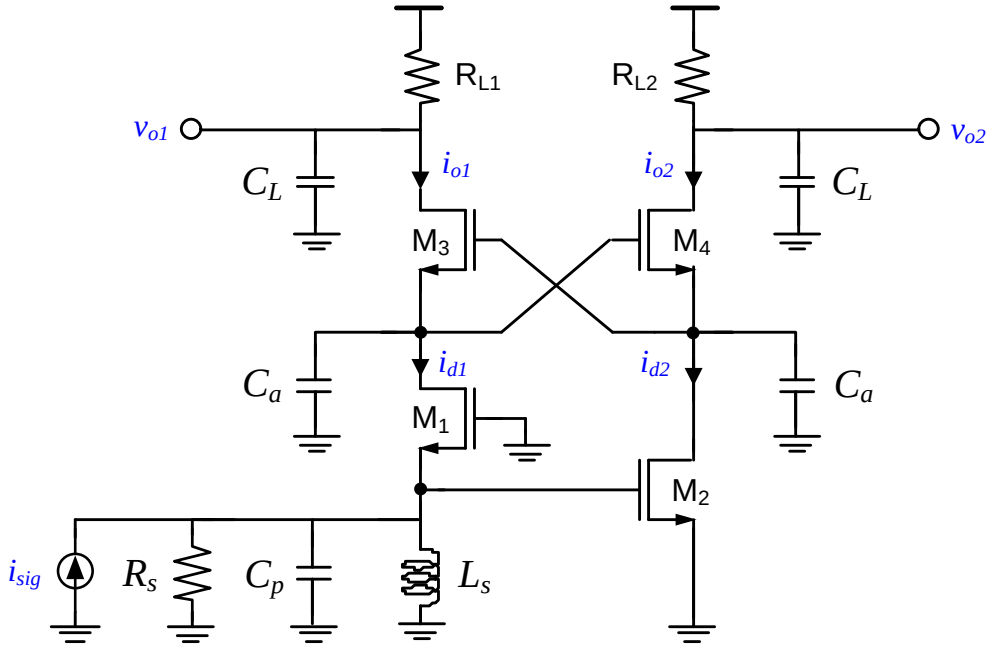


Fig. 4.22 Simplified schematic for the analysis of bandwidth limitation.

4.7.1.4 Bandwidth Limitation

Fig. 4.22 shows a simplified schematic of the proposed LNA for the analysis of bandwidth limitation. In the proposed version of Fig. 4.22 where a large bias inductor (*Ls*) is used, the transfer function of the LNA can be written as

$$\frac{v_{o1}}{i_{sig}}(s)=\frac{i_{d1}}{i_{sig}}(s)\times\frac{i_{o1}}{i_{d1}}(s)\times\frac{v_{o1}}{i_{o1}}(s)\,. \tag{4.38}$$

where the amplifier function is decomposed into three parts, the input transconductor, the cascode current buffer, and the output load. To simplify the analysis, the transistors' output resistance (r_{ds}) is ignored. Thus, the transfer function of the input stage can be derived as

$$\frac{i_{d1}}{i_{sig}}(s)\approx\frac{sL_s(g_{m1}R_s)-s^2(C_{ds1}L_sR_s)}{R_s+sL_s(1+g_{m1}R_s)+s^2(C_pL_sR_s)}, \tag{4.39}$$

$$\frac{i_{d2}}{i_{sig}}(s)\approx\frac{-sL_s(g_{m2}R_s)+s^2(C_{gd2}L_sR_s)}{R_s+sL_s(1+g_{m1}R_s)+s^2(C_pL_sR_s)}. \tag{4.40}$$

As can be seen, the input stage features a band-pass response and the two branches have a similar response except the non-dominant zero slightly different at relatively high frequency. The high-pass and low-pass corner frequency respectively is dominated by two poles derived as:

$$\omega_{pL} \approx \frac{R_s}{L_s(1+g_{m1}R_s)}; \tag{4.41}$$

$$\omega_{pH} \approx \frac{(1+g_{m1}R_s)}{R_sC_p} + \frac{R_s}{L_s(1+g_{m1}R_s)} \sim \frac{(1+g_{m1}R_s)}{R_sC_p}. \tag{4.42}$$

where C_p represents the total parasitic capacitance at the input port, including the parasitic capacitance of the ESD pad and external components, C_{gs1}, C_{sb1}, C_{gs2}, C_{gd2}, and etc. It is indicated that a large inductor allows for good performance in the lower frequency range. In the higher frequency range, the parasitic capacitance at the input port dominates.

On the other hand, both the cascode current buffer and the output load feature a low-pass response and can be expressed as:

$$\frac{i_{o1}}{i_{d1}}(s) \approx \frac{1}{1+\frac{s}{\omega_{p1}}}; \quad \omega_{p1} \approx \frac{2g_{m4}}{C_a}, \tag{4.43}$$

$$\frac{v_{o1}}{i_{o1}}(s) \approx \frac{R_L}{1+\frac{s}{\omega_{p2}}}; \quad \omega_{p2} \approx \frac{1}{R_LC_L}, \tag{4.44}$$

where C_a represents the total parasitic capacitance at the drain terminal of M_2 (or M_1), approximated to the sum of C_{gs3}, C_{gs4}, C_{d2}, and C_{s4}.

Assume two branches have symmetric device sizes. With g_{m1}=g_{m2}=20mS and R_L=400Ω, the balun LNA can achieve a voltage gain of 16, i.e., 24dB. However, the bandwidth associated with this high gain may be limited due to the dominant pole ω_{p2} at the LNA output. From (4.44), 0.1pF loading capacitance results in the 3 dB bandwidth limitation to 4GHz. On the other hand, another pole ω_{pH} at the input stage may also cause a significant effect on the bandwidth limitation. Since the parasitic capacitance C_p at the input port includes several components, such as the parasitic of the ESD pad (~250fF), C_{gs1}/C_{gs2} (~150fF), C_{gd1}/C_{gd2} (~100fF), and the parasitic capacitance of the external inductor (~300fF), this large C_p of 800fF may limit the bandwidth to 8GHz by (4.42).

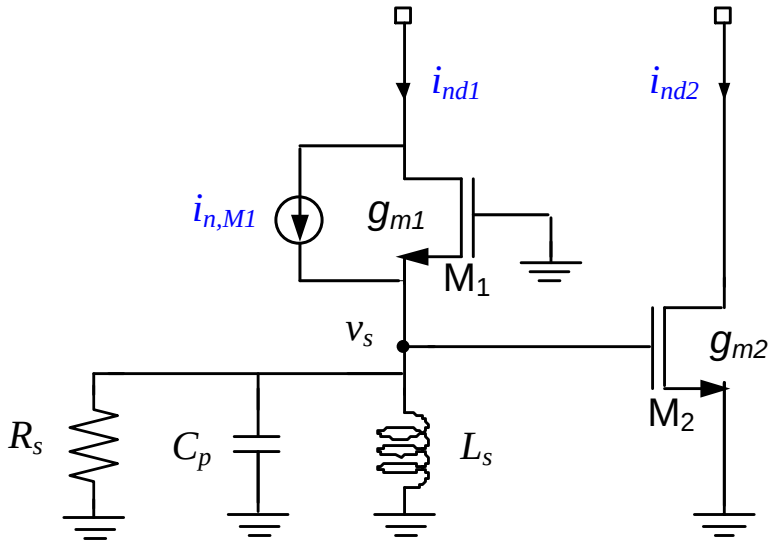


Fig. 4.23 Simplified schematic for exploring noise-canceling mechanism at high frequencies.

In addition to the effects on bandwidth limitation as well as impedance matching, the large parasitic capacitance C_p at the input port may also deteriorate the noise canceling mechanism at high frequencies. As aforementioned, the principle of noise-canceling LNA relies on phase and gain matching between the two branch outputs. Unfortunately, the parasitic C_p may cause significant gain and phase discrepancy at high frequencies. This effect can be observed from the simplified schematic shown in Fig. 4.23. As mentioned earlier and shown in Fig. 4.22, the cascode current buffer and the load feature the same response for the two branches. Thus, the input stage is mainly considered since it is the source which contributes to significant gain and phase discrepancy.

To explore the noise canceling mechanism of M_1, the transfer function is derived and expressed as

$$\frac{i_{nd1}}{i_{n.M1}}(s) \approx \frac{R_s + sL_s + s^2\left(C_p L_s R_s\right)}{R_s + sL_s\left(1 + g_{m1}R_s\right) + s^2\left(C_p L_s R_s\right)}. \tag{4.45}$$

$$\frac{i_{nd2}}{i_{n,M1}}(s) \approx \frac{-sL_s\left(g_{m2}R_s\right) + s^2\left(C_{gd2} L_s R_s\right)}{R_s + sL_s\left(1 + g_{m1}R_s\right) + s^2\left(C_p L_s R_s\right)}. \tag{4.46}$$

It is noted that (4.46) is the same as (4.40), and the poles in (4.45) and (4.46) are the same as that in (4.41) and (4.42). From (4.45), we can get two dominant zeroes at frequencies:

$$\omega_{zL} \approx \frac{R_s}{L_s} \quad ; \quad \omega_{zH} \approx \frac{1}{R_s C_p} \tag{4.47}$$

As can be found from (4.41), (4.42) and (4.47), ω_{zL} is double of ω_{pL} and ω_{zH} is half of ω_{pH}. With design parameters: g_{m1}=g_{m2}=20mS, Ls=100nH, C_p=800fF, C_{gd2}=75fF, and Rs=50Ω, Fig. 4.24 and Fig. 4.25 show the frequency response of $i_{n,M1}$ based on (4.45) an (4.46). A significant magnitude and phase discrepancy, which deteriorate the noise canceling mechanism, is observed at frequencies far away from the resonant frequency. To increase bandwidth and to maintain good noise performance in the high frequency range, a small parasitic capacitance C_p at the input port is critical.

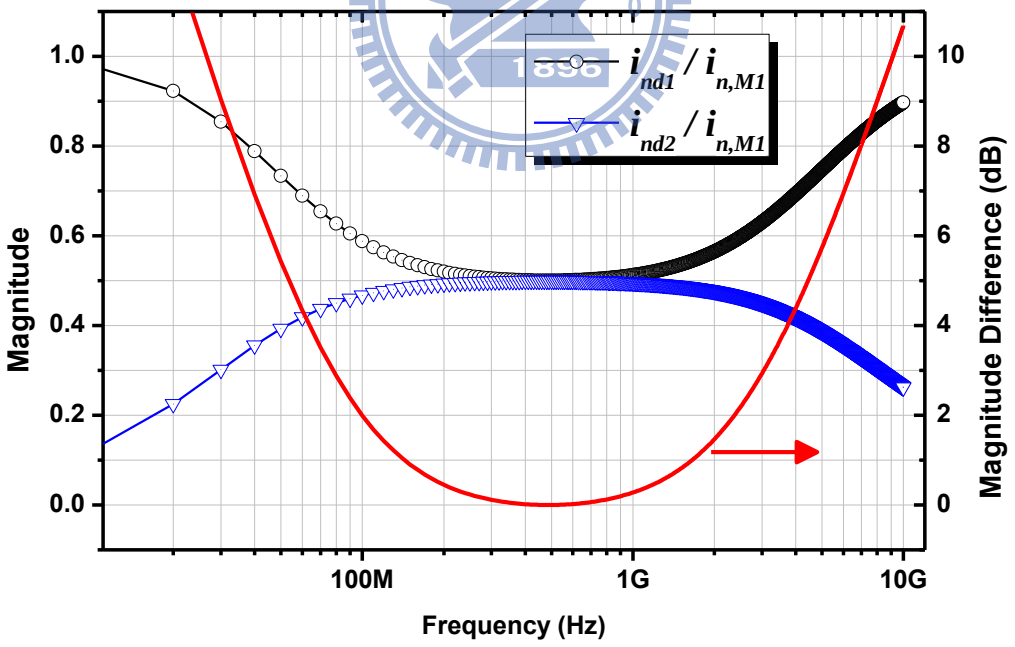


Fig. 4.24 Magnitude response of M_1 noise current.

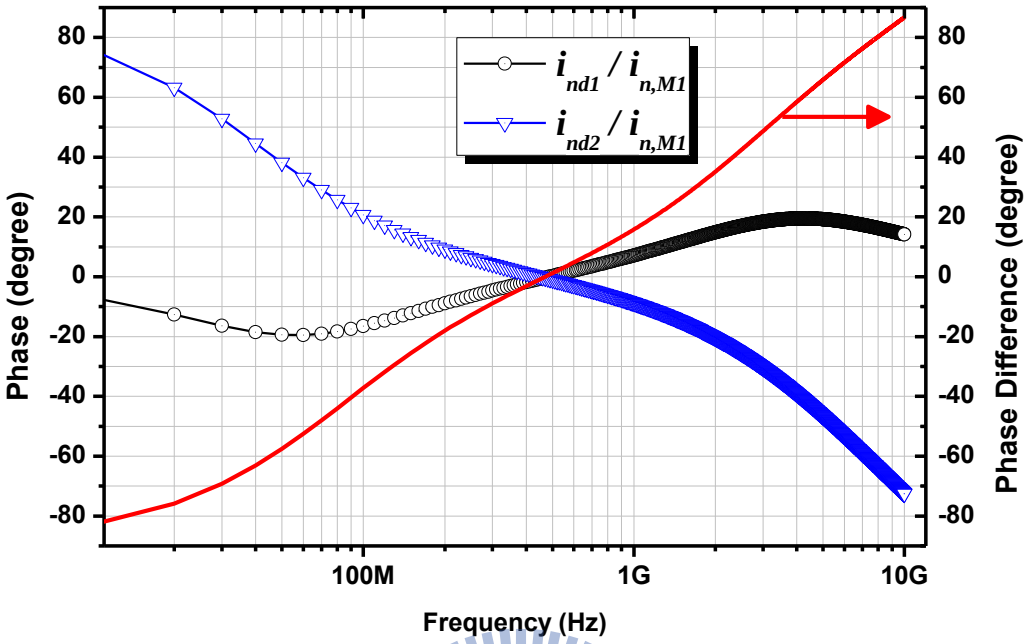


Fig. 4.25 Phase response of M_1 noise current.

4.7.2 Extended Measurement Results

Fig. 4.26 and Fig. 4.27 respectively illustrate the measured amplitude and phase imbalance between two output ports. The balun performance was characterized on 15 samples at a nominal DC current of 3.5mA. A gain imbalance within -0.1 to 0.3dB from 100MHz to 1GHz was measured in the proposed LNA, while within 0.2 to 0.6dB for the LNA using the conventional CG buffer. As to the phase imbalance, the proposed LNA remains within ±1 degrees from 100MHz to 1GHz, while the LNA using the CG buffer spreads from -2 to 4 degrees. The measurements show that the CMR buffer can compensate the gain mismatch and phase error by 0.3dB and 2 degrees, respectively.

Table 4.2 gives extra measurement results. Two additional bias conditions respectively based on the simulated G_{m1} of 25mS and 20mS are measured and listed.

Table 4.2 Performance Summary

Topology	Unit	Balun		
Technology	-	0.13μm CMOS		
Frequency	GHz	0.1 - 1.1		
Supply	V	1.5	1.2	1.0
G_{m1}	mS	30	25	20
Power (core)	mW	5.3	3	1.8
Voltage Gain	dB	23.5 - 25.5	22 - 24	21 - 23
Noise Figure	dB	2.3-2.7	2.5-2.9	2.9-3.3
IIP2	dBm	+18	+10	+8
IIP3	dBm	–2	–0.5	–1.7
Differential Imbalance	dB deg.	< 0.4 < 1		
LNA area	mm^2	0.06		

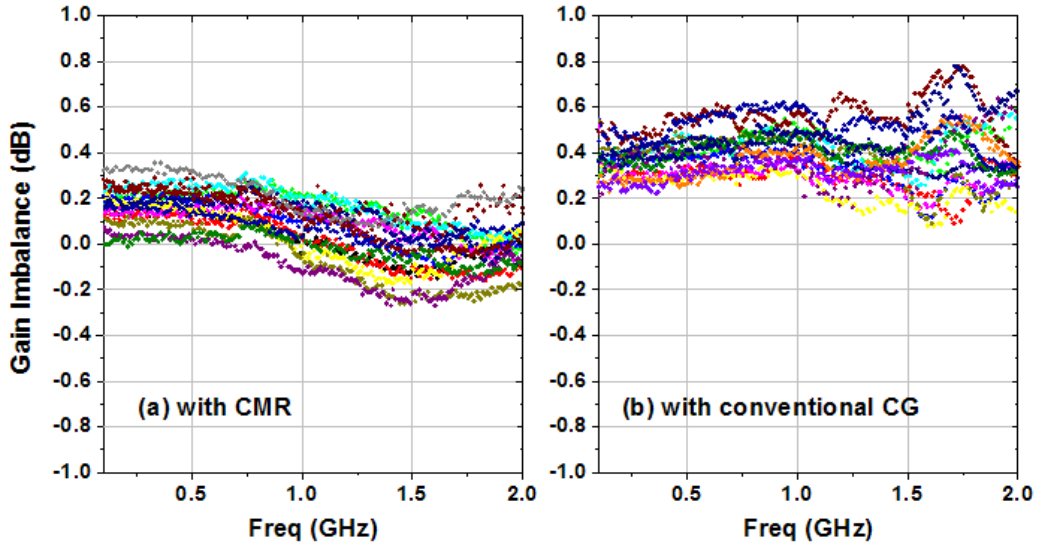


Fig. 4.26 Measured amplitude imbalance: a) the proposed LNA, and b) the LNA using the conventional CG buffer.

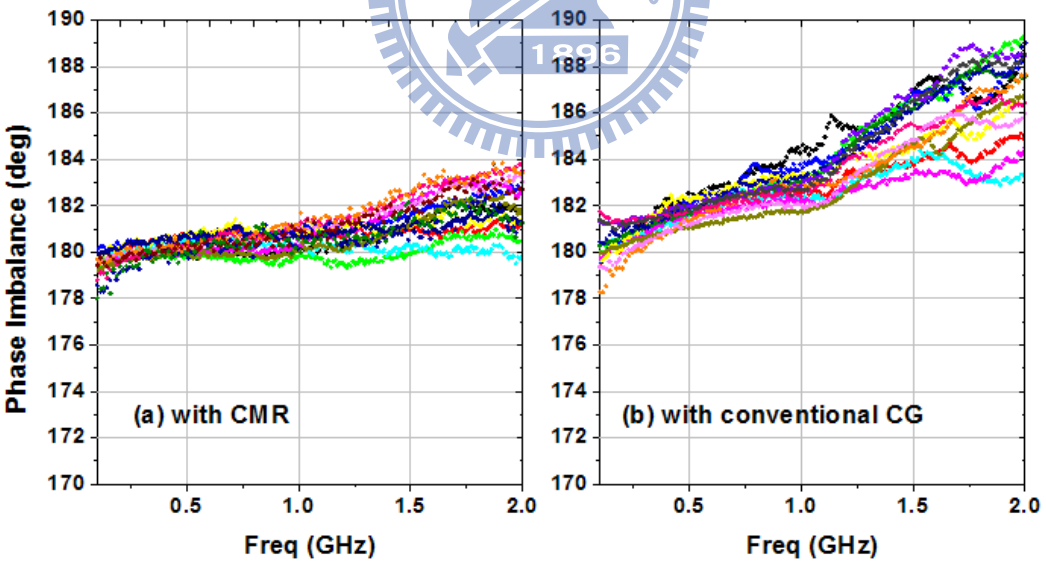


Fig. 4.27 Measured phase imbalance: a) the proposed LNA, and b) the LNA using the conventional CG buffer.

4.8 Appendix II – Asymmetric LNA Design

As discussed earlier, (4.3) indicates that a significant improvement to the noise factor can be obtained by increasing g_{m2} in the conventional CG-CS balun LNA. This appears to be effective in our proposed balun LNA which incorporates the CMR buffer and the bulk cross-coupling technique.

Assume the CS branch is *k* times bigger in the input transconductance compared with the CG branch, but *k* times smaller in the load resistor. It means that $g_{m2}=k \cdot g_{m1}$ and $R_{L1}=k \cdot R_{L2}$ as referred to Fig. 4.14. Since the two branches are not identical yet, some derivations in Appendix I should be revised accordingly. The derivations in noise factor could not be normalized to the load resistors as derived in Appendix I. Calculations based on the output voltage rather than the output current should be done, so (4.15) should be revised as

$$\begin{bmatrix} v_{o1} \\ v_{o2} \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \frac{1}{I} \cdot \begin{bmatrix} R_{L1} & 0 \\ 0 & R_{L2} \end{bmatrix} \cdot \begin{bmatrix} I_{11} & I_{12} \\ I_{21} & I_{22} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \tag{4.48}$$

Here, T_{ij} denotes the *transimpedance transfer function* from the *j-th* input (i_j) to the *i-th* output (v_{oi}). Thus, the overall noise factor (calculated in the voltage domain, rather the current domain) can be given by

$$F = 1 + \frac{R_s}{\left|T_{i,R_s}\right|^2} \left\{ \left(\frac{\gamma}{\alpha} \right) \cdot \left(g_{m1} \cdot \left|T_{i,M1}\right|^2 + g_{m2} \cdot \left|T_{i,M2}\right|^2 + g_{m3} \cdot \left|T_{i,M3}\right|^2 + g_{m4} \cdot \left|T_{i,M4}\right|^2 \right) + R_{L1} + R_{L2} \right\}$$

. (4.49)

Here, $T_{i,M1}$ — $T_{i,M4}$ and $T_{i,Rs}$ denotes transimpedance transfer gain and can be obtained from (4.25) — (4.33) and (4.48).

Fig. 4.28 illustrates the NF versus g_{m1} with different ratio *k* between two branches. Here, g_{m4} is also assumed to be *k* times bigger than g_{m3}. Different from Fig 4.19 which only takes the CMR effect into account, the improvement due to the BCC technique is considered in this calculation. It shows that if g_{m1} of 30mS is chosen, the LNA can achieve an NF of 2.05dB with k=1. The result shows that an extra NF improvement of 0.35dB benefits from the BCC technique as compared to Fig. 4.19. The NF can be decreased to 1.75dB with *k*=2, and 1.65dB with *k*=3.

To evaluate the effect of NF versus the ratio *k*, five test-kits were implemented for comparison. Fig. 4.29 shows the die microphotograph. The measured NF is illustrated in Fig. 4.30. As can be seen, the conventional LNA combining neither the CMR buffer nor the BCC technique has an NF of 3.6–4.1dB over 0.2-1.1GHz with *k*=1, and decreased to 2.45–2.9dB with *k*=2. As to our proposed LNA, it achieves an NF of 2.3-2.8dB with *k*=1, and decreased to 1.85–2.5dB with *k*=2. As a higher ratio *k*=3 is used, the NF is further decreased to 1.7dB, while rapidly increasing to 2.7dB at frequencies above 900MHz. This may result from the impact of larger parasitic at both input port and output load, which raises the noise contribution from M_1. It is noted that the measured NF results exclude the effect of the test buffer, which contributes an extra NF about 0.2dB based on the simulation results.

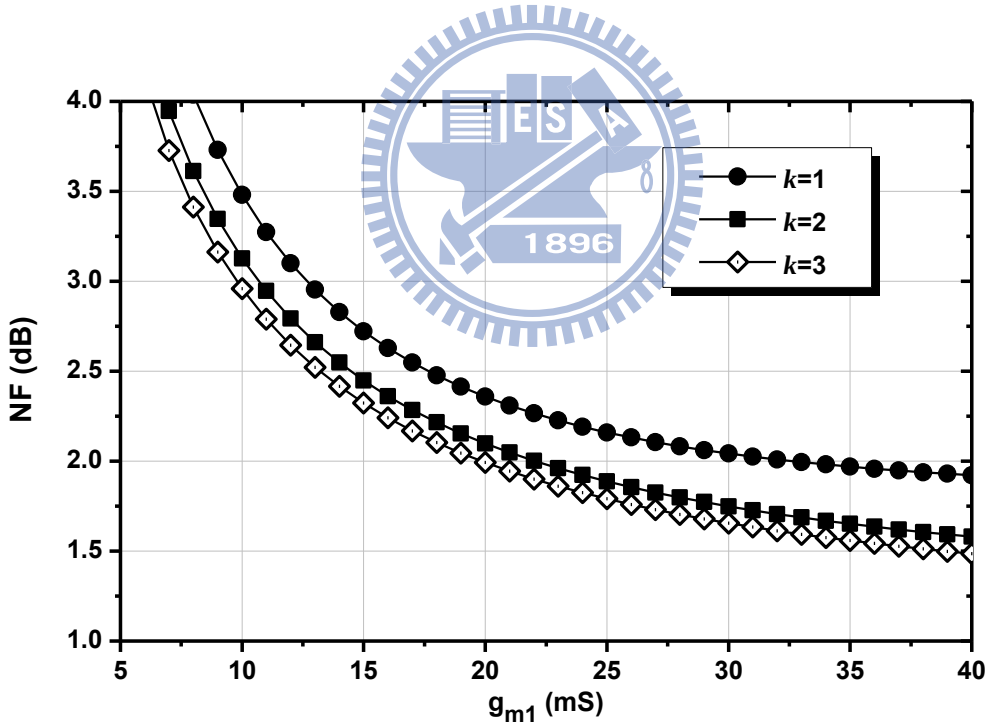


Fig. 4.28 Caculated NF versus g_{m1} with different ratio *k*.

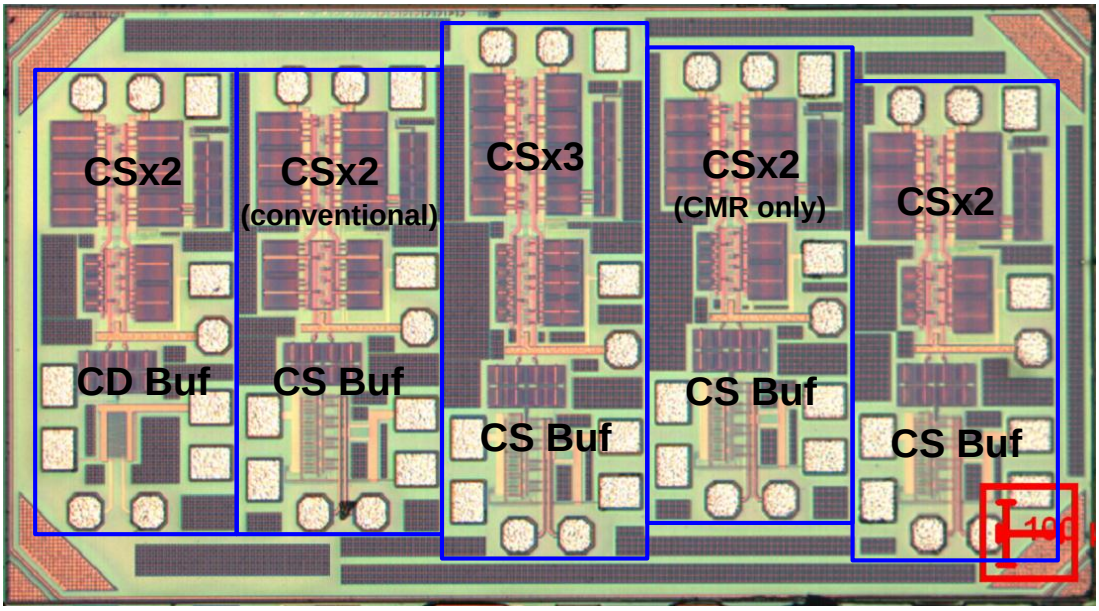


Fig. 4.29 Die micrograph of the fabricated LNA.

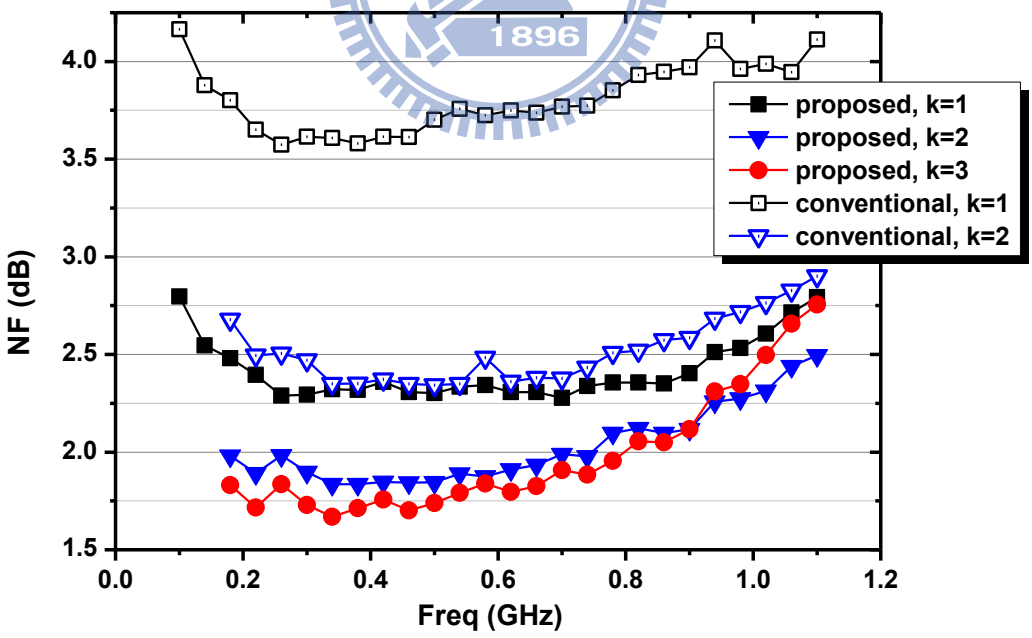


Fig. 4.30 Measured NF versus frequency with different ratio *k*.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Chapter 5

Dual-Band RF Tuner in 0.13μm CMOS

A fully integrated direct-conversion tuner is implemented in 0.13μm CMOS technology. The tuner achieves an overall noise figure from 3.7 to 4.3dB across the band of interest. The proposed current-mode switching scheme improves the achievable SNIR with a gain step of 15dB, while providing an IIP3 improvement of 18dB and an NF degradation of only 6dB. Design trade-offs are carefully considered in designing the baseband circuit, which provides wide gain tuning and accurate bandwidth against PVT variations with a DC offset residual less than 6mV. The measured maximum SNR values are better than 30dB over wide input power levels, ensuring robust receptions in a mobile environment. All circuit blocks are operated at 1.2V, and thus the tuner consumes low power of 114mW in the continuous mode. This compact tuner supports both UHF and L- bands, and occupies only 7.2 mm^2 die area.

5.1 Introduction

To be successfully integrated into a crowded handheld device, a DVB-H solution must meet the requirements of a small form factor and low power consumption. Several direct-conversion tuners have been reported in attempts to address these needs in recent years. Implemented in SiGe BiCMOS [18], [48], [49] or in 0.18-μm CMOS [16][17] technologies, these tuners consume 200-300 mW in the continuous receiving mode from the supply voltage around 2.7V. In order to further reduce the power

consumption and to provide a high level of integration, a mobile TV system-on-a-chip (SoC) is a good candidate by integrating a radio tuner, a baseband demodulator, and even a decoder into a single die. Towards this evolution, the first step is to develop a tuner in a finer deep-submicron or even nanometer CMOS technology [31].

The trend of technology scaling in advanced CMOS technologies benefits digital demodulators in both speed and power dissipation. The corresponding supply voltage reduction, which could be as low as 1.2V, however, causes issues to RF tuner design. In practice, a low supply voltage constrains stacking of several devices, and limits applications of many conventional circuit topologies. The reduced voltage headroom further degrades circuit linearity and an achievable signal-to-noise-and-interference ratio (SNIR). Therefore, the tuner architecture and each circuit block must be carefully designed to overcome the limitations of a low supply voltage and to comply with system requirements.

In this chapter, we focus on the implementation of circuit blocks, which can permit the maximum level of integration, minimize power dissipation, and reduce cost as well as physical size.

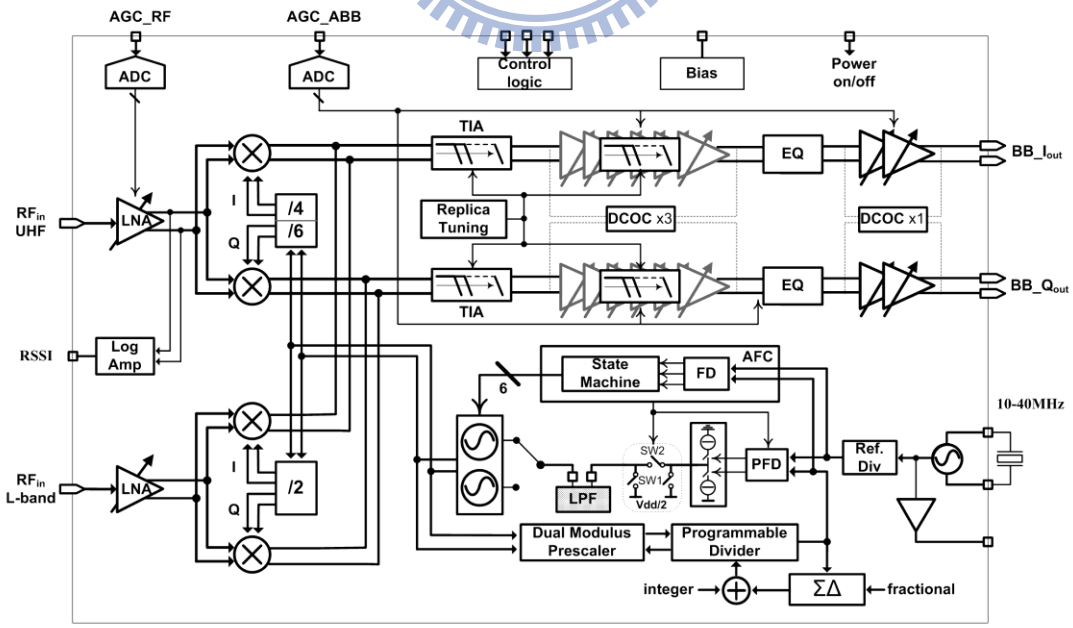


Fig. 5.1 Block diagram of the designed RF tuner.

5.2 Architecture and Frequency Plan

The block diagram of the tuner is shown in Fig. 5.1. The direct-conversion architecture is adopted to fulfill small physical size and low power consumption. All circuit blocks except for the front-end are shared for the dual-band operation to save chip area. The signal received from the UHF- or L-band antenna is amplified and down-converted to the baseband through two separate signal paths, which facilitates the connection to different external RF filters for each band. Moreover, two sets of I/Q mixers avoid complicated combinations required in both RF signal and LO paths. After down-conversion, both UHF and L-band signal chains are combined in the current mode at the input of the transimpedance amplifier (TIA). Subsequently, the analog baseband circuitry removes the out-of-channel interferers and amplifies the signal to the desired amplitude. Finally, the tuner produces I/Q balanced outputs for further signal processing at the baseband demodulator.

The single-ended-input differential-output low-noise amplifier (LNA), or balun LNA, facilitates the connection to the front antenna and to the following mixer of double balanced topology. It eliminates the need of an off-chip balun in front of the LNA for low noise figure and low external BOM. Also, it needs no on-chip balun after LNA, effective for low distortion as well as low power consumption. In this design, digitally controlled variable-gain function is included in both the front-end and the analog baseband to achieve the optimal SNIR. A wideband detector senses the total received RF power and then delivers an RSSI signal to the baseband demodulator to assist rapid front-end gain adjustment. Gain control can be done via a serial control bus or via an on-chip 7-bit SAR ADC by interfacing an analog signal from the baseband demodulator. To facilitate time slicing operation in the DVB-H system, one independent pin is ready for the baseband demodulator to switch the receiver on and off.

Frequency downconversion is essential in an RF tuner. A small LO frequency tuning range permits a small chip area and high performance. More specifically, a large LO tuning range generally leads to high VCO gain and/or a large number of capacitor banks, which trade off with good phase noise performance. In previous work, frequency downconversion required an LO source with dividers of divide-by-2 and/or divide-by-4 to cover the UHF and the L bands [17], [18], [47], [48]. Such schemes

call for very wide LO frequency tuning up to 62%, from 1.88 to 3.56GHz or from 0.94 to 1.78GHz. To reduce the required VCO tuning range, the LO chain was designed using divide-by-2 and divide-by-3 dividers for UHF quadrature LO generation, and using a first-order polyphase filter for the L-band in [16], [31]. The required VCO range is thus reduced to 40%, from 1.2GHz to 1.8GHz. This work utilizes a similar frequency plan while multiplying the frequency by two, requiring the VCO range from 2.56 to 3.84GHz. The quadrature LO signals are generated using divide-by-4 and divide-by-6 dividers in the UHF band, and using a divide-by-2 circuit in the L-band. Such a plan avoids using a polyphase filter and a divide-by-3 circuit, which potentially produces high I/Q mismatch. Furthermore, operating at higher frequencies enables the use of on-chip inductors with smaller area and higher Q-factors

5.3 RF Front-end Design

The front-end consists of two sets of LNAs and I/Q mixers for the UHF and L-band, respectively. Fig. 5.2 shows the simplified schematic for the UHF operation. An identical topology is used for the L-band implementation except replacing the LNA resistor load with an on-chip inductor load.

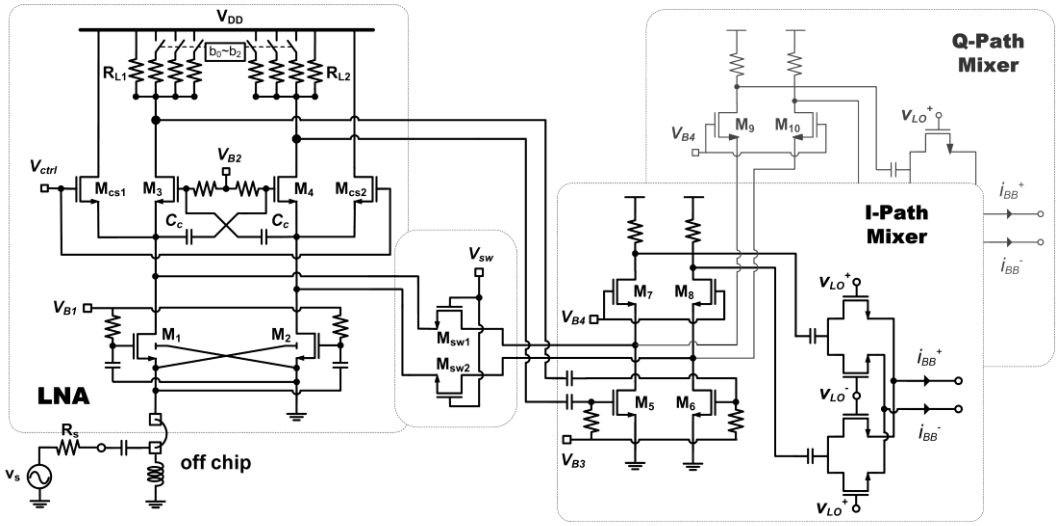


Fig. 5.2 Simplified schematic of RF front-end at UHF band.

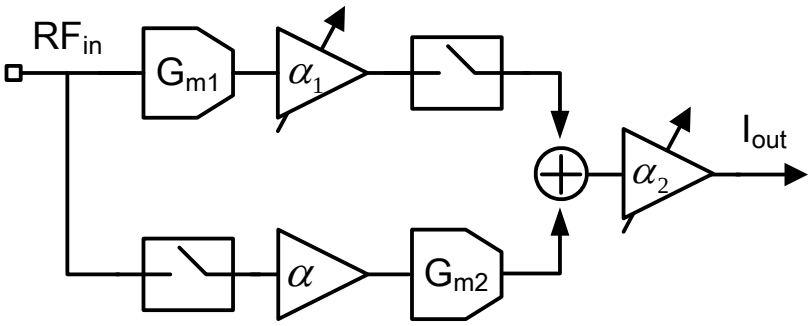


Fig. 5.3 The designed RFVGA topology.

5.3.1 RFVGA

As discussed in the previous chapter, the weak desired signal usually comes with strong interferers, which may degrade the signal quality without careful processing. There are two ways to alleviate this problem. The simplest way is utilizing a tracking filter prior to the LNA to filter out the interferers. However, the interferers may be only one or two channels away from the desired channel. This requires the filter to have an ultra-high quality factor, which is difficult to be integrated on chip. The other way feasible for on-chip integration is incorporating variable-gain functions into the RF front-end, called as RF Variable-Gain Amplifiers (RFVGA). Since the noise floor is mainly dominated by the added circuit noise and distortions, the role of the RFVGA is to trade-off the contributions between the added circuit noise and distortions by adjusting its gain settings. In theory, the RFVGA is expected to provide a constant output third-order intercept point (OIP3) across the gain range. When gain is reduced, input IP3 (IIP3) of the RFVGA should increase, but NF would degrade inevitably. As a result, the linearity of the RFVGA can be improved significantly at lower gains while preserving the noise performance at higher gain settings. It is noted that at a given gain setting the added circuit noise level is fixed, but the added distortions level increases rapidly with the input interference strength. For a given input interference to signal ratio, to sum up, the RFVGA would change its gain settings to maintain a maximum signal to

noise plus interference ratio (SNIR).

Typically, RFVGAs change their gain settings by varying either the input V-I converter or the load [50]. The adjustment of the V-I converter, furthermore, can vary either its received voltage input by tapped attenuator architectures [51] or its output current component by current steering methods [52]-[54]. Digital/discrete gain control is much flexible and easy to implement using any one of these methods. Analog/continuous gain control, on the other hand, is generally implemented only with the current steering method, which biases the current steering transistor pair in weak inversion region to realize an exponential transfer function.

In this design, the RFVGA has a digitally programmable gain with multi-step resolutions. The overall architecture is illustrated in Fig. 5.3, composed of two separate signal path. The upper path can provide a fine gain step as low as 2dB, while the lower path achieves a coarse gain step of 41dB further to extend the overall dynamic range. As illustrated in Fig. 5.2, the upper path is composed of two amplification stages, which provides a high voltage gain to compensate for the loss of the subsequent passive mixer. The first stage is implemented using our proposed LNA architecture as aforementioned in chapter 4. It provides wideband low noise amplification and an input impedance match to 50 Ω, while the second stage, i.e., the transconductance stage of the mixer, is cascaded to the proposed balun LNA to obtain maximum front-end gain. Variable gain control is implemented by three methods in combination of these two cascode amplifiers. Fine gain tuning is realized by a bank of digitally controlled resistor load, R_{L1} and R_{L2}. In actuality, it would be more desirable to realize all the gain reduction at LNA output, since this would achieve the best SNR over the other VGLNA architectures [50]. However, the parasitic of the switch transistors may load the output, degrading the bandwidth. Moreover, as the gain back-off becomes much larger, the small output resistor and the subsequent stages will dominates the noise performance. In this design, the variable load provides 12dB gain range in 2dB steps. Another gain control with coarse gain stepping is carried out by two different ways. One of them applies the current steering technique by switching M_{cs1} and M_{cs2} with a gain step of 6dB. The other one utilizes a novel current-mode scheme of switching the signal path and is explained as follows.

As shown in Fig. 5.2, a pair of switch transistors M_{sw1}/M_{sw2} is inserted between the low impedance terminals of the two cascode amplifiers, providing an alternative

path of gain attenuation. Fig. 5.4 illustrates how to achieve high-gain and low-gain by switching this alternative path. When the switch transistors are turned off, the front-end is configured as cascaded two-stage amplifiers, providing a transconductance of $g_{m1}R_{L1}g_{m5}$ to the input voltage V_{in}. When the switch transistors are turned on and transistors $M_{3\text{-}6}$ are all off, the front-end is configured as one single-stage cascode amplifier, giving a transconductance of g_{m1}. As a result, one-step gain attenuation of $g_{m5}R_{L1}$ is achieved. This current-mode scheme effectively reduces the distortions caused by voltage modulation. It avoids large voltage swings across the switch transistors as compared to the conventional voltage switching method. Moreover, it also substantially helps achieve high linearity by avoiding inter-stage intermodulation since the two cascaded amplifiers are reduced to a single-stage amplifier. In addition to better linearity, this scheme enables negligible loading effect on switch transistor parasitic due to its low-impedance terminations, which alleviates the degradation of operation bandwidth. Another important advantage comes from the fact that no input and output interface is affected after gain switching, so the input matching condition can be maintained well. Furthermore, this scheme also features much better noise performance if compared with the conventional variable load or current steering methods when the gain attenuation becomes much larger. The measured results show that this switched path offers a stepped attenuation of 15dB with a high IIP3 level of +5dBm, improved by 18dB from that at the maximum gain configuration while noise figure degrades only by 6dB in overall receive chain, 9dB better than the conventional pre-attenuation method [51].

As the gain continues to decrease, the input transconductance stage would limit the linearity performance. As this condition occurs, the VGLNA will turn-on the lower path and turn-off the upper path (Fig. 5.3) to extend the dynamic range. It is implemented using the one-step resistor taped attenuator method [55]. Single-ended input is applied to the transconductor of the second-stage amplifier. It provides a -5dB gain attenuation and +15dBm IIP3 to further extend the input dynamic range.

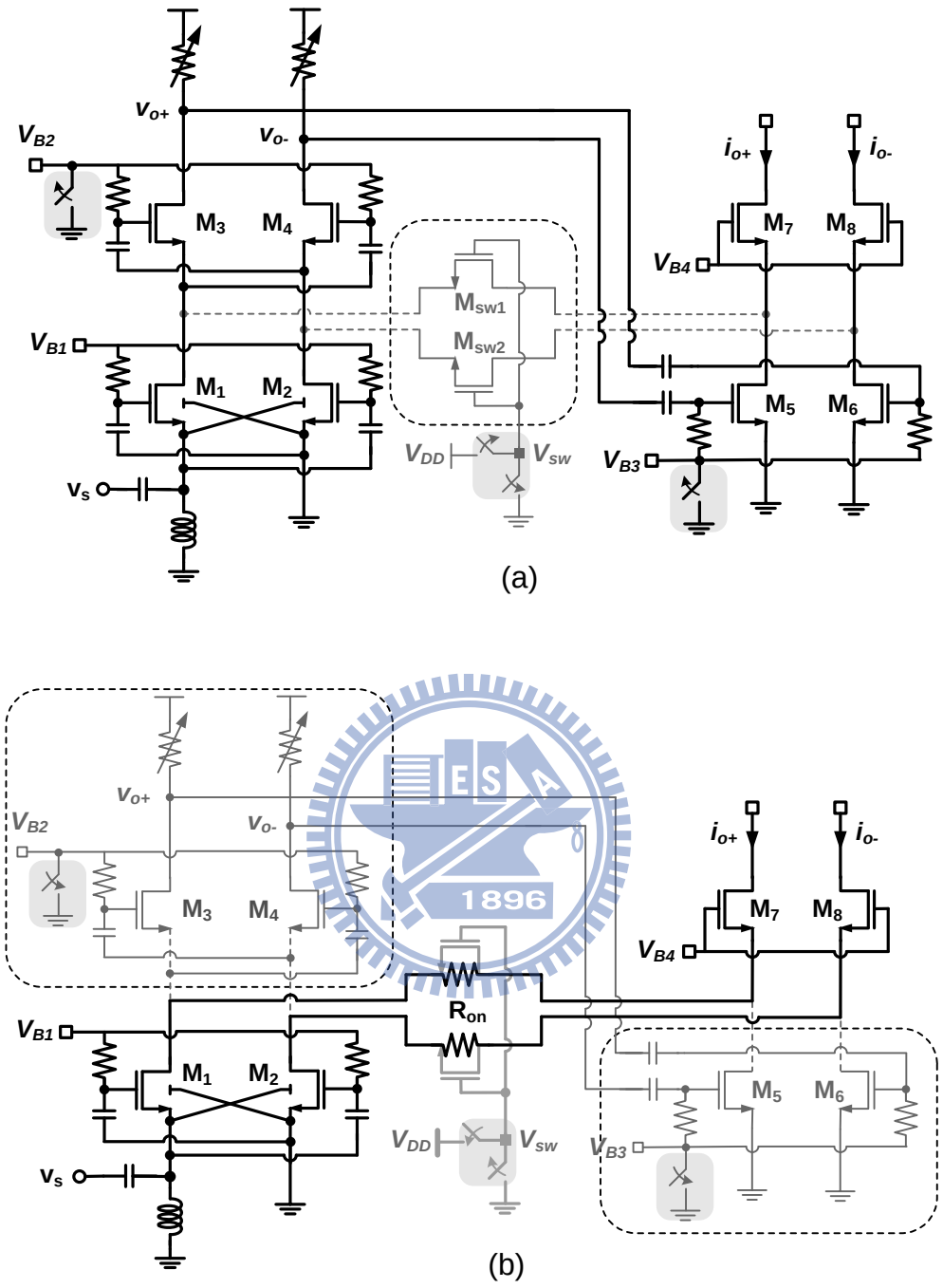


Fig. 5.4 Front-end configuration: (a) at high-gain mode, and (b) at low-gain mode.

5.3.2 Current Driven Passive Mixer

This design utilizes a current-mode passive mixer rather than a Gilbert mixer to achieve high linearity along with a flexible output DC level. Since the mixer output is directly coupled to the analog baseband in a direct-conversion receiver, its DC level should be compatible to the common-mode voltage of the analog baseband. To avoid dynamic range limitations at op-amp level, a rail-to-rail amplifier with a common-mode level of half supply voltage would be preferred. This means a common-mode level of 0.6V is used with a supply of 1.2V. Such a low common-mode level would pose a difficult challenge for a Gilbert mixer because it requires stacking of multiple devices. Instead, a current-mode passive mixer has no dc current dissipation, providing flexibility to set the DC level. In addition, the current-driven passive mixer can achieve relatively high linearity. By driving a very low impedance load, it avoids large voltage swing across the switching transistors, alleviating the distortions resulting from the switching behaviors. It should be noted that employing passive mixers may impose the linearity burden on the preceding blocks mostly the RF amplifier, which usually needs a high gain to suppress the noise contribution of the passive mixer.

As shown in Fig. 5.2, the mixer consists of double-balanced switching quads followed by a transimpedance amplifier (TIA). The I/Q mixers sink the RF current from the second-stage output of the VGLNA. Sharing one common input transconductor between I and Q paths benefits to minimize quadrature inaccuracy. After down-conversion through the switching quads, the baseband current driven into the TIA is converted to voltage output. Because the transconductor is ac coupled to the switching quad, no dc current flows through the switching transistors. Thus, the commutating switches operate from OFF to triode state and vice versa. This implies that any voltage source placed at the gate, representing flicker noise or switch pair offset, would not be transferred to the mixer output. In other word, this configuration is insensitive to the offset and switch flicker noise, which improves IIP2 and reduces flicker noise.

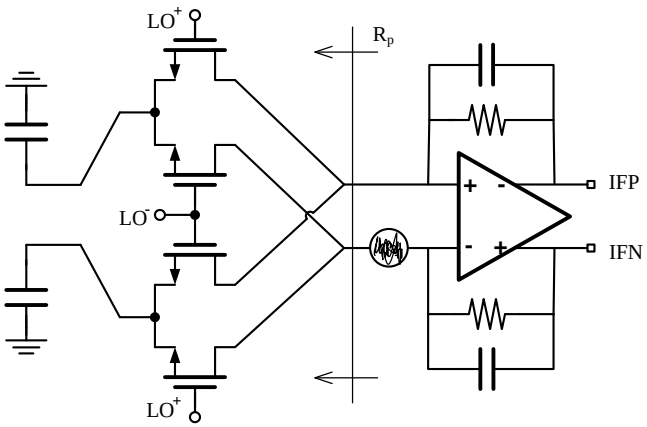


Fig. 5.5 Simplified schematic for noise analysis of the TIA.

As the TIA is implemented by a fully differential op-amp connected in RC shunt feedback, extreme care should be taken to limit the noise contribution from the op-amp. As shown in Fig. 5.5, the parasitic capacitance at the output of the transconductance stage is charged and discharged at the rate of the LO, causing that the resistance seen at the op-amp input terminals is actually a switched capacitor resistor [56]. Since there are two differential pairs connected to the op-amp terminals in parallel, the effective resistance is therefore given by

$$R_P = \frac{1}{4 f_{LO} C_{par}} \tag{5.1}$$

The op-amp input referred noise is thus transferred to the output with transfer function given by

$$\frac{\overline{v_{no}^2}}{\overline{v_{ni,op}^2}} = \left(1 + \frac{2R_F}{R_{par}}\right)^2 \tag{5.2}$$

To minimize this noise contribution, we have to minimize the parasitic capacitance C_{par} and the op-amp noise.

The simulated gain for the transconductance stage, mixing quads and the TIA in cascade was 15 dB and its simulated Noise Figure was 12 dB in double-side band (DSB) calculations. The transconductance stage consumes 3mA and each TIA consumes 7mA. This large current dissipation ensures the TIA to achieve a maximum output swing of over 2V peak-to-peak differentially. The feedback RC across the

op-amp realizes one tracked pole at 1.5 times of cut-off frequency, i.e., 6MHz for 8MHz channel bandwidth. This real pole can pre-filter the adjacent interference which may saturate the first stage of the subsequent filter due to its full swing limited by the low 1.2V supply.

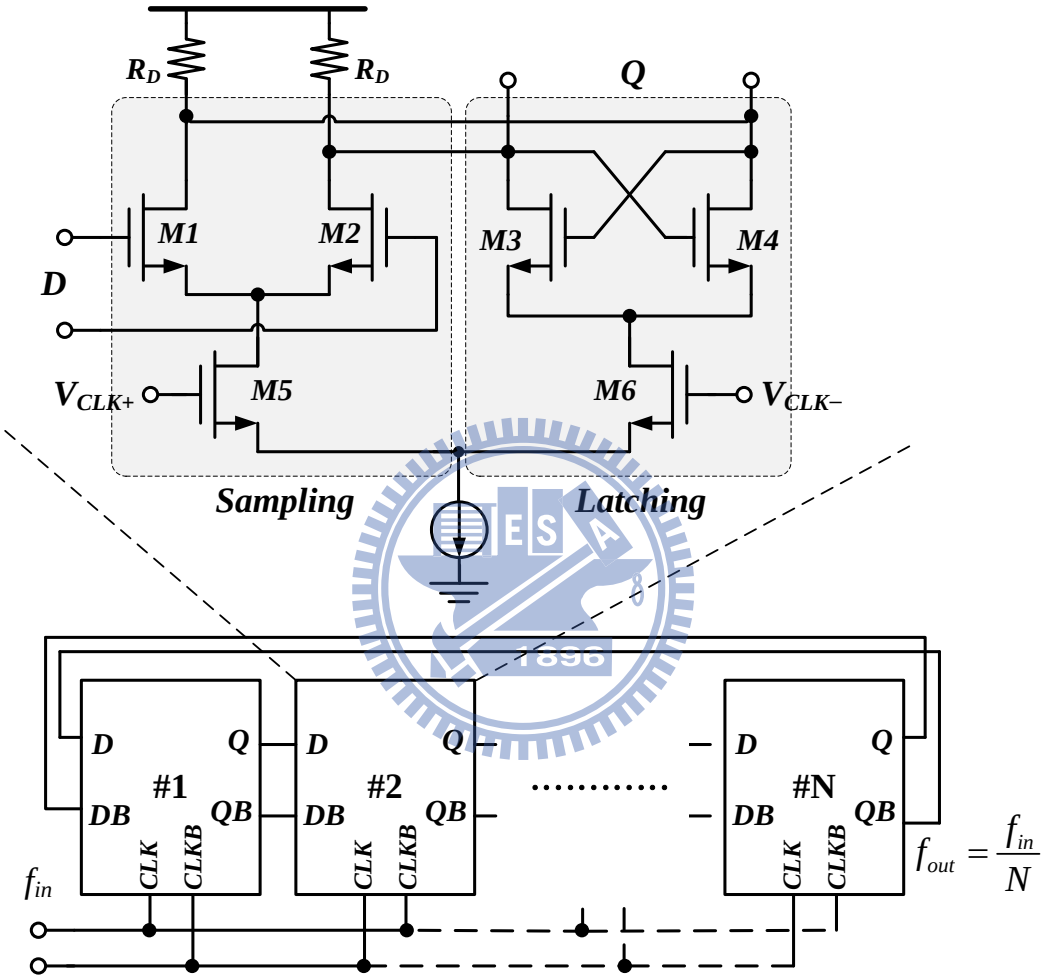


Fig. 5.6 Architecture of the divide-by-four divider, and the designed D-latch circuits.

5.3.3 Quadrature LO Generation

Accurate quadrature LO signals with 50% duty cycle is critical for high image rejection ratio. This design generates the quadrature LO signals through divide-by-N circuits, which are comprised of N D-latches in cascade and in a negative feedback

configuration. To cover a wide frequency range from 2GHz to 4GHz, these high-speed flip-flop based frequency dividers are implemented using current-mode-logic (CML) latches. Fig. 5.6 shows the architecture of divide-by-N dividers and designed D-latch circuits. In order to achieve higher operation speed at lower current consumption, the sampling stage uses larger device size than latching stage. The ratio between these two stages is four in the implemented design. It is noted that special attention should be paid to layout balance of the quadrature generators to avoid impairing the quadrature accuracy.

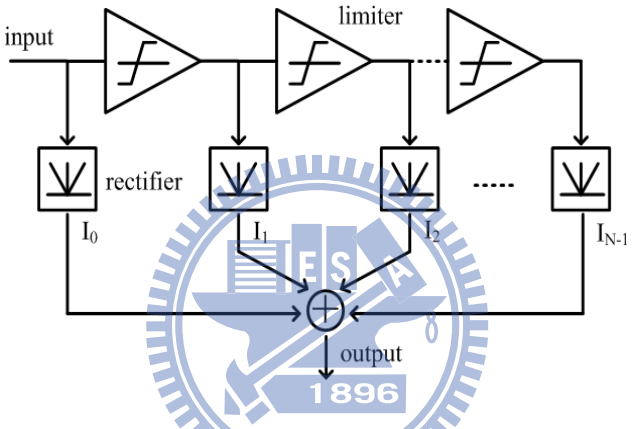


Fig. 5.7 Simplified diagram of successive-detection logarithmic amplifiers.

5.3.4 Received Signal Strength Indicator (RSSI)

A received signal strength indicator (RSSI) is extensively employed to provide the information necessary to adjust the receiver gain. For high frequency, wideband applications, the successive-detection architecture is widely used to realize a logarithmic amplifier. Fig. 5.7 shows the simplified diagram of a successive-detection logarithmic amplifier. The pseudo-logarithmic, piecewise linear function is realized as a cascade of limiters with their outputs rectified, summed, and filtered to produce a DC output signal. Moreover, the number of limiters is associated with the desired gain, bandwidth, and power consumption of the wideband power detector. Thus, choice of the number of stages is a compromise between a high gain-bandwidth product, a high input sensitivity, and low power consumption. In this work, four stages are cascaded

to achieve a dynamic range of 20 dB. The input is terminated at the low-impedance nodes, the source terminals of M_7/M_8, as shown in Fig. 5.2. Unlike the conventional termination at the LNA output, this termination is advantageous to avoid bandwidth degradation due to the parasitic capacitance.

5.4 Analog Baseband Design

The analog baseband functions as channel selection and programmable amplification for both In-phase and Quadrature signal processing. Programmable gain function provides the flexibility to optimize noise, linearity and power consumption. To optimize noise, power consumption and silicon area, it is necessary to make trade-offs in the Op-amp together with the input/feedback resistor pair. In this design, the analog baseband provides total gain control from 0 to 63.5dB in 0.5dB steps. It includes several circuit blocks as shown in Fig. 5.8: a variable-gain low-pass channel filter (VGCF) with cutoff frequency calibration, a first-order all-pass filter, a programmable-gain amplifier, four independent dc-offset cancellation (DCOC) loops with on-chip capacitors, and a unit-gain buffer.

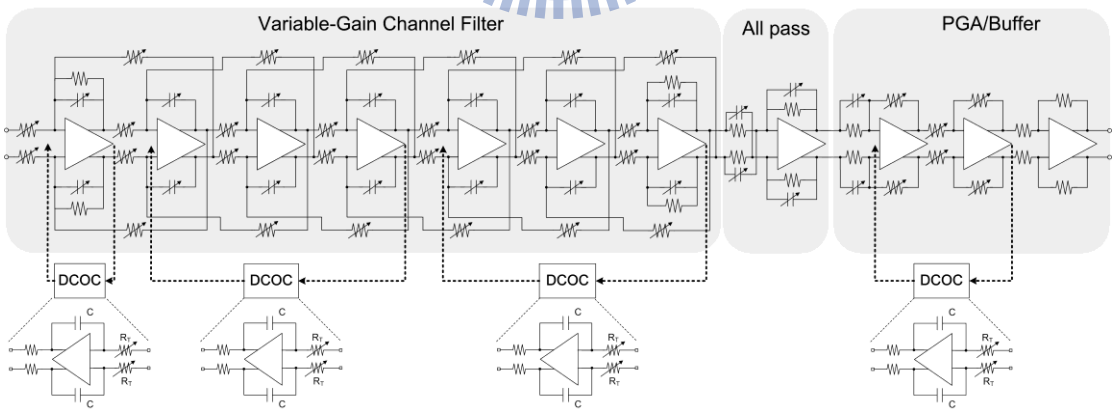


Fig. 5.8 Architecture of Analog Baseband.

The channel filter is a seventh-order Chebyshev type-I implemented using the leap-frog topology. Embedded into the filter blocks, gain control provides a range from

0 to 48dB with a tunable cutoff frequency from 2 to 5 MHz depending on the channel bandwidth in use. In the VGCF, the first two Op-amps consume high current for low noise and large signal-handling capability. Also small input/feedback resistor pairs are applied to reach better noise performance at the expense of large capacitor area. The remaining five Op-amps consume less current since the noise contributions are less critical. In addition, the input/feedback resistor pairs have high resistances to reduce the capacitor area. Following the VGCF, the first-order all-pass filter is added to improve the group delay. Then two PGA stages provide an extra gain of 15.5dB.

5.4.1 Auto-Bandwidth Calibration

On-chip RC auto-calibration activated at power up accurately sets up the channel bandwidth from 2.5 to 4 MHz against PVT variations. The architecture and the timing diagram are depicted in Fig. 5.9. A duplicate RC integrator compares the RC time constant with a reference clock generated from the crystal output through a programmable divider. The detailed procedure is described as follows.

Two successive states are utilized to complete the auto-calibration process in an iterative process. In the first phase, the clock *CLKB* is set to high. The integrator is configured as a resistive feedback amplifier with gain attenuation. As a result, both integrator outputs, V_{op} and V_{on}, are reset to the Op-amp's common-mode voltage. In the second phase, *CLKB* is low. The integrator is configured as a lossless integrator, which forces its positive output V_{op} to charge toward *VDD* and its negative output V_{on} to discharge to ground. Once V_{on} voltage becomes smaller than the reference voltage, the comparator will deliver a control signal to stop counting. The 6-bit counter's code is subsequently subtracted from the Bandwidth Code, a default value of RC time constant corresponding to the channel bandwidth. After that, the subtracted output code is sent to update the Capacitor Code used to control the capacitor banks. The calibration will continue until the capacitor code remains constant for several consecutive iterations. As soon as the calibration is finished, another control signal will be sent to power off the calibration circuits and stop the input clock. Finally, a 5-bit control word is provided to adjust the capacitors in the TIA and filter stages within ±3% bandwidth accuracy.

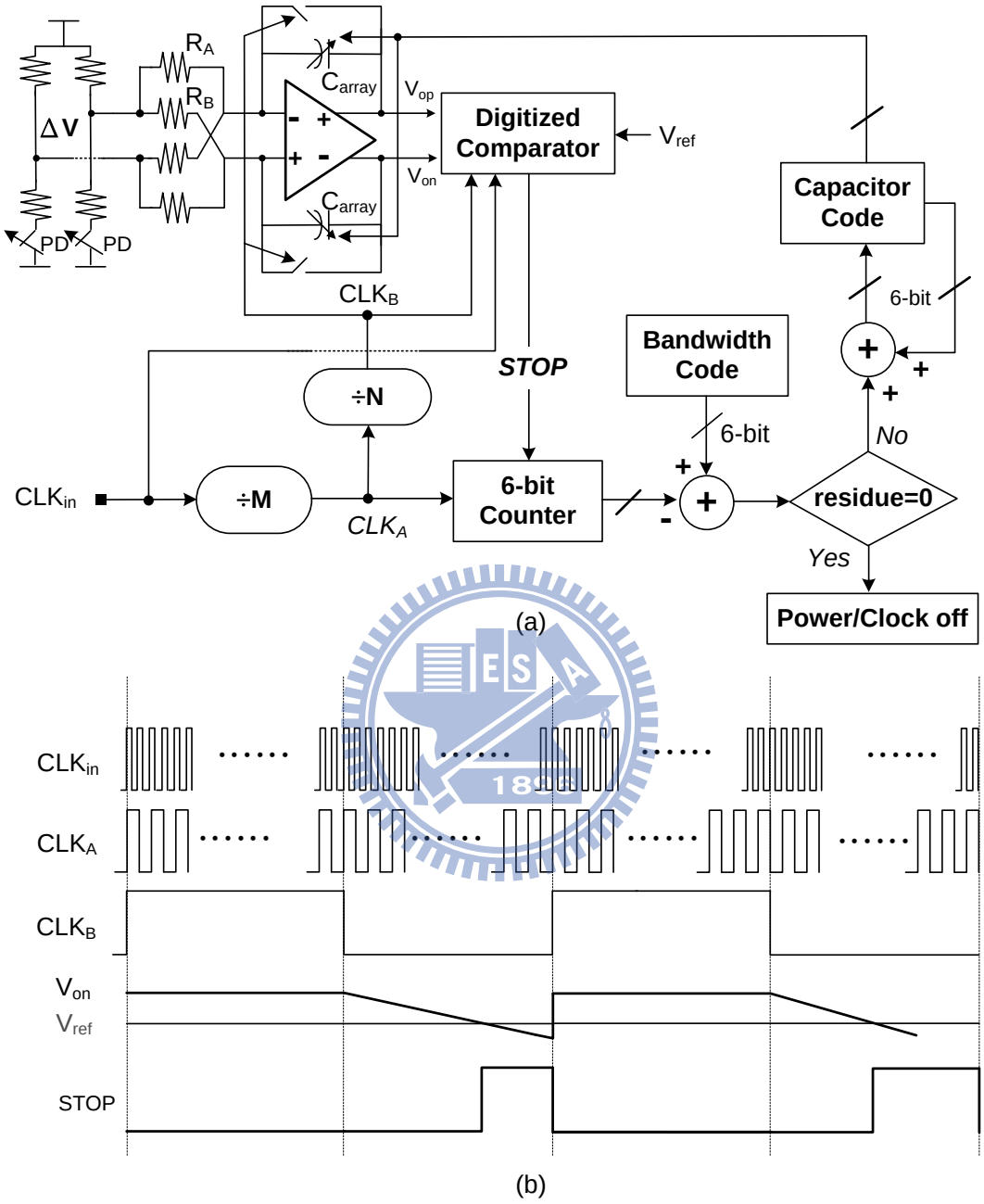


Fig. 5.9 (a) Architecture of the RC calibration loop. (b) Timing diagram of the RC calibration loop.

5.4.2 DC Offset Cancellation

DC-offset cancellation is indispensable in a direct conversion receiver because DC offset may saturate the baseband output and degrade the dynamic range. Featuring a high-pass response in the signal chain, the DCOC has a cutoff frequency less than 1 kHz to ensure sub-carriers around DC are not affected too much. However, if a single loop cancellation is utilized, such a low cutoff frequency will demand for large loop capacitors, inevitably implemented in off-chip components at the expense of four extra package pins [18], [49]. Since the high-pass corner frequency is proportional to the signal processing gain, but inverse to the loop capacitance, multi-loop cancellation can effectively reduce the required loop capacitances. For example, as the signal chain is uniformly divided into M segments in cascade and each segment has an independent servo-loop for DCOC, the processing gain and the used capacitance in each loop can be expressed by $A^{(1/M)}$ and C_{ml}/M, respectively, where A is the total gain of the signal chain and C_{ml} is the total capacitance required in M loops. To maintain the same high-pass corner frequency in the single-loop and multi-loop implementations, the ratio of the total required loop capacitance in single-loop calibration to that in multi-loop can be approximated as

$$\frac{C_{sl}}{C_{ml}} = \frac{A^{(1-\frac{1}{M})}}{M} \tag{5.3}$$

where C_{sl} is the total capacitance required in single-loop cancellation. In this design, four independent servo-loops are utilized to reject DC offset, in total using 16pF capacitance which is much easier to integrate on chip since 60 times less total capacitance is required compared with a single loop implementation.

The final high-pass cutoff frequency is set constant at 1 kHz for all gain settings by keeping the gain of feedback loop inversely proportional to that of the signal path. Furthermore, the remaining DC offset resulting from the last stage of the servo loop chain is carefully minimized by enhancing transistor symmetry and by using larger dimensions. The measured DC offset is less than 6mV with an average of 4mV characterized over 50 samples at the maximum gain setting. The analog baseband totally dissipates 22mA current, where 8.3mA is dissipated by the first two stages. The simulated input-referred noise level is about 6nV/$\sqrt{Hz}$.

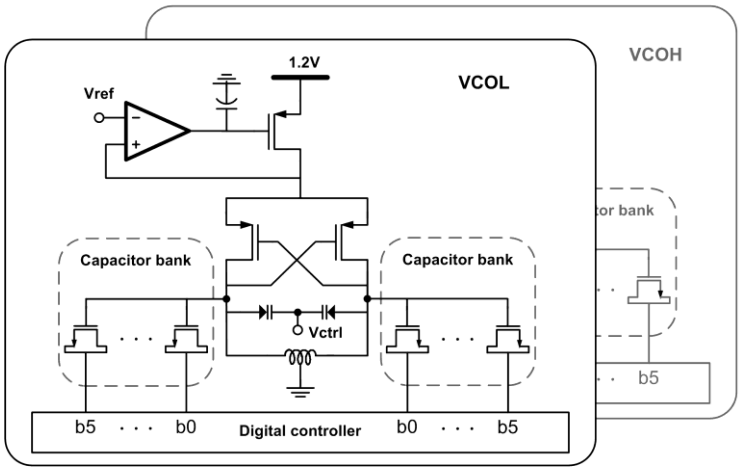


Fig. 5.10 Schematic of VCOs.

5.5 Frequency Synthesizer Design

A fractional-N PLL synthesizer using a 3rd-order delta-sigma modulator with 24-bit accumulators is employed to achieve a high resolution and fast switching time as well as good phase noise. The frequency step of this synthesizer is less than 10Hz to meet the requirement of multi-standard operation where different channel spacing is specified. In addition, fractional synthesis provides the flexibility to share the same crystal with the existing cellular platform to reduce the BOM cost and PCB area.

The synthesizer generates a wide frequency output from 2.56 to 3.84 GHz by using two VCOs with overlapped tuning characteristics. As shown in Fig. 5.10, each VCO consists of two PMOS cross-coupled transistors with an internal regulator and one LC tank. The on-chip voltage regulator reduces the impact of power supply noise [57]. Moreover, the tank which is terminated into DC ground enables a wide range of analog control almost from rail to rail, which is crucial for low-voltage VCO design.

As far as phase noise is concerned, the entire tuning range is divided into 64 sub-bands by a 6-bit capacitor bank to decrease the voltage-to-frequency gain. Consequently, adaptive frequency calibration (AFC) is needed to select a specific sub-band prior to starting the process of phase locking. The AFC procedure is

described as follows. In the beginning, the PLL loop is open and the analog control terminal of the VCO is biased at half supply voltage. Subsequently, AFC is activated, trying to select an appropriate sub-band using the binary search method by comparing the divided VCO frequency with the reference one. Instead of using counters [58], the frequency detector is implemented using a quadri-correlator to shorten the comparison time [59]. After one suitable sub-band has been chosen, the PLL loop is closed achieving phase locked, and AFC is turned off.

5.6 RF Integration Design

When many circuit blocks such as the front-end, analog baseband, and frequency synthesizer are integrated into a receiver system, some design considerations should be concerned. As the level of integration increases, there are many new challenges to be overcome, such as noise coupling issues among different blocks, programmable flexibility for high performance, and constraints of limited I/O pins. This section will describe the major issues concerning the integration and present the methods used in this implementation.

5.6.1 Noise Coupling Issues

One of the most critical issues to deal with in a highly integrated system is noise coupling among different blocks [60]. Noise coupling may result from cross-talk via silicon substrate, supply/ground traces either on the chip or board, and bonding wires. Several methods discussed as follows are utilized in this integration to mitigate noise coupling.

First, having separate power domains for different blocks with specific characteristics is important since noise can propagate via the low-impedance power and ground traces without much attenuation. This implementation categorizes different supply domains as LNA, Mixer/LO Quadrature Generator, analog baseband, VCO, PLL analog part, and PLL digital part/crystal oscillator. In fact, much more on-chip pads still can be utilized to mitigate the supply noise coupling. However, it

might inevitably need to bond several on-chip pads to the same package pin due to limited number of I/O leads. Nevertheless, this method can effectively trade off the supply coupling noise and occupied package pins.

Second, bypass capacitors are widely used in each bias network. The added RC network produces one extra pole to block the noise propagation through the current-mirroring paths. It should be noted that this filtering ability is a trade-off with the time to startup and shutdown. Generally, a dual time constant loop can be utilized to mitigate the trade-off if necessary.

As different blocks with specific characteristics are integrated on a common substrate, substrate isolation is very important for a successful integration. For example, with a ΔΣ fractional- N synthesizer, the use of large digital blocks such as N-bit (N>20) accumulators and adders can generate substantial digital switching noise to the sensitive RF [61]. To increase the level of isolation between the noisy digital part and the sensitive RF, careful floor plan with increased separation distance and extra layout techniques with P- and/or N-rings having a wide width larger than 10μm are helpful and utilized in this implementation [62].

5.6.2 Programmable Bias Current

To maintain stable bias current for all circuit blocks in the receiver, a bandgap reference circuit with an accurate off-chip resistor is used to generate a reference bias current, which is insensitive to PVT variations. Then, several branches of bias current required for each circuit block can be generated by mirroring from this stable reference current. Along with N-bit current banks as shown in Fig. 5.11, each bias current for a specific circuit block can be programmed to optimize the system performance. It is worth saying that programmable bias may further reduce power consumption without sacrificing too much performance. This mainly results from the fact that over-design which increases power consumption is usually taken in the stage of circuit design to avoid re-spins of the chip.

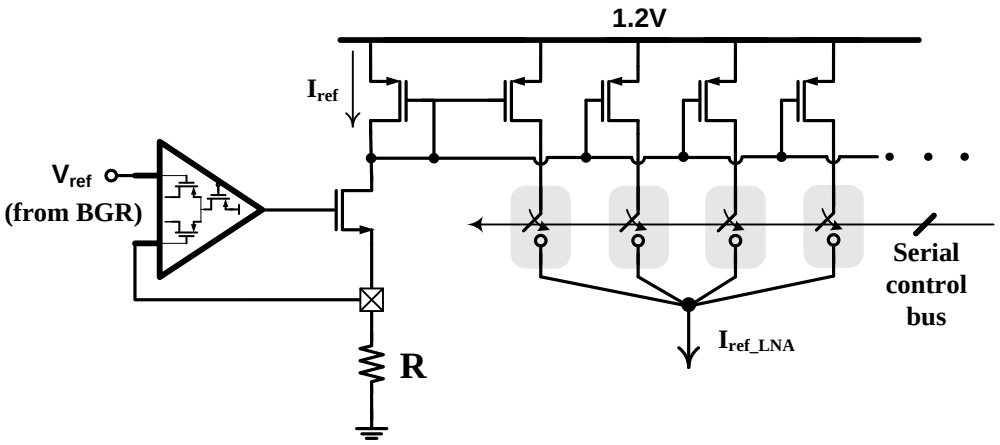


Fig. 5.11 Programmable bias current (3-bit is shown).

5.6.3 Serial Control Interface

As the level of integration increases, the amount of control information to set the gain, bandwidth, and frequency channel becomes much significant. For a wireless system, RF chip is typically controlled by the BBP/MAC IC via a serial bus. The serial bus can also facilitate testing, debugging, and optimization. To achieve this, RF systems usually contain registers that store part of the received control signals and can be programmed sequentially, either using a 3-wire serial bus or the I2C (Inter-Integrated Circuit) bus. The 3-wire serial interface is easier to implement, but difficult to control timing critical signals due to its low speed. On the contrary, the I2C bus developed by Philips Electronics in the early 1980's is a good compromise between speed and complexity. The I2C interface is widely used in modern communication ICs since the issued patent was expired. In this tuner prototype in 0.13μm CMOS technology, a 3-wire serial interface is adopted. In the other two prototypes in 65nm CMOS technology as will be described in the next chapter, however, the I2C bus is adopted.

5.6.4 Package Considerations

Packaging is very important in realizing an end-product and should be taken into account in the early stage of circuit design. To be concerned with both RF performance and board area, the use of leadless packages will be preferred. Leadless packages can reduce the inductance significantly by eliminating the part associated with the lead. Moreover, the applicability of paddle ground can allow for as many grounds as can be fit in the pad ring of the chip, effectively reducing the occupation requirement of package leads. Through down-bonds to the package paddle ground which is soldered onto the board assembly ground, the ground inductance can be reduced significantly. Typically, ground inductance lower than 0.5nH is possible in commercial QFN packages.

A simplified schematic as shown in Fig. 5.12 can be used to model the connection between the die and the plastic package [63]. Here, CP represents the capacitance between the bond pad and ground metal, LB models the inductance introduced by the bond wire, and CL represents the capacitance between the package leads and ground. In the stage of circuit design, CP and CL are modeled as 0.25pF and LB is modeled as 1nH for ground pads and 2nH for the other bonding pads, such as VDDs.

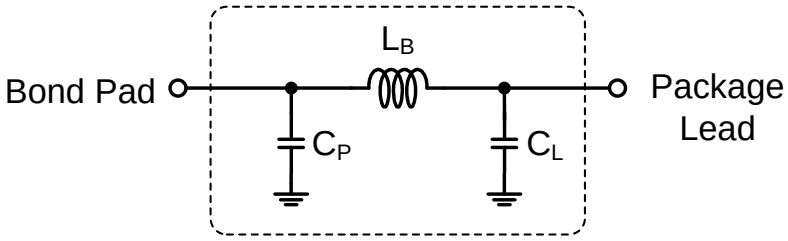


Fig. 5.12 Equivalent circuit of interconnection between the pad and the lead.

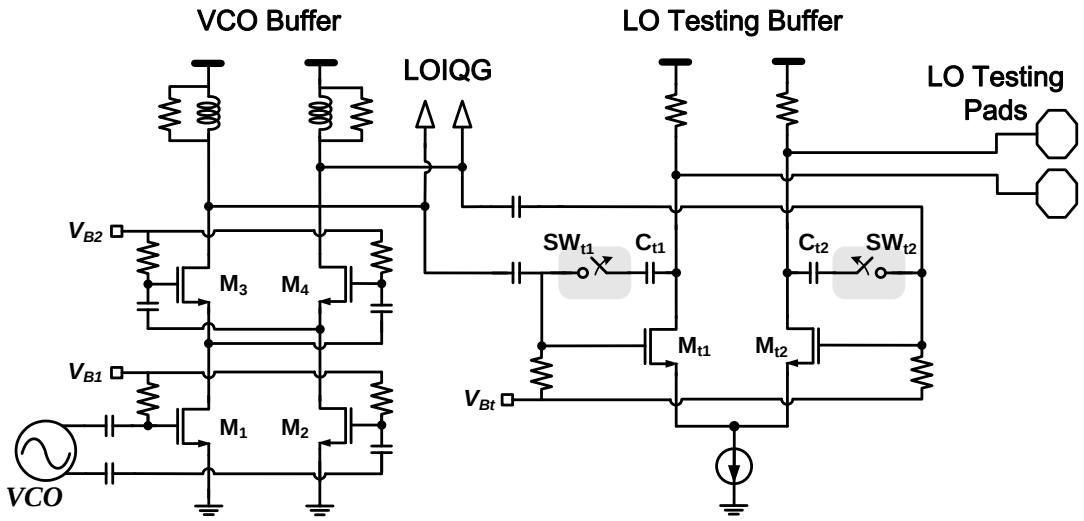


Fig. 5.13 Schematic of a bidirectional LO testing buffer.

5.6.5 Testability

To prevent errors in block design having a large impact on the testability, special test modes should be implemented to allow for testing of circuit blocks in-situ. As mentioned above, the receiver system typically can be divided into three main blocks, PLL, RF front-end, and analog baseband, from the view of functionality and division of labour. Therefore, there exist two interfaces needed to be reserved for testability. One of them is the interface between the front-end and the analog baseband. Since the signal passing though this interface is at the baseband in a voltage output, four pads can be reserved for connections to the signal traces at the TIA output. This facilitates a bidirectional I/O testing, either to observe the output of RF front-end or to be used as the signal input to allow observation of analog baseband if the front-end does not work. The other interface for testability exists between the front-end and the PLL. This interface is very important to verify the impacts of completely integrated LO chain on the overall receiver performance. At least, it can ensure that the receiver chain performance can be measured if the PLL does not work. As shown in Fig. 5.13, a bidirectional LO testing buffer is implemented to allow observation of the PLL output or the input of an external LO. If the PLL is to be measured, the testing buffer is activated and SW_{t1}/SW_{t2} are turned off, driving a 50Ω load of the measurement

instrument. Alternately, the LO pads can be used as inputs by turning on the VCO buffer and LO testing buffer, while activating SW_{t1}/SW_{t2}. Such a capability makes it possible to characterize performance using external LO compared with on-chip LO. In a normal operation mode, rather than a testing mode, both the LO testing buffer and SW_{t1}/SW_{t2} are turned off, and the on-chip LO source passes through the VCO buffer which drives the quadrature generator, i.e., dividers of divide-by-2/4/6.

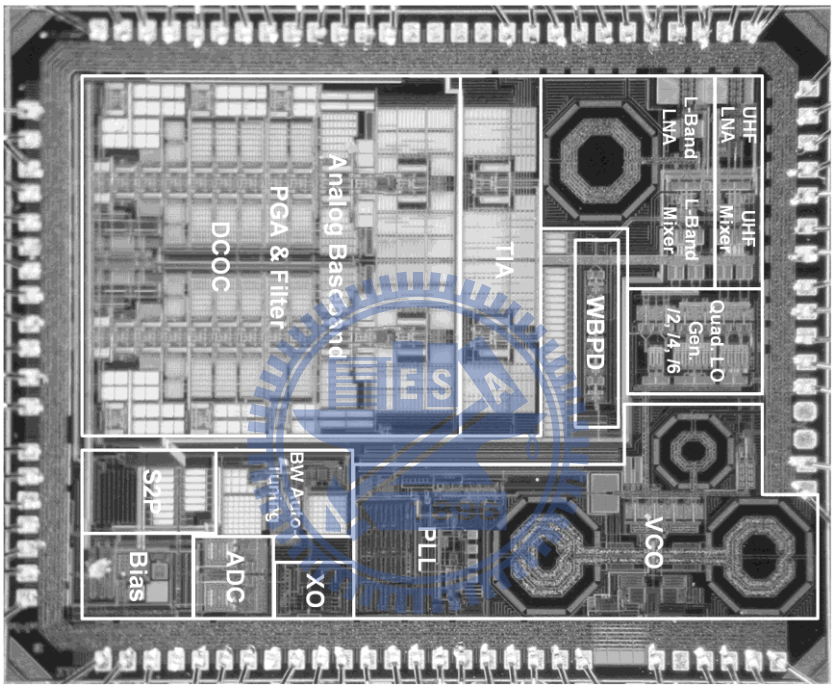


Fig. 5.14 Die photograph.

5.7 Measurement Results

The tuner chip was fabricated in 0.13-μm 1P8M CMOS process. It occupies a total silicon area of 7.2 mm^2 including all ESD pads. The chip is housed in a 5x5 mm^2 40-pin QFN package. The micrograph of the die is shown in Fig. 5.14, where the analog baseband occupies a significant portion of the chip area due to using low-density MIM capacitors of 1fF/um^2. A single 1.2 V supply is applied for the measurement. The measured performance referred to the SMA connector input is summarized in Table 5.1.

The measured NF ranges from 3.7dB to 4.3dB in the UHF band. The stated IIP3 values are measured, applying two-tone frequencies at 13.25MHz and 29.25MHz away from the desired frequency, whereas, for the IIP2, a two-tone test with blockers at 13.25MHz and 16MHz offset was performed. At 11dB back-off from maximum RF gain, which is convergent by the RSSI-AGC loop for L3 blocking test, IIP3 is -4.3dBm while NF is 8.7dB. The current switch path provides a 15dB RF gain backoff, achieving a baseband IIP2 of 50dBm in the UHF band.

The overall NF versus the RFE and ABB gain settings are measured and shown in Fig. 5.15. It is noted that as the ABB gain is towards 0dB, the contribution of the measurement instruments such as the differential probe and spectrum analyzer becomes much dominant. This means that the measured NF is much larger than the real case. Fig. 5.16 illustrates the measured NF at different IF frequency. As can be seen, the flicker noise corner is around 200 kHz.

The measured phase noise spectrum at the synthesizer output is as shown in Fig. 5.17. The noise profile will be lowered by 15dB after a /6 divider for 626MHz channel, resulting in an integrated noise from 400Hz to 4MHz better than 0.3 degrees. The measured transient frequency response during the locking process is depicted in Fig. 5.18, showing a locking time of 78μsec including coarse and fine tuning. The locking time is still less than 100μsec in the worst case of the power-up sequence. The C/N plot at the baseband output, evaluated in terms of EVM, is exhibited in Fig. 5.19 by applying an input signal of the 16-QAM 1/2 modulation scheme. The SNR shown is better than 30dB from -70dBm to -7dBm, allowing for robust operation in a mobile environment. Because the BER test (system performance) depends on not only the radio chip but also the baseband demodulator, the estimates in sensitivity, selectivity, and linearity tests are given according to the measured MER not exceeding one specific value based on the modulation scheme defined in the MBRAI specification. In Table 5.2 summarized are these measurement results.

Compared with the previously reported work related to DVB-H tuner, shown in Table 5.3, this chip achieves the lowest power consumption from a single 1.2V supply while maintaining comparable performance. The maximum power consumption is 114mW in the UHF band as all circuits are activated in the continuous mode. However, the power consumption reduces to 103mW in the L-band. The reduced power mainly results from the operation with divide-by-2

instead of divide-by-6 as well as no usage of RF power detector.

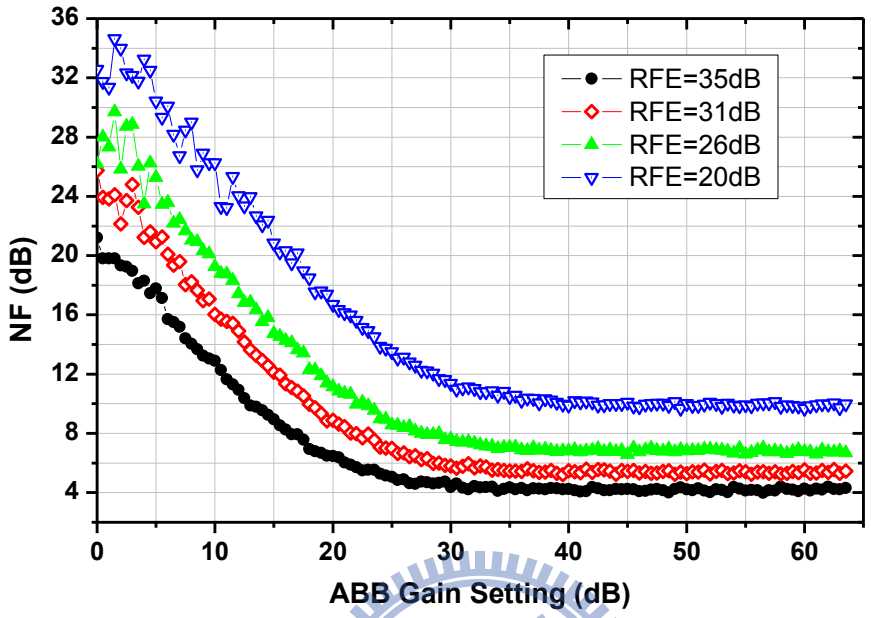


Fig. 5.15 Measured overall NF versus the RFE and ABB gain settings.

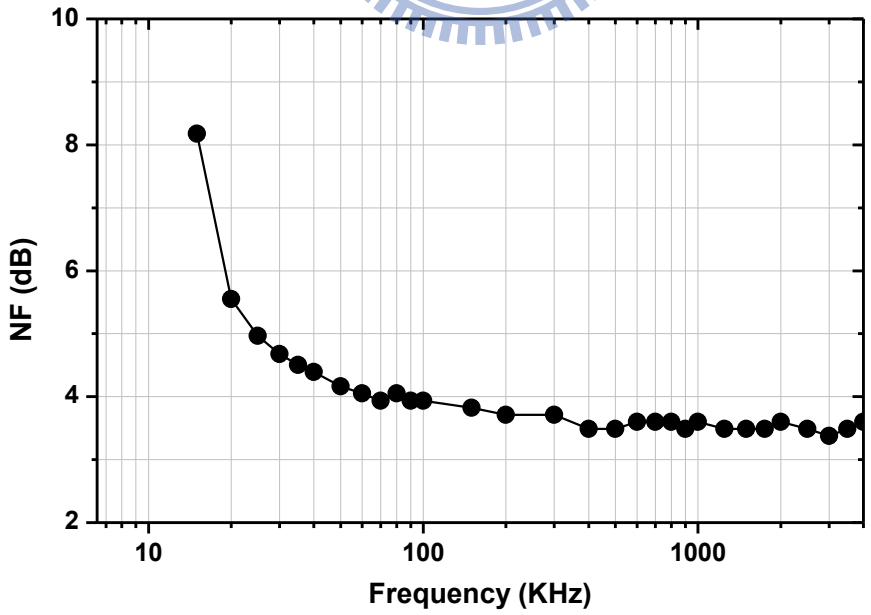


Fig. 5.16 Measured NF at different IF frequencies.

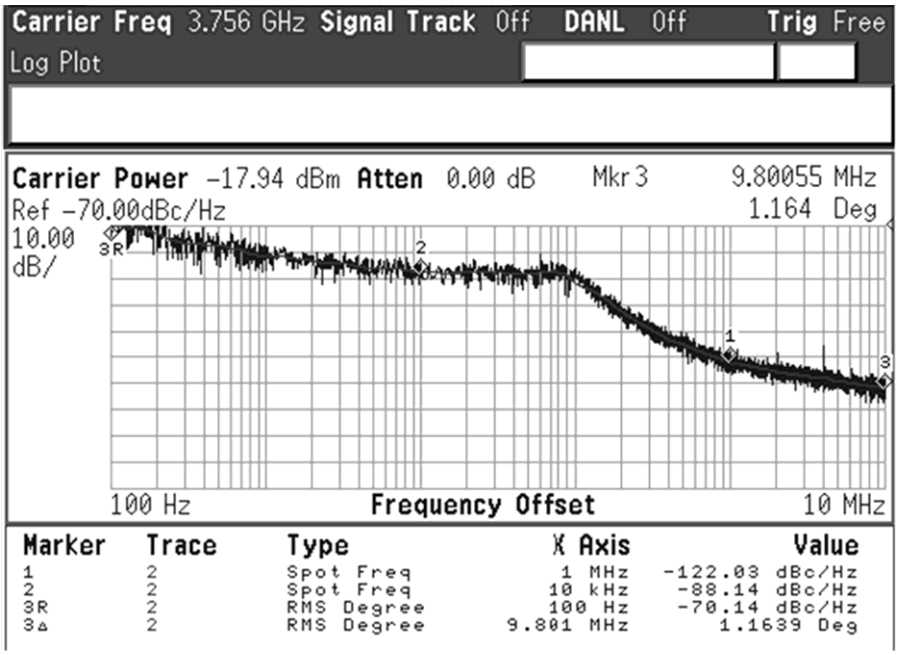


Fig. 5.17 Phase noise profile measured at synthesizer output.

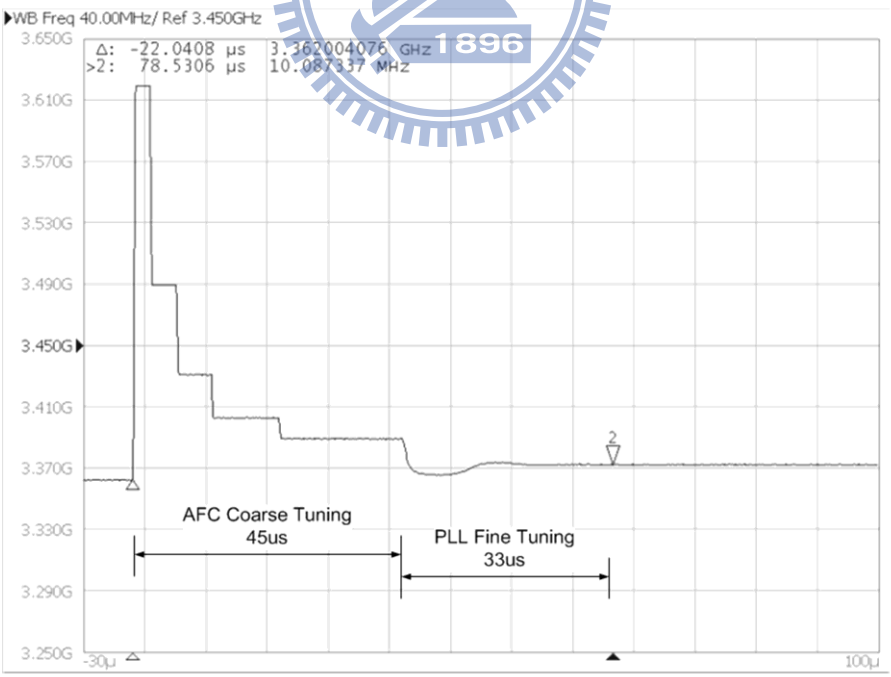


Fig. 5.18 Measured locking process of frequency synthesizer.

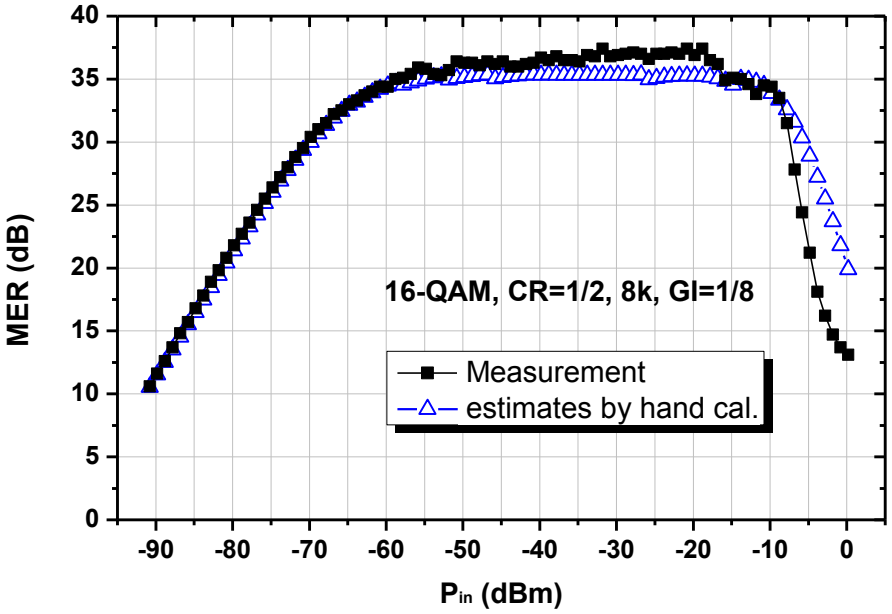


Fig. 5.19 Measured C/(N+I) vs. input power for the test chip comprising digital front-end.

Table 5.1
PERFORMANCE SUMMARY OF RF TUNER

Frequency Band (MHz)	**UHF-band (470–862MHz)**	**L-band (1670–1675MHz)**
Input Return Loss (dB)	<-12	<-12
Gain Max/Min/Step (dB)	95/-5/0.5	100/10/0.5
RF range/BB range (dB)	40/63.5	30/63.5
NF @ Max Gain (dB)	3.7~4.3	4.3
NF @ (Max RF -15dB) (dB)	9~10.5	13 [(a)]
IIP2 (N+2) @ Max Gain/ (Max RF -15dB) (dBm)	+35/+50	+27/+46 [(a)]
IIP3 (N+2,N+4) @ Max Gain/ (Max RF -15dB) (dBm)	-13/+5	-13/+8 [(a)]
Integrated phase noise (100-4MHz)	0.5° rms	1° rms
Filter rejection with 4MHz BW setting @ 5.25/13.25MHz	32/102 (dB)	
DC offset	6mV	
I/Q matching	<-35dBc	
Power consumption in continuous RX	114mW @ 1.2V	103mW @ 1.2V
Die size	7.2 mm^2 in 0.13 um CMOS	

[a] Measured at (Max RF -19dB).

Table 5.2
SELECTIVITY/LINEARITY AND SENSITIVITY MEASUREMENT RESULTS

Pattern	Modulation	Interferer location	U/D (dB) Spec.	U/D (dB) Measured
S1 (PAL-G)	8k 64-QAM 3/4	N+1	35	42
		N-1	35	43
		N+2	43	46.5
		N-2	43	46.5
S2 (PAL-G)	8k 64-QAM 3/4	N+1	27	35
		N-1	27	35
		N+2	40	45
		N-2	40	45
L1	8k 16-QAM 2/3	N+2, N+4	40/45	42.8/47.8
L2	8k 16-QAM 2/3	N+2, N+4	45	46.7
L3	8k 16-QAM 2/3	N+2, N+4	40	41.8
	Modulation	**C/N (dB)**	**Spec. (dBm)**	**Measured (dBm)**
Sensitivity	8k 64-QAM 3/4	19.9	-81.3	-80.9
	8k 16-QAM 2/3	12.7	-88.5	-88.4
	8k QPSK 1/2	4.6	-96.6	-96.7

Table 5.3
BENCHMARK OF RF TUNERS FOR DVB-H APPLICATIONS

Ref.–Year	Process	Power (mW)	Vdd (V)	Aerea (mm^2)	Band	NF (dB)	IIP3 (dBm)	IIP2 (dBm)	Phase Noise
[1] JSSC '05	0.35μm SiGe:C	240	2.775	11.5	UHF	8.5	+12 (Max RF-20dB)	+45	0.8°
[2] ISSCC '06	0.35μm SiGe	340	2.7	12.3	UHF L-Band	3.6	+4 (Max RF-20dB)	+27	0.3°
[3] JSSC '07	0.5μm SiGe	184	2.8	16	UHF	3.1 - 4.6	-6.8 (Max RF-8dB)	N/A	N/A
[5] ISSCC '06	0.18μm CMOS	295	2.7	9.7	UHF L-Band	3.5 [a]	-0.5 (Max RF-10dB)	+34	0.3°
[4] ISSCC '06	0.18μm CMOS	185	2.8	7.8	UHF L-Band	4.5	-5 (Max RF-0dB)	+40	1.0°
[6] JSSC '08	65nm CMOS	138	1.2/2.5	7	UHF/VHF L-Band	2.2 - 3.2	-3 (Max RF-5dB)	+40 [b]	0.5°
This work	0.13μm CMOS	114	1.2	7.2	UHF L-Band	3.7 – 4.3	+5 (Max RF-15dB)	+50	0.5°

[a] 5dB Noise Figure is measured at the channel above 800MHz.
[b] Measured at (Max RF -10dB).

5.8 Conclusion

A 1.2V highly integrated RF tuner for DVB-T/H applications in 0.13-μm CMOS technology is demonstrated. Utilizing a direct-conversion structure and a smart frequency plan, the tuner consumes only 114mW in the continuous mode and occupies a silicon area of 7.2 mm^2. Together with system and circuit design techniques, this tuner complies with the MBRAI 1.0 requirement, while slightly insufficient to meet the stringent MBRAI 2.0 specifications. However, low BOM as well as small PCB size are achieved, requiring a minimum number of external components: an inductor and a coupling capacitor for each LNA input, a crystal, and RC components for the loop filter. Since the supply voltage is as low as 1.2V, it is straightforward to convert to advanced technologies of 65nm and beyond towards a more competitive SoC solution.

Chapter 6

65nm Tuner Implementation and Verification

Current and future trends call for the highest levels of integration to achieve low cost and low power for handheld wireless devices. Such demands drive nanometer digital CMOS as the process of choice to integrate digital, mixed-signal, and RF components on a chip. For system-on-a-chip (SoC) solutions, the digital part usually occupies a significant part of chip area and consumes much power compared to the mixed-signal and RF parts [64], [65], [66], [67]. New CMOS technology nodes can bring great strides within the digital part in reduced cost, higher speed, and lower power consumption. These benefits also push more and more RF and mixed-signal components to be developed in nanometer CMOS technologies, towards a SoC evolution. This chapter introduces the impacts of technology scaling on RF/mixed-signal design. The previous 0.13-μm CMOS tuner has been migrated to 65nm for SoC integration. New features in this 65nm CMOS tuner will be highlighted in this chapter. In addition, chip verification will be also described in more details.

6.1 Effects of Technology Scaling

For RF and mixed-signal components, technology scaling is a mixed blessing [68]. High-frequency operation typically benefits from the scaling as the transit

frequency f_T continues to scale up with the reduced feature size. However, this comes along with worse performance parameters, including high leakage current, reduced intrinsic gain, large 1/f noise, reduced headroom, and severe substrate coupling. Such issues still need to be addressed in RF and mixed-signal design [69], [70].

Table 6.1 Device sizes in the designed LNAs

	0.13μm	65nm (feature size)	65nm
M_1, M_2 (in μm)	(2.5/0.13)×13×4	(2/0.065)×15×4	(2.5/0.13)×21×4
M_3, M_4 (in μm)	(2.5/0.13)×13×2	(2/0.065)×15×2	(2.5/0.13)×21×2
C_1, C_2 (pF)	10	10	10
C_{c1}, C_{c2} (pF)	1.5	1.5	1.5
R_1, R_2 (kΩ)	20	20	20
R_3, R_4 (kΩ)	10	10	10
R_{L1}, R_{L2} (Ω)	275	275	275

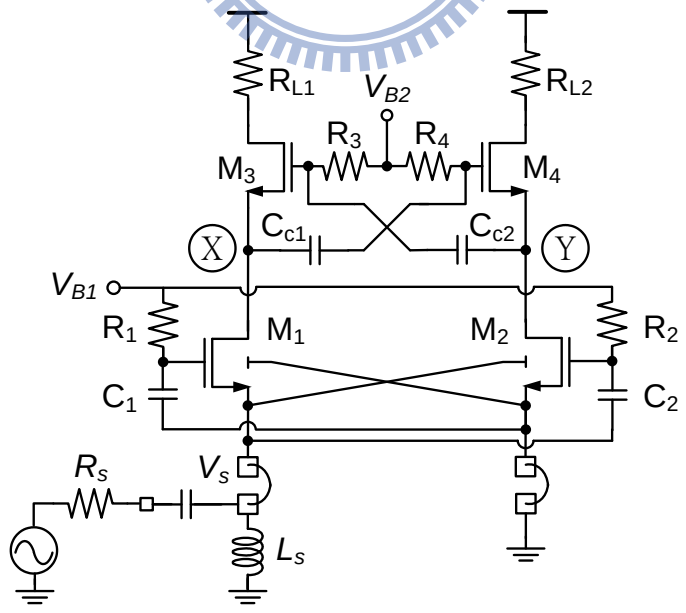


Fig. 6.1 Simplified schematic of the designed LNAs.

To evaluate the impacts of technology scaling on the RF/mixed-signal circuits, the design of our proposed LNA in chapter 4 is used as an example. Fig. 6.1 shows the circuit schematic. Three cases are studied to verify the effects of technology scaling. As shown in Table 6.1, the LNA is designed with different device dimensions in both 0.13μm and 65nm CMOS technologies. Two cases are implemented in 65nm CMOS, in which one is with the minimum feature size, and the other utilizes transistors with 0.13μm length.

As discussed in chapter 4, the LNA performance, such as voltage gain, input return loss and NF, directly depends on the choice of M_1/M_2 parameters. Table 6.2 shows this information of the designed LNAs. For these three cases, M_1/M_2 transistors have the same input transconductance of 25mS. They are biased in the moderate inversion region with 10mV－20mV overdrive voltage (V_{GS}-V_T). As can be found, the transistor's intrinsic gain decreases with the technology scaling. The case with 65nm feature size shows 0.36 times of intrinsic gain as compared with the 130nm case. Low intrinsic gain degrades analog performance. To increases transistor's intrinsic gain in nanometer technology, the use of a larger transistor length is favorable. Here, the third case realizes the LNA with 130nm channel length, rather than 65nm feature size. Another dominant factor to our proposed LNA is the benefit from the body transconductance. As can be seen, g_{mb} in 65nm technology is only one half of that in 130nm technology. This means a smaller effective transconductance (g_m+g_{mb}) in 65nm technology, leading to smaller voltage gain, poor NF, but better input matching. Fig. 6.1 shows the simulated S_{11}. The poor performance at lower frequencies results from small source inductance *Ls* of 22nH. The simulated voltage gain and NF are illustrated in Fig. 6.3 and Fig. 6.4, respectively. As can be seen, the design in 0.13μm CMOS has the best performance over the other two. As to 65nm cases, the design in use of 130nm length is better than that with 65nm feature size. As a result, devices with minimum feature sizes are barely used in realization of 65nm tuner design.

Table 6.2 Operation parameters of M_1/M_2 in the designed LNAs

Technology Nodes	0.13μm		65nm (feature size)		65nm	
W/L (M_1, M_2)	130 / 0.13	×1	128 / 0.065	×1.97	210 / 0.13	×1.62
I_D(mA)	1.57	×1	1.67	×1.06	1.51	×0.94
g_m (mS)	25.2	×1	25.2	×1	25.4	×1
g_{mb} (mS)	5.46	×1	2.24	×0.41	2.71	×0.49
g_{ds} (mS)	1.12	×1	3.11	×2.78	1.31	×1.17
C_g (fF)	142	×1	106.3	×0.75	253	×1.78
g_m/g_{ds}	22.5	×1	8.1	×0.36	19.4	×0.86
f_T (GHz)	28.2	×1	37.7	×1.34	23.4	×0.83
Vt (mV)	419	×1	414	×0.99	373	×0.89
Vdd (V)	1.2	×1	1.2	×1	1.2	×1

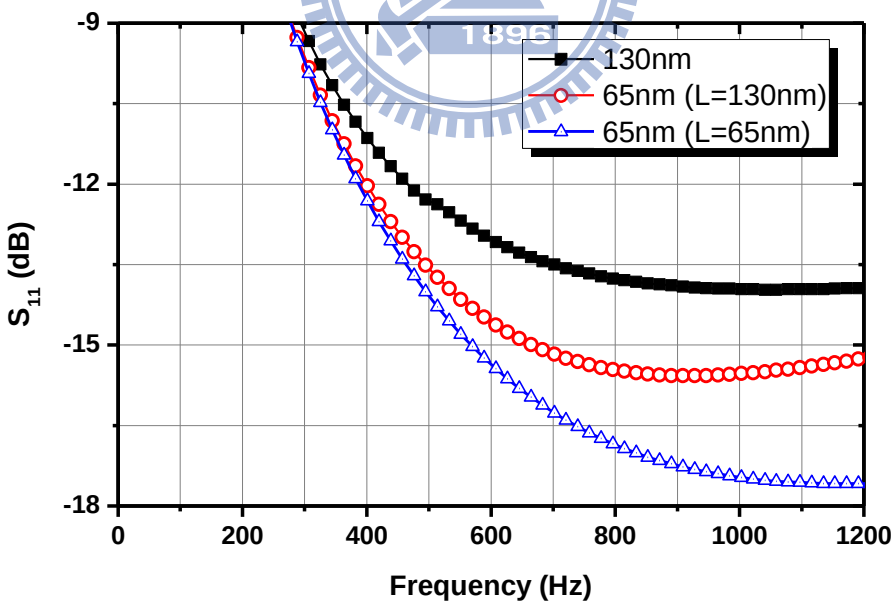


Fig. 6.2 Simulated S11 of the designed LNAs.

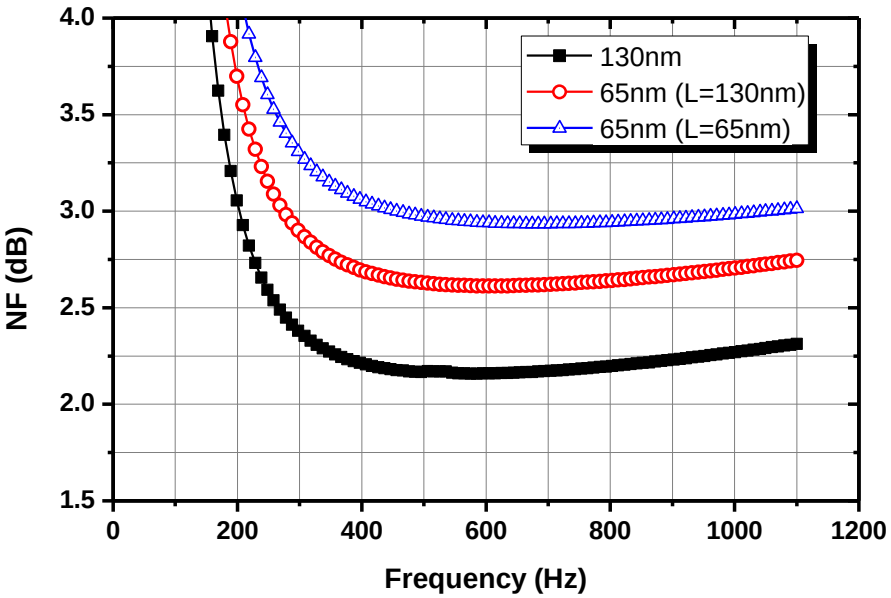


Fig. 6.3 Simulated NF of the designed LNAs.

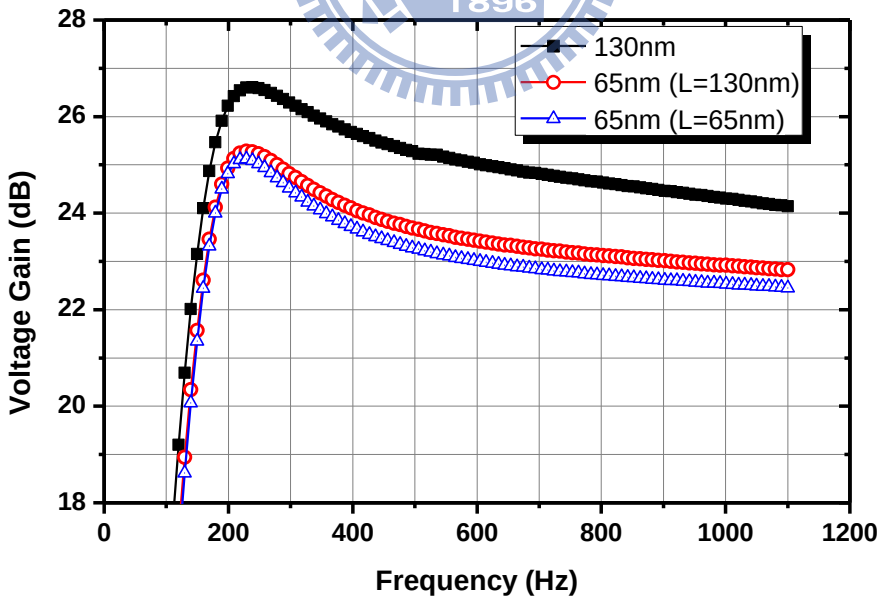


Fig. 6.4 Simulated voltage gain of the designed LNAs.

6.2 65nm Tuner with Reconfigurable Inputs

Towards a SoC evolution, the previous 0.13-μm CMOS tuner has been migrated to a 65nm CMOS technology. Based on the same architecture, the first tuner integrates the proposed LNA (in chapter 4) with reconfigurable inputs to adapt to the possibly noisy SoC environment. Fully differential topologies from the LNA input to the baseband output can be configured to have high immunity to digital switching noise. If the noise disturbance is not as severe as predicted, however, the LNA can be configured as a single-ended input receiving. As such, the external balun can be eliminated to reduce the BOM. The single-ended configuration is also highly preferred if some performance degradation could be acceptable in applications sensitive to cost and area [31]. The tuner chip is fabricated in 65nm 1P6M LP CMOS process. It occupies a total silicon area of 7.8 mm^2 including all ESD pads. Fig. 6.5 shows the die micrograph of the chip.

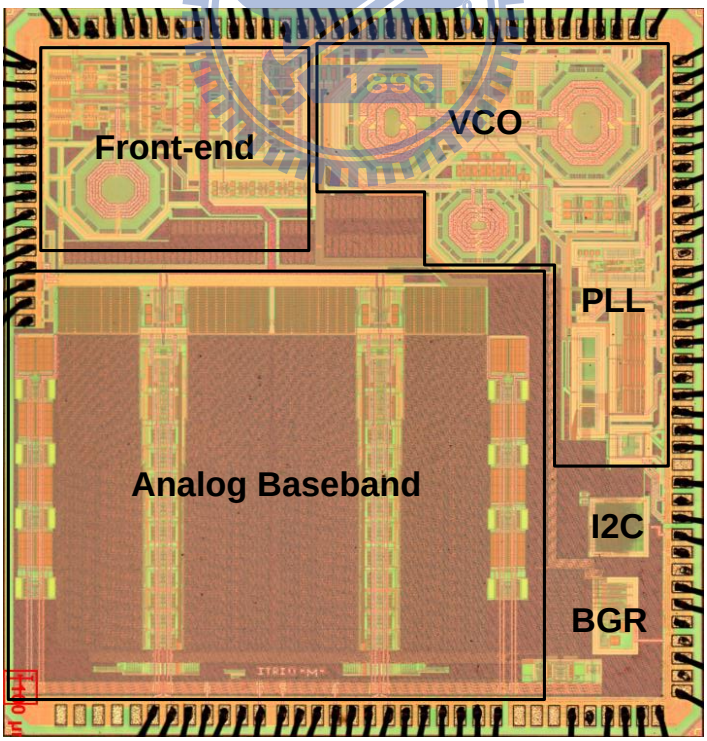


Fig. 6.5 The die micrograph of the chip.

6.3 Flowchart of Chip Verification

The simplified block diagram of testing chip is shown in Fig. 6.6, where a differential configuration is shown at the UHF-band input and a single-ended configuration is shown at the L-band input. The flowchart of chip verification is shown in Fig. 6.7. First, the chip is bonded on a FR-4 PCB (COB) for performance verification. The photograph of the actual PCB for the COB test is shown in Fig. 6.8. Initially, DC conditions are measured to verify the difference from the simulation values. After the DC conditions and I2C programming have passed the verifications, performance parameters of either the receiver chain with external LO or the PLL block should be measured. Then, the integrated receiver tests with the internal LO should be done. Until now, continuous-wave (CW) signals are applied to the measurements. Once we have finished the CW tests, system performance such as sensitivity, linearity, and selectivity, should be verified by applying a modulated signal. One major task to deal with during the COB verification is to determine the bonding diagram for the chip package. Several on-chip supply pads would be bonded on the same package pin to reduce pin counts. This is an iterative procedure. As a specific bonding diagram is wired, and again, CW and system performance should be verified completely. Finally, the chip die is housed in a commercial package. Fig. 6.9 depicts the bonding diagram in a 6x6 mm^2 40-pin QFN package. As can be seen, many package pins contain more than one wiring. The photograph of the actual PCB for final package test is depicted in Fig. 6.10. In addition to the above-mentioned items, more complete test should be performed, including the reliability test against temperature variations.

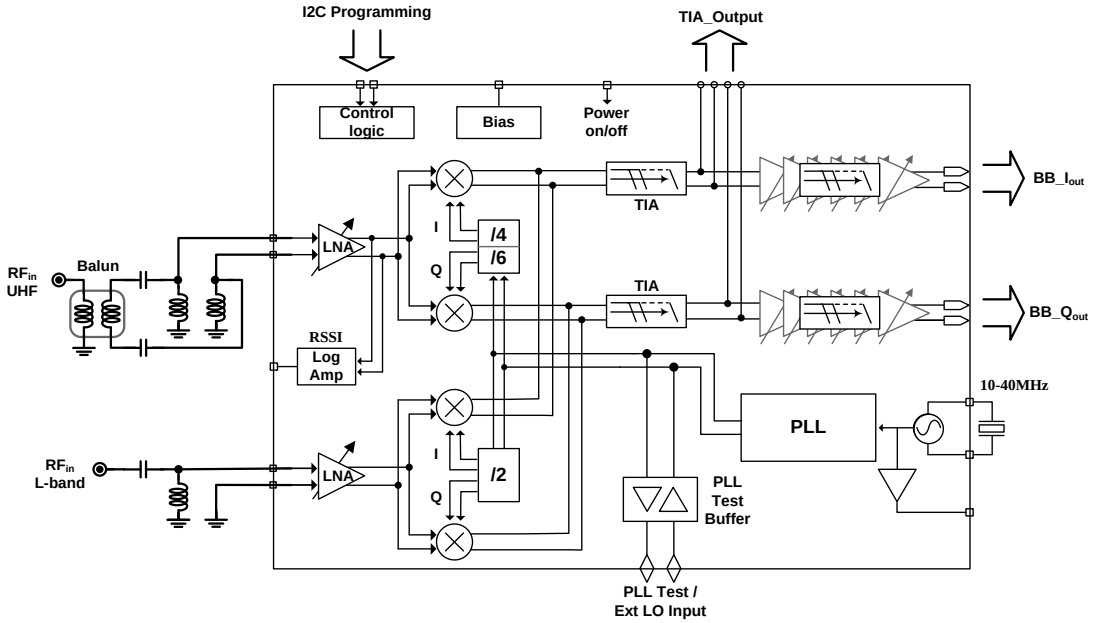


Fig. 6.6 Simplified block diagram of testing chip.

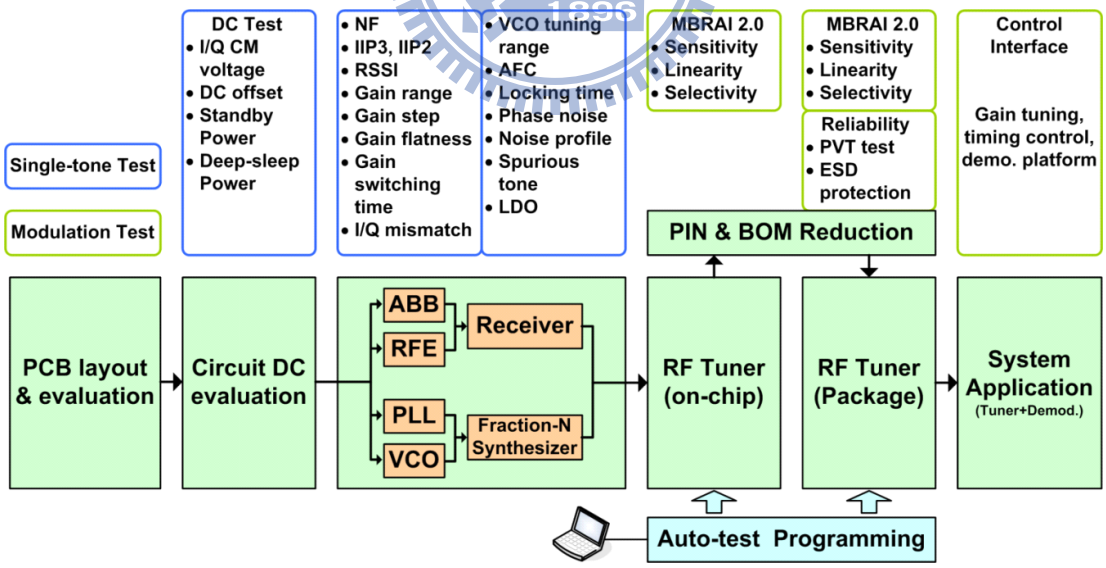


Fig. 6.7 Flowchart of chip verification.

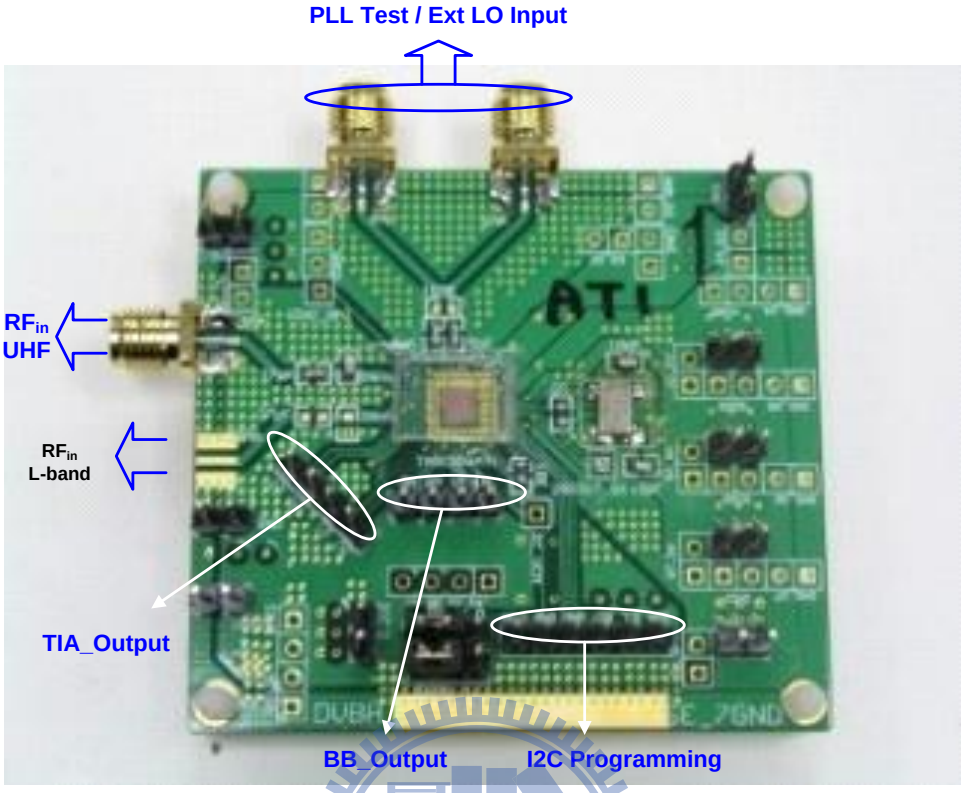


Fig. 6.8 The photograph of the actual PCB for COB test.

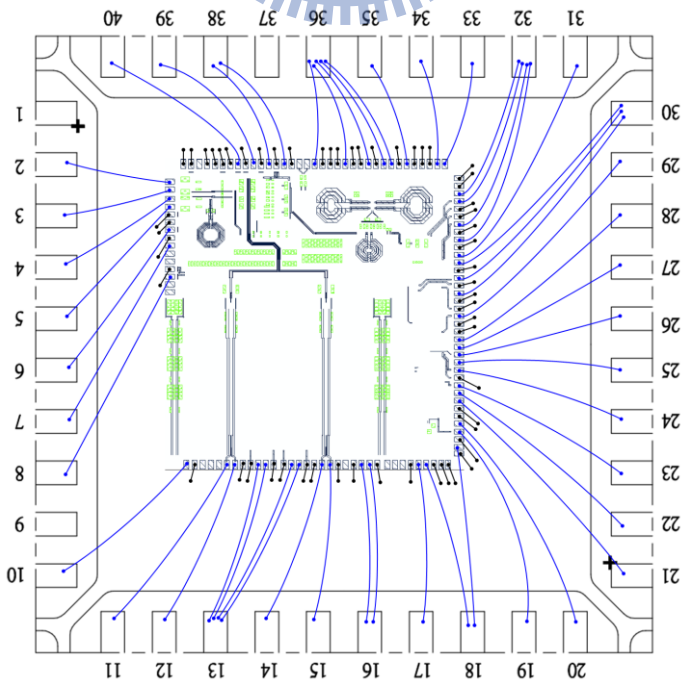


Fig. 6.9 Bonding diagram in a 40-pin QFN package.

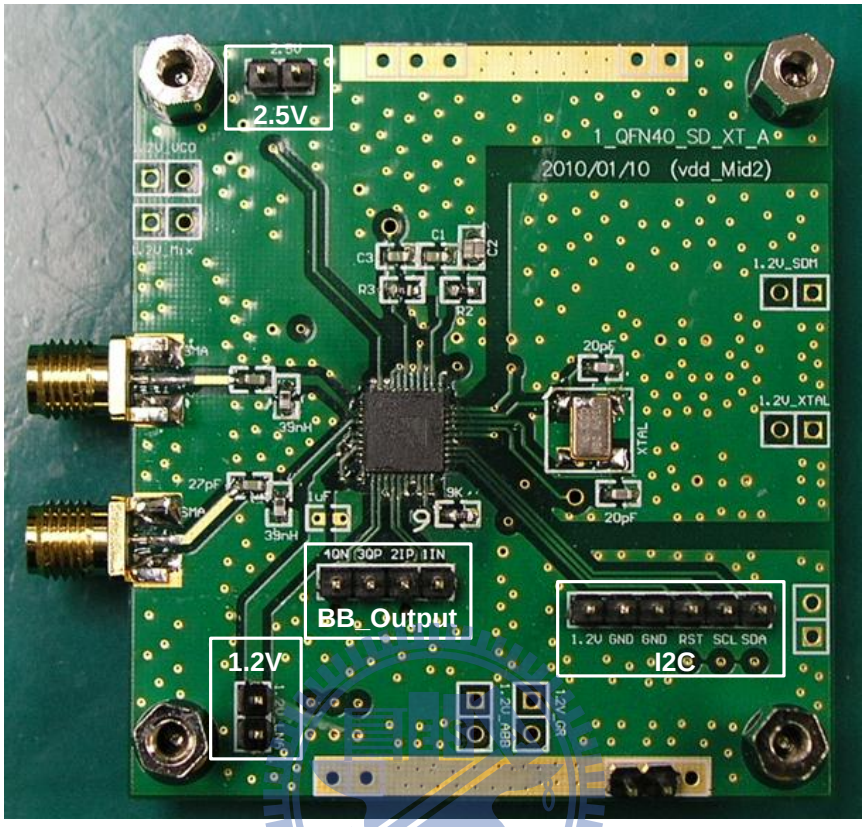


Fig. 6.10 The photograph of the actual PCB for package test.

6.4 Noise Immunity in a Differential or a Single-ended Configuration

To evaluate the impact of digital switching noise on the sensitive RF input, a poor PCB layout is especially developed, where the RF and digital circuits directly share common power/ground planes. More specifically, all power/ground pads from the RF, mixed-signal, and the digital parts are directly connected together without any separation and de-coupling. Such PCB layout features the noise coupling effect between the RF and digital part and can be applied to verify the ability of noise immunity in a single-ended and a differential mode. Fig. 6.11 and Fig. 6.12 depict the output SNR as the RF input is configured as a single-ended mode and a differential mode, respectively. The results are obtained by measuring the baseband output of the

receiver with the integrated PLL in an integer-N mode. The digital part such as the sigma-delta modulator is used as the switching noise source to observe its impact on the SNR degradation. As can be seen in Fig. 6.11, as the digital switching circuit is turned on, the output noise floor is raised by 10.2dB in a single-ended mode. As shown in Fig. 6.12, on the other hand, the output noise floor is raised by 1.75dB in a differential mode. Eq. (6.1) can be used to calculate the injected noise components and then evaluate the rejection ratio of the differential over the single-ended mode.

$$NF = \frac{N_o}{GN_i} = \frac{N_{o,sw}}{G(N_i + N_{inj})} \tag{6.1}$$

where $N_i=kTB$ is the thermal noise power, N_o is output noise as the digital switching circuits is disabled, and N_{inj} denotes the injected noise component referred to the RF input, $N_{o,sw}$ is output noise as the digital switching circuits is activated. Eq. (6.1) can be written as

$$\frac{(N_i + N_{inj})}{N_i} = \frac{N_{o,sw}}{N_o} \tag{6.2}$$

From (6.2), we can get that the injected noise power is 9.5 times of the thermal noise power in a single-ended mode, while only one half of the thermal noise power in a differential mode. This means that the differential mode has higher noise immunity, which is 13dB better than the single-ended mode.

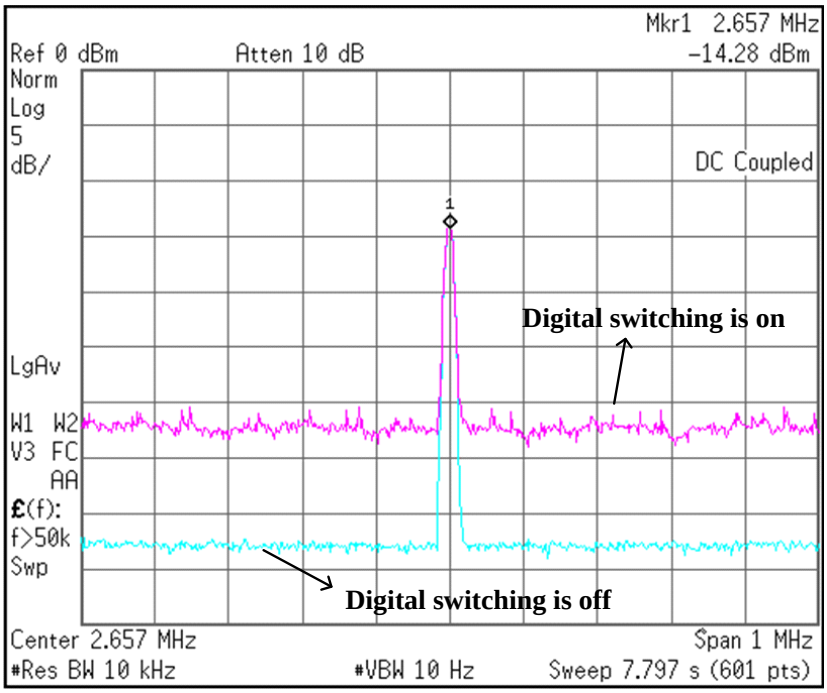


Fig. 6.11 Output SNR in a single-ended mode as the digital part is on/off.

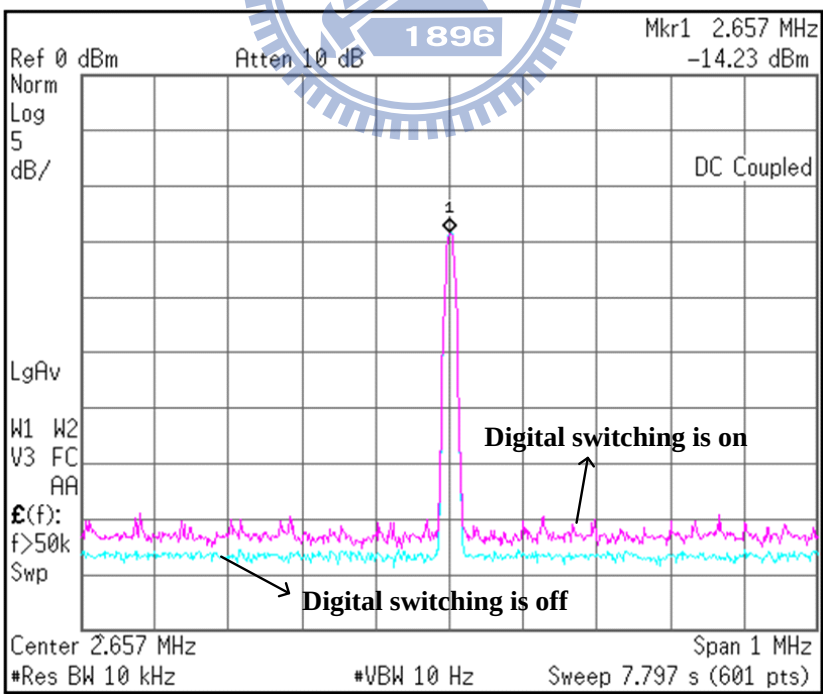


Fig. 6.12 Output SNR in a differential mode as the digital part is on/off.

6.5 Considerations on PCB Layout

As mentioned in the section 5.6.1, noise coupling via the path either on the chip or the board may significantly degrade the signal quality. For this chip, the tuner needs to receive a -96.6dBm signal at its RF input port in the presence of 1.2V digital switching noise. Since the magnitude difference between the digital and RF signal can be as large as 0.1 million (100 dB), the sensitive RF signal may be corrupted by the large digital noise without proper separations and shielding. Special attentions on the reduction of on-chip noise coupling [71] is applied by use of the additional *deep N-well shielding* [72] and block separation as distant as possible. In addition to the on-chip issue, the printed circuit board (PCB) design is also important to an RF integrated system.

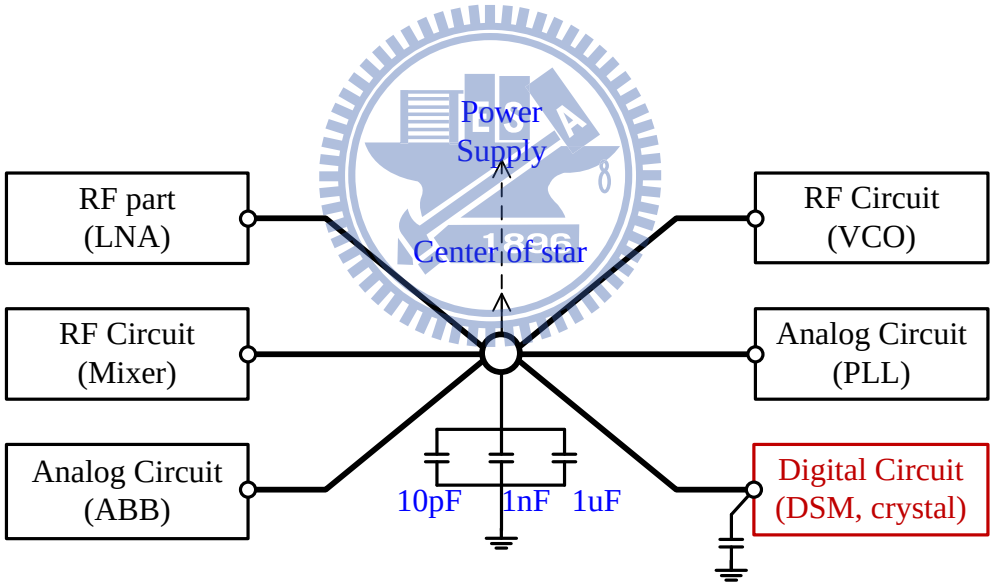


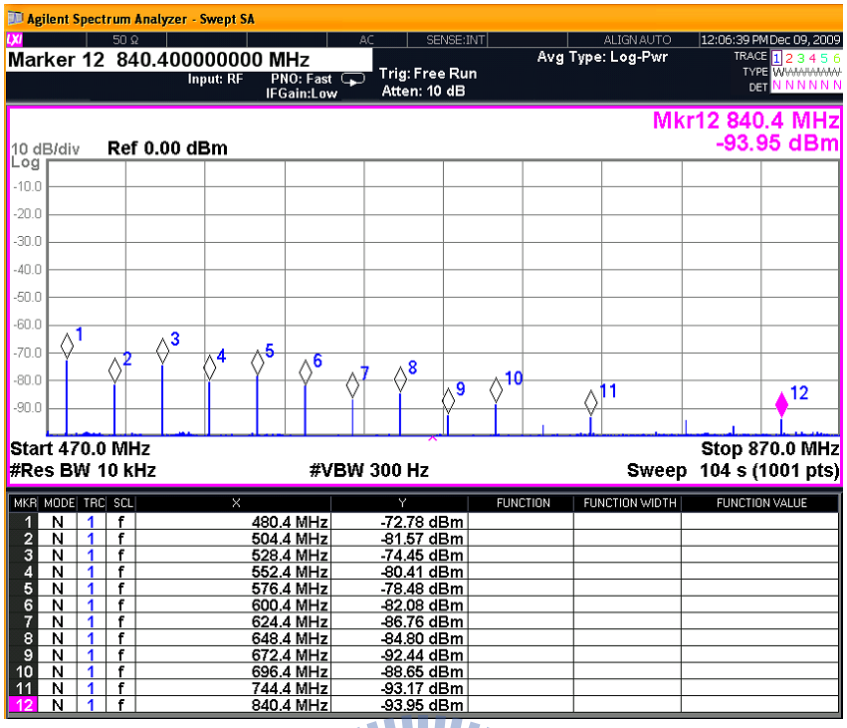
Fig. 6.13 A star configuration of VDD pins.

The PCB layout significantly affects the performance, stability and reliability of the wireless system. One critical issue to be concerned with is the power supply routing on PCBs. Noise propagation via the low-impedance power and ground traces needs more attentions to alleviate. To minimize coupling between different domains of the IC, a star configuration is widely adopted for the power-supply layout [73], [74].

As shown in Fig. 6.13, decoupling capacitors are placed at the central V_{DD} node, and the power traces branch out from this node, with each trace going to separate supply pins. Typically, each supply pin must have a bypass capacitor placed as close as possible to the pin with low impedance to ground at the frequency of interest. To reduce the BOM, some experiments can be applied to determine the essentially required bypass capacitors. To our experiences, the bypass capacitor at the supply pin of the digital switching circuit should not be eliminated, which shows significant benefits on suppressing the noise source.

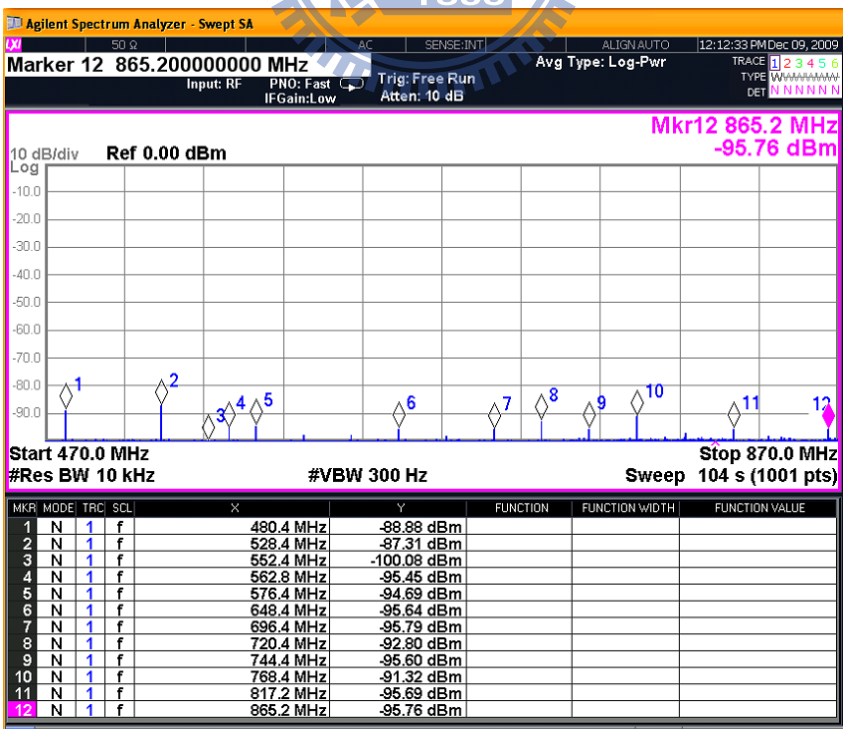
To evaluate the issues of PCB layout, two types of PCB are implemented. One directly shares common power/ground planes among the RF and digital circuits. The other one has separate power/ground planes among the RF and digital circuits as shown in Fig. 6.8. It follows the star routing rule in the supply connections of the RF and digital domains to sink the supply source. Fig. 6.14 and Fig. 6.15 depict the measured spectrum at the RF input port of these two boards, respectively. In this test, the tuner is configured in a single-ended mode and all circuit blocks are activated in the normal operation mode. High-order harmonics leakages from the clock switching to the RF input port are then measured. From the measurement results, it can be found that an extra isolation of 16dB can be achieved using separate power planes in contract to the common planes for the dominant components below 600MHz. It should be noted that the coupling mechanism is dominated by the board level, rather than the chip level from our experiments. Almost the same spectrum is observed as we remove the bonding wire of the RF input pad or disable the LNA bias current.

A star configuration has been demonstrated an efficient way of isolating power noise propagation from the digital part to the RF part. If the board contains an extremely noisy part, inductors or resistors can be placed in series with the power supply trace of these noisy parts to provide a higher level of isolation.



MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	480.4 MHz	-72.78 dBm			
2	N	1	f	504.4 MHz	-81.57 dBm			
3	N	1	f	528.4 MHz	-74.45 dBm			
4	N	1	f	552.4 MHz	-80.41 dBm			
5	N	1	f	576.4 MHz	-78.48 dBm			
6	N	1	f	600.4 MHz	-82.08 dBm			
7	N	1	f	624.4 MHz	-86.76 dBm			
8	N	1	f	648.4 MHz	-84.80 dBm			
9	N	1	f	672.4 MHz	-92.44 dBm			
10	N	1	f	696.4 MHz	-88.65 dBm			
11	N	1	f	744.4 MHz	-93.17 dBm			
12	N	1	f	840.4 MHz	-93.95 dBm			

Fig. 6.14 Clock leakage to the RF input with shared power/ground planes.



MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	480.4 MHz	-88.88 dBm			
2	N	1	f	528.4 MHz	-87.31 dBm			
3	N	1	f	552.4 MHz	-100.08 dBm			
4	N	1	f	562.8 MHz	-95.45 dBm			
5	N	1	f	576.4 MHz	-94.69 dBm			
6	N	1	f	648.4 MHz	-95.64 dBm			
7	N	1	f	696.4 MHz	-95.79 dBm			
8	N	1	f	720.4 MHz	-92.80 dBm			
9	N	1	f	744.4 MHz	-95.60 dBm			
10	N	1	f	768.4 MHz	-91.32 dBm			
11	N	1	f	817.2 MHz	-95.69 dBm			
12	N	1	f	865.2 MHz	-95.76 dBm			

Fig. 6.15 Clock leakage to the RF input with separate power/ground planes.

6.6 Measurement Results

The measurement setup is shown in Fig. 6.16. An external LDO chip is applied to provide a single 1.2V supply to the tuner core, and a 2.5V to the I/O supply. The measured performance is referred to the SMA connector input for either the single-ended or differential receiving mode. In other words, the balun effect is included in the measured performance of the differential mode. The external balun components used for the measurement are TDK TCM12B51-900-2P-T [75] and TDK HHM1525 [76] for the UHF and L-band, respectively. Fig. 6.17 depicts the photograph of the actual PCB for the differential mode test.

Fig. 6.18 shows the measured S11 of the receiver in the single-ended and differential mode, respectively. The broadband characteristic can be observed in the single-ended mode, while a slightly band-selecting characteristic is shown in the differential mode due to the external balun. At the band of interest, however, the S11 is below -10dB for both two modes. The measured S11 is more reliable across the band of interest compared to that of the previous work which use inductively source degeneration LNAs and feature S11 worse than -6.5dB [64]. Fig. 6.19 depicts the measured gain flatness of the receiver across the band of interest. As can be seen, the receiver has a gain flatness of ±1.5dB, much better than the previous work which use inductively source degeneration LNAs and feature gain flatness larger than ±4dB [16], [31], [18]. As shown in Fig. 6.20, the UHF receiver features an NF of 3.3－3.8dB in the single-ended mode and 3.0－3.8dB (including the balun loss) in the differential mode. As the RF front-end has a gain back-off of 16dB, i.e., in the low-gain mode, the measured NF is shown in Fig. 6.21. The receiver features an NF of 8.8－9.6dB in the single-ended mode and 8.9－10.1dB in the differential mode.

Fig. 6.22 shows the measured IIP3 and IIP2 of the receiver in the single-ended mode. The receiver is set at the gain mode of RFE=max and ABB=50dB. The IIP3 values are measured by applying two-tone frequencies at 13.25MHz and 29.25MHz away from the desired frequency, which models from the test scenario of the L3 pattern. For the IIP2, whereas, a two-tone test with blockers at 13.25MHz and 16MHz offset is performed. This condition models from the test scenario of the S2 pattern. At the high-gain mode (RFE=max and ABB=50dB), the receiver achieves an

IIP3 of -11dBm and an IIP2 of +29dBm.

To observe the clock leakage within the band of each desired channel, some experiments are made. First, the tuner is activated in the normal operation mode, but the input is terminated to a 50-ohm termination load. Fig. 6.23 shows the measured spectrum at the baseband output under a tuner setting of 666MHz channel and a 93dB gain. As can be seen, one -15dBm tone is measured at 2MHz. This corresponds to a leakage component of -108dBm at 664MHz or 668MHz as referred to the RF port. Next, we apply a QPSK signal of -96.6dBm to the RF input, and measure the EVM per subcarrier of the signals as shown in Fig. 6.24. As can be seen, the MER at subcarriers around 2MHz is significantly deteriorated due to this leakage noise. It should be noted that the measured MER is validated using Rohde & Schwarz SFU broadcast test system (modulation signal source) together with ETL TV analyzer (VSA). Fig. 6.25 depicts the measured leakage components across the desired 49 channels as the RF input is configured as a single-ended mode and a differential mode, respectively. The measurement result shows that the leakage component to the RF port is less than -98 and -112dBm in the single-ended and differential mode, respectively. Such components show minor impacts on the signal quality.

Fig. 6.26 and Fig. 6.27 respectively show the phase noise spectrum measured at the synthesizer and the receiver baseband output at the 474MHz channel. The synthesizer output centered at 2844MHz achieves an integrated phase noise less than 1.06° (or -34.6dBc) from 400Hz to 4MHz. When a sinusoidal signal with a -40dBm power level at 473MHz frequency was applied to the RF input, the IF signal at 1MHz can be measured at the receiver baseband output. The receiver now has a gain setting: the maximum gain in the front-end and 0dB in the baseband. The integrated phase noise measured at 1MHz at the baseband output is 0.316° (or -45.2dBc) from 400Hz to 4MHz, which is about 10.6dB lower than the synthesizer output. In theory, the LO signal (after the /6 divider) should have a noise profile which is 15dB lower than that of the VCO signal. This can be found by comparing Fig. 6.26 with Fig. 6.27 at the in-band frequencies. At 400Hz, for example, the synthesizer output has a level of -76.9dBc/Hz, while the baseband output has a level of -91.9dBc/Hz. Indeed, the difference is 15dB. However, at the frequencies far away from the central frequency, which have noise level much lower than the central tone, the noise contribution from the receiver chain will dominate the overall noise level and raise the noise floor. This

can explain the significant difference from the theoretical value of 15dB at frequencies beyond the loop bandwidth.

System performance has been measured on the tuner IC along with a measurement demodulator (VSA). To verify the impact of RF impairments on the signal quality, the MER or EVM is measured as the figures of merit (FOM). EVM is the root mean square of the sum of error vector magnitudes (across all data carriers). In the case of additive white Gaussian (AWG) noise, MER and SNR are equal [48]. Because the BER test (system performance) depends not only on the radio chip but the baseband demodulator as well, the estimate is given according to the measured C/N of the radio chip not exceeding one specific value based on the modulation schemes in the MBRAI specification. In general, the validation with a companion demodulator chip achieves the reference BER equal to 2E-4 with a lower C/N requirement in the Gaussian channel. Thus, the listed performance related to sensitivity, linearity, and selectivity test would be better when the chip is validated with a companion demodulator.

Fig. 6.28 illustrates the measured constellation diagram as a modulated signal (64QAM, CR=3/4, GI=1/8, 8k-mode, BW=8MHz) is applied. The MER (EVM) per subcarrier is measured as shown in Fig. 6.29. The slight roll-off around the edges may result from the impairment of the analog baseband, such as frequency-dependent I/Q imbalance. The measured performance overview after the digital demodulation is shown in Fig. 6.30. The standard defines a minimum requirement on the BER before RS not exceeding 2E-4. The receiver MER (EVM) as a function of the input power level is shown in Fig. 6.31, where a 64-QAM 3/4 OFDM signal was applied. The measurement shows that –81.4dBm/-81.5dBm sensitivity for the single-ended and differential mode is achieved. Similarly, the measurement result with a QPSK 1/2 modulation signal is shown in Fig. 6.32. The measurement shows that -97.5dBm/-97.7dBm sensitivity in the single-ended and differential mode is achieved. As can be seen, the MER better than 30dB ranges from -70dBm to -8dBm, allowing for robust operation in a mobile environment. Moreover, the differential mode shows a wider dynamic range due to its better linearity as the RF front-end is set at the minimum gain mode.

The measured performance is summarized in Table 6.3, including the single-end and differential modes. Table 6.4 presents the measurement results related to the

selectivity and linearity patterns based on the MBRAI 2.0 specification. The result shows that this tuner chip complies with the requirement.

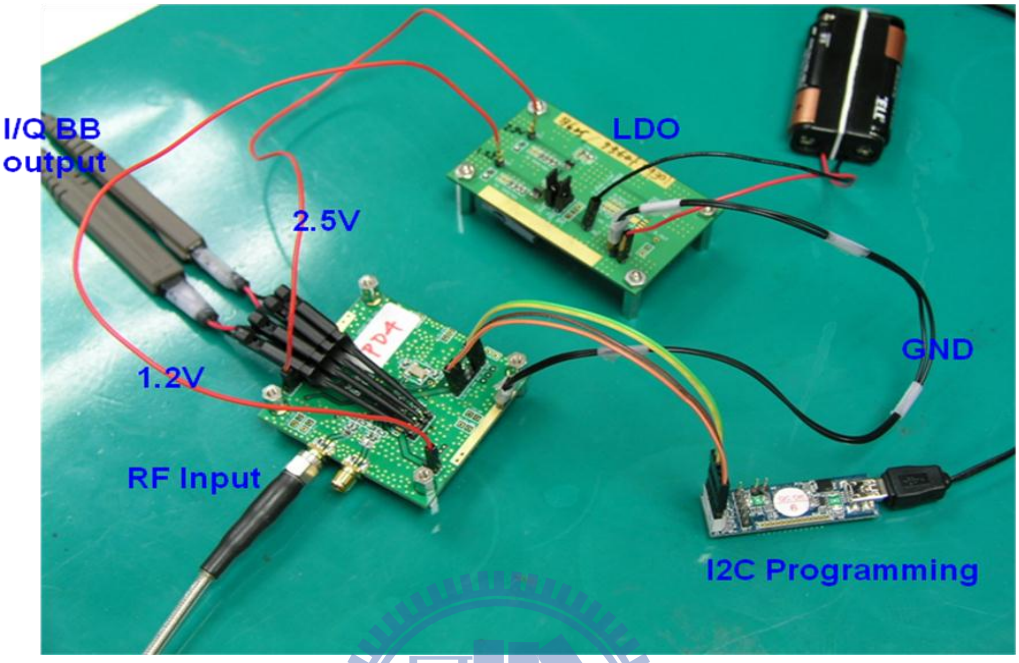


Fig. 6.16 Measurement setup with an external LDO.

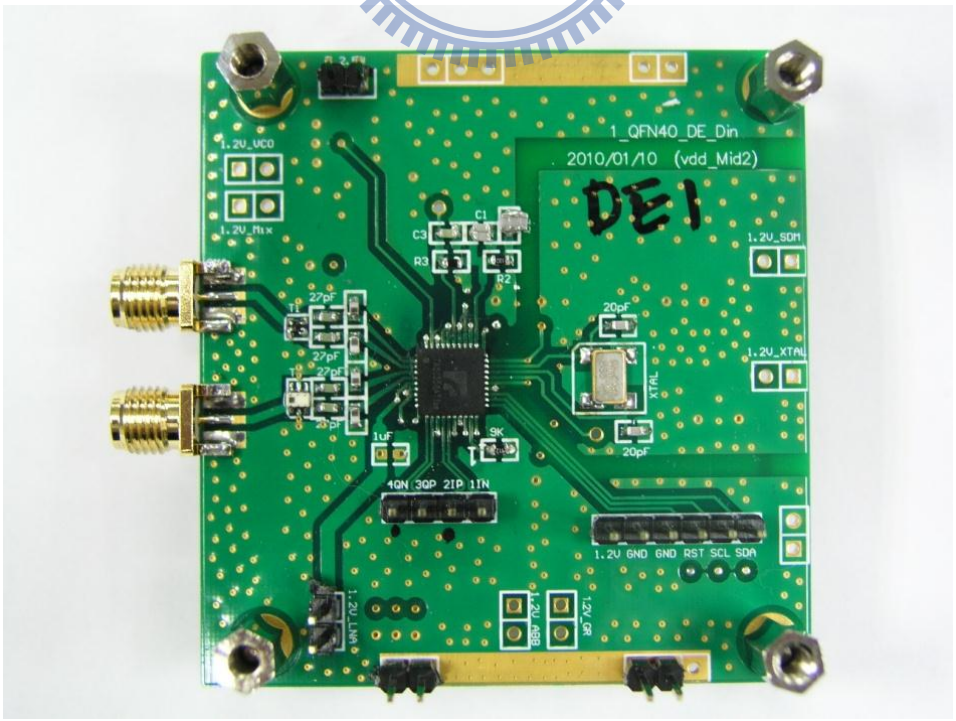


Fig. 6.17 Photograph of actual PCB in the differential receiving mode.

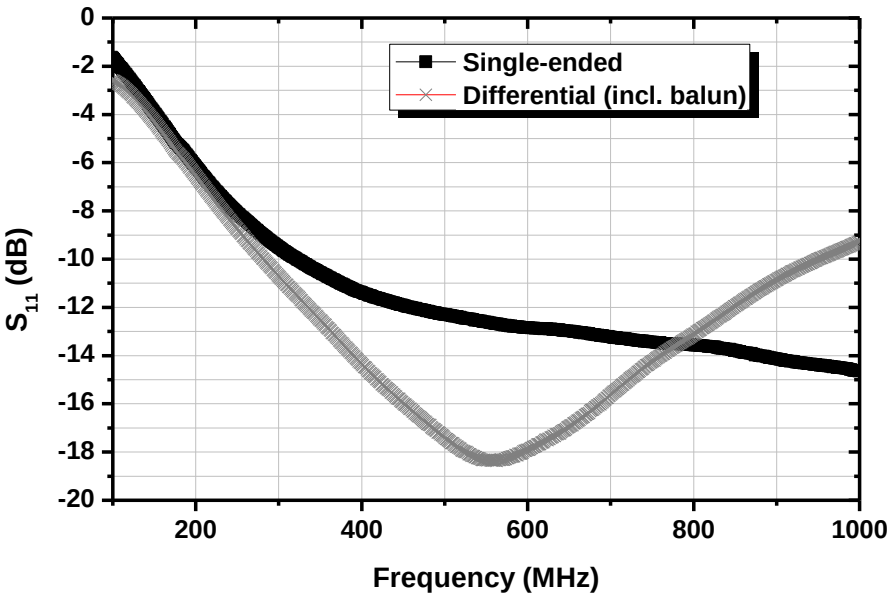


Fig. 6.18 Measured input return loss in both two receiving modes.

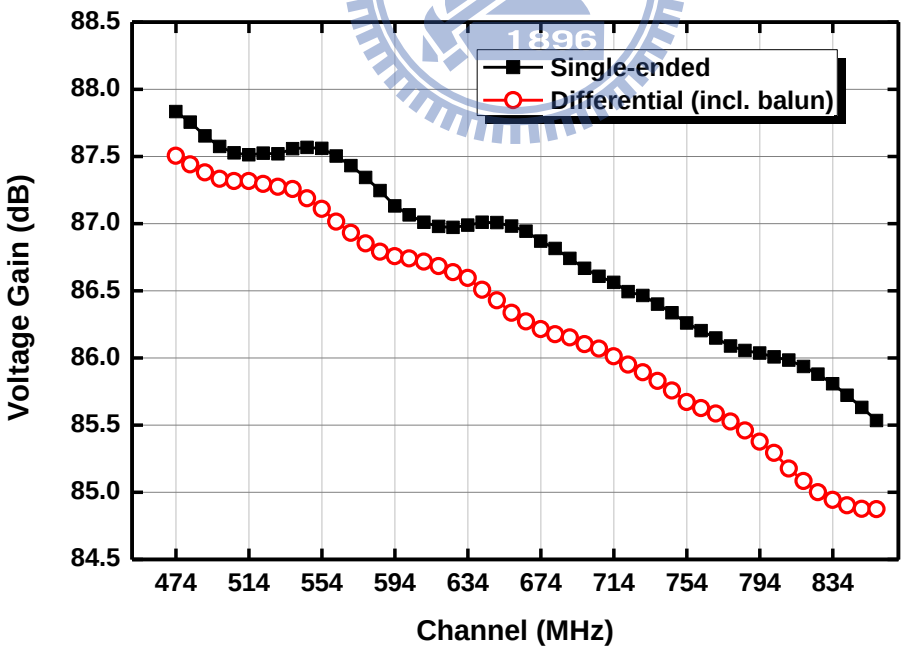


Fig. 6.19 Measured gain flatness across the band (RFE=max, ABB=50dB).

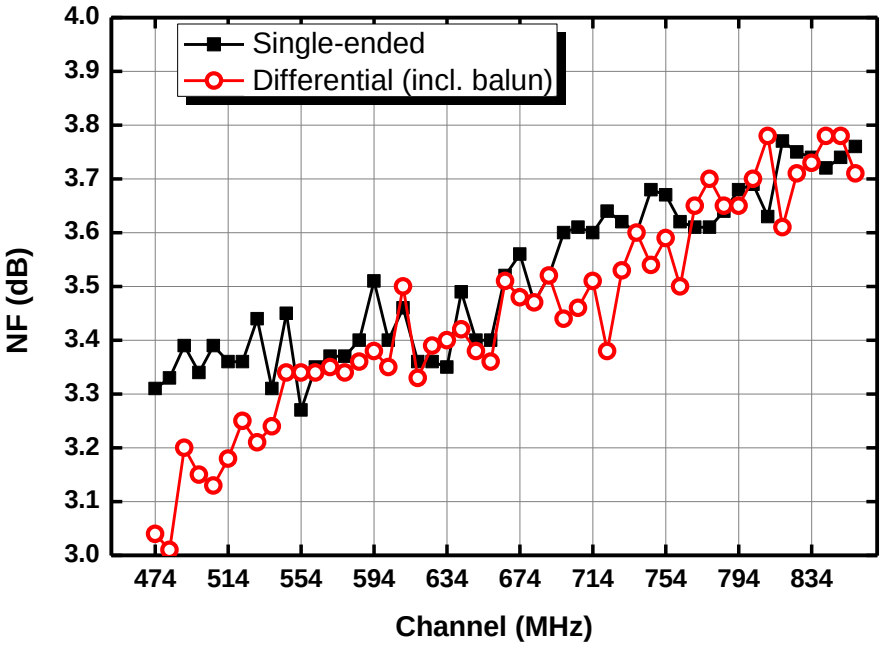


Fig. 6.20 Measured NF in the high-gain mode (RFE=max, ABB=50dB).

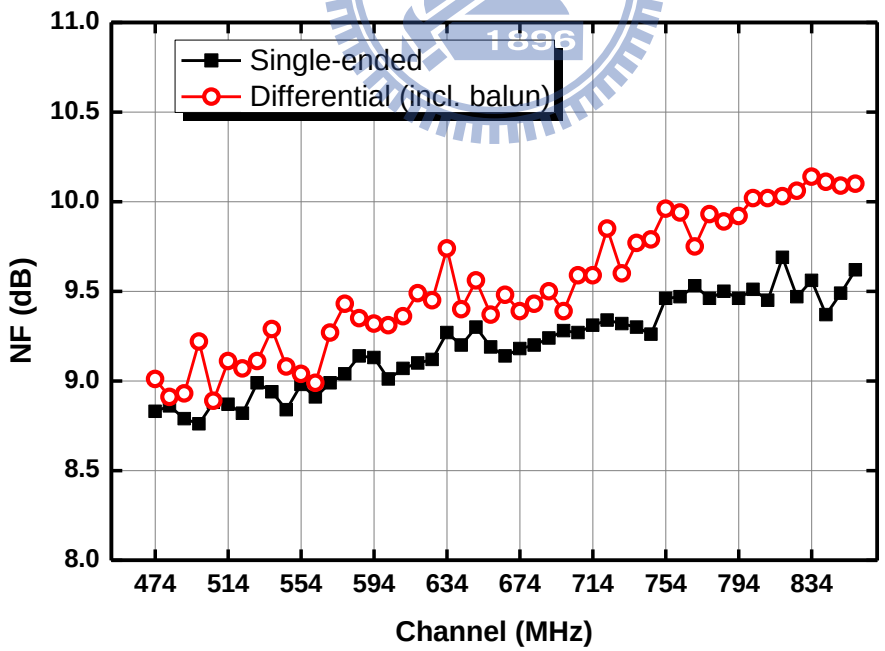


Fig. 6.21 Measured NF in the low-gain mode (RFE=max, ABB=50dB).

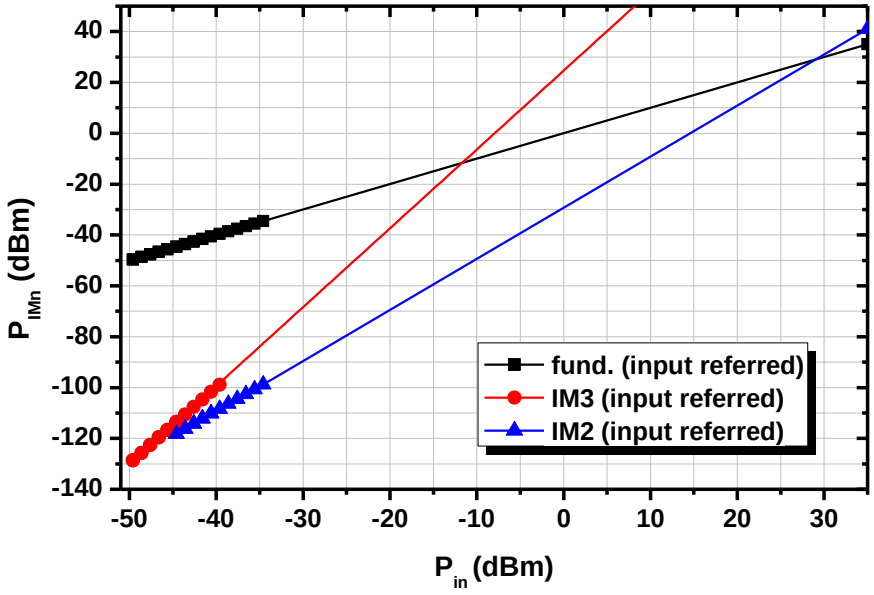


Fig. 6.22 Measured IIP3 and IIP2 in the high-gain mode (RFE=max, ABB=50dB).

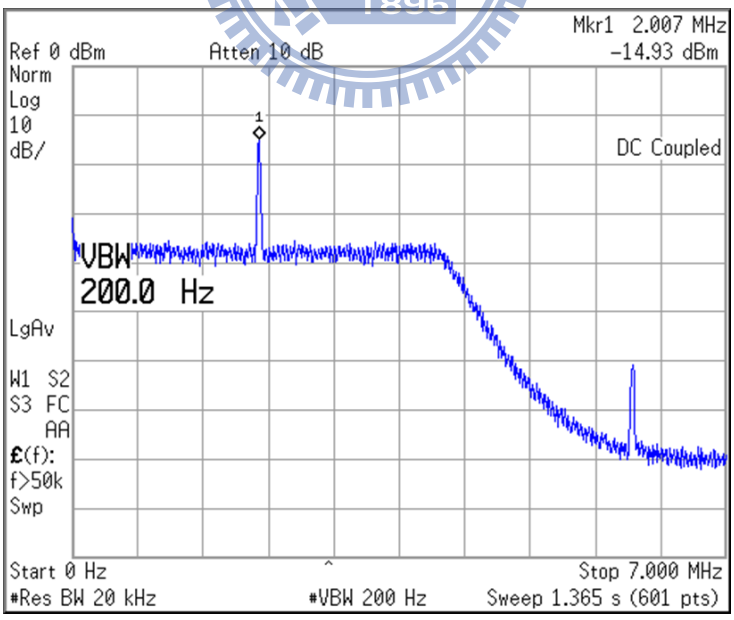


Fig. 6.23 Measured spectrum at the baseband output with the RF port terminated to a 50ohm terminator; clock leakage component at 2MHz is measured at the gain setting of 93dB.

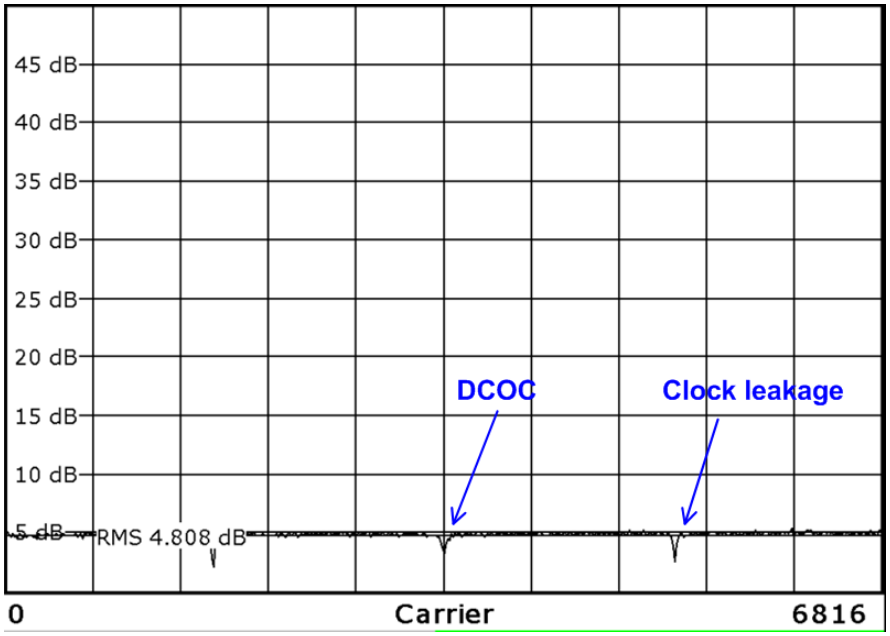


Fig. 6.24 Signal quality deterioration due to the clock leakage, measured with the RF port having an input of -96.6dBm QPSK signal.

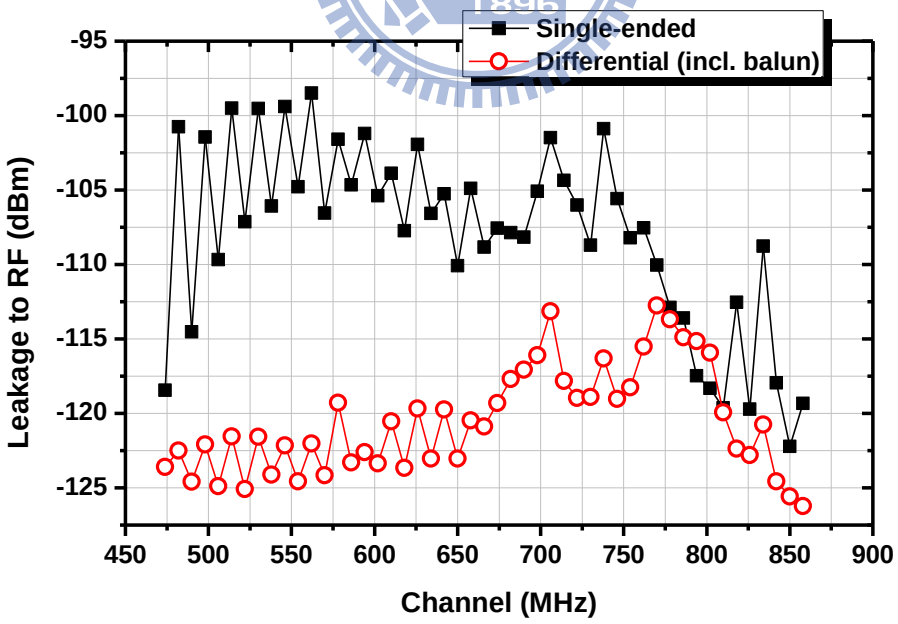


Fig. 6.25 Measured clock leakage level referred to the RF input across the band of interest.

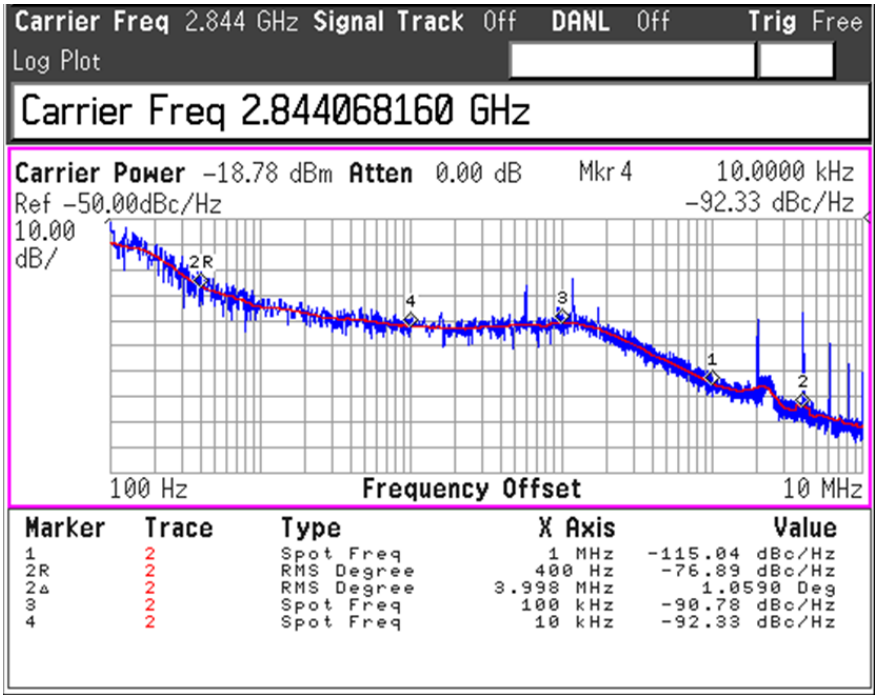


Fig. 6.26 Measured phase noise spectrum at the VCO output (2.844GHz).

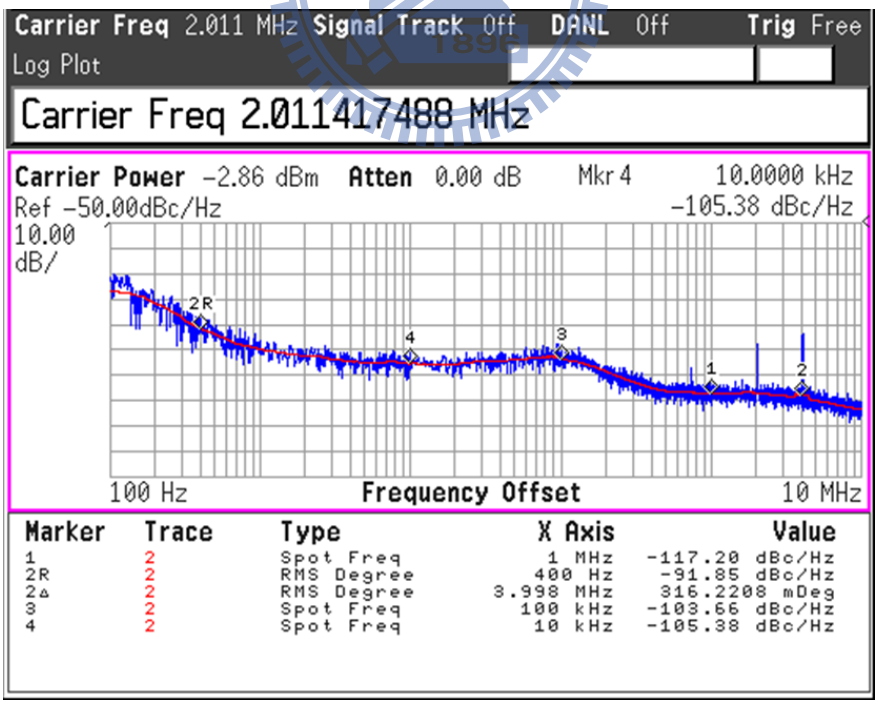


Fig. 6.27 Measured phase noise spectrum at the baseband output at the 474MHz channel (LO=2.844GHz/6).

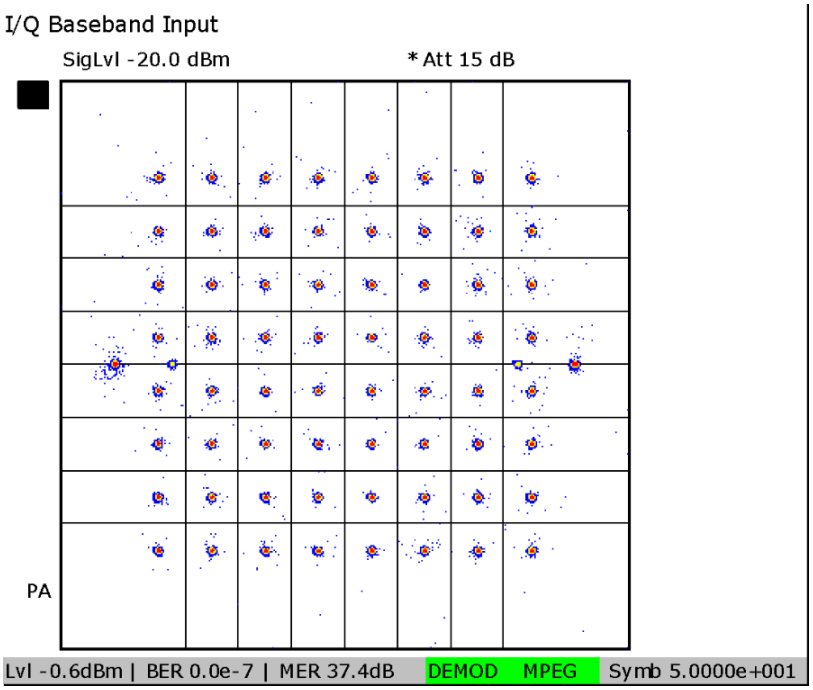


Fig. 6.28 Measured constellation diagram of DVB-H signal (64-QAM 3/4).

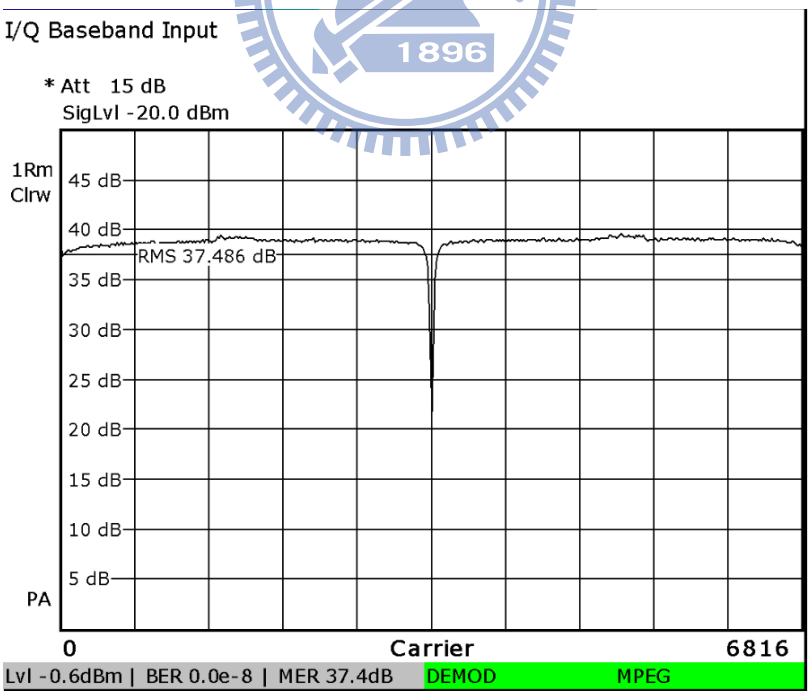


Fig. 6.29 Measured MER (EVM) per subcarrier for DVB-H signal (8k mode).

Fail	Limit	<	Results	<	Limit	Unit
Level	-60.0		-0.6		10.0	dBm
Constellation			64 QAM NH / normal			
MER (rms)	24.0		37.4		-----	dB
MER (peak)	10.0	*	3.7		-----	dB
EVM (rms)	-----		0.88		4.40	%
EVM (peak)	-----	*	52.23		22.00	%
BER before Viterbi			1.4e-4(10/10)		1.0e-2	
BER before RS			0.0e-8(37/100)		2.0e-4	
Packet Error Ratio			0.0e-5(23/100)		1.0e-8	
Packet Errors			0		1	/s
Carrier Freq Offset	-30000.0		-4567.1		30000.0	Hz
Bit Rate Offset	-100.0		-0.4		100.0	ppm
MPEG Ts Bitrate			24.882342			MBit/s

PA

64 QAM NH (64NH)	FFT 8k (8k)	GI 1/8 (1/8)	3/4,3/4 (3/4,3/4)	Cell ID 0
TPS Res. 0,0,0,0	INT N (N)	MPE FEC Off/Off	Time Sl. Off/Off	LI 21

Lvl -0.6dBm | BER 0.0e-8 | MER 37.4dB DEMOD MPEG

Fig. 6.30 Measured performance overview for DVB-H signal (8k mode).

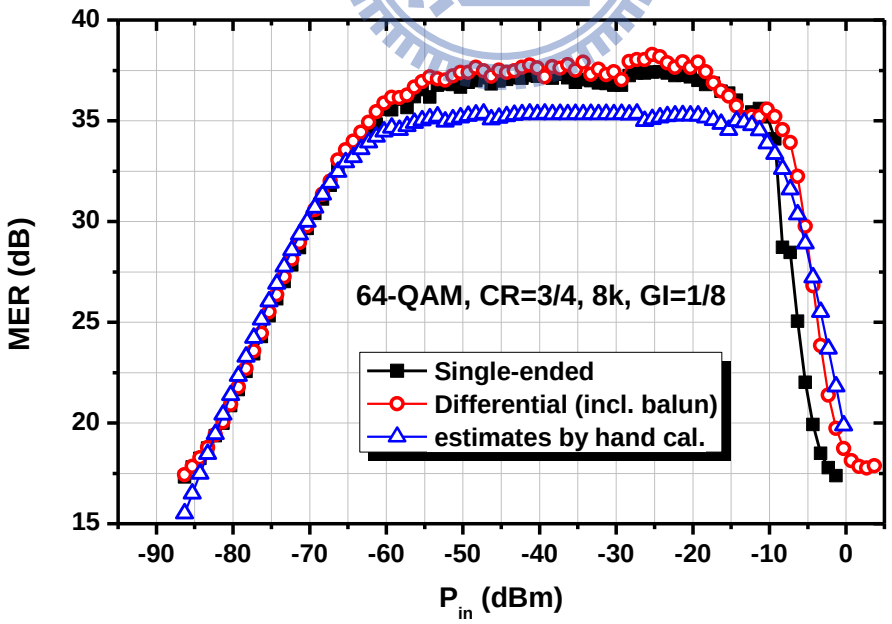


Fig. 6.31 Measured MER versus the input power level (64-QAM 3/4).

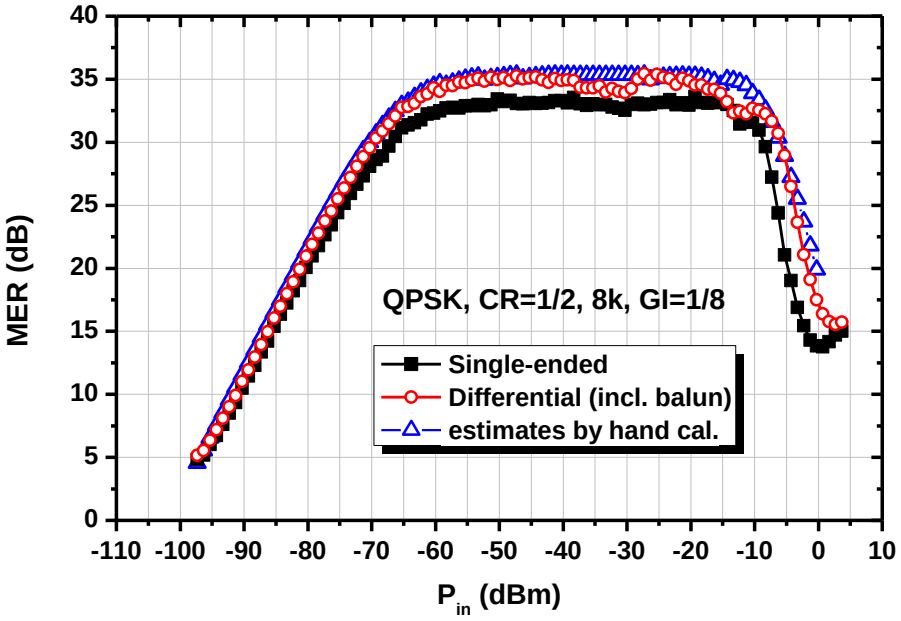


Fig. 6.32 Measured MER versus the input power level (QPSK 1/2).

TABLE 6.3
PERFORMANCE SUMMARY OF RF TUNER

Mode/Band / Parameter	Single-ended		Differential	
	UHF	L-band	UHF	L-band
Input Return Loss (dB)	< -12	< -12	< -11	< -11
Gain Max/Min (dB)	107 / -8	105 / 8	106.5 / -8.5	105 / 8
Gain Step (dB)	0.5	0.5	0.5	0.5
RF range/BB range (dB)	37 / 78	19 / 78	37 / 78	19 / 78
NF @[(a)]Max Gain (dB)	3.3—3.8	4.2	3.0—3.8	3.9
NF @ [(b)]Low Gain (dB)	8.7—9.7	11	8.8—10.2	12.2
IIP2 (N+2) @ [(a)]Max Gain/ [(b)]Low Gain (dBm)	29 / 50	34 / 55	35 / 54	40 / 58
IIP3 (N+2,N+4) @ [(a)]Max Gain / [(b)]Low Gain (dBm)	-11 / 6	-10 / 15	-9.5 / 8	-8 / 16
Phase noise @ 10k/100k/1M (dBc/Hz)	105/104/127	99/98/121	105/104/127	99/98/121
Integrated phase noise (400-4MHz)	< 0.4	< 1	< 0.4	< 1
Filter rejection [(c)] @ 5.25/13.25MHz	32 / 46	32 / 46	32 / 46	32 / 46
DC offset	< 6	< 6	< 6	< 6
I/Q matching	< -37	< -37	< -37	< -37
Leakage to RF (dBm)	<-98	< -115	-112	< -118
Supply Voltage (V)	1.2	1.2	1.2	1.2
Current Consumption (mA)	88	90	90	90
Die size (mm^2)	7.8	7.8	7.8	7.8

[(a)] Low Gain = Max RF -16dB, [(b)] Low Gain = Max RF -16dB, [(c)] at 4MHz BW setting.

TABLE 6.4
SELECTIVITY/LINEARITY AND SENSITIVITY MEASUREMENT RESULTS

Mode				**Single-ended**	**Differential**
Pattern	**Modulation**	**Interferer location**	**U/D (dB) Spec.**	**U/D (dB) Measured**	**U/D (dB) Measured**
S1 (PAL-G)	8k 64-QAM 3/4	N+1	35	38.4	38.8
		N-1	35	38.2	39
		N+2	43	45.6	46.2
		N-2	43	45.6	46.2
S2 (PAL-G)	8k 64-QAM 3/4	N+1	27	34.7	35.4
		N-1	27	34.7	35.4
		N+2	40	43.8	44
		N-2	40	43.8	44.4
L1	8k 16-QAM 2/3	N+2, N+4	40/45	41.8/46.8	41.4/46.4
L2	8k 16-QAM 2/3	N+2, N+4	45	46.9	46.4
L3	8k 16-QAM 2/3	N+2, N+4	40	44.8	43
	Modulation	**C/N (dB)**	**Spec. (dBm)**	**Measured (dBm)**	**Measured (dBm)**
Sensitivity	8k 64-QAM 3/4	19.9	-81.3	-81.4	-81.5
	8k 16-QAM 2/3	12.7	-88.5	-88.8	-89
	8k QPSK 1/2	4.6	-96.6	-97.3	-97.5

6.7 Conclusion

A 1.2V highly integrated RF tuner for DVB-T/H applications in 65nm CMOS technology is demonstrated. Based on the same architecture in the 0.13μm implementation, the tuner further integrates a wideband LNA compatible for differential and single-ended inputs to meet the requirements either on RF-alone or system-on-a-chip (SoC) developments. The impacts of technology scaling on RF/mixed-signal design have been explored by the study of the proposed LNA design. In addition, the critical issues of the board-level design are discussed. The tuner consumes only 88mA from a single 1.2V supply in the continuous mode and occupies a silicon area of 7.8 mm^2. The measurement results show that this tuner complies with the MBRAI 2.0 requirement.

6.8 Appendix I – 65nm Tuner (II)

Since *MBRAI 2.0* releases a stringent sensitivity specification, NF less than 4dB in RF tuners is required to meet the specification. Further to improve the overall NF, an auxiliary LNA with a lower NF is added in parallel with an established LNA. The auxiliary LNA has an imbalanced size ratio between the CG and CS branches as described in Section 4.8. Fig. 6.33 shows the simplified schematic of the UHF front-end. As can be seen, the auxiliary path contains an asymmetric CG-CS balun LNA along with a duplicated input transconductor of the mixer. The input port of each LNA is connected to one common ESD pad and the differential outputs of two transconductors are summed together in a current mode. The summation in a current mode can alleviate the impacts of the layout routing and the RC parasitic on circuit performance. The tuner chip is fabricated in 65nm 1P6M LP CMOS process. It occupies a total silicon area of 7.8 mm^2 including all ESD pads. Fig. 6.34 shows the die micrograph of the chip. The measurement result shows that this tuner achieves a NF of 3－3.5dB across 474－858MHz channels. It means that an improvement of 0.3dB, i.e., -97.6dBm sensitivity, can be achieved due to this auxiliary LNA. In addition, the performance of this tuner is similar to that of the single-ended mode in Table 6.3 and Table 6.4.

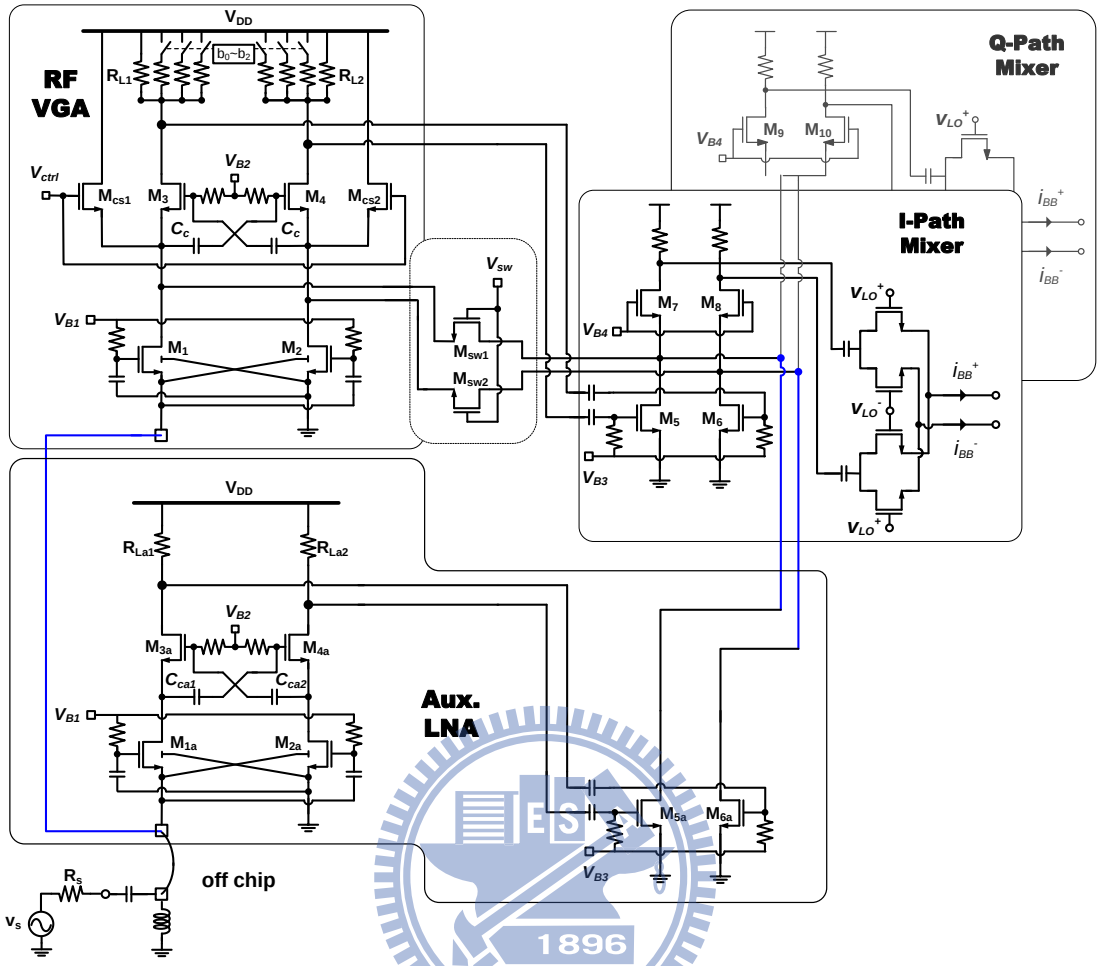


Fig. 6.33 Simplified schematic of the UHF front-end with an auxiliary LNA.

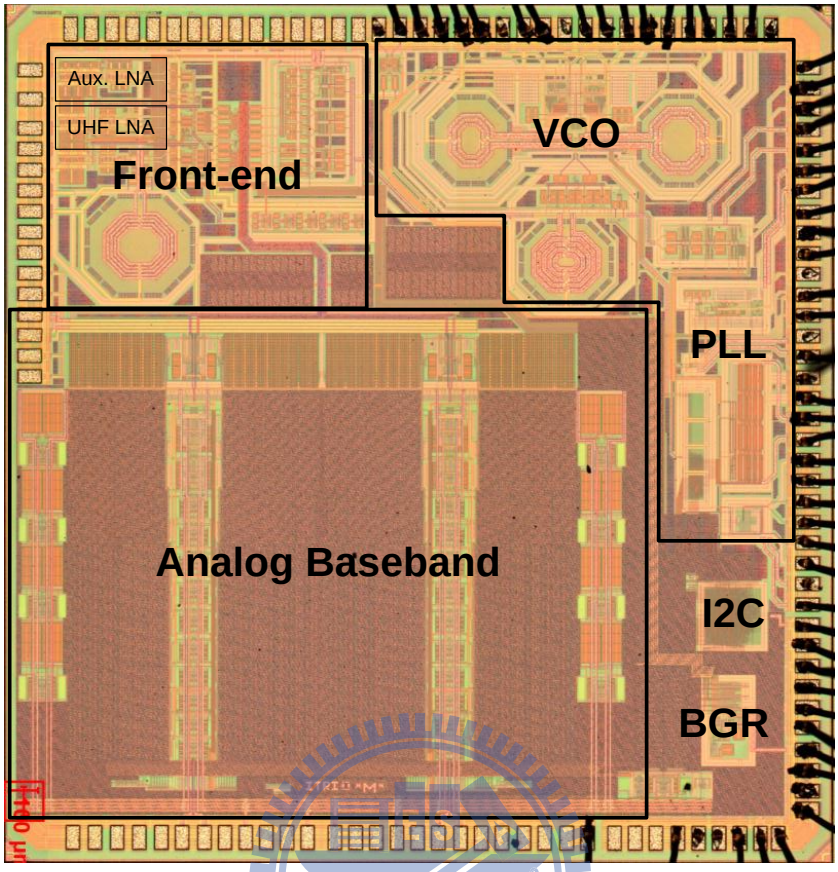


Fig. 6.34 The die micrograph of the high sensitivity tuner chip.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Chapter 7

Conclusion and Future Works

7.1 Conclusion

This dissertation concentrates on the design and implementation of CMOS RF tuners for mobile TV applications. In this dissertation, considerations on system-level and circuit-level design have been presented, mainly focused on the DVB-T/H standard, *MBRAI 2.0*.

The design aspects of DVB-T/H system have been described in chapter 2 and chapter 3. The design procedure starting from standard specifications, receiver specifications to building block requirements is presented. What we have illustrated is expected to bridge the gap between the circuit design and radio standards in realization of wireless communication system.

A CMR current buffer is proposed and analyzed in chapter 4. By incorporating an extra capacitor pair into the CG current buffer, the CMRR characteristic at RF frequencies can be enhanced by 10dB. In cascode of the CMR buffer, the CG-CS amplifier has a significantly reduced NF and improved linearity. With symmetric branch sizes, the LNA can be configured as a differential or single-ended receiving mode, both featuring a NF of 2.3dB. With asymmetric branch sizes, the LNA is approved to have a NF as low as 1.7dB.

To develop low-voltage, low-power, and high-integration tuners, direct-conversion architecture is adopted and a novel frequency plan is proposed. In use of divide-by-2/4/6 dividers, the frequency plan effectively reduces the required VCO

tuning range to 40%. Divide-by-N circuits with even number of N ensures high quadrature accuracy. Furthermore, operating at higher frequencies enables the use of on-chip inductors with smaller area and higher Q-factors.

Based on the proposed architecture and frequency plan, three fully integrated CMOS tuners compliant with DVB-T/H system are presented. Techniques in current-mode operation are widely used in the design, such as the high SNIR gain-switching method and the RSSI detection. The first tuner is implemented in 0.13μm CMOS technology. With the proposed balun LNA, the tuner achieves a sensitivity level of -96.6dBm and dissipates 114mW from a 1.2 V supply. The second tuner is implemented in 65nm CMOS technology. Incorporating the reconfigurable LNA, the tuner highly adapts to various market requirements, either RF stand-alone or SoC solutions. This tuner achieves a sensitivity level of -97.3dBm and dissipates 88mA from a 1.2 V supply. The third tuner is also implemented in 65nm CMOS technology. It is implemented to demonstrate even better sensitivity performance with an asymmetric balun LNA. The tuner achieves a sensitivity level of -97.6dBm and dissipates 88mW from a 1.2 V supply.

7.2 Future Works

In this dissertation, a wideband LNA is adopted and demonstrated in a tuner compliant with the DVB-T/H standard. Compared to narrow-band LNAs used in previous work [16], [17], [18], [31], [64], wideband LNAs achieve better performance and reliability. However, wideband receptions possibly suffer from the problem of GSM interference much more. To provide a more competitive solution, a GSM-rejecting notch function could be incorporated into the proposed LNA topology.

As can be found in the chip micrographs, the analog baseband occupies a significant part of the total die area. To minimize the area and power consumption of the RF tuner, more system budgeting can be left for the digital part in 65nm CMOS. Significant reduction in area/power can be achieved by removing most of the analog baseband function, while replaced with high performance ADC and digital filters [77] [78], [79], [80]. To meet the market requirements, more integration of system blocks

and functionality is a trend. To achieve multi-standard operation and to cover most popular mobile TV bands, the VHF III band (174–240 MHz) should be added. This new chain can be realized by duplicating the UHF-band RF front-end, but still need to extend the channel bandwidths from 0.3 to 8MHz in the baseband filters [31], [64].

With the transition from analog to digital TV, much more TV spectrum is released. More and more wireless standards target at TV-band operations, such as 802.11af, 4G LTE/WiMAX [81], 802.22 cognitive radio [82], etc. The proposed techniques could be generalized to the implementation of these new standards.

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Vita

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Publication List

Journal Papers：

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