# 國 立 交 通 大 學

## 電子工程學系電子研究所

## 博 士 論 文

具線性度補償之

互補金氧半層疊E類功率放大器設計

CMOS Cascode Class E Power Amplifier Design with Linearity Compensation

研 究 生 ： 鄒 文 安

指導教授 ： 溫 瓌 岸

中華民國 九十九 年 五 月

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博 士 論 文

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# 具線性度補償之互補金氧半層疊 E 類功率放大器設計

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## 摘　　要

本論文針對可應用於極座標調變傳送機之互補式金氧半層疊 E 類功率放大器提出 AM-AM 和 AM-PM 失真補償之設計。本文探討之 E 類功率放大器為使用小電感值 dc-feed 之層疊式架構，主要考量為互補式金氧半製程中，大電感值電感不易取得以及主動元件的低崩潰電壓特性。而當層疊 E 類功率放大器應用於極座標調變（亦即調變放大器之供給電壓）時，在放大器的輸出訊號上會產生 AM-AM 和 AM-PM 失真特性。

本文除探討 AM-AM 和 AM-PM 失真產生之原因，並且提出一失真補償技術 — 藉由改變層疊電晶體之閘極偏壓，使電晶體操作如一電阻性元件，進而改進放大器之非線性效應。由設計的 2.6 GHz 層疊 E 類功率放大器實驗結果顯示，經由外部改變偏壓的方式，在供給電壓大於 0.6 伏特時，補償後之輸出訊號相位偏移可從 30 度降低到 6 度，輸出訊號振幅相對供給電壓可成線性變化。而另一 2.6 GHz 層疊 E 類功率放大器整合自我偏壓控制電路設計之實驗結果顯示，輸出訊號振幅與供給電壓成 1V/V 之線性關係外，並有 5 度輸出訊號相位的偏移；在 1.8 伏特供給電壓和輸入功率為 6 dBm 下，輸出功率為 12 dBm，汲極效率為 17.8%，PAE 為 16.6%。實驗結果顯示，所提出的補償技術可有效的改進功率放大器之 AM-AM 和 AM-PM 失真。

並且利用射頻/基頻共同驗證方法，輸入為一 OFDM 訊號時，放大器經過補償後，模擬結果顯示，在 16QAM 的調變下，EVM 可從-17dB 到-19.2dB；在 64QAM 的調變下，EVM 可從-21dB 到-25.1dB。最後針對矽基底電感的低品質因素造成放大器效率的降低，因此整合多層金屬層之懸空式電感於放大器匹配電路中，模擬結果顯示可使放大器有最大 17%的效率提昇。

# CMOS Cascode Class E Power Amplifier Design with Linearity Compensation

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## ABSTRACT

The dissertation presents the design of the cascode Class E power amplifier with AM-AM and AM-PM compensation for polar applications. For integration and reliability analysis in CMOS process, the Class E designed with small dc-feed and using cascode topology has been presented. When the Class E is in supply modulation, the AM-AM and AM-PM distortion is introduced at the RF output signal.

This work not only analyzes the cause of the distortion but also presents a compensation technique. When modulating the gate bias voltage of the cascode transistor, the transistor operates as a resistance alike to improve the distortion of the amplifier. The experimental result of proposed 2.6 GHz cascode Class E power amplifier shows that when the PA is compensated the AM-PM is reduced from 30° to 6° and the output envelope voltage is linearly to supply voltage in $V_{DD}$ > 0.6 V. The experimental result of the 2.6 GHz cascode Class E power amplifier with self-biased control circuit shows that the voltage slope of AM-AM is 1 V/V and the phase error of AM-PM is 5°. The PA has a output power of 12 dBm, drain efficiency of 17.8% and PAE of 16.6% from a 1.8 V supply and an input driving of 6 dBm. Therefore, the experimental results demonstrate the proposed compensation technique can effectively improve the AM-AM and AM-PM distortion of the cascode Class E amplifiers.

In addition, the simulation results of the RF/baseband co-verification platform with OFDM-based signal source show that the EVM is improved from -17 dB to -19.2 dB at 16QAM modulation and from -21 dB to -25.1 dB at 64QAM modulation. Finally, due to the low quality factor of silicon-based inductor causing the degradation on PA efficiency, the PA with multi-metal layer suspended inductors has been presented. The simulation result shows that the PA can have a maximum efficiency improvement of 17%.

# 誌　　謝

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鄒文安

99 年 5 月

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# Chapter 1

# Introduction

To increase the capacity of wireless data transmission, recent wireless system, wireless LAN (WLAN), allows amplitude or envelope variations of the phase modulated RF carriers. In order to efficiently use the limited available frequency spectrum, these systems employ spectrally efficient spectrum, such as orthogonal frequency division multiplexing (OFDM). IEEE 802.11a/g systems, for example, are capable of transmitting data at the rate of 54 Mb/s while occupying a channel bandwidth of only 20 MHz. This bandwidth efficiency in the frequency domain comes at the expense of the increased peak-to-average-power ratio (PAPR) in the time domain. For example, 802.11a OFDM signals theoretically have a PAPR of 17 dB.

In contrast to constant envelope systems like GSM and Bluetooth, the signal with envelope variations requires a linear power amplifier (PA) in transmissions. A linear power amplifier, such as a Class A or AB amplifier, has the drawbacks of lower efficiency and hence reduced battery lifetime. Since the efficiency of PAs is and has always been a major topic in transmitter systems, decreasing the dissipated power and increasing battery lifetime are the driving forces in the development of efficient systems.

Therefore, the efficient transmitters of envelope elimination and restoration (EER), polar and envelope-tracking (ET) are more attractive in wireless communication systems in the latest years [1]-[37], as shown in Figure 1.1. The EER transmitter is first proposed as it can utilize efficient switching power amplifiers, while also providing high linearity [38]. Recently, the EER system and its modern derivative polar and ET systems have been extensively discussed in wireless communication applications [39]-[44].

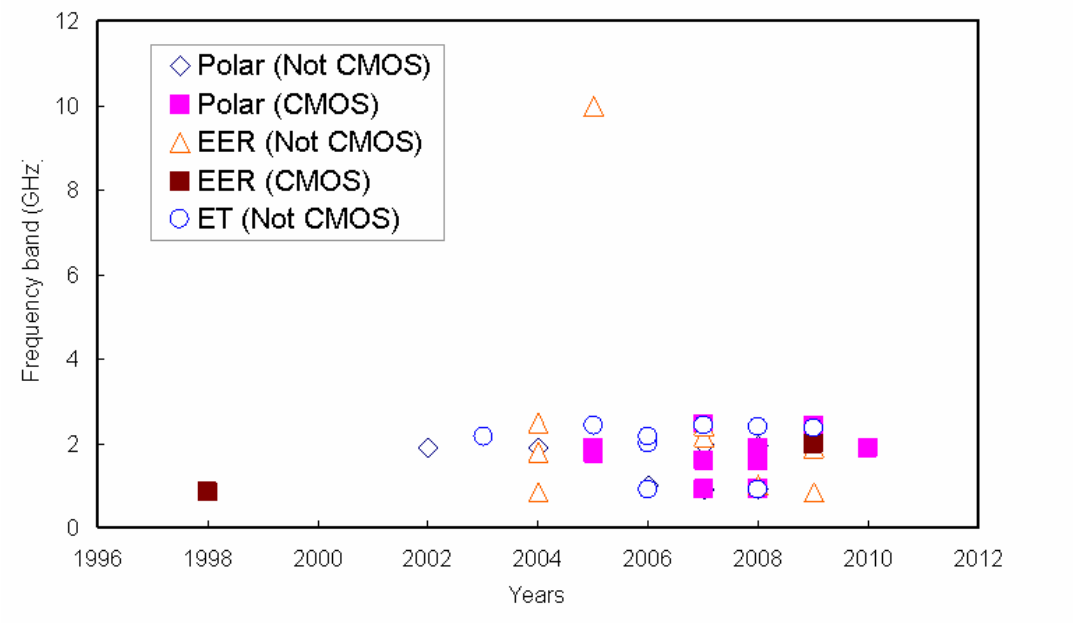



Figure 1.1 Cutting edge architecture of transmitters.

# 1.1 Motivation

For the efficient transmitters as shown in Figures 1.2, Figures 1.3 and Figures 1.4, to recombine the envelope and phase signal is to use a switching mode Class E power amplifier, which is a potential candidate for power amplification in wireless transceivers. The linearity requirements in Class E PAs have been concerned [45]-[50]. As shown in Figures 1.5, several techniques such as digitally modulated technique [10]-[14], using thick-oxide transistors [16]-[17], feedback topology [15] [29] and predistortion technique [28], have been proposed to solve the PA linearity problems in efficient transmitter applications. Moreover, the cascode-based topology of Class E PAs is considered for reliability analysis.

The research goal of this work is to explore the techniques for implementing a cascode Class E power amplifier for polar systems in low-cost complimentary metal-oxide semiconductor (CMOS) technology while provide sufficient performance. For reliability issues in a CMOS technology process, the cascode topology is a viable way to relax the device stress in Class E power amplifiers [42], [50]-[51]. Since the AM-AM and AM-PM

distortion is the important specification for PAs in polar transmitter applications, the design issues of compensating the distortion is one of the interests of the work. Moreover, CMOS multi-metal layer suspended inductors are presented to improve the efficiency of the PA.

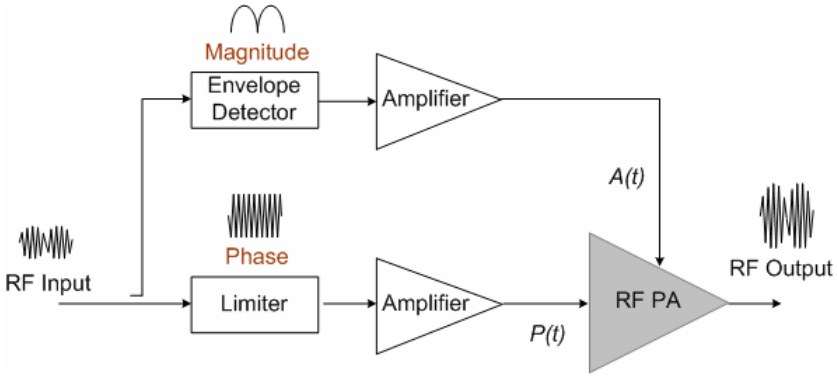



Figure 1.2 Envelope elimination and restoration (EER).

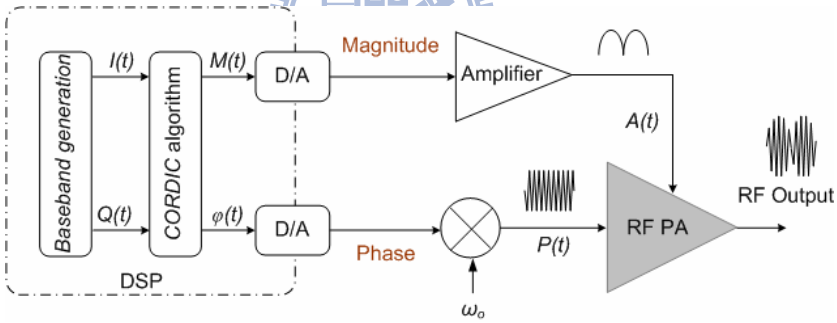



Figure 1.3 Polar transmitters.

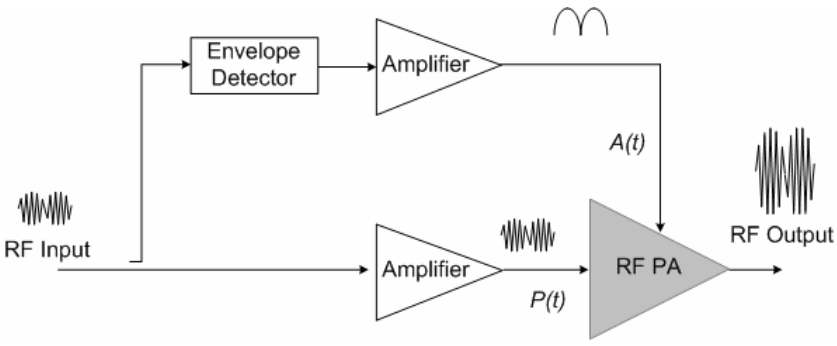



Figure 1.4 Envelope-tracking transmitters.

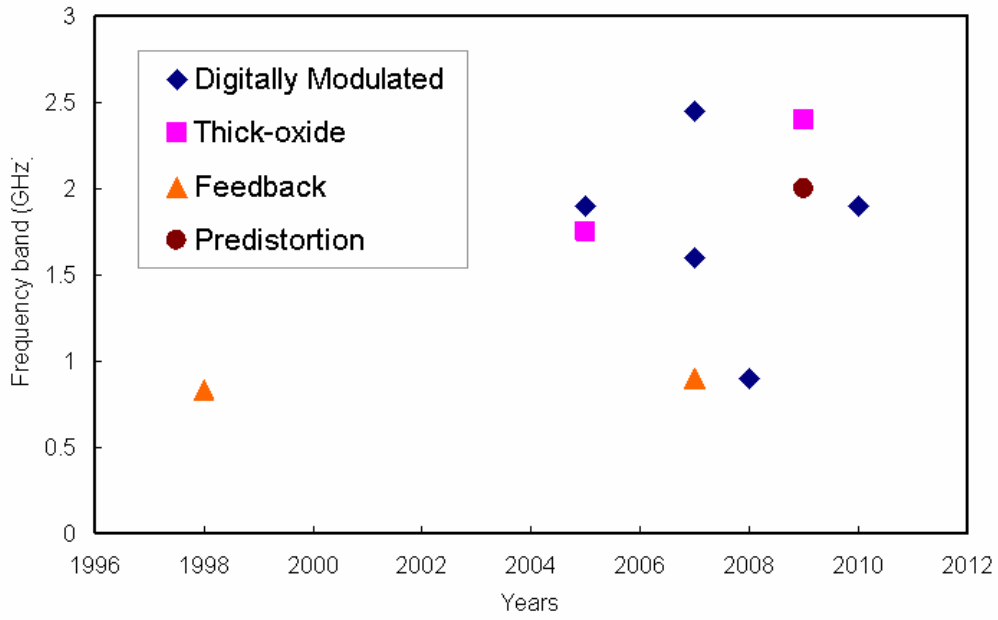



Figure 1.5 Technologies for linearity improvement.

## 1.2 Organization

The organization of the dissertation is overviewed as follows:

Chapter 2 begins with a review of conventional common source Class E power amplifiers. The characteristic of power control and practical considerations are included. The small dc-feed inductor for integration as well as the cascode topology of the Class E for reliability analysis is also discussed in the chapter.

Based on the design methodology of the Class E in Chapter 2, a conventional cascode Class E power amplifier using a CMOS 0.18 μm technology has been presented in Chapter 3. Moreover, the characteristics for supply modulation applications have been discussed. The detailed analysis for the AM-AM and AM-PM distortion is described in the chapter.

The AM-AM and AM-PM distortion of the cascode Class E amplifiers mainly comes from the nonlinear operation of the cascode transistor against the changed supply voltage.

Chapter 4 presents the technique to compensate the distortion. When modulating the gate bias voltage of the cascode transistor, the transistor is operated as a resistance alike and the distortion is improved. Moreover, the efficiency performance of the amplifier is discussed in the chapter.

One design of cascode Class E power amplifier implemented in a CMOS 0.18 μm technology process has been presented in Chapter 5. With controlling the external biasing voltage, the experimental results demonstrate the ability of proposed technique on compensating the AM-AM and AM-PM distortion. Furthermore, the design of cascode Class E power amplifier with auto-biasing control circuit has also been implemented in a CMOS 0.18 μm technology process. Its experimental results show the cascode Class E amplifier with compensated AM-AM and AM-PM characteristics.

Chapter 6 presents the RF/baseband co-verification platform with OFDM-based signal source for EER system. The co-simulation results demonstrate the improved system EVM due to the PA using proposed compensation technique.

The PA efficiency is severely degraded due to the internal inductors with low quality factor. To alleviate the problem, a developed CMOS MEMS process and stacked metal layer suspended inductors have been presented in Chapter 7. The simulation results shows that the efficiency of the PA with proposed technique and suspended inductors can effectively increased. For the completeness of the dissertation, the cascode transistor replaced by a resistance in the cascode Class E has been presented and its results compared with that of the compensated cascode Class E are included in Appendix B.

Chapter 8 concludes the summary of contributions and some suggestions for future work.

# Chapter 2

# Design Considerations of Class E Power Amplifiers

Progress in the last years has shown that CMOS, traditionally confined to the digital and baseband part of radio transceivers, is also a competitive technology for radio frequency (RF) front-end. The demand for compact, low-cost and low-power portable wireless devices has prompted the quest for single-chip radio transceivers realized in a standard CMOS technology. One of the most difficult remaining challenges is the integration of the power amplifier that meets the required output power with high efficiency. Recently, there have been considerable interest and research effort in the design, analysis and implementation of CMOS Class E tuned PAs [52]. This is due to its high efficiency, simplicity and high tolerance to circuit variations, comparing to other types of PA. As a result, the Class E is the most attractive power amplifier for power efficient transmitter designs. Therefore, understanding the operation of the Class E power amplifier is necessary. The circuit principle of the Class E is introduced in Section 2.1. After that, the cascode topology of Class E is also discussed in Section 2.2, where this topology is commonly used to reduce the high drain voltage swing on each transistor.

## 2.1 Common-Source Class E Power Amplifier

It is desirable to obtain high RF power amplifier efficiency in many practical applications. At least one, if not all, of the following requirements is important: low power consumption, low temperature rise of the components, high reliability, small size, and light weight. The Class E

power amplifiers can achieve very high efficiency by minimizing the dissipated power in the transistor.

### 2.1.1 Design Principles

The key idea behind any high efficiency power amplifier is to reduce the overlap of current conducting through the transistor and voltage across the transistor. This will result in less dissipation in the transistor and hence increases the efficiency of the amplifier. A second idea is to use the transistor not as a current source, but as a switch. A further efficiency enhancement is obtained by minimizing the voltage across the switch when it is closed, the so-called zero-voltage switching criteria (ZVS). Thus the product of the transistor voltage and current will be low at all time during the period. Figure 2.1 shows the ideal waveforms of the transistor voltage and current that meet the high-efficiency requirements [53]. The low voltage-current product can be made because:

1. "ON" state: The voltage is zero when the current is drawing.
2. "OFF" state: The current is zero when the voltage level is high.
3. The rise of transistor voltage is delayed until after the current has reduced down to zero.
4. The transistor voltage returns to zero before the current begins to rise.
5. The slope of the transistor voltage waveform is zero at turn-on time.
6. The transistor voltage at turn-on time is zero.

The basic topology of the Class E amplifier is shown in Figure 2.2 [54] [55]. The circuit includes a transistor $M_1$, operated as a switch, a shunt capacitor $C_{shunt}$, an RF choke $L_{ck}$, a series-tuned output circuit $L_s$-$C_s$, a reactance jX and the load resistance $R_L$. $C_{shunt}$ is the parasitic capacitance in parallel at the switch (including intrinsic transistor output capacitance and circuit stray capacitance).

The simple equivalent circuit is based on the following assumptions [50], [53].

- The RF choke $L_{ck}$ is ideal: zero series dc resistance and infinite reactance at the operating frequency. The RF choke therefore allows only a constant (dc) input current.
- The series resonant circuit $L_s$-$C_s$ is tuned to the operating frequency.

- At the operating frequency a series reactance jX produces the difference in the reactance of the inductor and capacitor of the series-tuned circuit.
- The active device acts as an ideal switch: zero saturated voltage, zero turn-on resistance, and infinite OFF resistance; the switching action is instantaneous and lossless.
- The total capacitance, $C_{shunt}$ plus the intrinsic transistor output capacitance, is independent of the drain voltage.
- All components are ideal.

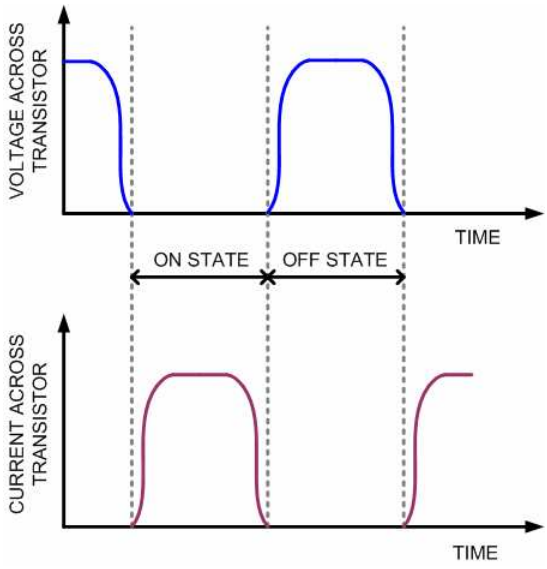



Figure 2.1 Ideal waveforms in high efficiency power amplifiers.

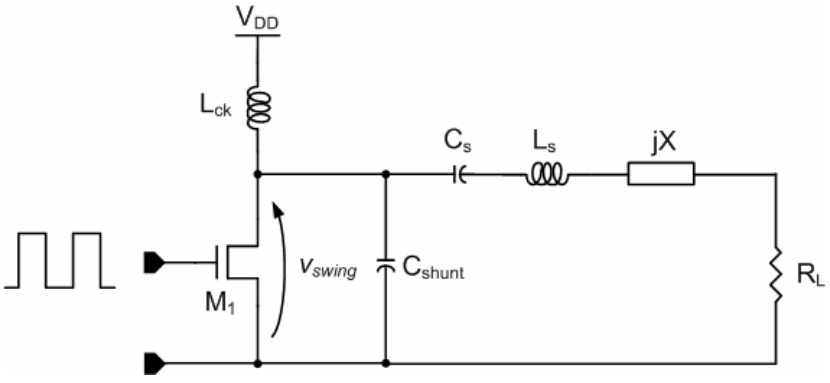



Figure 2.2 Schematic of common-source Class E power amplifier.

Therefore, the voltage-current separation and ZVS are obtained by the series-tuned LC network. The switch is closed at the instant where both the switch voltage and its first derivative are zero. The ZVS condition prevents dissipation of the energy stored by the shunt capacitor at turn-on time. The requirement of a zero first derivative makes the amplifier less sensitive to component, frequency and switching instants variations. This leads to the well-known Class E conditions as stated by Sokal [53]:

$$V_{swing}\ (t_1) = 0 \tag{2.1}$$

$$\left.\frac{\partial V_{swing}}{\partial t}\right|_{t = t_1} = 0 \tag{2.2}$$

where $t_1$ represents the instant at which the switch, and $V_{swing}(t_1)$ represents the switching voltage. A Class E amplifier then can generate waveforms that approximate the conceptual waveforms. The derived component values and the operation waveforms of the Class E amplifier will be discussed in the next section.

## 2.1.2 Design Equations

Based on the assumptions above, the equivalent circuit of the Class E amplifier can be obtained in Figure 2.3. A Class E amplifier consists of a switch S, an inductor $L_{ck}$ connecting the switch to the supply voltage $V_{DD}$, a capacitor $C_d$ in parallel with the switch, a tuned circuit $C_s$-$L_s$ in series with a reactive component $L_x$ and a load $R_L$.

The value of $R_L$ is chosen to deliver a desired amount of power with a specific supply voltage $V_{DD}$. This network acting as a filter also rejects the harmonics of the Class E waveform at the drain of the switch. In the original Class-E design of Sokal, the RF choke ($L_{ck}$) is made very large so it acts as a current source. $C_s$ and $L_s$ form a series resonator tuned at the desired frequency. Since the Class-E working conditions are given by two equations, two components of the circuit can be chosen in such a way that the amplifier fulfills the Class-E working conditions (Equations (2.1) and (2.2)). For the circuit of Figure 2.3, these two components are the capacitor $C_d$ and the inductor $L_x$. In this way, all components are

determined. The values of elements for Class E operation are given on Table 2.1, where $Q_{out}$ is the quality factor of the output network. The design parameter $Q_{out}$ involves a tradeoff between operation bandwidth and the harmonic content of the output signal. For design specifications of a Class E, $V_{DD}$=1.8 V, $\omega=2\pi\cdot 2$ Grad/sec, $P_{out}$=100 mW, $Q_{out}$=10000, its voltage and current waveforms are simulated by an ADS simulator. The switch with an on-resistance of 0.00001 Ω and an off-resistance of 1 MΩ are also assumed.

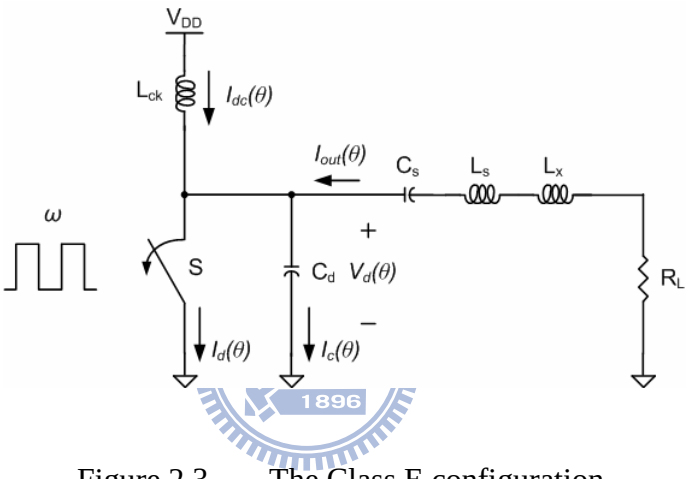



Figure 2.3 The Class E configuration.

Table 2.1 Class E design equations [52].

| | | |
|---|---|---|
| $P_{out}$ | Design output power | $\frac{\pi^2+4}{8} I_{DC}^2 R_L$ |
| $R_L$ | Load resistance | $\frac{8V_{DD}^2}{P_{out}(\pi^2+4)}$ |
| $L_X$ | Excess inductance | $\frac{\pi V_{DD}^2(\pi^2-4)}{2\omega P_{out}(\pi^2+4)}$ |
| $L_S$ | Resonator inductance | $\frac{8Q_{out}V_{DD}^2}{\omega P_{out}(\pi^2+4)}$ |
| $C_S$ | Resonator capacitance | $\frac{P_{out}(\pi^2+4)}{8\omega V_{DD}^2 Q_{out}}$ |
| $C_d$ | Shunt capacitance | $\frac{P_{out}}{\pi\omega V_{DD}^2}$ |

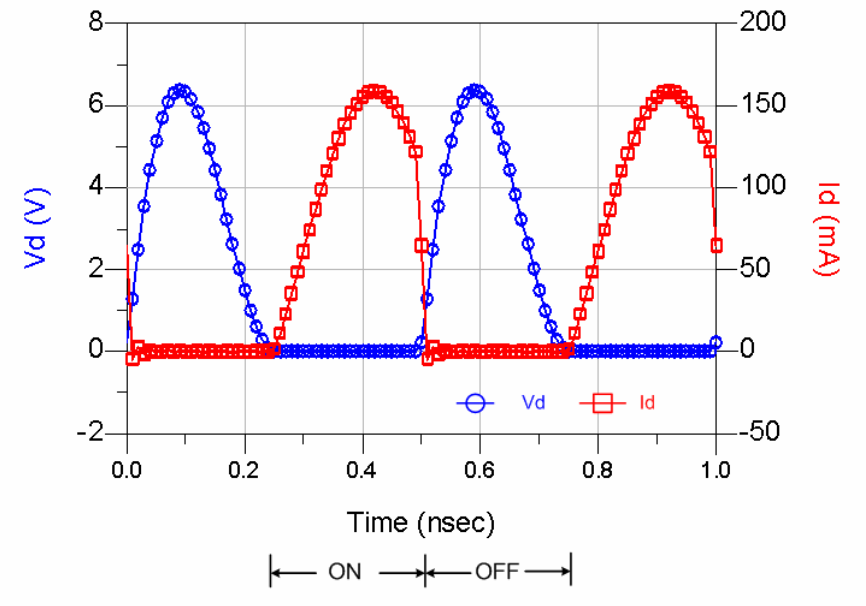



Figure 2.4 Switching voltage and switching current waveforms.

Figure 2.4 shows the switching voltage and the switching current waveforms of the Class E. The switching voltage and the switching current are not overlap, causing no power dissipation in the amplifier. When the switch is OFF, the voltage has a maximum value of 6.4 V, which is 3.56 times the supply value. When the switch is ON, the switch draws a large current $I_d$, as shown in Figure 2.5. When the switch is OFF, the switch draws a zero current, and then the capacitance $C_d$ begins to charge with a current $I_c$. This means that the amplifier switches correctly, changing alternately between ON and OFF. The output voltage and current with a sine wave, shown in Figure 2.6, are achieved when the switching voltage and current are through the series-tuned network. The harmonic content of the output signal are filtered out by this tuned network resonating at the carrier frequency. Finally, the efficiency ($Pout/V_{DD} \cdot I_{DC}$) of 99.78% is obtained, where the Class E has a theoretical efficiency of 100%. These results indicate that the analytic solution has an appropriate prediction on the operation of the Class E amplifier.

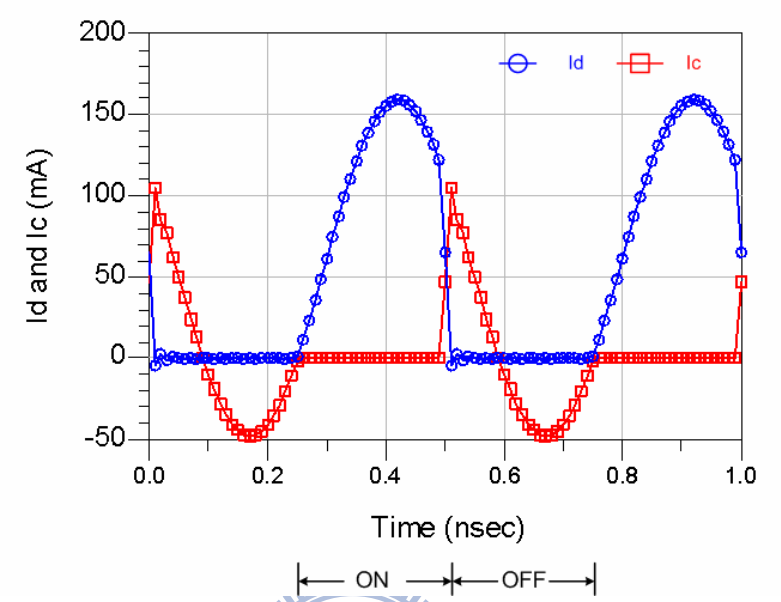



Figure 2.5 Current waveform of $I_d$ and $I_c$.

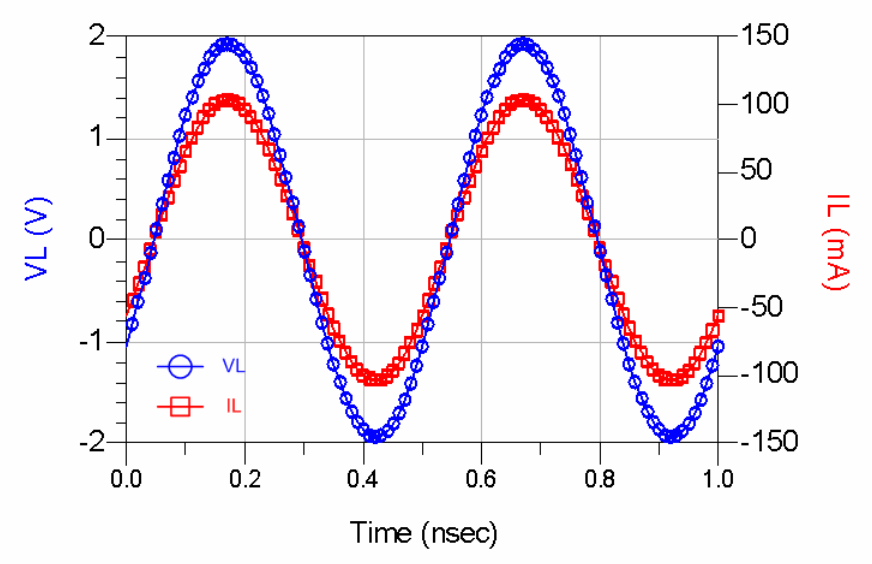



Figure 2.6 Output voltage and output current waveform.

### 2.1.3 Power Control

Since the input signal only provides timing information in a Class E power amplifier, the output power can not be controlled through the input signal like what is normally done in a linear or weakly nonlinear amplifier. Instead, the control of output power can be effectively realized through a variable supply voltage, for example, by a dc-dc converter. Since $V_{DD}$ is the only voltage reference in the switching circuit, the voltage at each node is proportional $V_{DD}$, and the power term of output power is proportional to $V_{DD}^2$. This means that the output power can be controlled through the supply voltage, which leads to the potential of maintaining a constant efficiency over a wide range of output power. This is illustrated in Figure 2.7, in which we assume, without loss of generality, that the loss is only from the finite on-resistance of the switch. Since both the loss and the output power scale with $V_{DD}^2$, their ratio, and the overall efficiency, are virtually unaffected as the output power is adjusted through the supply voltage.

$$P_{out}, P_{loss} \propto V_{DD}^2 \Rightarrow Efficiency = \frac{P_{out}}{P_{out} + P_{loss}} = const. \quad (2.3)$$

This characteristic is in sharp contrast to conventional power amplifiers with constant supply voltage in which the efficiency is typical optimized only at the maximum output power. Because the PA may spend most of its time operating at medium or low power levels in practical applications [56], a constant efficiency can potentially result in substantial power saving.

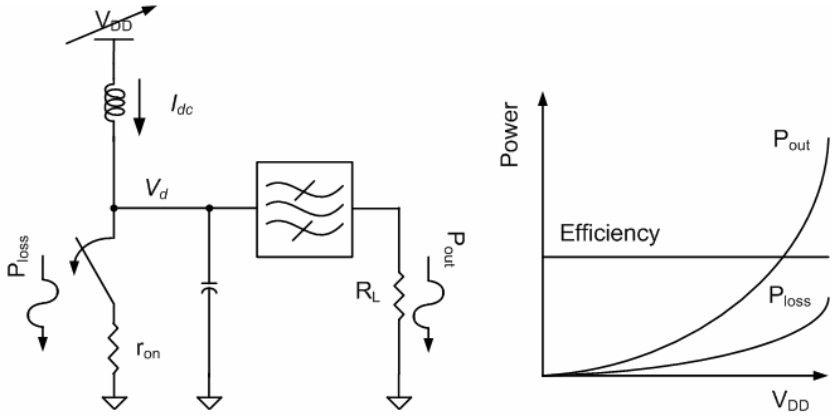



Figure 2.7 Constant efficiency over variable supply voltage.

### 2.1.4 Practical Considerations

The analysis presented in previous sections is based on several simple assumptions. In practice, however, some conditions are not acceptable in the implementation of chip design [57].

- Non-ideal passive components: The loss of passive components in CMOS technology can not be neglected because with low quality factor.
- A large RF choke is hard to implement in an on-chip design.
- Nonzero transition time: there exists inevitable transition time between ON and OFF. During the transition, the overlap of the switch voltage and the switch current causes the potential power dissipation in the typical switching amplifier.
- A square waveform as an input driving is not easy to implement.
- A nonzero on-resistance and a nonzero saturation voltage of the transistor [58].
- Finite Q of the load network: The output signal with a pure sine waveform can not be achieved, because the finite Q of the series-tuned output network.

### 2.1.5 Finite DC-Feed Inductor

The Class E required an RF choke between the dc supply voltage and the active device has been described in the previous section. However, the RF choke itself is large in size, and hence presents problems in terms of both large resistance loss and hard to implement in a single chip. Therefore, a small inductance is necessary for designing a fully-integrated Class E power amplifier.

While we have analytic solutions to the element values of a Class E amplifier with an RF choke, the element values for finite dc-feed inductance should be obtained by solving a set of differential equations with iterative numerical methods [53], [59]. Based on Equations (A.6)-(A.11) (see Appendix A), the component values of the Class E amplifier can be obtained. For example, the specifications of Class E are assumed as follows: $V_{DD}$=1.8 V, carrier frequency=2 GHz, $P_{out}$=24 dBm (~250 mW), and the dc-feed inductance of 2 nH. The calculated component values are summarized on Table 2.2. The simulated switching voltage and current waveforms are also reported in Figure 2.8. For given parameters, the Class E switches normally and its output signal waveform approximates a sine wave, as shown in Figure 2.9. Therefore, design parameters for the Class E amplifier with a dc-feed inductor are available.

Table 2.2 Design parameters of the Class E amplifier.

| Parameter | Value | Units |
|---|---|---|
| $V_{DD}$ | 1.80 | V |
| $P_{out}$ | 250 | mW |
| f | 2 | GHz |
| $L_{ck}$ | 2 | nH |
| $R_L$ | 13.3 | Ω |
| $C_d$ | 2.53 | pF |
| $L_x$ | 0.591 | nH |
| $L_s$ | 2.53 | nH |
| $C_s$ | 2.50 | pF |

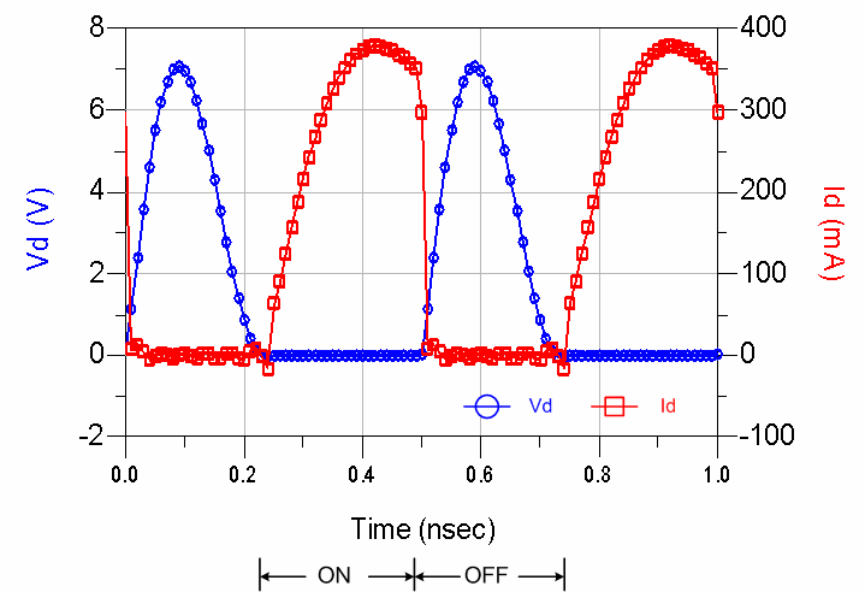



Figure 2.8 Switching voltage and switching current waveforms.

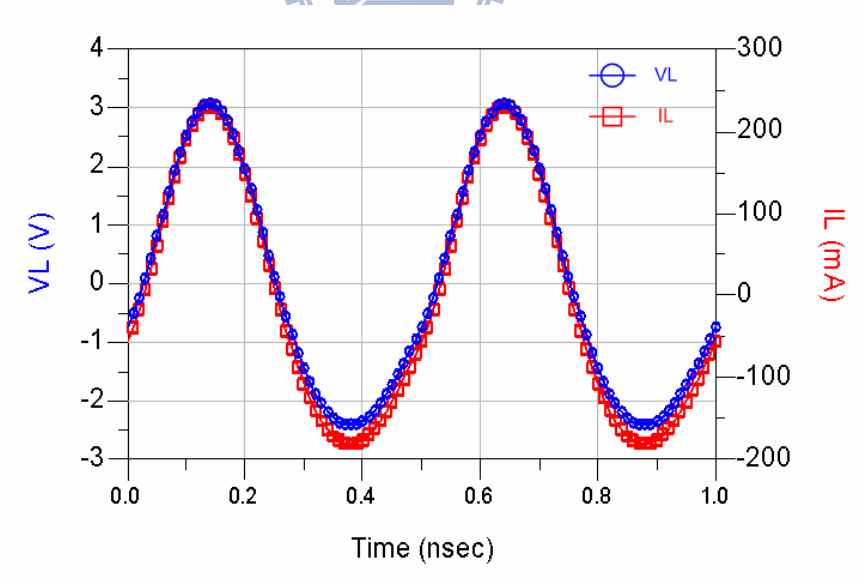



Figure 2.9 Output voltage and output current waveforms.

According to design equations mentioned previously, the required $R_L$ of Class E with a finite dc-feed inductance is 13.3 Ω and with an RF choke is 7.48 Ω on the same design

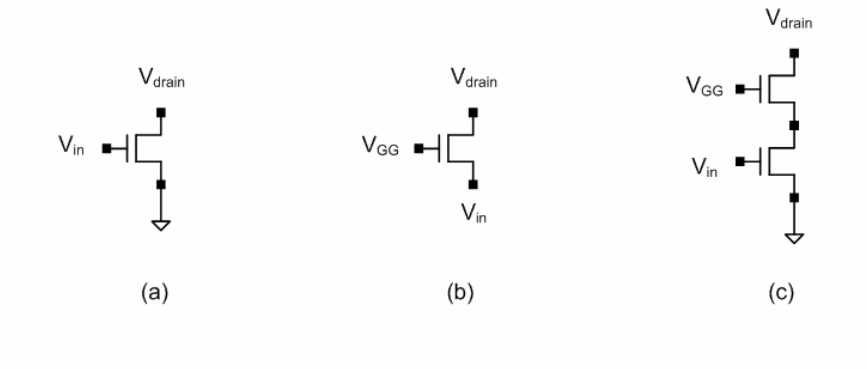
specifications. It was shown that the Class E configuration with finite dc-feed inductance increases the load resistance $R_L$ for a given output power and supply voltage by exploiting the property that the load resistance $R_L$ is a complex function of the dc-feed inductance.

In a Class E ensuring functionally switching, the inductor $L_{ck}$ can be either an RF choke or a finite inductor. One benefit of a finite inductance $L_{ck}$ instead of an RF chock is to provide the relief on the supply voltage and the load resistance [60]. If the dc-feed inductance is finite, we have one more degree of freedom, the value of dc-feed inductance, in choosing the element values for a given design requirement than with an RF choke.

## 2.2 Cascode-Based Topology

The feasibility of realizing efficient power amplifiers in regular CMOS technology is to receive increased attention because of considerable economic and fully-integration benefits. It was also shown that the Class E configuration with finite dc-feed inductance increases the load resistance $R_L$ for a given output power and supply voltage by exploiting the property that the load resistance $R_L$ is a complex function of the dc-feed inductance. For further increase of the load resistance $R_L$, it is desirable to find the way to allow high supply voltage for a given technology without stressing the transistors because the load resistance $R_L$ is basically proportional to the square of the supply voltage [53]. However, as the technology scale down the safe operating voltage will decrease.

Usually, the transistor is switched from the gate as shown in Figure 2.10 (a), but the maximum voltage across on the transistor is $V_{drain,max}$ can be as large as 3.56 times the dc supply voltage for an ideal Class E power amplifier. At this regard, gate-oxide breakdown, occurring when high voltages drop across the gate oxide, deserves particular care in a conventional common-source Class E power amplifier [58]. On the contrary, if the transistor is switched from source instead of the gate as shown in Figure 2.10 (b), the maximum voltage stress is reduced to $V_{drain,max}$-$V_{GG}$ because the source of the transistor swings up with the input voltage [61]. Therefore, the maximum allowable supply voltage is $V_{drain,max}/(V_{drain,max}$-$V_{GG})$ times larger for common gate switch than that for a common-source switch. The common-gate switch presents the input driving stage with a low impedance node, differing from the common-source switch with a high impedance node.




| | | (a) | (b) | (c) |
|---|---|---|---|---|
| ON | $V_{GS,max}$ | $V_{GG}$ | $V_{GG}$ | $V_{GG}$ |
| | $V_{DS,max}$ | 0 | 0 | 0 |
| OFF | $V_{GS,max}$ | 0 | 0 | $V_{GG}-V_T$ |
| | $V_{DS,max}$ | $V_{drain,max}$ | $V_{drain,max}-V_{GG}$ | $V_{drain,max}-V_{GG}+V_T$ |

(d)

Figure 2.10 (a) Common-source switch, (b) Common-gate switch, (c) Common-gate switch combined with common-source stage, (d) Maximum voltage stress for each case assuming the voltage $V_{in}$ swings from 0 to $V_{GG}$.

In order to avoid the damage to the transistor due to the low breakdown voltage in CMOS process and the low impedance driving node, the cascode topology is a viable way in designing Class E power amplifiers [42] [62]. In Figure 2.10 (c), a common-source stage is combined with the common-gate switch into the cascode topology. In this way, the maximum drain voltage is divided between the two devices, and also the maximum oxide voltage drop reduces since a constant voltage $V_{GG}$ is applied on the gate of common-gate transistor. During the OFF state, the drain voltage of the common-source switch transistor rises to $V_{GG}$-$V_T$. The maximum drain-source voltage drop, therefore, reduces from $V_{drain,max}$ to $V_{drain,max}$-$V_{GG}$+$V_T$. The additional benefit of the cascode Class E is the reduced output-input coupling [63].

The important feature of the Class E for communication system applications is the mechanism of modulating the supply voltage. Although cascode implementations of Class E

power amplifiers are present in the literatures, the source of AM-AM and AM-PM distortion as supply modulation has never been discussed nor identified.

## 2.3 Summary

This chapter gives an overview of Class E power amplifiers. The overview of the switching power amplifier designs, including common-source topology and cascode-based topology, are given. The design methodology of common-source Class E amplifiers with RF choke has been revisited, and for the fully-integration purpose the amplifiers with finite dc-feed inductor has also been described. The cascode topology, for reliability analysis in CMOS process technology, of Class E power amplifiers is required and its characteristics are also studied.

# Chapter 3

# Design Considerations of Cascode Class E Power Amplifiers

For reliability analysis and fully integration, the cascode Class E power amplifier with a small dc-feed inductance is a good candidate for communication system applications. For high efficiency transmitter applications, the characteristics of the cascode Class E power amplifier should be identified, especially in AM-AM and AM-PM distortion. In this chapter, Section 3.1 describes a design of CMOS cascode Class E power amplifier. Section 3.2 introduces the cause of AM-AM and AM-PM distortion. The physically based analysis compare with the simulation analysis give more details and understandings on the cause of the distortion.

## 3.1 Operation Waveform Analysis

The cascode Class-E power amplifier, shown in Figure 3.1, consists of two nMOS transistors, a dc-feed inductor, and output network comprised of a shunt capacitor, a series LC circuit and an impedance matching network. The series LC circuit appears inductive at the carrier frequency and the impedance matching network made of $L_m$-$C_m$ transforms 50 Ω, representative of the antenna resistance, into $R_L$. The inductor $L_s$, $L_x$ and $L_m$ can be realized by the inductor $L_{out}$. The shunt capacitor $C_p$ is implemented entirely by a parasitic capacitor of the transistor $M_2$ drain to ground. The transistor $M_1$ is biased at threshold voltage for a 50% duty cycle while the transistor $M_2$ is applied by a dc voltage $V_{GG}$. The input signal is used to switch the transistor $M_1$ on and off.

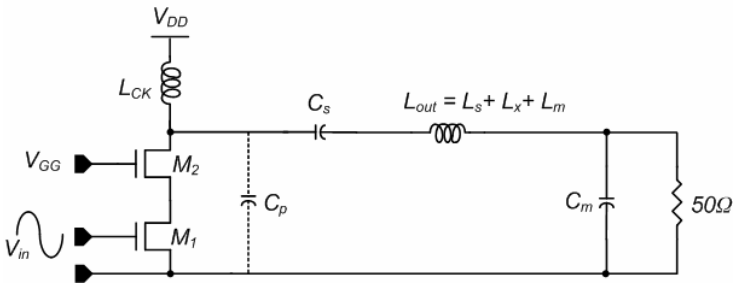



Figure 3.1 CMOS cascode Class E power amplifier.

Table 3.1 Design parameters of cascode Class E amplifier.

| Device | Value | Units |
|---|---|---|
| $L_{ck}$ | 2 | nH |
| $C_p$ | 1.1 | pF |
| $C_s$ | 5 | pF |
| $L_{out}$ | 2.5 | nH |
| $C_m$ | 0.9 | pF |

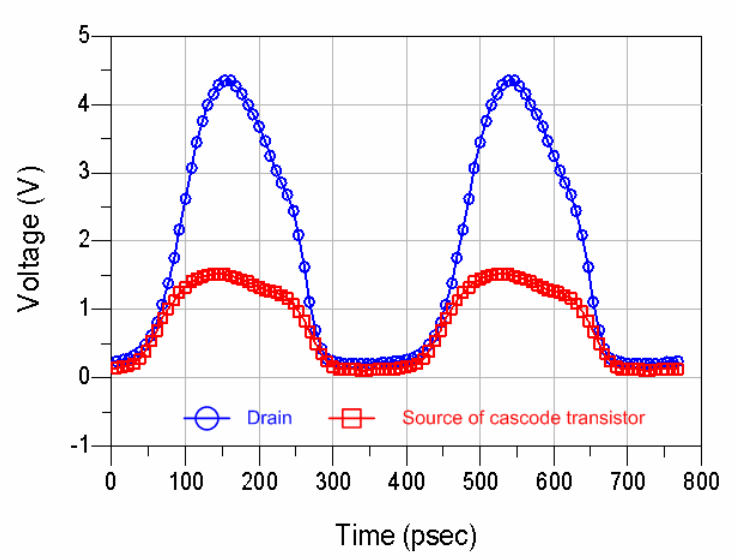



Figure 3.2 Simulated waveforms of the cascode Class E power amplifier.

For design specifications of $f$ = 2.6 GHz and $P_{out}$ = 125 mW (~21 dBm), all design parameters of the cascode Class E amplifier with a dc-feed inductor can be obtained, referring to the analytic solution in Appendix A. All component values of a CMOS 0.18 μm Class E amplifier are summarized on Table 3.1. The additional degree of freedom provided by finite dc-feed inductance $L_{ck}$=2 nH is set, whereas $L_{ck}$ is small enough to be implemented in CMOS process. The shunt capacitance is entirely absorbed by the output capacitances of cascode transistor. For an ideal Class E power amplifier with an RF choke, the peak voltage stress on the switch is no longer $3.56V_{DD}$. For practical Class E power amplifiers, the peak voltage can be as low as $2.4V_{DD}$, as illustrated in the simulated waveforms in Figure 3.2, which is obtained from ADS simulation of the circuit in Figure 3.1 with $V_{GG}$ = 1.8 V and $V_{DD}$ = 1.8 V. In order to switch the common-source transistor correctly, the input power of 6 dBm is required. Due to the voltage at the source of cascode transistor is nearly $V_{GG}$-$V_{TH}$, the maximum voltage stress of $V_{drain,max}$ is reduced to $V_{drain,max}$-$V_{GG}$+$V_{TH}$, where the threshold voltage $V_{TH}$ is ~ 0.45 V.

The correct component values of output network allows the drain voltage and current of the transistor $M_2$ operating separately without the overlap of waveforms and tunes out the desired frequency at the output load. However, in practice, the transistor $M_1$ has a finite on-resistance and transition time from the OFF-state to the ON-state. Therefore, the peak voltage is reduced to $2.4V_{DD}$ due to the nonzero on-resistance. These factors cause a certain amount of power dissipation on the switch, resulting in a reduction in power efficiency [60]. The simulated drain efficiency of the amplifier is degraded to 60%, and the output power is 18.5 dBm.

## 3.2 Physical Analysis of AM-AM and AM-PM Distortion

In EER or polar transmitters, the Class-E PA is driven by two input signals, one is the constant-envelope RF signal and the other is the modulating signal delivering to the PA supply voltage. The RF output signal, therefore, can be recombined by the Class E power amplifier. However, when the PA is in supply modulation, the modulated transistors cause the

AM-AM and AM-PM distortion on the RF output signal. The AM-AM distortion is the difference between the supply voltage and the envelope of the RF output voltage. Such a difference is caused by a nonlinear relationship between the supply voltage and the envelope of the RF output signal. The AM-AM distortion in the RF PA itself can be kept low if it is always operated as a switching amplifier. In other words, the supply voltage of the PA driver stage will be kept high to ensure the switching nature of the amplifier. Besides the AM-AM, the AM-PM distortion will also be presented in the circuit. This distortion is an unwanted phase modulation of the RF output carrier due to the modulation of the supply voltage. The distortion will severely degrade the system emission performances. It is necessary to identify the cause of this distortion in order to recover the transmitted RF signal.

## 3.2.1 Device Operation

As drain amplitude modulation of PAs, the transistor $M_1$ still acts as a switch, however, the transistor $M_2$ operating in different mechanisms dependents on the variations of supply voltage. When the transistor $M_1$ is turn-on, the voltage across these two transistors is very low because the transistor $M_1$ acts as a switch and the transistor $M_2$ only provides a path for current-flowing. When the transistor $M_1$ is cut-off, no current flows from the transistor $M_2$ drain to ground and the transistor $M_2$ drain voltage is still allowed to surpass the supply voltage.

In small supply voltage range, the transistor $M_2$ operates in the deep-triode region and therefore its drain-source voltage, $V_{DS2}$, is very low, occupying extremely small voltage headroom. $V_{DS2}$ means the dc component of the $M_2$ drain-source voltage, $V_{ds2}$. When the supply voltage is large enough to completely turn the transistor $M_1$ on, the transistor $M_2$ has the ability of current driving and occupies the significant drain-source voltage. According to the statement above, the voltage $V_{DS2}$ can be expressed as

$$V_{DS\,2} = 0 \qquad \text{, for } V_{DD} < V_c \quad (3.1)$$

$$V_{DS\,2} = V_{DD} \times \frac{\frac{1}{2}V_{DD,\max}}{V_{DD,\max} - V_c} - V_c \times \frac{\frac{1}{2}V_{DD,\max}}{V_{DD,\max} - V_c} \qquad \text{, for } V_{DD} \geq V_c \quad (3.2)$$

where $V_{DD,max}$=1.8 V, $V_c=(V_{GG}-V_{TH})/\lambda$ and λ is the ratio of the $M_2$ maximum drain voltage to $V_{DD,max}$. When λ is 2.4, $V_c$ is ~ 0.6 V. In Equations (3.1) and (3.2), the effect of the maximum drain voltage of the Class-E amplifier has been included. Equations (3.1) and (3.2) illustrate that the drain-source voltage of the transistor $M_2$ is changed not only by the supply $V_{DD}$ but also by the gate-biased voltage of the transistor $M_2$. In other words, the voltage $V_{DS2}$ is simultaneously modulated by the supply voltage and the voltage $V_{GG}$.

The theoretical result of Equations (3.1) and (3.2), and simulated $V_{DS2}$ are plotted in Figure 3.3. The supply $V_{DD}$ is swept from 0 to 1.8 V by 0.2 V per step. It shows that the theoretical result has a good agreement with the simulated result. It indicates that the operating mechanisms of transistors are varied with the modulated supply voltage. On this operating condition, the relationship of the voltage $V_{DS2}$ and the supply voltage is nonlinear. Furthermore, this variant condition of the transistor $M_2$ leads to a nonlinear drain-source voltage, which will also introduce a non-constant capacitance and a non-constant transconductance.

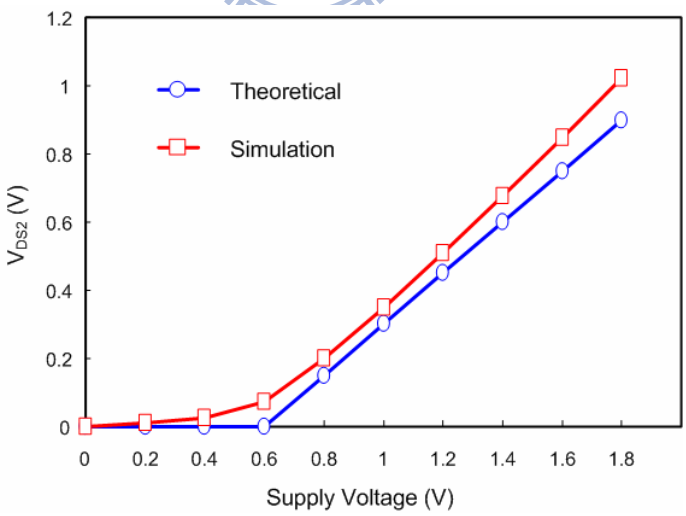



Figure 3.3 Theoretical and simulation results of $V_{DS2}$ against supply voltage.

### 3.2.2 I/V Curve

As the variations of $V_{DD}$, the transistor $M_1$ and $M_2$ operate in different operating mechanisms, which can be illustrated by drain voltage waveform of the transistor $M_1$ and $M_2$, respectively. The simulated drain voltage waveforms of the transistor $M_1$ and $M_2$ are reported in Figure 3.4. The supply voltage is swept from 0 V to 1.8 V by 0.2 V per step. As $V_{DD} \leq 0.6$ V, the transistor $M_1$ acts as a switch and the transistor $M_2$ just performs a transmission path for the current drawn from the power supply to $M_1$. The drain voltage waveforms of the transistor $M_1$ and $M_2$ are almost the same because the required drain-source voltage of the transistor $M_2$ is very small. When the supply approximates 0.6 V, the transistor $M_1$ is close to completely switching and the transistor $M_2$ begins to have the capability of amplifying the desired signal.

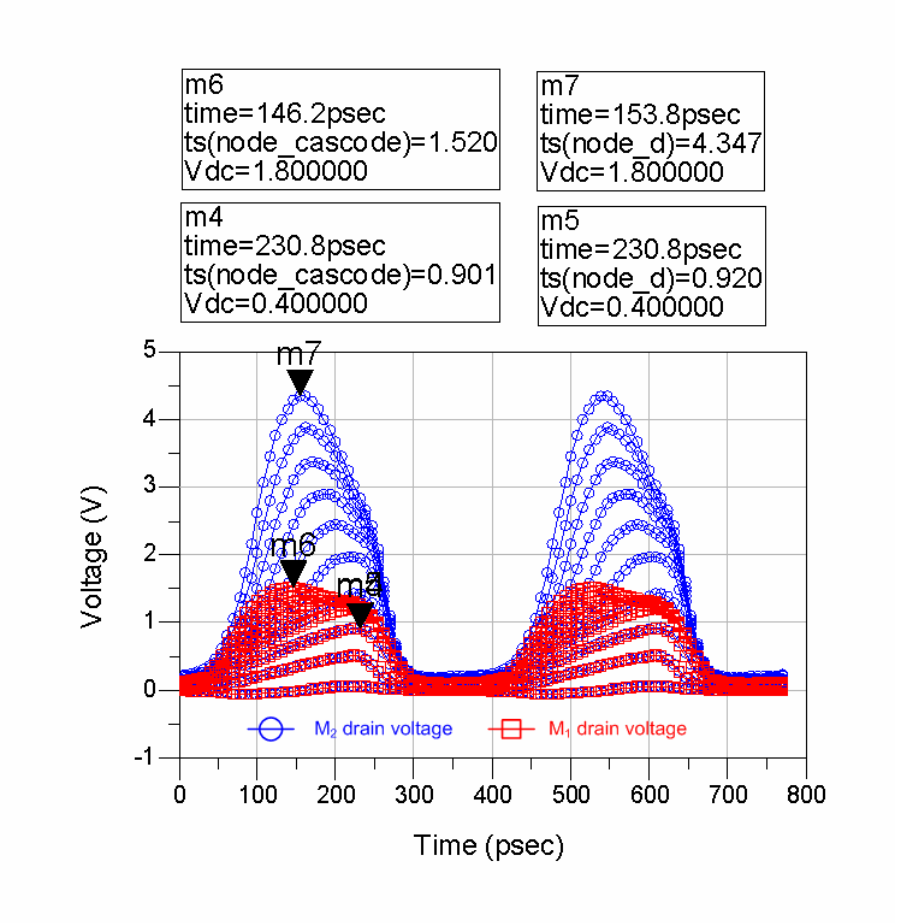



Figure 3.4 Drain voltage of $M_1$ and $M_2$ as the variations of $V_{DD}$.

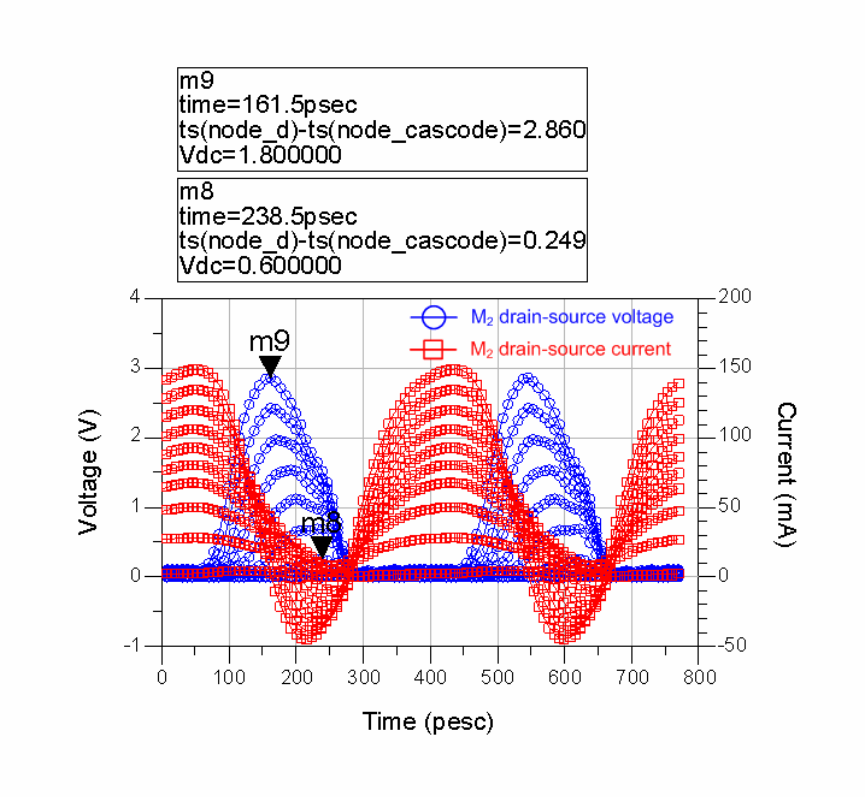



Figure 3.5 Drain-source voltage and drain current of $M_2$.

When $V_{DD}$ > 0.6 V, the drain voltage of transistor $M_1$ only has the slightly increase, but, the drain voltage of transistor $M_2$ begins to increase proportionally to $V_{DD}$. In this operating condition, the transistor $M_1$ acts as a switch and the transistor $M_2$ gradually amplifies the signal with the increased supply voltage. Furthermore, in order to understand the operating mechanisms of transistors, the drain-source voltage and drain waveforms of the transistor $M_2$ as shown in Figure 3.5 can have an illustration on that.

Figure 3.5 shows the drain current increases proportionally to the supply voltage. This indicates that the amplifier can regularly operate in the varied supply voltage. However, the drain-source voltage only amplifies proportionally to the supply voltage, as the supply voltage is swept from 0.6 to 1.8 V. It is owing to the transistor $M_2$ operating in different regions. Unfortunately, due to this nonlinear relationship of the voltage and current, the amplifier will have an amplitude error and a phase error on the RF output signal.

### 3.2.3 Impedance Variation

When modulating the PA supply voltage, the transistor $M_2$ operating in different regions has nonlinear drain voltage and current output waveforms, which are caused by a nonlinear capacitance and a transconductance. Moreover, the PA output signal would accompany the nonlinear characteristics of the transistor $M_2$. In this work, we propose that the drain-source impedance variation of the transistor $M_2$ is the cause of the AM-AM and AM-PM distortion. This can be understood by the physical model depicted in Figure 3.6.

This simplified equivalent model consists of the gate-source capacitor ($C_{gs2}$), the gate-drain capacitor ($C_{gd2}$), the drain-bulk capacitor ($C_{db2}$) and the current-source ($g_{m2}\cdot V_{gs2}$). Given an insight into impedance analysis, the capacitance $C_{db2}$ and transconductance $g_{m2}$ can be given by Equations (3.3) and (3.4).

$$C_{db2} = \frac{C_{j0}}{\sqrt{1+\frac{V_{DB2}}{V_{bi}}}} \tag{3.3}$$

$$g_{m2} = \mu_n C_{OX} \left(\frac{W}{L}\right)_{M_2} (V_{GS2} - V_{TH}) \tag{3.4}$$

where $V_{bi}$ is the built-in potential of the body diode, $C_{j0}$ is the output capacitance as the drain-bulk voltage $V_{DB2}$=0 and $V_{GS2}$ is the dc component of the $M_2$ gate-source voltage, $V_{gs2}$. Equations (3.1) and (3.2) show that the variations of the supply voltage caused a nonlinear voltage $V_{DS2}$. In Equation (3.4), the voltage $V_{GS2}$ can also be expressed as $V_{GG}$-($V_{DD}$-$V_{DS2}$). Substituting Equations (3.1)-(3.2) into Equations (3.3) and (3.4), the relationship of $C_{db2}$ and $g_{m2}$ against $V_{DD}$ are plotted in Figure 3.7. $C_{gd2}$ is difficult to be expressed by the close form of voltages. However, the values of $C_{gd2}$ are obtained by the interpolation method and also have been included in Figure 3.7. The result indicates that, as $V_{DD}$ is swept from 0 to 1.8 V, the nonconstant capacitances and the nonconstant tranconductance are introduced.

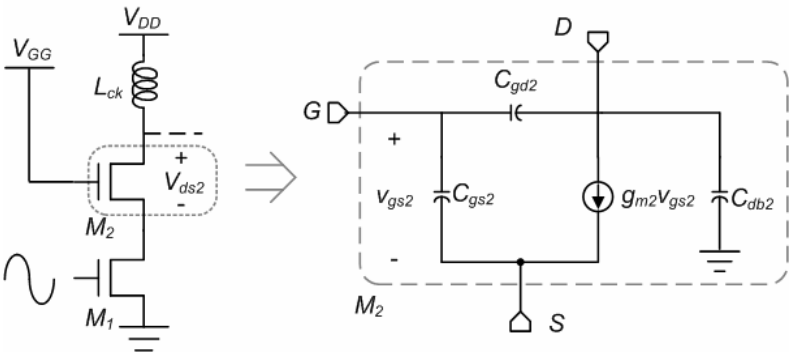



Figure 3.6 Equivalent model of the transistor $M_2$.

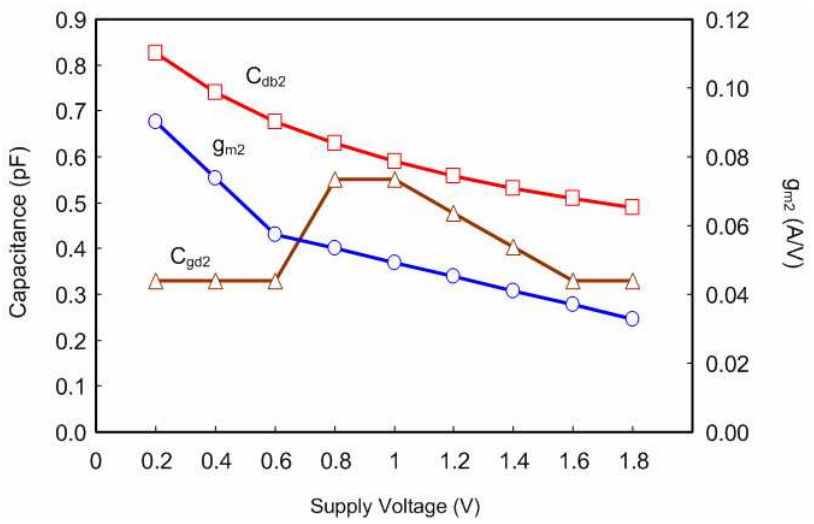



Figure 3.7 Theoretical results of $C_{db2}$, $C_{gd2}$ and $g_{m2}$ against supply voltage.

Since the component values are non-constant, the equivalent drain-source impedance, $Z_{ds2}$, at the carrier frequency should be non-constant. The impedance $Z_{ds2}$ is derived according to the equivalent model and has been given by Equation (3.5).

$$Z_{ds\,2} = \frac{V_{ds\,2}}{I_{ds\,2}} = \frac{V_{ds\,2}}{g_{m\,2}V_{gs\,2} + j\omega_o C_{db\,2}V_{ds\,2} + j\omega_o C_{gd\,2}\lambda V_{DD}}$$

$$= \frac{V_{ds\,2}}{g_{m\,2}(V_{GG} - (\lambda V_{DD} - V_{ds\,2})) + j\omega_o (C_{db\,2}V_{ds\,2} + C_{gd\,2}\lambda V_{DD})} \qquad (3.5)$$

where $I_{ds2}$ and $\omega_o$ denote the $M_2$ drain-source current at the carrier frequency and angular frequency, respectively. Equation (3.5) shows how the impedance $Z_{ds2}$ is a function of the transconductance, capacitances and voltages. Furthermore, the transconductance, capacitances and voltages in Equations (3.3)-(3.5) can be expressed as a function of $V_{DD}$, respectively. In order to simplify the analysis, the magnitude of $Z_{ds2}$, $|Z_{ds2}|$, has been plotted against $V_{DD}$ as shown in Figure 3.8, where $|Z_{ds2}|$ has been given by Equation (3.6).

$$
\begin{aligned}
|Z_{ds2}| &= \left|\frac{V_{ds2}}{I_{ds2}}\right| = \left|\frac{V_{ds2}}{g_{m2}V_{gs2} + j\omega_o C_{db2}V_{ds2} + j\omega_o C_{gd2}\lambda V_{DD}}\right| \\
&= \left|\frac{V_{ds2}}{g_{m2}(V_{GG} - (\lambda V_{DD} - V_{ds2})) + j\omega_o (C_{db2}V_{ds2} + C_{gd2}\lambda V_{DD})}\right| \\
&= \sqrt{\frac{V_{DS2}^2}{(g_{m2}(V_{GG} - \lambda V_{DD} + V_{ds2}))^2 + (\omega_o (C_{db2}V_{ds2} + C_{gd2}\lambda V_{DD}))^2}}
\end{aligned}
\tag{3.6}
$$

The comparison in Figure 3.8 shows that the theoretical result is in good agreement with the simulated result and also proves that the variant capacitances and the transconductance of $M_2$ really bring a nonconstant $|Z_{ds2}|$. This non-constant impedance will be converted to an imperfect voltage waveform, equally the magnitude and phase errors, at the $M_2$ drain node. The difference between the theoretical result and the simulated result is due to the saturation voltage of transistors and the voltage drops on $L_{ck}$ are neglected. Furthermore, the PA output signal accompanies with the magnitude and phase errors from the $M_2$ drain node, so-called the AM-AM and AM-PM distortion. The simulated AM-AM and AM-PM distortion has been shown in Figure 3.9.

The result reveals that the relationship of the envelope of the RF output voltage against the supply voltage is nonlinear and the voltage deviation at $V_{DD}$=0 V causes an additional distortion at low envelope levels. When the supply voltage deviates from its optimum value of 1.8 V down to 0.5 V the maximum AM-PM changes by 21 degrees/V and 21° of the phase error. In the supply voltage of 0 V to 0.5 V, the AM-PM is highly nonlinear and the phase error is as large as 78°. These characteristics indicate that low envelope levels are harder to reconstruct than high envelope levels.

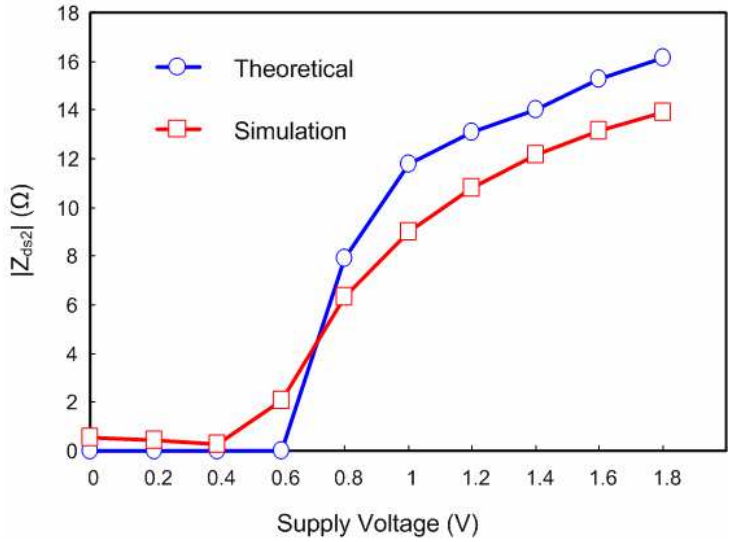



Figure 3.8 Theoretical and simulated result of $|Z_{ds2}|$ against supply voltage.

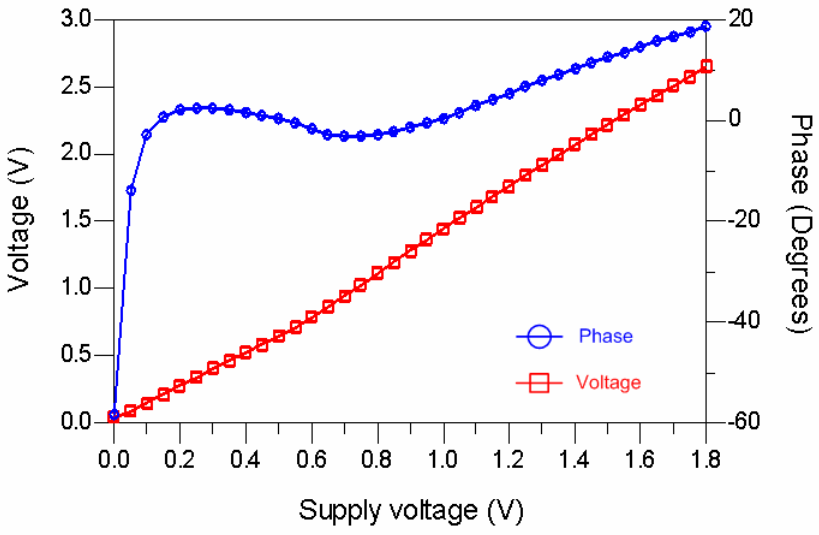



Figure 3.9 AM-AM and AM-PM distortion.

## 3.3 Summary

A prototype of cascode Class E power amplifier using CMOS technology has been presented. The characteristics of the cascode Class E amplifier in supply modulation have also been discussed. The theoretical analysis and simulation results illustrate that the cascode transistor operating in different regions cause the non-constant equivalent impedance at the drain node as the supply voltage is modulated. The impedance results in the magnitude and phase errors at the drain voltage as well as the AM-AM and AM-PM distortion on the output signal.

# Chapter 4

# Innovative Linearity Compensation Technique

Since the cause of the AM-AM and AM-PM distortion has been discussed, a technique for compensating this distortion is presented in this chapter. By controlling the gate voltage of the cascode transistor, the nonlinear effects at its drain node are minimized and the AM-AM and AM-PM distortion at the output node are improved. Furthermore, the efficiency performance of the amplifier is also discussed. In this chapter, Section 4.1 describes the compensation technique for AM-AM and AM-PM distortion. The comparison results of the amplifier with and without compensation are reported. The efficiency performance, as the amplifier has been linearized, is discussed in Section 4.2.

## 4.1 Improved AM-AM and AM-PM

Since the non-constant impedance causes the nonlinear effect at the cascode transistor drain node as well as the AM-AM and AM-PM distortion at the output load, having a constant $|Z_{ds2}|$ should be allowed to minimize the distortion. In supply modulation, the cascode transistor is driven by two input signals, one is from the drain node and the other is from the source node. The drawing current therefore is simultaneously reacted by the gate-source voltage $V_{GS2}$ and the drain-source voltages $V_{DS2}$. Moreover, the voltage $V_{GS2}$ and $V_{DS2}$ are the function of the $V_{DD}$ and can be expressed as Equations (4.1) and (4.2), respectively, where $V_{DS1}(V_{DD})$ means $V_{DS1}$ varied with $V_{DD}$. The equations also show that $V_{GS2}$ and $V_{DS2}$ are correlated to each other. When $V_{DS1}$ is nonlinear against $V_{DD}$, $V_{GS2}$ and $V_{DS2}$ are also nonlinear against $V_{DD}$, and

the non-constant component values are introduced.

$$V_{GS2} = V_{GG} - V_{DS1}(V_{DD}) \tag{4.1}$$

$$V_{DS2} = V_{DD} - V_{DS1}(V_{DD}) \tag{4.2}$$

In order to obtain a constant $|Z_{ds2}|$, it is feasible to get $V_{GS2}$ and $V_{DS2}$ linearly against $V_{DD}$, and the components value is linearly against $V_{DD}$. According to the Equation (3.4) the voltage of $V_{GS2} - V_{TH}$ should be linearly against $V_{DD}$. And substituting the Equations (4.1) and (4.2), the impedance $|Z_{ds2}|$ can be expressed by the parameters of $V_{GG}$ and $V_{DD}$. Therefore, the $M_2$ gate voltage is changed to $V_{DD} + V_{TH}$, which forces the transistor $M_2$ to act a resistance alike. When the cascode transistor has been operated as a resistance as shown in Figure 4.1, it is expected that the impedance $|Z_{ds2}|$ is constant.

In Figure 4.1, the adder produces a voltage, which equals the threshold voltage $V_{TH}$ plus the supply $V_{DD}$, on the $M_2$ gate node and therefore the transistor $M_2$ will be operated as a resistance. During drain amplitude modulation, the adder output voltage varied with the supply $V_{DD}$ always forces the transistor $M_2$ to operate as a resistance while the transistor $M_1$ acts as a switch. Therefore, a constant $|Z_{ds2}|$ is obtained and its simulated result has been shown in Figure 4.2. It shows that the voltage $V_{DS2}$ is linearly against the supply voltage and hence the constant $|Z_{ds2}|$ is obtained.

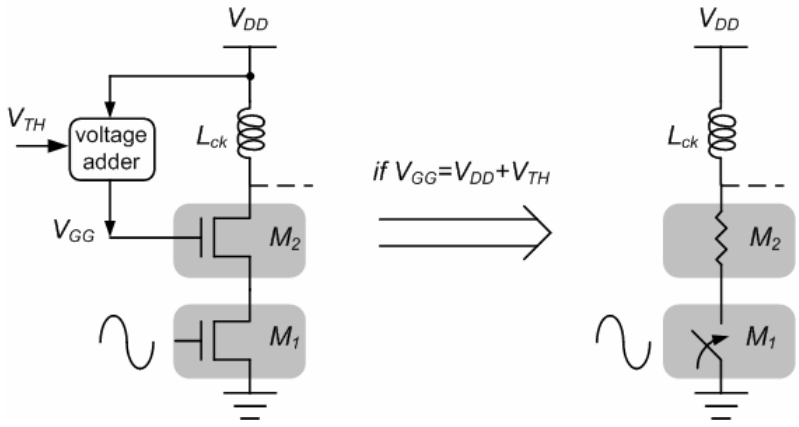



Figure 4.1 Equivalent schematic of the PA with AM-AM and AM-PM compensation.

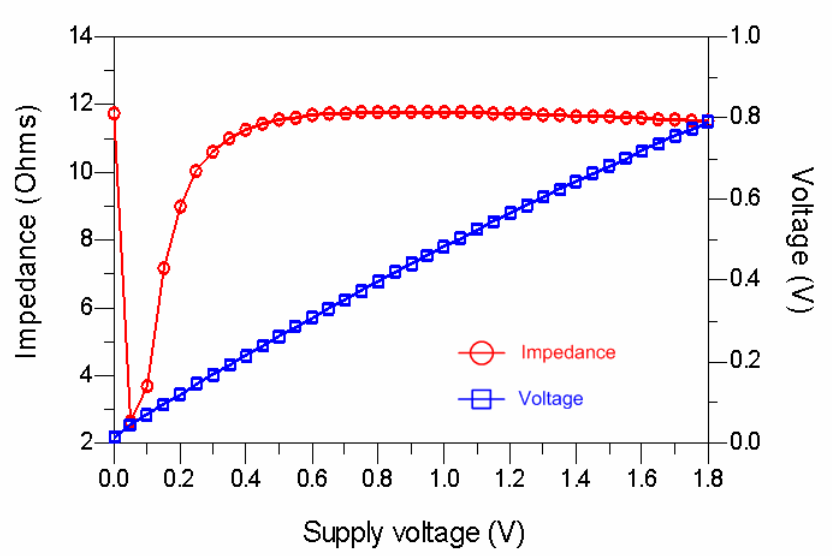



Figure 4.2 Simulated results of $|Z_{ds2}|$ and $V_{DS2}$ against supply voltage.

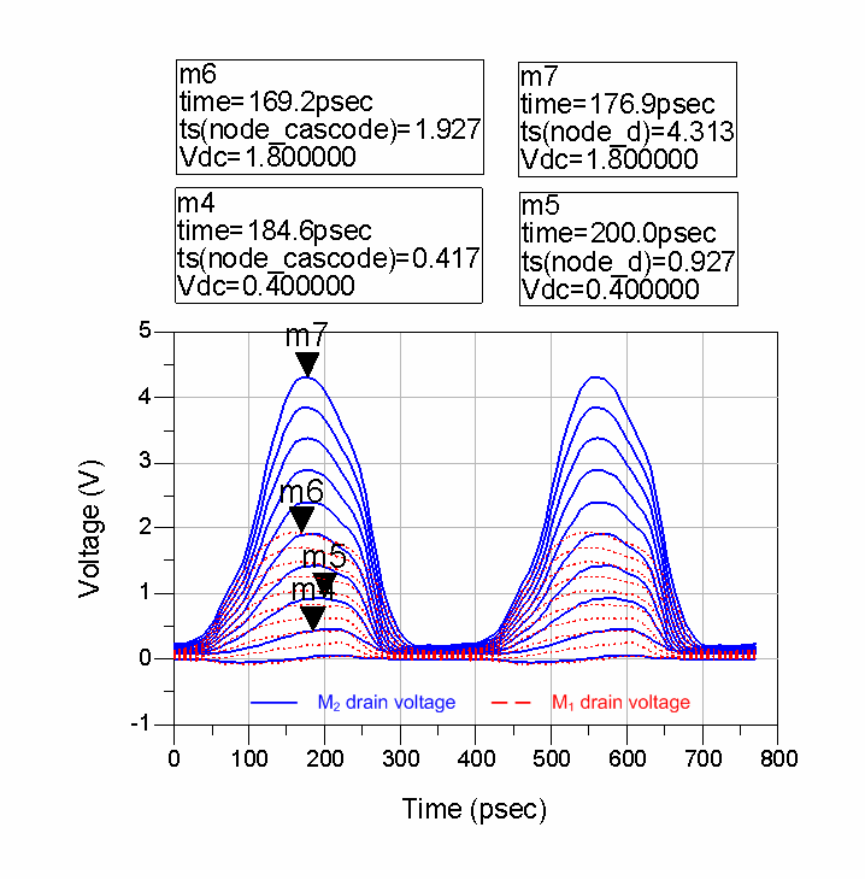



Figure 4.3 Simulated results of $M_1$ and $M_2$ drain voltages against supply voltage.

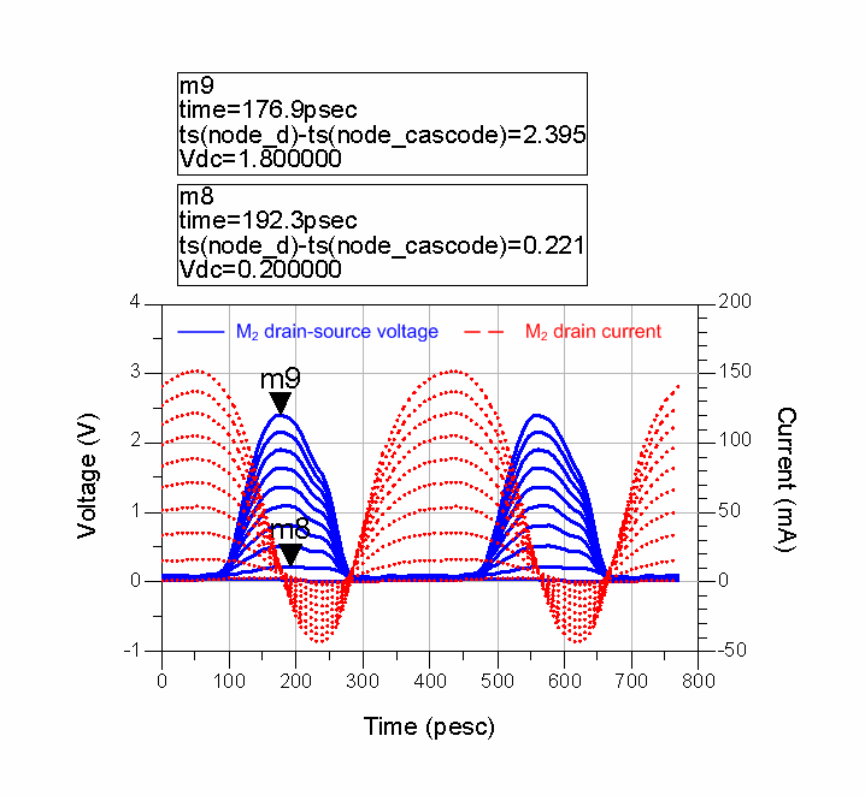



Figure 4.4 Simulated results of $M_2$ drain-source voltage and drain-source current against supply voltage.

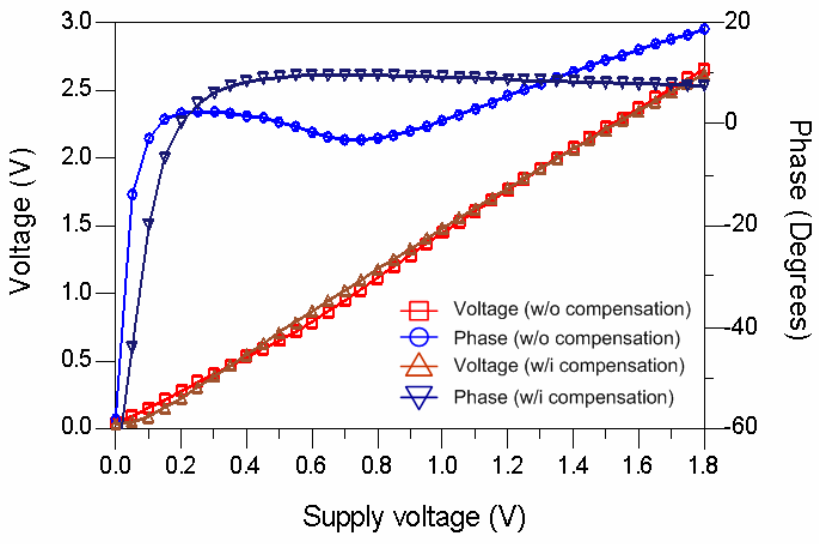



Figure 4.5 Compared AM-AM and AM-PM distortion.

Figure 4.3 shows the simulation results of $M_1$ drain voltage and $M_2$ drain voltage. The supply voltage is swept from 0 V to 1.8 V by 0.2 V per step. As expected, both the maximum drain voltages are proportionally increased with the supply voltage. It has much improvement comparing with the result in Figure 3.4. The results of $M_2$ drain-source voltage and drain current are shown in Figure 4.4. The drain-source voltage is also proportionally varied with the increase of the supply voltage. Therefore, when the cascode transistor $M_2$ is degenerated into a resistance, the linear voltage $V_{DS2}$ and the constant impedance $|Z_{ds2}|$ are achieved.

The results of the PA with and without the AM-AM and AM-PM compensation are compared in Figure 4.5. When the PA has the compensation, the relationship of the magnitude of the output voltage against the supply voltage is linear and the AM-PM in the supply voltage of 0.5 V to 1.8 V is improved from 21° to 2.2°. The proposed methodology evidently has compensated the AM-AM and AM-PM distortion of the PA during supply modulation.

## 4.2 Efficiency Improvement

One more advantage of the transistor $M_2$ operating as a resistance is to improve the drain efficiency in low supply voltage and extend the operating supply range. The dc current $I_{DC}$ in [64] can be rewritten by Equation (4.3), where $V_{dmin}$ means the finite drain-source voltage during the transistor conducting and $R_s$ is the source terminal resistance. The relationship between the PA efficiency and the dc current $I_{DC}$ is given in Equation (4.4). When the PA with or without the proposed compensation methodology, operating on the identical conditions of $P_{out}$ and $V_{DD}$, drain efficiency is inversely proportion to $I_{DC}$.

$$I_{DC} = \frac{\pi\omega(C_{db2} + C_{gd2})(V_{DD} - V_{dmin})}{1 + 2\pi\omega R_s(C_{db2} + C_{gd2})} \tag{4.3}$$

$$\text{Efficiency} = \frac{P_{out}}{P_{DC}} \times 100\% \propto \frac{P_{out}}{V_{DD} I_{DC}} \propto \frac{1}{I_{DC}} \tag{4.4}$$

Figure 4.6 shows the results of $I_{DC}$ against the supply voltage. In small supply voltage, the $I_{DC}$ value of the PA with compensation is less than the PA without compensation and

therefore drain efficiency of the PA is increased as shown in Figure 4.7. The maximum improvement of 20% is achieved at $V_{DD}$=0.55V. This improvement benefits the operation of the PA in low supply voltage. When modulating the supply voltage of the Class E PA, the consistent efficiency in entire operating supply range is demanded. In other words, the proposed methodology extends the operating supply range during supply modulation since the PA has the slightly degradation on drain efficiency in high supply voltage. The degradation in high supply voltage is due to the equivalent resistance has more dc power consumptions (see Appendix B). The results of power gain and output power against the supply voltage are also reported in Figure 4.8, where the input driving power is 6dBm. When the amplifier is compensated, the power gain and output power of the PA are not degraded. The result indicates that the proposed methodology can compensate the AM-AM and AM-PM distortion of the Class-E power amplifier without degrading the PA performance.

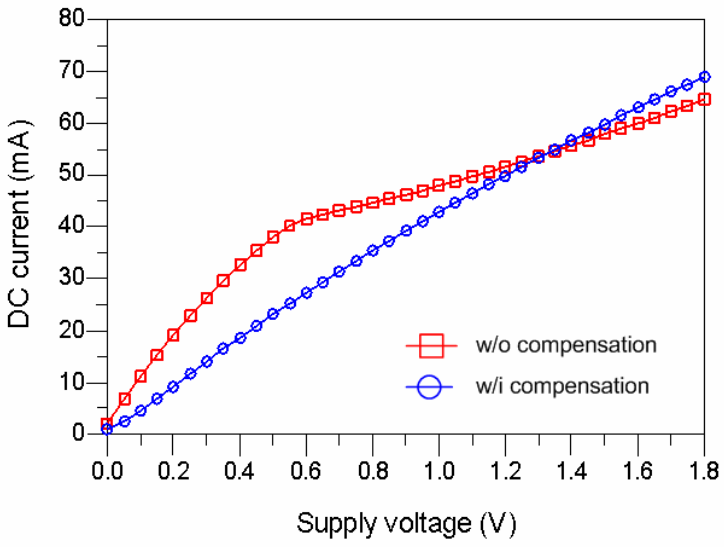



Figure 4.6 Compared dc current.

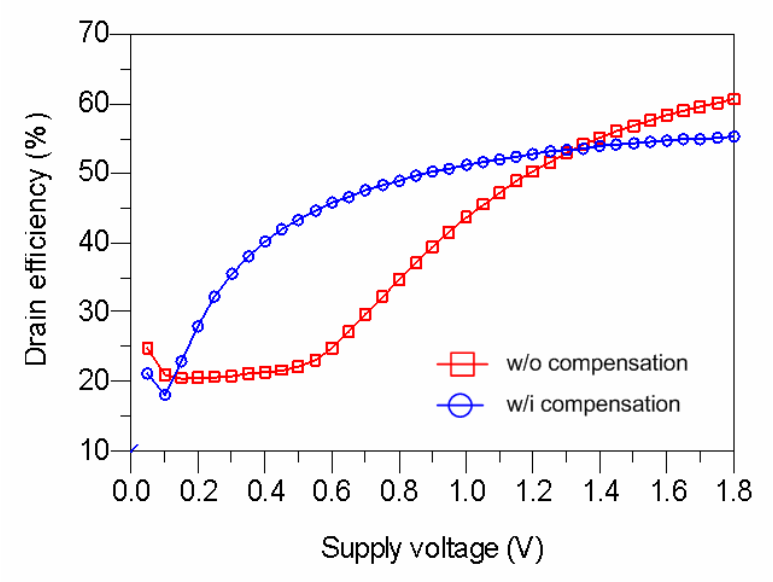



Figure 4.7 Compared drain efficiency.

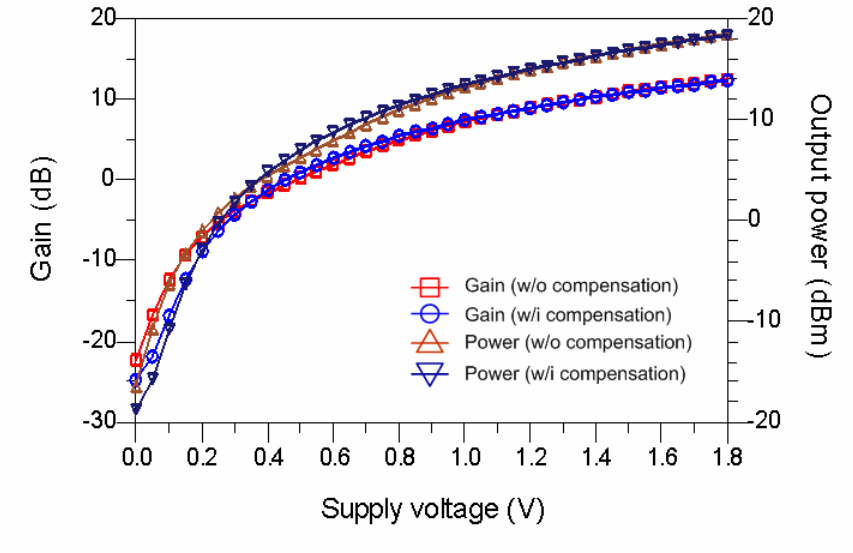



Figure 4.8 Gain and output power against supply voltage.

## 4.3 Summary

The design methodology for compensating the AM-AM and AM-PM distortion has been proposed in this chapter. By changing the gate bias voltage of the cascode transistor, the distortion is compensated and its comparison results of the PA with and without compensation have also been reported. In the operating supply range, the AM-PM phase error has been reduced from 21° to 2.2°. Furthermore, the efficiency performance has the maximum improvement of 20% when the PA has been compensated.

# Chapter 5

# Circuit Implementation and Experimental Results

In order to demonstrate the proposed compensation technique, designs of cascode Class E power amplifier and cascode Class E with auto-biasing control circuit have been implemented in CMOS technology process. In the design of Class E, the gate bias voltage of cascode transistor applied by the external supply intends to give a comparison of the AM-AM and AM-PM characteristic between the PA with and without compensation. Furthermore, the cascode Class E with auto-biasing control circuit is an example to show the PA with improved AM-AM and AM-PM characteristic. All of simulation and measurement results demonstrate that the compensation technique is allowed for improving the AM-AM and AM-PM distortion. In this chapter, the design of cascode Class E power amplifier and its measured results are described in Section 5.1. Section 5.2 presents the design of cascode Class E with self-biased control circuit and its measured results. The performances are summarized in Section 5.3.

## 5.1 CMOS Cascode Class E PA Design

### 5.1.1 Circuit Design

A fully integrated cascode Class E power amplifier has been implemented in a 0.18 μm

CMOS technology, as shown in Figure 5.1. The cascode topology of Class E amplifiers is used due to the concern of low breakdown voltage in CMOS process. For highly integration, all of passive devices are implemented by the internal components. The amplifier operates at 2.6 GHz from a 1.8 V supply voltage. The input matching network is designed to transfer the amplifier input impedance to 50 Ω at the carrier frequency. The series of $L_s$-$C_s$ is designed to have a 2.6 GHz resonant frequency. The 50 Ω load resistance is down-converted by means of the $L_m$-$C_m$ network. A fit value of the inductor $L_x$ is selected to separate the drain voltage waveform and the current waveform. The inductor $L_s$, $L_x$ and $L_m$ are integrated with an internal inductor. The series of $L_a$-$C_a$ is implemented to improve power efficiency [51]. A way to minimize the power loss is to tune out the parasitic capacitances by the inductor $L_a$, resonating parasitic capacitances on node P at the desired frequency of operation. A blocking capacitor $C_a$ is inserted between the inductor $L_a$ and ground. The RF choke is implemented by a small dc-feed inductance using an internal inductor. Considering the electrical performance of internal inductors, they have an allowed current density of 1mA/μm at the temperature of 85°C, and the maximum metal width of 20 μm, the thickness of 2 μm. Therefore, avoiding the metal damage of $L_{ck}$, the PA was designed to have an allowed current capacity. Hence, the large output power and drain efficiency are not the major design targets in this amplifier. The aspect sizes of the transistor $M_1$ and $M_2$ are 1080/0.18 μm/μm.

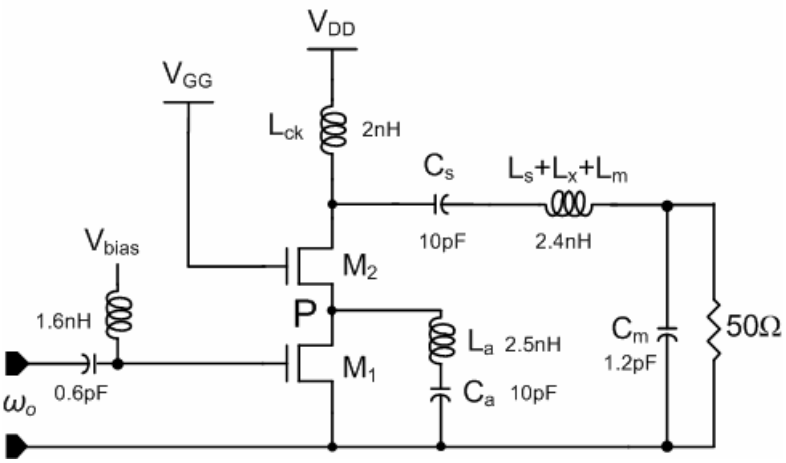



Figure 5.1 Cascode Class E power amplifier.

### 5.1.2 Simulation Results

A performance comparison is accomplished between the design of cascode Class E power amplifier without compensation and with compensation. The signal power of 6 dBm is applied at the input of the Class E amplifier. For the Class E amplifier without compensation the voltage $V_{GG}$ is applied at 1.8 V and for with compensation the voltage $V_{GG}$ is applied by $V_{DD}+V_{TH}$, where $V_{TH}$ is 0.5 V. The $V_{DD}$ is swept from 0 V to 1.8 V, per 0.1 V step. The comparison of AM-AM and AM-PM is shown in Figure 5.2. The relationship between the supply voltage and the envelope of the RF output signal has been linearized when the amplifier with compensation. The phase error is also improved from 15° to 2° as the $V_{DD}$ is swept from 0.5 V to 1.8 V. In other words, it can see that the operating supply voltage range has been extended. The simulated results of drain efficiency and dc current are reported in Figure 5.3. The PA without compensation has the maximum drain efficiency of 40%. Due to the low quality of internal inductors, the large resistive losses of inductors result in the low drain efficiency of amplifiers When the PA with compensation, the amplifier consumes the less dc currents in small supply voltage and therefore can have the maximum improved efficiency of 13% at the $V_{DD}$ of 0.6 V. Furthermore, the efficiency against the supply voltage is nearly constant in the extended operating supply voltage range. The peak drain efficiency is reduced to 37% at the $V_{DD}$ of 1.8 V. The amplifier has a maximum power gain of 10 dB and a maximum output power of 16 dBm as the $V_{DD}$ is 1.8 V, as shown in Figure 5.4.

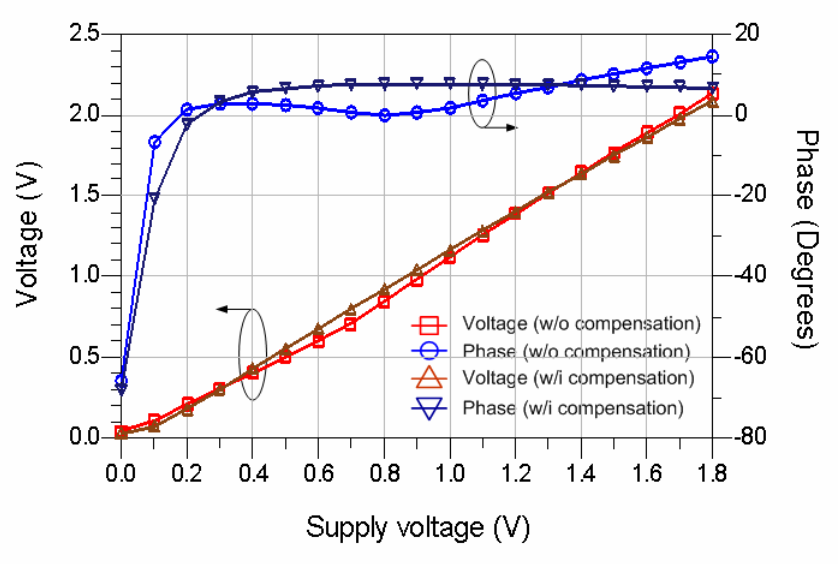



Figure 5.2 Simulation results of the AM-AM and AM-PM distortion.

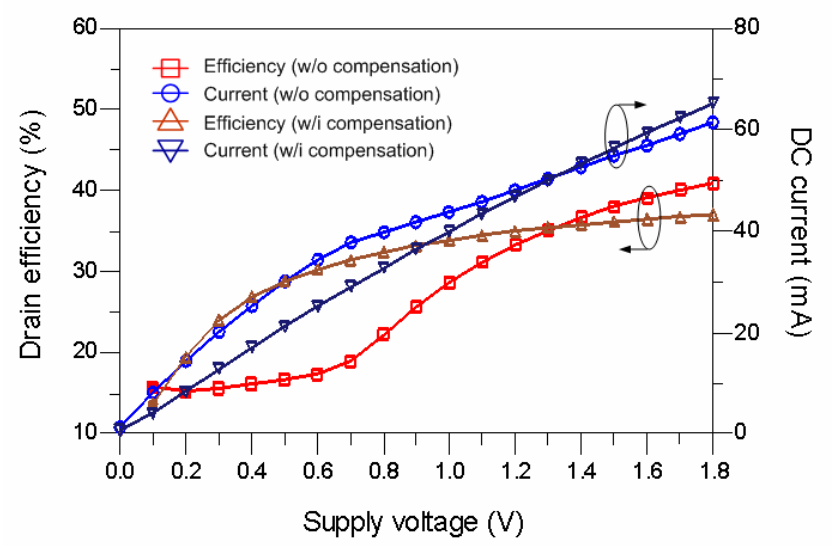



Figure 5.3 Simulation results of drain efficiency and dc current.

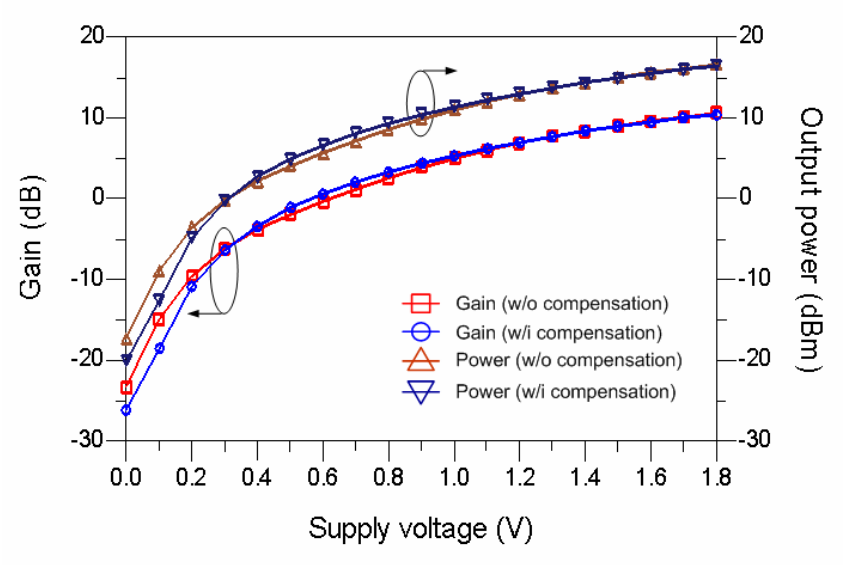



Figure 5.4 Simulation results of power gain and output power.

## 5.1.3 Experimental Results

The fully-integrated cascode Class E power amplifier has been implemented in CMOS 0.18 μm process. The chip photo is shown in Figure 5.5 and it has a die area of 1.25×1.3 $mm^2$. The measurement setup is shown in Figure 5.6. The signal power is 6 dBm and the $V_{DD}$ is swept from 0 V to 1.8 V. The output signal power is extracted from the spectrum analyzer and the output signal phase is extracted from the phase elements of S21 s-parameter by the network analyzer. For the condition of the PA without compensation, the $V_{GG}$ is applied at 1.8 V. For the PA with compensation, the $V_{GG}$ equals to ($V_{DD}$ + 0.5) V. The measured results are reported in Figures 5.7 and 5.8. Figure 5.7 shows the comparison result of the AM-AM and AM-PM distortion. It reveals that when the PA without compensation the output envelope voltage is nonlinear to the supply voltage. When with compensation, the linear relationship between the envelope voltage and the supply voltage is obtained. The PA with compensation has improved the phase shift of the output signal from 30˚ to 6˚ when $V_{DD}$ is 0.4 V to 1.8 V. At $V_{DD}$ below 0.5 V, the significant phase shift of the output signal due to the incomplete switching of transistor $M_1$ may severely degrade the system performance. Hence, an operating

voltage of above 0.5 V is recommended for EER/polar applications [49], [71]. Figure 5.8 shows the measured results of drain efficiency and output power. When the PA without compensation, the efficiency has the severe variation from 4.5% to 12% as the $V_{DD}$ is swept from 0.7 V to 1.8 V. When with compensation, the efficiency has the nearly constant value of 9%. When with compensation, the maximum output power is reduced from 9 dBm to 8 dBm at the supply voltage of 1.8 V. Due to the reduction on the measured PA power gain the output power and efficiency are decreased.

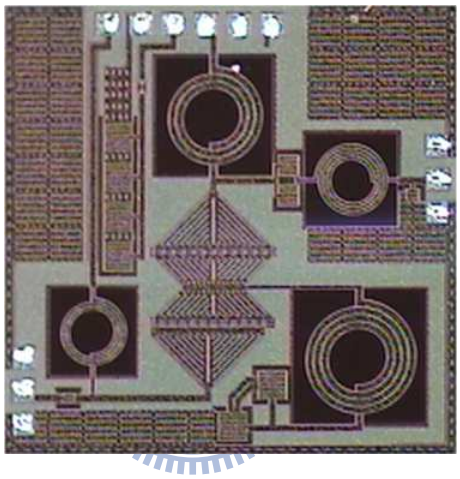


Figure 5.5 Chip photo of cascode Class E power amplifier.

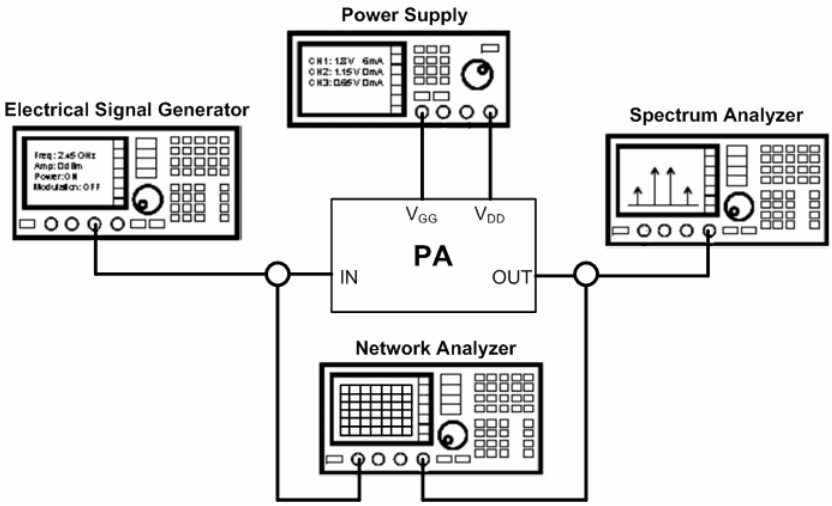



Figure 5.6 PA measurement setup.

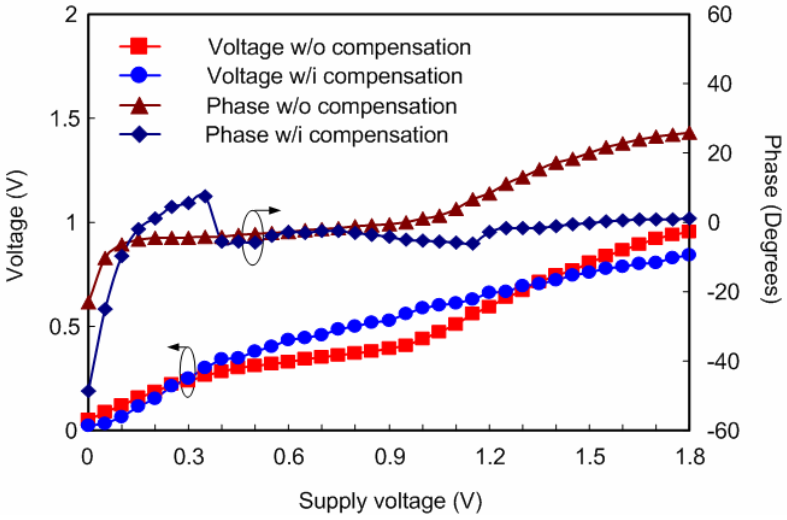



Figure 5.7 Measured results of AM-AM and AM-PM distortion.

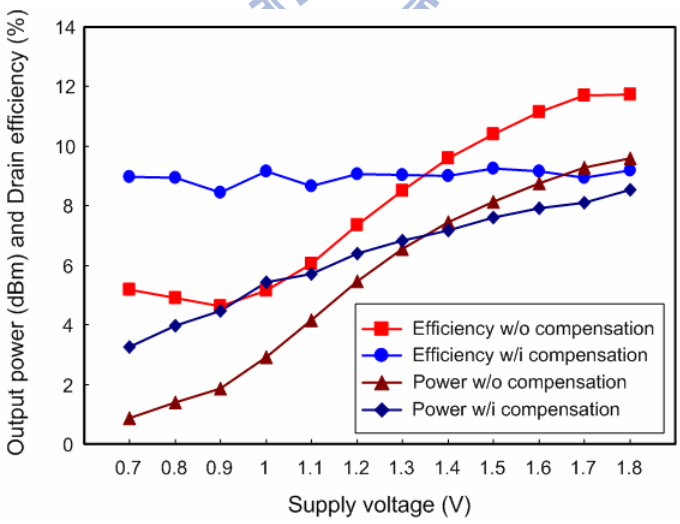


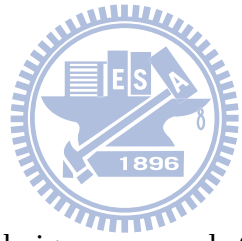

Figure 5.8 Measured results of output power and drain efficiency.

### 5.1.4 Summary

In order to demonstrate the proposed compensation technique of the AM-AM and AM-PM distortion, a cascode Class E PA has been proposed and implemented in CMOS process technology. By the given external control voltage, the comparison results between the PA with compensation and without compensation are obtained. The results demonstrates that the proposed technique for improving the AM-AM and AM-PM distortion of the output signal can effectively decrease the phase shift and linearize the output envelope voltage.

## 5.2 Cascode Class E PA with Self-Biased Control Circuit Design

### 5.2.1 Circuit Design



In order to realize the proposed technique, a cascode Class-E power amplifier shown in Figure 5.1, with a self-biased control circuit for compensating the AM-AM and AM-PM distortion has been implemented in a 0.18 μm CMOS technology process, as shown in Figure 5.9. The self-biased control circuit intends to produce a voltage, the sum of a dc voltage and an analogue voltage. It is implemented by a voltage adder, including an operating amplifier with five resistors. Selecting the ratio of resistors, the expected output voltage is obtained. The operating amplifier has the unit-gain frequency of 100 MHz for achieving a correct output voltage of the self-biased control circuit during supply modulation. The control circuit is just to produce an expected $M_2$ gate voltage $V_{GG}= V_{DD} + V_{TH}$, so that it only needs to draw few micro-amperes from the 3.3 V supply.

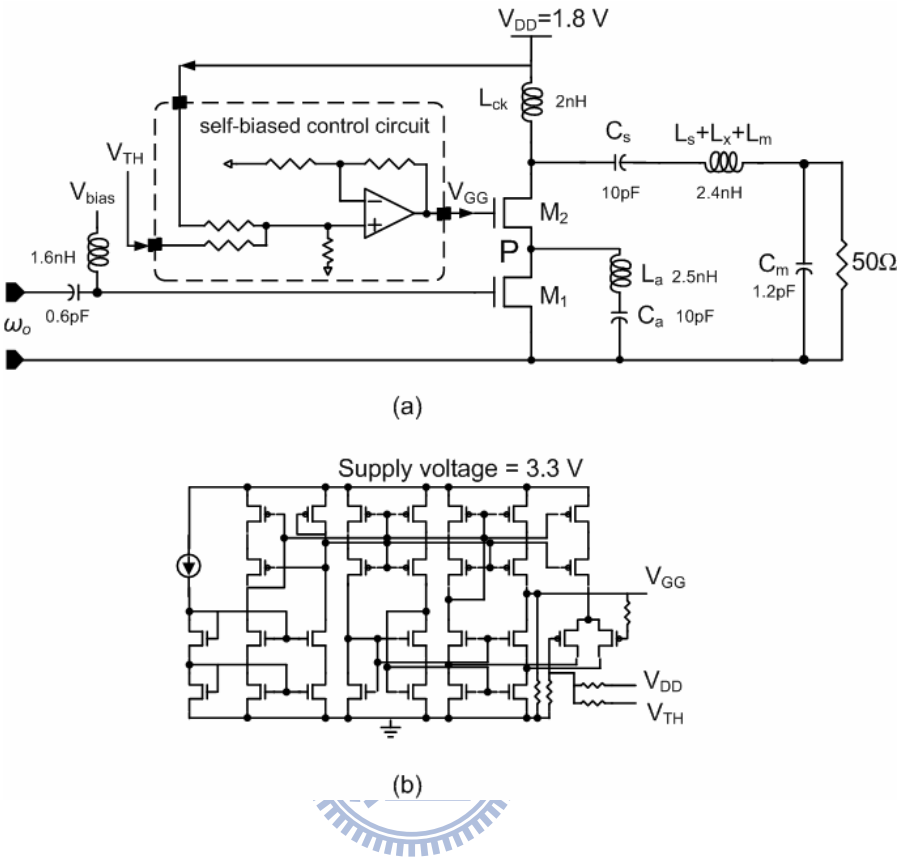



Figure 5.9 Detailed schematic of (a) cascode Class E PA with self-biased control circuit, and (b) self-biased control circuit.

## 5.2.2 Simulation Results

The result of the PA with self-biased control circuit is reported in Figure 5.10. The relationship of the envelope of the output voltage against the supply voltage is linear and the AM-PM in the supply voltage of 0.5 V to 1.8 V is less than 3°. Therefore, the proposed technique evidently has compensated the AM-AM and AM-PM distortion of the PA during supply modulation. The amplifier has the maximum output power of 16 dBm and drain efficiency of 38%, as shown in Figure 5.11. The drain efficiency is varied from 30% to 38% as the $V_{DD}$ is swept from 0.5 V to 1.8 V. The figure also shows the amplifier has the maximum PAE of 37% and the PAE is severely degraded with the decreased supply voltage, especially in small supply voltage.

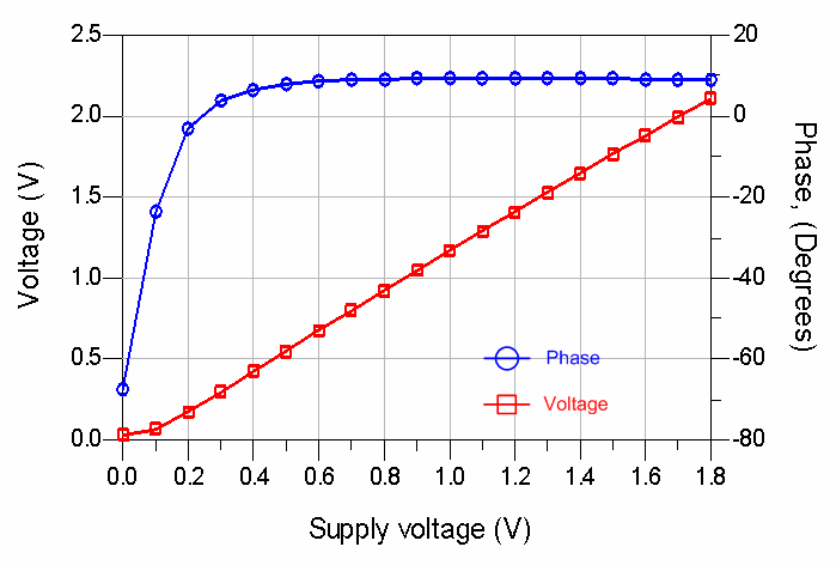



Figure 5.10 Simulation results of the AM-AM and AM-PM distortion.

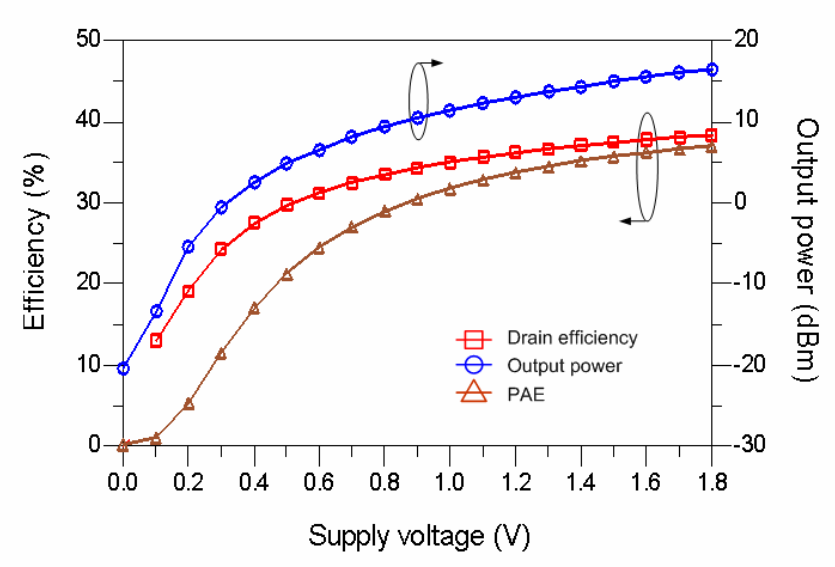



Figure 5.11 Simulation results of efficiency and output power.

### 5.2.3 Experimental Results

Fabricated prototypes have been measured by the probe testing. The chip photomicrograph is reported in Figure 5.12. Total die area is 1.6 mm². Figure 5.13 shows the PA measurement setup. The expected gate bias voltage of $M_2$ can be achieved when $V_{DD}$ is swept. Figure 5.14 shows the measured characteristics of the AM-AM and AM-PM of the PA. The phase error is reduced down to 5° as $V_{DD}$ is swept from 0.7 V to 1.8 V. A linear voltage relationship is also obtained and there is a small deviation in low supply voltage, from 0 V to 0.3 V. As expected, the AM-AM and AM-PM distortion of the Class-E PA has been compensated by using proposed design technique. The prototype delivers an output power of 12dBm with an input driving power of 6dBm from a 1.8 V supply voltage and. The output power can be regulated by changing the supply voltage of the amplifier. Figure 5.15 shows the measured output power, drain efficiency and power-added efficiency versus $V_{DD}$. The output power increases proportionally to $V_{DD}^2$, varying from -2 dBm to 12 dBm, as $V_{DD}$ is swept from 0.3 V to 1.8 V. In small supply voltage, the transistors can not be completely on so that the amplifications of the RF signal are not available. Drain efficiencies are 17.8% in $V_{DD}$ of 0.5 V to 1.8 V. As the supply voltage below 0.6 V, the PAE has seriously reductions, whereas the PAE reduces when the output power becomes comparable to the input power. Due to the targeted output power reduced from 16 dBm to 12 dBm, the maximum PAE is reduced to 16.6%. The output power and power gain versus the input power are also reported in Figure 5.16. The PA has the output power of 12 dBm and power gain of 6 dB with an input driving power of 6dBm. When the input driving power is above 7dBm, the power gain of the PA is degraded to 5dB. The result of the output power versus frequency is shown in Figure 5.17. The output power is above 12 dBm in the 2.3 GHz to 2.8 GHz frequency band, leading the power amplifier to operate in a wide frequency band. The maximum PAE in this wide frequency band is 23.5%.

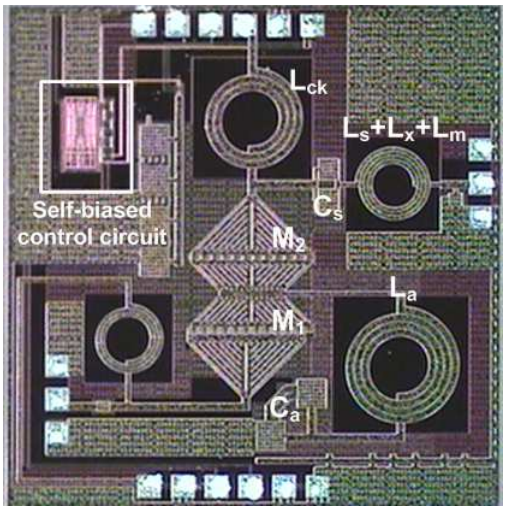



Figure 5.12 Chip photo of Class E amplifier with self-biased control circuit.

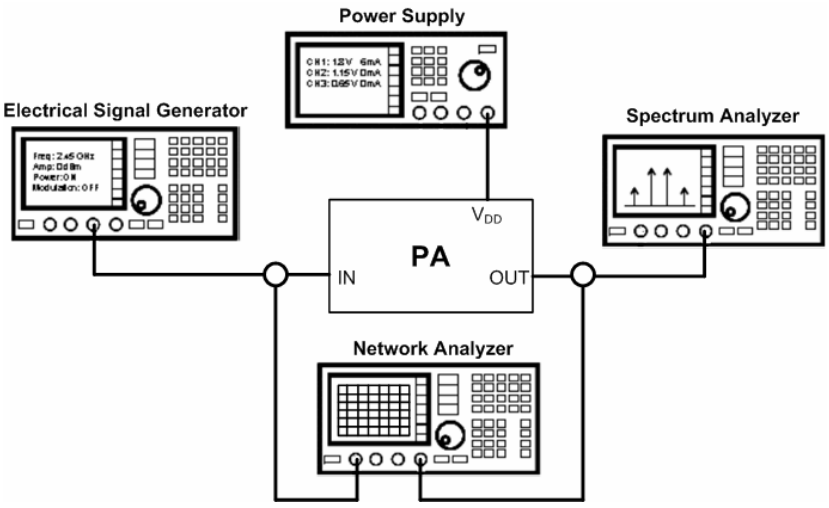



Figure 5.13 PA measurement setup.

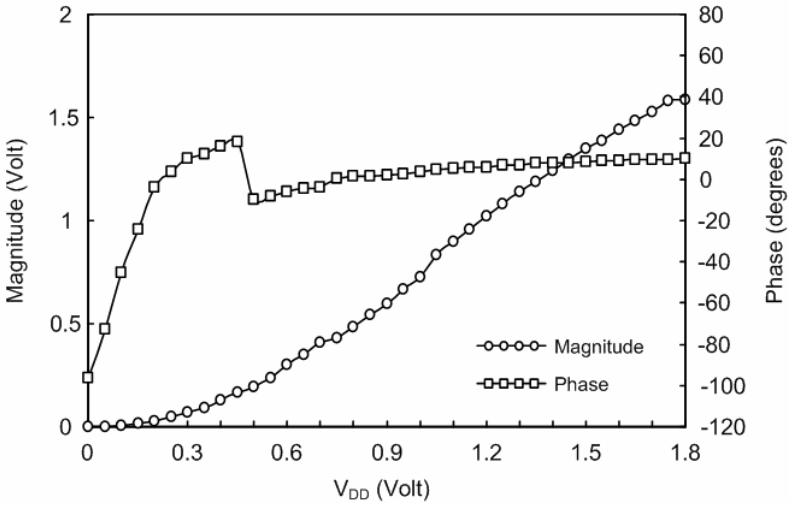



Figure 5.14 Measured results of the AM-AM and AM-PM distortion.

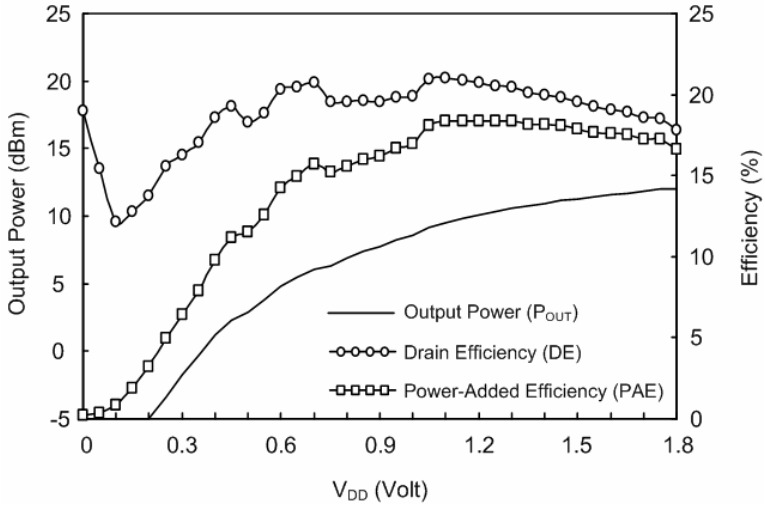



Figure 5.15 Measured output power, PAE and drain efficiency versus supply voltage.

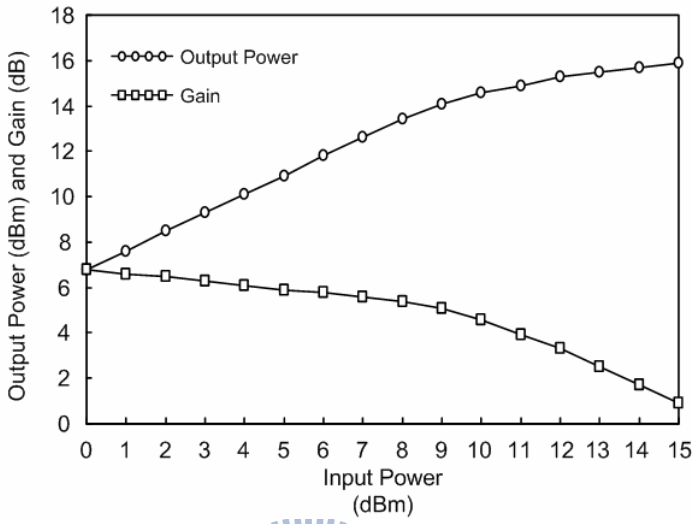



Figure 5.16 Measured output power and power gain versus input power.

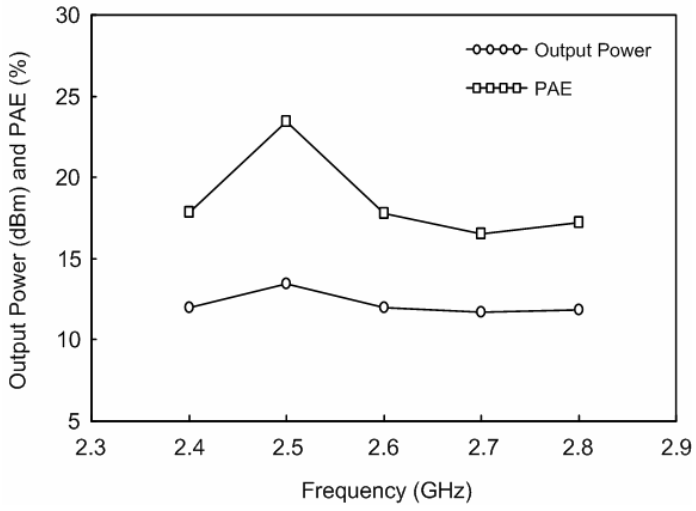



Figure 5.17 Measured output power and PAE versus frequency.

The design proposed here shows that the AM-AM and AM-PM distortion of the cascode Class-E PA has been compensated by a self-biased control circuit without dissipating more power. However, because of the concern of an allowed current capacity on the top metal layer, the aspect sizes of the transistors for efficiency optimization are difficult to achieve. Therefore, the equivalent series resistances of the transistor are large when the transistor is on, so that the reduction on the drain voltage waveform and the output power. Due to the reduction of the output power, the efficiency of the amplifier is also reduced.

### 5.2.4 Summary

A cascode Class E amplifier with AM-AM and AM-PM compensation has been implemented in CMOS technology process. The proposed compensation technique is realized by the internal auto-biasing control circuit. The measured results have demonstrated that the proposed compensation technique can effectively improve the AM-AM and AM-PM distortion of the Class E amplifier.

## 5.3 Summary

Designs of the Class E PA and the Class E PA with self-biased control circuit are implemented in CMOS 0.18 μm technology process. All of measured results show that the AM-AM and AM-PM distortion is improved as the Class E has been compensated by proposed technique. The AM-AM and AM-PM characteristic curves are important that they are a linear and a flat response to change in the supply voltage, respectively, in polar modulation. Furthermore, it is also to minimize the level of predistortion needed in polar modulation. The results are summarized in Table 5.1. The comparison result has also been summarized in Table 5.2.

Table 5.1 Performance summary.

| | | Simulation | Measurement |
|---|---|---|---|
| Cascode class E PA | Without compensation | 15° (0.5V – 1.8V) | 30° (0.4V – 1.8V) |
| | With compensation | 2° (0.5V – 1.8V) | 6° (0.4V – 1.8V) |
| Cascode class E PA with self-biased control circuit | | 3° (0.5V – 1.8V) | 5° (0.7V – 1.8V) |

Table 5.2 Comparison results.

| Design | Process (nm) | Freq. (GHz) | Compensation | Results |
|---|---|---|---|---|
| [42] | 250 | 0.9 | - | - |
| [50] | 130 | 1.7 | - | - |
| [61] | 180 | 1.9 | - | - |
| [51] | 65 | 2 | - | 18° (0.4V-1V) |
| [28] | 130 | 2 | Pre-distortion | 12° (0.2V-1V) |
| This work (simulated) | 180 | 2.6 | Self-biased | 3° (0.3V-1V) |
| This work (measured) | 180 | 2.6 | Self-biased | 5° (0.4V-1V) |

# Chapter 6

# RF/Baseband System Co-verification

The chapter presents the verification of AM-AM and AM-PM distortion in the system level. The co-verification platform is addressed in Section 6.1. The comparison results are described in Section 6.2.

## 6.1 RF/Baseband Co-verification Platform

An EER system co-simulation were performed in ADS-Ptolemy using an IEEE 802.11a OFDM-based waveform (36 Mbits/s, 52 carriers, 16-QAM modulation scheme and modulation bandwidth=20 MHz) up-converted to 2.6 GHz frequency band and the simulation platform of an EER is shown in Figure 6.1. In the platform, all of system blocks are ideal equation-based components, except the Class-E power amplifier. In the transmitter part, the modulation signal is up-converted and then amplified through an EER transmitter. In the receiver part, the received signal is down-converted and demodulated by a signal demodulator. The EVM and constellation performances can be evaluated by sink components such as Error Vector Magnitude Measurement. Furthermore, the EER transmitter shown in Figure 6.2 consists of a delay cell, an envelope detector, a limiter, an envelope amplifier and the Class E power amplifier. The power amplifier is driven by the voltage of approximately 1.2 V peak-to-peak swing. The compensated delay mismatch between the envelope path and the phase path is estimated by 2.8 ns for 40 dBc IMD (intermodulation distortion) [65]. The histogram of envelope voltage in Figure 6.3 shows that 93% of envelope voltages are in the range from 0.5 V to 1.8 V with a mean voltage of 1 V. It was obtained by adjusting the gain

of the envelope amplifier.

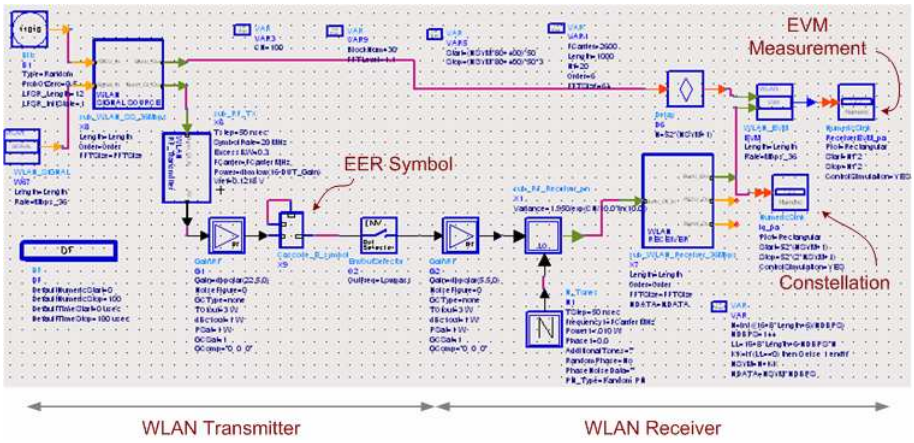



Figure 6.1 The system co-verification platform.

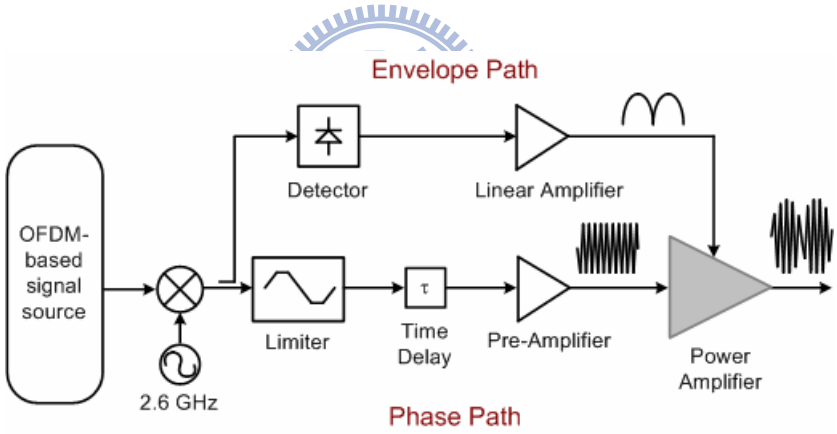



Figure 6.2 EER transmitter.

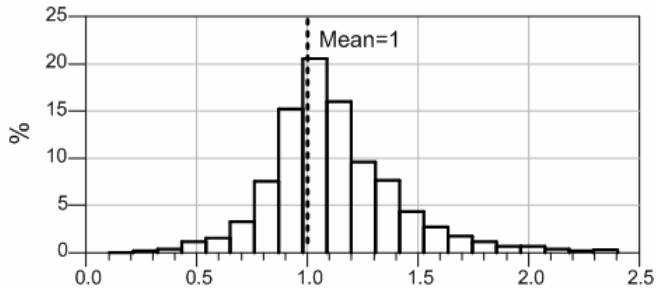



Figure 6.3 Histogram of the envelope voltage.

## 6.2 Co-verification Results

Designs of the Class-E with and without compensation have been simulated, respectively, in the EER co-simulation platform. The simulated results of received constellation have been shown in Figure 6.4. For the PA without compensation, the received constellation shown in Figure 6.4(a) reveals that the PA distortion causes the received symbol to move closer to an additional constellation point than the one transmitted and therefore the EVM is -17dB, -19 dB for system specification. For the PA with compensation, the received constellation shown in Figure 6.4(b) is closer to the transmitted constellation point and therefore the EVM is -19.2 dB. Furthermore, for the signal source with 64-QAM modulation scheme, the PA with compensation can also improve the system EVM from -21 dB to -25.1 dB. All of results have been summarized on Table 6.1. It shows that the proposed methodology can effectively compensate the AM-AM and AM-PM distortion of the Class E power amplifiers.

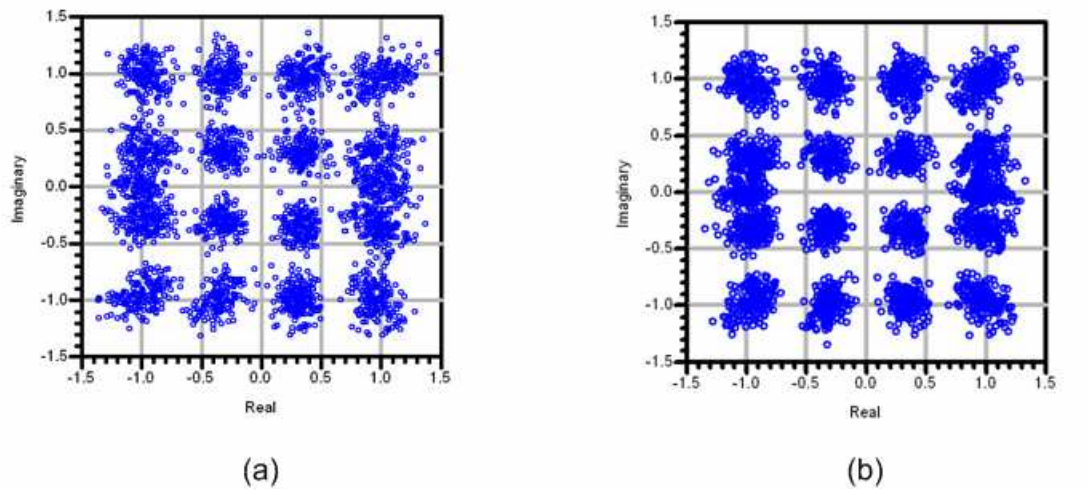



Figure 6.4 received constellations (a) PA without compensation, and (b) PA with compensation.

Table 6.1 Performance summary.

| | AM-AM | AM-PM | Modulation Scheme | |
|---|---|---|---|---|
| | | | 16-QAM | 64-QAM |
| Without compensation | 1.4 V/V (0.5V – 1.8V) | 15° or 17°/V (0.5V – 1.8V) | -17 dB | -21 dB |
| With compensation | 1.2 V/V (0.5V – 1.8V) | 2° or 5°/V (0.5V – 1.8V) | -19.2 dB | -25.1 dB |

## 6.3 Summary

The influence of the AM-AM and AM-PM characteristic on system performance has been discussed in this chapter. A system platform of EER with OFDM-based signal is constructed to demonstrate the PA distortion effect on EVM performance. When the PA distortion is compensated, the system EVM of an EER with the OFDM-based signal has been improved from -17 dB to -19.2 dB for 16-QAM modulation scheme, from -21 dB to -25.1 dB for 64-QAM modulation scheme.

# Chapter 7

# Efficiency Enhancement with Suspended Inductor

The internal inductors have the advantages of low cost and saving area for manufacturing. However, the low quality factor of internal inductors results in large resistive losses so that the PA efficiency is degraded. In the chapter, we presented a developed CMOS MEMS process and multi-metal layer suspended inductors to improve the quality factor of inductors for increasing the PA efficiency. In Section 7.1, the efficiency analysis of power amplifiers has been presented, in which the impact of low quality factor of inductors on efficiency is introduced. Section 7.2 describes the flow of CMOS MEMS process and multi-metal layer suspended inductors. The simulation performance of the Class E power amplifier with multi-metal layer suspended inductors has been reported in Section 7.3.

## 7.1 Efficiency Analysis

According to the well-known Class-E conditions as stated by Sokal [53], inductors used in the amplifiers are assumed ideal to have an infinite quality factor (Q) so that the efficiency of 100% is achieved. However, a large inductance and an inductor with high quality factor are difficult to achieve in silicon substrate. Moreover, due to the low Q-value of internal inductors, the PA has more power dissipations so that has degradations on efficiency.

For considering inductors parasitic losses of the PA shown in Figure 2.3, we will refer to the equivalent PA circuit reported in Figure 7.1, where parasitic elements of inductors are explicit and the PA's on resistance is taken into account. When the device is on, power is

dissipated through the conductive channel. A simplified expression for the power loss due to the finite device on resistance $R_{on}$, normalized to the output power ($P_{LOSS}/P_{OUT}$), can be written as Equation (7.1) [66]-[67].

$$\left.\frac{P_{LOSS}}{P_{OUT}}\right|_{R_{on}} = 1.365\frac{R_{on}}{R_L} \tag{7.1}$$

We assume all the inductors having the same Q-value, i.e., the parasitic series resistance is $R_x = \omega_o L_x/Q$ for the two inductors $L_{ck}$, $L_t$. Considering resistors $R_t$-$R_L$ realize a voltage divider, the power loss due to $R_t$ normalized to the output power is given by Equation (7.2).

$$\left.\frac{P_{LOSS}}{P_{OUT}}\right|_{R_t} = \frac{R_t}{R_L} = \frac{\omega_o L_t}{QR_L} \tag{7.2}$$

For the given $\omega_o$, $L_t$ and $R_L$, $(P_{LOSS}/P_{OUT})|R_t$ can be minimized by increasing Q-value.

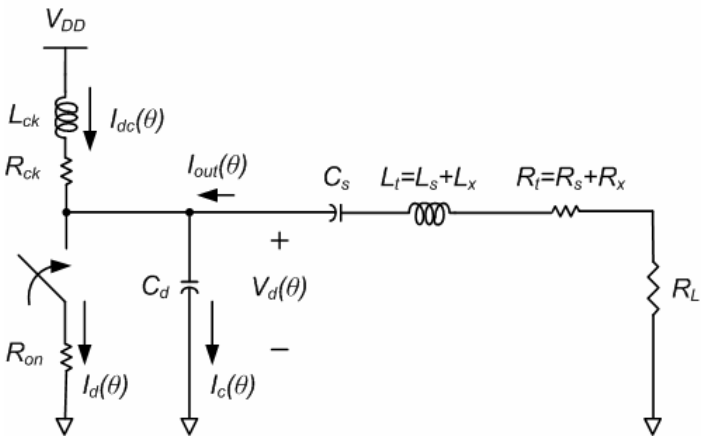



Figure 7.1 Schematic of basic Class-E amplifier with equivalent series resistances.

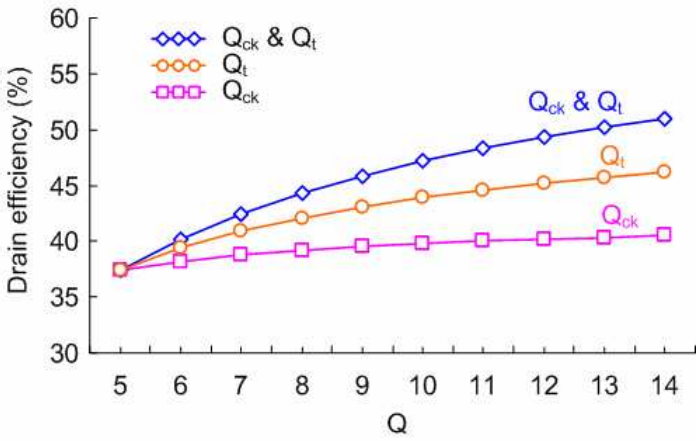



Figure 7.2 Drain efficiency versus Q-value of inductors $Q_{ck}$ and $Q_t$.

If a dc current is assumed through $L_{ck}$, the calculation of its power loss contribution is straightforward. The normalized power loss is then given by

$$\left.\frac{P_{LOSS}}{P_{OUT}}\right|_{R_{ck}} = \frac{P_{DC}-P_{OUT}}{p_{OUT}} = \frac{0.577\cdot\omega_o L_{CK}}{QR_L} \tag{7.3}$$

where $P_{DC}$ is the power supplied. It also shows that $(P_{LOSS}/P_{OUT})|R_{ck}$ can be minimized by increasing Q-value.

According to Equations (7.1)-(7.3), the calculated efficiency of power amplifiers can be expressed as $\eta=1/(1+\sum_i (P_{LOSS}/P_{OUT})|_i)$. To validate the above analysis, the parameter values on Table (2.2) are introduced: $R_{on}$= 5 Ω, $L_t$= 2.6 nH and $L_{ck}$= 2 nH. The result of calculated efficiency versus the Q-value of $L_{ck}$ and $L_t$ has been reported in Figure 7.2. In Figure 7.2, the curves marked as $Q_{ck}$ and $Q_t$ denote the variable Q-value of $L_{ck}$ and $L_t$, respectively, and the curve marked as $Q_{ck}$ and $Q_t$ means that the Q-value of $L_{ck}$ and $L_t$ both are variable. According to this analysis, the PA efficiency can be improved by increasing the Q-value of inductors. Moreover, the increased Q-value of $L_t$ has significant contributions to the PA efficiency. Therefore, the inductors with higher Q-value could be expected for improving the PA efficiency.

# 7.2 Suspended Inductor Design

## 7.2.1 CMOS MEMS Process

The fabrication for the suspended inductor is similar to any IC fabrication process. In this process, etching technology for releasing the oxide and silicon substrate was performed. The process flow has been shown in Figure 7.3. The first step is to deposit the metal layer (Hardmask), which is used to protect the top metal layer of the microstructure during the etching step. The second step is to remove the oxide layer by the anisotropic etching. After removing the oxide layer, silicon substrate is released by an isotropic etching process. The final step is to remove the Hardmask layer after the previous processing steps have been completed. After fabrication, the inductors will be suspended by 40 μm from the top metal layer to silicon substrate.

Figure 7.4 shows the photograph of fabricated suspended inductor. It shows the developed CMOS MEMS is allowed to fabricate CMOS-compatible suspended inductors.

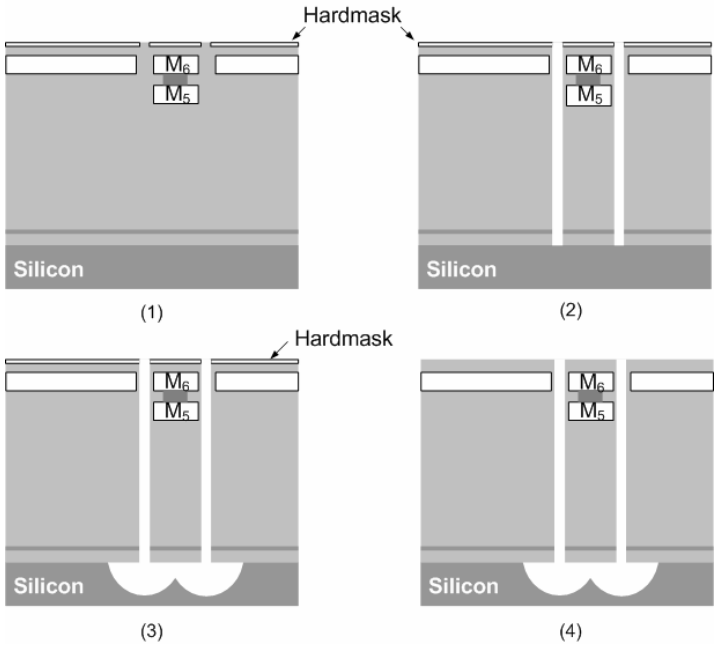



Figure 7.3 CMOS MEMS fabrication process.

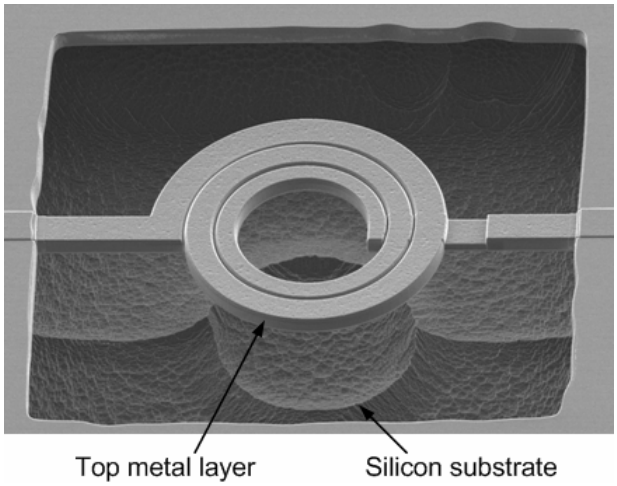



Figure 7.4 Fabricated suspended inductor photograph.

### 7.2.2 HFSS Simulation Model

The micrograph of a single-metal layer suspended inductor and its cross section view have been shown in Figure 7.5. This inductor has 7 turns of spiral coil on air suspension and 2 μm thick of the top metal layer. For perspective of circuit design, an equivalent model of suspended inductor is required. HFSS (high frequency structural simulator) is a commercial finite element method (FEM) solver for electromagnetic structures. The FEM is a numerical technique for finding approximate solutions of partial differential equations (PDE). HFSS uses 3-D FEM and 3-D boundary conditions. The solid models have been obtained from the 2-D layout. The measured and simulated results of this inductor are plotted in Figure 7.6. The comparison result shows that HFSS has good prediction on the characteristics of proposed suspended inductors. Therefore, the equivalent model of suspended inductors can be extracted from HFSS for requirements of circuit design.

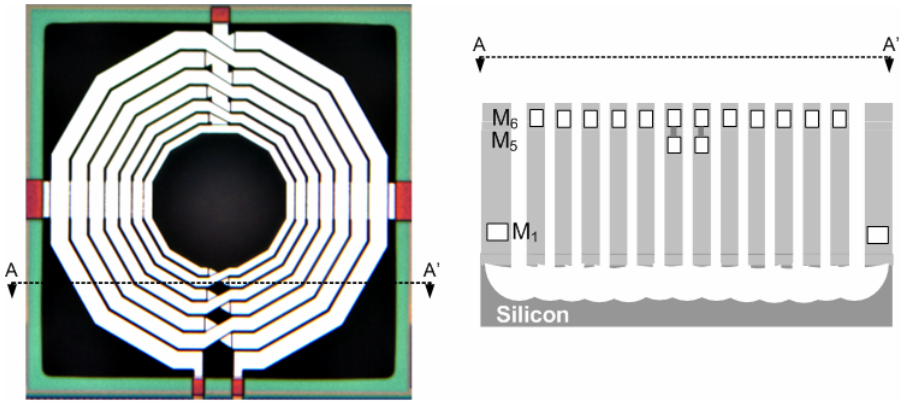



Figure 7.5 Micrograph and cross section view of the suspended inductor.

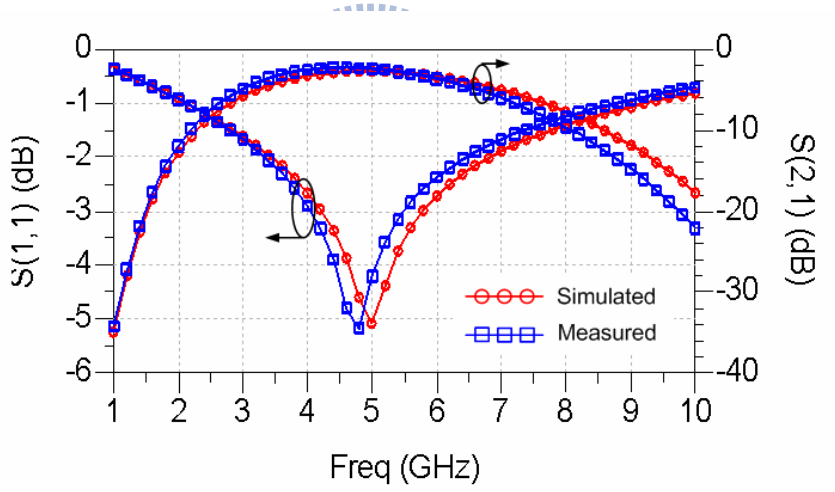



Figure 7.6 Simulated and Measured results of the suspended inductor.

## 7.2.3 Multi-Metal Layer Suspended Inductor

The suspended inductors can have an improved Q-value due to the reduction of power losses from the silicon substrate. However, it also moves the resonant frequency of Q-value to higher frequency band. In this literature, the stacked-metal layer topology of suspended inductors has been proposed. When stacking two or more meal layers, the thickened metal can

not only reduce the resistive loss but also shift the resonant frequency down to lower frequency band to desired operating frequency. A prototype of suspended inductor having two-metal layer ($M_5/M_6$) and the three-metal layer ($M_4/M_5/M_6$) are performed and the cross-section view is shown in Figure 7.7. The metal layers for signal transmission are stacked to optimize the Q-value and simulated results by HFSS have been plotted in Figure 7.8. The result shows that the Q-value is increased and the frequency of maximum Q-value is also shifted to the higher frequency band by the suspended structure. On the other hand, the frequency of maximum Q-value can be shifted to the lower frequency band by the stacked-metal structure. Therefore, for lower desired operating frequency, the stacked-metal layer suspended inductor effectively enhances the Q-value for efficiency improvement. In Figure 7.8, the slope of curve $M_{654}$ is nearly the same as the slope of other curves. However, the Q-value of curve $M_{654}$ at the dc frequency is different from others due to the different shunt capacitance of inductors and the boundary definition of simulator at the dc frequency.

For considering the impact of inductors on efficiency, the inductors having different metal thickness are performed. The simulated Q-value at 2.6 GHz by HFSS is reported in Figure 7.9. The inductor $M_6$(Si) with 20-μm metal width has a typical Q-value of 9.5 in standard CMOS process. For single-metal layer suspended inductor $M_6$, the Q-value is 9.7. When the suspended inductor stacked the three top-metal layers, the Q-value of 12 is achieved. The inductors $L_{ck}$ with more stacked-metal layer have a degraded Q-value due to the skin effect from the exceeding metal thickness.

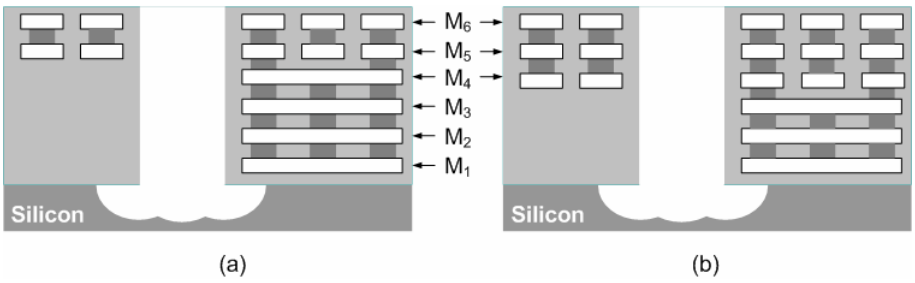
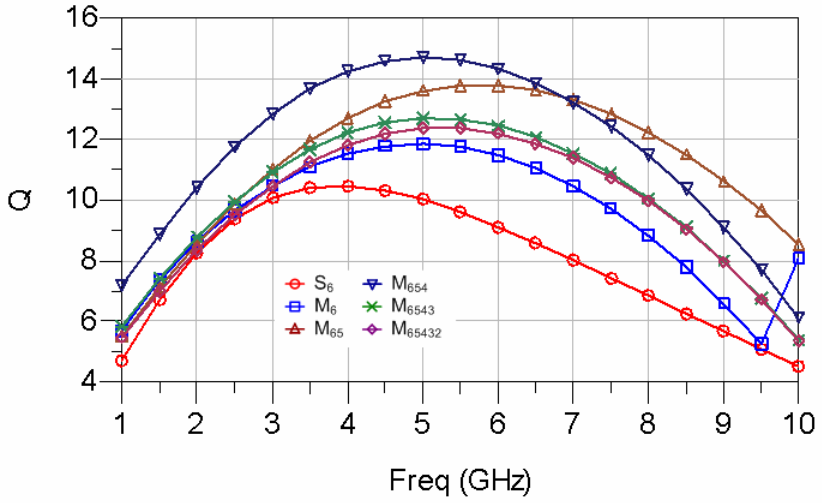



Figure 7.7 Cross-section view of suspended inductor
(a) two-metal layer, (b) three-metal layer.




| Turn | Width | Spacing | Diameter |
|---|---|---|---|
| 2.5 | 20-μm | 2-μm | 166-μm |

Figure 7.8 Q-value of CMOS inductor and suspended inductor.

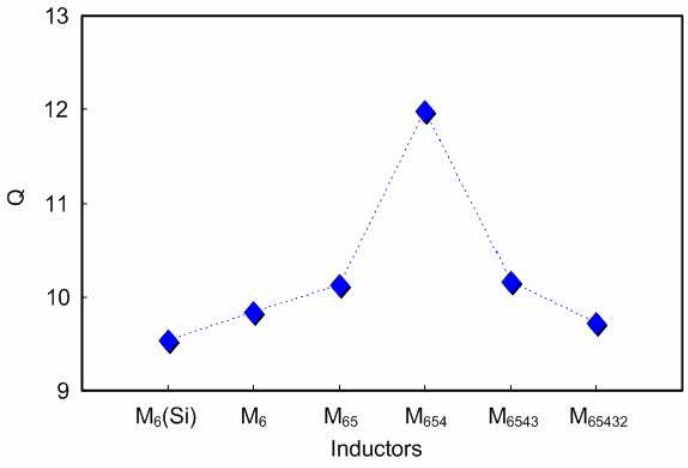



Figure 7.9 The Q-value of inductors with different metal thickness.

# 7.3 Simulation Results

The dc-feed inductor and the inductor of output matching network in Class E power amplifier proposed in Chapter 3 is implemented with multi-metal layer suspended inductors as shown in Figure 7.10. The simulation model of suspended inductors has been created by HFSS. The amplifier intends to demonstrate that the PA efficiency could effectively be enhanced with auto-biasing technique and suspended inductors. The comparison of simulation results will be reported as followings.

The dc current and output power of amplifiers are plotted in Figure 7.11. The output power has no change when proposed compensation technique and suspended inductors have been performed. The dc current still has no change if only suspended inductors are performed. Drain efficiency of the amplifiers versus the supply voltage has been plotted in Figure 7.12. It is apparently that the PA with the three-metal ($M_{654}$) layer suspended inductors has the maximum efficiency performance. When the auto-biasing cascode Class-E amplifier with the three-metal layer ($M_{654}$) suspended inductors, the efficiency can have the maximum improvement of the efficiency of 17% at the supply of 0.65 V. The result has demonstrated that the Class-E power amplifier with proposed compensation technique and suspended inductors effectively improves the power efficiency.

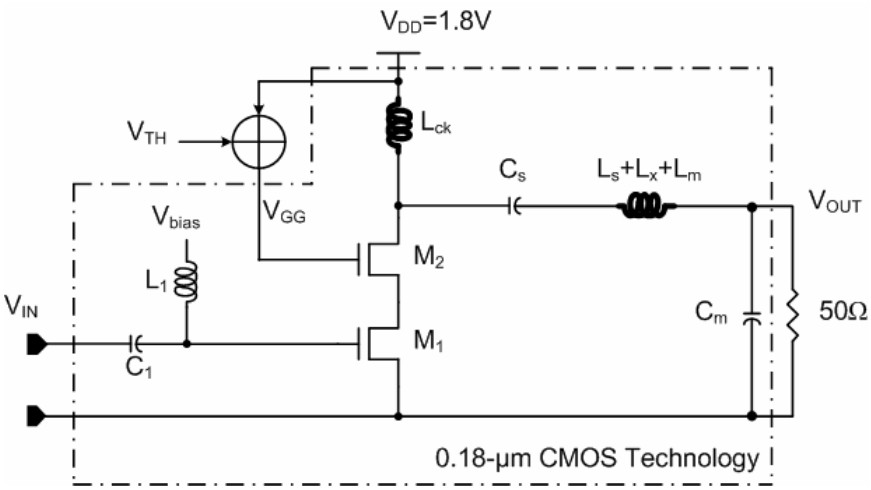



Figure 7.10 Cascode Class-E PA with suspended inductors.

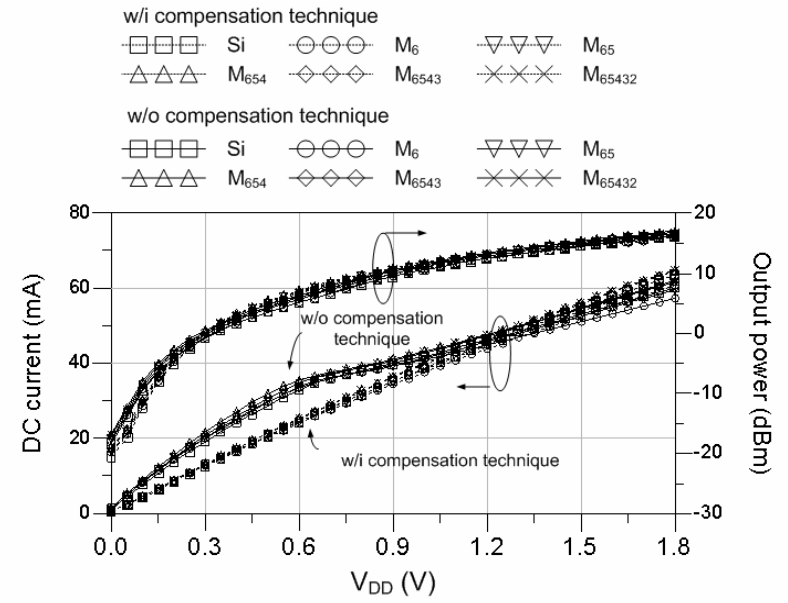



Figure 7.11 Comparison results of dc current and output power versus supply voltage.

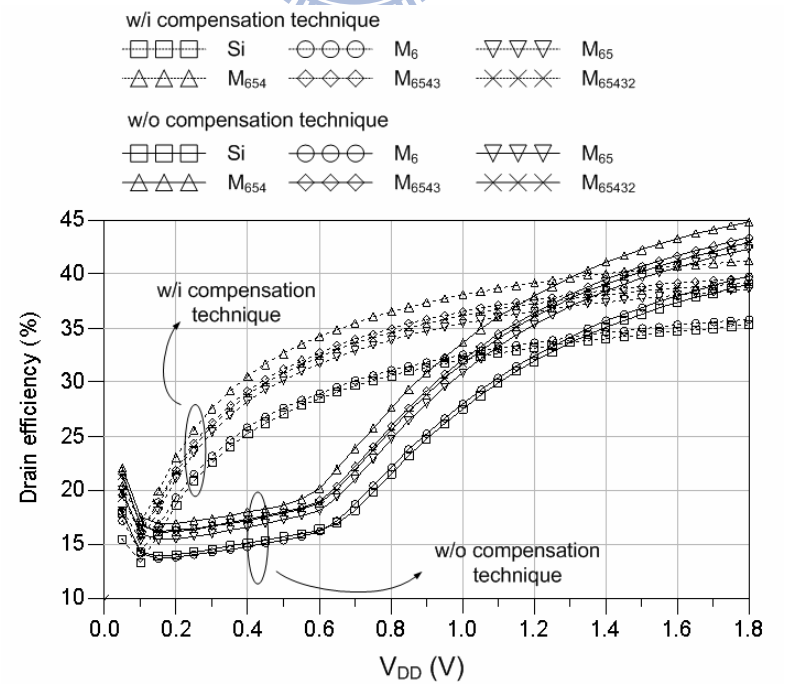



Figure 7.12 Comparison results of drain efficiency versus supply voltage.

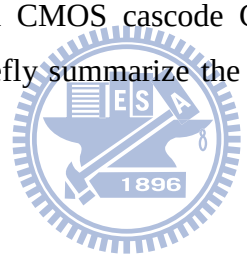
## 7.4 Summary

The analysis for efficiency improvement of the CMOS Class-E PA with suspended inductors has been presented. A process which can fabricate the suspended inductors is also introduced in this work. Furthermore, for increasing Q-value, the stacked-metal layer suspended inductors have been presented. Prototypes of inductors have been designed to demonstrate that the stacked-metal layer inductors in CMOS MEMS process can reduce the substrate loss and resistive loss for improving the Q-value of inductors. It has shown that the PA efficiency can be improved by the stacked-metal layer MEMS inductors and also provides a design methodology for improving the PA efficiency by optimizing the Q-value of fully integrated inductors. Finally, with proposed compensation technique and suspended inductors, the Class E power amplifier can have the maximum efficiency enhancement.

# Chapter 8

# Conclusions

The dissertation has presented the design of CMOS cascode Class E power amplifier with AM-AM and AM-PM compensation. The techniques presented in earlier chapters have enabled the implementation of a CMOS cascode Class E power amplifier in a 0.18 μm technology. To conclude, we briefly summarize the key contributions presented in precious chapters.



## 8.1 Summary

The design methodology of conventional common source Class E power amplifiers has been described in Chapter 2. For practical considerations of integration and reliability, the design requirements of cascode Class E power amplifier with small dc-feed inductance have been analyzed.

Chapter 3 has presented a conventional cascode Class E power amplifier in CMOS 0.18 μm technology. As cascode Class E power amplifiers in supply modulation, the reason for producing the envelope deviation and the phase error at the RF output signal is described. More detailed analyses including the current/voltage curves and impedance variations of transistors are also introduced in this chapter.

A design technique, which modulates the gate bias voltage of the cascode transistor to operate the transistor as a resistance, to compensate the AM-AM and AM-PM distortion of the cascode Class E amplifier has been presented in Chapter 4. The efficiency performance of the amplifier is also improved as the distortion has been compensated.

The design of cascode Class E power amplifier implemented in CMOS 0.18 μm technology has been presented in Chapter 5. The experimental results demonstrate the phase shift of the output signal from 30˚ to 6˚ when $V_{DD}$ is 0.4 V to 1.8 V. The design of cascode Class E power amplifier with self-biased control circuit implemented in CMOS 0.18 μm technology demonstrates the Class E power amplifier with compensated AM-AM and AM-PM distortion. The experimental result shows the phase error reduced down to 5° as $V_{DD}$ is swept from 0.7 V to 1.8 V. The output power is 12 dBm from a 1.8 V supply. Drain efficiency and PAE is18.7% and 16.6%, respectively.

For the RF/baseband co-verification, Chapter 6 presents the co-verification platform. The case study of a 2.6 GHz EER transmitter with OFDM-based signal source has been presented to demonstrate the feasibility of the AM-AM and AM-PM compensation.

A developed CMOS MEMS process and stacked metal layer suspended inductors have been presented in Chapter 7 to demonstrate the improved PA efficiency due to the increased quality factor of internal inductors. The amplifier has the maximum efficiency improvement of 17%.

## 8.2 Recommendations for Future Work

The determination of transistor size is constrained by the current density of internal inductors. The optimization of MOS size and inductor Q-value could help to enhance the circuit performance such as output power and efficiency. In addition, it should be feasible to improve the efficiency at high power level as the amplifier was compensated. Moreover, the characteristic of AM-AM and AM-PM curves could be optimized with the elimination of process variations.

# Appendix A

# Analysis of Ideal Class E PA with Finite DC-Feed Inductor

One of the first attempts was made to study finite dc-feed inductor in [60]. Some other related studies are included in [68]-[69]. All these researches have recommended that procedure of obtaining final circuit component values is either long, complex and iterative, and is difficult to provide a direct insight into the circuit design, or is too simplistic and not exactly. Practically, the design of the Class E PA with finite dc-feed inductor is a transcendent problem from the mathematical point of view. Therefore, the designer needs to iteratively figure out the systm of equations for a certain set of input parameters to gain the final circuit component values. If any of the input parameters is changed, the calculation must be repeated from the beginning. Thus, it is a tedious and extremely impractical procedure. In [70] an approach has been proposed to alleviate the problem. The system of transcendent equations is numerically solved for a certain number of discrete points of an input parameter, and the obtained results are interpolated by the Lagrange polynomial. The polynomial interpolation provides adequate accuracy and can be used for any value of the input parameter on that segment, if it performs with enough density of points on the segment of interest. In other words, it obtains clear and directly usable design equations for the Class E power amplifier.

The well-known design equations have been many times derived in the literature, and they are given by

$$R = 0.5768\frac{V_{DD}^2}{P_{out}} \tag{A.1}$$

$$B = 0.1836/R \tag{A.2}$$

$$X = 1.152R \tag{A.3}$$

where $V_{DD}$ and $P_{out}$ are the supply voltage and the desired output power, respectively, and the load resistance R, the shunt susceptance B and the excessive reactance X. The equations are based on the $L_{ck}$ is an RF choke with large inductance. But in case of the Class E amplifier with finite dc-feed inductor, the equations don't hold anymore. At the beginning of the design procedure, the designer could choose a value of inductance for the finite dc-feed inductor. Therefore, the reactance of the inductor is known and can be given by

$$X_{dc} = \omega L_{ck} \tag{A.4}$$

On the other hand, an ideal Class E amplifier provides a 100% dc-to-RF efficiency. Therefore, the dc resistance that the circuit presents to the supply source is also known from the PA specifications, and is simply given as

$$R_{dc} = \frac{V_{DD}^2}{P_{out}} \tag{A.5}$$

Depending on the value of $X_{dc}/R_{dc}$, the circuit parameters R, B and X will change their value from the given equations for the RF choke based Class E power amplifier. The three parameters have calculated by numerically solving the transcendent circuit equations for a number of different values of $X_{dc}/R_{dc}$. The results of these calculations are plotted in Figure A.1. In Figure A.1, the variations of the elements R, B and X is plotted as a function of $X_{dc}/R_{dc}$. However, the plots are not continuous functions and they are discrete character.

In order to obtain explicit design equations for the Class E PA component values, the Lagrange polynomial interpolation of the numerically obtained results is used. Finally, the

new equations for Class E power amplifier with finite dc-feed inductor are presented in the following equations.

If $1 < X_{dc}/R_{dc} \ (= z) < 5$,

$$R = \frac{V_{DD}^2}{P_{out}}(1.979 - 0.7783z + 0.1754z^2 - 0.01397z^3) \tag{A.6}$$

$$B = \frac{1}{R}(1.229 - 0.7171z + 0.1881z^2 - 0.01672z^3) \tag{A.7}$$

$$X = R(-1.202 + 1.591z - 0.4279z^2 + 0.03894z^3) \tag{A.8}$$

If $5 < X_{dc}/R_{dc} \ (= z) < 20$,

$$R = \frac{V_{DD}^2}{P_{out}}(0.9034 - 0.04805z + 0.002812z^2 - 5.707 \cdot 10^{-5} z^3) \tag{A.9}$$

$$B = \frac{1}{R}(0.3467 - 0.02429z + 0.001426z^2 - 2.893 \cdot 10^{-5} z^3) \tag{A.10}$$

$$X = R(0.6784 + 0.006641z - 0.003794z^2 + 7.587 \cdot 10^{-5} z^3) \tag{A.11}$$

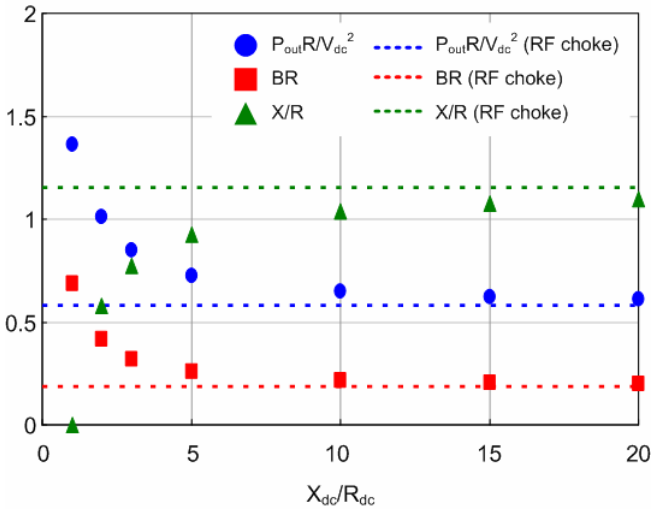



Figure A.1 Effect of the finite dc-feed inductance on the Class E circuit elements.

Design equations (A.6)-(A.11) are explicit, relatively simple and can be used for any value of $z=X_{dc}/R_{dc}$ within the corresponding segment. But outside these segments, they are not valid.

The utilization of a finite dc-feed inductor has several major benefits. First, it results in a higher load resistance in comparison to the case of RF choke. This effect makes the design of low-loss matching networks easier, since the designer typically needs to transform a standard 50 Ohm termination to the load resistance of several Ohms. Furthermore, the excessive inductance X is also lower, and the shunt susceptance B is increased. This increase of the shunt susceptance is particularly useful, as it extends the maximum frequency limitation of the device imposed by its output capacitance.

# Appendix B

# Common Source Class E PA with Stacked Resistance

In this work, we present that when the cascode transistor is operated as a resistance alike, the AM-AM and AM-PM distortion is improved. Therefore, of the Class E amplifier the cascode transistor replaced with a resistance has been shown in Figure B.1. With the same operating conditions the simulation results of the common source Class E with stacked resistance are obtained. The simulated result compared with that of the cascode Class E with compensation is shown in Figure B.2. It demonstrates that both of two amplifiers have good agreement on the AM-AM and AM-PM characteristic. However, the resistance captures more voltage headrooms so that the output power of the amplifier is degraded as shown in Figure B.3. There has a 3-dB reduction to the output power and the power gain of the amplifier. Even having smaller current consumptions as shown in Figure B.4, the efficiency is less than that of the cascode Class E owing to the severely degraded output power.

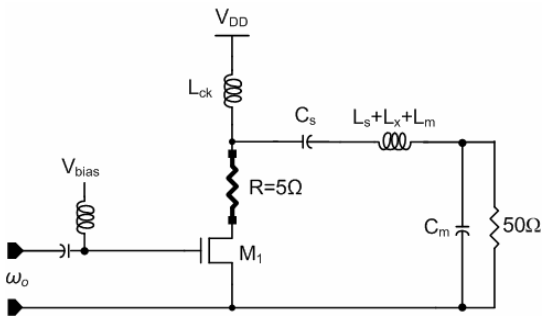



Figure B.1 Common source Class E with stacked resistance.

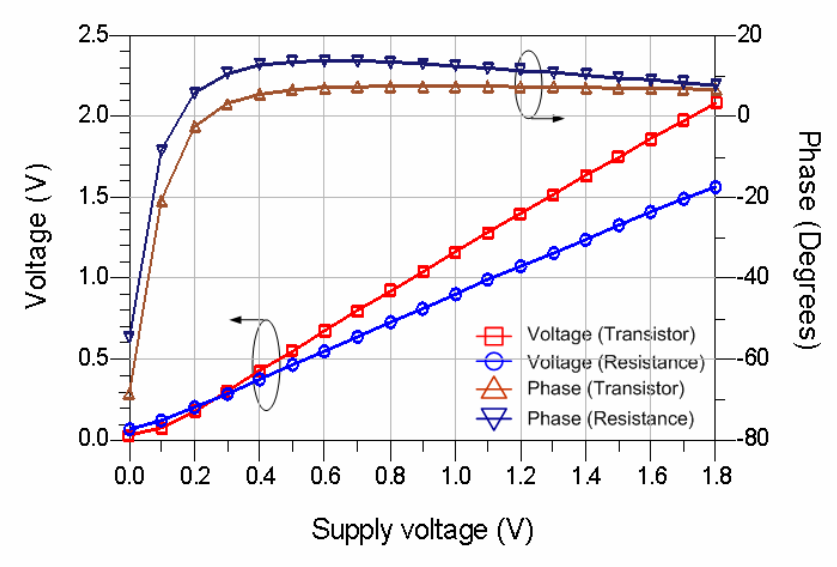



Figure B.2 Comparison of AM-AM and AM-PM distortion.

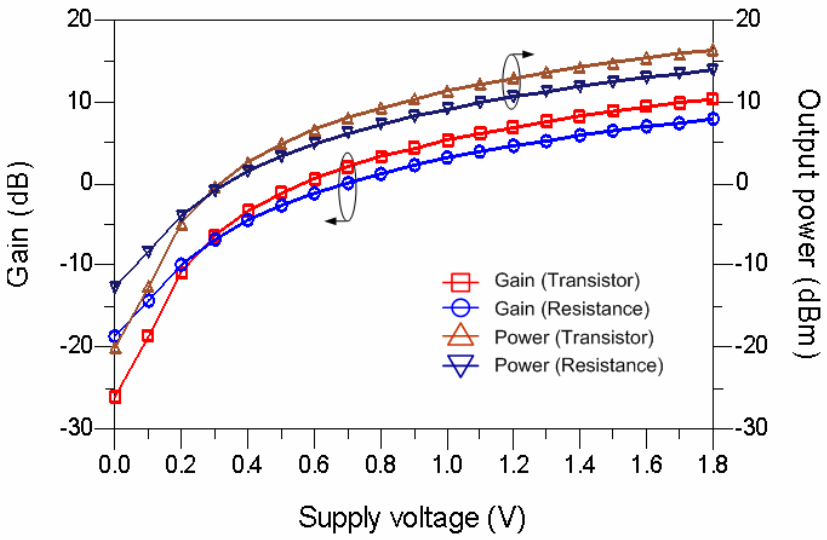



Figure B.3 Comparison of power gain and output power.

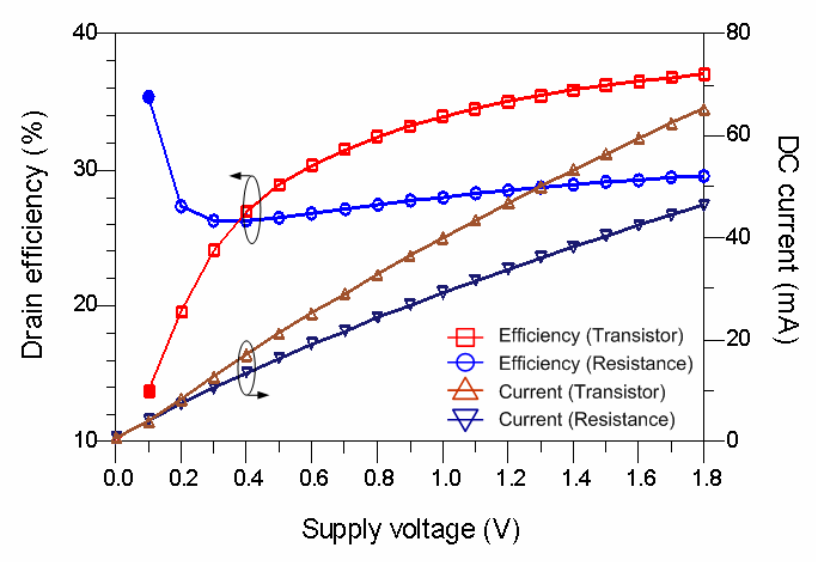



Figure B.4 Comparison of drain efficiency and dc current.

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# 著作目錄 - Publication List

## 1. *Journal Paper*

[1] Wen-An Tsou, Wen-Shen Wuen, Tzu-Yi Yang and Kuei-Ann Wen, "Analysis and Compensation of the AM-AM and AM-PM Distortion for CMOS Cascode Class-E Power Amplifier," *International Journal of Microwave Science and Technology*, March 2010.

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## 2. *Conference Paper*

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