國立交通大學

電子工程學系 電子研究所

博 士 論 文

深次微米互補式金氧半製程之寬頻射頻接收發射器設計

Design of a Wideband RF Transceiver in a Deep Sub-micro CMOS Process

研 究 生：施鴻源

指導教授：郭建男 教授

中 華 民 國 九 十 九 年 三 月

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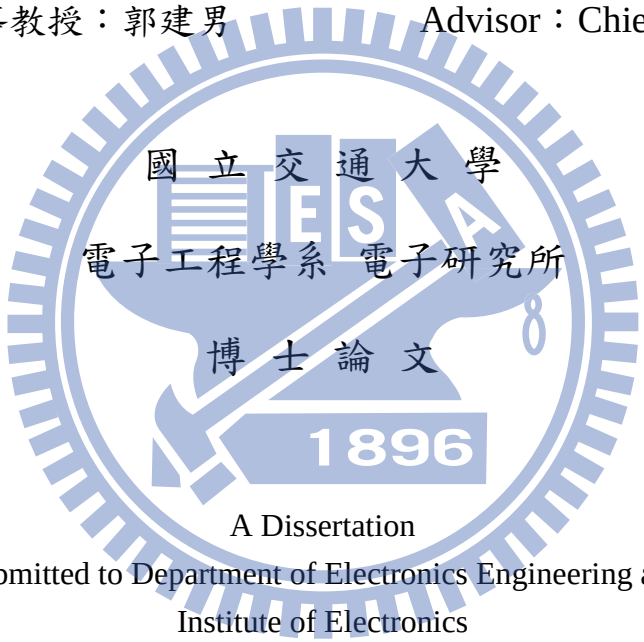

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深次微米互補式金氧半製程之寬頻射頻接收發射器設計

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國立交通大學電子工程學系電子研究所博士班

摘　　要

本論文描述一以 1.2 V 0.13 μm CMOS 製程實現，應用於超寬頻系統之寬頻射頻接收發射器設計。接收機設計在 3~5 GHz 的頻段。整個接收機是由一 3~5 GHz 的寬頻低雜訊放大器、三階槽口濾波器、電流式的降頻混頻器與一頻寬為 250 MHz 之類比基頻電路所組成。在類比基頻的電路中，可變增益放大器與濾波器利用電流式放大器的形式設計達到寬頻、高增益動態範圍、低雜訊與高線性度之特點。此外一電流式 Sallen-Key 低通濾波器被設計用來有效地濾除通道外的干擾訊號。一個六階的 Chebyshev 低通濾波器被設計用來提供通道選擇。一數位輔助的直流偏移校正電路用來降低整個類比基頻電路的二階諧波失真。整個接收器電路在 1.2 V 的操作電壓下消耗 100 mW。

在發射器的設計上，我們涵蓋 3~8 GHz 的頻率範圍。整個發射器電路整合了一類比基頻電路、調變器電路、可變增益放大器、差動轉單端放大器與功率放大器，並整合了發射訊號強度指標電路。調變器電路並包括一直流偏移消除電路來增進其載波洩漏的抑制能力。整個發射器提供 14 dB 的發射功率可調範圍，並具有-5 dBm 的最大發射功率與+1.5 dBm 的輸出 P1dB。藉由直流偏移消除電路可使得載波洩漏抑制達到 40 dB。其高線性度與調變精準度使得在 480 Mb/s 下 EVM 可達-28 dB，可滿足 WiMedia Mode 1 的規格要求。整個發射器電路在 1.2 V 的操作電壓下消耗 66 mW。

Design of a Wideband RF Transceiver in a Deep Sub-micro CMOS Process

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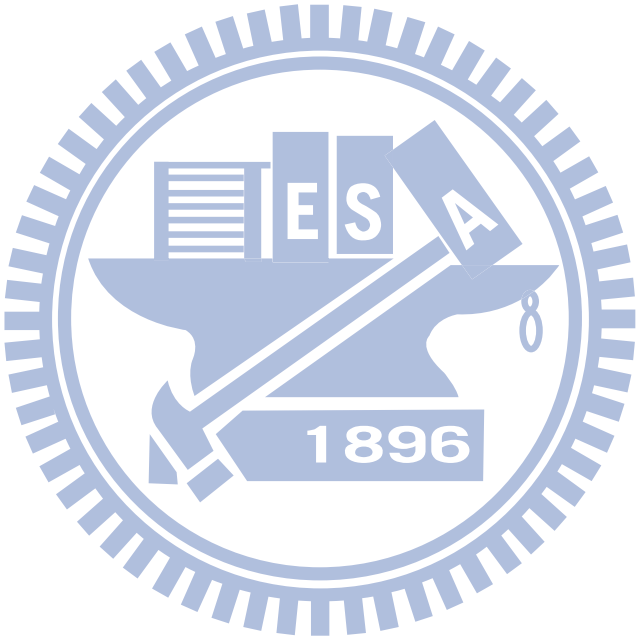
ABSTRACT

This dissertation presents a wideband RF transceiver for ultra-wideband (UWB) applications implemented in a 1.2 V 0.13 μm CMOS process. The receiver design focuses on mode 1 of multi-band (MB) orthogonal frequency division multiplexing (OFDM) UWB (3~5 GHz) which is defined as essential band by WiMedia Alliance. The receiver chain is composed by a broadband 3~5GHz ESD-protected low-noise amplifier, a 3^{th}-order notch filter, a current-mode down conversion mixer and a 250MHz wideband analog baseband. In the analog baseband, PGAs and filters are carried out by current-mode amplifiers to achieve wide bandwidth and wide dynamic range of gain, as well as low noise and high linearity. Besides, a current-mode Sallen-Key low-pass filter is adopted for effective rejection of out-of-band interferers. A 6^{th}-order Chebyshev low-pass filter realized in G_m-C topology is designed in the baseband chain for channel selection. Digitally-assisted DC-offset calibration improves second-order distortion of the entire chain. The entire receiver consumes 100 mW under a supply voltage of 1.2 V.

In the design of transmitter, we attempt to cover both mode 1 and Band Group 3 of MB-OFDM UWB (3~8 GHz). The 3~8 GHz transmitter

chain integrates an analog baseband, an in/quadrature-phase (IQ) modulator, a variable gain amplifier (VGA), a differential-to-single amplifier, a power amplifier, as well as a transmitted signal strength indicator (TSSI). The IQ modulator incorporates DC-offset cancellation circuits to improve carrier leakage suppression. This transmitter provides linear-in-dB output power tuning of 14 dB to fulfill the requirement of WiMedia UWB. Measured maximum output power and OP1dB are -5 dBm and +1.5 dBm, respectively. Measured carrier leakage suppression is over 40 dB after calibration. The high linearity and accurate IQ modulation lead to an error vector magnitude (EVM) of -28 dB under the data rate of 480 Mb/s in WiMedia Mode 1. The entire transmitter consumes 66 mW under a supply voltage of 1.2 V.

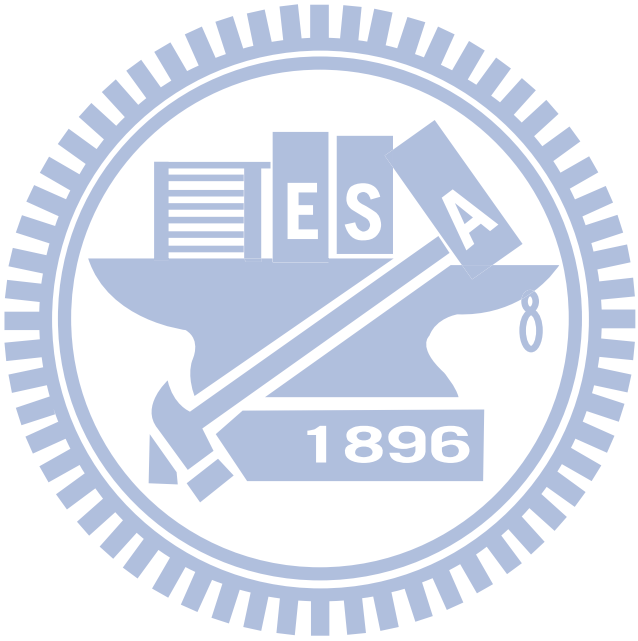


誌　　謝

感謝我的父母親，施國樑先生與吳梅蘭女士對我從小的付出與教導。父親常教導我做人處世應有的態度與方法，在我工作與學業遇到瓶頸與挫折時總是給我許多鼓勵讓我重新站起來面對挑戰。母親對於我生活上事物總是細心關懷，並無條件地付出與支持我。另外，我要感謝我的妻子陳雅慧，有她在背後的支持我才能順利完成學業。我的女兒幸昀與幸玫，妳們是我的最愛。最後，感謝我的博士班與碩士班指導老師郭建男教授與彭松村教授在研究上給我的指導與幫助。

目　　錄

Figures and Tables



Chapter 1

Introduction

Enlarging signal bandwidth is the most direct way to increase the data rate in wireless transmission. For the purpose, the spectrum from 3.1 GHz to 10.6 GHz was approved by FCC for commercial applications of Ultra-Wideband (UWB) systems in 2002. Proposed by the WiMedia alliance as Multi-Band (MB) OFDM UWB, the system realizes a high date rate of 480 Mbits/s in short-range communication as a wireless technique to replace cables. The spectrum is partitioned into five band groups. Each band group consists of three bands with a bandwidth of 500 MHz, which leads to a large baseband bandwidth of 250 MHz in direct-conversion transceiver [1-2]. Large signal bandwidth, however, leads to an interference problem. It occurs that signals of other narrowband communication systems, such as WiMax and WLAN, appear as interferers to an UWB RF transceiver, causing strict linearity requirement [3]. On the contrary, to avoid interfering the existing narrowband communication systems, the transmit power spectral density level is limited to -41.3dBm/MHz [4]. Low transmit power leads UWB to be suitable for wireless personal area network (WPAN) applications.

1.1 Area of focus

This dissertation focuses on design of a wideband RF transceiver for ultra-wideband

applications in a deep sub-micro CMOS process. The receiver should carry out a wide RF bandwidth of 3~5GHz, a wide baseband bandwidth of 250MHz. The receiver is also needed to be low noise figure and high linearity for sustaining sensitivity of -80.8dBm as co-existence with WLAN 802.11a systems. The transmitter should carry out a wide RF bandwidth of 3~5GHz, a wide baseband bandwidth of 250MHz and an output power of -10dBm. Power consumption of the transmitter should be as low as possible for extending battery life.

1.2 Proposed wideband RF receiver

As shown in Figure 1-1, an UWB RF receiver is composed of a 3~5GHz broadband RF front-end and a 250MHz wideband analog baseband. The RF front-end is consisted by a low noise amplifier, a notch filter and a down-conversion mixer. The low noise amplifier is designed to boost the incoming RF signals. The notch filter is designed to suppress the strong out-of-band signals, WLAN 802.11a signals allocated in 5.2~5.4 GHz. Then, the received RF signals are down converted to the baseband signals by the down-conversion mixer.

Typically the RF front-end carries out a low gain level, as compared to that in a narrowband receiver, such that the analog baseband can sustain those interferers. Consequently the analog baseband shall provide sufficient gain with very low input-referred noise to meet noise and gain requirements of the entire receiver. It therefore includes programmable gain amplifiers (PGAs) and filters. PGAs provide sufficient dynamic range, while filters give channel selection. In general, it is preferred to arrange in the order of PGAs, filters and PGAs for the optimal performance regarding to noise and linearity consideration of the overall analog

baseband.

PGAs and filters are typically designed in voltage-mode operational-amplifier (OP Amp)-based circuits in narrowband communication systems [5]. Those voltage amplifiers have advantages of good gain accuracy, low process-voltage-temperature (PVT) variation, and low power consumption. But they have a very limited bandwidth at high closed-loop gains, typically up to several tens of megahertz. Furthermore, in advanced deep sub-micron processes, linearity performance is greatly affected by rapid decrease of the maximum voltage rating as devices are scaled down. Therefore, it is getting harder to design high performance voltage-mode circuits. On the other hand, current-mode amplifiers turn out more suitable for realizing the UWB analog baseband. Low impedance at current-mode circuit nodes easily leads to a wider operating bandwidth [6-7]. In addition, current-mode circuits feature high linearity owing to small voltage swings and lower supply voltage sensitivity than voltage-mode circuits. In 1968, a current conveyer was proposed as the first building block intended for current signal processing [8], then several proposals for a CMOS current-mode OP-Amp have been published [9-10]. In 1997, BJT-based current-mode variable gain amplifiers (VGAs) are successfully realized by a trans-linear loop with at least 250 MHz bandwidth, good blocking and inter-modulation (IM) performance [11]. Later a 240 MHz low-pass-filter for an UWB receiver has been successfully realized in the G_m-C topology [12].

Another critical issue to baseband circuit design is DC-offset, which might lead to second-order distortions arising from the third-order nonlinearity in a balanced baseband circuit [13]. The third-order inter-modulation between the input signal and the DC-offset generates the second-order distortions. The propagation of the amplified second-order distortion from stage to stage in the baseband chain not only degrades signal-to-noise ratio (SNR) but also saturates circuits. Calibration is required

to improve this DC-offset related second-order nonlinearity.

In this design, the analog baseband circuit is implemented by balanced current-mode amplifiers. Current-mode PGAs are combined with a 6^{th}-order G_m-C low-pass filter to obtain a high gain, a high dynamic range and low noise. A current-mode Sallen-Key low-pass filter (SK LPF) is placed at the first stage to attenuate out-of-band interferers and relax linearity requirement of the following PGAs. Calibration circuits are also implemented to calibrate the corner-frequency of the G_m-C low-pass filter. DC-offset in the balanced circuits is resolved by a proposed digitally-assisted calibration loop.

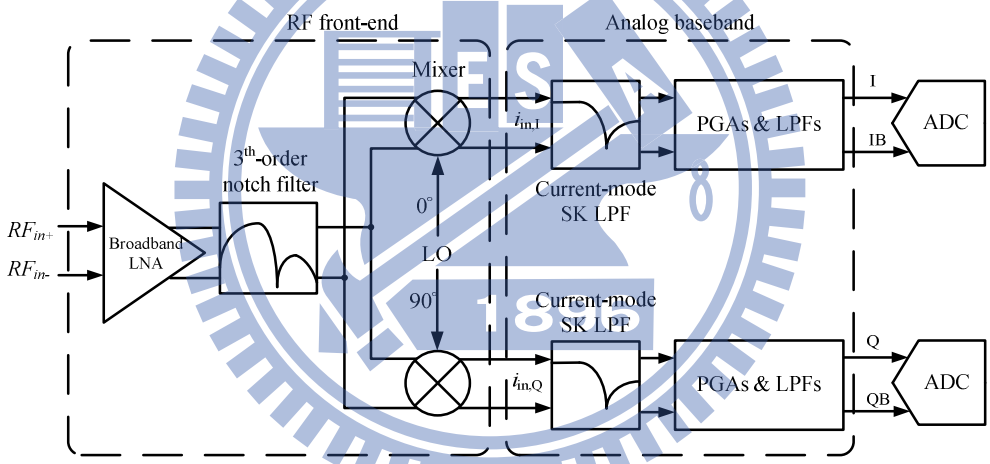


Figure 1-1: Architecture of the direct-conversion RF receiver for UWB.

1.3 Proposed wideband RF transmitter

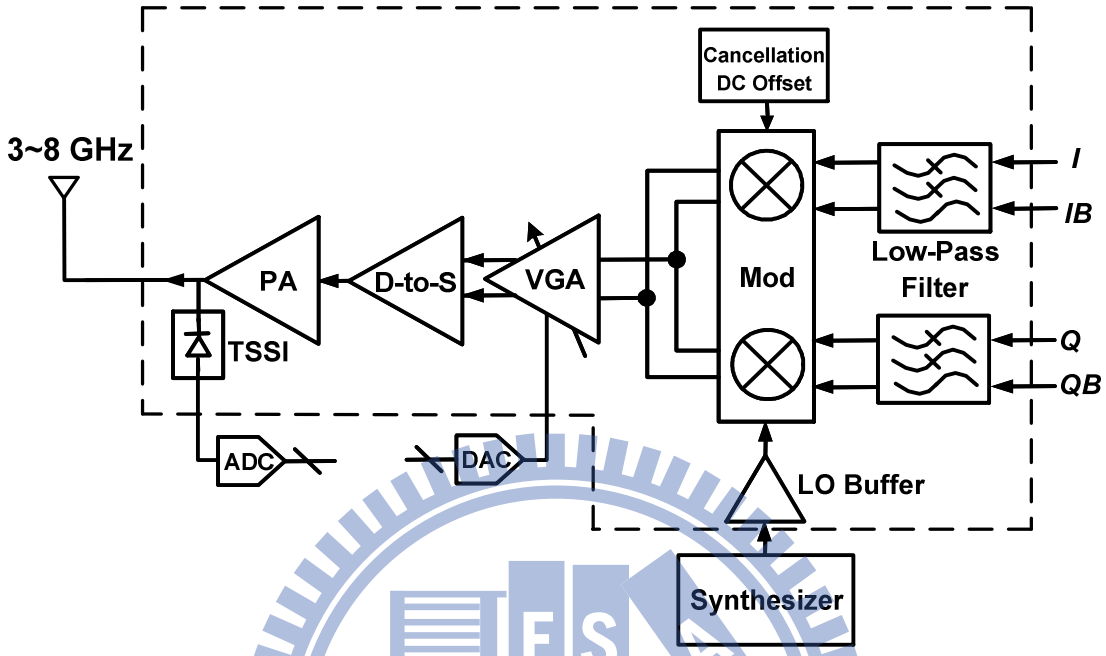


Figure 1-2: Architecture of the wideband RF transmitter.

A UWB RF transmitter should carry out wideband and high-linearity, as well as low power consumption for extending battery life. But in general, wideband and high-linearity require large power consumption. Therefore, architecture and circuit topology of the transmitter should be carefully considered to make power consumption as low as possible. Circuits in single-ended architecture consume only half of the power in their differential counterparts. But in the design of high frequency and wideband single-ended circuits, bonding wires in ground nodes of circuits causes gain degradation. Moreover, bonding wires in power lines add unwanted parasitic inductance to output loads. On the contrary, differential circuits form virtual grounds both in the ground notes and power lines. Bonding wires cause no effect on circuit performance. As shown in Figure 1-2, in the design of the UWB RF transmitter, power amplifier consumed largest power is designed in single-ended architecture for

power saving consideration. Other circuits especially the IQ modulator are designed in differential architecture for easing effect of bonding wires. Therefore, a wideband differential-to-single-ended (D-to-S) circuit is needed in the RF transmitter. In [14,15,16], power amplifiers for 3-5GHz applications are implemented by a common-source topology with open drain [14] or on-chip inductance load [15,16]. For providing sufficient output power and linearity performance up to 8GHz, more power consumption is needed by the common-source topology. Therefore, a proposed CMOS power amplifier is adopted for achieving sufficient output power and linearity performance up to 8GHz with low power consumption. Moreover, the proposed circuit topology of the power amplifier utilizes bonding wires in ground nodes and power line to form a shunt peaking load for extending its bandwidth and save die area efficiently.

In this design, a low-power 3-8 GHz wideband RF transmitter is implemented in a 1.2 V 0.13 μm CMOS process. The design techniques are addressed for low power, high linearity and wide bandwidth.

1.4 Contributions

This dissertation demonstrates techniques for design of a wideband, high-linearity RF transceiver in a deep sub-micro CMOS process.

In the receiver chain, we presents a 6.6 dB-NF 3~5 GHz wideband, high-linearity RF receiver architecture. The primary contributions of this part are as follows.

1. A receiver architecture that efficiently amplifies 3~5 GHz UWB RF signals and rejects strong close-in WLAN 802.11a signals is presented.

2. An analog baseband architecture that realizes wide bandwidth of 250 MHz, high IIP3 of -6 dBV and low noise figure of 14 dB under a low supply voltage of 1.2 V is presented.
3. A proposed current-mode PGAs that realizes wide bandwidth of 250 MHz and wide dynamic range of 82 dB is presented.
4. A current-mode Sallen-Key low-pass filter is adopted for effective rejection of out-of-band interferers.
5. Digitally-assisted DC-offset calibration improves second-order distortion of the entire chain. Therefore, IIP2 of -5 dBV is achieved.

In the transmit chain, we presents a 3~8 GHz wideband, high-linearity and low-power RF transmitter architecture. The primary contributions of this part are as follows.

1. A transmitter architecture that efficiently up-converts UWB baseband signals to radio frequency with low distortion, high modulation accuracy and low power consumption.
2. A proposed single-ended power amplifier that realizes 3~8 GHz wideband, high output P1dB of +1.5 dBm and low power consumption of 8 mA is presented.
3. Carrier leakage suppression is improved by calibration.
4. The high linearity and accurate IQ modulation lead to an error vector magnitude (EVM) of -28 dB under the data rate of 480 Mb/s in WiMedia Mode 1.

1.5 Overview of Dissertation

The remaining chapters in this dissertation provide further analysis and implementation details of the proposed techniques. An overview of the dissertation is as follows.

In Chapter 2, we first provide architecture of the receiver. Then the design challenges and specifications are discussed and addressed.

In Chapters 3, we provide architecture and specifications of the transmitter.

Chapter 4 focuses on design details and circuit implementation of the receiver.

Chapter 5 focuses on design details and circuit implementation of the transmitter.

In Chapter 6, measured results of the receiver are demonstrated.

In Chapter 7, measured results of the transmitter are demonstrated. Measured error vector magnitude (EVM) of WiMedia Mode 1 shows good linearity and modulation accuracy of the transmitter.

Finally, Chapter 8 concludes this dissertation and suggests some future research directions.

Chapter 2

Architecture and Specifications of Receiver

Figure 2-1 shows a direct-conversion RF receiver (DCR) for UWB. The receiver includes an RF front-end (a low noise amplifier, a 3th-order notch filter and a down-conversion mixer) and an analog baseband (PGAs and LPFs). The MB-OFDM UWB signal is amplified and down-converted to the baseband with a bandwidth of 250 MHz. The strong out-of-band interferer is down-converted as well. To avoid saturating the analog-to-digital converter (ADC) due to the interferer, the baseband is required to pass signals and suppress interferers. As compared to narrowband systems, design challenge of the UWB receiver lies in high linearity and wide bandwidth to handle both signals and interferers.

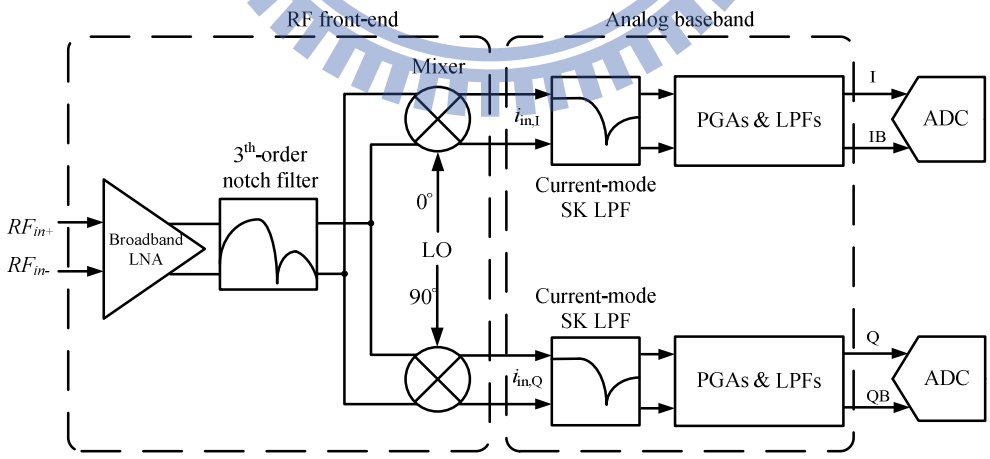


Figure 2-1: Architecture of a direct-conversion RF receiver for UWB.

The performance of the UWB band group1 (3168~4752 MHz) may be degraded by strong interferences which are signals of 802.11a WLAN system that occupies

frequency bands of 5.15~5.25, 5.47~5.725, and 5.725~5.875 GHz. In Figure 2-2, if the interferences are at 5.85 and 5.25 GHz, third-order inter-modulation (IM3) will be generated at 4.5GHz and saturate in-band desired signal and also desensitize the linearity. So the notch filter applied for the LNA is needed to reduce the interferences at 5~6 GHz [17] [18]. There are several advantages and trade-offs between each notch filter topology. Since the parasitic resistance of passive filter could not be canceled, the Q- factor is worse than that of active notch filter. Second-order active topology has better quality value, but some amount of wanted signal might be lost due to existing of only one zero. Third-order active notch filter provides not only one zero but also one pole that reduces the loss of gain of wanted signal [19]. Due to wide frequency range of interferences, the notch filter must have frequency tuning and gm tuning functions. If the interference could not be reduced enough, the gm tuning function can be turned on to solve this problem. In this design, a wideband differential LNA with integrated 3^{th}-order notch filter for interference rejection is designed.

Linearity restriction of the UWB RF receiver is at the output of the down-conversion mixer (input of the analog baseband). Large signal swing at the mixer output generates harmonics due to non-linearity of MOS transistors in the switching cells of the mixer and the input stage of the analog baseband. One way to reduce the signal swing without degrading SNR is to translate signals from the voltage domain to the current domain. To do so, a voltage-mode OP Amp can be configured as resistance feedback, forming low input impedance at the input of analog baseband. In addition, a capacitor can be parallel-connected with the feedback resistor to form a first-order low-pass filter to suppress out-of-band interferers. This method has already adopted in narrowband receiver design to achieve high linearity under a low supply voltage [20]. In this work, we further extend the method to a wideband RF

receiver, such as a UWB RF receiver. First of all, it requires realizing low input impedance over the entire wide bandwidth. Second, we need current-mode filters. Wideband current-mode circuits have been developed for applications of optical wireline communications. Some design techniques can be borrowed here. For example, the active feedback technique helps reduce input impedance of the amplifiers. Also filters constructed by current-domain circuits have been developed. Owing to WLAN 802.11a strong interferers are only 700 MHz away from MB-OFDM UWB 4.5 GHz channel, single-pole filter provides insufficient roll-off at 700MHz away. The Sallen-Key filter has been applied to deeply filter specific harmonics in some applications [21]. In this work, we realize a Sallen-Key filter constructed by current-domain circuits to filter the strong interferers in current domain efficiently.

Here, the reference specifications of the analog baseband are addressed following to the receiver conformance requirement. The entire receiver must meet the required sensitivity and signal-to-noise radio (SNR) of -80.8 dBm and 9.3 dB, respectively, under the data rate of 53.3 Mb/s with the longest transmission distance of 10 m which leads to the most strict sensitivity requirement to the receiver [2]. The maximum received signal strength is -10 dBm. Hence, the dynamic range of the RF receiver is 70.8 dB. 10 dB of the required dynamic range is contributed by RF front-end, the remainder is taken into account in the analog baseband. Owing to the full-scale of a UWB ADC is -14 dBV (200 mV_p), the required maximum voltage gain of the RF receiver is 67.8 dB to amplify signals from the sensitivity level to the ADC full-scale with a back-off of the MB-OFDM UWB signal peak-average radio (PAR) as 9 dB. Given that the RF front-end voltage gain is fixed at 15 dB, the analog baseband shall provide the maximum voltage gain of 52.8 dB. The required sensitivity translates to the required receiver noise figure (NF) as 6.6 dB. Assume the RF front-end NF is a

nominal value of 4 dB. Consequently the required noise figure of the analog baseband is less than 14 dB.

Linearity requirement for the RF receiver is constrained by the worst case that strong out-of-band interferers at the 5 GHz band (WLAN 802.11a) cause serious SNR degradation to the 4.5 GHz-channel as shown in Figure 2-2 [22]. The test case defines two interferers allocated at 5.2 GHz and 5.85 GHz with the power level of -4 dBm. The required sensitivity is -75 dBm and the required SNR remains 9.3 dB [23]. Assume the pre-filter in front of the RF receiver provides 25 dB attenuation for out-of-band interferers. The required input-referred third-order intercept point (IIP3) of the RF receiver is -1 dBm. In order to relax linearity requirement of the analog baseband, assume a notch filter is designed with LNA and provides 20 dB attenuation for out-of-band interferers. Therefore, the required out-of-band IIP3 of the analog baseband shall be over -8 dBV at the maximum gain setting. The interferers at 5.2 GHz and 5.85 GHz also could cause second-order inter-modulation distortion. To avoid degradation of SNR, the required IIP2 of the analog baseband should be better than -5 dBV as 10 dB attenuation of interferers is provided by the first stage of the analog baseband. According to the calculated specifications, Table I summarizes the receiver requirements to comply MB-OFDM UWB performance.

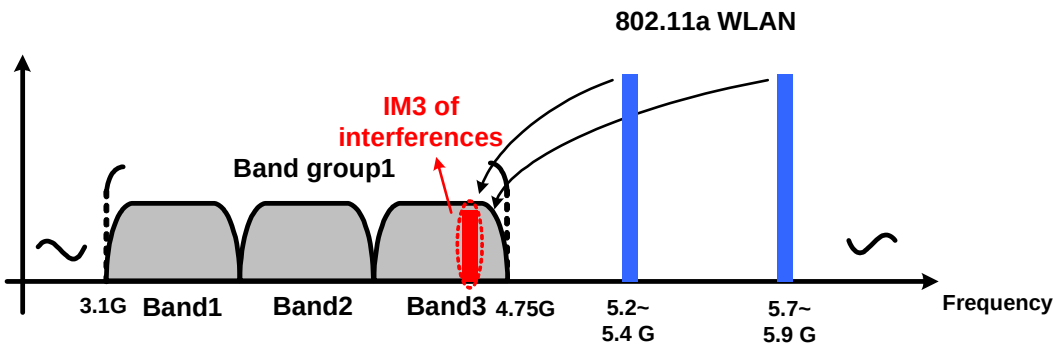


Figure 2-2: Strong nearby interferers at 5GHz (WLAN 802.11a) cause serious SNR

degradation at 4.5GHz channel.

TABLE I. Specifications of receiver

Overall receiver	
Sensitivity	-80.8 dBm
SNR	9.3 dB
Dynamic range	70.8 dB
Full-scale of a UWB ADC	-14 dBV
Maximum gain	67.8 dB
Attenuation of Pre-filter	25 dB
IIP3	-1 dBm
Noise figure	6.6 dB
RF front-end	
Gain	15 dB
Attenuation of Notch Filter	20 dB
Noise figure	4 dB
Analog baseband	
Bandwidth	250 MHz
Gain Range	61 dB
Maximum gain	53 dB
Gain control resolution	1 dB
Noise Figure	14 dB
Out-of-band IIP3	-8 dBV
Out-of-band IIP2	-5 dBV

Chapter 3

Architecture and Specifications of Transmitter

The architecture of the proposed transmitter is as shown in Figure 3-1, which carries out the direct-conversion architecture, including an analog baseband, an IQ modulator, a RF VGA, a D-to-S amplifier and a power amplifier. Moreover, a transmitted signal strength indicator (TSSI) is also integrated. The analog baseband consists of a 5^{th}-order Chebyshev low-pass filter and baseband VGAs. As the baseband signal input, the low-pass filter eliminates the output harmonics from a digital-to-analog converter (DAC). The baseband VGAs provide tunable attenuation from 9dB to 19dB to adjust the signal amplitude to a pre-determined proper level for the IQ modulator. The IQ modulator is designed to modulate baseband signals to RF frequency. A DC-offset cancellation circuit is also integrated for improving the performance of carrier leakage suppression. The RF VGA provides linear-in-dB gain tuning of 14dB. The D-to-S amplifier is designed before the single-ended power amplifier for combining differential signals with an acceptable gain and phase error from 3GHz to 8GHz. Finally, the power amplifier is designed to boost the RF signals and linearly drive the 50Ω antenna load.

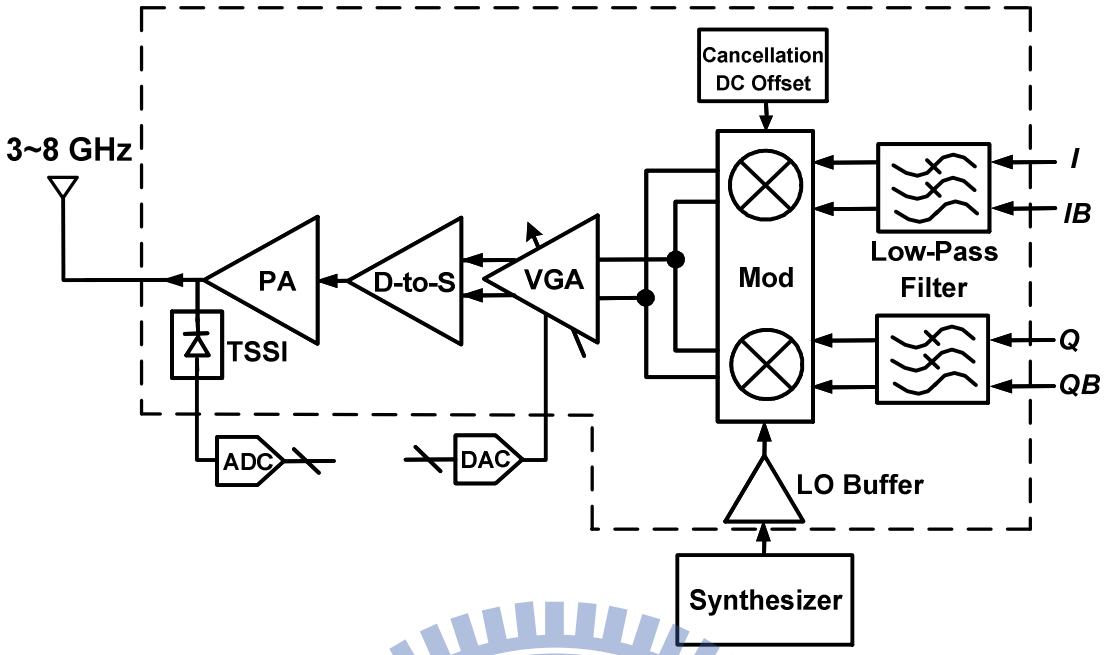


Figure 3-1: Block diagram of the wideband RF transmitter.

In digital baseband, DAC generates modulated signals with a sufficient spurious-free dynamic range (SFDR) to meet the system requirement. Then an RF transmitter performs $I + j \cdot Q$ to combine in-phase and quadrature-phase signals from the DAC and up-converts the modulated signals to the RF frequency. But the RF transmitter introduces unwanted effect on the output signals such as carrier leakage, sideband leakage and distortions simultaneously. The signal-to-noise ratio (SNR) is the most important parameter to receiver design. However, the key parameter of transmitter design is the signal-to-spur ratio (SSR). The carrier leakage, sideband leakage and distortions all lead to SSR degradation.

According to the FCC regulation, the output power spectrum density of UWB is limited to -41.3dBm/MHz. The maximum in-band signal power is calculated as

$$-41.3dBm\ /\ Hz + 10 \cdot LOG_{10}(528\,MHz) = -10\,dBm\ . \tag{3.1}$$

The transmitter output power should be up to -7.5dBm assuming the signal attenuation is 2.5dB due to the transmit/receive (T/R) switch at the transmitter output.

Listed in Table II is the transmitter link budget, which is a tradeoff between SSR and linearity. The input voltage swing to this transmitter, or the output voltage swing from a DAC, is assumed in the range from $125mV_p$ to $375mV_p$ for a flexible DAC interface. For the optimal linearity performance of the IQ modulator, the input voltage swing at the modulator input is fixed at 44.6mV (-27dBV). It requires gain tuning from -9dB to -19dB in the analog baseband filter. Thus, it is specified a gain tuning range of 10dB with the resolution of 1dB. The RF circuits following the analog baseband provide 9.5dB gain for the maximum output power of -7.5dBm.

Transmitter linearity is constrained by the signal peak-average ratio (PAR) of 9dB, which leads to an instantaneous power increase of 9dB. Therefore, the RF transmitter should have the ability to linearly transmit signals as large as +1.5dBm. Consequently the required OP1dB is +1.5dBm. The carrier leakage emission is also strictly regulated within -41.3dBm. Thus, the required carrier leakage suppression is derived as

$$-10\,dBm - (-41.3dBm) = 31.3dBc\ . \tag{3.2}$$

The leakage is lumped to the effect caused by DC offset. Since the voltage swing at the IQ modulator input is 44.6mV (-27dBV), the input-referred DC-offset of the IQ modulator should be less than 1.21mV (-58.3dBV). This small level requires a DC-offset cancellation circuit. According to the transmit spectrum mask specified by MB-OFDM UWB, the filter in the analog baseband should provide at least out-of-band attenuation of 12dB and 20dB at the frequencies of 285MHz and 330MHz, respectively. The design specification of the MB-OFDM UWB RF transmitter is listed in Table III.

TABLE II. Link budget of transmitter

DAC output swing	125 mV_p -to- 375m V_p (-18 dBV ~ -8.5 dBV)
Gain of analog filter	-9 dB ~ -19 dB
Modulator input swing	-27 dBV
Gain of RF stages	9.5 dB
Output power of transmitter	-7.5 dBm

TABLE III. Specifications

Analog Baseband	Bandwidth: 250 MHz
	Gain: -9 dB~-19 dB
	Gain resolution: 1 dB
	THD: -40 dBc
	Attenuation: 285MHz: 12 dB 330MHz: 20 dB
RF circuits	Gain: 9.5 dB
Overall Tx	Pout,max: -7.5 dBm
	OP1dB: +1.5 dBm
	Carrier Suppression > 31 dBc
	Sideband Suppression > 30 dBc
	Power control range: 14 dB

Chapter 4

Circuit Design of Receiver

4.1 RF Front-End

4.1.1 Low-Noise Amplifier (LNA)

The schematic of LC ladder LNA is shown in Figure 4-1. Gain switch function is formed by the control bit (Gain_SW) that has 10dB gain difference between high and low gain mode. Band control function is formed by the control bits LG (0~3) that change equivalent capacitance of output load to switch to the desired UWB channel in band group1 (3432, 3960 and 4488 MHz). In order to extend bandwidth at higher frequency band, we shunt switch M5 and large resistor R_L with the output loading LC tank. If bandwidth is not enough at higher frequency band (512MHz), M5 can be turned on by switch HF_ON to extend bandwidth, but it must sacrifice a little power gain. The proposed notch filter was connected on the drain of M1 that provided low impedance path for small signal current to ground at interference frequency. The ESD protection circuit was added on the virtual ground position of input matching, so it won't affect input return loss of the LNA.

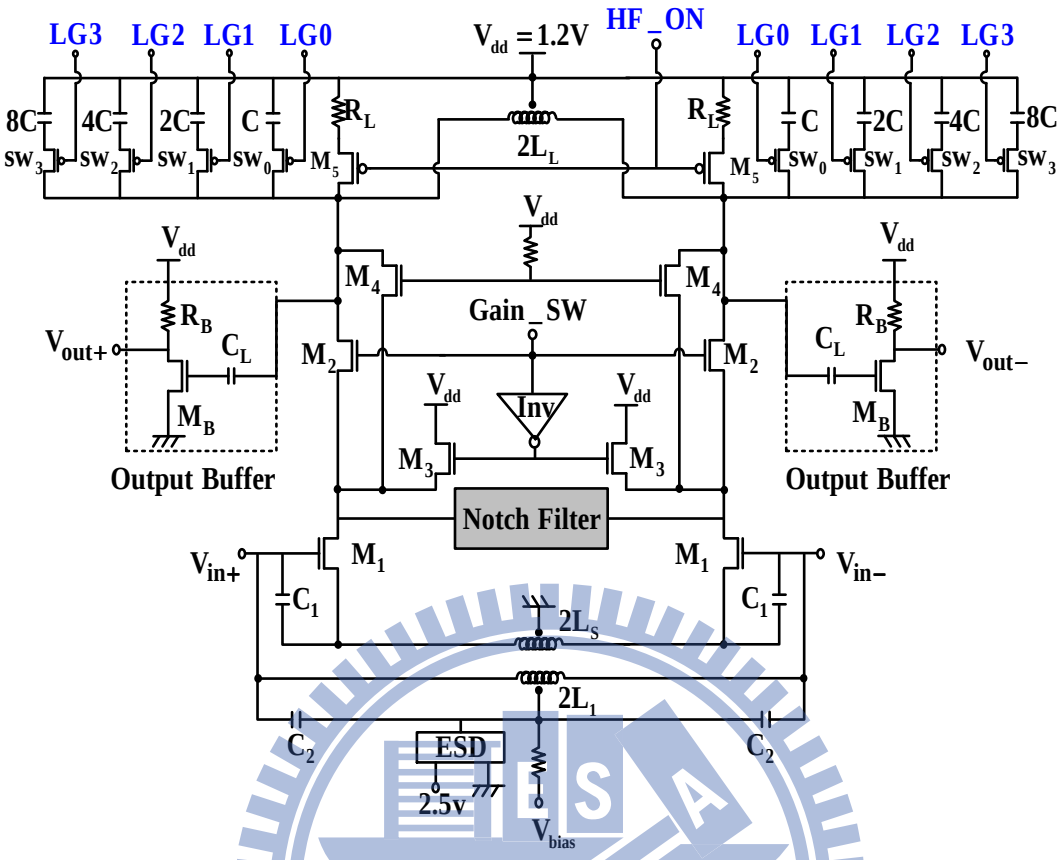


Figure 4-1: Schematic of LC ladder LNA core

4.1.2 Input Matching Analysis

Consider two-order low-pass-filter as shown in Figure 4-2(a). Using the low-pass to band-pass transformation, the shunt capacitor and series inductor can be transformed to parallel LC and series LC network respectively. The two corner frequencies of band-pass-filter are w_U and w_L that define the fractional bandwidth (n) as [24]:

$$n = \frac{w_U - w_L}{\sqrt{w_U \cdot w_L}} \tag{4.1}$$

Since n>1, the band-pass-filter can be viewed as a low-pass-filter combined with a high-pass-filter. In this case, w_U is decided by L_U, C_U and w_L is decided by L_L, C_L. The values of these components can be roughly expressed as:

$$L_L = \frac{R}{w_L} \quad C_L = \frac{1}{w_L \cdot R} \quad L_U = \frac{R}{w_U} \quad C_U = \frac{1}{w_U \cdot R} \tag{4.2}$$

and we determine desired bandwidth of input return loss by proper choosing component values of L_U, C_U, L_L and C_L. In Figure 4-2(b), Z_G is expressed as:

$$Z_G = w_T \cdot L_s + s \cdot L_s + \frac{1}{s \cdot C_T} \tag{4.3}$$

where $C_T = C_{GS1} + C_1$, and $w_T = \frac{g_{m1}}{C_T}$. If C_L is replaced by C_T and L_U by L_s, and choose M1 size to let $\frac{g_{m1}}{C_T} \cdot L_s = R$, the frequency response of input matching network will be the same with the designed band-pass-filter and generates two resonance frequency to expand S11 for broadband matching.

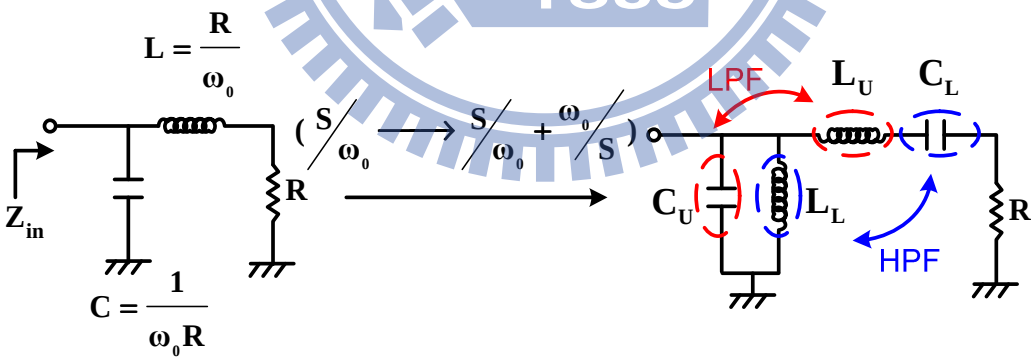
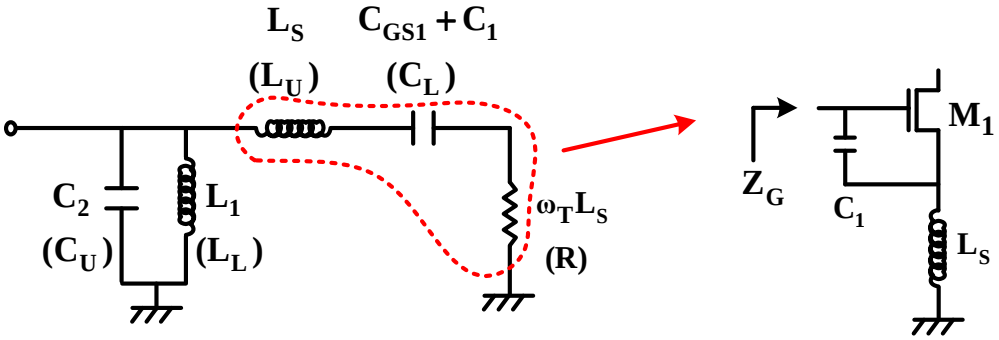


Figure 4-2(a): Transformation from LPF to BPF



(b) Schematic of the LNA input matching network

Figure 4-2(b): Design method analysis for input matching of the LNA core.

4.1.3 Gain analysis

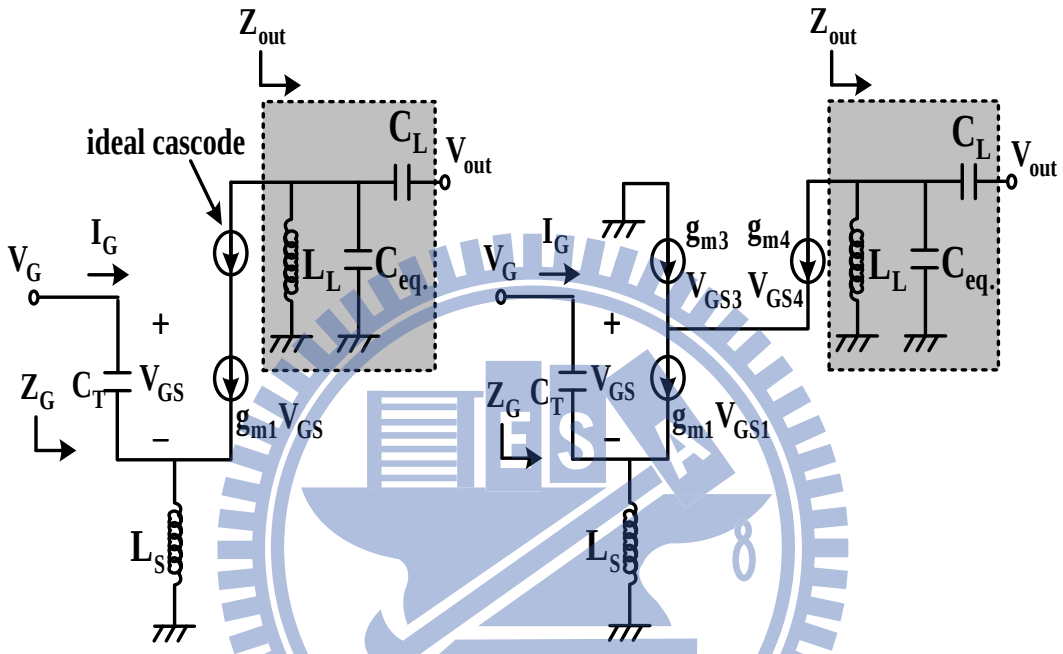
The small signal model of high gain mode is shown in Figure 4-3(a), the voltage gain can be derived by solving the trans-impedance and neglecting effects of output buffer. Overall voltage gain can be calculated as:

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{1+s\cdot g_{m1}\cdot L_s + s^2\cdot L_s\cdot C_T}\cdot\frac{s\cdot L_L}{1+s^2\cdot L_L\cdot C_{eq}} \tag{4.4}$$

where C_{eq} is the total capacitance at output node that including parasitic capacitor C_{db} of the cascode stage (M3 and M4) and capacitor array value which controlled by LG (0~3). From equation (4-4), If C_{eq} decreases, the voltage gain increases and desired band will “move” to higher frequency.

When switch to low gain mode as shown in Figure 4-3(b), M2 off and M3 on. If sizes of M2 and M3 are identical, the small signal current that flows into the drain of M1 is equal to that in high gain mode, so input frequency response (S_{11}) will be the same. We choose size ratio of M3 to M4 is 2 : 1, and the current flows from output

load will be 1/3 times of that flows into the drain of M1 (i.e. $g_{m1} \cdot V_{GS1} = 3 \cdot g_{m4} \cdot V_{GS4}$), so the overall voltage gain of low gain mode will be reduced by 3 times compared with high gain mode. That means the power gain (S21) of low gain path is 9.54 ($20 \cdot \log_{10} 3$) dB less than that of high gain mode.



(a) High gain mode model (b) Low gain mode model

Figure 4-3: Small signal model analysis for LC ladder LNA.

4.1.4 Third-Order Notch Filter Design

Third-order active notch filter is the best topology to reject interferences due to deep and steep notch at resonance frequency. It needs 2 series inductors for differential LNA and occupies large chip area. The circuit topology of proposed third-order active notch filter is shown in Figure 4-4 that only needs one center-taped parallel inductor to save chip area for differential topology. The input impedance from M1 gate can be derived as:

$$Z_{in}^{'} = (r_{g1} - \frac{g_{m1}}{w^2 \cdot C_{gs} \cdot C_f}) + \frac{1}{jw \cdot C_T} = R_x + \frac{1}{jw \cdot C_T} \tag{4.5}$$

where $C_T = \frac{C_{gs} - C_f}{C_{gs} + C_f}$ and $R_x = r_{g1} - \frac{g_{m1}}{w^2 \cdot C_{gs} \cdot C_f}$. So Z_{in} can be equivalent to the RLC network as shown in Figure 4-5. Total equivalent parallel parasitic resistance R_P can be expressed as:

$$R_p = R_{PL} // R_{PC} = \frac{\left(\frac{L_f}{C_T}\right)^2 \cdot \frac{1}{R_{Lf} \cdot R_x}}{\frac{(w \cdot L_f)^2}{R_{Lf}} + \frac{1}{R_x \cdot (w \cdot C_T)^2}} = \frac{(w \cdot L_f)^2}{R_x \cdot (w^{2\cdot} \cdot L_f \cdot C_T)^2 + R_{Lf}} \tag{4.6}$$

If R_P approaches to infinity, the condition of the best Q-factor of the filter occurs as shown in equation (4.7):

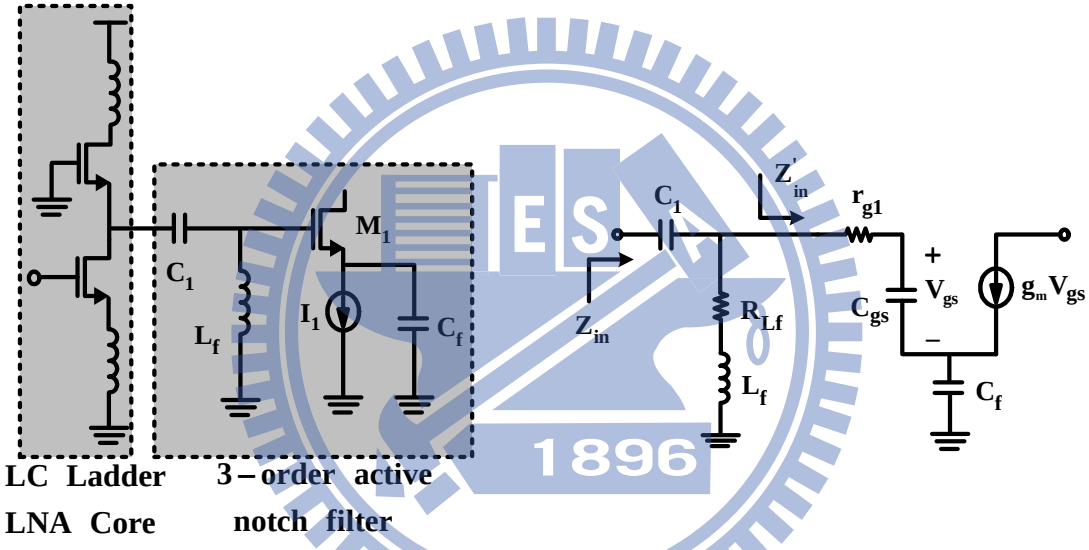
$$\frac{R_{Lf}}{(w^2 \cdot L_f \cdot C_T)^2} + r_{g1} = -\frac{g_{m1}}{w^2 \cdot C_{gs} \cdot C_f} \tag{4.7}$$

The power gain of LNA at interference frequency(w) will lower to minimum as the sizes of transistor M_1 and other passive elements satisfy equation (4-7), then Q-factor of this 3-order active filter will be maximize at the interference frequency. As the condition occurs, Z_{in} can be expressed as:

$$Z_{in} = \frac{1}{s \cdot C_1} + \left(\frac{1}{s \cdot C_T} // s \cdot L_f\right) = \frac{1 + s^2 \cdot L_f \cdot (C_1 + C_T)}{s \cdot C_1 \cdot (1 + s^2 \cdot L_f \cdot C_T)} \tag{4.8}$$

Equation (4.8) generates not only one zero but also one pole. The resonant frequency of pole is $f_{wanted} = \frac{1}{2\pi \cdot \sqrt{L_f \cdot C_T}}$, and resonant frequency of zero is $f_{wanted} = \frac{1}{2\pi \cdot \sqrt{L_f \cdot (C_1 + C_T)}}$. Figure 4-6 is the schematic of proposed 3-order active notch filter. Due to wide interference range (5.15~5.875 GHz), the filter has frequency

tuning function to track different positions of interferences. Zero resonant frequency f_{int} can be varied by C_T. Thus, varactor $C_{3,4}$ and C_6 are added to vary equivalent capacitor of C_{gs} and C_f respectively and controlled by 3-bits control (F_Tune). Since equivalent values of C_{gs} and C_f are varied, equation (4.7) is difficult to satisfy at fixed trans-conductance of M1 (g_{m1}). The switch transistors P_0~P_3 provide different current for M1 to change g_{m1} to satisfy equation (4.7) and compensate Q-factor of the notch filter. If gain attenuation is not enough at interference frequency, the g_{m1} tuning circuit can be turn on to achieve enough high Q-factor.



(a) Circuit topology (b) equivalent small signal model

Figure 4-4: Proposed 3-order active notch filter (half-circuit)

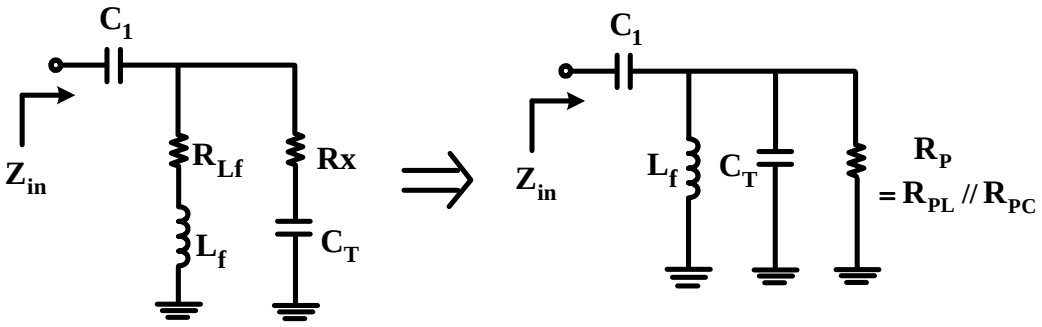


Figure 4-5: The equivalent circuit of proposed 3-order active notch filter.

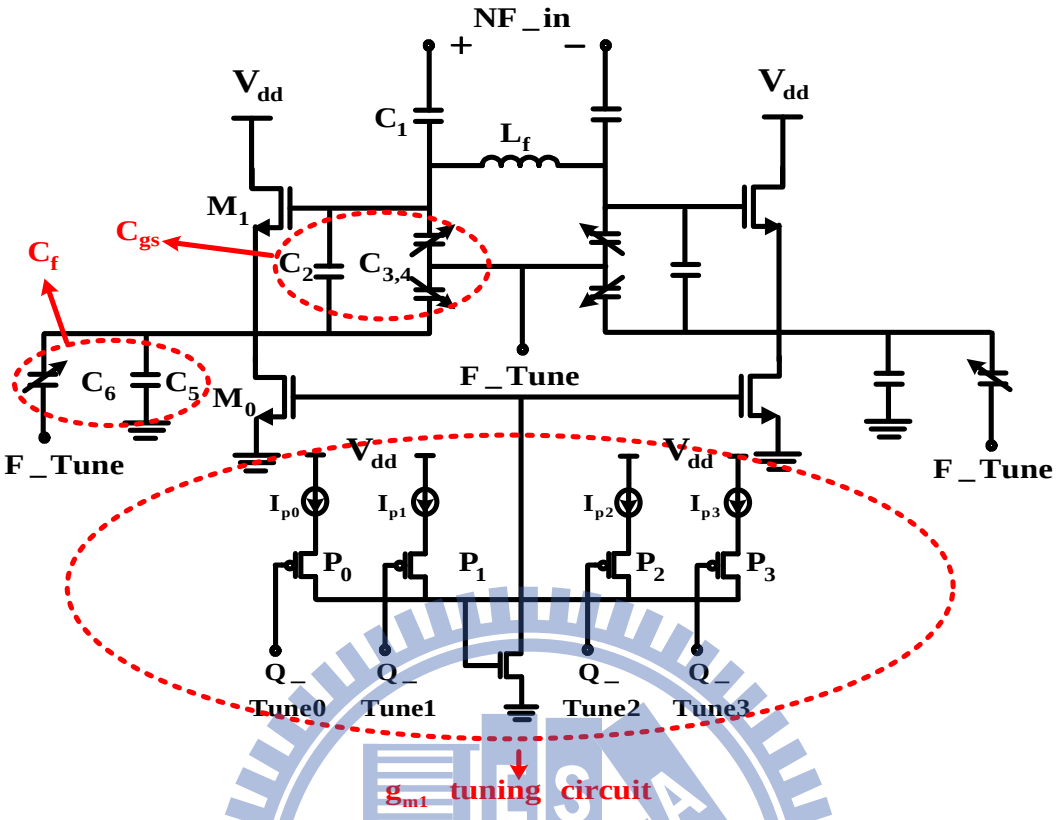


Figure 4-6: Schematic of third-order active notch filter.

4.2 Analog Baseband

As shown in Figure 4-7, a proposed wideband, wide dynamic range baseband chain is composed in the order of three-stage current-mode PGAs, a G_m-C filter, three-stage current-mode PGAs, an I-to-V converter and a voltage buffer. Besides, a digital-assisted DC-offset calibration loop is adopted to eliminate DC-offset of the baseband chain. The current-mode PGA is realized by balanced current-mode amplifiers to provide gain and gain tuning range. The first current-mode PGA also includes a current-mode SK LPF. Placed in the middle of the baseband chain, the G_m-C filter filters out-of-band unwanted signals. The I-to-V converter is used to covert output current-domain signals of the current-mode PGAs to voltage-domain signals.

Finally, a voltage buffer is designed for driving analog-to-digital converter (ADC).

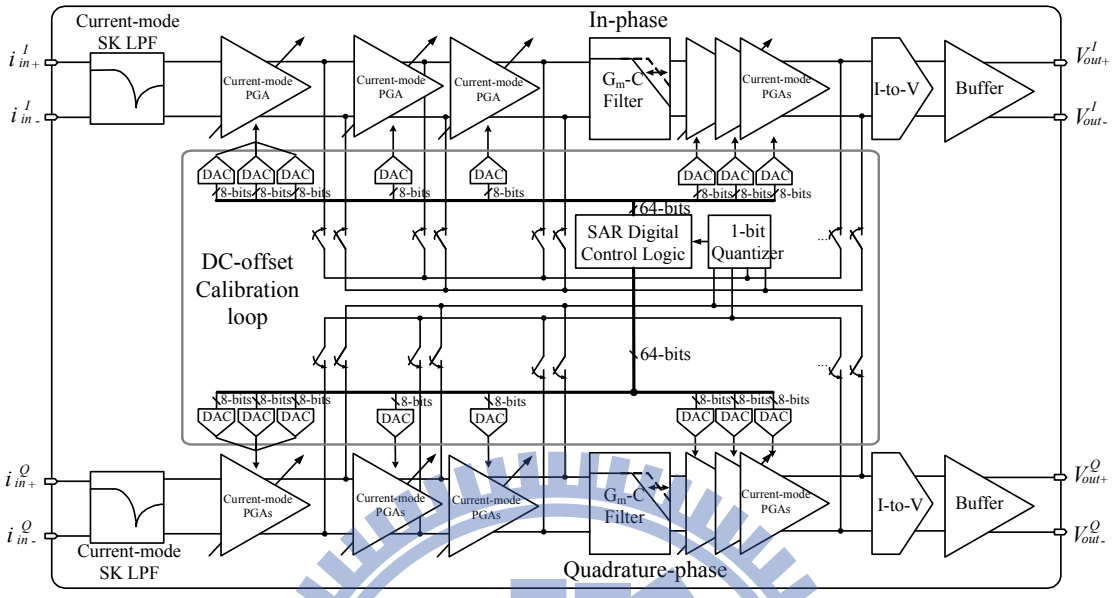


Figure 4-7: Block diagram of the wideband, wide dynamic range baseband chain.

In [11], the gain tuning function of the UWB low-pass filter is attained by controlling trans-conductance (g_m) in the filter circuits, resulting in less gain, less gain tuning range and poor noise figure performance. In this design, the gain tuning function of the analog baseband is accomplished by the current-mode PGAs. The three-stage current-mode PGAs in front of the G_m-C filter are designed with the gain of 47 dB to suppress G_m-C filter noise. So the analog baseband exhibits much better noise figure performance than that reported in [11]. The three-stage current-mode PGAs follow the G_m-C filter to achieve the required overall gain and dynamic range. The analog baseband has gain tuning range from -9 dB to 73 dB, which leads to maximum gain of 73 dB and the dynamic range of 82 dB with gain resolution of 0.5 dB. The corner frequency of the baseband chain, determined by the G_m-C filter and adjusted by the capacitors arrays, ranges from 250 MHz to 300 MHz. A G_m-C calibration circuit is also integrated to tune the capacitors arrays against PVT

variation.

4.2.1 Programmable gain Amplifiers (PGAs)

Ideally the current amplifier should have infinite output impedance and zero input impedance for optimal current signal transfer. But in the advance CMOS process, drain-source (R_{ds}) resistance is greatly decreased. Cascode topology for increasing output impedance cannot be easily realized due to the headroom limitation under a low supply voltage. Circuit design effort is therefore on very low input impedance.

PGAs are constructed by the current amplifier in the simple common-gate (CG) configuration, as shown in Figure 4-8(a), exhibiting an input resistance of 1/ g_{m1}. Low input impedance indicates a large-size transistor and high bias current, and in turn, leads to large input capacitance and high input-referred noise from the tail current source [25]. As shown in Figure 4-8(b), a series-series feedback loop through M3 and M4 is added to decrease the input resistance without degrading bandwidth and noise performance. The input impedance of the current amplifier with the feedback is derived as

$$Z_{in} = \frac{1}{g_{m1}} \cdot \frac{s^2 C_1 C_2 + s(C_1 g_{m2} + C_2 g_{m4}) + (g_{m4} \cdot g_{m2} - g_{m1} \cdot g_{m3})}{s^3 \frac{C_1 \cdot C_2 \cdot C_{in}}{g_{m1}} + s^2 \left[C_1 C_2 + \frac{C_{in}}{g_{m1}} (C_1 g_{m2} + C_2 g_{m4}) \right] + s \left[C_1 g_{m2} + C_2 g_{m4} + \frac{C_{in}}{g_{m1}} (g_{m4} g_{m2} - g_{m1} g_{m3}) \right] + g_{m4} \cdot g_{m2}} \tag{4.8}$$

where $C_1 = C_{gs4} + C_{ds4} + C_{ds3}$, $C_2 = C_{gs2} + C_{ds2} + C_{gs3}$. At low frequencies, the input resistance is reduced to

$$Z_{in,DC} = \frac{1}{g_{m1}} \cdot \left(1 - \frac{g_{m1}}{g_{m4}} \cdot \frac{g_{m3}}{g_{m2}}\right) \tag{4.9}$$

The input-impedance is reduced by a factor of $1 - g_{m1} \cdot g_{m3} / (g_{m4} \cdot g_{m2})$ due to the series-series feedback. If PMOS is used in M4, higher feedback gain can be found,

but the bandwidth of the current amplifier will be reduced.

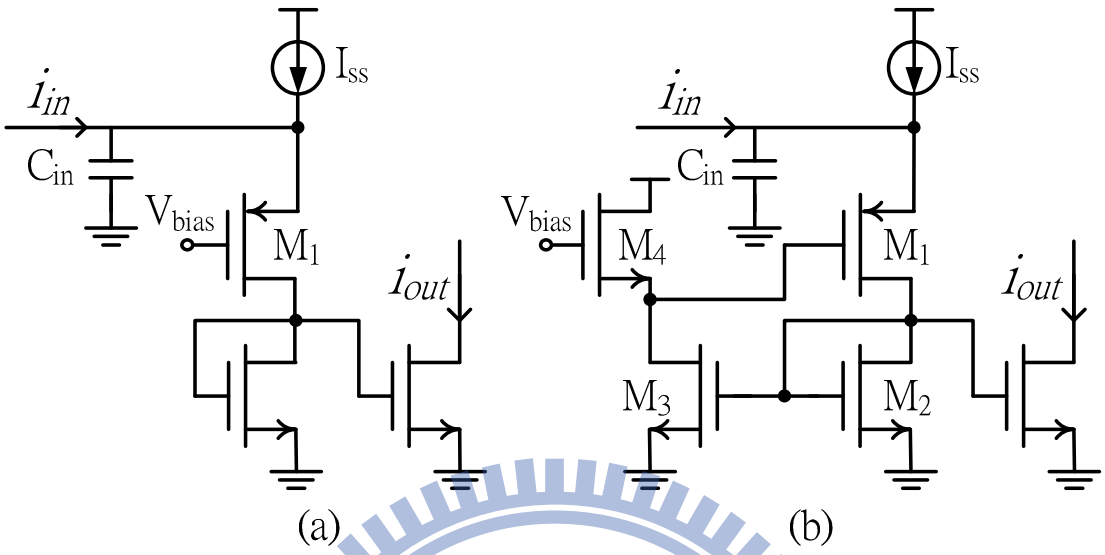


Figure 4-8: (a) Conventional CG current amplifier, (b) Proposed current amplifier with series-series feedback.

The complete schematic of the differential PGA is shown in Figure 4-9. The input stage is accomplished by the series-series feedback for low input impedance. The bandwidth of the feedback must be large enough across the entire channel band (250 MHz in this case since direct conversion is used). As shown in Figure 4-10, the simulated input impedance exhibits a low value of 15 ohm up to 1 GHz. The PGA load is composed of current mirrors in the cascode configuration for high output impedance. Current gain is programmable by changing the size ratio of the current mirror load using switches to turn on or off the cascode stage. Therefore, current consumption of the PGA is proportional to its gain. For linearity concern, DC bias current is designed in class-A operation. As to the output DC voltage, it is defined by a common-mode feedback (CMFB) amplifier and matched to the input DC voltage of the next PGA stage. Figure 4-11 shows the frequency response of the PGA over different gain settings.

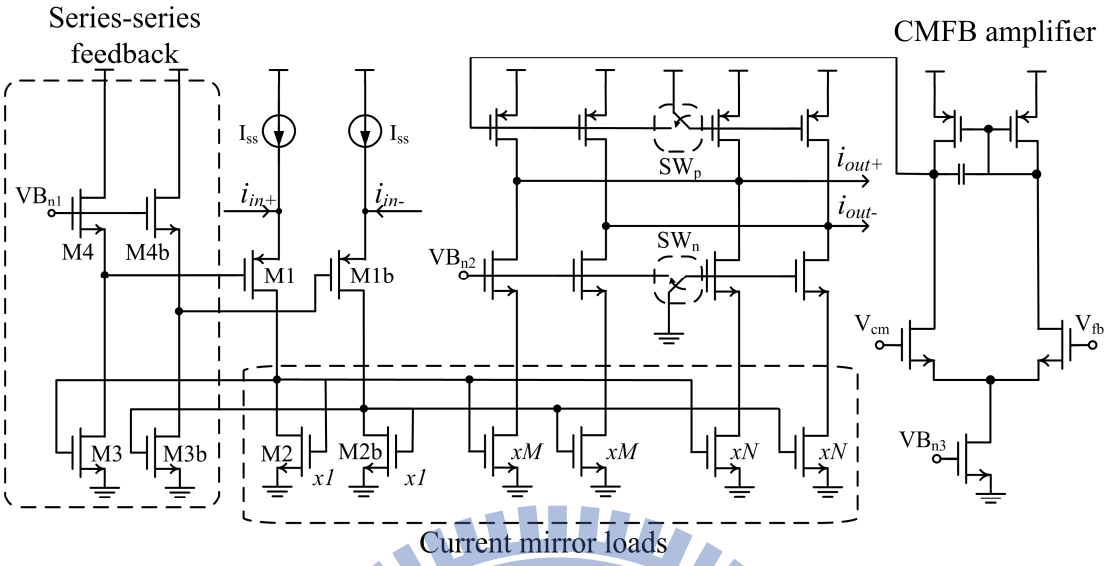


Figure 4-9: The schematic of PGA based on current amplifier.

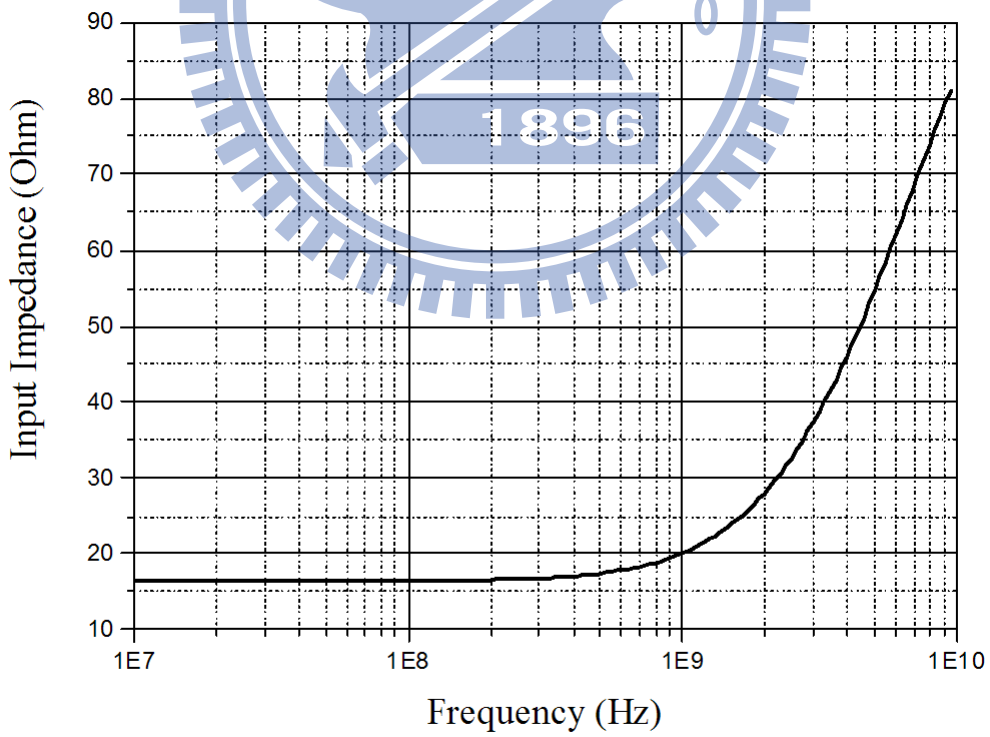


Figure 4-10: Simulated input impedance of PGA.

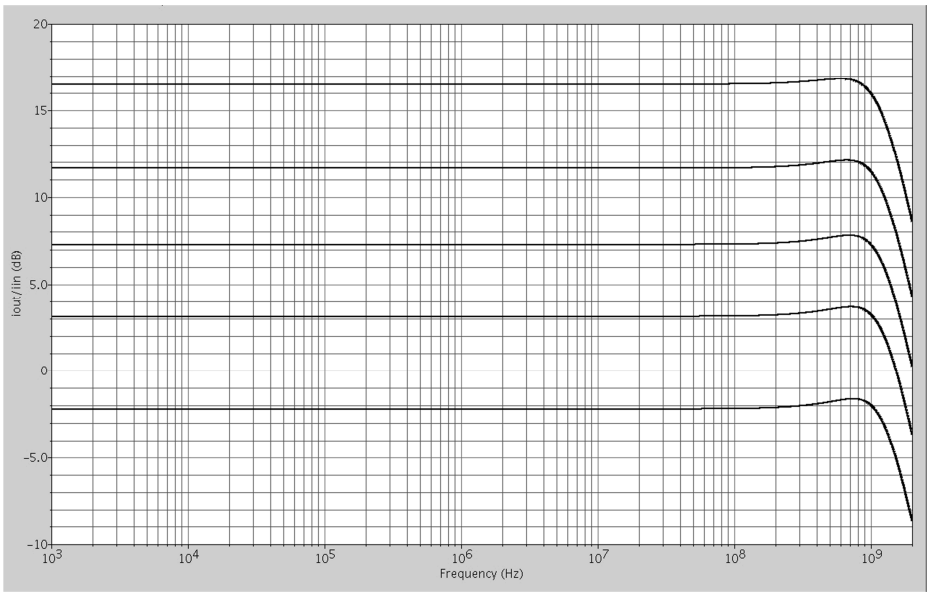


Figure 4-11: Frequency response of the PGA over different gain settings.

As shown in Figure 14-9, owing to high source impedance, noise contributed by M1 and the series-series feedback circuit (M3-M4) of the PGA can be neglected. The input-referred noise current of the PGA depends critically on the trans-conductance of M2 and current source (I_{ss}), as indicated in the following equation:

$$\bar{i}_{n,in}^2 = 4kT \cdot \gamma \cdot (g_{m2} + g_{mss}) \tag{4.10}$$

As g_{m2}=12mS and g_{mss}=5.77mS, the PGA exhibits a low input-referred noise current of 42.5 pA/$\sqrt{}$ Hz. Simulated by SpectreRF, noise analysis shows that the input-referred noise of the analog baseband is dominated by the current noise of the first two PGAs and governed by (4.10). Circuit noise after the first two PGAs is greatly suppressed by the high gain of the first two PGAs.

In the first stage of the PGAs, the current-mode SK LPF is implemented for filtering the interferers from WLAN 802.11a signals [26-27]. The schematic is similar to the current amplifier except the resistor-capacitor feedback at the output as shown in Figure 4-12. Therefore, the inter-modulation term due to the interferers is greatly

reduced, which leads to relaxed linearity requirement to the following PGAs. The equivalent circuit model of the current-mode SK LPF is shown in Figure 4-13. The transfer function of the current gain can be derived as

$$H(s)=\frac{i_{out}(s)}{i_{in}(s)}=\frac{s^2C_1C_2R_1r_i+sC_2r_i-F}{s^2[C_1C_2(R_1R_2+r_i(R_1+R_2))]+s\{C_1(R_1+R_2)+C_2[R_i+R_2(1+F)]\}+1} \tag{4.11}$$

where F is the current gain of the current amplifier and r_i is the non-zero input resistance of the current amplifier. Composed by a complex-conjugate pair, the zeros in equation (4.11) form a transmission zero and make a notch in the frequency response. By assuming that the zeros are located at $s=-a\pm jb$, we can write the numerator of (4.11) in the form of

$$H_{num}(s)=s^2+2as+(a^2+b^2) \tag{4.12}$$

The notch frequency (w_t) satisfies the following equation:

$$\frac{d(|H_{num}(s)|)}{ds}\Big|_{s=w_t}=0 \tag{4.13}$$

Substituting (4.12) into (4.13), we obtain the notch frequency as:

$$w_t=\sqrt{b^2-a^2} \tag{4.14}$$

Assume $C_1=C$, $C_2=\alpha C$, $R_1=R$, $R_2=\lambda R$, $r_i=\beta R$ and F=-1. (4.11) can be rewrote as follows:

$$H(s)=\frac{i_{out}(s)}{i_{in}(s)}$$

$$=\frac{\alpha\beta}{\alpha(\lambda+\beta+\beta\lambda)}\times\frac{s^2+\frac{1}{RC}s+\frac{1}{\alpha\beta(RC)^2}}{s^2+\frac{1+\lambda+\alpha\beta}{\alpha(\lambda+\beta+\beta\lambda)}s+\frac{1}{\alpha(\lambda+\beta+\beta\lambda)(RC)^2}} \tag{4.15}$$

Solving a and b by using (4.12) and numerator of (4.15), notch frequency (w_t) and quality factor (Q_z) can be expressed by the filter parameters (RC, α, β and λ) as

follows:

$$w_t = \frac{1}{RC}\sqrt{\frac{1}{\alpha\beta} - \frac{1}{2}} \tag{4.16}$$

$$Q_z = \sqrt{\frac{1}{\alpha\beta}} \tag{4.17}$$

Besides, pole frequency (w_p) and quality factor (Q_p) of the denominator of (4.15) can be derived as follows:

$$w_p = \frac{1}{RC}\sqrt{\frac{1}{\alpha(\lambda+\beta+\beta\lambda)}} \tag{4.18}$$

$$Q_p = \frac{\sqrt{\alpha(\lambda+\beta+\beta\lambda)}}{1+\lambda+\alpha\beta} \tag{4.19}$$

Finally, we can obtain the filter parameters (RC, α, β and λ) by solving (4.16), (4.17), (4.18) and (4.19).

Consider the worst case that the UWB channel of band 3 (frequency centered at 4.5 GHz) is used. The WLAN 802.11a interferer in the RF band of 5.7 GHz~5.9 GHz will be down-converted to the baseband frequency of 1.2 GHz~1.4 GHz. The notch can be designed in the frequency of 1.2 GHz~1.4 GHz to filter the interference signals. Actually another WLAN 802.11a interfere in the RF band of 5.2 GHz~5.4 GHz is down-converted to the baseband frequency of 0.7~0.9 GHz, closer to the signal band. Yet choosing the notch in 1.2~1.4 GHz causes less in-band signal degradation while reducing the same amount of baseband inter-modulation distortion due to these two interferers. Therefore, the inter-modulation term falls into band 3 caused by WLAN 802.11a signals in 5.2 GHz~5.4 GHz and in 5.7 GHz~5.9 GHz can be greatly reduced. Thus, we design the notch frequency (W_t) of the current-mode SK LPF at 1.3 GHz (middle frequency of 1.2 GHz~1.4 GHz) and the pole frequency (W_p) at 250 MHz (bandwidth of the channel). Furthermore, let Q_z and Q_p to be 3 and 0.707, respectively.

Assume C_1 is 1 pF, we can have the following filter parameters from (4.16~4.19):

$$\alpha = 2.0637$$

$$\beta = 0.0538$$

$$\lambda = 1.4116$$

$$RC = 3.5693 \times 10^{-10}$$

The simulated frequency response of the current-mode SK LPF is shown in Figure 4-14. In the circuit design, the capacitors (C_1 and C_2) and resistors (R_1 and R_2) in the SK LPF are designed in a binary-weighted array and can be tuned by a 3-wire control interface to cover PVT variations. As shown in Figure 4-14, by tuning the passive components (C_1, C_2, R_1 and R_2), the notch frequency of the current-mode SK LPF can be designed at 1.2 GHz, 1.3GHz and 1.4 GHz, respectively.

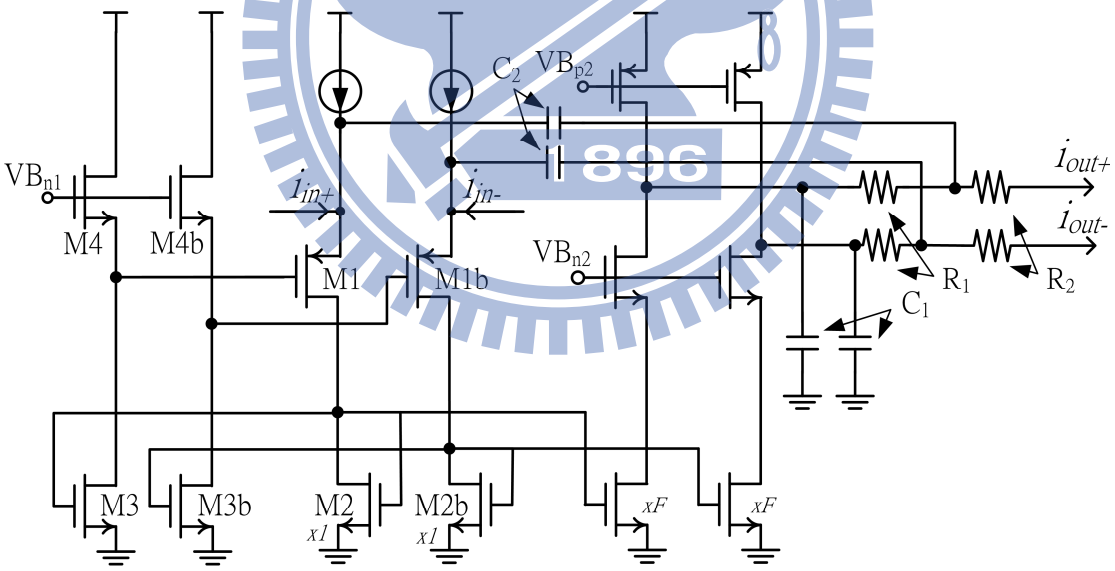


Figure 4-12: The schematic of current-mode SK LPF.

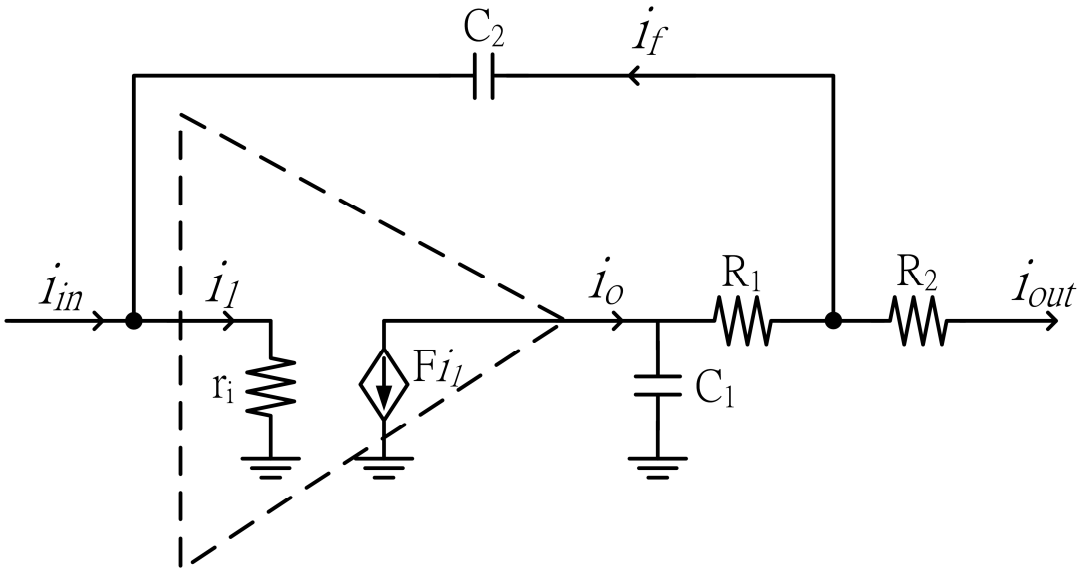


Figure 4-13: Equivalent circuit model of the current-mode SK LPF.

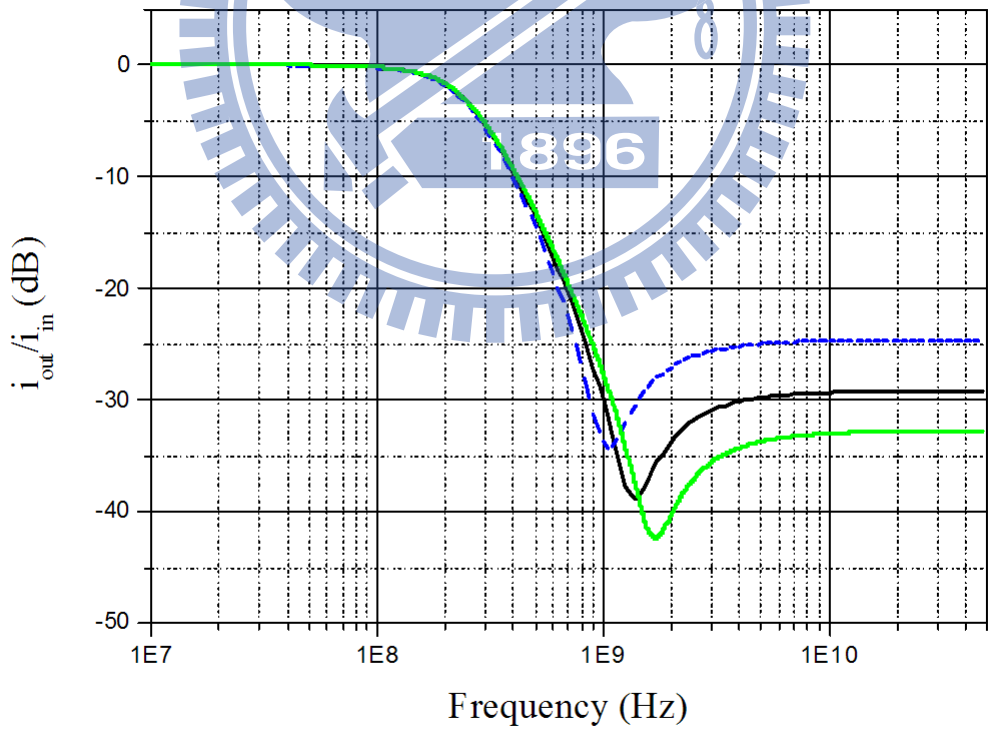


Figure 4-14: Frequency response of the current-mode SK LPF.

4.2.2 G_m-C filter

The G_m-C filter utilizes the LC ladder structure to accomplish the 6th-order Chebyshev low-pass filter as shown in Figure 4-15. The schematic of the G_m cell is as shown in Figure 4-16. The super source follower structure as in [28] is applied to improve the linearity of the G_m cells. Regulated by the gain-bandwidth product limit, the G_m-C filter is therefore designed with no gain to extend its bandwidth to 250 MHz. However, the PVT process variation might cause bandwidth change significantly. G_m-C calibration circuit is necessary to reduce impact on the cutoff frequency of the channel selection filter.

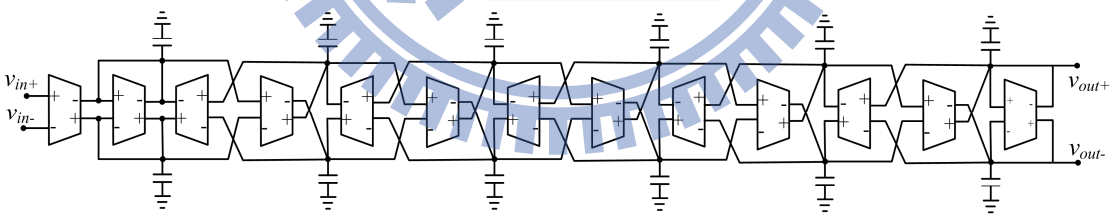


Figure 4-15: The 6th–order G_m-C filter.

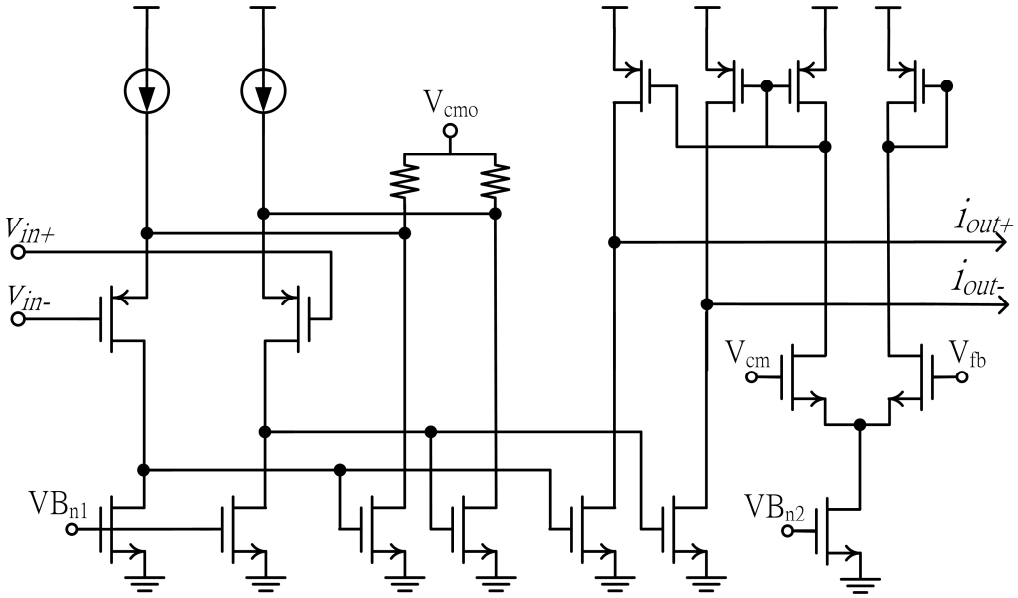


Figure 4-16: The schematic of G_m cell in G_m-C filter.

Calibration circuits are integrated to tune the capacitors arrays against the variation. The main issue is accurate implementation of the time constant (G_m/C). In [29], the time constant is tuned automatically by varying G_m. The analog-type tuning method is sensitive to noise and consumes much power. Instead, digital-type control of passive component C is chosen.

Figure 4-17 shows the architecture of the G_m-C calibration loop adopted in this design. The G_m-C calibration loop consists of a G_m cell, a capacitor array, a comparator and a digital controller. The G_m cell and the capacitor array are identically matched to those used in the filter chain. An accurate reference clock signal is used to control a MOS switch between DC voltage source (V_2) and the G_m cell output to decide the charging time of the capacitor array. The G_m cell output voltage (V(t)) is compared to a reference voltage (V_{ref}) corresponding to the desired G_m/C time constant. By the algorithm of successive approximation (SAR) search, the digital controller controls the capacitor array to an appropriate setting according to the comparator output result. In this control loop, the output voltage of the G_m cell in the

time domain is governed by

$$V(t)=\int_0^t e^{-\frac{1}{\frac{g_m}{C}(V_1-V_2)}t}\,dt+V_2\,. \tag{4.20}$$

Figure 4-18 shows an example of the timing diagram of CLK, CLKz and V(t) during the calibration. Initially, the capacitor array is set as <1 0 0 0> , CLK is high, and V(t) is charged to V_2. When CLK becomes low, V(t) is further charged with the time constant of G_m/C as indicated in (4.20). If C is too small, V(t) is eventually higher than V_{ref} as CLK turns from low to high, or vice versa. It takes four clock cycles for the digital controller to process SAR search to set the capacitor array to the appropriate result. Consequently, the capacitor array is calibrated to achieve the desired G_m/C time constant.

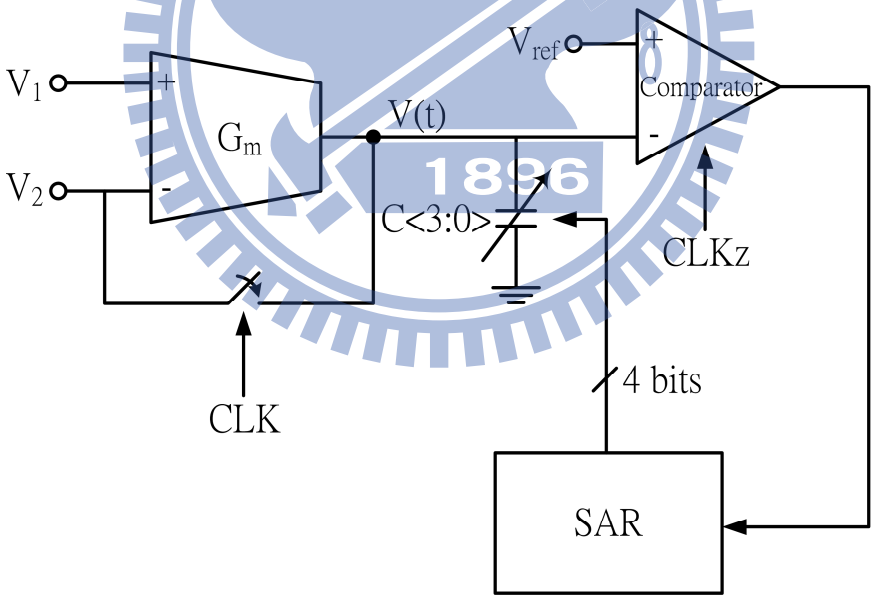


Figure 4-17: The architecture of G_m–C calibration loop.

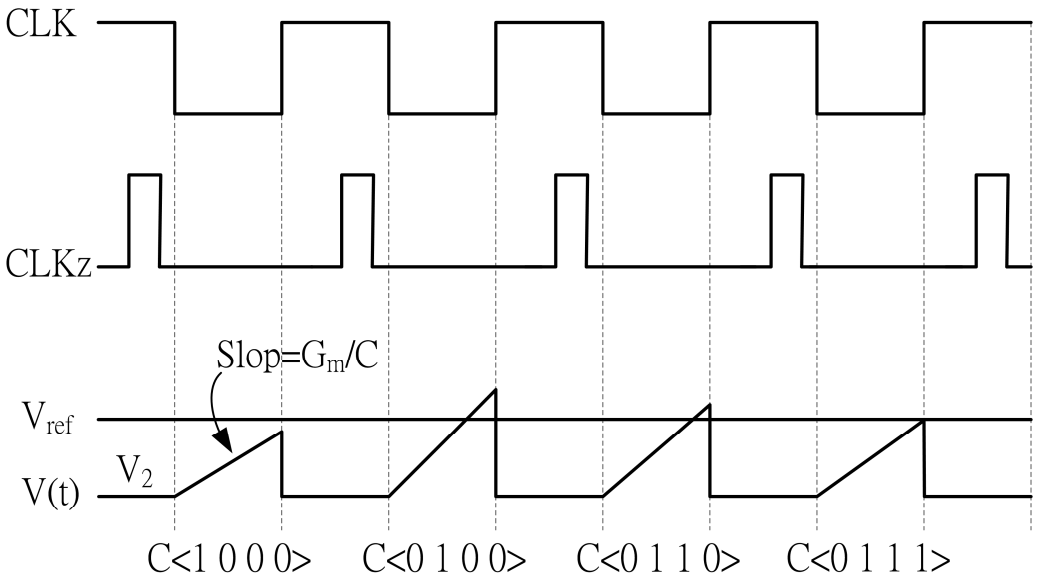


Figure 4-18: Timing diagram of G_m–C calibration.

4.2.3 DC-Offset Calibration

The issues of balanced current amplifiers are poor IP2 performance owing to DC-offset in the circuits. As shown in Figure 4-19, a typical balanced current amplifier is with an input-referred DC-offset current, I_{offset}. Therefore, the received input currents i_{in+} and i_{in-} to the amplifier can be described as

$$i_{in+} = I_{offset} + A \cdot \cos(wt), \qquad i_{in-} = A \cdot \cos(wt + 180^{\circ}) \tag{4.21}$$

Circuit non-linearity will lead to output current, i_{out} as

$$i_{out} = a + b \cdot i_{in} + c \cdot i_{in}^2 + d \cdot i_{in}^3 + \ldots \tag{4.22}$$

The balanced output of the current amplifier can be derived as

$$i_{out+} - i_{out-} = \ldots d \cdot 3 \cdot I_{offset} \cdot A^2 \cdot (1 + \cos(2wt)) + \ldots \tag{4.23}$$

It indicates that DC-offset current results in the second-order distortion at the output of the balanced current amplifier. Consequently it is uncommon in literature that cascading current amplifiers for high-gain and wide dynamic range applications.

Another second-order linearity issue is poor IP2 performance due to absence of common current biasing for the balanced branches in typical circuit implementation. In [30], a digital calibration scheme had been proposed for calibrating IIP2 of a down-conversion mixer. Here, the critical second-order distortion issue in the analog baseband is tackled by using a digitally-assisted DC-offset calibration. The digital technique benefits in circuits and substrate noise immunity, low power consumption and fast settling time.

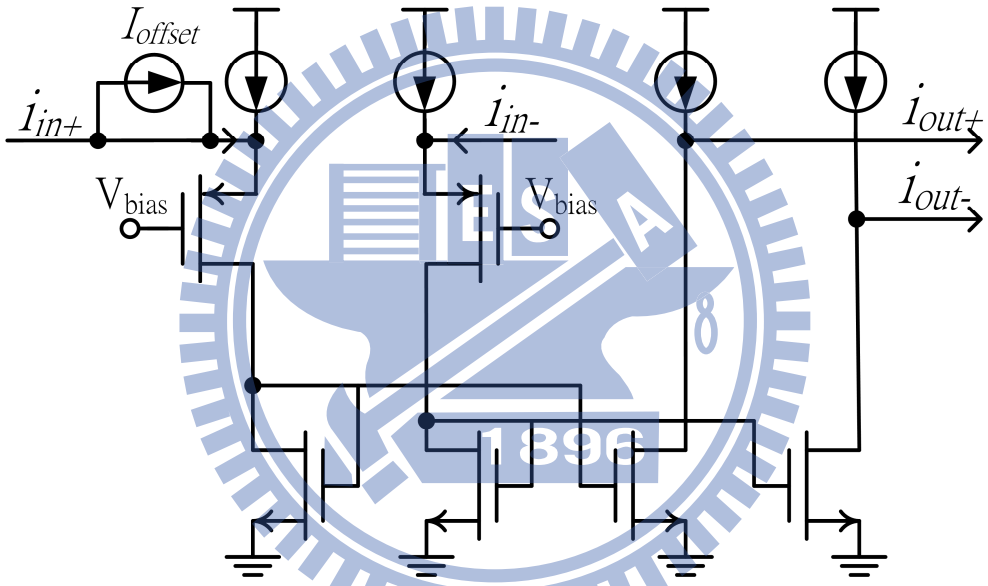


Figure 4-19: A typical balanced current amplifier with an input referred DC-offset current.

As shown in Figure 4-7, the digitally-assisted DC-offset calibration consists of a 1-bit quantizer, one digital control logic unit and digital-to-analog converters (DACs). DC-offset current in the current-mode PGA is converted to DC-offset voltage at the PGA output by the equivalent output resistance. Therefore, DC-offset of balanced branches in the PGA can be sensed by a voltage-mode 1-bit quantizer as shown in Figure 4-20. The 1-bit quantizer is composed of an auto-zeroing amplifier and a latch. The auto-zeroing amplifier eliminates its own DC-offset in half of a clock period and

then amplifies the DC-offset of balanced branches in another half of a clock period. The latch converts the output of the auto-zeroing amplifier into a 1-bit digital code. To save the time consumed by the DC-offset calibration, the auto-zeroing amplifier and the latch work as a pipeline in time domain. That is, as the latch works, the auto-zeroing amplifier performs self DC-offset elimination to prepare for sampling next incoming DC-offset.

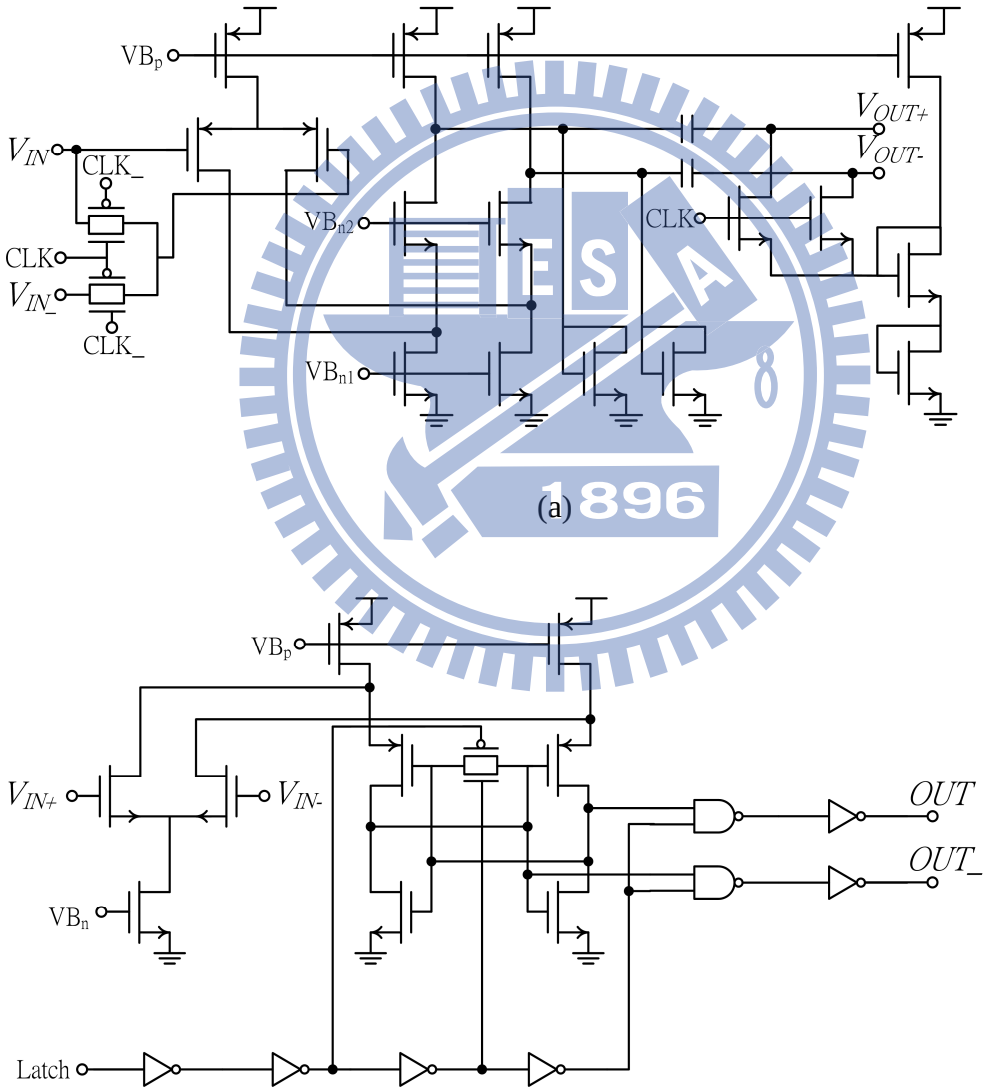


Figure 4-20: The schematic of 1-bit quantizer (a) Auto-zeroing amplifier (b) Latch.

The DC-offset calibration range and resolution are dependent on number of bits and LSB current of DAC, respectively. An 8-bit balanced DAC based on a current-steering structure is connected to the balanced branches of the PGA. The schematic of the DAC is shown in Figure 4-21. The DAC steals current from PGA to eliminate DC-offset of its balanced branches. Initially, the DAC is set in the middle code as <1, 0, 0, 0, 0, 0, 0, 0>, which leads to steal one more LSB current from one of balanced branches of PGA. The digital control logic performs successive approximation (SAR) search to set the DAC according to the output of the 1-bit quantizer.

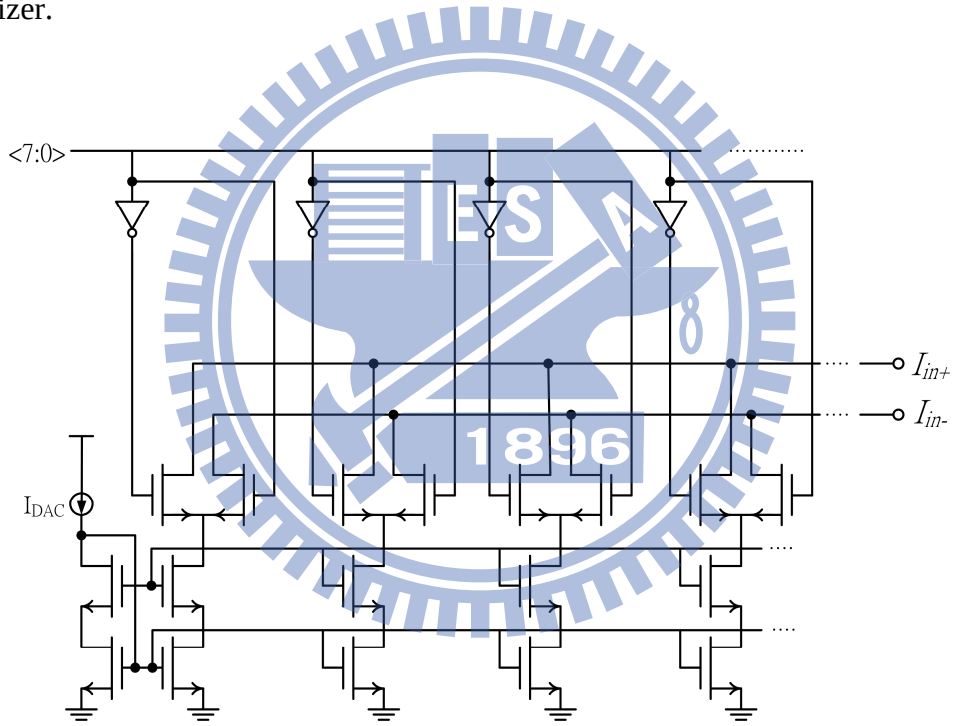


Figure 4-21: The schematic of 8-bits differential DAC.

Figure 4-22 shows an example of the DC-offset calibration procedure. Initially, the DAC is set as <1, 0, 0, 0, 0, 0, 0, 0>. Then, the output of the 1-bit quantizer is '0', which means output DC at the '-' branch of PGA is higher than that of the '+' branch. For eliminating the DC-offset, by SAR method, the DAC is re-set as <0, 1, 0, 0, 0, 0, 0, 0> by the digital control logic unit. This means that the DAC steals more current

from the ‘-’ branch of PGA (less current from the ‘+’ branch of PGA). After that, the output of the 1-bit quantizer becomes ‘1’, which means output DC at the ‘-’ branch of PGA is lower than that of the ‘+’ branch. Then, the DAC is re-set as <0, 1, 1, 0, 0, 0, 0, 0> by the digital control logic unit to steal more current from the ‘+’ branch of PGA, and so on. After the eight bits of DAC are set, the DC-offset of the PGA is calibrated to the minimum DC-offset limited by the LSB current of DAC, which consumes time of eight clock cycles. As the reference clock of 33MHz is used, the time consumed by calibrating DC-offset of one stage of PGAs only needs 0.25 μs.

In the analog baseband, the DC-offset calibration is performed in PGAs which amplify DC-offset and second-order nonlinearity. However, the 6^{th}-order Chebyshev low-pass filter designed with no gain doesn’t need to calibrate it’s DC-offset. The DC-offset calibration carries out by starting from the first PGA stage of the analog basebband and ending at the last PGA stage. Initially, the DC-offset calibration is performed as the receiver is power-on and before receiving the first symbol of data. Due to DC-offset varies with temperature, DC-offset calibration needs to be re-executed in the time slot of transmission (transmitter is working and receiver is idle) as obvious temperature variation is detected.

In MB-OFDM UWB, fast frequency hopping is adopted within three bands in a band group to interleave interference in time domain. Changing LO frequency will lead to DC-offset variation in the input of analog baseband, which needs individual DAC to recode DC-offset corresponding to different LO frequency. Therefore, as shown in Figure 4-7, there are three DACs used in the first stage of the analog baseband. As frequency hopping, the DAC corresponded to the frequency channel is switched for compensating the DC-offset. Frequency hopping is required to be performed within 9.5ns in MB-OFDM UWB. The switching time between DACs can fulfill the strict requirement. Every PGA stage unless the first PGA uses one DAC for

recoding results of DC-offset calibration. Totally, 16 DACs are used for calibrating two-phase (I-phase and Q-phase) of the analog baseband. Therefore, the calibration procedure can be completed within 4 μs.

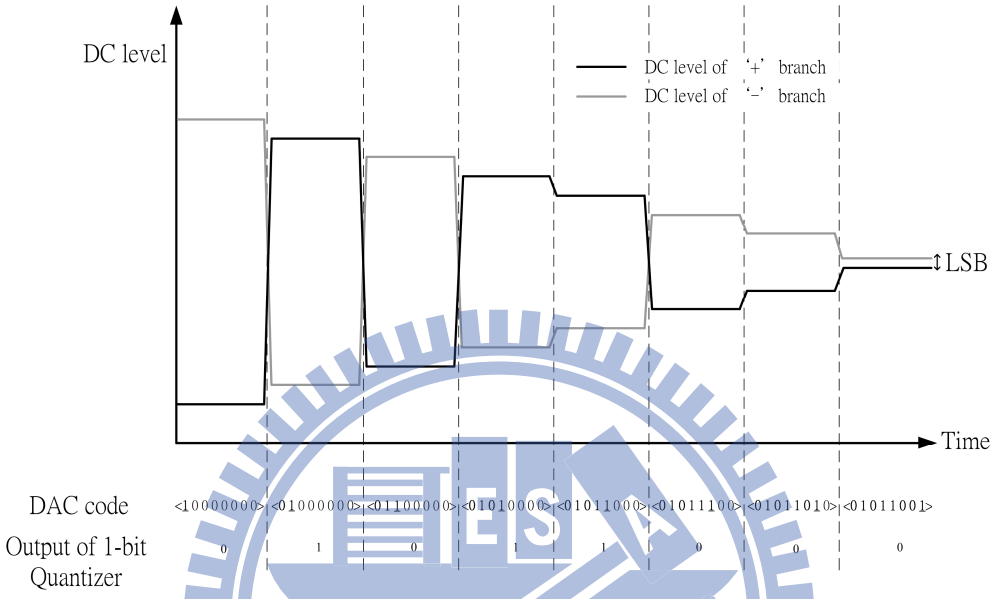


Figure 4-22: An example of the successive approximation (SAR) DC-offset calibration.

Chapter 5

Circuit Design of Transmitter

5.1 IQ Modulator

Figure 5-1 shows the schematic of the IQ modulator. For low voltage operation, a folded configuration is adopted to ensure sufficient voltage headroom for trans-conductor and switching cells. In order to increase linearity of the modulator, the input trans-conductor cells are designed with resistive degeneration. The modulator load is shunt inductive peaking with on-chip series resistor and inductor to form a load. This shunt peaking load is preferred to obtain the wide bandwidth requirement of 3~8GHz.

DC-offset in the IQ modulator leads to unwanted carrier leakage, which saturates receivers. The main DC-offset contributors are trans-conductor cells and bias current sources of the modulator. The input-referred DC-offset due to trans-conductor cells had been formulated as follows, [21]

$$V_{in,offset} = \Delta V_{th} + \frac{V_{ov}}{2} \times \frac{\Delta\left(\frac{W}{L}\right)}{\frac{W}{L}} + \frac{IR_s}{2} \times \frac{\Delta I}{I} \qquad (5.1)$$

where W/L, V_{th}, I and V_{ov} are the device size, threshold voltage, bias current and over-drive voltage of the trans-conductor cells (M1-M4), respectively. R_s denotes the degenerative resistance, R1 and R2.

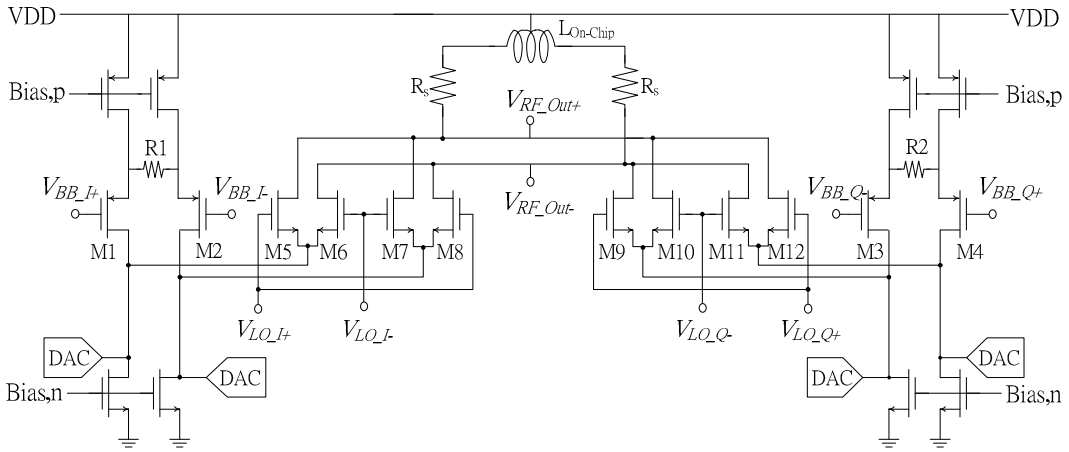


Figure 5-1: Schematic of the IQ modulator.

In the trans-conductor cells, the effect of transistor size mismatch is amplified by over-drive voltage (V_{ov}) and then is divided by two. Threshold voltage mismatch directly contributes DC-offset. These problems can be improved by using large transistors to decrease V_{ov} and a well-matched layout to reduce threshold voltage and transistor size mismatch. In the last term of (5.1), resistive degeneration in the trans-conductor cells amplifies the effect of current mismatch. Thus, resistance of degeneration is designed to trade-off between DC-offset and linearity. Mismatch among biasing current sources is alleviated by using large transistors, each with a fixed gate length of 2 μm and a total gate width larger than 500 μm and well-matched layout in this design. The mismatches of the switching cells also introduce carrier leakage. A symmetrical layout for the switching cells is important as well. For additional carrier leakage reduction, the modulator also incorporates a calibration mechanism. The DC-offset calibration function is realized by four eight-bit digital-to-analog converters (DACs). Output currents of these DACs are injected into the modulator bias branches to balance the offset. Figure 5-2 shows schematic of the DACs for carrier leakage calibration.

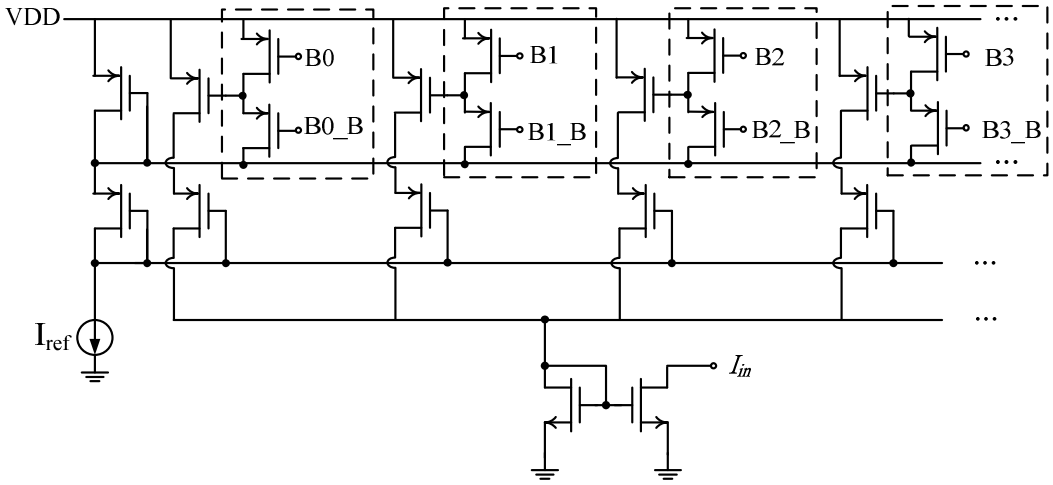


Figure 5-2: Schematic of DAC.

5.2 Variable gain amplifier (VGA)

Figure 5-3 depicts the schematic of the linear-in-dB variable gain amplifier (VGA). It consists of a cascode differential amplifier (M6-M7) with inductively peaked resistive loads to broaden the output bandwidth. Continuous analog gain control is achieved by current steering cells (M8-M11), controlled by a voltage transformation circuit (M1-M5 and R1) that regulates the input control voltage (V_{ctrl}). In order to realize linear-in-dB power control, the voltage transformation circuit translates the input control voltage exponentially to Vc as [31]

$$VDD - V_c = e^{K \cdot V_{ctrl}} \tag{5.2}$$

where K is $R_1 \cdot \mu_n \cdot Cox \cdot \left(\frac{W}{L}\right)_1$.

Current gain of the current steering cells (M8-M11) is tuned by Vc as

$$G_i = \frac{W_8}{W_9 \cdot (VDD - V_s - V_{th})} \cdot (VDD - V_c) \tag{5.3}$$

Therefore, according to (5.2) and (5.3), voltage gain of the RF VGA is expressed by

$$G_v = \frac{Z_L \cdot W_8}{W_9 \cdot (VDD - V_s - V_{th})} \cdot e^{K \cdot V_{ctrl}} \tag{5.4}$$

Owing to the current steering adopted in the cascade stage, constant bias current in the input stage (M6-M7) avoids linearity degradation during gain variation.

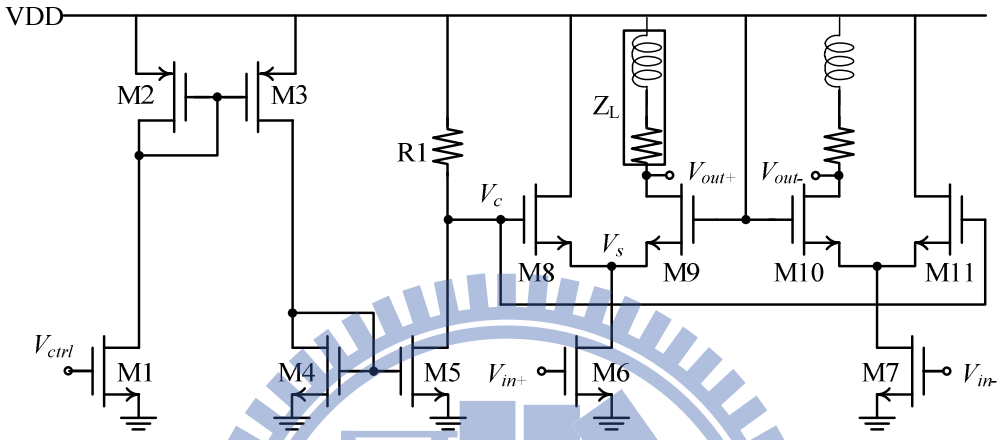


Figure 5-3: Schematic of variable gain amplifier.

5.3 Differential to single-ended (D-to-S) amplifier

A broadband gain buffer is used to perform the differential to single-ended conversion, as shown in Figure 5-4. The inductor serves as a shunt peaking component for the common-source stage (M1) and also as a series peaking element for the source follower (M2). Due to the unequal amplification of the positive and negative paths, the differential-to-single-ended conversion does not double the signal swing.

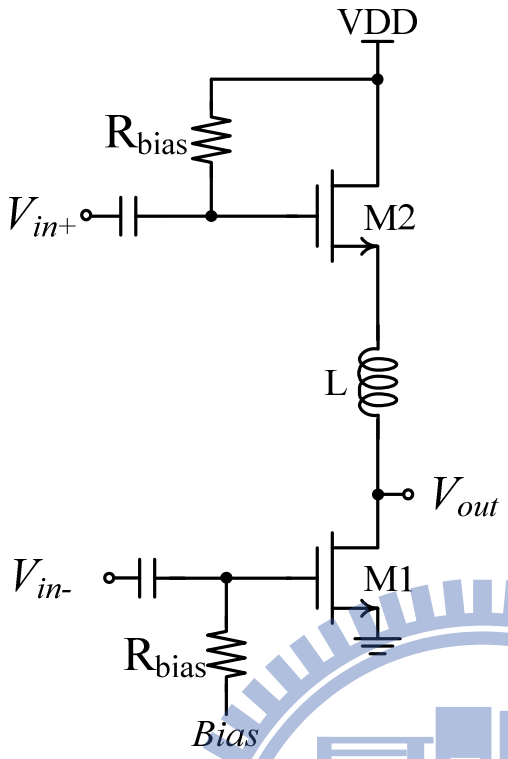


Figure 5-4: Schematic of the D-to-S voltage amplifier.

From the point of view of the incoming signal V_{in+}, the behavior of the D-to-S amplifier acts as a source follower. The equivalent circuit of the D-to-S amplifier is shown in Figure 5-5. On the contrary, from the point of view of the incoming signal V_{in-}, the D-to-S amplifier performs a common source amplifier with an inductive shunt peaking load. The M2 forms an equivalent resistor with resistance of $1/g_{m2}$ to reduce quality factor of the inductor for enlarge bandwidth. To equalize gain of the two paths from 3GHz to 8GHz, the following equation should be sustained.

$$\left|\frac{r_{o1}\,//\,\frac{1}{S\cdot C_L}}{\frac{1}{S\cdot C_L}\,//\,\frac{1}{g_{m2}}+S\cdot L+r_{o1}\,//\,\frac{1}{S\cdot C_L}}\right|=\left|\frac{g_{m1}}{1+S\cdot L_{bw}\cdot g_{m1}}\cdot\left[\left(\frac{1}{g_{m2}}+S\cdot L\right)//\,r_{o1}\right]\right| \qquad (5.5)$$

Where C_L is output loading capacitor, L_{bw} is bonding wire connected between source of M1 and ground. r_{o1} is output resistance of M1, g_{m1} and g_{m2} are trans-conductance of M1 and M2, respectively. Ideally, the output of source follower is equal phase to

the input and the output of common source amplifier has 180 degree phase rotation from input. Therefore, the incoming signals V_{in+} and V_{in-} will be in-phase at output of the D-to-S amplifier. But the parasitic capacitors and on-chip inductor cause phase rotation as they are charged and discharged by signals. The inductor causes opposite phase rotation from the parasitic capacitors, which compensates phase error caused by the parasitic capacitors. Therefore, by post-simulation, a gain error of 1dB and a phase error of 10 degree are obtained up to 8GHz by careful choosing size of MOS transistors (M1-M2) and on-chip inductor. The error is acceptable in this design.

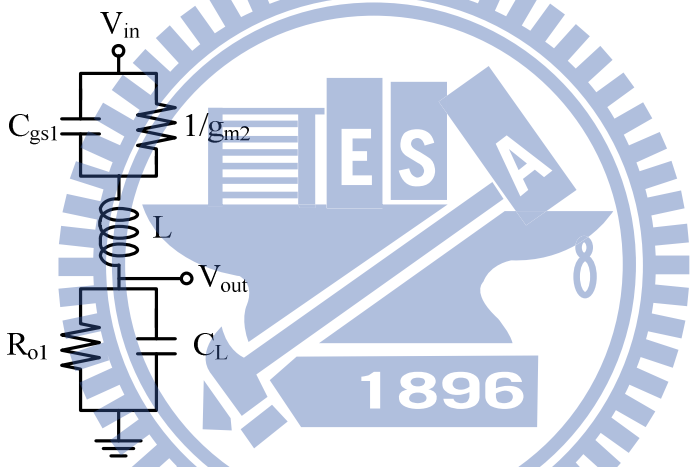


Figure 5-5: Equivalent circuit model of the D-to-S amplifier.

5.4 Power amplifiers

In design of the power amplifier (PA), it is difficult to achieve high linearity and a broadband output matching across 3GHz-8GHz, as well as low power consumption simultaneously. Three approaches have been commonly used for broadband PA design, including filter theory design, distributed amplifiers and resistive shunt-feedback [32]. Using filter theory design, LC-based networks help achieve wideband matching. However, multiple LC stages might be necessary to cover broad bandwidth such that

they usually occupy a substantial die area. Distributed amplifiers have high linearity, but their power consumption and occupied area can be quite high. In the approach of resistive shunt-feedback, the feedback resistor can lead to gain degradation.

To overcome these difficulties, the proposed power amplifier is realized by CMOS (both PMOS and NMOS) configuration, as shown in Figure 5-6. By using appropriate size of transistors, the parallel combination of the output impedances of the NMOS and PMOS transistors provides a low resistance, which is wideband conducive to 50Ω. Owing to large voltage swing in the output of the power amplifier, the NMOS and PMOS transistors are forced to operate in the triode region in the negative cycles and positive cycles of the output waveform, respectively as shown in Figure 5-7. In the negative cycles (Figure 5-7(a)), the PMOS transistor plays a role of trans-conductor and the NMOS transistor operated in triode region serves as a resistive load. On the contrary, in the positive cycles, the NMOS transistor plays a role of trans-conductor and the PMOS transistor operated in triode region serves as a resistive load. The output resistance of the power amplifier can be derived as output waveform in positive cycles and in negative cycles, separately.

$$r_{out} = r_{triode,p} // r_{o,n}$$
$$\approx \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p \left(V_{GS,p} - V_{in,rms} - V_{th,p}\right)} = \frac{1}{g_{m,p}} \text{ , in positive cycles.} \quad (5.6)$$

$$r_{out} = r_{o,p} // r_{triode,n}$$
$$\approx \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left(V_{GS,n} + V_{in,rms} - V_{th,n}\right)} = \frac{1}{g_{m,n}} \text{ , in negative cycles.} \quad (5.7)$$

The equivalent output resistance of the power amplifier is $1/g_{mp}$ and $1/g_{mn}$ in

negative and positive cycles of the output waveform, respectively.

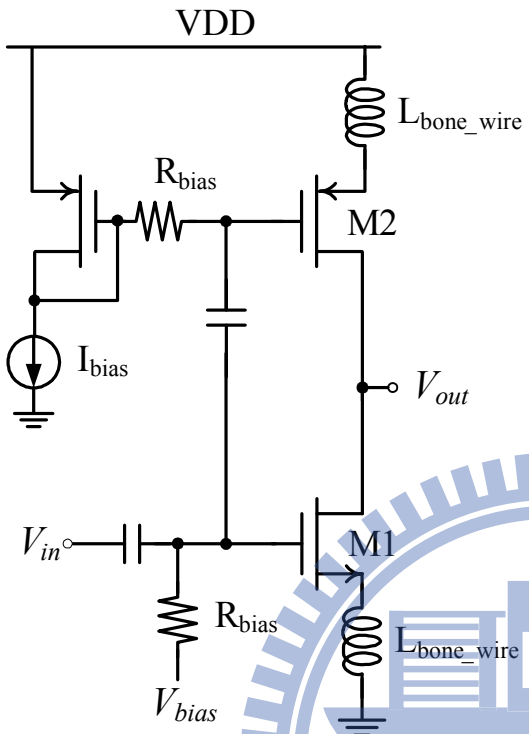


Figure 5-6: Schematic the wideband power amplifier.

The equivalent model of the power amplifier is shown in Figure 5-8. C_1 is parasitic capacitance as

$$C_1 = C_{bp} + C_{d1} + C_{d2} \tag{5.8}$$

C_{bp} denotes the parasitic capacitance of a bonding pad. C_{d1} and C_{d2} are drain capacitor of M1 and M2, respectively. In the model, bonding wires (L_{bw}) connected to the equivalent resistance of M1 and M2 in the triode region form an inductive shunt peaking load. Let L_{bw}=1nH, , C_1=C_{load}=1pF and R_{triode}=20Ω. The simulated frequency transfer function peaks at 8GHz to extend operation frequency of the power amplifier, as shown in Figure 5-9. The CMOS configuration of the power amplifier has wider linear operating range for processing signals with large voltage swing. Low resistance

load also helps to reduce voltage swing at the power amplifier output. Those properties all lead to better linearity performance.

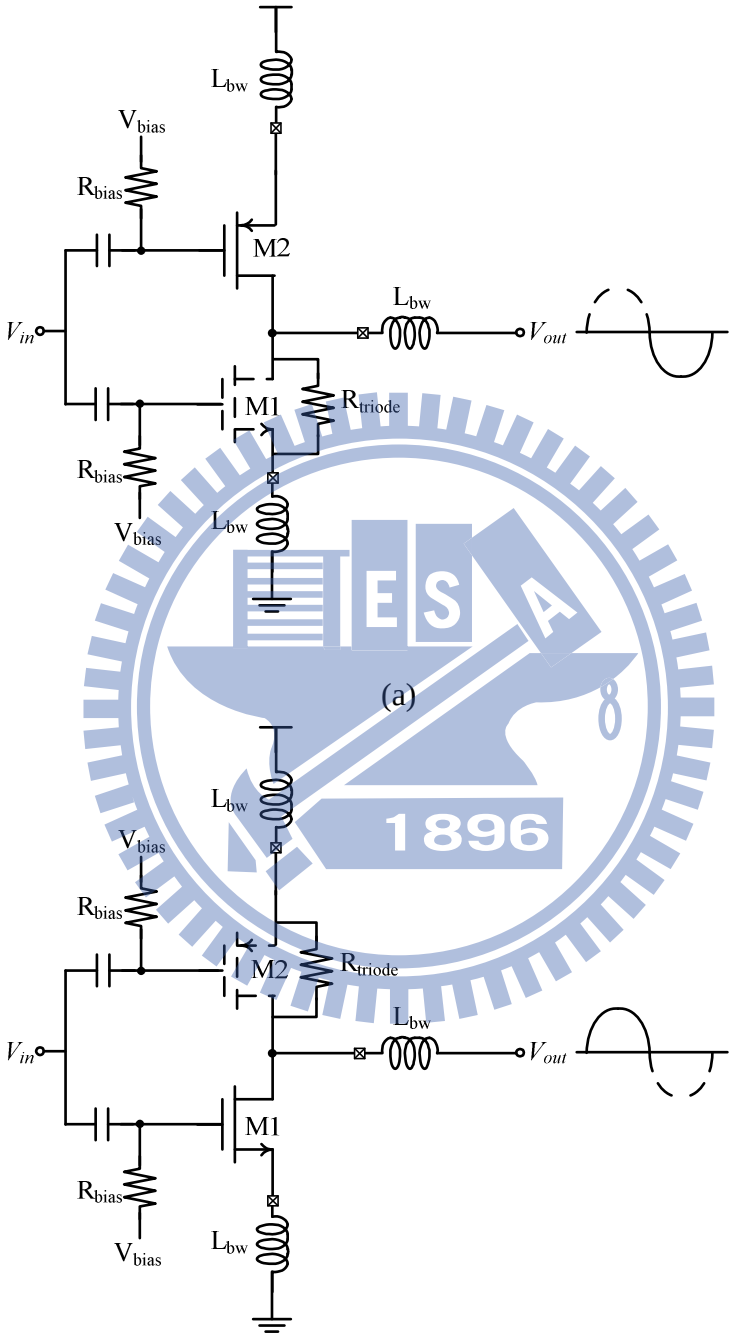


Figure 5-7: Power amplifier operates in (a) negative cycles of output waveform (b) positve cycles of output waveform.

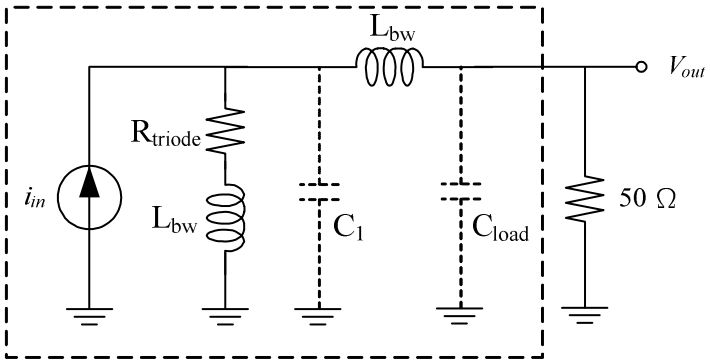


Figure 5-8: Effective model of the power amplifier.

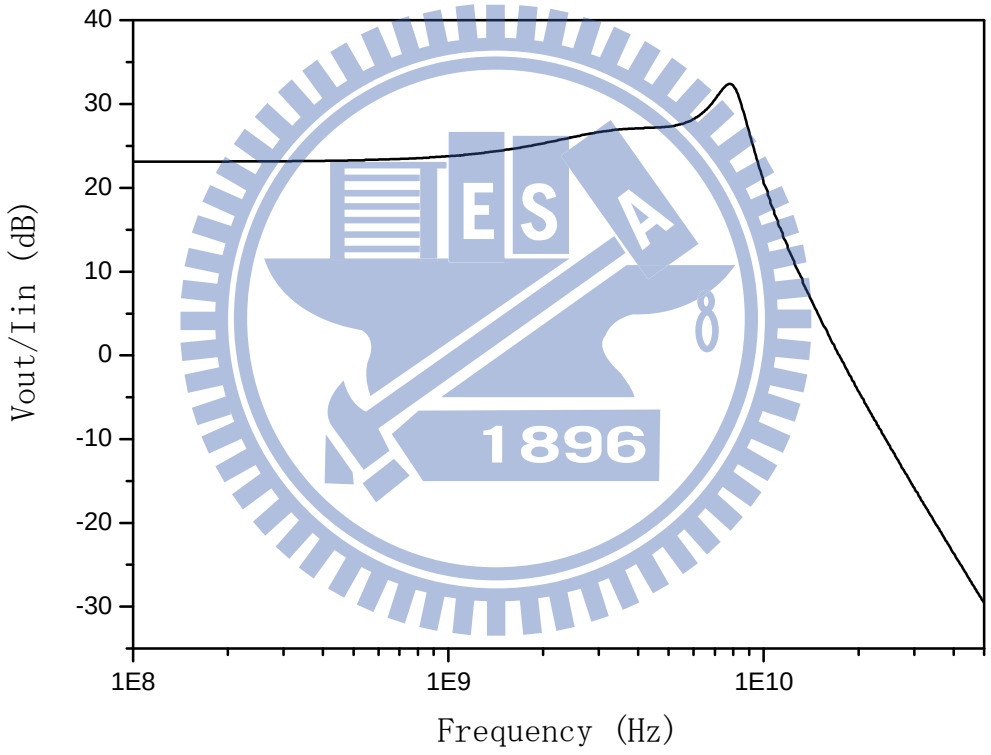


Figure 5-9: Simulated frequency transfer function of the power amplifier.

The proposed wideband power amplifier realized by the CMOS configuration with wideband output matching to 50Ω, high-linearity and small occupied chip area is addressed. The power amplifier also features low power consumption. As shown in Figure 5-10, the power amplifier consumes 9.6mW, which is only 15% of the power

consumption of the entire RF transmitter.

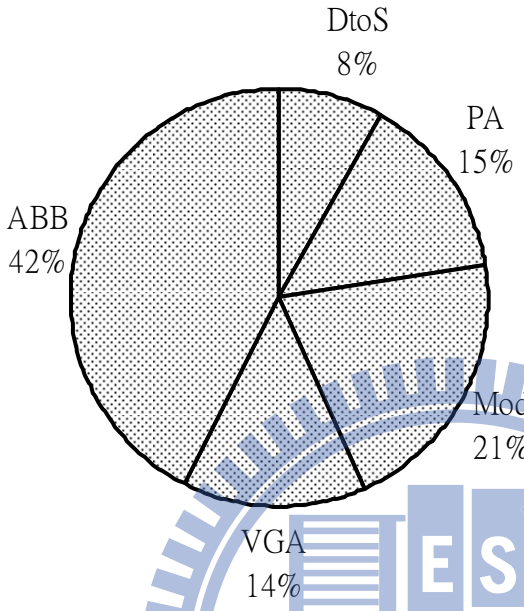


Figure 5-10: Distribution of power consumption in the RF transmitter.

5.5 Transmitted signal strength indicator (TSSI)

In Figure 5-11, an on-chip transmitted signal strength indicator (TSSI) is implemented to measure the transmitter output power. The TSSI consists of three stages. The first stage is a voltage amplifier (NM1 and R1) that increases the detecting sensitivity. The second stage is a peak detector (NM2 and C2) configured as a source follower with a capacitive load. The equivalent $1/g_{mNM2}$ resistor provided by NM2 is connected in series to the capacitive load (C2) to form a RC rectifier for detecting the rms voltage of the incoming RF signals. NM3 and C3 are used to provide a reference voltage. The third stage is a comparator (NM4-NM5, PM6-PM7 and R2-R3) that compares the rms

voltage of the incoming RF signals with the reference voltage. Finally, PM8 and R4 are used to transform the output current of the comparator into an output voltage.

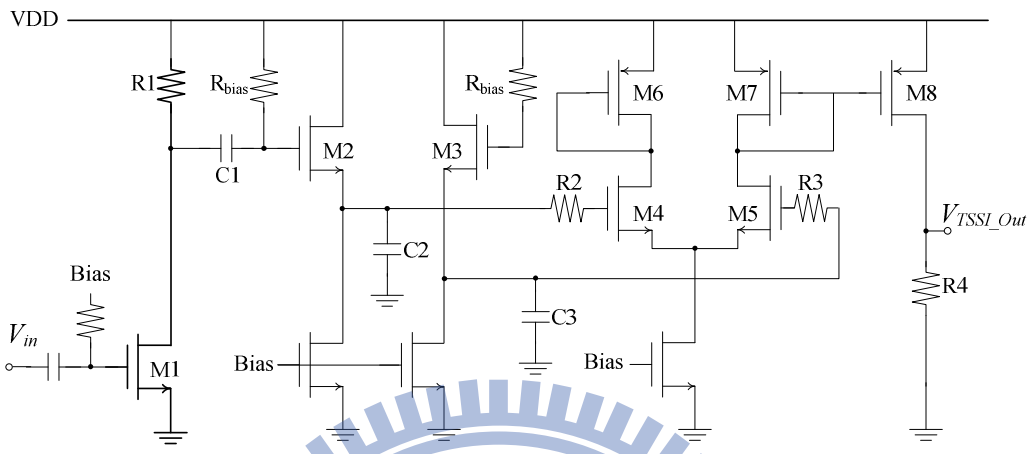


Figure 5-11: Schematic of the TSSI.

Chapter 6

Receiver Measurement

6.1 Low noise amplifier (LNA) and 3th-Order Notch Filter

The fabricated LNA with notch filter was bonded on FR4 PCB and tested by Agilent N5230A network analyzer for S-parameter and by N8975N noise figure analyzer for NF measurement. The chip photo is shown in Figure 6-2. Total current assumption including output buffer and notch filter is 22 mA under 1.2V supply. In Figure 6-2, the measured input return loss (S11) is less than -10dB at frequency range from 2.5 ~ 5.2 GHz and power gain (S21) has 10.75 dB difference at 3.5GHz between high and low gain mode switch. Band switch function is shown in Figure 6-3, the measured power gain is 13.56dB at 3432MHz (LG=0001), 15.86 dB at 3960MHz (LG=1000) and 15.87 dB at 4488MHz (LG=1111). The measured noise figures are 3.9 dB at 3432MHz, 3.19 dB at 3960 MHz and 4.7 dB at 4488MHz. When F_Tune=1.3V, the NF at 4488MHz will be improved by 0.5 dB and notch frequency will move to 5.85 GHz with gain degraded to -24.73 dB as shown in Figure 6-4 and 6-5.

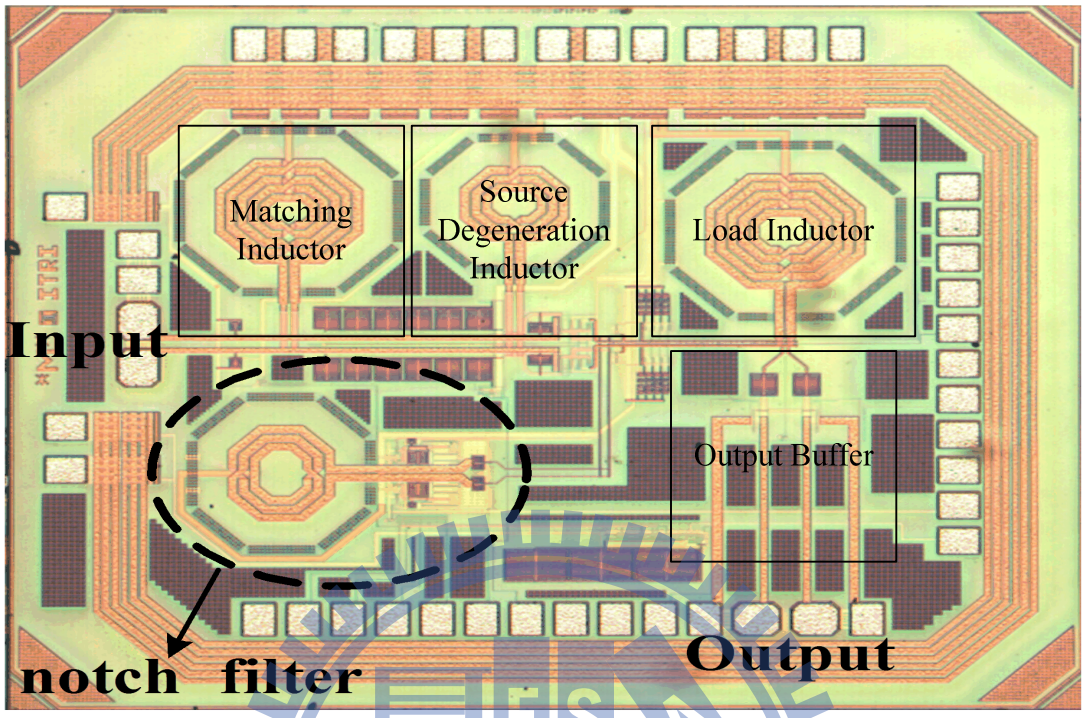


Figure 6-1: Chip photo of the LNA with notch filter.

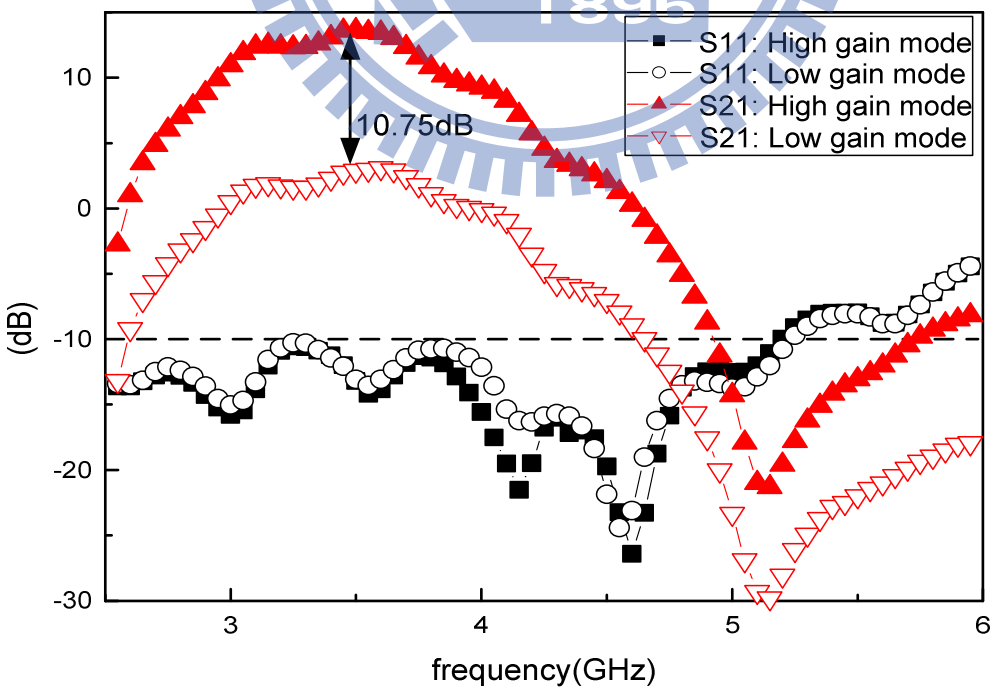


Figure 6-2: Measurement results for input return loss and high/low gain switch.

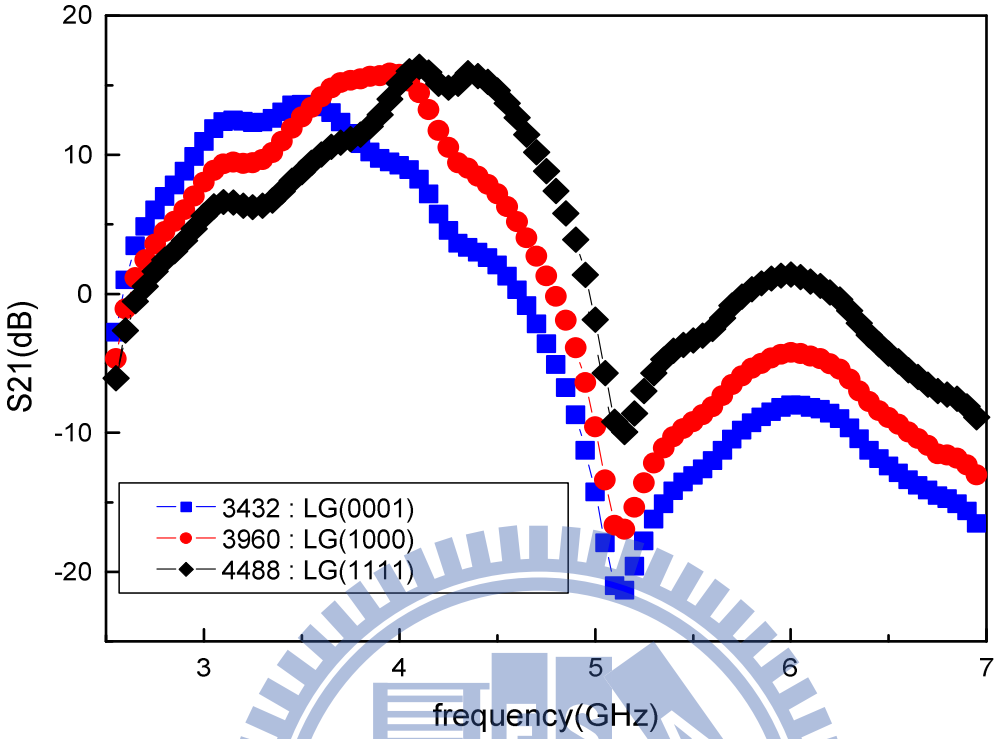


Figure 6-3: Measurement results for band group1 switching.

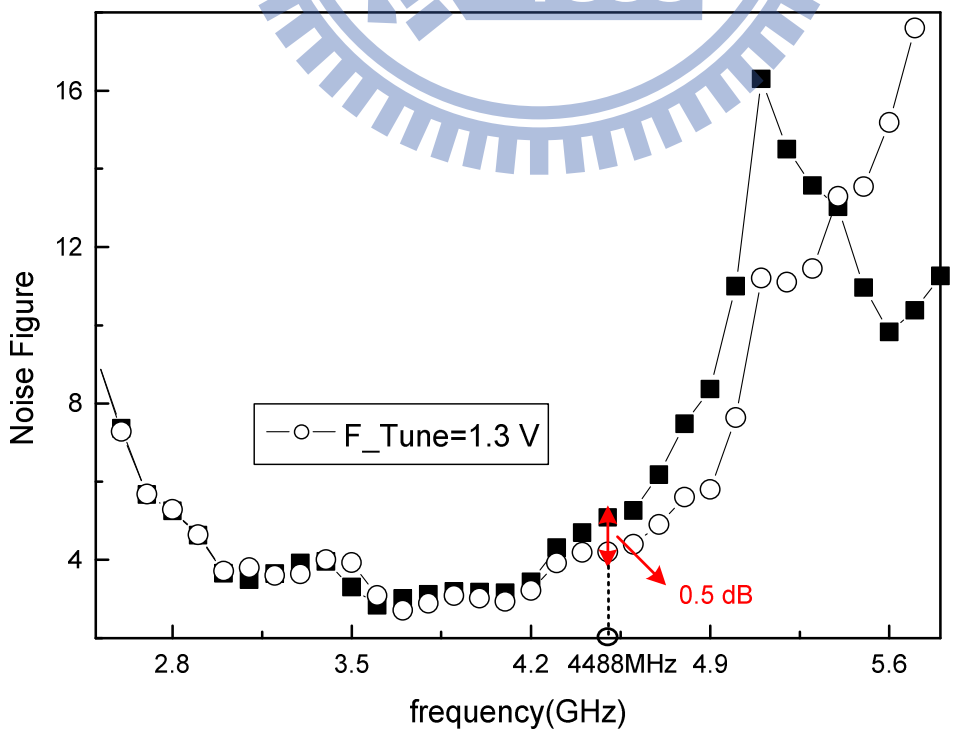


Figure 6-4: Measurement results of NF under different notch frequency.

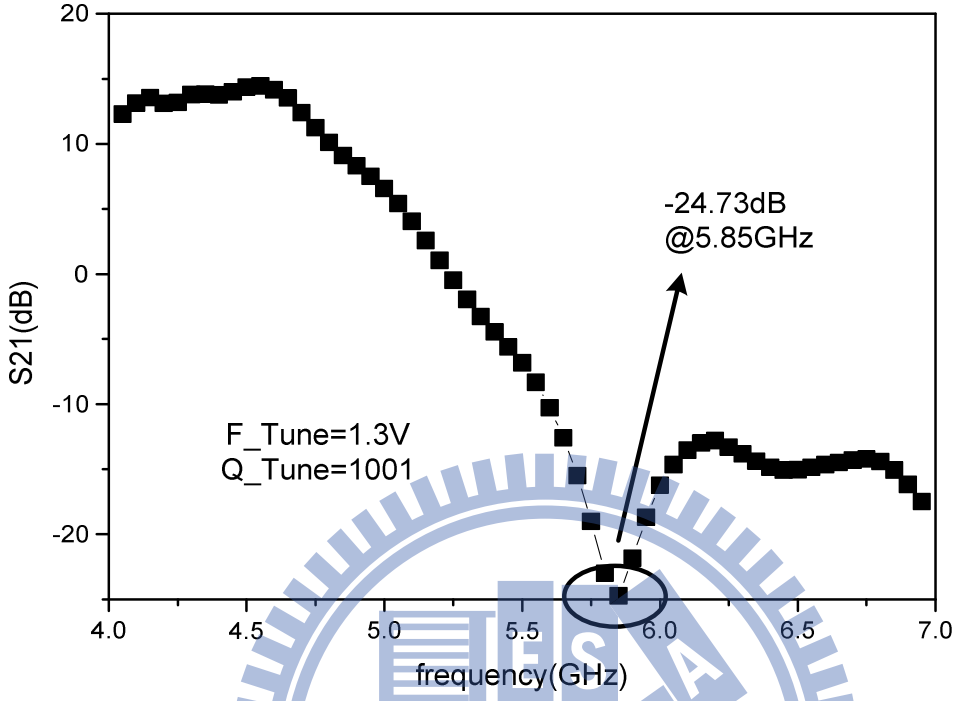


Figure 6-5: Measurement result of highest notch frequency setting.

The nonlinearity of LNA is assembled by input 1-dB compression point (P1dB) and IIP3. The measured P1dB at 4488 MHz are -16.82 / -6.98dBm at high/low gain mode as shown in Figure 6-6. Figure 6-7 shows the improvement value of IIP3 with proposed notch filter under two-tone test (5.25GHz and 5.85 GHz) that represent interference signals of 802.11a WLAN system. The measured IIP3 at 4.65GHz is 4.04 dBm; as notch frequency moves to 5.85 GHz (F_Tune=1.3V), IIP3 becomes 8.74 dBm. So the IIP3 at 4.65 GHz (4488MHz band) can be improved 4.7 dB by the proposed third-order active notch filter. Table IV summarizes the measurement results and compares them with previous wide-band LNA designs. [33] and [34] are the LNA designs with notch filter. There may be some stability problems due to the cross-coupled topology of notch filter, but it doesn't occur in this work. The IIP3 after

improved in this work is 8.74dBm which is 4.14 dB greater than that of [33] and 19.54 dB greater than that of [34]. So the proposed notch filter can be used to improve IIP3 of wide-band LNA successfully under out-band interferences.

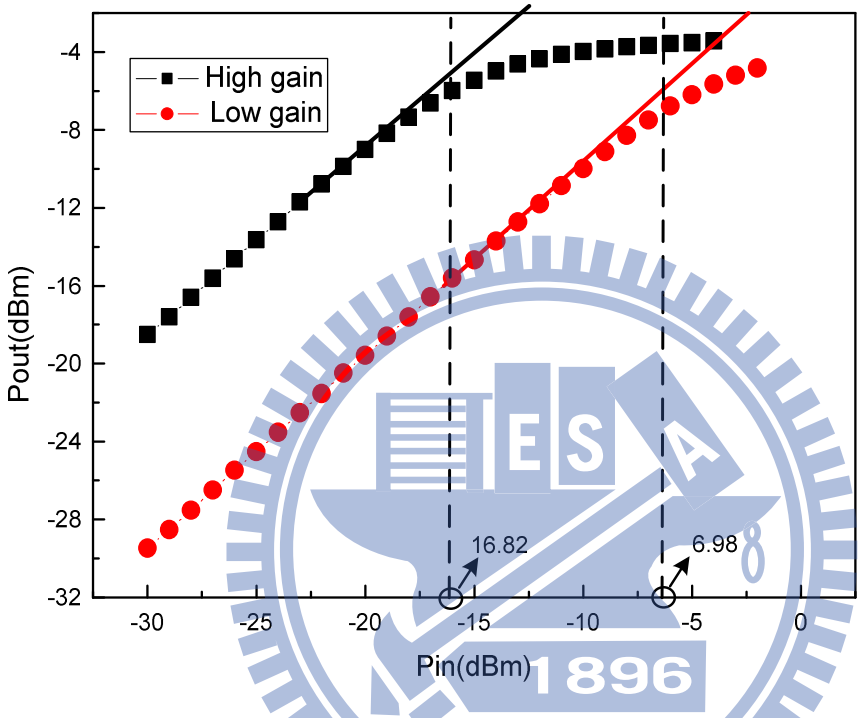


Figure 6-6: P1dB measurement of high gain mode and low gain mode.

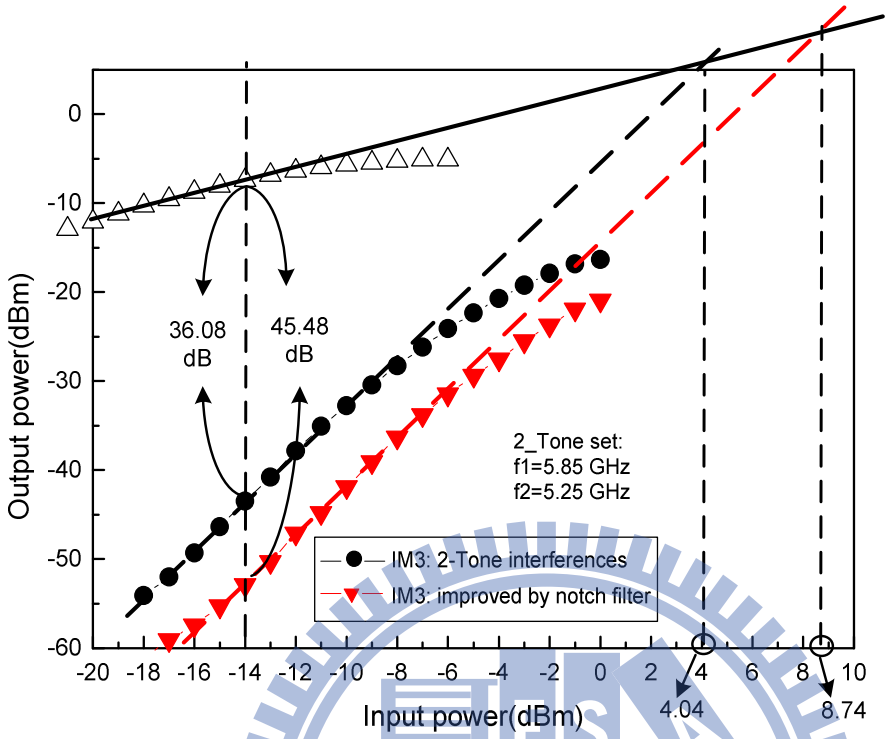


Figure 6-7: Nonlinearity measurement results of IIP3 under out-band interferences test.

TABLE IV. BENCHMARK OF ULTRA-WIDE-BAND LNA DESIGNS

References	[40]MWCL2006	[41]JSSC2004	[42]JSSCC2005	[43]ISSCC2007	[44]RFIC2007			**This work**		
Process	CMOS 0.13μm	CMOS 0.18μm	CMOS 0.18μm	CMOS 0.13μm	CMOS 0.18μm			**CMOS 0.13μm**		
Architecture	LC ladder	LC ladder	Resistive shunt feedback	Inductive-degeneration	Three-stages			**LC ladder**		
Frequency(GHz)	2~4.6	2.3~9.2	2~4.6	3~8.2	3.5	5.5	7.2	**3.43**	**3.96**	**4.49**
S21(dB)	9.5	9.3	9.8	18.5	20	10	15	**13.56**	**15.86**	**15.87**
NF (dB)	3.5	4	2.3	3.5	4	6.2	5.1	**3.9**	**3.19**	**4.7**
S11(dB)	<-10	<-9.9	<-9	<-10	-18	-12	-10.5	**-12**	**-14**	**-20**
P_{DC} (mW)	16.5	9	12.6	31.5	21.6			**26.4**		
IIP3 (dBm)	-0.8	-6.7	-7	4.6 (4.6GHz)	-18.5	-10.8	-15.5	**8.74 (4.65 GHz)**		
FoM (/mW)	-3.6	-2.03	0.3	2.59	4.87	-8.34	-1.83	**-2.27**	**1.3**	**-1.24**

$$\text{ie: FOM} = \frac{|S_{21}|}{|F-1| \cdot P_{diss}}$$

6.2 Analog baseband

The baseband chain has been implemented in a 1.2 V 0.13 μm CMOS technology. The chip micrograph is shown in Figure 6-8. It is embedded in a RF transceiver and occupies 0.8 mm^2. Figure 6-9 shows the measured frequency response of the analog baseband with comparing to the simulated frequency response of the 6th G_m-C filter and the analog baseband (SK LPF+6th G_m-C filter). The measured pass-band edge frequency is 250 MHz with 1 pF of probe capacitance. As shown in Figure 6-10, measured out-band IIP3 (f1=400 MHz, f2=790 MHz) of the filter is -6 dBV under voltage gain of 73 dB and pass-band edge frequency of 250 MHz. The high linearity performance is achieved under 1.2 V supply by the current-mode PGAs and the proposed current-mode SK LPF. Measured in-band IIP2 (f1=40 MHz, f2=50 MHz) of the filter is -59 dBV under voltage gain of 68 dB and pass-band edge frequency of 250 MHz. The measured out-of-band IIP2 (f1=400 MHz, f2=410 MHz) is −5 dBV under the voltage gain of 68 dB and the pass-band edge frequency of 250 MHz (Figure 6-11). Therefore, the issue of current amplifiers indicated by poor HD2 performance is improved by the proposed architecture and the DC-offset calibration. The measured Noise Figure (Figure 6-12) is 12~14 dB within the BW at the maximum gain setting of 73 dB. Performance summary and comparison to [12] are listed in Table V.

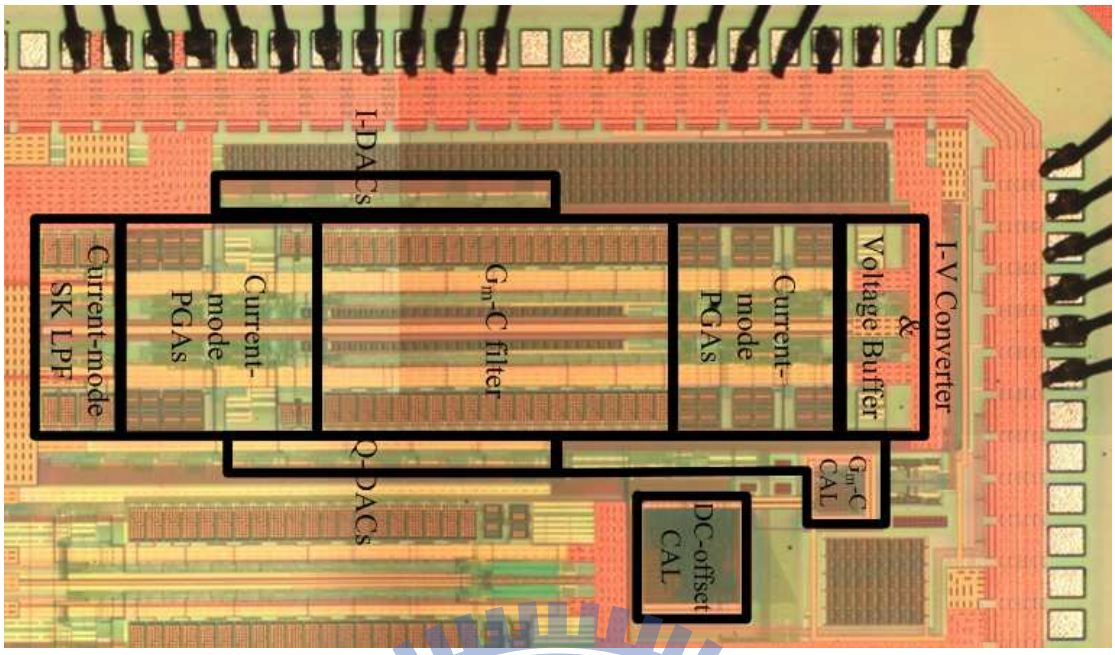


Figure 6-8: Die photo of the baseband chain in 0.13μm CMOS technology. The baseband chain comprises SK LPF, current-mode PGAs, 6th–order Chebyshev G_m-C filter and circuitry for G_m-C and DC-offset calibration.

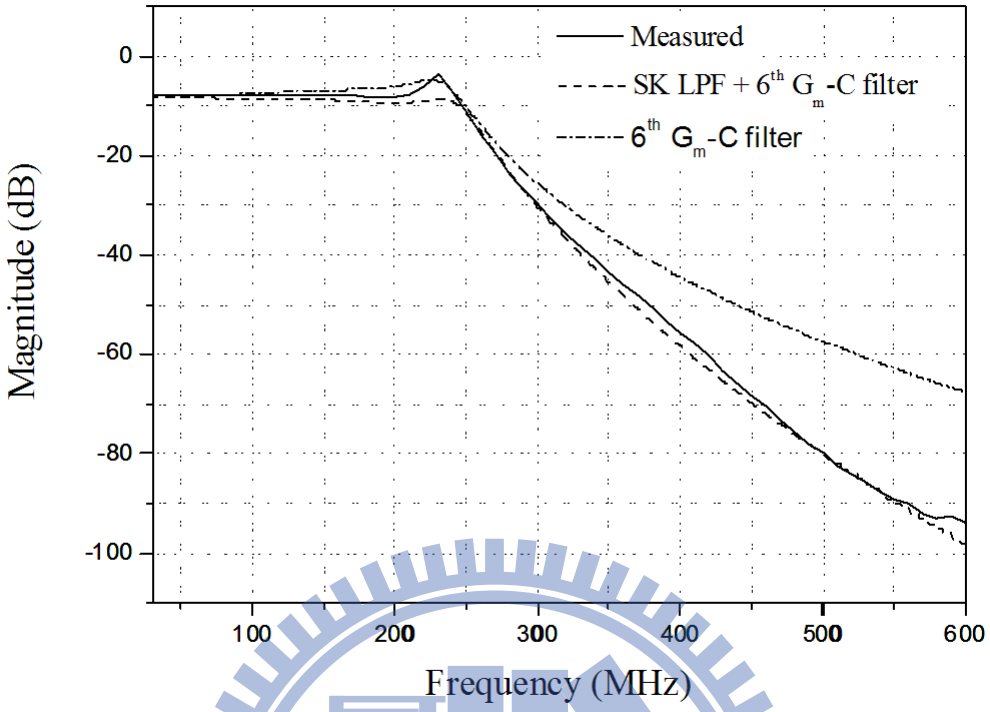


Figure 6-9: Measured frequency response of the baseband chain. The measured pass-band edge frequency can be varying from 250MHz to 300MHz with 1pF of probe capacitance.

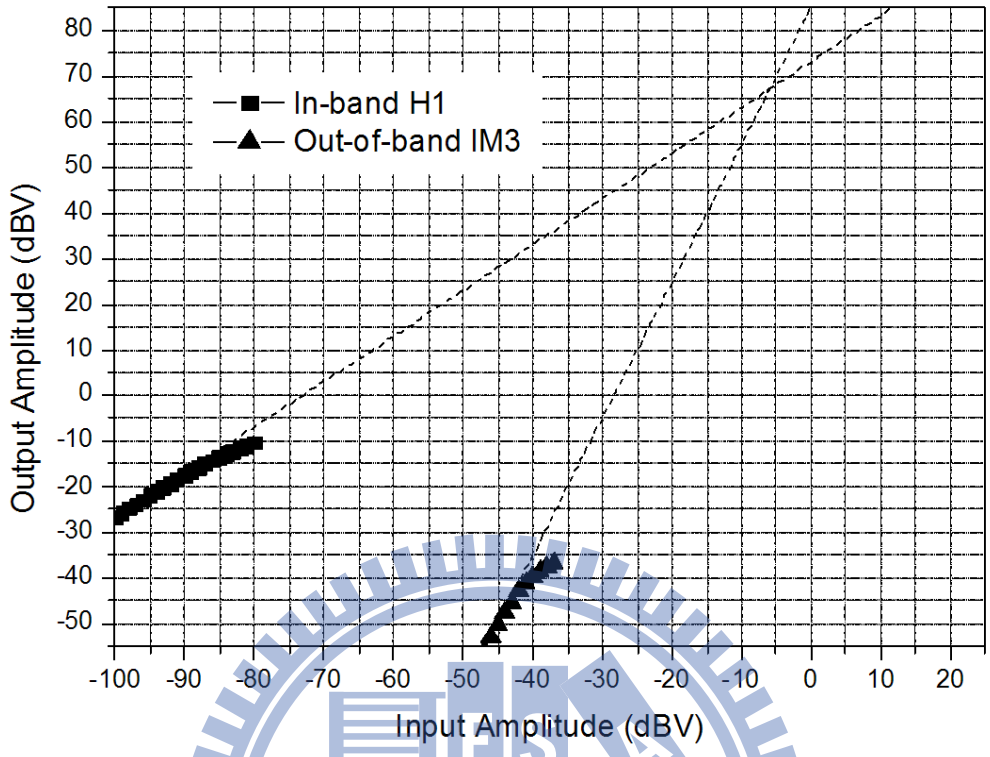


Figure 6-10: Measured out-band IIP3 (f1=400MHz, f2=790MHz) of the baseband chain under voltage gain of 73dB and pass-band edge frequency of 250MHz.

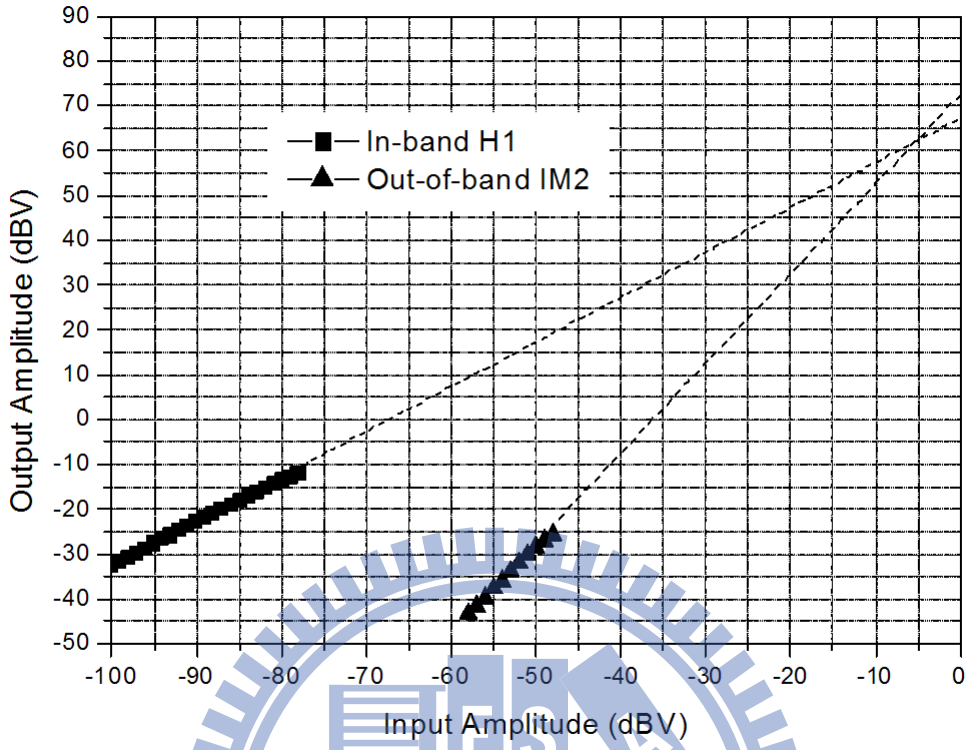


Figure 6-11: Measured out-band IIP2 (f1=400MHz, f2=410MHz) of the baseband chain under voltage gain of 68dB and pass-band edge frequency of 250MHz.

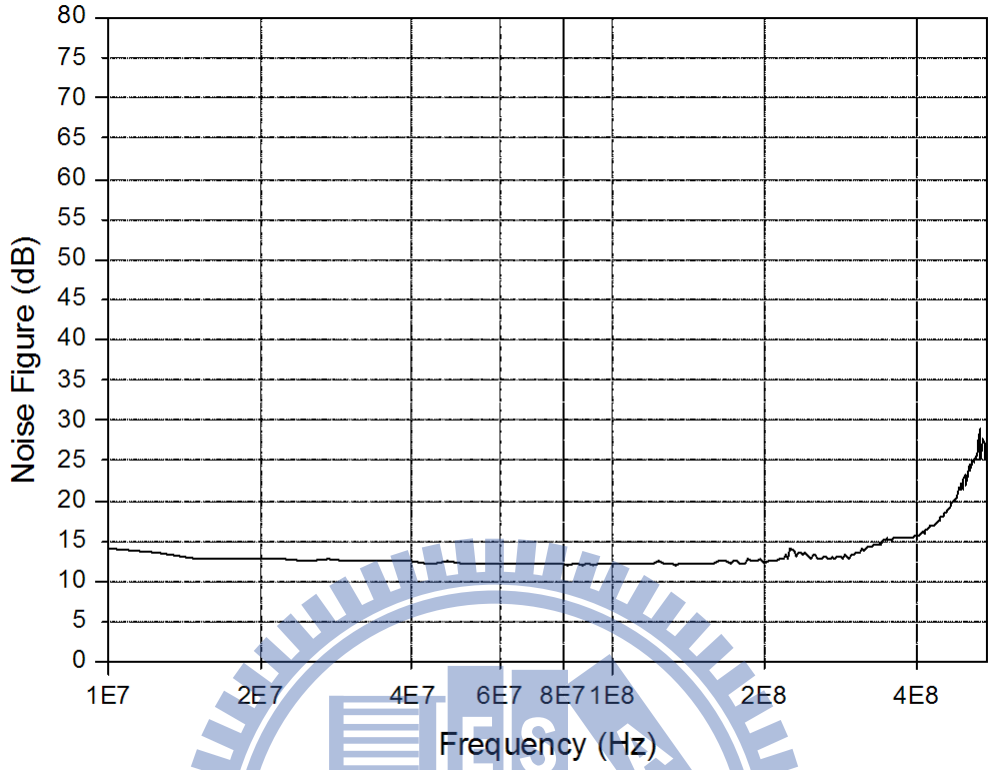


Figure 6-12: Measurement noise figure of the baseband chain under voltage gain of 73dB and pass-band edge frequency of 300MHz.

TABLE V: Performance summary of the baseband chain and compare to [12].

	[12]	This work	
Technology	0.13μm CMOS	0.13μm CMOS	
Supply Voltage	1.2V	1.2V	
Filter order	5	6	
Passband edge frequency	240MHz	250~300MHz	
Voltage Gain at 10MHz	12.9~47.6dB	-9~73dB	
Gain Resolution (dB)	N.A.	0.5	
Input-referred noise figure	7.7nV/$\sqrt{}$Hz (22dB)	14dB	
In-band IIP3 (f1=30MHz, f2=50MHz)	-48.2dBV (under gain of 47.6dB)	-71dBV (under gain of 73dB)	
Out-band IIP3 (f1=400MHz, f2=790MHz)	-8.2dBV (under gain of 47.6dB)	-6dBV (under gain of 73dB)	
In-band IIP2 (f1=40MHz, f2=50MHz)	N.A.	-59dBV (under gain of 68dB)	
Out-band IIP2 (f1=400MHz, f2=410MHz)	+18.2dBV (under gain of 47.6dB)	-5dBV (under gain of 68dB)	
Power consumption	24mW	Core	56.4mW
		DACs for DC-offset calibration	3.6mW

Chapter 7

Transmitter Measurement

The UWB RF transmitter is implemented in a 1.2 V 0.13 μm CMOS process. The photograph of the chip is as shown in Figure 7-1. The RF circuits and the analog baseband occupy an active area of 1.2x0.4mm^2 and 0.9x0.35mm^2, respectively. The following measurement results are based on the bias condition of current consumption of 55 mA from a 1.2 V supply. The frequency response of the analog channel-selection filter was measured, as shown in Figure 7-2. The measured corner frequency is 250 MHz. The pass-band ripple is less than 1 dB. The measured out-of-band rejection is over 35 dB at 500 MHz offset. The output impedance of the transmitter was matched to 50Ω over 3-8 GHz. As shown in Figure 7-3, the measured output return loss is better than -9.3 dB in the frequency range of 3-10 GHz. The IQ modulation accuracy is demonstrated by the parameters of sideband, carrier suppression and error vector magnitude (EVM). In Figure 7-4, the measured output power, sideband and carrier suppression at frequency of 3432 MHz are -5.1 dBm, 46.1 dBc and 31.6 dBc, respectively. In Figure 7-5, the measured output power, sideband and carrier suppression at the frequency of 7656 MHz are -9.7 dBm, 29.1 dBc and 43 dBc, respectively. In Figure 7-6, the measured EVM is -28 dB under the data rate of 480 Mbps in MB-OFDM modulation as output power of -10 dBm at 3432 MHz. Linearity performance is demonstrated by the parameter of output 1-dB

compression point (OP1dB). A one-tone test for extracting the output 1-dB compression point by sweeping the voltage swing of baseband signals is performed, and output power levels of the power amplifier are monitored by the spectrum analyzer. The measured output 1-dB compression point for each frequency in band group 1 and 3 is listed in Table VI. In the worst-case, the output 1-dB compression point is -0.6dBm in 7656 MHz. Table VI also lists the measured sideband and carrier suppression for each frequency from 3.4 GHz to 7.6 GHz. Table VII summaries the performance of this works and compares with the reported UWB transmitters.

A UWB transmitter need to provide the transmit power tuning to regulate the transmit power spectral density, while still providing a reliable link for the data transfer. The linear-in-dB gain tuning function is verified by sweeping the tuning voltage, which is described in Figure 7-7. The VGA exhibits a 14 dB linear-in-dB gain tuning curve within the tuning voltage of 0.4-0.95 V. An on-chip TSSI is implemented to measure the output power. The power detection function is examined by sweeping the baseband signals level, and Figure 7-8 shows the detection curve of the TSSI. The effective power detection range is from -24 dBm to -3 dBm.

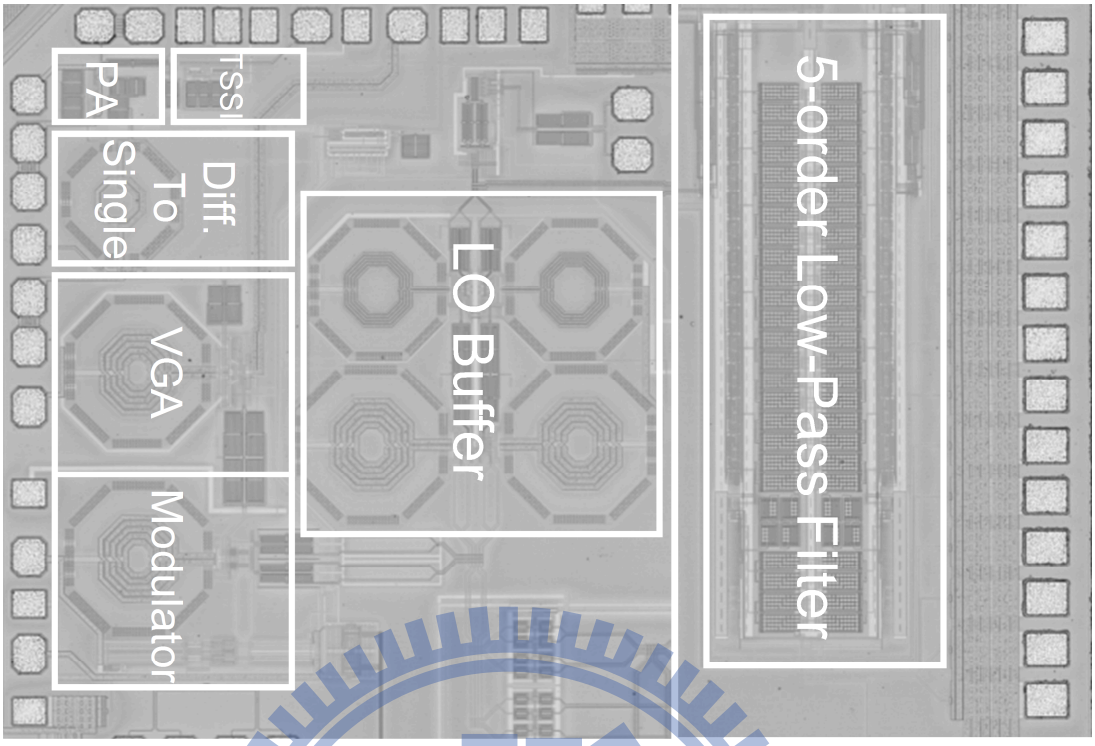


Figure 7-1: Photograph of the chip.

Figure 7-2: Measured frequency response of the analog channel-selection filter.

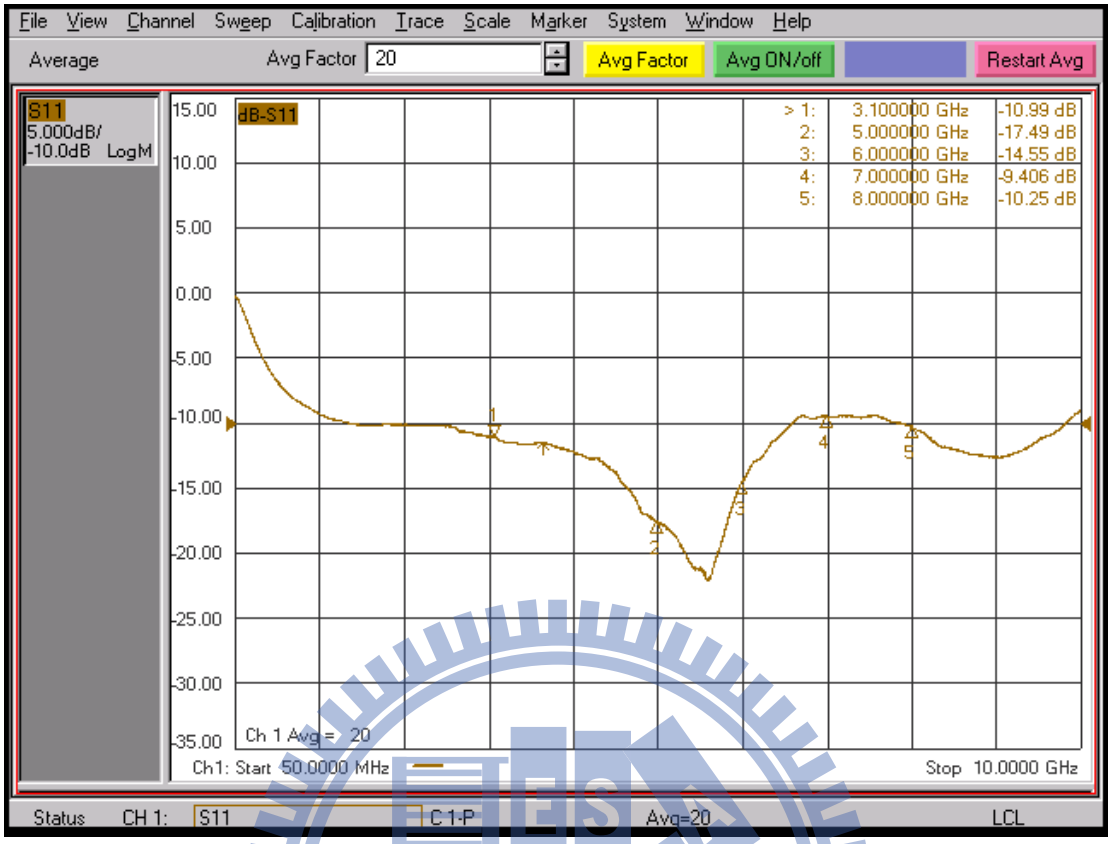


Figure 7-3 Measured output return loss of the transmitter front-end.

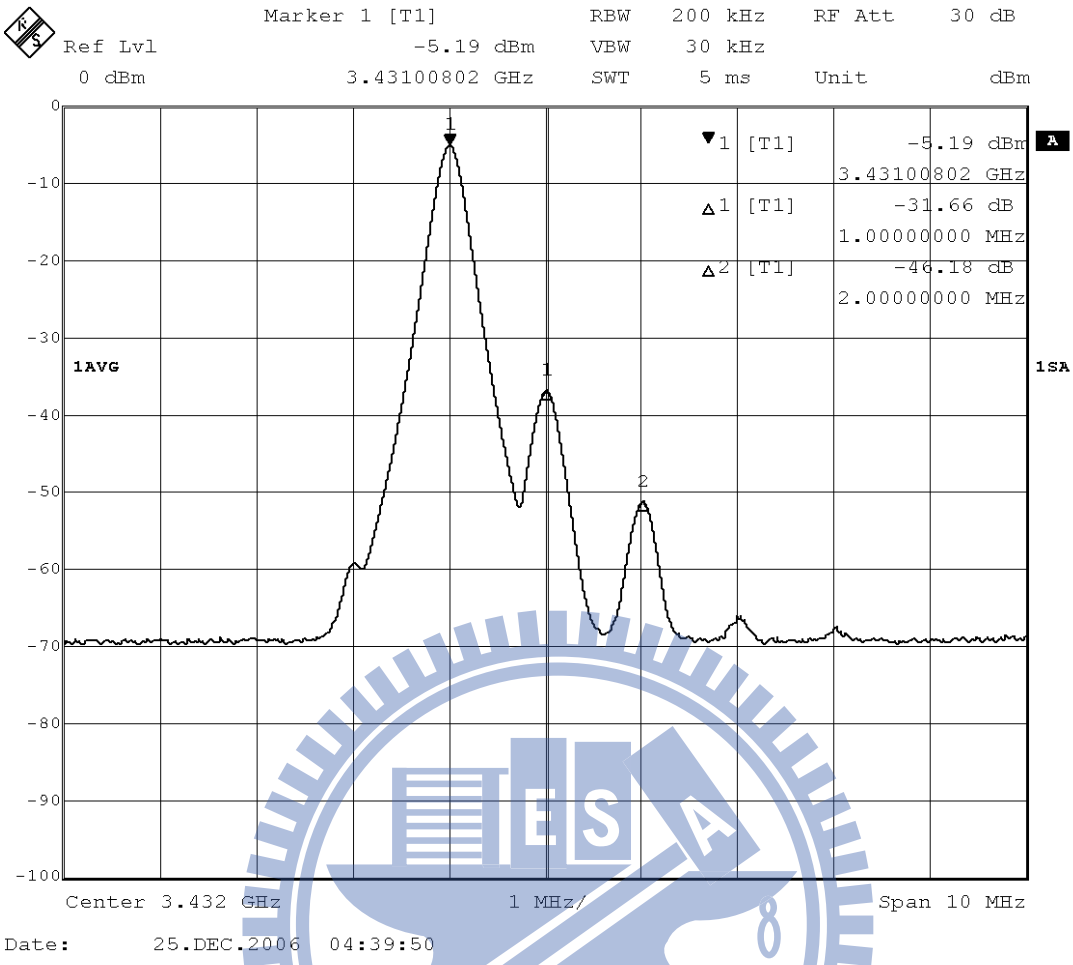


Figure 7-4: Measured output power, carrier suppression and sideband suppression performance at 3432MHz.

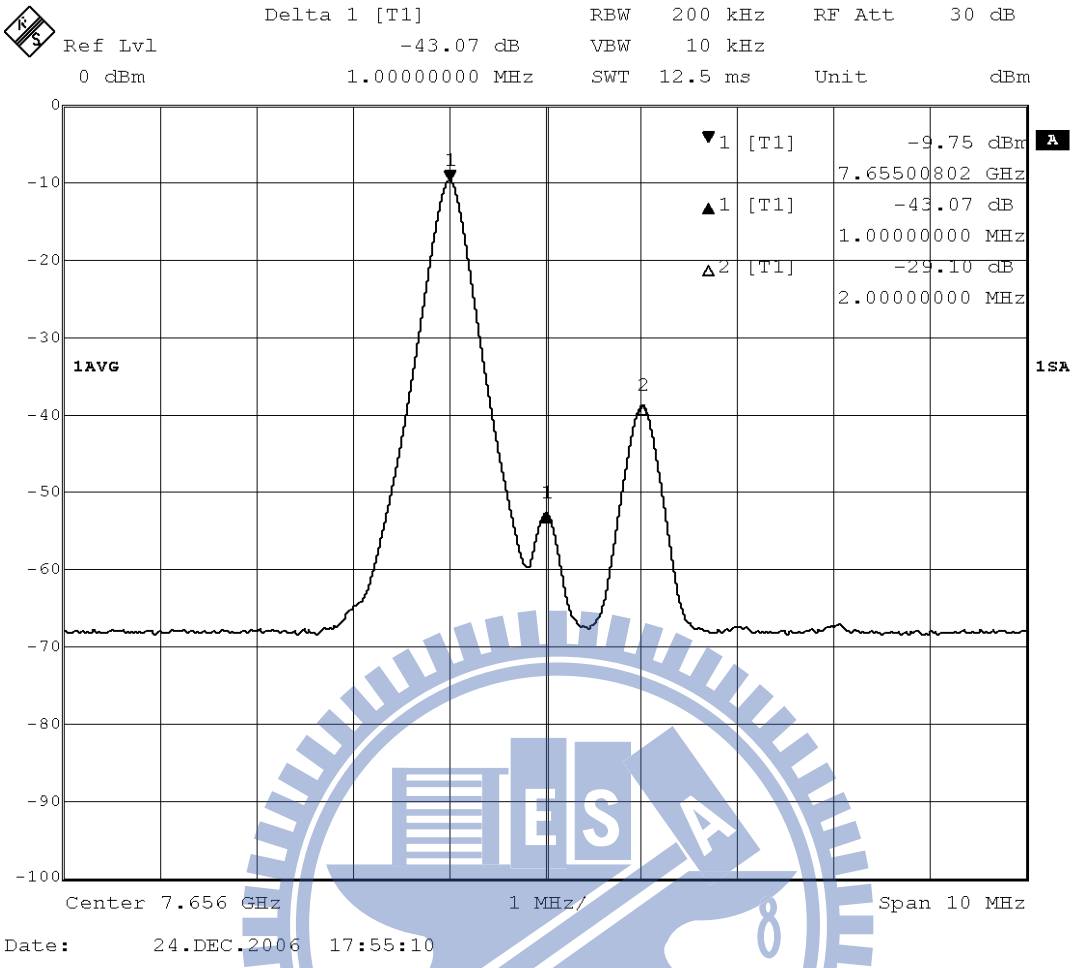


Figure 7-5: Measured output power, carrier suppression and sideband suppression performance at 7656MHz.

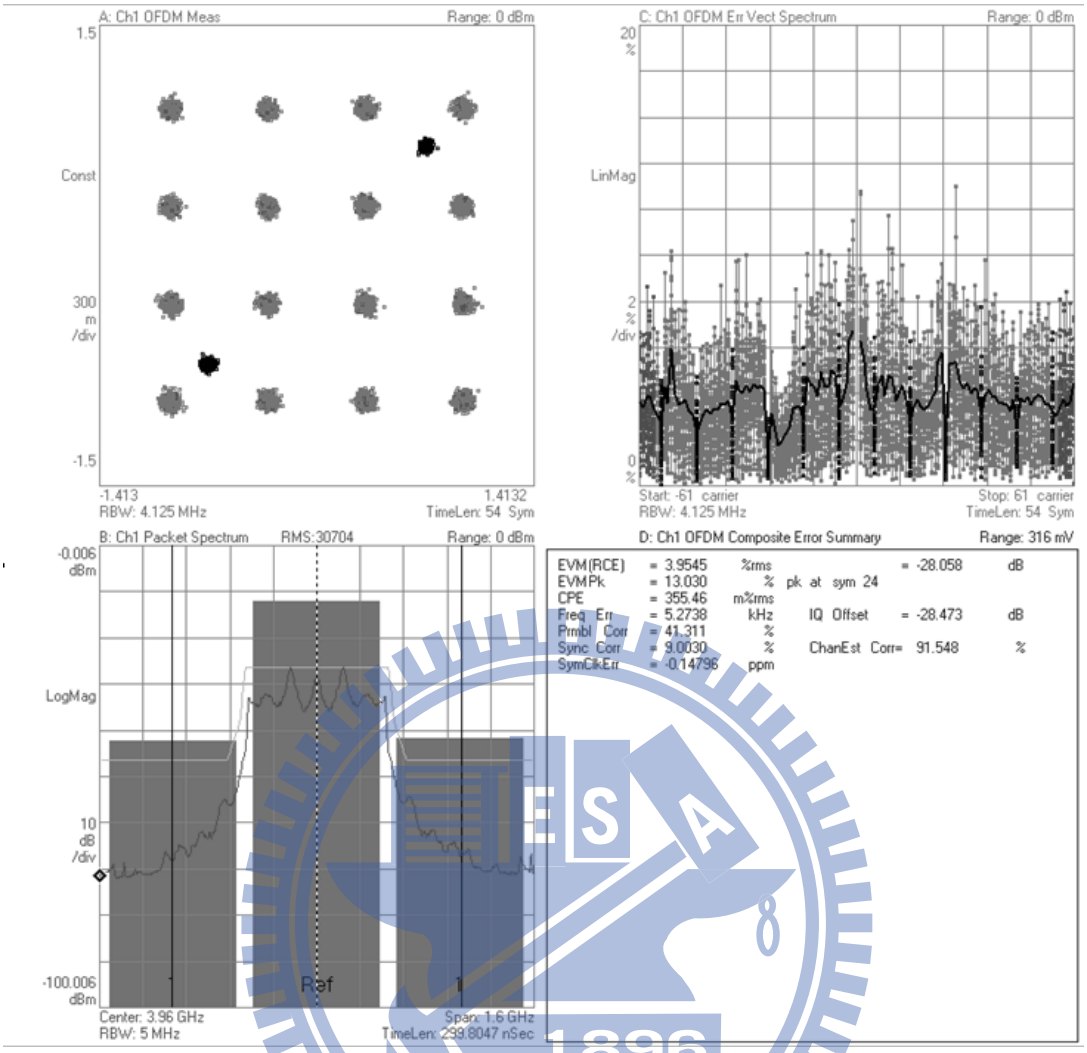


Figure 7-6: Measured error vector magnitude (EVM).

TABLE VI

PERFORMANCE SUMMARY

	3432MHz	3960MHz	4488MHz	6600MHz	7128MHz	7656MHz
Pout,max (dBm)	-5.17	-5.36	-6.06	-6.3	-8.8	-9.71
OP1dB (dBm)	1.5	1.3	1.7	0.2	0.4	-0.6
Sideband Suppression (dBc)	46.1	43.7	40.4	30.4	30.1	29.1
*Carrier Suppression (dBc)	31.6	29.4	27.6	21.0	25.5	43.7

* Carrier suppressions are shown before calibration. After calibration, Carrier suppressions are all over 40dBc.

TABLE VII

PERFORMANCE COMPARISON

	[3]	[4]	[5]	[6]	[10]	[11]	This work	
Frequency range (Hz)	3-5GHz	3-5GHz	3-5GHz	3-5GHz	3-9.5G	3-8GHz	3-8GHz	
$P_{out,max}$ (dBm)	-10	-6.8	-3.8	-4	N.A.	N.A.	-5 (3.4G)	-9.7 (7.6G)
Linrarity (dBm)	-6 (OP1dB)	9 (OIP3)	3.9 (OP1dB)	5 (OP1dB)	-2.8 (OP1dB)	N.A.	1.5 (OP1dB) (3.4G)	-0.6(OP1dB) (7.6G)
Sideband Suppression (dBc)	N.A.	32	N.A.	N.A.	N.A.	N.A.	46 (3.4G)	29 (7.6G)
Carrier Suppression (dBc)	30	28	46.2	N.A.	N.A.	-70dBm (3.4G)	31.6 (3.4G)	43.7 (7.6G)
EVM (dB)	-19.5	N.A.	-28	-27	-28	-28	-28	
Dynamic range (dB)	N.A.	13	N.A.	30	N.A.	N.A.	14 (linear-in-dB)	
Power Consumption (mW)	105* (1.5V)	116.1* (2.7V)	396.9* (1.8V)	97.5 (1.5V)	131* (1.1V)	108* (1.2V)	66 (1.2V)	
Technology	0.13μm CMOS	0.25μm SiGe	0.18μm CMOS	0.13μm CMOS	90nm CMOS	65nm CMOS	0.13μm CMOS	

* Includes power consumption of Synthesizer.

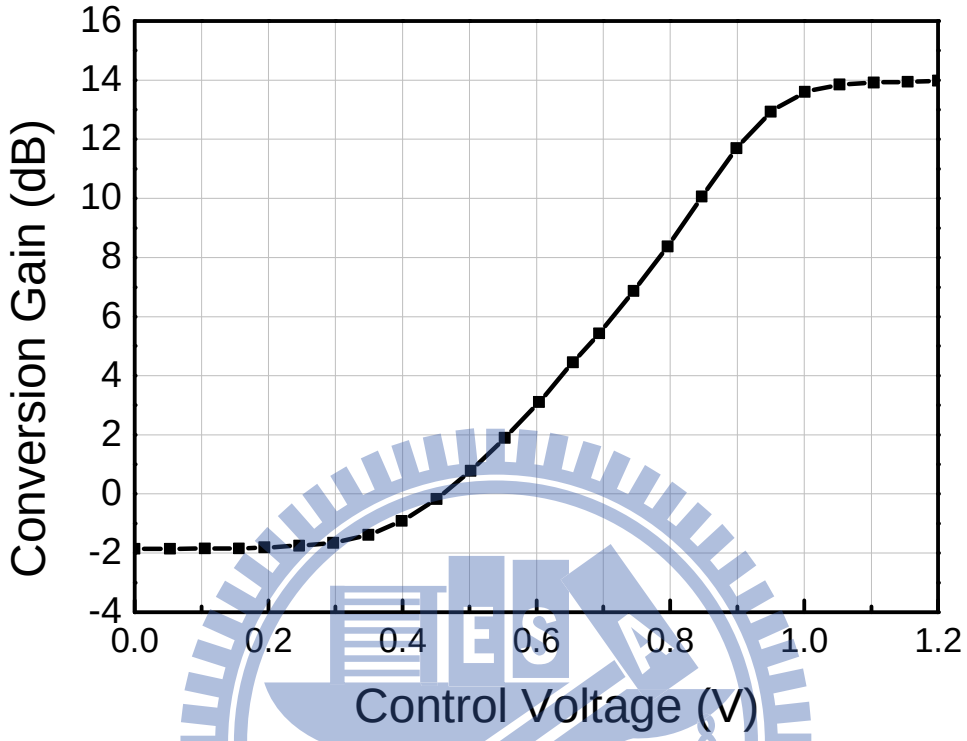


Figure 7-7: Measured voltage gain versus gain control voltage.

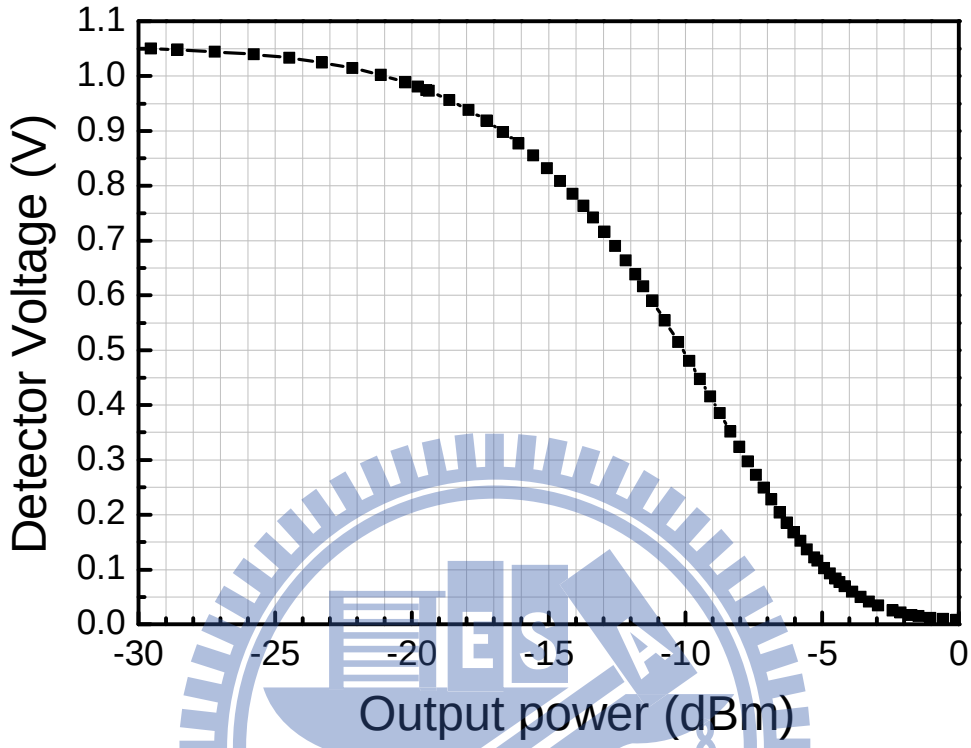


Figure 7-8 Measured detector voltage versus output power.

Chapter 8

Conclusion

A 3~5 GHz wideband, interference-robustness RF receiver had been designed and implemented in a 1.2 V 0.13 μm CMOS process. In the RF front-end, a differential LC ladder LNA with proposed 3-order active notch filter was designed in the receiver. There are many functions of band selection, gain switch, notch frequency selection and Q-factor tuning of notch filter are integrated in the LNA. The proposed notch filter was proved to eliminate the interference signal at 5.85 GHz and to increase IIP3 by 4.7 dB successfully under test interferences at 802.11a system to avoid saturating desired signals at 4488 MHz band. The LNA provides maximum power gain of 15.87 dB at 4488MHz, P1dB of -16.82dBm at 4488MHz and minimum NF of 3.19 dB at 3960MHz.

An analog baseband chain with features of wide-bandwidth and wide dynamic range of gain, as well as low noise and high linearity for UWB has been presented. Current-mode PGA gives excellent noise figure and IIP3 performance. Digital-assisted DC offset calibration solves the problem of poor IP2 performance associated with DC offset of the current-mode PGA. The bandwidth of the current-mode PGA and G_m-C filter can be further extended by using nanometer CMOS process. This work demonstrates a realization of a baseband chain applied for wideband communication systems.

A low-power, high-linearity 3-8 GHz wideband RF transmitter for UWB applications had been designed and implemented in a 1.2 V 0.13 μm CMOS process. An OP1dB of +1.5 dBm, maximum output power of -5 dBm and carrier leakage suppression of 31.66 dBc is achieved at the frequency of 3432 MHz. An OP1dB of -0.6 dBm, maximum output power of -9.7 dBm and carrier leakage suppression of 43 dBc is achieved at the frequency of 7656 MHz. The entire transmitter draws a current of 55 mA from a 1.2 V supply. The design techniques for realizing a low-power, high-linearity wideband RF transmitter are addressed in this work.

Further Work

1. The proposed current-mode wideband analog baseband implemented by using nano-meter CMOS process can extend its operating bandwidth up to over 1 GHz for 60 GHz UWB applications.
2. Gain and phase mismatch between in-phase and quadrature-phase paths of the analog baseband will lead to degradation of bits error rate (BER) performance of the entire receiver. Therefore, calibration schemes for compensating the gain and phase mismatch of the analog baseband need to be developed in the further works.

Reference

[1] Multiband OFDM Physical Layer Specification, v1.1a, WiMedia Alliance, Jul. 2005, pp. 59.

[2] Standard ECMA-368 High Rate Ultra Wideband PHY and MAC Standard. [Online]. Available: http://www.ecma-international.org/publications/standards/Ecma-368.htm.

[3] Aly Ismail and Asad A. Abidi, ”A 3.1- to 8.2-GHz Zero-IF Receiver and Direct Frequency Synthesizer in 0.18-µm SiGe BiCMOS for Mode-2 MB-OFDM UWB Communication,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2573-2582, Dec. 2005.

[4] Federal Communications Commission, Revision of Part 15 of the Commission’s Rules Regarding Ultra-Wideband Transmission Systems. Feb. 2002 [Online]. Available: http://hraunfoss.fcc.gov/edocs_public/attachmatch/FCC-02-48A1.pdf

[5] Stefano D’Amico, Andrea Baschirotto, Marcello De Matteis, et al., ”A CMOS 5 nV/$\sqrt{}$Hz 74-dB-Gain-Range 82-dB-DR Multistandard Baseband Chain for Bluetooth, UMTS, and WLAN,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, pp. 1534-1541, July 2008.

[6] Kimmo Koli and Kari Halonen, *CMOS Current Amplifiers*, Boston, Kluwer Academic Publishers, 2002, pp. 2.

[7] Fei Yuan, *CMOS Current-Mode Circuits for Data Communications*, New York, Springer Science+Bussiness Media, 2007, pp. 6.

[8] K. C. Smith and A. Sedra, “The current conveyor-A new circuit building block,” *Proceedings of the IEEE*, vol. 56, no. 8, pp. 1368-1369, Aug. 1968.

[9] E. Bruun, “Bandwidth Optimization of a Low Power, High Speed CMOS Current Op Amp,” *Int. J. Analog Integrated Circuit Design and Signal Processing*, vol. 7, pp.

11-19, Jan 1995.

[10] R. Zele, S. Lee, D. Allstot, “A High Gain Current-Mode Operational Amplifier,” in *Proc. IEEE Int. Symposium on Circuits and Systems* (ISCAS’92), San Diego, USA, pp. 2852-2855.

[11] Gurkanwal (Kamal) Singh Sahota, Charles James Persico, “High Dynamic Range Variable-Gain Amplifier for CDMA Wireless Application,” *ISSCC Dig. Tech. Papers*, pp. 374-375, Feb., 1997.

[12] Ville Saari, Mikko Kaltiokallio, Saska Lindfors *et al.*, “A 1.2V 240MHz CMOS Continuous-Time Low-Pass Filter for a UWB Radio Receive,” *ISSCC Dig. Tech. Papers*, pp. 122-123, Feb., 2007.

[13] A. A. Abidi, ”General Relations Between IP2, IP3, and Offsets in Differential Circuits and the Effects of Feedback,” *IEEE Transaction on Microwave Theory and Techniques*, vol. 51, no. 5, pp. 1610-1612, May 2003.

[14] B. Razavi et *al.*, “A UWB CMOS Transceiver,” *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2555–2562, Dec. 2005.

[15] S. Aggarwal, D. Leenaerts, R. van de Beek, *et al.*, “A Low Power Implementation for the Transmit Path of a UWB Transceiver,” *Proceedings of IEEE Custom Integrated Circuits Conference (CICC)*, pp. 149–152, Sept., 2005.

[16] C. Sandner, S. Derksen, D. Draxelmayr, et al., “A WiMedia/MBOA Compliant CMOS RF Transceiver for UWB,” *ISSCC Dig. Tech. Papers*, pp. 122-123, Feb., 2006.

[17] YAlberto Valdes-Garcia, Chinmaya Mishra, Faramarz Bahmani, *et al.*, “An 11-Band 3–10 GHz Receiver in SiGe BiCMOS for Multiband OFDM UWB Communication,” *J. Solid-State Circuits*, vol. 42, no. 4, Apr. 2007.

[18] A.Vallese, A. Bevilacqua, C. Sandner, *et al.*, “An Analog Front-end with Integrated Notch Filter for 3–5 GHz UWB Receivers in 0.13 μm CMOS,” in *Proc. IEEE European Solid-State Circuits Conf. (ESSCIRC)*, München, Germany, Sep. 2007,

pp.139–142.

[19] Trung-Kien Nguyen, Nam-Jin Oh, Choong-Yul Cha, *et al.*,"Image-Rejection CMOS Low-Noise Amplifier Design Optimization Techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, Feb. 20 2005

[20] Jing-Hong Conan Zhan, Brent R. Carlton, and Stewart S. Taylor," A Broadband Low-Cost Direct-Conversion Receiver Front-End in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1132-1137, May 2008.

[21] Peng-Un Su," A 0.25-μm CMOS OPLL Transmitter IC for GSM and DCS Applications," *IEEE Transactions on Microwave Theory and Tchniques*, vol. 53, no. 2, pp. 462-471, Feb. 2005.

[22] Mahim Ranjan, and Lawrence E. Larson," A Low-Cost and Low-Power CMOS Receiver Front-End for MB-OFDM Ultra-Wideband Systems," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 3, pp. 592-601, March 2007.

[23] Raf Roovers, Domine M. W. Leenaerts, Jos Bergervoet, et al.," An Interference-Robust Receiver for Ultra-Wideband Radio in SiGe BiCMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2563-2572, Dec. 2005.

[24] Aly Ismail and Asad A. Abidi, "A 3–10-GHz Low-Noise Amplifier with wideband *LC*-Ladder Matching Network," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, Dec. 2004.

[25] Chih-Fan Liao, and Shen-Iuan Liu, "40 Gb/s Transimpedance AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 642-655, March 2008.

[26] G. Roberts, A. Sedra," All Current-mode Frequency Selective Circuits," *Electronics Letters*, vol. 25, pp. 759-761, June 1989.

[27] G. Roberts, A. Sedra," A General Class of Current Amplifier-Based Biquadratic

Filter Circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 39, no. 4, pp. 259-263, April 1992.

[28] J. J. F. Rijns," CMOS Low-Distortion High-Frequency Variable-Gain Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 7, pp. 1029-1034, July 1996.

[29] Rolf Schaumann, Mac E. Van Valkenburg, Design of Analog Filter, New York, OXFORD UNIVERSITY PRESS, 2001, pp. 646.

[30] Krzystof Dufrene, Zdravko Boos, and Robert Weigel, " Digital Adaptive IIP2 Calibration Scheme for CMOS Down conversion Mixers," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 11, pp. 2434-2445, Nov. 2008.

[31] Hui Dong Lee, Kyung Ai Lee and Songcheol Hong, "A Wideband CMOS Variable Gain Amplifier with an Exponential Gain Control," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, issue 6, part 2, pp. 1363–1373, June 2007.

[32] Sajay Jose, Hyung-Jin Lee, Dong Ha and Sang S. Choi, "A Low-power CMOS Power Amplifier for Ultra Wideband (UWB) Applications," *IEEE International Symposium on Circuits and Systems*, vol. 5, pp. 5111–5114, May 23-26, 2005.

[33] Andrea Bevilacqua, Alessio Vallese, Christoph Sandner, *et al.*, "A 0.13µm CMOS LNA with Integrated Balun and Notch Filter for 3-to-5GHz UWB Receivers," *ISSCC Dig. Tech. Papers*, pp. 11-15. Feb. 2007.

[34] Yuan Gao, Yuanjin Zheng and Ban-Leong Ooi, "A 0.18-µm CMOS UWB LNA with 5 GHz Interference Rejection," *IEEE RFIC Symp.*, pp.47-50. June 2007.

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EDUCATION: National Chiao-Tung University, HsinChu, Taiwan.

Institute of electronics (June 2004~Present)

Currently pursuing PhD degree with a concentration in RF and analog circuits design for wireless communication and frequency synthesizers.

Advisor: Prof. C. N. Kuo (郭建男)

National Chiao-Tung University, HsinChu, Taiwan.

Master of Science in Communication Engineering, June, 2000.

Advisor: Prof. S. T. Peng (彭松村)

Tamkang University, Tamsui, Taiwan.

Bachelor of Science in Electrical Engineering, June, 1997.

BIOGRAPHY:

Horng-Yuan Shih (M'03) was born in Taipei, Taiwan, in 1976. He received the B.S. degree in electrical engineering from Tamkang University, Tamsui, Taiwan in 1997, and the M.S. and Ph.D degree in communication engineering and electronics engineering from National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 2000 and 2010, respectively.

In 2001, He joined System-on-Chip (SoC) Technology Center (STC), Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. From 2001 to 2002, he was a RF design engineer. He designed power amplifiers for GSM system in a GaAs HBT process, a low phase noise 1.8 GHz LC-VCO for fulfilling strict requirement of GSM/DCS system in a 0.18 μm CMOS process and an RF transmitter for W-CDMA system in a 0.35 μm SiGe BiCMOS process. From 2003 to 2006, he was as a section manager and was responsible for developing a RF transceiver for W-CDMA system. He also designed a fractional-N synthesizer for a multi-mode RF transceiver (GSM/DCS and WLAN) in a 0.13 μm process. From 2007 to 2008, he was responsible for designing a wideband RF transceiver for UWB applications. He is now as a technical manager in STC, ITRI. He also serves as an adjunct lecturer in department of electrical engineering, Tamkang University.

He had published eleven conference and journal papers, one in the area of electromagnetic field and ten in the area of RF/analog circuits. Moreover, He holds two U.S. patent and three R.O.C. patents. His research interests include RF and analog circuit design for wireless/wireline transceivers and frequency synthesizers.

EXPERIENCE:

RF Design Engineer, Industrial Technology Research Institute. (Jan. 2001~Nov. 2003)

Jan. 2001 – Dec. 2002

Design power amplifier test circuit for GSM system in GaAs HBT process.

Design a low phase noise 1.8GHz CMOS LC-VCO to fulfill GSM/DCS system. Measured frequency tuning range is 1742~1923MHz . Measured phase noise performance is -106.4, -125.1dBc/Hz and -138.2dBc/Hz at100k, 600 kHz and 3 MHz offset, respectively. The result was published in Asia Pacific Microwave Conference 2003 in Seoul, Korea [2].

Jan. 2002 – Nov. 2003

Design IF variable gain amplifier (VGA), Tx mixer and RF VGA of transmitter for W-CDMA system in SiGe BiCMOS process.

Integrated W-CDMA RF transmitter was measured. The measured dynamic range is 80dB. Measured EVM is 1.86dB at maximum output power of 0dBm. The result was published in Radio Frequency Integrated Circuit Symposium. 2004 (RFIC 2004) [3].

Section Manager, Industrial Technology Research Institute. (Nov. 2003~Dec. 2006)

Dec. 2003 – Dec. 2004

Lead designer of W-CDMA RF transceiver project. Finish two-step conversion receiver, transmitter and synthesizer measurement. The measured result was published in IEEE MTT-S International Microwave Symposium (IMS2005), Long Beach, CA [4].

Jan. 2005 – Dec. 2006

Design multi-modulus divider (divide number from 32 to127 with step of 1) of fractional-N synthesizer for GSM/DCS phase-modulated transmitter in 0.18um process.

Design dead-zone free phase-frequency detector (PFD) and charge pump circuit of fractional-N synthesizer for GSM/DCS and WLAN RF transceiver in 0.13um process. The charge pump circuit has small up and down current mismatch in a wide dynamic range of VCO tuning voltage.

Technical Manager, Industrial Technology Research Institute. (Jan. 2007~Present)

Jan. 2007 – Dec. 2008

Project leader of UWB RF transceiver (also define Spec. of building blocks). Design fast frequency-hopping frequency for MB-OFDM UWB Bang Group. Design differential CMOS LNA with high/low gain function and input ESD-protection. The result of UWB project was published in IEEE Asia solid state circuit conference (ASSCC2008) [6].

Jan 2009 – Present

Research focuses on All-Digital PLL for low jitter clock generator and wideband frequency synthesizer.

A differential UWB CMOS LNA with a notch filter for suppressing WLAN 802.11a signals is accepted by ICUWB 2009.

A paper titled "A 250 MHz 14 dB-NF 73 dB-Gain 82 dB-DR Analog Baseband Chain with Digital-Assisted DC-Offset Calibration for Ultra-Wideband" is submitted to Journal of Solid-Sate Circuits. (2009.4.1)

A paper titled "A 1.2V Low-Power, High-linearity 3-8GHz Wideband RF Transmitter for Ultra-Wideband" is submitted to Transactions of Microwave Theory and Techniques. (2009. 6. 8)

SKILLS: Cadence-Composer/SpectreRF/Virtuoso/Dracula, Avanti-HSPICE, Agilent-ADS, Mentor Graphics-Calibre, Cohension-System Designer.

PUBLICATIONS:

Journal papers:

[1] **Horng-Yuan Shih**, Chien-Nan Kuo, et al, 'A 250 MHz 14 dB-NF 73 dB-Gain 82 dB-DR Analog Baseband Chain with Digital-Assisted DC-Offset Calibration for Ultra-Wideband,' IEEE *Journal of Solid-State Circuits*, vol. 45, no 2, pp. 338-350, Feb. 2010.

[2] Horng-Yuan Shih, Chien-Nan Kuo and Chih-Wei Wang, 'A 1.2V Low-Power, High-linearity 3-8GHz Wideband RF Transmitter for Ultra-Wideband,' prepare to *submit to Transactions of Circuits and Systems II.*

[3] **Horng-Yuan Shih,** Chien-Nan Kuo, et al, 'A 400 MHz 500-fs-Jitter Open-Loop DLL-Based Multi-Phase Clock Generator Utilizing a Noise-Free All-Digital Locking Detection Circuitry,' prepare to submit to *IEEE Microwave and Wireless Components Letters (MWCL).*

[4] Horng-Yuan Shih, 'Introduction to Wireless Radio Frequency Transceiver,' *SoC Technical Journal* 001.

[5] **Horng-Yuan Shih, et al, '**A 1.2V Interference-Sturdiness, DC-Offset Calibrated CMOS Receiver Utilizing a Current-Mode Filter for UWB,' *SoC Technical Journal* 011.

Conference papers:

[1] S.T. Peng, R.B. Hwang, and **H.Y. Shih**,' Anomalous absorption of resonance-type periodic structures,' *IEEE Antennas and Propagation Society International Symposium*, vol. 3, pp. 1792 – 1795, July 2000.

[2] **Horng-Yuan Shih**,' A 1.8-GHz Low-Phase-Noise Integrated CMOS LC-VCO with a Low Q Inductor for GSM/DCS Band,' *Asia Pacific Microwave Conference (APMC '03) Proceedings*, Nov. 2003.

[3] **Horng-Yuan Shih**, Peng-Un Su, Yen-Horng Chen, et al., ' A highly-integrated inductor-less SiGe W-CDMA transmitter,' *IEEE Radio Frequency Integrated Circuits (RFIC '04) Symposium Digest of Papers*, pp.439 – 442, June 2004.

[4] **Horng-Yuan Shih**, Tz-Heng Fu, Yen-Horng Chen, et al.,' Highly-integrated low-power WCDMA SiGe transceiver for mobile terminals,' *IEEE International Microwave Symposium (MTT-S '05) Digest*, pp. 93-96, June 2005.

[5] Chao-Shiun Wang, Wei-Chang Li, Chomg-Kuang Wang, **Horng-Yuan Shih** and Tzu-Yi Yang,' A 3–10 GHz full-band single VCO agile switching frequency generator for MB-OFDM UWB,' *IEEE Asian Solid-State Circuits Conference (ASSCC '07)*, pp. 75-78, Nov. 2007.

[6] **Horng-Yuan Shih**, Wei-Hsien Chen, Kai-Chenug Juang, Tzu-Yi Yang and Chien-Nan Kuo, 'A 1.2V Interference-Sturdiness, DC-Offset Calibrated CMOS Receiver Utilizing a Current-Mode Filter for UWB,' *IEEE Asian Solid-State Circuits Conference (ASSCC '08)*, pp. 345-348, Nov. 2008.

[7] Yu-Lin Tsou, **Horng-Yuan Shih**, Chien-Nan Kuo and Chia-Hung Chang, 'Differential LC Ladder LNA with Proposed third-Order Active Notch Filter for UWB Band Group1,' *IEEE International Conference on Ultra-Wideband (ICUWB'09)*, pp. 511-515, Sep. 2009.

[8] **Horng-Yuan Shih,** Chien-Nan Kuo, et al, 'A 400 MHz 500-fs-Jitter Open-Loop DLL-Based Multi-Phase Clock Generator Utilizing an Noise-Free All-Digital Locking Detection Circuitry,' submitted to *IEEE International Symposium on Circuits and Systems* (ISCAS 2010).

Patents:

[1] Kai-Cheung Juang, **Horng-Yuan Shih**, Peng-Un Su," Voltage controlled oscillator with anti supply voltage variation and/or process variation," U.S. Patent no. 7,449,972.

[2] Kai-Cheung Juang, Wei-Hsien Chen, **Horng-Yuan Shih**," DC offset calibration method," U.S. Patent no. 7,629,906.

[3] 莊凱翔, **施鴻源**, 蘇秉恩,' 可抵抗電源變動與/或製程變異之電壓控制振盪器,' 中華民國專利 No. I264875.

[4] 蘇秉恩, 陳志宏, **施鴻源**,' 自動校正的頻率合成裝置,' 中華民國專利 No. I241069.

[5] 蘇秉恩, **施鴻源**, 郭明清,' 具電壓雜訊壓抑與快速啟動的裝置,' 中華民國專利 No. I304289.

[6] Peng-Un Su, Chih-Hung Chen, **Horng-Yuan Shih**," Frequency synthesizing device with automatic calibration," 美國專利 US 2006/0104398 A1，公告中。

[7] Peng-Un Su, **Horng-Yuan Shih**, Ming-Ching Kuo, "Device for voltage-noise rejection and fast start-up," 美國專利 US 2007/0115061 A1，公告中。

[8] Chao-Shiun Wang, Chorng-Kuan Wang, **Hormg-Yuan Shih**, Zhi-Wei Wang, Kai-Cheung Juang," Ultra-wideband (UWB) frequency synthesizer system and method," 美國專利 US 2009/0028217 A1，公告中。

[9] Chien-Nan Kuo, **Horng-Yuan Shih**, Yi-Hsin Pang," Radio front-end with coherent-tuning filters," 美國專利，審查中(2008/05 申請)。

[10] 蘇秉恩, **施鴻源**, 郭明清,' 具電壓雜訊壓抑與快速啟動的裝置,' 中國專利，審查中(2006/03 申請)。

[11] 王照勳, 汪重光, **施鴻源**, 王志偉, 莊凱翔," 超寬頻頻率合成器系統與方法," 中華民國專利，審查中(2007/08 申請)。

[12] 莊凱翔, 陳威憲, **施鴻源**," 直流偏移校正電路及方法," 中華民國專利，審查中(2007/12 申請)。

[13] 郭建男, **施鴻源**, 龐一心," 具有協調性之可調濾波器的無線通訊前端," 中華民國專利，審查中(2007/12 申請)。

[14] 王照勳, 汪重光, **施鴻源**, 王志偉, 莊凱翔," 超寬頻頻率合成器系統與方法," 中國專利，審查中(2007/12 申請)。

[15] 莊凱翔, 陳威憲, **施鴻源**," 直流偏移校正電路及方法," 中國專利，審查中(2008/01 申請)。

[16] 郭建男, **施鴻源**, 龐一心," 具有協調性之可調濾波器的無線通訊前端," 中國專利，審查中 (2009/02 申請)。