國立交通大學

材料科學與工程研究所
博士論文

高頻高功率應用之氮化鎵系列半導體元件製作與特性研究

Fabrication and Characterization of GaN-based Semiconductor Devices for High Frequency and High Power Applications

研 究 生：張家達

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摘要

氮化鎵系列材料爲新世代半導體之星，其應用範圍涵蓋高頻元件、功率電子元件、以及光電元件。本論文即針對氮化鎵材料的高頻與高功率應用所做之研究。首先是機械張應力對氮化鋁鎵/氮化鎵高電子遷移率電晶體之效應的研究，研究發現機械張應力能使元件產生額外的通道電子，進而改變通道飽和電流特性，此現象同時取決於電子通道的方向；另外，張應力能使元件的脈衝電流特性變差，這表示張應力透過增加壓電極性使元件表面產生更多電子能井，這些額外的表面能井侷限住更多電子，使通道瞬間電流受到抑制。論文第二部分成功驗證了氮化鋁鎵/氮化鎵高電子遷移率電晶體在 30GHz 下依舊保有優良的低雜訊特性，當該元件偏壓在閘極爲-3V 與汲極爲 10V 時，其 30GHz 的最低雜訊值爲 1.6dB 且元件的增益值爲 5dB，在現今文獻中，此項成果是第一篇將氮化鎵元件低雜訊特性提升至 30GHz 之國際期刊。論文第三部分結合氟離子電漿與金氧半閘極結構技術，成功製作出具備高閘極起始電壓的增強型氮化鋁鎵/氮化鎵電晶體。透過 16nm 的氧化鋁閘極氧化層，使閘極起始電壓提升至 5.1V，同時，該元件依舊保有高電流密度 500mA/mm，此成果是第一篇將閘極起始電壓提升至超過 5V 並能同時具備高電流密度之國際期刊。

Fabrication and Characterization of GaN-based Semiconductor Devices for High Frequency and High Power Applications

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Abstract

GaN-based semiconductors are promising candidates for RF high frequency wireless, power electronics, and optoelectronics applications. This thesis focuses GaN-based High Electron Mobility Transistors (HEMTs) for high frequency and high power application. First of all, the characteristics of unpassivated AlGaN/GaN HEMTs under uniaxial tensile strain were investigated. Mechanical stress can produce additional charges resulting in the change of HEMT channel current. This phenomenon depends on gate orientation, and may be the result of the piezoelectric effect and changes in electron mobility due to the applied uniaxial stress. Additionally, results show that tensile strain reduces the transient current, which is likely due to the additional donor-like surface states created through the piezoelectric effect. Secondly, a 100-nm gate-recessed n-GaN/AlGaN/GaN HEMT with low noise properties at 30 GHz is demonstrated. The recessed GaN HEMT exhibits a low ohmic-contact resistance of 0.28 Ω·mm, and a low gate leakage current of 0.9 μA/mm when biased at $V_{GS} = -3$ V and $V_{DS} = 10$ V. At the same bias point, a minimum noise figure of 1.6 dB at 30 GHz and an associated gain of 5dB are achieved. To the best of our knowledge, this is the first and the best noise performance reported at 30 GHz for gate-recessed AlGaN/GaN HEMTs. Finally, a normally-off operation AlGaN/GaN HEMT with high threshold voltage is developed utilizing a Fluorine-based treatment technique combined with a metal-oxide-semiconductor gate architecture. Threshold voltage as high as 5.1 V was achieved using a 16-nm-thick Al_2O_3 gate oxide film. Additionally, the device performed a drain current density of 500 mA/mm and a peak transconductance of 100 mS/mm. These performances are comparable to the conventional normally-on devices.

致謝

感謝張翼老師給我機會，讓我從大四做專題開始，能在實驗室學習化合物半導體的知識及其他許多新的事物，並且兩度讓我有機會出國交換，在日本東京工業大學與德國 Leibniz institute-FBH 交流與學習，這兩次出國的體驗，都是對我的成長有極大助益的重要人生經驗；並感謝張老師的指導，讓我有幸能發表國際期刊與國際研究接軌。

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Contents

Figure Captions

Chapter 1

Introduction

Considerable interests have been paid to the development of GaN-based semiconductors for RF high-frequency wireless, power electronics and optoelectronic applications due to their potentials, such as high breakdown field, high electron mobility, and direct band gap property[1-1,1-2]. Table 1-1 shows GaN physical properties compared with Si and GaAs.

For RF devices, AlGaN/GaN high electron mobility transistors (HEMTs), one of the key issues encountered in the early stages of investigating these devices is the significant RF current dispersion. The dispersion is due to the sensitive surface of AlGaN layer, and this may be related to its polarization nature, as illustrated in Figure 1-1[1-3]. Donor-like surface states of AlGaN was thought be the electron source for the AlGaN/GaN heterojunction through the polarization, as shown in Figure 1-2 [1-4]. These states would trap electrons to deplete the device channel current during RF operation and then degrade the device performance. One approach to solve this problem is by applying a silicon nitride (SiN_x) passivation layer on the ungated region, as illustrated in Figure 1-3. This technique improves the DC and RF performances by eliminating the surface states density and then reducing the surface-related RF dispersion [1-5, 1-6]. Further, the increase in DC current can be explained by additional charges induced by piezoelectric polarization resulting from tensile strain in the SiNx film [1-7], as shown in Figure 1-4 and Figure 1-5. However, no study has not examined the effect of purely strain on AlGaN/GaN HEMTs. Such an impact of the strain on the surface states of the AlGaN/GaN HEMT was investigated for the first time, as presented in Chapter 2.

For practical RF applications, the need for on-demand broadband capacity for all types of communication has led to the development of a broadband radio-based access network communication system capable of providing tens of mega bits per second in the downlink stream [1-8]. The local multipoint distribution system (LMDS) with frequency bands allocated at 28–29 GHz in the US and at 40.5–42.5 GHz in Europe is one such system based on cellular architecture offering flexible high-capacity connections. In point-to-point LMDS systems, RF front-end technology is the key for such systems to meet the stringent requirements of broadband performance; this is especially true in the case of the receiving chain where minimum signal distortion is a must for the received signals. Thus, low noise amplifiers with high linearity play a critical role in such systems. Towards this purpose, low noise GaN device technology is certainly a promising candidate because it can provide both low noise and high power performance by biasing at high drain voltages. The potential of GaN-based HEMTs for low noise applications up to 30 GHz has been demonstrated. The result is presented in Chapter 3.

Another practical application of GaN-based HEMTs is for high power electronics, particularly referring to those with normally-off operation. For power switching applications, devices with normally-off operation are necessary because they can not only help simplify the complexity of the circuit but also reduce the standby power consumption. In addition, they provide a fail-safe function because a noise higher than 3 V may occur on the gate electrode during the device operation [1-9]. Several approaches toward such requirements based on AlGaN/GaN heterostructure have been investigated, such as recessed gate [1-10], Fluoride-based treatment [1-11], and band diagram engineered [1-12, 1-13]. However, these approaches still encounter an issue which is either lower current density or insufficient threshold voltage for the gate noise blocking. Fabrication of the normally-off GaN-based HEMTs with high threshold voltage is successfully developed, as presented in Chapter 4.

In addition to high frequency and high power applications, GaN-based light-emitting diodes grown on patterned sapphire substrates are also studied, of which details can be referred to Appendix B.

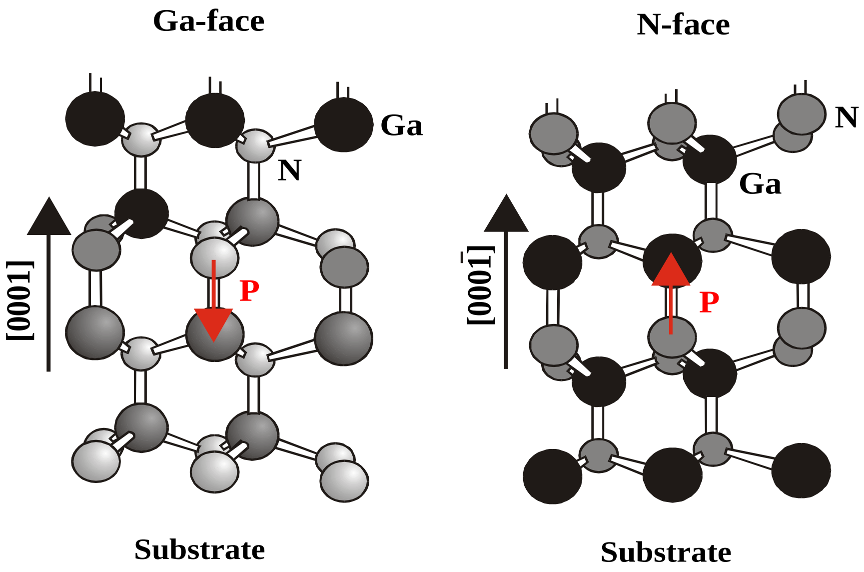

Figure 1-1. Atomic arrangement in Ga-face and N-face Wurzite GaN lattice. The red rows show the direction of spontaneous polarization.

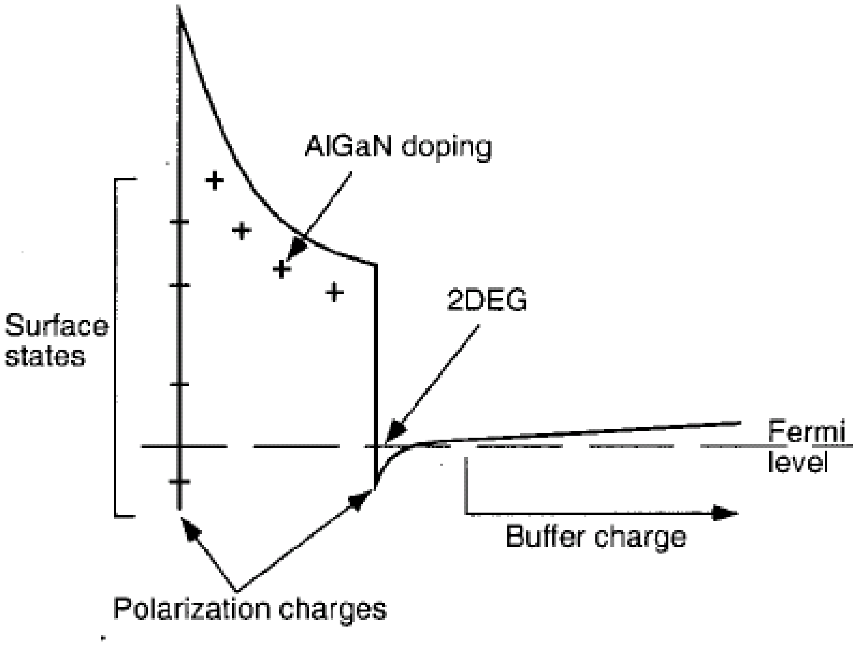

Figure 1-2. Schematic conduction band diagram for an AlGaN/GaN heterojunction showing the various charge components

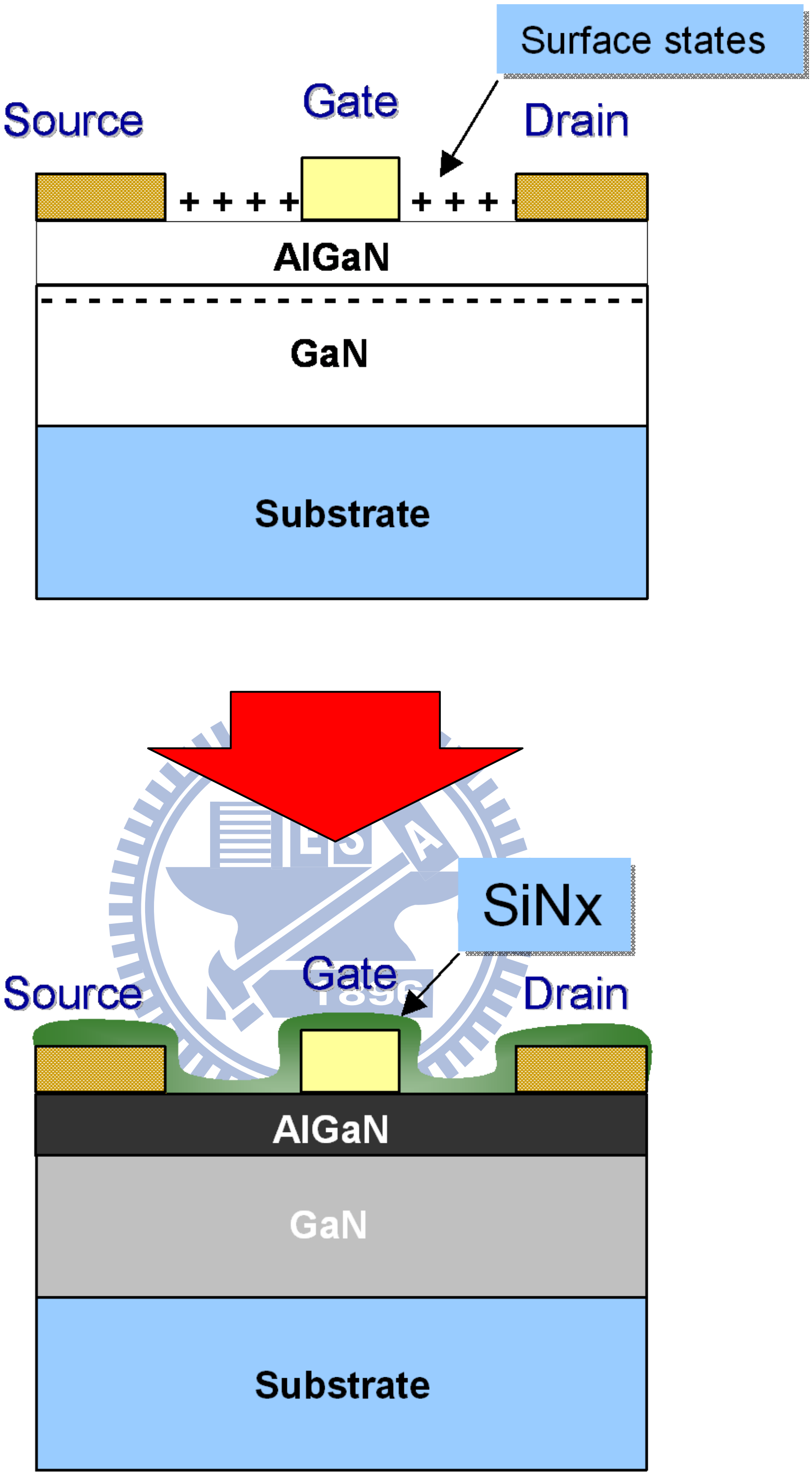

Figure 1-3. Schematic diagram for an AlGaN/GaN HEMT before and after SiN_x passivation.

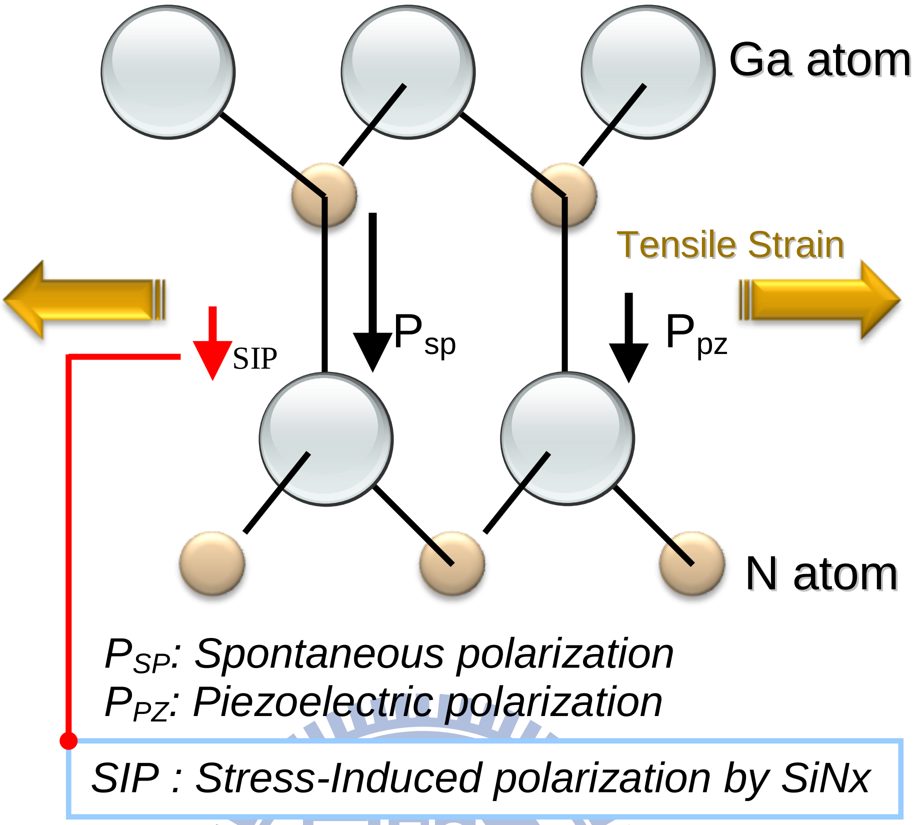

Figure 1-4. Atomic arrangement diagram of AlGaN layer for stress-induced polarization by SiN_x passivation.

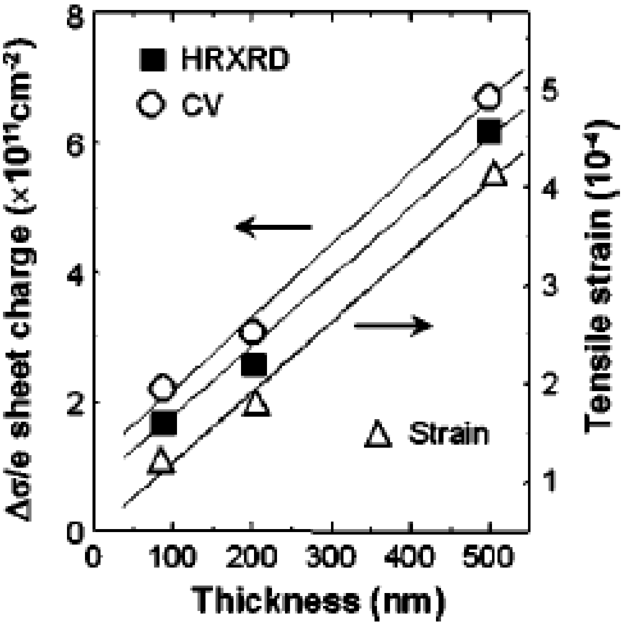

Figure 1-5. Change of sheet charge density and external tensile strain applied to the AlGaN layer in the AlGaN/GaN HFET structure as a function of SiN_x thickness.

	Si	GaAs	InP	SiC	GaN
Energy Bandgap (eV)	1.12	1.43	1.34	3.26	3.39
Critical Breakdown Field (MV/cm)	0.25	0.4	0.5	2.2	3.3
Thermal Conductivity (W/cm-K)	1.5	0.5	0.69	4.9	1.7
Mobility (cm^2/V-s)	1400	8500	5400	260	2000 (2DEG)
Peak Saturation Velocity (cm/s)	1.0×10^7	2.1×10^7	2.3×10^7	2.0×10^7	2.7×10^7

Table 1-1. Property comparison of different materials.

Chapter 2

Electrical Characteristics for AlGaN/GaN HEMTs under Uniaxial Tensile Strain

2.1 Introduction

This chapter describes the characteristics of unpassivated AlGaN/GaN HEMTs under mechanical uniaxial tensile strain and the effect of this strain on DC forward and transient characteristics of devices with gates oriented along the [10-10] and [11-20] directions. The work was done by using a three-point bending test fixture that simulates the tensile strain on the *c*-axis induced by SiNx passivation

2.2 Experiment

An undoped AlGaN/GaN HEMT heterostructure was grown on a 2-inch (0001) sapphire substrate using metal-organic chemical vapor deposition (MOCVD). The epitaxial structure consisted of a 2-μm-thick GaN buffer layer, followed by a 30nm-thick $Al_{0.25}GaN_{0.75}N$ barrier layer. The room temperature Hall mobility and sheet electron concentration of the sample were 1100 cm^2/Vs and 1×10^{13} cm^{-2}, respectively.

The wafer was cut into test die (25mm × 15mm) with the edges along the [10-10] and [11-20] directions, as illustrated in Figure. 2-1(a). The HEMT devices fabrication started with ohmic contact formation. Ti/Al/Ni/Au metal stack (20/120/25/100nm) was evaporated and subsequently annealed at 800 ˚C for 60 sec in N_2 ambient. Device mesa isolation was then formed by utilizing inductively coupled plasma etcher with Cl_2-based gas plasma. For gate formation, devices with gates oriented along [11-20] and [10-10] directions were defined by optical lithography with 7 μm drain-source spacing, followed by evaporation of Ni/Au (20/300nm) as gate metal. The gate length and width were 1 μm and 2 × 50 μm, respectively. Devices were left unpassivated in order to avoid the stress effects caused by SiNx passivation.

A bending test fixture consisting of three stainless steel cylindrical bars was used to apply the stresses, as Figure. 2-1(b) shows. The tensile strain was calculated as

$$\varepsilon_{yy} = 3hJ_0 / L^2 \text{ [2-1]}$$

where h is the thickness of the test die, J_0 is the deformation at the center, and L is the length of the test die. Devices were probed through the region between the two cylindrical bars on the top. The DC characterizations of the devices were performed by Agilent E5270B semiconductor analyzer. An Accent DiVA D225 measured the pulsed I-V characteristics with a pulse-width of 100 ns, 1ms separation between each pulse signal, and pulsed from the bias point of $V_{GS} = V_{pinch\text{-}off}$ and $V_{DS} = 0$ V and $V_{GS} = V_{pinch\text{-}off}$ and $V_{DS} = 20$ V.

2.3 Results and Discussion

Before applying uniaxial tensile strain, DC characterization of the devices performed as reference level, one of which are shown in Figure 2-2, Figure 2-3, and Figure 2-4. The device before being under tensile strain performed approximately 670mA/mm, 150mS/mm, and 150V for saturation current density, peak transconductance, and off-state breakdown voltage, respectively. Since the off-state breakdown voltage was found to be independent of the applied uniaxial tensile strain, following discussion will be focus on DC forward characteristics of the devices under mechanical uniaxial strain.

Figure 2-5 shows the saturation current density (I_{DSS}) shift of the devices with two gate orientations under different uniaxial tensile strains. Devices with gates oriented along the [10-10] direction exhibited an increase in I_{DSS} when the uniaxial tensile strain increased. The saturation current increased by approximately 3.42% under an uniaxial tensile strain of 3.94×10^{-4}. For devices with gates oriented along the [11-20] direction, I_{DSS} declined by about 0.73% at a strain level of 1.47×10^{-4} and then increased to approximately 0.96% at a strain level of 3.94×10^{-4}. Figure 2-6 shows the peak transconductance shift of the devices with both gate orientations as a function of uniaxial tensile strains. Due to the changes of the saturation current, the peak transconductance changed accordingly. For the device with gate oriented along the [10-10] direction, the peak transconductance continuously increased up to about 4.5% at a strain level of 3.94×10^{-4}; for the other orientation, however, the shift of the peak transconductance fluctuated at 0%, which can be explained by the slight change of the channel current.

The additional polarization charge induced by the mechanical uniaxial strain, P_{un} is theoretically calculated by

$$P_{un} = (e_{31} - e_{33}\frac{C_{12}}{C_{13}})\varepsilon_{yy} \quad [2\text{-}2]$$

where e is the piezoelectric constant and C is the elastic constant of the Wurzite lattice [2-3]. Figure 2-5 also plots the results normalized to the original electron sheet concentration from the Hall measurement as a function of uniaxial tensile strain. These results agree with those for devices with gate orientations of [10-10]. However, for devices with a gate orientation of [11-20], this deviation is likely due to the modulation of electron mobility by the uniaxial strain. The decrease of the electron mobility in the current flow direction of [10-10] dominates the current density behaviours at lower strain states. The increase in the charge density then dominates as the strain becomes greater. Previous research reports that hole mobility of p-type GaN material under the uniaxial strain depends upon direction [2-4], but such an effect on the electron mobility of AlGaN/GaN requires further investigation.

Figure 2-7 compares the pulsed I_D-V_D and DC I_D-V_D characteristics. Devices under a uniaxial tensile strain of 1.47×10^{-4} exhibited a significant reduction in transient drain current. To observe this phenomenon more clearly, a current ratio term called current recovery was induced and plotted in Figure 2-8. Figure 2-8 shows the current recovery (I_T / I_{DC}) (i.e., transient drain current at V_{GS} = 0 V and V_{DS} = 10 V, I_T normalized to DC values at the same bias point) as a function of different uniaxial tensile strains. No significant difference in current recovery appears in devices with these two gate orientations, and there is an approximately 10% reduction in current recovery at a strain level of 1.47×10^{-4}. When the strain exceeds 1.47×10^{-4}, there is still an approximately 5% reduction in current recovery at a strain level of 3.94×10^{-4}. This implies that the existence of additional donor-like surface states, which provide the electrons for the 2DEG through the additional piezoelectric polarization, resulting in the increased gate lag. This finding agrees with the source for electrons in AlGaN/GaN heterostructure reported by *J. P. Ibbetson, et. al.* [2-5]. The slight upward trend in current recovery beyond a strain level of 1.47×10^{-4} implies that there could be other sources for the electrons [2-6]. Figure 2-9 shows the current recovery measured at V_{GS} = 0 V and V_{DS} = 20 V as a function of strain. The transient I-V pulsed from the class B bias point is used to monitor the gate lag and drain lag simultaneously [2-7, 2-8, 2-9]. Similar trend on the change of current recovery measured at these two different bias points was observed. This means that the electron trapping under uniaxial strain was dominated by the gate lag effect which is related to the additional surface states induced by such strain instead of by the buffer trapping-related drain lag effect.

To further confirm the role of the SiN_x-induced tensile strain in drain current transient behaviour, another wafer was fabricated using the same process flow mentioned above and then passivated with a sequence of SiN_x films using the standard PECVD process, as Figure 2-10 illustrates. The first SiN_x layer helped avoid the contribution due to interface reactions between AlGaN and SiN_x. The second SiN_x layer induced a tensile stress of 2.32×10-4 to the devices, as determined by the lattice deformation on the AlGaN c-axis using high resolution x-ray diffraction (Bade-D1 HR-XRD), as shown in Figure 2-11. Figure 2-12 and Figure 2-13 compare the transient characteristics of device measured at bias point of $V_{GS} = V_{pinch\text{-}off}$ and V_{DS} = 0 V and V_{GS} = Vpinch-off and V_{DS} = 20 V, respectively, before and after the second nitride layer passivation. The transient drain currents decreased after the tensile stress SiNx passivation, and this phenomenon is independent of gate orientation. Figure 2-14 and Figure 2-15 plot the transient currents as a function of transient time before and after stress SiNx passivation, which were measured from both bias point to bias point of V_{GS} = 0V and V_{DS} = 8V. A large reduction on transient current at the pulse time of 100ns was found. With the transient time increasing to steady state (1ms), the reduction tended to be smooth and the current level became similar between each passivation condition. It means that SiNx-induced tensile strain only affect the transient characteristics which are predominated by the surface states.

2.4 Summary

The channel current density of AlGaN/GaN HEMTs can be modulated by applying uniaxial tensile strain and it depends on the gate orientation. Additionally, tensile strain severely degrades current recovery. This could be attributed to the additional donor-like surface states induced by the additional piezoelectric polarization that the tensile strain produces.

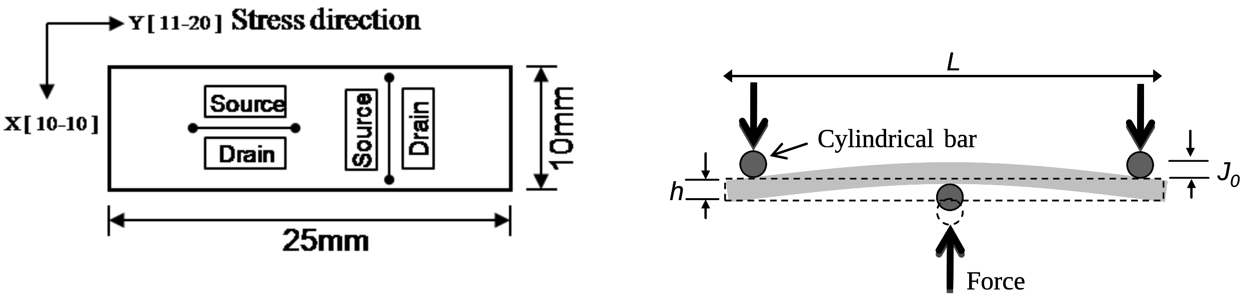

Figure 2-1(a). Top view of the test die and gate orientations under uniaxial stress along [11-20] and [10-10], and (b) schematic configurations of the three-point bending test fixture for the tensile stress.

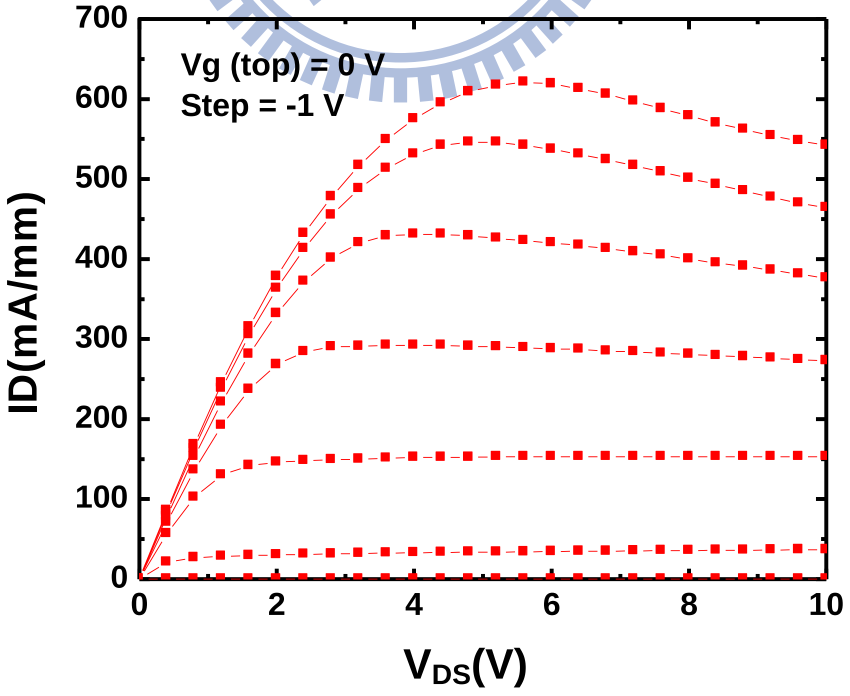

Figure 2-2. I_D-V_D curves of the device without the uniaxial tensile strain.

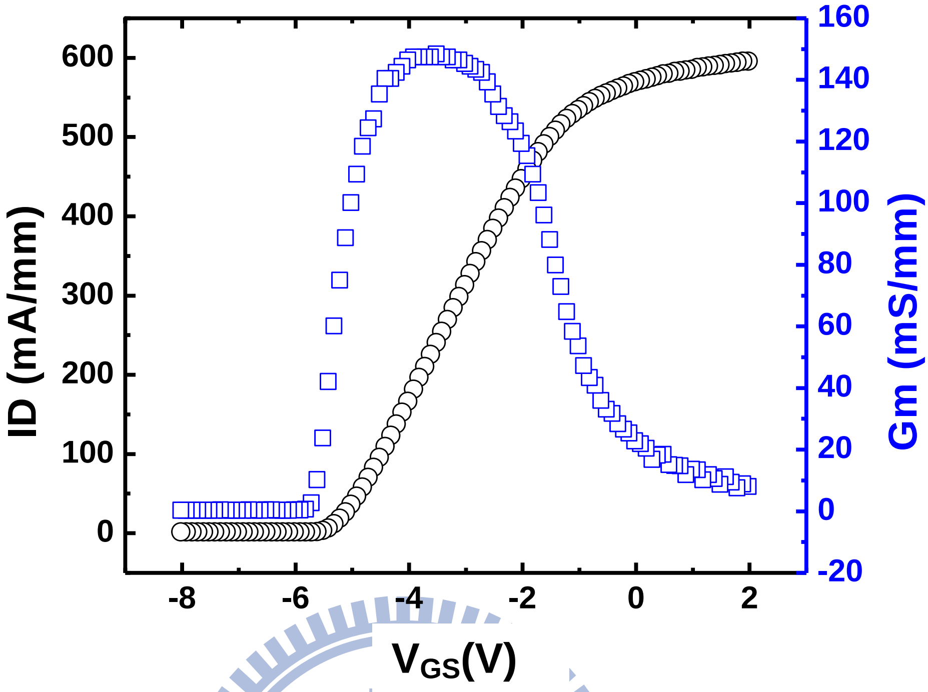

Figure 2-3. Transconductance characteristic of the device without the uniaxial tensile strain.

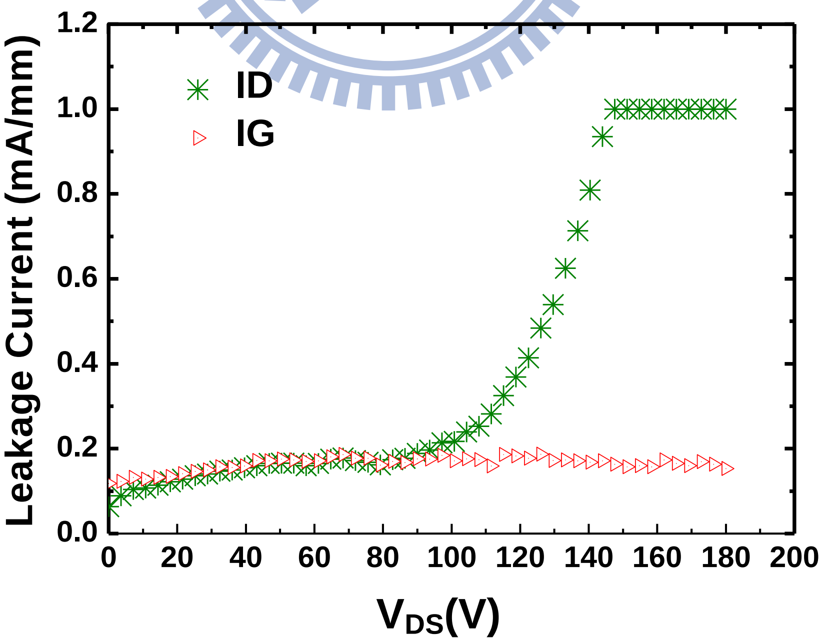

Figure 2-4. Three-terminal breakdown performance of the device without the uniaxial tensile strain. The breakdown down voltage is defined by drain leakage current up to 1mA/mm.

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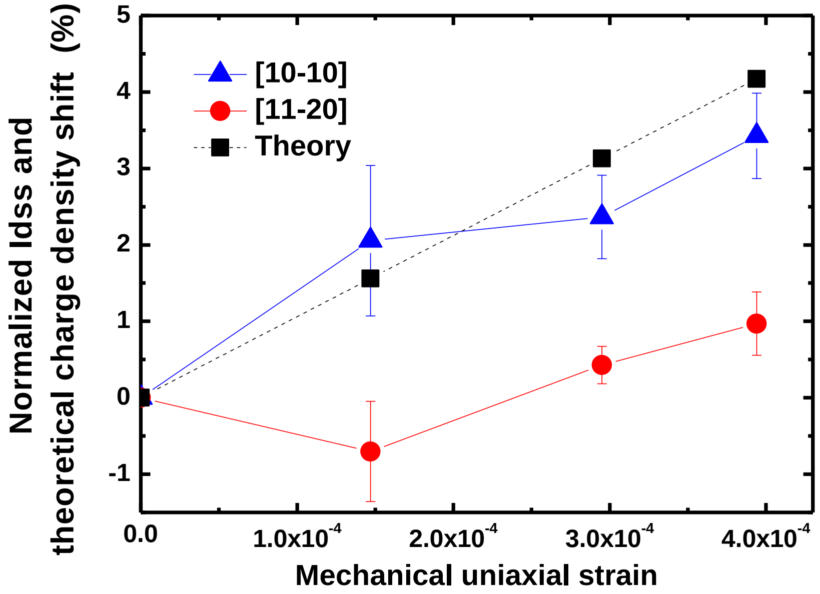

Figure 2-5. Normalized I_{DSS} of the devices with gates oriented [10-10] and [11-20] directions, and theoretical charge density shift as a function of mechanical uniaxial strain.

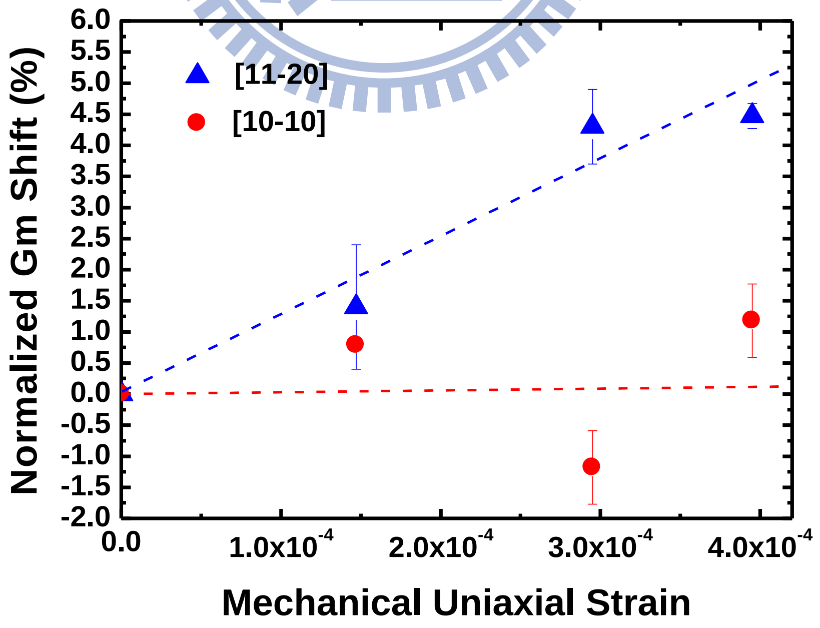

Figure 2-6. Normalized transconductance shift of the devices with gates oriented [10-10] and [11-20] directions as a function of mechanical uniaxial strain.

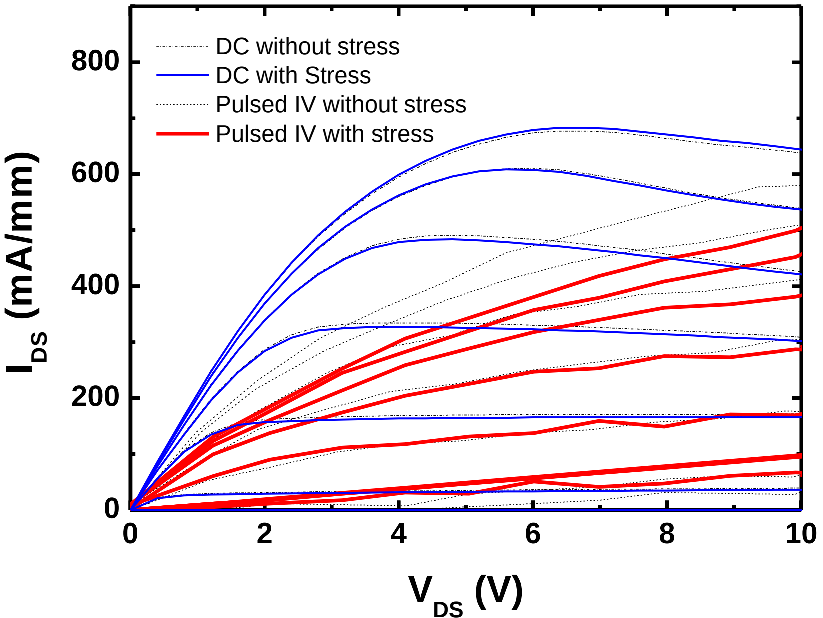

Figure 2-7. Transient characteristics (V_{GS} = $V_{pinch\text{-}off}$ to 0V, 1V/step) of unpassivated AlGaN/GaN HEMTs under the strain of zero and 1.47×10^{-4} in comparison with the DC characteristics.

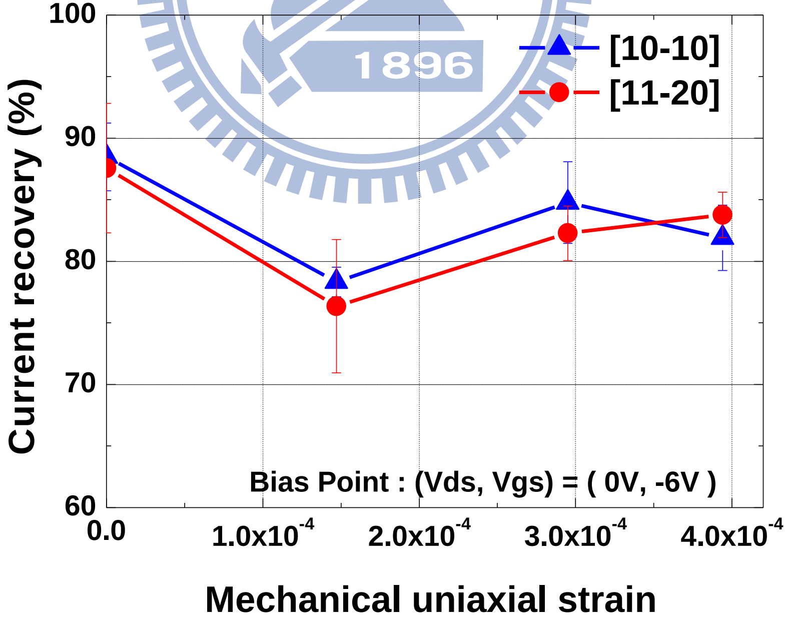

Figure 2-8. Current recovery of the unpassivated AlGaN/GaN HEMTs as a function of mechanical uniaxial strain, measured at the bias point of V_{GS} = $V_{pinch\text{-}off}$ and V_{DS} = 0 V.

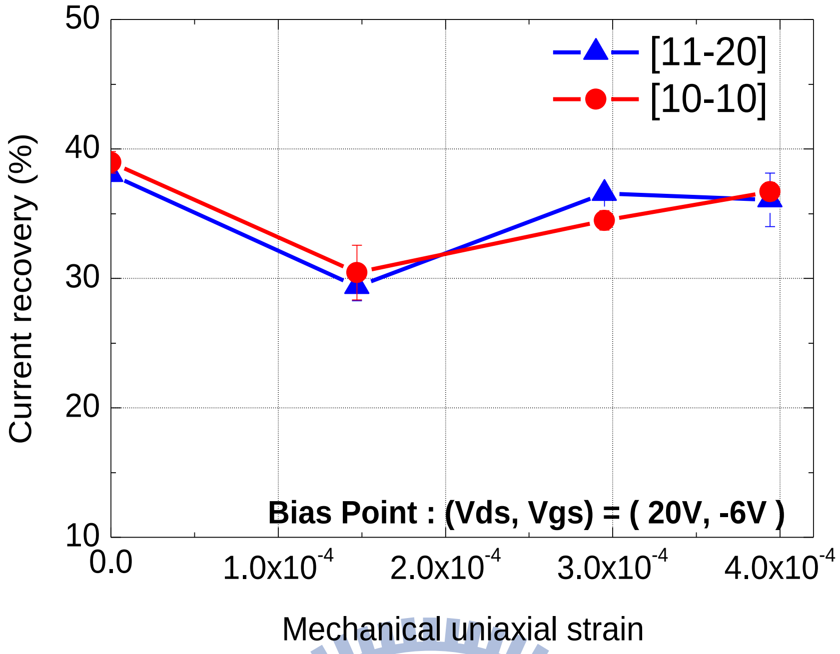

Figure 2-9. Current recovery of the unpassivated AlGaN/GaN HEMTs as a function of mechanical uniaxial strain, measured at the bias point of $V_{GS} = V_{pinch\text{-}off}$ and $V_{DS} = 20$ V.

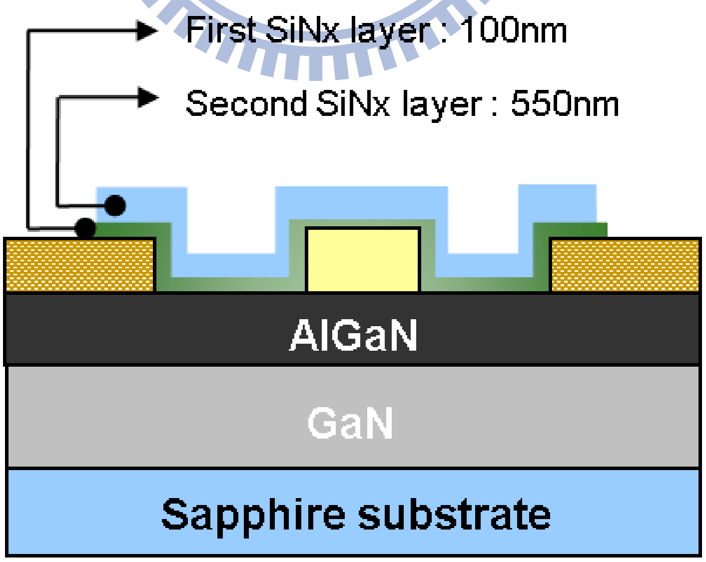

Figure 2-10. Cross-section of the HEMT device with a sequence of SiN_x passivation, including the first 100nm-thick SiN_x layer and the second 550nm-thick SiN_x layer.

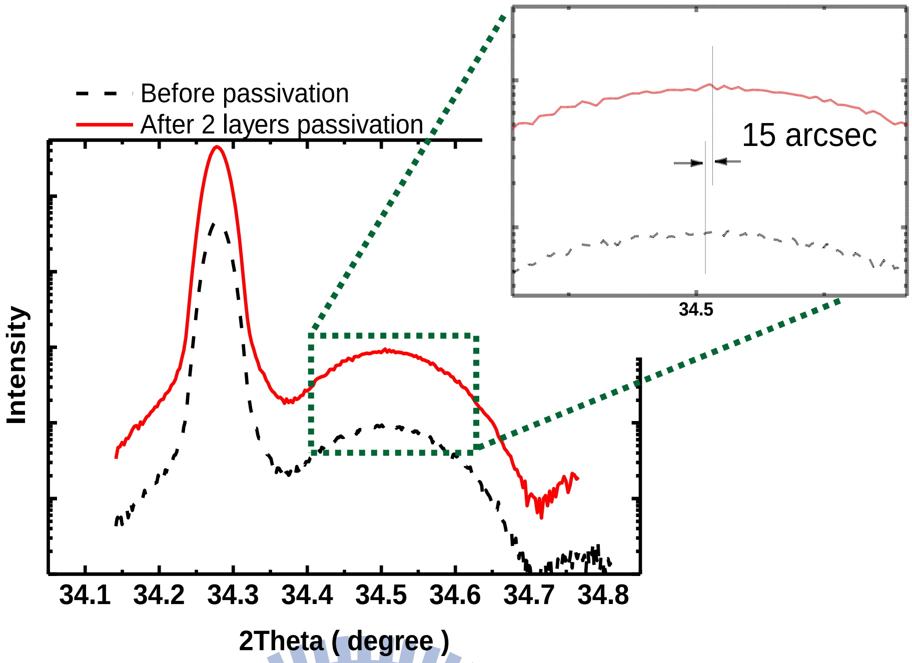

Figure 2-11. Omega-2Theta scan by high-resolution x-ray diffraction with an accuracy of ±7 arcsec.

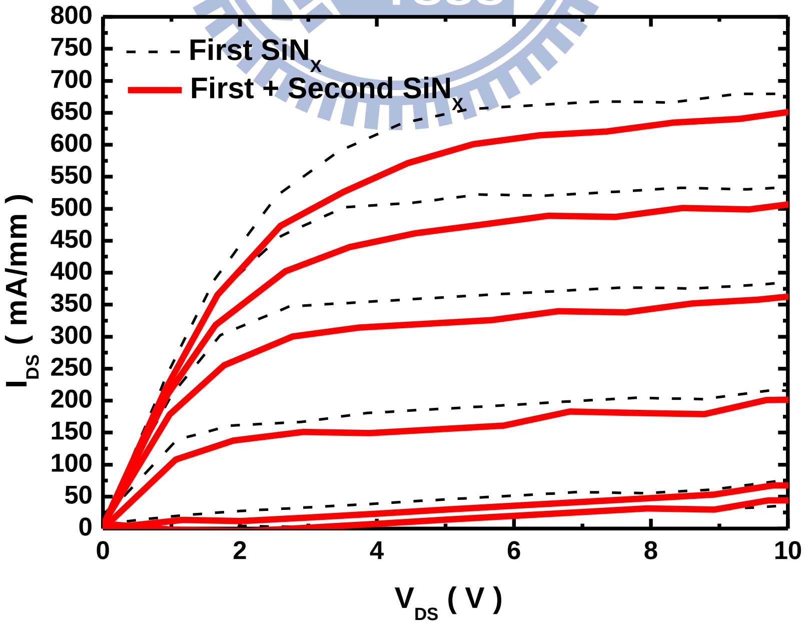

Figure 2-12. Transient characteristics(V_{GS} = $V_{pinch\text{-}off}$ to 0V, 1V/step) of the device before and after second layer passivation, , measured at the bias point of V_{GS} = $V_{pinch\text{-}off}$ and V_{DS} = 0 V.

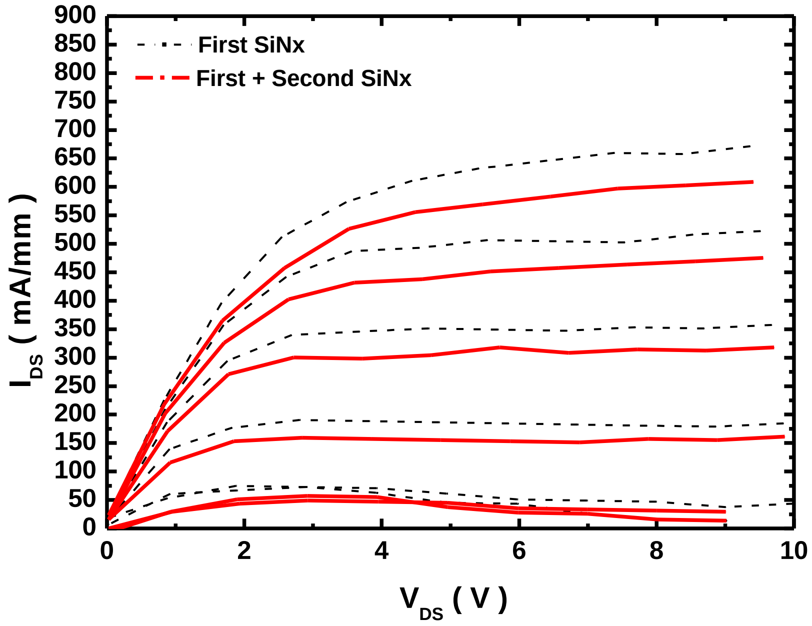

Figure 2-13. Transient characteristics (V_{GS} = $V_{pinch\text{-}off}$ to 0V, 1V/step) of the device before and after second layer passivation, , measured at the bias point of V_{GS} = $V_{pinch\text{-}off}$ and V_{DS} = 20 V.

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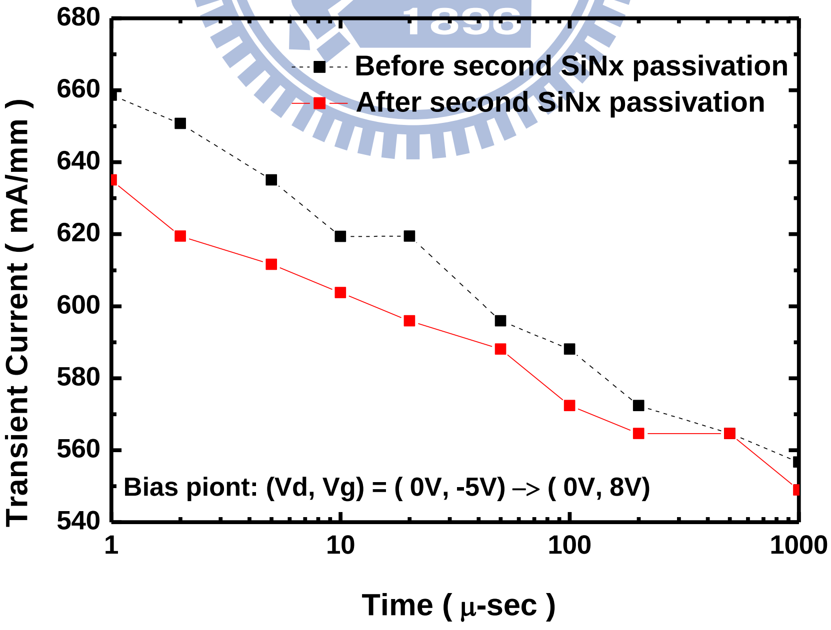

Figure 2-14. Transient current as a function of transient time measured from the bias point of V_{GS} = $V_{pinch\text{-}off}$ and V_{DS} = 0 V to the bias point of V_{GS} = 0V and V_{DS} = 8 V.

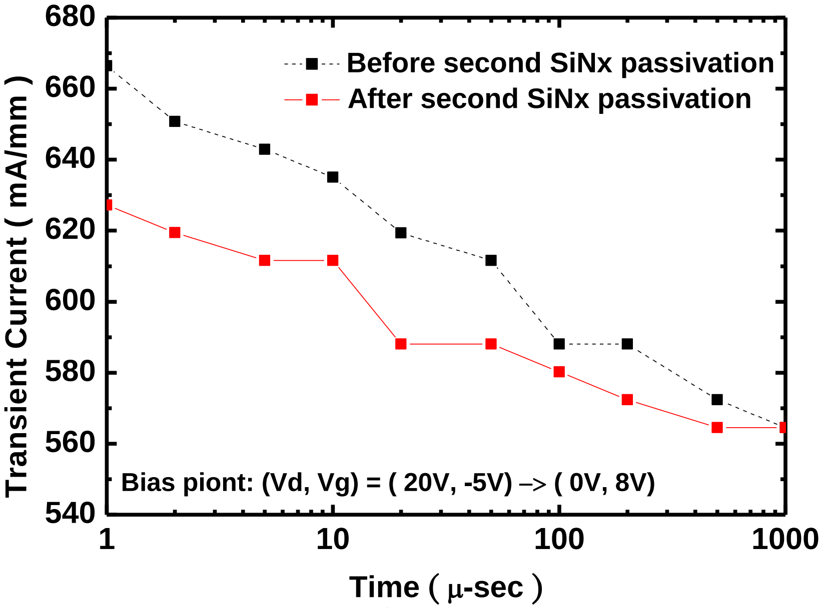

Figure 2-15. Transient current as a function of transient time measured from the bias point of $V_{GS} = V_{pinch\text{-}off}$ and $V_{DS} = 20$ V to the bias point of $V_{GS} = 0$V and $V_{DS} = 8$ V.

Chapter 3

30 GHz Low Noise Performance of 100nm-Gate-Recessed n-GaN/AlGaN/GaN HEMTs

3.1 Introduction

The power performance of gate-recessed AlGaN/GaN HEMTs at 30 GHz has been reported and the results demonstrate that they are suitable for high-frequency and high-power applications [3-1]. For low noise performance, GaN-based HEMTs can achieve a minimum noise figure (NF_{min}) of less than 2 dB over the frequency of 10–20 GHz [3-2, 3-3, 3-4, 3-5]. These results were achieved without a recessed gate and short channel effects were observed when the gate length was scaled down to the deep-submicrometer range. In this chapter, a heavily Si-doped GaN cap layer and a recessed gate were proposed to demonstrate the potential of GaN-based HEMTs for low noise applications up to 30 GHz.

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3.2 Device Fabrication

The AlGaN/GaN heterostructure was grown on a 3-inch (0001) sapphire substrate using metal-organic chemical vapor deposition (MOCVD). The epitaxial structure consisted of a nucleation layer, a 2-μm-thick GaN buffer layer, a 25-nm-thick $Al_{0.25}GaN_{0.75}N$ barrier layer, and a 5-nm-thick Si-doped (3×10^{18} cm^{-3}) GaN cap layer, as illustrated in Figure 3-1. The heavily Si-doped cap layer was proposed to reduce contact resistance [3-6]. Figure 3-2 shows the band diagram of the proposed structure, where Ec level is still higher than femi level as a Schottky gate contacting with n-GaN layer. Schottky barrier height here is assumed to be 1.1eV [3-7]. It suggests that the heavily Si-doped cap layer would not result in a leaky gate to degrade the device low noise performance.

The HEMT device fabrication started with ohmic-contact formation. Ti/Al/Ni/Au metal stacks (20/120/25/100 nm) were evaporated as ohmic metals and subsequently annealed at 800°C for 60 s in ambient N_2. An ohmic-contact resistance of 0.28 $\Omega \cdot$mm was obtained using the TLM method. Mesa isolation was formed utilizing inductively coupled plasma etcher with Cl2-based gas. For the T-shaped gate process, it was defined in the center of the 7 μm drain-source spacing by a 50 kV JEOL electron beam lithography system (JBX 6000 FS) with trilayer e-beam resist. The e-beam resist was also used as a mask for recess etching afterward. Before Ni/Au (20 nm/300 nm) gate metal deposition, gate recess was performed using inductively coupled plasma etcher with BCl_3 gas. The recess etching rate was controlled at 0.05nm per second. In this work, approximately 12 nm recess depth was etched to enhance the aspect ratio to around 5.5. Finally, gate metal was lifted off by acetone and dimethylacetamide (ZDMAC) to form a 100-nm T-shaped recessed gate. The gate width of the device in this work was 2 × 50 μm.

3.3 Device Characterization

The DC performance of the device was measured by Agilent E52702B. As shown in Figure 3-3, the drain current characteristics of the device with a 100 nm recessed gate exhibit a good pinch-off behavior, which is due to the enhanced aspect ratio by the gate recess technique. The off-state breakdown voltage is 90 V, as defined by the drain leakage current up to 1 mA/mm. Figure 3-4 shows the gate leakage current (I_G) during the device operation. It can be seen that the gate leakage current is lower than 2μA/mm at each bias point. Such a low leakage current might be attributed to the extremely low recess etching rate which helps reduce the damage caused during the dry etching process. After recessing, more than one order reduction in the reverse leakage current was observed using a Schottky diode, as shown in Figure 3-5. This finding was in agreement with that of Okamoto et al. [3-8]. They suggested that the reduction of leakage current after recessing is due to the suppression of the tunnelling component of the gate leakage current by slight removal of the surface n-type AlGaN. However, the mechanism is not understood clearly and needs further study. The pulsed I_D-V_D is shown in Figure 3-6, where the bias point is (V_{DS}, V_{GS}) = (0V, $V_{pinchoff}$). Comparing with DC I_D-V_D curve, it indicates that not much damage was induced due to the recess dry etching.

The S parameters of the fabricated device were measured using an on-wafer probing system with an Agilent E8361A network analyzer. The standard LRRM calibration method was adopted to calibrate the measurement system with reference planes set at the tips of the probes. Figure 3-7 shows the frequency dependence of the current gain H_{21} and Mason's unilateral gain U of the device measured at V_{DS} = 10 V and V_{GS} = −3 V. The parasitic effects (mainly capacitive) due to the probing pads have been carefully removed from the measured S parameters using the same method as in [3-9] and the equivalent circuit model in [3-10]. The unity current gain cutoff frequency (F_T) and the maximum frequency of oscillation (F_{MAX}) were extrapolated as 48 GHz and 75 GHz respectively using −20dB/decade regression.

High-frequency noise properties at room temperature were measured over the frequency range of 18–40 GHz using an Auriga noise measurement system with a Agilent 8975A noise figure analyzer. Figure 3-8 plots the 30GHz minimum noise figure (NF_{min}) as a function of gate bias at V_{DS} = 10V. The lowest noise figure of around 1.5dB can be obtained at gate bias of –3V. Figure 3-9 plots the minimum noise figure and the associated gain (G_{ass}) as a function of frequency at the bias point of VGS = −3V and VDS = 10V, where the lowest noise figure was achieved. A NF_{min} value of 1.2 dB (1.6 dB) with G_{ass} = 6.5dB (5dB) at 20 GHz (30 GHz) was observed. Such a low noise performance could be attributed to the low contact resistance of 0.28 Ω·mm, source resistance of 2.5Ω extracted from S parameters, and also the low gate leakage current of 0.9 μA/mm during the device operation. To the best of our knowledge, this 30 GHz noise performance is the best reported so far for GaN-based HEMTs with a recessed gate. Another important figure of merit used to characterize the performance of a broadband low-noise amplifier is the equivalent noise resistance Rn normalized to the optimal noise matching impedance $|Z_{opt}|$ ($|R_n/Z_{opt}|$)[3-11]. The fabricated device exhibited 0.47 (0.57) of $|R_n/Z_{opt}|$ at 20Ghz (40GHz) and an average value of 0.53 from 20 GHz to 40 GHz, indicating an excellent potential for broadband low-noise amplifier applications.

3.4 Summary

A minimum noise figure of 1.6 dB was obtained at 30 GHz, which could be attributed to the low gate leakage current as well as the low contact resistance due to the use of a heavily Si-doped GaN cap layer. Furthermore, an average value of 0.53 for $|R_n/Z_{opt}|$ from 20 GHz to 40 GHz was obtained.

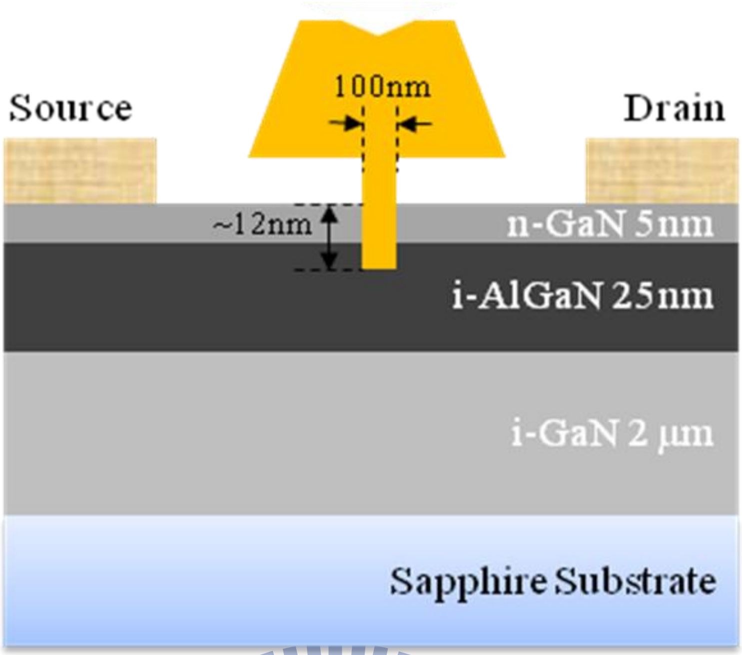

Figure 3-1. Cross section of 100nm-gate-recessed n-GaN/AlGaN/GaN HEMT.

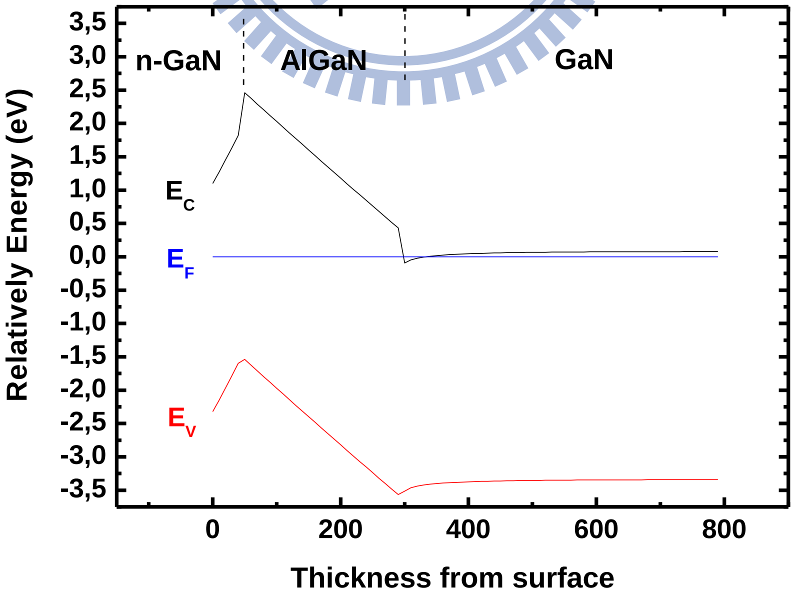

Figure 3-2. Band diagram for n-GaN/AlGaN/GaN with a Schottky contact.

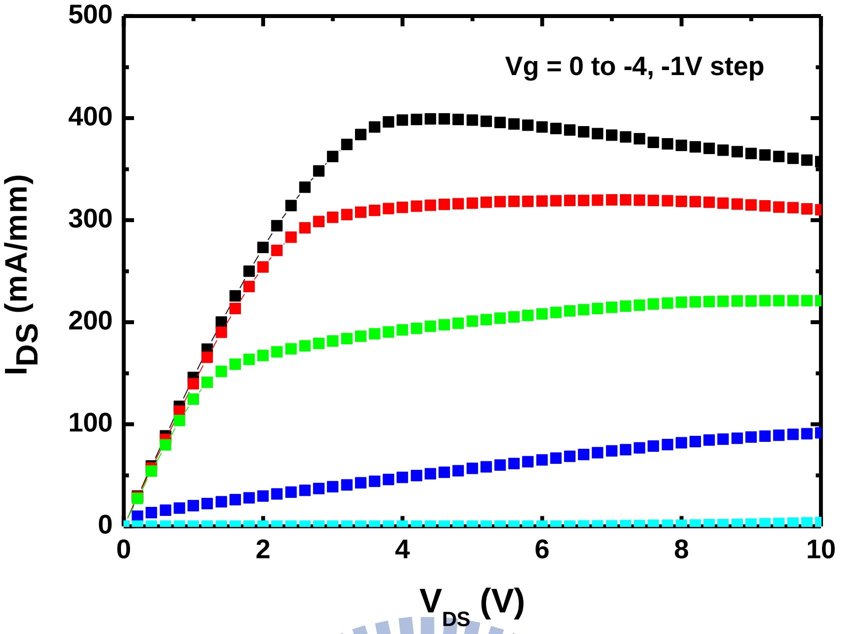

Figure 3-3. DC forward characteristics of 100nm-gate-recessed n-GaN/AlGaN/GaN HEMT.

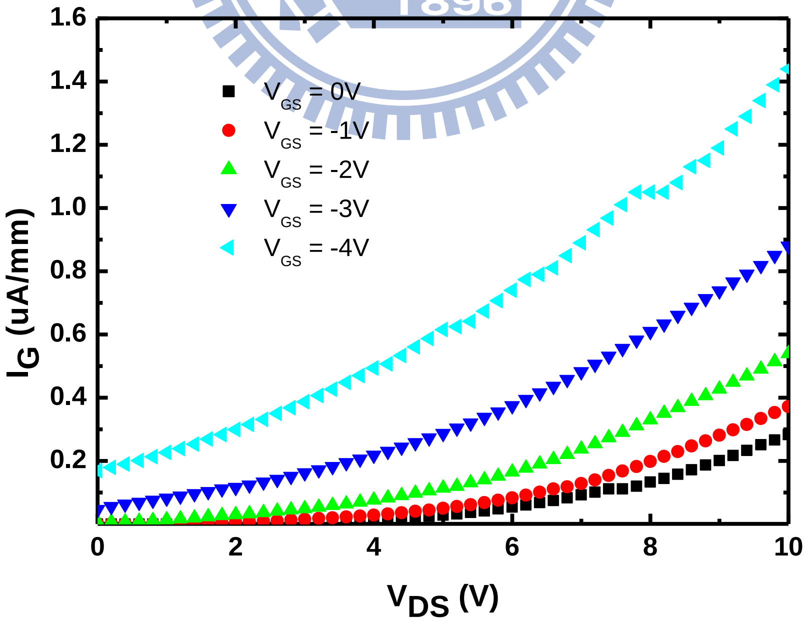

Figure 3-4. Gate leakage current density during the device operation.

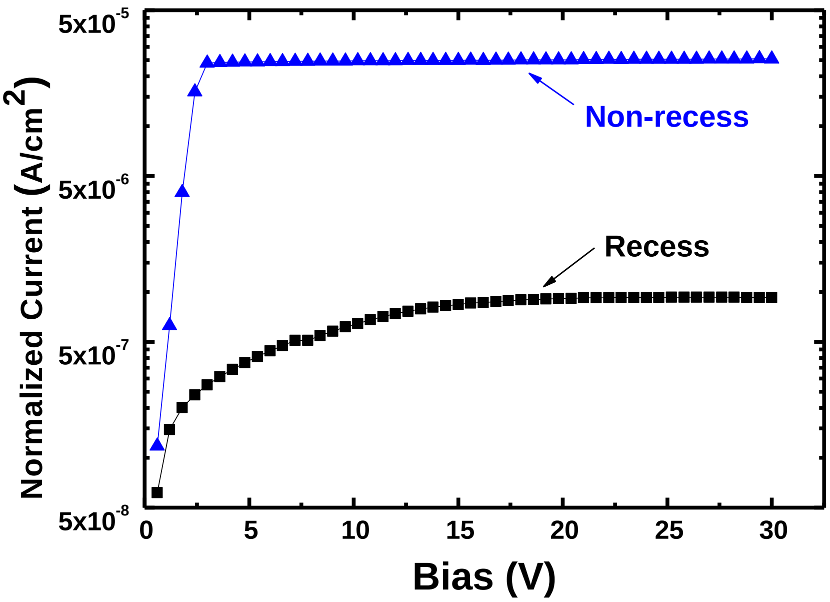

Figure 3-5. Reverse I-V characteristics of non-recessed and recessed Schottky diode.

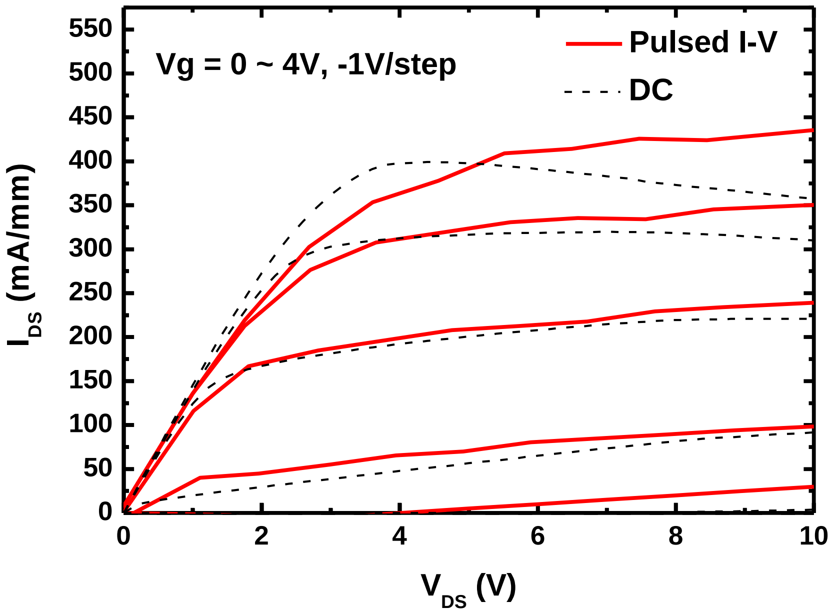

Figure 3-6. Pulsed I_D-V_D compared with DC forward I_D-V_D of the proposed device, which was measured at the bias point of (V_{DS}, V_{GS}) = (0V, Vpinchoff).

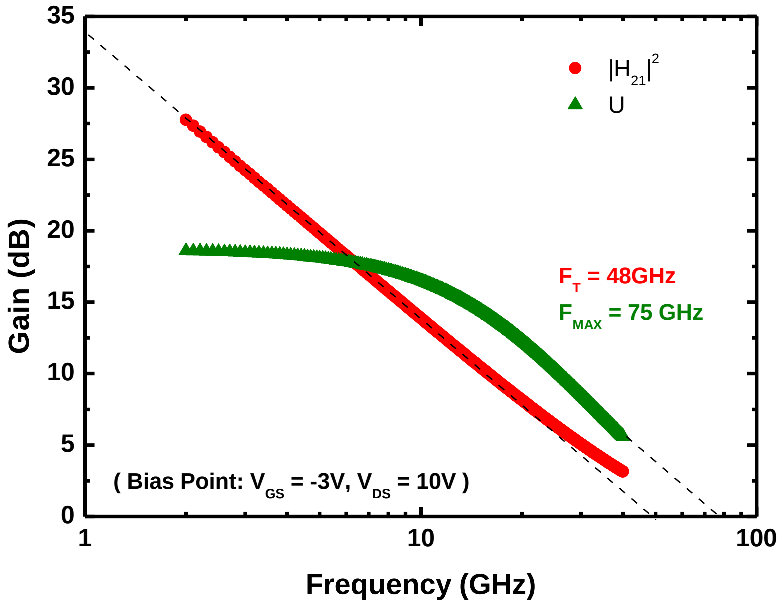

Figure 3-7. Intrinsic S-parameter performance of the device at bias point of V_{GS} = -3V, V_{DS} = 10V.

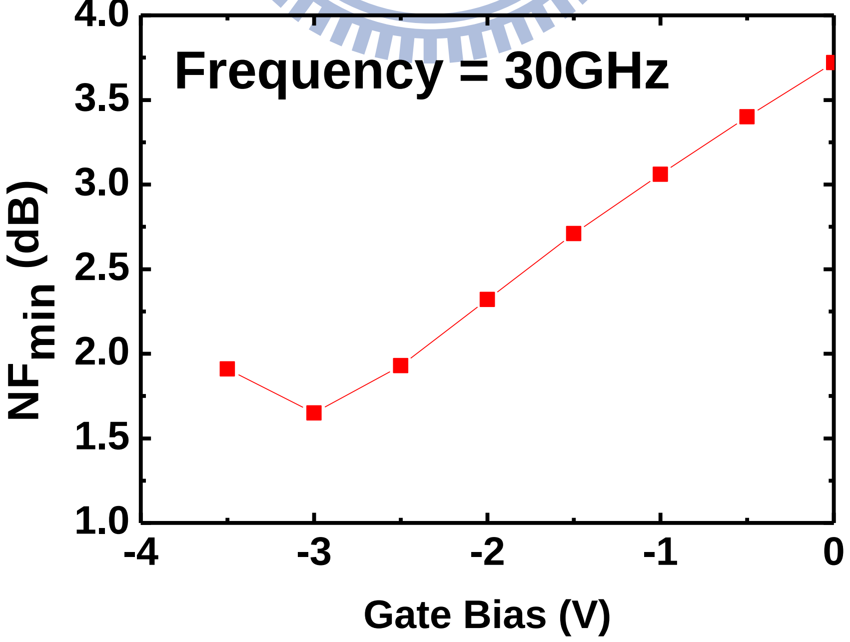

Figure 3-8. NF_{min} against gate bias at V_{DS} = 10V, and 30GHz.

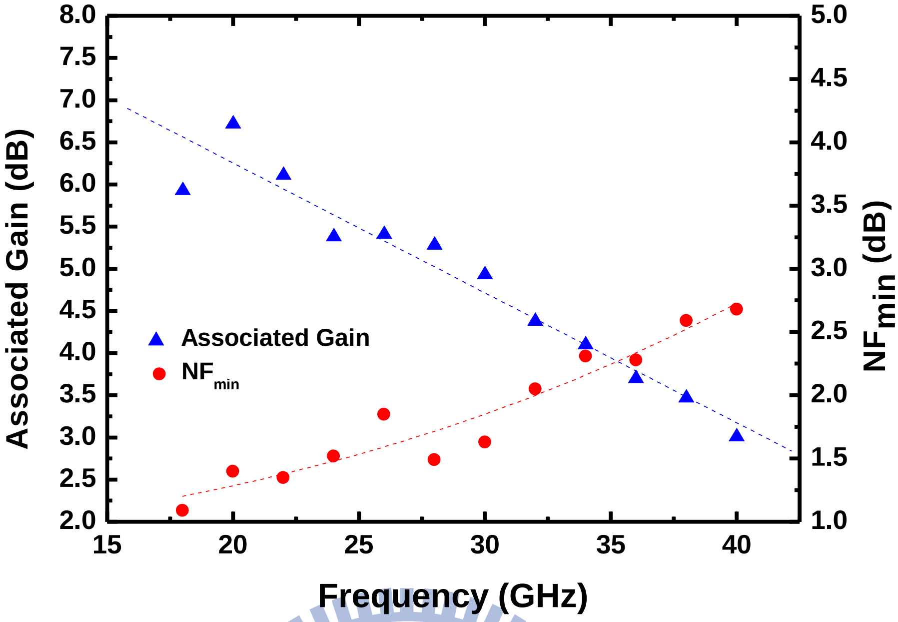

Figure 3-9. Frequency dependence minimum low noise figure (NF_{min}) and associated gain of the device at bias point V_{GS} = -3V, V_{DS} = 10V.

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Chapter 4

Normally-off Operation AlGaN/GaN MOS-HEMT with High Threshold Voltage

4.1 Introduction

In this Chapter, Fluorine-based treatment technique was used in combination with an Al_2O_3 film as gate oxide layer to demonstrate normally-off operation AlGaN/GaN MOS-HEMTs with high threshold voltage, of which the current density was comparable with conventional normally-on HEMTs.

4.2 Device Fabrication

An AlGaN/GaN heterojunction was grown on a 2-inch c-plane sapphire substrate using metal-organic chemical vapor deposition (MOCVD). The epitaxial structure consisted of a nucleation layer, a 2-μm-thick GaN buffer layer, a 1-nm-thick AlN interlayer, and a 13-nm-thick $Al_{0.25}Ga_{0.75}N$ barrier layer. The room-temperature Hall mobility and sheet electron concentration of the sample were 1900 cm^2/Vs and 8.8×10^{12} cm^{-2}, respectively.

Fabrication of the MOS-HEMTs started with ohmic-contact formation with 7 μm drain-source spacing. Ti/Al/Ni/Au metal stacks (20/120/25/100 nm) were evaporated as ohmic metals and subsequently annealed in N_2 ambient at 800°C for 1 min. Mesa isolation was formed utilizing inductively coupled plasma (ICP) etcher with Cl_2-based gas. A 100-nm-thick SiNx layer was deposited using plasma-enhanced chemical vapor deposition (PECVD) and then was patterned by lithography with 1-μm-width etching window in the center of the 7 μm drain-source gap. Before removal of the photo-resist, the SiNx was etched by reactive-ion etcher (RIE) with CF_4/O_2 gas mixture, and then the device was treated with CF_4 plasma, of which the condition was similar with that reported in [4-1]. Afterward, a 16-nm-thick Al_2O_3 oxide layer was deposited using atomic-layer deposition (ALD) and the devices were subsequently annealed at 400 °C for 10 min in N_2 ambient. The thermal annealing was not only for damage recovery [4-2] but also for post oxide-deposition annealing. Before gate metallization, electrode pads were patterned by lithography and the oxide layer was removed by wet etching with HF solution. Finally, a 3-μm-length gate was evaporated with Ni/Au (20/300 nm) to cover the F ion treatment region, as illustrated in Figure 1. The gate width of the devices in this work was 2 × 50 μm.

4.2 Device Characterization

DC performances of the devices were measured by Agilent E5270B. Figure 2 compares I_G-V_{GS} characteristics of normally-off operation HEMTs using F-based treatment technique with and without Al_2O_3 layer. In reverse and forward performances, the MOS-HEMT appeared lower gate leakage current than that of HEMT without oxide layer. The gate of the conventional device started to turn on at V_{GS} = 2 V, as defined by 1 mA/mm leakage current; however, the 16-nm-thick Al_2O_3 layer prevented the other device from not only Schottky gate leakage but also tunnelling leakage current up to V_{GS} = 12.7 V. Figure 3 compares I_{DS}-V_{GS} characteristics of the devices with and without oxide layer. Although the conventional device performed higher drain current and higher peak transconductance at V_{GS} = 5 V and 2.5 V, respectively, such performances suffered from huge gate forward leakage current which can be seen in Figure 2. On the contrary, the MOS device showed a peak transconductance of 100 mS/mm, and a drain current of approximately 500 mA/mm while the gate still maintained off at 11 V. This was higher than the drain current of 250 mA/mm obtained at V_{GS} turn-on voltage (V_{on}=2 V) from the device without oxide layer. Additionally, the threshold voltage was increased from 0.7 V to 5.1 V due to the insertion of Al_2O_3 gate oxide layer. Fig. 4-4 shows the benchmark of maximum drain-source saturation current (I_{DSS}) and V_{th} for the reported E-mode GaN-based HFETs. A high V_{th} of 5.1 V with high current density of 500 mA/mm were demonstrated in this work.

Pulsed I_{DS}-V_{DS} measurements were performed at bias points of V_{DS}=10V and V_{GS}=0V, as shown in Fig. 4-5. In order to reveal dispersion effects of the surface trap, we plotted DC I_D-V_D curve in the same figure as a reference. When gate was biased at 5 V with grounded drain voltage, pulsed I_{DS}-V_{DS} exhibited higher current density than DC one. About 50% increment of current density than that of DC measurement at V_{GS}= 10 V, which implied some charging effects would happen during DC measurement. At bias point V_{GS}= 0 V and V_{DS}= 10 V, the current density was even higher, with a drain current density of 750 mA/mm. Both pulsed I_{DS}-V_{DS} curves showed no dispersion effect due to surface traps, no current degradation, which could be attributed to SiNx passivation and Al_2O_3 gate insulator.

Fig. 4-6 shows the frequency response of F-based MOS-HEMT. The F_T and the F_{MAX} were 4.74 GHz and 12.24 GHz, respectively, when the device was biased at $V_{GS} = 7$ V and $V_{DS} = 10$ V. Compared with the device without gate insulator as shown in Fig. 4-7, the F_T of MIS-HEMT was almost the same, while the F_{MAX} of the MOS device exhibited better small-signal response. Better frequency response could be due to lower gate leakage current under bias point, which could be found in Fig. 4-2. According to above results, Al_2O_3/AlGaN/GaN MOS-HEMTs demonstrated the potential of RF electronics, and the RF response could be improved by scaling down gate length along with smaller source-drain spacing.

4.3 Summary

Lower gate leakage current and higher gate turn-on voltage, as compared with the conventional CF_4-treated normally-off device, was achieved by using the Al_2O_3 gate oxide layer. As a result, a high drain current density of 500 mA/mm was obtained at a gate voltage of 11V without the large gate leakage current, and the threshold voltage as high as 5.1 V was achieved.

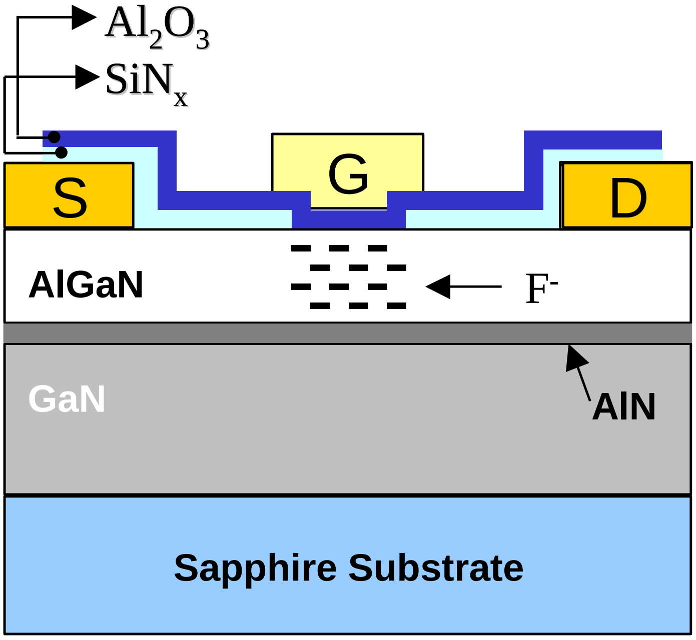

Figure 4-1. Schematic cross-section of the fabricated normally-off MOS-HEMT.

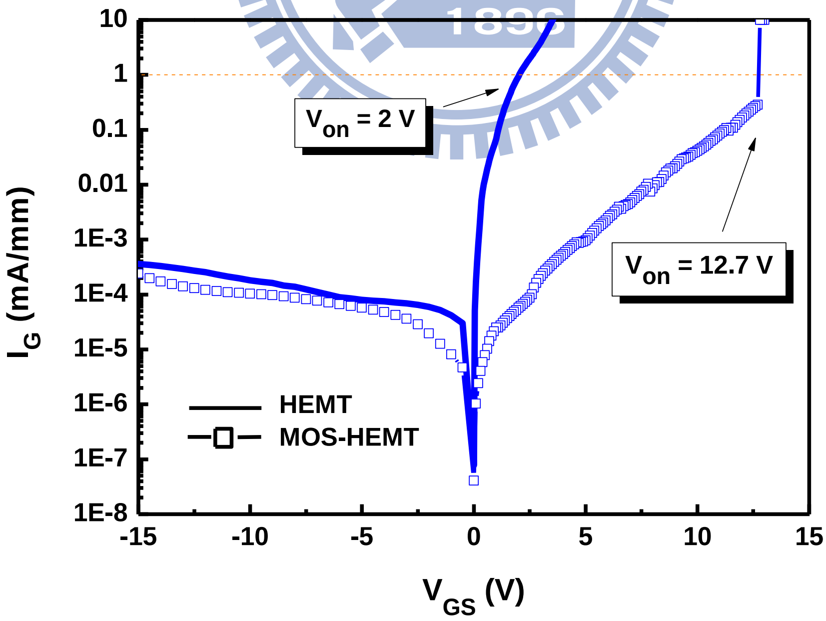

Figure 4-2. I_G-V_{GS} characteristics of the normally-off HEMT with and without gate oxide layer.

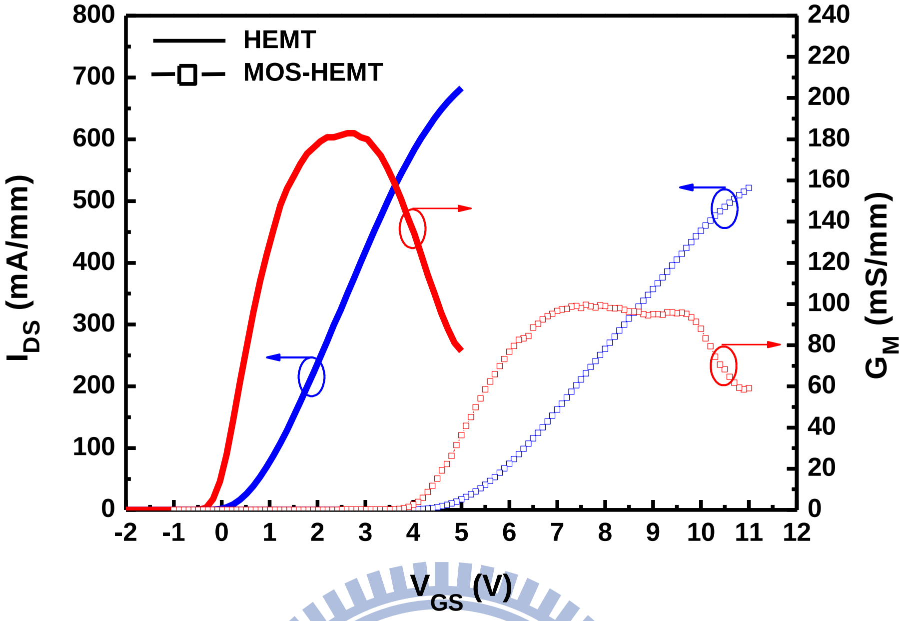

Figure 4-3. I_{DS}-V_{GS} characteristics of the normally-off HEMT with and without oxide layer.

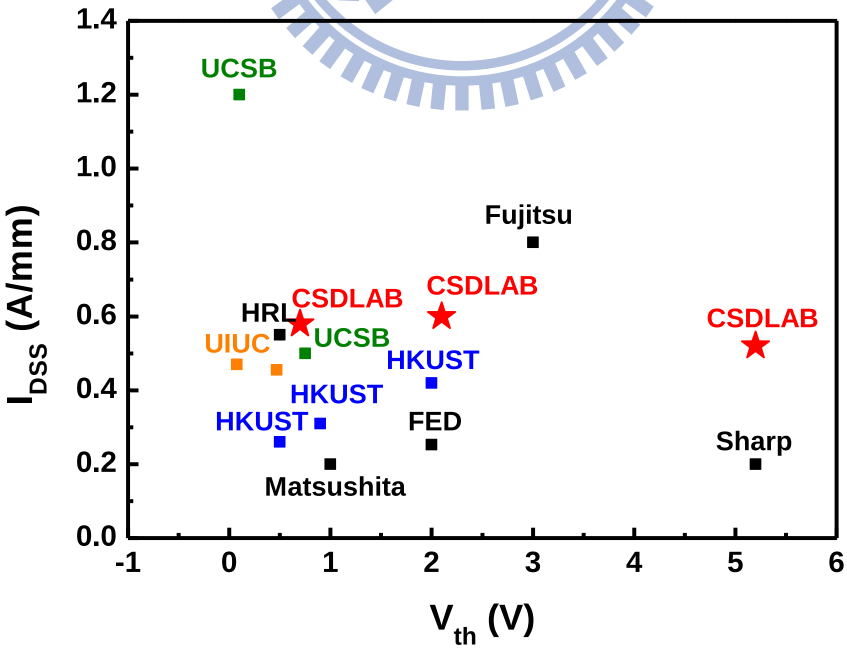

Figure 4-4. Benchmark of I_{DSS} and V_{th} for normally-off GaN-based HEMTs.

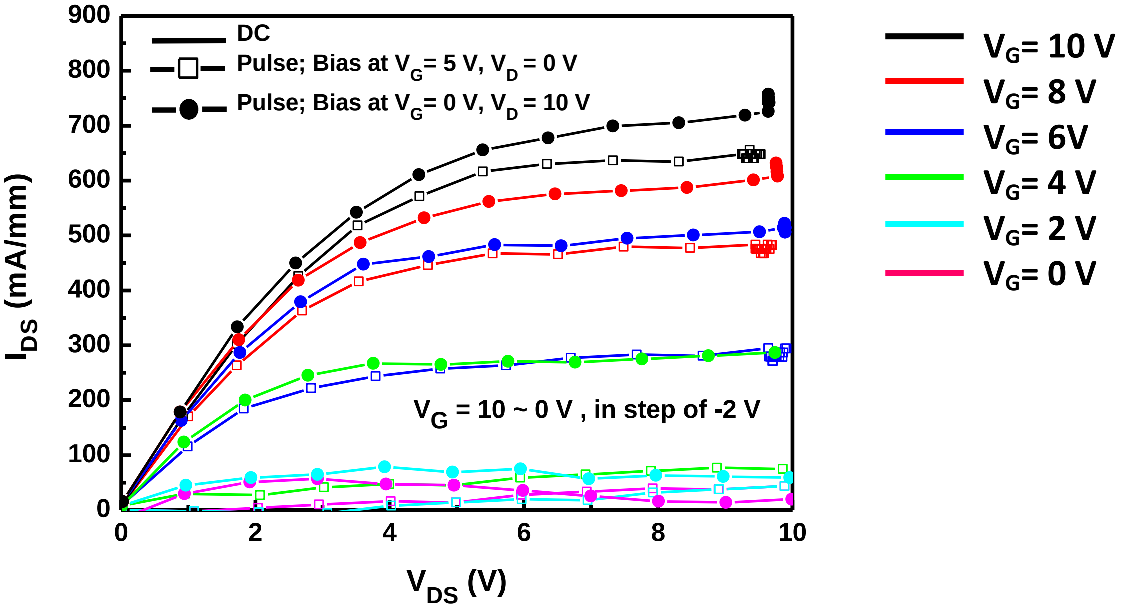

Figure 4-5. Pulsed I_{DS}-V_{DS} measurements of F-based normally-off Al_2O_3/AlGaN/GaN MOS-HEMT

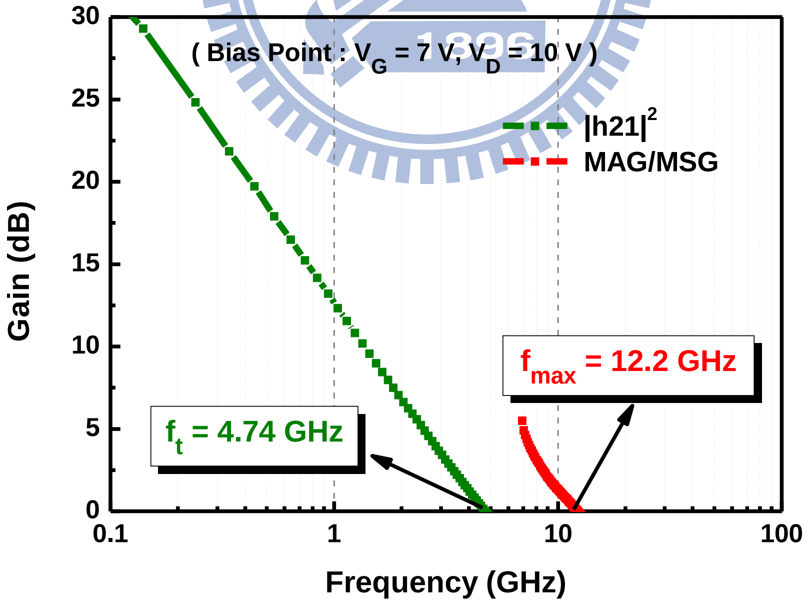

Figure 4-6. S-parameter performance of F-based normally-off MOS-HEMT at bias point of V_{GS} = 7 V and V_{DS} = 10 V.

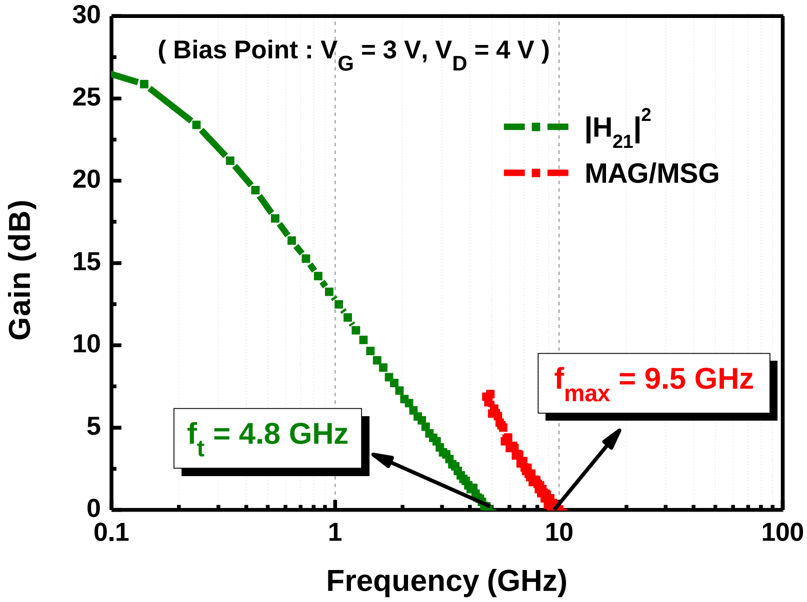

Figure 4-7. S-parameter performance of F-based normally-off HEMT at bias point of V_{GS} = 3V and V_{DS} = 4V

Chapter 5

Conclusion

For the strain experiments of the AlGaN/GaN HEMTs, the channel current density of devices can be modulated by applying uniaxial tensile strain. The magnitude of the change in current density depends on the gate orientation. Although this strain can enhance DC characteristics, it also severely degrades current recovery. Similar results from a SiNx passivation test suggest that tensile strain degrades the device transient performance. This could be attributed to the additional donor-like surface states induced by the additional piezoelectric polarization that the tensile strain produces. These findings could be useful for the optimization of SiNx passivation on AlGaN/GaN HEMTs and it also suggests that any tensile train which might occur during the device processing should be taken into consideration carefully.

For practical applications, the 100-nm gate-recessed AlGaN/GaN HEMT device was presented for 30 GHz low noise application. The minimum noise figure of 1.6 dB was obtained at 30 GHz, which could be attributed to the low gate leakage current as well as the low contact resistance due to the use of a heavily Si-doped GaN cap layer. Furthermore, an average value of 0.53 for $|R_n/Z_{opt}|$ from 20 GHz to 40 GHz was obtained, suggesting that such a device is a promising candidate for broadband low-noise amplifier applications in modern communication networks. Additionally, the normally-off operation AlGaN/GaN MOS-HEMT with high threshold voltage was demonstrated successfully. Lower gate leakage current and higher gate turn-on voltage, as compared with the conventional CF_4-treated normally-off device, was achieved by using the Al_2O_3 gate oxide layer. As a result, the high drain current density of 500 mA/mm was obtained at gate voltage of 11V without the huge gate leakage current, and the threshold voltage as high as 5.1 V was achieved. Such the device should be used for power electronic applications.

Appendix A

Benchmark of AlGaN/GaN HEMTs (CSDLab)

A.1 RF Power Application

The epi-structure of n-GaN 5nm / i-AlGaN 30nm / i-GaN 2μm was grown on a 3-inch semi-insulating SiC substrate using metal-organic chemical vapor deposition (MOCVD). The room temperature Hall mobility and sheet electron concentration of the wafer were 1800 cm^2/Vs and 1×10^{13} cm^{-2}, respectively.

The HEMT device fabrication started with ohmic-contact formation. Ti/Al/Ni/Au metal stacks (20/120/25/100 nm) were evaporated as ohmic metals and subsequently annealed at 800°C for 60 s in ambient N_2. Mesa isolation was formed utilizing inductively coupled plasma etcher with BCl_3/Cl_2 gases. An ohmic-contact resistance of 0.28 $\Omega\cdot$mm was obtained using the TLM method. For the gate metallization, it was defined in the center of the 7 μm drain-source spacing by a optical lithography system with double-layer resist stack (PMMA/Co-polymer), followed by the metal stack of Ni/Au (20 nm/300 nm) gate deposition by e-beam evaporator. After the lift-off process, a $50\times2\times0.7$ μm gate was formed. Afterward, a 100-nm-thick SiNx layer was deposited using plasma-enhanced chemical vapor deposition (PECVD). Finally, an air-bridge structure was electro-plated with 5 μm-thick gold. Figure A-1 illustrates the fabricated device cross-section with related geometry dimension.

Figure A-2~A-8 present DC and RF characteristics of the fabricated device. For the DC performance, the device demonstrated 800mA/mm, 275mS/mm, and higher than 100V of saturation current density, transconductance, and three-terminal breakdown voltage, respectively. For the small signal performance, the device demonstrated 18GHz and 50GHz of F_T and F_{MAX}, respectively. For the large signal performance, the device demonstrated 7W/mm, 5.5W/mm, and 5W/mm output power density at 2GHz, 3.5GHz, and 8GHz with 61.7%, 35.28%, and 26.23% power-add-efficiency, respectively.

A.2 High Voltage Application

The epi-structure of n-GaN 2.5nm / i-AlGaN 18nm / i-GaN 2.6µm was grown on a 4-inch Si substrate using metal-organic chemical vapor deposition (MOCVD). The room temperature Hall mobility and sheet electron concentration of the wafer were 1500 cm^2/Vs and 1×10^{13} cm^{-2}, respectively.

Normally-on and Normally-off HEMT devices were both fabricated, which started with ohmic-contact formation. Ti/Al/Ni/Au metal stacks (20/120/25/100 nm) were evaporated as ohmic metals and subsequently annealed at 800°C for 60 s in ambient N_2. Mesa isolation was formed utilizing inductively coupled plasma etcher with BCl_3/Cl_2 gases. For the normally-off device, the fluorine plasma treatment was done underneath the gate region prior to gate metallization. The 3µm-length gate metallization was defined by an optical lithography system with double-layer resist stack (PMMA/Co-polymer), followed by the metal stack of Ni/Au (20 nm/300 nm) gate deposition by e-beam evaporator. After the lift-off process, a 20mm-width gate was formed. Afterward, a 600-nm-thick SiNx layer was deposited using plasma-enhanced chemical vapor deposition (PECVD) and then the electrode pads were patterned for interconnection. Finally, an air-bridge accompanied with a source field plate structure was electro-plated with 5 µm-thick gold. Figure A-9 and A-10 illustrate the cross sections of the fabricated devices.

Figure A-11~A-16 show the DC forward and reverse characteristics of the normally-on and the normally-off devices. For the normally-on device, it performed higher than 1A of channel current and higher than 575mS of transconductance. The measured horizontal lines appeared on Figure A-11and A-13 is due to the limitation of the measurement facility. For the normally-off device, it performed 0.7A of channel current and 500mS of transconductance. The three-terminal breakdown voltage of both devices is higher than 200V. Extension voltage was not measured also due to the limitation of the measurement equipment.

Figure

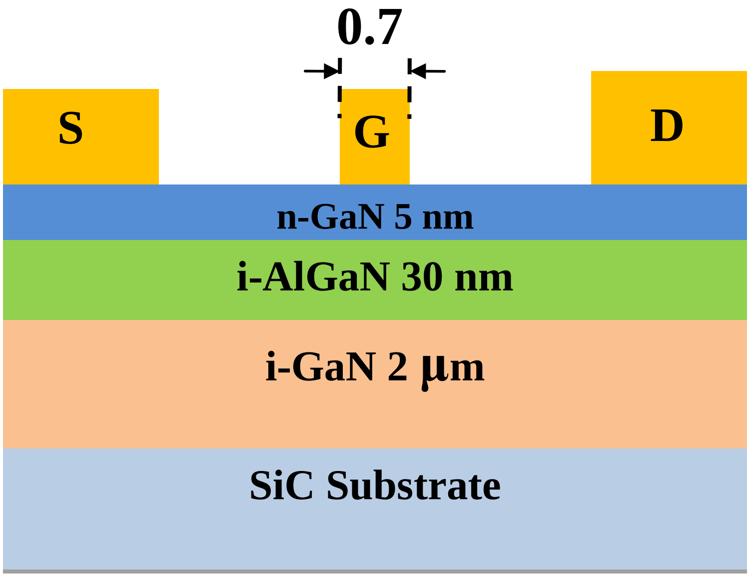

Figure A-1. Schematic diagram of the fabricated AlGaN/GaN HEMT for RF power application.

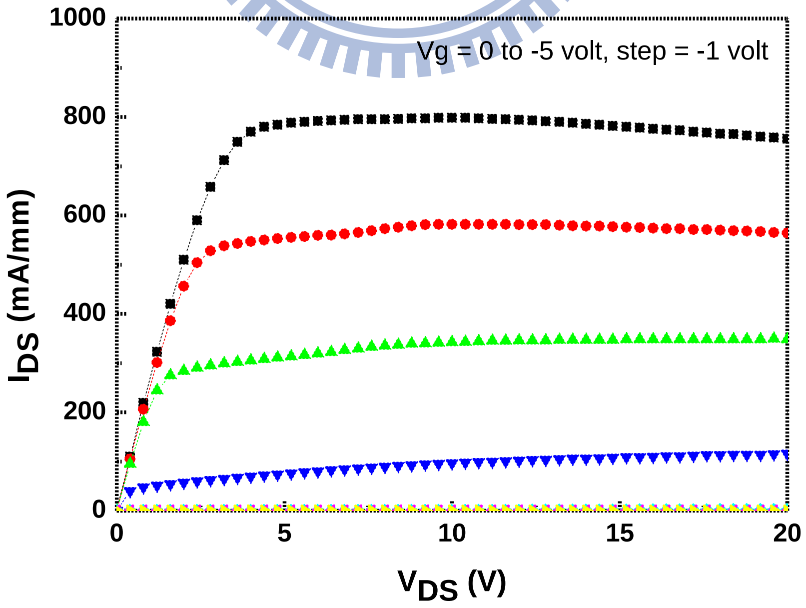

Figure A-2. DC output characteristics of AlGaN/GaN HEMTs for RF power application.

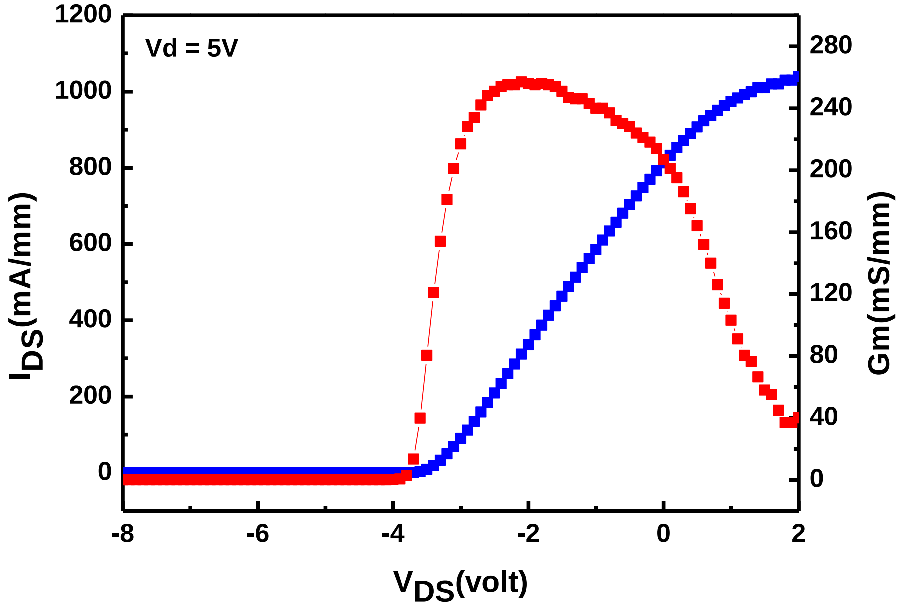

Figure A-3. Transconductance characteristics of AlGaN/GaN HEMTs for RF power application.

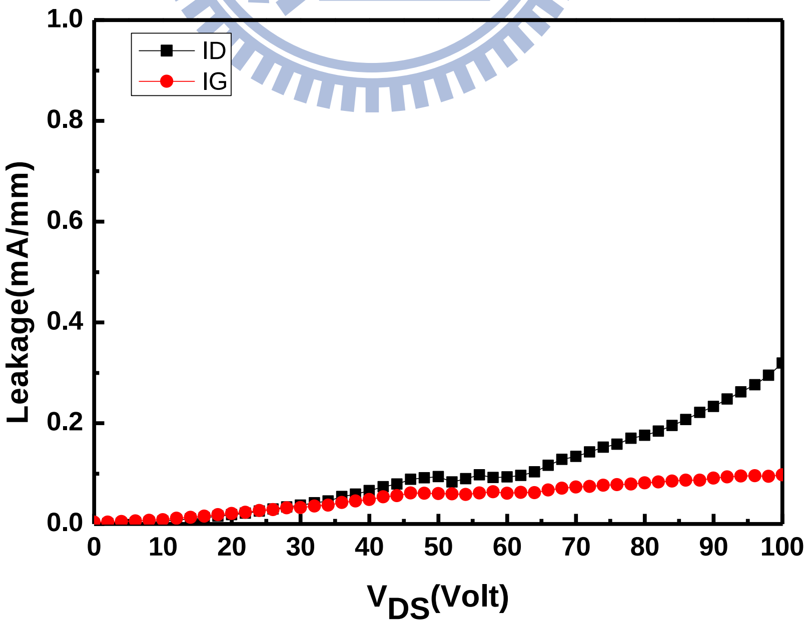

Figure A-4. Three-terminal off-state characteristics of AlGaN/GaN HEMTs for RF power application.

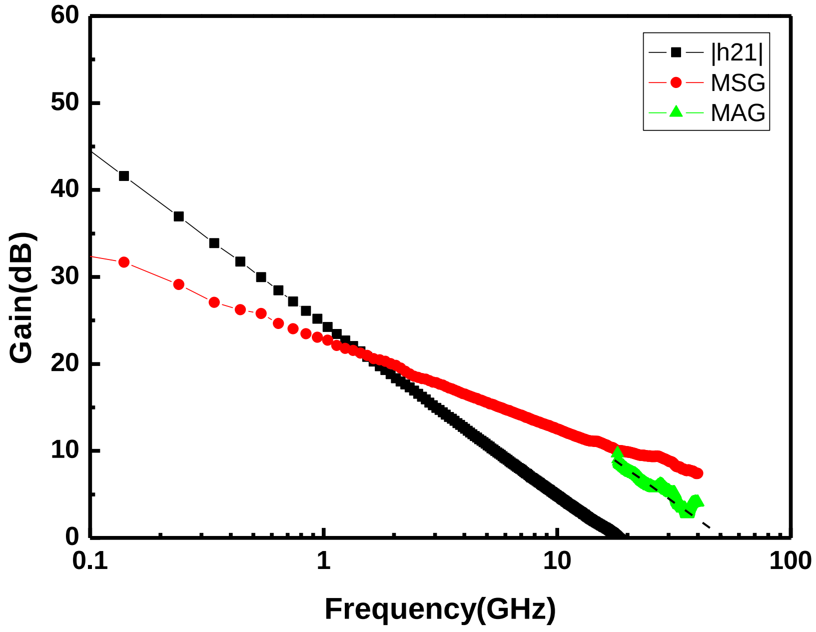

Figure A-5. Small-signal characteristics of AlGaN/GaN HEMTs for RF power application. Bias-point is V_{GS} = -2.5V and V_{DS} = 10V.

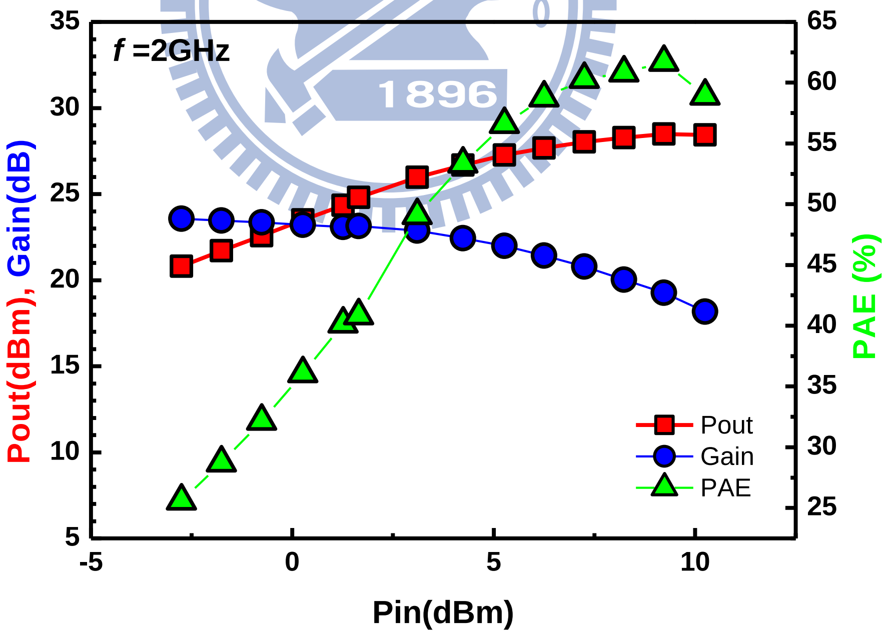

Figure A-6. Large-signal characteristics of AlGaN/GaN HEMTs at 2GHz for RF power application. Bias-point is V_{GS} = -3.5V and V_{DS} = 30V.

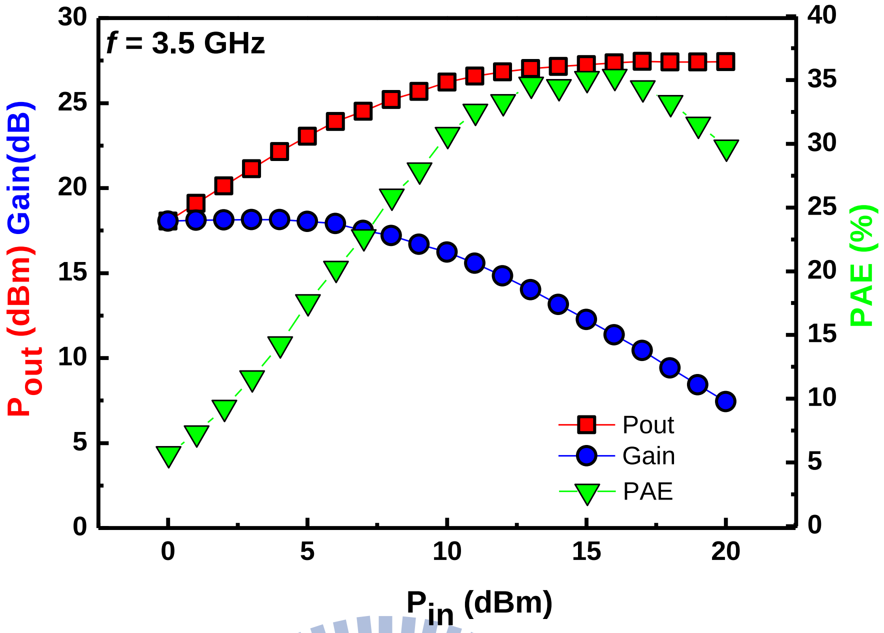

Figure A-7. Large-signal characteristics of AlGaN/GaN HEMTs at 3.5GHz for RF power application. Bias-point is V_{GS} = -2V and V_{DS} = 30V.

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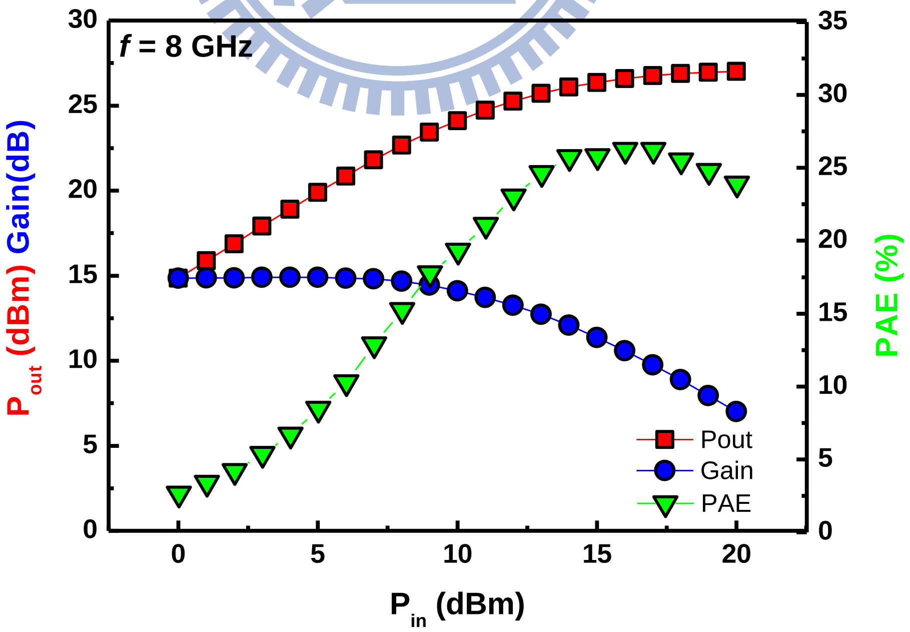

Figure A-8. Large-signal characteristics of AlGaN/GaN HEMTs at 8GHz for RF power application. Bias-point is V_{GS} = -2V and V_{DS} = 30V.

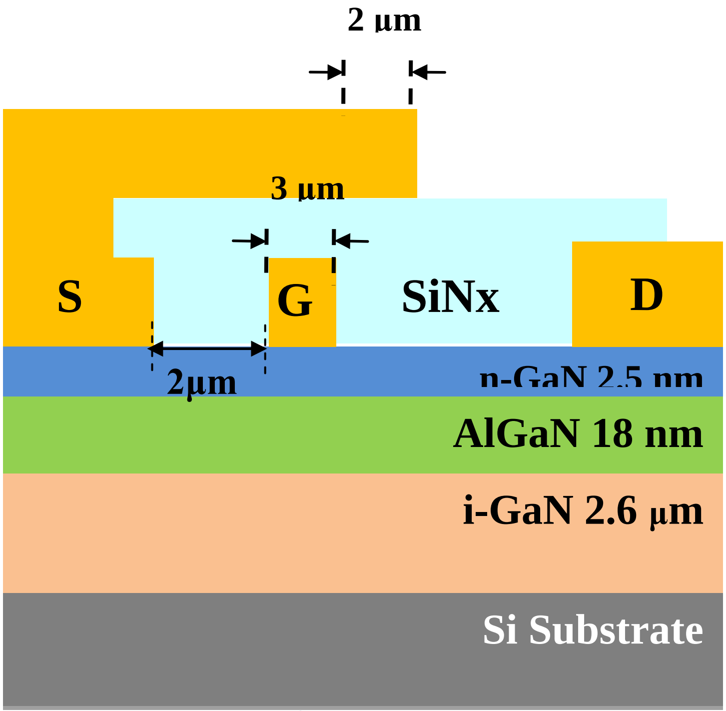

Figure A-9. Schematic diagram of the fabricated normally-on AlGaN/GaN HEMT for high voltage application.

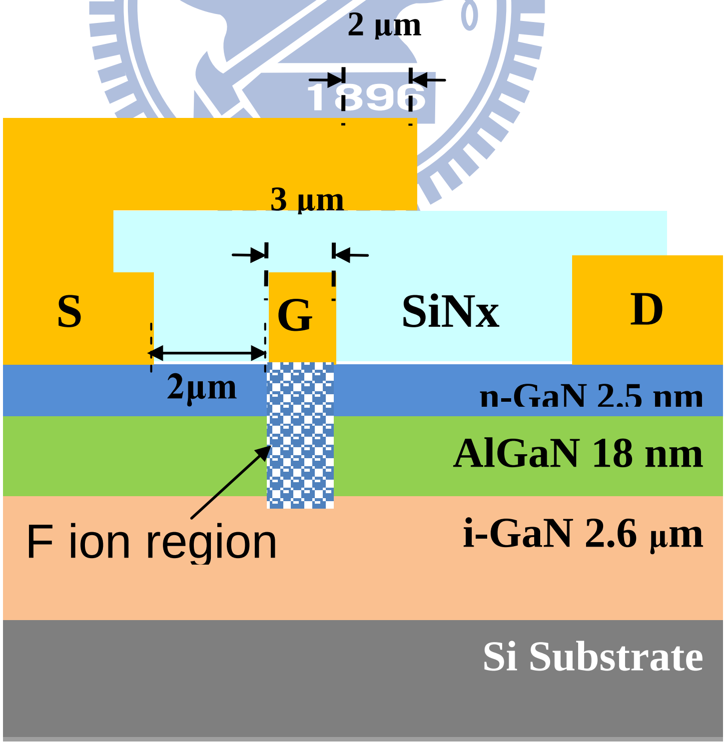

Figure A-10. Schematic diagram of the fabricated normally-off AlGaN/GaN HEMT for high voltage application.

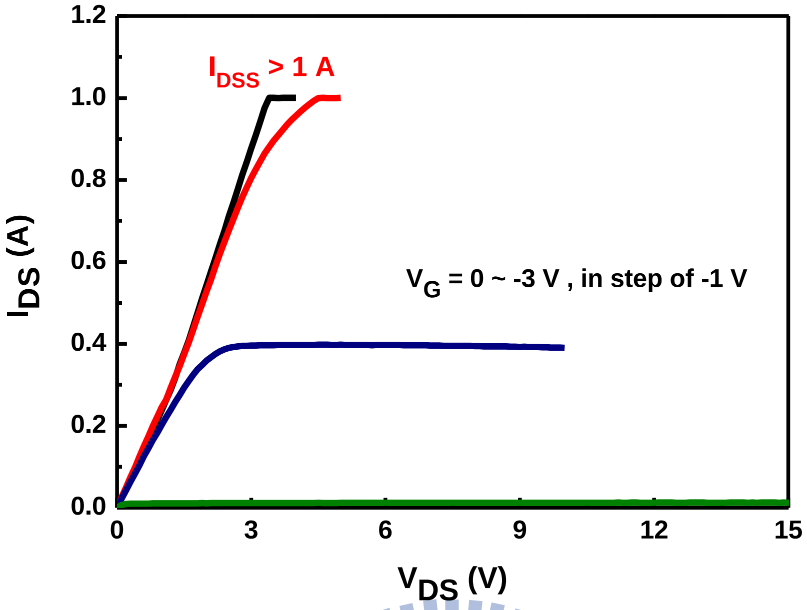

Figure A-11. DC output characteristics of normally-on AlGaN/GaN HEMTs with 20-mm gate width.

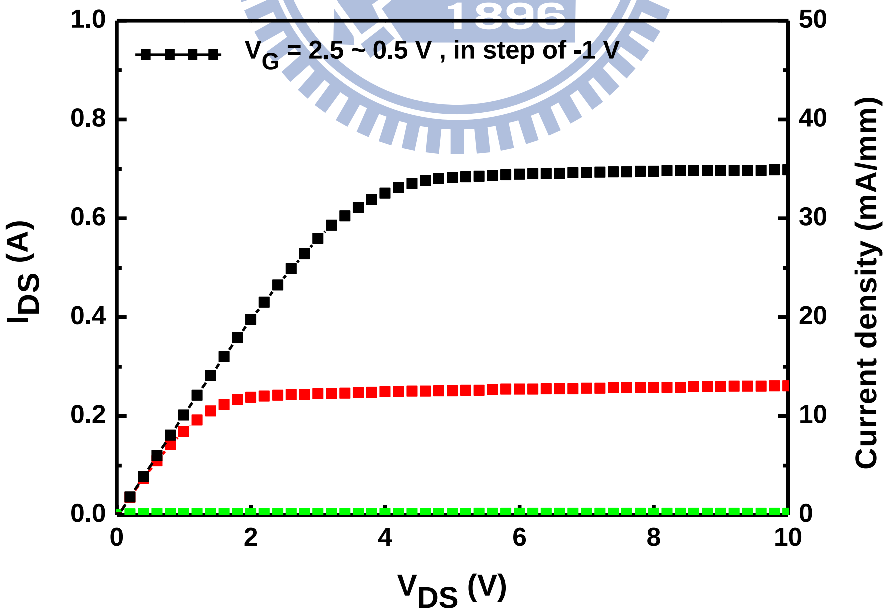

Figure A-12. DC output characteristics of normally-off AlGaN/GaN HEMTs with 20-mm gate width.

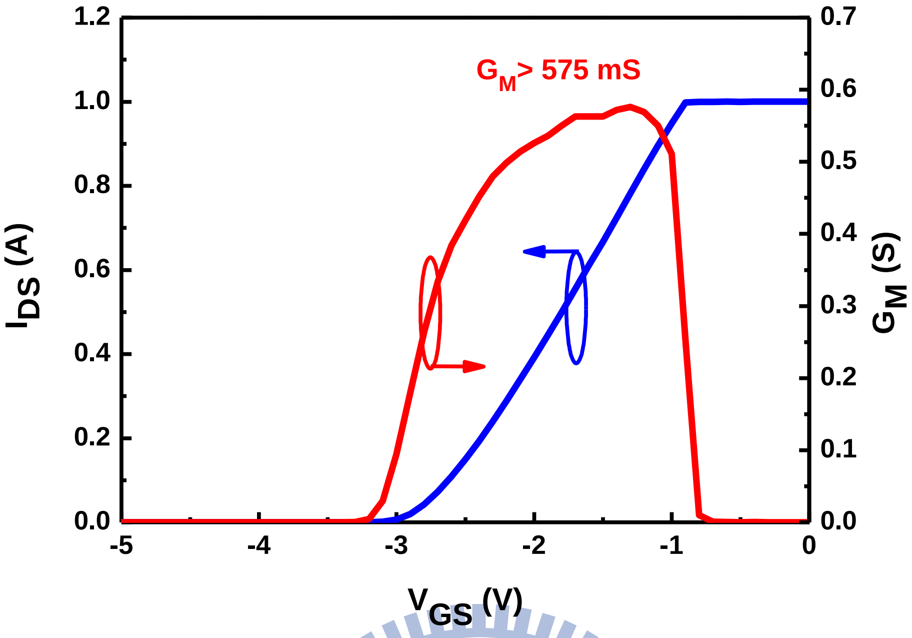

Figure A-13. Transconductance characteristics of normally-on AlGaN/GaN HEMTs with 20-mm gate width.

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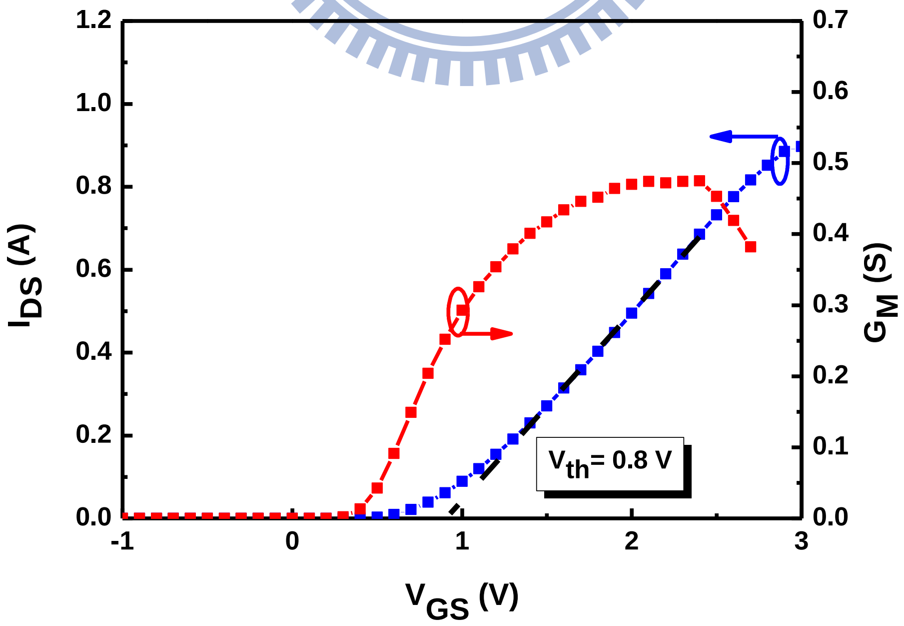

Figure A-14. Transconductance characteristics of normally-off AlGaN/GaN HEMTs with 20-mm gate width.

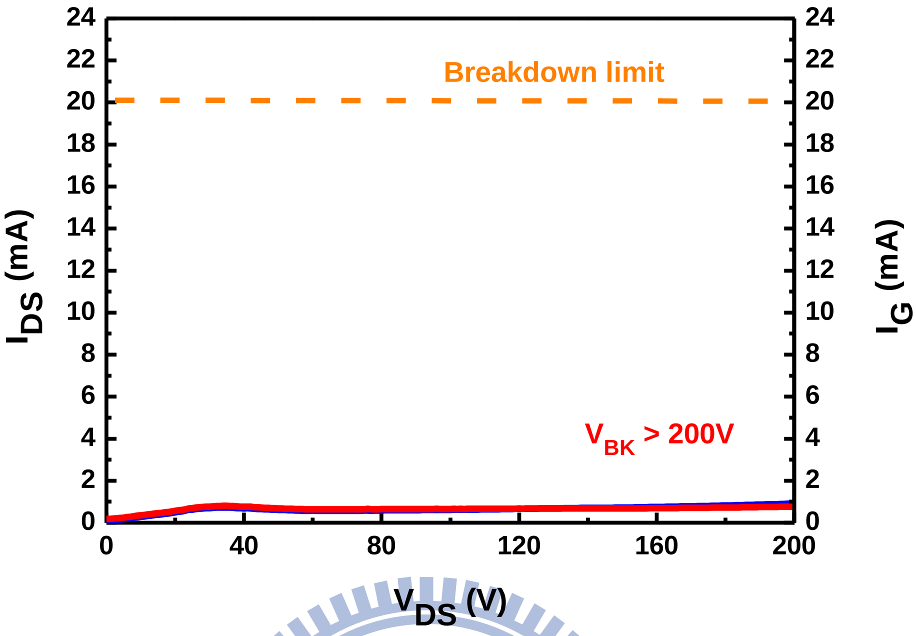

Figure A-15. Three-terminal off-state breakdown of 20-mm gate-width normally-on AlGaN/GaN HEMTs.

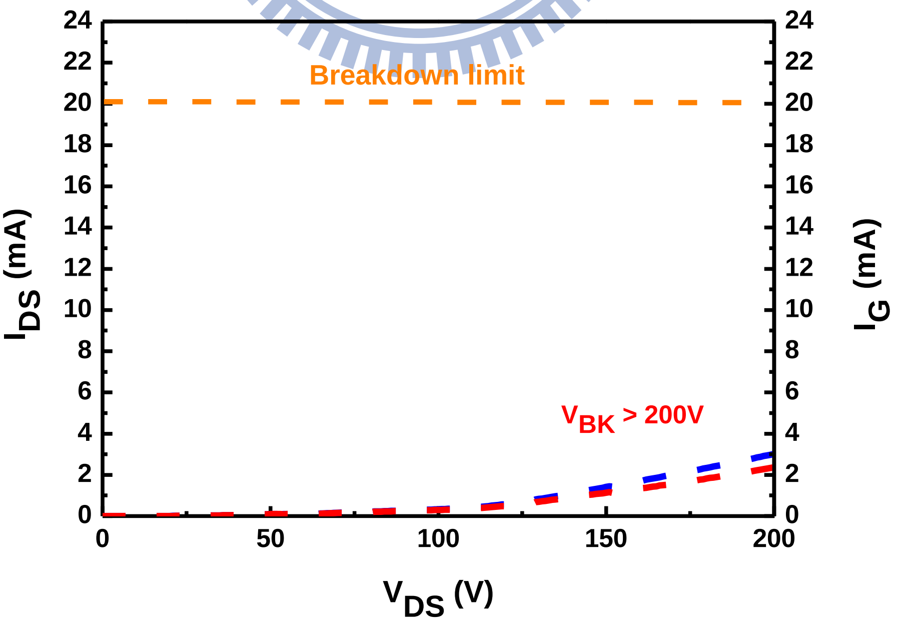

Figure A-16. Three-terminal off-state breakdown of 20-mm gate-width normally-off AlGaN/GaN HEMTs.

Appendix B

InGaN-based LEDs Grown on Fully Inclined Hemisphere-Shape-Patterned Sapphire Substrate with Submicron Spacing

B.1 Introduction

For optoelectronic devices, InGaN-based light-emitting diodes, investigations on these GaN devices reveal that the quality of epitaxial material is the predominating factor for the device performances. These devices are generally grown on sapphire substrate; however, a high threading dislocation density with the order of 10^9-10^{10} cm^{-2} is induced due to the large lattice mismatch between GaN-based film and sapphire substrate [B-1, B-2]. The approach using patterned sapphire substrate (PSS) to solve this problem has been typically reported [B-3, B-4]. Figure B-1 shows cross section transmission electron microscope (TEM) images of GaN buffer grown on conventional and patterned sapphire substrate. LEDs performance can be enhanced by PSS technique due to the reduction of dislocation density by the lateral growth mechanism. Additionally, it was found that inclined facets of patterned sapphire substrate were another important factor for the enhancement of performance due to the increase of light extraction by such facets [B-5], as illustrated in Figure B-2. Furthermore, smaller spacing between each pattern was also found to help enhance the LEDs performance [B-6]. Figure B-3 shows atomic force microscope (AFM) images of cone-shaped patterned sapphire substrates with different spacings. The LEDs grow on the substrate with spacing of 1μm had the best output power performance, as shown in Figure B-4.

A thermally reflowed photoresist technique was used to fabricate inclined PSS using dry etching and to increase the pattern density by reducing the spacing to submicron scale. To the author’s acknowledgement, such submicron scale spacing is the smallest ever reported for patterned sapphire substrate at least up to 2009 year. In this Chapter, the improvement of the GaN film quality and the performances of the

GaN LEDs grown on such substrates were examined by materials analysis, and electrical and optoelectronic characterization.

B.2 Diode Fabrication

Fabrication of patterned sapphire substrates (PSS) was accomplished by process steps as shown in Figure B-5. A SiN_x film was first deposited on 2-inch sapphire substrate by PECVD method (plasma-enhanced chemical vapor deposition) as etching mask and was patterned using polymethyl methacrylate (PMMA) by contact aligner with Deep UV lamp. Then, the spacing of the developed structure was reduced using thermal reflow technique. Figure B-6 shows the SEM (Hitachi S4700) images of spacing variation with the thermal reflow time. A spacing of 0.5μm was achieved while reflow time was up to 2min, of which cross-section SEM image is shown in Figure B-7. After the hemisphere-like profile was transferred to SiNx by reactive ion etcher, the sapphire substrate was then etched utilizing inductively coupled plasma etcher with BCl_3 plasma. By altering the thickness ratio between PMMA and SiNx, a mesa-shape and a hemisphere-shape-patterned sapphire substrate (MPSS and HPSS) were obtained, of which the cross-section SEM images are shown in Figure B-8. The height of each PSS was 1μm. Figure B-9 shows the top-view SEM image of the patterned sapphire substrates (MPSS and HPSS). The diameter and the closest spacing of the hemisphere on both substrates were 4.3μm and 0.5μm, respectively.

The InGaN-based LEDs were grown on c-plane 2inch-diameter patterned sapphire substrate (PSS) and conventional sapphire substrate (CSS) using metal-organic chemical vapor deposition (MOCVD). The epitaxial structure consisted of an undoped GaN buffer layer, a Si-doped n-type GaN layer, an active region with five periods of InGaN/GaN multiple quantum wells, an undoped $Al_{0.05}Ga_{0.95}N$ layer, and an Mg-doped p-type GaN layer. The epi-structure was confirmed using Omega-2Theta scan by high-resolution x-ray diffraction (Bede D1) and relevant lattice architecture simulation, as shown in Figure B-10. The epitaxial wafers were fabricated by the conventional LEDs process flow as described below. The p-GaN layer was partially etched to the n-GaN layer to define the device size of 350×350μm^2. 300nm-thick indium tin oxide (ITO) layer was deposited and then patterned on the p-GaN layer. Finally, a metal stack of Ti/Al/Au was evaporated onto both p-GaN and n-GaN layers as contact electrodes. Figure B-11 illustrates the cross-section of the finished InGaN-based LEDs on PSS.

B.3 Results and Discussion

Figure B-12 shows the cross-section TEM (JEOL 2100) bright field images of GaN buffer layer grown on mesa-shape and hemisphere-shape-patterned sapphire substrate (MPSS and HPSS), respectively. As shown in Figure B-12(a), there are two voids observed clearly near the mesa-shape edge for MPSS. These voids were thought to be the evidence of free standing laterally growth GaN which helps reduce the threading dislocation density [B-7]. For HPSS, however, no void was observed but 90^o bending dislocations appear above the hemisphere shape region, as shown in Figure B-12(b). It suggests HPSS prevent dislocation propagation in c-axis direction and reduce the threading dislocation density. The founding is similar to the GaN grown on cone-shape-patterned sapphire substrate reported by J. H. Lee, *et al* [B-8]. To further realize the 90^o bending dislocations found in HPSS sample, another two TEM bight field images under multiple-beam and two-beam condition were taken, as show in Figure B-13. By comparing both TEM images, it can be concluded that the 90^o bending dislocations are edge dislocations since the edge dislocations are invisible under the two beam condition of g = (002).

To compare the dislocations density of the GaN buffer layer grown on CSS, MPSS, and HPSS, rocking curve of high-resolution x-ray diffractions were performed with an accuracy of ±7 arcsec and the results are shown in Figure B-14. In Figure B-14(a), the full width at half maximum (FWHM) of the (002) plane rocking curves of the GaN films grown on each substrate were 274arcsec, 277arcsec, and 256arcsec, respectively. These similar results could be due to that the rocking curves of the symmetric planes, such as (002) plane, is insensitive to the edge threading dislocations which are the predominant component for the threading dislocations in GaN films grown on sapphire [B-9]. It has been reported that the pure edge threading dislocations distort the asymmetric planes so that the rocking curves of asymmetric planes are required to analyze the pure edge threading dislocations of the GaN films [B-10]. Figure B-14(b) compares the asymmetric (102) plane rocking curves of GaN grown on CSS and PSS. In comparison with GaN grown on CSS, the FWHM of GaN decreases from 480arcsec to 293arcsec and 262arcsec for MPSS and HPSS, respectively. It indicates that the quality of the GaN film grown on PSS was improved and GaN on HPSS was slightly better than that on MPSS.

Figure B-15 shows the electrical characteristics of the LEDs grown on CSS and HPSS. It can be seen that the leakage current was reduced by more than one order at –30V by using HPSS technique. This can be contributed to the better material quality of the GaN buffer grown on HPSS. Fig B-16 plots the EL spectrum of the LEDs on each substrate. Under the driving current of 20mA, the wavelength of each LED was approximately 460nm. Figure B-17 plots the light-output power as a function of the injection current for non-encapsulated 460nm-LEDs grown on CSS and PSS, where the output power was measured using an integrated sphere detector. The output powers were 4.05mW, 5.32mW, and 5.86mW for CSS, MPSS, and HPSS, respectively, under the typical driving current of 20mA. As compared with LEDs on CSS, the output power of LEDs on MPSS and HPSS were enhanced by 31% and 44%, respectively. It has been reported that the inclined facets of the PSS can redirect photons back to the device surfaces so that the efficiency of the light extraction can be increased [B-11]. Therefore, enhancement of brightness in this work resulted not only from the improvement of the epitaxial layer quality of the GaN films by PSS technique but also from the increase of the light extraction by the inclined facets of the PSS. It is worth noticing that LEDs on HPSS exhibited higher output power than those on MPSS. In addition to slightly better quality of GaN grown on HPSS, the HPSS could also redirect more photons due to its fully inclined geometry. As a result, there is an additional 13% increase in the output power for the LEDs grown on the MPSS compared to those grown on HPSS.

B.4 Conclusion

For the optoelectronic application, the performances of 460nm InGaN-based LEDs grown on mesa-shape and hemisphere-shape-patterned sapphire substrates (MPSS and HPSS) were presented. From rocking curve measurements of GaN asymmetric (102) plane, the full width at half maximum decreases from 480 arcsec to 293arcsec and 262 arcsec for GaN grown on MPSS and HPSS, respectively. It indicates that lower threading dislocation density can be achieved through such PSSs technique. For light-output power performance, although GaN materials grown on

MPSS and HPSS demonstrated similar dislocation density, a 44% improvement of light-output power for the LEDs grown on HPSS was observed, which is higher than a 31% improvement for the LEDs grown on MPSS. This result can be contributed not only to better quality of LEDs grown on HPSS but also to HPSS’s fully inclined facets which increases light redirecting and thus increases the LED light extraction efficiency. In addition to the LED application, patterned sapphire substrates presented in this letter can also be used for laser diode applications due to their contributions to the improvement of GaN film quality which is very important for high quality laser diode.

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Figure

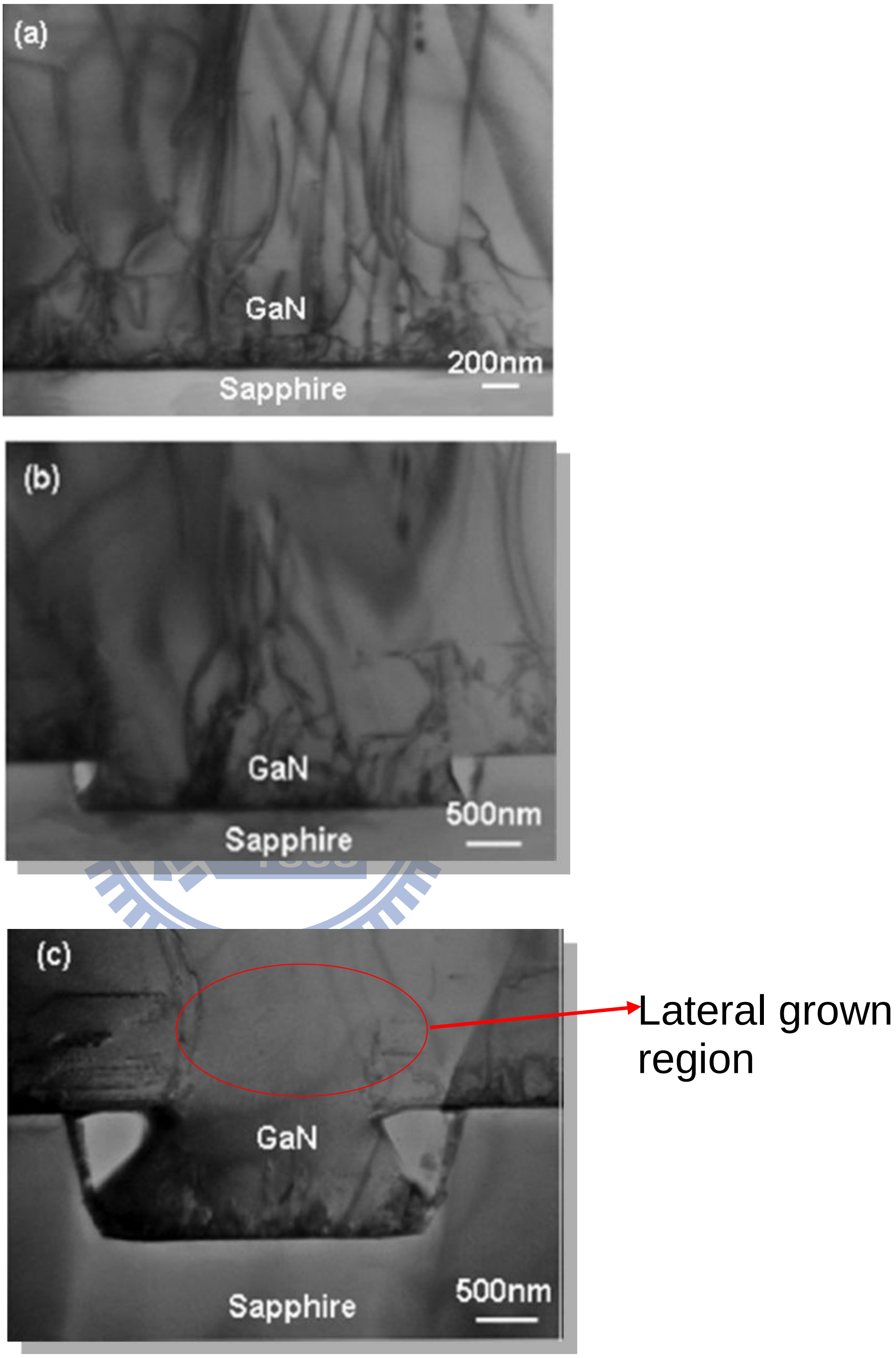
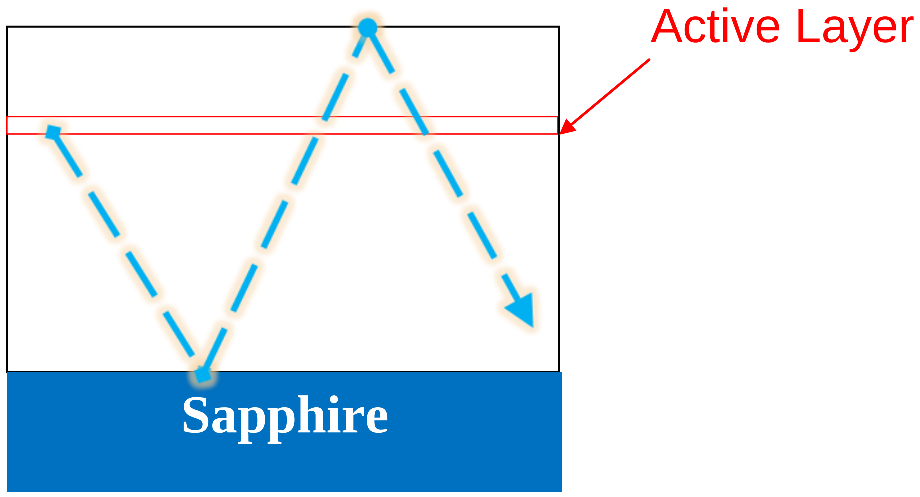
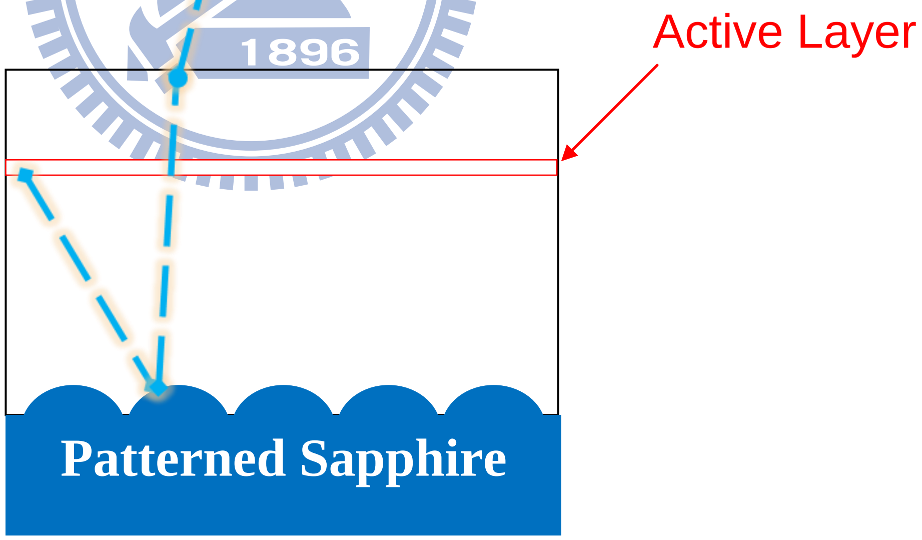


Figure B-1. Cross section TEM image of GaN epilayer grown on (a)conventional and patterned-sapphire substrate, (b) pattern depth = 0.5 µm, and (c) 1.5 µm.



Conventional Substrate



Patterned Substrate

Figure B-2. A schematic ray-tracing of the LEDs grown on conventional and patterned sapphire substrates.

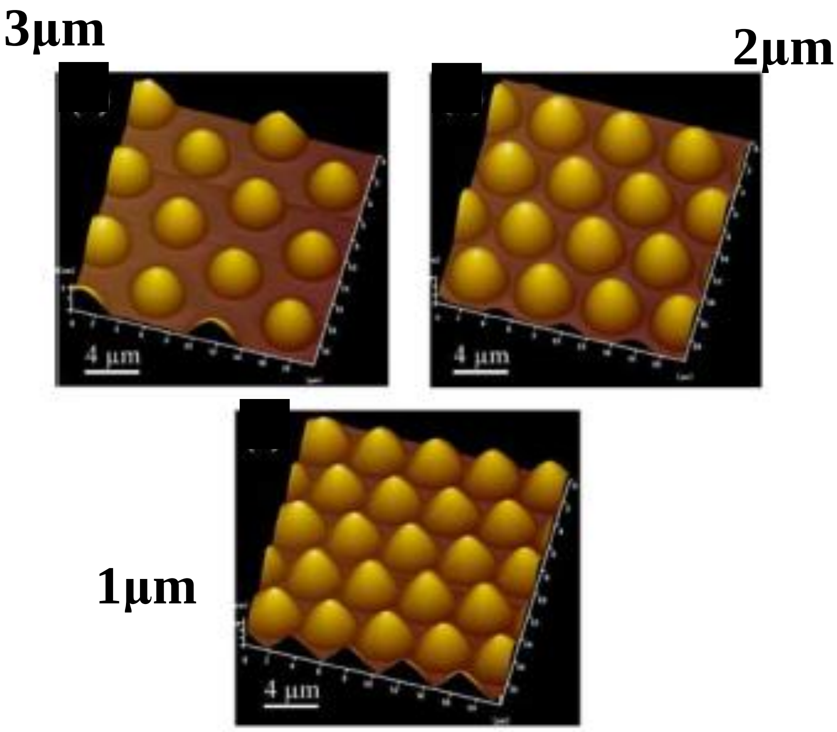


Figure B-3. AFM images of cone-shaped-patterned sapphire substrates with different spacing.

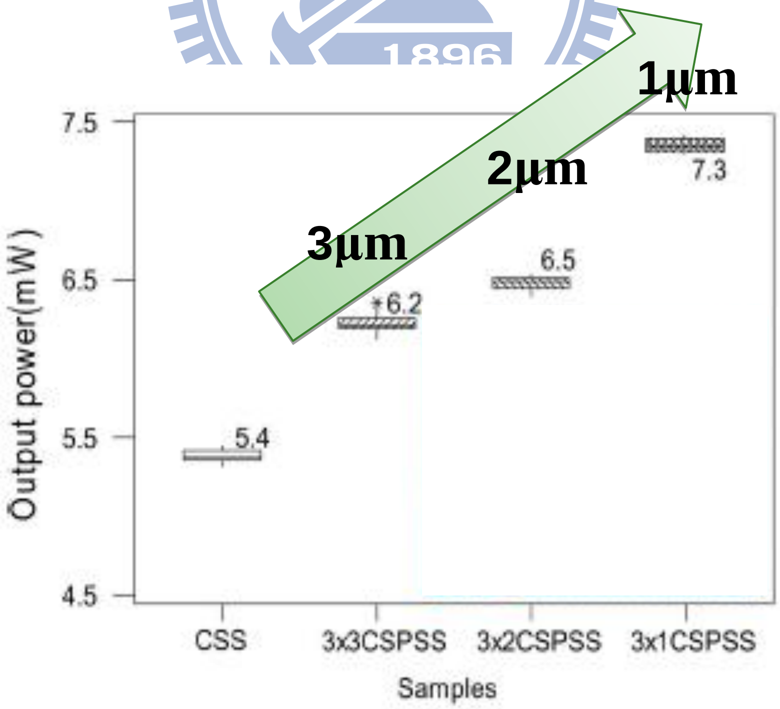


Figure B-4. Light output power of LEDs grown on cone-shaped-patterned sapphire substrates with different spacing.

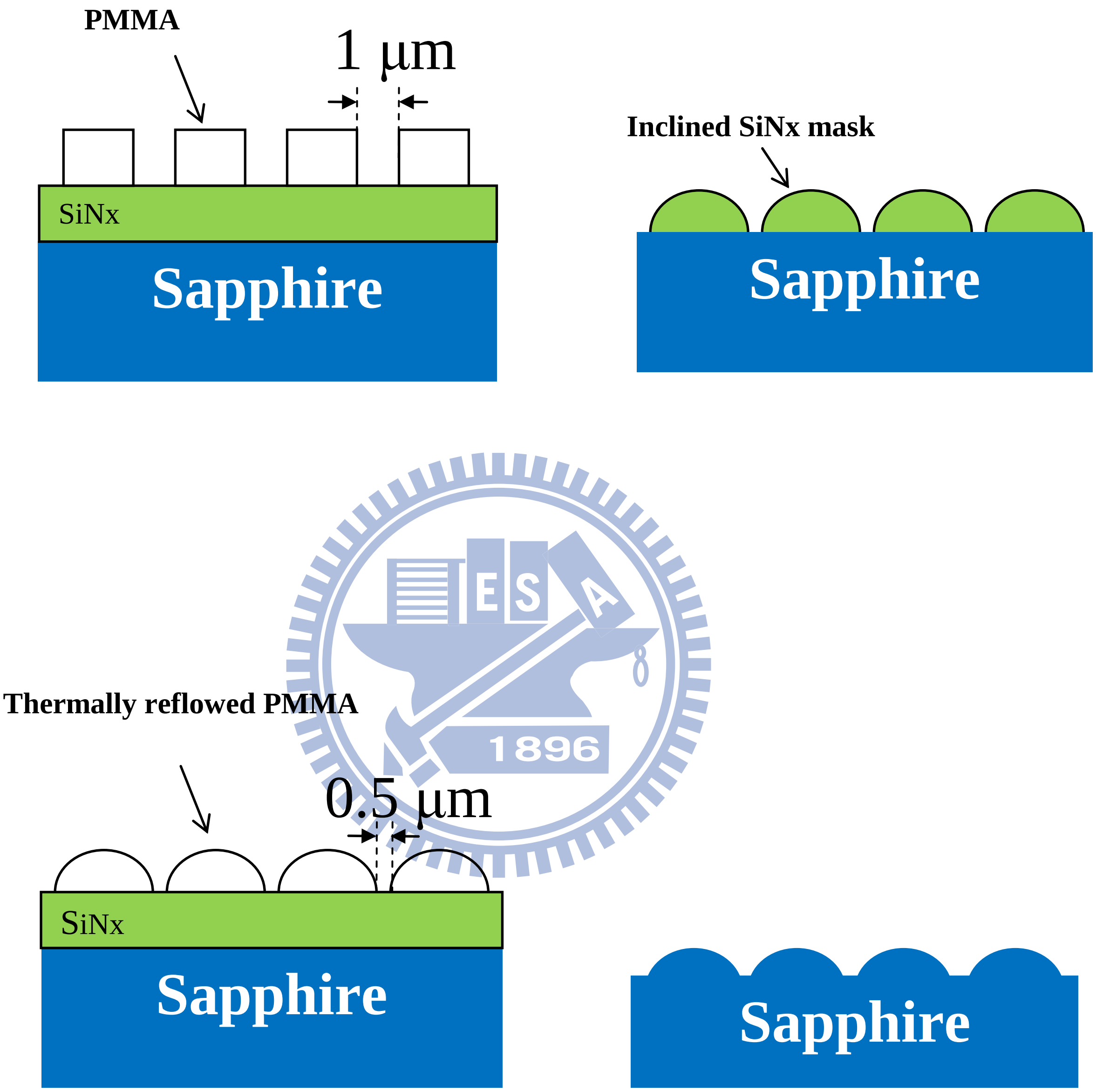
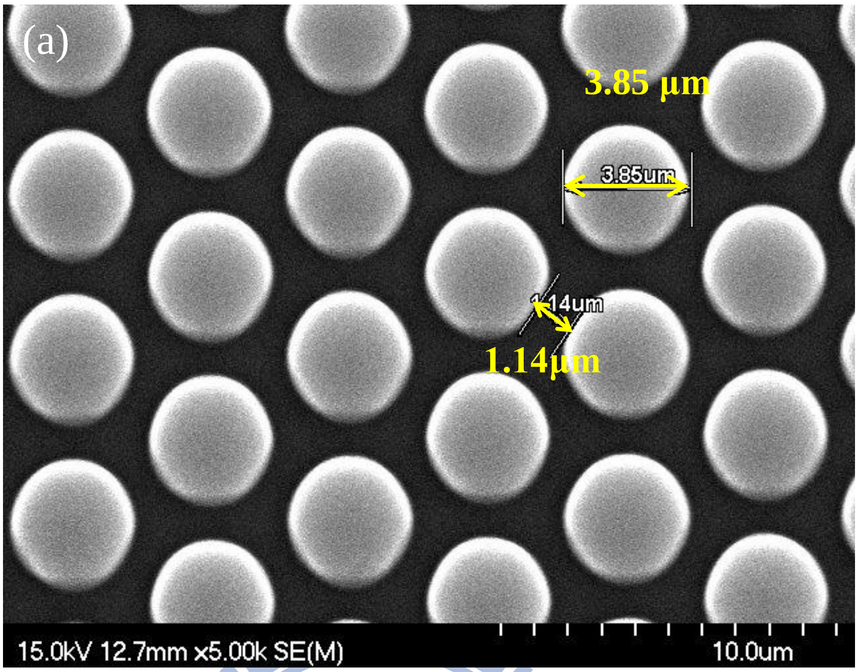


Figure B-5. Process flow of the hemisphere-shape-patterned sapphire substrate with submicron spacing.



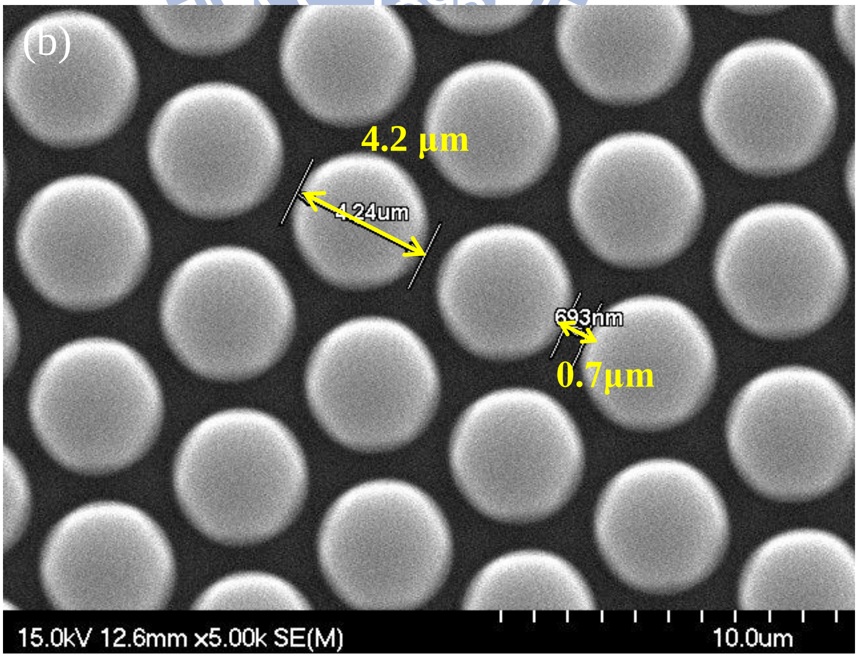


Figure B-6. Top-view SEM images of lithography result with reflow (a) 0 min (b) 1 min.

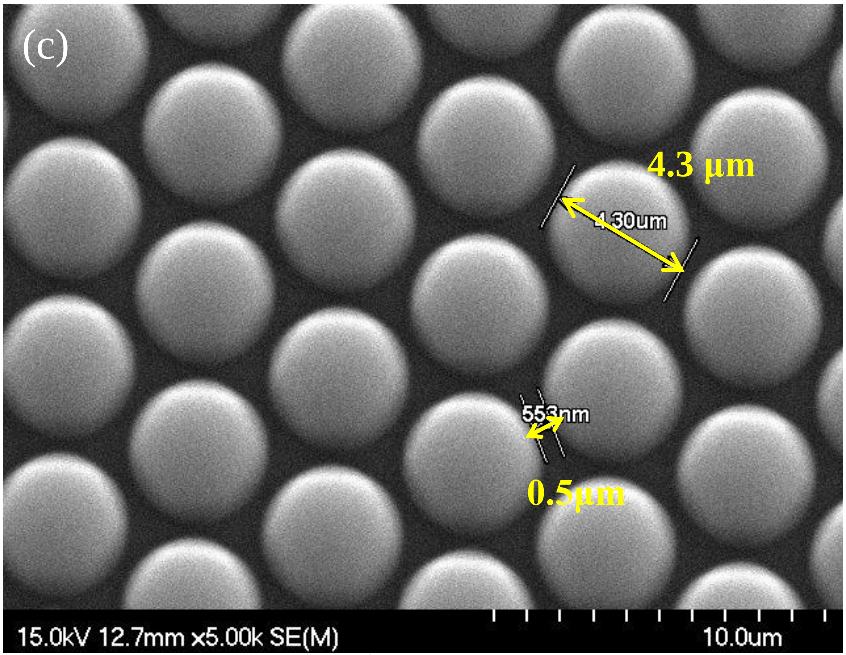


Figure B-6. Top-view SEM images of lithography result with reflow (c) 2min

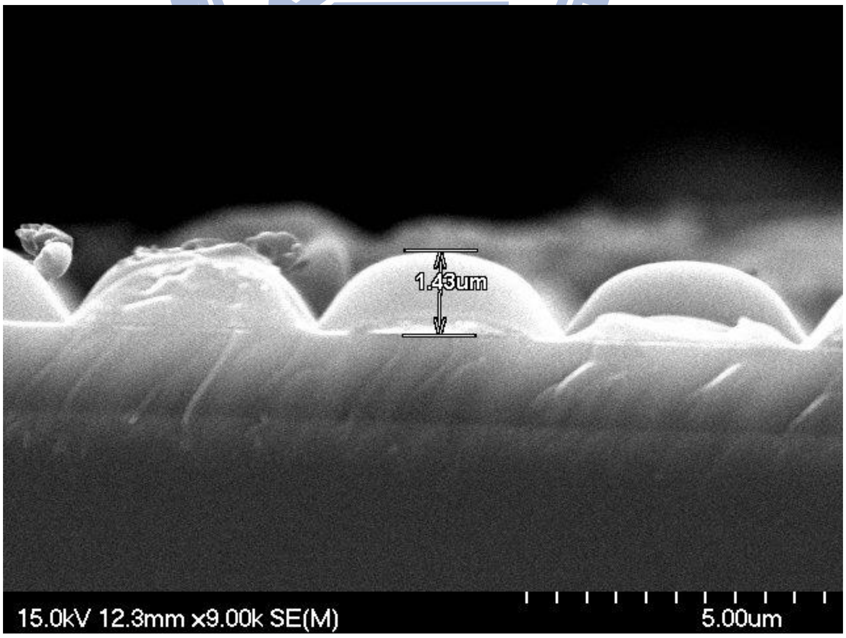


Figure B-7. Cross-section SEM image of lithography result with reflow time of 2min.

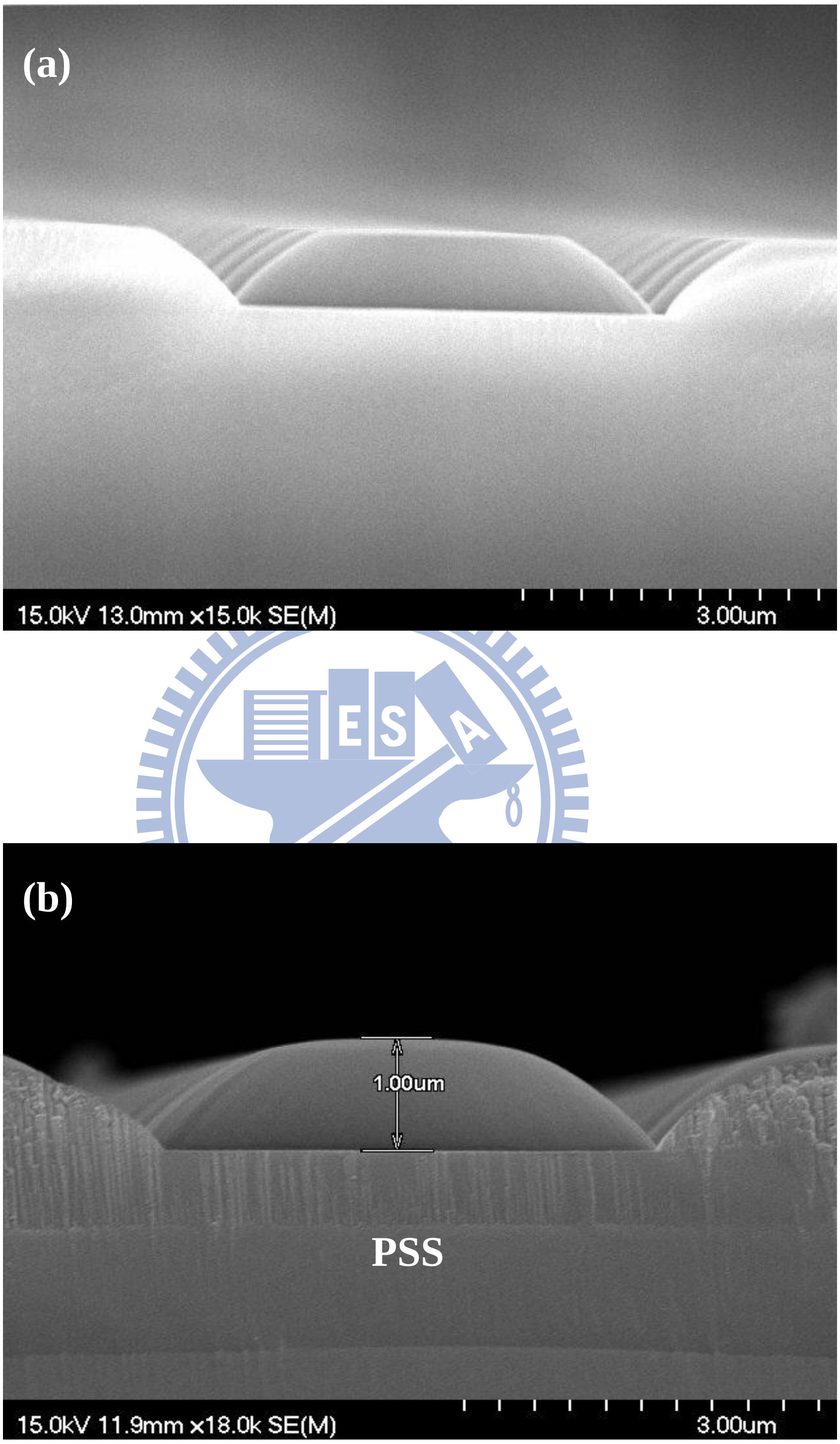


Figure B-8. Cross-section SEM images of patterned sapphire substrates (a)MPSS (b)HPSS.

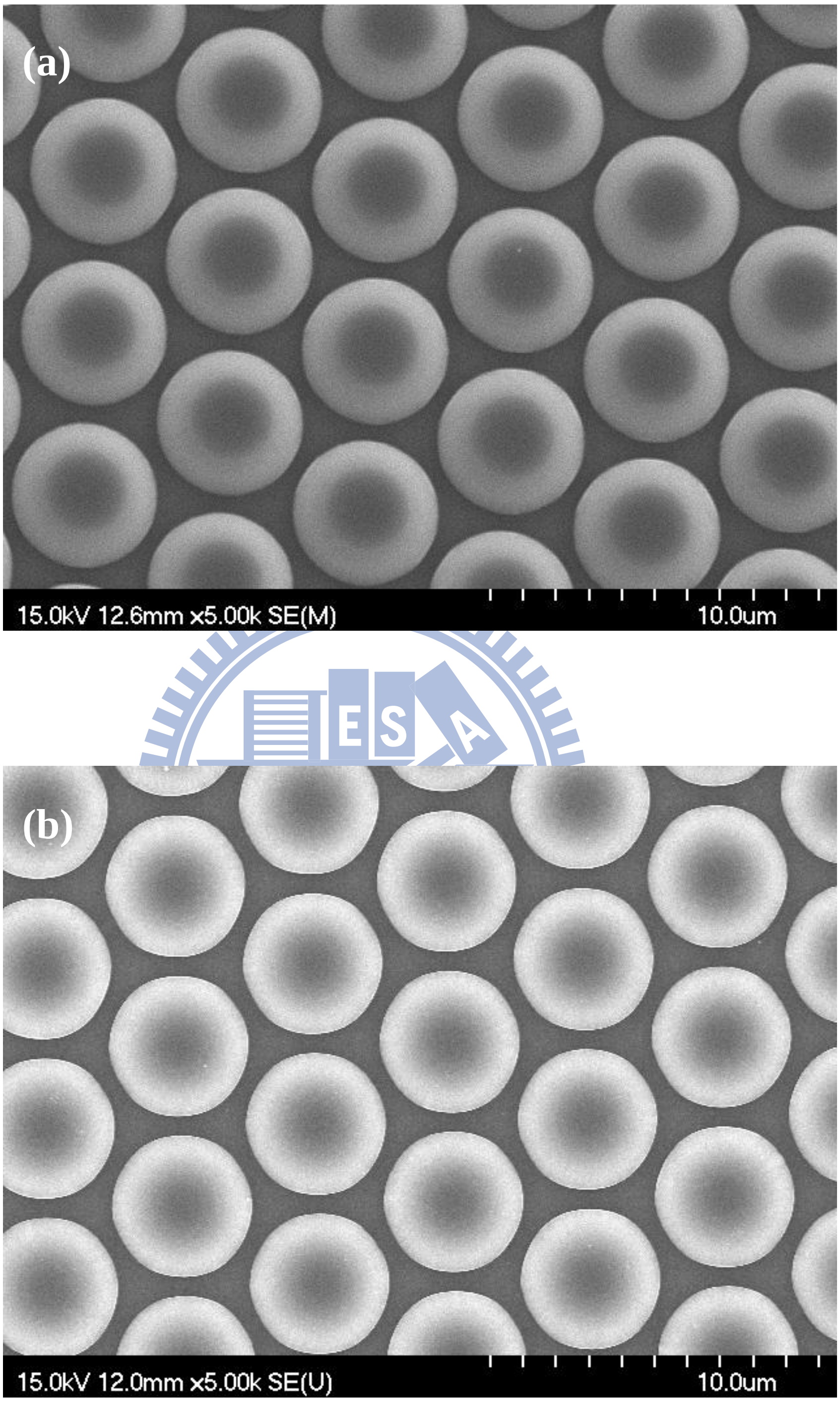


Figure B-9. Top-view SEM images of patterned sapphire substrates (a)MPSS (b)HPSS.

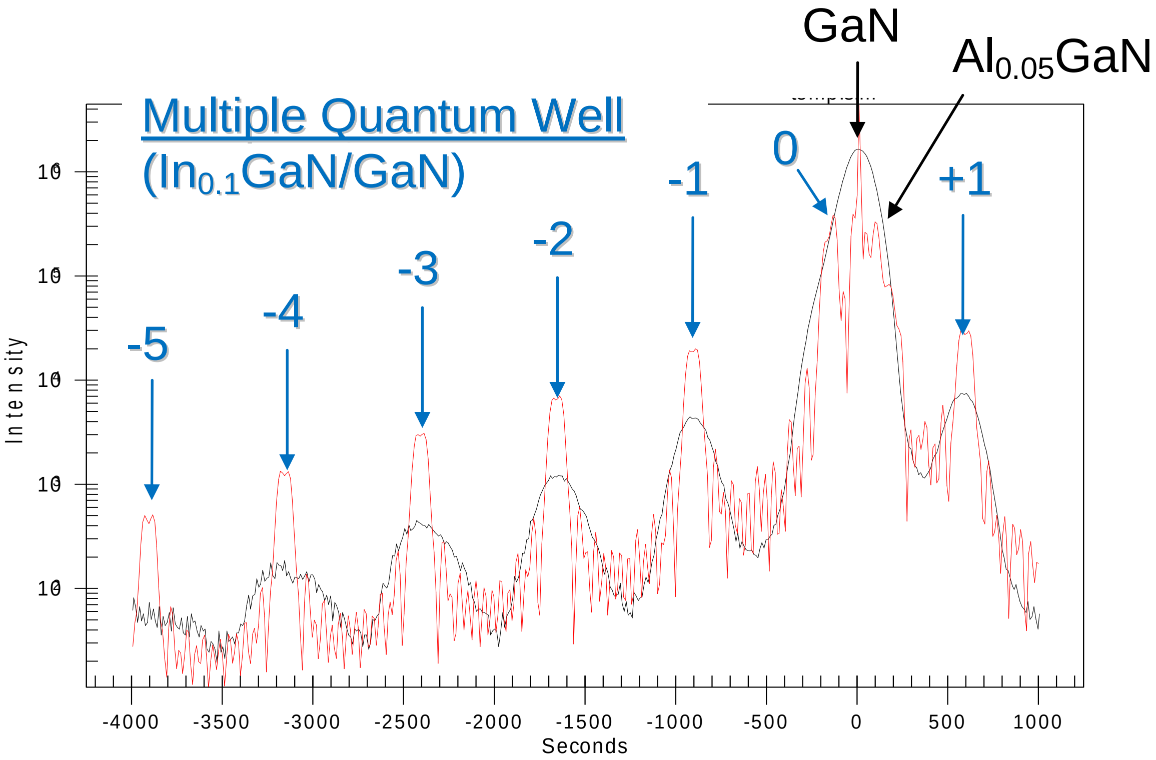


Figure B-10. Omega-2Theta scan of high-resolution x-ray diffraction (black line) and the lattice architecture simulation(red line).

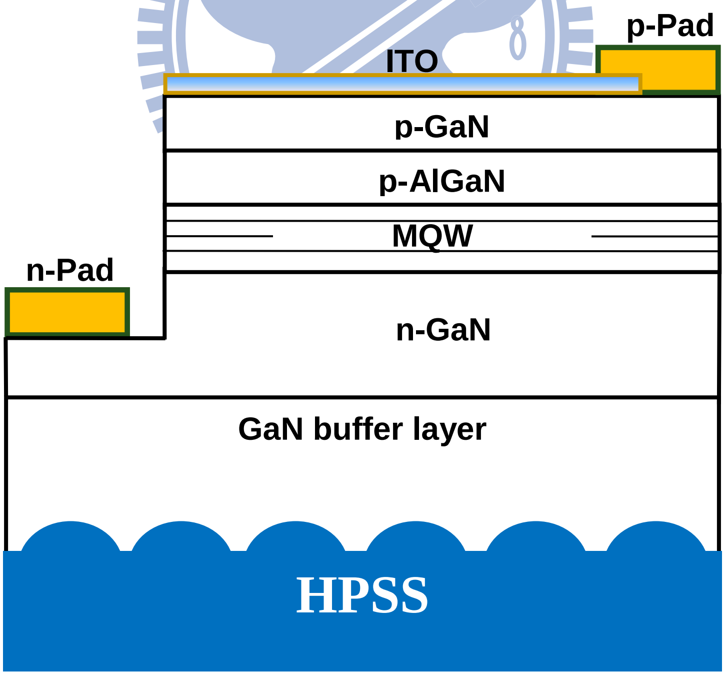


Figure B-11. Schematic cross-section of the fabricated LED grown on hemisphere-like shape patterned sapphire substrate.

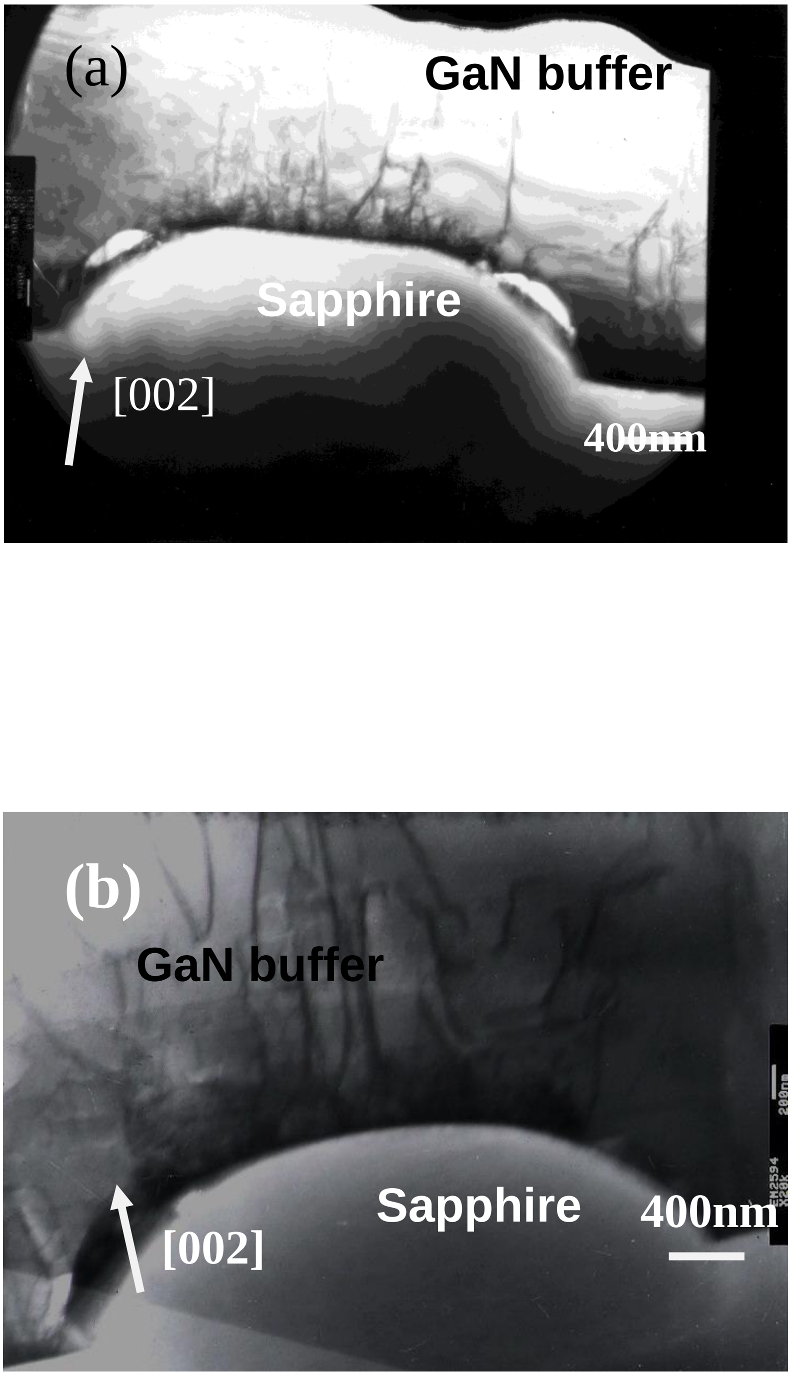


Figure B-12. Cross-section bright-field TEM image of GaN buffer layer grown on (a) mesa-shape- and (b) hemisphere-shape-patterned sapphire substrate. The images were taken on <11-20> zone axis.

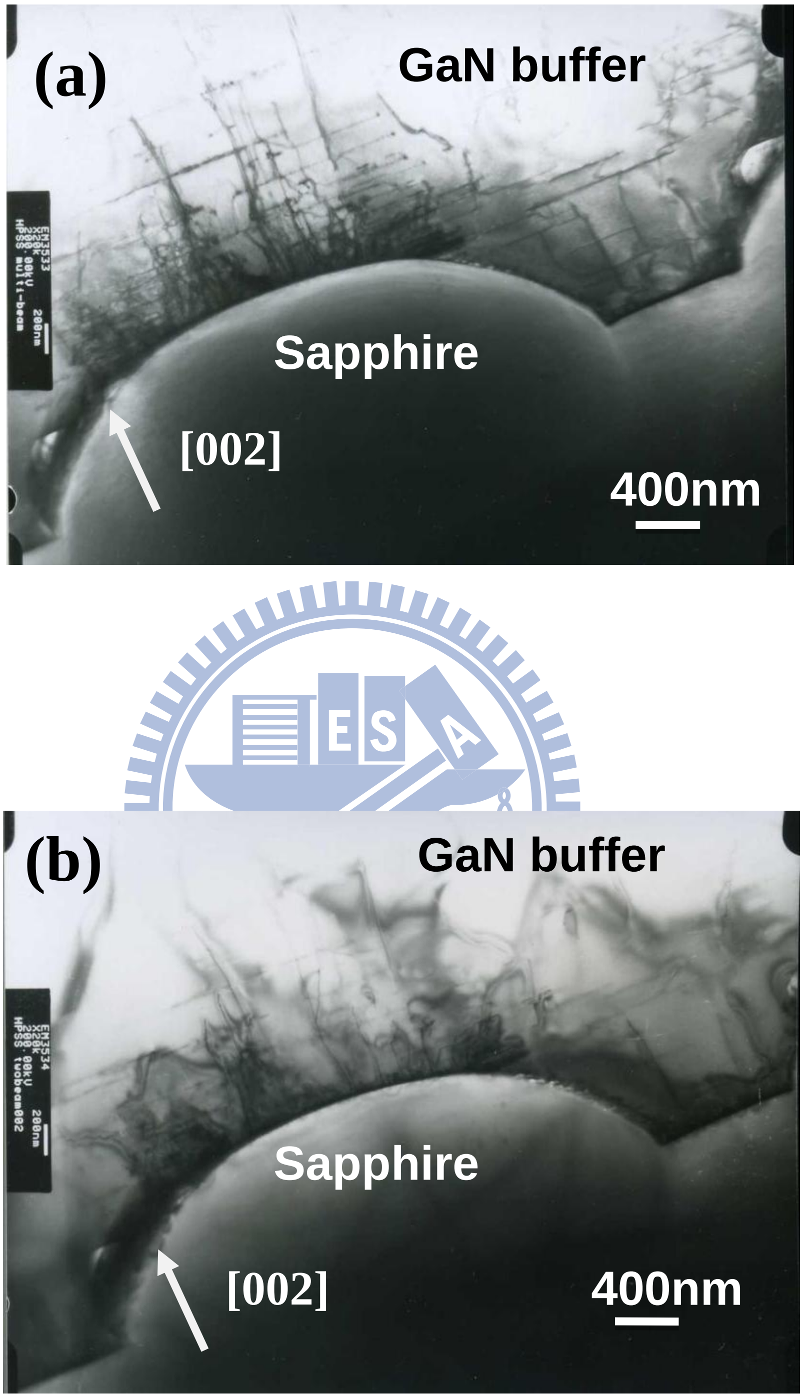


Figure B-13. Cross-section bright-field TEM image of GaN buffer layer grown on hemisphere-shape-patterned sapphire substrate. The images were taken on (a) <11-20> zone axis and (b) under two beam condition of (002).

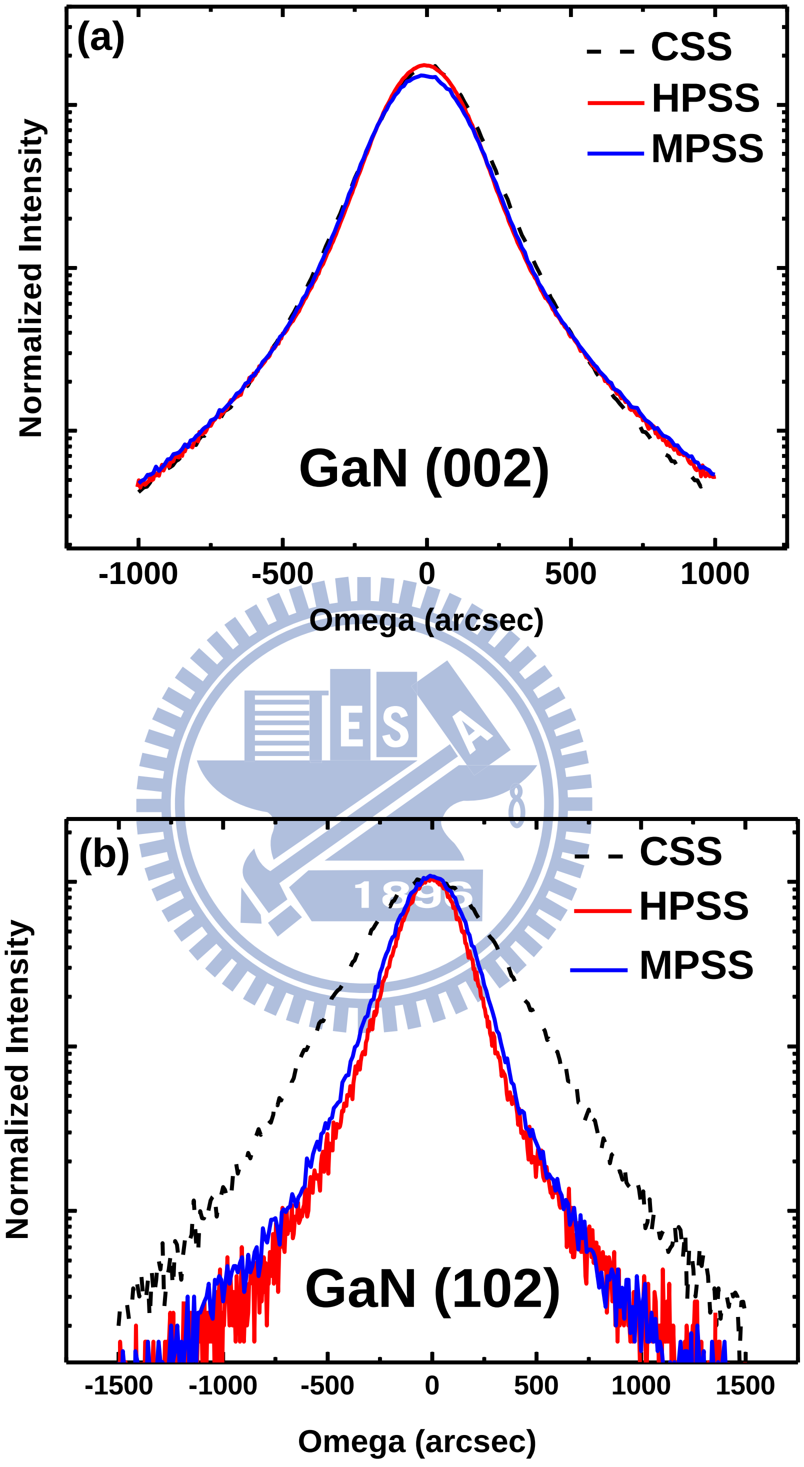


Figure B-14. Rocking curves of the GaN films grown on CSS, MPSS, and HPSS. (a) (002) plane, (b) (102) plane.

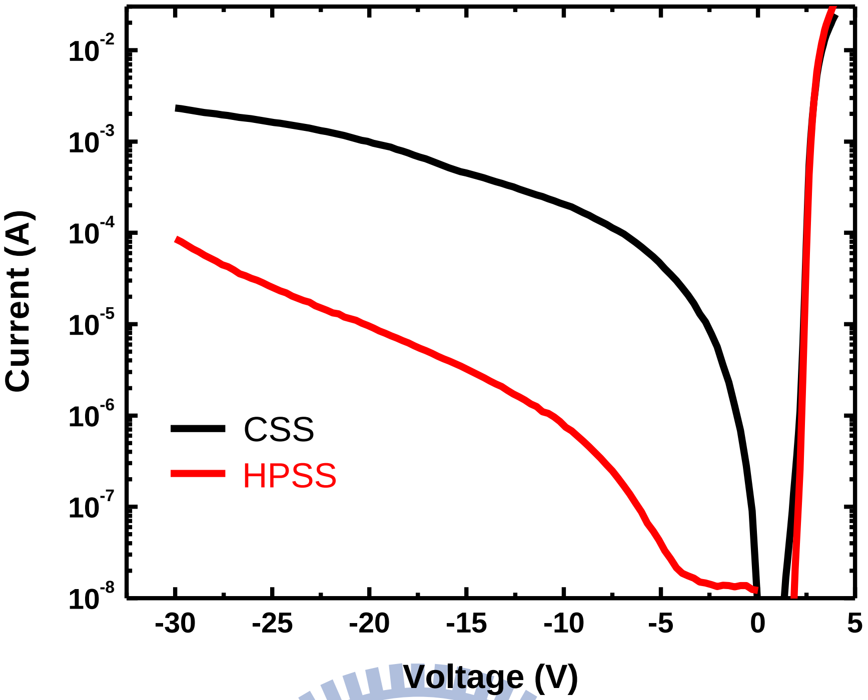


Figure B-15. Forward and reverse I-V characteristics of the LEDs grown on conventional (CSS) and patterned sapphire substrate (HPSS).

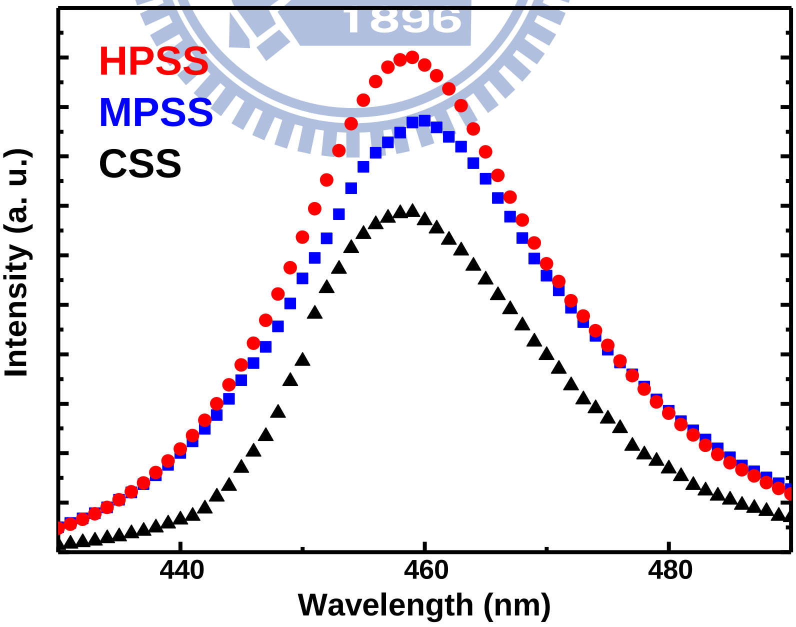


Figure B-16. The EL spectra of the InGaN-based LEDs grown on CSS, MPSS, and HPSS, where the injection current was 20mA.

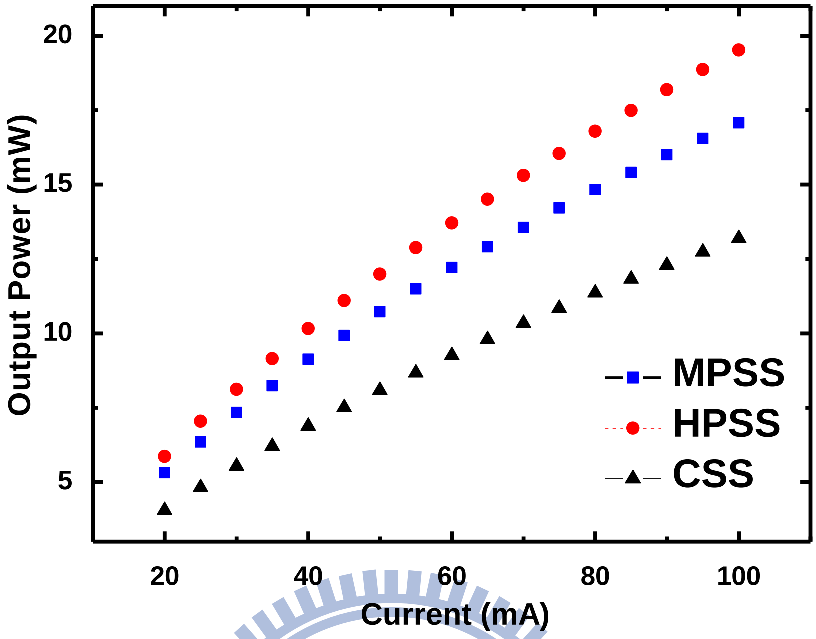


Figure B-17. The light-output power characteristics of 460nm InGaN-based LEDs grown on CSS, MPSS, and HPSS.

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