Improvement of Water-Related Hot-Carrier Reliability by Optimizing the Plasma-Enhanced Tetra-ethoxysilane Deposition Process

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ABSTRACT

As-deposited, steam-exposed O_3-tetra-ethoxysilane (TEOS)-based intermetallic dielectric were characterized according to the IR-absorption spectra. The plasma-enhanced-TEOS films investigated here were formed by mixed-frequency plasma processes and differentiated by reaction oxidizers and/or plasma powers. Increasing stress and nitrogen or oxygen concentrations improved the moisture resistance of PE-TEOS oxide films. In addition to the moisture resistance of PE-TEOS films, another factor affecting hot-carrier robustness is the maximun thickness of the underlayer for O_3-TEOS films, which is limited by their conformity. The integrated intermetallic dielectrics were evaluated by constant-current and hot-carrier stressing. In obtaining the best device reliability, a trade-off exists between moisture resistance, gapfilling capacity of the PE-TEOS underlayer, and plasma damage. Our results indicate that an O_2-rich, PE-TEOS film with a mechanical stress of 3×10^9 dyn/cm^2 is the optimum.

Introduction

The integration of intermetallic dielectric (IMD) is one of the most critical issues for reliable interconnection in the high-density memory of sub-0.5 μm devices. The challenge for IMD technology is to provide a manufacturable deposition and planarization process that can fill aspect ratios greater than 2.5 with minimum impact on the reliability of the underlying device structure and the interconnection lines. For sub-0.5 μm regime, O_3-TEOS oxide prepared under subatmospheric-pressure chemical vapor deposition (SACVD) is considered as a promising intermetallic dielectric for multilevel interconnection, because it provides conformal step coverage and reflow-like morphology. However, O_3-TEOS oxide that is prepared by SACVD using TEOS and ozone (O_3) has some disadvantages, such as surface sensitivity on certain underlayers and moisture absorptivity, both of which degrade deposited film quality and device reliability. So the selection of an O_3-TEOS underlayer is very important. The step coverage of a silane-based PECVD film is generally inadequate, primarily because of geometric shadowing. By contrast, a PE-TEOS oxide has a better step coverage owing to surface migration.[1] For hot-carrier aging immunity in a device, the underlayer is particularly important because it plays an important role in blocking moisture induced by a back-end process,[2] but hot-carrier aging immunity using a plasma-enhanced TEOS oxide is greatly inferior to that of silane-based PE-oxide layers.[3] It is therefore necessary to improve the moisture resistance of PE-TEOS oxides.

We have reported that different PE-TEOS oxides acting as O_3-TEOS underlayers strongly affect the surface sensitivity of O_3-TEOS oxide deposition, their conformity and resulting O_3-TEOS oxide gap-fill, stress stability, and moisture resistance.[4] In this work, we focus on improving water-related hot-carrier reliability by optimizing the PE-TEOS process. Device reliability is characterized by time-dependent dielectric breakdown, n- and p-type metal-oxide semiconductor field effect transitor (MOSFET) reliability, and plasma damage. Finally we obtain the optimum PE-TEOS processing conditions.

Experimental

The plasma-enhanced chemical vapor deposited (PECVD) TEOS and SACVD O_3-TEOS reactor used in this study were implemented in an Applied Materials Precision 5000 multichamber single-wafer machine. The PE-TEOS films were deposited using a mixed-frequency PECVD process: high-frequency (13.56 MHz) and low frequency (350 kHz) power sources were connected to a "showerhead" gas inlet and the susceptor was grounded. Reactive gases were introduced from the showerhead over a wafer heated by halogen lamps. The unreacted gases and reaction by-products were exhausted through a throttle valve below the wafer. TEOS vapor was supplied to the reactor by a bubbler mechanism with a carrier gas of He. The bubbler temperature was set to about 44°C. All depositions occured at 400°C under a chamber pressure of 5.0 to 8.2 Torr. The deposited TEOS oxides were modified to have either different stress or composition by varying key process parameters such as plasma powers and oxidants. The processing conditions are shown in Table I.

The moisture resistance of various PE-TEOS oxides was monitored by comparing infrared (IR) spectroscopy results before and after a 48 h 2 atm-saturated steam test at 125°C. The scanned samples consisted of 2000 Å PE-TEOS oxides deposited over a 5000 Å undoped O_3-TEOS. Nuclear resonance analysis (NRA) was used to probe hydrogen content in the O_3-TEOS oxides and the underlying PE-TEOS oxide after exposure to air for 48 h. The stress of all films was measured by a stress gauge which is

Table I. Various PE-TEOS oxide deposition processes used in this study.[a]

Process conditions	A 1E9 TEOS	B 2.5E9 TEOS-N_2	C 1E9 TEOS-N_2O-O_2	D 3E9 TEOS	E 3E9 TEOS-O_2-rich
TEOS (sccm He)	560	350	600	560	300
O_2 (sccm)	840	—	180	840	510
N_2O (sccm)	—	1150	1000	—	—
High-frequency power	375	185	185	375	450
Low-frequency power	83	145	130	160	75

[a] Notation for an oxide film with a stress of 1×10^9 dyn/cm^2 deposited from TEOS using the PECVD process.

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Table II. Wet-etch-rate ratio of PE-TEOS films tuned according to different recipes.

Characteristics	A	B	C	D	E
Wet-etch-rate ratio[a]	2.01	1.07	1.96	1.45	1.45

[a] Represents the PE-TEOS film wet-etch rate normalized to that of thermal oxide in 6:1 BOE.

a commercial laser wafer-flatness measuring device. The measurement of stress is a relatively straightforward procedure based on beam bending. This technique also allows the stress to be directly determined on the substrate that the film is deposited upon. The procedure is based upon the phenomenon that the stresses in a film on a thin substrate will result in the bending of the substrate.

The devices used for this investigation were fabricated via a twin-tub double-level metallization complementary metal-oxide semiconductor (CMOS) technology. The gate oxide thickness was 142 Å. The effective channel length (L_{eff}) ranged from 0.5 to 1.0 μm. The implemented IMD scheme involved a PE-TEOS underlayer followed by O_3-TEOS CVD at 600 Torr. The thickness of the PE-TEOS underlayer was varied in order to obtain seamless IMD; the designed thickness is presented in Table II. Nitrogen treatment was conducted using mixed-frequency plasma at 400°C to protect O_3-TEOS from moisture attack. Subsequent to the deposition of a PECVD oxide cap layer, the IMD was planarized by spin-on-glass (SOG) etchback. Following of SOG etchback, the IMD process was completed with a final plasma oxide deposition.

[c] Films are identified by their mechanical stress and the reactants used for deposition. The oxide film "1E9 TEOS" is formed from TEOS by PECVD having a mechanical stress of 1×10^9 dyn/cm^2.

Results and Discussion

Film wet-etch rate and moisture resistance.—The wet-etch-rate ratios of 1E9 TEOS,[c] 2.5E9 TEOS-N_2O, and 1E9 TEOS-N_2O-O_2 films, along with those of 3E9 TEOS and 3E9 TEOS-O_2 rich films, are shown in Table II. The wet-etch-rate ratio represents the PE-TEOS wet-etch rate normalized to that of thermal oxide in 6:1 buffered oxide etchant (BOE). We can see that more compressive PE-TEOS oxides exhibit a lower wet-etch-rate ratio; *e.g.*, 1.45 (3E9) *vs.* 2.00 (1E9). Besides stress, another factor determining film wet-etch rate is the nitrogen content in PE-TEOS. It has been reported that nitrogen-rich PE-TEOS has better quality. Comparing 3E9 TEOS-O_2 and 2.5E9 TEOS-N_2O oxide, we found that using an N_2O oxidizer apparently improves film quality (wet-etch-rate ratio 1.07 *vs.* 1.45), although the latter has lower compressive stress.

A 48 h 2 atm saturated steam test at 125°C was carried out. The infrared (IR) absorption spectra of 0.5 μm O_3-TEOS without PE-TEOS cap layers immediately after deposition and then after being in the pressure cooker for 48 h are shown in Fig. 1a. The moisture absorbed by the O_3-TEOS film can be seen in various absorbance bands: 3650 cm^{-1} (Si-OH) and 960 cm^{-1} (Si-OH hydrogen bonded to H_2O). We previously reported that 3E9 TEOS oxide shows an improved moisture resistance over 1E9 TEOS oxide.[4] The IR absorption spectra of 0.5 μm O_3-TEOS with 0.2 μm PE-TEOS cap layers immediately after deposition,

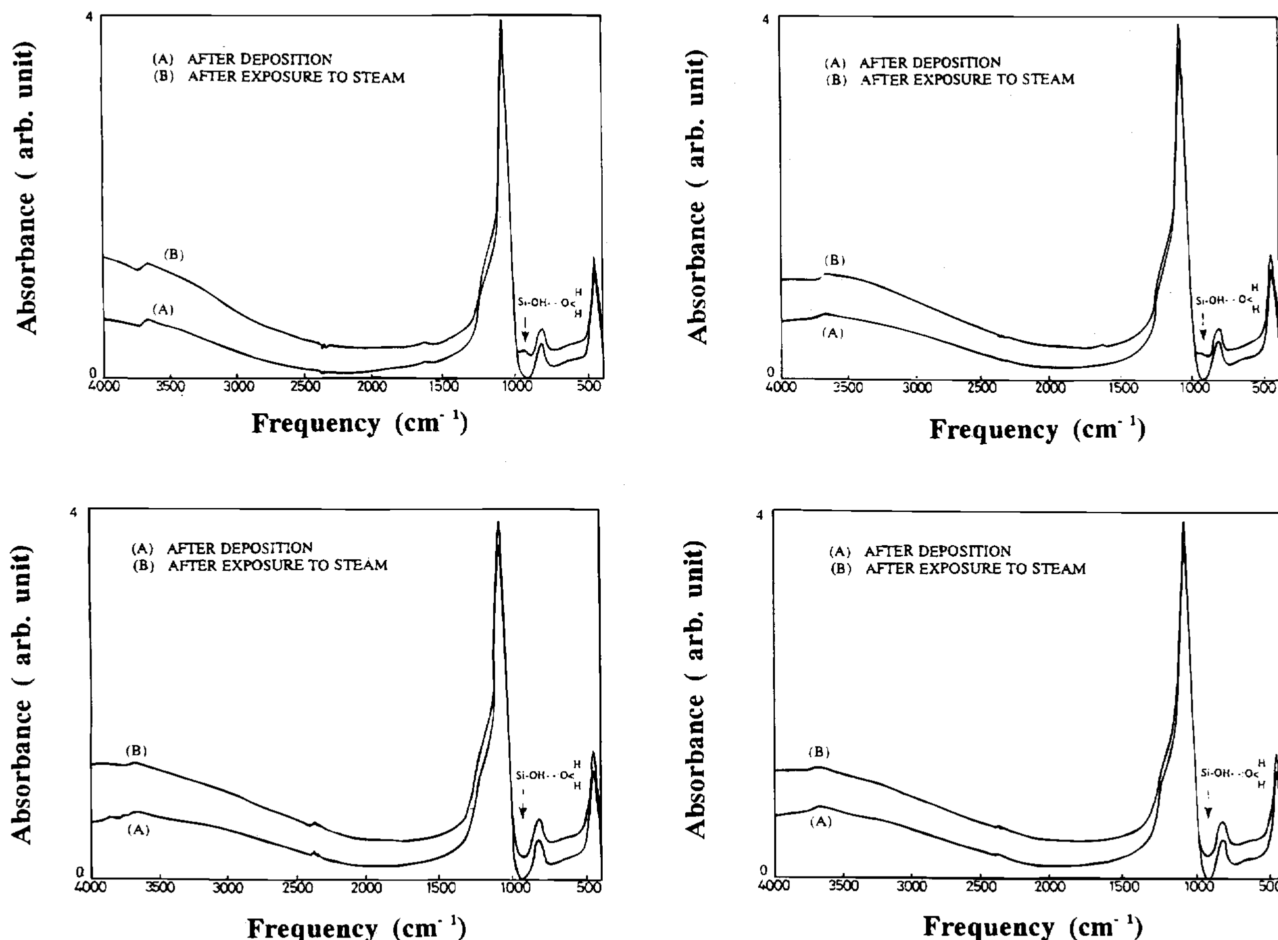

Fig. 1. IR spectroscopy of O_3-TEOS films (a, top left) without cap, and with a 0.2 μm PE-TEOS cap of (b, top right) 1E9 TEOS, (c, bottom left) 2.5E9 TEOS-N_2O, and (d, bottom right) 3E9 TEOS-O_2-rich before (lower curve) and after (upper curve) the steam test.

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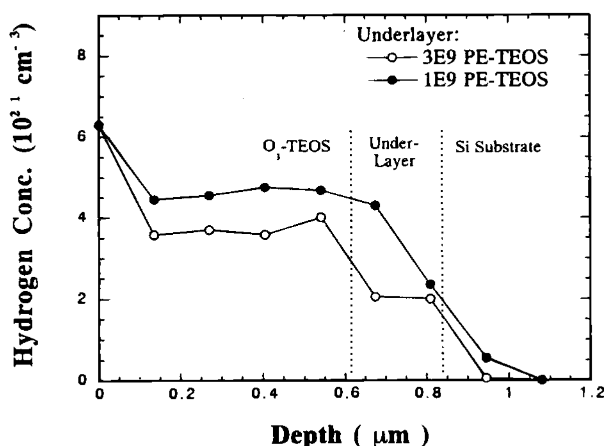
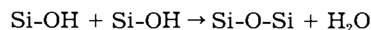


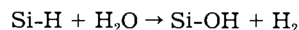
Fig. 2. Hydrogen profiles in the oxide structures of O_3-TEOS / 1E9 PE-TEOS and O_3-TEOS/3E9 PE-TEOS films.

and then after being in the pressure cooker for 48 h, are shown in Fig. 1b-d. Figure 1b shows the IR spectra of the film stack with TEOS-O_2 of an as-deposited compressive film with a stress of 1×10^9 dyn/cm^2. After being in the cooker for 48 h, there is an increase in Si-OH and Si-OH hydrogen bonding to H_2O in the absorbance bands at 3650 and 960 cm^{-1}, indicating that the 0.2 μm TEOS-O_2 PECVD oxide is not a good moisture barrier. By contrast, Fig. 1c shows the IR spectra of the film stack with TEOS-N_2O having an as-deposited compressive film stress of 2.5×10^9 dyn/cm^2 immediately after deposition and then after being in the pressure cooker for 48 h. Note that there is no increase in Si-OH and Si-OH hydrogen bonding to H_2O shown in the absorbance band. The same situation can also be seen for a TEOS-O_2-rich film stack having an as-deposited compressive film stress of 3×10^9 dyn/cm^2. Figure 2 shows the hydrogen concentrations in O_3-TEOS deposited on 1E9 and 3E9 PE-TEOS underlayer. H_2O protons were detected by NRA, and two distinct regions are noted in the O_3-TEOS/3E9 PE-TEOS structure. The second region has approximately half the hydrogen concentration of the first region, which implies that moisture penetration was effectively blocked by the 3E9 PE-TEOS underlayer. O_3-TEOS on 1E9 PE-TEOS produced a smooth hydrogen profile, however, suggesting moisture diffusion into the 1E9 PE-TEOS underlayer. This implies that the moisture resistance of PE-TEOS can be enhanced by increasing stress and nitrogen or oxygen concentration.

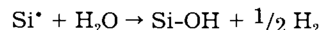
In a dual-frequency plasma process, the high-frequency power gave a stable discharge and generates some of the reactive species. The low-frequency power provided ion bombardment to enhance chemical reactions and cause a low-energy ion implantation which densified the film and provided an intrinsic compressive stress.[5] We can get high compressive stress PE-TEOS oxide film which has better quality by increasing the low-frequency power. It was reported that 3×10^9 dyn/cm^2 TEOS-N_2O oxides contain more Si-H bonding at 2260 to 2100 cm^{-1} than 1×10^9 dyn/cm^2 TEOS-N_2O oxide films.[6] Machida *et al.*[7] have proposed a moisture-trapping mechanism for Si-rich films which involves



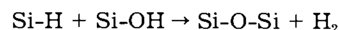
$$\text{Si-OH} + \text{Si-OH} \rightarrow \text{Si-O-Si} + H_2O$$



$$\text{Si-H} + H_2O \rightarrow \text{Si-OH} + H_2$$



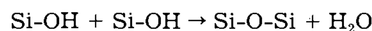
$$\text{Si}^{\bullet} + H_2O \rightarrow \text{Si-OH} + 1/2\, H_2$$



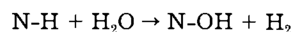
$$\text{Si-H} + \text{Si-OH} \rightarrow \text{Si-O-Si} + H_2$$

where H_2O produced by "wet" dielectric is gettered by Si-H or dangling Si$^{\bullet}$, resulting in the formation of the Si-O-Si structure and the release of H_2 gas. Therefore, the presence of Si-H bonding in the high-stress oxide enhances moisture resistance.

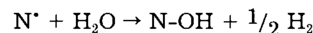
It was also reported that the 3E9 TEOS films contained about 1 atom percent (a/o) nitrogen.[6] It is reasonable to speculate that the TEOS-N_2O films contain more N-H bonds than the TEOS-O_2 films. Lee *et al.*[8] have proposed a moisture-trapping mechanism for N-rich films



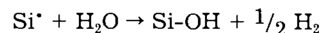
$$\text{Si-OH} + \text{Si-OH} \rightarrow \text{Si-O-Si} + H_2O$$



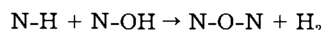
$$\text{N-H} + H_2O \rightarrow \text{N-OH} + H_2$$



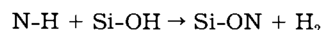
$$\text{N}^{\bullet} + H_2O \rightarrow \text{N-OH} + 1/2\, H_2$$



$$\text{Si}^{\bullet} + H_2O \rightarrow \text{Si-OH} + 1/2\, H_2$$



$$\text{N-H} + \text{N-OH} \rightarrow \text{N-O-N} + H_2$$



$$\text{N-H} + \text{Si-OH} \rightarrow \text{Si-ON} + H_2$$

Since N-rich oxide films contain various fragments consisting of either N or Si in an amorphous network, it is likely that H_2O can be gettered by either N-H or dangling N$^{\bullet}$ or Si$^{\bullet}$. The resulting mechanism will then involve the formation of N-O-N and Si-O-N structures, and also the release of H_2 gas. Therefore, the incorporation of nitrogen in the TEOS-N_2O oxide also enhances moisture resistance.

It is reported that the water evolution characteristics of TEOS-O_2 strongly depend on the flow ratio of TEOS + He/O_2.[9] The amount of water evolution drastically decreases with an increase in the O_2 flow rate. As a result, TEOS-O_2-rich PECVD oxides contains less water compared to TEOS-O_2 PECVD oxides.

Film step coverage.—Increasing the packing density of ultralarge-scale integrated (ULSI) circuits requires the filling of small gaps between the metal lines with CVD dielectric oxide, thus eliminating voids. The presence of voids adversely affects production yields and device reliability, since thinning of metal films occurs over sharp steps. To achieve the best gap-fill results, thickness of PE-TEOS underlayer has been varied among 0.1, 0.15, and 0.2 μm. Thicker underlayers are desirable for more moisture resistance, which improves water-related hot-carrier reliability. But for voidless 0.5 μm gap filling, the maximum PE-TEOS thickness is related to its step coverage. Table III summarizes the measured step coverages and corresponding maximum thickness for voidless 0.5 μm gap filling.

Qbd.—The effect of the various PE-TEOS IMD structures on charge-to-breakdown (Q_{bd}) was studied using a constant-current stress of −30 mA/cm^2. We performed gate injection on P^- well, ensuring that the substrate was in accumulation. Capacitor area was 1.563×10^{-4} cm^2. Figure 3 compares Weibull plots of the charge-to-breakdown for various PE-TEOS IMD structures. Thirty capacitors were stressed for each PE-TEOS IMD structure. The

Table III. Step coverage of various PE-TEOS oxides and their maximum thickness for 0.5 μm gapfill.

PE-TEOS type	Sidewall/top (0.5 to 0.8 μm)	Bottom/top (0.5 to 0.8 μm)	Maximum thickness for 0.5 μm gapfill
(A) 1E9 TEOS	0.50 to 0.70	1.00 to 1.00	0.2 μm
(B) 2.5E9 TEOS-N_2O	0.27 to 0.33	0.86 to 0.93	0.1 μm
(C) 1E9 TEOS-N_2O-O_2	0.36 to 0.45	0.82 to 0.92	0.2 μm
(D) 3E9 TEOS	0.43 to 0.50	0.83 to 0.95	0.15 μm
(E) 3E9 TEOS-O_2 Rich	0.42 to 0.50	0.83 to 0.92	0.15 μm

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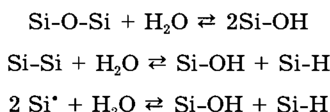
inclined parts of the curves in Fig. 3 refer to the defect-related component. The upright parts of the curves represent the intrinsic breakdown strength. We find that the samples with the higher stress, nitrogen and oxygen-rich PE-TEOS IMD had larger Q_{bd} and fewer defects. In particular, 3E9 TEOS-O_2-rich oxide had the largest Q_{bd}. TEOS/O_3 oxide contains many more water-related components than gate oxide.[10] After subsequent back-end processes, these components diffuse to the gate oxide. As a result, it is known that minute water-related impurities such as H and OH, are introduced into oxides to create additional Si-H and Si-OH bonds in the SiO_2 itself and at the SiO_2/Si interface[11,12]



$$\text{Si-O-Si} + H_2O \rightleftarrows 2\text{Si-OH}$$

$$\text{Si-Si} + H_2O \rightleftarrows \text{Si-OH} + \text{Si-H}$$

$$2\,\text{Si}^{\bullet} + H_2O \rightleftarrows \text{Si-OH} + \text{Si-H}$$

Recent studies have shown that Si-H and Si-OH bonds at the interface are precursors of interface states (Si$^{\bullet}$) generated by HC stress.[13-15] Figure 4 shows the midgap interface state density (ΔD_{itm}) plotted against stress time using a constant current stress of -10 $\mu A/cm^2$ for various PE-TEOS IMD structures. Each datum point is an average of several measurements. Capacitor area was 2.5×10^{-3} cm^2. We find that the samples with the higher stresses, nitrogen and oxygen-rich PE-TEOS IMD, had fewer interface state generations. Consistent with preceding discussions, we found that higher stress, nitrogen-rich and oxygen-rich PE-TEOS films had better moisture resistance. According to the physical-damage model,[16] we can assume that higher stress, nitrogen and oxygen-rich PE-TEOS IMD samples that have better moisture resistance also have larger Q_{bd} values. In comparison to n-MOSFETs lifetime (see next section), the improvement in charge-to-breakdown and ΔD_{itm} are not so outstanding. It is believed that IMD influences the interface property of gate oxide only near the source-drain edges and therefore affects short channel devices more strongly.[3]

Device reliability.—The importance of IMD in controlling hot-carrier performance has been reported before.[2] Shimoyama *et al.*[2] reported that desorbed water from O_3-TEOS causes MOS transistor hot-carrier degradation. In this study, we also examined the process described previously by evaluating hot-carrier-induced degradation, since they strongly depend on the quality of gate oxide which is in turn affected by the back-end processing. n-MOSFETs with 0.5 μm long and 20 μm wide gates were used for hot-carrier stress testing. p-MOSFETs with 1 μm long and 20 μm wide gates, with and without protection

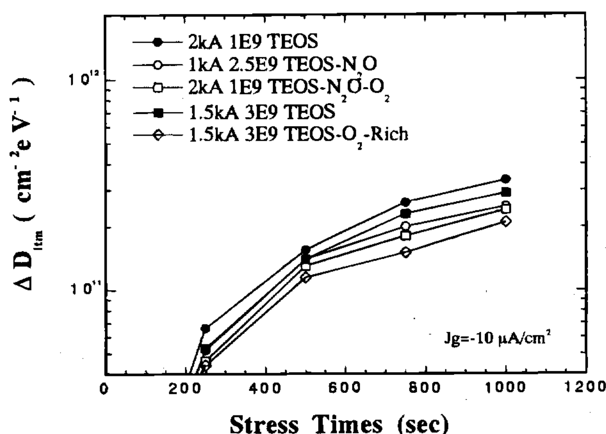


Fig. 4. Midgap interface state density shift plotted against stress time for various PE-TEOS IMD structures at current density of -10 $\mu A/cm^2$. Each data point is an average of several measurements.

diodes, were also used for hot-carrier stress testing. MOS transistor testing of all five groups of wafers revealed no tangible differences in their original threshold voltages, *I-V* characteristics, and transconductance values. This indicates that mechanical stress has no effect on initial device characteristics. For n-MOSFETs, the best monitor of hot-carrier stress effects is the substrate current (I_{sub}),[17] while in p-MOSFETs the gate current (I_g) is the preferred indicator.[18] In this study, we applied the gate voltage that produced either peak I_{sub} or I_g for any given drain voltage, depending on the transistor type. The transistors were stressed at drain voltages of 6.8, 7.0, and 7.5 V for n-MOSFETs and -8.0, -8.2, -8.4, and -8.6 V for p-MOSFETs .

The degradation in n-channel device performance produced by these stress conditions resulted mainly from surface state generation and charge trapping near the Si/SiO_2 interface. In these devices, the trapping component was small. Figure 5 shows device lifetime *vs.* the substrate current per unit gate width for various IMDs. Device lifetimes were determined using the criterion of 10% transconductance (g_m) decrease during the stress. Each datum point is an average of several measurements, and clearly, PE-TEOS underlayer selection has a conspicuous effect on device reliability. This result is consistent with the preceding conclusion. Compared to 1E9 PE-TEOS, the n-MOSFET

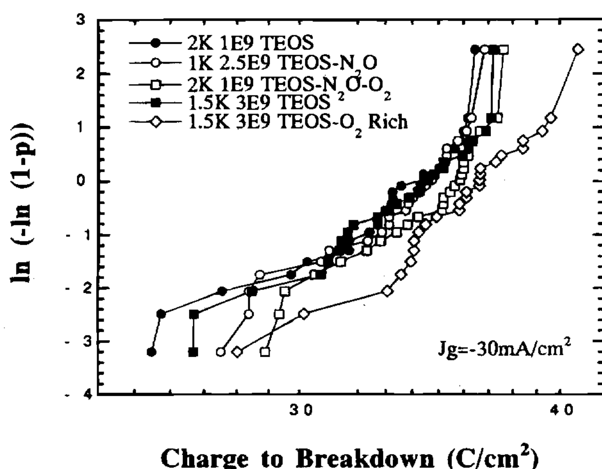


Fig. 3. Weibull distribution of charge-to-breakdown for various PE-TEOS IMD structures stressed at current density of -30 mA/cm^2. K = 1000 Å.

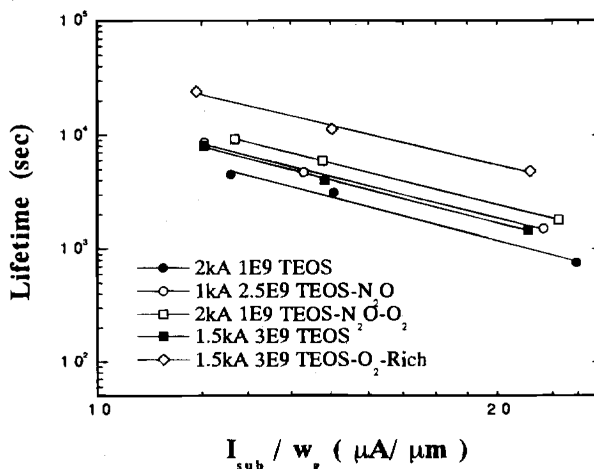


Fig. 5. n-Channel transistor hot-carrier lifetime plotted against substrate current per unit gate width for various PE-TEOS IMD structures. Each datum point is an average of several measurements.

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lifetimes are extended by using 3E9 TEOS as an underlayer. Further improvement is obtained by 2.5E9 TEOS-N_2O and 1E9 TEOS-N_2O-O_2, and 3E9 TEOS-O_2-rich oxide leads to the most stable devices. As the preceding discussion suggests, devices with 3E9 TEOS, 2.5E9 TEOS-N_2O, 1E9 TEOS-N_2O-O_2, and 3E9 TEOS-O_2-rich IMDs have less Si-OH and Si-H near the Si-SiO_2 interface; therefore, these devices have improved water-related hot-carrier reliability compared to that of control samples. Note that the PE-TEOS underlayer thickness varied with step coverage, and the optinum thickness also has an impact on hot-carrier lifetime. From IR spectroscopy, 2.5E9 TEOS shows more moisture resistance than 1E9 TEOS-N_2O-O_2;[4] however, the latter exhibits superior device reliability. This results in the thickness difference in both cases. In order to achieve voidless gapfill, the 2.5E9 TEOS-N_2O thickness was decreased to 1 kÅ which unfortunately reduced its ability of blocking water. As a result, in spite of its superior quality, a thinner TEOS-N_2O underlayer does not provide greater device reliability. On the other hand, although 1E9 PE-TEOS can be deposited up to 2 kÅ, its poor moisture resistance still leads to more severe device degradation compared to other PE-TEOS oxides. Both the film property and gap-fill ability of PE-TEOS has to be considered in attempting to optimize device reliability. The data show that 1.5 K 3E9 TEOS-O_2-rich film is indeed the best choice with respect to gap filling and device lifetime. In addition to good moisture resistance, its superior film quality is due to a drastic decrease in water evolution in oxygen-rich PE-TEOS oxide.[9]

The degradation of p-channel device performance produced by the above stress conditions results from electron trapping,[18] as evidenced by increase in g_m and I_{ds}. Figure 6 shows p-MOSFET lifetimes plotted against the initial peak gate current per unit gate width for various IMDs. The p-MOSFET had antenna ratios of 1051:1 and protective diodes. Device lifetimes were determined using the criterion of a 5% I_{ds} increase during the stress test. The p-MOSFET trend with various IMDs is quite contrary to that of n-MOSFETs. This same condition is also seen in Ref. 3 in which they reported observing that the rate of hole trapping and/or hole-like donor-type interface trap generation was higher in TEOS devices, and that devices with TEOS layers showed less electron trapping than devices with PE-oxide layers. One possible mechanism that accounts for this is a donor-like trap.[19-22] The donor-like turnaround phenomenon was first observed by Gdula in 1976.[19] In water-diffused oxides, production of negative bulk oxide charges, Q_{ot}, and positive interface charge, Q_{it}, by an avalanche-injected electron flux was observed. The efficiencies of both processes were enhanced by water indiffusion.[21] It seems that water-related n-MOSFET hot-carrier reliability improves, while p-MOSFET hot-carrier reliability deteriorates. But it is noteworthy that the difference in p-MOSFET lifetimes for various IMD structures are not pronounced. In particular, the p-MOSFET lifetime of 1E9 TEOS is the same as that of 3E9 TEOS.

It has been reported that plasma damage affects the hot-carrier failure times of p-MOSFETs but does not affect n-MOSFET degradation.[23,24] p-MOSFETs without protective diodes were also stressed at a drain voltage of −7.7 V and a gate voltage of −1.8 V. The antenna ratios were 1051, 2102, and 4205. Figure 7 shows the cumulative distribution of p-MOSFET lifetime for low and high-stress TEOS film.[25] The larger the antenna ratio, the shorter the lifetime of p-MOSFETs. Figure 7 shows that increasing low-frequency RF power produces devices with shorter lifetimes. Figure 6 shows that the lifetime of a device with 3E9 PE-TEOS as an underlayer is almost the same as those of devices with 1E9 PE-TEOS. Increasing the low-frequency power to obtain high stress film thus causes plasma damage. Furthermore, increasing the thickness of the underlayer PE-TEOS to improve the moisture resistance also degrades p-MOSFET hot-carrier robustness (not shown). The thickness-dependent reduction in n-channel transistor hot-carrier lifetime due to PE-TEOS deposition had also been reported.[26] There is a trade-off between plasma damage and film quality with respect to blocking water diffusion, but the 1.5 kÅ, 3E9 TEOS-O_2-rich films have the least low-frequency power and are of suitable thickness. Further detailed study is in progress.

Conclusions

We have studied the effects of PE-TEOS processes on O_3-TEOS-based IMDs. The performance of PE-TEOS oxide strongly depends on processing conditions. Increasing stress and nitrogen or oxygen concentrations improve the moisture resistance of PE-TEOS oxide, which inhibits hot-carrier aging and improves Q_{bd} and interface integrity. The same treatments can also affect n-MOSFET lifetime. We also evaluated the plasma damage due to PE-TEOS deposition using different antenna ratios, with and without protective diodes. As a result, in order to improve film moisture resistance, we increased the low-frequency power and film thickness. Unfortunately, this results in more serious plasma damage. To obtain the best device reliability, trade-offs exist among moisture resistance, gap-filling ability of a PE-TEOS underlayer, and plasma damage. Our results indicate that a TEOS-O_2-rich PECVD oxide with a stress of 3×10^9 dyn/cm^2 is the optimum processing condition.

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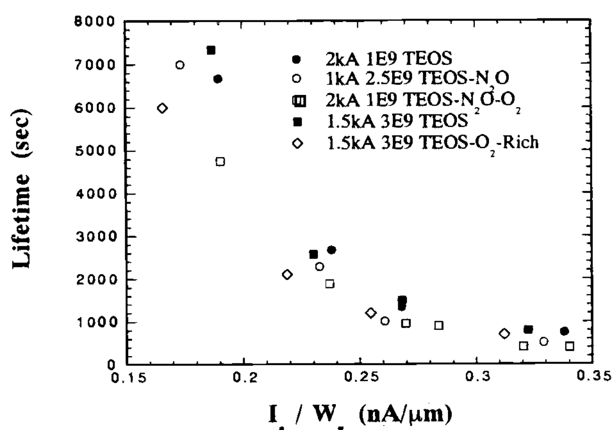

Fig. 6. p-Channel transistors with protective diodes hot-carrier lifetime plotted against gate current per unit gate width for various PE-TEOS IMD structures.

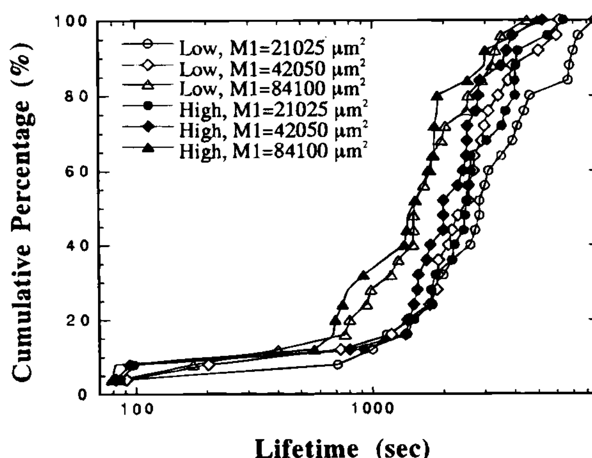

Fig. 7. p-Channel transistors with protective diodes hot-carrier lifetime plotted against gate current per unit gate width for various PE-TEOS IMD structures and various antenna areas.

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Investigations on Reaction Mechanisms in a Surface Modification Resist Process Using Chemical Vapor Deposition of Polysiloxane

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ABSTRACT

A surface modification resist process (SMR), in which polysiloxane is formed on the exposed resist surface by chemical vapor deposition, was studied for subquarter micron pattern fabrication. This paper describes the microscopic and macroscopic reaction mechanisms in SMR when methyltriethoxysilane is used as the chemical vapor deposition gas. Hydrolysis and condensation reactions occurring in acid-catalyzed polysiloxane formation were investigated through Fourier transform infrared spectroscopy. It was demonstrated that the hydrolysis is the dominant reaction rather than the condensation, and is dependent on the generated acid catalyst and sorbed water. Polysiloxane layer growth at the near resist surface was observed by Rutherford backscattering spectroscopy and from cross-sectional views of the polysiloxane layer. The polysiloxane layer initially grows in the resist film because of the dominant diffusion of methyltriethoxysilane molecules. Afterward the diffusion is prevented due to the excessive networking of the polysiloxane so that the polysiloxane layer grows on the resist surface. Furthermore, 0.20 μm pattern fabrication was demonstrated by applying SMR to KrF excimer laser lithography with an alternating phase-shifting mask.

Introduction

Optical lithography using a KrF (248 nm) or ArF (193 nm) excimer laser is an important technology for production of ultralarge scale integrated circuits (ULSIs) with subquarter micron features. A single-layer resist process generally has been developed, because a commercial infrastructure such as materials and equipments is steady. This process, however, results in an impractical lower focus latitude and poor accuracy of the pattern width due to reflection from the substrate for a fine pattern fabrication.

Top-surface imaging (TSI) is a very attractive process for overcoming these problems. Silylation, a process in which a silicon compound such as hexamethyldisilazane reacts with the phenolic hydroxyl group of the resist, has received much study.[1-3] Recently, a silylation process for ArF excimer laser lithography was reported by several researchers.[4,5]

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