An Analytic Saturation Model for Drain and Substrate Currents of Conventional and LDD MOSFET's

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***Abstract*—An analytic saturation model for conventional and LDD MOSFET's is developed by using the pseudo-two-dimensional approximation (PTDA) in the channel and drain regions to obtain both the channel length modulation factor and the maximum electric field. Using the established *I-V* model in the linear region, the drain currents of conventional and LDD MOSFET's can be explicitly calculated. Furthermore, the substrate currents of conventional/LDD MOSFET's are calculated by using an existing simplified substrate current formula and the developed maximum electric field model. Using a two-dimensional numerical MOS device simulator, it is shown that the accuracy of the developed maximum electric field model is acceptable for calculating the substrate currents of conventional/LDD MOSFET's. Moreover, the parameters used in the developed model can be determined by the existing extraction methods and the developed optimization technique. Comparing the calculated drain and substrate currents with the experimental data measured from the test transistors with conventional/LDD MOS structures, the developed saturation model is shown to be valid for a wide range of channel lengths and bias conditions.**

Nomenclature

$V_{gs}(V_{ds})$	External gate (drain) to source voltage.
V_{BG}	Substrate bias.
$V_{d'}(V_{s'})$	Intrinsic drain (source) voltage.
$V_{gs'}(=V_g - V_{g'})$	Intrinsic gate-source voltage.
$V_{d's'}(=V_{d'} - V_{s'})$	Intrinsic drain-source voltage.
$V_{d\,\text{sat}}$	Saturation drain-source voltage in the channel region.
I_{ds}	Drain current.
$I_{d\,\text{sat}}$	Drain current at the onset of saturation condition.
I_{sub}	Substrate current.
$R_d(R_s)$	Parasitic resistance of the drain (source).
$R_{nd}(R_{ns})$	Resistance of the lightly doped region near the drain (source) side of LDD MOS devices.
$L(W)$	Effective channel length (width).
$\Delta L_1(\Delta L_2)$	Channel length modulation factor in the channel (drain or n^-) region.
$t_{ox}(C_{ox})$	Oxide thickness (capacitance per unit area).
$\epsilon_{si}(\epsilon_{ox})$	Dielectric permittivity of silicon (oxide).
μ_n	Maximum electron mobility in the inversion layer of the active channel device.
V_{T0}	Threshold voltage at zero drain bias.
V_{FB}	Flat-band voltage of the active channel device.
$\phi_{s,\text{inv}}$	Surface potential at strong inversion condition.
$\phi(x)$	Electric potential in PTDA section.
α, η	Empirical constants for electron mobility in the inversion layer of the active channel device.
$E_c(=1/\beta)$	Critical electric field.
$V_{s1}(=\mu_n E_c)$	Saturation velocity.
d_0	Flowing path depth of the drain current in PTDA section near the channel side.
d_0'	Flowing path depth of the drain current at the pinch-off point.
$Y_d(x)$	Depletion width in PTDA section near the channel side.
Y_d	Depletion width in GCA section.
$N(y)$	Doping profile in the channel region.
Q_m	Mobile charge density.
$R_j(r_n)$	Junction depth of the drain (lightly doped) region.
W_d	Depletion width under the drain region.
$N_d(N_n)$	Doping concentration in the drain (lightly doped) region.
A_0, B_0	Empirical constants for the substrate current.
$E_{\max}$	Maximum electric field in PTDA section.

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I. Introduction

When the electric field near the drain side reaches the critical field for saturation velocity, a short-channel MOSFET will operate in the saturation region.

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Furthermore, the high electric field in the drain junction may result in carrier impact ionization and produces the substrate current. On the other hand, the pinch-off point of the inversion channel may move toward the source side as the drain bias increases, resulting in the rise-up of the drain current. In order to analyze the high-field effects of a short-channel MOSFET, a so-called pseudo-two-dimensional approximation, which can obtain the analytic expression, has been proposed by El-Mansy *et al.* [1]. Based on this approximation, Ko *et al.* [2] have proposed an unified model to characterize both the drain and substrate currents. Later on, this model has been further modified by using the empirical equation [3] in order to improve the existing deficiency. However, this model is valid only for the case of the uniformly doped substrate, which is not realistic for the currently fabricated MOS devices. Recently, Tanaka *et al.* [4], based on the same approach, have also proposed a self-consistent model by involving very complicated iterations in order to calculate the currents directly. However, both models mentioned above do not show wide-range validity for different biases and channel lengths. More recently, Mayaram *et al.* [5] have proposed a model for LDD MOSFET's, in which the electric field and the channel length modulation factor have been calculated by assuming the uniformly doped substrate. However, the channel length modulation factor is found not to be equal to zero at the onset of saturation condition. This deficiency will cause the discontinuity of the drain current at the transition between the linear and saturation regions.

In this paper, an analytic saturation model for conventional/LDD MOSFET's is presented. The major advantage of the proposed model is that the drain and substrate currents of conventional/LDD MOSFET's can be analytical calculated from the external voltages without any iterations. This property is very important for applications in circuit analysis. In Section II, the pseudo-two-dimensional approximation is applied to the channel and drain regions of conventional/LDD MOS structures to obtain both the channel length modulation factor and the maximum electric field. Based on the well-established *I-V* model for the linear region published in [6]–[9] and using the calculated channel length modulation factor, the drain current in the saturation region can be easily calculated. Using a simplified expression for the substrate current proposed by Chan *et al.* [10] and the calculated maximum electric field, the substrate current can be easily obtained. Since the simplified substrate current expression is very sensitive to the maximum electric field in the drain junction, a two-dimensional numerical MOS device simulator is used to verify the calculated maximum electric field. In Section III, the fabrication data of the fabricated conventional/LDD MOSFET's and the methods to extract the parameters for calculating the drain and substrate currents are described. In Section IV, the calculated drain and substrate currents are compared with the experimental data measured from the fabricated conventional/LDD MOSFET's. It is shown that good agreement between the developed model and the experimental results has been obtained for a wide range of biases and channel lengths by using a set of parameters, and the calculated drain current is continuous at the transition between the linear and saturation regions. In Section V, conclusions are given.

II. The Saturation Model

When a MOSFET is operated in the saturation region, the channel region can be divided into two sections, as shown in Fig. 1(a). One is called the gradual-channel-approximation (GCA) section, where the channel electric field is less than the critical field; the other is called the pseudo-two-dimensional-approximation (PTDA) section, where the electric field exceeds the critical field and carriers move with the saturation velocity.

A. The Gradual-Channel-Approximation Section

In this section, it is assumed that impact ionization can be neglected. This assumption is similar to that used in the channel region where the gradual-channel approximation is valid. Therefore, the drain current in the saturation region can be calculated from the formulas derived for the linear region with slight modifications. Based on our previously published model [6]–[9], the drain current in the linear region can be written as

$$I_{ds} = \frac{\mu_n C_{ox} W (V_{gs'} - V_{T0} - aV_{d's'}) V_{d's'}}{L\left\{1 + \frac{\alpha C_{ox}}{2\epsilon_{si}} [V_{gs'} + V_{T0} - 2(V_{FB} + \phi_{s,\text{inv}}) - bV_{d's'}] + \left(\eta + \frac{\beta}{L}\right) V_{d's'}\right\}} \tag{1}$$

where

$$V_{d's'} = V_{ds} - I_{ds}(R_s + R_d)$$

and

$$V_{gs'} = V_{gs} - I_{ds} R_s$$

as shown in Fig. 1(b); $a = \frac{1}{2} - k$, $b = \frac{1}{2} + k$, and k is the slope of the threshold voltage with respect to V_{ds} at zero drain bias. The parameters used above have been defined in [6]–[9], which can be easily determined by a series of extraction techniques.

Substituting L and $V_{d's'}$ with $L - \Delta L_1$ and $V_{d\,\text{sat}}$, respectively, the drain current in the saturation region can

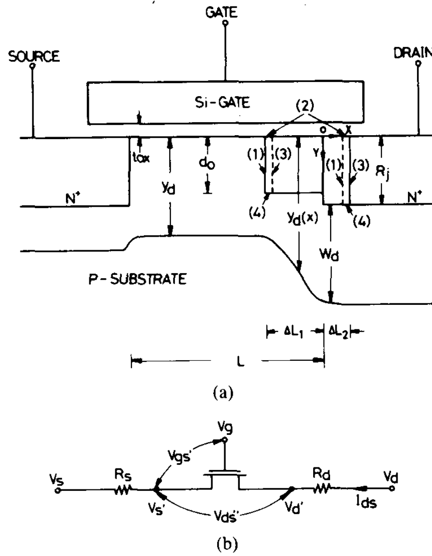


Fig. 1. (a) The schematic diagram of a MOSFET operated in the saturation region. (b) Equivalent circuit of a MOSFET.

be written as

$$I_{ds} = \frac{\mu_n C_{ox} W (V_{gs'} - V_{T0} - aV_{d\,sat}) V_{d\,sat}}{(L - \Delta L_1)\left\{1 + \frac{\alpha C_{ox}}{2\epsilon_{si}}[V_{gs'} + V_{T0} - 2(V_{FB} + \phi_{s,inv}) - bV_{d\,sat}] + \left(\eta + \frac{\beta}{L - \Delta L_1}\right) V_{d\,sat}\right\}} \quad (2)$$

where ΔL_1 is the channel length modulation factor in the channel region, which can be calculated directly from the terminal voltages and will be given in Section II-B; $V_{d\,sat}$ is the saturation voltage in the channel region, which can be obtained from equations in [6] by setting R_{ns} equal to zero.

Using $V_{gs'} = V_{gs} - I_{ds}R_s$ and (2), I_{ds} can be solved as [6]

$$I_{ds} = \frac{-B_1 + (B_1^2 - 4A_1C_1)^{1/2}}{2A_1} \quad (3)$$

where

$$A_1 = -\frac{\alpha C_{ox}}{2\epsilon_{si}} R_s \quad (4)$$

$$B_1 = 1 + \frac{\alpha C_{ox}}{2\epsilon_{si}}[V_{gs} + V_{T0} - 2(V_{FB} + \phi_{s,inv}) - bV_{d\,sat}] + \left(\eta + \frac{\beta}{L - \Delta L_1}\right) V_{d\,sat} + \frac{\mu_n C_{ox} W}{L - \Delta L_1} R_s V_{d\,sat} \quad (5)$$

$$C_1 = -\frac{\mu_n C_{ox} W}{L - \Delta L_1}(V_{gs} - V_{T0} - aV_{d\,sat}) V_{d\,sat}. \quad (6)$$

It is noted that the drain current can be directly calculated from the terminal voltages.

B. The Pseudo-Two-Dimensional-Approximation Section

In order to consider the two-dimensional effects in the drain region and apply the developed model to LDD MOS devices, the PTDA method is used in both channel and drain regions. It is assumed that the channel current in this section is uniformly distributed with the finite depths of d_0 and R_j for the channel and drain edges, respectively. By applying Gauss' law to the rectangular boxes labeled (1)–(4) for both regions as shown in Fig. 1(a), we obtain the following equation for the channel region:

$$E_c d_0 - \int_{-\Delta L_1}^{x} \frac{C_{ox}}{\epsilon_{si}}[V_{gs'} - V_{FB} - \phi_{s,inv} - \phi(x)] \cdot dx - d_0 \frac{d\phi}{dx} + \frac{q}{\epsilon_{si}} \int_{-\Delta L_1}^{x} \int_{d_0}^{Y_d(x)} N(y)\, dy\, dx = -\frac{q}{\epsilon_{si}} \int_{-\Delta L_1}^{x} \int_{0}^{d_0} N(y)\, dy\, dx - \int_{-\Delta L_1}^{x} \frac{Q_m}{\epsilon_{si}} dx. \quad (7)$$

Similarly, the equation in the drain region can be written as

$$R_j \frac{d\phi}{dx} - \int_{x}^{\Delta L_2} \frac{C_{ox}}{\epsilon_{si}}[V_{gs'} - V_{FB} - \phi_{s,inv} - \phi(x)] \cdot dx - E_c R_j + \frac{q}{\epsilon_{si}} \int_{x}^{\Delta L_2} \int_{R_j}^{R_j + W_d(x)} N(y)\, dy\, dx = \frac{q}{\epsilon_{si}} \int_{x}^{\Delta L_2} N_d R_j\, dx - \int_{x}^{\Delta L_2} \frac{Q_m}{\epsilon_{si}} dx. \quad (8)$$

From (7) and (8), the differential equations for the potential distribution in both regions can be written as (see Appendixes I, II)

$$\frac{d^2\phi}{dx^2} - \theta_1^2 \phi = -\theta_1^2 (G_1 + V_{d\,sat}), \qquad -\Delta L_1 \le x \le 0 \quad (9)$$

and

$$\frac{d^2\phi}{dx^2} - \theta_2^2 \phi = -\theta_2^2 (G_2 + V_{d's'}), \qquad 0 \le x \le \Delta L_2 \quad (10)$$

where

$$\theta_1 = \left[\frac{C_{ox}}{\epsilon_{si} d_0}\right]^{1/2} \tag{11}$$

$$\theta_2 = \left[\frac{C_{ox}}{\epsilon_{si} R_j}\right]^{1/2} \tag{12}$$

$$G_1 = -\left\{\frac{q}{C_{ox}}\left[\frac{1}{2}(SA + SB) + SC\right] - (V_{gs'} - V_{FB} - \phi_{s'\text{inv}}) + \frac{2I_{d\,\text{sat}}}{C_{ox} V_{s1} W}\right\} - V_{d\,\text{sat}} \tag{13}$$

and

$$G_2 = -\left\{\frac{q}{C_{ox}}[SB - N_d R_j] - (V_{gs'} - V_{FB} - \phi_{s'\text{inv}}) + \frac{2I_{d\,\text{sat}}}{C_{ox} V_{s1} W}\right\} - V_{d's'}. \tag{14}$$

Note that SA, SB, and SC are defined in Appendix I and are explicitly calculated for a MOSFET with double-channel-boron implantations by using the step-profile approximation [7]; $I_{d\,\text{sat}}$ is the drain current at the onset of saturation condition; and $V_{gs'}$ and $V_{d's'}$ can be simply expressed as

$$V_{gs'} = V_{gs} - I_{d\,\text{sat}} R_s \tag{15}$$

$$V_{d's'} = V_{ds} - I_{d\,\text{sat}}(R_s + R_d). \tag{16}$$

Using the following boundary conditions:

$$\phi\big|_{x=-\Delta L_1} = V_{d\,\text{sat}} \qquad \frac{d\phi}{dx}\bigg|_{x=-\Delta L_1} = E_c$$

$$\phi\big|_{x=0^-} = \phi\big|_{x=0^+} \qquad \frac{d\phi}{dx}\bigg|_{x=0^-} = \frac{d\phi}{dx}\bigg|_{x=0^+}$$

$$\phi\big|_{x=\Delta L_2} = V_{d's'} \qquad \frac{d\phi}{dx}\bigg|_{x=\Delta L_2} = E_c \tag{17}$$

the differential equatons in (9) and (10) can be solved and written as

$$\phi(x) = E_1 \exp(\theta_1 x) + F_1 \exp(-\theta_1 x) + G_1 + V_{d\,\text{sat}}, \quad -\Delta L_1 \le x \le 0 \tag{18}$$

$$\phi(x) = E_2 \exp(\theta_2 x) + F_2 \exp(-\theta_2 x) + G_2 + V_{d's'}, \quad 0 \le x \le \Delta L_2 \tag{19}$$

where

$$E_1 = \frac{1}{2}\left(-G_1 + \frac{E_c}{\theta_1}\right)\exp(\theta_1 \Delta L_1) = Q_{a1}\exp(\theta_1 \Delta L_1) \tag{20}$$

$$F_1 = \frac{1}{2}\left(-G_1 - \frac{E_c}{\theta_1}\right)\exp(-\theta_1 \Delta L_1) = Q_{b1}\exp(-\theta_1 \Delta L_1) \tag{21}$$

$$E_2 = \frac{1}{2}\left(-G_2 + \frac{E_c}{\theta_2}\right)\exp(-\theta_2 \Delta L_2) = Q_{a2}\exp(-\theta_2 \Delta L_2) \tag{22}$$

$$F_2 = \frac{1}{2}\left(-G_2 - \frac{E_c}{\theta_2}\right)\exp(\theta_2 \Delta L_2) = Q_{b2}\exp(\theta_2 \Delta L_2). \tag{23}$$

Using $Q_b = G_2 + V_{d's'} - G_1 - V_{d\,\text{sat}}$ and the boundary conditions in (17), we obtain the following quadratic equation: (see Appendix III)

$$A_2[Q_{a1}\exp(\theta_1 \Delta L_1) + Q_{b1}\exp(-\theta_1 \Delta L_1)]^2 + B_2[Q_{a1}\exp(\theta_1 \Delta L_1) + Q_{b1}\exp(-\theta_1 \Delta L_1)] + C_2 = 0 \tag{24}$$

where

$$A_2 = -(\theta_2^2 - \theta_1^2) \tag{25}$$

$$B_2 = 2\theta_2^2 Q_b \tag{26}$$

$$C_2 = -4\theta_1^2 Q_{a1} Q_{b1} + 4\theta_2^2 Q_{a2} Q_{b2} - \theta_2^2 Q_b^2. \tag{27}$$

Solving (24) for the bracketed term, we obtain

$$[Q_{a1}\exp(\theta_1 \Delta L_1) + Q_{b1}\exp(-\theta_1 \Delta L_1)] = \frac{-B_2 + (B_2^2 - 4A_2 C_2)^{1/2}}{2A_2} = A_{n1}. \tag{28}$$

Equation (28) can be further rewritten as

$$Q_{a1}\exp(\theta_1 \Delta L_1)^2 - A_{n1}\exp(\theta_1 \Delta L_1) + Q_{b1} = 0. \tag{29}$$

Solving (29), $\exp(\theta_1 \Delta L_1)$ can be written as

$$\exp(\theta_1 \Delta L_1) = \frac{A_{n1} + (A_{n1}^2 - 4Q_{a1} Q_{b1})^{1/2}}{2Q_{a1}} = A_{n2}. \tag{30}$$

Therefore, ΔL_1 can be expressed by

$$\Delta L_1 = \frac{\ln(A_{n2})}{\theta_1}. \tag{31}$$

Similarly, $\exp(\theta_2 \Delta L_2)$ and ΔL_2 can be calculated as

$$\exp(\theta_2 \Delta L_2) = \frac{-B_{n1} + (B_{n1}^2 - 4Q_{a2} Q_{b2})^{1/2}}{2Q_{b2}} = B_{n2} \tag{32}$$

and

$$\Delta L_2 = \frac{\ln(B_{n2})}{\theta_2} \tag{33}$$

where $B_{n1} = Q_b - E_1 - F_1$.

Note that $I_{d\,\text{sat}}$ is the drain current at the onset of satu-

TABLE I
THE EXTRACTED PARAMETERS FOR THE CHANNEL DOPING PROFILE USING THE STEP-PROFILE APPROXIMATION SHOWN IN FIG. 8

Parameters / MOS Structures	t_{ox}(Å)	N_{AS}(cm^{-3})	N_{AD}(cm^{-3})	N_{AB}(cm^{-3})	Y_B(μm)	W_b(μm)	V_{FB}(V)	R_j, r_n(μm)	N_d, N_n(cm^{-3})
Conventional	250	3.80×10^{16}	8.07×10^{15}	3.97×10^{14}	0.18	0.54	-0.60	0.33	1.8×10^{20}
LDD	250	4.08×10^{16}	8.97×10^{15}	4.13×10^{14}	0.17	0.51	-0.60	0.25	1.0×10^{18}

ration condition and is independent of ΔL_1. Therefore, G_1 in (13) and G_2 in (14) can be easily calculated from the terminal voltages. Moreover, Q_{a1}, Q_{b1}, Q_{a2}, Q_{b2}, and Q_b are expressed in terms of G_1 and G_2, so A_{n1} in (28) can be obtained from the terminal voltages. Therefore, it is easily seen that ΔL_1 in (31) can be calculated from the terminal voltages without any iterations. Similarly, the same conclusion can be given to ΔL_2 in (33). Besides, ΔL_1 and ΔL_2 are equal to zero at the onset of saturation condition, the drain current is therefore continuous at the transition between the linear and saturation regions.

C. The Substrate Current

In order to obtain the analytic form for the substrate current, a simplified substrate current expression proposed in [10] is used and expressed as

$$I_{sub} = A_0 E_{max} I_{ds} \exp\left(-\frac{B_0}{E_{max}}\right) \tag{34}$$

where I_{ds} can be obtained by (3); A_0 and B_0 are the fitting parameters, which can be determined by the least square method; E_{max} is the maximum electric field and can be expressed as

$$E_{max} = \theta_1(E_1 - F_1) \tag{35}$$

in which θ_1, E_1, and F_1 can be calculated by (11), (20), and (21), respectively.

From (34), it is clearly seen that the accuracy of E_{max} in (35) is extremely important for calculating the substrate current. Using the parameters listed in Tables I and II, Fig. 2(a) shows a comparison of the calculated E_{max} between the developed analytic model in (35) and the numerical simulation for different external drain/gate biases and gate oxide thicknesses.[1] It is shown that the accuracy of the calculated maximum electric field using (35) for conventional MOSFET's is acceptable.

D. Applications to LDD MOSFET's

For LDD MOS devices, the electric field distribution in the lightly doped n^- region becomes very complicated, depending on the doping concentration in the n^- region and its overlap with respect to the gate. However, if the maximum electric field occurs at the channel-n^- junction in the drain side and the channel length modulation factor in the n^- region does not exceed the gate edge, the de-

[1]The numerical analysis presented in the text was accomplished by an efficient 2-D MOS simulator called SUMMOS (Submicrometer MOS), which has been developed by the Advanced Semiconductor Device and Technology Research Division, National Chiao-Tung University, Taiwan, Republic of China.

TABLE II
THE EXTRACTED PARAMETERS FOR SIMULATING THE DRAIN CURRENT IN THE LINEAR REGION

Parameters / MOS Structures	μ_n(cm^{-2}/V-s)	α(cm/v)	η(1/V)	β(cm/v)	R_s, R_d(Ω)
Conventional	671.46	1.76×10^{-6}	5.94×10^{-2}	4.83×10^{-5}	11.27
LDD	604.88	1.18×10^{-6}	5.04×10^{-2}	5.22×10^{-5}	11.27

veloped model can be easily extended to the LDD MOS devices with slight modifications. The major modifications are that R_j, N_d, R_s, and R_d in the above derived formulas are replaced by r_n, N_n, $R_s + R_{ns}$, and $R_d + R_{nd}$, respectively. Note that R_{ns} and R_{nd} can be analytically calculated from the formulas presented in [6]. In order to verify the accuracy of the calculated maximum electric field in LDD MOS structure, the device parameters listed in Tables I and II are used for both the analytic model and the two-dimensional (2-D) numerical analysis. A comparison of the calculated maximum electric field between the developed analytic model and the numerical analysis[1] for LDD MOS devices with different gate oxide thicknesses and the n^- doping concentration of $10^{18}/cm^3$ is shown in Fig. 2(b), and a similar comparison for different n^- doping concentrations and the gate oxide thickness of 250 Å is shown in Fig. 2(c). It is clearly seen that the accuracy of the maximum electric fields calculated by the developed analytic model is also acceptable for applications in LDD MOS devices with different gate oxide thicknesses and n^- doping concentrations. It should be noted that the doping concentration in the n^- region used for the above calculations is equal to or larger than $10^{17}/cm^3$, the maximum electric field occurs at the channel-n^- junction. However, as the doping concentration in the n^- region is lighter, the substrate current of LDD MOS devices may exhibit a double-hump characteristic for high gate bias. This phenomenon is mainly due to high source-to-drain conductivity modulated by the gate, and the peak electric field occurs not only in the drain side but also in the source side. It is noted from 2-D device simulations that the peak electric field in the drain side occurs simultaneously at the channel-n^- and n^--n^+ junctions [5], [11]. Moreover, the peak electric field may occur near the gate edge of the n^- region in the source side if the applied gate voltage is further increased [12], [13]. Since the substrate current is caused by the effects of carrier impact ionization, both the electric field and the avalanche rate must be simultaneously considered. As described in [13], the location of the peak electric field near the gate edge of the n^- region in the source side is always operated in the accumulation mode, resulting in a higher avalanche

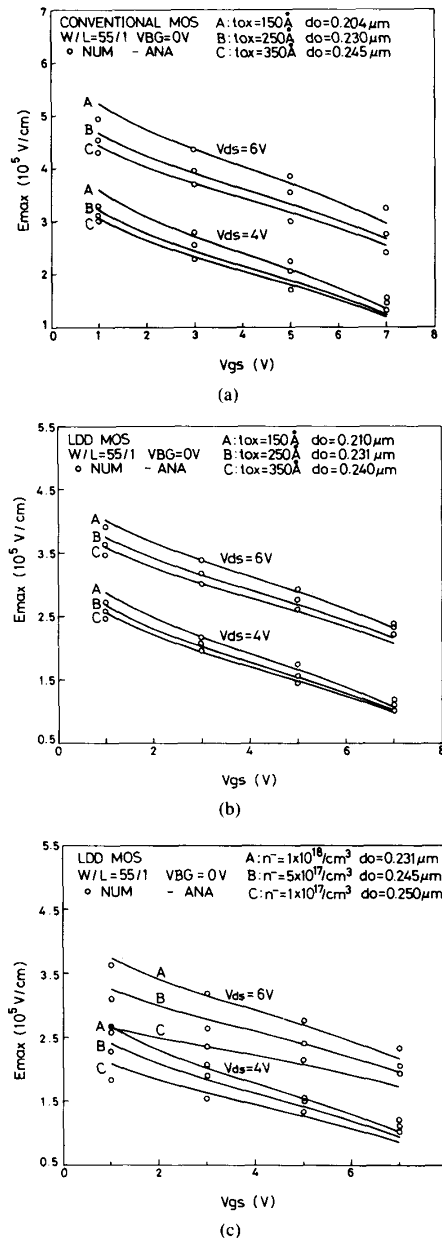


Fig. 2. Comparisons of the maximum electric field between the developed analytic model and the numerical analysis for (a) conventional MOS devices with different gate-oxide thicknesses, (b) LDD MOS devices with different gate-oxide thicknesses, (c) LDD MOS devices with different n^- doping concentrations.

rate than in the drain side. This is the major reason that the substrate current is increased with increasing the applied gate voltage after the first substrate current peak. The analytic modeling of this phenomenon is quite complicated and is beyond the scope of our developed model. Furthermore, from our numerical analysis, it has been shown that the developed analytic model is valid for all self-aligned MOS devices, and will produce appreciable errors for the cases when the polysilicon gate edge does not overlap the lightly doped n^- region.

III. Experimental Data and Parameter Determination

A. Fabrication Data and Measurements

Experimental Si-gate n-channel MOSFET's with conventional/LDD MOS structures were fabricated by using a set of test structures with the designed mask channel lengths of 1.3, 1.5, 1.7, 2.0, 2.4, 3.0, and 27.5 μm, and the designed mask channel width of 55 μm. Note that the silicon substrate used was of ⟨100⟩ orientation and its resistivity was about 40–60 $\Omega \cdot$ cm. The process sequences for conventional and LDD MOS devices were quite standard. The double-channel-boron implantations were performed through the gate oxide of 250 Å with an energy of 25 keV and a dose of $7.5 \times 10^{11}/\text{cm}^2$ for shallow implantation and with an energy of 150 keV and a dose of $4 \times 10^{11}/\text{cm}^2$ for deep implantation. The lightly doped regions of the LDD MOS structure were formed by implanting the phosphorus ions with an energy of 30 keV and a dose of $3 \times 10^{13}/\text{cm}^2$. After depositing the CVD oxide on the polysilicon gate, the sidewall spacers of LDD MOS devices were formed by using a directional RIE. Then, the source–drain n^+ regions were implanted with an energy of 60 keV and a dose of $6 \times 10^{15}/\text{cm}^2$.

The gate oxide thickness (250 Å) of the fabricated conventional/LDD MOS devices was measured by the control sample after the gate oxide growth using an ellipsometer and checked by the fabricated MOS capacitor using the C–V measurement. The junction depths of the lightly doped and n^+ regions and the width of the spacer were measured by an auto-spreading resistance probe and the SEM cross-section technique, respectively. The junction depths in the lightly doped and n^+ regions are 0.25 and 0.33 μm, respectively. The spacer width (l_1) is 0.2 μm and the lateral diffusion depth of the lightly doped region (l_2) is 0.2 μm. The threshold voltages and the drain and substrate currents were measured by using a personal-computer-controlled HP 4145B.

B. Model Parameter Extractions and Optimizations

As shown in (2) and (34), several model parameters need to be determined in order to calculate the threshold voltage, the drain current, and the substrate current. Referring to our previous papers [6], [7], the channel doping profile with double-boron implantations can be approximated by a double-steps profile shown in Fig. 8, and the parameters in the threshold voltage model can be extracted by comparing the measured threshold voltages under different substrate biases with the theoretical results as listed in Table I. Using the linear-region resistance versus $(V_{gs} - V_{T0} - \frac{1}{2}V_{ds})^{-1}$ curve and its slope and intercept measured from the fabricated MOS devices with different mask channel lengths, as described in [6], [8], [9], the effective channel lengths of the fabricated conventional and LDD MOS devices and the model parameters listed in Table II can be extracted. Using the extracted parameters listed in Tables I and II, the drain currents of conventional and LDD MOS devices operated in the linear region can be calculated. In order to fit the drain and

substrate currents in the saturation region simultaneously, the model parameters in ionization coefficient (A_0 and B_0) and the flowing path depth of the drain current in the PTDA section near the channel side (d_0) must be optimized. In our optimization process, two kinds of errors based on (1) and (34) are defined. One is the error for the drain current, which is expressed as

$$ER_{ds} = \sum_i \left| I_{ds,\exp,i} - I_{ds,\text{sim},i} \right| L_i \quad (36)$$

the other is the error for the substrate current, which is expressed as

$$\text{ER}_{\text{sub}} = \sum_i \ln \left(\frac{I_{\text{sub},\exp,i}}{I_{ds,\text{sim},i} E_{\max,\text{sim},i}} \right) - \ln (A_0) + \left(\frac{B_0}{E_{\max,\text{sim},i}} \right)^2 \quad (37)$$

where the subscripts of sim, exp, and i represent the simulation results, experimental data, and different bias conditions or geometric structures, respectively.

Applying the least squares method to (37), A_0 and B_0 can be determined by solving the following equations:

$$A_{11} \ln (A_0) + A_{12} B_0 = B_{11} \quad (38)$$

and

$$A_{21} \ln (A_0) + A_{22} B_0 = B_{21} \quad (39)$$

where A_{11}, A_{12}, A_{21}, A_{22}, B_{11}, and B_{21} are defined in Appendix IV.

Based on (36) and (37), d_0 can be determined as these two errors are within the assigned values. The flow chart for determining A_0, B_0, and d_0 is shown in Fig. 3, and the extracted values are listed in Table III. Using the extracted parameters listed in Tables II and III, the drain and substrate currents in the saturation region can be calculated.

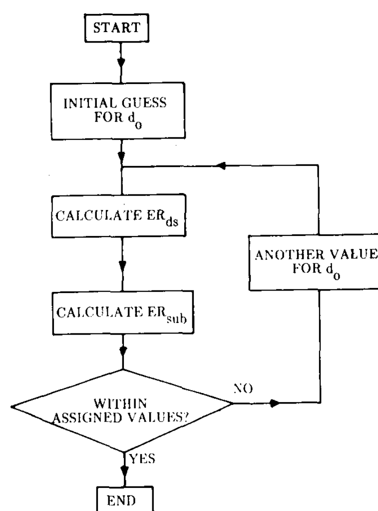


Fig. 3. The flow chart for determining d_0, A_0, and B_0.

TABLE III
THE PARAMETERS FOR SIMULATING THE SUBSTRATE CURRENT

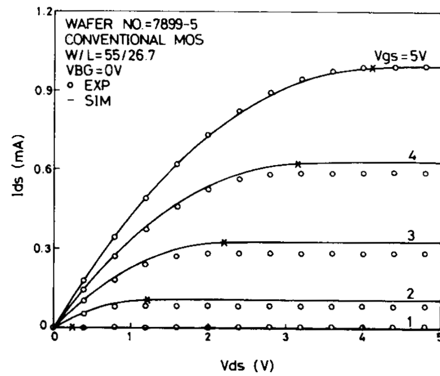
Parameters / MOS Structures	d_0(μm)	A_0(cm/V)	B_0(V/cm)
Conventional	0.230	6.71×10^{-5}	3.00×10^{6}
LDD	0.231	5.82×10^{-5}	3.10×10^{6}

IV. Comparisons Between Experimental Results and Simulations

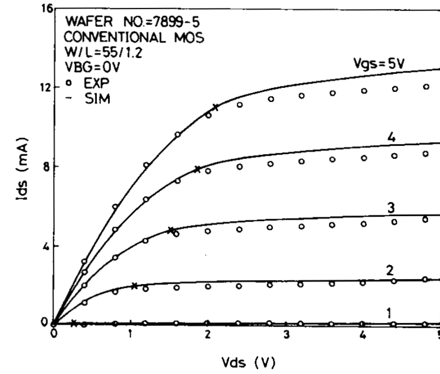
Using the extracted model parameters described in the previous section, Figs. 4 and 5 show comparisons between the experimental data and the developed model for the drain and substrate currents of conventional MOS devices, and good agreements are obtained for conventional MOS devices with a wide range of channel lengths and bias conditions by using only a set of extracted parameters. The asterisks on the I–V curves indicate the calculated saturation voltages. It is easy to see that the calculated drain current is continuous at the transition between the linear and saturation regions. This consequence is mainly due to the fact that the derived ΔL_1 is equal to zero at the onset of the saturation condition. Note that the effect of carrier impact ionization has been neglected in the linear region, and the calculated substrate current shown is only limited to the saturation region. However, the interesting range of the substrate current is almost included. Similarly, Figs. 6 and 7 show comparisons between the experimental data and the developed model for the drain and substrate currents of LDD MOS devices. It is clearly seen that satisfactory agreements are also obtained for LDD MOS devices with a wide range of channel lengths and bias conditions by using only a set of extracted parameters even though ΔL_2 may extend outside the gate region for some bias conditions. It should be noted that the implanted dose in the n^- region of the fabricated LDD devices is $3 \times 10^{13}/\text{cm}^2$ which is equivalent to the doping concentration of about $10^{18}/\text{cm}^3$; the measured substrate currents do not exhibit the double-hump characteristics.

V. Conclusions

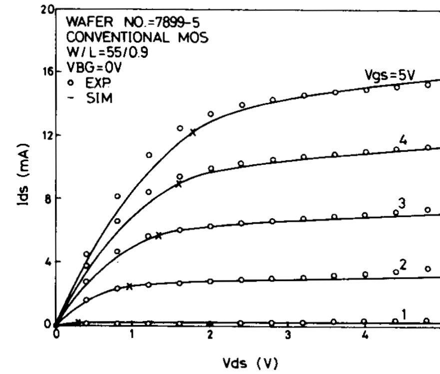
In this paper, an analytic saturation model has been developed for conventional and LDD MOS devices by using the pseudo-two-dimensional approximation in the channel and drain regions to simultaneously obtain both the channel length modulation factor and the maximum electric field. Using our published models for the I–V characteristics in the linear region, the drain currents of conventional and LDD MOS devices in the saturation region are analytically derived. The calculated drain current is shown to be continuous at the transition between the linear and saturation regions. Using a simplified substrate current formula and the derived maximum electric field, the substrate currents of conventional and LDD MOS devices can be easily calculated. The extraction techniques for the model parameters in the derived I–V model are presented. Furthermore, the accuracy of the developed maximum electric field model for conventional and LDD MOS devices is verified by a 2-D numerical analysis. In order to verify the accuracy of the developed saturation model, the calculated drain and substrate currents are compared with the experimental results measured from the fabricated test



(a)

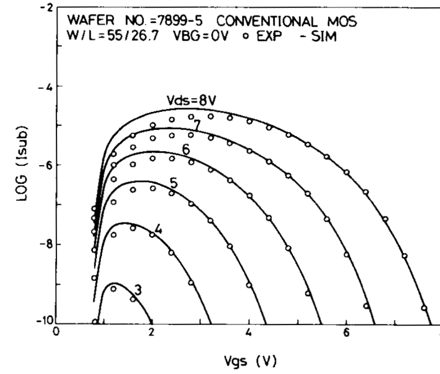


(b)

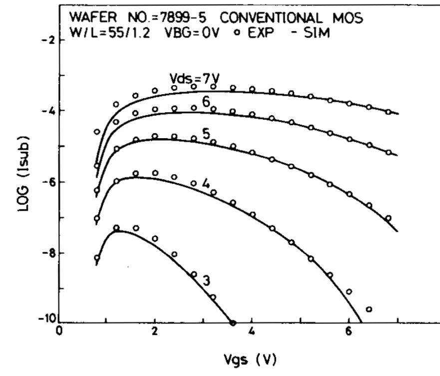


(c)

Fig. 4. Comparisons between the measured and calculated I-V characteristics of conventional MOS devices with (a) $L = 26.7$ μm, (b) $L = 1.2$ μm, (c) $L = 0.9$ μm.



(a)



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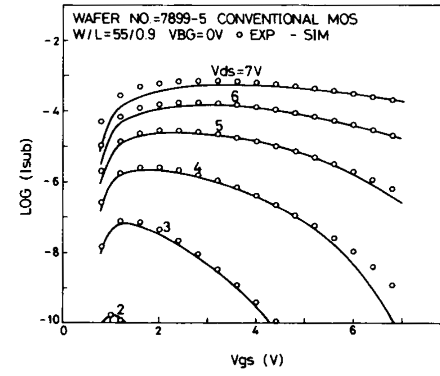


(c)

Fig. 5. Comparisons between the measured and calculated substrate currents of conventional MOS devices with (a) $L = 26.7$ μm, (b) $L = 1.2$ μm, (c) $L = 0.9$ μm.

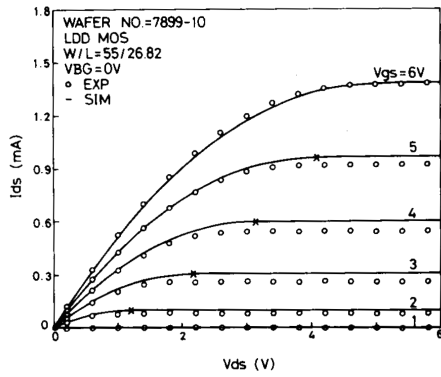
devices with conventional/LDD MOS structures, and a good agreement is obtained for a wide range of channel lengths and bias conditions by using a set of extracted parameters. Therefore, the developed I-V model can be used for device design and circuit analysis in a CAD system.

Appendix I

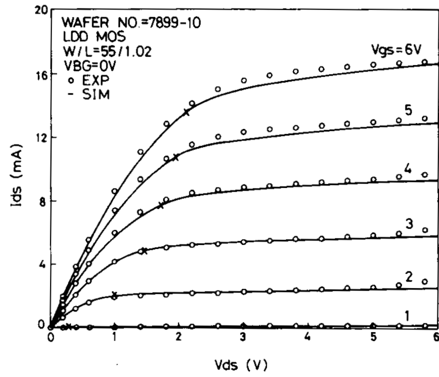
For a MOSFET operated in the saturation region, the drain current will spread out from the pinch-off point to the drain region, and the depletion width below the drain current is a complicated function along the channel direction. For simplicity, it is assumed that

$$\int_{d_0}^{Y_d(x)} N(y)\, dy$$

can be calculated by averaging the integrations in the GCA section and in the drain region, and the depletion width under the drain region is constant along the drain direc-



(a)



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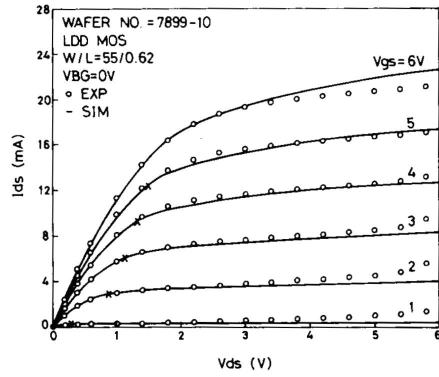
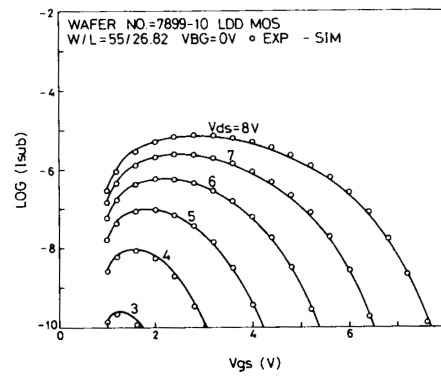
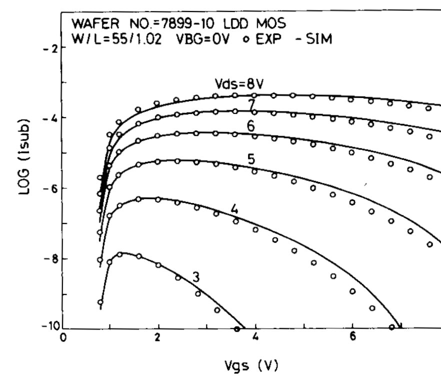


(c)

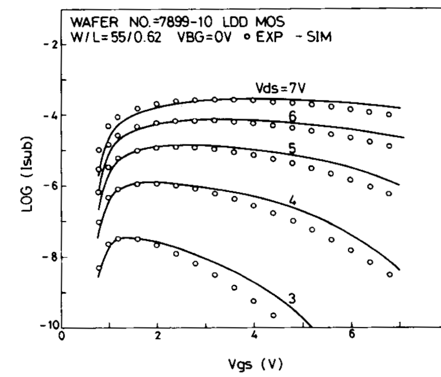
Fig. 6. Comparisons between the measured and calculated I-V characteristics of LDD MOS devices with (a) $L = 26.82$ μm, (b) $L = 1.02$ μm, (c) $L = 0.62$ μm.



(a)



(b)



(c)

Fig. 7. Comparisons between the measured and calculated substrate currents of LDD MOS devices with (a) $L = 26.82$ μm, (b) $L = 1.02$ μm, (c) $L = 0.62$ μm.

tion. Therefore, we obtain

$$\int_{d_0}^{Y_d(x)} N(y)\, dy = \tfrac{1}{2}(SA + SB) \qquad \text{(A1)}$$

where

$$SA = \int_{d_0'}^{Y_d} N(y)\, dy$$

and

$$SB = \int_{R_j}^{W_d(x) + R_j} N(y)\, dy \simeq \int_{R_j}^{W_d + R_j} N(y)\, dy.$$

Y_d is the depletion width in the GCA section, which can be obtained from the formula in [7]; W_d is the depletion

width under the drain region, which can be easily calculated from the one-dimensional Poisson's equation; d_0' is the spreading depth of the drain current at the pinch-off point, which can be expressed as

$$d_0' = \frac{K_B T}{q|E_s|} \tag{A2}$$

where E_s is the surface electric field and can be calculated from [7]. It is noted that d_0' is always less than Y_d.

The integration of

$$\int_0^{d_0} N(y)\, dy$$

can be expressed as

$$\int_0^{d_0} N(y)\, dy = SC. \tag{A3}$$

Note that SA, SB, and SC used above can be explicitly calculated by using the step-profile approximation. For a double-channel-implanted profile as shown in Fig. 8, we obtain

$$\begin{aligned} SA &= (N_{AS} + N_{AB})(Y_d - d_0'), \quad \text{for } Y_d \le Y_s \\ &= N_{AS}(Y_s - d_0') + N_{AD}(Y_d - Y_s) + N_{AB}(Y_d - d_0'), \\ &\qquad \text{for } Y_s \le Y_d \le Y_s + W_b \\ &= N_{AS}(Y_s - d_0') + N_{AD}W_b + N_{AB}(Y_d - d_0'), \\ &\qquad \text{for } Y_s + W_b \le Y_d \end{aligned} \tag{A4}$$

$$\begin{aligned} SB &= (N_{AD} + N_{AB})W_d, \quad \text{for } R_j + W_d \le Y_s + W_b \\ &= (Y_s + W_b - R_j)N_{AD} + N_{AB}W_d, \\ &\qquad \text{for } R_j + W_d \ge Y_s + W_b \end{aligned} \tag{A5}$$

$$\begin{aligned} SC &= (N_{AS} + N_{AB})d_0, \quad \text{for } d_0 \le Y_s \\ &= N_{AS}Y_s + N_{AD}(d_0 - Y_s) + N_{AB}d_0, \\ &\qquad \text{for } Y_s \le d_0 \le Y_s + W_b \\ &= N_{AS}Y_s + N_{AD}W_b + N_{AB}d_0, \quad \text{for } Y_s + W_b \le d_0. \end{aligned} \tag{A6}$$

Appendix II

The mobile carriers in PTDA section are assumed to move with the saturation velocity. However, the mobility model used in the text is a hyperbolic form, and V_{s1} will be overestimated by using $V_{s1} = \mu_n E_c$ ($E_c = 1/\beta$). In order to improve this deficiency, the drift velocity at the onset of saturation is equal to $V_{s1}/2$ which can be obtained from

$$V_{\text{drift}} = \frac{\mu_n E}{1 + \dfrac{E}{E_c}}$$

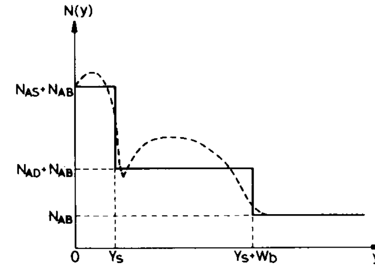


Fig. 8. A schematic diagram showing the double-channel-implanted profile approximated by a step profile.

by setting $E = E_c$. In order to simplify the analysis, the drain current in PTDA section is assumed to be equal to $I_{d\,\text{sat}}$, so the mobile charge density in (7) and (8) can be written as

$$Q_m = \frac{I_{d\,\text{sat}}}{WV_{\text{drift}}(E_c)} = \frac{2I_{d\,\text{sat}}}{WV_{s1}}. \tag{A7}$$

Appendix III

Using the boundary conditions in (17), we can obtain

$$E_1 + F_1 = E_2 + F_2 + Q_b \tag{A8}$$

$$\theta_1 E_1 - \theta_1 F_1 = \theta_2 E_2 - \theta_2 F_2. \tag{A9}$$

After some mathematical manipulations, (A8) and (A9) can be rewritten as

$$2\theta_2 E_2 = (\theta_2 + \theta_1)E_1 + (\theta_2 - \theta_1)F_1 - \theta_2 Q_b \tag{A10}$$

$$2\theta_2 F_2 = (\theta_2 - \theta_1)E_1 + (\theta_2 + \theta_1)F_1 - \theta_2 Q_b. \tag{A11}$$

Multiplying (A10) by (A11), ΔL_2 can be omitted, and (24) can be obtained.

Appendix IV

Applying the least squares method to (37), we can obtain

$$\frac{dER_{\text{sub}}}{d \ln (A_0)} = 0 \tag{A12}$$

and

$$\frac{dER_{\text{sub}}}{dB_0} = 0. \tag{A13}$$

Using (A12) and (A13), the coefficients in (38) and (39) can be easily obtained as

$$A_{11} = \sum_i 1 \tag{A14}$$

$$A_{12} = \sum_i \frac{-1}{E_{\text{max,sim},i}} \tag{A15}$$

$$A_{21} = -A_{12} \tag{A16}$$

$$A_{22} = \sum_i \frac{-1}{E^2_{\text{max,sim},i}} \tag{A17}$$

$$B_{11} = \sum_i \ln\left(\frac{I_{\mathrm{sub,exp},i}}{I_{ds,\mathrm{sim},i}E_{\mathrm{max,sim},i}}\right) \quad \text{(A18)}$$

$$B_{21} = \sum_i \ln\left(\frac{I_{\mathrm{sub,exp},i}}{I_{ds,\mathrm{sim},i}E_{\mathrm{max,sim},i}}\right)(E_{\mathrm{max,sim},i})^{-1}. \quad \text{(A19)}$$

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