國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

金氧半及鰭式場效電晶體閘極穿隧電流之
先進模擬及其潛在應用

Advanced Modeling of Gate Tunneling Current in CMOSFETs and FinFETs and Its Potential Application

研 究 生 ：許智育

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研 究 生：許智育　　Student：Chih-Yu Hsu
指導教授：陳明哲 博士　　Advisor：Dr. Ming-Jer Chen

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摘　　要

應用於傳統多晶矽閘極以及現代高介電金屬閘極場效電晶體的直接穿隧電流和 Fowler-Nordheim 穿隧電流的解析模型，已在本文建構完成。除此之外，有關缺陷如何提供額外穿隧電流的相關模型也同時被探討及建立。藉由自力完成的量子模擬器所計算出的能階值及已知的等效質量，此穿隧電流模型的可靠度已被完整的驗證。尤其，基於此模型，先進技術的潛在應用則首次被提出。藉由此嶄新提出的技巧，製程及材料參數可以被正確的萃取，而此得到的參數則可以對元件的組成本質及其對製造流程的相關性質有進一步的了解。

首先，對於一閘極氧化層為 1.27 奈米厚之 p 型金氧半場效電晶體，其淺溝槽隔離的製程會對通道內部造成壓縮應力，我們發現，實驗的電洞穿隧電流會隨著此壓縮應力增加而增加。然而，在文獻中，藉由外加應力所導致價電帶的能帶分裂的物理圖像，可以合理的解釋：電洞穿隧電流隨著外加壓縮應力增加而減少，但這和我們的實驗結果卻是相互牴觸。為了解釋這不一致的趨勢，我們把量子模擬器和穿隧電流模型加以整合，並驗證此模擬器之正確性。對於此相反趨勢，藉由模擬結果和實驗結果相互的比較探討，導引出一個物理解釋：淺溝槽隔離不但會造成通道內部的壓縮應力，並同時阻礙氧化的成長，而氧化層厚度隨著應力的改變量，精確至 0.001 奈米，被我們的穿隧電流模型偵測得到。氧化層隨著淺溝槽隔離壓縮應力而變薄，大量增加了穿隧電流，因此反轉了文獻中，電洞穿隧電流隨著外加壓縮應力增加而降低的趨勢。

接下來，我們在一個樣本為 TaC/HfSiON/SiON 高介電金屬閘極之 n 型金氧半場效電晶體量測的閘極漏電流中，發現漏電流中，有一個過渡區域。而其對應的 dlnIg/dVg-Vg 圖形可以顯著的呈現此過渡區域。在此，我們有系統的模擬此區域的穿隧電流及其 dlnIg/dVg-Vg 的特性，我們發現可以因此正確的萃取出一些重要的材料參數，如金屬的功函數，高介電閘極層的電子親和力，還有電子的穿隧等效質量。首先，我們完成了直接和 F-N 穿隧電流的計算，並提出了一個如何模擬和重現實驗值的指導方針。藉由此漏電流模擬的指導方針，相對應的材料參數被正確的萃取出來，甚至在更高的溫度下還有電場下我們的模擬結果仍維持其正確性。我們也提出一個結論，若在做漏電流模擬時，沒有針對其 dlnIg/dVg-Vg 的特性做模擬和匹配，有可能會因此萃取出錯誤的材料參數。因此，dlnIg/dVg-Vg 的特性模擬，對於高介電金屬閘極金氧半場效電晶體的穿隧電流模擬是非常重要的。除此之外，我們發覺，藉由表面缺陷提供的穿隧電流，對於要完整重現實驗漏電流，是必須加入探討的。

此外，其等效氧化層厚度為 0.75 奈米的 TiN/HfO_2/SiON 高介電金屬閘極之 n 型金氧半場效電晶體的閘極漏電流及其 dlnIg/dVg 模擬和匹配在本文中被完整呈現。首先，我們發現無論是 HfO_2 還是 HfSiON 的等效穿隧質量都為 0.03 m_0。0.03 m_0 是目前文獻中最低的等效質量值，而此值和高介電閘極層的材料無關，這些結果指出了一些目前無法解釋的物理現象。在模型中，藉由將一層其介電值、等效穿隧質量、電子穿隧能障都逐步變化的過渡層導入 HfO_2 高介電層和 SiON 介面層之間，實驗值可以完美的被模擬器重現。藉由模擬值和實驗比較的結果，然而我們發現，HfSiON/SiON 之間則沒有此過渡層。最後，電子藉由 IL/Si 介面的缺陷而產生的穿隧電

流，對於整體穿隧電流的重要性在本文中則被突顯出來。

再一次，對於等效氧化層厚度為 1.5 奈米的 TaC/HfSiON/SiON 還有等效氧化層厚度為 0.85 奈米的 TiN/HfO_2/SiON 高介電金屬閘極之 p 型金氧半場效電晶體其量測出的閘極、汲極/源極、基極電流，我們對其做廣泛完整的模擬及重現。整合分別來至於通道反轉層載子和 IL/Si 介面缺陷中載子的穿隧電流，再加上藉由在介面層中的缺陷(可以達到最大穿隧機率)，而造成的缺陷輔助穿隧電流，TiN/HfO_2/SiON p 型金氧半場效電晶體的漏電流可以被完美的重現。然而，缺陷輔助穿隧電流，沒有在 TaC/HfSiON/SiON p 型金氧半場效電晶體的量測電流中被發現。除此之外，在本文中也完成了，模擬電子從金屬端穿隧到基極端所造成的穿隧電流。最後，額外的 dlnIg/dVg-Vg 圖型模擬，其對於正確萃取材料參數的重要性也在本文中被突顯。

最後，一個適用於等效氧化層厚度為 0.8 奈米的高介電金屬閘極鰭式場效電晶體的先進模型被驗證。首先，適用於雙閘極電晶體結構的解析模型被建立。接下來，我們整合並完成 Ig-Vg、Cg-Vg、和 dlnIg/dVg-Vg 實驗圖型的模擬和重現，得到了數個值得注意的結果。首先，只有在模擬器中，高介電層和介面層之間導入了一層過渡層，實驗值才可以被精確的模擬，而穿隧式電子顯微鏡所拍攝的圖片可以支持此論點。第二點，我們萃取出的高介電材質的等效穿隧質量為 0.02 m_0。第三點，鰭式電晶體包含了(001)和(110)的晶面，就算如此，我們藉由重現其穿隧電流所萃取得到的材料參數，和相同製程下在平面式 n 型金氧半場效電晶體所萃取得到的參數是一致的。最後，藉由模擬從表面缺陷穿隧至金屬閘極之穿隧電流，低電壓下的實驗漏電流可以被完美的解釋。

關鍵字：機械應力，淺溝槽隔離，穿隧，壓電阻，元件佈局，金氧半場效電晶體，鉿金屬矽化物，鉿氧化物，高介電係數，金屬閘極，鰭式場效電晶體。

Advanced Modeling of Gate Tunneling Current in CMOSFETs and FinFETs and Its Potential Application

Student: Chih-Yu Hsu Advisor: Dr. Ming-Jer Chen

Department of Electronics Engineering and Institute of Electronics

National Chiao-Tung University

Abstract

Analytic gate direct tunneling and Fowler-Nordheim tunneling current model for conventional polysilicon gate oxide MOSFETs and present-day metal-gate/high-k/IL gate stack CMOSFETs and n-FinFETs is established. In addition, trap related tunneling is incorporated as well. Validity of the model, with the known effective masses and subband energies created using an in-house quantum confinement simulator, is thoroughly corroborated. Particularly, advanced techniques on the application of the model are proposed for the first time. Resulting process and material parameters of the device under study not only can provide new insight into underlying manufacturing process but also can be quantitatively more accurate than those obtained from conventional method without advanced techniques in this work.

At first, on a nominally 1.27-nm thick gate oxide p-MOSFET with STI longitudinal compressive mechanical stress, experimental hole gate tunneling current exhibits an increasing trend with STI compressive stress. However, this is exactly opposed to the currently recognized trend: Hole gate direct tunneling current decreases with externally applied compressive stress, which is due to the strain altered valence-band splitting. To determine the mechanisms responsible, the combination of the model and a quantum strain simulator is established and its validity is confirmed. The simulator then systematically leads us to the finding of the origin: A reduction in the physical gate oxide thickness, with the accuracy identified down to 0.001 nm, occurs under the influence of the STI compressive

stress. The strain-retarded oxide growth rate can significantly enhance hole direct tunneling and thereby reverse the conventional trend due to the strain altered valence-band splitting.

Next, for planar bulk n-MOSFET low-EOT (1.4 nm) TaC/HfSiON/SiON high-κ gate stacks, there is a transition region in the electron gate tunneling current Ig, as characterized by a plot of dlnIg/dVg versus Vg. Here, we systematically construct a new fitting over the region, which can accurately determine the material parameters including the metal workfunction, the high-*k* electron affinity, and the tunneling effective masses of electrons. First of all, a calculation of gate current due to electron direct tunneling and/or Fowler-Nordheim tunneling from the inversion layer is performed, yielding the guidelines of the fitting. The underlying material parameters are extracted accordingly and remain valid for higher temperature and gate voltage. We also demonstrate that the conventional method without the dlnIg/dVg fitting might lead to erroneous results. Thus, dlnIg/dVg fitting is crucial to the metal-gate high-*k* material parameters assessment. In addition to electron tunneling from inversion layer to metal electrode, additional tunneling component via the interface states is shown to be significant in reproducing experimental gate leakage current.

Further, for 0.75-nm EOT TiN/HfO_2/SiON nMOSFETs, experimental gate tunneling current and its dlIg/dVg fittings are presented. First of all, electron tunneling effective mass in HfO_2 dielectric lies at around 0.03 m_o, which is consistent with the HfSiON counterpart. This dictates some unexplained physical mechanisms, which not only are common to both HfO_2 and HfSiON but also are responsible for unconventionally low effective mass in tunneling. Furthermore, a graded transition (intermixing) region from SiON interfacial layer to HfO_2 high-κ can ensure a good fitting. This suggests that a transition layer exists in HfO_2 based high-κ gate stacks whereas it does not exist in HfSiON/SiON gate stacks. The importance of electron tunneling via IL/Si interface states in overall gate leakage is highlighted.

For both 1.5 nm-EOT TaC/HfSiON/SiON and 0.85nm-EOT TiN/HfO_2/SiON gate dielectric p-MOSFET counterparts, a comprehensive fitting of measured tunneling current components through source/drain, bulk, and gate is performed. Combining electron direct and F-N tunneling from both the

inversion layer and IL/Si interface states with the trap-assisted tunneling (TAT) current around the favorable trap (in interfacial layer for the maximum tunneling probability there), the experimental hole tunneling current for TiN/HfO_2/SiON gate dielectric pMOSFETs is reproduced well. However, TAT mechanism does not exist in the experimental gate current data for TaC/HfSiON/SiON gate stacks pMOSFETs. The fittings of the substrate current stemming from gate-to-substrate electron tunneling for both test devices are also conducted. Furthermore, the importance of extra dlnIg/dVg-Vg fitting to ensure accurate assessment of gate material parameters is highlighted as well.

At this point, we will demonstrate advanced modeling in 0.8-nm EOT HfO_2 based high-κ/metal-gate n-FinFETs. First of all, an analytic model suitable for double-gate structure is newly constructed. Then, the combination of Ig-Vg, Cg-Vg, and additional dlnIg/dVg-Vg curve fittings leads to several remarkable results. First, only with a transition layer between high-κ and interfacial layer can a good fitting be obtained, as supported by TEM analysis. Second, the tunneling effective mass in HfO_2 based high-κ dielectric is around 0.02 m_0, a minimum value reported to date. Third, all extracted gate material parameters remain valid, taking into account the difference between (001) and (110) surfaces, for the planar bulk n-MOSFET counterparts formed on the same wafer. Finally, the experimental electron tunneling current at low gate bias can be fitted well by adding the role of tunneling from IL/Si interface states to metal gate.

Keyword: Mechanical stress, shallow trench isolation, tunneling, piezoresistance, layout, MOSFET, HfSiON, HfO_2, high-κ, metal gate, FinFET.

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List of Symbols

Cg	Gate capacitance
Ig	Gate leakage current
Id	Drain leakage current
Ib	Substrate leakage
EOT	Effective oxide thickness
IL	Interfacial layer
N_{sub}	Substrate doping concentration
N_{poly}	Poly gate doping concentration
N(j,i)	Hole density per unit area of the *j*-th subband in the *i*-th valence band
$N_{interface}$	Interface trap density
N_t	Trap density
Q_{depl}	Depletion charge density
t_{ox}	Physical oxide thickness
t_{IL}	Physical IL thickness
t_k	Physical high-κ layer thickness
t_{mix}	Physical thickness of transition layer
t_{body}	Distance between two controlled gate stacks
t_{stack}	Physical thickness of gate stacks (t_k+t_{IL})
x_t	Trap distance apart from IL/Si interface
x_{t_fav}	Specific favorable trap position can contribute maximum TAT current
t_{eff}	Effective thickness that the trap-assisted current flow mainly
W	Channel width
W_{mask}	Mask gate width
L	Channel length
Fin Height	Fin sidewall height of a FinFET
a	gate to STI spacing
$V_{thermal}$	Thermal velocity (10^7 cm/s at room temperature)
σ	Channel stress
σ_c	Trap cross section area
E(j,i)	Energy of the *j*-th subband in the *i*-th valence band
E_{Vi}	Energy of the *i*-th valence band
E_F	Fermi level
F_s	Silicon surface electric field strength
F_k	Electric field in high-κ layer
F_{IL}	Electric field in IL
F	Fermi-Dirac distribution function

m_{zhi}	Hole out-of-plane effective mass associated with the *i*-th valence band
m_{dhi}	2-D DOS (density of states) effective mass of the *i*-th valence band
m_{ox}*	Hole effective mass in oxide
m_k*	Tunneling effective mass in high-κ layer
m_{IL}*	Tunneling effective mass in IL
$m^*_{k\_h}$	Hole tunneling effective mass in high-κ layer
$m^*_{IL\_h}$	Hole tunneling effective mass in IL
m^*_M	Effective mass in metal (1 m_0)
f	Impact frequency on the Si/SiO_2(IL) interface
$P_t(E(j,i))$	Hole transmission probability across the SiO_2 film
T_{WKB}	Transmission probability across the high-κ film
T_R	Reflection correction factor
J	Electron/hole direct/F-N tunneling current
$J_{interface}$	Tunneling current from IL/Si interface states
J_{TAT}	Trap-assisted-tunneling current
J_{MGe}	Metal gate-to-substrate electron tunneling current
Φ_m	Metal workfunction
φ_k	Band offset of high-κ layer with respect to silicon conduction band
φ_{IL}	Band offset of IL with respect to silicon conduction band
φ_{k_h}	Valence band offset of high-κ layer to silicon valence band
φ_{IL_h}	Valence band offset of IL to silicon valence band
φ_{k_e}	Conduction band offset of high-κ layer to silicon conduction band
φ_{IL_e}	Conduction band offset of IL to silicon conduction band
φ_{k_m}	$(\varphi_{k\_e} + (\Phi_m - \chi_s))$
φ_{IL_m}	$(\varphi_{IL\_e} + (\Phi_m - \chi_s))$
φ_t	Trap energy with respect to the valence band of high-κ layer or IL
$\varphi_{depl}(Vg)$	Potential band bending across depletion region versus gate voltage bias
Window	A local region, sited in the forbidden band gap with respect to conduction (valence) band edge, allowing electrons (holes) to populate
$Window_{empty}$	A region in IL/Si interface allows electron tunneling from metal-gate to occupy
ε_{si}	Silicon permittivity
ε_{ox}	Permittivity of SiO_2
ε_k	Permittivity of high-κ layer
ε_{IL}	Permittivity of IL
$\varepsilon_{mix}(n)$	Permittivity of *n*-th abrupt barrier
χ_k	Electron affinity of high-*k* layer
χ_{IL}	Electron affinity of IL
k_B	Boltzmann's constant

Chapter 1

Introduction

1.1 Background

Aggressive scaling of complementary metal-oxide-semiconductor field-effect transistors (CMOSFETs) continues for the purpose of reducing average cost per transistor, boosting device performance, and enhancing chip's functionality with higher transistor density. Scaling of CMOSFETs is usually accompanied with equivalent oxide thickness (EOT) reduction for maintaining the gate control over the channel. However, the downward scaling of EOT directly increases the power consumption of the device because the leakage current increases significantly with decreasing physical thickness of gate dielectric. Advanced technologies are developed to overcome the leakage problem while keeping constant transistor performance improved. One of the crucial technologies is high-κ materials that are adopted in gate dielectric manufacturing [1.1],[1.2] with aim to reduce gate leakage. Due to thicker physical thickness of high-κ layer with the same EOT manufactured from conventional SiO_2 dielectric, the leakage problem was mitigated. Furthermore, a tri-gate structure (FinFET) has attracted much attention in recent years [1.3]-[1.16]. Utilizing the strong gate control ability of tri-gate structure, the pressure on EOT scaling can be considerably released. Hence, the low gate leakage level can ~~be~~ hold as the scaling continues for FinFET structure.

Strain technologies are also extensively used to boost the transistor performance [1.17]-[1.20]. Due to serious power consumption issue originating from significant tunneling current in modern-day device, direct tunneling current across the gate oxide of MOSFETs has been extensively studied in the presence of an *external*

mechanical stress applied during the measurement of this current [1.21]-[1.23]. Those studies attributed the external stress induced gate leakage change to both change of the carrier repopulation and the effective SiO_2/Si barrier height due to strain induced band splitting. However, process-induced stress may affect some process parameters rather than simply the strain altered valence-band splitting. For example, the study has proven that oxidation rate can be affected by stressing [1.24]. The effects of process-induced variation on direct tunneling current have not been fully addressed. Hence, it remains unclear whether the trend of the hole direct tunneling with the external stress, as claimed in the literature [1.21],[1.22], could hold for the process induced case. In this work, the test samples are designed with different dimensions of gate edge to STI edge spacing in order to alter level of stress in channel. We find that the experimental hole gate direct tunneling current of p-MOSFETs versus STI (shallow trench isolation) induced longitudinal compressive stress, which does not appear to follow the trend [1.21],[1.22], is caused by the strain altered valence-band splitting alone. The physical explanation of the deviation between process- and external induced hole direct tunneling current change is systematically drawn. Furthermore, we find that direct tunneling current modeling can serve as a sensitive detector of process parameters.

The dimensions of CMOS continue to shrink such as to meet the requirements of Moore's law that the number of transistors in a chip counts double every two years. To keep the device performance improvement, the scaling procedure is not only to shorten the gate length but also scale the thickness of gate dielectric and depletion region in gate and substrate. One of most troublesome issues in scaling path is the unacceptable power consumption due to significant tunneling current effect as the oxide/oxynitride thickness is reduced down to around one nanometer. To solve this power consumption issue, high-κ materials were adopted in gate dielectric

manufacturing [1.1],[1.2]. Comparing SiO_2 gate dielectric counterpart, the high-κ can achieve the same EOT but with thicker physical thickness of gate dielectric. Therefore, the leakage current can be effectively reduced in MOSFETs with high-κ gate dielectric. In addition, high-κ gate dielectric is usually integrated with metal gate in order to eliminate the poly depletion to get lower capacitance equivalent thickness (CET). Hence, metal-gate/high-κ gate stacks system has replaced poly-gate SiO_2 gate dielectric system in advanced VLSI technologies. High-κ gate stacks usually include an ultra-thin interfacial layer (IL) for high quality Si-SiO_2 interface beneath the high-κ material. Accurate modeling and characterization of the tunneling current through high-κ stacks is crucial to understanding the limitation in power consumption of the devices with high-κ metal-gate. Many studies [1.25]-[1.33] have been dedicated to modeling direct tunneling through high-κ gate stacks of MOSFETs. However, these works, which neglected the transition of direct tunneling and Fowler-Nordheim (F-N) tunneling across high-κ layer [1.34], may lead to wrong fitting parameters. Because the band offset of high-κ materials to silicon is usually smaller than that of SiO_2 [1.35], the transition between direct tunneling and F-N tunneling is potentially important in the modeling of tunneling current through high-κ gate stacks. In this work, combining the gate tunneling current fitting with its dlnI/dVg fitting, the gate tunneling current fitting guideline for accurately extracting the parameters of high-κ layer is created. The validity of this new proposed gate tunneling fitting guideline has been proven throughout this work, along with TaC/HfSiON/SiON and TiN/HfO_2/SiON gate stacks n (p)-MOSFETs and metal-gate/HfO_2 based high-κ layer/IL n-FinFET serving as test samples. Furthermore, the gate leakage current modeling at low gate bias is still a challenge work. Hence, we propose a model for simulating electron tunneling from IL/Si interface states in forbidden band gap of Si to metal gate, with aim to explain the

physical meaning of gate current at low gate bias. The validity of this extra modeling is verified experimentally throughout this work.

Following the fitting guideline established by electron tunneling current fitting of n-MOSFET with high-κ gate stacks [1.36], good reproduction of hole tunneling current is achieved and the corresponding material parameters are accurately extracted. However, based on our measured tunneling current data, we find that gate-to-substrate electron tunneling current (Ib) dominates overall gate leakage current at particular range of gate bias. This phenomenon is caused by the fact that tunneling barrier height seen by holes at inversion layer is higher than that seen by electrons in metal gate. Although Ib is getting importance for metal-gate high-κ p-MOSFETs at inversion condition, its fitting work is still lacking. In this work, the hole tunneling current from both inversion layer and IL/Si interface states and gate-to-substrate electron tunneling at inversion condition in metal-gate high-κ p-MOSFETs are excellently modeled.

As the scaling of CMOSFETs continues, maintaining the ability of gate control over channel is challenging. Short channel effect (SCE) and DIBL are serious issues in nano-scaled conventional planar devices. Under the circumstances, a transistor with 3-D multi-gate structure (FinFET) was developed [1.3]-[1.16]. The FinFET transistors have superior capability in gate control over planar transistors as the gate length becomes shorter and shorter [1.3],[1.7],[1.9]-[1.10]. Excellent short channel effect control was proven for gate length of less than 25 nm [1.9]-[1.10]. Owing to the strong ability of gate control, strict demand of EOT scaling is mitigated in FinFETs. In other words, the power consumption (due to gate tunneling leakage) issue in FinFET devices gets better control than that in planar ones. Although the FinFET structures were widely discussed in the open literature, the fitting work of gate tunneling leakage current in FinFET devices was rarely addressed [1.37]. In this

work, with an analytical model for double-gate structure, reproduction of experimental gate tunneling current in metal-gate high-κ gate stacks nFinFET is achieved. The already established gate tunneling current fitting guideline for planar devices [1.36] has been successfully applied in fitting experimental gate tunneling current in metal-gate high-κ gate stacks FinFETs, leading to underlying process parameters.

1.2 Organization of this Dissertation

Introduction is given in Chapter 1. In Chapter 2, a strain quantum simulator is established. To control the process-induced channel stress, different gate edge to STI edge spacings are designed. Hole tunneling currents versus Vg for different STI-induced channel stresses are measured. Then, the physical origin of experimental hole current change due to process-induced stress is determined in terms of ultra-small oxide thickness change with internal stress.

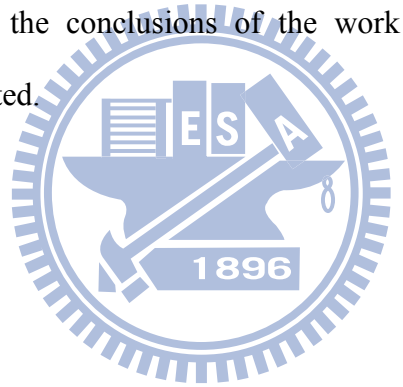
Chapter 3 and 4 clearly describe direct and F-N tunneling models for metal-gate high-κ nMOSFETs. Reproduction of experimental tunneling current measured from TaC/HfSiON/SiON and TiN/HfO_2/SiON gate stacks n-MOSFETs is achieved. A new advanced fitting approach by combining conventional Ig-Vg and Cg-Vg curve fittings with its dlnIg/dVg fitting is established. The ability and validity of this new gate tunneling approach are shown. Then, the fitting guideline of gate tunneling current for metal-gate high-κ nMOSFETs is established as well. Furthermore, the physical origin of experimental gate leakage at low gate bias is captured accordingly.

In Chapter 5, the theory and model of hole direct tunneling current for metal-gate high-κ pMOSFETs are presented. TaC/HfSiON/SiON and TiN/HfO_2/SiON gate stacks pMOSFETs serve as test devices. Owing to the dominance of the gate-to-substrate tunneling current in overall gate current leakage, the model used for

calculating metal-to-substrate electron tunneling current at inversion condition is constructed and discussed. Direct and F-N tunneling currents originating from hole inversion layer and IL/Si interface states are combined with TAT current component to explain experimental result.

Chapter 6 focuses on fitting gate tunneling current of FinFET transistors with metal-gate high-κ stacks. A simple simulator for double-gate structure is established and used to reproduce the tunneling current components through gate dielectric of FinFET. The validity of the simulator in combination of analytical tunneling model is confirmed for different fin widths. Good reproduction of electron gate leakage current versus Vg curve in a wide range of six decades is obtained.

Finally, in Chapter 7, the conclusions of the work are given and the major contributions are highlighted.



Chapter 2

Enhanced Hole Gate Tunneling Current in Process-Induced Uniaxial Compressive Strained p-MOSFETs

2.1 Introduction

Hole direct tunneling current across the gate oxide of p-MOSFETs has been extensively studied in the presence of an *external* mechanical stress applied during the measurement of this current [2.1]-[2.3]. The corresponding gate oxide thickness change due to the effect of Poisson's ratio has been shown to be negligible in magnitude; for example, in the citation [2.1], around 0.03 % change in the gate oxide thickness has been estimated for an external stress of 300 MPa. Therefore, the physical gate oxide thickness essentially remains unchanged, regardless of the externally applied stress. Under the circumstances, the induced gate current variation can be properly attributed, through the change in both the carrier repopulation and the effective SiO_2/Si barrier height, to the strain induced valence-band splitting. It has been therefore argued that the hole gate direct tunneling current decreases with the external compressive stress [2.1],[2.2]. On the other hand, for the case of p-MOSFETs undergoing a *process*-induced (*internally* applied), mobility-boosting mechanical stress during the manufacturing of the device, hole gate direct tunneling current may encounter complicated situations (gate oxide thickness change due to strain dependence of the oxidation rate, for example), rather than simply the strain altered valence-band splitting. So far, it has been unclear whether the decreasing trend of the hole direct tunneling with the compressive stress, as claimed in the literature [2.1],[2.2], could hold for the internal case. Thus, the ability to distinguish the external stress effect from the internal one and/or find the similarities between the two is

crucial.

In this work, we will elaborate on the above subject. First of all, we will present the experimental hole gate direct tunneling current of p-MOSFETs under STI (shallow trench isolation) induced longitudinal compressive stress, which does not appear to follow the trend [2.1],[2.2] caused by the strain altered valence-band splitting alone. A quantum strain simulator will be developed to resolve this contradictory issue. The validity of the simulator will be examined in detail. Then, the quantum simulator will be combined, in a systematic manner, with the experimental data in order to determine the underlying physical origin.

2.2 Experimental

P-channel MOSFETs as schematically shown in Fig. 2.1 were fabricated using a state-of-the-art manufacturing process. In this process, the STI induced compressive stress was applied prior to the growth of the gate oxide and the source/drain implantation. The nominal process parameters were obtained by the capacitance-voltage fitting: p^+ polysilicon doping concentration $N_{poly} = 1 \times 10^{20}$ cm^{-3}, physical gate oxide thickness $t_{ox} = 1.27$ nm, and n-type substrate doping concentration $N_{sub} = 6 \times 10^{17}$ cm^{-3}. The gate width to length ratio was fixed at $W/L = 10$ μm /1 μm. The devices were formed on (001) wafer with the channel length direction along <110>. The use of the wide structures ensures that the transverse channel stress can be reasonably ignored. To control the longitudinal channel stress, the gate to STI spacing as labeled a in Fig. 2.1 was drawn with three values of 10.0, 0.495, and 0.21 μm. The corresponding stress magnitude can be determined via the piezoresistance coefficients. First of all, the peak hole mobility at $V_D = -0.025$ V was measured across the wafer. The relative change of the average peak hole mobility was then obtained with respect to that of $a = 10$ μm, as plotted in Fig. 2.2 versus stress. Here, the state-of-the-art

inversion-layer piezoresistance coefficient for holes, as quoted elsewhere [2.2], was employed as demonstrated by a straight line in the figure. The corresponding longitudinal channel stress σ is therefore determined to be around -120 and -215 MPa for a = 0.495 and 0.21 μm, respectively. To testify to the validity of the extracted stresses, one empirical formula, which connects the layout parameters to the stress quantities, was also cited elsewhere [2.4]: $\sigma(a) = \sigma(a_{min})\ (1+V_{m\sigma}(a-a_{min})/a)$, where $a_{\min}$ is the minimum gate-to-STI spacing and $V_{m\sigma}$ is the maximum variation for a $\to\infty$ with respect to $\sigma(a_{min})$. Excellent fitting was achieved with $V_{m\sigma}$ = -1.02, as shown in the inset of Fig. 2.2.

To examine the poly stress, the threshold voltage was also measured across the wafer with the results in Fig. 2.3 in terms of the average and standard deviation of the distribution. The threshold voltage variation appears to be a weak function of the gate-to-STI spacing and its trend looks irregular, prohibiting the poly stress from being determined. However, in our previous work [2.9], the electron direct tunneling data confirm the existence of a lateral STI induced stress in the polysilicon, and since the gate oxide is rather thin, the lateral stress near the polysilicon surface is reasonably close to that of the underlying silicon. The same wafer was used in this study and thereby the poly stress was made equal to the channel stress. Extra evidence will be given later.

The hole gate direct tunneling current was measured in inversion with the source, drain, and substrate tied to the ground. Strikingly, the gate current versus gate voltage characteristics measured across the whole wafer do not appear to deviate from each other. This situation is displayed in Fig. 2.4 for several samples with different a values and different device positions. Obviously, it is difficult to distinguish the measured *I-V* characteristics in a wide current range. This argument remains valid, regardless of

the device position on wafer or the value of a used. To produce a clear difference, the average and standard deviation of the gate current distribution at a specific gate voltage, V_G = -1 V, was adopted, as inserted into Fig. 2.4. The inset of the figure clearly reveals an increasing trend of the average hole gate direct tunneling current with the compressive stress (decreasing a), exactly contrary to that published in the literature [2.1],[2.2]. The role played by the standard deviation of the gate current will be described later. Additionally, the relative change of the average gate current with respect to that of a = 10 μm was found to be a weak function of the gate voltage, as shown in Fig. 2.5 for σ = -215 MPa. This specific characteristic over the gate voltage can serve as the corroborating evidence while determining the underlying physical mechanisms, as will be explained later.

2.3 Quantum Strain Simulation

To resolve the above contradicting issue, a quantum strain simulator was developed around the hole direct tunneling process as schematically described in Fig. 2.6 in terms of the energy band diagram. First of all, with the combination of the six-band $k \bullet p$ Hamiltonian and a triangular-well approximation as detailed elsewhere [2.5], the strain-induced valence-band edge shift can be calculated under a certain surface electric field:

$$E(j,i) = \left(\frac{\hbar^2}{2m_{zhi}}\right)^{1/3} \left(\frac{3\pi q F_s \left(j - \frac{1}{4}\right)}{2}\right)^{2/3} + q(E_{V1} - E_{Vi}) \qquad (2.1)$$

where $E(j,i)$ represents the energy of the j-th subband in the i-th valence band; i = 1, 2, and 3 correspond to the first, second, and third valence band, respectively; m_{zhi} is the hole out-of-plane effective mass associated with the i-th valence band; F_s is the silicon surface electric field strength; E_{Vi} is the energy of the i-th valence band; and q is the elemental charge. The calculated energy levels at V_G = -1 V for the top (first), second,

and split-off (third) hole subbands are shown in Fig. 2.7 versus stress. Here it can be seen that the top subband is insensitive to the stress while for the remaining subbands, the energy levels rise up thereby reducing the corresponding SiO_2/Si barrier height seen by the holes while tunneling across the oxide. The involved hole out-of-plane effective masses in the inversion layer were found to be fairly constant: $m_{zh1} = 0.27\ m_0$, $m_{zh2} = 0.22\ m_0$, and $m_{zh3} = 0.23\ m_0$, the same values as those of the citation [2.1].

Then, the carrier repopulation under stress can be calculated accordingly:

$$N(j,i) = (\frac{m_{dhi} k_B T}{\pi \hbar^2}) \ln(1 + \exp(\frac{E_F - E(j,i)}{k_B T})) \tag{2.2}$$

where $N(j,i)$ represents the hole density per unit area of the j-th subband in the i-th valence band; m_{dhi} is the 2-D DOS (density of states) effective mass of the i-th valence band; E_F is the hole Fermi level; k_B is Boltzmann's constant; and T is the absolute temperature. Finally, the triangular potential based hole direct tunneling model in our previous work [2.6] can be applied, in which the hole direct tunneling current per unit area reads as:

$$J_h = \sum_i \sum_j q f(j,i) N(j,i) P_t(E(j,i)) \tag{2.3}$$

where $f(j,i)$ is the hole impact frequency on the Si/SiO_2 interface and equals to $(qF_s/2)(2m_{zhi}E(j,i))^{-1/2}$; where ε_{si} is the silicon permittivity; and $P_t(E(j,i))$ is the hole transmission probability across the SiO_2 film. The hole effective mass in oxide, m_{ox}^*, can play a critical role in determining the transmission probability $P_t(E(j,i))$.

Therefore, by incorporating both the conduction-band deformation potential (see Ref. [2.7] for the complete formulas, which were also cited in our previous work dedicated to the electron direct tunneling [2.8],[2.9]) and the valence-band $k \cdot p$ calculation results into the triangular potential based hole direct tunneling simulator [2.6], the strain altered hole gate current is able to be readily quantified. The validity of the presented quantum strain simulator can be examined by three different aspects.

First, fairly good agreement with the measured gate current versus gate voltage characteristics was created in a wide range of four decades, as demonstrated in Fig. 2.3 for σ = 0. This means that the simulator is reliable for the gate voltage more negative than -0.2 V. The same argument holds for the nonzero stress. Secondly, the hole effective mass in the oxide, m_{ox}^{*}, is exactly equal to the literature value (0.32 m_o) [2.10]. This also is the case for the hole out-of-plane effective masses in the inversion layer as mentioned above. Finally, with the fixed gate oxide thickness, the simulated hole gate direct tunneling current change at V_G = -1 V due to the strain altered valence-band splitting was found to be close to those measured under the *externally* applied compressive stress [2.1],[2.2], as depicted in Fig. 2.8. Therefore, the validity of the quantum strain simulator is confirmed.

2.4 Physical Origin and Discussion

To find out the plausible physical mechanisms that account for the hole gate current enhancement, we employed the above verified quantum strain simulator through the changes in the process parameters. First, with polysilicon doping concentration N_{poly} and substrate doping concentration N_{sub} both fixed at their nominal values, the simulated gate current change percentage is given in Fig. 2.9(a) versus gate voltage with the gate oxide thickness t_{ox} as a parameter. The corresponding fractional gate current change, remains constant in a wide range of the gate voltage, regardless of t_{ox}. This means that the same flat characteristics as those experimentally encountered over the gate voltage can be reached as long as the appropriate gate oxide thickness has been determined. Secondly, to reflect the stress effect on impurity diffusion [2.9],[2.11]-[2.13], additional simulations were conducted for varying N_{poly} and N_{sub}. The results are given in Fig. 2.9(b) and 2.9(c). The gate current change

presented in Fig. 2.9(b) corresponds to two different values of N_{poly} under fixed t_{ox} and N_{sub}, clearly revealing a profoundly significant deviation for more negatively biased gate voltages. Such a huge deviation also appears in Fig. 2.9(c) for two different values of N_{sub} under fixed t_{ox} and $N_{poly,}$ which occurs instead in the direction of less negative gate voltage. Therefore, the stress induced dopant redistribution is unlikely to serve as the responsible mechanism. Furthermore, the remaining possible factors were considerably ruled out: (i) the channel area change due to source/drain extension diffusion retardation [2.9],[2.13] is insignificant (~10^{-3}); and (ii) the trap assisted tunneling as the dominant mechanism is impossible because of less correlation with the mobility data in Fig. 2.2; specifically, the mobility change at -215 MPa stress is about three times the gate current change.

The above analyses suggest the reduction in the physical gate oxide thickness over the whole gate area, as the principal factor in producing the gate current enhancement. Thus, the quantum strain simulation was further carried out for different gate oxide thicknesses with other process parameters kept unchanged. The results are plotted in Fig. 2.10 versus stress along with the data for comparison. The underlying gate oxide thickness can be straightforwardly obtained with an accuracy of 0.001 nm: t_{ox} = 1.267 and 1.264 nm for -120 and -215 MPa stress, respectively. The extracted gate oxide thickness reduction is around 0.003 and 0.006 nm for -120 and -215 MPa stress, respectively. Again, the gate current change for t_{ox} = 1.264 nm and σ = -215 MPa was simulated with respect to the nominal case (t_{ox} = 1.27 nm and σ = 0 MPa). The results are given in Fig. 2.5. Here it can be seen that good agreements with the data are created for a wide range of gate voltage down to -0.2 V, achieved without adjusting any parameters.

At this point, it is interesting to make a comparison with the existing thermal oxidation experiment on a bending silicon wafer [2.14],[2.15]. In one of the citations

[2.14], an externally applied mechanical stress of -100 MPa was shown to have no noticeable effect on the thickness of the formed oxide (800 ^{o}C dry O_2 100% oxidation), especially in a certain range down to 2 nm thick which is comparable with the gate oxide thickness used in this work. In the second citation [2.15], the effect of the external compressive mechanical stress was also shown to be insignificant as well, valid with an accuracy of 0.5 nm. However, with the combination of both the quantum strain simulator and the hole direct tunneling data as done in this work, we reached the gate oxide thickness with the greatly improved precision down to 0.001 nm. Indeed, it is difficult for current capacitance measurements to deliver such a precision of 0.001nm or 0.08% in gate oxide thickness variation. However, direct tunneling current itself is highly sensitive to the change in the gate oxide thickness. This means that the gate direct tunneling current may serve as an ultra-precision detector of the oxide thickness. However, care must be taken in this direction. This explains the importance of a quantum simulator as demonstrated in this work.

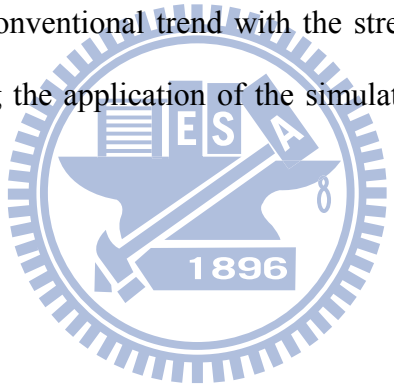
Additionally, the inset of Fig. 2.4 clearly points out that the standard deviation of the gate current is comparable between different gate-to-STI spacing values. This dictates that the spatial fluctuation in the gate oxide thickness is caused by the random process during the thermal oxidation, regardless of the stress. Only the average of the gate current steadily increases with the stress. This means that applying a compressive stress may retard the oxidation rate and thus give rise to a reduction in the physical gate oxide thickness. On the other hand, the presented change of up to 0.47 % in the gate oxide thickness is larger than that (0.03 %) caused by the Poisson's ratio [2.1]. This means that the strain-retarded gate oxidation rate may dominate over the strain altered valence-band splitting counterpart. As a result, the currently recognized trend [2.1],[2.2] that the hole gate direct tunneling current decreases with the compressive stress is significantly reversed, as clearly demonstrated in this work.

Finally, the simulator was again carried out to examine the effect of the poly stress. The resulting gate current change of zero poly stress with respect to poly stress of -215 MPa is plotted in Fig. 2.11 as a function of gate voltage for channel stress of -215 MPa. It can be seen from the figure that significant discrepancies exist, especially for less negative gate voltage. Thus, this deviation, as well as its striking trend, can provide the extra evidence to support the aforementioned hypothesis that the poly stress is close to the channel stress. On the other hand, modeling the gate current through a metal-gate/high-k/interfacial SiO_2/p-type inversion layer/n-type silicon system remains to be a challenging issue. It is expected for the presented simulator to find applications in this metal-gate high-k gate stack case. To achieve the goal, some suggestions are given. First of all, the subband energy calculation by the triangular potential approximation in the presence of the stress can be directly applied in the p-type inversion layer. The corresponding energy band diagram in Fig. 2.6 can be retained but with the poly side removed. The remaining energy band part corresponding to the metal gate and high-k dielectrics may be roughly constructed from the electrostatics aspects in terms of the capacitance, the inversion charge density, and the threshold voltage. Refining of the overall band diagram may be achieved through the fitting of the gate current. At this point, the tunneling model used in this work must be modified substantially. Specifically, the trap-related tunneling might dominate the overall gate current in metal gate/high-k devices due to the thicker insulator and the higher trap density within the insulator of the metal gate/high-k devices. Multilayer tunneling and/or hopping mechanisms may be significant as well.

2.5 Conclusion

The measured hole gate direct tunneling current on a nominal 1.27-nm gate

oxide p-MOSFET has exhibited an increasing trend with STI compressive stress, exactly contrary to that of the externally applied compressive stress. To resolve this contradicting issue, a quantum strain simulator has been established. The validity of the simulator has been examined in detail. The combination of the verified simulator and the experimental data has systematically led to the finding of the origin: A reduction in the apparent physical gate oxide thickness over the whole gate area, with an accuracy of 0.001 nm, occurs under the influence of the STI compressive stress. A linkage to the mechanical stress dependent thermal oxidation experiment in the open literature has been constructed. The extracted gate oxide reduction in this work has been shown to be able to significantly enhance the hole direct tunneling current and consequently reverse the conventional trend with the stress. Some suggestions have also been given concerning the application of the simulator in the metal-gate/high-k devices.



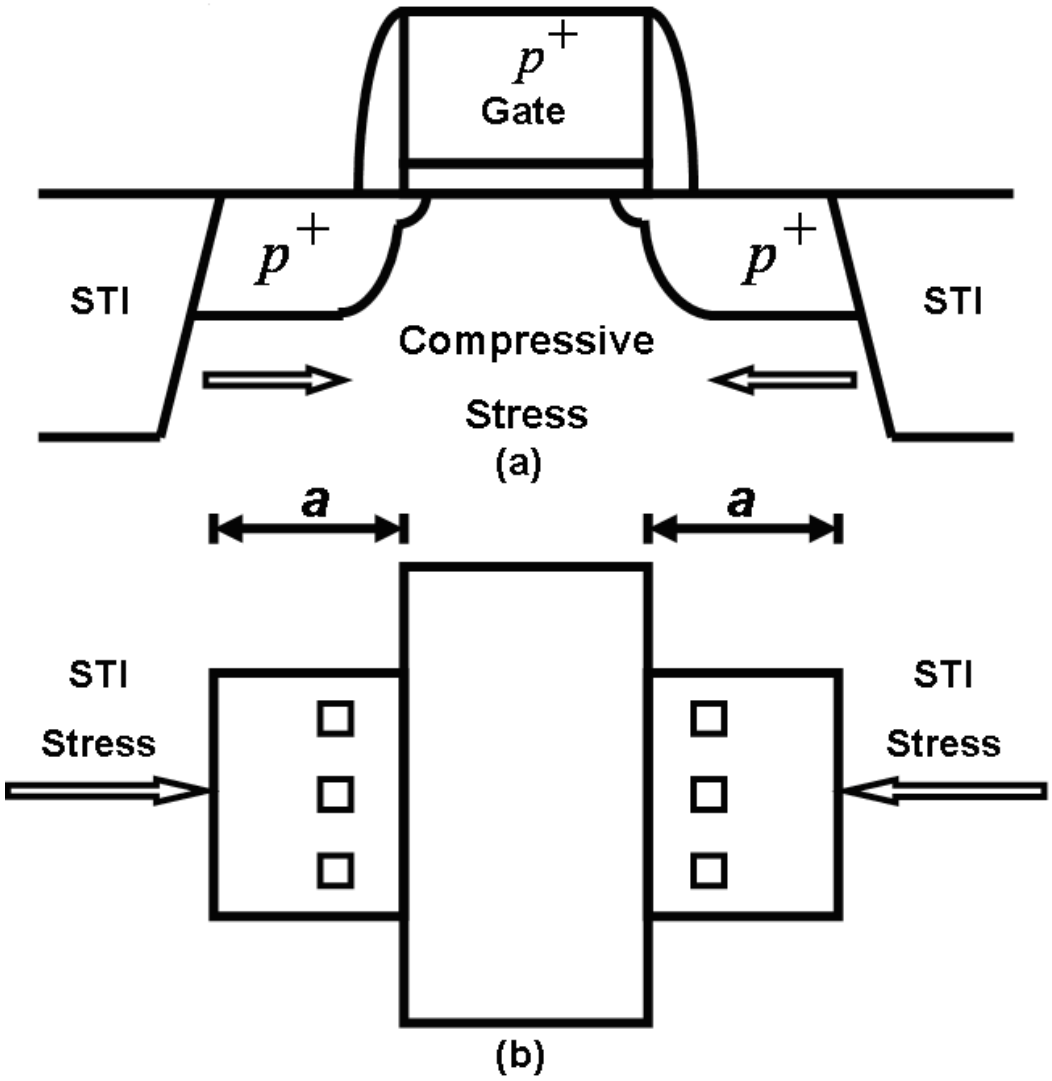


Fig. 2.1(a) Schematic demonstration of the cross-sectional view of the test device.
Fig. 2.1(b) Schematic demonstration of topside view of the test device. The gate edge to STI edge spacing as labeled *a* is highlighted. The compressive stress is due to the lower thermal expansion rate of STI oxide compared to silicon.

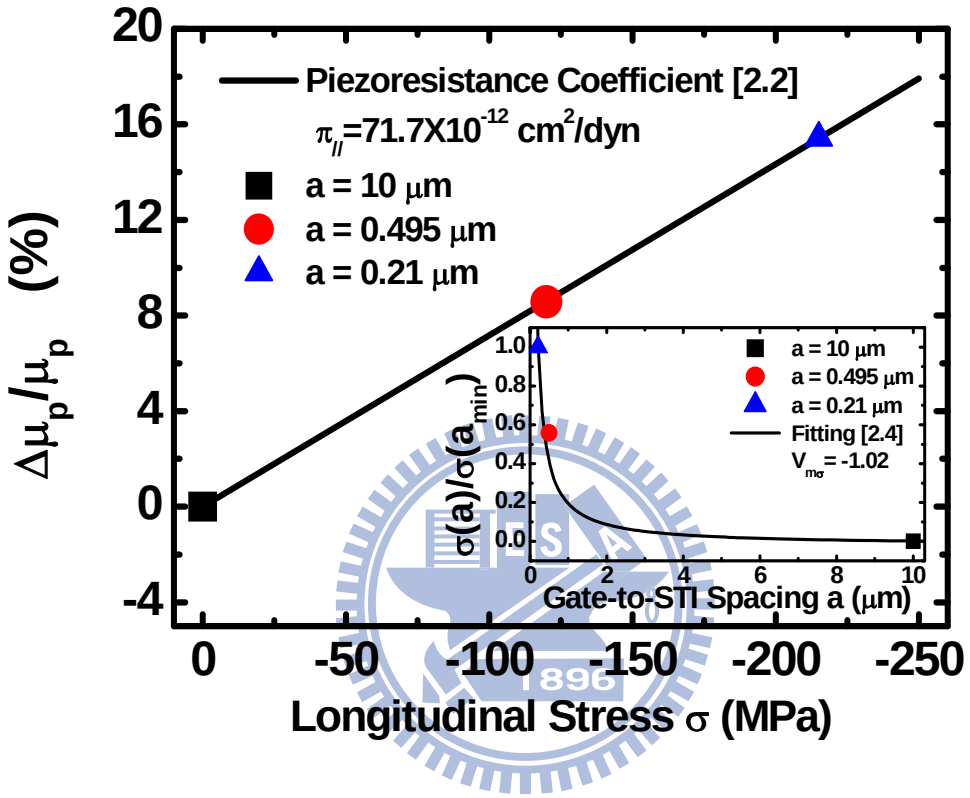


Fig. 2.2 Measured (symbols) and calculated (line) hole mobility change versus STI stress. The straight line is from the piezoresistance coefficient [2.2]. The inset shows the extracted stress divided by that of the minimum *a* as a function of *a*, along with a fitting curve as cited in Ref. [2.4].

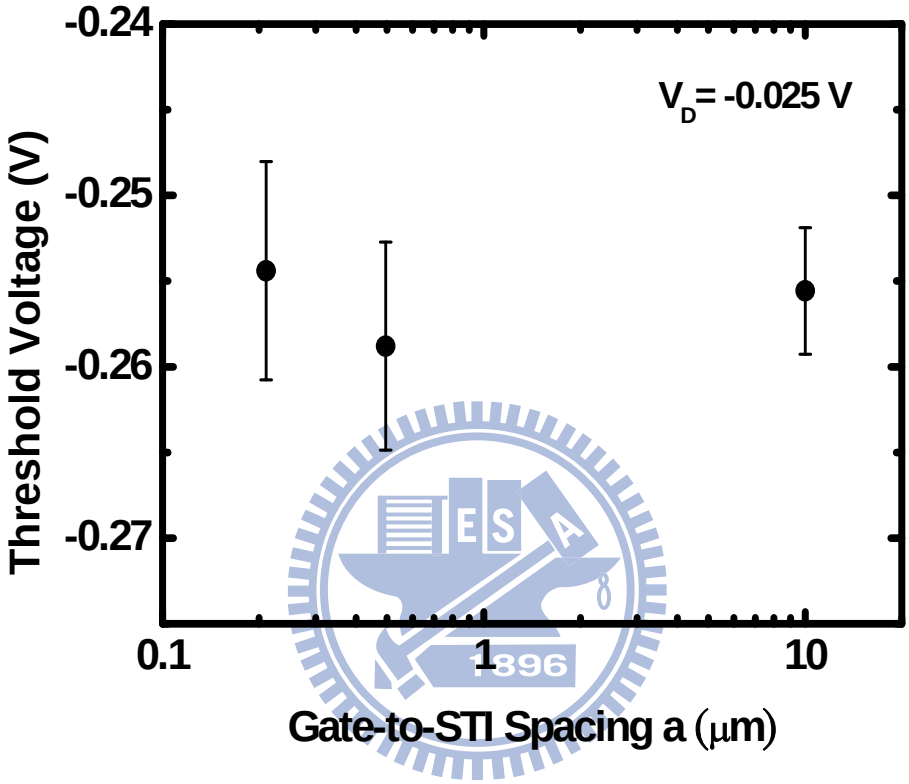


Fig. 2.3 Measured threshold voltage versus gate-to-STI spacing at V_D = -0.025 V. The error bar represents the standard deviation of the distribution and the data point (symbol) represents the average of the distribution.

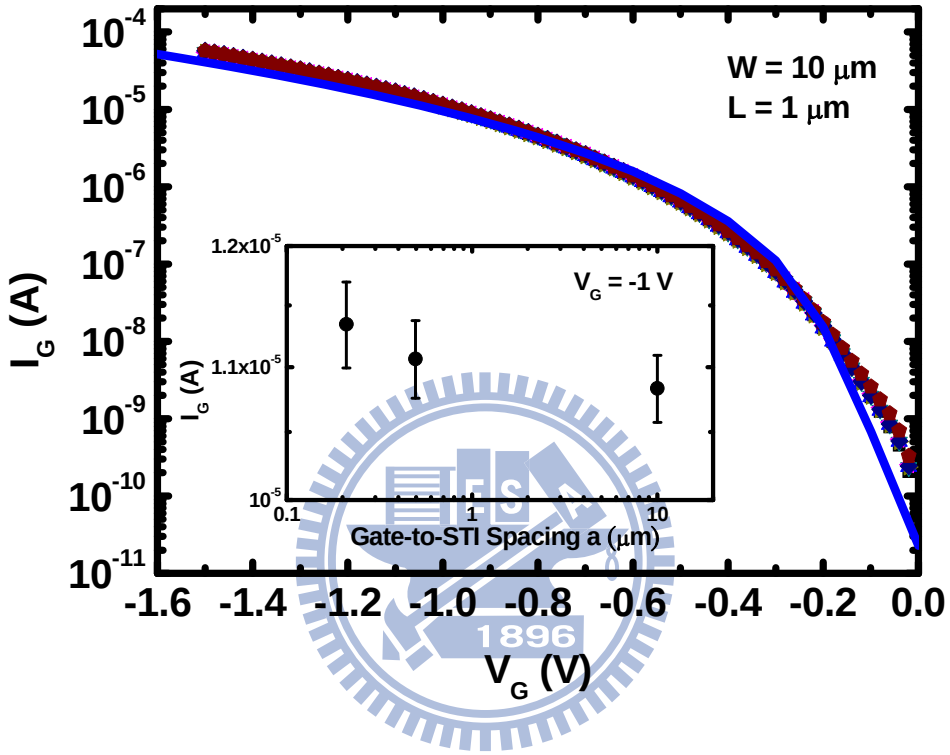


Fig. 2.4 Comparison of simulated (line) gate current versus gate voltage with those (symbols) measured from eight samples. The different symbols stand for the different device positions on wafer and the different gate-to-STI spacing values. The line represents the no-stress simulation result with the nominal process parameters. The source, drain, and substrate are all tied to the ground. The inset shows the distribution of the measured gate current at V_G = -1 V versus gate-to-STI spacing. The error bar represents the standard deviation of the distribution and the data point represents the average of the distribution.

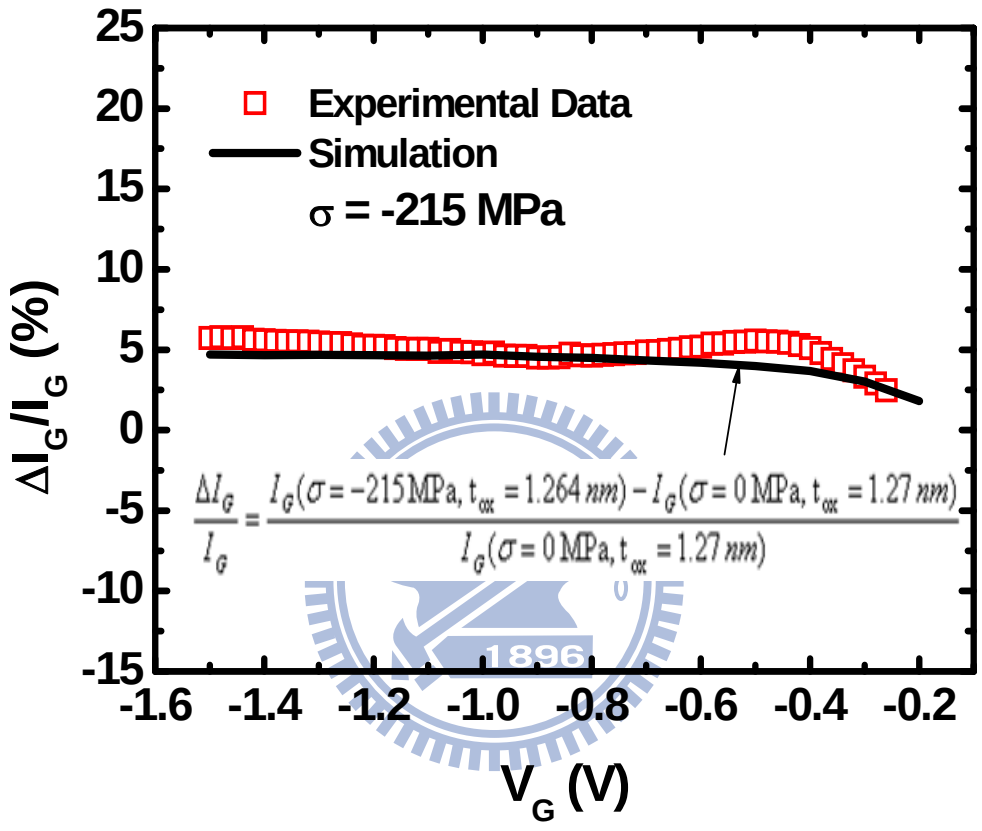


Fig. 2.5 Experimental and simulated gate current change versus gate voltage under -215 MPa longitudinal stress. The formulas used are inserted.

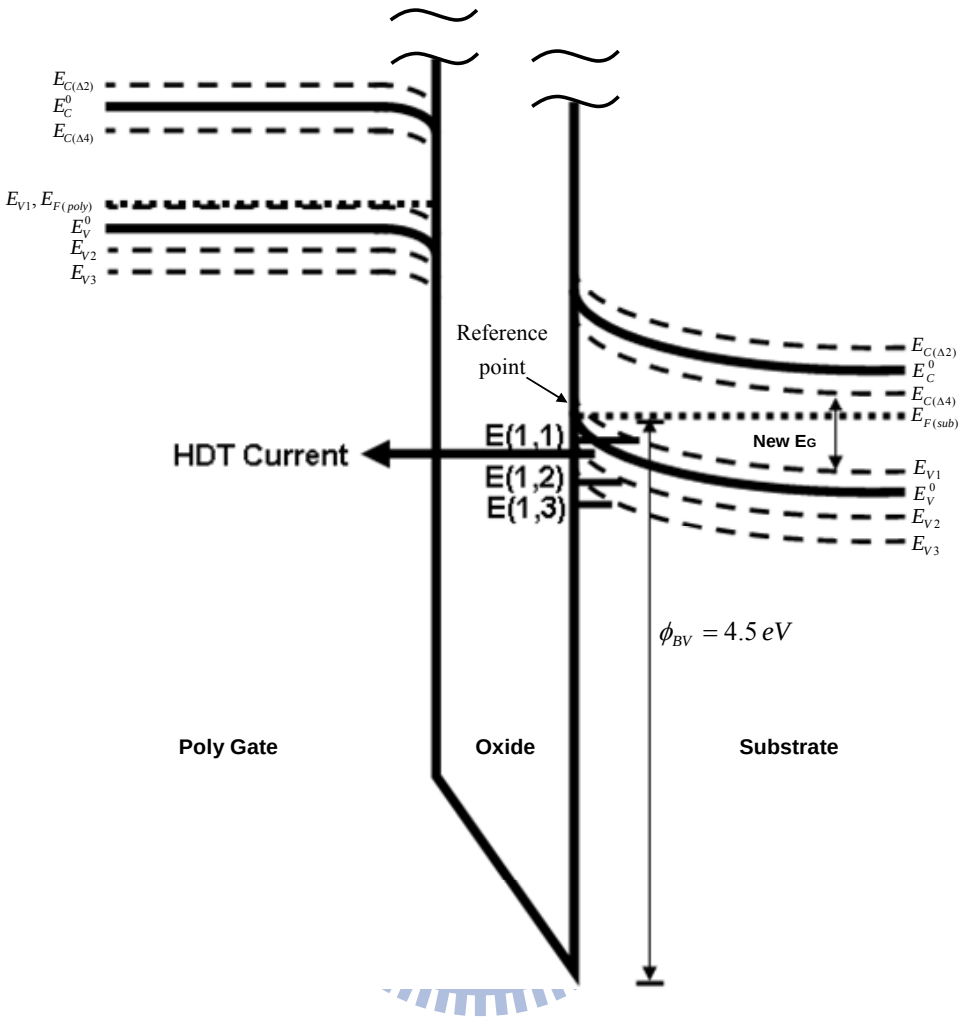


Fig. 2.6 Schematic energy band diagram of a p^+ polysilicon/SiO_2/n-Si system biased in the inversion condition and stressed with uniaxial compressive conditions. The solid lines indicate the conduction and valence band edge without external stress. The dotted lines indicate the stress induced band edge shift of the conduction and valence band. The figure also shows the energy quantization effect in the inversion layer and the hole direct tunneling process from the inversion layer to the polysilicon gate.

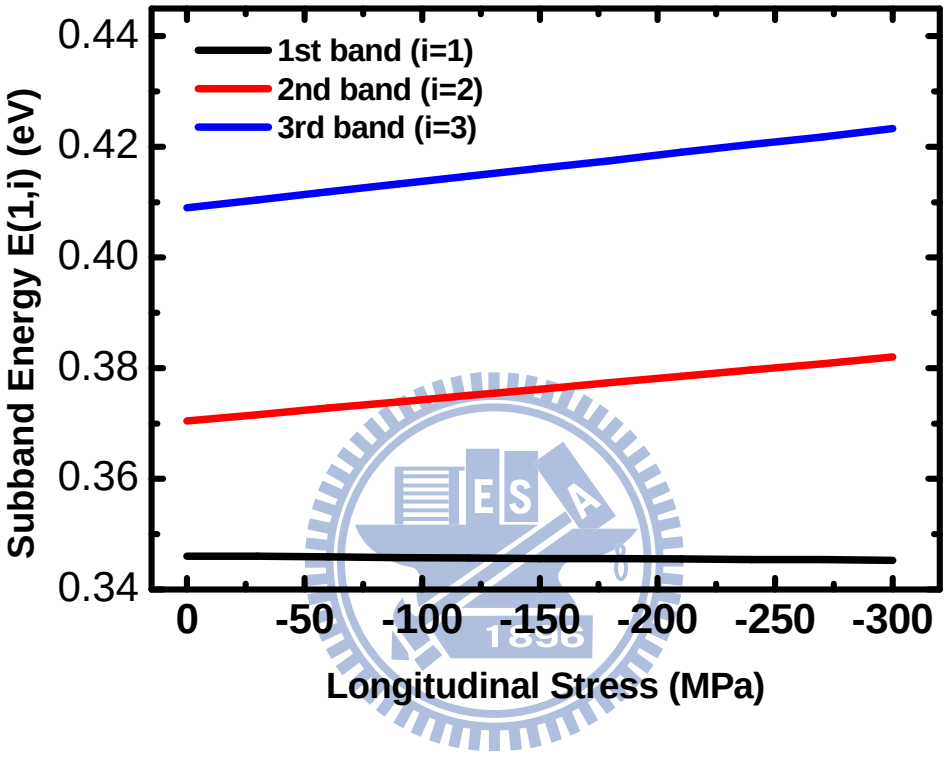


Fig. 2.7 Calculated energy levels versus stress for the top (first), second, and split-off (third) hole subbands.

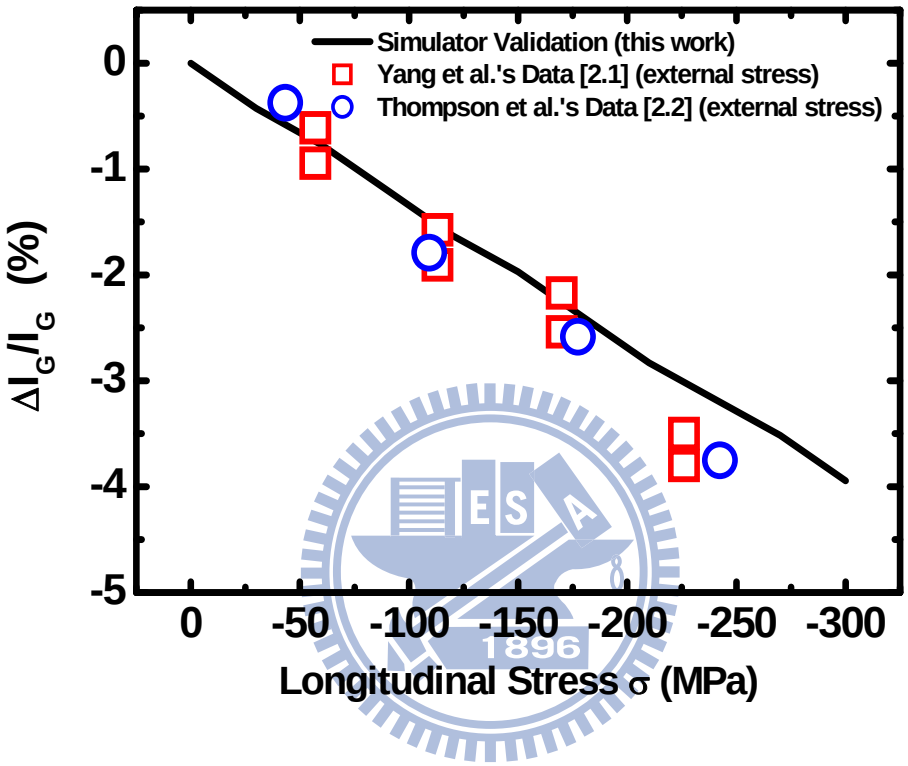
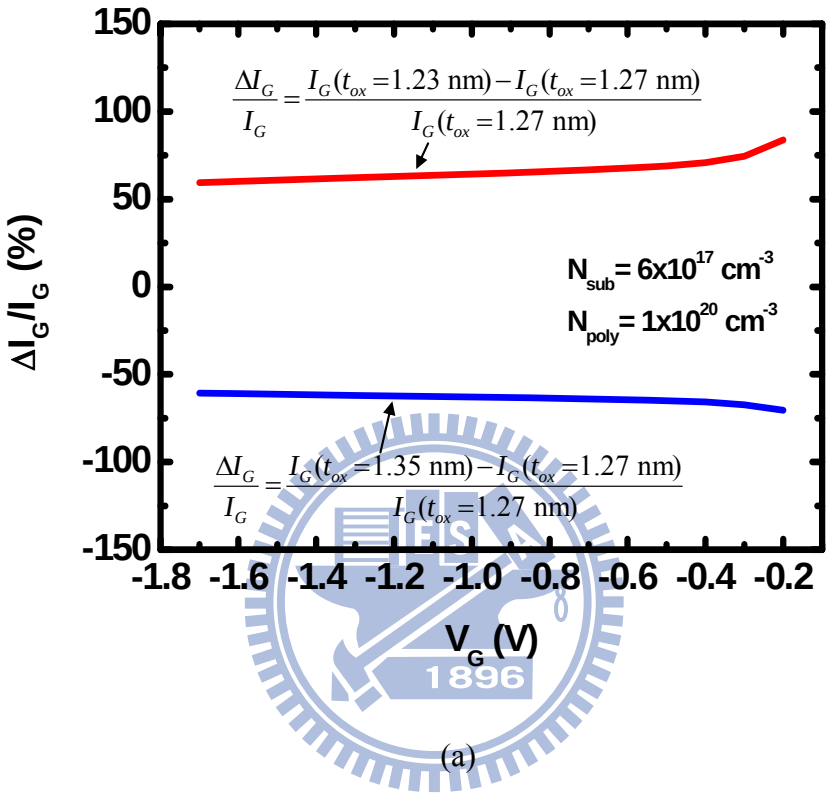
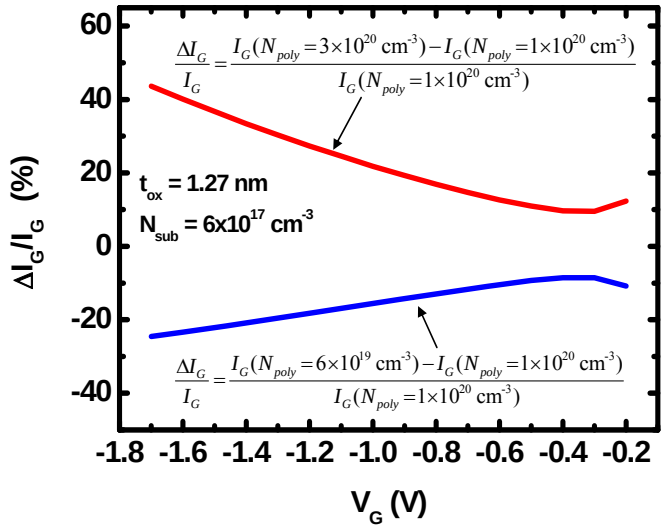


Fig. 2.8 External stress dependent hole gate current data [2.1],[2.2] (symbols) used to examine the validity of the quantum strain simulator. The line represents the simulation result due to the strain altered valence-band splitting only.

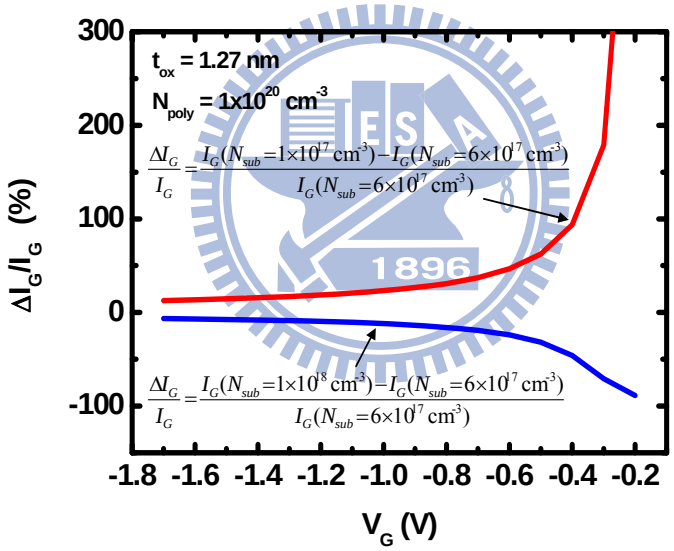


(a)

Fig. 2.9(a) Simulated gate current change versus gate voltage for different gate oxide thicknesses. The formulas used are inserted.



(b)



(c)

Fig. 2.9(b) Simulated gate current change versus gate voltage for different poly gate doping concentrations. The formulas used are inserted.

Fig. 2.9(c) Simulated gate current change versus gate voltage for different substrate doping concentrations. The formulas used are inserted.

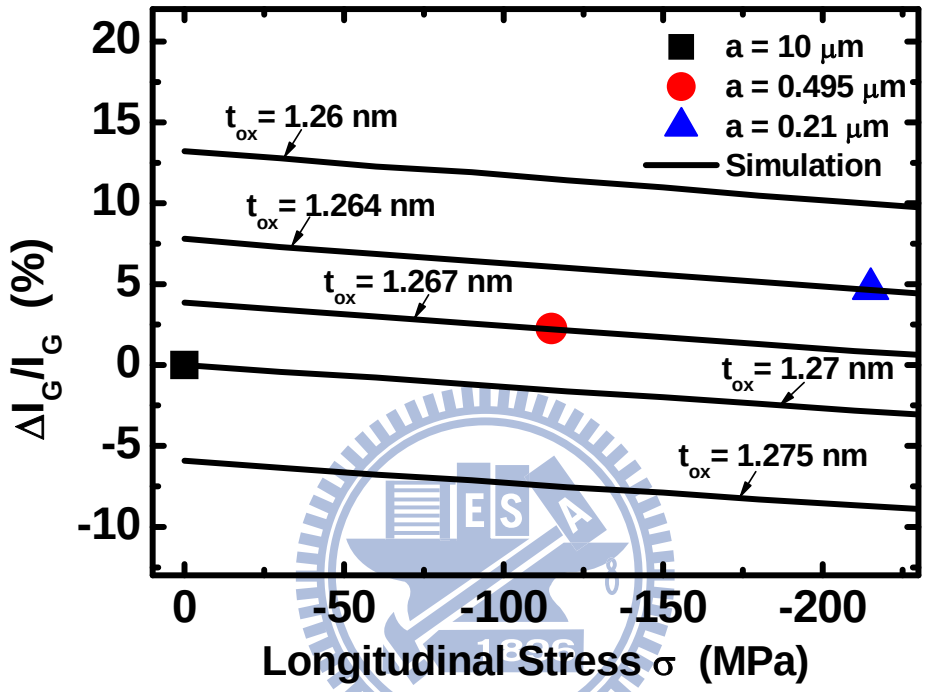


Fig. 2.10 Simulated gate current change versus stress for several oxide thickness with respect to the gate current of $\sigma = 0$ case (that is, t_{ox} = 1.27 nm). Both the polysilicon doping concentration and substrate doping concentration are kept at the nominal values. Also shown for comparison are the experimental data (symbols) corresponding to the inset of Fig. 2.4.

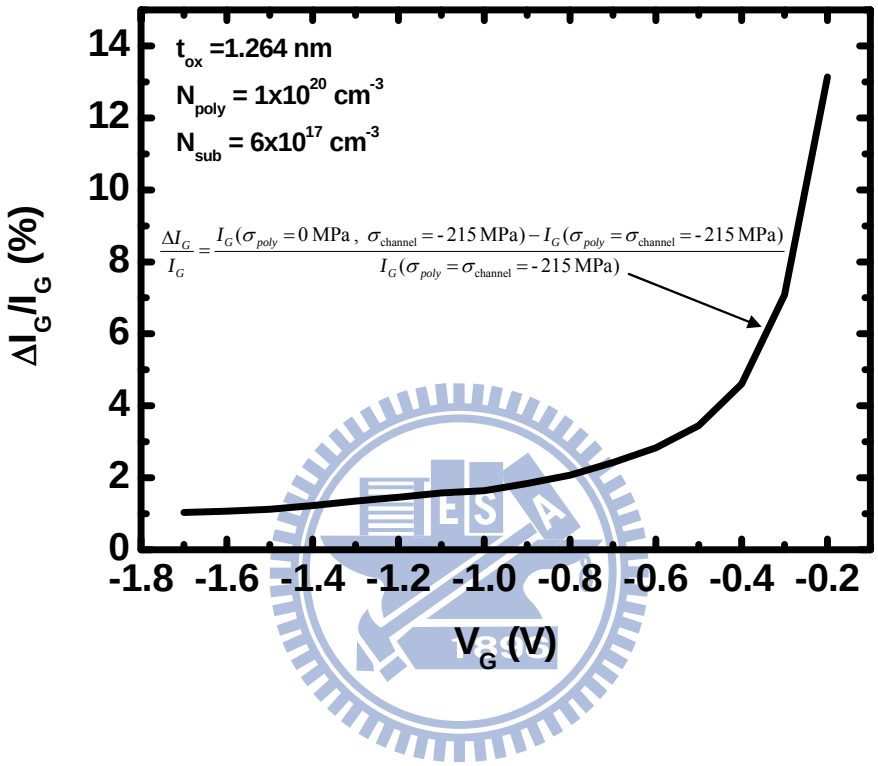


Fig. 2.11 Simulated gate current change of zero poly stress with respect to poly stress of -215 MPa as a function of gate voltage for channel stress of -215 MPa. The formulas used are inserted.

Chapter 3

Extracting Metal-Gate High-*k* Material Parameters by Electron Gate Tunneling Current Transition Modeling

3.1 Introduction

Owing to the dual advantages of eliminating the polysilicon depletion and managing the gate leakage current in the scaling direction, metal gate high-*k* dielectrics are currently replacing the conventional polysilicon gate oxide (SiO_2 or SiON) ones in the MOSFETs manufacturing [3.1],[3.2]. Thus, it is imperative to *experimentally* construct a MOS system in terms of the material and process parameters: the metal workfunction, the physical thickness, permittivity, and electron affinity of high-*k* part, and the physical thickness, permittivity, and electron affinity of the interfacial layer (IL). In addition, the conduction (tunneling in this work) related material parameters must be included as well: the tunneling effective masses in high-*k* and the IL. To achieve the goal, the two standard methods [3.3]-[3.12] may be applied together: (i) fitting of the gate capacitance C_g versus gate voltage V_g and (ii) fitting of the gate tunneling current Ig versus Vg. However, to further ensure the precision of the extraction results, use of the other methods may be needed.

Recently, Zafar, et al. [3.14] proposed one such method in terms of a plot of $d\ln I_g/dV_g$ versus V_g, valid only for I_g dominated by the direct tunneling and/or Fowler-Nordheim tunneling. According to Zafar, et al. [3.14], the peak of $d\ln I_g/dV_g$ indicates the transition of direct tunneling and Fowler-Nordheim tunneling across the high-*k* part and as a consequence, the position of the $d\ln I_g/dV_g$ peak over V_g can provide a direct estimate of the metal workfunction and high-*k* electron affinity. This unique feature was also applied elsewhere [3.15],[3.16]. However, the other features

concerning the height of the $dlnI_g/dV_g$ peak and the shape of the $dlnI_g/dV_g$ curve around the peak were not yet addressed to date. Also, the guidelines needed for the fitting in the context of the $dlnI_g/dV_g$ method were lacking.

The gate leakage modeling studies [3.3]-[3.12] only consider the mechanism of electron direct tunneling from inversion layer. However, large deviation of gate current fitting appear at low gate bias [3.7],[3.9]-[3.13] and the corresponding explanation for this deviation has not been addressed. The model for simulating gate leakage current at low gate bias is needed.

In this work, we propose a new fitting technique dedicated to the $dlnI_g/dV_g$ method, along with the combination of the conventional C_g-V_g and I_g-V_g fitting. First of all, a calculation of gate current due to the electron direct tunneling and/or Fowler-Nordheim tunneling from the inversion layer and IL/Si interface states is carried out, leading to the guidelines of the fitting. The experimental samples are presented in terms of nMOSFETs with low-EOT (1.4 nm) TaC/HfSiON/SiON gate stacks. The underlying material parameters are assessed accordingly, followed by the corroborating evidence.

3.2 Simulations and Guidelines

The energy band diagram of the metal-gate/high-*k*/IL/p-substrate MOS system in flat-band condition is schematically shown in Fig. 3.1. In the figure, the relevant material and process parameters are labeled: Φ_m for the metal workfunction; t_k, ε_k, and χ_k for the physical thickness, permittivity, and electron affinity of high-*k* layer, respectively; t_{IL}, ε_{IL}, and χ_{IL} for the physical thickness, permittivity, and electron affinity of the *IL*, respectively; and χ_s for the silicon electron affinity. The band offsets with respect to silicon, φ_k and φ_{IL}, are equal to $\chi_s - \chi_k$ and $\chi_s - \chi_{IL}$, respectively. Also labeled in Fig. 3.1 are those associated with the tunneling conduction: the tunneling

effective masses of electrons, m_k* for high-*k* and m_{IL}* for *IL*. These parameters now serve as the model parameters in the calculation of the electron gate tunneling current from the inversion layer.

Here, we slightly modified an existing triangular-potential based quantum simulator as already established in our previous works on the polysilicon gate oxide stacks [3.17],[3.18]. This change was made primarily through the WKB transmission probability T_{WKB}:

$$T_{WKB} = Exp[-2(\int_{z_1}^{z_2} \kappa_1(z)dz + \int_{z_2}^{z_3} \kappa_2(z)dz)] \tag{3.1}$$

where z_1, z_2, and z_3 indicate the IL/Si interface, the high-*k*/IL interface, and the metal/high-*k* interface, respectively; and $\kappa_1(z)$ and $\kappa_2(z)$ are the magnitude of the imaginary wave vector in the forbidden bandgap of IL and high-*k* layer, respectively. It is a straightforward task to derive analytic models for T_{WKB} according to the four tunneling criteria φ_1, φ_2, φ_3, and φ_4 as depicted in Fig. 3.2. Here, φ_1 and φ_2 represent the difference of the high-*k* conduction-band sidewall edges with respect to the tunneling stream from the level *E* of subband *j* and valley *i*; and φ_3 and φ_4 represent the difference of the IL conduction-band sidewall edges with respect to the tunneling stream. In case 1 ($\varphi_1(E) > 0$, $\varphi_2(E) > 0$, $\varphi_3(E) > 0$, $\varphi_4(E) > 0$), where the direct tunneling prevails in both layers, T_{WKB} from the subband *j* of valley *i* is the product of the two direct tunneling probabilities for the layers in series:

$$T_{WKB} = Exp[\frac{4\sqrt{2m_k}(\varphi_1^{3/2}(E) - \varphi_2^{3/2}(E))}{3q\hbar F_k}] \times Exp[\frac{4\sqrt{2m_{IL}}(\varphi_3^{3/2}(E) - \varphi_4^{3/2}(E))}{3q\hbar F_{IL}}] \tag{3.2}$$

where F_k and F_{IL} are the electric field in high-k and IL, respectively. In case 2 ($\varphi_1(E) < 0$, $\varphi_2(E) > 0$, $\varphi_3(E) > 0$, $\varphi_4(E) > 0$), the tunneling in high-*k* is the Fowler-Nordheim tunneling and thus T_{WKB} is the product of one direct tunneling probability and one Fowler-Nordheim tunneling probability:

$$T_{WKB} = Exp[\frac{4\sqrt{2m_k}(-\varphi_2^{3/2}(E))}{3q\hbar F_k}] \times Exp[\frac{4\sqrt{2m_{IL}}(\varphi_3^{3/2}(E) - \varphi_4^{3/2}(E))}{3q\hbar F_{IL}}] \quad (3.3)$$

In case 3 ($\varphi_1(E) < 0$, $\varphi_2(E) < 0$, $\varphi_3(E) > 0$, $\varphi_4(E) > 0$), only the IL undergoes tunneling and the T_{WKB} simply becomes

$$T_{WKB} = Exp[\frac{4\sqrt{2m_{IL}}(\varphi_3^{3/2}(E) - \varphi_4^{3/2}(E))}{3q\hbar F_{IL}}] \quad (3.4)$$

Finally, the electron tunneling current from all the populations in the inversion layer can be calculated:

$$J = q\sum_{i,j} f(j,i) g_{2D} \int_{E(j,i)}^{\infty} F(E) T_{WKB}(E) T_R(E) dE \quad (3.5)$$

Here, the formalisms used to calculate the electron impact frequency *f*, the density of states per unit area for the two-dimensional electron gas g_{2D}, the Fermi-Dirac distribution function *F*, and the reflection correction factor T_R were the same as those in [3.17]. Note that in this work, T_R was limited to the IL/Si interface. The reasons are that the reflection at the high-*k*/IL interface, as well as between metal and high-*k*, is quite weak and thus was neglected in the calculation. Fig. 3.3 shows the calculated I_g and $d\ln I_g/dV_g$ versus V_g to highlight these different tunneling cases.

The calculated I_g and $d\ln I_g/dV_g$ are plotted in Fig. 3.4 versus V_g with one of the model parameters as variable. The nominal values of the model parameters in the calculation are Φ_m = 4.48 eV, φ_{IL} = 2.36 eV, φ_k = 1.1 eV, m_{IL}^* = 0.95 m_0, m_k^* = 0.03 m_0, t_{IL} = 1.3 nm, t_k = 2.2 nm, ε_{IL} = 7 ε_0, and ε_k = 12.4 ε_0. By a careful observation of the calculated $d\ln I_g/dV_g$ curves in Fig. 3.4, the relevant guidelines can be drawn. First, m_k^*, t_k, t_{IL}, m_{IL}^*, ε_k, and ε_{IL} can adjust the height of the peak but with different trends: the peak is nearly vertically raised with increasing m_k^*, t_k, t_{IL}, m_{IL}^*, and ε_k while the height of the peak decreases with increasing ε_{IL}. Specifically, m_k^* is the most effective factor in changing the height of the peak. Note that the m_k^*, t_k, t_{IL}, m_{IL}^*,ε_{IL}, and ε_k are

all weak in producing a horizontal shift of the peak.

Second, an increase in Φ_m or φ_k can give rise to a horizontal shift in the position of the peak toward the increasing V_g direction. Only for the φ_k can a simultaneous change in the height of the peak be noticed. Relatively, Φ_m produces little change in the height of the peak. Third, the shape of the $d\ln I_g/dV_g$ curve around the peak can be characterized by a decay from the peak until a saturation of about 2 to 5 V^{-1} in the increasing gate voltage direction. It can be seen that all the parameters have the comparable shape of the $d\ln I_g/dV_g$ curve, except the m_k*; that is, the shape of the $d\ln I_g/dV_g$ curve is only sensitive to the m_k*. Finally, the $d\ln I_g/dV_g$ curve around the peak is independent of φ_{IL}.

3.3 Experimental and Fitting

The presented samples were nMOSFETs with TaC/HfSiON/SiON gate stacks as fabricated in a state-of-the-art process [3.19]. In this process [3.19], the nominal physical thicknesses of SiON and HfSiON were around 1.3 and 2.2 nm, respectively. The process parameters were obtained by C_g-V_g fitting using a Schrödinger-Poisson equations solver Schred [3.20], as depicted in Fig. 3.5: the metal workfunction Φ_m of 4.48 eV; the effective oxide thickness (EOT) of 1.4 nm; and the p-type substrate doping concentration of 3×10^{17} cm^{-3}. The channel width and length of the device were 10 and 1 μm, respectively. The threshold voltage extracted from the measured drain current at V_d = 0.025 V was found to be in agreement with that by Schred (not shown here). Then, we took the permittivity of the hafnium silicate HfSiON, ε_k, as the literature value of 12.4 ε_o [3.19] and reasonably assumed the permittivity of the SiON, ε_{IL}, to be 7 ε_o. The corresponding IL/Si interface barrier height φ_{IL} is 2.36 eV, as determined from the published relationship between the SiON permittivity and its electron affinity [3.21]. Here, we want to stress that owing to the unknown nitrogen

concentration in IL and the possible process induced thickness variation, the uncertainties in the values of ε_{IL} and φ_{IL}, as well as t_{IL} and t_k, exist, as will be addressed later.

The gate current was measured with the source, drain, and substrate tied to the ground. The measured results are depicted in Fig. 3.6 versus V_g. To confirm whether the measured I_g stems from the pure (direct or Fowler-Nordheim) tunneling, a temperature dependent measurement was conducted. The results are shown in Fig. 3.7. Apparently, two distinct tunneling mechanisms occur. The I_g for $V_g > 1$ V slightly increases with the temperature as a result of the pure tunneling, whereas for $V_g < 1$ V I_g significantly increases due to the trap assisted tunneling. Thus, in the subsequent analysis, the fitting will be devoted to the region of $V_g > 1$V.

At this point, all the model parameters are known, except φ_k, m_k*, and m_{IL}*. Initially, we fit the I_g data in a gate voltage range of 1 to 2 V. By following the guidelines above, the fitting process can be straightforward: (i) first adjust φ_k to shift the fitting curve of $d\ln I_g/dV_g$ versus V_g until the position of the peak is close to the experimental value (~1.5 V); (ii) then adjust m_k* until the height of the $d\ln I_g/dV_g$ peak approaches the experimental value (~7 V^{-1}); and (iii) finally adjust m_{IL}* until the fitting I_g versus V_g curve matches the experimental one. The extracted results are φ_k = 1.1 eV, m_k* = 0.03 m_o, and m_{IL}* = 0.95 m_o. The fitting quality is good as displayed in Fig. 3.6 for both the I_g and $d\ln I_g/dV_g$ versus V_g. The extracted φ_k is quantitatively reasonable as compared with the literature value [3.22]. In addition, it has been reported [3.23]-[3.25] that the effective mass of the electrons tunneling through the SiO_2 or silicon oxynitride gate insulator increases significantly with decreasing gate dielectric thickness, thus supporting the very high value of the extracted m_{IL}* in this work.

The extracted electron tunneling effective mass m_k* in the presented HfSiON

sample appears to be rather low. This is the unconventional value relative to the published one (0.24 m_o [3.8]). To address this issue, we performed a second fitting with the m_k* fixed at a typical value of 0.18 m_o. The best fitting can again be obtained in I_g versus V_g characteristics for gate voltage smaller than 2 V, leading to φ_k = 1.9 eV and m_{IL}* = 0.3 m_o. This is the well-known conventional fitting technique. However, as shown in Fig. 3.6, the shape of the calculated $d\ln I_g/dV_g$ curve around the peak is exactly opposite to the measured one, particularly for the gate voltage less than 2 V. Therefore, the conventional method without the $d\ln I_g/dV_g$ fitting might lead to erroneous results. This also dictates that the tunneling effective mass in the high-*k* layer is process dependent. The same argument was also mentioned elsewhere [3.26].

3.4 Extra Evidence

To testify to the validity of the new fitting, extra works were done. First, the experimental I_g was fitted with increasing V_g up to 3.5 V, as shown in Fig. 3.6. We found that the above extracted values of φ_k = 1.1 eV, m_k* = 0.03 m_o, and m_{IL}* = 0.95 m_o remain valid in such a wide V_g range, along with the same fitting quality for both the I_g and $d\ln I_g/dV_g$ versus V_g. However, this is not the case for the conventional fitting technique. As clearly shown in Fig. 3.6, the conventional fitting fails in the whole V_g range. Thus, a wide V_g measurement range can help to justify the validity of the fitting scheme.

The second evidence concerns the reproduction of the temperature effect. The quantum simulator mentioned above was again executed with the same material and process parameters as those obtained in the new fitting technique. In this simulator, the published temperature dependencies were incorporated into the IL/Si interface barrier height φ_{IL} and silicon bandgap Eg: $d\varphi_{IL}(T)/dT = -5\times10^{-4}$ eV/K and

$E_g(T) = E_0 - \frac{\alpha T^2}{T+\beta} + E_x$ where $E_x = 10^{-2}$ eV, $E_0 = 1.17$ eV, $\alpha = 4.73\times10^{-4}$ eV/K, and $\beta = 636$ K [3.27]. The results are given in Fig. 3.7(b). Good agreement with the data not only supports the extracted parameters in the context of the $d\ln(I_g)/dV_g$ method, but also reconfirms the origin of the tunneling for $V_g > 1$ V. Also shown in Fig. 3.7(b) is the case of the conventional method using the same temperature dependencies of φ_{IL} and Eg. Clearly, the new fitting method is closer to data than the conventional one.

Until now, we can examine the uncertainty issue. First, the uncertainty of the IL thickness t_{IL} was done with two different values of t_{IL}: 0.7 and 1.2 nm. The corresponding t_k values were 3.2 and 2.3 nm such as to meet the EOT value. The fitting results are plotted in Fig. 3.8, leading to (i) $\varphi_k = 1.1$ eV, $m_k^* = 0.03\ m_o$, and $m_{IL}^* = 2.8\ m_o$ for $t_{IL} = 0.7$ nm and $t_k = 3.2$ nm; and (ii) $\varphi_k = 1.1$ eV, $m_k^* = 0.03\ m_o$, and $m_{IL}^* = 1.1\ m_o$ for $t_{IL} = 1.2$ nm and $t_k = 2.3$ nm. Strikingly, the extracted m_k^* is equal to $0.03\ m_o$, regardless of the t_{IL} used under the same EOT. This is also the case for the uncertainty in ε_{IL} and φ_{IL}, as demonstrated in Fig. 3.9. Fig. 3.9 reveals that even with the different sets of ε_{IL} and φ_{IL}, only with m_k^* equal to $0.03\ m_o$ can be a good fitting be obtained. Finally, one might think the possible origin of the unconventional m_k^* in this work in terms of the potential drop in the remainder of the high-k conduction band on which the electrons propagate (not tunneling but classical conduction, as shown in Case 2 and 3 of Fig. 3.2). To take this into account, additional calculation was done and the results are given in Fig. 3.10 with the potential drop, denoted as ΔV_k, in the high-k region as a parameter. Obviously, good agreements with the data can be achieved with the same m_k^*, regardless of the potential drop in the high-k layer.

3.5 Physical Origin of Gate Leakage at Low Vg

Physical meaning of serious deviation between experimental gate current and simulated direct tunneling result at low gate bias is still unclear, as shown in Fig. 3.11. In this section, a simple physical model is proposed and then the physical insight of gate leakage at low gate bias is captured.

Due to low population in the conduction band subband energy at low gate bias, calculated direct tunneling is restricted to few available carriers and therefore far lower than experimental value. One possible point of view is that high carrier density population in the IL/Si interface states close to conduction band edge in forbidden band gap of Si may explain the imperfect fitting of experimental gate leakage data, as schematically shown in Fig. 3.12. In Fig. 3.12, the label "Window" represents a local region, sited in the forbidden band gap with respect to conduction band edge, allowing electrons to populate. A simple model can read as:

$$J_{interface} = qV_{thermal} \int N_{interface} F(E) T_{WKB}(E) dE \tag{3.6}$$

where $V_{thermal}$ is thermal velocity (10^7 cm/s at room temperature); and $N_{interface}$ is interface trap density in "Window" ($cm^{-3}eV^{-1}$) and can serve as fitting factor in this work. The refitting result for both direct tunneling current and $J_{interface}$ is shown in Fig. 3.11. Excellent reproduction of experiment gate leakage is achieved by means of incorporating the mechanism of $J_{interface}$ in our model. The fitting parameters are Window = 0.5 eV and $N_{interface} = 1.1\times10^{20}$ $cm^{-3}eV^{-1}$. If we assume that interface states locate in a width of 0.5 nm, the 2-D interface trap density ($N_{interface}$) equals 5.5×10^{12} $cm^{-2}eV^{-1}$ that is one to two orders of magnitude larger than the conventional values of SiO_2/Si interface [3.28]. The large $N_{interface}$ may be caused by high nitrogen concentration and Hf incorporation in IL in our test samples. We present how the values of Window affect calculated results, as shown in Fig. 3.13. Evidently, the smaller turn-on voltage of $J_{interface}$, the larger Window due to higher population in

interface states with Window increasing. Hence, the fitting guideline and physical origin of gate leakage at low gate bias is satisfactorily constructed.

3.6 Valence Band Electron Tunneling through High-κ Gate Stacks

In this section, we focus on simulating the valence band electron tunneling current, as schematically shown in Fig. 3.14. We modified the valence band electron tunneling model for SiO_2 gate dielectric [3.29] to apply to high-κ/metal-gate dielectric MOSFETs. The modified model can read as:

$$J_{Val\_e} = \frac{4\pi q m^*_{valence}}{h^3} \int_0^{E_{M\max}} E_M \times T_{WKB}(E_M) dE'_M \quad (3.7)$$

$$T_{WKB} = Exp[\frac{4\sqrt{2m^*_{k\_val}}(\varphi_1^{3/2}(E) - \varphi_2^{3/2}(E))}{3q\hbar F_k}] \times Exp[\frac{4\sqrt{2m^*_{IL\_val}}(\varphi_3^{3/2}(E) - \varphi_4^{3/2}(E))}{3q\hbar F_{IL}}] \quad (3.8)$$

where $m^*_{valence}$ is the effective mass in silicon valence band and it is equal to 0.65 m_0 [3.29]; $m^*_{IL\_val}$ and $m^*_{k\_val}$ are the valence electron tunneling effective mass in IL and high-κ layer, respectively; and E_M is defined as the electron energy in silicon valence band with respect to Fermi level of metal gate and only the electrons in valence band with the energy of $E_M>0$ have the opportunity to tunnel from substrate to metal gate.

With this modified model for high-κ gate stacks MOSFETs, the experimental substrate current due to valence band electron tunneling can be modeled well, as shown in Fig. 3.15. We find that the valence electron tunneling effective mass in IL is smaller than conduction electron tunneling effective mass. This phenomenon concerning tunneling effective mass reduction was also reported elsewhere on gate oxide or oxynitride [3.30].

3.7 Conclusion

To accurately extract the material and process parameters in the metal gate high-*k*

dielectrics, we have systematically constructed a new fitting scheme over the $dlnI_g/dV_g$ versus V_g curve, along with the combination of the C_g-V_g and I_g-V_g fitting. With the guidelines created for the fitting in the experimental samples with low-EOT TaC/HfSiON/SiON gate stacks, the underlying material and process parameters have been extracted. The extracted results have been verified by extra measurements at higher temperature and drain voltage. The uncertainties encountered in the determination of some process parameters have been adequately clarified. In addition, we have demonstrated that the conventional method without the $dlnI_g/dV_g$ fitting might lead to erroneous results. Thus, $dlnI_g/dV_g$ fitting should be taken into account in the assessment of the metal-gate high-*k* material parameters.

The physical origin of gate leakage at low gate bias has been proposed. From our excellent fitting works, the gate leakage current at low gate bias can be attributed to electron tunneling from IL/Si interface states to metal-gate. Furthermore, good fitting of experimental Ig-Vg curve across eight decades of current has been achieved.

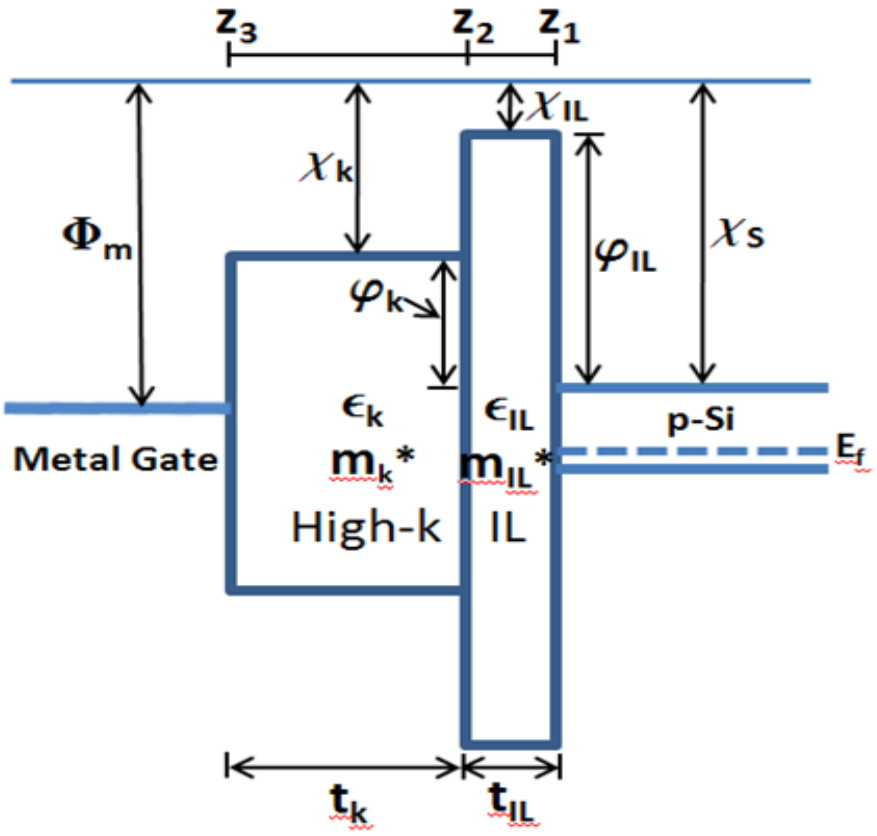
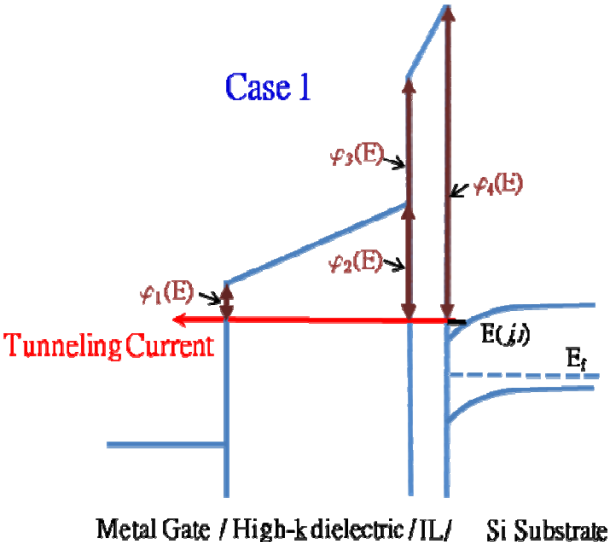
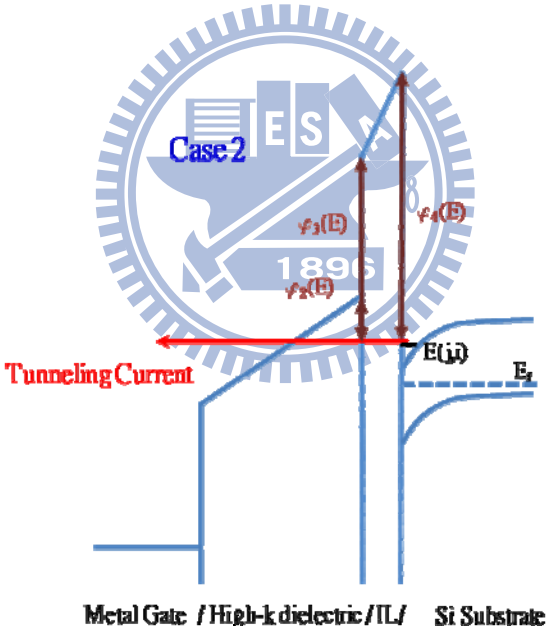


Fig. 3.1 Schematic of the energy band diagram of a metal-gate/high-κ/IL/p-Si system biased in flat-band condition. The process and material parameters involved in this work are labeled.



(a)



(b)

Fig. 3.2(a) Schematic description of tunneling case 1: direct tunneling through both high-κ and IL.

Fig. 3.2(b) Schematic description of tunneling case 2: F-N tunneling occurring in high-κ layer.

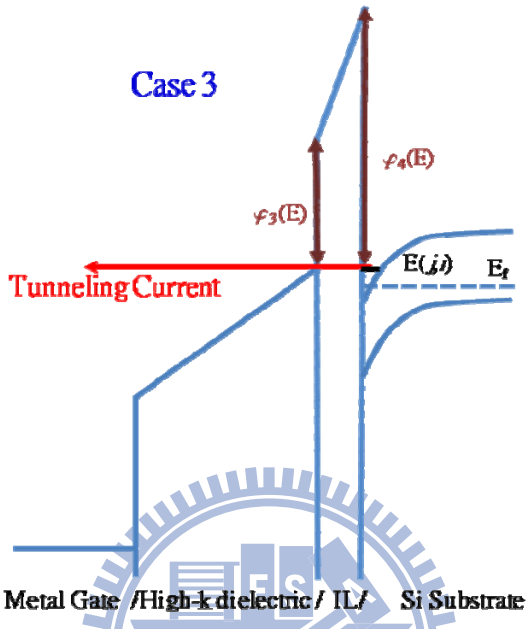


Fig. 3.2(c) Schematic description of tunneling case 3: only direct tunneling through IL.

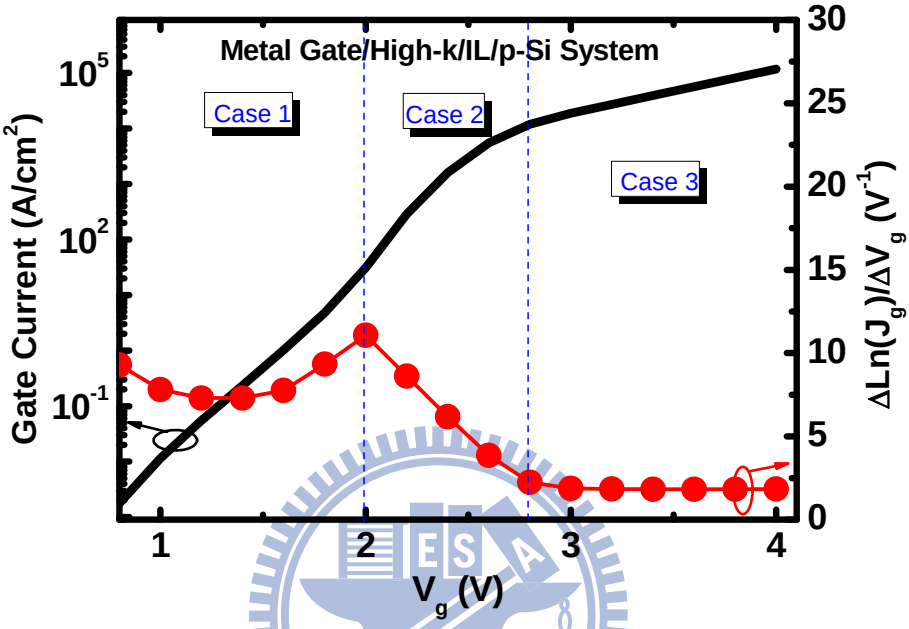
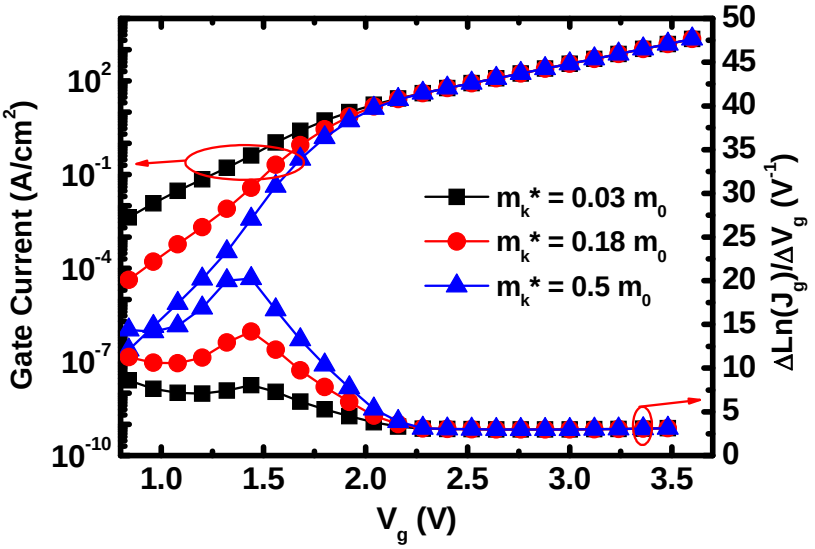
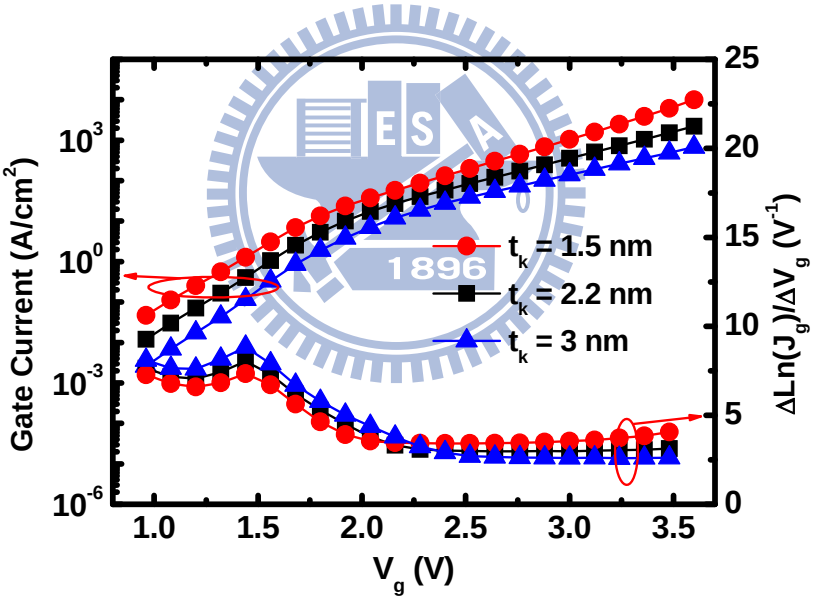


Fig. 3.3 Simulated gate current and $d\ln I_g/dV_g$ in a wide range of gate voltage up to 4 V. The parameters used in the calculation are: $\Phi_m = 4.48$ eV, $\varphi_k = 1.65$ eV, $\varphi_{IL} = 3.15$ eV, $m_k^* = 0.18\ m_o$, $m_{IL}^* = 0.5\ m_o$, $t_k = 2$ nm, $t_{IL} = 1$ nm, $\varepsilon_k = 12.4\ \varepsilon_0$, and $\varepsilon_{IL} = 3.9\ \varepsilon_0$.

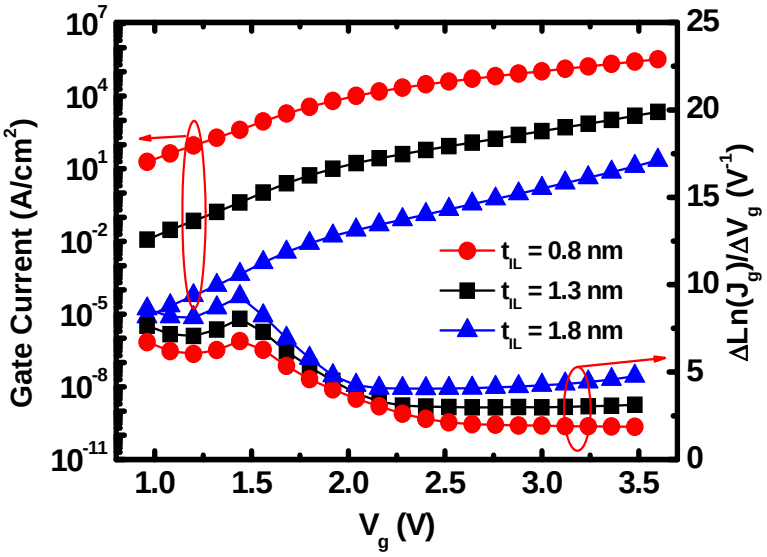


(a)

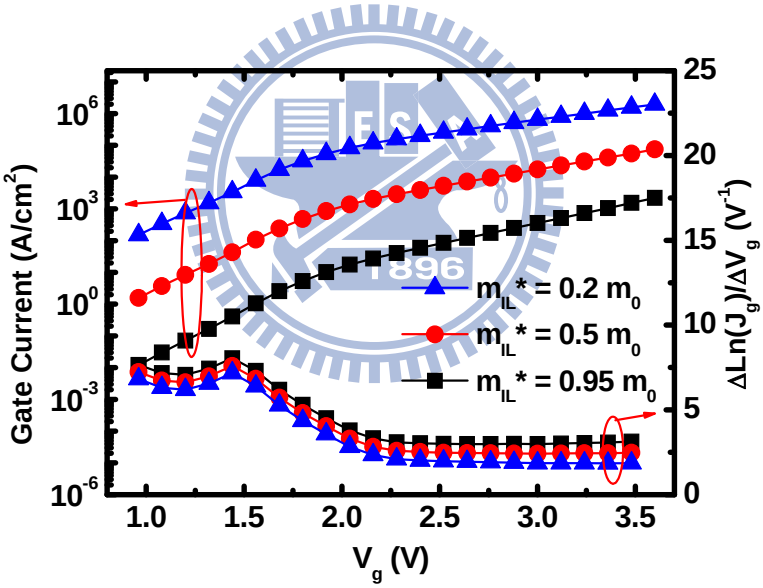


(b)

Fig. 3.4(a) Simulated gate current I_g and $d\ln I_g/dV_g$ versus V_g for varying m_k*.
Fig. 3.4(b) Simulated gate current I_g and $d\ln I_g/dV_g$ versus V_g for varying t_k.



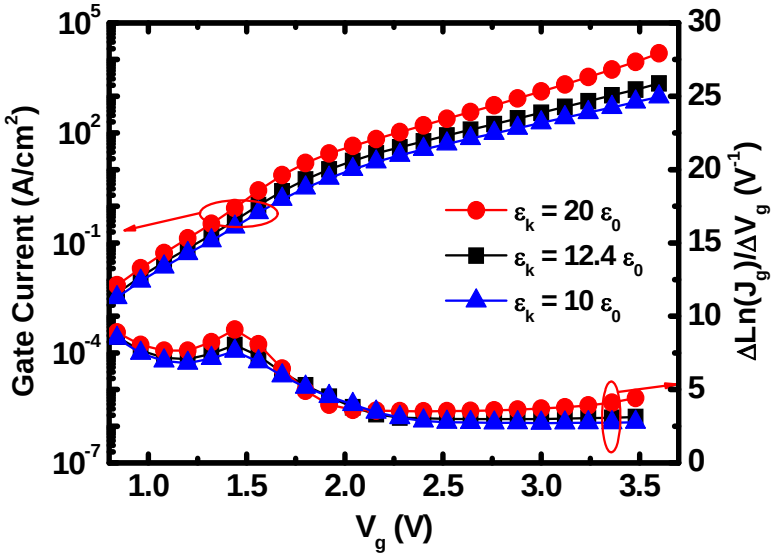
(c)



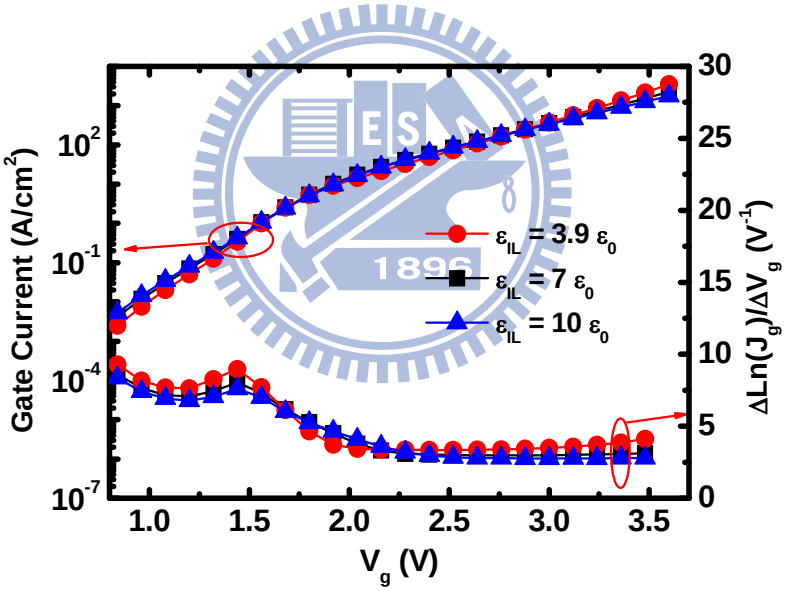
(d)

Fig. 3.4(c) Simulated gate current I_g and $d\ln I_g/dV_g$ versus V_g for varying t_{IL}.

Fig. 3.4(d) Simulated gate current I_g and $d\ln I_g/dV_g$ versus V_g for varying m_{IL}*.



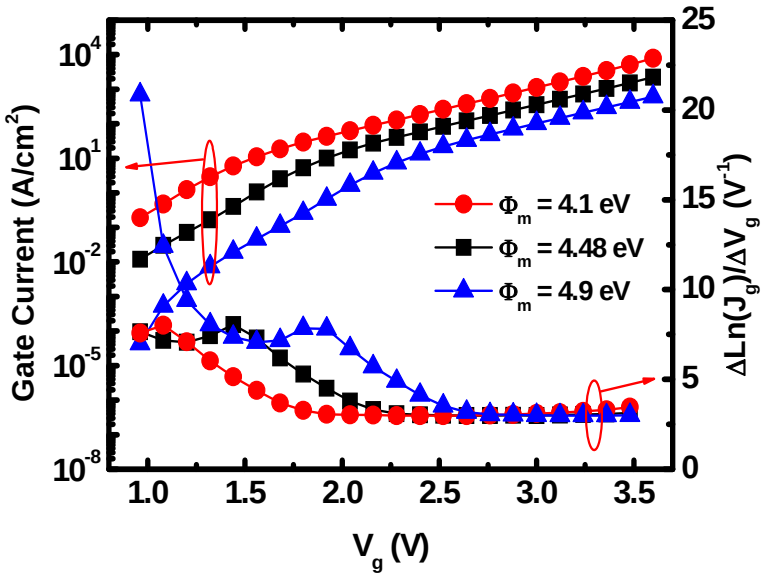
(e)



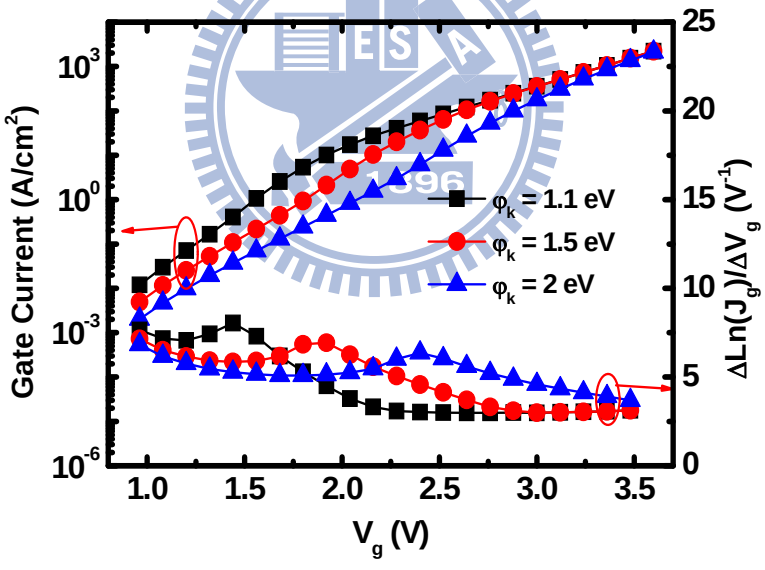
(f)

Fig. 3.4(e) Simulated gate current I_g and $d\ln I_g/dV_g$ versus V_g for varying ε_k.

Fig. 3.4(f) Simulated gate current I_g and $d\ln I_g/dV_g$ versus V_g for varying ε_{IL}.

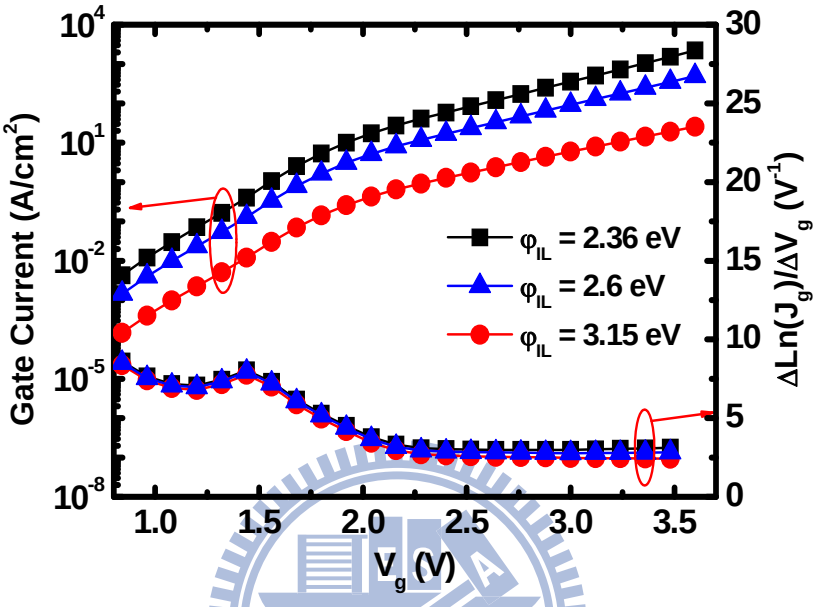


(g)



(h)

Fig. 3.4(g) Simulated gate current I_g and $d\ln I_g/dV_g$ versus V_g for varying Φ_m.
Fig. 3.4(h) Simulated gate current I_g and $d\ln I_g/dV_g$ versus V_g for varying φ_k.



(i)

Fig. 3.4(i) Simulated gate current I_g and $dlnI_g/dV_g$ versus V_g for varying φ_{IL}.

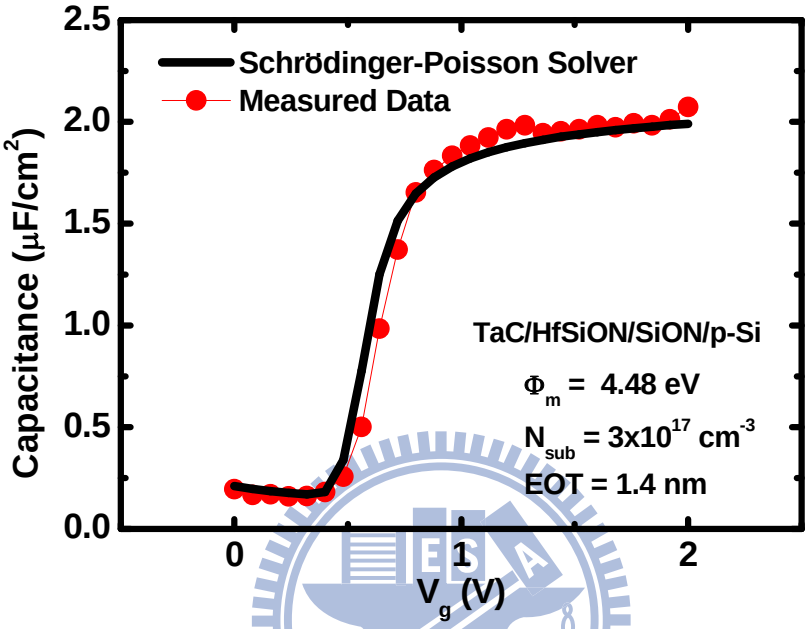


Fig. 3.5 Experimental (symbol) and simulated (line) C_g versus V_g for TaC/HfSiON/SiON gate stacks n-MOSFET. The extrated parameters are: effective oxide thickness EOT = 1.4 nm; substrate doping concentration $N_{sub} = 3\times10^{17}$ cm^{-3}; metal-gate workfunction $\Phi_m = 4.48$ eV.

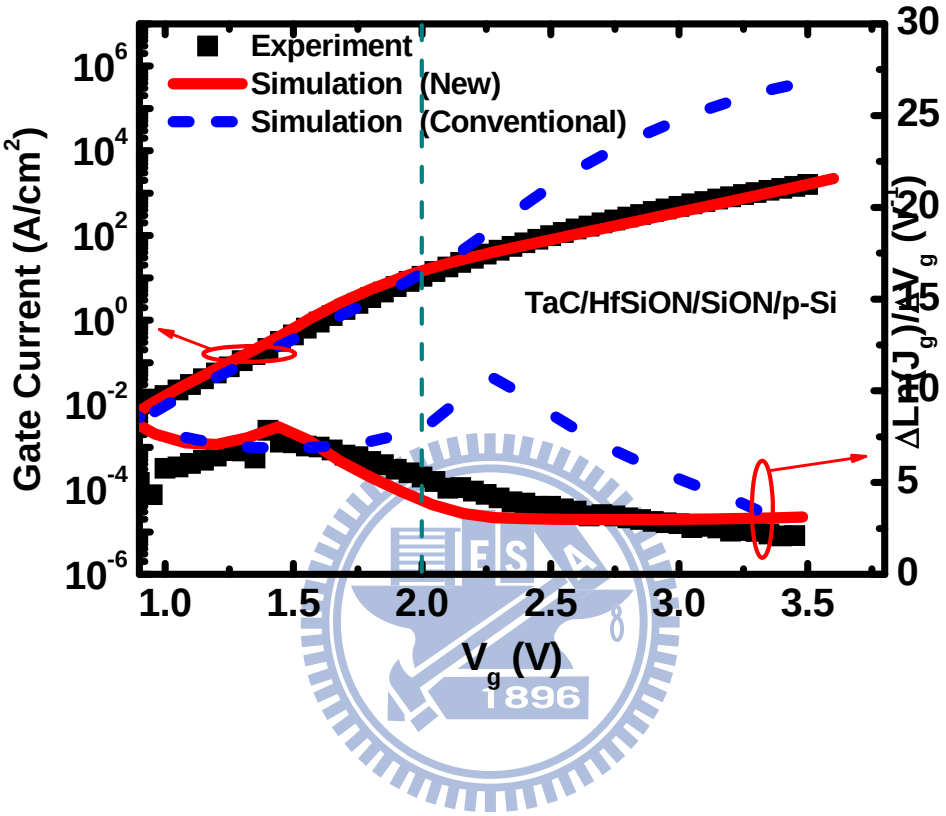
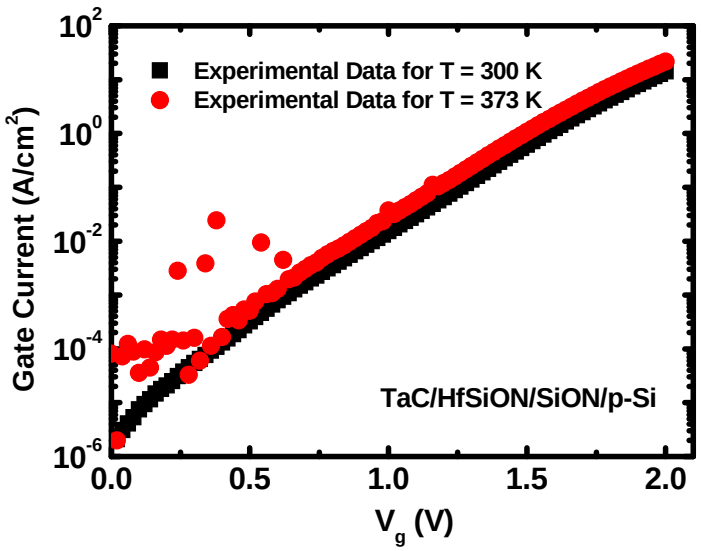
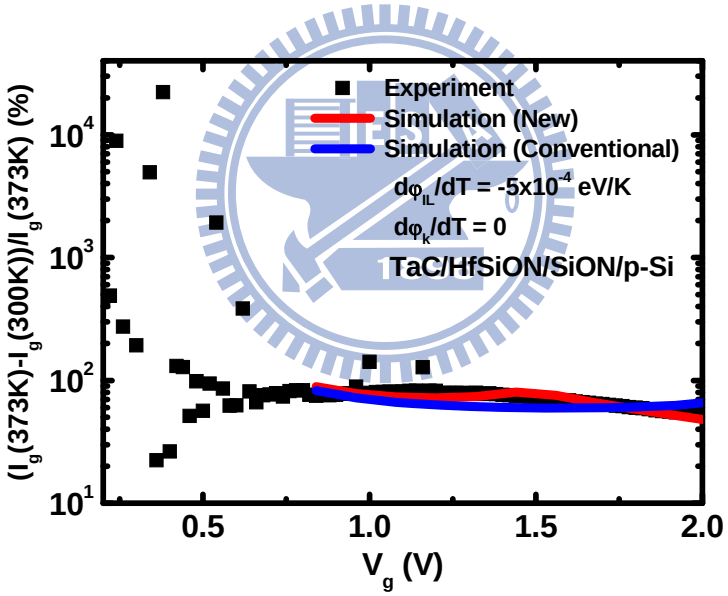


Fig. 3.6 Comparison of the experimental (symbols) gate current and $d\ln I_g/dV_g$ versus V_g with calculated (lines) results using two sets of parameters. Red Line (new method): $\varphi_k = 1.1$ eV, $m_k^* = 0.03\ m_o$, and $m_{IL}^* = 0.95\ m_o$. Blue Line (conventional method): $\varphi_k = 1.9$ eV, $m_k^* = 0.18\ m_o$, and $m_{IL}^* = 0.3\ m_o$. Other parameters are t_{IL} = 1.3 nm and t_k = 2.2 nm.



(a)



(b)

Fig. 3.7(a) Measured gate current at T = 300 and 373 K versus gate voltage for TaC/HfSiON/SiON n-MOSFETs.

Fig. 3.7 (b) Comparison of simulated (line) gate current change of T = 373K with respect to T = 300K versus V_g with measured data (symbols). The parameters used to create the red line (new method) and blue line (conventional method) in Fig. 3.6 are also used here.

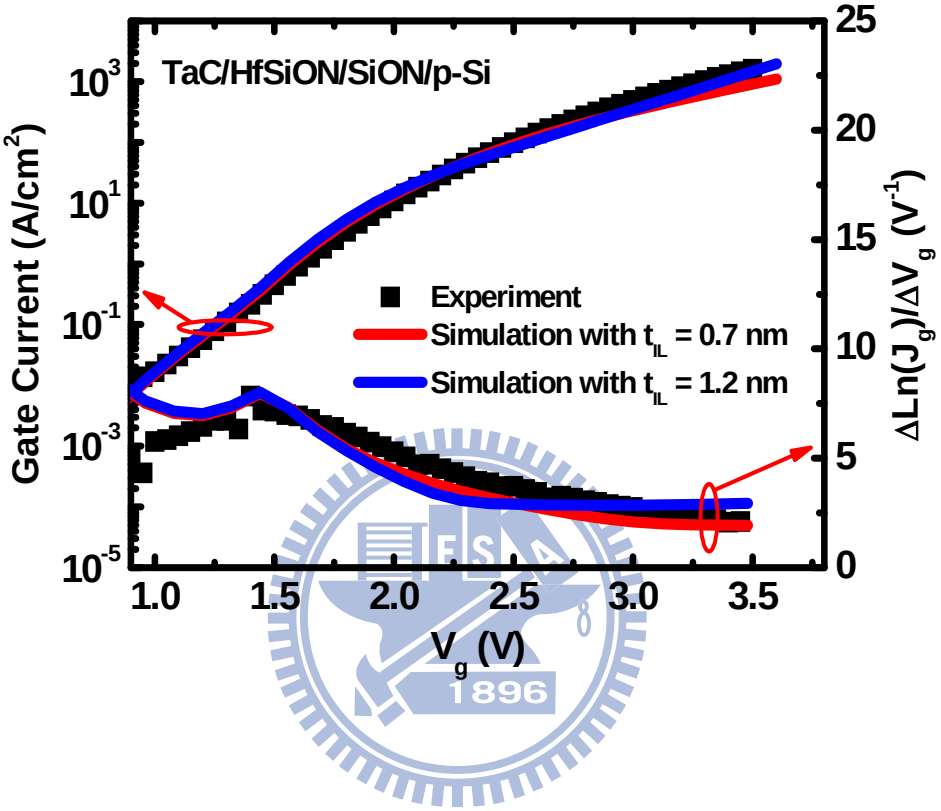


Fig. 3.8 Comparison of the experimental (symbols) gate current and $dlnI_g/dV_g$ versus V_g with calculated (lines) results using two sets of t_k and t_{IL} for the same EOT (1.4 nm). Red Line: t_{IL} = 0.7 nm, t_k = 3.2 nm, and m_{IL}^* = 2.8 m_o. Blue Line: t_{IL} = 1.2 nm, t_k = 2.3 nm, and m_{IL}^* = 1.1 m_o. Other parameters are m_k^* = 0.03 m_o and φ_k = 1.1 eV.

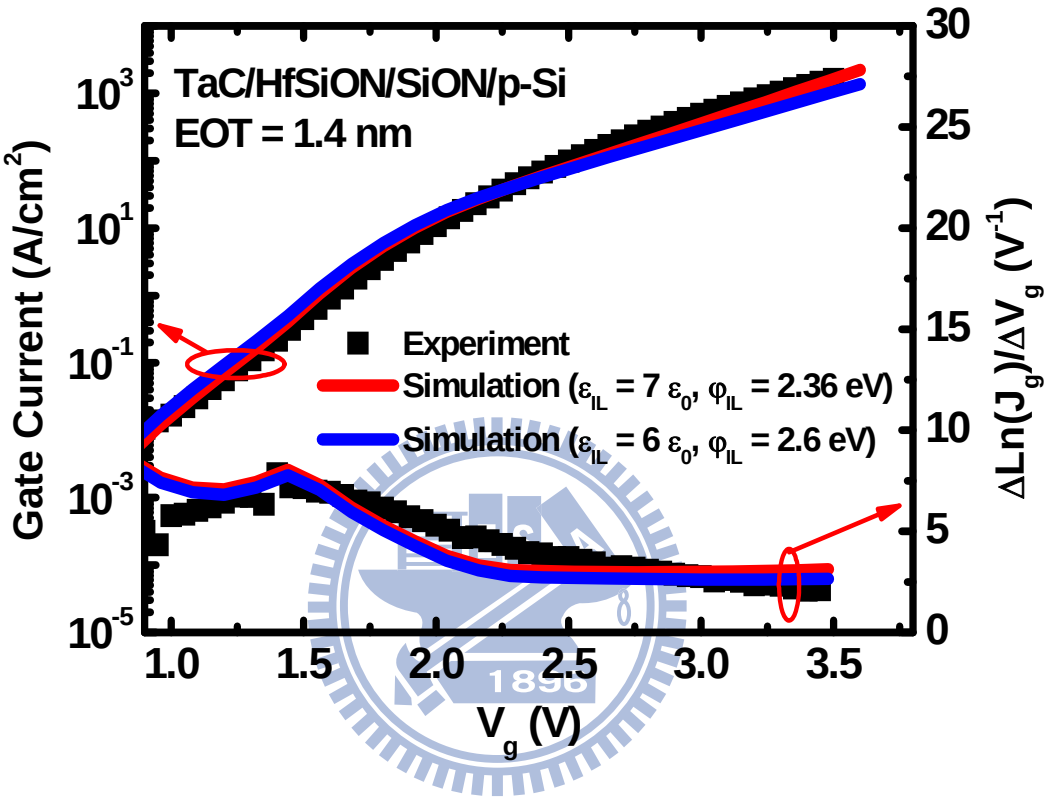


Fig. 3.9 Comparison of the experimental (symbols) gate current and $d\ln I_g/dV_g$ versus V_g with calculated (lines) results using two sets of ε_{IL} and φ_{IL}. The same EOT (1.4 nm) is preserved. Red Line: $m_{IL}^* = 0.95\ m_o$, and $t_{IL} = 1.3$ nm. Blue Line: $m_{IL}^* = 1.15\ m_o$, and $t_{IL} = 1.1$ nm. Other parameters are $\varphi_k = 1.1$ eV, $m_k^* = 0.03\ m_o$, and $t_k = 2.2$ nm.

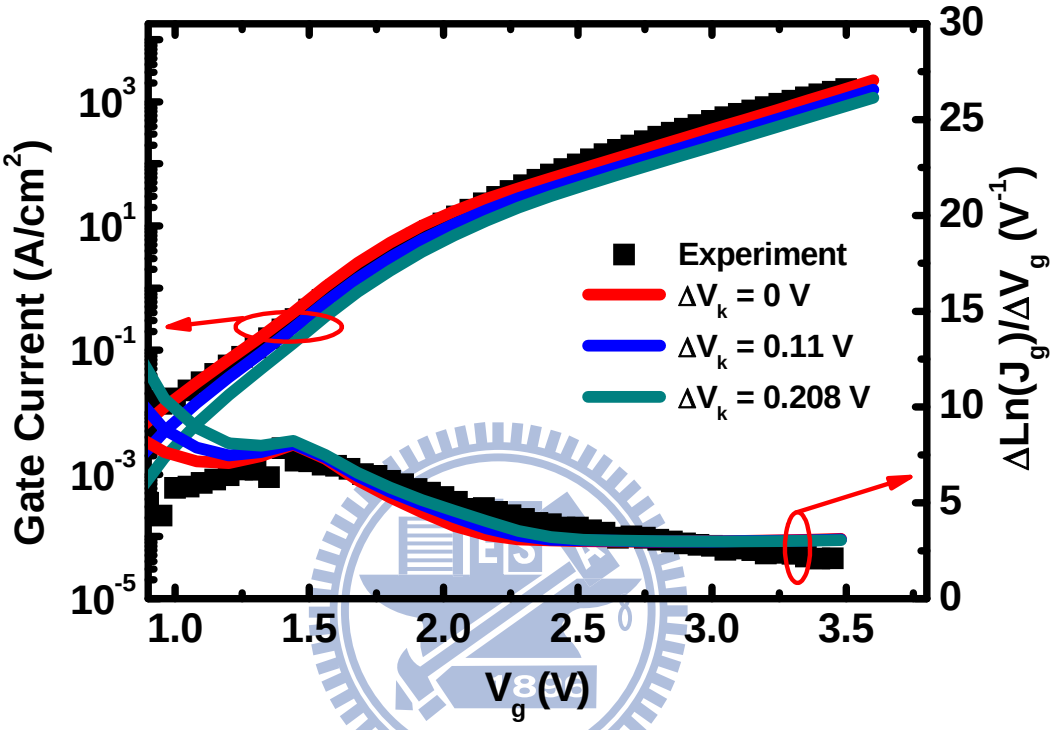
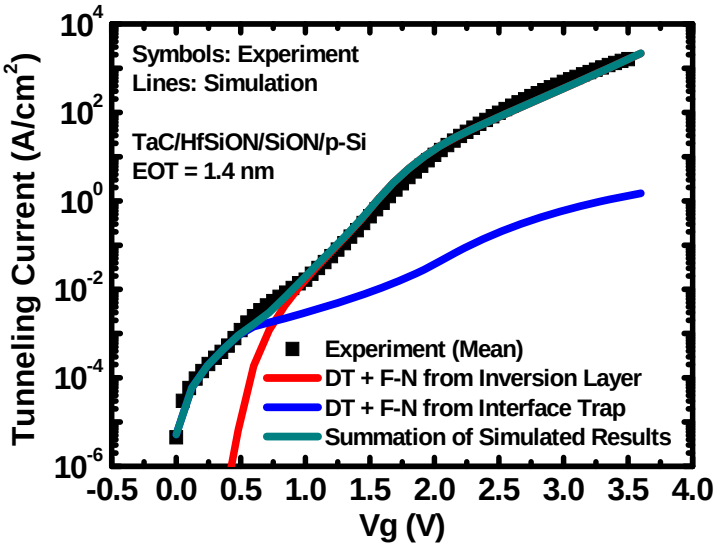
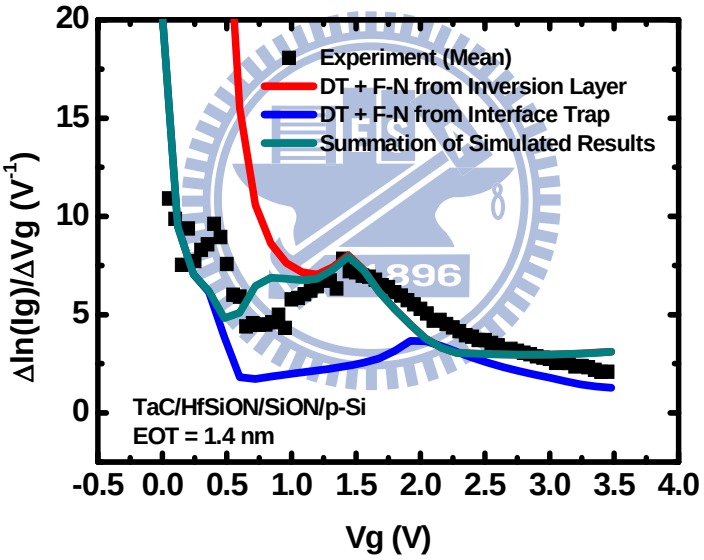


Fig. 3.10 Comparison of the experimental (symbols) gate current and $d\ln I_g/dV_g$ versus V_g with calculated (lines) results with the potential drop in high-k dielectric (ΔV_k) as a parameter. Fitting parameters: Φ_m = 4.48 eV, φ_k = 1.1 eV, φ_{IL} = 2.36 eV, m_k^* = 0.03 m_o, m_{IL}^* = 0.95 m_o, t_k = 2.2 nm, t_{IL} = 1.3 nm, ε_k = 12.4 ε_0, and ε_{IL} = 7 ε_0.



(a)



(b)

Fig. 3.11(a) Comparison of experimental data versus Vg with calculated direct and F-N tunneling current from inversion layer and interface states. Summation of both calculated tunneling current components is also shown. Parameters for calculating electron tunneling from interface states are Window = 0.5 eV and $N_{interface} = 1.1\times10^{20}$ $cm^{-3}eV^{-1}$. Other parameters are the same as those used in the red line of Fig. 3.6.

Fig. 3.11(b) Comparison of the experimental (symbols) dlnIg/dVg versus Vg with calculated (lines) results of direct and F-N tunneling current from inversion layer and interface states. Parameters for calculating electron tunneling from interface states are Window = 0.5 eV and $N_{interface} = 1.1\times10^{20}$ $cm^{-3}eV^{-1}$. Other parameters are the same as those used in the red line of Fig. 3.6.

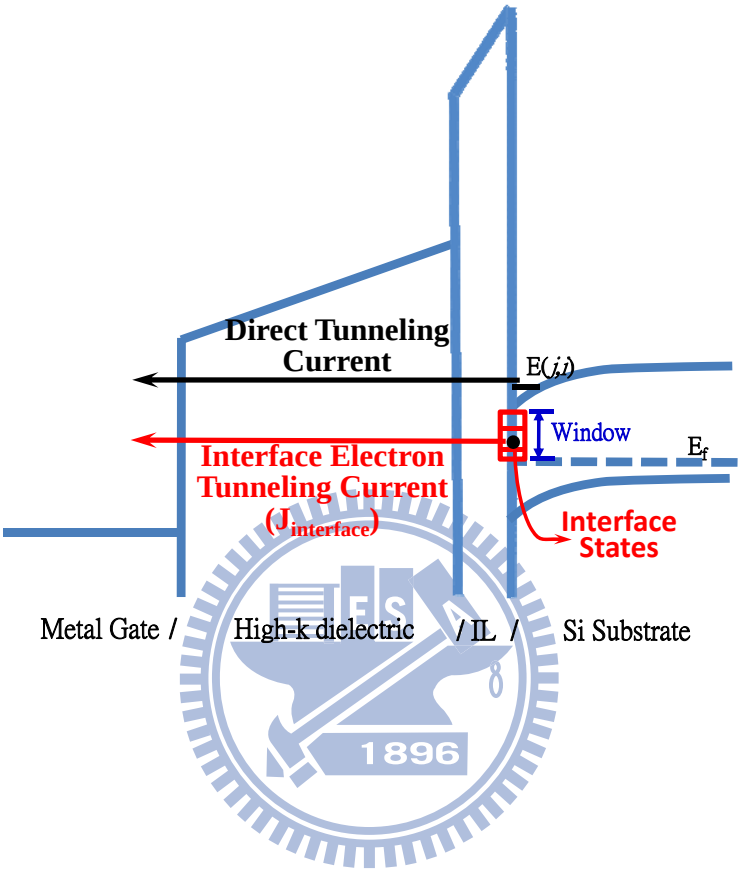


Fig. 3.12 Schematic band diagram showing the mechanism of electron tunneling from IL/Si interface states.

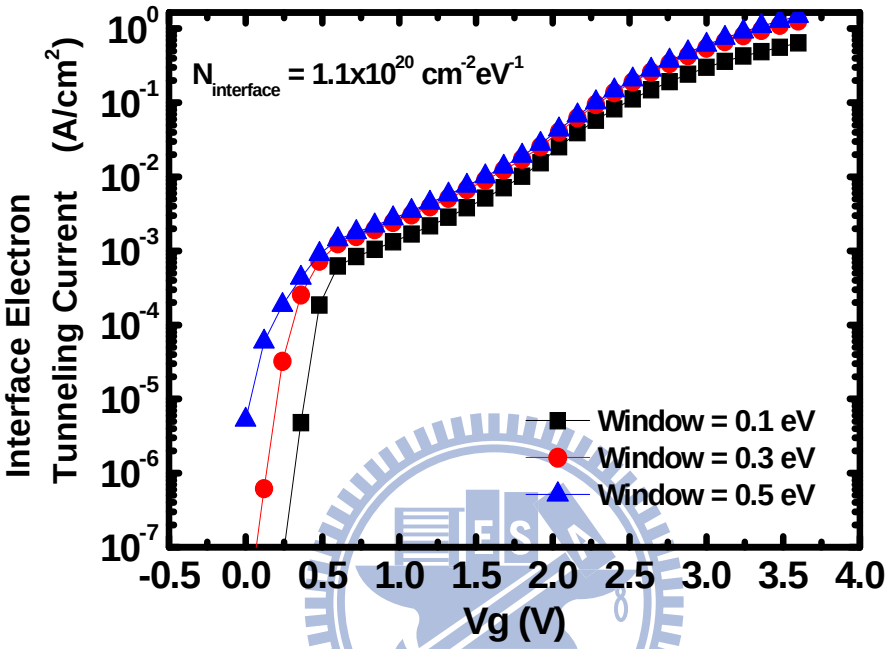


Fig. 3.13 Calculated electron tunneling current from IL/Si interface states versus Vg for different values of Window.

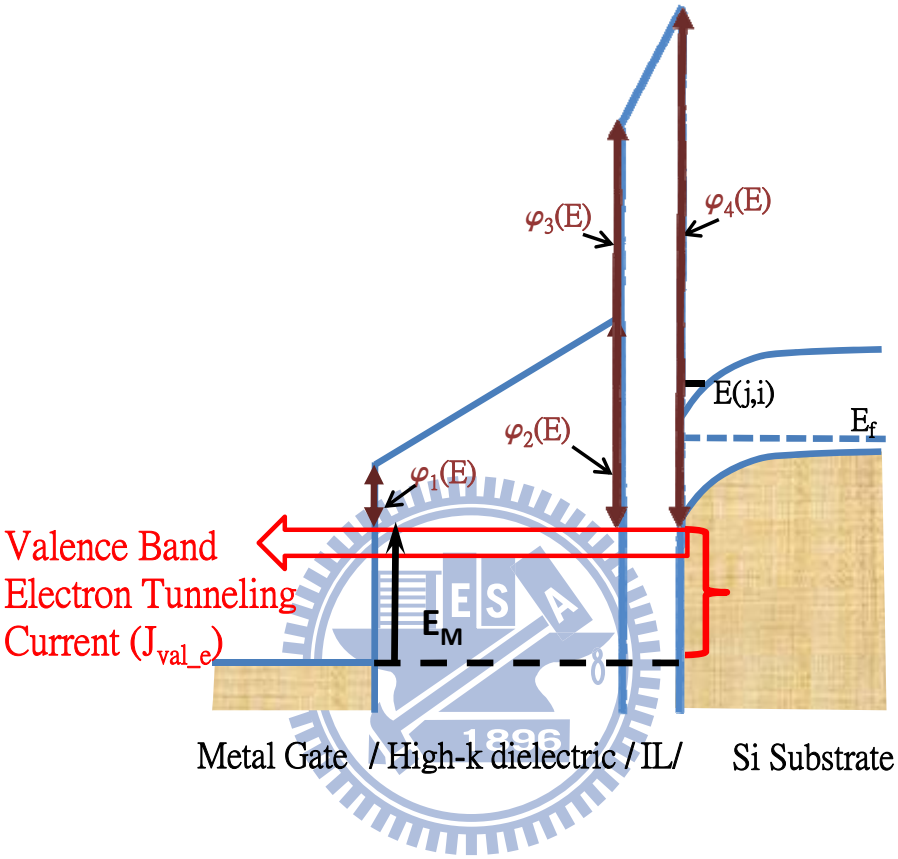


Fig. 3.14 Schematic of energy band diagram showing the mechanism of valence band electron tunneling through high-κ stacks.

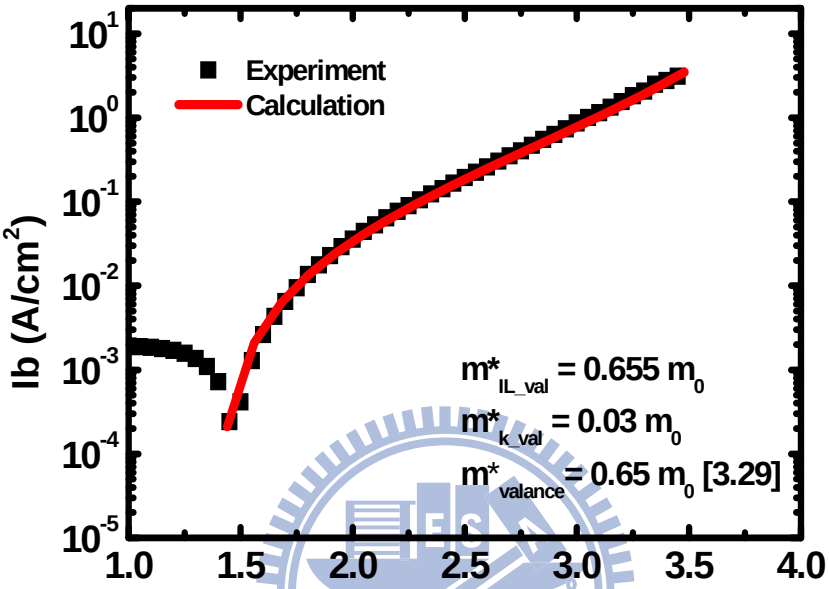


Fig. 3.15 Comparison of experimental substrate current data versus Vg with calculated valence electron tunneling current. Parameters for calculating valence electron tunneling current are $m^*_{IL\_val} = 0.655\ m_0$, $m^*_{k\_val} = 0.03\ m_0$, and $m^*_{valence} = 0.65\ m_0$. Other parameters are the same as those used in the red line of Fig. 3.6.

Chapter 4

Determination of Tunneling Effective Mass and Transition Dielectric in High-κ Metal-Gate Stacks by dlnIg/dVg Fitting

4.1 Introduction

High-κ metal-gate stacks are currently taking the place of conventional polysilicon gate oxide ones in advanced MOSFET manufacturing. Thus, experimental assessment of gate-stack material parameters is imperative. Specifically, Zafar et al. [4.1] proposed a fast method in terms of a dlnIg/dVg versus Vg plot, valid only for gate current Ig stemming from an inversion layer via direct tunneling and/or Fowler-Nordheim tunneling. The method [4.1] relied on a gate-voltage criterion featuring the peak of dlnIg/dVg, which has a linkage to the onset of tunneling transition and hence can readily furnish metal work function and high-κ electron affinity. To find more general applications, recently we have modified the method, resulting in a new curve fitting around the peak of dlnIg/dVg, along with the created guidelines for the fitting [4.2]. While applying to 1.4-nm EOT TaC/HfSiON/SiON n-channel MOSFETs, the dlnIg/dVg fitting, in combination with both gate capacitance Cg-Vg fitting and Ig-Vg fitting, has exhibited the ability to accurately extract material parameters of interest [4.2]; particularly, a very low value of 0.03 m_o was encountered in electron tunneling effective mass in HfSiON layer. However, it is uncertain whether such unconventionally low effective mass exists in other high-κ materials. On the other hand, additional thermal treatment after deposition of high-κ gate stack may give rise to a reaction and hence formation of a transition (intermixing) layer between high-κ and interfacial layer (IL) [4.3]-[4.6]. A good dlnIg/dVg fitting in

TaC/HfSiON/SiON case [4.2] pointed to the absence of such transition dielectric. Whether this applies to case of other high-κ materials remains unclear.

To clarify aforementioned issues, in this work we present additional samples in terms of 0.75-nm TiN/HfO_2/SiON nMOSFETs undergoing the dlnIg/dVg fitting.

4.2 **Experimental and Fitting**

N-channel MOSFETs with TiN/HfO_2/SiON gate stack were fabricated in a state-of-the-art process. Nominal physical thicknesses of HfO_2 and SiON were 1.4 and 0.9 nm, respectively. Through Cg-Vg fitting, as shown in Fig. 4.1, we obtained EOT of 0.75 nm, metal-gate work function Φ_m of 4.5 eV, and p-type substrate doping concentration of 8×10^{17} cm^{-3}. The permittivity of HfO_2 (ε_k) was estimated at 22 ε_0 [4.7]. To meet EOT = 0.75 nm, the permittivity of SiON (ε_{IL}) was determined to be 7 ε_0 and hence the band offset of SiON (φ_{IL}) to silicon conduction-band edge was 2.36 eV [4.8]. Then, a carrier separation method (with source, drain, and bulk all tied to ground) was used. We found that the measured Ig for Vg > 0 is dominated by source/drain current, indicating a tunneling from inversion layer. Measured Ig data from different positions on wafer are given in Fig. 4.2 for two temperatures. It can be seen that only for Vg > 1 V where gate current slightly increases with temperature can the dlnIg/dVg fitting hold; that is, a pure tunneling mechanism dominates therein.

Following the guidelines addressed in Chapter 3 [4.2], both Ig-Vg and dlnIg/dVg-Vg fittings were conducted accordingly. The energy band diagram of the metal-gate/high-*k*/IL/p-substrate MOS system in flat-band condition with the symbols serve as model parameters in calculation is schematically shown in Fig. 4.3. The best fitting results are displayed in Fig. 4.4. The remaining parameters were therefore determined: high-κ band offset φ_k = 1 eV, electron tunneling effective mass in high-κ layer m_k^* = 0.03 m_o, and the electron tunneling effective mass in IL m_{IL}^* = 1.3 m_o.

Obviously, unconventionally low tunneling effective mass, with the same value (0.03 m_o) as in HfSiON layer [4.2], does exist in other materials like HfO_2.

4.3 **Fitting with Transition Layer**

Even with the best fittings as shown in Fig. 4.4, a discrepancy is noticeable, especially in high Vg region. This is the case of a system of two abrupt barriers (one of high-κ and one of IL; see the Fig. 4.3). Additionally, the simulated results in previous chapter (Fig. 3.4) show that no model parameters can effectively adjust the curvature of dlnIg/dVg-Vg at a gate bias range behind the peak position. Thus, we change the structure of the high-κ gate stacks by taking into account a gradual transition (intermixing) layer between HfO_2 and SiON in the calculation. To make a fair comparison, refitting was performed with a transition layer between high-κ and IL. Here, the involved parameters within the transition layer, including permittivity, band offsets, and tunneling effective masses, all varied in a gradual way in terms of a linear and a parabolic distribution, as schematically plotted in Fig. 4.5. In doing so, the transition layer was equally divided into many abrupt-type barriers. The corresponding EOT becomes

$$EOT = t_{IL}\frac{\varepsilon_{ox}}{\varepsilon_{IL}} + t_k\frac{\varepsilon_{ox}}{\varepsilon_k} + \sum_{n=1}^{n=N}\frac{t_{mix}}{N}\frac{\varepsilon_{ox}}{\varepsilon_{mix}(n)} \tag{4.1}$$

where ε_{ox} is the permittivity of SiO_2; t_{mix} is the physical thickness of transition layer; N is the total number of abrupt barriers in transition layer; and $\varepsilon_{mix}(n)$ is the permittivity of n-th abrupt barrier.

The refitting results are shown in Fig. 4.6. Obviously, fitting quality can be improved with the transition layer included, especially for the parabolic one. This can thereby serve as corroborating evidence for the existence of the gradual transition layer. The TEM analysis, as shown in Fig. 7 (a), can support this. Extracted material

parameters are φ_k = 1 eV, m_k* = 0.03 m_o, m_{IL}* = 0.75 m_o, t_k = 0.3 nm, t_{mix} = 1.41 nm, and t_{IL} = 0.5 nm for linear-type transition layer; and φ_k = 1 eV, m_k* = 0.03 m_o, m_{IL}* = 1.46 m_o, t_k = 0.2 nm, t_{mix} = 1.33 nm, and t_{IL} = 0.4 nm for parabolic one. Note that the EOT is maintained at 0.75 nm in the way. In a sense, the total physical thickness is 1.93 nm (the parabolic case, for instance), less than that (2.3 nm) without the transition layer. In other words, if the total physical thickness were the same between each other, then the EOT with the transition layer included would be larger than that with no transition layer. This is consistent with recent experiments [4.4]. Once again, extracted m_k* remains intact. This dictates some unexplained physical mechanisms, which not only are common to both HfO_2 and HfSiON but also are responsible for unconventionally low effective mass in tunneling.

Extra fitting was performed on 1.4-nm EOT TaC/HfSiON/SiON nMOSFETs [4.2] but with the transition layer taken into account. However, this only led to a poor fitting as shown in Fig. 4.8, meaning that the transition layer essentially does not exist in HfSiON/SiON stack. The corresponding evidence in terms of TEM picture is shown in Fig. 7 (b). This is in agreement with the recent claims from the industry [4.6]: (i) a gate dielectric with a graded dielectric constant is produced between silicon oxynitride layer and high-κ layer; and (ii) HfSiON-like materials were not included in the list of high-κ dielectrics associated with the graded layer. Thus, we argue, through this fitting work, that a certain reaction, due to the thermal treatment in the manufacturing process, is active between HfO_2 and SiON whereas for HfSiON/SiON stack, it is unlikely to occur.

Unfortunately, TEM analysis cannot precisely determine the thickness of transition layer due to its limited resolution. To further realize how the transition layer affects the gate tunneling current, three shapes of parabolic transition layer between high-κ layer and IL are considered, as schematically shown in Fig. 4.9. Case I

condition is that a transition layer penetrates both high-κ layer and IL and its simulated results have been shown in Fig. 4.6 (b). Case II condition is that transition layer mainly penetrates IL. Case III condition is that transition layer mainly penetrates high-κ layer. The refitting results corresponding to the three cases are shown in Fig. 4.10, which appear to be excellent, regardless of which case is chosen for parabolic transition layer in high-κ stacks. Extracted material parameters are φ_k = 1 eV, m_k* = 0.03 m_o, m_{IL}* = 1.46 m_o, t_k = 0.2 nm, t_{mix} = 1.33 nm, and t_{IL} = 0.4 nm for Case I; φ_k = 1 eV, m_k* = 0.02 m_o, m_{IL}* = 1.9 m_o, t_k = 1 nm, t_{mix} = 0.95 nm, and t_{IL} = 0.4 nm for Case II; and φ_k = 1 eV, m_k* = 0.07 m_o, m_{IL}* = 1.11 m_o, t_k = 0.2 nm, t_{mix} = 0.88 nm, and t_{IL} = 0.7 nm for Case III. The φ_k is unchanged and m_k* are still the smallest extracted value to date for three cases.

Based on the equation (3.6) and the description of the tunneling mechanism in Fig. 4.11, the $J_{interface}$ can be estimated. Combining direct tunneling current from inversion layer with $J_{interface}$ without considering transition layer, refitting work of experimental gate leakage was performed, as shown in Fig. 4.12. The gate leakage data at a gate voltage range of 0.4-0.8 V support the calculated $J_{interface}$, as shown in Fig. 4.12. The same works with additional $J_{interface}$ in the presence of a gradual linear/parabolic transition layer between high-κ layer and IL were performed as well, as shown in Fig. 4.13 and Fig. 4.14. Perfect reproduction of gate leakage at a gate bias range of 0.4-2.4 V was achieved, especially for the case of parabolic transition layer included in the model.

4.4 Conclusion

We have performed dlnIg/dVg curve fitting on TiN/HfO_2/SiON samples. Several important arguments have therefore been drawn. First, there should be some unexplained physical mechanisms, which not only are common to both HfO_2 and

HfSiON but also are responsible for unconventionally low effective mass in tunneling. Second, a certain reaction, due to the thermal treatment in the manufacturing process, prevails in HfO_2/SiON stack while for HfSiON/SiON case, it is unlikely to occur. Third, by incorporating the $J_{interface}$ in model, the gate leakage at low gate bias range can be adequately explained.

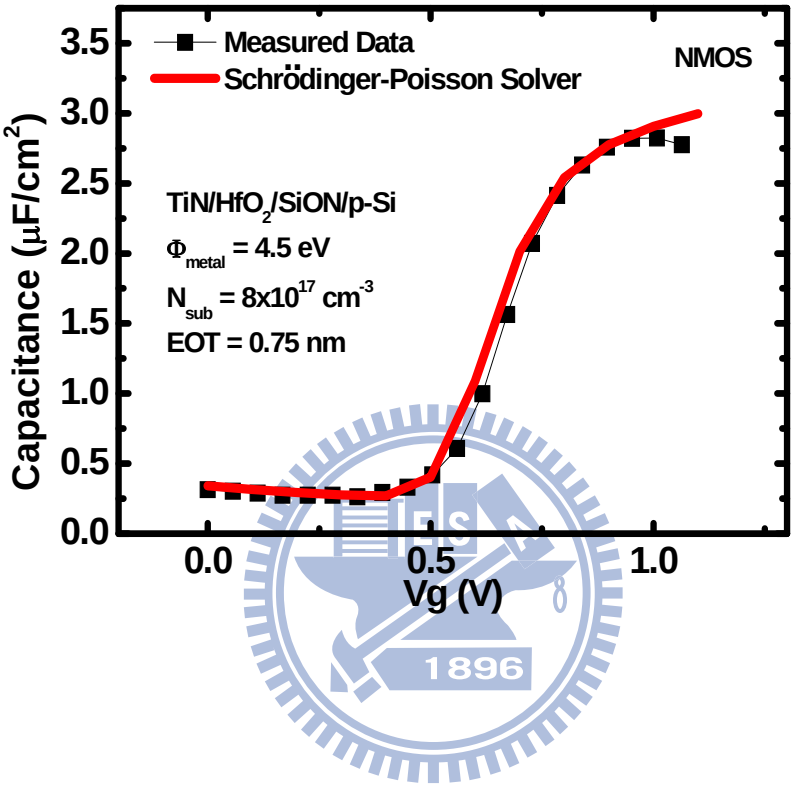


Fig. 4.1 Experimental (symbol) and simulated (line) C_g versus V_g for $TiN/HfO_2/SiON$ gate stacks n-MOSFET. The extrated parameters are: effective oxide thickness EOT = 0.75 nm; substrate doping concentration $N_{sub} = 8\times10^{17}$ cm^{-3}; metal-gate workfunction $\Phi_m = 4.5$ eV.

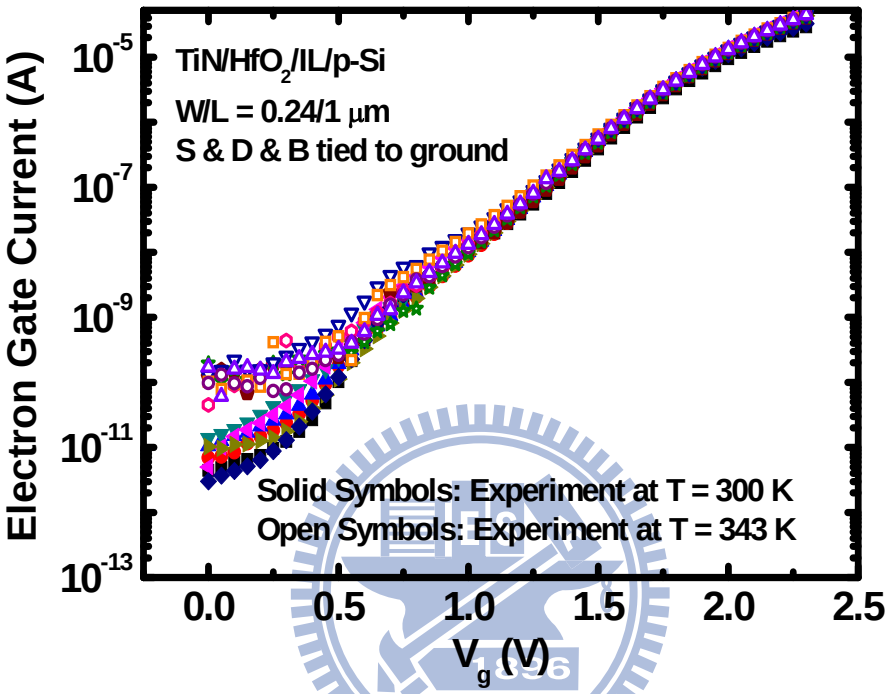


Fig. 4.2 Experimental gate current versus gate voltage data, measured from different positions on wafer, for two temperatures.

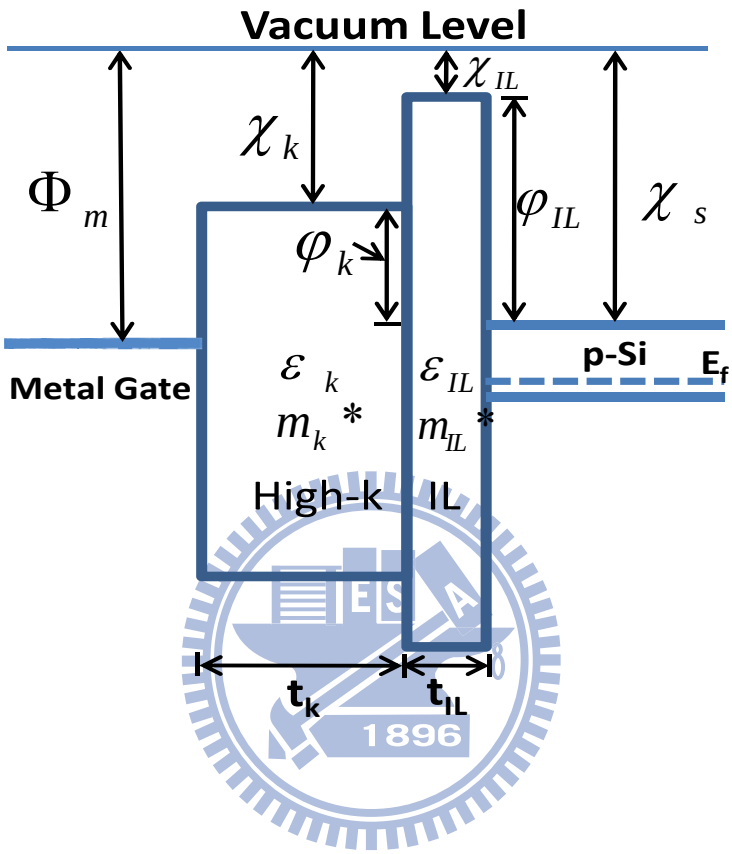


Fig. 4.3 Schematic of the abrupt energy band diagram of a metal-gate/high-κ/IL/Si system for NMOS. The symbols serve as model parameters in calculation.

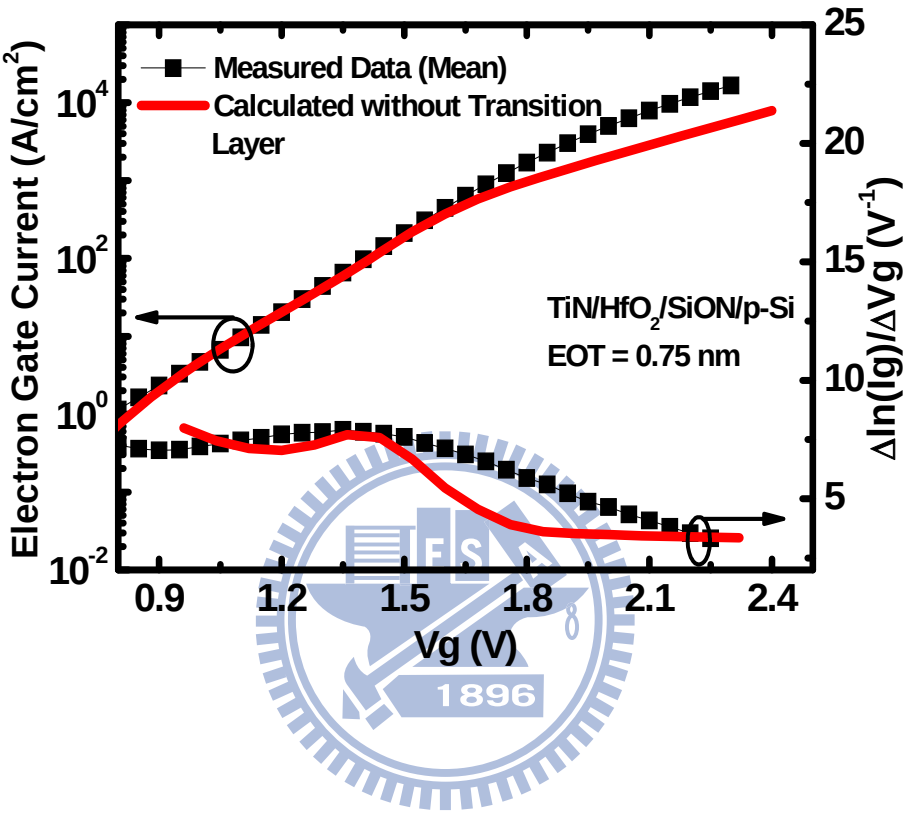
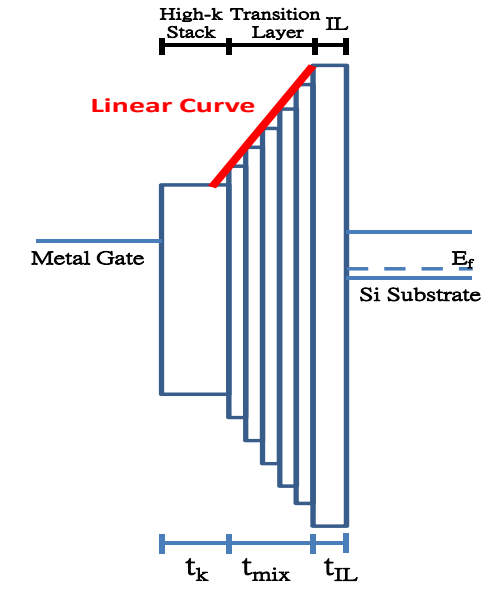
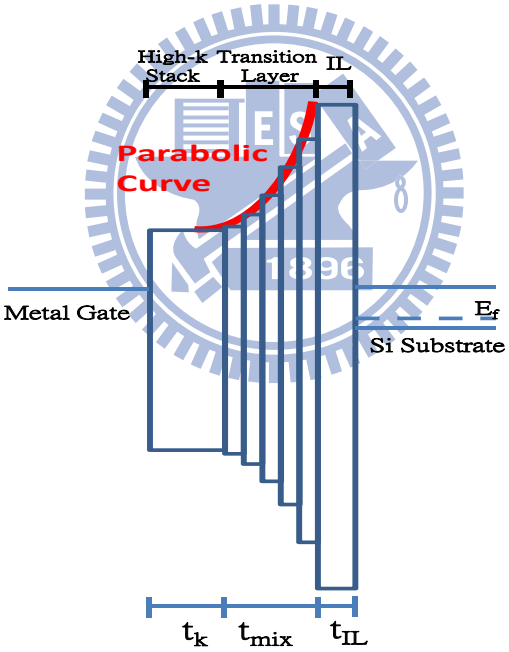


Fig. 4.4 Comparison of experimental (symbols) electron gate current and $dlnI_g/dV_g$ versus V_g with calculated (lines) results. Fitting parameters are $\varphi_k = 1$ eV, $m_k^* = 0.03$ m_o, $m_{IL}^* = 1.3$ m_o, $t_k = 1.4$ nm, and $t_{IL} = 0.9$ nm.



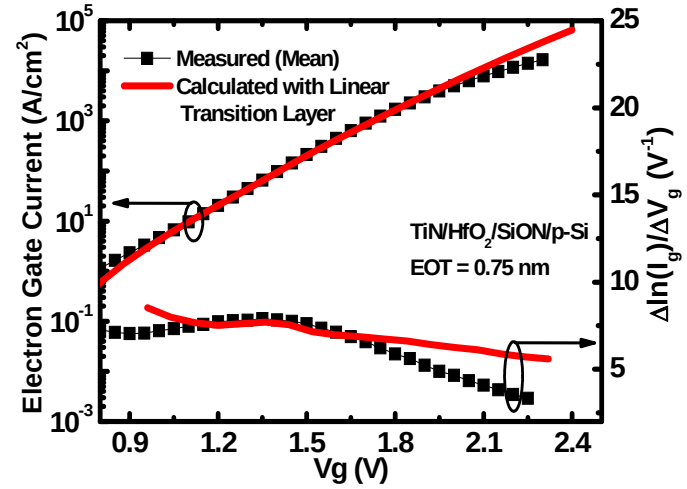
(a)



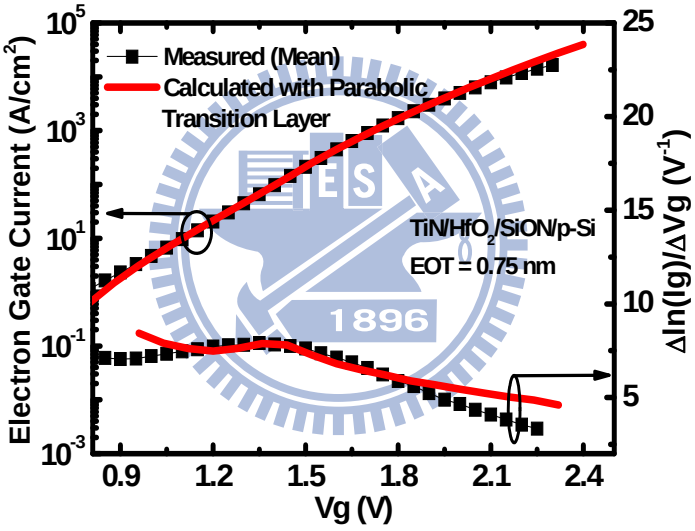
(b)

Fig. 4.5(a) Schematic of the energy band diagram for a linear gradual transition layer.

Fig. 4.5(b) Schematic of the energy band diagram for a parabolic gradual transition layer.



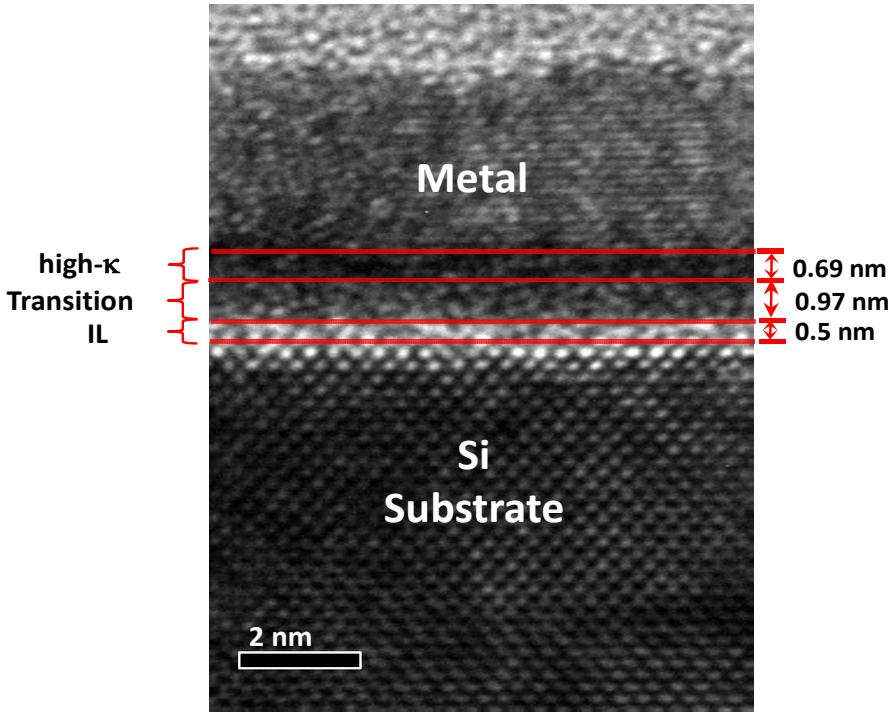
(a)



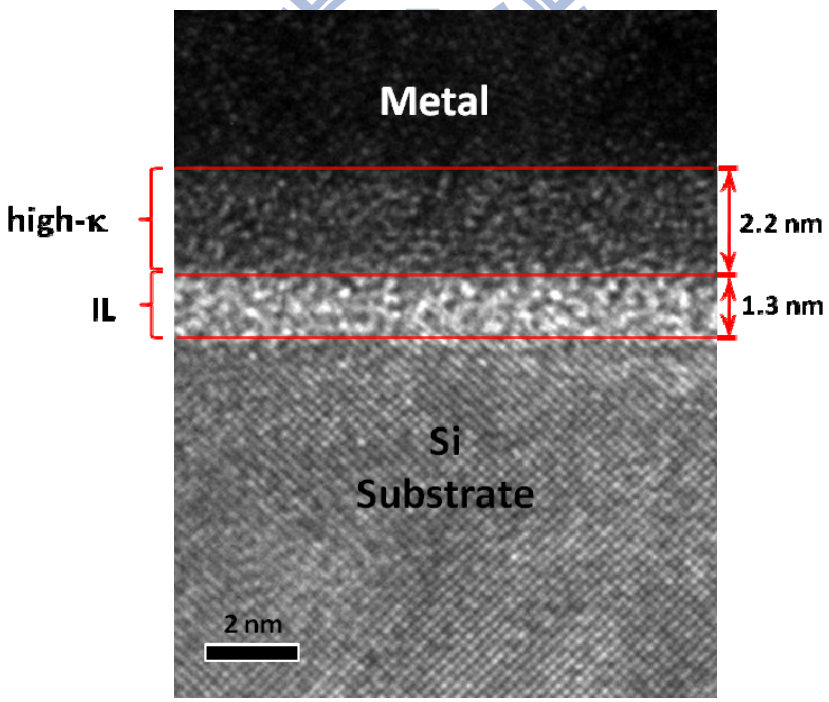
(b)

Fig. 4.6(a) Comparison of experimental (symbols) electron gate current and $d\ln I_g/dV_g$ versus V_g with calculated (lines) results in the presence of a linear transition layer. The same EOT (0.75 nm) is preserved. The fitting parameters are: for linear gradual transition layer, $\varphi_k = 1$ eV, $m_k^* = 0.03\ m_o$, $m_{IL}^* = 0.75\ m_o$, $t_k = 0.3$nm , $t_{mix} = 1.41$ nm, and $t_{IL} = 0.5$ nm.

Fig. 4.6(b) Comparison of experimental (symbols) electron gate current and $d\ln I_g/dV_g$ versus V_g with calculated (lines) results in the presence of a parabolic transition layer. The same EOT (0.75 nm) is preserved. The fitting parameters are: for parabolic gradual transition layer, $\varphi_k = 1$ eV, $m_k^* = 0.03\ m_o$, $m_{IL}^* = 1.46\ m_o$, $t_k = 0.2$ nm , $t_{mix} = 1.33$ nm, and $t_{IL} = 0.4$ nm.



(a)



(b)

Fig. 4.7(a) TEM picture of TiN/HfO_2/SiON gate stacks.

Fig. 4.7(b) TEM picture TaC/HfSiON/SiON gate stacks.

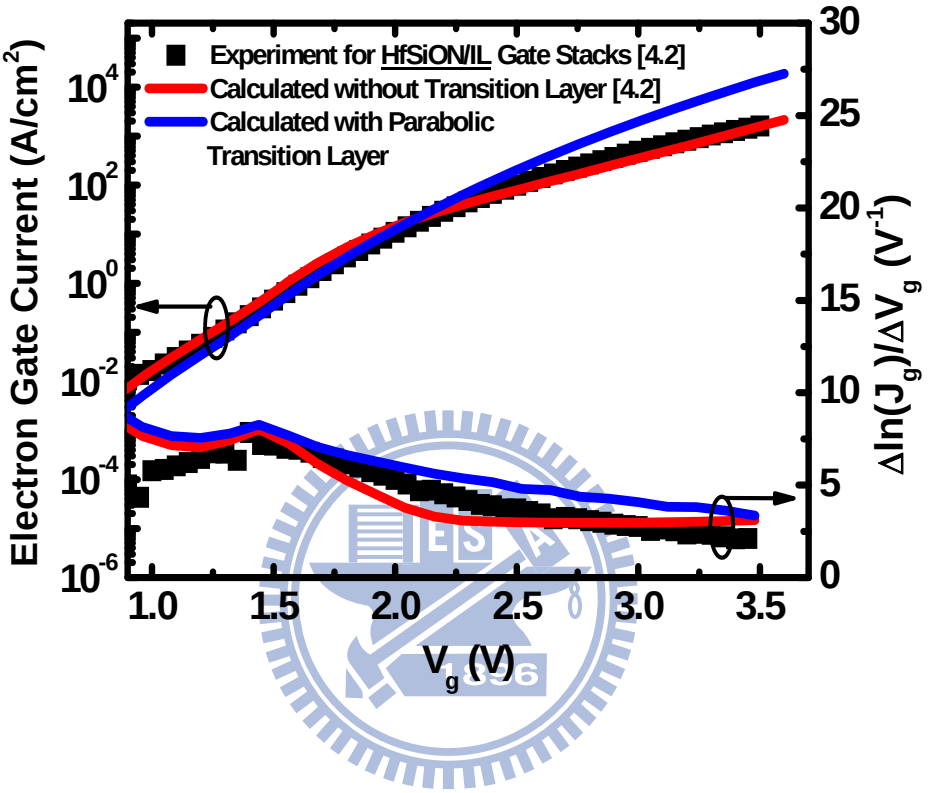
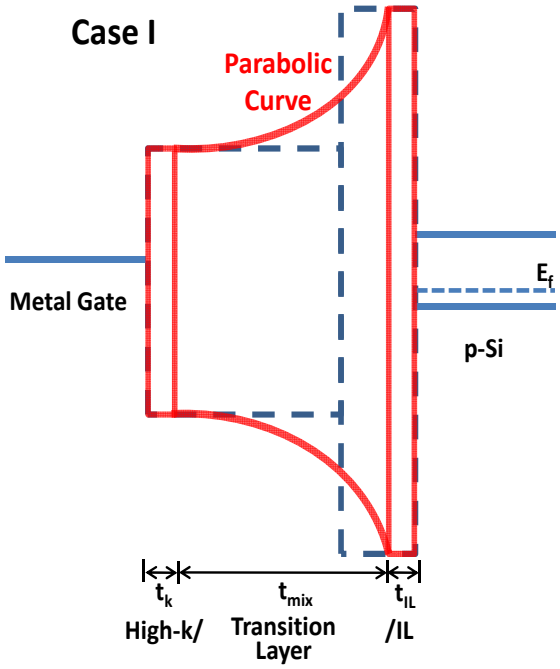
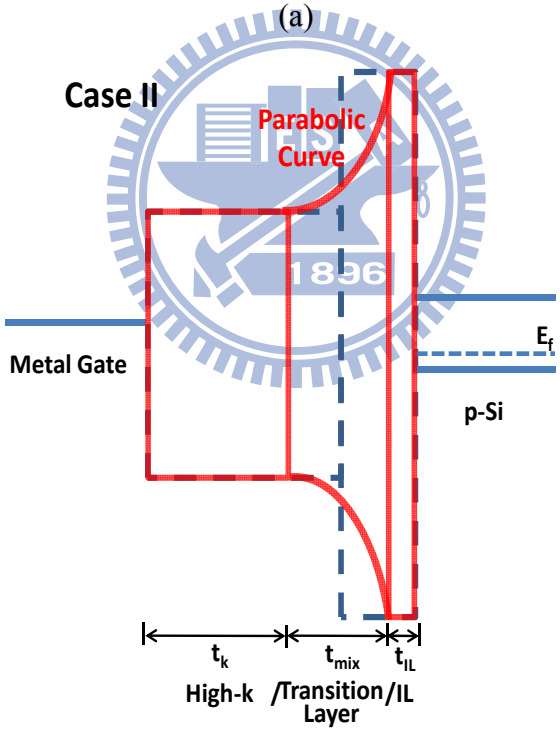


Fig. 4.8 Comparison of experimental (symbols) electron gate current Ig and $d\ln I_g/dV_g$ versus V_g with calculated (lines) results with and without the transition layer. The same EOT (1.4 nm) is preserved. The fitting parameters are: for no transition layer (red lines), φ_k = 1.1 eV, m_k* = 0.03 m_o, m_{IL}* = 0.95 m_o, t_k = 2.2 nm, and t_{IL} = 1.3 nm; for parabolic transition layer (blue lines), φ_k = 1.1 eV, m_k* = 0.02 m_o, m_{IL}* = 1.2 m_o, t_k = 0.5 nm, t_{mix} = 2.1 nm, and t_{IL} = 0.5 nm. Other parameters are the same: Φ_m = 4.48 eV and $N_{sub} = 3\times10^{17}$ cm^{-3}.



(a)



(b)

Fig. 4.9(a) Schematic of the energy band diagram for case I: parabolic transition layer penetrates both high-κ layer and IL.

Fig. 4.9(b) Schematic of the energy band diagram for case II: parabolic transition layer mainly penetrates IL.

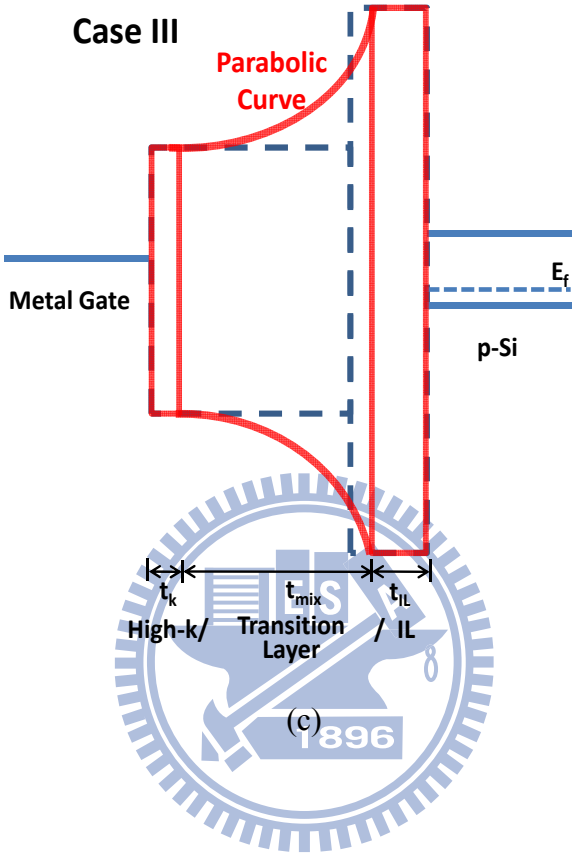


Fig. 4.9(c) Schematic of the energy band diagram for case III: parabolic transition layer mainly penetrates high-κ layer.

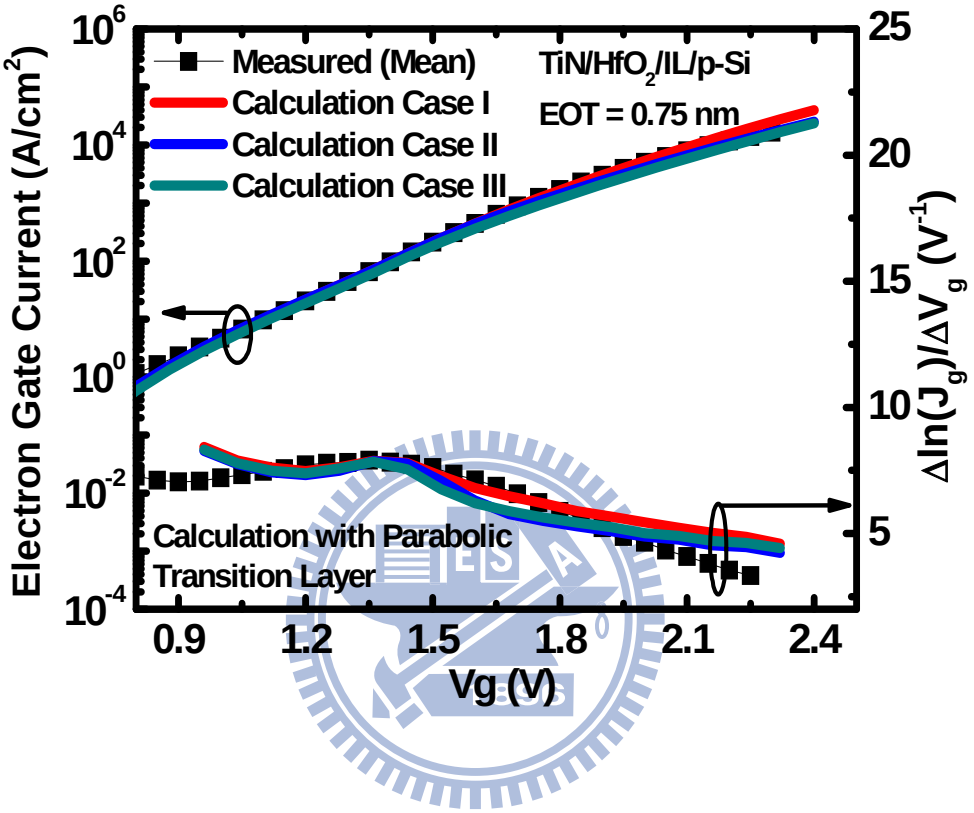


Fig. 4.10 Comparison of experimental (symbols) electron gate current and $d\ln I_g/dV_g$ versus V_g with calculated (lines) results in the presence of three distribution cases of the parabolic transition layer. The same EOT (0.75 nm) is preserved. The fitting parameters are: for case I (red line), $\varphi_k = 1$ eV, $m_k^* = 0.03\ m_o$, $m_{IL}^* = 1.46\ m_o$, $t_k = 0.2$ nm, $t_{mix} = 1.33$ nm, and $t_{IL} = 0.4$ nm; for case II (blue line), $\varphi_k = 1$ eV, $m_k^* = 0.02\ m_o$, $m_{IL}^* = 1.9\ m_o$, $t_k = 1$ nm, $t_{mix} = 0.95$ nm, and $t_{IL} = 0.4$ nm; and for case III (green line), $\varphi_k = 1$ eV, $m_k^* = 0.07\ m_o$, $m_{IL}^* = 1.11\ m_o$, $t_k = 0.2$ nm, $t_{mix} = 0.88$ nm, and $t_{IL} = 0.7$ nm.

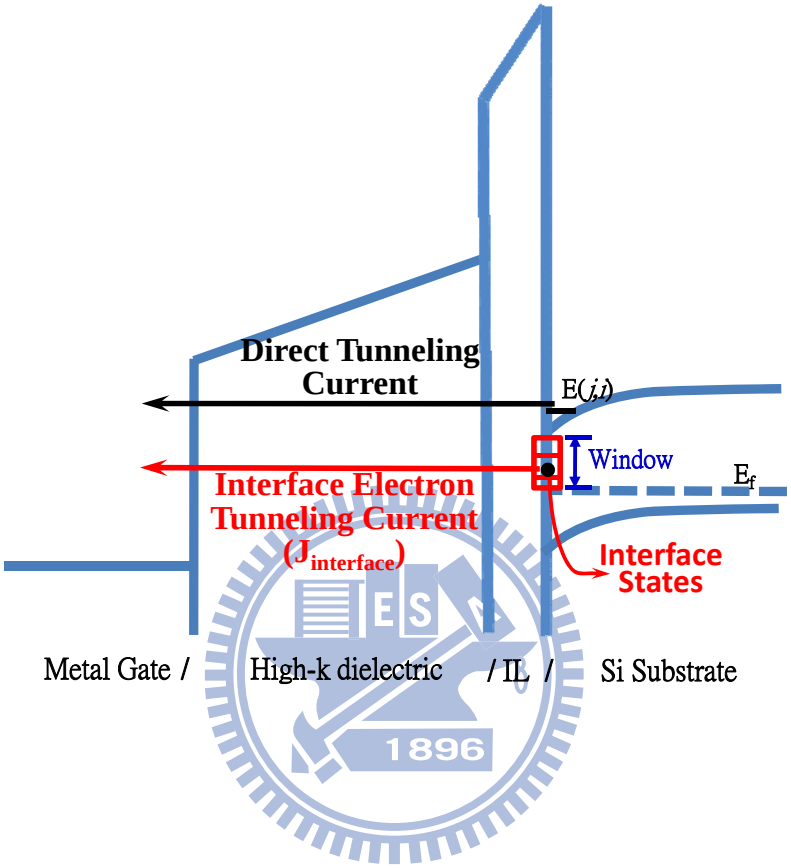
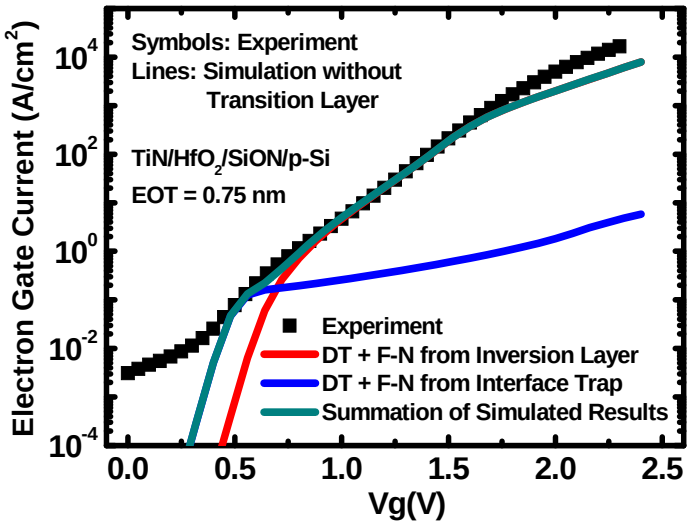
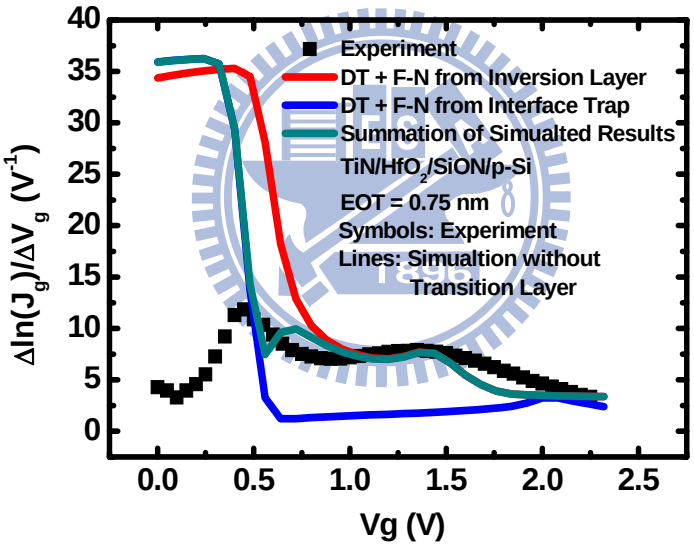


Fig. 4.11 Schematic of energy band diagram showing the mechanism of electron tunneling from IL/Si interface states.



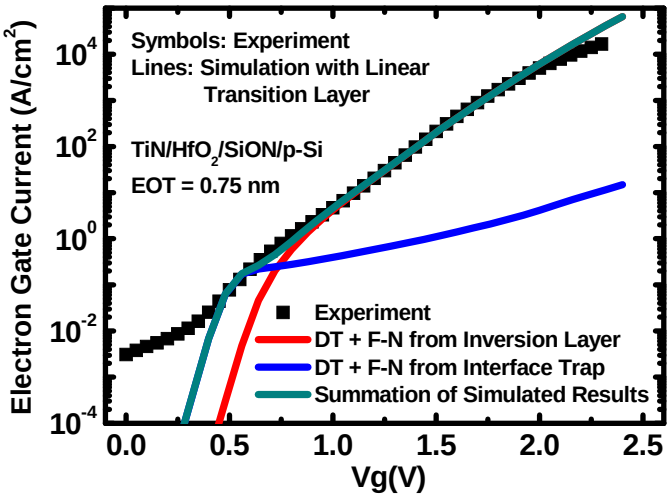
(a)



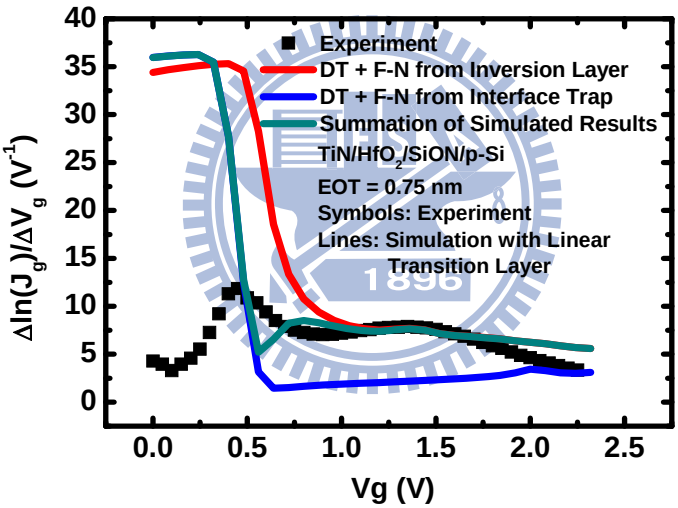
(b)

Fig. 4.12(a) Comparison of experimental data versus Vg with calculated direct (DT) and F-N tunneling current from inversion layer and IL/Si interface states. Summation of both calculated tunneling current components is also shown. Parameters for calculating electron tunneling from interface states are Window = 0.11 eV and $N_{interface}$ = 1.1×10^{20} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 4.4.

Fig. 4.12(b) Comparison of the experimental (symbols) dlnIg/dVg versus Vg with calculated (lines) results of direct and F-N tunneling current from inversion layer and interface states. Parameters for calculating electron tunneling from interface states are Window = 0.11 eV and $N_{interface}$ = 1.1×10^{20} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 4.4.



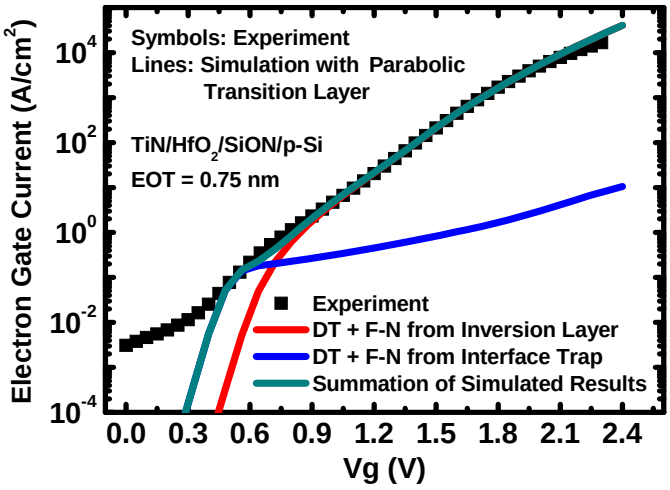
(a)



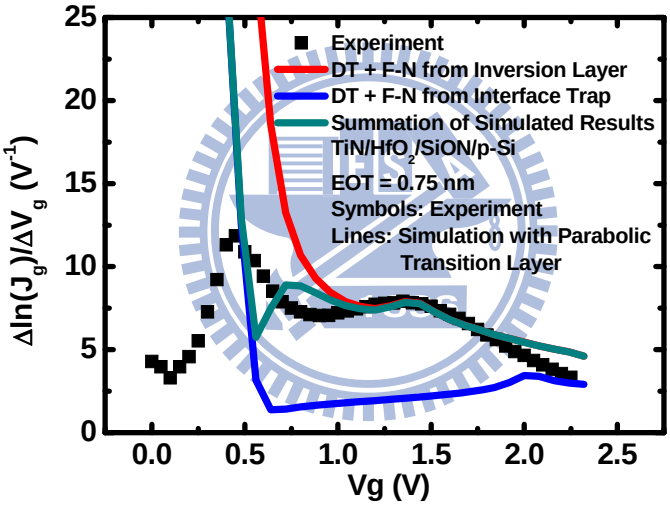
(b)

Fig. 4.13(a) Comparison of experimental data versus Vg with calculated direct (DT) and F-N tunneling current from inversion layer and IL/Si interface states in the presence of a linear transition layer. Summation of both calculated tunneling current components is also shown. Parameters for calculating electron tunneling from interface states are Window = 0.11 eV and $N_{interface}$ = 1.8×10^{20} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 4.6(a).

Fig. 4.13(b) Comparison of the experimental (symbols) dlnIg/dVg versus Vg with calculated (lines) results of direct and F-N tunneling current from inversion layer and interface states in the presence of a linear transition layer. Parameters for calculating electron tunneling from interface states are Window = 0.11 eV and $N_{interface}$ = 1.8×10^{20} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 4.6(a).



(a)



(b)

Fig. 4.14(a) Comparison of experimental data versus Vg with calculated direct (DT) and F-N tunneling current from inversion layer and IL/Si interface states in the presence of a parabolic transition layer. Summation of both calculated tunneling current components is also shown. Parameters for calculating electron tunneling from interface states are Window = 0.11 eV and $N_{interface}$ = 1.8×10^{20} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 4.6(b).

Fig. 4.14(b) Comparison of the experimental (symbols) dlnIg/dVg versus Vg with calculated (lines) results of direct and F-N tunneling current from inversion layer and interface states in the presence of a parabolic transition layer. Parameters for calculating electron tunneling from interface states are Window = 0.11 eV and $N_{interface}$ = 1.8×10^{20} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 4.6(b).

Chapter 5

Comprehensive Modeling of Tunneling Current and its dlnI/dVg in High-k Metal-Gate p-MOSFETs

5.1 Introduction

The poly-Si gate/SiO_2(SiON)/Si system has been replaced by metal gate/high-κ/interfacial layer (IL)/Si system in advanced VLSI technology for the purpose of eliminating the polysilicon depletion and controlling the leakage at acceptable level as EOT scales down [5.1],[5.2]. Hence, it is important to determine the parameters of metal gate/high-κ/IL system such as metal-gate workfunction, band offset of high-κ layer and IL to silicon, tunneling effective mass of high-κ and IL, and EOT. Conventionally, two methods are used to determine these parameters: one is a curve fitting of capacitance versus gate voltage bias (Cg-Vg) and the other is a curve fitting of gate current versus gate voltage bias (Ig-Vg), as reported for high-κ gate stacks n-MOSFETs [5.3]-[5.9] and p-MOSFETs [5.10]-[5.12]. To further accurately extract these parameters, additional work of dlnIg/dVg-Vg curve fitting is needed, as demonstrated in our previous work with the TaC/HfSiON/SiON gate dielectric n-MOSFETs as test device [5.13]. However, the description of the benefit of additional dlnIg/dVg-Vg fitting to extract the parameters for metal gate/high-κ pMOSFETs is still lacking.

The tunneling barrier height seen by electrons in metal gate is usually lower than that seen by electrons in valence band of p^+-poly gate for p-MOSFETs because the Fermi level of metal gate usually locates around mid-gap of silicon in manufacture. Furthermore, tunneling barrier height seen by holes in inversion layer is higher than that seen by electrons in metal gate. Hence, the substrate current (Ib) due to

gate-to-substrate electron tunneling has the opportunity to dominate the overall gate current at inversion condition for metal-gate p-MOSFETs, as will be shown in this work later. To our knowledge, modeling of gate-to-substrate electron tunneling current at inversion condition for metal-gate high-κ p-MOSFETs has not yet been performed in the open literature.

In this work, the calculations of hole gate tunneling current from inversion layer and IL/Si interface states and gate-to-substrate electron tunneling current are conducted. Experimental samples are presented in terms of 1.5 nm-EOT TaC/HfSiON/SiON gate stacks p-MOSFETs and 0.85 nm-EOT TiN/HfO_2/SiON gate stacks p-MOSFETs.

5.2 Physical Model

In this work, five tunneling mechanisms are used to explain the experimental data. The clear descriptions of these tunneling models are presented below.

(i) Direct and F-N tunneling model for high-κ/IL gate stacks p-MOSFETs

The energy band diagram of metal-gate/high-κ/IL/n-Si system in flat band condition is shown in Fig. 5.1. The material and tunneling related parameters in calculation are labeled as follows: Φ_m for metal-gate workfunction; ε_k and ε_{IL} for permittivity of high-κ layer and IL, respectively; t_k and t_{IL} for physical thickness of high-κ layer and IL, respectively; $m^*_{k\_h}$ and $m^*_{IL\_h}$ for hole tunneling effective mass in high-κ layer and IL, respectively; and φ_{k_h} and φ_{IL_h} for valence band offset of high-κ layer and IL to silicon valence band, respectively.

The analytical model of transmission probability (T_{WKB}) through high-κ/IL stacks for n-MOSFETs is described in our previous work [5.13]. The same theory for T_{WKB} calculation can readily apply on metal-gate high-κ p-MOSFETs. Three tunneling cases are included in calculation and the corresponding band diagrams are depicted in

Fig. 5.2. The analytical formula of T_{WKB} for three tunneling cases can read as follows: Tunneling case I ((φ_1(E) > 0, φ_2(E) > 0, φ_3(E) > 0, φ_4(E) > 0)): direct tunneling through both high-κ layer and IL. T_{WKB} is the product of direct tunneling probability for both layers as follows:

$$T_{WKB} = Exp[\frac{4\sqrt{2m^*_{k\_h}}(\varphi_1^{3/2}(E)-\varphi_2^{3/2}(E))}{3q\hbar F_k}]\times Exp[\frac{4\sqrt{2m^*_{IL\_h}}(\varphi_3^{3/2}(E)-\varphi_4^{3/2}(E))}{3q\hbar F_{IL}}] \quad (5.1)$$

Tunneling case II ((φ_1(E) < 0, φ_2(E) > 0, φ_3(E) > 0, φ_4(E) > 0)): direct tunneling through the IL and F-N tunneling occurring in high-κ layer. T_{WKB} is the product of direct tunneling probability for IL and F-N tunneling probability for high-κ layer as follows:

$$T_{WKB} = Exp[\frac{4\sqrt{2m^*_{k\_h}}(-\varphi_2^{3/2}(E))}{3q\hbar F_k}]\times Exp[\frac{4\sqrt{2m^*_{IL\_h}}(\varphi_3^{3/2}(E)-\varphi_4^{3/2}(E))}{3q\hbar F_{IL}}] \quad (5.2)$$

Tunneling case III ((φ_1(E) < 0, φ_2(E) < 0, φ_3(E) > 0, φ_4(E) > 0)): only direct tunneling through the IL. T_{WKB} is direct tunneling probability through IL as follows:

$$T_{WKB} = Exp[\frac{4\sqrt{2m^*_{IL\_h}}(\varphi_3^{3/2}(E)-\varphi_4^{3/2}(E))}{3q\hbar F_{IL}}] \quad (5.3)$$

where φ_1 and φ_2 are tunneling barrier height seen by holes at subband j, vally i for high-κ valence-band sidewall edges; φ_3 and φ_4 are tunneling barrier heights seen by holes at subband j, vally i for IL valence-band sidewall edges; and F_k and F_{IL} are the electric fields in the high-κ layer and IL, respectively.

Then, the hole tunneling current can be calculated:

$$J = q\sum_{i,j} f(j,i) g_{2D} \int_{E(j,i)}^{\infty} F(E) T_{WKB}(E) T_R(E) dE \quad (5.4)$$

where f is the hole impact frequency at the interface of IL/Si; g_{2D} is the 2-dimensional density-of-states per unit area; F is the Fermi-Dirac distribution; T_R is the reflection correction factor at the interface of IL/silicon. The reflection at the interface of

high-κ/IL and metal gate/high-κ is weak and thus is neglected in the calculation.

(ii) Trap-assisted tunneling (TAT) for high-k/IL gate stacks p-MOSFETs

Trap-assisted tunneling model was used to explain the stress-induced leakage current (SILC) for SiO_2/SiON gate dielectric MOSFETs [5.14]-[5.16], as well as the gate leakage current in metal-gate/high-κ MOSFETs [5.17]. Energy band diagram of the metal gate/high-κ/IL/n-Si system for description of the TAT mechanism is shown in Fig. 5.3. The trap-assisted tunneling current can be calculated [5.15]:

$$J_{Steady} = \sigma N_t \frac{J_{in\_trap} J_{out\_trap}}{J_{in\_trap} + J_{out\_trap}} \tag{5.5}$$

$$J_{in/out\_trap} = q \sum_{i,j} f(j,i) g_{2D} \int_{E(j,i)}^{\infty} F(E) T_{WKB\_in/out}(E) T_R(E) dE \tag{5.6}$$

if a hypothetical trap is in IL, the $T_{WKB\_in/out}$ can be modified as:

$$T_{WKB\_in} = Exp[\frac{4\sqrt{2m^*_{IL\_h}}((\varphi_4(E) - F_{IL}x_t)^{3/2} - \varphi_4^{3/2}(E))}{3q\hbar F_{IL}}] \tag{5.7}$$

$$T_{WKB\_out} = Exp[\frac{4\sqrt{2m^*_{k\_h}}((\varphi_t - F_{IL}(t_{IL} - x_t) - (\varphi_{IL} - \varphi_k) - V_{high-k})^{3/2} - (\varphi_t - F_{IL}(t_{IL} - x_t) - (\varphi_{IL} - \varphi_k))^{3/2})}{3q\hbar F_k}] \times Exp[\frac{4\sqrt{2m^*_{IL\_h}}((\varphi_t - F_{IL}(t_{IL} - x_t))^{3/2} - \varphi_t^{3/2}(E))}{3q\hbar F_{IL}}] \tag{5.8}$$

if a hypothetical trap is in high-κ layer, the $T_{WKB\_in/out}$ can be modified as:

$$T_{WKB\_in} = Exp[\frac{4\sqrt{2m^*_{k\_h}}((\varphi_2(E) - F_k(x_t - t_{IL}))^{3/2} - \varphi_2^{3/2}(E))}{3q\hbar F_k}] \times Exp[\frac{4\sqrt{2m^*_{IL\_h}}(\varphi_3^{3/2}(E) - \varphi_4^{3/2}(E))}{3q\hbar F_{IL}}] \tag{5.9}$$

$$T_{WKB\_out} = Exp[\frac{4\sqrt{2m^*_{k\_h}}((\varphi_t - F_k(t_{stack} - x_t))^{3/2} - \varphi_t^{3/2})}{3q\hbar F_k}] \tag{5.10}$$

where J_{in_trap} and J_{out_trap} are the tunneling current density from inversion layer to trap state and the tunneling current density from trap state to gate, respectively; φ_t is trap energy with respect to the valence band of high-κ layer or IL; t_{stack} is the physical

thickness of gate stacks (t_k+t_{IL}); N_t is the trap density; and x_t is the trap distance apart from IL/Si interface.

As the trap located at specific favorable trap position (x_{t_fav}) can contribute maximum TAT current, the equation (5.5) can be approximated as:

$$J_{TAT} = t_{eff}\sigma_c N_t \frac{J_{in\_trap}(x_t = x_{t\_fav})}{2} = t_{eff}\sigma_c N_t \frac{J_{out\_trap}(x_t = x_{t\_fav})}{2} \quad (5.11)$$

where t_{eff} is the effective thickness that the trap-assisted current flow mainly [5.15]; and σ_c is the trap cross section area . The value of t_{eff} is estimated at 0.33 nm and that is independent of gate voltage bias, as reported in [5.15].

(iii) Metal gate-to-substrate electron tunneling current for high-k/IL gate stacks p-MOSFETs

The band diagram of metal/high-κ/IL/n-Si system at inversion condition for description of the gate-to-substrate electron tunneling mechanism is shown in Fig. 5.4(a). The band diagram of metal-gate/high-κ/IL/n-Si system at flat band condition with the labels serving as input parameters is shown in Fig. 5.4 (b). In the figure, φ_{k_e} and φ_{IL_e} are the conduction band offset of high-κ layer and IL to silicon conduction band, respectively; φ_{k_m} and φ_{IL_m} are defined as (φ_{k_e} + (Φ_m-χ_s)) and (φ_{IL_e} + (Φ_m-χ_s)), respectively; $m^*_{k\_e}$ and $m^*_{IL\_e}$ are the electron tunneling mass in high-κ layer and IL, respectively; and a region in IL/Si interface called $Window_{empty}$ allows electron tunneling from metal-gate to occupy. Note that φ_{k_e} can be determined by means of electron tunneling current and its dlnI/dVg fittings at inversion condition for n-MOSFETs.

Based on the study reported by Yang et al. [5.18], the gate-to-substrate tunneling current for high-k metal gate p-MOSFETs can be modified as:

$$J_{MGe} = \frac{4\pi q m^*_{Metal}}{h^3} \int_0^{E_{M\max}} E_M \times T_{WKB}(E_M) dE'_M \quad (5.12)$$

$$T_{WKB} = Exp[\frac{4\sqrt{2m^*_{k\_e}}(\varphi_2^{3/2}(E)-\varphi_1^{3/2}(E))}{3q\hbar F_k}]\times Exp[\frac{4\sqrt{2m^*_{IL\_e}}(\varphi_4^{3/2}(E)-\varphi_3^{3/2}(E))}{3q\hbar F_{IL}}] \quad (5.13)$$

where m^*_M is the effective mass in metal and it is equal to 1 m_0; E_M is defined as the electron energy in metal gate reference to the bottom edge of $Window_{empty}$ and only the electrons in gate with the energy of $E_M>0$ have the opportunity to tunnel from gate to substrate.

(iv) Hole tunneling from IL/Si interface states to metal-gate

In Fig. 5.5, the meaning of "Window" is a local energy region with respect to valence band edge in the forbidden band gap, allowing holes to populate. A simple model for calculating the hole current tunneling from IL/Si interface states ($J_{interface}$) can read as:

$$J_{interface} = qV_{thermal}\int N_{interface}F(E)T_{WKB}(E)dE \quad (5.14)$$

where $V_{thermal}$ is thermal velocity (10^7 cm/s at room temperature); and $N_{interface}$ is interface trap density in "Window" ($cm^{-3}eV^{-1}$) and is used as fitting factor in this work.

With combinations of these tunneling models, the experimental tunneling currents measured from source/drain, gate, and bulk terminals at strong inversion condition for metal-gate high-κ p-MOSFETs can be reproduced well. The details and fitting results are shown later.

5.3 Test Samples

Two presented samples were p-MOSFETs with TaC/HfSiON/SiON and TiN/HfO_2/SiON gate stacks. The material and process parameters for these test devices can be determined by the extraction approach addressed in our previous work [5.13]. One of the test devices is p-channel MOSFET with TiN/HfSiON/SiON gate

stack fabricated in a state-of-the-art process [5.19]. Nominal physical thicknesses of HfSiON (t_k) and SiON (t_{IL}) were 2.2 and 1.3 nm, respectively. Through Cg-Vg fitting, as shown in Fig. 5.6(a), we obtained EOT of 1.5 nm, metal-gate work function Φ_m of 4.48 eV, and n-type substrate doping concentration of 1×10^{17} cm^{-3}. The permittivity of HfSiON (ε_k) was estimated at 12.4 ε_0 [5.19]. To meet EOT = 1.5 nm, the permittivity of SiON (ε_{IL}) was determined to be 6.2 ε_0 and hence the conduction (valence) band offset of SiON to silicon conduction (valence) band edge was φ_{IL_e} = 2.54 (φ_{IL_h} = 3.06) eV [5.20].

Using the same extraction approach, the parameters of TiN/HfO_2/SiON gate stacks p-MOSFETs can further be determined. The corresponding Cg-Vg fitting is shown in Fig. 5.6(b). The parameters for TiN/HfO_2/SiON gate stacks p-MOSFETs are: EOT = 0.85 nm, Φ_m = 4.5 eV, N_{sub} = 6×10^{17} cm^{-3}, t_k = 1.4 nm, and t_{IL} = 0.9 nm. The permittivity of HfO_2 was estimated at 22 ε_0 [5.21]. To meet EOT = 0.85 nm, the permittivity of IL was estimated at 5.8 ε_0 and its corresponding φ_{IL_e} (φ_{IL_h}) was estimated at 2.623 (3.35) eV [5.20]. The effects of the uncertainties in the values of ε_{IL} and φ_{IL}, as well as t_{IL} and t_k, on fitting results can be neglected, as have been demonstrated in our previous work [5.13].

5.4 Experimental and Fitting

(i) TaC/HfSiON/SiON p-MOSFETs

The tunneling current was measured from TaC/HfSiON/SiON p-MOSFETs with the source, the drain, and the substrate tied to the ground. The measured results are shown in terms of the solid symbols in Fig. 5.7. The current detected from drain terminal (Id) is the hole tunneling current and the current detected from substrate terminal (Ib) is the gate-to-substrate electron tunneling current. The gate current is the total tunneling current through the gate stacks. We find that the Ib current dominates

the overall gate current at some range of gate voltage biases. Two reasons can explain this. First, the tunneling barrier height of high-κ layer and IL for hole tunneling is usually higher than that for electron tunneling. Second, the Fermi level of metal-gate usually aligns with the mid-gap of silicon. Thus, the tunneling barrier height seen by electrons in metal gate is much lower than that seen by electrons in p^+-poly gate at strong inversion condition.

Based on the tunneling model described in the section of physical model, the good fittings of Id and its dlnId/dVg versus Vg curves at strong inversion condition are done, as shown in Fig. 5.8. The fitting parameters used for the red fitting line in Fig. 5.8 are φ_{k_h} = 3 eV, $m_{k\_h}^*$ = 0.03 m_0, and $m_{IL\_h}^*$ = 0.67 m_0. Additionally, gate-to-substrate (Ib) tunneling current modeling was performed as well. With the variable $Window_{empty}$ introduced in Fig. 5.4(a), good fitting of Ib is obtained as shown in Fig. 5.9. This result suggests that there are many interface traps, close to conduction band in the Si forbidden gap, having strong ability to allow electron tunneling from metal-gate to occupy. This conclusion about interface traps is self-consistent with the results of $J_{interface}$ dominating the gate leakage at low gate bias for metal-gate high-κ nMOSFETs in previous chapters. The fitting parameters used for best Ib fitting are $\varphi_{k\_m} = \varphi_{k\_e}+(\Phi_m-\chi_s)$ = 1.1+(4.48-4.05) eV, $m^*_{k\_e}$ = 0.03 m_0, $m^*_{IL\_e}$ = 0.95 m_0, and $Window_{empty}$ = 0.1 eV. The parameters used for electron tunneling calculation such as φ_{k_e}, $m_{k\_e}^*$, and $m_{IL\_e}^*$ are based on the values extracted in our previous work for n-MOSFETs with the same gate stacks [5.13]. Other parameters extracted by Cg-Vg fitting hold unchanged for both Id and Ib fittings.

In contrast to our previous work [5.13], no peak is observed in dlnId/dVg-Vg curve due to large valence band offset of HfSiON to silicon valence band. We find at least two sets of parameters that can be used to fit the experimental Id well, as shown in Fig. 5.8. Hence, without the information obtained from a transition between direct and F-N

tunneling in current fitting, the parameters like $\varphi_{k\_e/h}$ and $m^*_{k\_e/h}$ cannot be determined. It suggests that the studies [5.3]-[5.12] to extract the parameters such as $\varphi_{k\_e/h}$ and $m^*_{k\_e/h}$ dealt with only a curve fitting of tunneling current data, which may lead to wrong values of extracted parameters.

We still try to explain the mismatch between experiment Id data and simulated hole tunneling current at low gate bias. The schematic band diagram for description of the mechanism of $J_{interface}$ is shown in Fig. 5.5. The excellent refitting work of experiment (Id) with additional $J_{interface}$ calculated by equation (5.14) was obtained, as shown in Fig. 5.10. Based on the good fitting result, the leakage current at low gate bias is ascribed to $J_{interface}$. Finally, the total current though the gate stack (Ig) is estimated in terms of the summation of calculated Id and Ib. The good fitting results are shown as open symbols in Fig. 5.7.

(ii) TiN/HfO_2/SiON p-MOSFETs

Current separation measurement was performed for TiN/HfO_2/SiON gate stacks p-MOSFETs, as shown in Fig. 5.11. First, we use direct and F-N tunneling current model to fit the experimental hole tunneling current (Id), as shown as black line in Fig. 5.12. However, simulated hole gate current has much stronger Vg dependence than that of experimental data. This suggests that other mechanisms dominate the experimental Id current. In this work, TAT mechanism is used to explain weak Vg dependence in the experiment. With the favorable trap position estimated at 0.6 nm away from interface of IL/Si by means of the calculated tunneling probability versus trap position curve shown in Fig. 5.13, TAT current can be calculated by a simplified equation (5.11). The calculated TAT current result with x_{t_fav} = 0.6 nm, φ_t = 3.35 eV, and $t_{eff}\times\sigma_c\times N_t = 3.3\times10^{-3}$ presents good reproduction of Id at -2.5< Vg < -1 V, as shown as red line in Fig. 5.12. In the figure, φ_t is assumed to be equal to φ_{IL_h} due to its weak effect on TAT current for ultra-thin gate stack; and $t_{eff}\times\sigma_c\times N_t = 3.3\times10^{-3}$ is a

fitting parameter and this value is comparable with another group's result (1×10^{-3}) in the open literature [5.15]. Combining calculated direct and F-N tunneling current with TAT current, the experimental Id for TiN/HfO_2/SiON gate stacks p-MOSFET can be fitted very well at strong inversion condition, as shown as blue line in Fig. 5.12(a). The corresponding dlnId/dVg is also fitted well, as shown in Fig. 5.12(b). The φ_{k_h} = 1.95 eV and $m^*_{k\_h}$ = 0.08 m_0 can be determined accurately by means of the peak horizontal position and peak height of dlnId/dVg-Vg curve, respectively. The ability of dlnI/dVg fitting for accurately extracting the parameters of high-κ layer still works in p-MOSFETs.

The importance of dlnId/dVg-Vg fitting is highlighted in Fig. 5.14. Without considering the dlnId/dVg fitting, a fair good fitting of experiment data is presented with a large test value of φ_{k_h} = 3 eV for the purpose to vanish the F-N tunneling mechanism at a gate bias range of |Vg|<3V, as shown in Fig. 5.14(a). However, the simulated of dlnId/dVg-Vg curves significantly deviate from the experimental data, as shown in Fig. 5.14(b). Hence, for getting the accurately parameters of high-κ layer, extra dlnId/dVg fitting is needed. Additionally, comparing the simulated results in Fig. 5.12 (b) with that in Fig. 5.14(b), we can further confirm that the peak in experimental dlnId/dVg-Vg curve is caused by a transition between direct and F-N tunneling rather than caused by a transition between direct tunneling and TAT.

The gate-to-substrate electron tunneling current fitting for TiN/HfO_2/SiON p-MOSFETs is performed with two different values of $Window_{empty}$, as shown in Fig. 5.15. Again, with non-zero value of $Window_{empty}$, good reproduction of Ib for TiN/HfO_2/SiON gate stacks p-MOSFETs is obtained. The best fitting parameters are: φ_{k_m} = 1+(4.5-4.05) eV, $m^*_{k\_e}$ = 0.03 m_0, $m^*_{IL\_e}$ = 0.85 m_0, and $Window_{empty}$ = 0.15eV.

$J_{interface}$ is used to explain the hole gate leakage (Id) at a low gate bias range that still

cannot be explained by TAT. A complicated and huge work was done, as shown in Fig. 5.16. Combining calculated DT, F-N, and TAT current from inversion layer with $J_{interface}$, an excellent reproduction of complicated experimental Id curve in a wide current range of eight decades is achieved. Both the very large fitting value of $N_{interface}$ (1.1×10^{22} $cm^{-3}eV^{-1}$) and the occurrence of TAT mechanism suggest that the quality of high-κ gate stacks near Si valence band edge is terribly poor. There may be some relation between the large $N_{interface}$ and occurrence of TAT. Finally, combining the simulated results of Id and Ib, the good fitting of experimental Ig is shown in Fig. 5.11. The complete tunneling fittings for TaC/HfSiON/SiON and TiN/HfO_2/SiON gate stacks p-MOSFETs are demonstrated in this work.

In this work, we neglect the effects of the transition layer on tunneling current calculation because the transition layer only affects the gate current at a gate voltage bias behind the F-N tunneling occurrence, as shown in Fig. 5.17. Due to the large band offset of high-κ layer to Si valence band edge for our test samples, the transition layer effect on gate current fitting may be numerically neglected.

5.5 Conclusion

The gate-to-substrate electron tunneling current and hole tunneling current from inversion layer and IL/Si interface states for TaC/HfSiON/SiON and TiN/HfO_2/SiON gate stacks p-MOSFETs are reasonably modeled. The corresponding tunneling physical models are clearly described as well. Combining TAT with $J_{interface}$ models can explain the small Vg dependence of experimental hole tunneling current for fresh TiN/HfO_2/SiON stacks p-MOSFETS. By means of advanced fitting work, $J_{interface}$ is determined to be responsible for experimental hole leakage current at low gate bias for the test devices. The importance of substrate tunneling current in overall gate leakage current for metal gate high-κ p-MOSFETs is highlighted. Finally, with the

additional of dlnI/dVg fitting, we find that the valence band offset of HfSiON to silicon is larger than that of HfO_2.

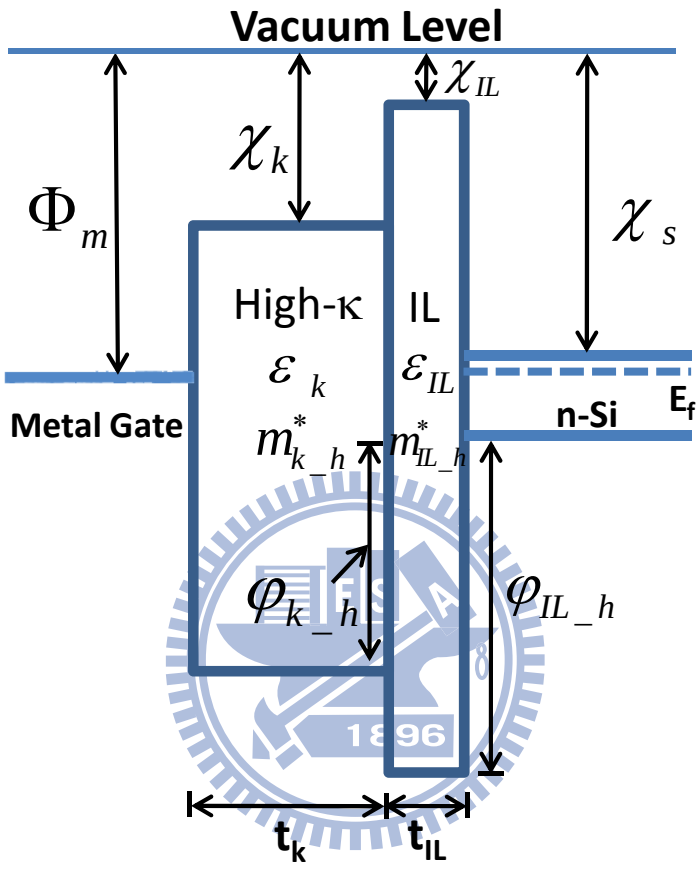
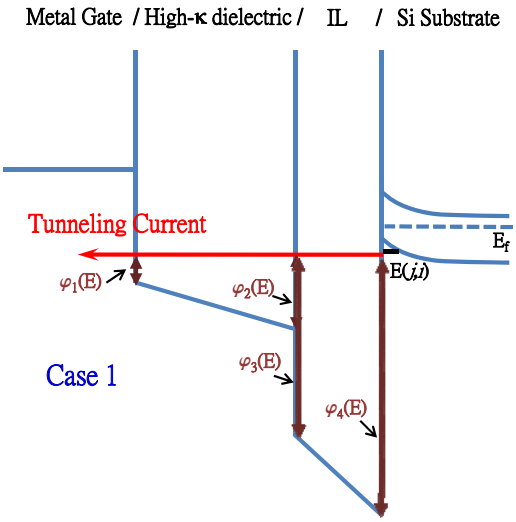
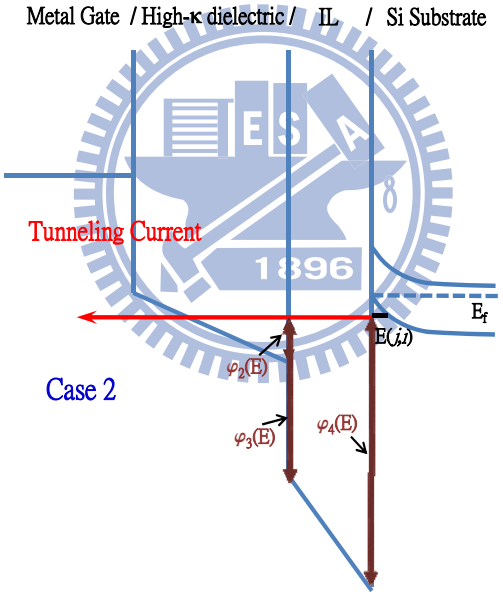


Fig. 5.1 Schematic of the energy band diagram of a metal-gate/high-κ/IL/n-Si system biased in flat-band condition. The process and material parameters for hole tunneling current calculation are labeled.



(a)



(b)

Fig. 5.2(a) Schematic description of tunneling case 1: direct tunneling through both high-κ and IL.

Fig. 5.2(b) Schematic description of tunneling case 2: F-N tunneling occurring in high-κ layer.

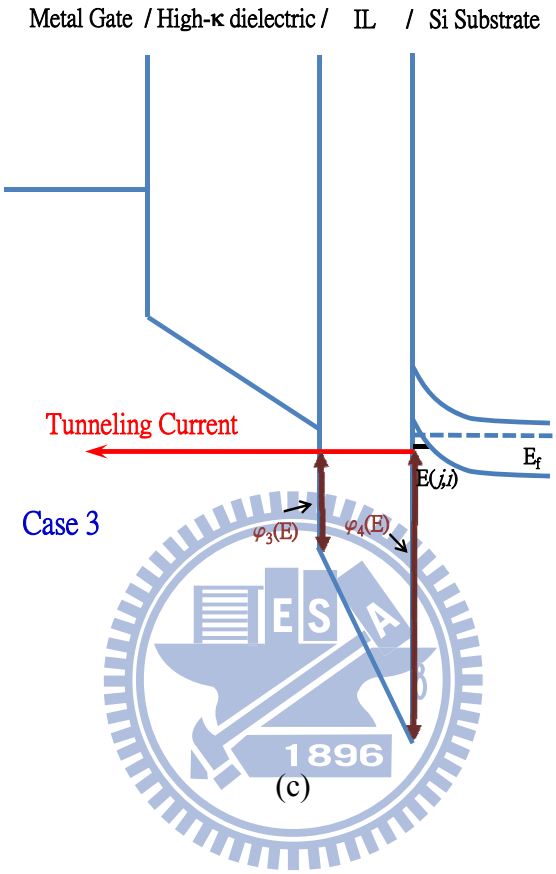


Fig. 5.2(c) Schematic description of tunneling case 3: only direct tunneling through IL.

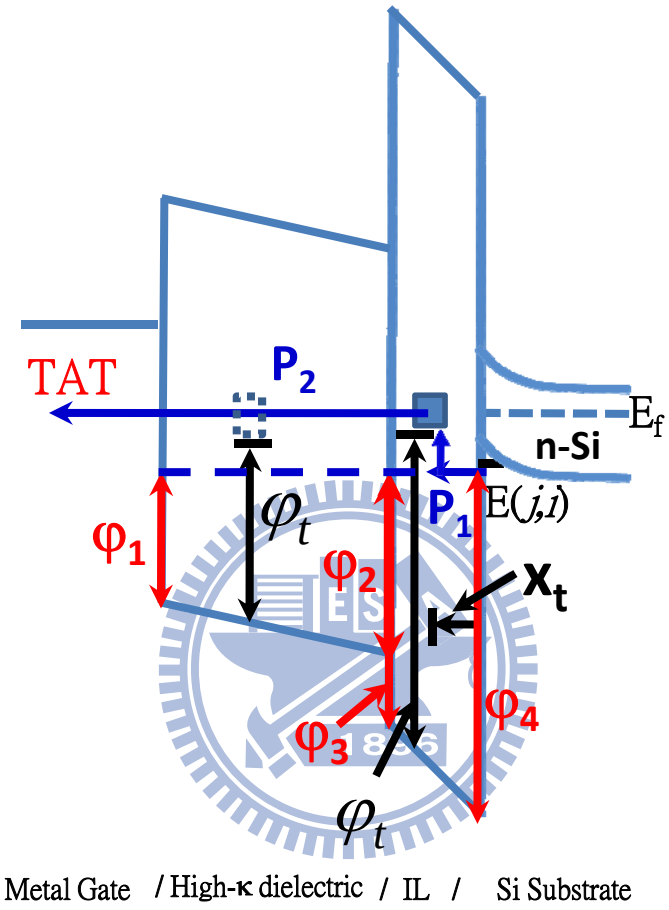
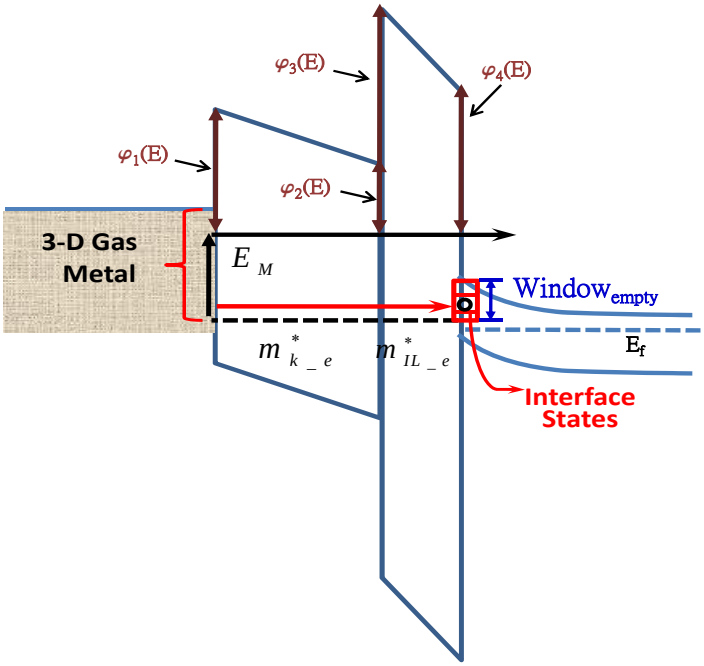
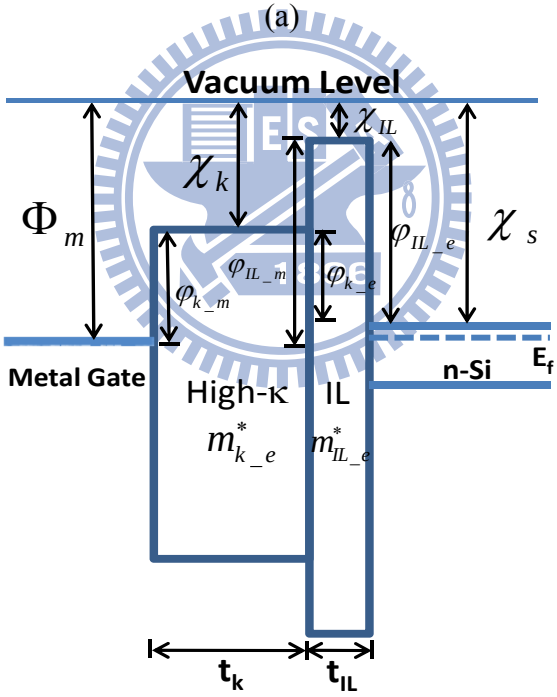


Fig. 5.3 Schematic description of trap-assisted tunneling mechanism. The parameters used for TAT current calculation are labeled.



(a)



(b)

Fig. 5.4(a) Schematic description of gate-to-substrate electron tunneling mechanism. A region called $\text{Window}_{\text{empty}}$ in IL/Si interface allows electron tunneling from metal-gate to occupy.

Fig. 5.4(b) The band diagram of a metal-gate/high-κ/IL/n-Si system biased at flat band condition with the labels of parameters used for gate-to-substrate electron tunneling current calculation.

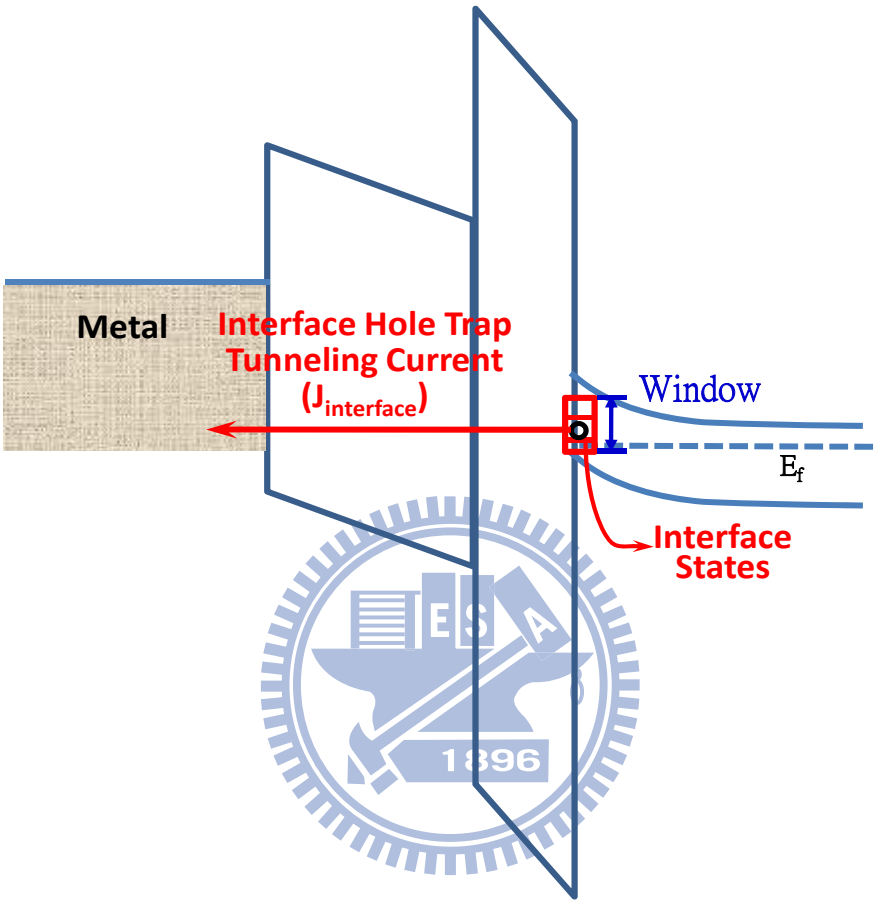
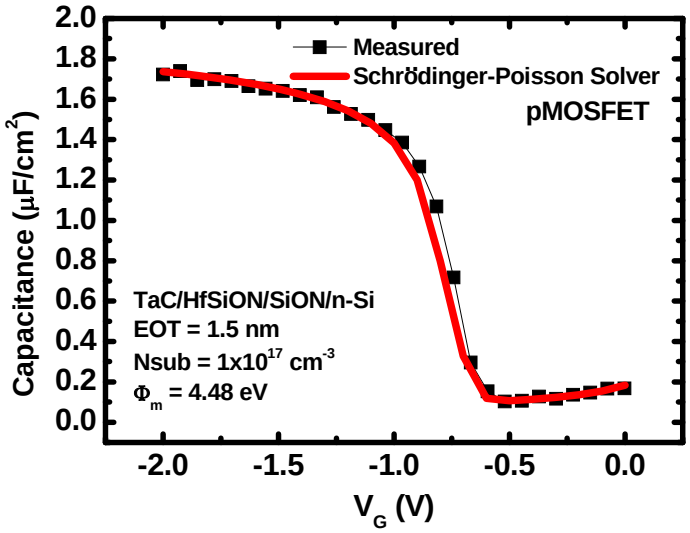
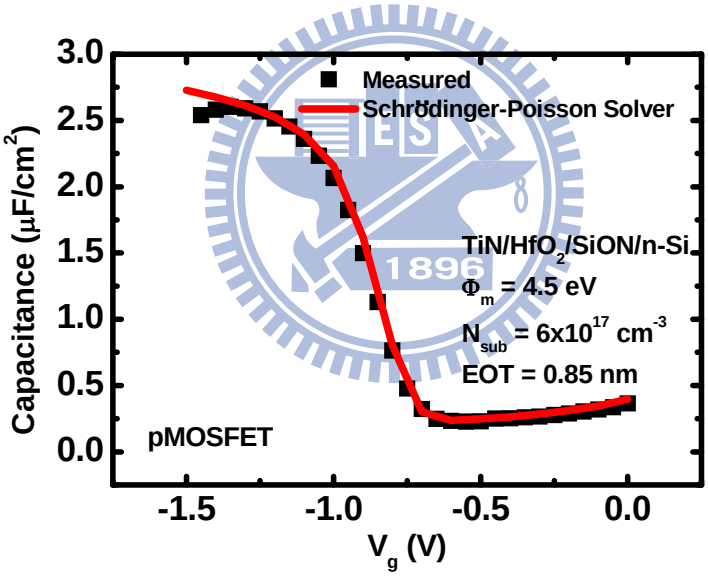


Fig. 5.5 Schematic band diagram showing the mechanism of hole tunneling from IL/Si interface states to metal-gate. A region called Window in IL/Si interface allows hole to occupy.



(a)



(b)

Fig. 5.6(a) Experimental (symbol) and simulated (line) C_g versus V_g for TaC/HfSiON/SiON p-MOSFETs. The extrated parameters are: effective oxide thickness EOT = 1.5 nm; substrate doping concentration N_{sub} = 1×10^{17} cm^{-3}; metal-gate workfunction Φ_m = 4.48 eV.

Fig. 5.6(b) Experimental (symbol) and simulated (line) C_g versus V_g for TiN/HfO_2/SiON p-MOSFETs. The extrated parameters are: effective oxide thickness EOT = 0.85 nm; substrate doping concentration N_{sub} = 6×10^{17} cm^{-3}; metal-gate workfunction Φ_m = 4.5 eV.

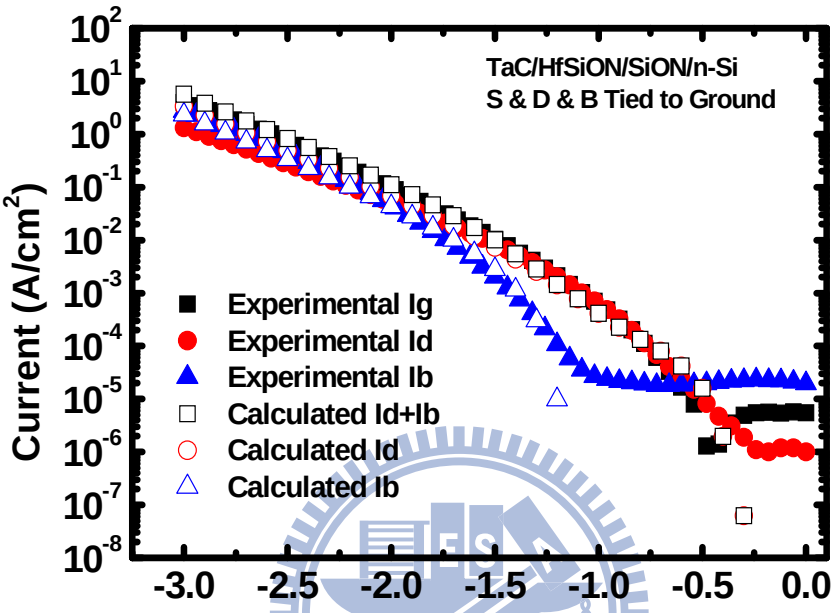


Fig. 5.7 Experimental (solid symbol) and simulated (open symbol) Ig, Id, and Ib versus Vg for TaC/HfSiON/SiON p-MOSFETs. The current are measured with source, drain, and bulk tied to ground.

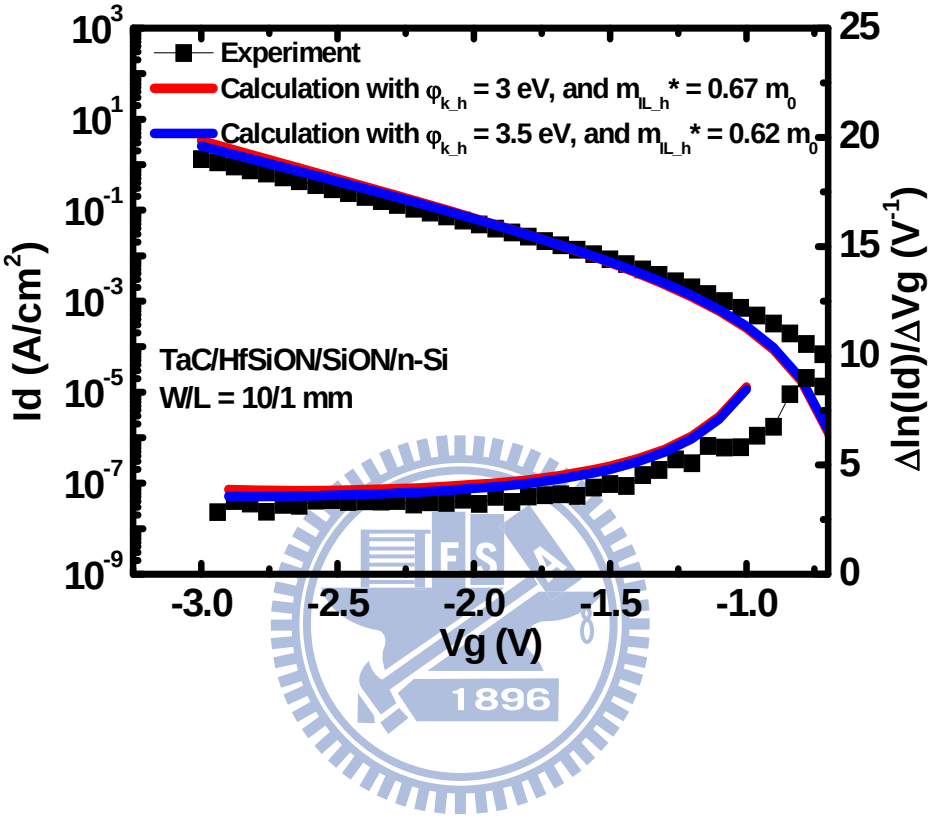


Fig. 5.8 Comparison of the experimental (symbols) hole tunneling current (Id) and dlnId/dV$_g$ versus Vg with calculated (lines) results using two sets of parameters. Parameters for Red Line: φ_{k_h} = 3 eV and $m^*_{IL\_h}$ = 0.67 m_o; and for Blue Line (test): φ_{k_h} = 3.5 eV and $m^*_{IL\_h}$ = 0.62 m_o. Other parameters are $m^*_{k\_h}$ = 0.03 m_o, t_{IL} = 1.3 nm and t_k = 2.2 nm.

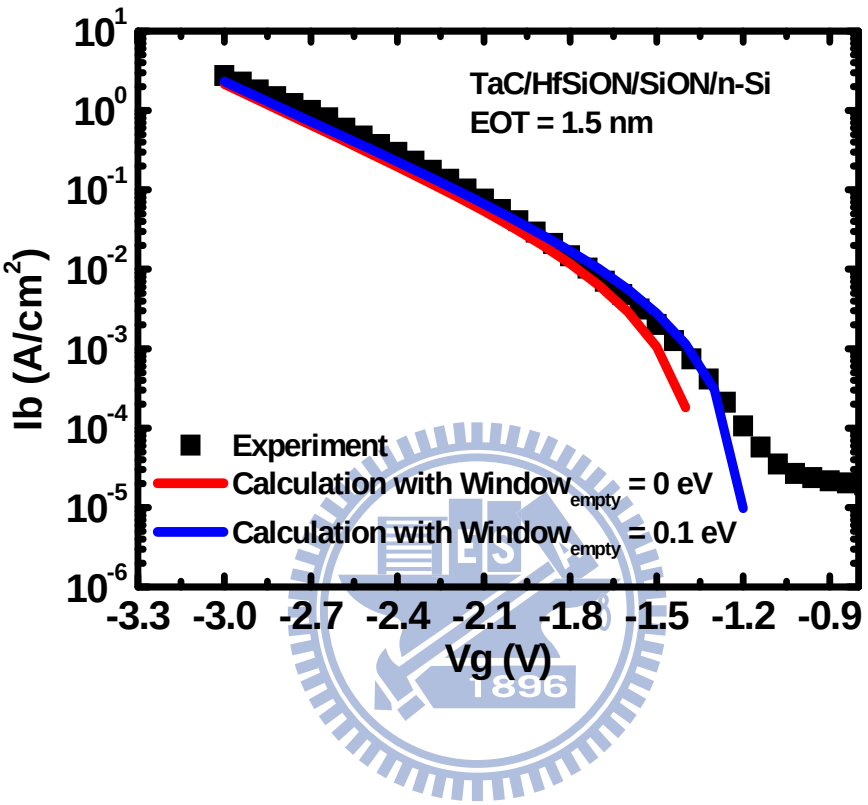
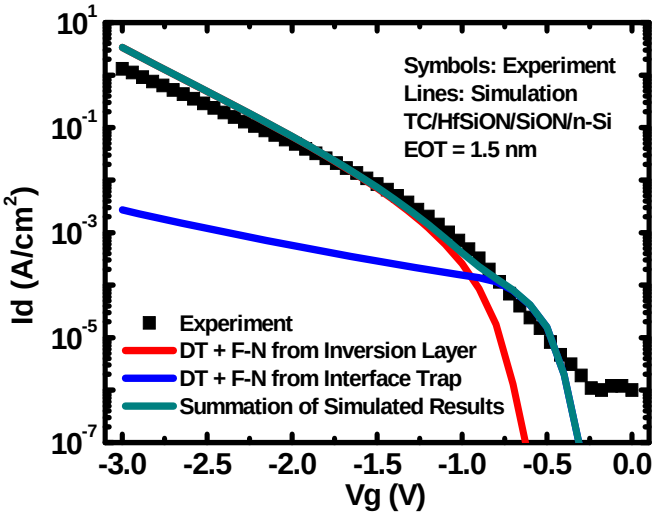
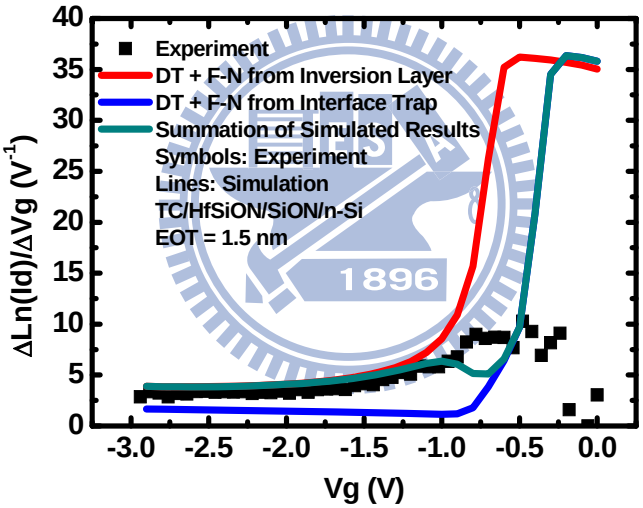


Fig. 5.9 Comparison of the experimental (symbols) gate-to-substrate electron tunneling current (Ib) and dlnIb/dV$_g$ versus Vg with calculated (lines) results for different values of Window$_{empty}$. The parameters used here are: φ_{k_m} = 1.53 eV, $m^*_{k\_e}$ = 0.03 m_0, $m^*_{IL\_e}$ = 0.95 m_o, t_{IL} = 1.3 nm and t_k = 2.2 nm.



(a)



(b)

Fig. 5.10(a) Comparison of experimental data versus Vg with calculated direct (DT) and F-N tunneling current from inversion layer and IL/Si interface states. Summation of both calculated tunneling current components is also shown. Parameters for calculating electron tunneling from interface states are Window = 0.35 eV and $N_{interface}$ = 6×10^{19} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in the red line of Fig. 5.8.

Fig. 5.10(b) Comparison of the experimental (symbols) dlnId/dVg versus Vg with calculated (lines) results of direct and F-N tunneling current from inversion layer and interface states. Parameters for calculating electron tunneling from interface states are Window = 0.35 eV and $N_{interface}$ = 6×10^{19} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in the red line of Fig. 5.8.

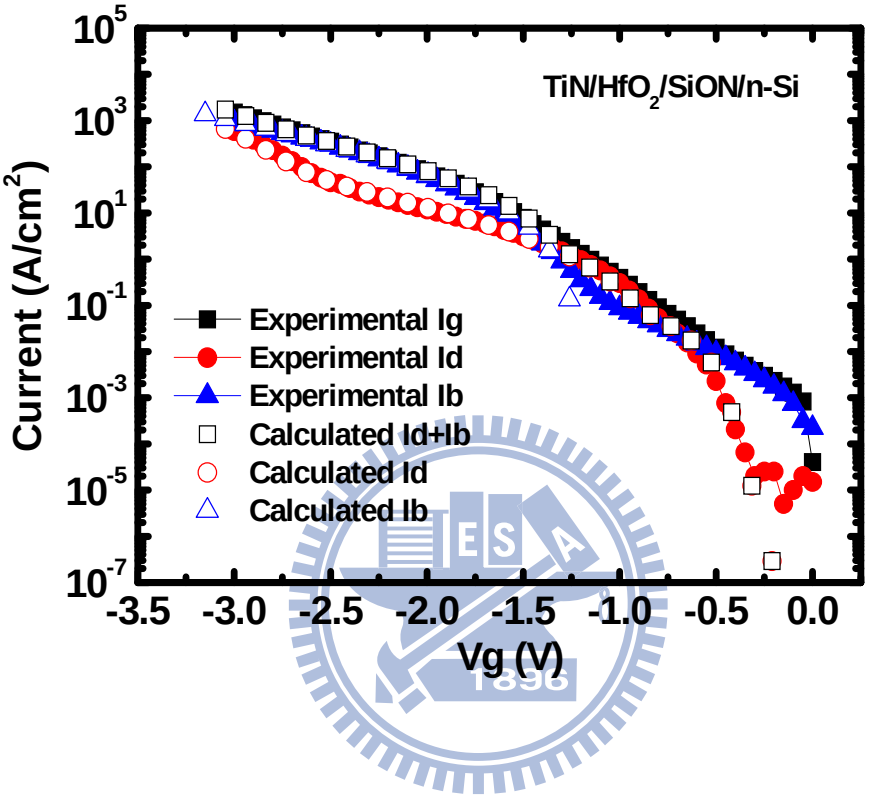
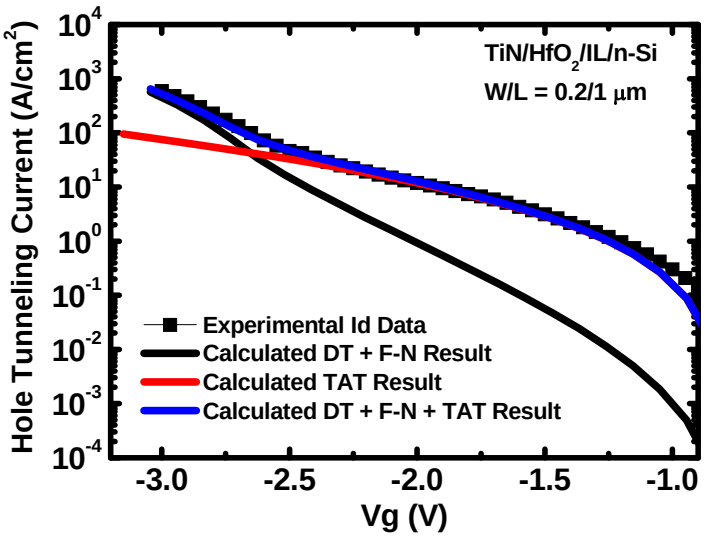
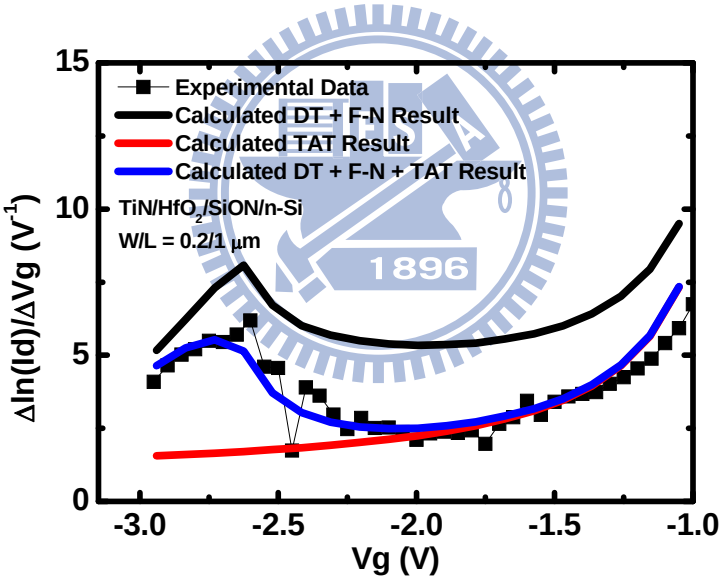


Fig. 5.11 Experimental (solid symbol) and simulated (open symbol) Ig, Id, and Ib versus Vg for TiN/HfO_2/SiON p-MOSFETs. The current are measured with source, drain, and bulk tied to ground.



(a)



(b)

Fig. 5.12(a) Comparison of the experimental (symbols) hole tunneling current (Id) versus Vg with calculated (lines) results of direct tunneling (DT), F-N tunneling, and TAT current. The parameter used in calculation are: φ_{k_h} = 1.95 eV, $m^*_{k\_h}$ = 0.08 m_o, $m^*_{IL\_h}$ = 1.33 m_o, x_{t_fav} = 0.6 nm, $t_{eff}\times\sigma_c\times N_t = 3.3\times10^{-3}$, t_k = 1.4 nm, and t_{IL} = 0.9 nm.
Fig. 5.12(b) Comparison of the experimental (symbols) dlnId/dV_g versus Vg with calculated (lines) results of direct tunneling (DT), F-N tunneling, and TAT current. The parameter used in calculation are: φ_{k_h} = 1.95 eV, $m^*_{k\_h}$ = 0.08 m_o, $m^*_{IL\_h}$ = 1.33 m_o, x_{t_fav} = 0.6 nm, $t_{eff}\times\sigma_c\times N_t = 3.3\times10^{-3}$, t_k = 1.4 nm, and t_{IL} = 0.9 nm.

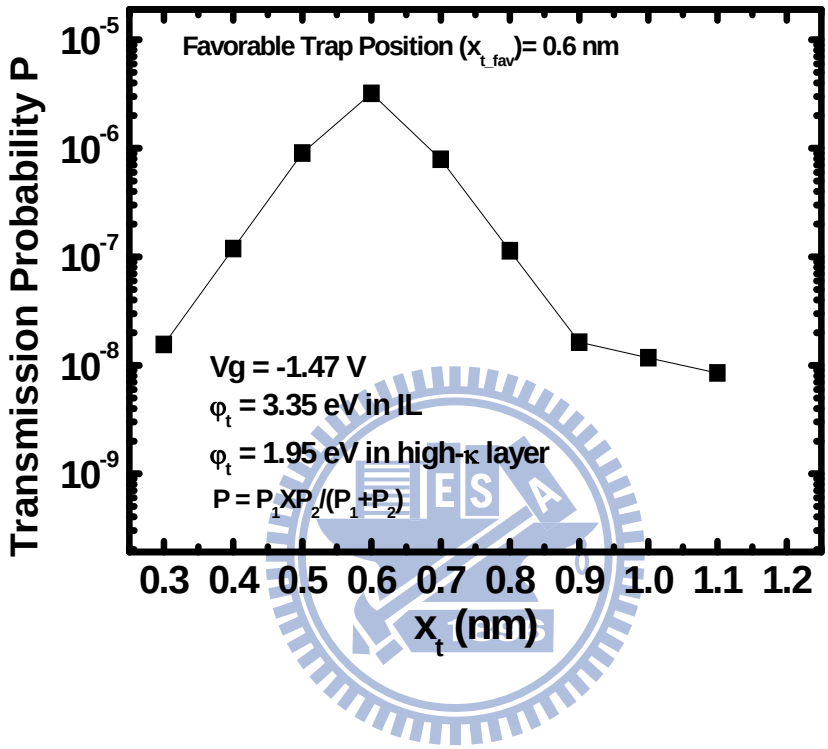
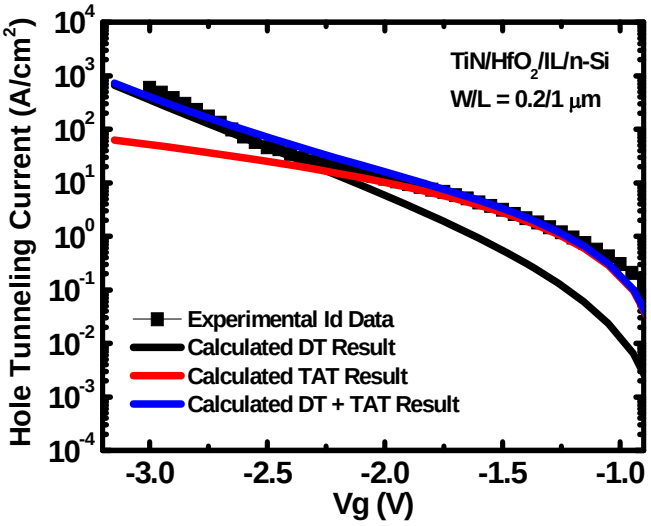
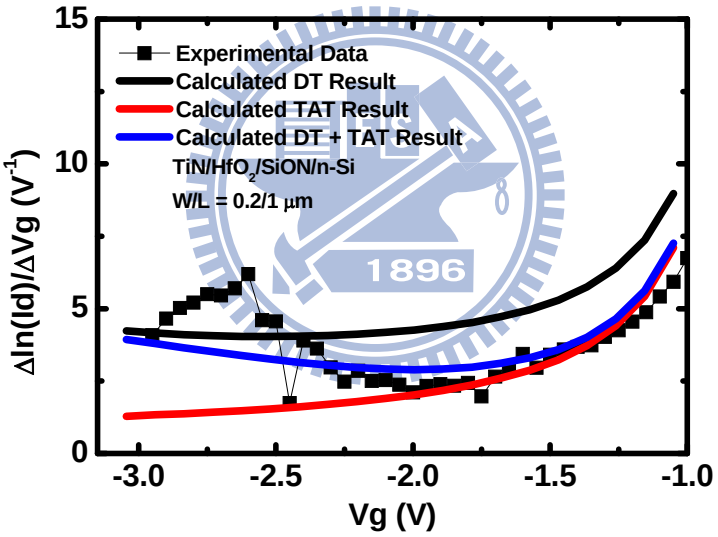


Fig. 5.13 Hole trap-assisted transmission probability though gate dielectric versus trap position (x_t).



(a)



(b)

Fig. 5.14(a) Comparison of the experimental (symbols) hole tunneling current (Id) versus Vg with calculated (lines) results of direct tunneling (DT) and TAT current. The parameters used in calculation are: $\varphi_{k\_h} = 3$ eV, $m^*_{IL\_h} = 0.8\ m_o$, and $t_{eff} \times \sigma_c \times N_t = 1.65 \times 10^{-3}$. Other parameters are the same as those used in Fig. 5.12.

Fig. 5.14(b) Comparison of the experimental (symbols) $dlnId/dV_g$ versus Vg with calculated (lines) results of direct tunneling (DT) and TAT current. The parameters used in calculation are: $\varphi_{k\_h} = 3$ eV, $m^*_{IL\_h} = 0.8\ m_o$, and $t_{eff} \times \sigma_c \times N_t = 1.65 \times 10^{-3}$. Other parameters are the same as those used in Fig. 5.12.

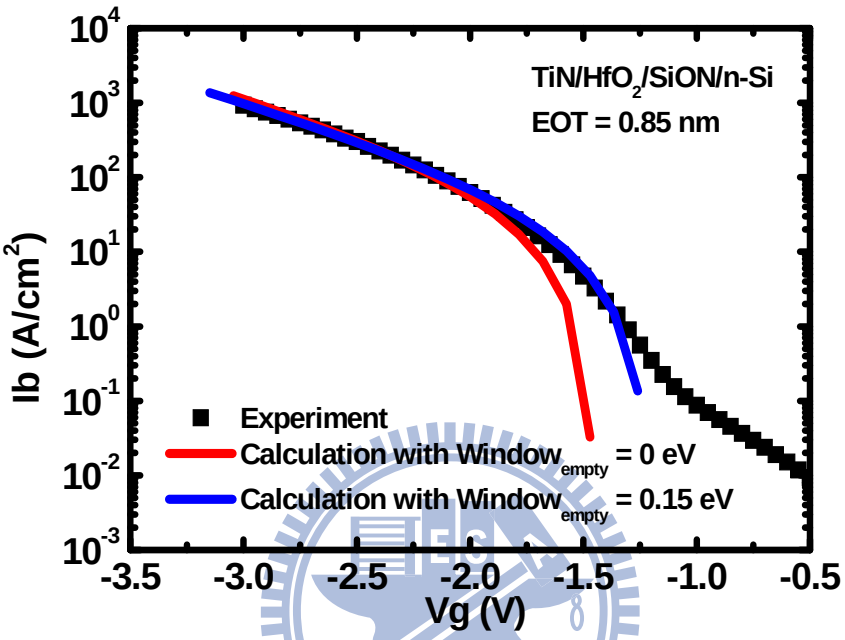
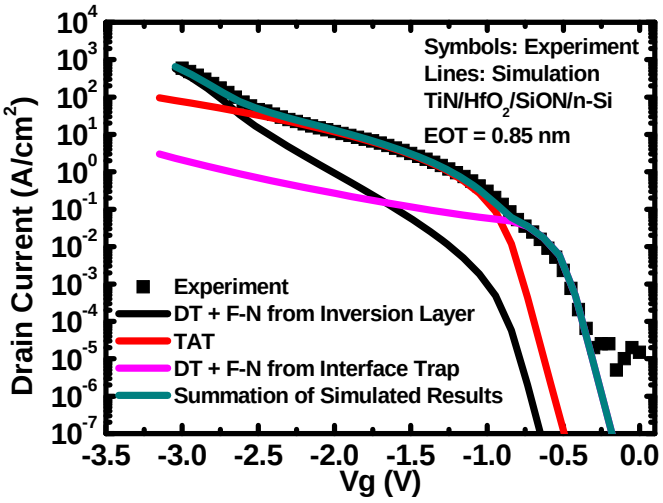
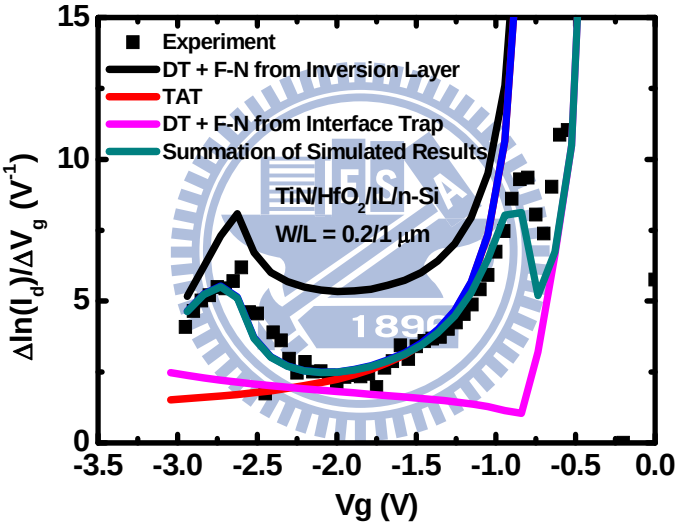


Fig. 5.15 Comparison of the experimental (symbols) gate-to-substrate electron tunneling current (Ib) and dlnIb/dV_g versus Vg with calculated (lines) results for different values of $Window_{empty}$. The fitting parameters are: φ_{k_m} = 1.45 eV, $m^*_{k\_e}$ = 0.03 m_0, $m^*_{IL\_e}$ = 0.85 m_o, t_{IL} = 0.9 nm and t_k = 1.4 nm.



(a)



(b)

Fig. 5.16(a) Comparison of experimental data versus Vg with not only calculated direct (DT) and F-N tunneling current from inversion layer and IL/Si interface states but also calculated TAT current. Summation of all components of calculated tunneling current is also shown. Parameters used in calculating electron tunneling current from interface states are Window = 0.32 eV and $N_{interface}$ = 1.1×10^{22} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 5.12.

Fig. 5.16(b) Comparison of the experimental (symbols) dlnId/dVg versus Vg with calculated (lines) results of direct and F-N tunneling current from inversion layer and interface states and TAT current. Parameters for calculating electron tunneling from interface states are Window = 0.32 eV and $N_{interface}$ = 1.1×10^{22} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 5.12.

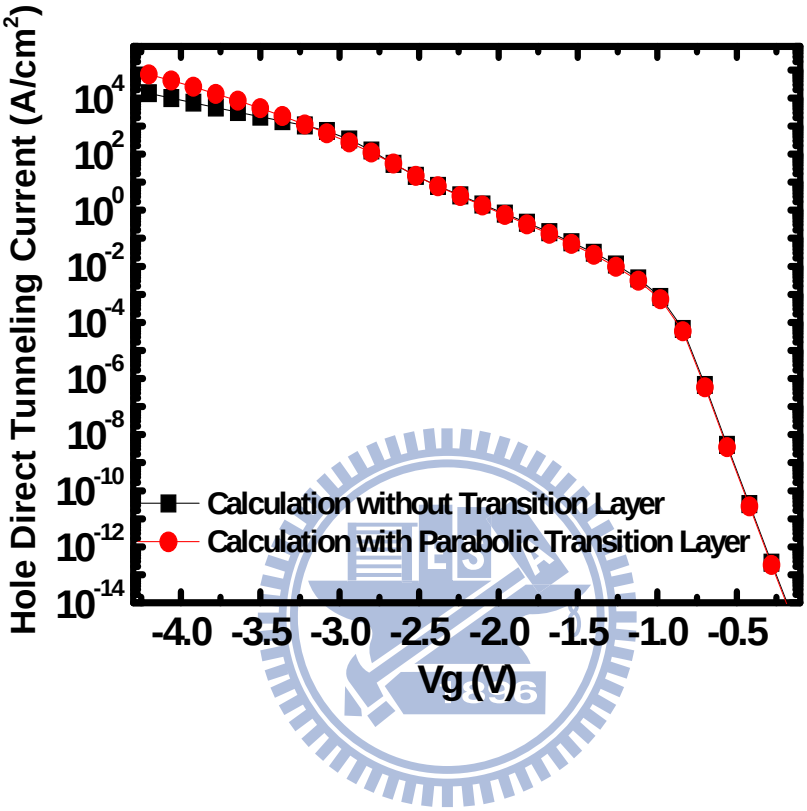


Fig. 5.17 Simulated hole gate tunneling results with/without transition layer versus V_g.

Chapter 6

Combined Experimental Fitting of Cg-Vg, Ig-Vg, and dlnIg/dVg-Vg Curves in High-κ/Metal-Gate FinFETs

6.1 Introduction

While metal-gate high-κ gate stacks are adopted to mitigate the limitation of leakage in device scaling, other issues like short channel effect (SCE), drain induced barrier lowing (DIBL), and mobility degradation caused by high substrate doping are still hard to overcome. A tri-gate structure called FinFET [6.1] shows superior gate control ability over single-gate planar devices. Furthermore, due to its compatibility to the conventional front-end process technology, FinFET is promising in keeping the trend of Moore's law.

From the aspects of the manufacturing process and device physics, it is imperative to experimentally determine gate material parameters in high-*κ*/metal-gate FinFET devices. Conventionally, this can be conducted with two standard electrical methods: a curve fitting of gate capacitance Cg versus Vg and a curve fitting of gate tunneling current Ig versus Vg. More recently, we modified a dlnIg/dVg criterion [6.2], resulting in a new curve fitting around the peak of dlnIg/dVg [6.3]. The guidelines for extra fitting have also been created [6.3]. Underlying gate stack material parameters can therefore be accurately extracted, as has been demonstrated in 1.4-nm EOT TaC/HfSiON/SiON planar bulk n-MOSFETs [6.3].

As for high-*κ*/metal-gate FinFETs, the study to date was limited to the conventional fitting [6.4], not including the dlnIg/dVg one. In this work, we combine Cg-Vg, Ig-Vg,

and dlnIg/dVg-Vg curve fittings on n-FinFETs having 0.8-nm EOT metal/high-κ/IL gate stack. Extracted results are remarkable and can be supported by independent experiments.

6.2 Analytical Model for double-gate structure

Based on triangular potential approximation, a quantum simulator for planar bulk structure has been established and its validity has been proved by excellent gate current reproduction in previous chapters. However, FinFET devices usually have an ultra-thin body structure for the purpose of eliminating SCE and DIBL. The conventional subband energy calculation and estimation of depletion charge density have to be modified. Furthermore, due to the ultra-thin body structure of FinFET, a simulator based on double-gate structure was adopted to characterize and fit the experimental tunneling leakage current of FinFET. The details of the simulator framework for double-gate structure are described as below.

Ultra-narrow double-gate structure induces additional confinement that we call structure confinement. Combining the effects of structure confinement with the field confinement, the subband energy estimation in double-gate structure can read as [6.5],[6.6]:

$$E(j,i) = \left(\frac{\hbar^2}{2m_{zhi}}\right)^{1/3}\left(\frac{3\pi q F_s\left(j-\frac{1}{4}\right)}{2}\right)^{\eta} + \frac{j^2(2\pi\hbar)^2}{8m_{zhi}t_{body}^2} \tag{6.1}$$

where *E(j,i)* represents the energy of the *j*-th subband in the *i*-th valence band; m_{zhi} is the out-of-plane effective mass associated with the *i*-th valence band; F_s is the silicon surface electric field strength; and t_{body} is the distance between two controlled gate stacks. The first term in right hand side is responsible for evaluating field confinement effect. Based on triangular potential approximation, the η is theoretically estimated at 2/3 but it is used as fitting factor in this work. However, the values of η that we

obtained are all close to theoretical value (2/3) even for different subband, as will be shown below. The second term in right hand side is responsible for evaluating structure confinement effect. Those two terms on right hand side of (6.1) are calculated for t_{body} = 10 nm and t_{body} = 20 nm, as shown in Fig. 6.1. In Fig. 6.1, we find that the structure confinement dominates at small gate bias for t_{body} = 10 nm.

The depletion activity is restricted to the small number of dopant in ultra thin double-gate structure. Two depletion conditions, partial and full depletion, are considered in calculation:

$$If\ \sqrt{2q\varepsilon_{Si}N_{sub}\varphi_{depl}(Vg)} > \frac{qN_{sub}t_{body}}{2} \xrightarrow{Full\ Depletion} Q_{depl} = \frac{qN_{sub}t_{body}}{2} \tag{6.2}$$

$$If\ \sqrt{2q\varepsilon_{Si}N_{sub}\varphi_{depl}(Vg)} < \frac{qN_{sub}t_{body}}{2} \xrightarrow{Partial\ Depletion} Q_{depl} = \sqrt{2q\varepsilon_{Si}N_{sub}\phi_{depl}(Vg)} \tag{6.3}$$

where Q_{depl} is depletion charge density; N_{sub} is substrate doping concentration; and $\varphi_{depl}(Vg)$ is potential band bending across depletion region versus gate voltage bias. Equation (6.2) presents full depletion condition, which shows that half of dopants in substrate are totally depleted. Equation (6.3) presents partial depletion condition. Deletion charge density calculations for different t_{body} and N_{sub} are shown in Fig. 6.2. For $N_{sub} = 1\times10^{18}$ cm^{-3}, partial deletion condition only occurs at t_{body} = 50 nm. For $N_{sub} = 2\times10^{18}$ cm^{-3}, partial deletion appears on smaller body thickness (t_{body} = 40 nm) at small gate bias range.

To verify our analytical model for double-gate structure, we comprehensively compare and fit the numerical results [6.7] with analytical ones. With adjusting η factor in (6.1), the analytical model shows good reproduction of numerically calculated subband energies for (110) surface from t_{body} = 10 nm to 50 nm, as shown in Fig. 6.3. The corresponding fitting η factors are labeled in Figures. The surface potential and surface electric field calculated by numerical method are reproduced by analytical model as well, as shown in Fig. 6.4. The independence of η on process

parameters for getting good reproduction of numerical subband energy is shown in Fig. 6.5 and this result confirms that the compact model is reliable once the η for particular t_{body} has been determined. Finally, gate tunneling current calculated with numerical method matches that calculated with analytical method, as shown in Fig. 6.6. Hence, the validity of analytical model for double structure is proved.

Best fitting values of η for different t_{body} are collected in Fig. 6.7. We find that the values of η have linear relation with t_{body} between 10 nm and 50 nm. The corresponding linear fitting equations are also shown in Fig. 6.7. The gate current change of tunneling current calculated with the η obtained by linear fitting equation with respect to that calculated with best fitting values of η versus t_{body} is plotted in Fig. 6.8. Small discrepancy of gate current change between t_{body} = 10 nm and 50 nm is obtained. Hence, with introducing the linear fitting equation of η in calculation, our analytical model not only works well for different process parameters but also performs well for different t_{body}. For extensive discussion, the values of η for (001) surface are collected as well, as shown in Fig. 6.9. Linear relations of η with t_{obdy} between t_{body} = 10 nm and t_{body} = 50 nm are still observed for (001) surface. Additionally, a possible mechanism that a strong interaction of the carriers is controlled by two different gates may cause the linear equation of η breakdown as t_{body} scales from 10 nm to 5 nm, as shown in Fig. 6.7 and 6.9. Hence, the compact model needs more investigation as t_{body} is smaller than 10 nm.

6.3 Experimental and Fitting

N-type FinFETs with 0.8-nm EOT HfO_2 based high-κ/metal-gate on (001) wafer were used for this work. The n-FinFET structure is schematically shown in Fig. 6.10. Gate material parameters are labeled in Fig. 6.11 in terms of the abrupt energy band diagram in flat-band condition. Due to the small ratio of top gate width to fin height,

the FinFET under study can approximately reduce to a double-gate structure.Through Cg-Vg fitting technique, as shown in Fig. 6.12, we obtained effective oxide thickness (EOT) of 0.8 nm, metal-gate work function Φ_m of 4.6 eV and p-type body doping concentration of 1×10^{18} cm^{-3}. The permittivity of HfO_2 (ε_k) is estimated at 22 ε_0 [6.8] and to meet EOT = 0.8 nm, the permittivity of IL (ε_{IL}) is determined to be 6.6 ε_0. Corresponding band offset of IL (φ_{IL}) to silicon conduction band is therefore 2.44 eV [6.9].

As shown in Fig. 6.13, the temperature dependence of experimental Ig of FinFET devices is weak, indicating that direct/F-N tunneling mechanism dominates the gate current. Following the guidelines [6.3], both Ig-Vg and dlnIg/dVg fittings were conducted as demonstrated in Fig. 6.14, valid only for Vg > 1 V. This leads to φ_k = 1.1 eV, m_k^* = 0.02 m_o, and m_{IL}^* = 1.22 m_o. Note that a serious deviation occurs at high Vg. Thus, we further took into account a transition (intermixing) layer between high-κ and IL. The experiments in the open literatures [6.10],[6.11] in terms of the TEM analysis, as shown Fig. 6.15, can support this. The refitting results are shown in Fig. 6.16. Obviously, fitting quality can be improved with the transition layer included, especially for the parabolic one. In this case, the permittivity, band offsets, and tunneling effective masses of transition layer vary in linear or parabolic type, as schematically plotted in the inset of Fig. 6.16. For the first time, the combination of Cg-Vg, Ig-Vg and dlnIg/dVg-Vg fittings can thereby serve as corroborating evidence for the existence of the transition layer. Note that the extracted values of φ_k and m_k^* were kept unchanged in extra fitting. The reasons are that the height of dlnIg/dVg peak and its Vg position are most sensitive to m_k^* and φ_k, respectively, according to fitting guidelines [6.3].

Here we want to stress that in the presence of transition layer, the conventional approach with no dlnIg/dVg fitting leads to poor reproduction as shown in Fig. 6.17.

The corresponding material parameters are therefore incorrect. Thus, the tunneling effective masses in hafnium dioxide and hafnium silicate in the literature [6.4],[6.8],[6.12]-[6.17], which were obtained using the conventional method only, were all overestimated. As depicted in Fig. 6.18, the correct tunneling effective masses, due to the incorporation of dlnIg/dVg fitting, should lie at around 0.02 m_o, the minimum value to date.

The model suitable for double gate structure for calculating electron tunneling current from IL/Si interface states has been constructed and the picture of this mechanism is shown in Fig. 6.19. Calculated $J_{interface}$ reproduces the gate leakage of FinFET at low gate voltage bias even without considering the transition layer in high-κ stacks, as shown in Fig. 6.20. Summation of calculated direct tunneling current from inversion layer and interface states in the presence of a linear/parabolic gradual transition layer in high-κ gate stacks is shown in Fig. 6.21. Excellent reproduction of electron gate tunneling leakage versus Vg in a wide range of six decades for FinFET devices is obtained, especially for the case of parabolic transition layer included in model.

Using (3.7) and (3.8), the experimental substrate current due to valence band electron tunneling can be calculated, as shown by a red line in Fig. 6.24. However, the turn-on voltage of simulated valence band electron tunneling current is much larger than that of experimental data. One idea is used to explain the deviation between experimental Ib and simulated result. As schematically shown in Fig. 6.25, we assume that an energy region called window sitting above valence band edge allows extra valence electron tunneling through gate stacks. With Window = 0.21 eV, the fitting quality can be improved, as shown as blue line in Fig. 6.24. Hence, based on good fitting result under the assumption of extra electron tunneling current from the region in forbidden band gap close to valence band edge, we suggest that the interface

quality of gate stack around valence band edge is poor.

6.4 Extra Evidence

Further, C-V curve fitting for planar devices on the same wafer was performed, as shown in Fig. 22. The discrepancy from experimental data is due to large leakage current for large area of planar test device used. However, the fitting can still be performed near the turning point of C-V curve (around Vg = 1 V) in Fig. 6.22 while keeping the same EOT and Φ_m as the FinFET devices under the same process flow of gate stacks. The resulting N_{sub} is slightly increased relative to FinFET one.

Without changing the material parameters φ_k, m_k*, and m_{IL}* obtained in Fig. 6.16 (b), experimental gate tunneling current from planar devices is well modeled, as shown in Fig. 6.23. This further confirms the validity of our proposed fitting approach. To hold the same m_{IL}* for the fitting of planar devices, the t_{IL} must slightly change from 0.59 nm to 0.54 nm. This points out the fact that the oxidation rate on (001) surface is slightly slower than that of (110) surface even in ultrathin oxide or oxynitride.

6.5 Conclusion

A compact analytical model for double-gate structure has been established. Due to small ratio of top gate width to Fin-height for our FinFET test samples, we find that I-V and C-V characteristics of FinFET device can be described by a simulator based on doubel-gate structure. This simulator in combination with analytical model for double-gate structure has been verified experimentally in this work.

Combination of Cg-Vg, Ig-Vg, and dlnIg/dVg-Vg curve fittings has been established. The merits of determining gate material parameters in high-κ/metal-gate FinFETs, more accurately and in greater detail, have been justified. The results

obtained may provide relevant information for the manufacturing process analysis and device physics oriented study. Furthermore, we have argued that the physical origin of gate leakage current at low gate bias is attributed to electron tunneling from IL/Si interface states to metal electrode.

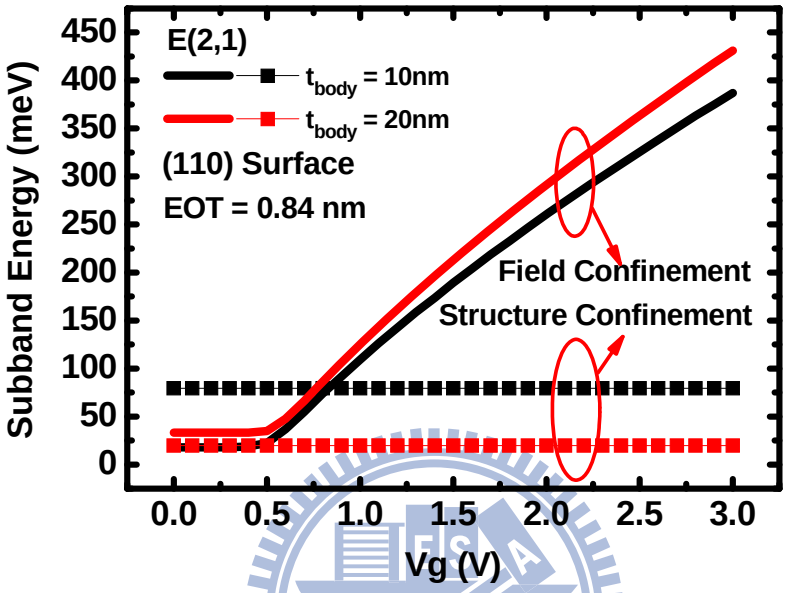
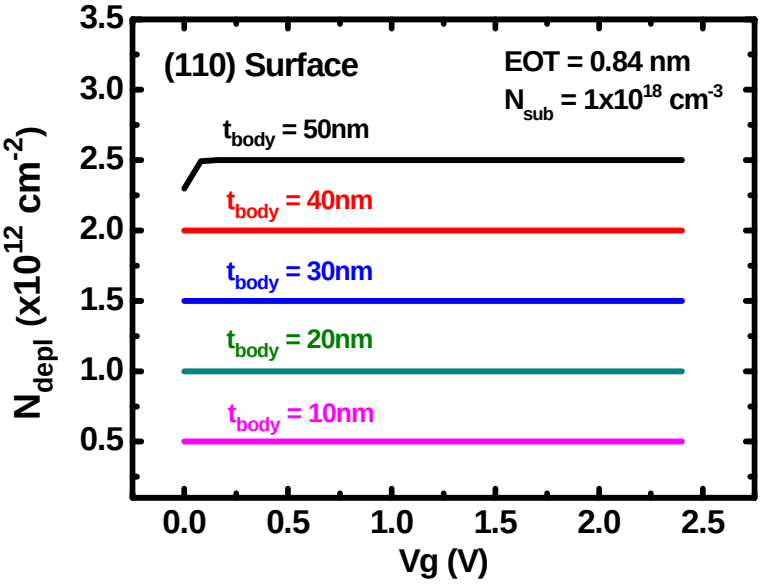
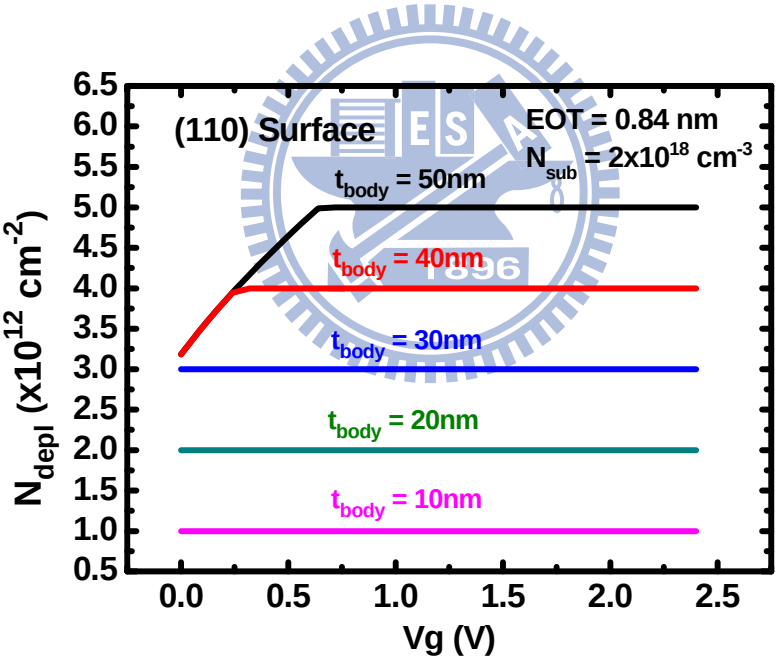


Fig. 6.1 Calculated subband energy associated with field confinement (line) and structure confinement (line+symbol) versus Vg for t_{body} = 10 nm and t_{body} = 20 nm.



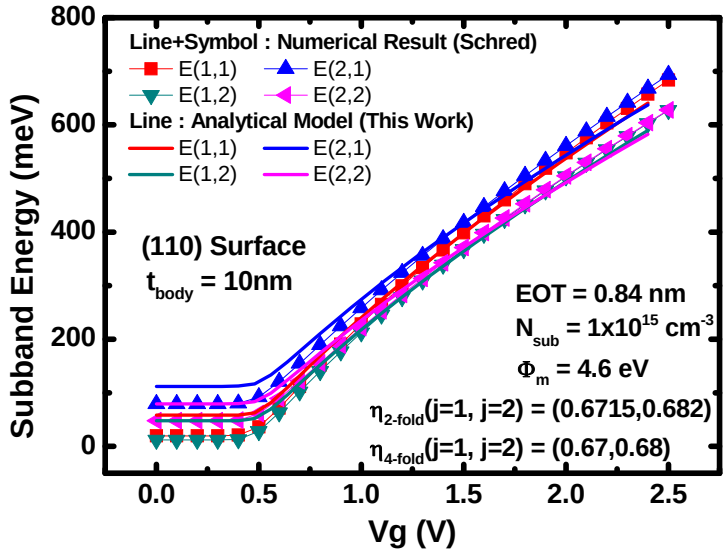
(a)



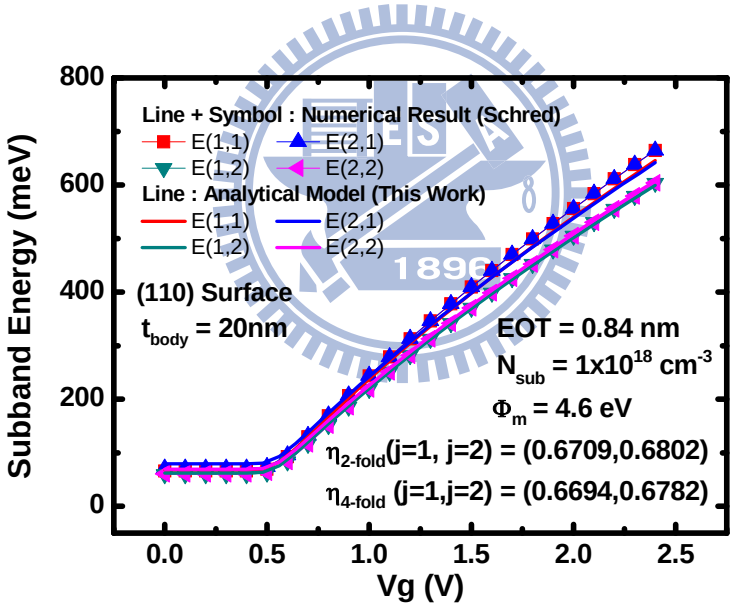
(b)

Fig. 6.2(a) Calculated depletion charge density versus Vg for N_{sub} = 1×10^{18} cm^{-3} and different t_{body}.

Fig. 6.2(b) Calculated depletion charge density versus Vg for N_{sub} = 2×10^{18} cm^{-3} and different t_{body}.



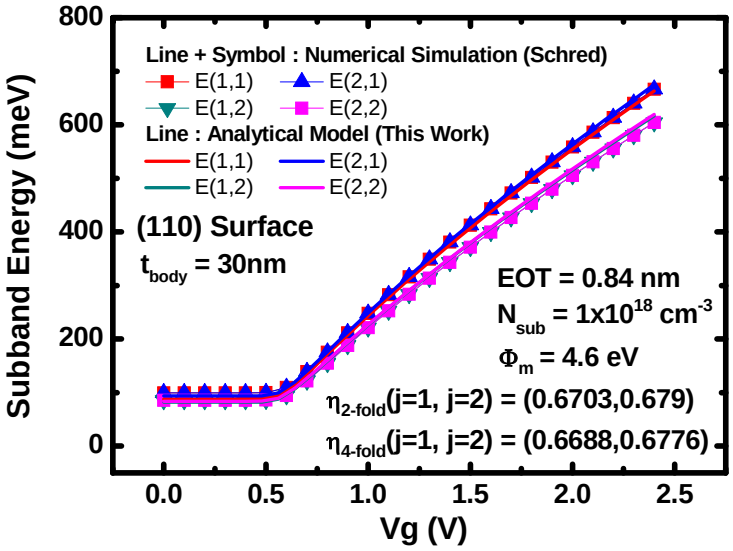
(a)



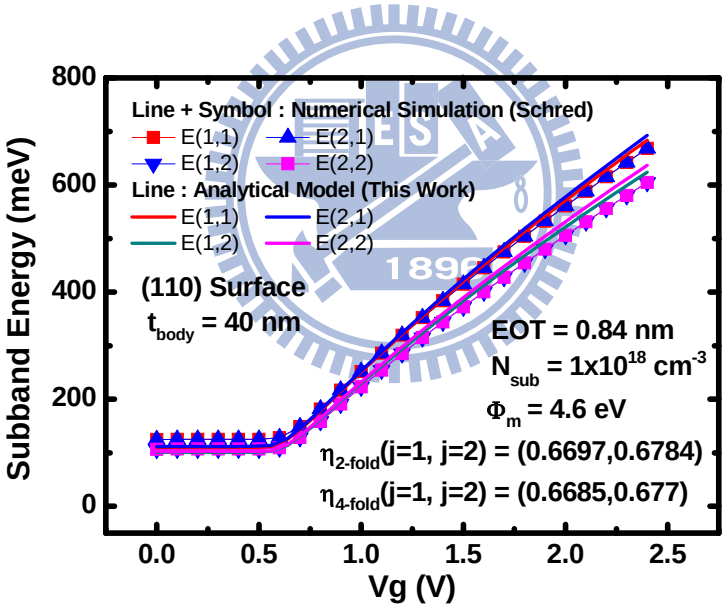
(b)

Fig. 6.3 (a) Comparison of numerically calculated subband energies (line + symbol) versus Vg with analytical ones (line) for t_{body} = 10 nm. Other parameters and fitting factor η used in calculation are labeled in figure.

Fig. 6.3 (b) Comparison of numerically calculated subband energies (line + symbol) versus Vg with analytical ones (line) for t_{body} = 20 nm. Other parameters and fitting factor η used in calculation are labeled in figure.



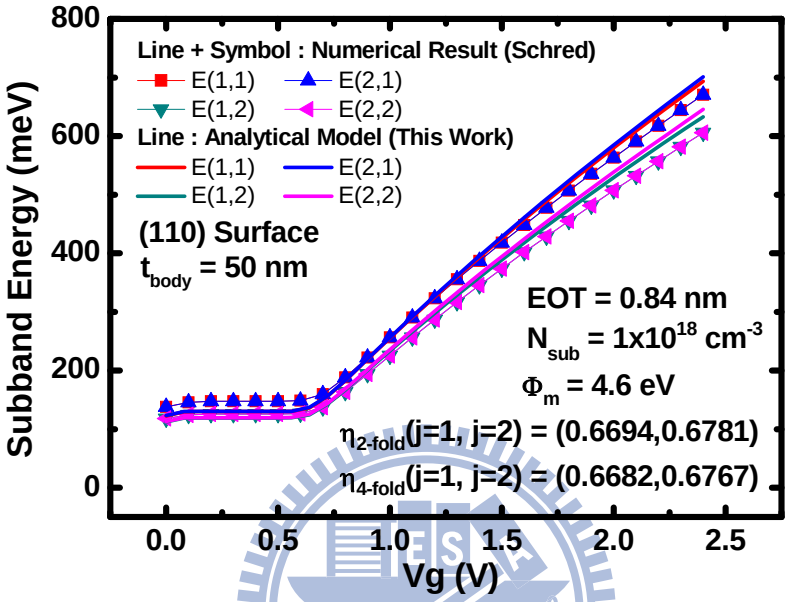
(c)



(d)

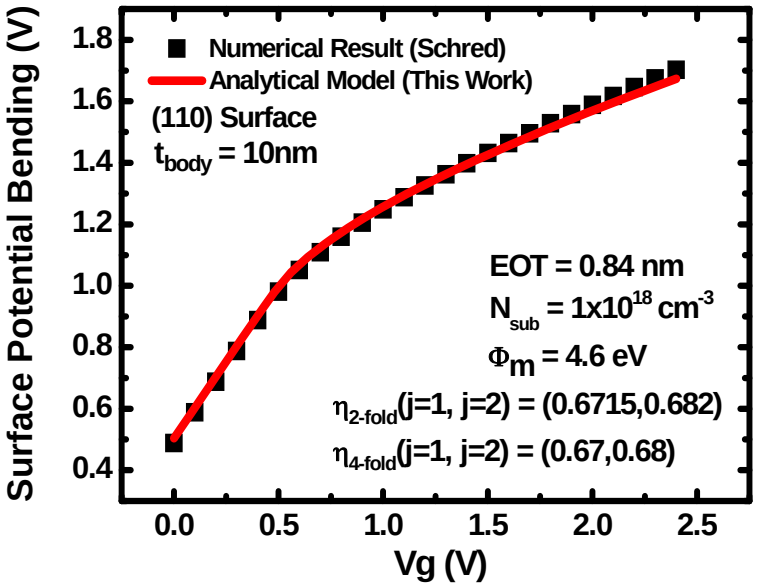
Fig. 6.3 (c) Comparison of numerically calculated subband energies (line + symbol) versus Vg with analytical ones (line) for t_{body} = 30 nm. Other parameters and fitting factor η used in calculation are labeled in figure.

Fig. 6.3 (d) Comparison of numerically calculated subband energies (line + symbol) versus Vg with analytical ones (line) for t_{body} = 40 nm. Other parameters and fitting factor η used in calculation are labeled in figure.

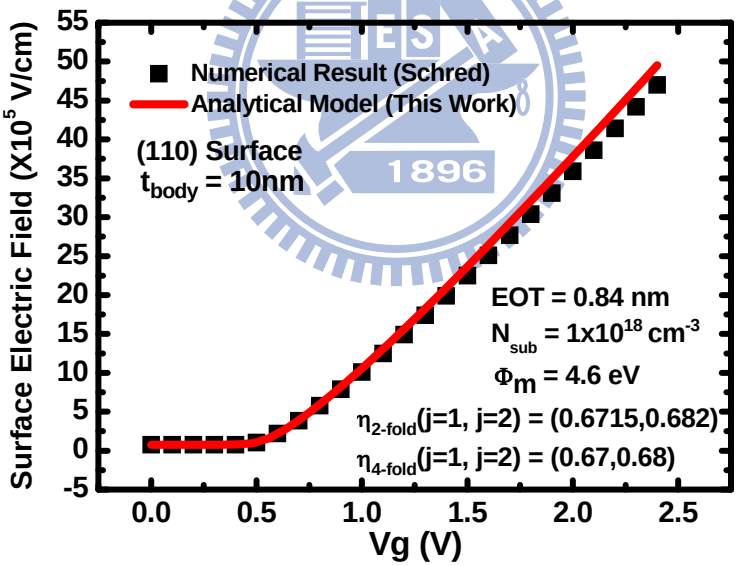


(e)

Fig. 6.3 (e) Comparison of numerically calculated subband energies (line + symbol) versus Vg with analytical ones (line) for t_{body} = 50 nm. Other parameters and fitting factor η used in calculation are labeled in figure.



(a)



(b)

Fig. 6.4 (a) Comparison of numerically calculated surface potential bending (line + symbol) versus Vg with analytical ones (line). Parameters and fitting factor η used in calculation are labeled in figure.

Fig. 6.4 (b) Comparison of numerically calculated surface electric field (line + symbol) versus Vg with analytical ones (line). Parameters and fitting factor η used in calculation are labeled in figure.

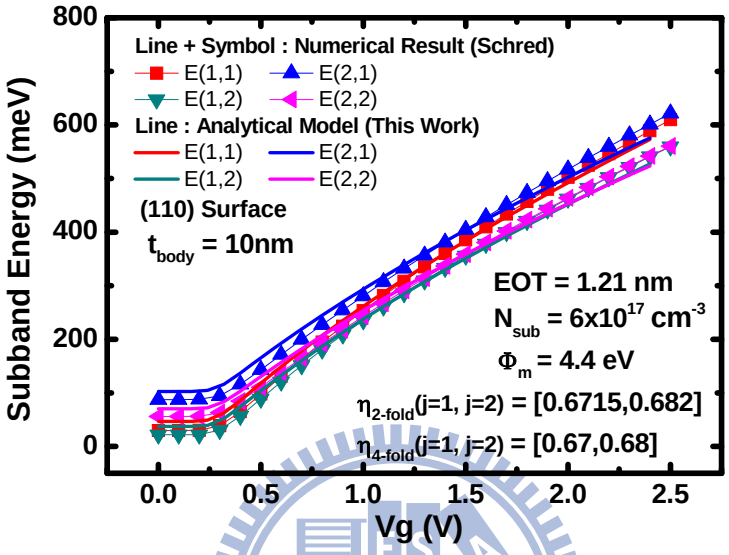


Fig. 6.5 Comparison of numerically calculated subband energies (line + symbol) versus Vg with analytical ones (line) for t_{body} = 10 nm. The material parameters used here are different from those used in Fig. 6.3 but the best fitting values of η hold the same with that used in Fig. 6.3.

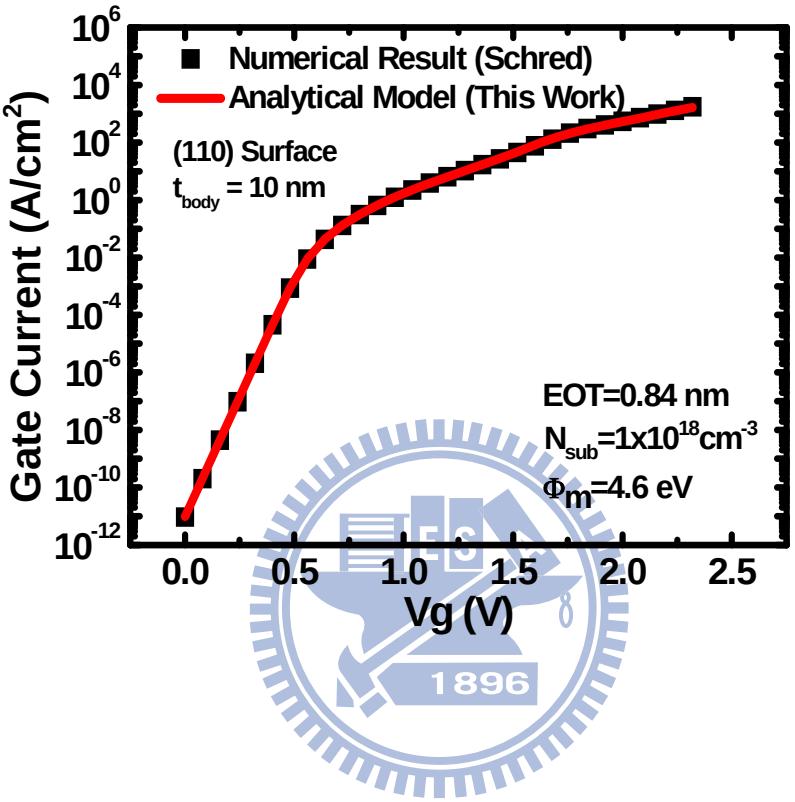


Fig. 6.6 Comparison of numerically calculated gate tunneling current with analytical one versus Vg.

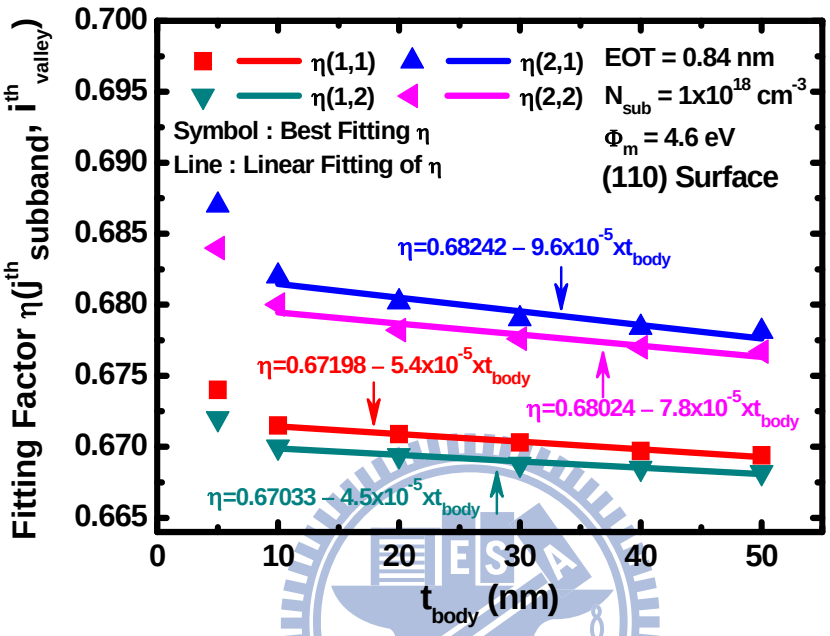


Fig. 6.7 η for best subband fitting versus t_{body} for (110) surface. Linear fittings of the η are shown as lines and the fitting equations are labeled as well.

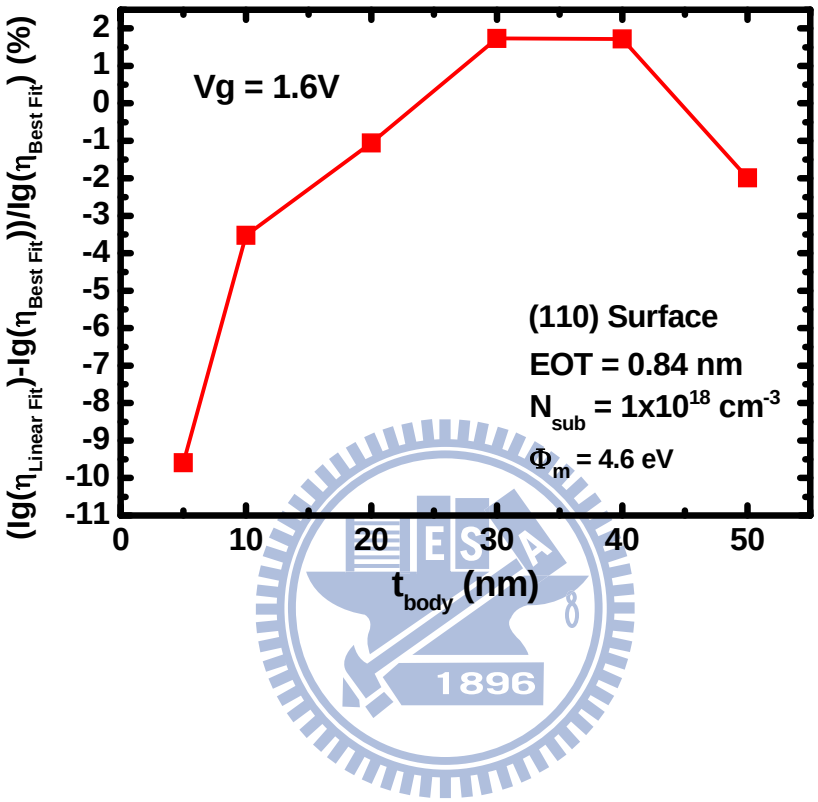


Fig. 6.8 Gate tunneling current change of gate tunneling current calculated with the linear fitting η with respect to that calculated with best fitting η versus t_{body}.

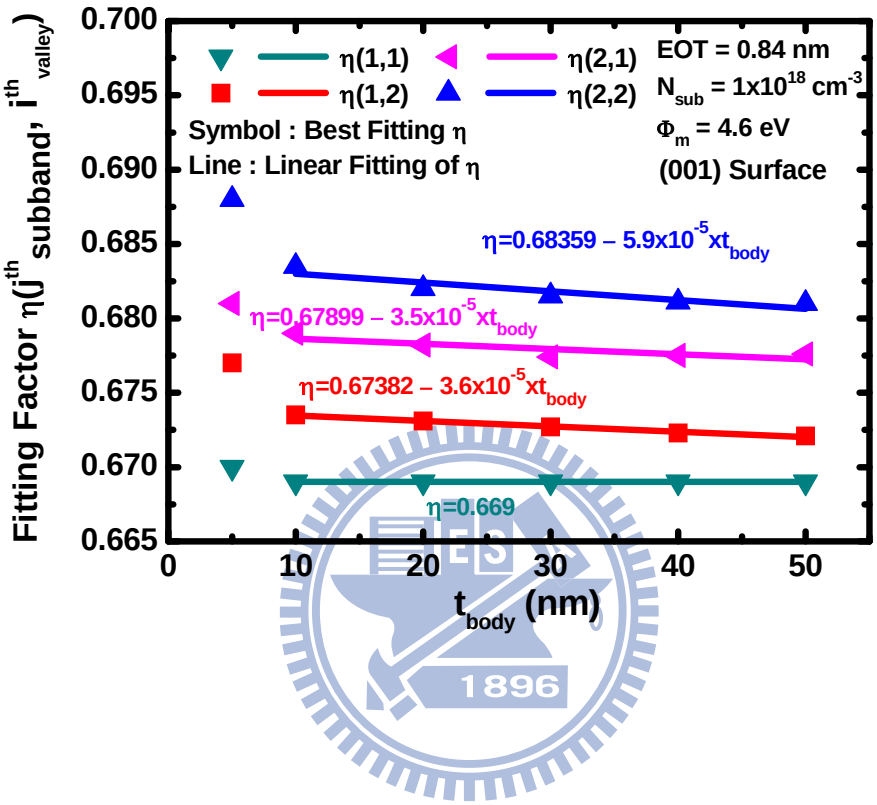


Fig. 6.9 η for best subband fitting versus t_{body} for (001) surface. Linear fittings of the η are shown as lines and the fitting equations are labeled as well.

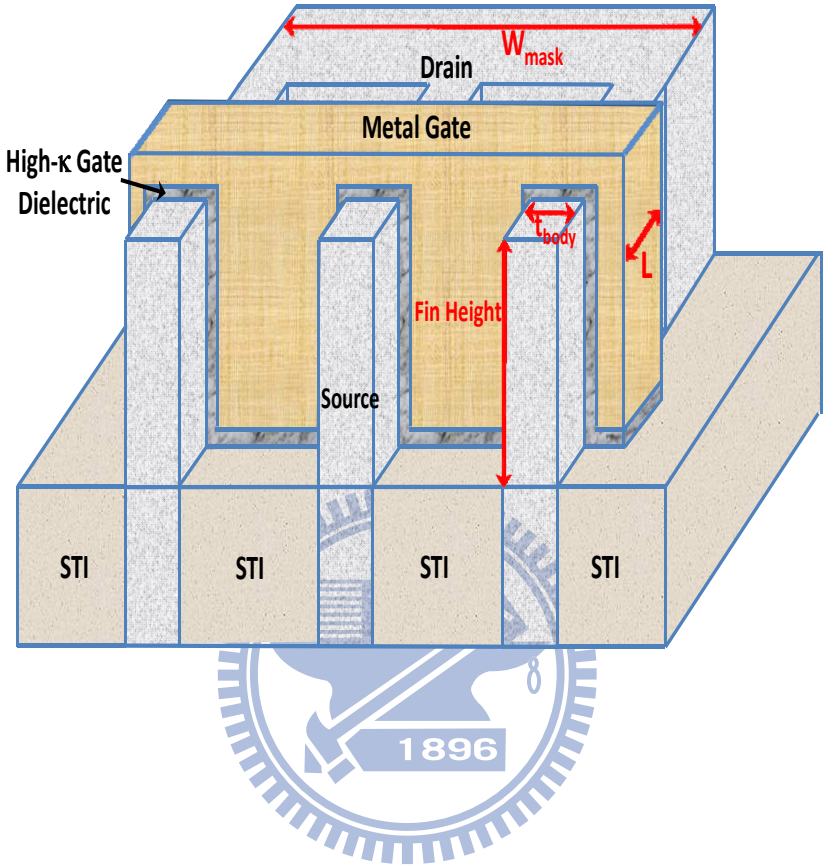


Fig. 6.10 Schematic cross-sectional view of FinFET device used in this work.

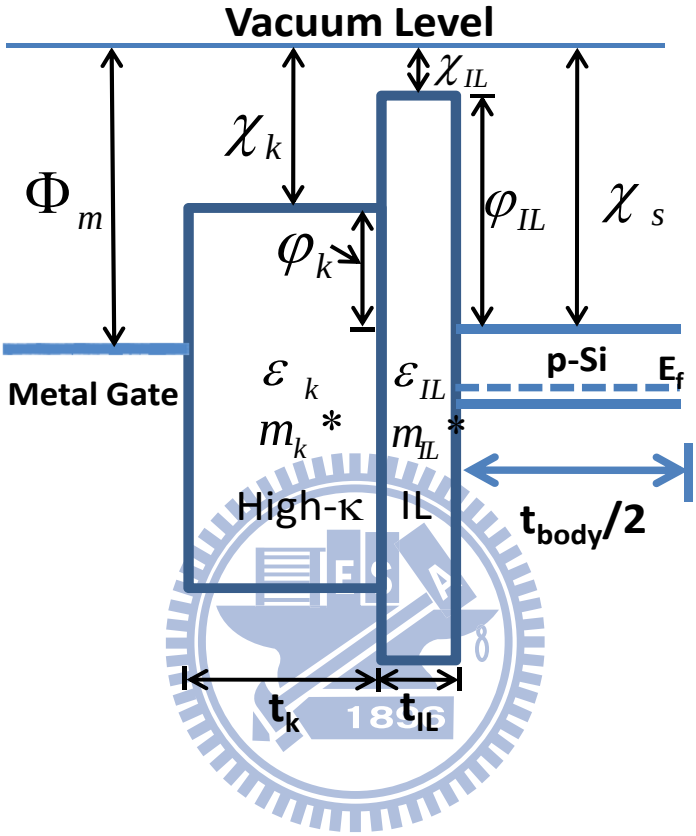


Fig. 6.11 Schematic of the abrupt energy band diagram of a metal-gate/high-κ/interfacial layer(IL)/Si system. The material parameters involved in this work are labeled.

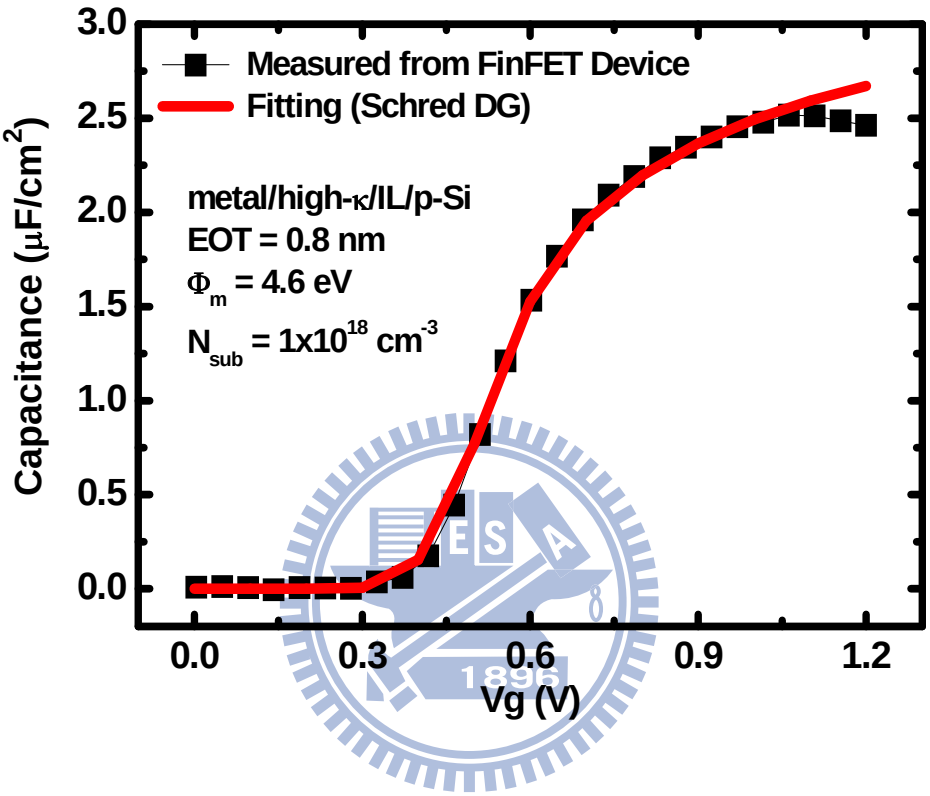


Fig. 6.12 Experimental Cg data (symbols) and fitting result for double-gate structure (line) versus Vg for n-type FinFETs. The extracted process parameters are EOT = 0.8 nm, Φ_m = 4.6 eV, and N_{sub} = 1×10^{18} cm^{-3}.

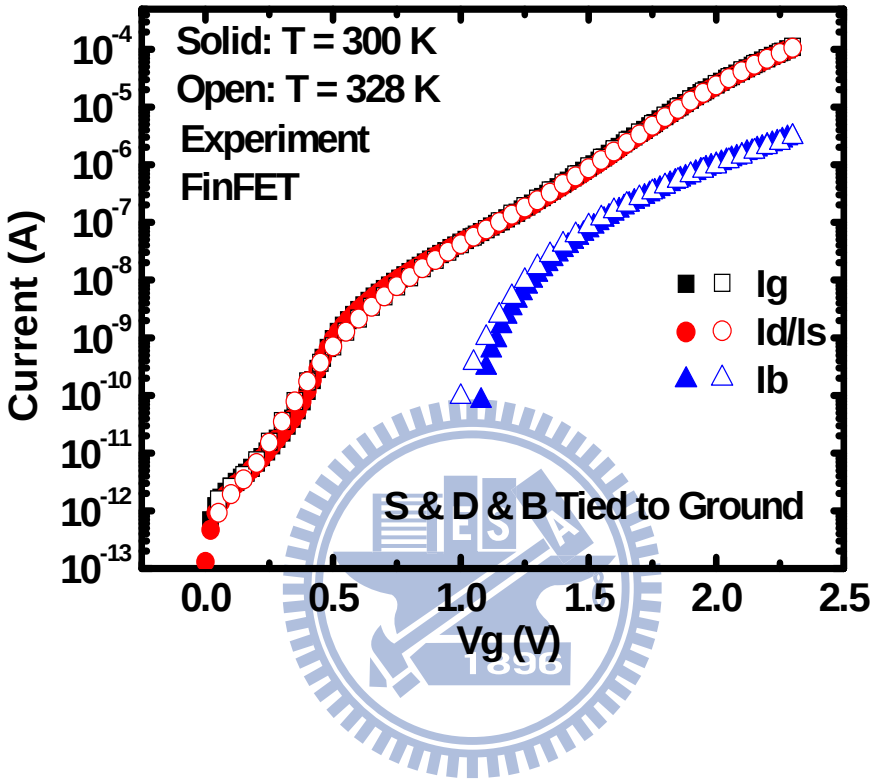


Fig. 6.13 Measured gate, source/drain, and bulk current at T = 300 and 328 K versus gate voltage. Weak temperature dependence of measured data indicates that the tunneling mecahanism dominates the gate leakage current. The source, drain, and bulk are all tied to ground.

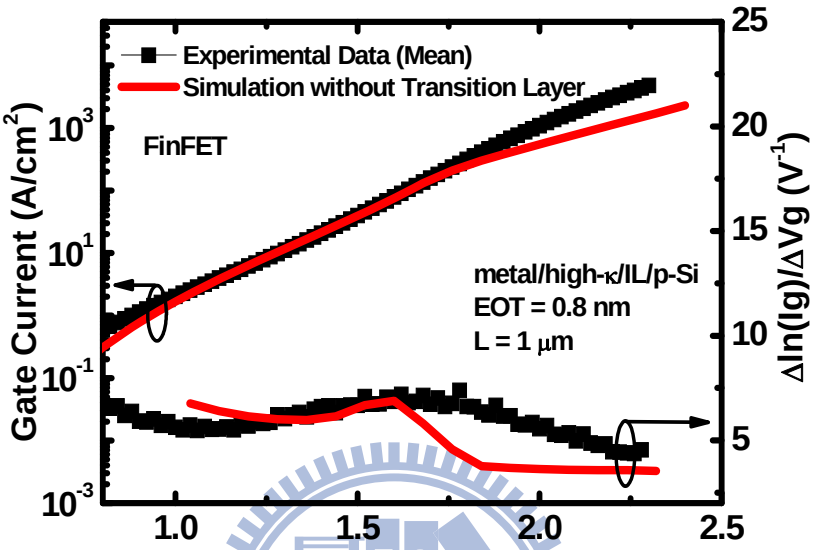
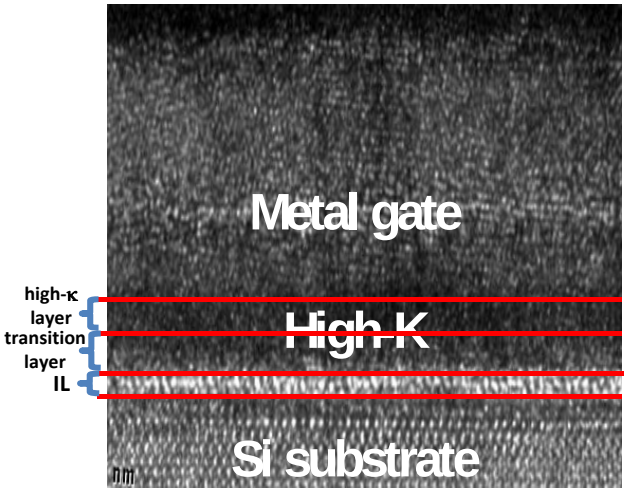
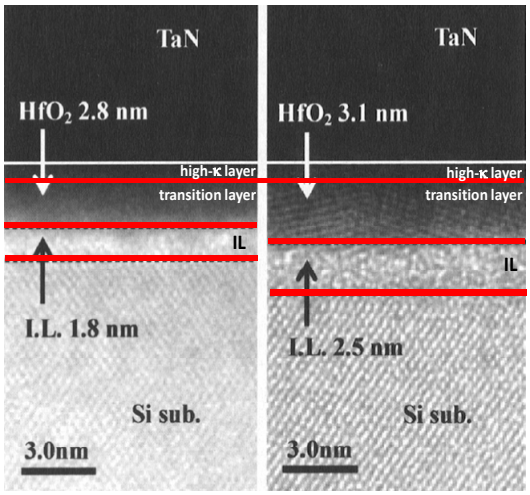


Fig. 6.14 Comparison of experimental (symbols) electron gate current Ig and its dlnIg/dVg versus Vg with calculated (lines) results under the assumption of two abrupt layers (one of high-κ and one of IL; see Fig. 6.11) of high-κ metal-gate dielectric. Fitting parameters are φ_k = 1.1 eV, m_k* = 0.02 m_o, m_{IL}* = 1.22 m_o, t_k = 1.2 nm, and t_{IL} = 1 nm.



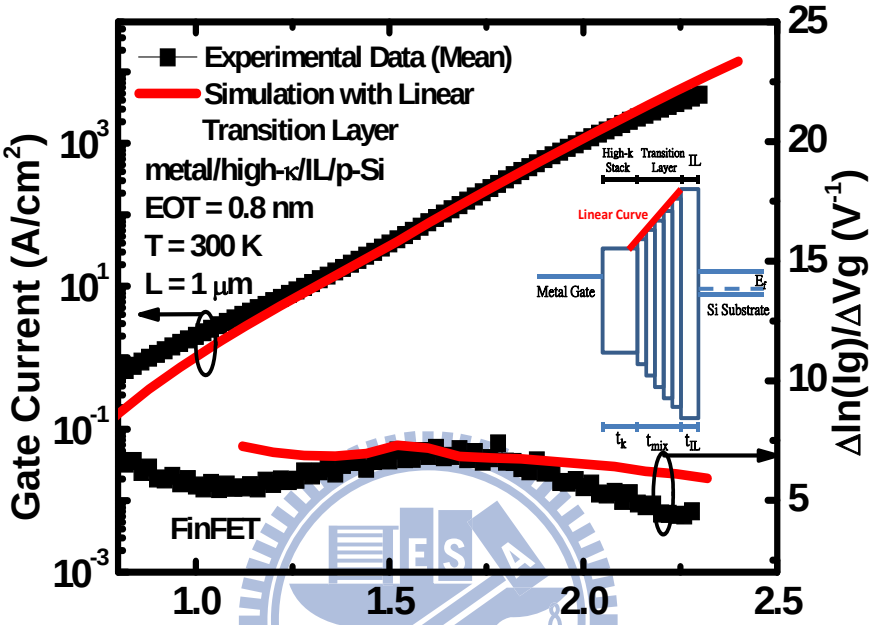
(a)



(b)

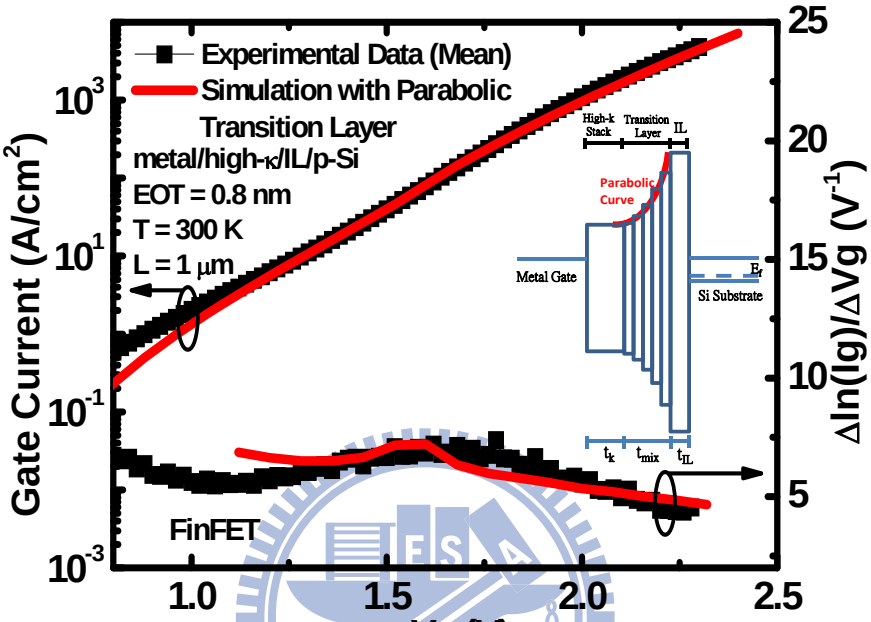
Fig. 6.15(a) TEM picture of high-κ metal-gate stack cited from the references [6.10], showing a transition region between IL and high-κ layer.

Fig. 6.15(b) TEM picture of high-κ metal-gate stack cited from the references [6.11], showing a transition region between IL and high-κ layer.



(a)

Fig. 6.16(a) Comparison of experimental (symbols) electron gate current Ig and dlnIg/dVg versus Vg with calculated (lines) results in the presence of a transition layer. The same EOT (0.8 nm) is preserved. The fitting parameters for linear gradual transition layer are φ_k = 1.1 eV, m_k^* = 0.02 m_o, m_{IL}^* = 0.8 m_o, t_k = 0.3nm , t_{mix} = 1.31 nm, and t_{IL} = 0.6 nm. The insets show the schematic of the energy band diagram for a linear gradual transition layer.



(b)

Fig. 6.16(b) Comparison of experimental (symbols) electron gate current Ig and dlnIg/dVg versus Vg with calculated (lines) results in the presence of a transition layer. The same EOT (0.8 nm) is preserved. The fitting parameters for parabolic gradual transition layer are φ_k = 1.1 eV, m_k* = 0.02 m_o, m_{IL}* = 1.39 m_o, t_k = 0.4 nm , t_{mix} = 1 nm, and t_{IL} = 0.59 nm. The insets show the schematic of the energy band diagram for a parabolic gradual transition layer.

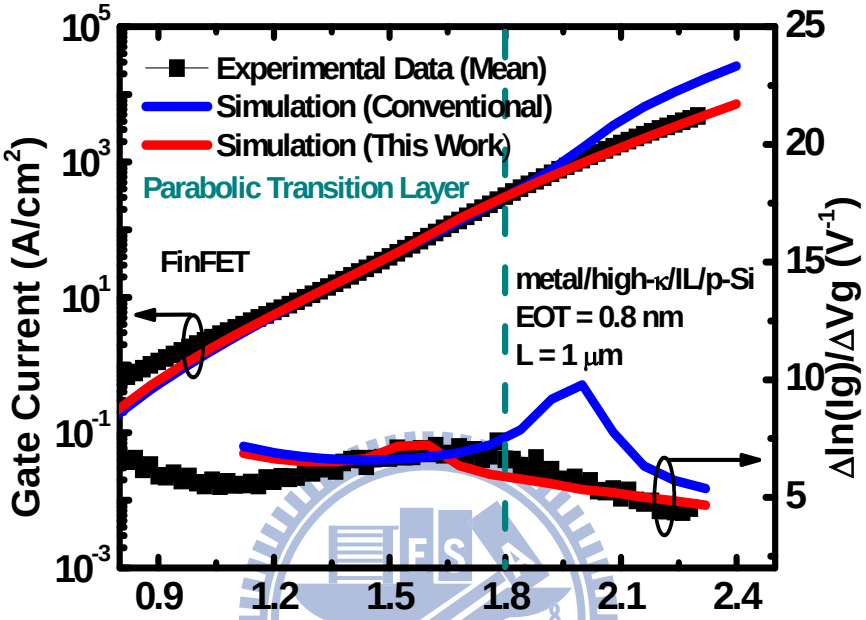


Fig. 6.17 Comparison of experimental (symbols) electron gate current Ig and dlnIg/dVg versus Vg with calculated (lines) results in the presence of a parabolic gradual transition layer using two sets of fitting parameters. Red line (this work) came from the same parameters as used in Fig. 6.16(b) while blue line (conventional method) came from φ_k = 1.5 eV, m_k^* = 0.18 m_o, m_{IL}^* = 0.93 m_o, and the same physical thicknesses as used in Fig. 6.16(b).

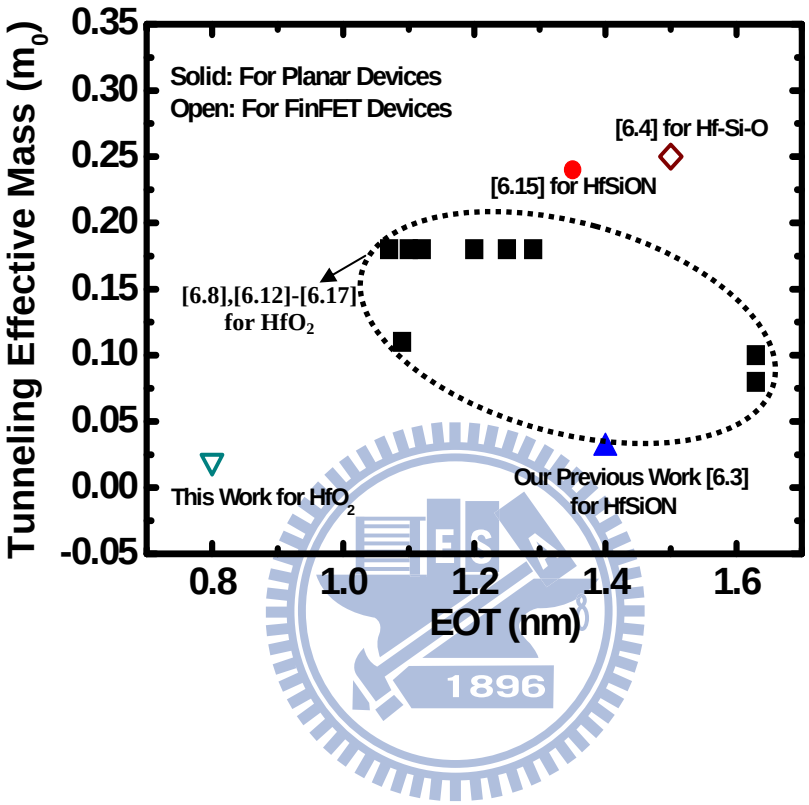


Fig. 6.18 The tunneling effective mass for hafnium based high-κ layer in the open literature and in our previous work versus effective oxide thickness (EOT). Solid symbols are for planar devices and open symbols are for FinFET devices.

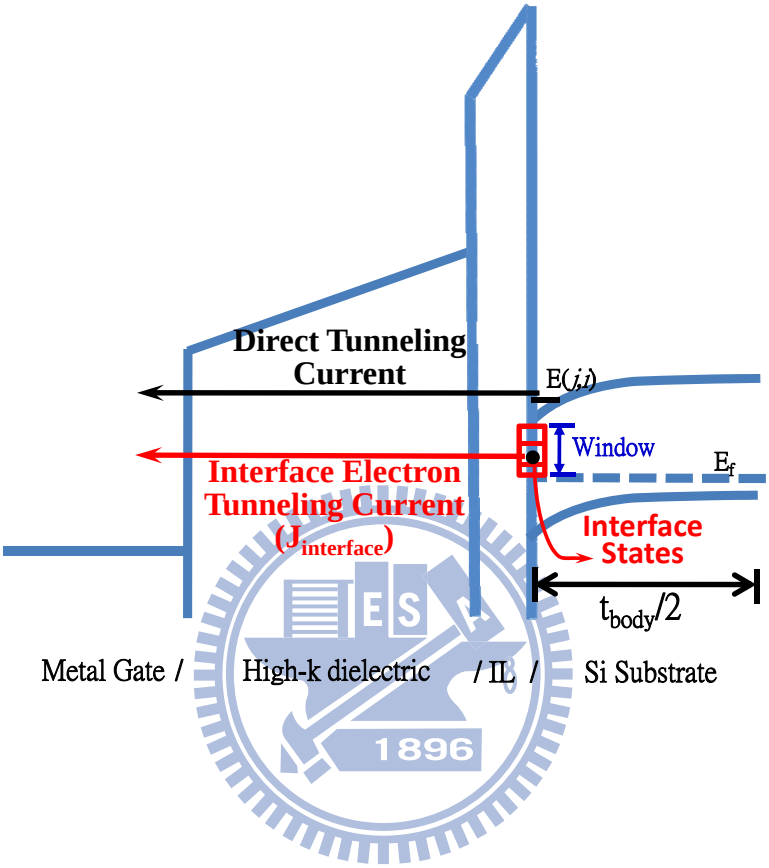
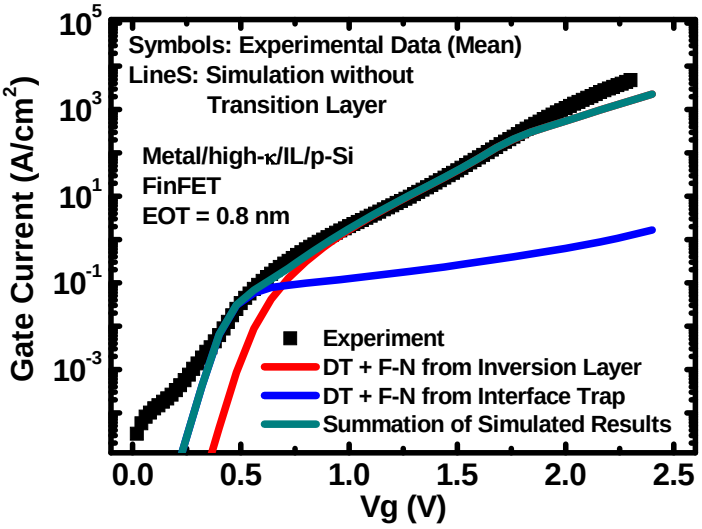
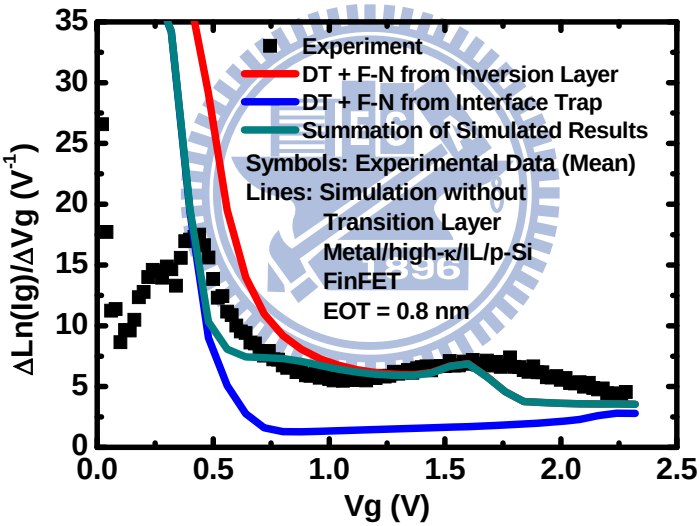


Fig. 6.19 Schematic band diagram showing the mechanism of electron tunneling from IL/Si interface states.



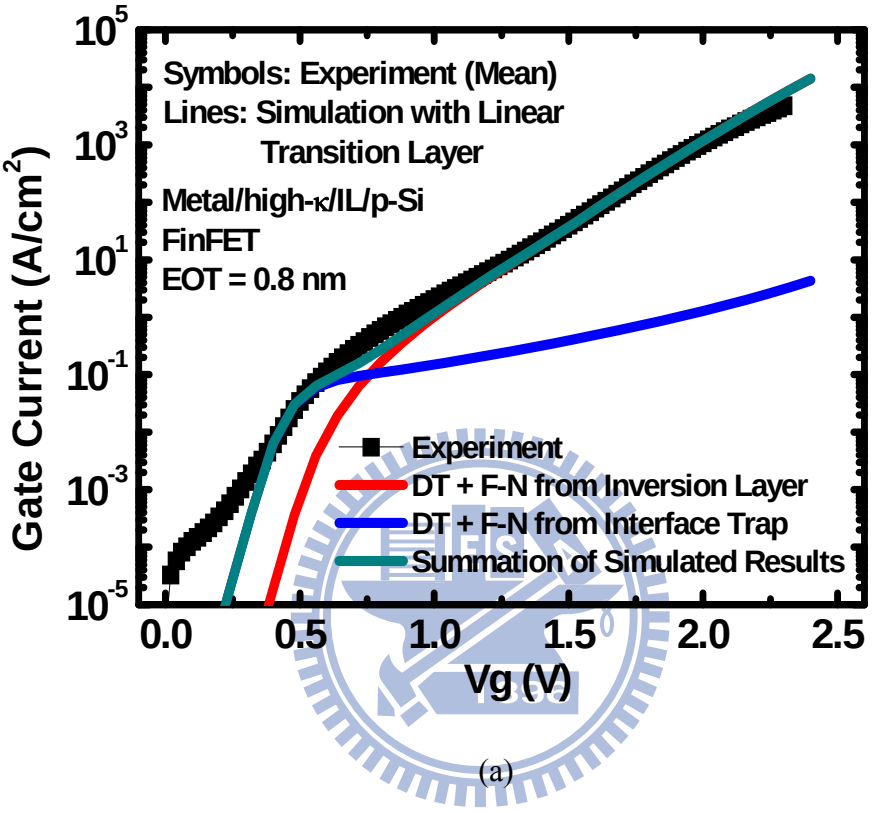
(a)



(b)

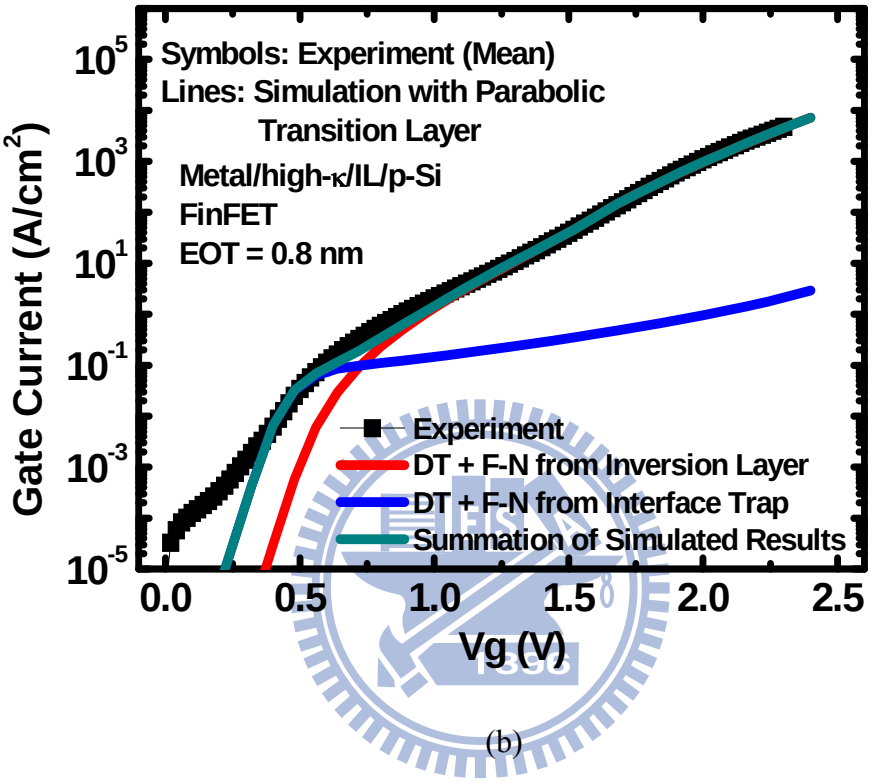
Fig. 6.20(a) Comparison of experimental data versus Vg with calculated direct (DT) and F-N tunneling current from inversion layer and IL/Si interface states. Summation of both calculated tunneling current components is also shown. Parameters for calculating electron tunneling from interface states are Window = 0.17 eV and $N_{interface}$ = 1.1×10^{20} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 6.14.

Fig. 6.20(b) Comparison of the experimental (symbols) dlnIg/dVg versus Vg with calculated (lines) results of direct and F-N tunneling current from inversion layer and interface states. Parameters for calculating electron tunneling from interface states are Window = 0.17 eV and $N_{interface}$ = 1.1×10^{20} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 6.14.



(a)

Fig. 6.21(a) Comparison of experimental data versus Vg with calculated direct (DT) and F-N tunneling current from inversion layer and IL/Si interface states in the presence of a linear transition layer. Summation of both calculated tunneling current components is also shown. Parameters for calculating electron tunneling from interface states are Window = 0.17 eV and $N_{interface}$ = 2.5×10^{20} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 6.16(a).



(b)

Fig. 6.21(b) Comparison of experimental data versus Vg with calculated direct (DT) and F-N tunneling current from inversion layer and IL/Si interface states in the presence of a parabolic transition layer. Summation of both calculated tunneling current components is also shown. Parameters for calculating electron tunneling from interface states are Window = 0.17 eV and $N_{interface}$ = 2×10^{20} $cm^{-3}eV^{-1}$. Other parameters are the same as those used in Fig. 6.16(b).

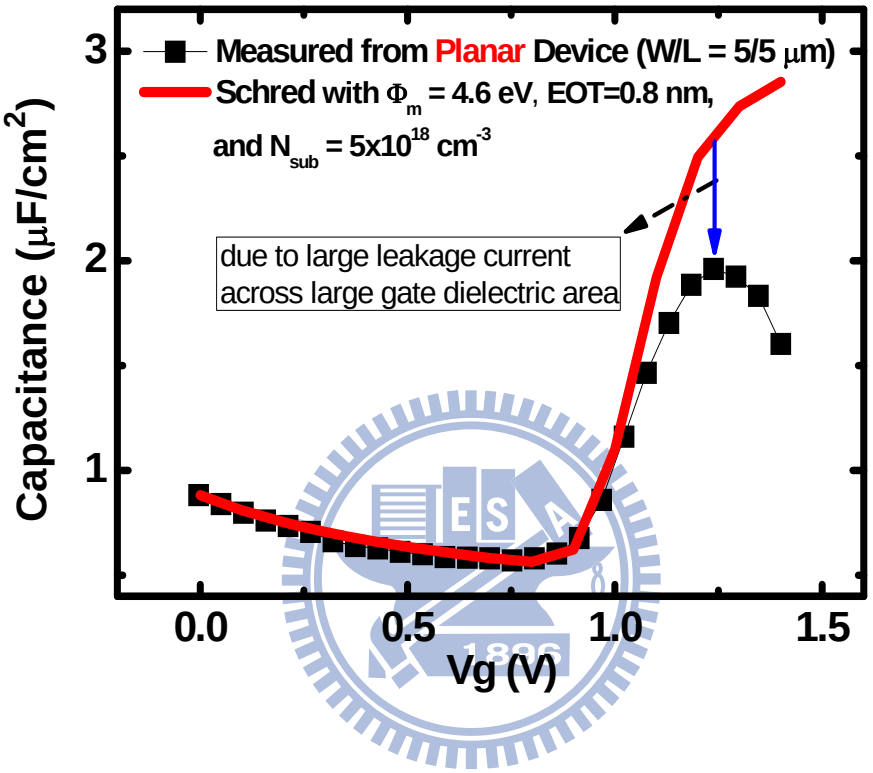


Fig. 6.22 Experimental (symbols) and simulated (line) C_g versus V_g for nMOSFETs. The discrepancy from experimental data is caused by large gate leakage current across large gate dielectric area.

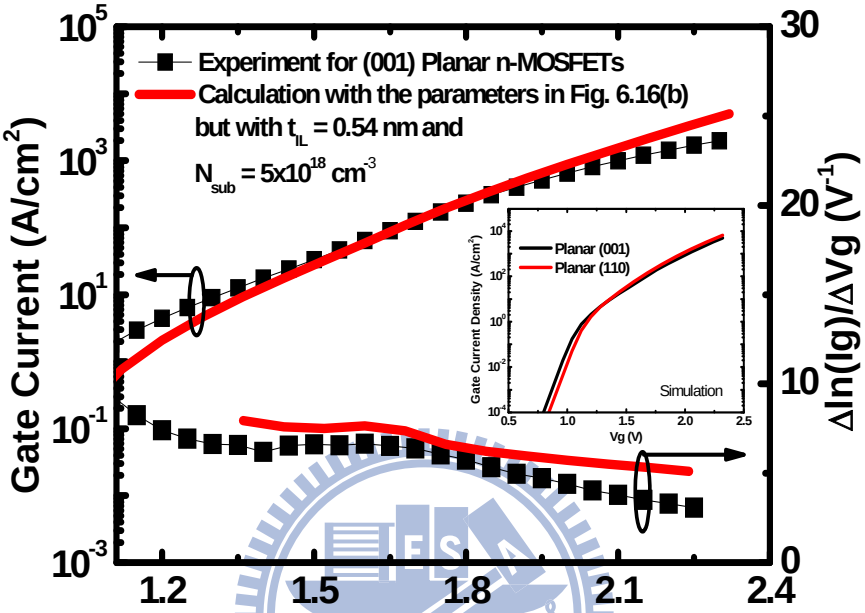


Fig. 6.23 Comparison of experimental (symbols) electron gate current and $d\ln I_g/dV_g$ versus V_g with calculated (lines) results. The inset shows that surface orientation does not strongly affect gate tunneling current. The fitting parameters are $\varphi_k = 1.1$ eV, $m_k^* = 0.02\ m_o$, $m_{IL}^* = 1.39\ m_o$, $t_k = 0.4$ nm , $t_{mix} = 1$ nm, and $t_{IL} = 0.54$ nm.

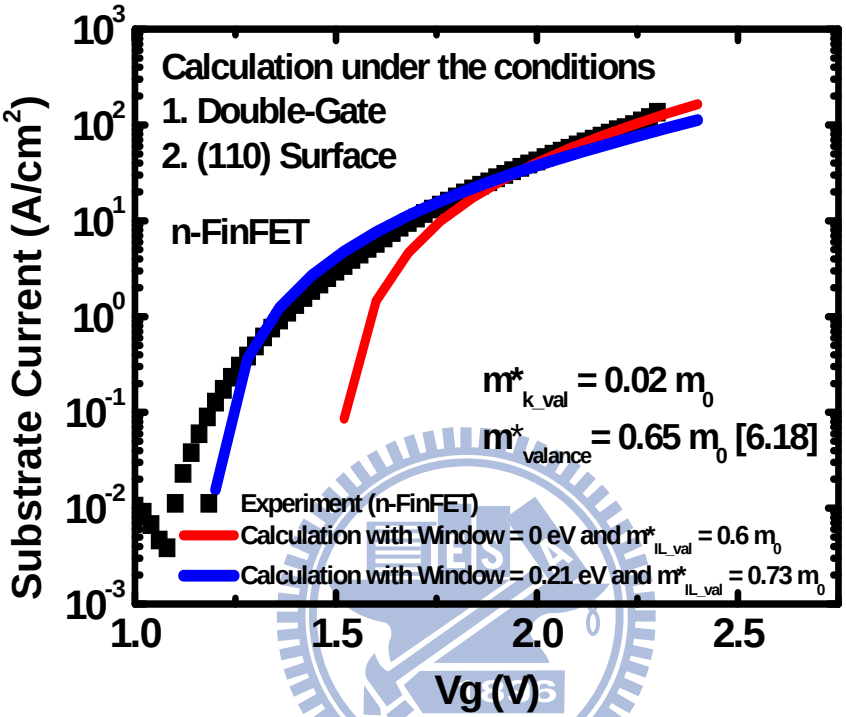


Fig. 6.24 Comparison of experimental data versus Vg with calculated valence electron tunneling current. Parameters for calculating valence electron tunneling current are: for red line, Window = 0 eV, $m^*_{IL\_val} = 0.6\ m_0$, $m^*_{k\_val} = 0.02\ m_0$, and $m^*_{valence} = 0.65\ m_0$; and for blue line, Window = 0.21 eV, $m^*_{IL\_val} = 0.73\ m_0$, $m^*_{k\_val} = 0.02\ m_0$, and $m^*_{valence} = 0.65\ m_0$. Other parameters are the same as those used in Fig. 6.14.

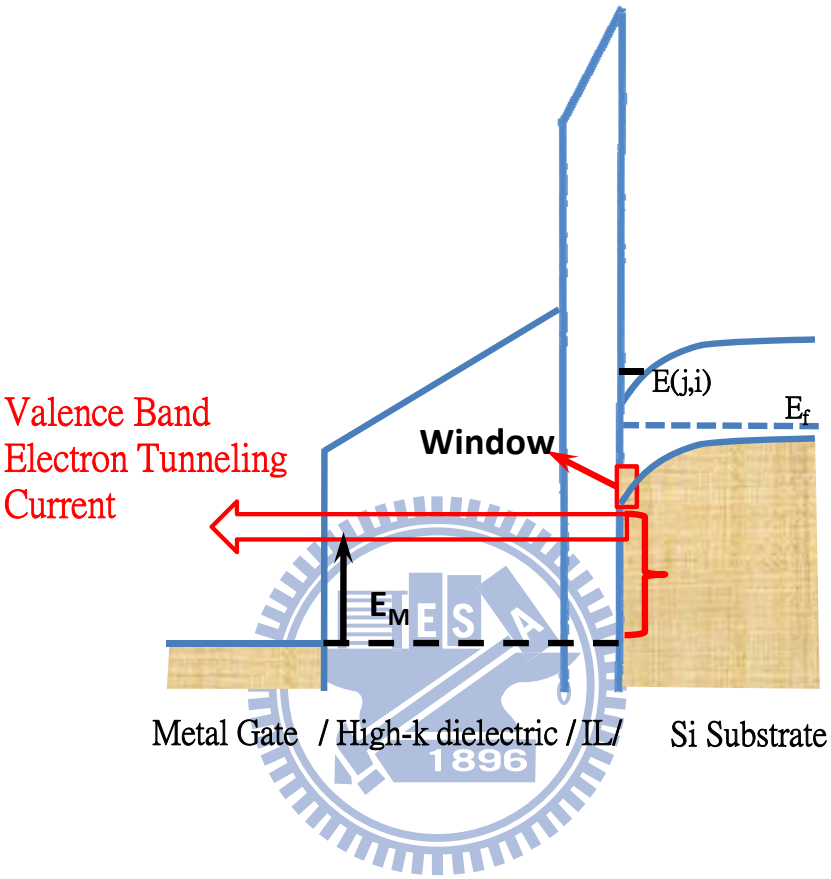


Fig. 6.25 Schematic of energy band diagram showing the mechanism of valence band electron tunneling through high-κ stacks.

Chapter 7

Conclusion

7.1 Summary of Contribution

This dissertation presents advanced and comprehensive gate tunneling current modeling effort on poly gate/SiO_2 gate dielectric MOSFETs, metal-gate/high-k gate stacks CMOSFETs, and metal-gate/high-k gate stack n-FinFETs. The resulting process and material parameters not only can provide new insight into underlying manufacturing process but also can be quantitatively more accurate than those obtained from conventional method without advanced techniques in this work.

First of all, the unconventional increasing trend of hole gate direct tunneling current on a nominal 1.27-nm gate oxide p-MOSFET with STI compressive stress was newly observed. To resolve this contradicting issue, a quantum strain simulator has been established and its validity has been verified experimentally. The combination of the verified simulator and the experimental data has systematically led to the finding of the origin: A reduction in the apparent physical gate oxide thickness over the whole gate area, with an accuracy of 0.001 nm, occurs under the influence of the STI compressive stress. Hence, presented tunneling current model can serve as a sensitive detector of the stress altered thickness of gate stacks.

Tunneling model taking into account a transition zone between direct tunneling and Fowler-Nordheim tunneling for metal-gate/high-k gate stacks has been established. A new approach by combining a fitting scheme over the $d\ln I_g/dV_g$ versus V_g curve with the C_g-V_g and I_g-V_g fittings has been proposed in order to accurately extract the material and process parameters of metal gate high-*k* dielectrics. The guideline for fitting gate tunneling current and extracting the high-κ layer parameters of

TaC/HfSiON/SiON gate stacks nMOSFET has been created. The extracted results have been supported by extra measurements at higher temperatures and gate voltages. Additionally, a physical tunneling model describing the electron tunneling from IL/Si interface states perfectly reproduce the experimental data at low gate bias and thereby the underlying physical origin has been captured. The significance of electron tunneling via interface states has been examined throughout the work and has been quantitatively verified by extensively performed experiments and fittings.

Based on the fitting guideline proposed in Chapter 2, C_g-V_g, I_g-V_g and its $d\ln I_g/dV_g$ versus V_g curve fitting for TiN/HfO_2/SiON gate stacks nMOSFETs have been carried out. Material and process parameters have been accurately assessed accordingly. Two important arguments about the properties of high-κ layer have therefore been drawn. First, the smallest m_k^* (0.03 m_0) to date exists in both HfO_2 and HfSiON high-κ layers. Second, by means of gate tunneling modeling, a transition layer appears to exist between HfO_2 and SiON layers but not in the case of HfSiON/SiON gate stacks.

Hole tunneling current modeling for TaC/HfSiON/SiON and TiN/HfO_2/SiON gate stacks pMOSFET has been done. Due to relative weak dependence of hole tunneling current data on gate bias, trap-assisted tunneling is not absent in contributing hole tunneling current for the fresh pMOSFETs with TiN/HfO_2/SiON gate stacks. Current separation method has further revealed that gate-to-substrate electron tunneling dominates over the overall gate leakage current. Hence, for the first time, the model for dealing with metal-gate-to-substrate electron tunneling current has been established. The validity of this model has been verified experimentally. Comparing experiment with simulation in a systematical manner, we have found that unfilled-states around Si conduction band in the forbidden gate are considerably occupied and additional tunneling from metal gate is plausible for both test samples.

Finally, a new compact simulator for double-gate structure has been established.

Gate tuuneling leakage of FinFET can be modeled by this analytical model. Our proposed fitting approach by combining a curve fitting of dlnIg/dVg-Vg with Ig-Vg and Cg-Vg curves fitting has been conducted for metal-gate/high-κ nFinFET as well. Again, the material and process parameters of FinFETs have been accuratly extracted.

7.2 Suggestions to Future Work

One of the main contributions in this dissertation is that a curve fitting around the peak of dlnIg/dVg-Vg can help accurately determine the band offset of high-κ layer to silicon conduction band. If we further observe the temperature dependence of the dlnIg/dVg-Vg curve, some new insight into the band offset of high-κ layer may be obtained.

In this work, several remarkable findings about the properties of high-κ gate stacks have been presented. First, interface states dominant gate leakage current at low gate bias has been demonstrated. Second, the HfO_2 based high-κ layer may have transition layer between high-κ layer and IL but HfSiON may not have that. However, how the transition layer and interface states affect mobility properties is an important topic. It is interesting to observe if theoretically calculated mobility with those $N_{interface}$ obtained by gate current fittings can match the experimental mobility at low Vg. This approach can further verify the value of $N_{interface}$. By manufacturing two different high-κ gate stacks: one has transition layer but the other does not have, the effect of transition layer on mobility can be captured. Furthermore, the kinetic tapping and de-trapping properties of the trap states in the presence of a gradual transition layer between high-κ layer and IL may be examined by means of RTS and low-frequency noise measurement. Finally, many studies show a strong relationship of NBTI with interface traps. Hence, a further task to relate the measured gate leakage current at low gate bias to NBTI stress is worthy to do.

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Chapter 1

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學經歷表 Vita

姓名/Name ： 許智育 Chih-Yu Hsu **性別**： 男
生日/DOB ： 1983/09/04 **籍貫**： 新竹縣
地址/Address： 304 新竹縣新豐鄉復興街一巷 5 號

學歷/Education：

國立新竹高級中學	1998.9-2001.6
National HsinChu Senior High School	
國立交通大學電子物理學系	2001.9-2005.6
Dept. of Electrophysics, NCTU	
國立交通大學電子工程研究所碩士班	2005.9-2006.6
Master Program, Dept. of Electronics Engineering, NCTU	
國立交通大學電子工程研究所博士班	2006.9-2011.9
Ph. D., Dept. of Electronics Engineering, NCTU	

博士論文題目/Ph. D. Dissertation：
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