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博士論文

奈米點記憶體元件之製作及其電性特性研究

Fabrication and Electrical Characteristics of the
Nanocrystal Nonvolatile Memory Devices



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新穎性奈米點記憶體元件之製作及其電性機制研究
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中文摘要

近年來，非揮發性記憶體元件帶動了攜帶性產品的發展，如手機、筆記型電腦、mp3 隨身聽、隨身碟、數位相機等。傳統非揮發性記憶體的操作原理是利用複晶矽浮停閘(floating-gate)做為載子儲存單元，其操作模式是透過儲存的電荷自反轉層之通道以穿隧效應躍遷過穿隧氧化層並儲存至複晶矽浮動閘極內。當移除所施加於元件的閘極偏壓後，由於所儲存電荷無足夠的電場或動能來穿過或躍遷穿隧氧化層，該電荷便侷限於浮動閘極中，並造成電晶體之起始電壓的改變。藉此，我們透過記憶體元件起始電壓的變化來判讀其狀態。然而，隨著元件微縮技術的需求，使得傳統的浮停閘極記憶體結構也面臨了元件可靠度上的挑戰，在元件進入奈米尺度後，為了維持閘極控制能力則必須等比例微縮下的穿隧氧化層，使其厚度不再具有絕對的阻障效果，導致保存在浮停閘內的儲存電荷容易再穿隧回通道。另外，在經過長時間而高速的操作後，薄化的穿隧氧化層亦容易產生漏電路徑，因而導致記憶體元件的失效。另外，在橫向的微縮上，當其中單一元件寫抹或讀取時，可能連帶影響到鄰近的元件的狀態。因此，為了解決浮停閘極結構記憶體未來將遭遇的困境，以分離式獨立儲存單元作為電荷儲存層之奈米量子點(Nanocrystal)因而被提出，該結構透過將電荷儲存在分離性的儲存中心的想法，因此即便元件有漏電路徑產生，仍可保留大部分的儲存電荷，做為有效之邏輯判讀以解決可靠度的瓶頸，相較於浮停閘極元件，奈米量子點可容許較薄的穿隧氧化層，可進而降低操作電壓以及提高寫抹效率。在目前已發表之奈米點記憶體元件中，最常被廣泛討論的材料可分為金屬、介電質及半導體奈米點三類。其中以金屬或類金屬的奈米點結構開發為近年來之研究重點，由於具有其具

有高功函數、高閘極耦合能力以及擁有較低的聚積溫度等優點。在本論文中，我們將研究以鎳及鈷為主要材料來製作奈米點結構並討論其應用於非揮發性記憶體元件之電性結果。在目前，奈米量子點的製作方式主要可分為薄膜的自我析出特性、過飽和而析出以及透過氧化反應而分離等方式。因此，在此，我們將針對這些方式作進一階的探討及改善。

在自我析出的製作方式中，我們透過共蒸鍍的方式將鎳元素加入常見之矽化鎳自我析出的系統當中，探討加入的鎳元素對於矽化鎳奈米點的形成所造成的影響，在與其未加鎳之矽化鎳之比較組相對照下，可發現摻有鎳的矽化鎳在較低的退火溫度下，得到一個較佳的奈米點尺寸及密度分佈。其主要原因為加入的鎳使得矽化鎳較容易由非晶態轉為複晶態，在轉態的過程中所釋放的能量將促進了奈米點的析出過程，因而可得到一個較好的奈米點均勻性。此外，可發現，摻有鎳之矽化鎳元件在電性特性上展現 9 的記憶窗口在正負 10 伏特的電容電壓特性上。而在可靠度上，該元件亦可維持 2.4 伏特的記憶窗口即使經過 10^4 秒的載子保存能力測試後。

在奈米點元件製作上，離子佈植法發現可以製作相當高密度且多層分佈之奈米點結構，而常被應用於光電元件製作上。然而，在記憶體元件上，離子佈植法却有可能傷害穿隧氧化層的可能性，且摻入的元素分佈亦較難侷限，因此可能進而影響元件的可靠度特性。在此，我們亦希望透過共蒸鍍的方式以形成可形成類似離子佈植法的金屬及介電質混和之結構以製作鎳金屬奈米點埋入氧化矽之記憶體元件。而透過高解析穿透式電子顯微鏡，可發現所形成之奈米點呈現雙層及單層的分佈在不同的退火溫度下，其原因是由於共蒸鍍時鎳金屬是任意分佈於介電層當中，熱退火時，鎳金屬會任意擴散碰撞，並在適當的成核點聚積成奈米點，由於共蒸鍍時核點是任意分佈的，因此可再是適當的膜厚下，形成多層或單層的結構，而較高溫下退火時，足夠的能量將促使任意分佈的奈米點之間互相聚積而兼併，進而形成較大尺寸較低密度的奈米點結構，透過進階的穿隧式電子顯微鏡照片，證實即使是單層結構下，亦可得到一個極高密度 ($4.5 \times 10^{12} \text{cm}^{-2}$) 的奈米點結構，其結果有助於改善奈米點結構的均勻性的問題。該元件在電性上亦有優秀的特性表現， 800°C 退火的元件展現 4 伏特的記憶窗口以及 2.1 伏特的載子保存能力。另外，我們亦嘗試透過共蒸鍍的方式製作鎳金屬點埋入氮化矽之結構，其結果與埋入氧化矽相當的類似，且有較佳的可靠度，其結果是因於使用氮化矽層，由於下層的氮化矽可以降低庫倫屏障效應時的介面電場，因而降低載子從奈米點躍出的可能性。

另外，氧化反應亦是一個常見的方式以致做奈米點元件，透過不同元素之間的氧化能力來達成元素析出的方式製作奈米點。然而，直接氧化的方式仍有著過度氧化的可能性，因此於本論文中，我們嘗試透過反應式蒸鍍的方式來製作奈米點元件，實驗中，於蒸鍍矽化鈷時通入適當的氧氣流量，在反應式蒸鍍過程中，所蒸鍍之矽化鈷可能會被局部氧化或是氧摻雜，因此後續的熱退火過程中只需在氮氣下進行。只要有效控制蒸鍍時氧的流量，即可以避免反應時，其矽化鈷薄膜

被過度氧化的問題，實驗結果顯示透過反應式濺鍍所製作的元件有明顯的奈米點形成於穿隧氧化層上，其奈米點尺寸和密度分別為 5-6 奈米 and $3.2 \times 10^{12} \text{cm}^{-2}$ 。而該元件亦展現 7 伏特的記憶窗口。另外，我們也研究了不同氧流量上及不同退火溫度下所造成的效應，以提出製作該元件的最佳化條件，並嘗試透過濺鍍時通入氮氣體，探討製作以反應式濺鍍製作奈米點埋入氮化矽之可能。

最後，我們亦嘗試使用硝酸氧化的方式來製作矽化鈷奈米點元件的穿隧氧化層，其動機在於現今所發表的文獻中，元件穿隧氧化層的製程溫度常常需要高於 800°C 以上，反而高於奈米點製作溫度，而此高溫退火可能不利於奈米點元件應用於多層結構亦或玻璃基板等，而近年來所提出之硝酸氧化法是透過硝酸水解時所帶來的高氧化能力以氧化金屬或半導體薄膜，形成薄而緻密的介電層，實驗結果可以發現使用硝酸氧化製作出的氧化鋁作為穿隧氧化層的記憶體元件仍然可以擁有 10 伏特的記憶窗口及 2.1 伏特的載子保存能力。該結果亦表示該氧化鋁有能力保存寫入之載子於奈米點內而不會輕易地漏回，亦證實硝酸氧化有潛力使用於製作低溫的穿隧氧化層。



Fabrication and Electrical Characteristics of the Nanocrystal Nonvolatile Memory Devices

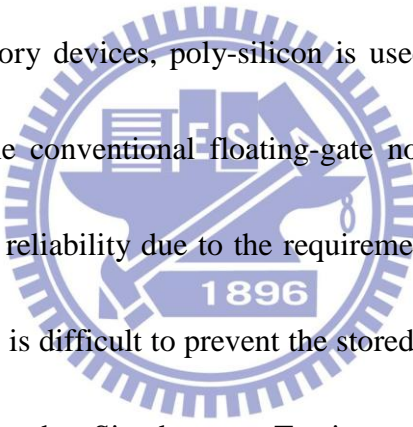
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Abstract

The logo of National Chiao Tung University is a circular emblem. It features a gear-like outer border. Inside, there is a stylized representation of a building or structure with the letters 'NCTU' integrated into it. Below the building, the year '1896' is inscribed. The entire logo is rendered in a light blue or purple color.

In conventional memory devices, poly-silicon is used as the “floating-gate” to store charge. However, the conventional floating-gate non-volatile memory device has faced the challenge of reliability due to the requirement of down-scaling device. The scaled tunneling oxide is difficult to prevent the stored charge in the floating-gate from tunneling back into the Si-substrate. To improve the retention time of conventional floating-gate memories, nanocrystal memory devices have been proposed. In the nanocrystal structure, the device can store charge in distributed charge trapping centers. Even if the leakage path is formed in the tunneling oxide, the device still can keep enough charge for the correct data of logic circuit.

In the thesis, the nanocrystal memory devices using Co and Ni as charge trapping center have been fabricated and studied due to the higher work-function, better gate coupling ability and lower fabricating temperature. In addition, the most common

methods to form nanocrystal structures are by the self-assembled characteristic of thin film, aggregation by the over-saturation, and different oxidized tendency between elements. Many improvements of the aforementioned methods have been discussed and proposed.

In the self-assembled system, a novel nanocrystal structure has been fabricated by annealing the Ge-incorporate NiSi (NiSiGe) film. After a RTA process, it is found that the annealed NiSiGe film shows a larger nanocrystal size (~8-9nm) and lower density distribution ($3.02 \times 10^{11} \text{ cm}^{-2}$) than the conventional NiSi nanocrystal. The large size and lower density of nanocrystal are due to the internal Ge elements that provide an easier crystallization and enhance the nanocrystal formation. Furthermore, the NiSiGe nanocrystal memory device shows a 9V of memory window under $\pm 10\text{V}$ operation in capacitance-voltage measurement due to the improved nanocrystal formation process. In the retention test, the NiSiGe nanocrystal memory device also has a 2.4V of memory window after 10^4 sec measurement.

Ion implantation can control the nanocrystal aggregation sites and density by adjusting the energy and dosage of the implantation. However, the implantation method also brings a drawback of oxide damage. Therefore, a co-evaporation has been proposed to fabricate nickel nanocrystal structure. The co-evaporation to form Ni nanocrystal reveals double- and single-layer structures after 700 and 800°C

annealing process, respectively. The distributed nucleation sites provided by the co-evaporation bring a double layer distribution. The double layer nanocrystal device shows an 8V memory window due to a higher nanocrystal density. However, the 800 °C-annealed device has an extra high density distribution ($\sim 4.5 \times 10^{12} \text{cm}^{-2}$) even if the device only has single layer structure. In the retention test, the 800 °C-annealed sample also can keep a 2.3V memory window due to a improvement of dielectric layer surrounded the nanocrystal.

Several literatures have studied the segregation of the nanocrystal by the difference of the oxidation free energy between the elements. A reactive sputtering has been used to fabricate the Co nanocrystal structure to avoid the over-oxidation of the charge-trapping layer. In the reactive sputtering process, the deposited CoSi_2 thin film is oxygen-doped or partially oxidized. After a 700°C RTA process, it can be found that Co nanocrystal were aggregated on the tunneling oxide obviously. The size and density of the nanocrystal are about 5-6nm and $3.2 \times 10^{12} \text{cm}^{-2}$, respectively. The nanocrystal memory device shows a 7V memory window under $\pm 15\text{V}$ operation. In the retention characteristic, the memory device also can keep a 3.1V memory after 10^4 sec measurement.

Low-temperature oxide deposited technology is critical for the next generation NVM device. In this work, the combination of nanocrystal structure and nitric acid

oxidation has been studied. The decomposition of HNO_3 as powerful oxidizing agent can provide a high concentration of atomic oxygen to oxidize the immersed metal or semiconductor layer. It can be found that the CoSi_2 nanocrystal memory device with nitric acid oxidized ZrO_2 film as tunneling oxide shows a 10V memory window and 2.1V of memory window in the retention measurement. The nitric acid oxidation is advantageous to improve the thermal budget issue of the thermal oxide demand of the conventional nanocrystal memory devices because the higher fabrication temperature of the NVM devices is determined by the nanocrystal.

Keywords: Nanocrystal; Nonvolatile memory; Nickel silicide; Cobalt silicide; Nitric acid oxidation.



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2010 年季夏於新竹交大

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Chapter 1

Introduction

1.1 Overview of floating-gate memory device

Recently, floating-gate (FG) structure devices are the mainstream technology for the nonvolatile memory. It was invented by Kahng and Sze at Bell Labs in 1967 [1.1]. The FG structure is shown in the Fig 1-1. A modified FG structure device called flash memory was proposed by Fusio Masuoka et al in 1987, which is the most important one member of the FG family [1.2]. The structure and operation of the flash are similar as the original FG memory device. However, the flash memory device uses an additional erase contact, which can reduce the erase time by a block erase mode. In addition, the flash memory devices can be classified into two types, NOR and NAND flash memories, according to their functions and advantages. The NOR Flash offers faster read speed and random access capabilities, making it suitable for code storage in devices. In contrast, the NAND memory, which offers faster write/erase capability and higher density, is typically used for storing large quantities of data [1.3].

1.1.1 Operation of the floating-gate memory device

The basic operation of the memory device is by applying positive voltage on the control gate to promote the electron in the channel to pass through the tunneling oxide and store in the poly-silicon FG under the write mode. The stored electron in the FG

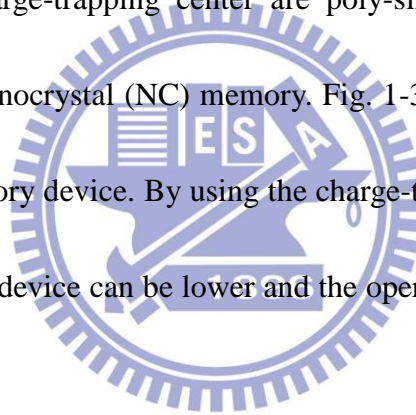
induce a positive threshold voltage shift (ΔV_T) as the “1” state for the memory device. In contrast, the stored electrons will tunnel back to the Si substrate when a negative voltage is applied to the control gate electrode in the erase mode. Then, the ΔV_T is think as the “0” state of the memory device. Based on the advantages of the FG structure such as low-power, easy process and compatibility with the current complementary-metal-oxide-semiconductor (CMOS) process, FG nonvolatile memory structures have attracted much attention on the portable products especially for the cell phone, mp3 player and digital camera.

1.1.2 Challenge of the conventional floating-gate structure

According to the 2009 International Technology Roadmap for Semiconductors (ITRS) for flash memory as shown as the Fig. 1-2 [1.4], tunneling oxide thickness must be thinner than 8-nm to assure enough gate control ability to reduce the short-channel effect. In the vertical scaling, the thinner tunneling oxide leads to high leakage current and poorer charge retention for the memory device. Furthermore, after endurance test, traps can be generated in tunneling oxide, which may induce a leak path in the tunneling oxide and results in a serious leakage current. In addition, in the lateral scaling limit, the space between devices is reduced [1.5]. When one device is written or erased, the nearby memory cell may also be written or erased. Therefore, these difficult trade-off problems hinder the device scaling.

1.2 The solutions for the down-scaling memory device

To overcome the trade-off problems of the FG memory, discrete trapping center instead of electrically continuous poly-silicon FG have been received much attention in the recent years. Unlike to the poly-silicon gate, the charge-trapping layer memory devices stored charges in the distributed centers. Therefore, even if an intrinsic defect or extrinsic defect chain exists in the tunneling oxide, the memory device still can provide correct information because only partial stored charge will be lose. The main structures of discrete charge-trapping center are poly-silicon/oxide/nitride/oxide/Si (SONOS) memory and nanocrystal (NC) memory. Fig. 1-3 illustrates the structure of the SONOS and NC memory device. By using the charge-trapping layer structure, the operational voltage of the device can be lower and the operational speed of the device can be improved further.



1.2.1 SONOS structure memory device

An original idea for the SONOS device is proposed by Wegener et al in 1967 [1.6]. Wegener using an additional silicon nitride placed in between the control gate and tunneling oxide to be charge-trapping layer. The silicon nitride can provided a trap density of the order 10^{18} - 10^{19} cm^{-3} to cause a ΔV_T for the memory device. In the early 1970s, the initial device structure was p-channel metal-nitride-oxide-silicon (MNOS) structures. The devices use an Al electrode as control gate and thicker

(~45nm) silicon nitride as the charge storage layer. Due to a serious leakage current of the device, a thicker tunneling oxide is essential, which also cause the write/erase voltages of device operation need to be 25-30V. In the early 1990s, n- and p-channel device can be operated by a write/erase voltage of 5-12V due to the improvement of the fabrication. To improve the disadvantages of the original MNOS device, the SONOS structure was proposed. The basic operation and charge storage mechanism are similar as the MNOS device. The SONOS have attracted a lot of attention due to its advantages of include a reduced cell-to cell interference, a high speed operation, a lower voltage operation, improved cycling endurance, and elimination of drain-induced turn-on [1.7]. The SONOS structure uses a poly-silicon gate to replace the Al gate due to the self-aligned process. An additional blocking oxide between the control gate and nitride also can restrain the programmed charge to lose into the gate electrode. In the recent year, High-K material such as Al_2O_3 , HfO_2 and ZrO_2 has also been applied into the SONOS memory device [1.8]. By using a High-K material as the device blocking oxide, the applied gate voltage during write/erase operation will mostly drop in the tunneling oxide. A higher tunnel current can improve the write/erase speed of the device. Also, the use of High-K material can improve the gate coupling conditions because silicon nitride will share the higher applied gate voltage compared with the conventional FG structure. In the improvement of

charge-trapping layer, a band-gap engineering (BE) has been proposed as shown as the Fig. 1-4. By controlling Si/N ratio of the nitride layer, the trap density and band gap of the charge trapping layer can be adjusted [1.9]. The BE SONOS device shows an excellent endurance and retention characteristics. In addition, in the replacement of charge storage layer, a High-K material also is a choice by adjusting the band-gap of the charge trapping layer or the band offset between the tunneling oxide/charge-trapping layer and blocking oxide/charge-trapping layer [1.10-1.11]. In the gate electrode, a metal gate will be next leading role due to the High-K material needs a metal gate to reduce the mobility lowering effect of device. The use of metal gate also can provide energy-band engineering for the SONOS. For example, using a higher work-function material such as TaN, NiSi₂ or Mo, the tunnel current from the control gate can be reduced during the erase operation. Therefore, an erase saturation of the device will be avoided. In the device structure, 3-D SONOS such as double-gate, tri-gate and gate-all-around is critical for the next generation memory device [1.12-1.15]. However, the theoretical modeling for the devices is difficult due to the non-uniform electric field distribution and non-uniform charge storage. The SONOS device also can store 2-bit by a cell due to the localization of trapped charge. By channel hot electron injection (CHI) to program device, charge can be controlled to write near the source or drain side as shown as the Fig. 1-5. Then, the memory

devices will have four kind of V_T to be four stored states.

1.1.2 Nanocrystal structure memory device

The idea of NC structure using discrete nanodots as the charge-trapping centers is similar as SONOS memory device. When a thin film (~6-8nm) was deposited, a followed annealing process may induce the thin film to aggregate and form NC to reduce the system energy. The NC also can provide trapping sites by itself or the traps created by NC and its surrounded oxide. The advantages of the NC include immunity to stress induce leakage current (SILC), lower power consumption, higher write/erase speed and lower process cost. The NC nonvolatile memory device also can be 2-bits storage because the device operated by charge trapping mode, which is similar as SONOS device. In the research of NC, to control the size and density of NC is important because the uniformity of NC becomes critical when the device is down-scaling. Therefore, several high-density NC technologies have been proposed to improve the NC characteristic [1.16-1.17]. A double NC layer structure also attracts much attention due to the higher NC density [1.19-1.20]. By choosing a different NC material, a band-gap engineering of double NC as shown as Fig. 1-6 can improve the performance of the memory device because the bottom layer NC with a lower work-function can restrain the stored charge to loss [1.21]. Also, High-K material is potential to fabricate blocking oxide or the NC surrounded oxide [1.22]. The NC can

also combine with the SONOS structure to create more charge-trapping sites for the memory application.

1.3 The further study of the nanocrystal memory device

To apply NC structure into the memory device, more detailed studies are very critical. A suitable can reduce the NC fabricating cost and obtain excellent NC uniformity, which bring a better electrical performance of the memory devices.

1.3.1 Formation of the nanocrystal structure

Generally, the most common NC fabricating methods are by self-assembled characteristic of thin film, selective oxidation, and over-saturation of the doped elements.

(a) Self-assembled system:

Self-assembled system has been studied for the nanodot or nanowire structure extensively. Fig. 1-7 is the schematic illustration of the driving forces in the self-assemble system [1.23]. The most importation driving force for the aggregation of NC is the relaxation of film stress. To reduce the intrinsic energy of the system, the atom will bond and form a sphere. However, the aggregation of the atoms is limited by the surface mobility. The surface mobility is depended on the diffused ability of elements. A rapidly thermal annealing (RTA) process after the film deposition is critical after to enhance the atoms of the thin film to diffuse and

bond. The density and size of the NC is also depended on the annealing process.

The first step of the aggregation is the diffusion of initial elements during the thermal annealing. Then, nuclei are nucleated due to the collisions. The NC grows, where by diffusing atoms bond to existing nuclei. As the NC grows to touch the nearby NC, the smaller NC will merge with larger NC. The density of NC will decay and size of NC will be larger.

(b) Selective oxidation system:

In the case of SiGe system, during the oxidation process, the difference of oxidized ability between Si and Ge cause the external oxygen elements tend to react with the Si elements during the thermal oxidation process. It brings that a selective oxidation process to enhance the Ge aggregation as the NC embedded in SiO₂ dielectrics layer. The chemical reaction process can also be used in the silicide system as NiSi, CoSi and PtSi [1.24-1.25]. The advantage of the oxidation process is the oxidation always brings a lower thermal-budget than the self-assembled system due to the oxidation process can enhance the aggregation. In addition, the formed NC have better size and density distribution. However, the time or temperature during the oxidation process must be controlled carefully to avoid over-oxidation.

(c) Over-saturation:

The segregation of NC also can be procured by over-saturation mechanism. The method is common in fabrication of optical devices. The process is to dope metal or semiconductor ions into dielectric layer by an ions implantation. Based on each dielectric material has its specific solid solubility, a followed annealing process will cause the excess of dose will be segregated. The segregated dose will diffuse in the dielectrics layer and form NC.

1.2.2 The material of the nanocrystal

With different applications, to find an adaptable material to satisfy the requirements is a major subject. In addition, the uniformity and density of NC distribution are the essential issue for the NC formation engineering. Generally, the common material of the NC can be divided into (a) semiconductor (Si, Ge and GaAs) (b) dielectric (GeO_2 , CoO and HfO_2) and (c) metallic (Ni, Co, NiSi_2 and Pt). Semiconductor-based NC is first NC, which can avoid the issue of the metal contamination but have a higher formation temperature. In addition, semiconductor-based NC is potential to fabricate the optical devices such as laser or solar cell due to that the band-gap of the NC can be controlled by quantum confinement effect. In the dielectric NC, more charge storage sites such as the concept of SONOS device will be created by distributed charge storage sites between the NC and its surrounded oxide, which may provides a better retention behavior. The

disadvantages of the dielectric NC is its gate voltage coupling efficiency. The High-K trapping layer may be the solution for the issue. The metallic NC has attracted much retention because more charge storage sites can be provided due to the metal has more density of states. The metallic NC also has a lower quantum confinement effect compared with semiconductor-based NC. It is also believed that a high work-function NC provided by the band engineering can restrain the stored charge to tunnel back to channel and improve the device reliability characteristics.

1.2.3 Motivation

The FG memory faces a challenge in down-scaling device. Among the reported literature, a structure with distributed NC as charge storage sites is considered a potential solution to replace the conventional memory structure. Many different researches of the NC such as the development of material, the improvement of performance and the electrical operation of NC device have been reported in recent years. The most important topic for the NC formation included easy process, lower formation temperature and better NC distribution. In the thesis, several improved methods for NC nonvolatile memories have proposed.

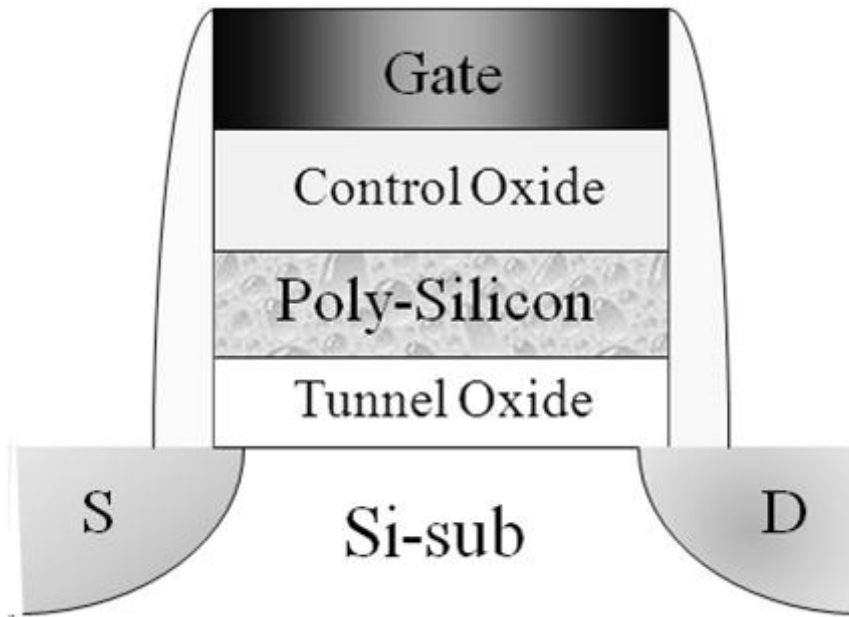


Fig. 1-1 The floating-gate memory device.



<i>Year of Production</i>	2009	2010	2011	2012	2013	2014	2015
A. Floating Gate NAND Flash							
Tunneling oxide thickness (nm)	6-7	6-7	6-7	6-7	6-7	6-7	6-7
Interpoly dielectrics material	ONO	ONO	ONO	High-K	High-K	High-K	High-K
Control gate material	n-Poly	n-Poly	n-Poly	Poly/metal	Poly/metal	Poly/metal	Poly/metal
Highest W/E voltage (V)	17-19	17-19	17-19	15-17	15-17	15-17	15-17
Endurance (erase/write cycles)	1.00E+05	1.00E+05	1.00E+05	1.00E+04	1.00E+04	1.00E+04	1.00E+04
Nonvolatile data retention (years)	10-20	10-20	10-20	10-20	10-20	10	5-10
B. Floating Gate NOR Flash							
Tunneling oxide thickness (nm)	8-9	8-9	8-9	8-9	8	8	8
Gate length L_g physical (nm)	110	110	100	100	90	90	90
Interpoly dielectrics material	ONO	ONO	ONO	ONO	High-K	High-K	High-K
Highest W/E voltage (V)	7-9	7-9	7-9	7-9	6-8	6-8	6-8
Endurance (erase/write cycles)	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+06	1.00E+06	1.00E+06
Nonvolatile data retention (years)	10-20	10-20	10-20	10-20	20	20	20

Manufacturable solutions are not known.
 Solutions are known.
 Solutions are existed.

Fig. 1-2 2009 ITRS roadmap [1.4].

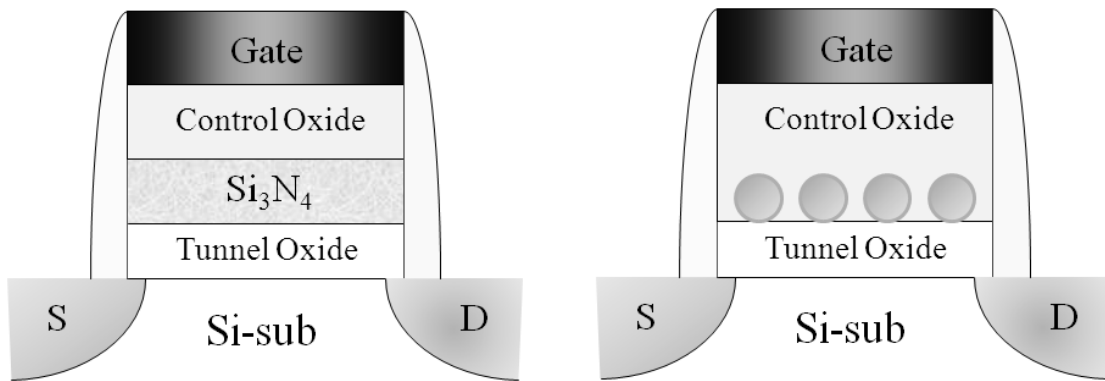


Fig. 1-3 The SONOS and NC memory devices.

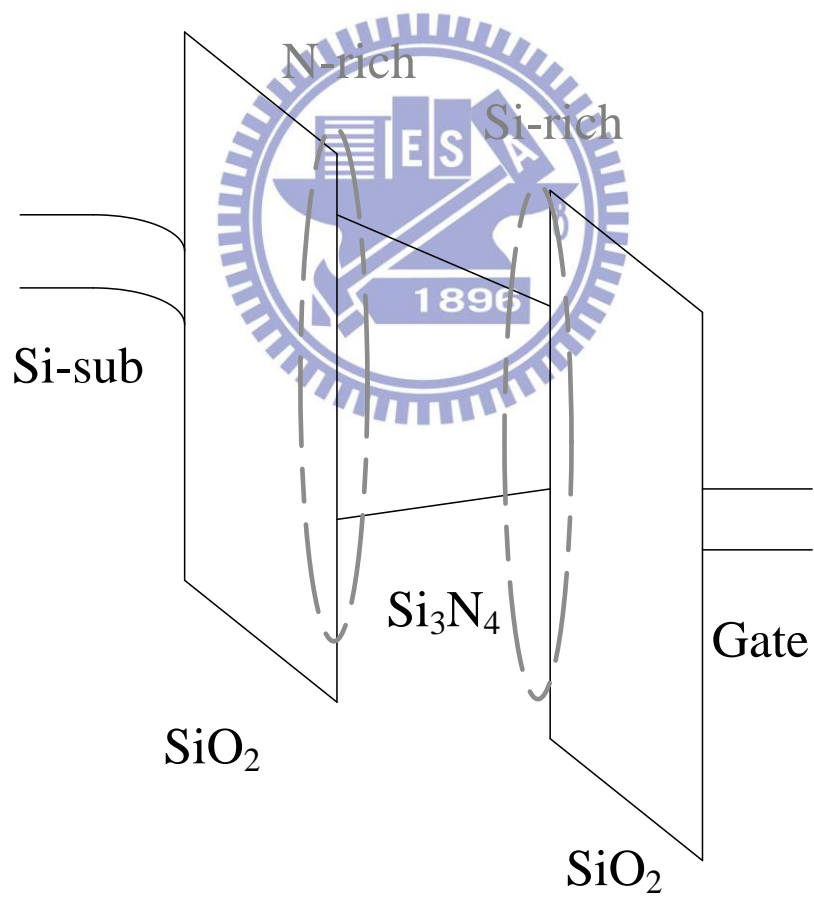


Fig. 1-4 The BE SONOS memory devices [1.9].

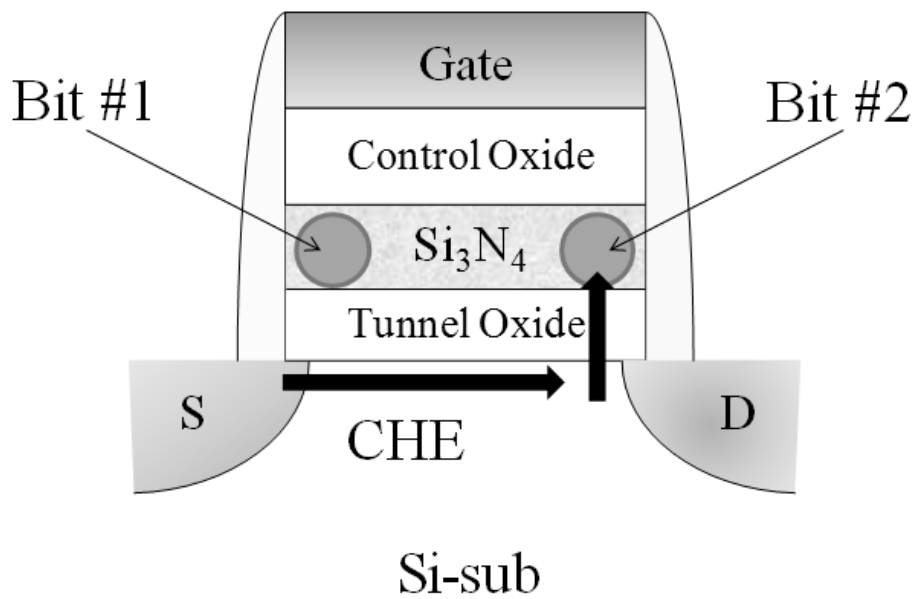


Fig. 1-5 2 bit per cell for SONOS memory device.

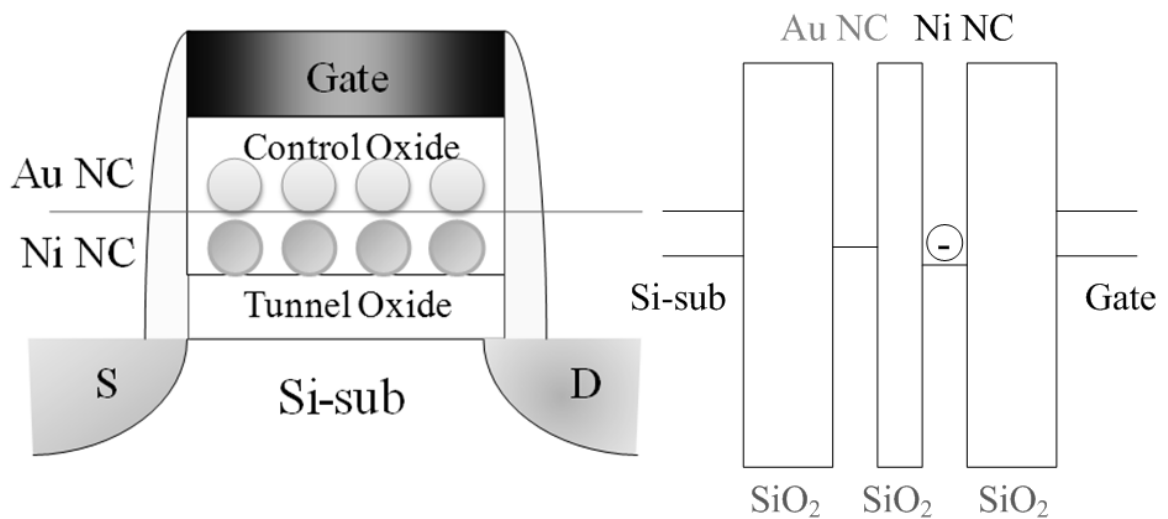
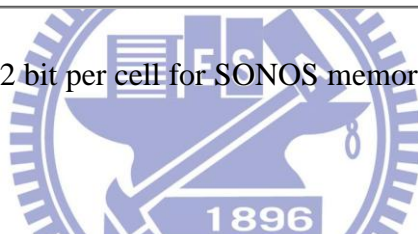


Fig. 1-6 Double layer NC memory device.

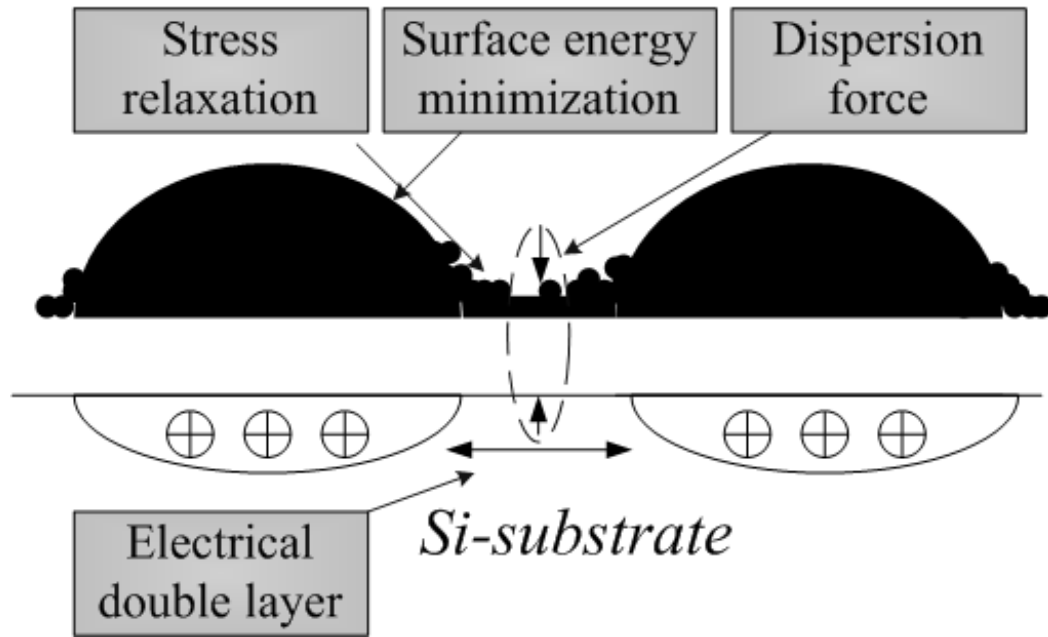
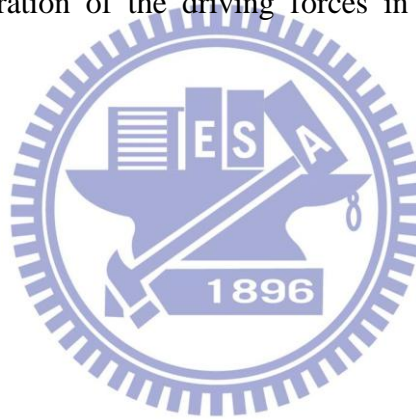


Fig. 1-6 Schematic illustration of the driving forces in the self-assembly process

[1.23].



Chapter 2

Basic Principle of Nonvolatile Memory

2.1 Introduction

The states of NVM memory can be defined by threshold voltage V_T of the transistor, charge displacements, or resistance change. If electrons have to be stored in a cell of the memory, the ΔV_T of a Flash transistor can be written as [2.1]:

$$\Delta V_T = -\frac{\bar{Q}}{C_{FC}}$$

where \bar{Q} is the charge weighted with respect to its position in the gate oxide, and the capacitances between the FG and control gate. Fig. 2-1 shows the ΔV_T between two states in a Flash memory. It can be found that the threshold voltage of the memory cell is changed by charging the amount of electron or hole between the gate and the channel, corresponding to the two states of the memory cell, i.e., the binary values (“1” and “0”) of the stored bit.

In this chapter, the write/erase mechanisms of the memory device will be discussed by the relation between gate bias and energy band diagram of the transistors. We also demonstrated the detailed operation of the device such as the tunneling injection, channel hot electron injection, and band to band assisted electron/hole injection. Finally, the reliability characteristics of nonvolatile memory such as

retention and endurance tests have also been discussed.

2.2 Basic write and erase mechanisms

The nonvolatile memory device included NC and SONOS memories is changed its state by writing or erasing the stored electrons. In exact definition for the memory cells, “erase” is to change the state of a group of memory cell and “write” is to change the state of one cell. However, the definition is too difficult to differentiate the transmission of carrier. Therefore, we define when electrons are injected into charge-trapping layer is called “write” and when the stored charges are de-trapped to silicon substrate is called “erase”.

2.2.1 Energy band diagram during write and erase operation

Fig. 2-2 illustrates the defined write/erase physical operation of a NC memory device. In the write operation, a positive voltage is applied on gate electrode relative to the p-type substrate, which forms an electron channel. Then the electrons tunnel through the tunneling oxide into the charge-trapping layer and are stored in NC. Some electrons not trapped in the NC are also possible to tunnel through a blocking oxide into the gate electrode. The trapped electrons result in a ΔV_T of the transistor. In the erase operation, the gate electrode is on a negative voltage bias, the trapped electrons can be de-trapped into the conduction band of the NC and then tunnel back to the channel of Si substrate. It is worth noted that the de-trapped process is the main

parameter to affect the erase speed of the device. To improve the erase speed of the memory device, the holes tunnel becomes very important. In the erase operation, the applied negative voltage bias also can enhance the holes tunnel from the substrate into the NC and are partially trapped in the trapping layer. The ΔV_T results from the trapped electron and hole are neutralized.

2.2.2 Carrier injection mechanisms

Tunneling Injection-

In 1924, De Broglie had proposed the matter wave or de Broglie wave theory. The matter wave theory indicates that the motion of a particle can be thought as a wave in the quantum size as shown as Fig. 2-3. Therefore, tunneling injection is reasonable because a particle becomes possible to pass through wall or a barrier motion of the wave. The Schrödinger equation provided by Erwin Schrödinger accomplished the theoretical framework and calculates.

$$T = \exp\left(-2 \int_0^d \frac{\sqrt{\phi(x) * m_e}}{\hbar} dx\right)$$

In the tunneling theory, tunneling probability is depended on electron barrier height ($\phi(x)$), tunnel dielectric thickness (d), and effective mass (m_e) inside the tunnel dielectric [2-2].

Based on the tunneling theory, the electronic started to discuss the tunneling

possibility for the electrical devices especially when the device is down-scaled to nanometer scale. For the memory device, several tunneling processes such as Fowler-Nordheim tunneling (FN), Direct tunneling (DT), trap assistant tunneling (TAT), modified Fowler-Nordheim tunneling (MFN) have also be studied successively. Today, the tunneling processes also affected the operation and performance of the memory device.

1. Fowler–Nordheim tunneling

The Fowler–Nordheim (FN) tunneling is the most important tunneling effect for the memory device as shown as the Fig. 2-4. The FN tunneling always occurs in a strong electric field (about 8–10MV/cm). In a strong electric field, the height and thickness of the barrier is changed. Then, the electrons have more chance to pass through the barrier wall from a metal or and semiconductor and arrive at the other side of the barrier wall. By the Wentzel–Kramers–Brillouin (WKB) approximation and free-electron gas model [2.3]. The equation of the FN tunneling can be obtained as the followed as [2.4]:

$$J = \frac{q^3 F^2}{16\pi^2 h^2 \Phi_B} \exp \left[\frac{-4(2m_{OX}^*)^{1/2} \Phi_B^{3/2}}{3\hbar q F} \right]$$

In this equation, Φ_B is the barrier height, m_{OX}^* is the effective mass of the electron in the forbidden gap of the dielectric, h is the Planck's constant, q is the electronic charge, and F is the electrical field through the oxide. The FN tunneling is

the original write and erase method for the FG memory device especially for a thicker tunneling oxide. The write and erase by the FN tunneling is easier because only the gate electrode is used. However, the drawback for the FN tunneling is that it needs a higher oxide field but has slower write speed.

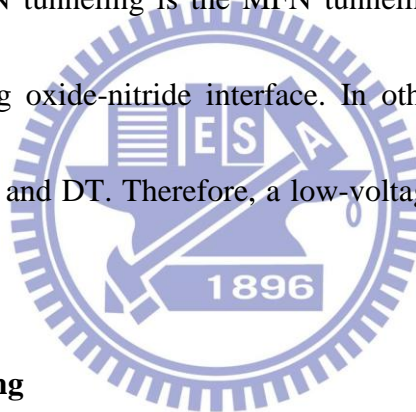
2. Direct tunneling

Different from the F-N tunneling, the Direct Tunneling always occurs in the thinner barrier wall or dielectrics layer. According to the equation of the tunneling theory, the tunneling possibility is increased as the thinner of the barrier. For the electrical device, the DT becomes an important issue for the successively down-scaling. With the device scaling, the gate oxide needs to be thinner to assure the device has enough gate control ability. However, the gate leakage current increases seriously. Then, the researcher modifies the gate oxide from the conventional SiO_2 to be SiON [2.5]. Recently, High-K materials (such as HfO_2 , Al_2O_3 and ZrO_2) become the major topic for the next generation MOSFET device as shown as the Fig. 2-5 [2.6-2.8]. In the NC memories, the NC usually uses a thinner oxide (the thickness is less than 3nm) as the device tunneling oxide. Therefore, the direct tunneling, which with the advantages of fast write/erase and low operation voltage, is the main operation model for the device writing or erasing. In addition, the direct tunneling also affect the reliability performance of the memory. The charge stored in the NC is

possibly tunnel back to the channel. Fortunately, the charge always stored in the defects existed in the surface between the NC and dielectrics. Moreover, we also can use a metal with larger work function such as Au or Pt to improve the device performance [2.9-2.10].

3. Modified Fowler–Nordheim tunneling

Modified Fowler–Nordheim (MFN) is observed in SONOS memory device. The principle for the MFN tunneling is similar to the FN tunneling. The main difference between the MFN and FN tunneling is the MFN tunneling need to pass a distance further from the tunneling oxide-nitride interface. In other words, MFN tunneling includes the FN tunneling and DT. Therefore, a low-voltage operation is possible for the SONOS device.



4. Trap assistant tunneling

Trap Assistant Tunneling is based on the initial tunneling theory. As the wall barrier exists some defects, the carrier transmission not only by the pure tunneling or emission. The defects can provide an additional route to pass through the barrier height. In addition, in the NC or SONOS memory devices, the trap assistant tunneling also affects the retention behavior.

5. Channel hot electron injection (CHEI)

An electron traveling from the source to the drain can obtain energy from the

lateral electric field and loses energy to the lattice vibrations (acoustic and optical phonons). When the applied electrical field exceeds this value, electrons are “heated” by the high lateral electric field, and a small fraction of them have enough energy to pass through the barrier between oxide and silicon conduction band edges as shown as the Fig. 2-6. Then, we called the electrons as channel hot electron (CHE) [2.12]. In the other hand, the effective mass of hole is heavier than one of electron and the barrier height for hole is higher than electron in the SiO₂ system. Then, it is difficult to obtain enough energy to pass through oxide barrier for hole. The injected electron depends on two factors: (1) the generation rate of electrons at the lateral electric field and (2) the collection rate of electrons for the vertical electric field. In general, the injection efficiency of CHE in n-channel MOSFET device is not high because the vertical electric field is relative to the lateral electric field of transistor. Therefore, a source-side injection (SSI) hot electron device has been proposed as shown as the Fig. 2-7 [2.13-2.15]. In the conventional CHE injection (drain-side), the injected injection efficiency is low even if several electron-hole pairs are generated at a high lateral electrical field because the vertical electrical field is too lower to prompt the generated electrons to inject into the charge-trapping layer. The SSI memory has a higher voltage on the FG but lower voltage on the control gate, which can form a local pitch-off region near the overlapped region. An enough electron-hole pairs are

formed in the pitch-off region and injected into the FG effectively because the vertical electrical field can be larger and do not depends on the control gate. The injected injection efficiency for the SSI device is about 1000 higher than the drain-side injection memory device. However, the SSI also has several disadvantages: (1) the N^+ region of the drain side not an additional drive in process, (2) the cell size is too large to down-scale and (3) the short channel effect is more obvious than the drain-side memory device.

6. Band to band tunneling (BTBT)

Band to band tunneling in the nonvolatile memory was first proposed in 1989. I. C. Chen et al [2.16]. From the experiment results, it is found a high injection efficiency method to writing EPROM devices.

a. Band to band hot electron tunneling injection

Band to band tunneling induced hot electron (BBHE) injection in the p-channel MOSFET device has several advantages of lower power consumption, higher injection efficiency, faster writing speed, and wider electron injection than the CHE injection in the n-channel MOSFET device [2.16-2.18]. Fig. 2-8 shows the energy-band diagram and device operation during BBHE injection. When band-bending of silicon substrate is higher than the energy gap of the semiconductor, hat the electron tunnels from the valence band to the conduction band of Si becomes

significant. The tunneling electrons can be accelerated by a vertical electrical field provide by the positive gate voltage. Then, some of the electrons can get sufficient energy and pass through the potential barrier of oxide. The only drawback of the BBHE injection is it needs a higher oxide field than CHE.

b. Band to band hot hole tunneling injection

In p-type substrate, when a negative gate voltage and a positive drain voltage are applied to the cell, electron-hole pairs are generated by BTBT in the drain region as shown as the Fig. 2-10. The holes are accelerated by a lateral electric field toward the channel region and some of them obtain high energy. The hot holes inject into charge trapping layer through the tunneling oxide and recombine the stored electrons. This injection is used for a new erase operation for nonvolatile memory device [2.19].

c. Negative gate erase (NGE)

“Negative gate erase” is base on the idea of band-band hot hole tunneling injection to erase the stored electron [2.20]. Fig. 2-11 is two different operations of the band-to band hot hole erase. The NGE can reduce the interface damages and subsequent hole trapping due to the large number hot hole provided by the source side under serious reverse bias.

2.3 Basic Reliability of Nonvolatile Memory

The most important characteristic of the memory device is its reliability

characteristics. Especially for the NC device, the down-scaling tunneling oxide causes the storing charge loss more seriously. In general, the reliability of the memory device includes retention and endurance characteristics.

2.3.1 Retention

In the standard of device retention, “ten year” is the criterion for the memory products. In the ten year, the device needs to keep enough charges in the charge-trapping layer to be a correct logical judgement. In my thesis, the common retention measurements include (i) C-V measurement and (ii) C-t measurement. The difference between the C-V and C-t measurement is only the sensed object during the retention test. The C-V measurement senses the flat-band voltage shift (ΔV_{FB}) but the C-t measurement senses a specific capacitance charge with increase of the test time. In addition, the possible causes of charge loss are: 1) by tunneling or thermionic emission mechanisms; 2) defects in the tunneling oxide; and 3) de-trapping of charge from insulating layers surrounding the storage medium; 4) mobile ion contamination.

2.3.2 Endurance

“Endurance” is the ability of the nonvolatile memory to withstand a repeated write and erase cycles. In a conventional Flash memory the maximum number of write/erase cycles that the device must sustain is 10^6 cycles. In the endurance tests, continuous constant pulses are used to extract the write/erase threshold voltage window closure of the device. From the reduction of the threshold voltage with

cycling, we can assure the trap generation in the tunneling oxide or oxide interface. In the NC structure, the reduction can be thought as the failure of partial NC. Fig. 2-10 is the typical phenomenon during the endurance test. The threshold voltage widening is because the hole induced at the interface between the SiO_2 and Si substrate at the write operation. The trapped positive charges lower the tunneling barrier when the device is at the write mode and induces a memory window opening. However, after filling the existing hole trapped during the first few cycles, electron trapping begins to dominate. The electron-trap exists uniformly cross SiO_2 and keeps generated by passing and damaging the SiO_2 , which causes the memory window closure.

2.3.3 Self-converging

In the write/ erase operation, the FG memory device usually can find the erased-threshold voltage has broader distribution as shown as Fig. 2-12. The poly-silicon layer has larger different crystallite in each cell [2.21]. The broader distribution of the erase mode is because the stored charge tunnel back from the poly-silicon layer to the Si substrate. By two step erasing scheme or channel electron induce avalanche can improve the erased- threshold voltage distribution of the device.

2.4 The Basic Physical Characteristic of Nanocrystal NVM

In the NC memory, some quantum effect will affect the device performance such as retention or charge storage ability. The quantum effect is also affected by the size

of NC.

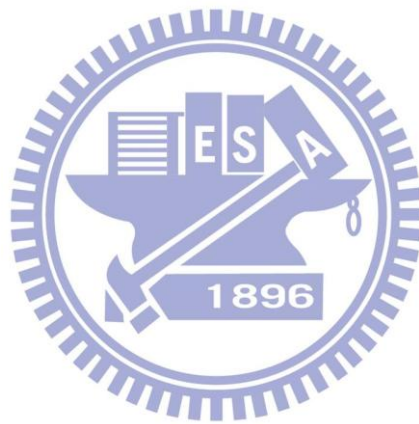
2.4.1 Quantum confinement effect

The quantum confinement effect depends on the NC size has been studied both experimentally and theoretically with the tight-binding model [2.22]. The quantum dot is a quasi-zero-dimensional nano-scaled system. Therefore, the quantum confinement effect becomes significant if the NC size shrinks to the nanometer range. Then, the actual conduction band of the NC increases to be a higher energy level compared with bulk material [2.23]. The quantum confinement effect limits the amount of the total stored charge. An enough NC density becomes important for a clear judgment for the logic circuit. In addition, the quantum confinement effect also can be used to restrain the stored to loss. For example, the double-layer NC can keep a better retention behavior by the raised energy caused by the quantum confinement effect.

2.4.2 Coulomb blockade effect

The coulomb blockade effect means that the potential energy is raised as the electrons are stored in the potential well. For example, if one electron is stored in the NC, the potential energy of the NC is raised as the charging energy $e^2/2C$. C is the NC capacitance, which depends mainly on the NC size, tunneling oxide thickness and control oxide thickness [2.24]. In addition, the electron charge will raise the NC

potential energy and reduce the electric field across the tunneling oxide, resulting in reduction of the tunneling current density during the write process. In the retention tests, we always can find the device shows rapid memory window decay due to the Coulomb blockade effect. Excessive charge during the writing causes the stored charges with the energy higher than the conduction band of Si substrate to tunnel back to the channel. In addition, it is worth to note that the Coulomb blockade effect can be reduced by fabricating appropriate NC size.



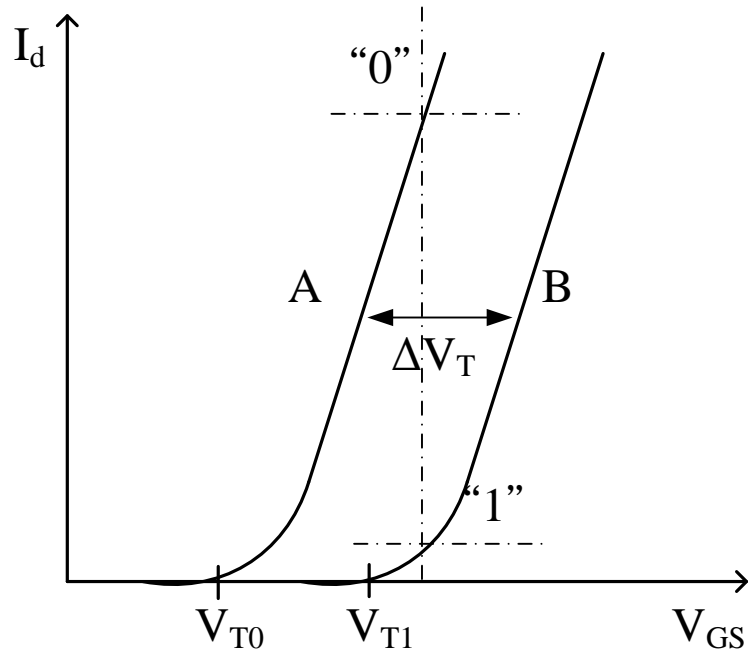


Fig. 2-1 I_D - V_G curves of an FG device when there is no charge stored in the FG (curve A) and when negative charges are stored in the FG (curve B).

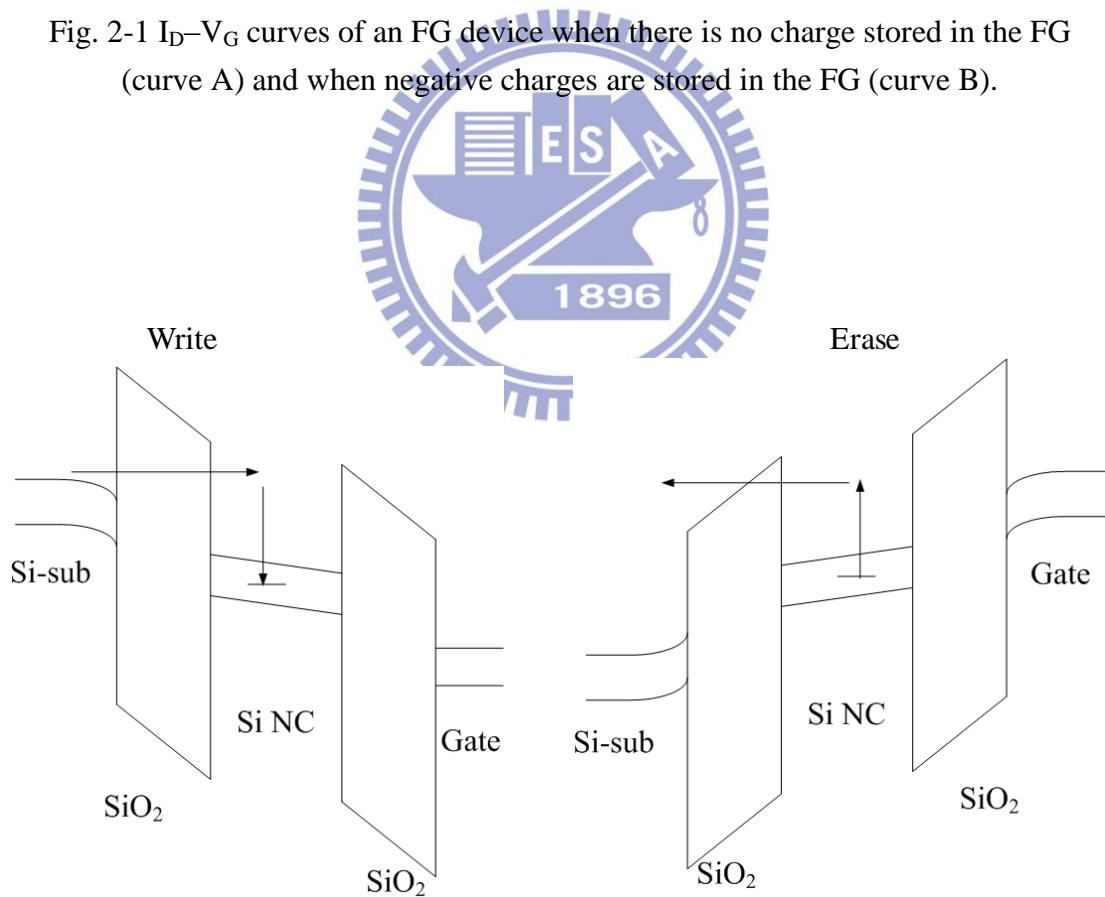


Fig. 2-2 the write and erase mode of the FG memory device.

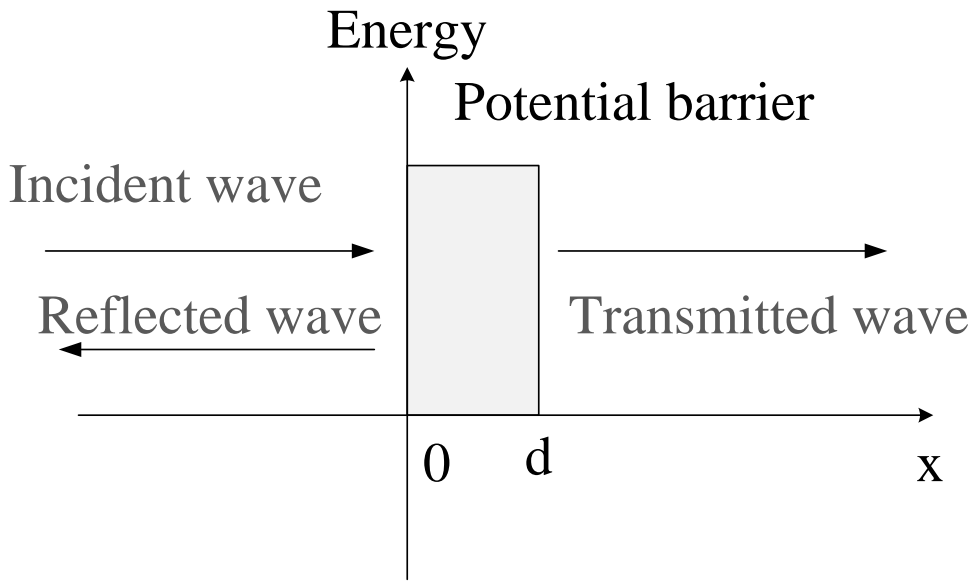


Fig. 2-3 The diagram of tunneling effect.

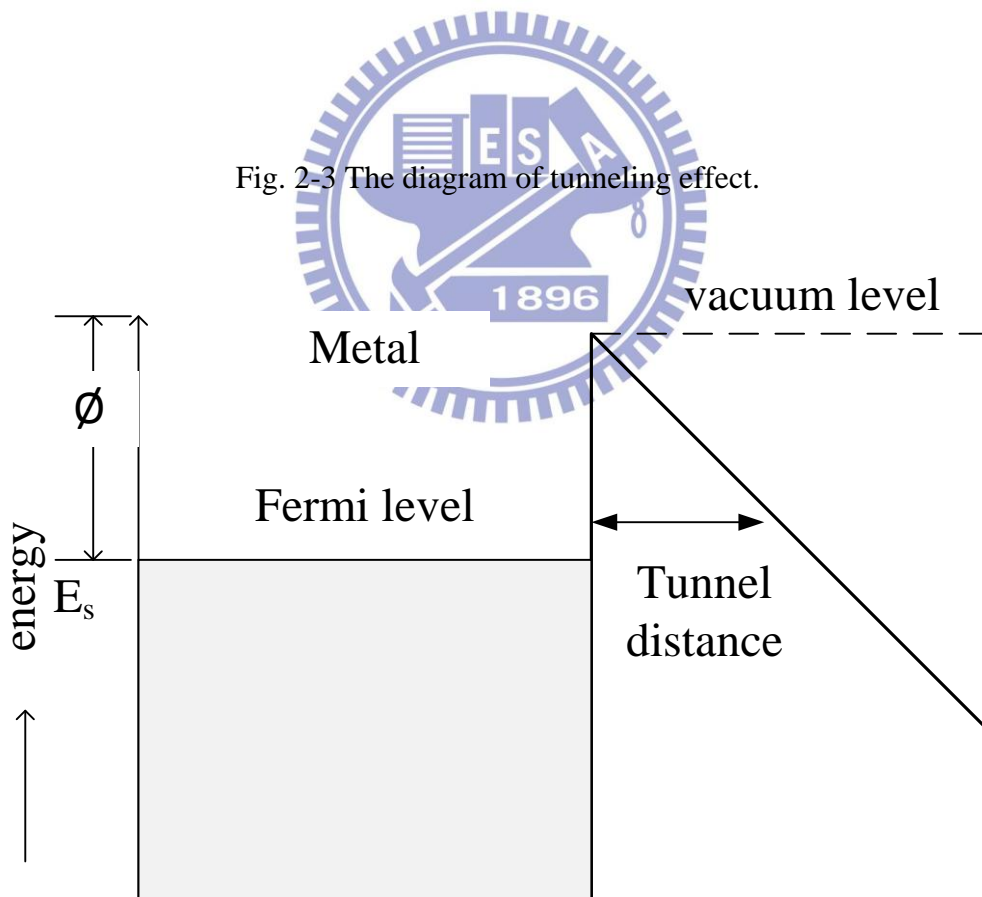


Fig. 2-4 The band-diagram of FN tunneling.

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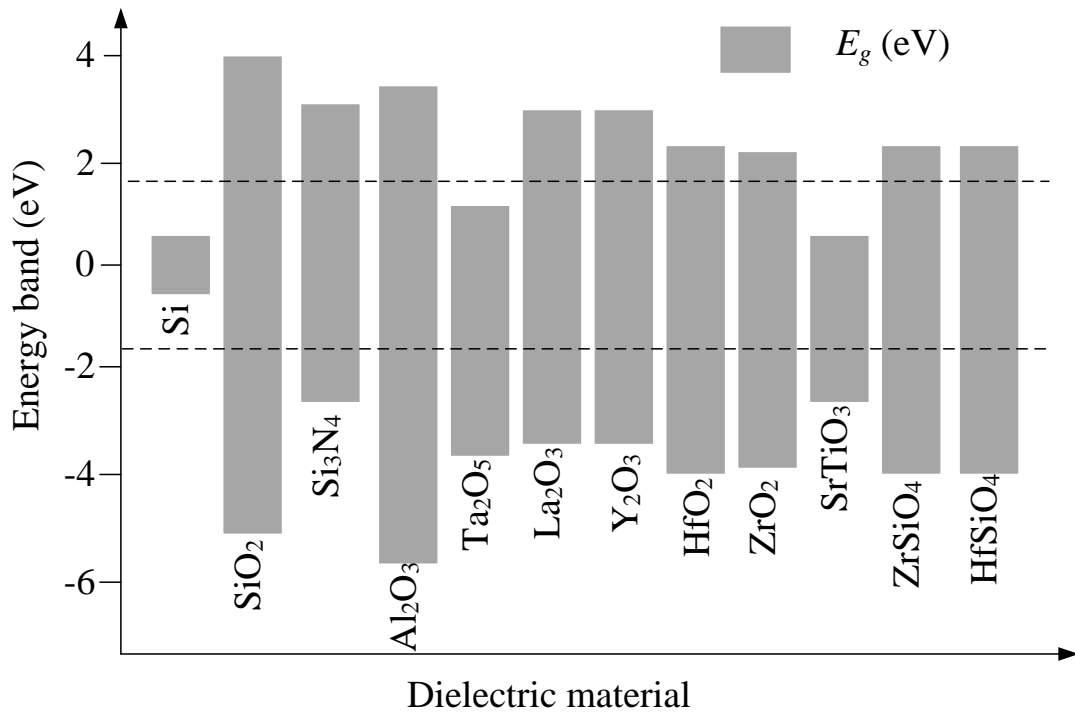


Fig. 2-5 Band gap of the High-K dielectrics.

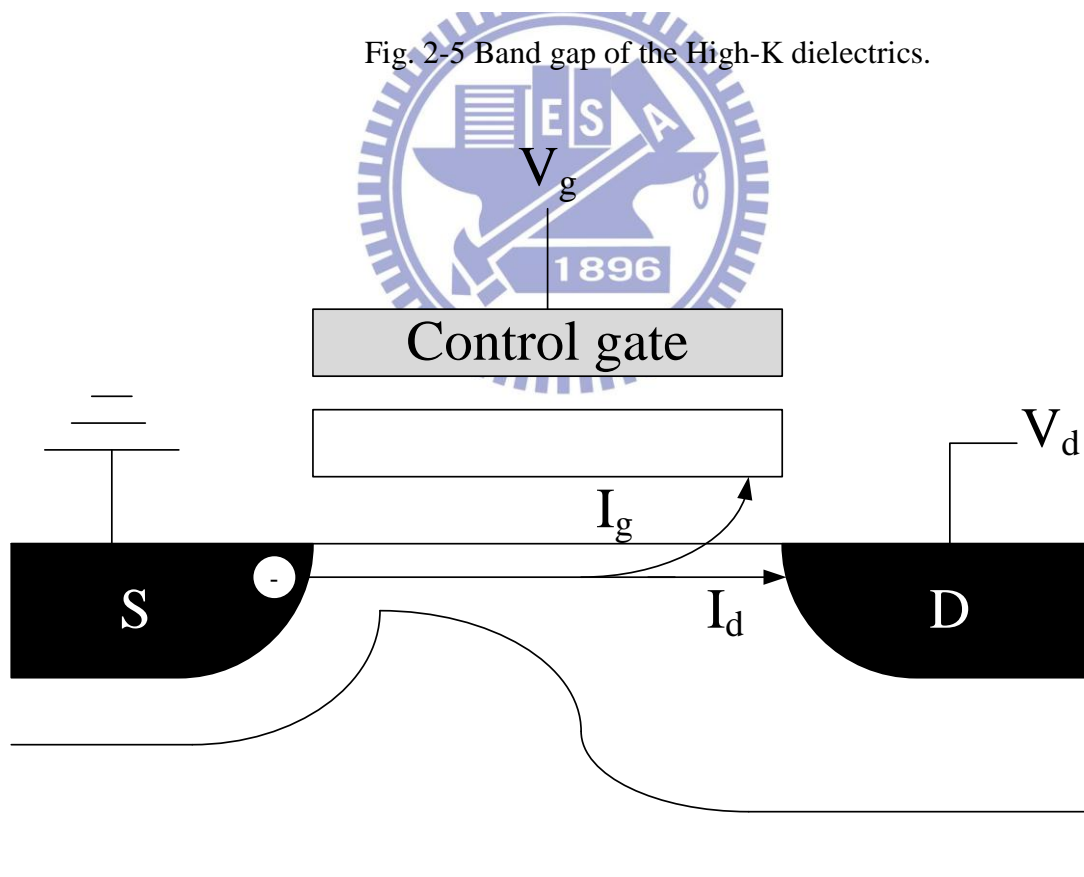


Fig. 2-6 Channel hot electron injection.

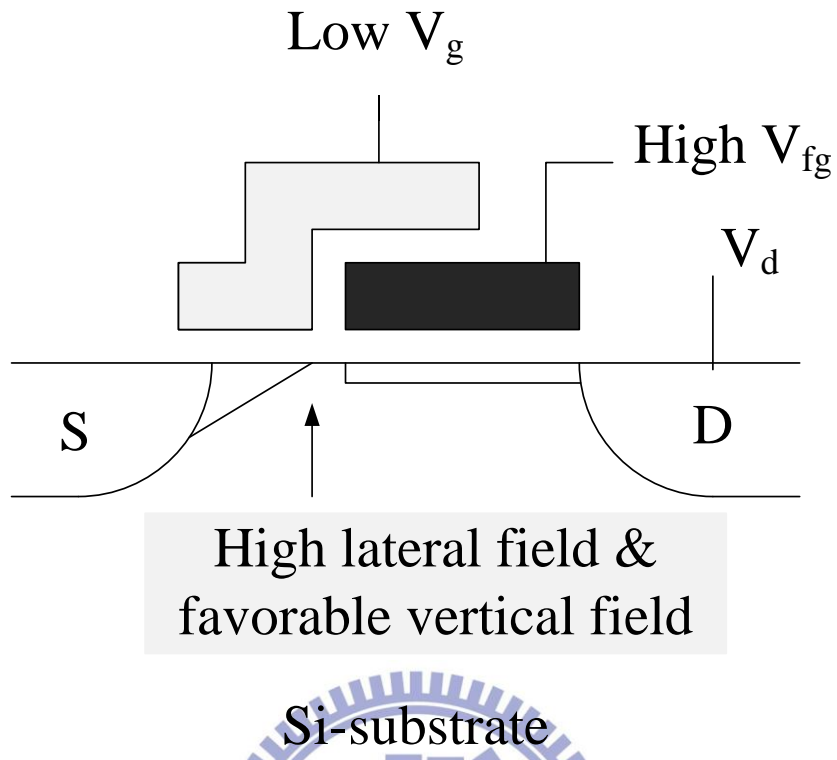


Fig. 2-7 Source-side hot-electron writing

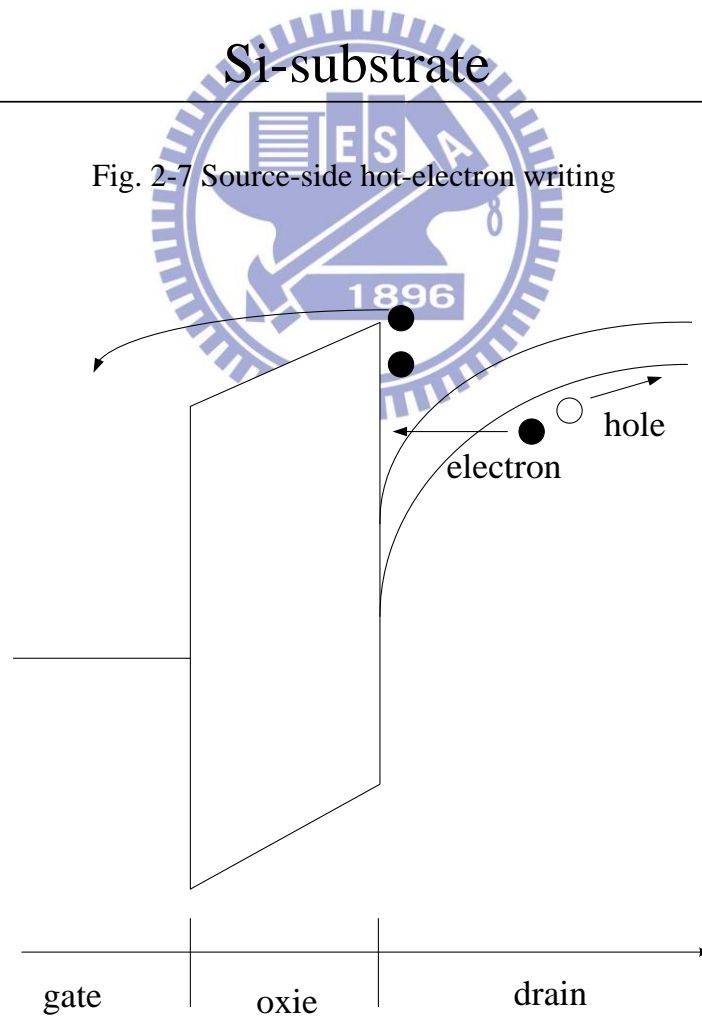


Fig. 2-8 Band to band hot electron injection in p-channel MOSFET.

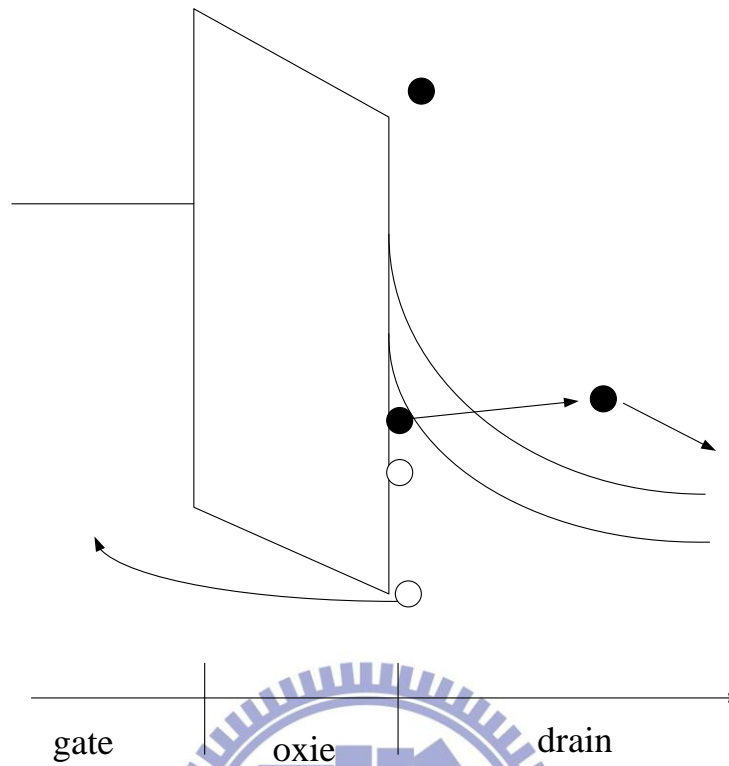


Fig. 2-9 Band to band hot hole injection in n-channel MOSFET.

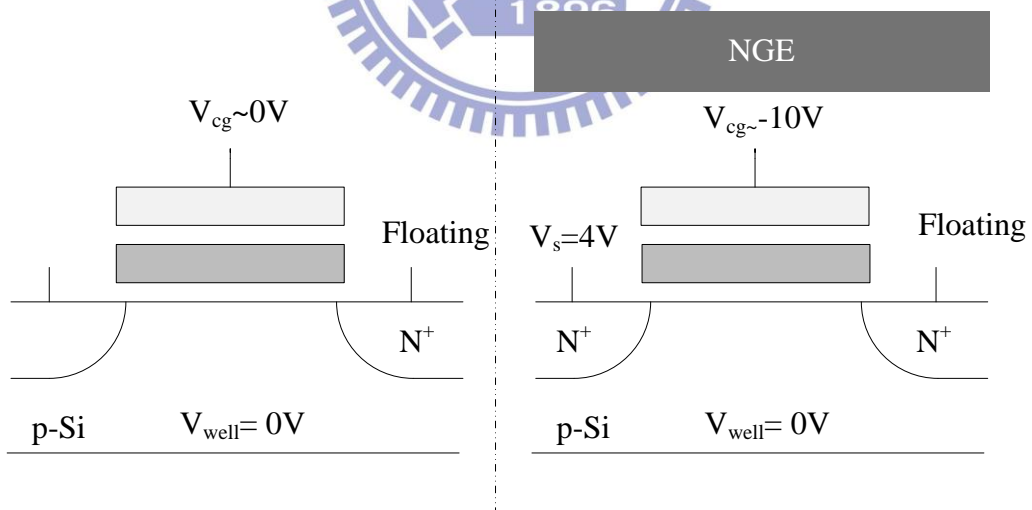


Fig. 2-10 The operation of negative gate erase.

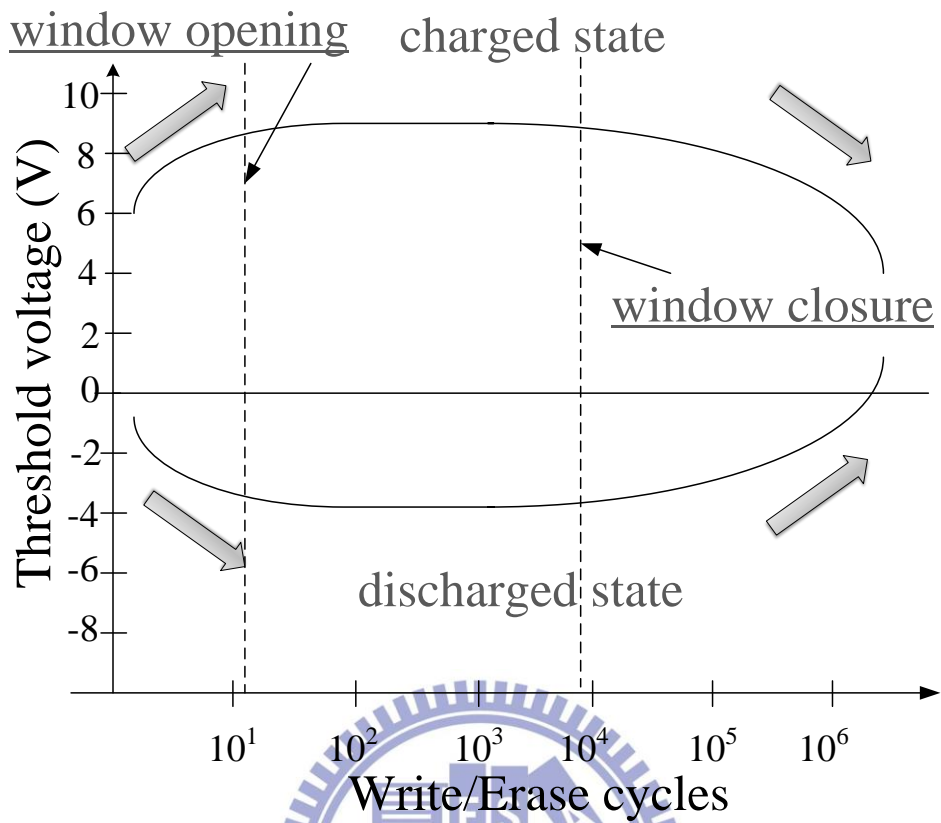


Fig. 2-11 Typical endurance characteristic of memory devices.

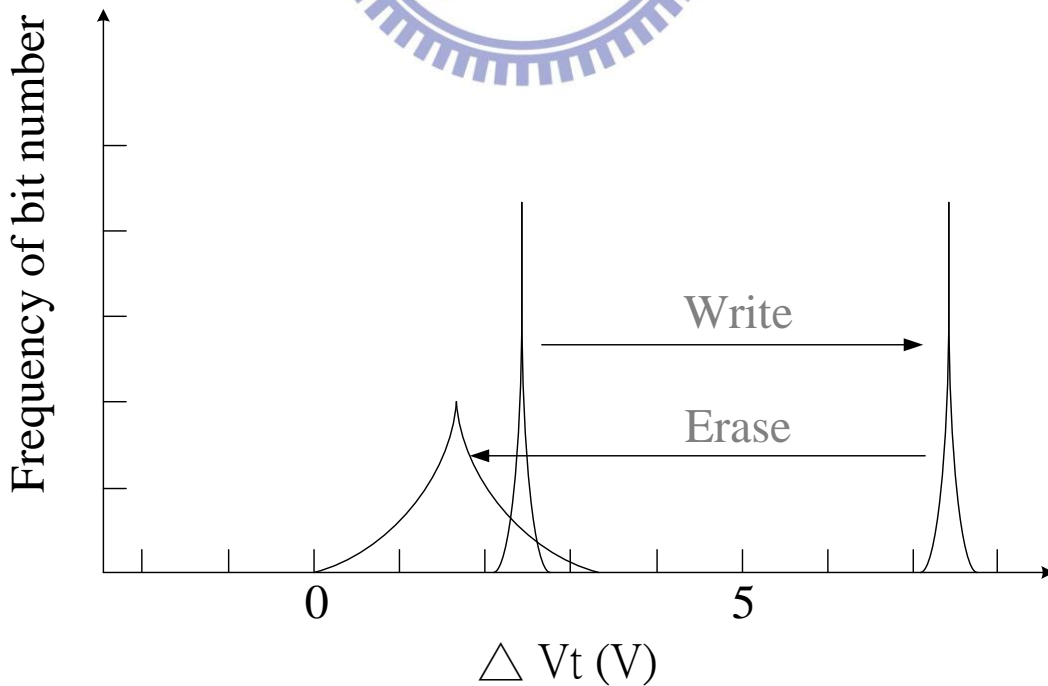


Fig. 2-12 The diagram of the erased-threshold voltage distribution.

Chapter 3

Fabrication and Memory Effect of Ni nanocrystal by Co-evaporating with Dielectric Layer

3.1 The co-evaporating method to form the Ni nanocrystal embedded in SiO₂ dielectric layer for the memory application.

3.1.1 Introduction

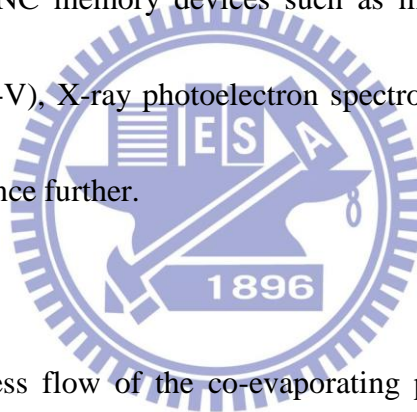
Recently, FG NVM is declared to be end when the tunneling oxide of device is down-scaled to be thinner than 8 nm [3.1]. Therefore, Sandip Tiwari et al. presented NC structure instead of the conventional FG as the novel charge-storage layer [3.2]. The NC is favorable for the next generation NVM because the structure can use the similar fabricating process flow and circuit design as the FG structure. Therefore, a large number of literatures have been proposed to study the NC device such as the fabrication, material characteristics and electrical analyses [3.3-3.5]. In the NC formation, the most common methods to form the NC structure are by the self-assembled characteristic of thin film, different oxidized tendency between elements or additional ions implantation [3.6-3.8]. Among these methods, the ions implantation is the potential one because the method can control the NC aggregation sites and density by adjusting the energy and dosage number of the implantation. However, the implantation method also brings a drawback of the oxide damage,

which may degenerate the reliability characteristic of the memory device.

In this work, we have proposed a co-evaporated method instead of the implantation to prepare the mixed film composed of Ni and SiO₂. After the deposition of the mixed film, a followed RTA process in N₂ ambient for 60sec has used to separate the Ni NC. It is also found that the Ni NC shows double- and single-layer structure at 700 and 800°C RTA condition, respectively. A reasonable forming process for the structures has also been proposed. In addition, the electrical results and material analyses of the NC memory devices such as memory window, retention, current density-voltage (J-V), X-ray photoelectron spectroscopy (XPS) have used to study the device performance further.

3.1.2 Experiment

Fig. 3-1 is the process flow of the co-evaporating process. The fabrication of memory structure was started with a dry oxidation at 950°C to form a 5 nm-thick tunneling oxide on p-type (100) Si wafer which had been removed native oxide and particles by RCA process. Afterward a Ni and SiO₂ mixed film about 9-nm-thick was deposited by the dual e-gun system. In the co-deposition process, Ni and SiO₂ pellets was placed in the respective crucible. The ratio of Ni and SiO₂ was controlled to be about 1:8. Subsequently, a RTA system set at 700 and 800°C was performed for 60sec in N₂ ambient to form Ni NC structure, respectively. After the RTA process, a



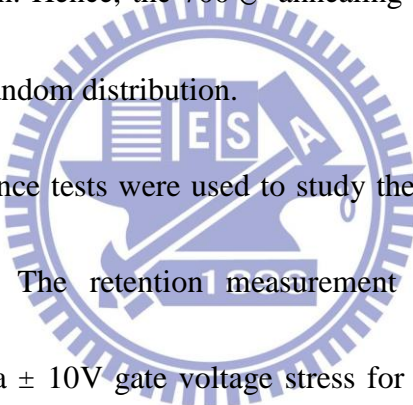
50-nm-thick blocking oxide (SiO_2) was capped by plasma enhanced chemical vapor deposition (PECVD) system. Finally, Al gate electrode was patterned to form metal-oxide-insulator-oxide silicon (MOIOS) structure.

3.1.3 Result and discussion

Fig. 3-2 (a) demonstrate the cross-section TEM image of the mixed film after 700°C RTA process. The double-stacked Ni NC about 5nm were nucleated between the tunneling oxide and blocking oxide randomly. The distribution of the NC is as similar as the reported literatures of the NC structure formed by the implantation [3.9-3.11]. In addition, C-V measurement has also been used to study the charge-storage ability of the Ni NC. Fig. 3-2 (b) is the C-V curves for the double-stacked Ni NC memory device. The bidirectional C-V sweeps were performed from deep inversion to deep accumulation and in reverse, which exhibited a ΔV_{FB} , indicating charge-storage ability of the NC. The NC memory device shows an excellent memory window of 8V under $\pm 10\text{V}$ gate voltage operations. The excellent memory window is attributed to the high density NC distribution.

The XPS analysis of the charge-trapping layer with 700°C annealing condition has been proposed to study the composition of the charge-trapping layer further. In Fig. 3-3 (a) and (b), Ni-Ni peak at about 853eV and Si-O peak at about 103eV were seen obviously during the XPS analysis [3.12]. The results can be evidence to confirm

the formed structure is the Ni NC embedded in the SiO₂ dielectrics layer, which can provide a good memory window for the device application. Then, we also propose the forming process of the double-stacked Ni NC as shown as the Fig. 3-3 (c). During the co-deposition process, nucleation sites for the Ni NC are distributed over the mixed film randomly. With the external energy is a provided, thermal-driving Ni atom tends to diffuse and aggregate to form the NC structure due to the surface energy and the interface stress [3.13]. The Ni NC nucleates randomly in the trapping layer for the nucleation sites distribution. Hence, the 700°C annealing temperature though causes the Ni aggregate but in a random distribution.



Retention and endurance tests were used to study the reliability behavior of the Ni NC memory device. The retention measurement was performed at room temperature by operating a $\pm 10V$ gate voltage stress for 10sec and measured up to 10^4 sec. The memory device keeps about 0.76V at 10^4 sec as shown as the Fig. 3-4 (a). The memory devices show an excellent memory window but a poorer retention characteristic. In the endurance test, a continuous pulse with $\pm 10V$ of gate voltage for 1msec was used to stress the samples. After the stress, a followed C-V measurement was used to observe the variation of the charge-storage ability. As shown as the results in the Fig. 3-4 (b), a negligible decay of memory window is found, which is attributed to that the tunneling oxide is formed by the high temperature furnace process.

To enhance the retention characteristic of the memory device, a higher annealing temperature (800°C for 1min) has been used. However, it is found that the double-stacked Ni NC transfers to single layer structure after the annealing as shown as the TEM result of Fig. 3-5 (a). Also, the reasonable forming process for the single layer Ni NC has also been proposed as shown as the Fig. 3-5 (b). According the reported literature, the NC formation is affected by the annealing temperature strongly [3.14]. The Ni atoms obtained more driving force to move as the thermal temperature increasing to 800°C. It causes that the larger size and lower density of NC aggregated on the tunneling oxide. From the C-V result as shown as the Fig. 3-6, the device provides a 4V memory window under $\pm 10V$ gate voltage sweep. The degenerated memory window is due to that the single layer with lower NC density.

Fig. 3-7 (a) and (b) is the retention and endurance characteristics of the single-layer Ni NC memory device, respectively. It can be found that an obvious improvement of memory window ($\sim 2.3V$) at 10^4 sec in the single-layer Ni NC memory. The device shows a similar endurance characteristic with the 700°C annealed- one due to the same tunneling oxide forming process. To explain the improvement of retention behavior, a J-V characteristic has been proposed to study the leakage current behavior of the devices. As shown as the Fig. 3-8, it can be found the gate current density of the device with 800°C RTA process is about half order of

magnitude smaller than the sample with 700°C RTA treatment. Based on the tunneling and blocking oxide of the devices are formed by the similar process, it can be inferred that the 700°C- sample have additional leakage paths. The additional leakage paths come from the trap of the interface at the charge-trapping layer and the surrounding oxide between NC. The traps cause the current is easier to pass through the capacitor structure during the J-V measurement. A higher temperature during the NC formation can improve the dielectrics layer. Therefore, the device formed by the 800°C RTA process can keep more charge in the retention test.

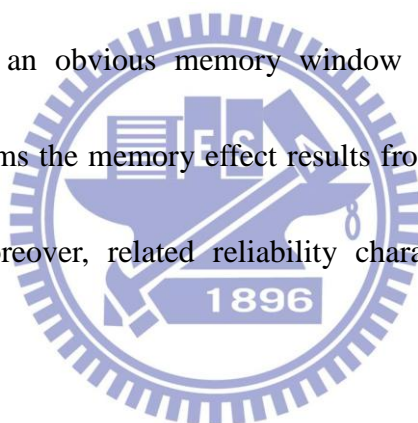
3.1.4 Conclusion

In conclusion, we have demonstrated a co-evaporated method to fabricate the Ni NC structures successfully. It is found that the diffuse of Ni NC at different annealing temperature is thought as the major parameter to cause the different Ni NC structures. We also fabricated the Ni NC memory device to study the memory effect further. Excellent charge-storage ability is found based on the higher density of double-stacked Ni NC. However, the device has a poor retention due to the additional defects provided by the oxide interface. A higher temperature formation process is confirmed to reduce the device leakage paths. The devices formed by annealing at 800°C shows an excellent charge-storage ability characteristic in the retention test.

3.2 High density Ni nanocrystal formed by co-evaporating Ni and SiO₂ pellets for the nonvolatile memory device application

3.2.1 Introduction

In this work, we propose a method to fabricate Ni NC structure by co-evaporating Ni and SiO₂ pellets, simultaneously. An 800°C RTA was used to enhance the Ni NC to aggregate. Transmission electron microscope indicates the formed Ni NC show a high density distribution about $4.5 \times 10^{12} \text{cm}^{-2}$. Then, the memory device using the Ni NC as charge-trapping centers was fabricated. The Ni NC memory device has an obvious memory window under capacitance-voltage measurement. XPS confirms the memory effect results from the Ni NC embedded in SiO₂ dielectric layer. Moreover, related reliability characteristics have also been extracted.



3.2.2 Experiment

The memory structure was fabricated on a 6 in. p-type Si substrate. First, a 5-nm-thick SiO₂ was grown as the tunneling oxide by dry oxidation in atmospheric pressure chemical vapor deposition furnace. Then, a dual E-gun system was used to deposit the charge-trapping layer of the device. In the co-deposition process, Ni and SiO₂ pellets were placed in the respective crucible. Subsequently, an about 10-nm-thick mixed film composed of Ni and SiO₂ was deposited by co-evaporating the pellets, simultaneously. The rate of Ni and SiO₂ was controlled to be about 1:8.

After the trapping layer deposition, a followed RTA treatment set at 800°C in N₂ ambient for 60sec was used to form the Ni NC structure. Afterward a 50-nm-thick blocking oxide was capped by PECVD system. Finally, top and bottom Al gate electrode were patterned to form the MOIOS structure.

3.2.3 Results and discussion

Fig. 3-9 (a)-(d) demonstrates the cross-section and plane-view TEM images of the Ni and SiO₂ mixed film after the thermal annealing. It can be found obviously that the NC aggregated between the tunneling and blocking oxide. The average diameter and area density of the formed Ni NC calculated by the plane-view TEM image are around 5nm and $4.5 \times 10^{12} \text{cm}^{-2}$, respectively. The excellent NC density is superior to the reported literature [3.15-3.20]. In addition, the most appropriate Ni NC size about 5nm can reduce the effect of quantum-confinement because the charge stored in smaller NC size is unsteady and easy to tunnel back to the Si substrate [3.21]. The TEM results confirm that the co-evaporated method brings an excellent NC characteristic indeed. Moreover, XPS analyses had also been used to realize the compositions of the trapping layer further. Fig. 3-10 (a) and (b) demonstrate the XPS results of the Ni and SiO₂ mixed film after the thermal annealing process. In Fig. 3.9 (a), it can be found that a peak at 853eV in the Ni XPS 2p spectra, which corresponds to the binding energy of the Ni-Ni. In addition, an obvious Si-O signal at about 533eV

can be seen in the O 1s XPS spectra as shown as the Fig. 3-9 (b). Through the XPS results, it can be concluded that the Ni-Ni signal is attributed with the aggregated Ni NC and the trapping layer is the Ni NC embedded in the SiO₂ dielectric layer. The process of the co-evaporated method to form the high-density Ni NC has also been demonstrated. In the NC formation, we also tried to form the Ni NC at 700°C RTA condition. It is found that Ni NC structure reveals a multi-layer distribution (not shown). Through the comparison between the structures under different annealing processes, it can be speculated the improved NC characteristics result from that the formation process of co-evaporated method is different from the self-assembled method. The co-evaporated process cause the Ni elements are distributed in the trapping layer similar as the after-mentioned implantation method. As the external thermal annealing is provided, the evaporated Ni elements can obtain enough energy to leave the initial sites and diffuse in the mixed film. The Ni diffusion with a large number of collisions brings the Ni nuclei formation. With the increase of annealing temperature, more Ni elements tend to bond to the Ni nuclei and form the Ni NC structure near the interface between trapping layer and tunneling oxide. Then, a high-density distribution of Ni NC structure is formed without the drawback of the implantation.

Fig. 3-10 (a) shows the C-V measurement of the formed Ni NC memory device.

ΔV_{FB} extracted by the bidirectional C-V sweeps indicates charge-storage ability of the Ni NC. An obvious memory window of 4V can be obtained under $\pm 10V$ gate voltage operations. It can be approximately speculated that about one charge was stored in one Ni NC by the calculation of memory window and NC density. In addition, the J-V characteristic of MOIOS structure was also extracted. Fig. 3-10 (b) indicates the Ni NC memory device without serious leakage current is potential for the trapping layer of the memory structure.

To study the reliability behavior of the Ni NC memory device, retention test has been demonstrated in the Fig. 3-11 (a). The retention characteristic was measured at room temperature by giving $\pm 10V$ gate voltage stress for 10sec and measured up to 10^4 sec. It is found the memory window of the Ni NC device is steady after the rapid drop of the initial 100sec. We think that the initial drop may result from the shallow trapping of the charge-storage layer similar as the result of the reported literature [3.22]. Moreover, the endurance behavior has also been studied as shown as Fig. 3-11 (b). In the endurance test, continuous voltage pulse set at $\pm 10V$ for 1msec was used to stress the memory device. After the continuous voltage pulse operations, a followed C-V measurement was used to observe the degeneration of the charge-storage ability. It can be found only a slight decay of the memory effect after 10^6 cycle operations. The results mean the tunneling oxide has enough quality to prevent the charge loss

even after a repeated stress.

3.2.4 Conclusion

In conclusion, a mixed film deposited by co-evaporating Ni and SiO₂ pellets has been studied to form the Ni NC structures for the nonvolatile memory device application in this work. It is found that the Ni NC reveal a high density distribution of $4.5 \times 10^{12} \text{cm}^{-2}$ after the 800°C thermal annealing process. The reasonable process has also been proposed to realize the Ni NC formation during the annealing. In addition, MOIOS structure using the Ni NC as the charge-storage centers have also been fabricated and measured. The Ni NC memory device formed by the co-evaporated method shows an obvious memory window and good reliability characteristics.

3.3 Formation of double- and single- layer nickel nanocrystal embedded in Si₃N₄ dielectric layer by co-evaporating Ni and Si₃N₄ pellets

3.3.1 Introduction

In this work, a co-evaporating method has been used to fabricate the Ni NC embedded in Si₃N₄ dielectric layer. After 700 and 800°C RTA process, Ni NC reveal double- and single-layer structure, respectively. It is believed that the key parameter for the Ni NC distributions is the diffusion of Ni atoms during thermal annealing. In addition, the memory devices using the double- and single-layer Ni NC

as charge-trapping centers were also fabricated. The electrical performances of the devices have also been demonstrated such as memory window, retention and endurance characteristics.

3.3.2 Experiment

The fabrication of memory structure was started with a dry oxidation at 950°C to form a 5-nm-thick tunneling oxide on p-type (100) Si wafer, which had been removed native oxide and particles by RCA process. Afterward a Ni and Si₃N₄ mixed film about 10-nm-thick was co-deposited by dual e-gun system. The ratio of Ni and Si₃N₄ was controlled to be about 1:10. Then, a followed RTA process set at 700 and 800°C was performed for 60sec in N₂ ambient, respectively. After the RTA process, a 50-nm-thick blocking oxide was capped by PECVD system. Finally, Al gate electrodes were patterned to form MOIOS structure. Related material analysis and electrical measurements were used to study the composition of trapping layer and the charge-storage ability of the memory devices.

3.3.3 Results and discussion

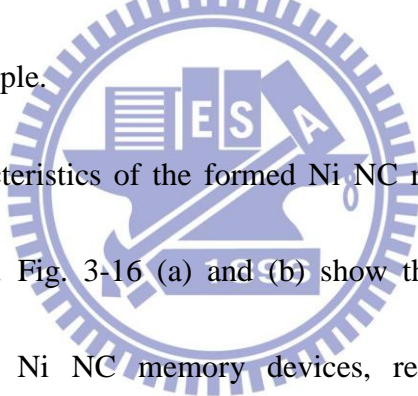
Fig. 3-13 (a) and (b) demonstrate the cross-section TEM images of the Ni NC memory device for 700 and 800°C thermal annealing. It is found the Ni NC nucleated between the tunneling oxide and blocking oxide after the RTA processes. In the Fig. 3.13 (a), the 700°C -nucleated Ni NC, are about 5nm, reveal a double-layer

distribution. In contrast, single-layer Ni NC around 10-12nm was found on the tunneling oxide after the 800°C annealing process.

In the XPS analysis, the data of 700°C- annealed sample was only shown for similar results of 800°C- annealed one. The Ni NC embedded in the Si₃N₄ dielectrics layer are evidenced by XPS analysis for Ni-Ni peak at 853eV and Si-N peak at 399eV as shown as the Fig. 3-14 (a) and (b). Then, a reasonable process for the formation of the structures under different annealing temperature is proposed. According to the reported literature, thermal-driving Ni atoms tend to diffuse and aggregate to form the NC structure due to the surface energy and the interface stress [3.23]. In addition, the nucleation of NC depends on the nucleation sites of the deposited film [3.24-3.27]. The nucleation sites distribute over the mixed film randomly during the co-deposition process. Therefore, the lower thermal annealing temperature (700°C) though causes the Ni aggregate but in a random distribution. The Ni atoms obtained more driving force to move as the thermal temperature increasing to 800°C [3.25-3.26]. As shown as Fig. 3-13 (b), the large size of Ni NC only located at the interface of tunneling oxide layer.

Figs. 3-15 (a) and (b) show the C-V measurements for the double- and single-layer Ni NC memory device, respectively. The bidirectional C-V sweeps were performed to study the charge-storage ability of the NC. In Fig. 3-15 (a), the

double-layer-distributed Ni NC memory device shows a 6V memory window under $\pm 10V$ gate voltage operations. In addition, the single-layer Ni NC memory exhibited a 1.5V memory window, which is still enough to define “1” and “0” states. The NC density is the major parameter to affect the memory window difference between the devices [3.27]. As a positive gate voltage was applied during the program mode, electrons of channel were prompted to pass through the capacitor structure or stored in the Ni NC. The double-layer NC structure has a higher capture possibility than the single-layer one. Therefore, more electrons stored in the NC brought obvious ΔV_{FB} in the 700°C-annealed sample.

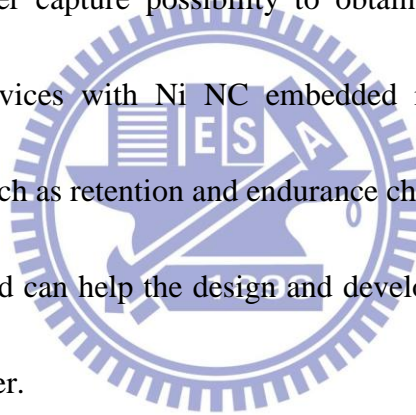


The reliability characteristics of the formed Ni NC memory devices were also investigated in this study. Fig. 3-16 (a) and (b) show the retention results of the double- and single-layer Ni NC memory devices, respectively. The retention measurement was used a $\pm 10V$ gate voltage stress to write the devices to a similar ΔV_{FB} and measured up to 10^4 sec. It is found both of the memory devices can keep obvious memory window after 10^4 sec. However, the 800°C-annealed sample has better retention characteristic for the improved interface trap or the surrounding oxide characteristics of NC in high annealing process [3.28]. In the endurance test, a continuous voltage pulse set at $\pm 10V$ for 1msec has been used to stress the devices. After the continuous voltage pulse test, the C-V measurement was used to observe the

degeneration of charge-storage ability. As shown as the results in the Fig. 3-17 (a) and (b), a negligible decay of memory window is found.

3.3.4 Conclusion

In conclusion, the co-evaporated method was used to fabricate double- and single-layer Ni NC structures successfully by controlling the temperature of NC nucleation process. The diffusion of Ni elements under thermal treatment is the key point for formation of Ni NC structures. In the C-V measurement, double-layer Ni NC memory device has higher capture possibility to obtain larger memory effect. In addition, the memory devices with Ni NC embedded in Si_3N_4 layer have good reliability performance, such as retention and endurance characteristics. Moreover, the easy co-evaporated method can help the design and development of the double-layer Ni NC memory devices further.



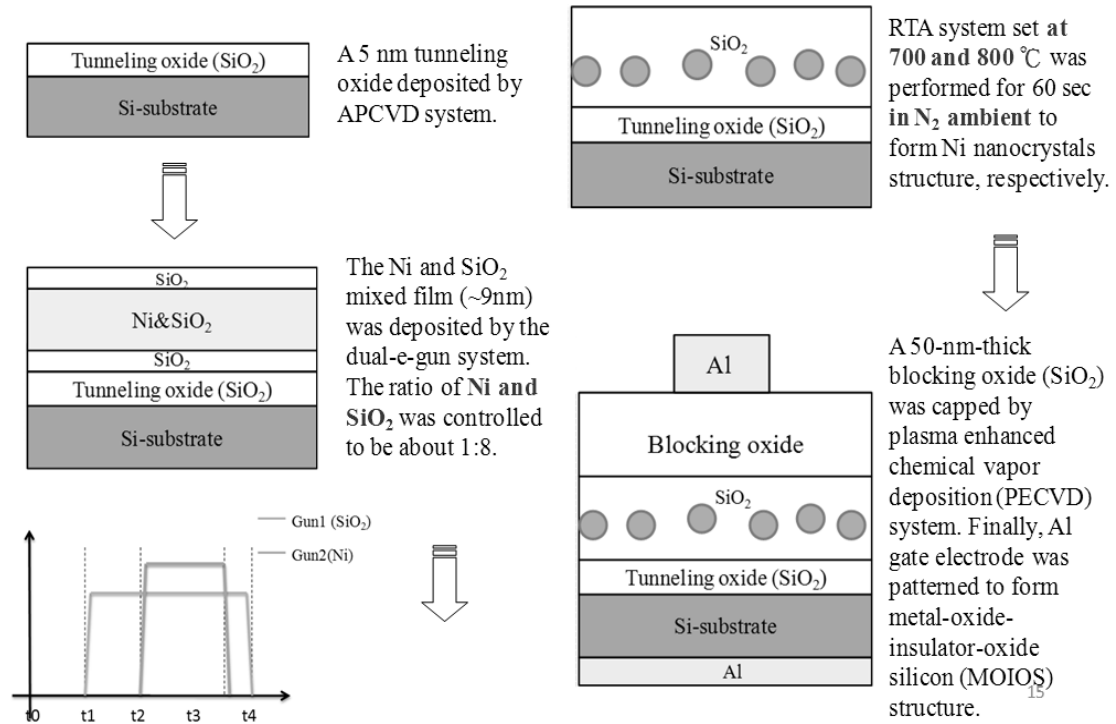


Fig. 3-1 The process of the co-evaporating process.

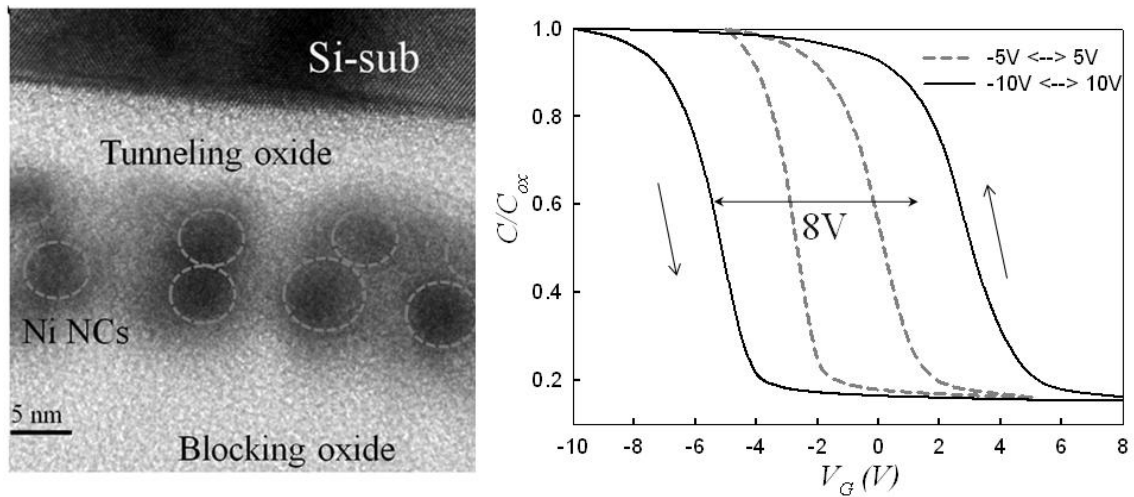


Fig. 3-2 The (a) cross-section TEM micrographs and (b) C-V result of the NC memory devices formed by annealing at 700 °C for 1 min.

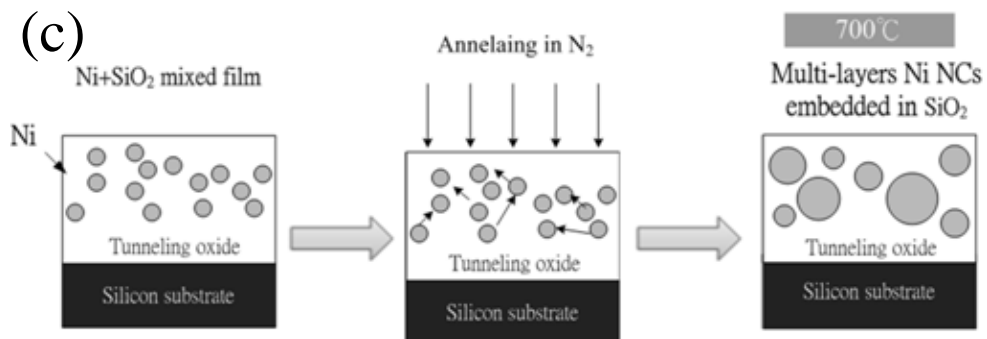
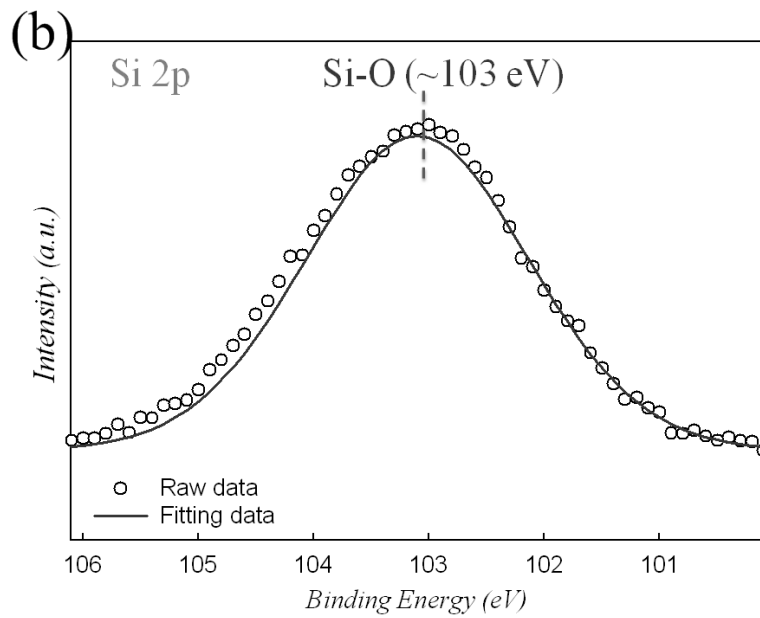
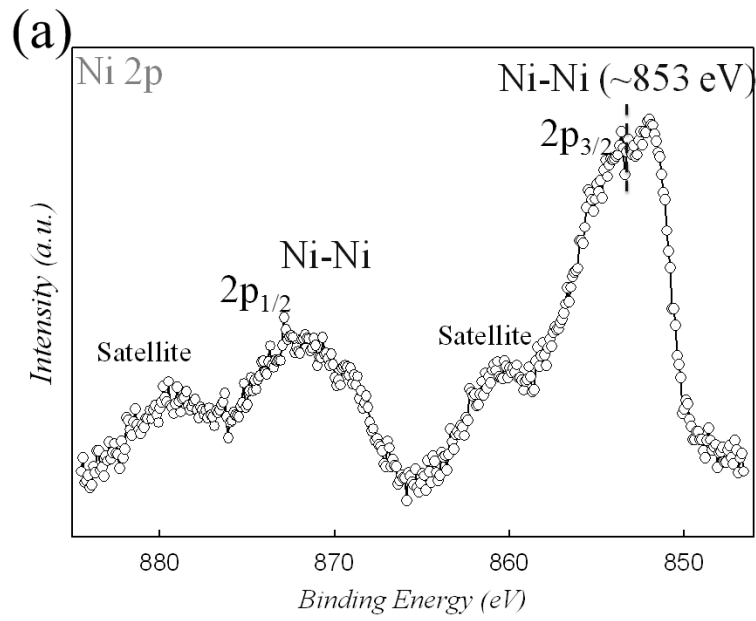


Fig. 3-3 (a) The Ni 2p and (b) O 1s XPS spectra of the charge trapping layer after 700 °C thermal annealing. (c) The forming process of the Ni NC structure during thermal annealing.

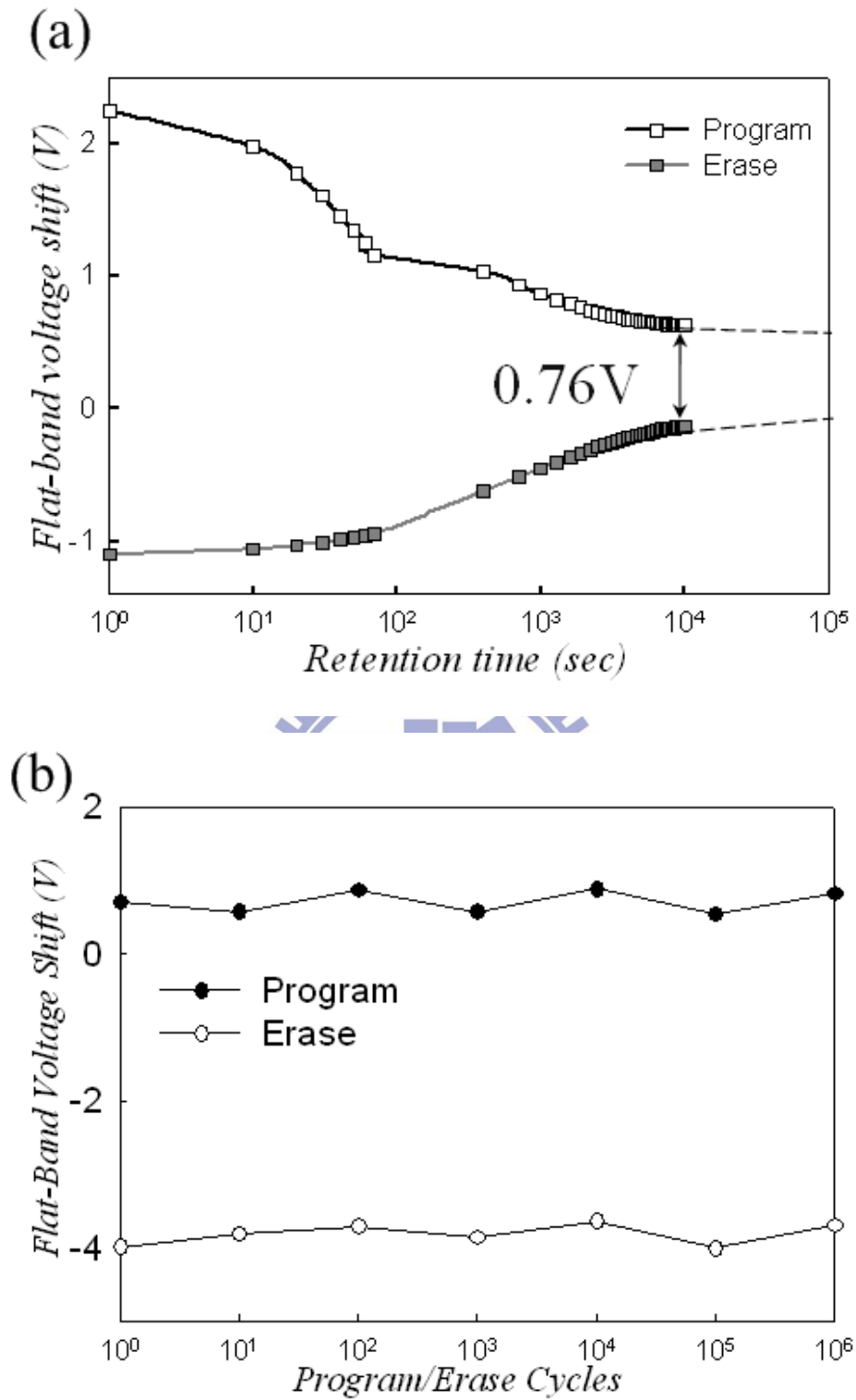


Fig. 3-4 (a) Charge retention and (b) endurance characteristics of the Ni NC formed by annealing at 700°C for 1 min.

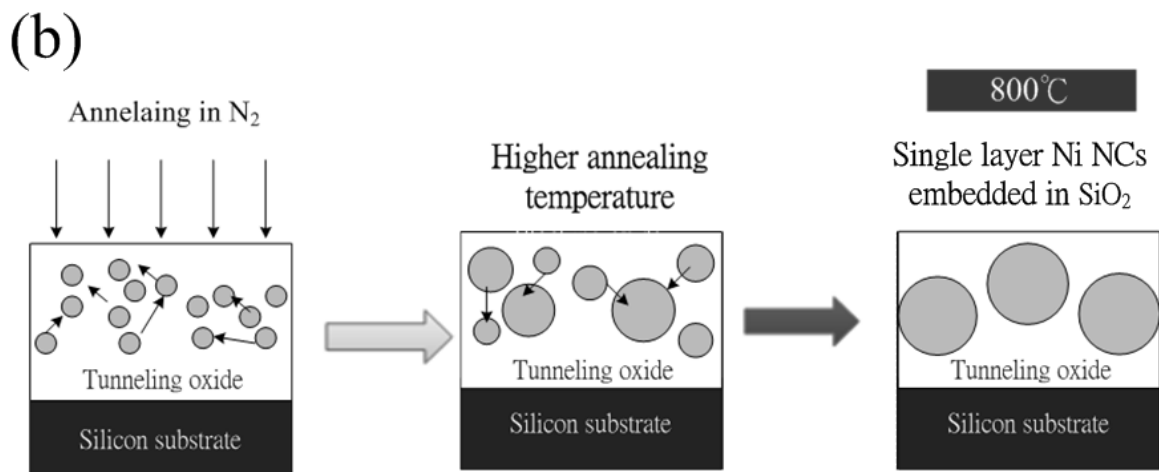
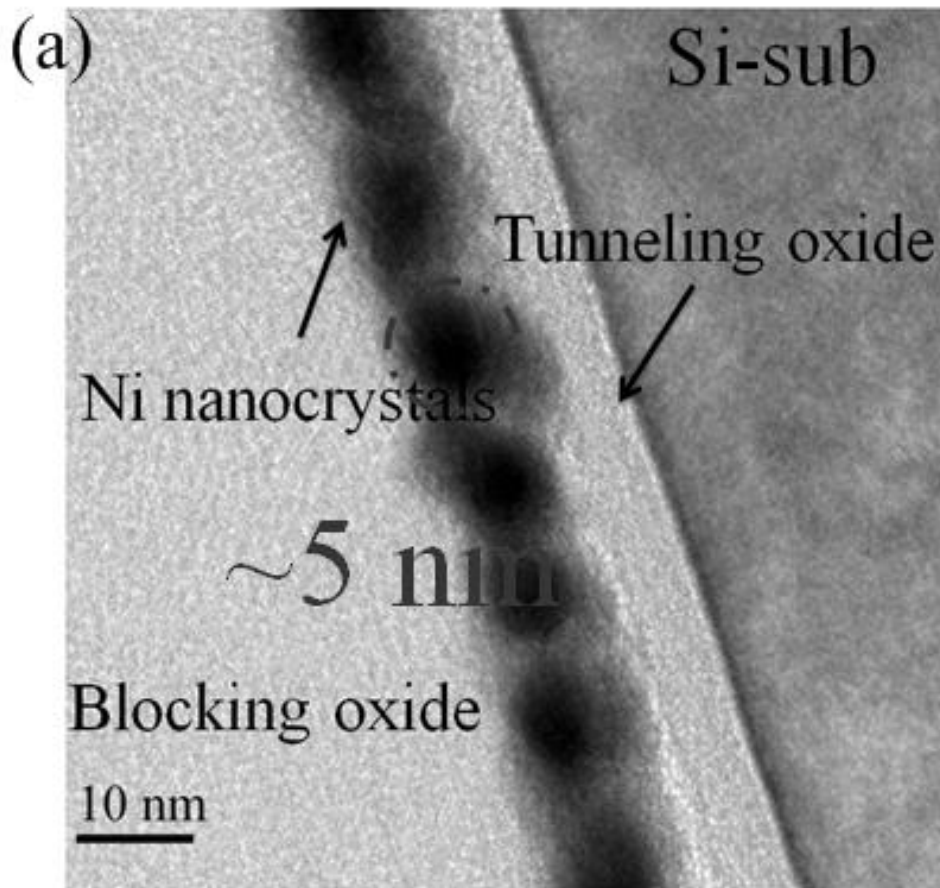


Fig. 3-5 (a) The cross-section TEM micrographs and (b) forming process of the Ni NC at 800°C annealing for 1 min.

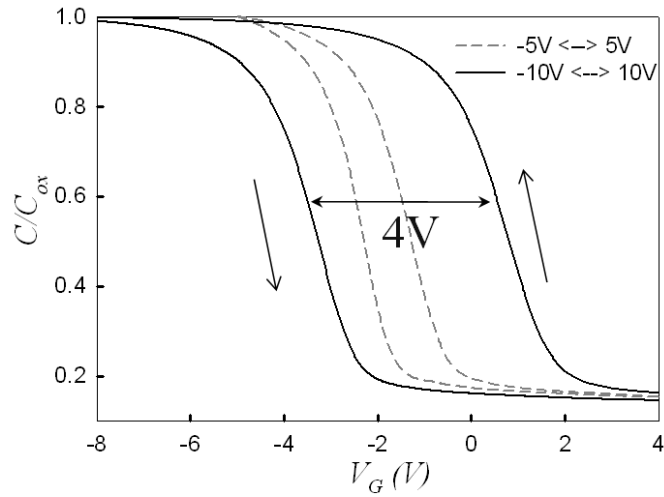


Fig. 3-6 The C-V result of the Ni NC memory device formed by the 800°C annealing for 1 min.

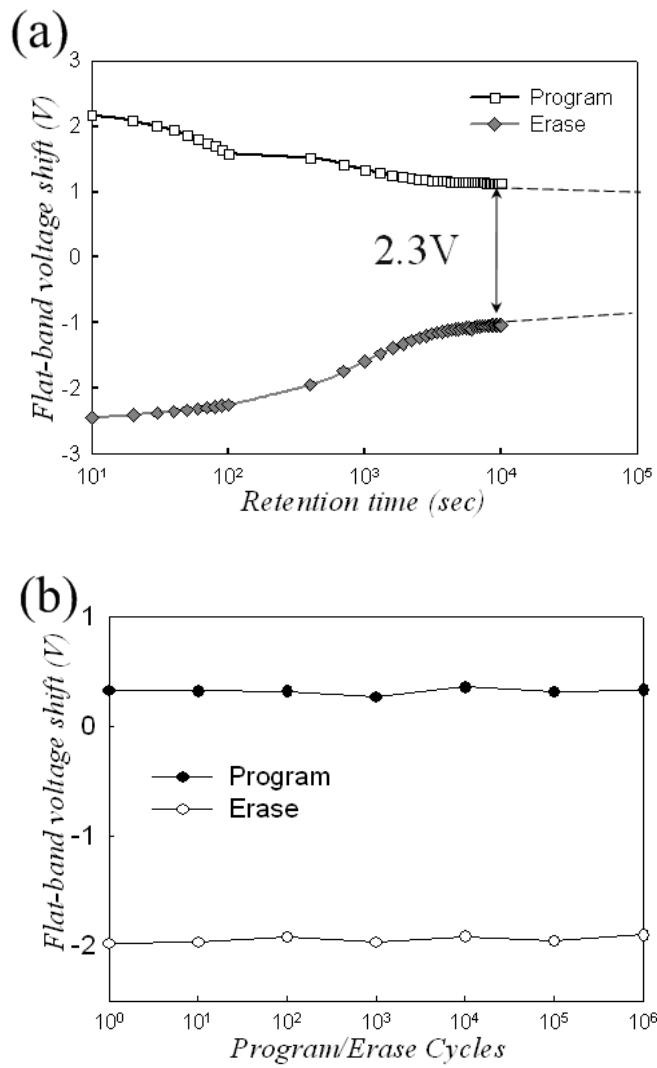


Fig. 3-7 (a) Charge retention and (b) endurance characteristics of the Ni NC formed by annealing at 800°C for 1 min.

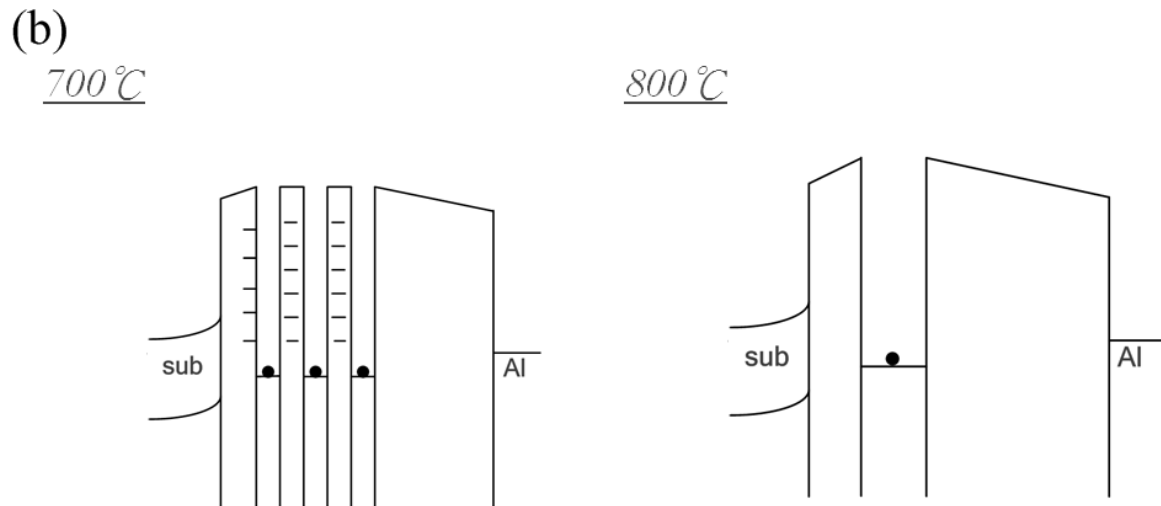
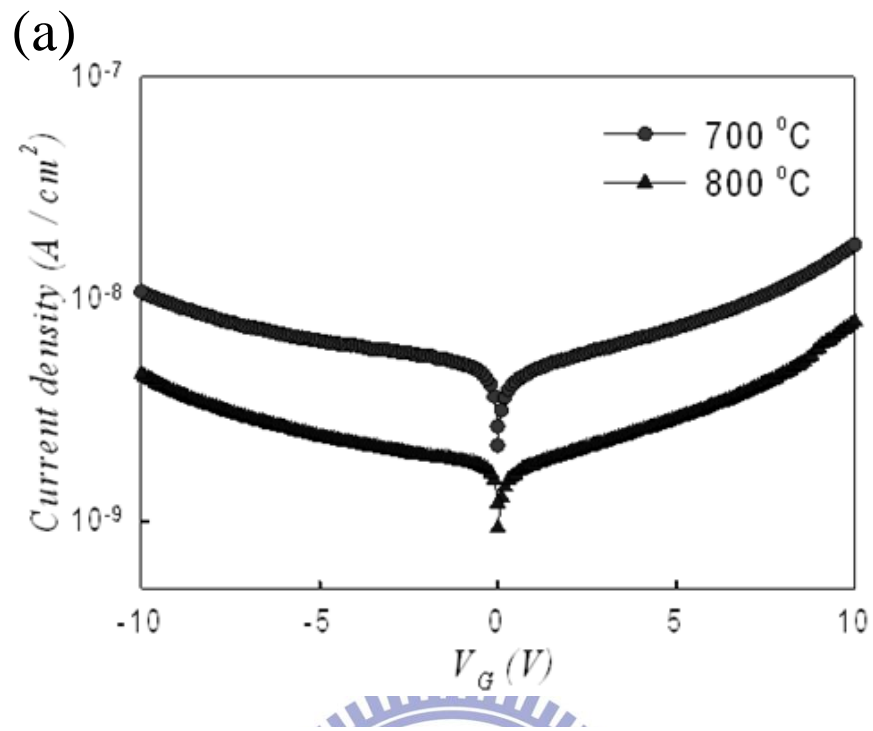
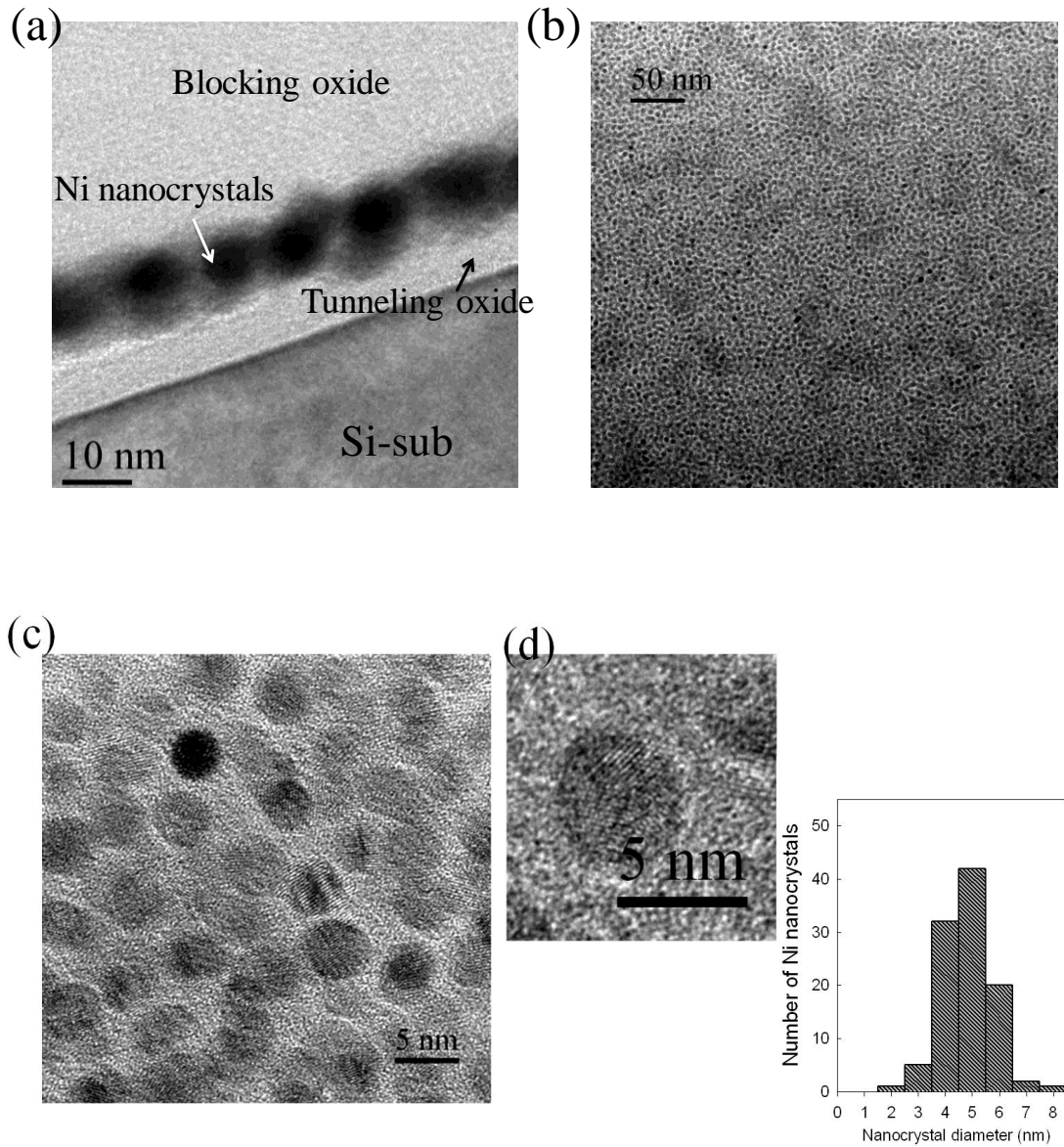


Fig. 3-8 The comparison of gate current density (J-V) and leakage mechanism between the memory devices.



	nanocrystal	process	size(nm)	density(cm^{-2})	calculated method
Refenece [1]	Pt	sputtering technique	2.2	3×10^{12}	
Refenece [2]	NiSi ₂	sputtering technique	4-6	2.67×10^{12}	cross-section TEM
Refenece [3]	Ni	Thermal evaporation	6.3	6.5×10^{11}	cross-section TEM
Refenece [4]	InAs	MBE	3	7×10^{11}	
Refenece [5]	RuO _x	ALD	5-8	1×10^{12}	
Refenece [6]	TiN	ALD	2-3	2×10^{12}	cross-section TEM
Refenece [7]	Ru	ALD	2	9.7×10^{11}	
our experiment	Ni	co-evaporation	5	4.5×10^{12}	

Fig. 3-9 (a) The cross-section and (b-d) plane-view TEM images of the Ni and SiO₂ mixed film after 800°C RTA. The size distribution can be seen in the dispersion of NC size.

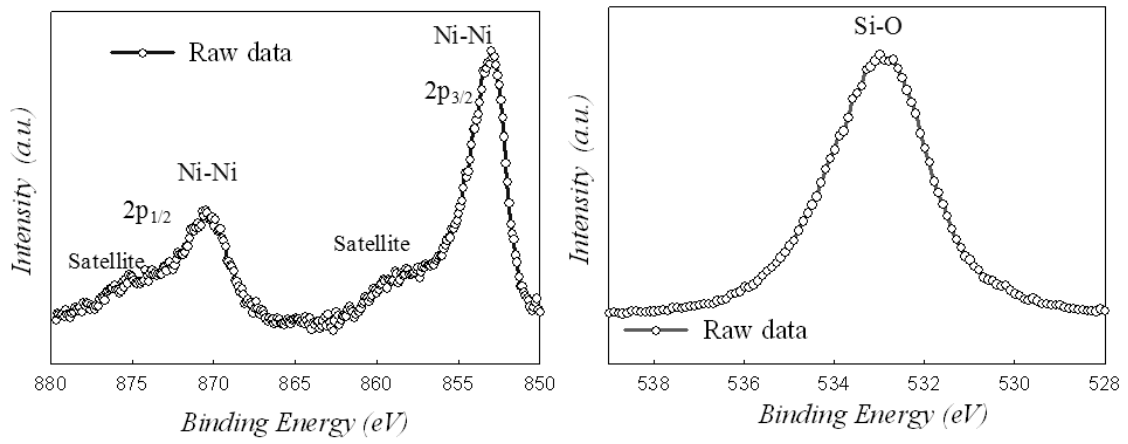


Fig. 3-10 (a&b) The Ni 2p XPS spectra and O 1s XPS spectra of the charge trapping layer after thermal annealing.

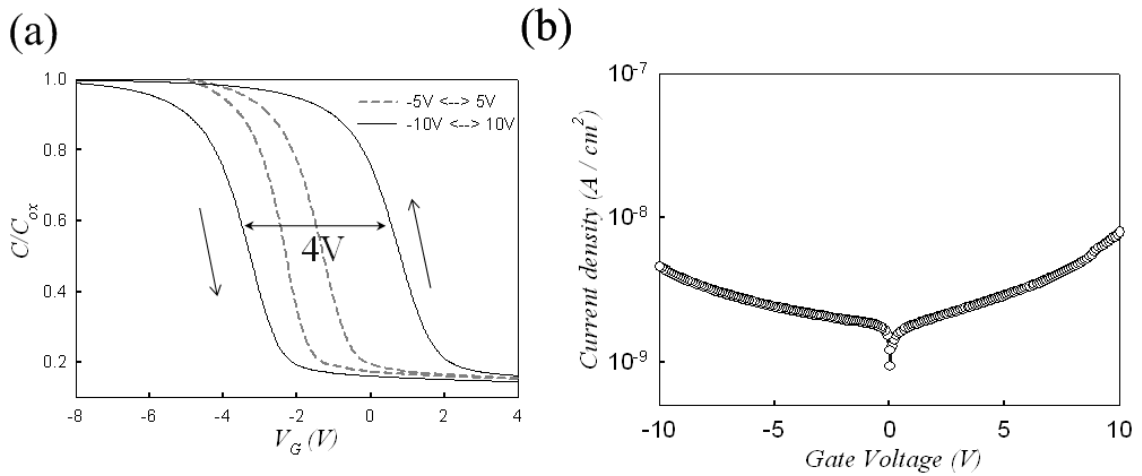


Fig. 3-11 (a) High-frequency C–V characteristic and (b) J–V characteristic of the Ni NC memory device.

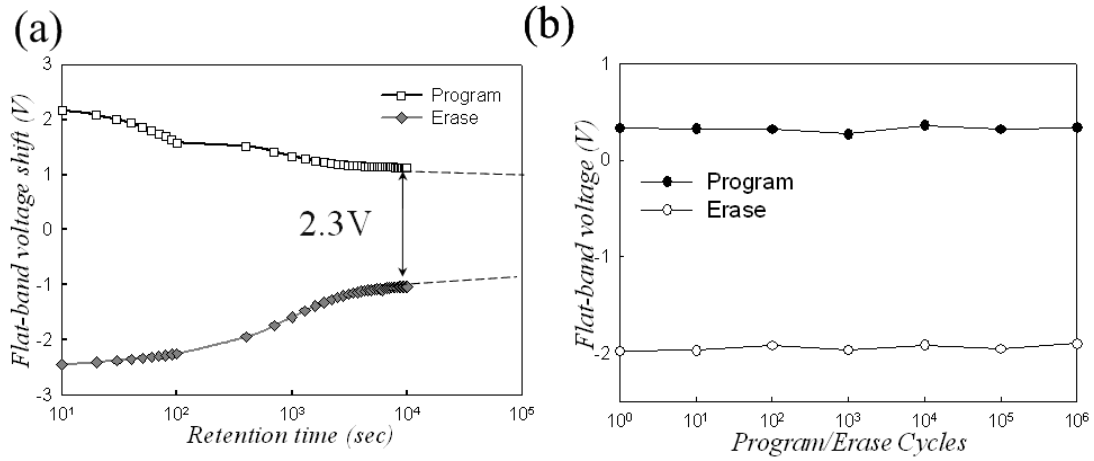


Fig. 3-12 (a) Charge retention characteristic and (b) endurance characteristic of the formed Ni NC memory device.

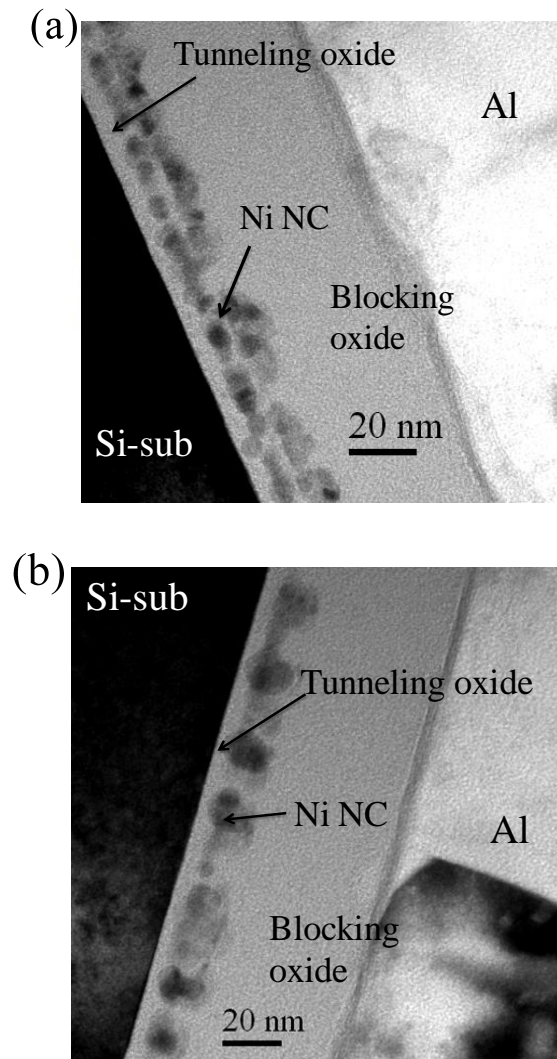


Fig. 3-13 (a&b) The cross-section TEM micrographs of the Ni and Si_3N_4 mixed film after 700 and 800°C RTA, respectively.

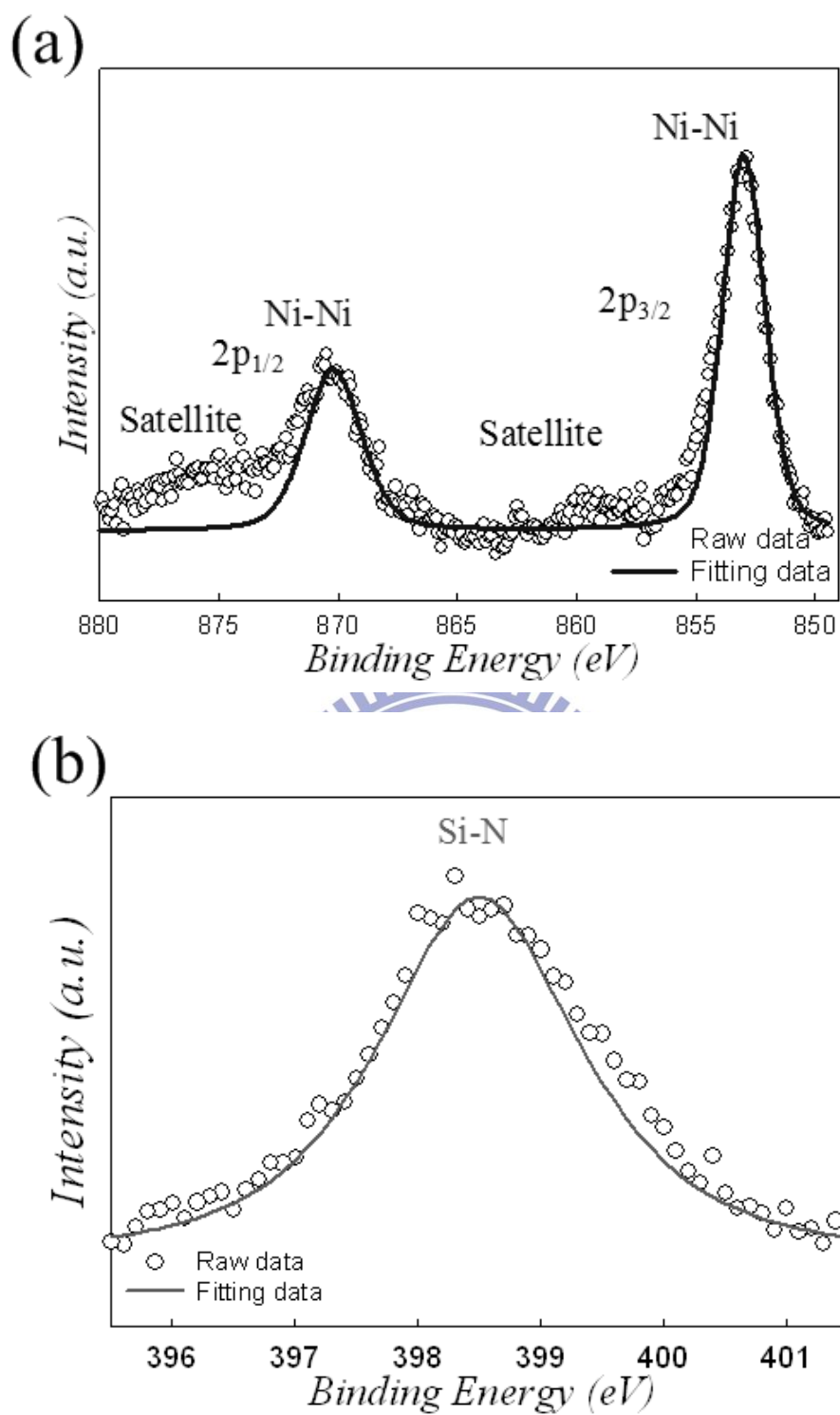


Fig. 3-14 (a) The Ni 2p and (b) N 1s XPS spectra of the charge trapping layer after 700°C thermal annealing.

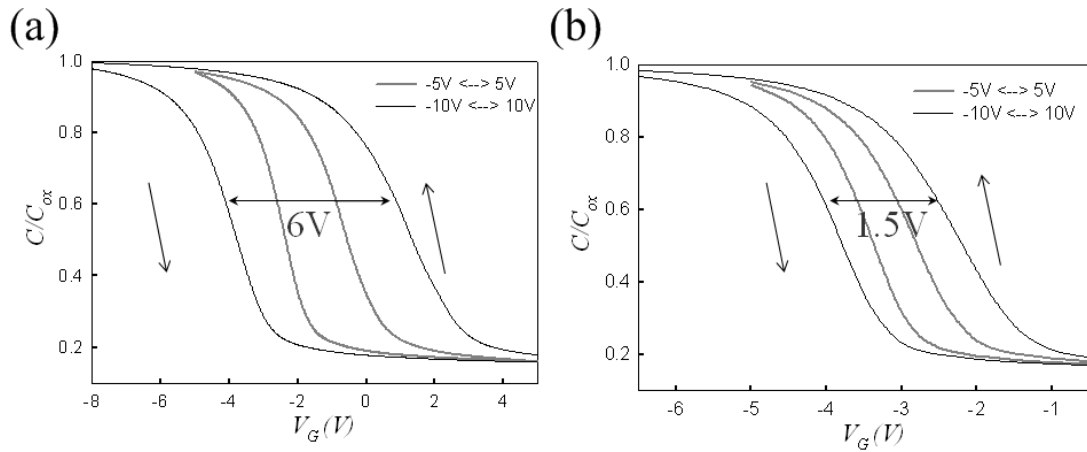


Fig. 3-15 (a&b) High-frequency C-V characteristics of the Ni NC formed by annealing at 700 and 800°C, respectively.

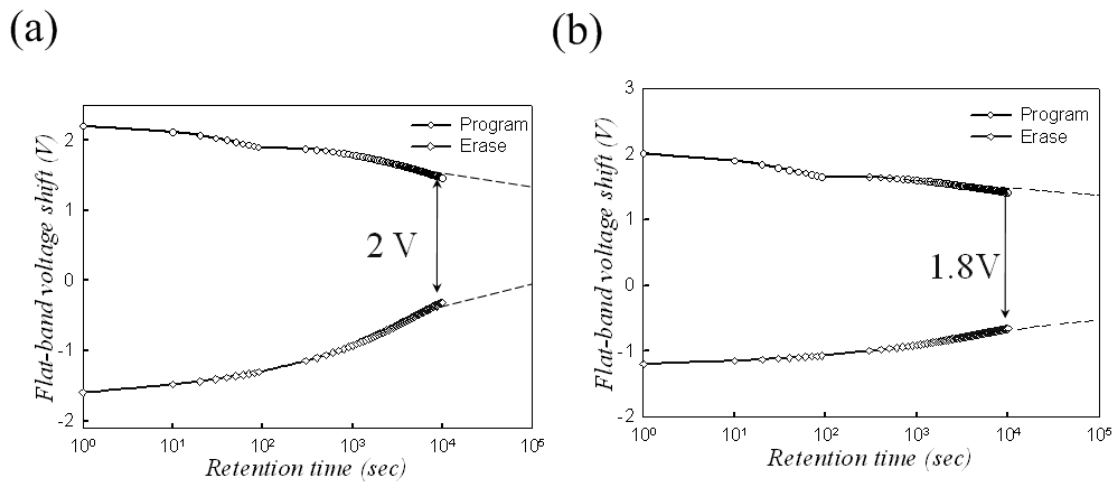


Fig. 3-16 (a&b) The retention of the Ni NC formed by annealing at 700 and 800°C, respectively.

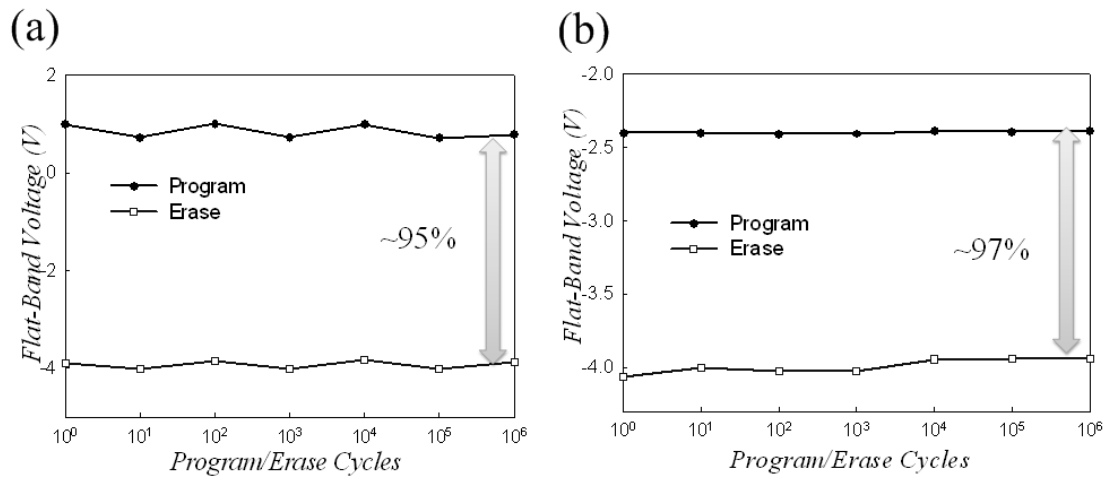
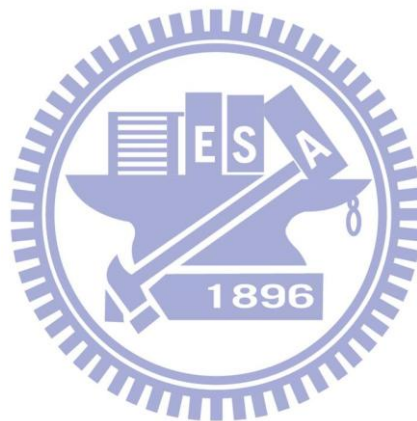


Fig. 3-16 (a&b) The endurance of the Ni NC formed by annealing at 700 and 800°C ,

respectively.



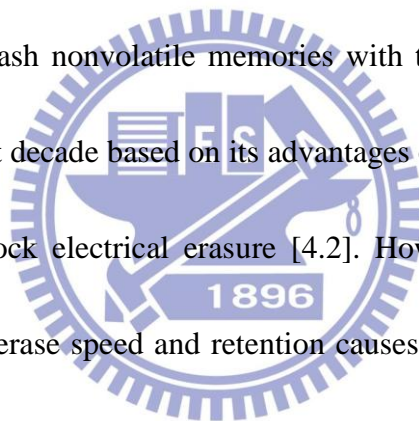
Chapter 4

Fabrication and Memory Effect of Co nanocrystal by Sputtering in the O₂/N₂ Ambiance

4.1 Cobalt nanocrystal embedded in silicon oxide fabricated by incorporating oxygen elements during sputtering process

4.1.1 Introduction

In 1967, S. M. Sze and D. Kahng invented the FG structure nonvolatile memory at Bell Labs [4.1]. The flash nonvolatile memories with the FG structure drove the portable market in the past decade based on its advantages of low-power consumption, easy downscaling and block electrical erasure [4.2]. However, a trade-off relation between the device write/erase speed and retention causes the FG structure to face a challenge when the tunneling oxide is down-scaled to about 8 nm [4.3]. The structures with distributed charge-storage centers such as NC or SONOS are considered as the next-generation nonvolatile device [4.4-4.5]. In the study of NC device, metallic NC such as Co, Ni and W attracts more attentions than semiconductor one due to the advantages of higher work-function, better gate voltage coupling rate and lower fabricating temperature [4.6-4.8]. The most common NC fabricating methods are by selective oxidation and self-assembled characteristic of thin film [4.9-4.11]. However, the self-assembled method usually has the issue of NC uniformity and needs a higher



annealing process [4.12]. The conventional oxidation by the different oxidized ability between elements during thermal oxidation can lower the fabricating temperature but have the drawback of over-oxidation [4.13].

In the section, a CoSi_2 thin film incorporated oxygen element was deposited by reactive-sputtering process. Therefore, the deposited CoSi_2 thin film is oxygen-doped or partially oxidized. The reactive-sputtering process has better control ability for the oxidation method to form NC structure. After a RTA process, it can be found that Co NC was aggregated on the tunneling oxide obviously. In addition, the relations between annealing temperature and memory performance has been discussed by fabricating the NC under 700 and 800°C annealing condition, respectively. A higher annealing is confirmed to provide better retention characteristics. Moreover, it is also found that the memory window of the device is affected by the O_2 ambient of the sputtering condition.

4.1.2 Experiment

The fabrication of memory structure was started with a dry oxidation at 950°C to form a tunneling oxide about 5-nm-thick on p-type (100) Si wafer, which had been removed native oxide and particles by RCA process. Afterward, a about 6-nm-thick CoSi_2 thin film served as a charge trapping layer was deposited by the reactive-sputtering the pure CoSi_2 target in the Ar/O_2 (24 sccm/5 sccm) ambient at

room temperature. Subsequently, a followed RTA process set at 700 and 800°C for 1 min in N₂ ambient was performed to form Co NC structure. After the RTA process, a 50-nm-thick blocking oxide was capped by the PECVD system. Finally, Al gate electrodes were patterned by shadow mask to form capacitor structure. In addition, the CoSi₂ films with 2, 7 and 10sccm of oxygen flow parameters have also been formed to study the effect of oxygen flow rate. After the device fabricating process, electrical characteristics such as memory window, gate leakage current retention characteristics were measured by Keithley 4200 and HP 4284 Precision LCR meter. In addition, the NC formation and composition of the charge-trapping layer have also been analyzed by TEM and XPS.

4.1.3 Result and discussion

Fig. 4-1 (a) is the cross-section TEM results of the NC formed by annealing the deposited CoSi₂ film with 5sccm oxygen flow rate during sputtering process. It can be found that the NC about 5nm was nucleated on the tunneling oxide obviously. Then, the XPS analysis as shown as the Fig. 4-1 (b) was used to analyze the compositions of the NC. From the Co 2p XPS of the charge-trapping layer, it is found that the main composition includes the Co-Co (778.3eV) and Co-O (782eV) signals, which confirms the formed structure is the Co NC embedded in the SiO₂ dielectric layer [4.14]. The 700°C RTA process can completely oxidize the trapping layer and

enhance the Co NC formation. The forming mechanism is that Si element ($\Delta G_1 = -856$ kJ/mol) is easier to be oxidized than Co ($\Delta G_1 = -214$ kJ/mol) [4.15]. The difference of the oxidized ability between the Si and Co causes that the oxygen prefers to react with the Si element than Co during the annealing process. Moreover, the method by incorporating oxygen elements during sputtering process to form NC shows a better control ability than direct oxidation.

Fig. 4-2 (a) is the C-V characteristic of the Co NC memory device. It can be found that the device reveals a 7V of ΔV_{FB} under ± 15 V gate voltage sweep. The memory window is attributed with the injection of electrons from the inversion layer of the Si substrate due to its counterclockwise C-V hysteresis loops. In the retention test, ± 15 V gate voltage stress were used to write the device to an appropriate ΔV_{FB} and measured up to 10^4 sec. As shown as the Fig. 4-2 (b), it is found that an about 31V (~80 %) of memory window is found after 10^4 sec test. The electrical results indicate that the Co NC memory device can obtain an excellent memory window and reliability behavior.

The temperature effect has also been studied by measuring the Co NC formed by a higher annealing temperature (800°C). Fig. 4-3 (a) and its inset are the C-V curve and cross-section TEM image of the formed device. It can be found that the device has a about 6.4V memory window, which is slightly smaller than the 700°C -annealed

device. In addition, we also compared with the retention data between the memory devices. The 800°C-annealed device shows a less charge-storage decay rate in the retention test. Then, plane-view TEM images of the samples have been proposed as the Fig. 4-4 (a) and (b) to study the detailed reasons to bring the electrical improvement. From the comparison of the plane-view TEM images, the 800-annealed sample shows a smaller NC size and lower density after the annealing process. Moreover, a comparison of the J-V characteristic between the samples has been proposed as shown as the Fig. 4-5. From the J-V data, it can be found the gate current density of the 800°C - annealed device is about a half order of magnitude smaller than the 700°C-annealed one. Obviously, the 700°C-annealed sample has more current leakage paths, which also cause the stored charge in the Co NC is easier to tunnel back to the Si substrate in the retention test [4.16-4.17]. The improvement of the retention characteristic in the 800°C - annealed device is attributed with the betterment of the oxide such as the tunneling oxide quality, the interface between the tunneling oxide/charge-trapping layer and the surrounding NC oxide.

To further study the detailed relations between the memory window and reactive-sputtering conditions, the Co NC devices with 2, 7 and 10sccm of oxygen flow rate have also been fabricated. Fig. 4-6 demonstrates the comparisons of memory window about the devices. However, it is found that the memory window of the

devices is depended on the oxygen flow obviously. Then, we infer that the degenerated memory window may be attributed with the oxygen flow restrains the NC aggregation. First, the TEM results have been proposed as shown as the Fig. 4-7. From the Fig. 4-7 (a), it can be found that the 2-sccm device shows a local continuous characteristic, which may mean that less trapping sites for memory device results from the incomplete oxidation. However, the NC were clearly formed in the samples with 7 and 10sccm oxygen flow rate as shown as the Fig. 4-7 (b) and (c). By the TEM results, it can be speculated the suppression of NC may not be the critical parameter to bring the decay of memory window in the 7sccm- and 10sccm- samples. Therefore, the followed XPS tool was used to study the compositions of each sample after the annealing as shown as the Fig. 4-8. An obvious Co-Si signal is found in the 2-sccm sample means the oxygen elements is too less to oxidize the silicon completely. Furthermore, it is found that the main peak of the XPS in the 5-sccm sample transfers to the Co-Co peak, which attributed to the Co NC embedded in the SiO₂ dielectrics. A more completely oxidation is obtained when the oxygen flow rate is altered to be 5sccm. However, the main composition of the charge-trapping layer transfers to Co-O signal when the oxygen flow rate is increased above 7sccm. Obviously, the selective oxidation is failed when a higher oxygen flow is provided. It also means that the oxygen elements not only oxidized the Si elements but also the Co NC.

4.1.4 Conclusion

The Co NC embedded in SiO₂ dielectrics have been proposed successfully by incorporating oxygen elements during sputtering process. An excellent memory effect and reliability characteristics is obtained by measuring the memory device using the formed Co NC as charge-trapping centers. In addition, the retention characteristic of Co NC memory device can be further improved by a higher annealing temperature to reduce the needless leakage paths. Moreover, oxygen flow rate during sputtering process is thought as the main parameter to cause the different NC structures because the NC formation by reactive-sputtering process depends on the oxidation process strongly. An incomplete oxidation causes a continuous trapping layer to degenerate the device performance. The excessive amount of gas flow during the sputtering induces the failure of selective oxidation, which also reduces device charge-storage ability.

4.2 Co NC embedded in Si₃N₄ dielectrics by sputtering in the N₂ ambiance

4.2.1 Introduction

In the section, the reactive-sputtering in N₂ ambient was used to fabricate the Co NC embedded in Si₃N₄ dielectrics layer. It is believed the Si₃N₄ as the surrounded NC dielectrics layer can provided many deep traps and share the electrical field between the NC and tunneling oxide, which may induce a better retention characteristic. The

reactive-sputtering can form the NC embedded in the Si_3N_4 dielectrics is easier than the layer-by-layer deposition because the sputtering only needs a deposition process. In addition, we also discuss the temperature and gas flow rate effect for the device performance in the work.

4.2.2 Experiment

Based on our discussions in the section 4.4, the 800°C -annealing condition has been chosen to study the relation between the flow rate of the ambience in sputtering process and device memory effects because the NC by treated by 800°C has a better charge-retention behavior than by 700°C . The condition of the samples can be divided into 5, 10 and 20sccm nitrogen flow during the CoSi_2 film deposition. After the film deposition, the fabrication of memory devices is the same as the aforementioned process flow.

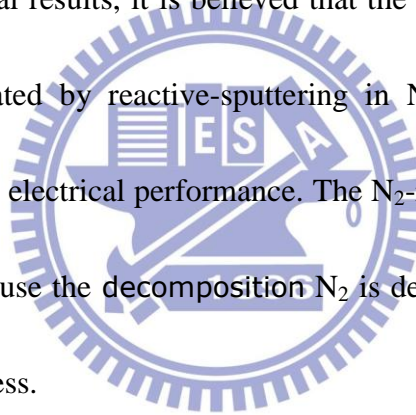
4.2.3 Results and discussion

Fig. 4-8 is the C-V characteristics of the Co NC formed by sputtering at different N_2 flow rate condition. It can be found that the ΔV_{FB} of the Co NC devices are 1.7, 2.1 and 0V. The results of C-V shifts indicate that the memory effect of Co NC is related to the different N_2 flow rate during the sputtering process. Fig. 4-9 is the TEM images of the Co NC formed with 5, 10 and 20sccm N_2 flow rate, respectively. When the N_2 flow rate is set as 5sccm, the Co NC were separated un-obviously as shown as

Fig. 5-10 (a). When the N_2 flow rate was increases to 10sccm, the NC can be segregated more completely. The segregation of the Co NC can bring the difference of the memory device performance. Nevertheless, it can be found the charge trapping layer becomes a continuous $CoSi_2$ thin film by the N_2 flow rate increases to 20sccm. We concluded the continuous film is caused by the N_2 gas will be difficult to form the plasma state and join into the sputtering process if the flow rate of N_2 is too high.

4.2.4 Conclusion

From the experimental results, it is believed that the Co NC embedded in Si_3N_4 dielectrics can be fabricated by reactive-sputtering in N_2 ambiance. The Co NC devices also obtain a good electrical performance. The N_2 -reactive-sputtering also has a optimum condition because the decomposition N_2 is depends on the gas flow rate during the sputtering process.



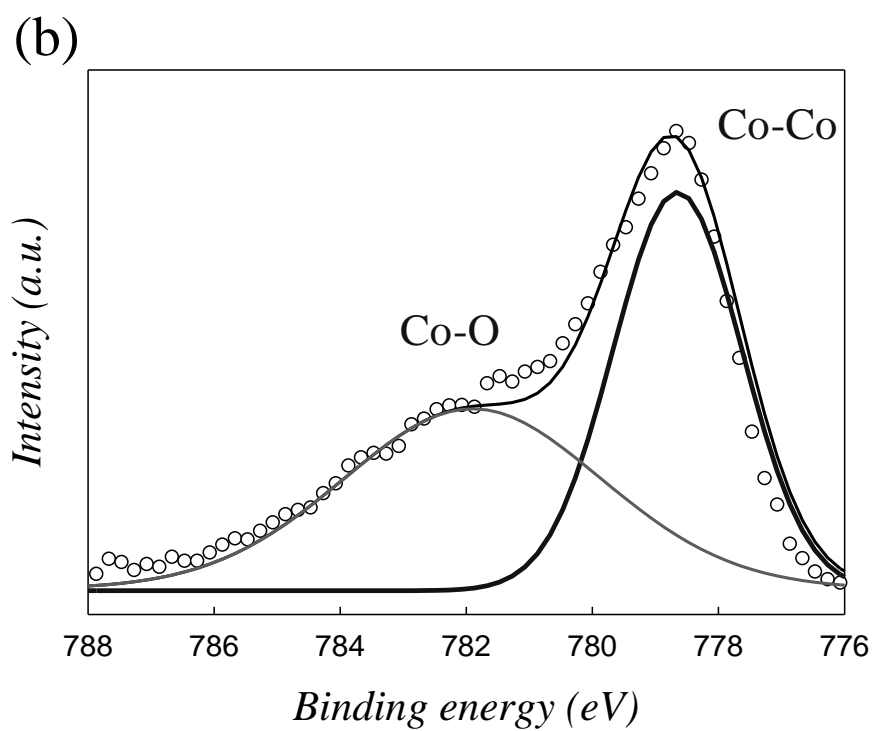
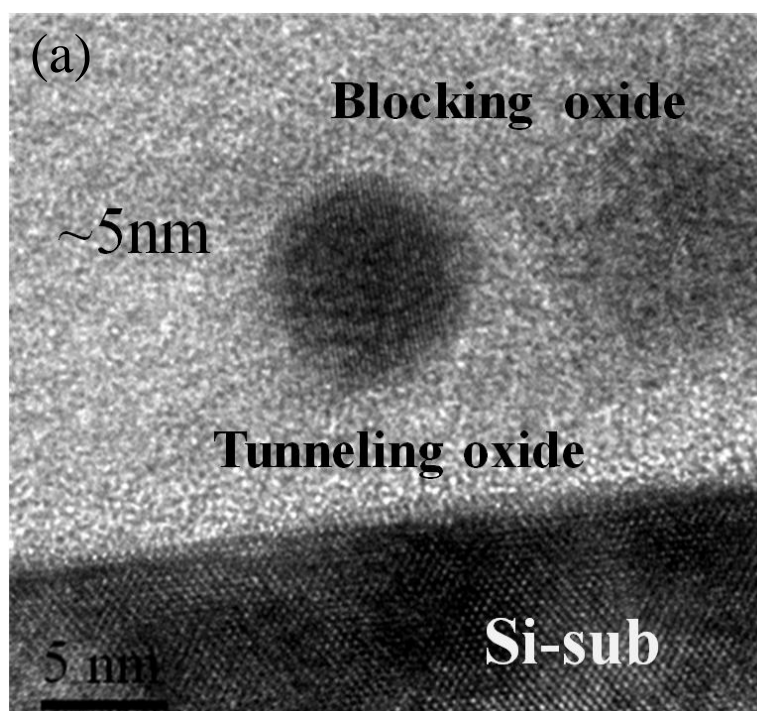


Fig. 4-1 (a) The cross-section TEM image and (b) the Co 2p XPS spectra of the Co NC formed by the sputtering in Ar/O₂ (24 sccm/5 sccm) ambient. The NC forming process is 700°C RTA in N₂ for 1min.

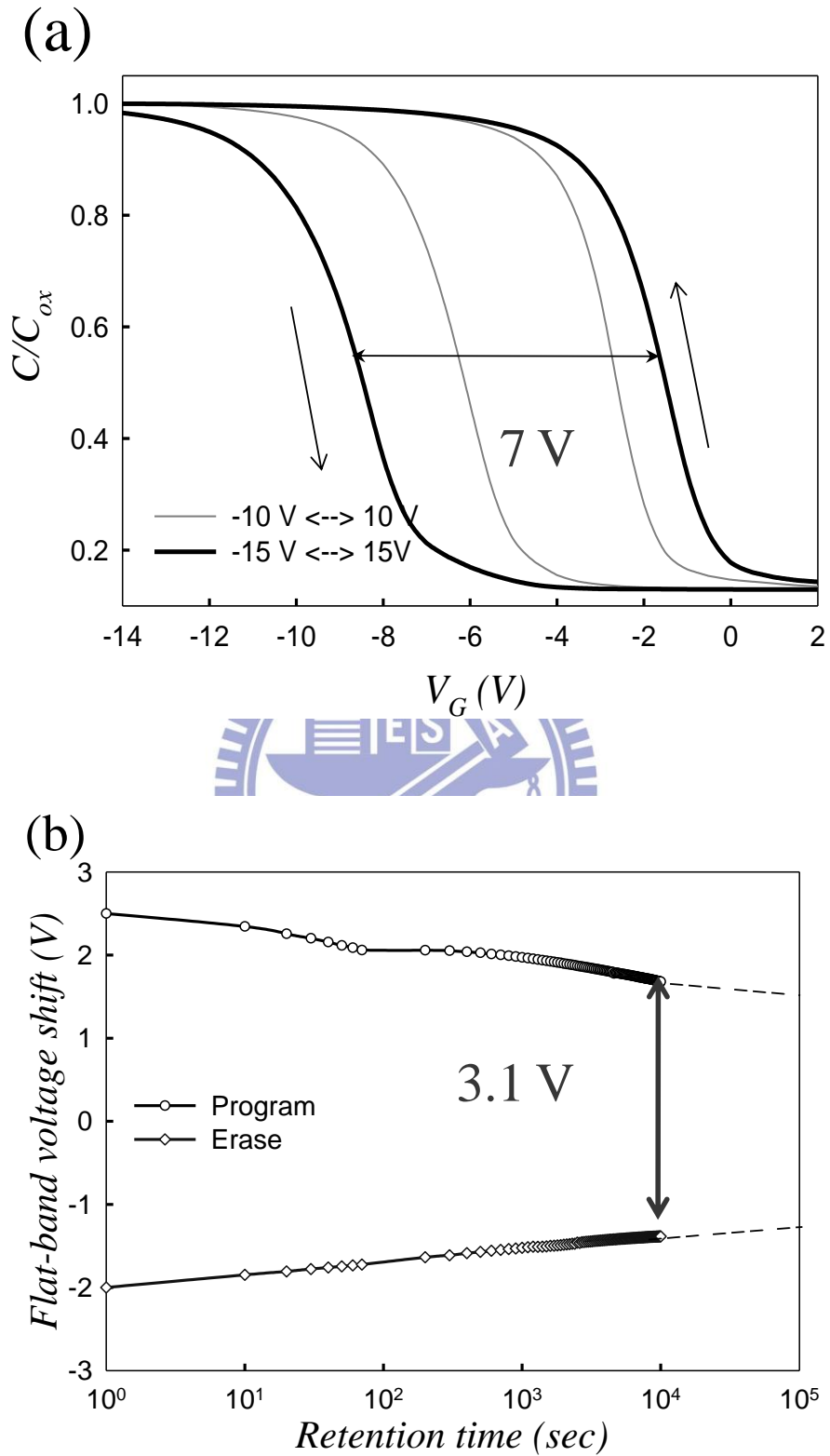
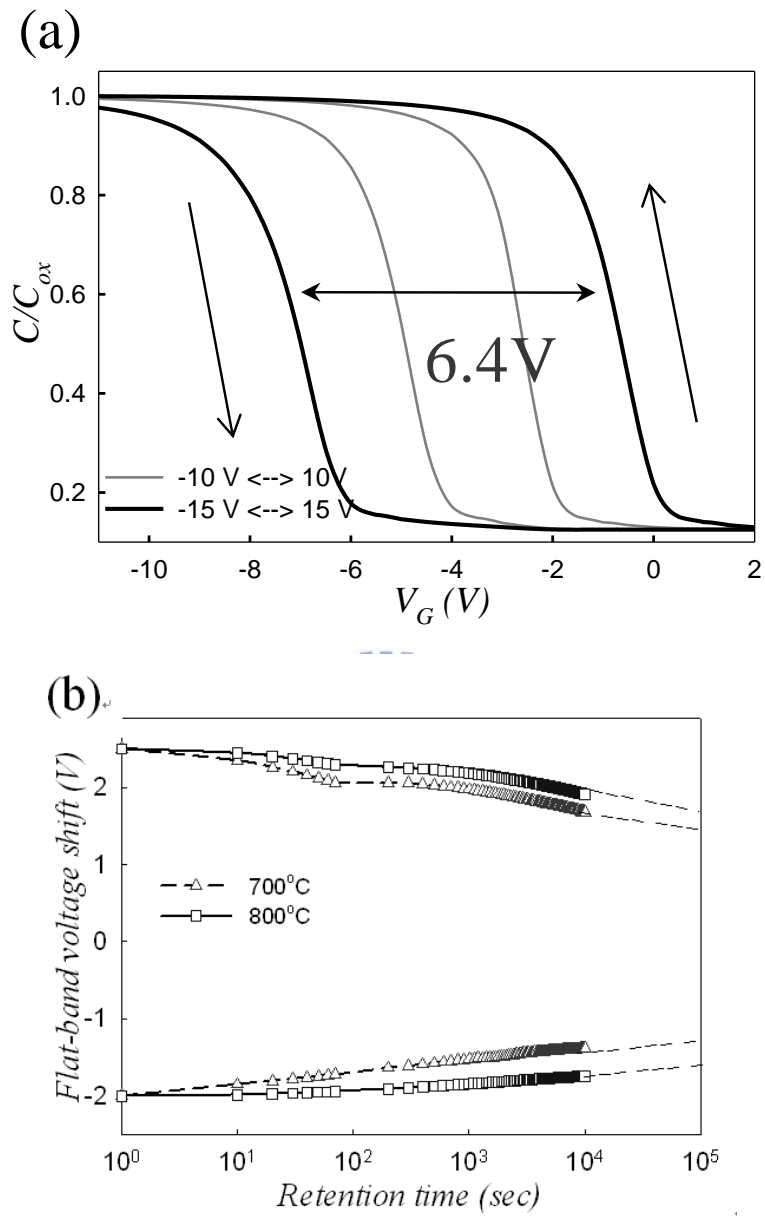


Fig. 4-2 (a) The C-V characteristic and (b) retention characteristics of the Co NC formed by the sputtering in Ar/O₂ (24 sccm/5 sccm) ambient.



	Memory Window (ΔV_{FB} under ± 15 V operation)	Nanocrystal size	Retention (at 1 sec test)
700°C	7 V	~6.5 nm	~70 %
800°C	6.4 V	~7 nm	~86 %

Fig. 4-3 (a) The C-V characteristic and (b) retention characteristics of the Co NC formed by annealing by 800°C annealing temperature for 1 min.

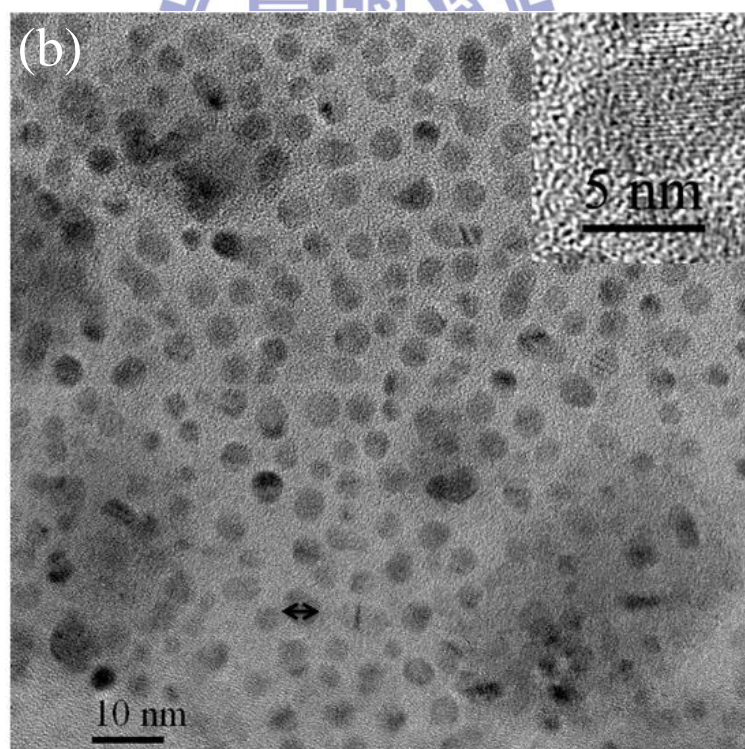
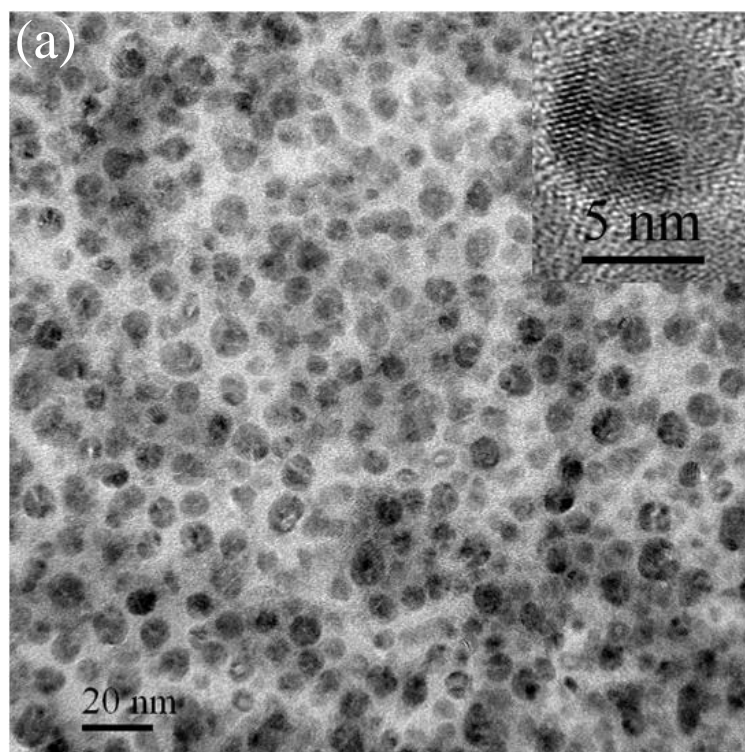


Fig. 4-4. The plane-view TEM image of the NC formed by (a) 700 and (b) 800°C RTA process, respectively.

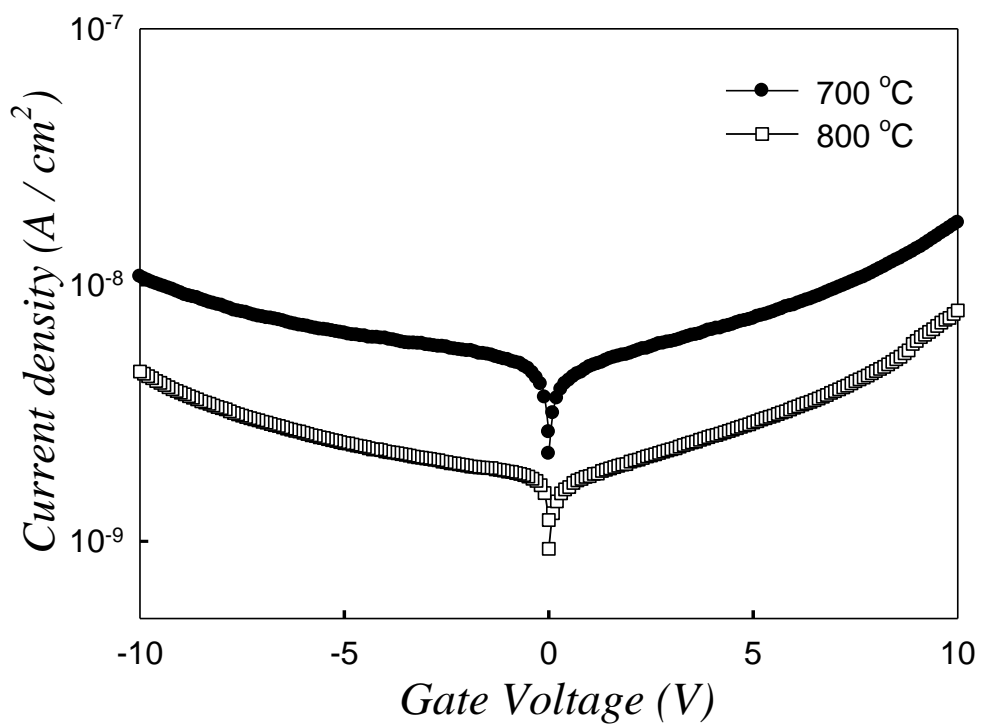


Fig. 4-5 The comparison of the current density-voltage (J-V) characteristic between the samples.

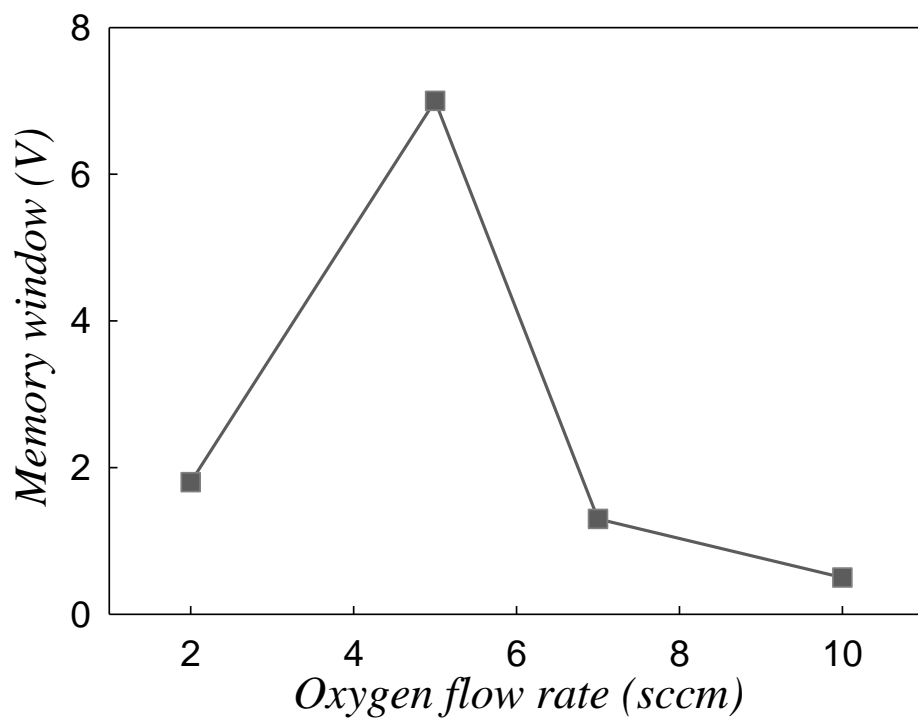


Fig. 4-6 The comparison of memory window about the Co NC devices with 2, 5, 7 and 10 sccm of O₂ flow rate during the sputtering process.

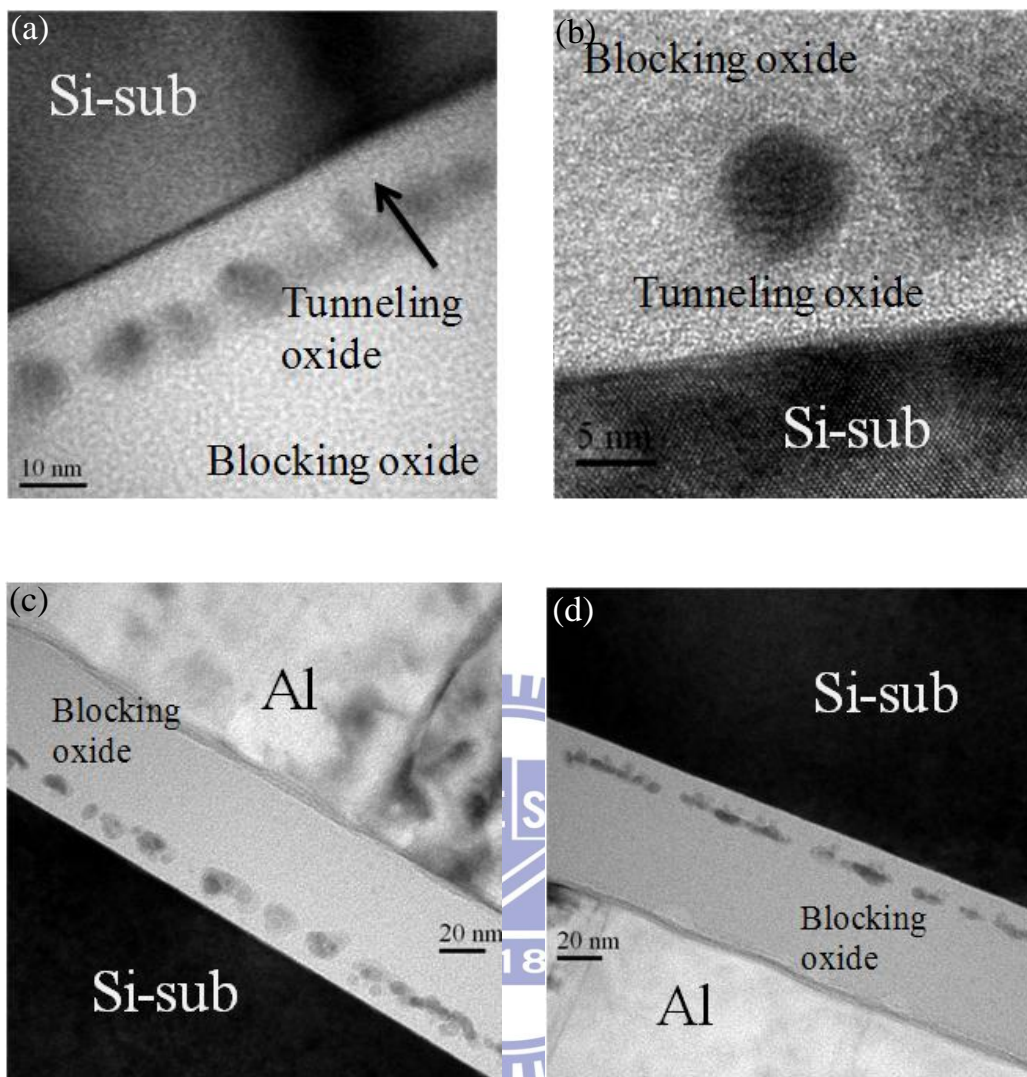


Fig. 4-7 (a)-(d) The cross-section TEM images of the Co NC memory devices formed with 2, 5, 7 and 10 sccm of O₂ flow rate during the sputtering process, respectively.

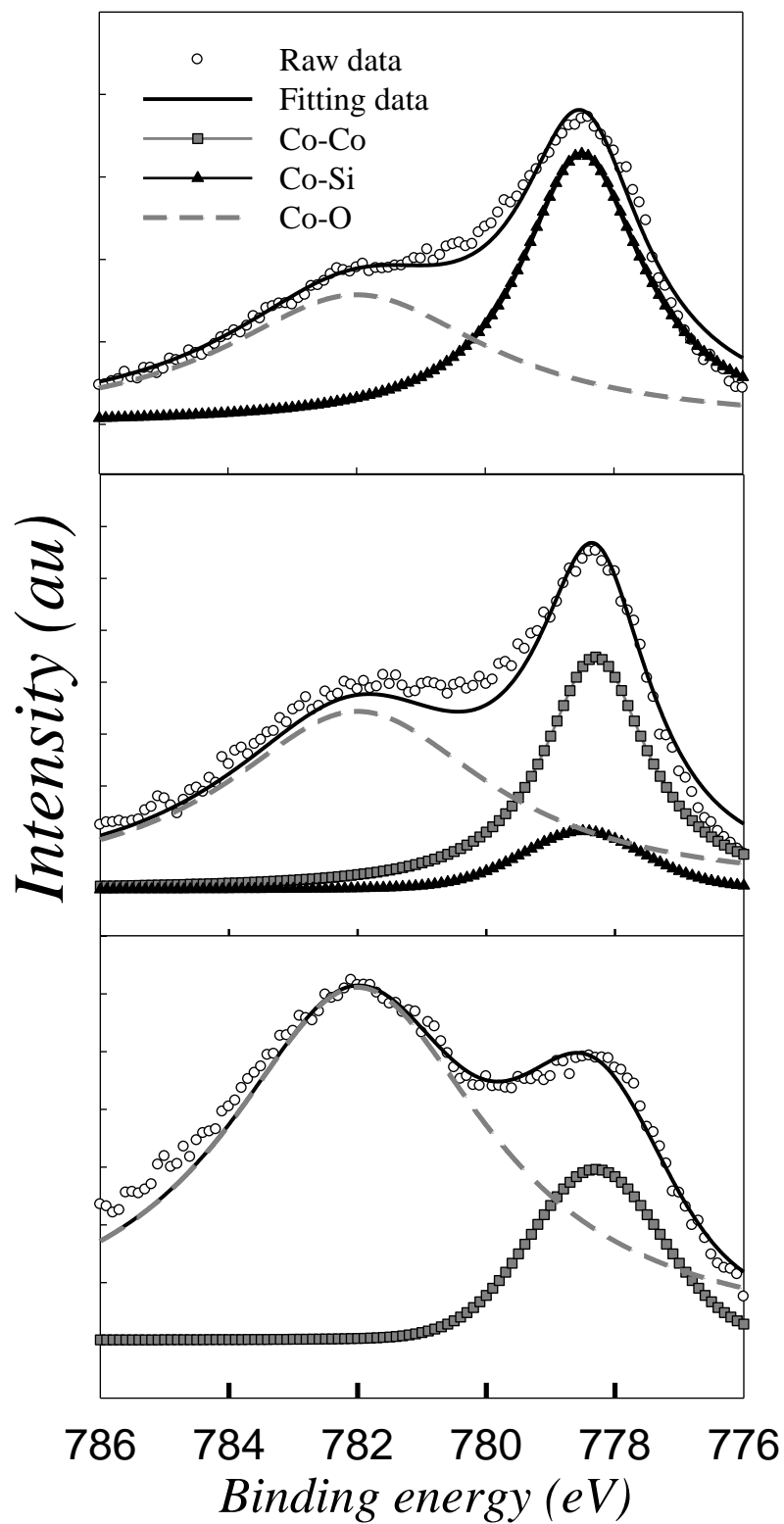


Fig. 4-8 The comparison of the Co 2p XPS spectra about the Co NC devices with 2, 5, and 7 of O₂ flow rate during the sputtering process.

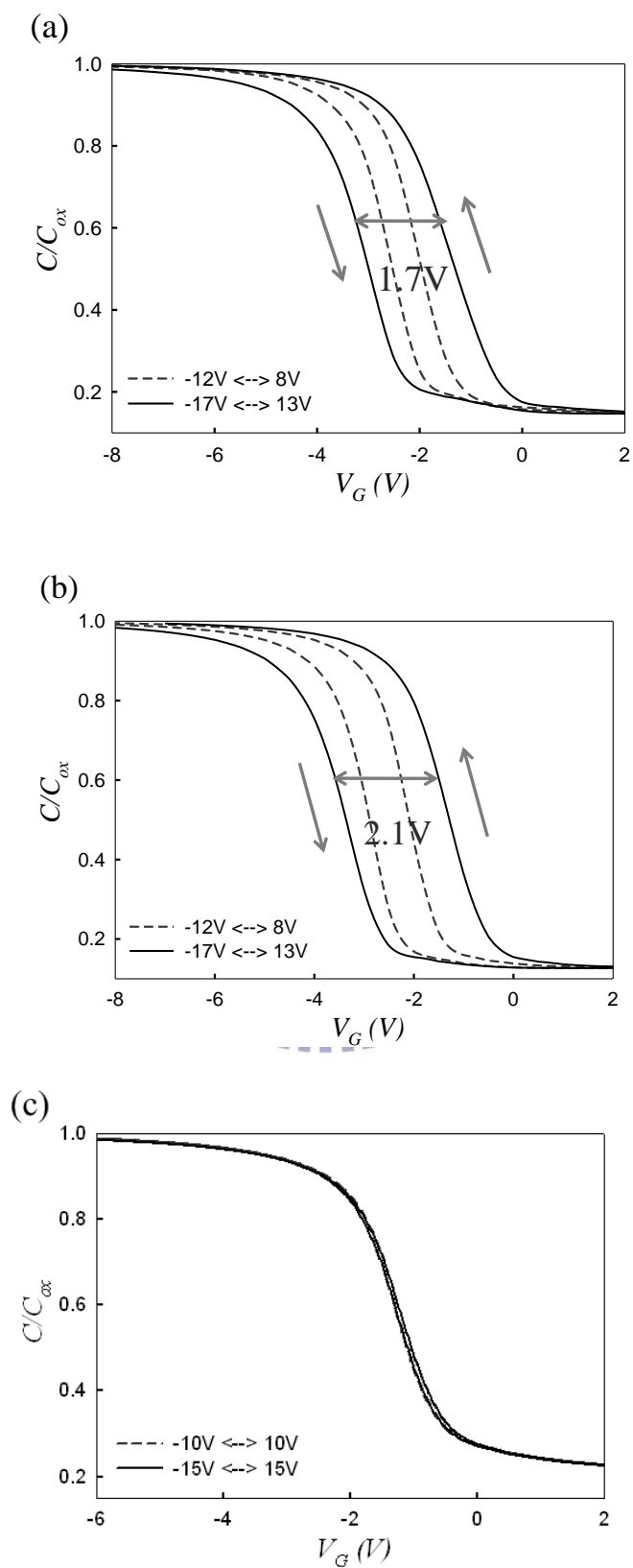


Fig. 4-9 The C-V hysteresis of the CoSi_2 thin film deposited at (a) 5sccm (b) 10sccm (c) 20sccm of the nitrogen flow rate.

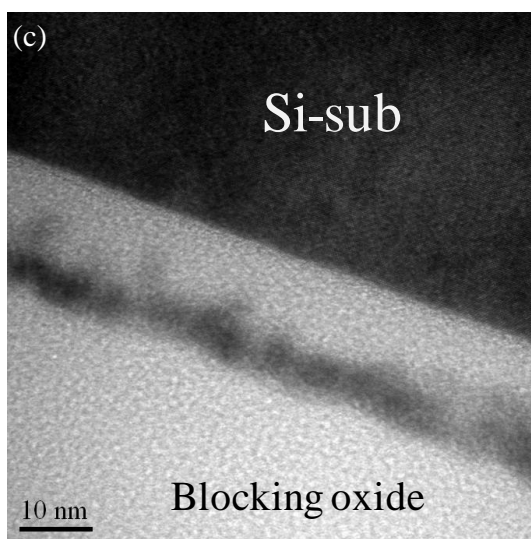
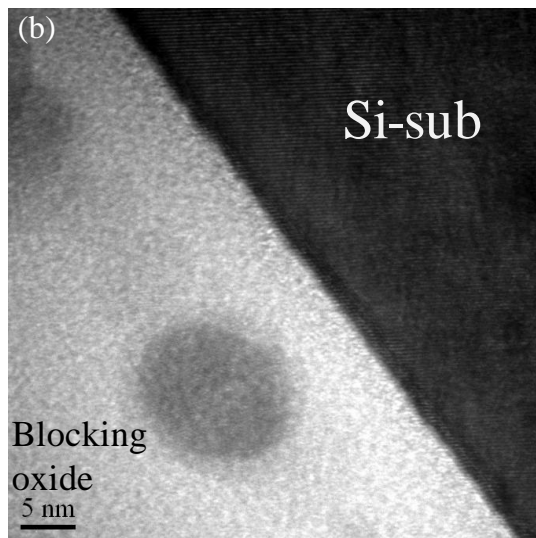
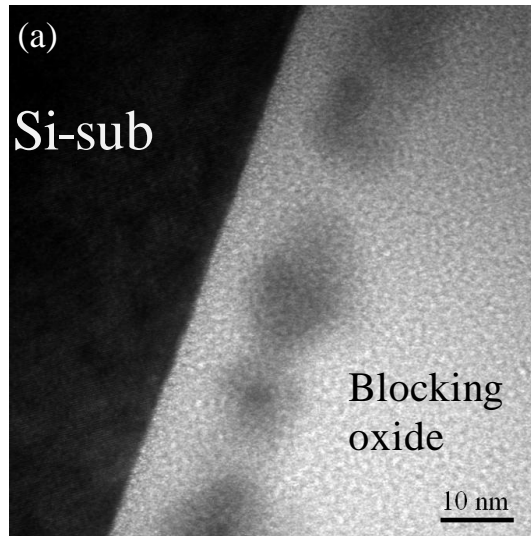


Fig. 4-10 The cross-sectional TEM images of the CoSi_2 thin film deposited at (a) 5sccm (b) 10sccm (c) 20sccm of the nitrogen flow rate.

Chapter 5

Fabrication and Investigation on the Application of Ni-Si-Ge Nanocrystal for Nonvolatile Memory

5.1 Enhancement of NiSi-based nanocrystal formation by incorporating Ge elements for nonvolatile memory devices

5.1.1 Introduction

In the recent years, the arrays of NC structure attracts much attention in several applications such as the nano-scale pattern, magnetic data storage, light emitting devices and nonvolatile memory devices [5.1-5.4]. With the difference of the application, finding a suitable material to satisfy the requirements is a major subject. NiSi-based NC is considered as the possible material for the current memory manufacturing technology due to its compatibility and low-resistivity [5.5-5.6]. The uniformity and density of NC distribution are also the essential issue for the NC formation engineering. Several methods to form a high density distribution NC structure have been proposed in previous research [5.7-5.8]. In addition, it is disadvantageous to apply the NC into the device process if the NC formation needs a high fabricating temperature. Self-assemble method indicates that the aggregation of NC depends on the nucleation centers and growth rate [5.9-5.10]. The method to enhance the NC aggregation through diffusing additional elements to be extra

nucleation centers has been proposed to improve the NC characteristic [5.11]. Therefore, we think that adjusting the compositions of the self-assembled film to increase the nucleation centers is the possible method to enhance the NC formation. An easier formation process for the NC is advantageous to control the size and density distribution.

In this section, the nickel-silicon-germanium (NiSiGe) mixed film was prepared by co-sputtering NiSi₂ and Ge targets on the 6-inch silicon wafer with a 5nm thermal oxide, simultaneously. A RTA was used to treat the stacked structure with NiSiGe and NiSi thin film, respectively. The uniformity and density of the NC were also estimated by TEM. In addition, detailed compositions of the annealed film were analyzed by XPS, Raman spectroscopy and energy dispersive spectrometer (EDS) system. Then, the NC formation behaviors are speculated by the material analyses results. We also fabricated the memory device using the NiSiGe and NiSi NC as charge trapping layer to investigate the charge-storage ability. Superior electrical characteristics of NiSiGe NC memory devices such as C-V, retention and endurance characteristics have also been demonstrated and discussed.

5.1.2 Experiment

Fig. 5-1 is the process flow of the experiment. First, a 5-nm-thick oxide was grown on the p-type silicon wafer in APCVD furnace. Afterward a 6-nm-thick

NiSiGe mixed film was deposited by co-sputtering approach. Then, a 20-nm-thick capped oxide was deposited to form a tri-layer structure by PECVD system. Subsequently, a RTA at 600°C was performed for 30sec in N₂ ambient to form NC structure. After the RTA process, a 30-nm-thick blocking oxide was capped by PECVD system. Finally, Al gate electrode was patterned to form MOIOS structure. In addition, the structure with NiSi NC was formed by the same process for comparison. After the fabricating of devices, we studied the formation of the NC by related material analyses and the charge-storage ability of the memory devices by electrical measurements.

5.1.3 Result and discussion

The plane-view and cross-section TEM images of the fabricated samples are shown in Fig. 5-2. The Fig. 5-2 (a) and (b) indicate the NiSi and NiSiGe layer after the thermal annealing process, respectively. It is found the NC was nucleated between the tunneling oxide and blocking oxide after the annealing process. We also calculated the NC density and size from the plane-view TEM. It is found that the NiSiGe NC reveal lager density and size distribution. We think that the improved NiSi-based NC formation could be attributed to the help of Ge elements. In order to further realize the NiSiGe NC formation, the XPS spectra was used. Fig. 5-3 (a) demonstrates the Ni 2p_{3/2} XPS spectra of the NiSi and NiSiGe mixed film after thermal annealing. The NiSi₂ signal is determined in both samples. In addition, there is less difference

between the samples. The main difference of XPS spectra between annealed NiSi and NiSiGe thin film is found at Ge 3d result as shown in Fig. 5-3 (b). The Ge-Ge peak at ~29.4eV is found in Fig. 5-3 (b), which is reference to the annealed NiSiGe sample. Furthermore, a higher binding energy is found at ~31.5eV, reported by the previous literature indicated as nickel-germane-silicide (Ni-Si-Ge) binding [5.12]. Hence, the NiSiGe annealing process includes of Ge-Ge, Ni-Si and Ni-Si-Ge formation. The appearance of peak at 29.4eV is due to that partial Ge elements tend to segregate out at high temperature thermal process [5.13]. In addition, it is believed that the unobvious Ni 2p_{3/2} XPS binding energy shift in the annealed NiSiGe film is because that the binding energy between NiSi₂ and Ni-Si-Ge are close. Then, it is difficult to recognize the difference between the samples.

Fig. 5-4 (a) is the Raman spectra of the annealed NiSiGe samples. We found that for the annealed NiSiGe film, there is a broad peak at about 220cm⁻¹, corresponding to the Ni-Si-Ge phase. Whereas a Ge-Ge peak peaks at about 300cm⁻¹, was found at 600°C thermal annealed samples [5.14]. In addition, the EDS analysis was used to analyze the compositions of the NC as shown as Fig. 5-4 (b). The electron beam of the EDS analysis was focused at the NC region about 10nm. We found that the NC composed with Ni, Si and Ge elements. Through the results of the material analyses, it is believed that the main composition of the NC is not pure NiSi₂ because the Ge

can be the initial nucleation centers to form the NC. Compared with the NiSi mixed film, the NiSiGe layer offers more additional nucleation centers for the NC formation. Therefore, the NiSiGe film provides a more complete nucleation process and induces a higher size and density distribution at lower fabricating temperature.

The detail nucleation of NiSi-based NC during the RTA process is speculated as shown in Fig. 5-5. From the reported literature, the Ge elements tend to precipitate during the thermal annealing [5.15]. In NiSiGe film, NiSi₂ and Ge serve as nucleation centers at the initial of thermal annealing process. For detailed compositions, the starting clusters include Ge-Ge and Ge-O which are evidenced from the XPS analysis as shown in Fig. 5-3 (d). The additional nucleation centers enhance the NC nucleation and bring larger density in the annealed NiSiGe sample. The advantage for the addition of the Ge elements also involves the low temperature process. The characteristics, such as density and size, of the NiSiGe NC formation at 600°C are superior to the conventional NiSi NC formation at 700°C. Hence, the NiSi-based NC with better size and density distribution can be obtained at lower temperature by adding Ge elements.

In order to study the feasibility for the NiSiGe NC to apply into the memory devices, the MOIOS structure had been fabricated and measured. Fig. 5-5 shows the C-V hysteresis after bidirectional sweeps, which implies electron charging and

discharging effect of the memory device. In Fig. 5-6 (a), the conventional NiSi NC memory device shows ΔV_{FB} shift of 4.5V under ± 10 V gate voltage operation. In contrast to the NiSi NC, the NiSiGe NC memory device exhibits 9V of ΔV_{FB} in Fig. 5-4 (b). We think that the larger memory device of NiSiGe, is advantage to be defined as “1” or “0” for the logic-circuit design, results from the improved NC size and density distribution. An early nuclei formation can bring a larger NC size and better uniformity distribution to improve the charge-storage performance of memory device.

Fig. 5-7 shows the data retention characteristic of (a) NiSi NC and (b) NiSiGe NC device. It is found that the NiSiGe NC device reveals better data retention ability than the NiSi NC after 10^4 sec. The better retention characteristic is because the NiSiGe NC have lower quantum confinement effect due to the larger NC size distribution. According the reported literature, the NC (<2nm) is difficult to apply into the NC memory devices because the quantum confinement effect depends on the NC size strongly [5.16-5.17]. The better uniformity of NiSiGe NC can reduce the possibility that the stored charge tunnel back during the retention test. In addition, it is also found that an obvious charge-storage decay at the initial 10^3 sec for the NC devices. We think that decay is because the charges stored in the shallow traps are easy to lose. Nevertheless, both of the NiSi and NiSiGe NC memory devices can keep steady after the decay. Fig. 5-8 shows the endurance characteristics of NiSi and

NiSiGe NC memory. After 10^6 operation cycles, the performance of the NC memory devices reveals an un-obvious degradation. We think the endurance behavior is related to the quality of the tunneling oxide, which was deposited by the same APCVD process in our experiment. Therefore, the devices show similar characteristic for the endurance test. Moreover, it is also confirmed that the additional Ge does not degrade the quality of the tunneling oxide and affect the reliability of the NC memory devices [5.18]. The NiSiGe NC memory device can provide an enough reliability characteristics for the application of nonvolatile memory devices.

5.1.4 Conclusion

In conclusion, it has been studied that the formation of NC by incorporating Ge elements into NiSi. Better uniformity and density is found in the annealed NiSiGe samples. It is resulted from that the Ge elements offer more nucleation centers to help the formation of the NC. In addition, the incorporated Ge method with lower thermal budget is advantage to apply to the current devices fabrication. We also demonstrate the NiSiGe NC memory devices formed by annealing the NiSiGe film. The NiSiGe NC memory device shows a superior memory window to the conventional NiSi NC due to the improved formation process. The better size and uniformity of NC is principal reason for the improved charge-storage ability. In addition, we also tested the reliability characteristic of the NiSiGe NC memory device

by retention and endurance measurement. The good reliability characteristic of the NiSiGe NC device is also advantageous to the memory devices.

5.2 Formation of the distributed NiSiGe nanocrystal nonvolatile memory formed by rapidly annealing in N₂ and O₂ ambient

5.2.1 Introduction

In this section, electrical characteristics of the NiSiGe NC memory device formed by the RTA in N₂ and O₂ ambient have been studied. The trapping layer was deposited by co-sputtering the NiSi₂ and Ge, simultaneously. Transmission electron microscope results indicate that the NiSiGe NC was formed obviously in both the samples. The memory devices show obvious charge-storage ability under capacitance-voltage measurement. However, it is found that the NiSiGe NC device formed by annealing in N₂ ambient has smaller memory window and better retention characteristics than in O₂ ambient. Then, related material analyses were used to confirm that the oxidized Ge elements affect the charge-storage sites and the electrical performance of the NC memory.

5.2.2 Experiment

The fabrication of memory structure was started with a 5-nm-thick oxide grown on the p-type silicon wafer in APCVD furnace. Afterward a 6-nm-thick NiSiGe thin film was deposited by co-sputtering the NiSi₂ and Ge targets, simultaneously. Then, a

20-nm-thick capped oxide was deposited to form a tri-layer structure by PECVD. Subsequently, the samples were divided into two groups, which is annealed by the RTA (sample A) and RTO (sample B) processes at 600°C for 60sec, to form the NiSiGe NC structure. After the formation processes, a 30-nm-thick blocking oxide was capped by PECVD system. Finally, Al gate electrode was patterned to form MOIOS structure. After the fabricating of memory device, electrical measurements were used to study the charge-storage ability and material analyses were used to clarify the reason for causing the difference of electrical performance between the sample A and B.

5.2.3 Results and discussion

Fig. 5-9 (a) and (b) demonstrates the cross-sectional TEM images of the formed trapping layers after the RTA and RTO process, respectively. The result shows that the NiSiGe NC uniformly distribute between the blocking oxide and the tunneling oxide obviously. The size and density, which is about 8-10 nm and $1.42 \times 10^{12} \text{ cm}^{-2}$, are similar in the samples. The NC formation mechanism is that the Ge element, which is easier to form nano-clusters at lower annealing temperature, can be the initial nucleation center for the enhancement of NiSiGe NC formation. The NiSiGe NC were aggregated steady if the enough energy was provided by the annealing process. In addition, it is also found that the additional oxidation did not affect the formation of

NC obviously.

High-frequency C-V characteristic was used to investigate memory effect of the sample A and B as shown as the Fig. 5-10. The sweeping gate voltage was set at $\pm 5V$ and $\pm 10V$. In the C-V measurement, a positive voltage is used to promote the electron of channel to pass through the tunneling oxide and stored in the NC under the write mode. Then, the stored electron of the NC induce a ΔV_{FB} as the “1” state for the memory device. In contrast, the stored electron tend to tunnel back to the Si substrate when a negative voltage is applied to the gate electrode at erase mode operation. Then, the ΔV_{FB} is think as the “0” state of the memory device. As shown as the Figures, the sample A and B both reveal a remarkable memory window, which is advantageous to provide an enough judgment for the logic circuit. However, it is also found that the NiSiGe NC device formed by RTO get a larger memory window than by RTA process.

In the endurance measurement, sample A and B were tested by the continuous voltage pulse set at $\pm 5V$ for 1msec. A negligible degradation of the memory window of the sample is observed after a 10^6 write/erase cycles operation as shown as the Fig. 5-11. The result is because the endurance performance is related to the quality of the tunneling oxide strongly, which was formed by the same APCVD process in our experiment. Therefore, the tunneling oxide shows similar ability for the repeated

operation. In addition, the retention measurement was performed at room temperature by operating a $\pm 10\text{V}$ gate voltage stress for 10sec and measured up to 10^4sec . As shown as the Fig. 5-12, sample A maintain a 2.5V (~57%) of ΔV_{FB} but sample B only keeps a 2V (~39%) of ΔV_{FB} . In general, the retention can be improved by the additional oxidation process to reduce the defect existed in the device [5.19]. However, the RTO-treated sample shows a different tendency in the retention characteristic.

To study the retention characteristic of the devices further, more material analyses had been used. Fig. 5-13 (a) and (b) demonstrate the Ge 3d XPS results of the trapping layers after the annealing processes. As shown as the Fig.s, the main compositions of the trapping layer after RTA and RTO process includes Ge-Ge (29.4 eV), Ni-Si-Ge (31.5 eV) and Ge-O (32.5 eV) [5.20-5.21]. The Ni-Si-Ge peak of the XPS indicates the NiSiGe NC formation and the Ge-Ge peak may results from the initial Ge nuclei. In addition, it must be noted that both the sample A and B have the Ge-O signal. The amount of the Ge-O can be extracted by calculating the area of the XPS data approximately. It is found that the amount of Ge-O in RTO sample is higher than in RTA one obviously. The better memory window of the RTO sample may be attributed with that the Ge-O can provide additional charge storage sites for the device. However, the Ge-O elements also play a critical role in the device retention

characteristic. Fig. 5-14 is the current J-V results of the sample A and B. It is found that the RTO-treated one shows a higher leakage current under the J-V measurement. Then, we assume the RTA- treated sample as the standard sample. The tunneling and blocking oxide of the devices are formed by the similar process. The main different composition between RTA- and RTO-treated samples is the concentration of additional Ge-O. Therefore, the difference of the current density can be thought as the contribution of the Ge-O trap. With the amount of the Ge-O, the current density of the devices is increased. Moreover, the SIMS of the sample B has also been proposed in the Fig. 5-15 to support the conclusion of the J-V result. It is found that an obvious Ge signal was accumulated at the interface between the tunneling oxide and trapping layer of the sample B. Although confirmed to be the additional charge-storage sites for NVM, the Ge-O also provides an extra leakage path to enhance the stored charge to lose [5.22-5.23]. Therefore, the retention characteristic decays obviously as the increase of the oxidized Ge.

5.2.4 Conclusion

In conclusion, the formation and memory effect of the NiSiGe NC formed by RTA and RTO process have been demonstrated. It is found that both of the RTA- and RTO-treated samples have a remarkable memory effect and reliability characteristics. In the retention test, the RTA-treated sample has a better retention performance than

RTO-treated one. The related material and electrical analyses confirm that additional oxidation process is the important parameter to affect the charge-storage ability of the memory devices. Moreover, the oxidation of Ge elements is difficult to avoid during thermal process even if the Si (-204.75 kcal/mol) has lower oxidation free energy than Ge (-111.8 kcal/mol) [5.24-5.25]. Although the Ge elements can enhance the memory performance, the oxidation process still needs to be controlled carefully because the extra defects, provided by the formed Ge-O, cause the stored-charge to loss easily and decay the performance of NVM devices.

5.3 Improved aggregation of the NiSiGe nanocrystal by pre-capping oxide method for nonvolatile memory device application

5.3.1 Introduction

In this section, a NiSiGe film was deposited by co-sputtering approach. After the mixed film deposition, three kind of oxide thickness were deposited before the annealing process to improve the NC aggregation. After the RTA, it is found that the structure with a 20nm pre-capped oxide shows the most obvious NC aggregation among the samples by TEM analyses. EDS results were used to indicate the formed NC includes Ni, Si and Ge elements. Then, the effect of the pre-capped oxide for the NC aggregation during the forming process was proposed. In addition, the charge-storage ability of the formed NiSiGe NC memory devices has also been

discussed by fabricating capacitor structure. Through the material and electrical results, we think the capped oxide method is easy and effective to improve the NiSiGe NC formation further.

5.3.2 Experiment

The fabrication of memory structure as shown as the Fig. 5-16 was started with a 5-nm-thick oxide grown on the p-type silicon wafer in APCVD furnace. Afterward a 6-nm-thick NiSiGe thin film was deposited by co-sputtering the NiSi₂ and Ge targets, simultaneously. Then, 10- and 20-nm-thick capped oxide was deposited on the partial samples to form a tri-layer structure by PECVD. Subsequently, the samples were annealed in N₂ ambient at 600 °C for 30 sec, to form the NiSiGe NC structure. After the formation process, a total 50-nm-thick blocking oxide (SiO₂) was formed by PECVD system. Finally, Al gate electrode was patterned to form the capacitance structure. After the fabricating of memory device, electrical measurements such as C-V, retention and endurance characteristics were used to study the charge-storage ability of the devices.

5.3.3 Result and discussion

Fig. 5-16 demonstrates the cross-section TEM images of the deposited NiSiGe film before and after the annealing process. The deposited NiSiGe film is about 6 nm as shown as the Fig. 5-16 (a). The forming process of NC is that atoms of the mixed

film can diffuse if the thermal process provides enough energy. The diffused atoms were driven to form NC to reduce the internal energy of the self-assembled system [5.26]. Then, the interface stress and surface free energy induce the NC aggregate at the interface of tunneling oxide. However, it can be found that the NC cannot separate completely at 600°C annealing process as shown as the Fig. 5-16 (b). A easy pre-capped oxide process before the NC formation can improve the separation of the NC as shown as Fig. 6-16 (c)-(d).

Fig. 5-17 is the EDS analyses of the formed NC structure to study the composition of the NC. During the EDS analyses, the electron beam was focused at the NC region about 10nm. Region *a* and *b* are the space and NC region, respectively. The main compositions of the NC include Ni, Si and Ge signal as shown as the EDS of region *b*. In contrast, that region *a* only have slight Ni and Ge means the complete NC aggregation. Through the EDS analyses, it also confirms that the NiSiGe NC formation is through the aggregation of the elements during the thermal annealing. The mechanism for the RTA system to accomplish the NC formation is through the heat provided by the light absorption of the Si substrate or the mixed film. The heat lose easily because the larger temperature gradient between the substrate and RTA chamber. Moreover, the pre-capped oxide play a heat-accumulation layer to reduces the heat loss behavior and enhances the NC aggregation even at lower temperature

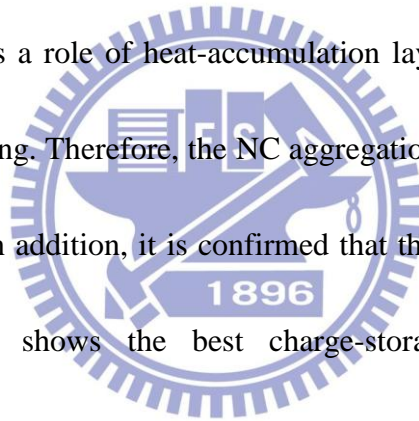
annealing process. Hence, the increase of the pre-capped oxide thickness brings a more complete NC aggregation.

To study the memory effect of the NC aggregation for the nonvolatile memory application, a high-frequency C-V characteristic was used as shown as the Fig. 5-18. The sweeping gate voltage was set at $\pm 5V$ and $\pm 10V$, which is defined by flat-band voltage of the devices. It is found that the incomplete aggregation degrades the electrical performance of the memory devices indeed. As the increase of the pre-capped oxide thickness, the C-V curve of the NiSiGe NC devices is improved obviously. The devices with 20 nm pre-capped oxide shows a 9V of ΔV_{FB} under the C-V measurement. In addition, related reliability measurements had been tested as shown in Fig. 5-19. The retention measurement was performed by operating a $\pm 10V$ gate voltage stress for 10sec and measured up to 10^4 sec. It is found that sample A maintains a 1.1V of ΔV_{FB} but sample B keeps a 2.2 V of ΔV_{FB} . The poorer retention maybe resulted from the leakage paths forms due to the incomplete segregation. The structure with 20 nm pre-capped oxide has superior charge-storage and retention characteristics to sample A due to the more complete NC aggregation. Moreover, samples were tested by the continuous voltage pulse set at $\pm 5V$ for 1ms in the endurance measurement. A negligible degradation of the memory window is observed after a 10^6 write/erase cycles operation in the samples because the endurance

performance is related to the quality of the tunneling oxide, which was formed by the same APCVD process. It is confirmed that both the samples reveal a remarkable memory window, which is advantageous to provide an enough judgment for the logic circuit.

5.3.4 Conclusion

In conclusion, the aggregation of the NiSiGe mixed film has been discussed in this work. The more complete NC aggregation is found if the NiSiGe film was deposited a 20 nm pre-capped oxide before thermal annealing process. We think the pre-capped oxide provides a role of heat-accumulation layer to reduce the heat loss during the thermal annealing. Therefore, the NC aggregation can be achieved at lower fabricating temperature. In addition, it is confirmed that the NiSiGe NC formed with 20nm pre-capped oxide shows the best charge-storage performance by the measurements of the C-V characteristic, retention and endurance tests. The related material and electrical results exhibit that the NC formation with a pre-capped oxide is advantageous to lower the forming temperature.



Process flow

- (1) (100) P-type Si wafer with modified RCA clean
- (2) 5 nm SiO₂ deposited by APCVD system
- (3) 6nm NiSiGe/NiSi thin film deposited by co-sputtering method
- (4) 20nm pre-capped oxide deposited by PECVD system
- (5) RTA in N₂ ambient to form NCs structure
- (6) Blocking oxide (30nm) deposited by PECVD
- (7) Top and bottom Al electrode pattern

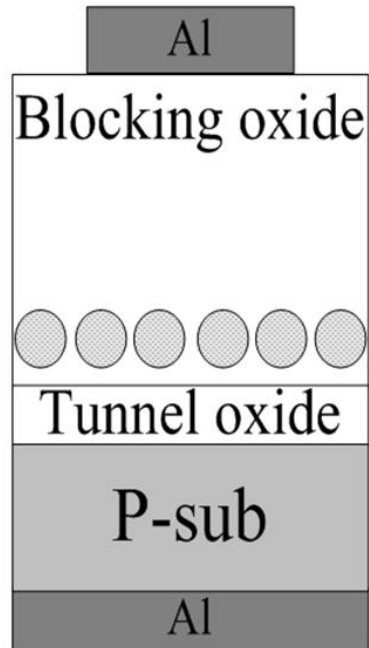


Fig. 5-1 Process of flow and device structure of this study.

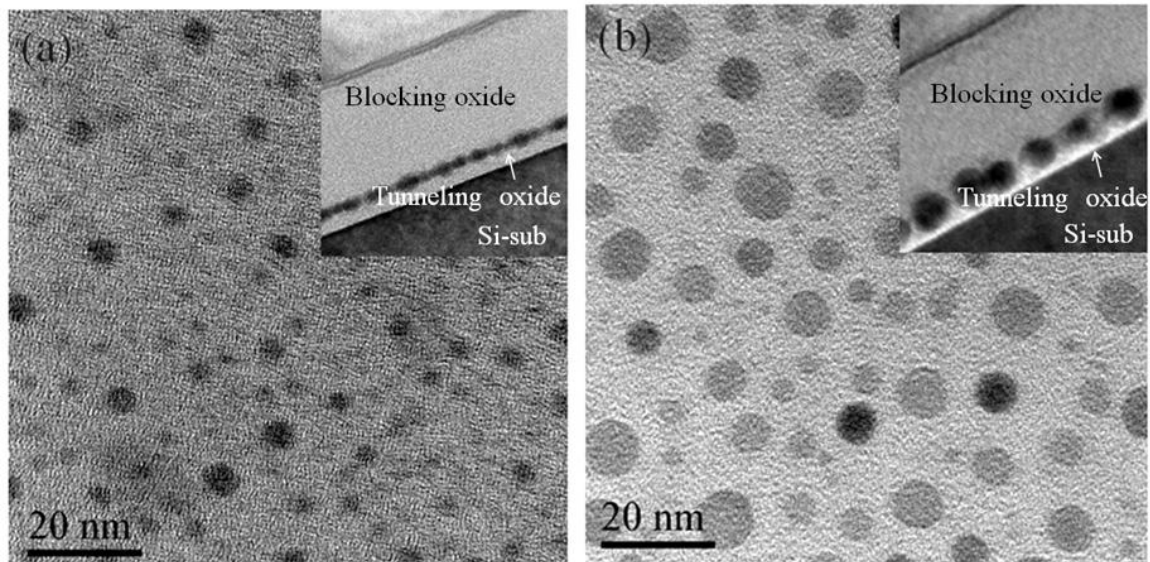


Fig. 5-2 The plane-view and cross-section TEM micrographs of the annealed (a) NiSi and (b) NiSiGe film.

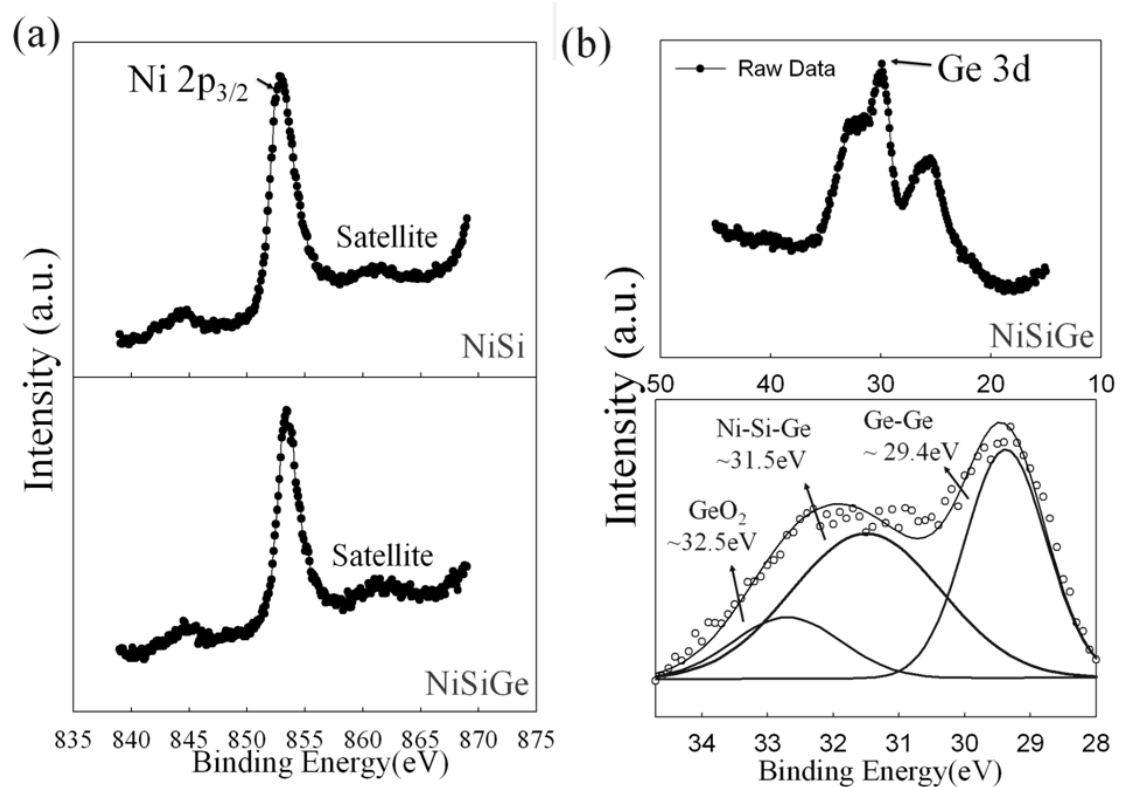


Fig. 5-3 (a) The Ni 2p_{3/2} XPS spectra of the annealed NiSi and NiSiGe mixed film. (b) The Ge 3d XPS spectra raw data and the fitting data of NiSiGe film after thermal annealing.

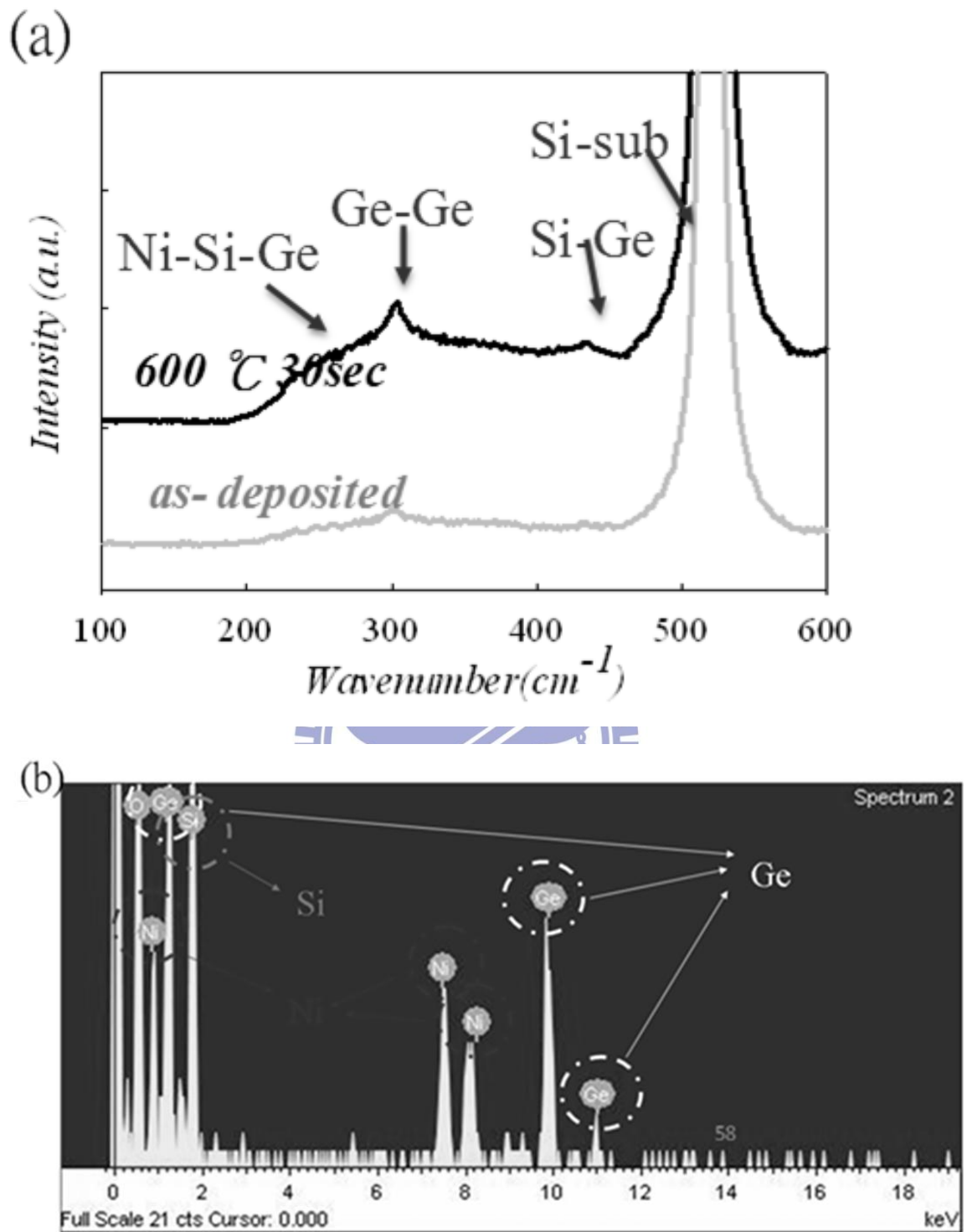


Fig. 5-4 (a) Raman spectroscopy and (b) EDS of the NiSiGe film after thermal annealing.

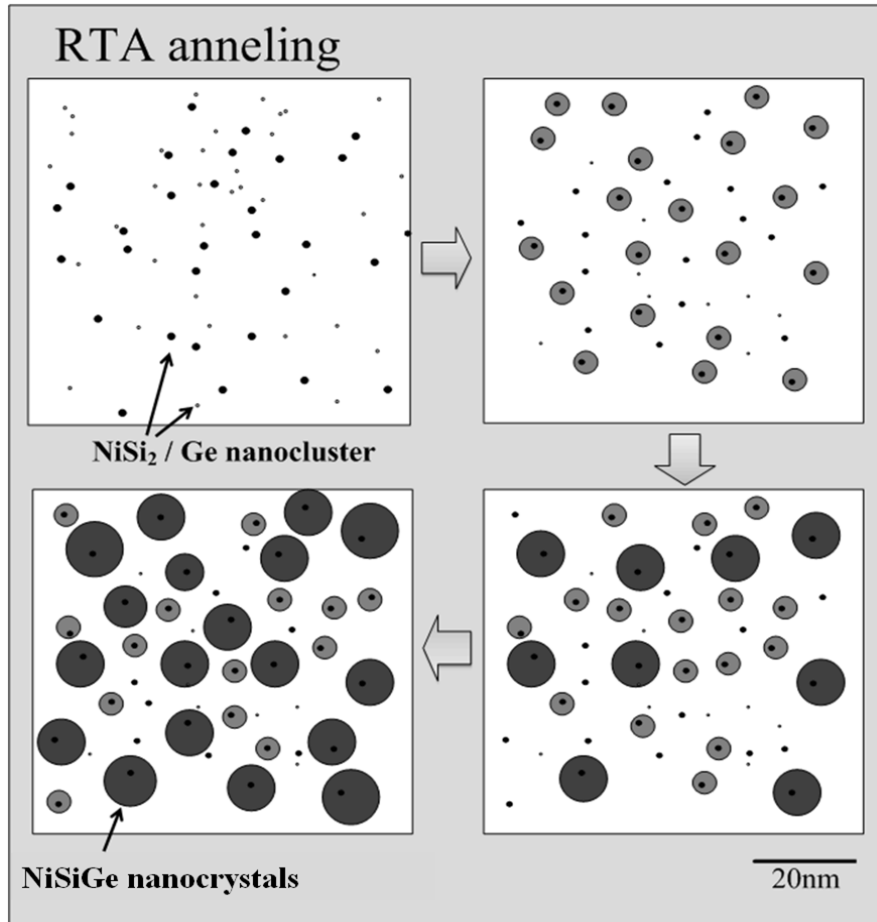


Fig. 5-5 The speculated picture for the formation process of the NiSiGe NC during RTA process.

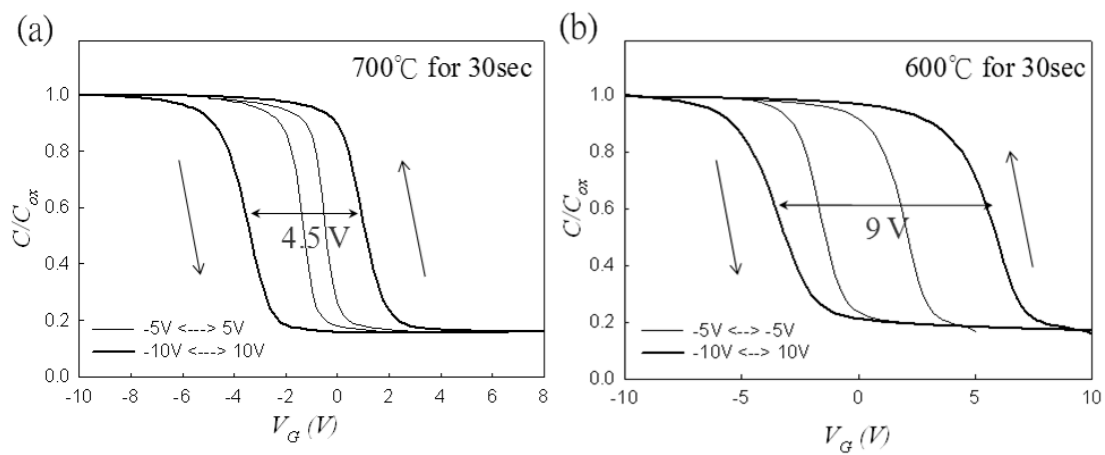


Fig. 5-6 C-V characteristics (1 MHz) of the MOIOS structures: (a) with NiSi and (b) NiSiGe NC as the trapping layer of the memory device.

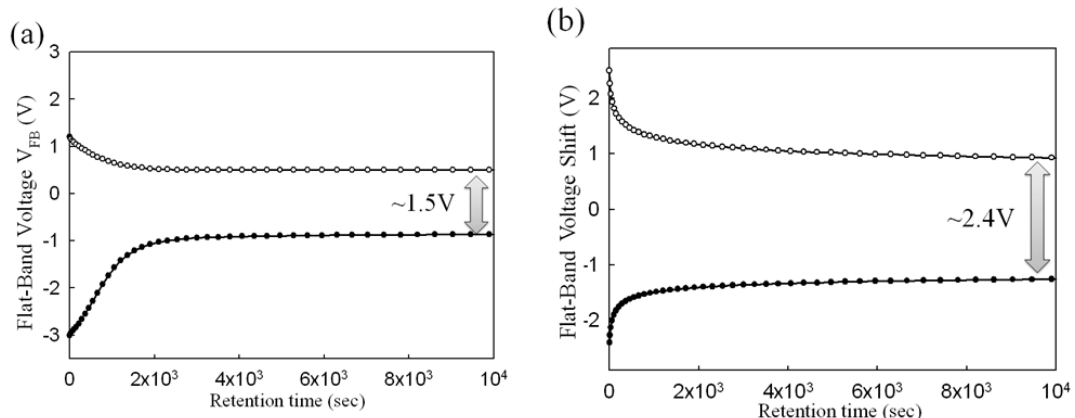


Fig. 5-7 Retention characteristics of the (a) NiSi and (a) NiSiGe NC memory devices.

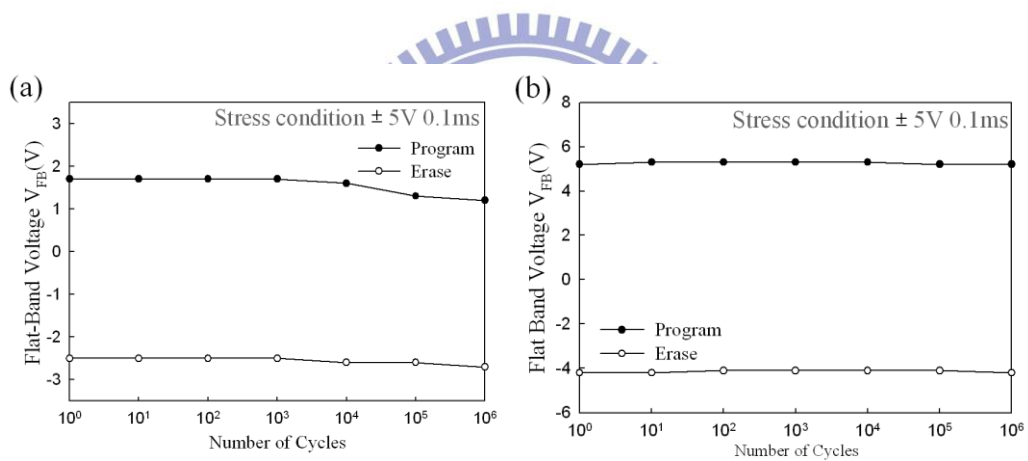


Fig. 5-8 Endurance characteristics of the (a) NiSi and (b) NiSiGe NC memory devices.

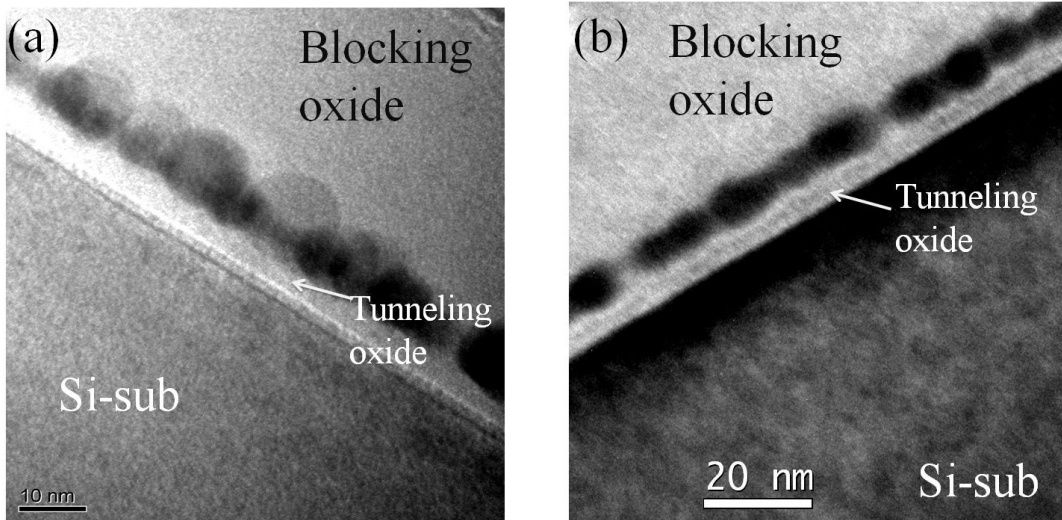


Fig. 5-9 The cross-section TEM micrographs of the NiSiGe film after the (a) RTA and (b) RTO process for 60 sec.

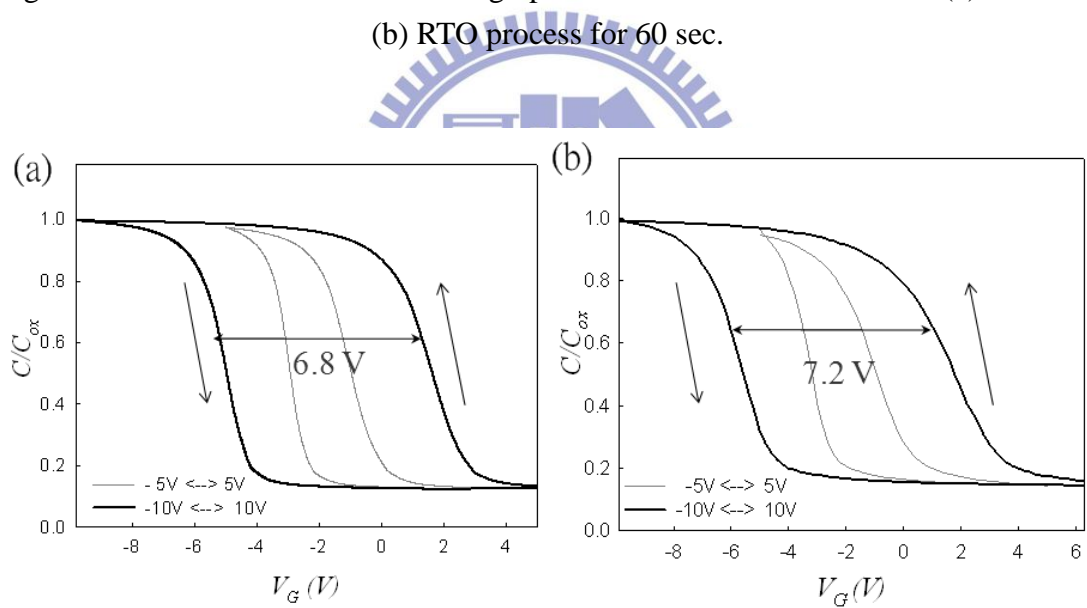


Fig. 5-10 The C–V characteristics of the MOIOS structures: NiSiGe NC formed by (a) RTA and (b) RTO process.

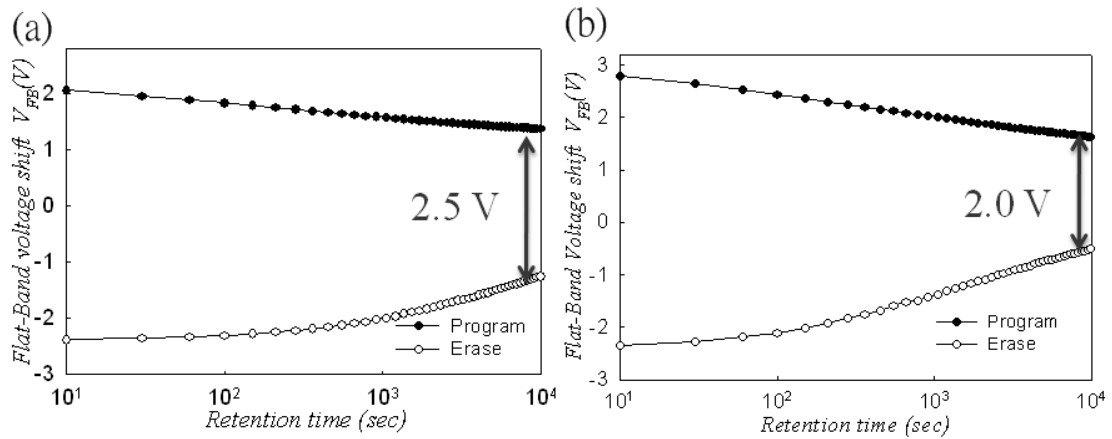


Fig. 5-11 The endurance characteristic of the NiSiGe film after (a) RTA and (b) RTO process.

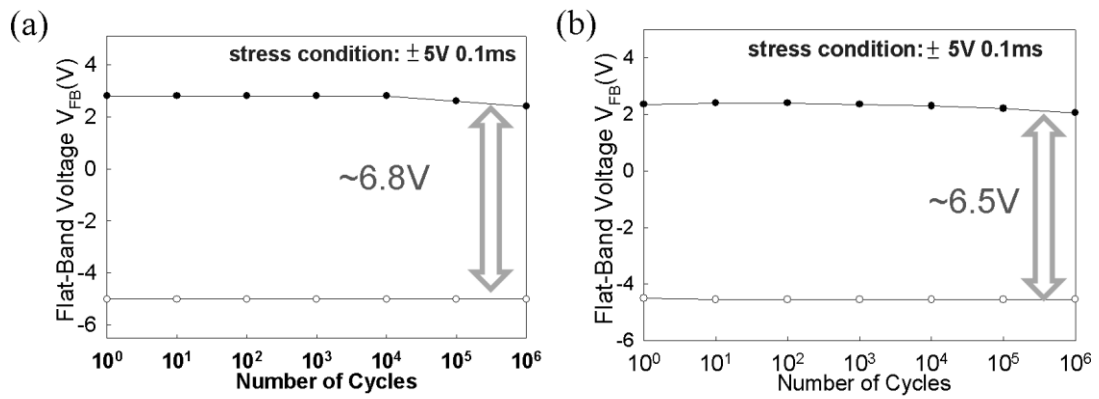


Fig. 5-12 The retention characteristic of the NiSiGe film after (a) RTA and (b) RTO process.

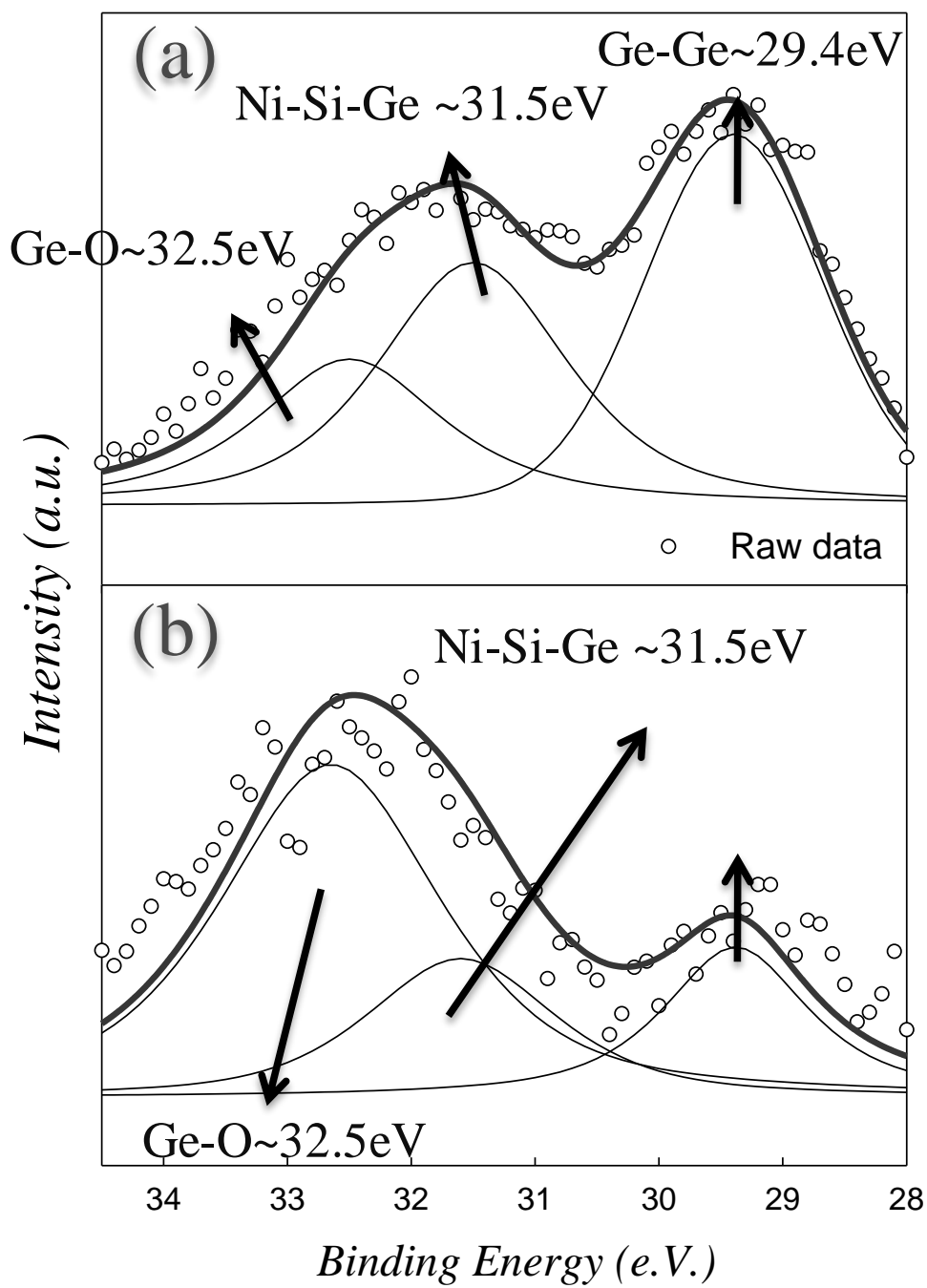


Fig. 5-13 The Ge 3d XPS spectra of the NiSiGe film after (a) RTA and (b) RTO process.

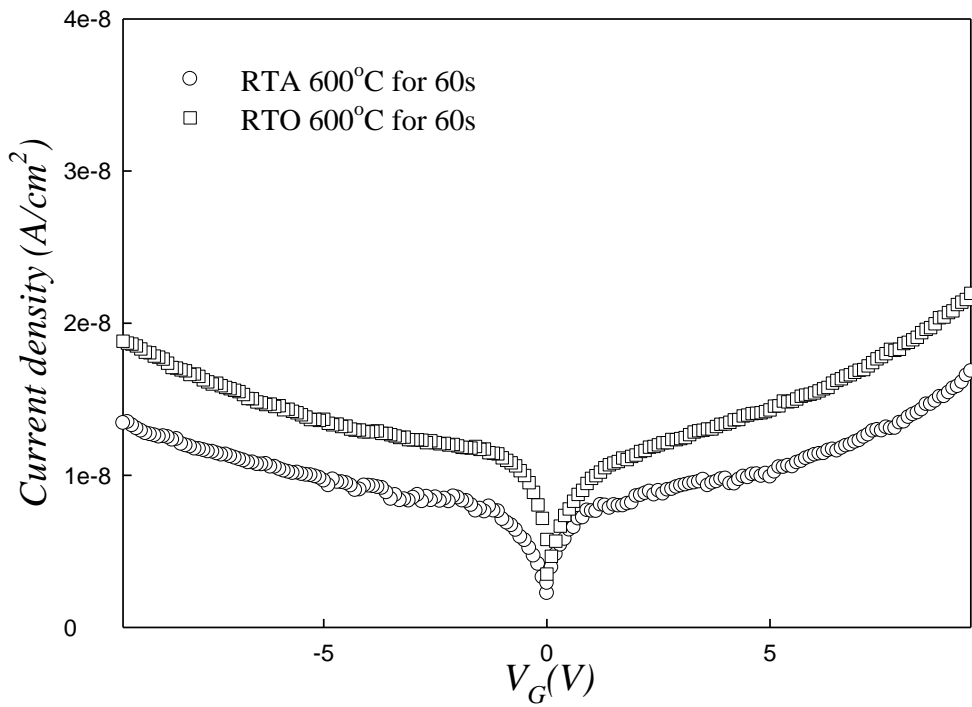


Fig. 5-14 The J-V characteristics of the NiSiGe film after (a) RTA and (b) RTO process.

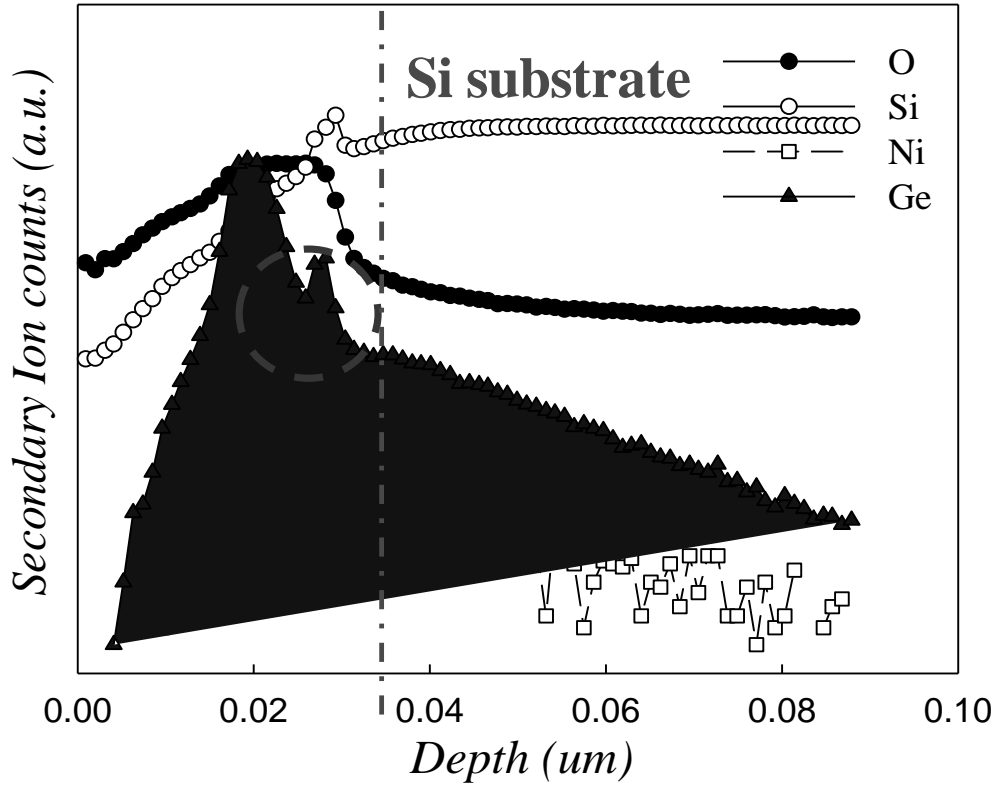
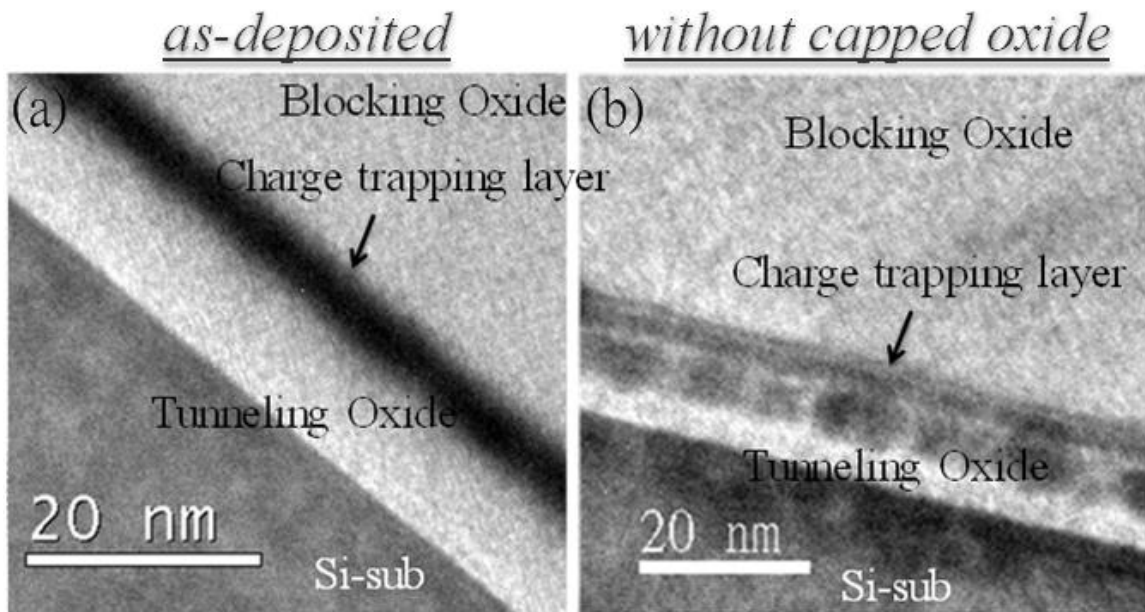


Fig. 5-15 The SIMS analysis of the NiSiGe NC formed by RTO process.



with 10 nm capped oxide *with 20 nm capped oxide*

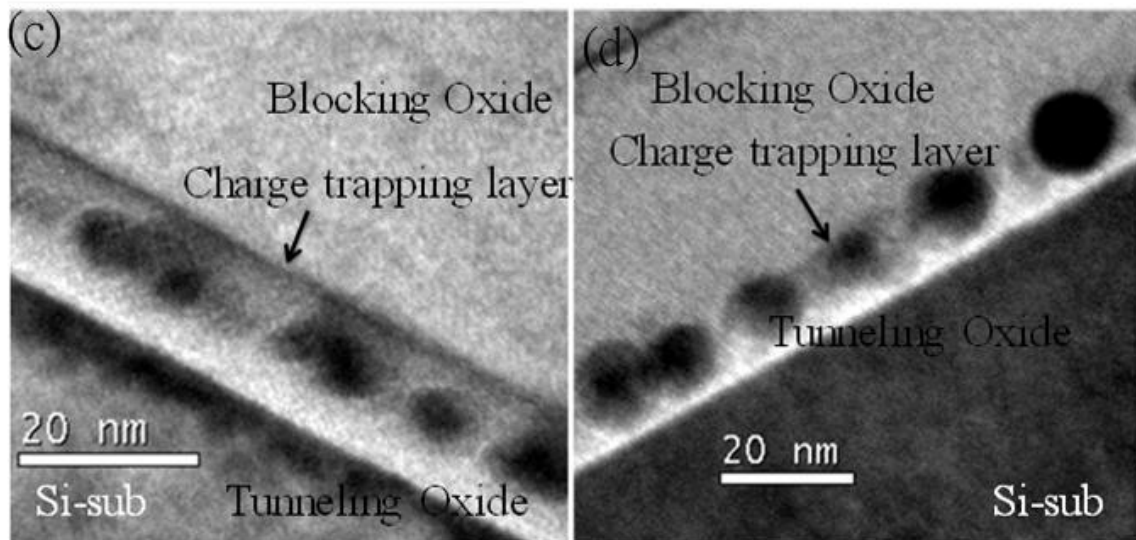


Fig. 5-16 The cross-section TEM micrographs of the NiSiGe thin film.

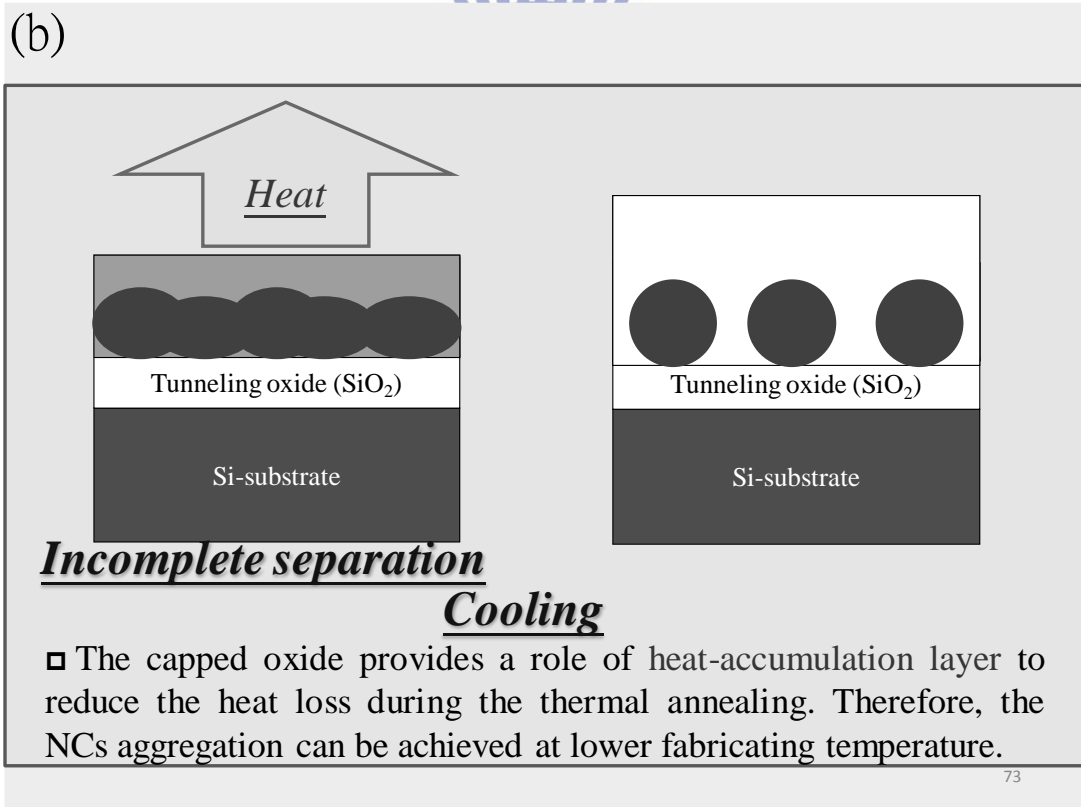
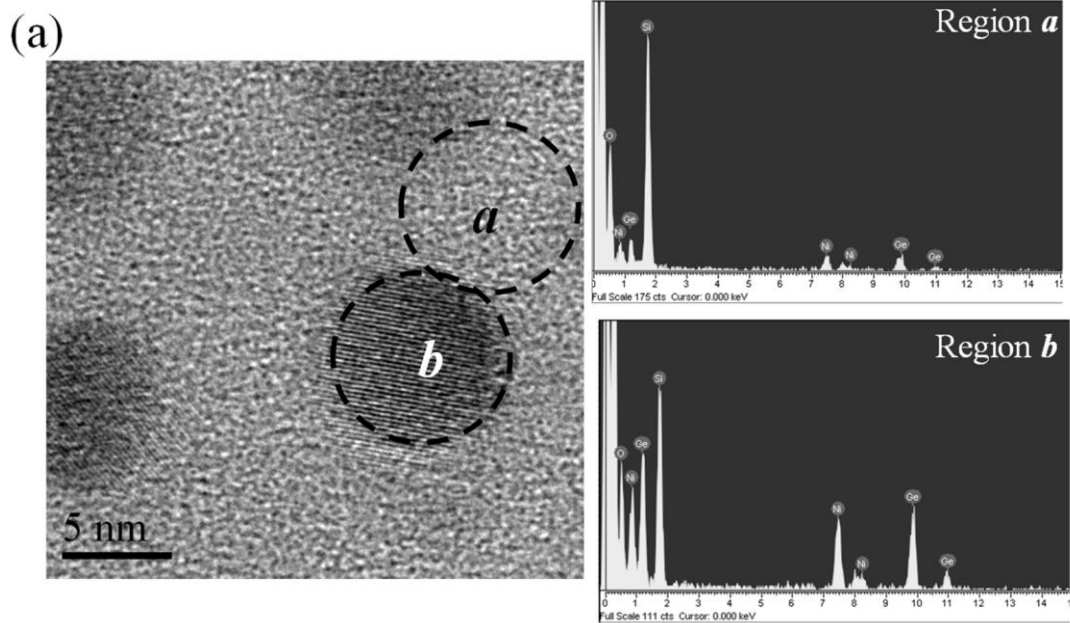


Fig. 5-17 The EDS analyses of the formed NC structure. Region a and b is the space and NC region, respectively.

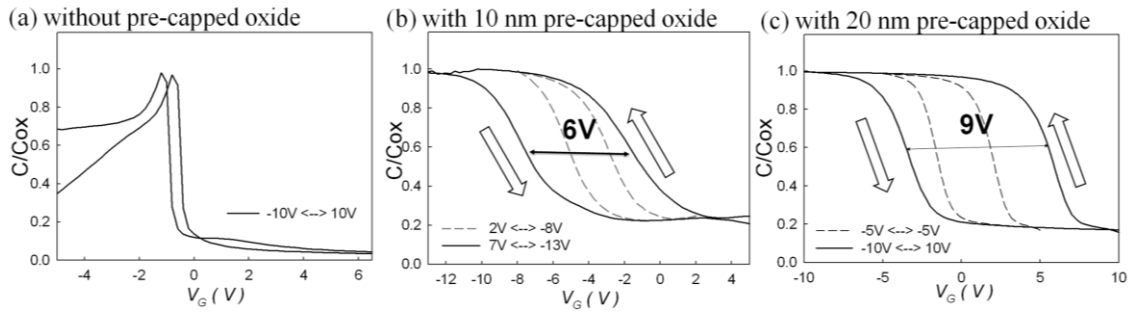


Fig. 5-18 The C-V results of the NiSiGe thin film (a) without, (b) with 10nm and (c) with 20 nm pre-capped oxide before the thermal annealing process, respectively. It is found that the structure with 20nm pre-capped oxide has the best performance among the samples.

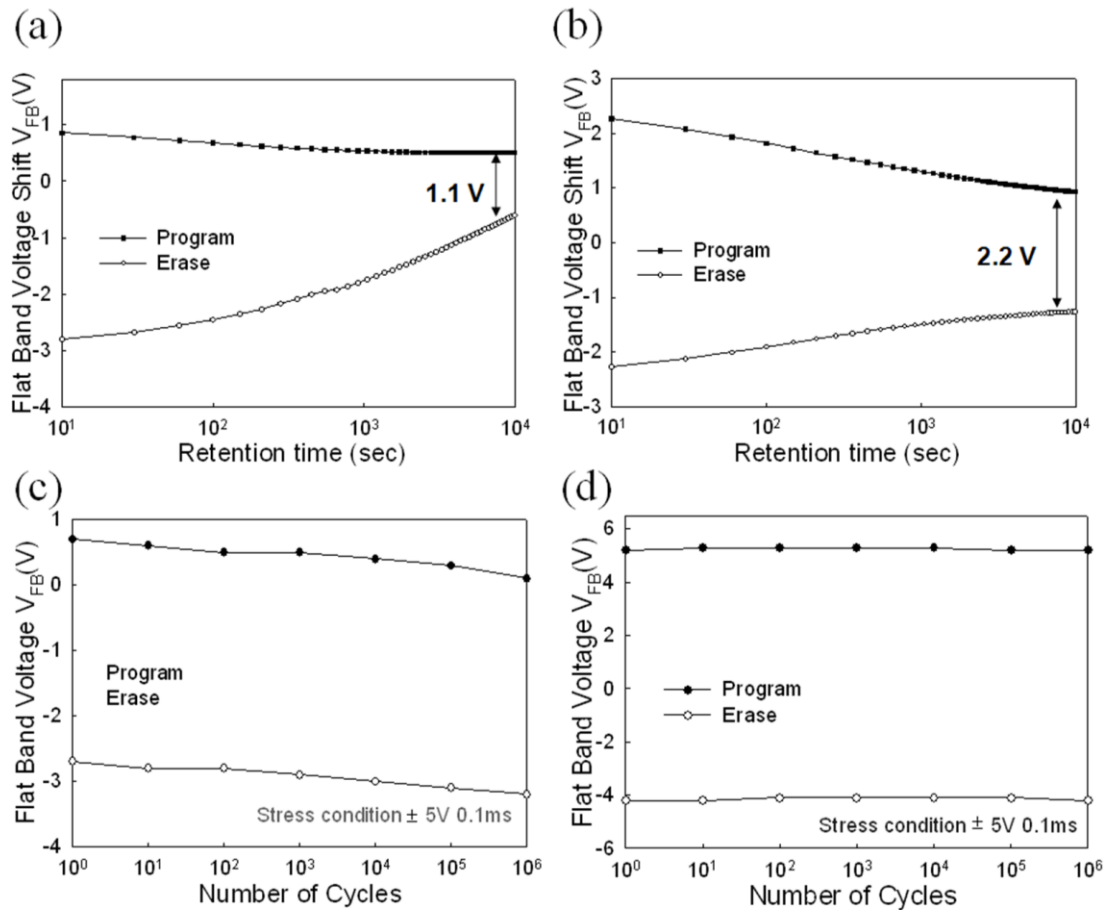


Fig. 5-19 Retention and endurance of the NiSiGe thin film (a&c) with 10nm and (b&d) with 20nm pre-capped oxide before the thermal annealing process.

Chapter 6

Nitric acid oxidation for the tunneling oxide application on CoSi_2 nanocrystal nonvolatile memory

6.1 Nitric acid oxidation of Si for the tunneling oxide application on CoSi_2 nanocrystal nonvolatile memory

6.1.1 Introduction

In recent years, the development of portable products market promotes the requirements of NVM devices. However, the tendency of device scaling down makes the conventional FG structure face the reliability challenges [6.1]. Therefore, distributed NC structure is thought as the solution of the issue because the charge is stored by individual trapping center [6.2]. In the research of NC memory devices, it can be found that the formation of tunneling oxide is still an important topic for the devices application because that the highest fabricating temperature of the current NC memory devices is not limited to the NC aggregation but the tunneling oxide deposition. A high-temperature furnace system is still the most common tool because the current NC memory devices need a tunneling oxide with adequate quality to assure its storage capacity [6.3-6.5]. Hence, a low-temperature oxide deposited technology is important for the advanced NVM devices [6.6-6.8]. Moreover, cost and throughput of the reported processes must be considered further to apply into the

current devices fabrication. Recently, it is found that nitric acid oxidation is potential to form an enough quality oxide at lower temperature [6.9-6.10]. It is believed that more detailed discussions of the nitric acid oxidation method to form the dielectric layer are advantageous to the development of low-temperature memory device technology.

In this section, nitric acid solution ($\text{HNO}_3:\text{H}_2\text{O}= 1:10$) was used to oxidize the sputtered Si thin film. After the formation of nitric acid oxidized SiO_2 (NAO- SiO_2), metal-insulator-silicon (MIS) structure was fabricated to investigate the process of the nitric acid oxidation and the effect of the post-oxidation annealing (POA). It has been indicated the POA process plays an important role for the improvement of the NAO- SiO_2 thin film by XPS analyses. Sequentially, a CoSi_2 thin film was deposited on the NAO- SiO_2 layer to be the self-assembled trapping layer. After a thermal annealing process, it is found the CoSi_2 NC aggregated on the tunneling oxide obviously. The CoSi_2 NC memory device shows excellent memory window under the C-V measurement. Moreover, the related electrical characteristics of the memory devices such as the leakage current, charge-retention and endurance have also been demonstrated.

6.1.2 Experiment

Fig. 6-1 is the process flow of the experiment. The fabrication of memory

structure was started with a sputtering process to form an about 2-nm-thick Si thin film on p-type (100) Si wafer which had been removed native oxide and particles by RCA process. Then, the Si film was immersed in the nitric acid solution ($\text{HNO}_3:\text{H}_2\text{O}=1:10$) for 60 sec at room temperature to form the NAO-SiO₂ layer. Portion of the NAO-SiO₂ were fabricated to be the MIS structure. In addition, a 6-nm-thick CoSi₂ film was deposited on the other portion of the samples by the sputtering system to be the self-assembled trapping layer. Then, the samples were annealed by RTA system set at 700°C for 30sec in pure N₂ ambience to form the CoSi₂ NC structure. After the RTA process, a 50-nm-thick blocking oxide was capped by plasma enhanced chemical vapor deposition system. Final, top and bottom Al electrodes were patterned by a shadow mask to form MOIOS structure. After the fabrication of the devices, the related material and electrical analyses were used to analyze the CoSi₂ NC memory devices using the NAO-SiO₂ as the tunneling oxide.

6.1.3 Result and discussion

Fig. 6-2 (a) and (b) show the C-V and J-V characteristics of MIS structure using the NAO-SiO₂ as the gate oxide, respectively. In the Fig. 6-2 (a), the conditions of the samples are divided as (a) without and (b) with a followed 700°C RTA treatment for 30 sec. The C-V measurement was swept from -3V to 3V to extract the quality of the oxide. It can be found that the sample without RTA treatment has an obvious ($\sim 0.5\text{V}$)

hysteresis. Moreover, the formed oxide without a POA process has an obvious leakage behavior at higher gate voltage operation and poorer uniformity of the electrical performance. However, it can be found that the hysteresis and leakage current can be improved by the followed 700°C annealing process. From the results, we think that the improved characteristics may mean that an enough RTA process can reduce the defect of the NAO-SiO₂ layer. We also extract the equivalent oxide thickness (EOT) through the C-V results. The EOT of the NAO-SiO₂ with RTA at 700 °C for 30 sec is about 4nm obtained by calculating the 88.56pF of the accumulation capacitance in C-V curves. It can be found that the result fits in with the cross-section TEM image of the inset of Fig. 6-2 (a). In addition, the J-V characteristic of the MIS structure using the NAO-SiO₂ (after 700°C annealing process) as the gate oxide has also been measured as shown as the Fig. 6-2 (b). The highest gate leakage current of the NAO-SiO₂ layer is about 10⁻²A/cm² under -2V gate voltage operation, which is lower than the defined gate limit of the reported literature [6.11-6.12]. The result also indicates the NAO-SiO₂ without serious leakage current is potential for the application of the electric device. In the J-V result, a non-symmetric leakage behavior was found obviously. It can be explained that the higher gate injection current density under negative gate voltage is resulted from the electrons injected from the Al gate to the Si substrate. In contrast, a current saturation of the J-V characteristic is found when a

positive gate bias is applied because the gate leakage current in the deep depletion region is related to the generation of minority carriers via the bulk traps and interface states in the depletion region [6.13].

Fig. 6-3 demonstrates the Si 2p XPS spectra of (a) the as-deposited Si film, the NAO-SiO₂ (b) before and (c) after the RTA at 700°C for 30sec process, respectively. It can be found that the Fig. 6-3 (a) shows a peak at about 99.3eV corresponding to the Si-Si bonding energy. In addition, we also found an additional peak at about 103eV, which is attributed with the native oxide formed during the sample fabrication. After the nitric acid immersion, an obvious Si elements transition to SiO₂ means that most of as-deposited Si film was oxidized by the nitric acid solution as shown as the Fig. 6-3 (b). Also, some sub-oxide (SiO_x, x<2) can be found that confirms the oxide still has a poorer quality. With an annealing temperature was used to improve the oxide quality, it is found that the Si-O peak was shifted toward higher binding energy and the sub-oxide element was reduced. The oxidation mechanism of the nitric acid oxidation is that the decomposition of HNO₃ can provide a high concentration of atomic oxygen with a strong oxidizing ability to oxidize the sputtered Si film. Hence, the oxidation can be accomplished by the brief nitric acid immersion and a POA treatment.

To study the feasibility for the NAO-SiO₂ layer to apply into the NC memory

device, the MOIOS structure had been fabricated and measured. After the 700°C RTA process, it is found the SiO₂ formation and CoSi₂ NC aggregation obviously as shown as the Fig. 6-4. The formed NAO-SiO₂ film of the memory device is about 4nm and the CoSi₂ NC are about 6.5nm, respectively. The use of the 700°C RTA is to promote the CoSi₂ NC to be aggregated. According to the reported literature, an adequate external energy provided by the thermal system can induce the aggregation of the deposited CoSi₂ thin film [6.14]. The total energy of the thin film is reduced when the surface area is minimized by forming a discrete and roughly spherical NC structure. Moreover, XPS analyses were used to confirm the CoSi₂ NC aggregation. The chemical composition of the charge-trapping layer is demonstrated in the Fig. 6-5 (a) and (b). It can be found that the main peak of 778.5eV in the Co 2p_{3/2} XPS spectrum corresponded to binding energy of CoSi₂ phase confirm the charge storage centers are mainly composed of CoSi₂ NC. The Co-Si signal also can be found in the Si 2p XPS of the trapping layer as shown as the Fig. 6-5 (b). Energy dispersive spectrometer (EDS) has also been used to analyze the compositions of the NAO-SiO₂ and NC as shown as Fig. 6-5 (c) and (d), respectively. In the Fig. 6-5 (c), the EDS of the NC region is composed of strong Co and Si signals attributed with the self-assembled CoSi₂ NC. In addition, only the Si and O elements can be found in the EDS results of the tunneling oxide reveals that the NAO-SiO₂ have enough quality to restrain the Co

elements of charge trapping layer to diffuse into the Si-substrate even after 700°C thermal annealing process as shown as Fig. 6-5 (d). We also used the secondary ion mass spectrometer (SIMS) to study the possibility of Co contamination further. Fig. 6-6 is the results of SIMS analysis for the CoSi₂ NC memory device. It can be found that the main Co signal only accumulated at the tunneling oxide. Hence, it is believed that the Co contamination issue of the CoSi₂ memory device using the NAO-SiO₂ thin film as tunneling oxide can be excluded.

Fig. 6-7 (a) shows the high-frequency (1MHz) C-V curves of the formed CoSi₂ NC memory structure. While the gate voltage of the device was swept by $\pm 10V$ operation, a 7V of ΔV_{FB} can be observed. The counterclockwise of C-V hysteresis loops means the injected carrier is related to the inversion layer of the Si substrate. The obvious memory window of the NC memory devices is advantageous to be the judgment of the logic circuit. In addition, the J-V characteristic of MOIOS structure was also investigated as shown as the Fig. 6-7 (b). Compared with the J-V result of MIS structure in the Fig. 6-2 (b), it can be found the MOIOS structure shows a lower leakage characteristic and symmetric behavior. The result is attributed with that the gate current of the MOIOS structure is determined by the blocking oxide, which restrains the passing electron in both the positive or negative gate voltage mode.

To study the reliability characteristics of the formed CoSi₂ NC memory device,

retention and endurance characteristics have also been demonstrated. The retention characteristic of MOIOS structure was extracted by the capacitance-time (C-t) measurement as shown as the Fig. 6-8 (a). The normalized capacitance, ΔC_{ret} is defined as equation [1]:

$$\Delta C_{ret} = \{ C(t) - C_{FB} \} / \{ C(0) - C_{FB} \} \quad [1]$$

, where $C(0)$, $C(t)$ and C_{FB} of the equation [1] are the initial capacitance after the programming operation, the measured capacitance during the retention test and the referred capacitance at flat-band voltage, respectively [6.15]. The ΔC_{ret} of the memory device can be stable as about 48% of the initial capacitance after 10^4 sec test even if a obvious 20% capacitance drop within the first 100sec. In addition, we also demonstrated the endurance characteristic of the MOIOS structure as shown as Fig. 6-8 (b). The endurance characteristic of the device by the continuous voltage pulse set at $\pm 10V$ for 1msec. After the continuous stress, a followed C-V measurement was used to examine the degeneration of the memory charge-storage ability. A slight decay of the memory window is found even after 10^6 cycles of pulse operations. The retention and endurance tests confirm the memory using the NAO-SiO₂ as tunneling oxide has an enough quality.

6.1.4 Conclusion

In conclusion, nitric acid oxidation method was studied to prepare a thin oxide as

the gate oxide of the electrical device. It is found the Si film can be oxidized completely by the TEM and XPS results. Also, the process of the nitric acid oxidation and the effect of the POA have also been demonstrated. The oxide quality can be improved as the sub-oxide element is decreased during the POA process. In addition, the CoSi_2 NC has also been formed as the charge storage centers to study the feasibility for the NAO- SiO_2 to apply into the memory device. The NAO- SiO_2 can bring a memory window of 7V under $\pm 10\text{V}$ gate voltage sweeps. The retention and endurance tests of the formed CoSi_2 NC memory device has also been demonstrated in this work. From the reported data, it is believed that that the NAO- SiO_2 film can provide an adequate quality and hold the stored charge during the reliability tests. Moreover, the nitric acid oxidation is easy and advantageous to improve the thermal budget issue for the current NC memory devices because the higher fabrication temperature for the improved NVM devices is only determined by the NC.

6.2 ZrO_2 formed by nitric acid oxidation as the tunneling oxide of cobalt-silicide nanocrystal nonvolatile memory device

6.2.1 Introduction

In this section, the nitric acid solution ($\text{HNO}_3:\text{H}_2\text{O}= 1:10$) was used to oxidize a sputtered Zr film. After the immersion, X-ray photoelectron spectroscopy has been used to confirm that the deposited Zr can be oxidized completely after the oxidation

process. The quality of the formed ZrO_2 was also analyzed by the capacitance-voltage and current density-voltage measurements. In addition, the $CoSi_2$ NC memory using the ZrO_2 as the tunneling oxide has been fabricated. After the device formation, the followed TEM and EDS have been used to observe the formation and composition of the NC. The retention and endurance tests have been used to confirm that the ZrO_2 can prevent the stored charge from losing.

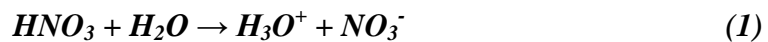
6.2.2 Experiment

An about 2-nm-thick pure Zr film was deposited on the p-type (100) Si wafer which had been removed the native oxide and particles by RCA process by the sputtering system. The deposited Zr film was immersed in nitric acid solution ($HNO_3:H_2O= 1:10$) for 60 sec at room temperature. After the nitric acid oxidation, a followed RTA process was used to improve the ZrO_2 quality. The MIS structure has also been formed to study the quality of the ZrO_2 film. To study the feasibility to apply the nitric acid oxidized Zr as the NC tunneling oxide, an about 6-nm-thick $CoSi_2$ film was deposited on the ZrO_2 film as the self-assembled layer. In the sputtering process, the DC power and process pressure were set at about 50 W and 7.6mTorr to yield a deposition rate of 0.01nm/s. Subsequently, a RTA set at $700^\circ C$ was performed in N_2 ambient for 30sec to enhance the $CoSi_2$ thin film to aggregate and improve the quality of the ZrO_2 film. After the RTA process, a 50-nm-thick

blocking oxide (SiO₂) was capped by plasma enhanced chemical vapor deposition system. Finally, Al electrode was patterned to form the MOIOS structure. After the fabricating of the NC memory device, TEM and XPS analyses were used to study the compositions of the ZrO₂ and CoSi₂ NC. Furthermore, the electrical measurements such as C-V, J-V, retention and endurance measurements were used to investigate the charge-storage ability of the formed NVM device.

6.2.3 Results and discussion

Fig. 6-9 (a) and (b) shows the XPS and oxidation process of the ZrO₂ in the MIS structure. It can be found an obvious peak of the Zr-O binding energy at about 183eV and no pure Zr signal at about 179eV in the result of Zr 3d XPS analysis [6.16]. The results can confirm that the sputtered Zr film was oxidized completely. By the results, the detailed oxidation process has been proposed. The process of nitric acid oxidation is depended on that the nitric acid can be decomposed completely in aqueous solution according to the followed chemical equation (1) [6.17]:



The decomposition of HNO₃ as powerful oxidizing agent can provide a high concentration of atomic oxygen to oxidize the immersed metal layer. Therefore, the Zr thin film can be effectively oxidized after the brief nitric acid immersion. The followed annealing process can improve the oxide quality after the immersion further.

In addition, the thickness of ZrO₂ tunneling oxide can be controlled by the thickness of the as-deposited Zr layer. With the increase of the ZrO₂ thickness during the immersion, the oxidation rate tends to decay and become slow. Finally, the thickness of the nitric acid oxidized film reaches the maximum of the oxidation.

Fig. 6-10 (a) and (b) is the C-V and J-V results of the MIS structure. It is found the ZrO₂ formed by the nitric acid oxidation shows an unobvious hysteresis phenomenon in the Fig. 6-10 (a). The result indicates a negligible oxide charges existed in the ZrO₂ film even the oxide was formed by the brief nitric acid immersion and RTA process. In addition, we also tried to extract the interface characteristic by the conductance method [6.18]. The interface trap density of the nitric acid oxidized ZrO₂ is about $7.27 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2}$, which is acceptable for the current electrical device. In the J-V characteristic, the formed ZrO₂ film before and after the annealing process was compared as shown as Fig. 6-10 (b). It can be found that the gate current density of the ZrO₂ after the RTA process is about one order of magnitude smaller than the sample without RTA treatment. The results confirm that the followed annealing treatment can bring an additional improvement of the oxide quality. The improved gate current is attributed with the traps in the ZrO₂ and Si/ZrO₂ interface was reduced by the RTA process further.

To study the feasibility for applying the nitric acid oxidation process into the

tunneling oxide of memory devices, the CoSi_2 NC have been formed as the charge-trapping centers. Fig. 6-11 shows the C-V and J-V measurements for the CoSi_2 NC memory device. The bidirectional C-V sweeps were performed from deep inversion to deep accumulation and in reverse, which exhibited a ΔV_{FB} , indicating charge-storage ability of the NC. In Fig. 6-11 (a), it is found that the CoSi_2 NC memory device shows an excellent memory window of 10V under $\pm 10\text{V}$ gate voltage operation. The result also shows that the formed ZrO_2 can hold the charge in the NC instead to lose into the Si-substrate. The excellent charge-storage ability is enough to provide a judgment for the logic circuit design. In addition, the J-V result of the MOIOS structure as shown as the Fig. 6-11 (b) indicates the nitric acid oxidized ZrO_2 without serious leakage current ($\sim 10^{-7}\text{A}/\text{cm}^2$ at $V_G=10\text{V}$) is potential for the application of the memory tunneling oxide.

Fig. 6-12 (a) and (b) exhibit the retention measurement and the endurance characteristics of the CoSi_2 NC memory device, respectively. The retention test was by operating a $\pm 10\text{V}$ gate voltage stress for 10sec and measured up to 10^4sec at 60°C . It is found that retention result of the device has obvious memory window decay in the first 10sec. The decay is attributed with the stored charge in the shallow trap is unsteady and is easier to tunnel back to the substrate due to the coulomb repulsion and shallow trapping. The Coulomb repulsion of the several electrons stored in one NC

may provide a larger energy raise and causes the charge to lose easily. In addition, some charges may be stored in the shallow traps provided by the interface between the NC, surrounding oxide and tunneling oxide. The shallow trapping mechanism is believed to cause serious memory window decay during the initial retention test. After the fast degeneration of memory window at the first 10sec, the formed memory device tends to maintain its charge-storage ability. The device can keep an about 2V memory window after 10^4 sec in the retention test. In the Fig. 6-12 (b), the endurance characteristic of the device was extracted by the continuous voltage pulse set at $\pm 10V$ for 1msec. It is found that only slight memory window is degraded after a 10^6 write/erase cycles operation. The measurements show that the NC memory has an enough reliability characteristics for the memory device application.

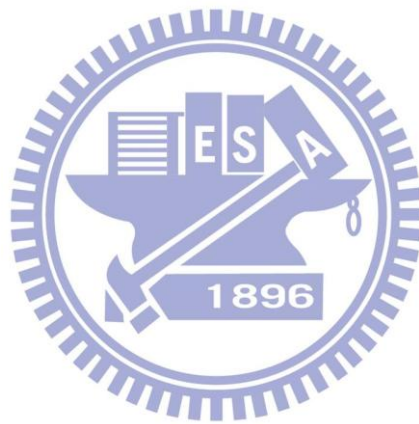
To assure to formation and composition of the NC, more material analyses have been used. Fig. 6-13 (a) is the cross-section and plane-view TEM images of the formed CoSi_2 NC memory device. It is found the ZrO_2 formation and CoSi_2 NC aggregation obviously. The thickness of the formed ZrO_2 film, the size and density the CoSi_2 NC are about 4~5nm, 5-6nm and $4.7 \times 10^{11} \text{cm}^{-2}$, respectively. In addition, AES analysis has also been proposed to eliminate the issue of Co contaminants as shown as the Fig. 6-13 (b). In the Fig. 6-13 (b), it is found that the Co and Zr show an un-obvious diffusion behavior. Therefore, we believed that the formed ZrO_2 can

restrain the Co diffusion even after an annealing process. The composition of the NC is confirmed by the Co 3d XPS in the Fig. 6-14 (a), which is extracted by analyzing the charge-trapping layer. The appearance of peak at 778.3eV fits in with the CoSi₂ phase of the reported literature [6.19]. In addition, an energy-dispersive spectrometer (EDS) analysis of the NC can be the additional tool for the composition of the NC as shown as the Fig. 6-14 (b). During the EDS analysis, the electron beam was tried to focus at the NC region. The EDS result can support the XPS results because that the NC composed with Co and Si elements obviously. The formation of NC is based on the self-assembled system that the deposited CoSi₂ thin film tends to aggregate and form NC structure to minimize the surface energy and relax the interface stress when enough energy was provided by the RTA system. Then, the CoSi₂ NC can attribute the charge-storage sites for the memory application.

6.2.4 Conclusion

In conclusion, a ZrO₂ film formed by the nitric acid oxidation is proposed to be the tunneling oxide for the CoSi₂ NC memory device. Material and electrical results were used to assure the Zr thin film can be oxidized completely after immersing in the nitric acid solution. The result also indicates the followed annealing process can improve the oxide quality further. In addition, the detailed oxidation process of the nitric acid solution has also been proposed in this work. By the fabricating the

MOIOS structure, the formed CoSi_2 NC memory reveals an obvious memory effect and good reliability characteristics. The ZrO_2 film formed by nitric acid oxidation is advantageous to improve the thermal budget issue of the thermal oxide demand of the conventional NC memory devices. Moreover, the nitric acid oxidation method with the cost-effective and easy property to form the tunneling oxide is potential to form the tunneling oxide of the current NVM devices.



Process flow

- (1) (100) P-type Si wafer with modified RCA clean
- (2) 2-nm-thick Si (~2nm) deposited by sputtering system
- (3) Immersion in the nitric acid solution ($\text{HNO}_3:\text{H}_2\text{O}=1:10$) to form the SiO_2 layer as a device tunneling oxide.
- (4) 6-nm-thick CoSi_2 film was deposited by the sputtering system to be the self-assembled trapping layer
- (5) RTA in N_2 ambient to form NCs structure
- (6) Blocking oxide (50nm) deposited by PECVD
- (7) Top and bottom Al electrode pattern

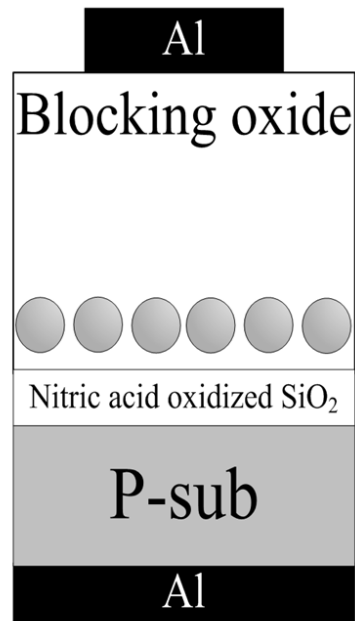


Fig. 6-1 The process flow proposed in this work.

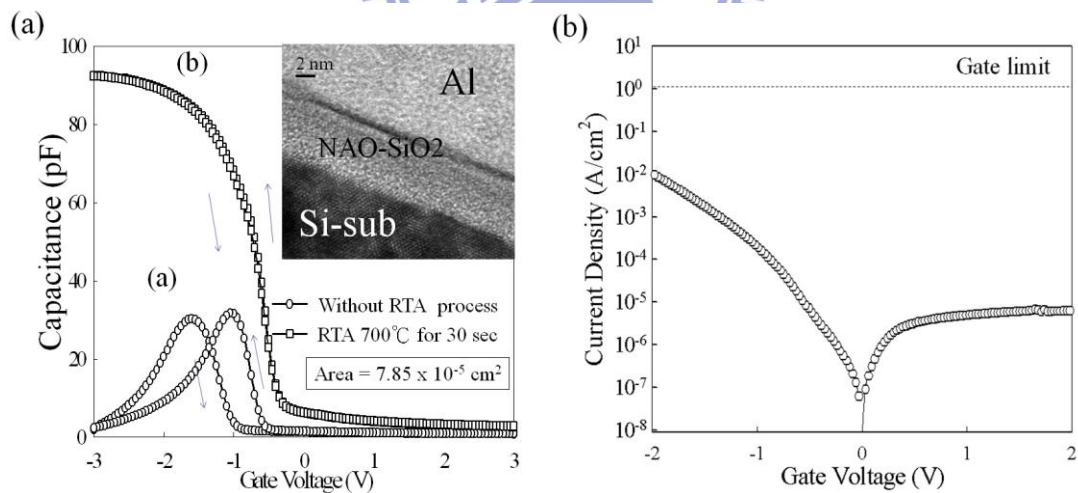


Fig. 6-2 The (a) C-V and (b) J-V characteristics of MIS structure using the NAO-SiO_2 layer as the gate oxide. The inset-of 6-2 (a) is the cross-section TEM image of the MIS structure.

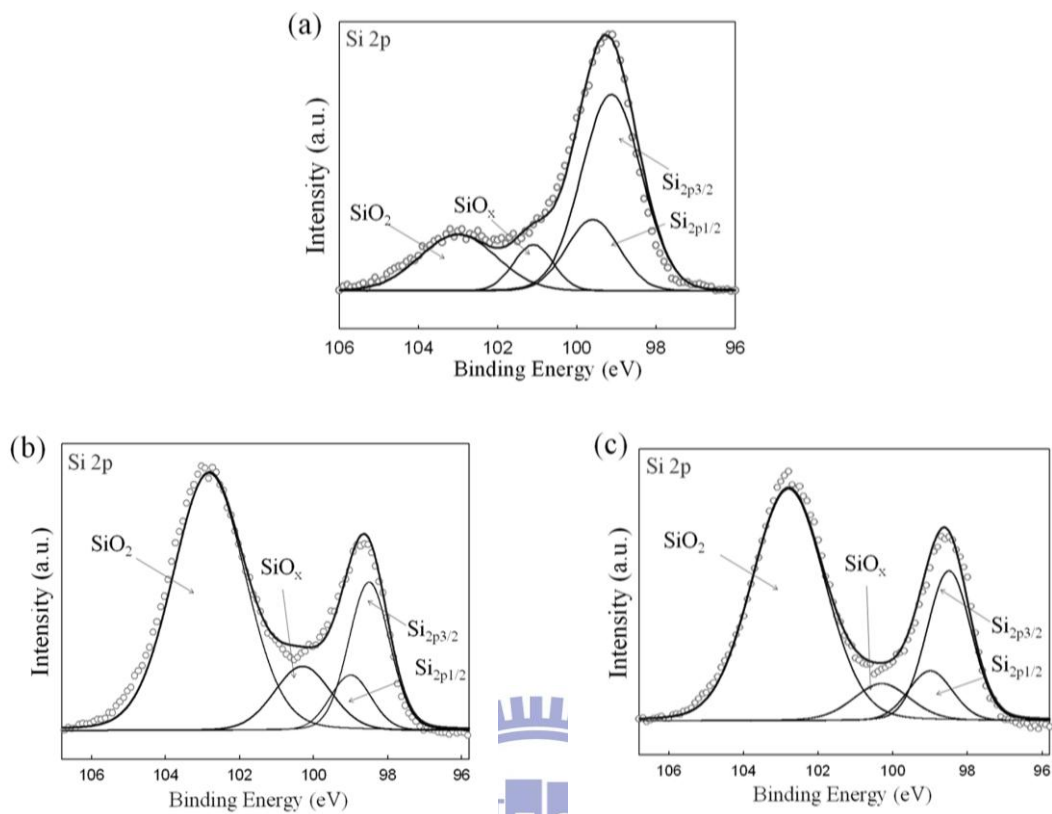


Fig. 6-3 The Si 2p XPS spectra of (a) the as-deposited Si film, the NAO-SiO₂ (b) before and (c) after the RTA set at 700°C for 30 sec, respectively.

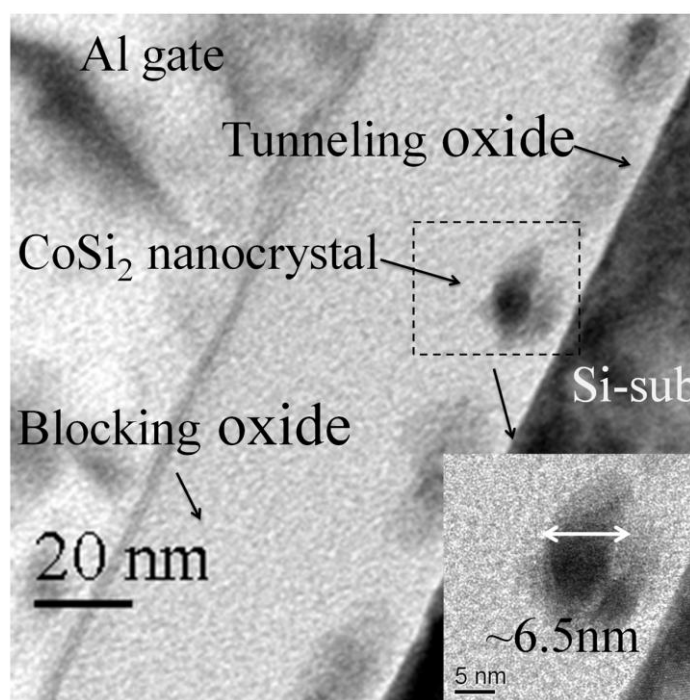


Fig. 6-4 The cross-section TEM image of the formed memory structure using the NAO-SiO₂ as device tunneling oxide.

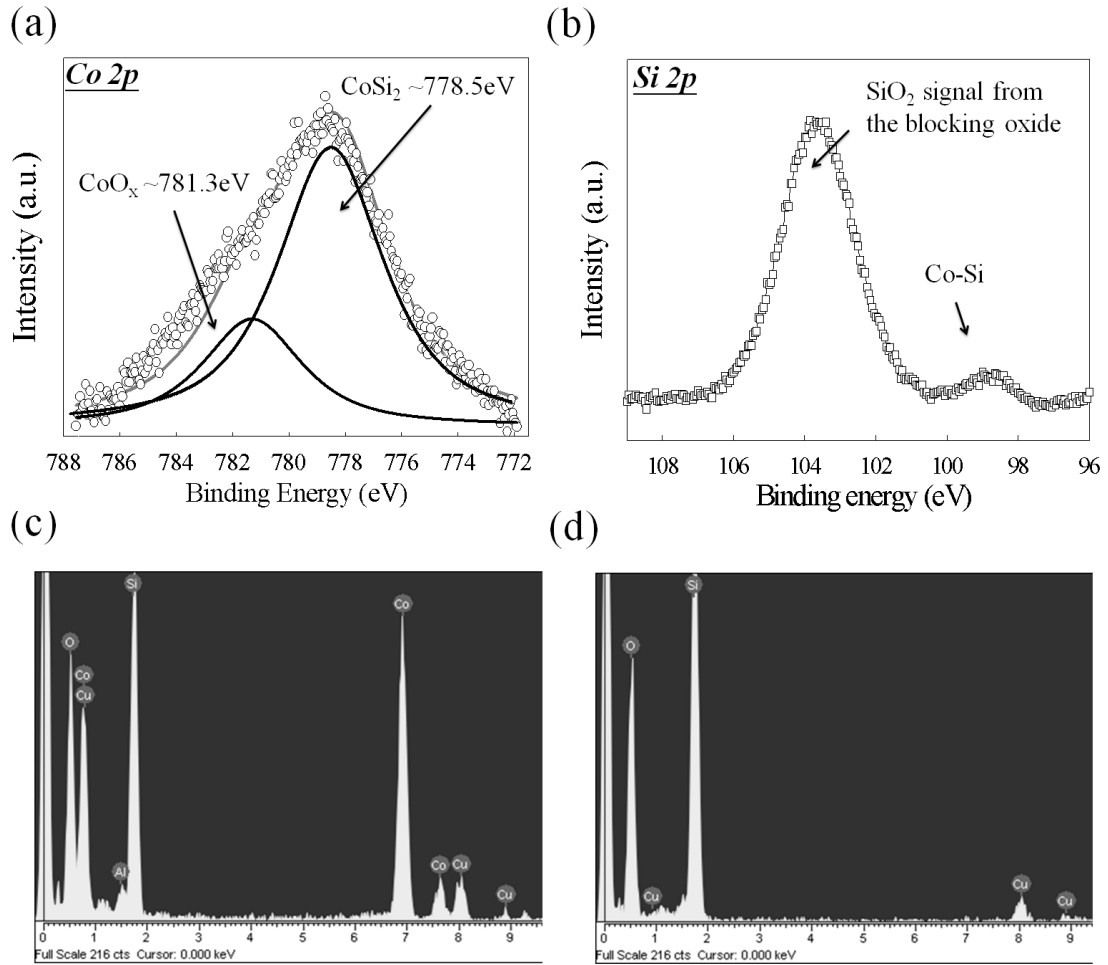


Fig. 6-5 (a&b) The Co 2p_{3/2} and Si 2p XPS spectrum of the charge-trapping layer after the RTA at 700°C for 30sec. (c&d) The EDS analyses of the compositions of the NAO-SiO₂ and NC.

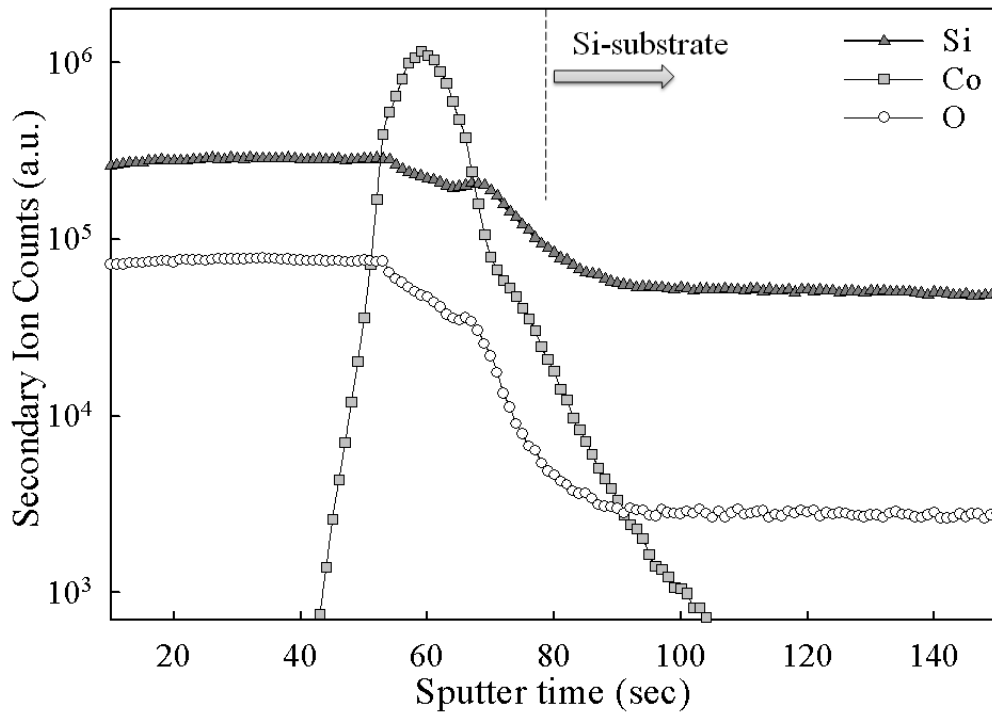


Fig. 6-6 The SIMS analysis of the CoSi_2 NC memory device.

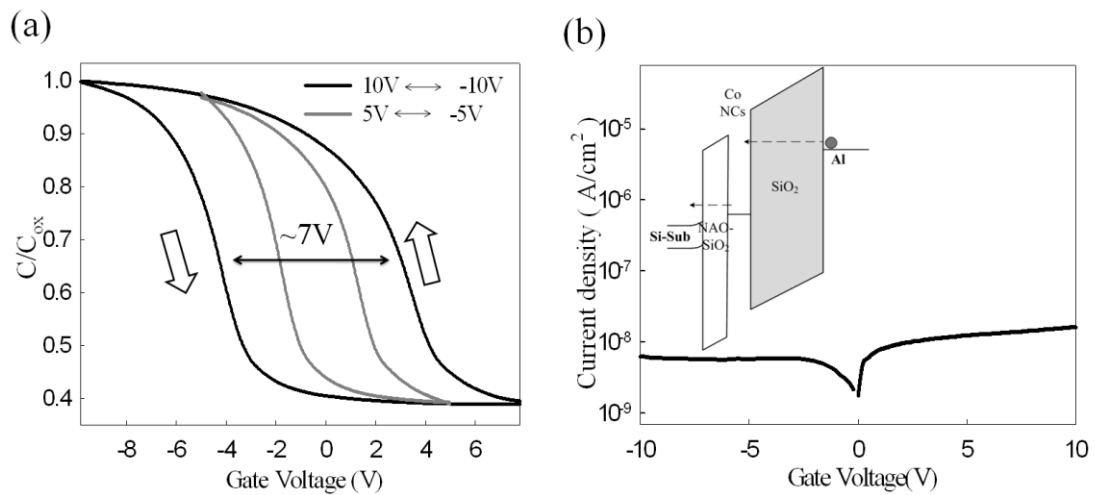


Fig. 6-7 The (a) C-V and (b) J-V curve of the MOIOS structure using the NAO-SiO₂ as device tunneling oxide.

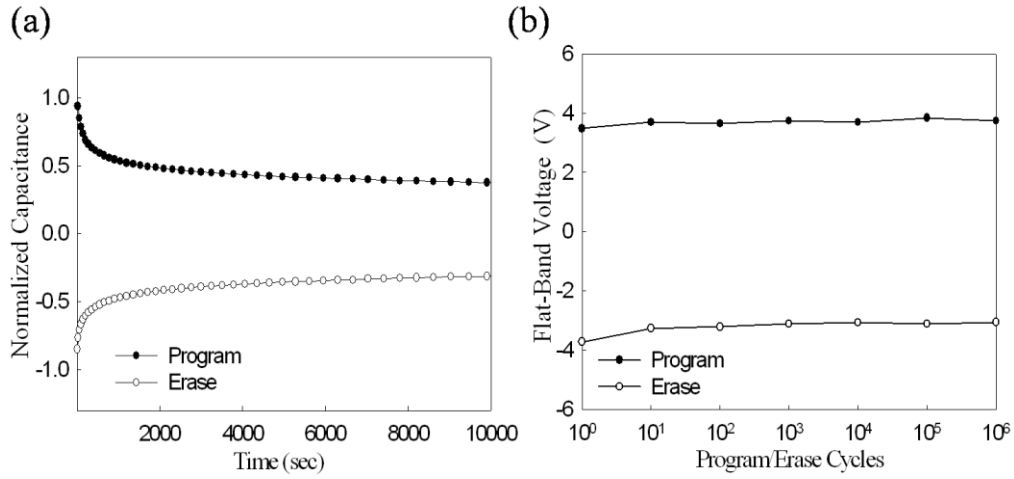


Fig. 6-8 The (a) retention and (b) endurance characteristics of the MOIOS structure using the NAO-SiO₂ as tunneling oxide.

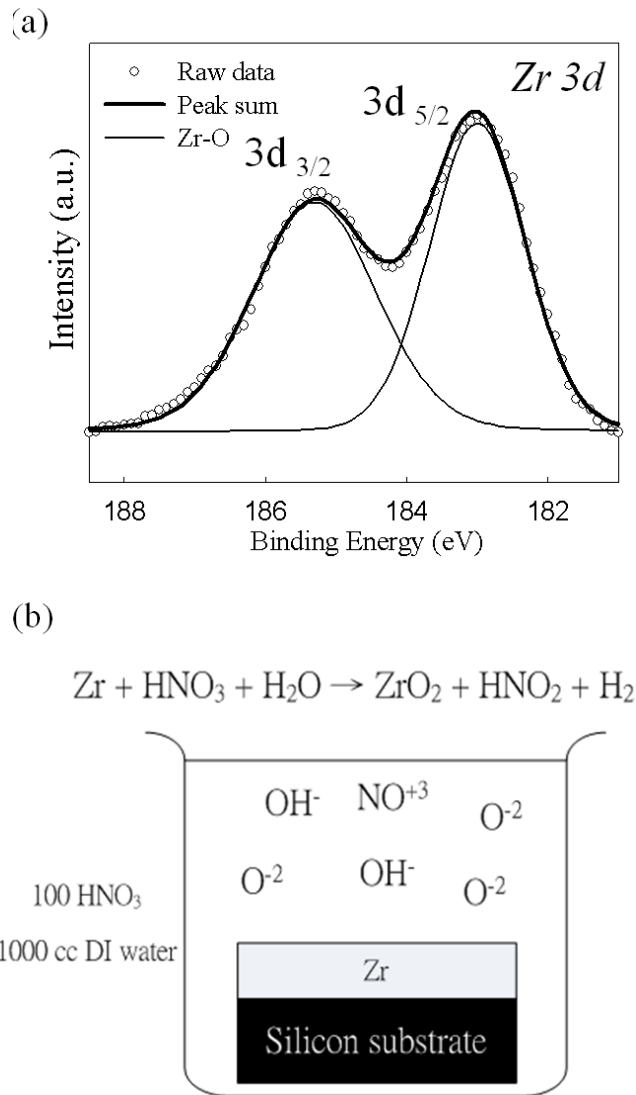


Fig. 6-9 The XPS and oxidation process of the ZrO₂ film.

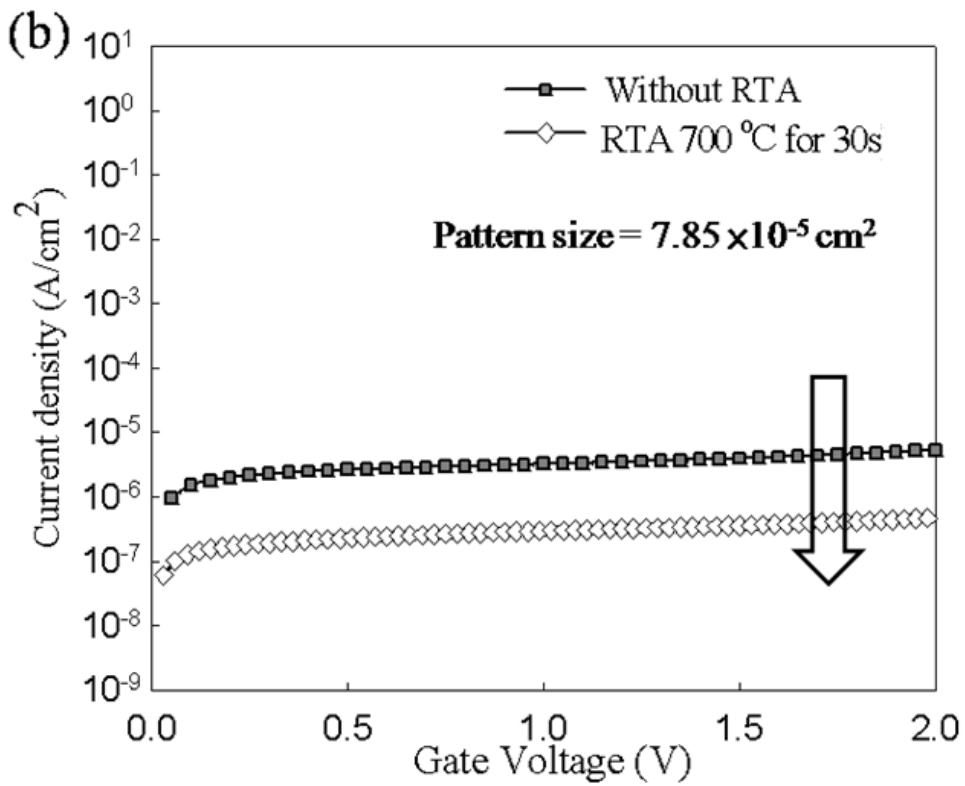
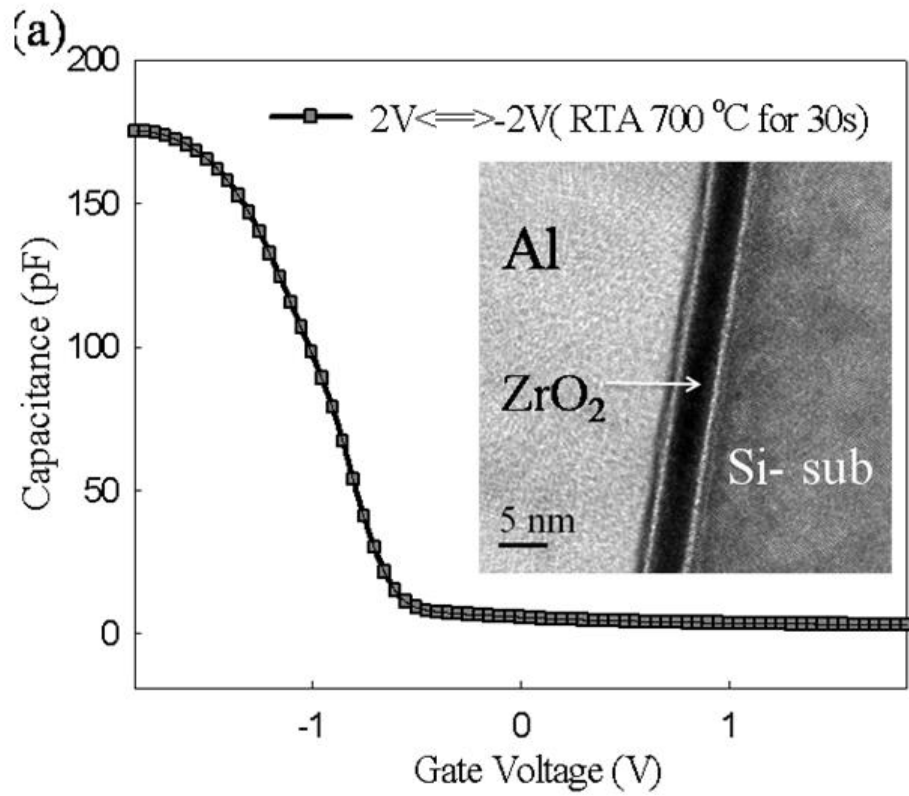


Fig. 6-10 The (a) C-V and (b) J-V results of the MIS structure.

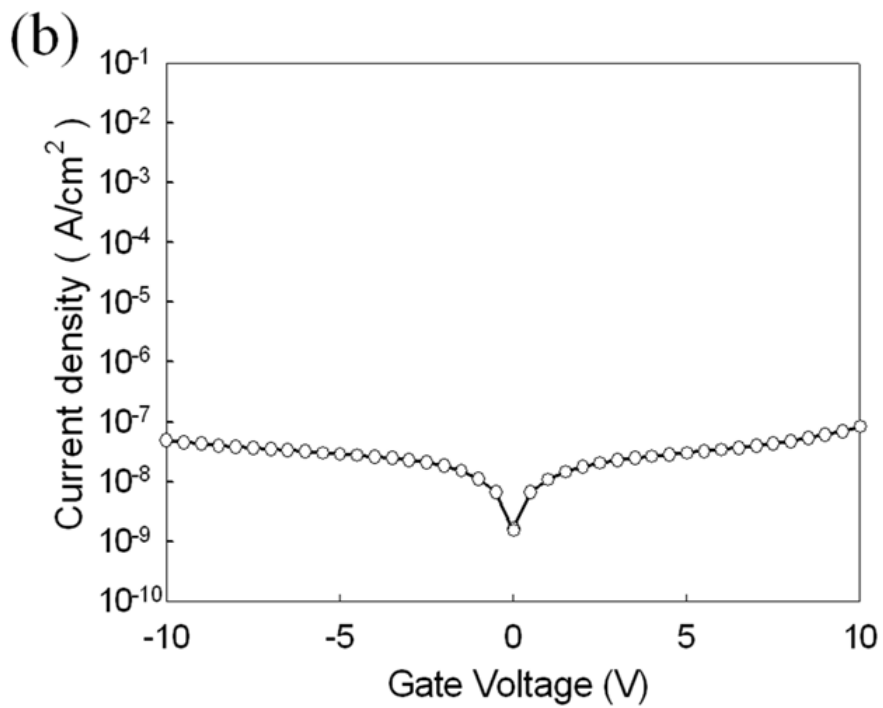
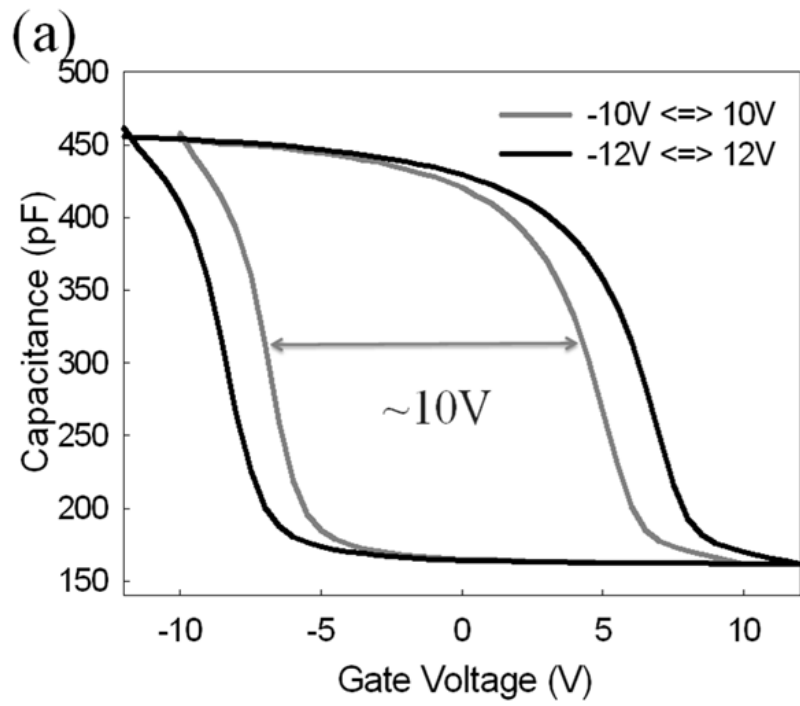


Fig. 6-11 Memory effect obtained from C-V characterization and (b) current density measurement of the formed CoSi₂ NC memory device.

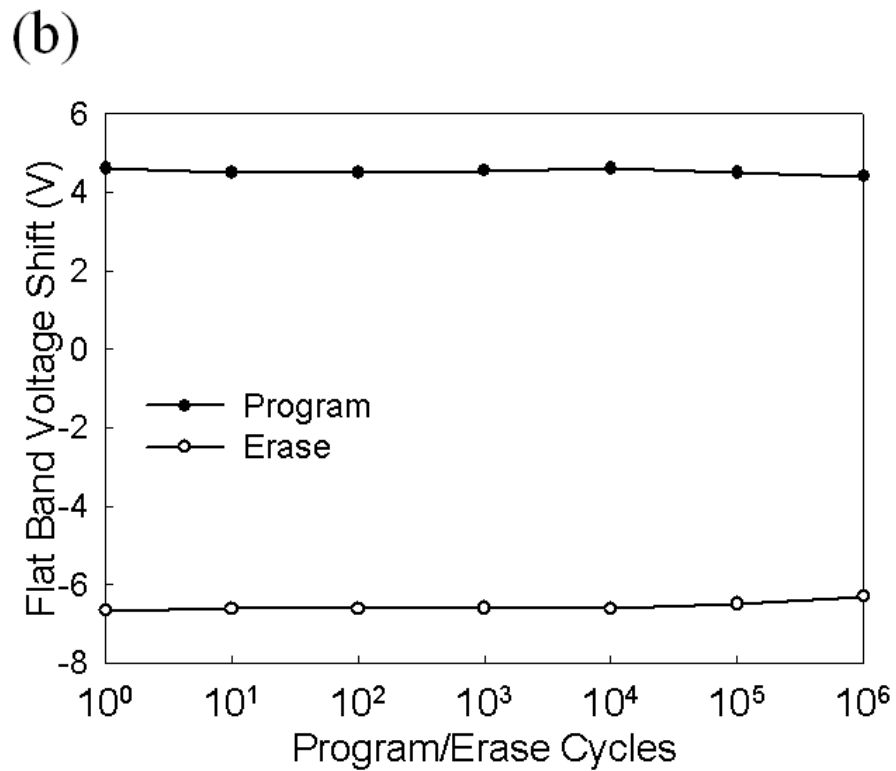
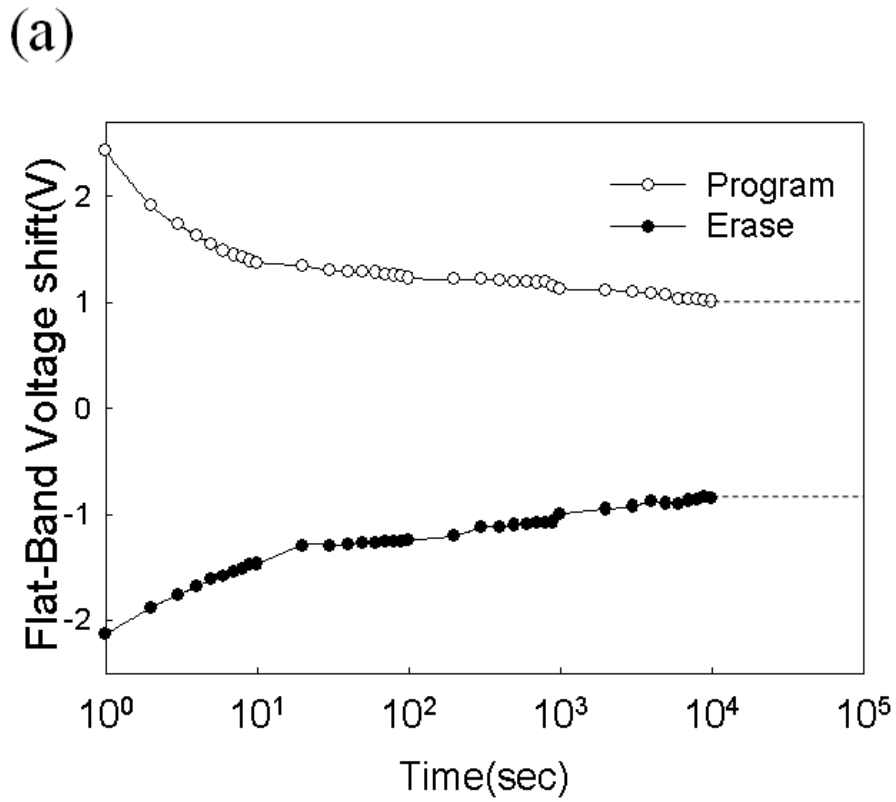


Fig. 6-12 The (a) retention and (b) endurance characteristics of the formed CoSi_2 NC memory device.

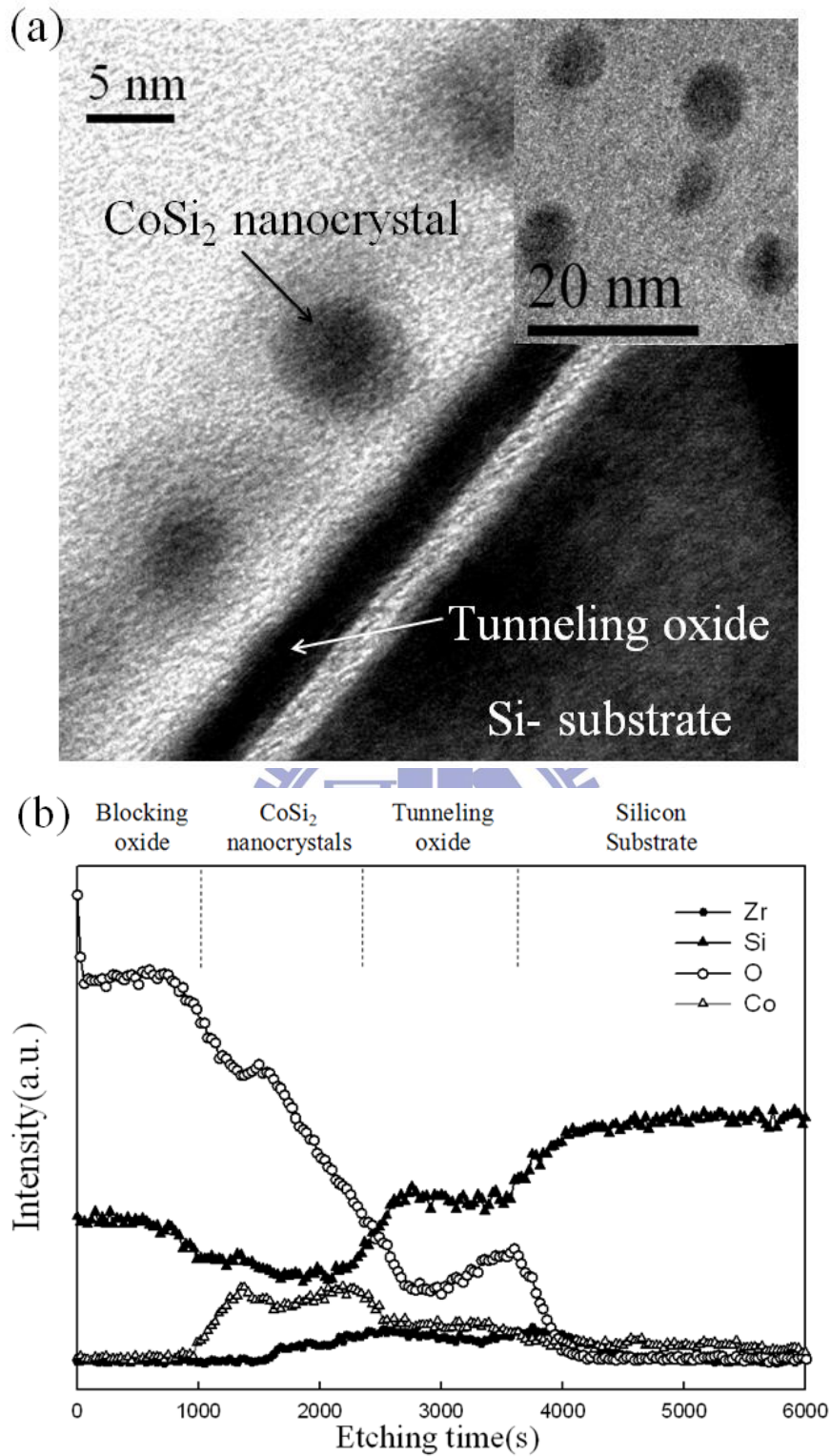


Fig. 6-13 The (a) TEM and (b) AES analyses of the CoSi₂ NC memory device using the nitric acid oxidized ZrO₂ as the tunneling oxide.

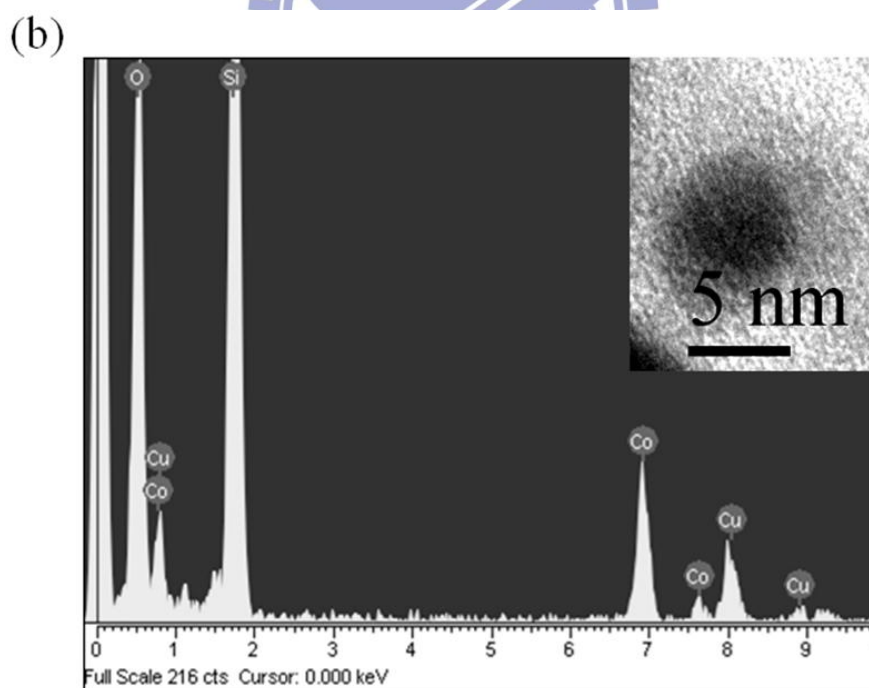
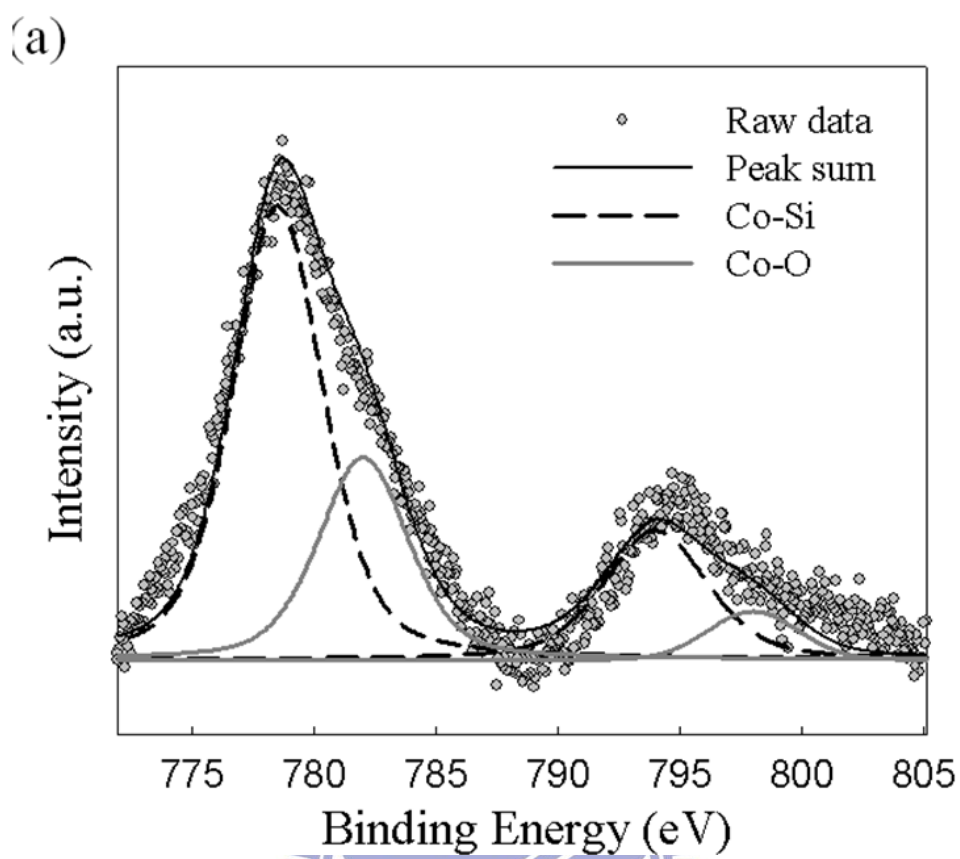


Fig. 6-14 The (a) XPS and (b) EDS analyses of the NC.

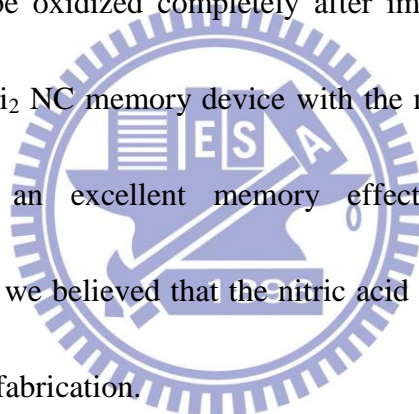
Chapter 7

Conclusion Remarks

In the thesis, we have studied the NC formation by the self-assembled method, the selective oxidation and the co-evaporation. In chapter 3, the co-evaporating method can fabricate double- and single-layer Ni NC structure by controlling the temperature of RTA process. After a 700°C annealing process, we have found that the NC is distributed randomly. A double layer NC structure can be formed by only one deposition and one annealing. The Ni NC embedded in Si₃N₄ layer shows an excellent 6V of memory window in C-V measurement. The NC memory device can keep 47 % of memory window in the 10⁴ retention test. Even if the samples becomes a single layer after 800°C annealing process, the devices still shows a extra high density of 4.5×10¹² cm⁻². In addition, the co-evaporation also can be used to fabricate the NC embedded in High-K dielectric easily by changing the evaporated pellet. In chapter 4, a reactive sputtering method is used to form the Co NC. A CoSi₂ thin film was deposited by incorporating oxygen element to form reactive-sputtering process. Therefore, the deposited CoSi₂ thin film is oxygen-doped or partially oxidized. A subsequent annealing is used to promote the added oxygen to oxidize the silicon element of the silicide. The purpose of the reactive sputtering process is to avoid over-oxidation, which may reduce the charge storage ability of the NC memory

device. The memory window of the Co NC memory device formed at 5sccm of O₂ flow rate is about 7V under $\pm 15V$ operation. The size and density of NC formed by 700°C annealing condition is about 6nm and $3.2 \times 10^{12} \text{ cm}^{-2}$, respectively. In addition, we have found the NC formation depends strongly on the oxygen flow rate and the annealing temperature strongly. The NC memory device only shows a 1.3V of memory window in the 7sccm- sample. As the oxygen flow rate increases, failure of selective oxidation causes an over-oxidation of the deposited CoSi₂ film. In chapter 5, the addition of Ge elements in the NiSi₂ system is confirmed to affect the NiSi₂ NC formation. The result has also been compared with the pure NiSi₂ NC. the Ge-incorporated NiSi₂ thin film shows a better size distribution (~8-9nm) even at lower annealing temperature. By incorporating Ge elements, a larger memory (~9V) window can be obtained in the C-V measurement. The reason for the improved formation is because of the added Ge which can enhance the silicide to crystallize during the thermal annealing. Then, the deposited NiSi₂ can be aggregated at lower temperature. We also tried to discuss the effect of oxygen during the NC aggregation because the oxidation of the Ge elements is difficult to avoid. In addition, the oxidized Ge usually has many defects and brings more leakage paths to affect the performance of the memory device. From the experimental data, the memory window of RTO-sample shows 0.4 V larger than the RTA-one. The oxidized Ge can provide an

additional memory window for the memory device. However, the device with more oxidized Ge only keep a ~ 39% of memory window in the 10^4 retention test. By the material analyses, it is confirmed that the oxidized Ge aggregated at the interface between the tunneling oxide and the charge-trapping layer. The oxidized Ge may enhance the stored charge to loss in the retention test. In chapter 6, nitric acid oxidation is used to fabricate the tunneling oxide to lower the thermal budget of the NC memory device. The XPS result confirms that the deposited metal or semiconductor film can be oxidized completely after immersing in the nitric acid solution. The formed CoSi_2 NC memory device with the nitric acid oxidized film as tunneling oxide shows an excellent memory effect ($\sim 10\text{V}$) and reliability characteristics. Therefore, we believed that the nitric acid oxidation is useful method in advanced NVM device fabrication.



Chapter 7

Future work

In the thesis, we have studied several NC formation processes. The co-evaporation can be used to fabricate the metal NC embedded in the High-K materials such as the HfO_2 , Al_2O_3 and HfAlO . The High-K dielectrics layer using as NC surrounded oxide can improve the write/erase speed and retention characteristic by increasing the gate voltage drop on the tunneling oxide and reducing the electrical field at the interface between the NC and tunneling oxide. However, the study of the aggregation of NC in the High-K system is still not clear. In addition, it is worthy to study for the effects of the other gas in the reactive-sputtering process such as N_2 or NH_3 ambient. For example, the NH_3 may bring a passivation for surround NC oxide or oxide interface, which can enhance the reliability characteristic of the NC memory device. In NiSiGe system, a detailed analysis is critical to describe the electrical characteristic of the NiSiGe NC memory device. The energy-band diagram for the NiSiGe NC can be established by XPS measurement or optical analysis. In the nitric acid oxidation, more materials and more detailed parameters during the oxidation need to be studied further.

References

Chapter 1:

- [1.1] D. Kahng and S. M. Sze, "A floating-gate and its application to memory devices", Bell Syst. Tech. J. 46, 1288 (1967).
- [1.2] F. Masuoka, M. Momodomi, Y. Iwata, R. Shirota, "New ultra high density EPROM and Flash EEPROM with NAND structure cell", IEEE IEDM Tech. Dig. 552 (1987).
- [1.3] R. Bez, E. Camerlenghi, A. Modelli, A. Visconti, "Introduction to flash memory". Proc. of IEEE, 91, 489 (2003).
- [1.4] "International Technology Roadmap for Semiconductors, 2009 update" at <http://www.itrs.net/Links/2009ITRS/Home2009.htm>
- [1.5] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash memory cells—An overview". Proc. of IEEE, 85, 1248 (1997).
- [1.6] H. A. R. Wegener, A. J. Lincoln, H. C. Pao, M. R. O'Connell and R. E. Oleksiak, "The variable threshold transistor, a new electrically alterable, non-destructive read-only storage device", IEEE IEDM Tech. Dig., (1967).
- [1.7] M.H. White, Y. Yang; A. Purwar; M.L French, "A low voltage SONOS nonvolatile semiconductor memory technology". IEEE Transactions on components, packing, and manufacturing technology, 20, 190 (1997).
- [1.8] V. A. Gritsenko, K.A. Nasyrov, Yu. N. Novikov, A. L. Aseev, S. Y. Yoon, J. W. Lee, E. H. Lee, C. W. Kim, "A new low voltage fast SONOS memory with high-k dielectric" Solid-State Electronics, 47, 1651 (2003).
- [1.9] K. H. Wu, H. C. Chien, C. C. Chan, T. S. Chen, and C. H. Kao, "SONOS device with tapered bandgap nitride layer", IEEE Trans. Electron Devices 52, 987 (2005).

- [1.10] X. Wang and K. D. Lee, "A novel high- κ SONOS memory using TaN/Al₂O₃/Ta₂O₅/HfO₂/Si structure for fast speed and long retention operation" IEEE Trans. Electron Devices 53, 78 (2006).
- [1.11] X. Wang, J. Liu, W. Bai, D. L. Kwong, "A novel MONOS-type nonvolatile memory using high- κ dielectrics for improved data retention and programming speed", IEEE Trans. Electron Devices, 51, 597 (2004).
- [1.12] P. Xuan, M. She, B. Harteneck, A. Liddle, J. Bokor, and T. J. King, "FinFET SONOS flash memory for embedded applications," in IEDM Tech. Dig., pp. 609, 2003.
- [1.13] Y. K. Lee, K. W. Song, J. W. Hyun, J. D. Lee, B. G. Park, S. T. Kang, J. D. Choe, S. Y. Han, J. N. Han, S. W. Lee, O. I. Kwon, C. Chung, D. Park, and K. Kim, "Twin SONOS Memory With 30-nm Storage Nodes Under a Merged Gate Fabricated With Inverted Sidewall and Damascene Process". IEEE Electron Device Lett., 25, 205, (2004).
- [1.14] S. D. Suk, K. H. Yeo, K. H. Cho, M. Li, Y. Y. Yeoh, K. H. Hong, S. H. Kim, Y. H. Koh, S. G. Jung, W. J. Jang, D. W. Kim, D. G. Park, and B. I. Ryu, "Gate-all-around twin silicon nanowire SONOS memory," in VLSI Symp. Tech. Dig , pp.142, 2007.
- [1.15] J. Fu, N. Singh, K. D. Buddharaju, S. H. G. Teo, C. Shen, Y. Jiang, C. X. Zhu, M. B. Yu, G. Q. Lo, N. Balasubramanian, D. L. Kwong, E. Gnani, and G. Baccarani, "Si-Nanowire Based Gate-All-Around Nonvolatile SONOS Memory Cell" IEEE Electron Device Lett., 29, 518, (2008).
- [1.16] D. B. Farmer¹ and R. G. Gordon, "High density Ru nanocrystal deposition for nonvolatile memory applications" J. Appl. Phys. 101, 124503 (2007).
- [1.17] X. B. Lu, P. F. Lee, and J. Y. Dai, "Synthesis and memory effect study of Ge nanocrystals embedded in LaAlO₃ high-k dielectrics" Appl. Phys. Lett., 86,

203111 (2005).

- [1.18] F. M. Yang, T. C. Chang, P. T. Liu, P. H. Yeh, U. S. Chen, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Lou, "Using double layer CoSi_2 nanocrystals to improve the memory effects of nonvolatile memory devices" *Appl. Phys. Lett.*, 90, 212108 (2007).
- [1.19] Y. S. Jang, J. H. Yoon, and R. G. Elliman, "Formation of nickel-based nanocrystal monolayers for nonvolatile memory applications" *Appl. Phys. Lett.*, 92, 253108 (2008).
- [1.20] J. Wang, L. Wu, K. Chen, L. Yu, X. Wang, J. Song, and X. Huang, "Charge storage in self-aligned doubly stacked Si nanocrystals in SiN_x dielectric" *J. Appl. Phys.* 101, 017325 (2007).
- [1.21] S. W. Ryu, J. W. Lee, J. W. Han, S. Kim, and Y. K. Choi, "Designed work-function engineering of double-stacked metal nanocrystals for nonvolatile memory application" *IEEE Trans. Electron Devices*, 56, 377 (2009).
- [1.22] F. M. Yang, T. C. Chang, P. T. Liu, P. H. Yeh, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Lou, "Memory characteristics of Co nanocrystal memory device with HfO_2 as blocking oxide", *Appl. Phys.* 90, 132102 (2007).
- [1.23] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal nanocrystal memories. I. Device design and fabrication". *IEEE Trans. Electron Devices*, 49, 1606 (2002).
- [1.24] P. H. Yeh, C. H. Yu, L. J. Chen, H. H. Wu, P. T. Liu, and T. C. Chang, "Low-power memory device with NiSi_2 nanocrystal embedded in silicon dioxide layer" *Appl. Phys. Lett.*, 90, 193504 (2005).
- [1.25] B. Li, J. Ren, and J. Liu, "Synthesis of high-density PtSi nanocrystal for memory application", *Appl. Phys. Lett.*, 96, 172104 (2010).

Chapter 2

- [2.1] C. Yuan and C. C. Yeh, Invited Talk for 15th International Conference on Ion Implantation Technology, (2004).
- [2.2] T. Ohnakado, H. Onoda, O. Sakamoto, K. Hayashi, N. Nishioka, H. Takada, K. Sugahara, N. Ajika and S. Satoh, "Device characteristics of 0.35 μm P-channel DINOR flash memory using band-to-band tunneling-induced hot electron (BBHE) programming". IEEE Trans. Electron Devices, 46, 1866, (1999).
- [2.3] J. Moll, Physics of Semiconductors. New York: McGraw-Hill, (1964)
- [2.4] M. Lezlinger and E. H. Snow, "Fowler-Nordheim tunneling into thermally grown SiO". J. Appl. Phys., 40, 278 (1969).
- [2.5] C. Hu, "Gate oxide scaling limits and projection". Invited paper in IEDM Tech. Dig. 1996.
- [2.6] Y. Okada, P. J. Tobin, K. G. Reid, R. I. Hegde, B. Maiti, and S. A. Ajuria, "Furnace grown gate oxynitride using nitric oxide (NO)" IEEE Trans. Electron Devices, 41, 1608, (1994).
- [2.7] S. W. Huang and J. G. Hwu, "Electrical characterization and process control of cost-effective high-k aluminum oxide gate dielectrics prepared by anodization followed by furnace annealing" IEEE Trans. Electron Devices, 50, 1658, (2003).
- [2.8] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-k/metal-gate stack and its MOSFET characteristics". IEEE Trans. Electron Devices, 25, 408, (2004).
- [2.9] E. P. Gusev, D. A. Buchanan, and E. Cartier et al., et al., "Ultrathin high-k gate stacks for advanced CMOS devices," in IEDM Tech. Dig. p.451, (2001).
- [2.10] C. C. Wang, J. Y. Tseng, T. B. Wu, L. J. Wu, C. S. Liang, and J. M. Wu, "Charging characteristics of Au nanocrystals embedded in metal - oxide-semiconductor structures" . J. Appl. Phys., 99, 026102 (2006).

- [2.11] C. Lee, J. Meter, V. Narayanan, E. C. Kan, "Self-assembly of metal nanocrystals on ultrathin oxide for nonvolatile memory applications". *Journal of Electronic Materials*, 34, 1 (2005).
- [2.12] S. Tam, P. K. Ko and C. Hu, " Lucky-electron model of channel hot-electron injection in MOSFET's" *IEEE Trans. Electron Devices*, 31, 1116, (1984).
- [2.13] A. T. Wu, T. Y. Chan, P. K. Ko and C.Hu, "A source-side injection erasable programmable read-only-memory (SI-EPROM) device" *IEEE Electron Device Lett.*, 7, 540, (1986).
- [2.14] H. Guan, D. Lee, G. P. Li, "An analytical model for optimization of programming efficiency and uniformity of split gate source-side injection Superflash memory". *IEEE Trans. Electron Devices*, 50, 809, (2003).
- [2.15] J. F. Van Houdt, G. Groeseneken, and H. E. Maes, "An analytical model for the optimization of source-side injection flash EEPROM devices". *IEEE Trans. Electron Devices*, 42, 1314, (1995).
- [2.16] M. T. Wu, H. T. Lue, K. Y. Hsieh, R. Liu, C. Y. Lu, "Study of the band-to-band tunneling hot-electron (BBHE) programming characteristics of p-channel bandgap-engineered SONOS (BE-SONOS)". *IEEE Trans. Electron Devices*, 54, 699, (2007).
- [2.17] M. She, T. J. King, C. Hu, W. Zhu, Z. Luo, J. P. Han and T. P. Ma, "JVD silicon nitride as tunnel dielectric in p-channel flash memory" *IEEE Electron Device Lett.*, 23, 91, (2002).
- [2.18] J. T. Park, J. Y. Chun, H. K. Kim, S. J. Jang and C. G. Yu, "New programming and erasing schemes for p-channel flash memory" *IEEE Electron Device Lett.*, 21, 491, (2000).
- [2.19] L. Sun, L. Pan, H. Pang, Y. Zeng, Z. Zhang, J. Chen and J. Zhu, "Characteristics of band-to-band tunneling hot hole injection for erasing

- operation in charge-trapping memory”. Jpn. J. Appl. Phys. 45, 3179, (2006).
- [2.20] M. Gh. Mohammad, K. K. Saluja, “Analysis and test procedures for NOR flash memory defects”. Microelectronics Reliability, 48, 698 (2008).
- [2.21] S. Yamada, T. Suzuki, E. Obi, M. Oshikiri, K. Naruke, and M. Wada, “A self-convergence erasing scheme for a simple stacked gate Flash EEPROM,” in IEDM Tech. Dig., p.307 (1991).
- [2.23] C.Y. Ng, T.P. Chen, M. Yang, J. B. Yang, L. Ding, C. M. Li, A. Du, A. Trigg, “Impact of programming mechanisms on the performance and reliability of nonvolatile memory devices based on Si nanocrystals” IEEE Trans. Electron Devices, 53, 663 (2006).
- [2.22] Y. M. Niquet, G. Allan, C. Delerue and M. Lannoo, “Quantum confinement in germanium nanocrystals” Appl. Phys. Lett., 77, 1182 (2000).
- [2.23] B. Delley and E. F. Steigmeier, “Quantum confinement in Si nanocrystals” Phys. Rev. B, 47, 1397, (1993).
- [2.24] J.D.Jackson, “Classical Electrodynamics”, published by John Wiley & Sons, (1999).

Chapter 3

- [3.1] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, “Introduction to flash memory”. Proc. of the IEEE, 91, 489 (2003).
- [3.2] S. Tiwari, F. Rana, K. Chan, H. Hanafi, C. Wei, and D. Buchanan, “Volatile and non-volatile memories in silicon with nanocrystal storage” Tech. Dig. - Int. Electron Devices Meeting. p. 521 1995.
- [3.3] Y. S. Jang, J. H. Yoon, and R. G. Elliman, “Formation of nickel-based nanocrystal monolayers for nonvolatile memory applications”. Appl. Phys. Lett., 92, 253108 (2008).
- [3.4] D. Panda, S. Maikap, A. Dhar, and S. K. Ray, “Memory characteristics of Nickel

- nanocrystals with high-k dielectric tunneling barriers” *Electrochem. Solid-State Lett.* 12(1), H7 (2009).
- [3.5] A. Miura, R. Tsukamoto, S. Yoshii, I. Yamashita, Y. Uraoka, and T. Fuyuki, “Non-volatile flash memory with discrete bionanodot floating gate assembled by protein template” *Nanotechnology*. 19, 255201 (2008).
- [3.6] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, “Metal nanocrystal memories. I. Device design and fabrication” *IEEE Trans. Electron Devices*, 49, 1606 (2002).
- [3.7] M. Yang, T. P. Chen, J. I. Wong, Y. Liu, L. Ding, K. Y. Liu, S. Zhang, W. L. Zhang, D. Gui and C. Y. Ng, “Influence of thermal annealing on charge storage behaviour of Ge nanoclusters synthesized with low-energy Ge ion implantation”. *J. Phys. D: Appl. Phys.* 42, 035109 (2009).
- [3.8] J. G. Zhu, C. W. White, J. D. Budai, S. P. Withrow, and Y. Chen, “Growth of Ge, Si, and SiGe nanocrystals in SiO₂ matrices”. *J. Appl. Phys.* 78, 4386 (1995).
- [3.9] W. K. Choi, V. Ho, V. Ng, Y. W. Ho, S. P. Ng, and W. K. Chim, “Germanium diffusion and nanocrystal formation in silicon oxide on silicon substrate under rapid thermal annealing”. *Appl. Phys. Lett.*, 86, 143114 (2005).
- [3.10] H. G. Chew, W. K. Choi, Y. L. Foo, F. Zheng, W. K. Chim, Z. J. Voon, K. C. Seow, E. A. Fitzgerald and D. M. Y. Lai, “Effect of germanium concentration and oxide diffusion barrier on the formation and distribution of germanium nanocrystals in silicon oxide matrix”. *Nanotechnology*, 17, 1964 (2006).
- [3.11] J. H. Yoon, G. H. Lee and R. G. Elliman, “Direct growth of nickel disilicide nanocrystals in silicon dioxide films”. *J. Appl. Phys.* 99, 116106 (2006).
- [3.12] P. Argyrakis, R. Cheung, “Plastic deformation magnetic assembly of out-of-plane structures using vapour phase hydrofluoric (HF) acid release”. *Microelectronic Engineering*, 86, 2176 (2009).

- [3.13] S. Duguay, J. J. Grob, A. Slaoui, Y. Le Gall, and M. Amann-Liess, “Structural and electrical properties of Ge nanocrystals embedded in SiO by ion implantation and annealing”. *J. Appl. Phys.* 97, 104330 (2005).
- [3.14] X. Xiang, X. T. Zu, J. W. Bao, S. Zhu and L. M. Wang, “Optical properties and structure characterization of sapphire after Ni ion implantation and annealing”. *J. Appl. Phys.* 98, 073524 (2005).
- [3.15] J. Dufourcq, S. Bodnar, G. Gay, D. Lafond, P. Mur, G. Molas, J. P. Nieto, L. Vandroux, L. Jodin, F. Gustavo, and Th. Baron, “High density platinum nanocrystals for non-volatile memory applications”. *Appl. Phys. Lett.* 92, 073102 (2008).
- [3.16] W. R. Chen, T. C. Chang, P. T. Liu, P. S. Lin, C. H. Tu and C. Y. Chang, “Formation of stacked Ni silicide nanocrystals for nonvolatile memory application”. *Appl. Phys. Lett.* 90, 112108 (2007).
- [3.17] M. Hocevar, P. Regreny, A. Descamps, D. Albertini, G. Saint-Girons, A. Souifi, and M. Gendry, “InAs nanocrystals on SiO / Si by molecular beam epitaxy for memory applications”. *Appl. Phys. Lett.* 91, 133114 (2007).
- [3.18] S. Maikap, T. Y. Wang, P. J. Tzeng, C. H. Lin, L. S. Lee, J. R. Yang and M. J. Tsai, “Charge storage characteristics of atomic layer deposited RuO nanocrystals”. *Appl. Phys. Lett.* 90, 253108 (2007).
- [3.19] S. Maikap, P. J. Tzeng, P. J. Tzeng, H. Y. Lee, C. C. Wang, T. C. Tien, L. S. Lee, and M. J. Tsai, “Physical and electrical characteristics of atomic layer deposited TiN nanocrystal memory capacitors” *Appl. Phys. Lett.* 91, 043114 (2007).
- [3.20] S. S. Yim, M. S. Lee, K. S. Kim and K. B. Kim, “Formation of Ru nanocrystals by plasma enhanced atomic layer deposition for nonvolatile memory applications” *Appl. Phys. Lett.* 89, 093115 (2006).

- [3.21] M. She and T. J. King, "Impact of crystal size and tunnel dielectric on semiconductor nanocrystal memory performance". IEEE Trans. Electron Devices 50, 1934 (2003).
- [3.22] P. F. Lee, X. B. Lu, J. Y. Dai, H. L. W. Chan, E. Jelenkovic and K. Y. Tong, "Memory effect and retention property of Ge nanocrystal embedded Hf-aluminate high-k gate dielectric" Nanotechnology 17, 1202 (2006).
- [3.23] J. von Borany, R. Grotzschel, K. H. Heinig, A. Markwitz, W. Matz, B. Schmidt and W. Skorupa, "Multimodal impurity redistribution and nanocluster formation in Ge implanted silicon dioxide films". Appl. Phys. Lett. 71, 3217 (1997).
- [3.24] U. Kaiser, D. A. Muller, J. L. Grazul, A. Chuvilin and M. Kawasaki, "Direct observation of defect-mediated cluster nucleation". Nature Materials. 1, 102 (2002)
- [3.25] W. K. Choi, V. Ng, S. P. Ng, H. H. Thio, Z. X. Shen and W. S. Li, "Raman characterization of germanium nanocrystals in amorphous silicon oxide films synthesized by rapid thermal annealing". J. Appl. Phys. 86, 1398 (1999).
- [3.26] J. J. Lee, Y. Harada, J. W. Pyun, and D.-L. Kwong, "Nickel nanocrystal formation on HfO₂ dielectric for nonvolatile memory device applications". Appl. Phys. Lett. 86, 103505 (2005).
- [3.27] C. Lee, T. H. Hou, and E. C. Kan, "Nonvolatile memory with a metal nanocrystal/nitride heterogeneous floating-gate". IEEE Trans. Electron Devices, 52, 2697 (2005)
- [3.28] J. K. Kim, H. J. Cheong, Y. Kim, J.-Y. Yi, H. J. Bark, S. H. Bang, and J. H. Cho, "Rapid-thermal-annealing effect on lateral charge loss in metal-oxide-semiconductor capacitors with Ge nanocrystals Appl. Phys. Lett., 82, 2527 (2003).

Chapter 4

- [4.1] D. Kahng and S. M. Sze, "A floating-gate and its application to memory devices". Bell Syst. Tech. J. 46, 1288 (1967).
- [4.2] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, Proc. "Flash memory cells-an overview". Proc. of IEEE, 85, 1248 (1997).
- [4.3] R. Bez, E. Camerlenghi, A. Modelli, A. Visconti, "Introduction to flash memory". Proc. IEEE, 91, 489 (2003).
- [4.4] S. Tiwari, F. Rana, K. Chan, H. Hanafi, C. Wei, and D. Buchanan, "Volatile and non-volatile memories in silicon with nanocrystal storage" Tech. Dig. - Int. Electron Devices Meeting. p. 521 1995.
- [4.5] E. Suzuki, H. Hayashi, K. Ishii, and Y. Hayashi, "A low-voltage alterable EEPROM with Metal-Oxide-Nitride-Oxide-Semiconductor/MONOS/structures". IEEE Trans. Electron Devices, 30, 122 (1983).
- [4.6] F. M. Yang, T. C. Chang, P. T. Liu, U. S. Chen, P. H. Yeh, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Lou, "Nickel nanocrystals with HfO₂ blocking oxide for nonvolatile memory application". Appl. Phys. Lett. 90, 222104 (2007).
- [4.7] Y. S. Jang, J. H. Yoon, and R. G. Elliman, "Formation of nickel-based nanocrystal monolayers for nonvolatile memory applications". Appl. Phys. Lett. 92, 253108 (2008).
- [4.8] Y. Pei, M. Nishijima, T. Fukushima, T. Tanaka, and M. Koyanagi, "Memory characteristics of self-assembled tungsten nanodots dispersed in silicon nitride". Appl. Phys. Lett. 93, 113115 (2008).
- [4.9] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal nanocrystal memories. I. Device design and fabrication". IEEE Trans. Electron Devices, 49, 1606 (2002).
- [4.10] L. Bi, Y. He, J. Y. Feng and Z. J. Zhang, "Effect of post-annealing in oxygen

- atmosphere on the photoluminescence properties of nc-Si rich SiO₂ films”.
Nanotechnology. 17, 2289 (2006).
- [4.11] P. H. Yeh, C. H. Yu, L. J. Chen, H. H. Wu, P. T. Liu and T. C. Chang,
“Low-power memory device with NiSi nanocrystals embedded in silicon
dioxide layer”. Appl. Phys. Lett. 87, 193504 (2005).
- [4.12] R. Peibst, T. Dürkop, T. Bugiel, A. Fissel, I. Costina, and K. R. Hofmann,
“Driving mechanisms for the formation of nanocrystals by annealing of
ultrathin Ge layers in SiO₂”. Physical review B 79, 195316 (2009).
- [4.13] T. Stoica and E. Sutter, “Ge dots embedded in SiO₂ obtained by oxidation of
Si/Ge/Si nanostructures”. Nanotechnology, 17, 4912 (2006).
- [4.14] S. Laureti, E. Agostinelli, G. Scavia, G. Varvaro, V. Rossi Albertini, A.
Generosi, B. Paci, A. Mezzi, S. Kaciulis, “Effect of oxygen partial pressure on
PLD cobalt oxide films”. Applied Surface Science 254, 5111 (2008).
- [4.15] D. R. Lide, Handbook of Chemistry and Physics, 81st Edition (2000).
- [4.16] Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, “Effects of traps on charge
storage characteristics in metal-oxide-semiconductor memory structures based
on silicon nanocrystals”. J. Appl. Phys. 84, (1998) 2358 (1998).
- [4.17] P. Normand, E. Kapetanakis, P. Dimitrakis, D. Tsoukalas, K. Beltsios, N.
Cherkashin, C. Bonafos, G. Benassayag, H. Coffin, A. Claverie, V. Soncini, A.
Agarwal and M. Ameen, “Effect of annealing environment on the memory
properties of thin oxides with embedded Si nanocrystals obtained by
low-energy ion-beam synthesis”. Appl. Phys. Lett. 83, 168 (2003).

Chapter 5

- [5.1] G. R. Lin, C. J. Lin, H. C. Kuo, H. S. Lin, and C. C. Kao, “Improving carrier
transport and light emission in a silicon-nanocrystal based MOS light-emitting

- diode on silicon nanopillar array”. *Appl. Phys. Lett.* 90, 143102 (2007).
- [5.2] H. Wang, Y. Chen, H. B. Wang, C. Zhang, F. J. Yang, J. X. Duan, and C. P. Yang, Y. M. Xu, M. J. Zhou, and Q. Li, “High resolution transmission electron microscopy and Raman scattering studies of room temperature ferromagnetic Ni-doped ZnO nanocrystals”. *Appl. Phys. Lett.* 90, 052505 (2007).
- [5.3] J. M. Moon, J. H. Bae, J. A. Jeong, S. W. Jeong, N. J. Park, H. K. Kim, J. W. Kang, J. J. Kim, and M. S. Yi, “Enhancement of hole injection using ozone treated Ag nanodots dispersed on indium tin oxide anode for organic light emitting diodes”. *Appl. Phys. Lett.* 90, 163516 (2007).
- [5.4] S. Tiwari, F. Rana, K. Chan, H. Hanafi, C. Wei, and D. Buchanan, “Volatile and non-volatile memories in silicon with nanocrystal storage” *Tech. Dig. - Int. Electron Devices Meeting*, p. 521 1995.
- [5.5] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, “Metal nanocrystal memories. I. Device design and fabrication”. *IEEE Trans. Electron Devices*, 49, 1606 (2002).
- [5.6] Z. Tan, S. K. Samanta, W. J. Yoo, and S. Lee, “Self-assembly of Ni nanocrystals on HfO and N-assisted Ni confinement for nonvolatile memory application”. *Appl. Phys. Lett.* 86, 013107 (2005).
- [5.7] Y. Nakamura, Y. Nagadomi, K. Sugie and N. Miyata, “Formation of ultrahigh density Ge nanodots on oxidized Ge/Si (111) surfaces”. *J. Appl. Phys.* 95, 5014 (2004).
- [5.8] J. H. Chen, W. J. Yoo, D. S. H. Chan, and L. J. Tang, “Self-assembly of Al₂O₃ nanodots on SiO₂ using two-step controlled annealing technique for long retention nonvolatile memories”. *Appl. Phys. Lett.* 86, 073114 (2005).
- [5.9] D. Aurongzeb, S. Patibandla, M. Holtz and H. Temkin, “Self-assembly of faceted Ni nanodots on Si (111)”. *Appl. Phys. Lett.* 86, 103107 (2005).

- [5.10] H. G. Chew, W. K. Choi, Y. L. Foo, F. Zheng, W. K. Chim, Z. J. Voon, K. C. Seow, E. A. Fitzgerald and D. M. Y. Lai, "Effect of germanium concentration and oxide diffusion barrier on the formation and distribution of germanium nanocrystals in silicon oxide matrix". *Nanotechnology*. 17, 1964 (2006).
- [5.11] L. Bi, Y. He, J. Y. Feng and Z. J. Zhang, "Nickel induced phase separation and nanocrystal growth in Si-rich silica films". *Nanotechnology*. 17, 2289 (2006).
- [5.12] S. K. Ray, T. N. Adam, G. S. Kar, C. P. Swann and J. Kolodzey, "Low Thermal Budget NiSi Films on SiGe Alloys". *Mat. Res. Soc. Symp. Proc.* 745, N6.6.1 (2003).
- [5.13] H. B. Yao, M. Bouville, D. Z. Chi, H. P. Sun, X. Q. Pan, D. J. Srolovitz and D. Mangelinckd, "Interplay Between Grain Boundary Grooving, Stress, and Dealloying in the Agglomeration of NiSiGe Films". *Electrochemical and Solid-State Letters*. 10(2), H53-55 (2007).
- [5.14] K. L. Pey, W. K. Choi, S. Chattopadhyay, H. B. Zhao, E. A. Fitzgerald, D. A. Antoniadis and P. S. Lee, "Stability and composition of Ni-germanosilicided SiGe films". *J. Vac. Sci. Technol. A*. 20(6), 1903 (2002).
- [5.15] W. K. Choi, V. Ng, S. P. Ng, H. H. Thio, Z. X. Shen and W. S. Li, "Raman characterization of germanium nanocrystals in amorphous silicon oxide films synthesized by rapid thermal annealing". *J. Appl. Phys.* 86, 1398 (1999).
- [5.16] Y. Nakayama, I. Matsuda, S. Hasegawa, and M. Ichigawa, "Quantum regulation of Ge nanodot state by controlling barrier of the interface layer". *Appl. Phys. Lett.* 88, 253102 (2006).
- [5.17] M. She and T. J. King, "Impact of crystal size and tunnel dielectric on semiconductor nanocrystal memory perform". *IEEE Trans. Electron Devices*, vol. 50, pp. 1934, (2003).
- [5.18] T. H. Ng, W. K. Chim, W. K. Choi, V. Ho, L. W. Teo, A. Y. Du, and C. H.

- Tung, "Minimization of germanium penetration, nanocrystal formation, charge storage, and retention in a trilayer memory structure with silicon nitride/hafnium dioxide stack as the tunnel dielectric". *Appl. Phys. Lett.* 84, 4385 (2004).
- [5.19] B. Garrido, S. Cheylan, O. González-Varona, A. Pérez-Rodríguez, "The effect of additional oxidation on the memory characteristics of metal-oxide-semiconductor capacitors with Si nanocrystals". *Appl. Phys. Lett.* 82, 4818 (2003).
- [5.20] G. Hollinger, P. Kumurdjian, J. M. Mackowski, P. Pertosa, L. Porte, and T. M. Duc, "ESCA study of molecular $\text{GeS}_{3-x}\text{Te}_x\text{As}_2$ glasses" *J. Electron Spectrosc. Relat. Phenom.* 5, 237 (1974).
- [5.21] P. X. Xu, S. R. Das, J. P. McCaffrey, C. J. Peters, L. E. Erickson, *Mater. Res. Soc. Symp. Proc.* 402, 59 (1995).
- [5.22] T. C. Chang, S. T. Yan, Y. H. Tai, P. T. Liu, and S. M. Sze, "A distributed charge storage with GeO nanodots". *Appl. Phys. Lett.* 84, 2581 (2004).
- [5.24] C. L. Yuan and P. S. Lee, "Enhanced charge storage capability of Ge/GeO₂ core/shell nanostructure". *Nanotechnology.* 19, 355206 (2008).
- [5.25] J. H. Chen, Y. Q. Wang, W. J. Yoo, Y. C. Yeo, G. Samudra, D. S. Chan, A. Y. Du and D. L. Kwong, "Nonvolatile flash memory device using Ge nanocrystals embedded in HfAlO high-tunneling and control oxides: device fabrication and electrical performance" *IEEE Trans. Electron Devices* ED-51, 1840 (2004).
- [5.26] H. Kim, S. Woo, H. Kim, S. Bang, Y. Kim, D. Choi, and H. Jeon, "Pt nanocrystals embedded in remote plasma atomic-layer-deposited HfO₂ for nonvolatile memory devices". *Electrochem. Solid-State Lett.* 12, H92 (2009).

Chapter 6

- [6.1] J. D. Blauwe, "Nanocrystal nonvolatile memory devices". IEEE Trans. Nanotechnology. 1, 72 (2002).
- [6.2] S. Tiwari, F. Rana, K. Chan, H. Hanafi, C. Wei, and D. Buchanan, "Volatile and non-volatile memories in silicon with nanocrystal storage" Tech. Dig. - Int. Electron Devices Meeting. p. 521 1995.
- [6.3] Y. H. Kwon, C. J. Park, W. C. Lee, D. J. Fu, Y. Shon, T. W. Kang, C. Y. Hong, H. Y. Cho, and K. L. Wang, "Memory effects related to deep levels in metal-oxide-semiconductor structure with nanocrystalline Si". Appl. Phys. Lett. 80, 2502 (2002).
- [6.4] B. Li and J. Liu, "CoSi₂-coated Si nanocrystal memory". J. Appl. Phys. 105, 084905 (2009).
- [6.5] Y. S. Lo, K. C. Liu, J. Y. Wu, C. H. Hou, and T. B. Wu, "Bandgap engineering of tunnel oxide with multistacked layers of Al₂O₃/HfO₂/SiO₂ for Au-nanocrystal memory application". Appl. Phys. Lett. 93, 132907 (2008).
- [6.6] H. Kim, S. Woo, H. Kim, S. Bang, Y. Kim, D. Choi, and H. Jeon, "Pt nanocrystals embedded in remote plasma atomic-layer-deposited HfO₂ for nonvolatile memory devices". Electrochem. Solid-State Lett. 12, H92 (2009).
- [6.7] C. L. Yuan, P. Darmawan, Y. Setiawan, and P. S. Lee, "LaAlO nanocrystals embedded in amorphous LuO high-k gate dielectric for floating gate memory application", Electrochem. Solid-State Lett. 9, F53 (2006).
- [6.8] V. Mikhelashvili, G. Eisenstein, F. Edelman, "Structural properties and electrical characteristics of electron-beam gun evaporated erbium oxide films". Appl. Phys. Lett. 80, 2156 (2002).
- [6.9] W. B. Kim, T. Matsumoto, and H. Kobayashi, "Ultrathin SiO layer with an extremely low leakage current density formed in high concentration nitric acid".

- J. Appl. Phys. 105, 103709 (2009).
- [6.10] J. C. Chiang and J. G. Hwu, "Low temperature (<400 °C) Al₂O₃ ultrathin gate dielectrics prepared by shadow evaporation of aluminum followed by nitric acid oxidation". Appl. Phys. Lett. 90, 102902 (2007).
- [6.11] Asuha, T. Kobayashi, O. Maida, M. Inoue, M. Takahashi, Y. Todokoro, and H. Kobayashi, "Ultrathin silicon dioxide layers with a low leakage current density formed by chemical oxidation of Si". Appl. Phys. Lett. 81, 3410 (2002).
- [6.12] Asuha, Y. L. Liu, O. Maida, M. Takahashi, and H. Kobayashi, "Postoxidation annealing treatments to improve Si/ultrathin SiO characteristics formed by nitric acid oxidation". J. Electrochem. Soc. 151, G824 (2004).
- [6.13] C. S. Kuo, J. F. Hsu, S. W. Huang, L. S. Lee, M. J. Tsai, and J. G. Hwu, "High-k Al₂O₃ gate dielectrics prepared by oxidation of aluminum film in nitric acid followed by high-temperature annealing". IEEE Trans. Electron Devices 51, 854 (2004).
- [6.14] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal nanocrystal memories. I. Device design and fabrication". IEEE Trans. Electron Devices, 49, 1606 (2002).
- [6.15] J. K. Kim, H. J. Cheong, Y. Kim, J.-Y. Yi, H. J. Bark, S. H. Bang, and J. H. Cho, "Rapid-thermal-annealing effect on lateral charge loss in metal-oxide-semiconductor capacitors with Ge nanocrystals Appl. Phys. Lett. 82, 2527 (2003).
- [6.16] S. K. Kang, B. G. Min, J. H. Yoo, S. W. Nam, D.H. Ko, H. B. Kang, C. W. Yang, and M. H. Cho, "Interfacial Reaction in Poly Si_{1-x}Ge_x/ZrO₂ with Ge Content in Poly Si_{1-x}Ge_x Films" Electrochem. Solid-State Lett. 5(12), G113 (2002).
- [6.17] H. K. Asuha, O. Maida, M. Takahashi, and H. Iwasa, "Nitric acid oxidation of

Si to form ultrathin silicon dioxide layers with a low leakage current density”. J. Appl. Phys. 94, 7328 (2003).

[6.18] R. J. Carter, E. Cartier, A. Kerber, L. Pantisano, T. Schram, S. De Gendt, and M. Heyns, “Passivation and interface state density of SiO/ HfO-based/ polycrystalline-Si gate stacks”. Appl. Phys. Lett. 83, 533 (2003).

[6.19] K. Prabhakaran and T. Ogino, “Behavior of ultrathin layers of Co on Si and Ge systems”. Appl. Surf. Sci. 100-101, 518 (1997)



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Publication List (著作目錄)

International Journals:

1. **C. W. Hu**, T. C. Chang, P. T. Liu, C. H. Tu, S. K. Lee, S. M. Sze, C. Y. Chang, B. S. Chiou, and T. Y. Tseng, "Formation of cobalt-silicide nanocrystal in Ge-doped dielectric layer for the application on nonvolatile memory" Appl. Phys. Lett., 92, 152115 (2008).
2. C. C. Lin, T. C. Chang, C. H. Tu, W. R. Chen, **C. W. Hu**, S. M. Sze, Chun-Yen Chang, T. Y. Tseng, "Formation of Mo Silicide Nanodot Memory by Rapid Thermal Annealing Dual Electron-Gun Evaporated Mo-Si Layer," Electrochem. and Solid-State Lett., 11, H202 (2008).
3. C. C. Lin, T. C. Chang, C. H. Tu, W. R. Chen, **C. W. Hu**, S. M. Sze, T. Y. Tseng, S. C. Chen, and J. Y. Lin, "Charge storage characteristics of Mo nanocrystal dependence on Mo oxide reduction," Appl. Phys. Lett., 93, 222101 (2008).
4. **C. W. Hu**, T. C. Chang, C. H. Tu, C. N. Chiang, C. C. Lin, S. M. Sze, and T. Y. Tseng, "NiSiGe nanocrystal for nonvolatile memory devices" Appl. Phys. Lett., 94, 062102 (2009). Also selected to be published in Virtual Journal of Nanoscale Science & Technology, February 23, (2009)
5. **C. W. Hu**, T. C. Chang, C. H. Tu, P. K. Shueh,, C. C. Lin, S. M. Sze, T. Y. Tseng, and M. C. Chen, "Cobalt nanodots formed by annealing the CoSiO layer for the application of the nonvolatile memory" Appl. Phys. Lett., 94, 102106 (2009).
6. **C. W. Hu**, T. C. Chang, C. H. Tu, C. N. Chiang, C. C. Lin, S. W. Lee, C. Y. Chang, S. M. Sze, and T. Y. Tseng, "Enhancement of NiSi-Based Nanocrystal Formation by Incorporating Ge Elements for Nonvolatile Memory Devices" J. Electrochem. Soc. 156(9), H751 (2009).
7. C. C. Lin, T. C. Chang, C. H. Tu, W. R. Chen, **C. W. Hu**, S. M. Sze, T. Y. Tseng, S. C. Chen, and J. Y. Lin, "Improved reliability of Mo nanocrystal memory with ammonia plasma treatment," Appl. Phys. Lett., 94 , 062106 (2009).
8. C. C. Lin, T. C. Chang, C. H. Tu, W. R. Chen, C. W. Hu, S. M. Sze, T. Y. Tseng, S. C. Chen, and J. Y. Lin, "Charge storage characteristics of Mo nanocrystal memory influenced by ammonia plasma treatment", J. Electrochem. Soc. 156 (9) H716 (2009).
9. **C. W. Hu**, T. C. Chang, C. H. Tu, Y. H. Huang, C. C. Lin, M. C. Chen, F. S. Huang, S. M. Sze, and T. Y. Tseng, "High Density Ni Nanocrystal Formed by Coevaporating Ni and SiO₂ Pellets for the Nonvolatile Memory Device Application" Electrochemical and Solid-State Lett. 13 (3), H49 (2010).
10. **C. W. Hu**, T. C. Chang, C. H. Tu, Y. H. Huang, C. C. Lin, M. C. Chen, F. S.

Huang, S. M. Sze, and T. Y. Tseng, "Nitric Acid Oxidation of Si for the Tunneling Oxide Application on CoSi₂ Nanocrystal Nonvolatile Memory" J. Electrochem. Soc. 157(3), H332 (2010).

11. C. C. Lin, T. C. Chang, C. H. Tu, S. C. Chen, **C. W. Hu**, S. M. Sze, T. Y. Tseng, S. C. Chen, and J. Y. Lin, "Charge storage characteristics of Mo nanocrystal memory influenced by ammonia plasma treatment", J. Phys. D: Appl. Phys. 43, 075106 (2010).
12. M. C. Chen, T. C. Chang, S. Y. Huang, S. C. Chen, **C. W. Hu**, C. T. Tsai, and S. M. Sze, Electrochemical and Solid-State Lett. 13 (6), H191 (2010).
13. **C. W. Hu**, T. C. Chang, C. H. Tu, C. N. Chiang, C. C. Lin, M. C. Chen, C. Y. Chang, S. M. Sze, and T. Y. Tseng, "Formation of the distributed NiSiGe nanocrystal nonvolatile memory formed by rapidly annealing in N₂ and O₂ ambient, has been accepted by Thin Solid Films 2010.
14. M. C. Chen, T. C. Chang, C. T. Tsai, S. Y. Huang, S. C. Chen, **C. W. Hu**, S. M. Sze, and M. J. Tsai, "Influence of electrode material on the resistive memory switching property of indium gallium zinc oxide thin films," Appl. Phys. Lett., 96 , 262110 (2010).

International conference:

1. **C. W. Hu**, T. C. Chang, P. T. Liu, C. H. Tu, C. C. Lin, C. N. Chiang, C. Y. Chang, T. Y. Tseng "Improved grain size of polysilicon using Fluorine/Nitrogen implantation technology" International Conference on Metallurgical Coating and Thin Films, San Diego, CA, USA (2008).
2. C. C. Lin, T. C. Chang, S. C. Chen, and J. Y. Lin, C. H. Tu, **C. W. Hu**, S. M. Sze, T. Y. Tseng, "Influence of annealing temperature on formation of Mo nanocrystal memory in oxygen incorporated Mo and Si thin film," International Conference on Metallurgical Coating and Thin Films, San Diego, CA, USA (2009).
3. **C. W. Hu**, T. C. Chang, C. H. Tu, C. N. Chiang, C. C. Lin, M. C. Chen, C. Y. Chang, S. M. Sze, T. Y. Tseng "Formation of the distributed NiSiGe nanocrystal nonvolatile memory formed by rapidly annealing in N₂ and O₂ ambient" Taiwan Association for Coatings and Thin Films Technology (TACT 2009), Taipei, Taiwan (2009).
4. **C. W. Hu**, T. C. Chang, C. H. Tu, Y. H. Huang, C. C. Lin, M. C. Chen, F. S. Huang, S. M. Sze, and T. Y. Tseng "Cobalt nanocrystal embedded in silicon oxide fabricated by incorporating oxygen elements during sputtering process " International Conference on Metallurgical Coating and Thin Films, San Diego, CA, USA (2010).