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博 士 論 文

碳摻雜製程與高性能多晶矽奈米線薄膜電晶體之研究

A Study on Carbon Doping Technology and High-Performance Poly-Si Nanowire TFTs

研 究 生：李 振 銘

指導教授：崔 秉 鉞

中華民國 一〇〇 年 十一 月

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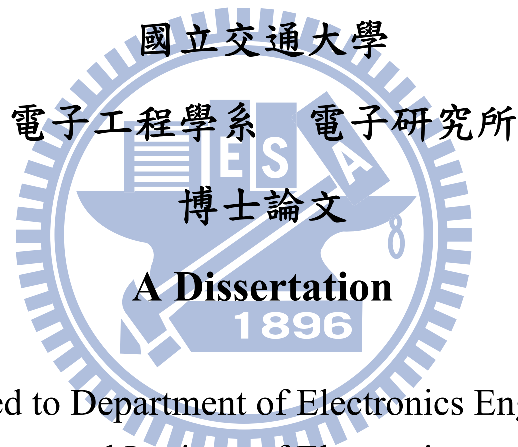

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摘要

在本論文中，吾人首先研究碳摻雜製程對於矽化鎳薄膜之熱穩定性、矽化鎳接觸之 n^+/p 接面之影響，並利用低溫碳離子佈植技術搭配固態磊晶退火方式，完成碳化矽薄膜的製作。其次，吾人成功製作出閘極長度僅三十奈米之高性能多晶矽奈米線薄膜電晶體，藉由元件結構設計，能得到良好的短通道特性與極高的導通電流值。吾人也探討元件尺寸大小對於多晶矽薄膜電晶體之電流傳導機制的影響，並用來解釋所觀察到的兩種自我加熱（self-heating）現象。最後在小尺寸多晶矽奈米線薄膜電晶體上，吾人首次觀察到隨機電報雜訊（random telegraph noise）現象，並藉由模型推導與高溫測量，證實晶界陷阱也能造成隨機電報雜訊現象。

我們採用電漿浸潤式離子佈植法（plasma immersion ion implantation），將碳離子植入至矽基材表面，此技術具備高劑量摻雜與低能量植入的優點，但在低能量與長時間的佈植過程中，同時會沈積類鑽碳膜（diamond-like carbon）在矽基材表面上，阻擋矽化鎳的形成，因此，必須將反應溫度提升至 800 °C，才能形成矽化鎳。另一種離子植入方式為傳統離子佈植法，碳離子植入矽基材表面能改善矽化鎳薄膜之熱穩定性，特別是高溫下的結塊現象，其改善效率與存在於矽化鎳與

矽介面間的碳原子數量相關，在足夠的碳原子濃度下，矽化鎳薄膜的結塊溫度與晶相轉換溫度高達 850 °C 以上。即使矽化鎳薄膜厚度減薄時，碳摻雜技術仍能有效提升矽化鎳薄膜之結塊溫度高達 300 °C。然而，對於矽化鎳接觸之 n^+/p 接面來說，矽基材表面經過高劑量（$5x10^{15}$ cm^{-2}）的碳離子佈植與高溫退火後，仍有許多殘餘缺陷存在於矽基材表面，在矽化鎳反應的過程中，大量的鎳原子能經由這些缺陷快速擴散並抵達接面空乏區，造成 n^+/p 接面漏電流增加。

其次，藉由最佳化碳離子佈植與低溫固態磊晶退火製程，我們已經成功製作出取代位置上的碳原子濃度百分比為 1.046 %的碳化矽薄膜。然而，過高的碳原子濃度會減緩非晶矽區域的固態磊晶再結晶速率，造成不完全的再結晶與磷摻雜物重新分佈的現象，此兩因素皆會造成再結晶的碳化矽薄膜的片電阻值上升。

整合全包覆式閘極（gate-all-around）、超薄多晶矽奈米線基體與修正型蕭基能障（modified Schottky barrier）源汲極結構後，成功實現了閘極長度僅三十奈米的高性能多晶矽奈米線薄膜電晶體，具備良好的轉移曲線特性。碳離子佈植技術能解決極薄的全矽化鎳源汲極區域發生的結塊現象。我們也探討短通道效應、窄線寬效應及氨氣電漿處理對於元件直流特性之影響。當進一步採用高介電常數二氧化鉿來取代傳統二氧化矽閘極氧化層時，高性能多晶矽奈米線薄膜電晶體在低閘極電壓（2.587 V）與汲極電壓（1 V）操作下，其驅動電流值高達 549 μA/μm，為已發表過的文獻中最高的驅動電流值。這些實驗結果開啟多晶矽薄膜電晶體應用於三維積體電路（three-dimensional integrated circuits）的可能性。

我們也發現多晶矽薄膜電晶體中存在不同的電流傳導機制，大尺寸多晶矽薄膜電晶體的電流傳導機制為熱游離發射，然而，由於晶界效應消失，小尺寸多晶矽薄膜電晶體的電流傳導機制會轉變成飄移擴散模型。因此，當多晶矽薄膜電晶

體發生自我加熱效應時，大尺寸多晶矽薄膜電晶體的導通電流會增加，但是小尺寸多晶矽薄膜電晶體的導通電流會下降。

最後，我們分析小尺寸多晶矽奈米線薄膜電晶體的隨機電報雜訊，包含時域分析與頻域分析。除了氧化層陷阱與介面能態外，我們也推導由晶界陷阱所導致之載子數目擾動模型，並藉由高溫測量證實晶界陷阱也能造成隨機電報雜訊現象，未來欲將多晶矽薄膜電晶體實際應用到三維積體電路或是非揮發性記憶體時，此晶界陷阱導致之隨機電報雜訊必須納入考慮。

A Study on Carbon Doping Technology and High-Performance Poly-Si Nanowire TFTs

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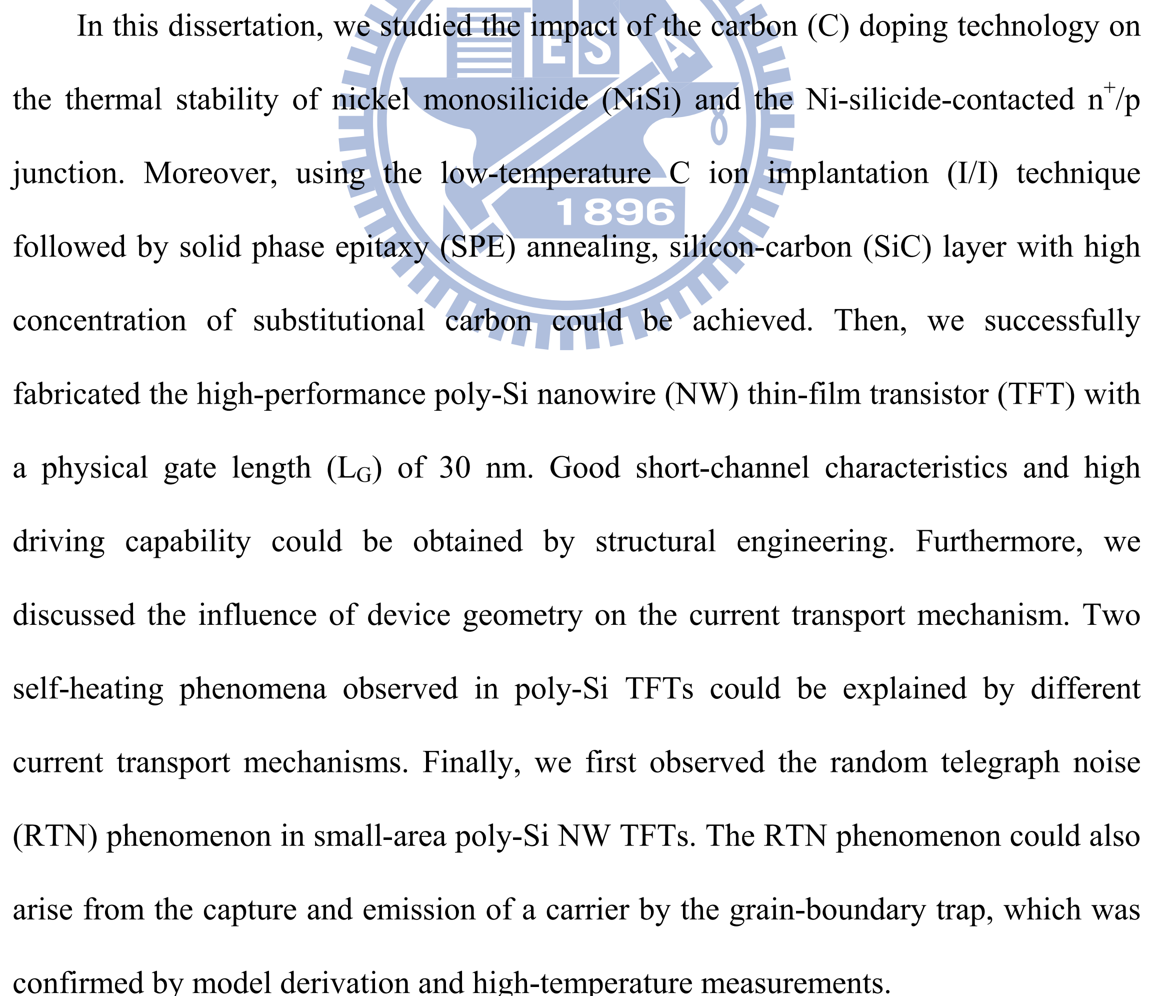
Abstract



In this dissertation, we studied the impact of the carbon (C) doping technology on the thermal stability of nickel monosilicide (NiSi) and the Ni-silicide-contacted n^+/p junction. Moreover, using the low-temperature C ion implantation (I/I) technique followed by solid phase epitaxy (SPE) annealing, silicon-carbon (SiC) layer with high concentration of substitutional carbon could be achieved. Then, we successfully fabricated the high-performance poly-Si nanowire (NW) thin-film transistor (TFT) with a physical gate length (L_G) of 30 nm. Good short-channel characteristics and high driving capability could be obtained by structural engineering. Furthermore, we discussed the influence of device geometry on the current transport mechanism. Two self-heating phenomena observed in poly-Si TFTs could be explained by different current transport mechanisms. Finally, we first observed the random telegraph noise (RTN) phenomenon in small-area poly-Si NW TFTs. The RTN phenomenon could also arise from the capture and emission of a carrier by the grain-boundary trap, which was confirmed by model derivation and high-temperature measurements.

We adopted the plasma immersion ion implantation (PIII) technology to implant C ions into the Si substrate surface. PIII has the advantages of high ion fluences and low energy implantation. However, for low energy and long period PIII process, a diamond-like carbon (DLC) film simultaneously deposited on the Si substrate surface and prevented Ni-silicide formation. Therefore, the silicide formation temperature must be raised to 800 °C. Another I/I method used in this study is the conventional C I/I process. Implanting C ions into the Si substrate surface could improve the thermal stability of the NiSi film, especially for the agglomeration phenomenon at high temperatures. The efficiency of improvement is related to the amount of C atoms at the NiSi/Si interface. With sufficient C concentration, the agglomeration and phase transformation temperatures of the NiSi film could be raised to higher than 850 °C. Even if the Ni-silicide film was thin, the C doping technology could still effectively raise the agglomeration temperature of the Ni-silicide film at high as 300 °C. Moreover, For the Ni-silicide-contacted n^+/p junction, after high-dose (5x10^{15} cm^{-2}) C I/I and high-temperature annealing, there were still many residue defects existing in the Si substrate surface. During the formation of Ni silicide, a large number of Ni atoms would rapidly diffuse and arrive at the junction depletion region via these defects, which caused the increase of the n^+/p junction leakage current.

We have successfully fabricated the SiC film with substitutional C concentration of 1.046 % by optimizing the C I/I and SPE annealing processes. Nevertheless, excess C concentration retarded the SPE regrowth rate in the amorphous Si region. Therefore, the incomplete recrystallization and phosphorus (P) dopant redistribution phenomena were observed and both resulted in the increase in sheet resistance of the recrystallized SiC film.

After the integration of the gate-all-around (GAA) structure, ultra-thin and narrow

poly-Si body, and modified Schottky barrier (MSB) source/drain (S/D) junction, the high-performance poly-Si NW TFT with L_G= 30 nm was successfully realized. It had good transfer characteristics. The fully-Ni-silicided S/D was agglomerated owing to the thinner NiSi film, which could be resolved by the C I/I technology. We also discussed the effects of the short channel, narrow width, and ammonia (NH_3) plasma treatment on the dc characteristics of the poly-Si NW TFTs. When the silicon dioxide (SiO_2) gate dielectric was further replaced by high permittivity (high-κ) hafnium oxide (HfO_2), the driving current of the high-performance poly-Si NW TFT biased at low gate and drain voltages (V_{GS}= 2.587 V and V_{DS}= 1 V) was up to 549 μA/μm. This value is the highest among the published literature. These experimental results open the possibility that poly-Si TFTs could be applied in three-dimensional integrated circuits (3D IC).

We also found different current transport mechanisms in poly-Si TFTs. The current transport mechanism in large-area poly-Si TFTs is considered as thermionic emission. However, the current transport mechanism in small-area poly-Si TFTs transformed into the drift-diffusion model owing to the disappearance of the grain-boundary effect. Therefore, as the self-heating effect (SHE) occurs in poly-Si TFTs, the on-state current increases in large-area poly-Si TFTs but decreases in small-area poly-Si TFTs.

Finally, we analyzed the RTN phenomenon in small-area poly-Si TFTs, such as time-domain and frequency-domain analysis. In addition to the gate oxide trap and the interface state, we also derived the carrier number fluctuation model induced by the grain-boundary trap. By high-temperature measurements, we proved that a capture and a release of a carrier by the grain-boundary trap could also cause the RTN phenomenon. As poly-Si TFTs are applied to future 3D IC or 3D nonvolatile memories, the RTN phenomenon induced by the grain-boundary trap should be considered.

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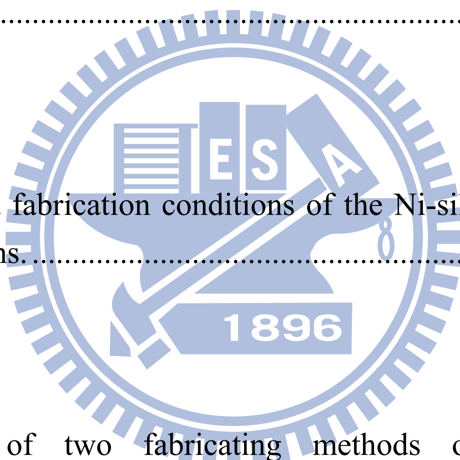

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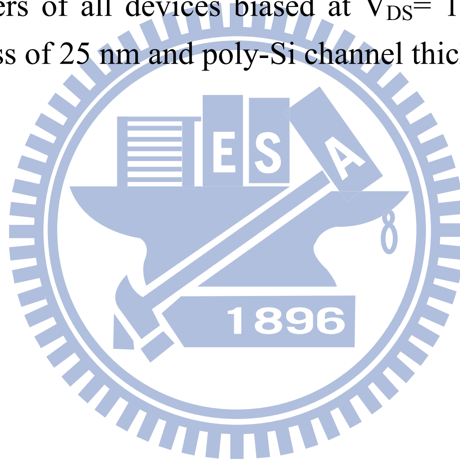

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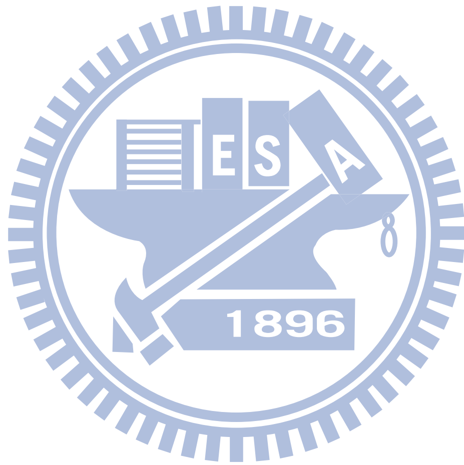

Chapter 1

Introduction

1.1 The Development of CMOS Technology

Over the past several decades, CMOS scaling successfully drives the development of the electronic industry. It follows Moore's law proposed by Gordon Moore in 1965 [1]. Gordon Moore predicted the number of available transistors in the same chip area would be doubled every two years. Device feature size scaling not only reduces production cost and the operating voltage but also increases the operation speed and device density. Therefore, due to these benefits, transistor size has been continuously scaled down to 22 nm in 2011. During the 1965-to-2011 time period, in order to accelerate feature size scaling and sustain Moore's law, MOSFET structures, materials, and process technologies have changed greatly. First, for solving alignment problems, the aluminum (Al) gate was replaced by the poly-crystalline silicon (poly-Si) gate in the 1970's [2]. The non-self-aligned gate-last process was changed to the self-aligned gate-first process. Second, the titanium (Ti) self-aligned silicidation (salicide) process was first employed in the early 1990's to reduce the gate and source/drain (S/D) resistance [3]. Although the silicide material changes from Ti-silicide to cobalt-silicide (Co-silicide) and then nickel-silicide (Ni-silicide), the salicide process is the standard CMOS process flow until now. Third, the strained Si technology was adopted to increase the carrier mobility at the 90-nm technology node in 2003 [4]. Strain engineering can effectively compensate the mobility degradation

caused by high channel doping. Fourth, the high-permittivity (high-κ) gate dielectric/metal gate stack was used to further reduce the equivalent oxide thickness (EOT) at the 45-nm technology node in 2007 [5]. The self-aligned gate-first process was changed to the self-aligned gate-last process because of thermal stability issues associated with the high-κ gate dielectric/metal gate stack. At this time, the MOSFET structure still belonged to the planar bulk structure. Figure 1-1 shows new device structures and materials of the new MOSFET generation predicted by the 2009 International Technology Roadmap for Semiconductors (ITRS) [6].

Although the 2009 ITRS predicted the planar bulk structure can still be used at the 22-nm technology node, on May 4, 2011, Intel Corporation has announced that the three-dimensional (3D) tri-gate transistor structure will go into mass production in the end of 2011 [7]. As compared to the planar bulk structure, the benefits of the tri-gate transistor structure include steeper subthreshold slope, lower leakage currents, and better short-channel effect (SCE) immunity [8]. Therefore, the tri-gate transistor can operate at lower voltage to reduce operating power and improve switching speed. However, according to the 2010 ITRS update, there still remain many difficult challenges to overcome below the 16-nm technology node, such as control of short-channel effects (SCEs) and S/D parasitic series resistance, and continued EOT (< 0.7 nm) and junction depth (~10 nm) scaling [9]. To relax MOSFET scaling issues mentioned above, the concept of 3D integrated circuits (IC) demonstrated as early as in 1979 has been reproposed recently [10]. It is a vertical extension of IC technology and contains the multiple active layers stacked together with vertical interconnections between the layers to achieve 3D on-chip integration. The benefits of 3D IC include improved packing density, reduced total power, and noise immunity [11]. It has been reported that poly-Si thin-film transistors (TFTs) have the potential for extensive

applications in 3D IC [12]. Therefore, the poly-Si-based 3D IC is one of the possible solutions as device feature size scaling faces severe limitations in the future.

1.2 Carbon (C) Doped Ni-Silicide-Contacted Junction

To control SCEs and reduce parasitic S/D resistance, the silicide-contacted junction should simultaneously have ultra-shallow junction depth, low junction leakage, high doping concentration, low sheet resistance (R_s), and low contact resistivity. Their specific requirements in future technology nodes are listed in Table 1-1. Ni monosilicide (NiSi) is used for the contact material in present CMOS technology owing to its several advantages including low resistivity, low contact resistivity, low formation temperature, less Si consumption during silicide formation, line-width independent silicidation, no exhibition of bridging failure, and compatibility with SiGe [3, 13]. However, the major drawback of using NiSi is its poor thermal stability. The NiSi film normally agglomerates at 700 °C and transforms into high-resistive Ni disilicide ($NiSi_2$) phase at 750 °C [14]. Junction depth scaling is accompanied by silicide thickness scaling. The thermal stability of the Ni-silicide film degrades with the thickness reduction, which causes an increase in the R_s values of Ni silicide [15]. For thinner NiSi films, the primary degradation mechanism at a higher temperature is agglomeration [15]. The NiSi film with a thickness of 12 nm on an arsenic (As) doped (100) substrate agglomerates at the temperature as low as 575 °C [15]. Therefore, the thermal degradation of a thin NiSi film becomes a main issue for two-dimensional (2D) IC or 3D IC applications. Although the raised S/D process can relax the thickness scaling issues of Ni silicide [16], it also increases the parasitic capacitance between the gate and S/D electrodes. Furthermore, the contact resistance at the Si/Ni silicide contact interface increases with the decrease in contact area [17].

Therefore, high S/D parasitic series resistance arises from the increased contact resistance and R_s. In recent years, several methods have been studied to reduce the contact resistance [18-20] and to enhance the thermal stability of Ni silicide [21-25].

The impact of the carbon (C) atom on pn junction characteristics has been extensively researched for several years [26-28]. The substitutional C atom (C_s) interacts with Si self-interstitial (I) to form the interstitial C atom (C_i), as shown below [28]:

$$C_s + I \rightarrow C_i, \qquad (1\text{-}1)$$

Furthermore, C atoms can also trap Si self-interstitials and then form immobile C/I clusters with higher order complex [26]. The effects of the C atoms and C/I clusters in Si are summarized in Table 1-2. The utility of the C atoms depends on its lattice location. The effect of C/I clusters on the ability to getter gold (Au) and copper (Cu) atoms was first discovered by H. Wong *et al.* in 1988 [29-30]. Later, H. Wong *et al.* also found that C atoms in Si can suppress the formation of extrinsic secondary defects after annealing owing to C-interstitial trapping reactions [31]. If secondary defects locate within the depletion region of the pn junction, it leads to an increase of reverse-bias pn junction leakage. Therefore, reduction in the reverse-bias leakage current is achieved by incorporating C atoms into Si [27]. Furthermore, the interstitial trapping characteristics of C atoms imply that they can also reduce interstitial-assisted dopant diffusion in Si. Many experimental results have confirmed that transient enhanced diffusion (TED) of boron (B) and phosphorus (P) is strongly suppressed in C-rich Si [32-34]. Hence, an ultra-shallow pn junction with an abrupt dopant profile can be formed by the retard dopant diffusion in the presence of C atoms. Recently, it has been reported that raising the thermal stability of NiSi is another benefit of the existence of C atoms in Si [25, 35]. Segregation of C atoms at the NiSi grain

boundaries and NiSi/Si interface effectively suppresses the agglomeration of NiSi. Therefore, it is feasible to improve the thermal stability of NiSi with the incorporation of C atoms.

The solid solubility of C in Si is only at concentrations of the order of 1×10^{17} cm^{-3} [26], so a small number of the incorporated C atoms are located at the substitutional sites in thermal equilibrium. If a large number of the incorporated C atoms have continued to reside on the substitutional Si lattice site of the S/D junction (~1 % substitutional C atoms in Si) without precipitation after MOSFET fabrication, they can produce uniaxial tensile stress in the Si channel of n-type MOSFETs [36-38]. Hence, using silicon-carbon (SiC or $Si_{1-x}C_x$) S/D stressors provides another way to enhance the electron mobility for future application in state-of-the-art n-type MOSFETs. In addition to several advantages described above, the junction degradation arises from interaction products between C atoms and I [26, 28]. The C_i and C/I clusters create deep-trap energy levels in the Si band gap [26, 39], which causes an increase in the thermal generation leakage current. Furthermore, C/I clusters can also act as neutral scattering centers to reduce the carrier mobility [26]. Therefore, the quantity of the C_i and C/I clusters in the depletion region of a C-doped pn junction should be reduced.

The above brief introduction of the C-doping effects in Si suggests that it is possible to integrate all advantages into the Ni-silicide-contacted pn junction and exclude the disadvantages. The junction characteristics of the C-doped diode with a Ni silicide contact have never been reported before. The C-doping effects on the thermal stability of Ni silicide and their related Schottky and n^+/p junction characteristics are both investigated in this thesis. Since it is feasible to integrate SiC

S/D stressors into the C-doped Ni-silicide-contacted n^+/p junction, the method of fabricating SiC alloys is also discussed in this thesis.

1.3 The Evolution of Poly-Si Nanowire (NW) TFTs

It is well known that active-matrix liquid crystal displays (AM-LCDs) and an active-matrix organic light emitting diode (AM-OLED) display have been successfully mass-produced with poly-Si TFTs. For high-level applications such as system on panel (SOP) and 3D IC in the future, the characteristics of poly-Si TFTs should be improved to achieve high performance. In the past several years, to achieve this goal, many studies focused on new recrystallization technologies combined with novel device structures. In addition to the conventional solid phase crystallization (SPC) method, large-grain poly-Si films are realized by excimer laser annealing (ELA) or metal-induced lateral crystallization (MILC) [40-43]. The device characteristics exhibit higher performance than the device characteristics of SPC poly-Si TFTs owing to a significant reduction of grain-boundary defects in the poly-Si channel region. Furthermore, the double-gate and tri-gate transistor structures integrated with the poly-Si nanowire (NW) or fin-like channel offer excellent short-channel control. However, the physical gate length (L_G) of these high-performance devices is longer than 1 μm.

High-performance SPC poly-Si NW TFTs with multi-gate structures have also been demonstrated recently [44-46]. All of them employed the gate-all-around (GAA) structure to enhance the gate-to-channel controllability and the multiple poly-Si NW channels to raise the current driving capability. H. H. Hsu *et al.* also reported that device variation of poly-Si NW TFTs can be suppressed by the GAA structure and the multiple poly-Si NW channels [44]. Excellent short-channel behaviors resulting from

the GAA structure and their relative long L_G ($L_G \geqq 0.4$ μm) were demonstrated. For future application in the 3D IC technology, similar to conventional MOSFETs, poly-Si TFTs should be scaled down to increase device density. The ultra-short-channel characteristics have been extensively investigated in GAA Si NW MOSFETs [47-50]. K. H. Yeo *et al.* demonstrated that short-channel immunity of GAA Si NW MOSFETs with L_G of 15 nm was achieved [49]. However, the ultra-short-channel characteristics of poly-Si TFTs are seldom reported in the literature. In 2005, B. Y. Tsui *et al.* first fabricated high-performance poly-Si TFTs with L_G as short as 100 nm [51]. Three years later, in 2008, M. Im *et al.* reported that poly-Si NW TFTs with L_G= 20 nm showed poor switching performance [52]. In this thesis, we study the ultra-short-channel characteristics of poly-Si TFTs by structural engineering. The multi-gate structure, ultra-thin poly-Si body, and hafnium dioxide (HfO_2) high-κ gate dielectric are employed to obtain good ultra-short-channel characteristics. To lower S/D parasitic resistance, we also fabricate the modified Schottky barrier (MSB) S/D structure via the two-step Ni-salicide process and the implant-to-silicide (ITS) technique [53]. Hence, the high current driving capability is also obtained in this work. Furthermore, the C ion implantation (I/I) technology is used to suppress the agglomeration of the fully-Ni-silicided S/D. These low-temperature fabrication processes are very suitable for 3D IC application.

In addition to the device characteristics, the self-heating phenomenon and noise properties of our high-performance poly-Si TFTs are also discussed in this thesis. The self-heating effect (SHE) resulting Joule heating becomes more and more significant with increasing the current driving capability [54]. The thermal problems of 3D IC are greater than those of 2D IC owing to many dielectric layers [11]. The device is completely surrounded by low thermal conductive inter-layer dielectric (ILD).

Therefore, the device characteristics of high-performance poly-Si TFTs with the high driving capability can be affected by the SHE, which is studied in this thesis.

Low frequency noise (LFN) in large-area poly-Si TFTs has been deeply investigated for several years [55-58]. For small-area poly-Si TFTs, LFN becomes more important because it is inversely proportional to the gate area [59]. The LFN behavior of small-area poly-Si TFTs has never been published. As the device size scales down, random telegraph noise (RTN) can be frequently observed in small-area MOSFETs [60]. RTN has been considered as the origin of LFN and becomes a main issue during device operation. The threshold voltage fluctuation arising form RTN affects the stability of static random access memory (SRAM) and the multi-level cell (MLC) operation of Flash memory [61-62]. In this thesis, we successfully observe the RTN phenomenon in our small-area poly-Si TFTs for the first time. When small-area poly-Si TFTs are applied in 3D IC and 3D stackable TFT Flash memories, RTN should be eliminated by advanced process technology.

1.4 Thesis Organization

In this dissertation, the main research topics can be divided into two parts. The first part contains the C-doping effects on the thermal stability of Ni silicide, the Ni-silicide-contacted junction characteristics, and the formation of SiC alloys. The process technologies and characteristics of GAA poly-Si NW TFTs are discussed in the second part.

In the first chapter of this dissertation, we briefly review the development of CMOS technology. To reduce the S/D series resistance and avoid SCEs, S/D engineering is necessary to achieve low parasitic resistance contacts and the abrupt doping profile. The advantages and disadvantages of the C-doping effects in Si are

also described in detail. The C-doping technology is a promising candidate for the fabrication of the ultra-shallow Ni-silicide-contacted junction. To relax several scaling barriers, 3D IC composed of poly-Si TFTs is one of the possible solutions. Therefore, the evolution of poly-Si NW TFTs is briefly introduced. High-performance poly-Si TFTs with a small device area are needed to build 3D IC. Furthermore, two main issues including the SHE and RTN phenomena in small-area poly-Si TFTs should be resolved in the near future.

In chapter 2, we study the impact of C and dopant atoms on the thermal stability of Ni silicide by using different C I/I technologies. A novel I/I technology, plasma immersion ion implantation (PIII), is used to implant C ions into the Si substrate surface. The thermal stability and formation of Ni silicide are dependent on the implantation and silicide-forming conditions. These experimental results will be discussed in this chapter.

In chapter 3, the influence of C atoms on the Ni-silicide-contacted Schottky and n^+/p junctions is discussed in detail. The reverse-bias leakage current mechanism of the C-doped Ni-silicide-contacted Schottky junction is considered as the increased thermionic-field emission. Furthermore, the agglomeration of the Ni-silicide film and the diffusion of Ni atoms into the depletion region result in an increase of the reverse-bias leakage current of the C-doped Ni-silicide-contacted n^+/p junction.

In chapter 4, we propose a low-temperature C I/I technology followed by solid phase epitaxy (SPE) regrowth to fabricate SiC alloys. Different SPE annealing technologies are employed to recrystallize the amorphous Si layer. High substitutional C concentration (C_{sub}) can be obtained by process optimization. We find that excess C concentration in Si leads to incomplete recrystallization and P redistribution phenomena.

In chapter 5, we successfully fabricate the smallest GAA poly-Si NW TFT with L_G of 30 nm. Good electrical characteristics are demonstrated by structural engineering. The agglomeration of thin Ni-silicide films in the S/D regions can still be improved by the C I/I technology. The difference of current transport mechanisms in large-area and small-area poly-Si TFTs is clarified. The device characteristics can be further improved by using an ammonia (NH_3) plasma treatment.

In chapter 6, to reduce the EOT, the HfO_2 high-κ gate dielectric is first introduced into poly-Si NW TFTs. Excellent device characteristics can be achieved, especially for high driving capability. Two SHE phenomena related to different current transport mechanisms are observed in large-area and small-area poly-Si TFTs.

In chapter 7, the two-level and complex RTN phenomena can be both observed in our small-area poly-Si NW TFTs for the first time. They can arise from the slow trap or the fast trap. We also derive the carrier number fluctuation model induced by the grain-boundary trap. Model accuracy is determined by high-temperature measurements.

Finally, in chapter 8, we will summarize important conclusions of this thesis. Future works are also suggested in this chapter.

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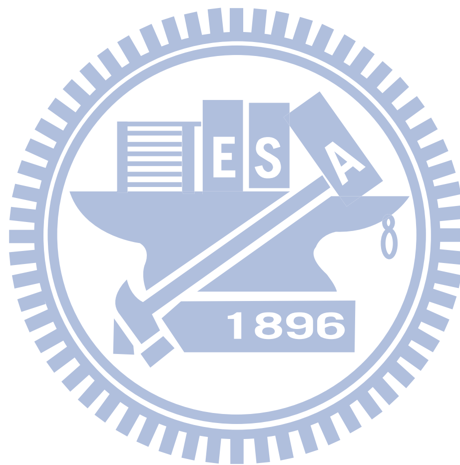
Table 1-1 Doping process technology requirements reported by the 2010 ITRS update for bulk microprocessor unit (MPU) [9].

Year of production	2011	2012	2013	2014	2015
MPU physical gate length (nm)	24	22	20	18	17
Drain extension junction depth (nm)	10.5	9.5	8.7	8	7.3
Maximum allowable parasitic series resistance (Ω/□)	160	140	130	110	110
Maximum drain extension sheet resistance (Ω/□)	660	680	750	810	900
Extension lateral abruptness (nm/decade)	2.8	2.4	2.3	2	1.8
Contact junction depth (nm)	29	26.7	24.7	22	19.8
Allowable junction leakage (μA/μm)	0.1	0.1	0.1	0.1	0.1
Maximum silicon consumption (nm)	14.5	13.4	12.4	11	9.9
Silicide thickness (nm)	17.9	16.2	14.7	13	12
Contact silicide sheet resistance (Ω/□)	9.1	9.9	10.8	12.1	13.5
Contact maximum resistivity ($\Omega\text{-cm}^2$)	8×10^{-8}	4×10^{-8}	2×10^{-8}	1×10^{-8}	8×10^{-9}

Table 1-2 Utility of the substitutional C atom, the interstitial C atom, and C/I clusters in Si.

Utility	Needed C-related elements
Gettering of Au and Cu	**C/I clusters**
Elimination of secondary defects	**substitutional C atom and interstitial C atom**
Suppression of B and P diffusion	**substitutional C atom and interstitial C atom**
Improvement of the thermal stability of NiSi	**segregated C atoms at the NiSi grain boundaries and NiSi/Si interface**
Application of SiC S/D stressors	**substitutional C atom**
Formation of deep-level defects	**interstitial C atom and C/I clusters**
Formation of neutral scattering centers	**C/I clusters**



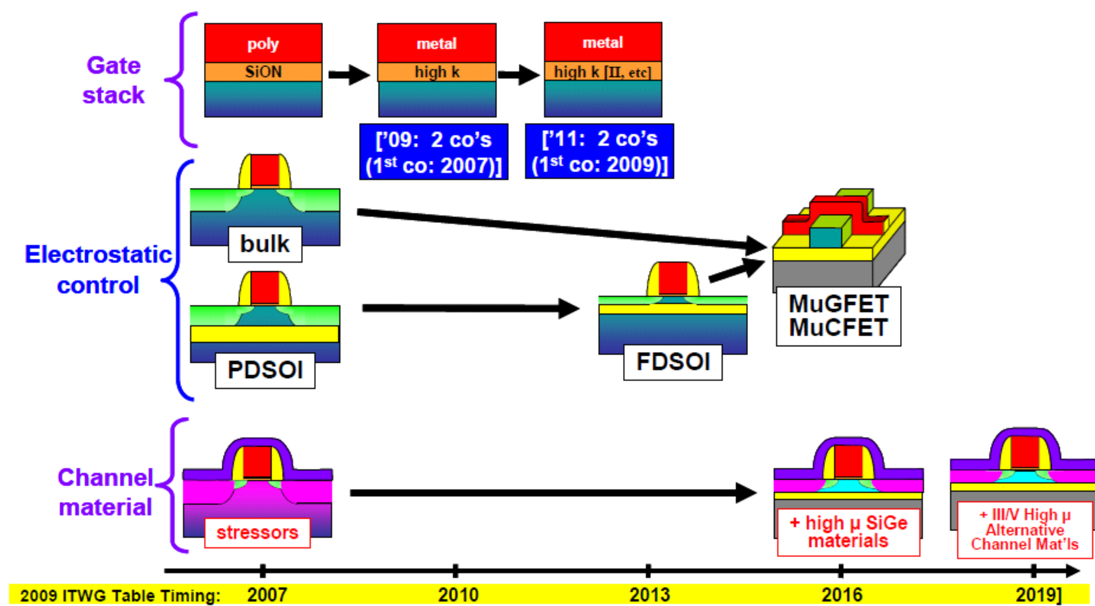


Fig. 1-1 Future evolution of the MOSFET including device structures and materials [6]. Where PD SOI and FD SOI represent partially depleted silicon-on-insulator and fully depleted silicon-on-insulator, respectively. MuGFET and MuCFET are the abbreviation for multi-gate FET and multi-channel FET, respectively.

Chapter 2

Thermal Stability and Formation of Nickel Silicide with Carbon Ion Implantation

2.1 Introduction

NiSi has been used as the S/D contact material of sub-100 nm MOSFET technology owing to its low resistivity, low contact resistivity, low-temperature process, less Si consumption during the silicide formation process, no bridging phenomenon, and no line-width effect [1]. For further scaling down the device, the main issue of NiSi is its poor thermal stability. It is known that the NiSi film agglomerates at 700 °C and transforms into $NiSi_2$ at 750 °C [2]. These two factors result in poor morphology and an increase of R_s and Si consumption. To suppress SCEs in the MOSFET, one of the well-known requirements is reducing the depth of the S/D junction. Therefore, for the Ni-silicide-contacted shallow junctions, the thickness of the NiSi film must be simultaneously thinned down to reduce the junction leakage current. However, O. Chamirian *et al.* have reported that the thermal stability of the NiSi film further degraded with reducing its thickness, and an abrupt increase in the R_s values was mainly caused by the agglomeration of the NiSi film [3].

Many different solutions have been proposed to improve the thermal stability of NiSi. These solutions involve I/I utilizing fluorine (F) or nitrogen (N_2) ions before NiSi formation, Ti or platinum (Pt) deposition as a capping layer or an interposing layer, and $Ni_{1-x}Ti_x$ or $Ni_{1-x}Pt_x$ alloy [4-9]. Recently, S. Zaima *et al.* reported that the

Ni film on the p^+ $Si_{0.996}C_{0.004}$ epitaxial layer grown by low-pressure chemical vapor deposition (LPCVD) can effectively suppress the NiSi agglomeration after annealing at 750 °C and retard its phase transformation until annealing at 850 °C [10]. This result indicates that adding C atoms in a Si substrate is a feasible method to enhance the thermal stability of NiSi. Since the solid solubility of C in Si and NiSi is very low [11], C atoms segregate to the NiSi grain boundary and NiSi/Si interface and modify grain-boundary and interfacial energy to suppress the agglomeration and phase transformation [12]. In this work, we introduce the I/I technology to dope C atoms into a Si substrate. This process is easier than the epitaxy process and can be integrated with the conventional CMOS process flow. The correlation between the C I/I dose and the thermal stability of NiSi is discussed. Furthermore, a novel I/I technology, PIII, is used to implant C ions into the Si substrate surface. The advantages of PIII include cheap equipment, high efficiency, conformal doping, large-area processing, and batch processing [13]. The effect of the C PIII technology on the thermal stability and formation of the NiSi film is also investigated.

2.2 Sample Fabrication

All samples can be divided into two main groups: the C I/I samples and the C PIII samples. The substrate types, experimental splits, and their corresponding notations are listed in Table 2-1.

2.2.1 The C I/I samples

The main process flow of the C I/I samples is described first. The lowest implantation energy of the high energy implanter utilized in this study is 30 keV. Because the atomic weight of C is only 12.011, in order to locate the projected range

(R_p) of C ions near the Si substrate surface, a rather thick screen silicon dioxide (SiO_2) was thermally grown to a thickness of 70 nm. Carbon ions were implanted into the Si substrate through the screen SiO_2 at 30 keV or 40 keV to a dose of $1x10^{15}$ cm^{-2} or $5x10^{15}$ cm^{-2}. The R_p of the implanted C ions at 30 keV and 40 keV below the SiO_2/Si interface are 28.5 nm and 58.7 nm, respectively. The lower implantation energy would lead to more C ions located near the Si substrate surface. After C I/I, some samples were annealed by a rapid thermal annealing (RTA) system in N_2 ambient at 1050 °C or 1100 °C for 30 sec to annihilate the implantation-induced defects. The samples implanted only with C ions and annealed at 1050 °C for 30 sec are called the C-implantation-annealing (CIA) samples. The samples implanted only with C ions and without post-implantation annealing are called the w/o CIA samples. A second of samples annealed at 1100 °C for 30 sec are fabricated to study whether C atoms could still enhance the thermal stability of the NiSi film with the existence of As atoms or not. After etching the screen SiO_2 by using dilute hydrofluoric acid (DHF) solutions, As ions were implanted into the Si substrate at 35 keV or 85 keV to a dose of $5x10^{15}$ cm^{-2} followed by a 1050 °C spike annealing process. The lower As I/I energy of 35 keV results in more dopants within the Ni-silicide film.

After etching the screen or native SiO_2 by using DHF solutions, a-25 nm-thick Ni layer and a 5-nm-thick titanium nitride (TiN) were sequentially deposited on these samples by a physical vapor deposition (PVD) system. The one-step RTA or two-step annealing process was performed to form the Ni-silicide film. The temperature range of the one-step RTA process in N_2 ambient varied from 500 °C to 850 °C for 30 sec. Then, un-reacted Ni and TiN capping metals were selectively removed by a mixture solution of H_2SO_4 and H_2O_2. For the two-step annealing process, the first step was performed in a vacuum environment at 300 °C for 60 min. After that, the TiN capping

layer and unreacted Ni were selectively removed by a mixture solution of H_2SO_4 and H_2O_2. The second annealing step was performed at the temperature range of 500-800 °C for 30 sec.

Another similar experiment was performed on the last set of samples in order to study the effect of C atoms on thinner Ni-silicide films. The different conditions are the implantation energy and dose of carbon. Carbon ions were implanted into a Si substrate at 7 keV to a dose of $5x10^{15}$ cm^{-2}. The R_p of the implanted C ions at 7 keV below the Si substrate surface is 27.7 nm. The thickness of the as-deposited Ni film was reduced to 10 nm. Silicide formation was performed at the temperature range from 500 °C to 900 °C for 30 sec. These samples are named the thin-Ni-silicide (TNS) samples. For three sets of samples, samples without C I/I were also prepared as reference.

2.2.2 The C PIII samples

Carbon ions were implanted into the Si substrate by a PIII system. The PIII system used in this study consists of a process chamber, a vacuum pumping system, a gas supply system, and an electrical power system. During this process, a Si wafer was put on a wafer holder, and the antenna in the chamber could generate the plasma between the antenna and the wafer. Methane (CH_4) gas was used as the source of C ions, and its flow rate controlled by a mass flow controller was 50 sccm. During the PIII process, the process pressure was fixed to be $1.2x10^{-3}$ Torr. The plasma was generated by a dc voltage supply with a value of 150 V. The input pulse voltage representing the implantation voltage was set to 3 kV or 5 kV, and the implantation time associated with the implantation dose was set to 1 min or 5 min. Then, the RTA process was employed in N_2 ambient at 900 °C for 15 sec to remove

implantation-induced damage. After removing the native SiO_2, a thin 15-nm-thick Ni film was deposited on the Si substrate surface. The one-step RTA process in N_2 ambient was performed from 500 °C to 900 °C for 30 sec to form the Ni-silicide film. Finally, un-reacted Ni was selectively removed by a mixture solution of H_2SO_4 and H_2O_2.

2.2.3 Material Analysis

The four-point probe technique was used to measure the R_s values of all samples. X-ray diffraction (XRD) was adopted to distinguish the NiSi phase from the $NiSi_2$ phase. Plan-view Scanning Electron Microscope (SEM) was used to inspect whether nickel silicide agglomerates. The thickness of the Ni-silicide film was inspected by transmission electron microscopy (TEM). The depth profile analysis of C atoms was obtained by secondary ion mass spectrometry (SIMS).

2.3 Results and Discussion

2.3.1 The C I/I samples

Figure 2-1 shows the R_s values of the CIA samples and control1 samples as a function of annealing temperature at a constant annealing time of 30 sec. As the silicide formation temperature is lower than 700 °C, it can be observed that the R_s values of the CIA samples are slightly higher than those of the control1 samples due to the existence of C atoms in the Ni-silicide film. Therefore, low-energy or high-dose C I/I results in slightly higher R_s values. According to the R_s values measured after deposition of the Ni film, we found that the thickness of the Ni film on the CIA samples implanted at 30 keV with a dose of $5x10^{15}$ cm^{-2} is thinner than those of the other samples, so its R_s values after Ni silicide formation are higher than the other

samples. The R_s values of the controll samples gradually increase after 700 °C because of serious agglomeration and phase transformation. At the same time, the R_s values of the CIA samples implanted at 40 keV with a dose of $1x10^{15}$ cm^{-2} are almost stable until 700 °C and start to increase at 800 °C because lightly agglomeration and phase transformation simultaneously occur, as shown in Fig. 2-2 and 2-3, respectively. As the C I/I dose increases up to $5x10^{15}$ cm^{-2}, the R_s values are stable without increasing until 850 °C. For the CIA samples implanted at 30 keV with a dose of $5x10^{15}$ cm^{-2}, the R_s values increase slightly at 850 °C. However, for the controll samples, the R_s values increase greatly at 850 °C due to serious agglomeration. For the CIA samples implanted at 40 keV with a dose of $5x10^{15}$ cm^{-2}, the R_s values keep unchanged even at 850 °C. The NiSi film is still continuous without agglomerating after 850 °C, as shown in Fig. 2-4(d). According to the XRD spectra shown in Fig. 2-5, the phase transformation dose not occur as well. Hence, the function of C atoms within the Ni-silicide film is suppressing agglomeration and phase transformation. Figure 2-6 and 2-7 show the cross-sectional TEM image and SIMS depth profile, respectively, of the CIA sample implanted at 40 keV with a dose of $5x10^{15}$ cm^{-2} after silicide formation at 500 °C for 30 sec. The thickness of the NiSi film is 52 nm. According to SIMS analysis, it is clearly observed that C atoms are distributed within the NiSi film and pile-up at the NiSi/Si interface.

Figure 2-8 shows the R_s values of the w/o CIA samples as a function of the annealing temperature for 30 sec. For the w/o CIA samples implanted to a dose of $1x10^{15}$ cm^{-2}, lightly agglomeration and phase transformation simultaneously take place at 800 °C, as shown in Fig. 2-9(b) and Fig. 2-10, respectively. The agglomeration and phase transformation temperatures of 800 °C are the same as those of the CIA samples under the same implantation conditions. When the C I/I dose

increases to $5x10^{15}$ cm^{-2}, as comparing between Fig. 2-1 and Fig. 2-8, the temperature dependence of the R_s values of the w/o CIA samples is more apparent than those of the CIA samples. We speculate that this phenomenon arises from the grain size variation of the Ni-silicide film. Because the Si surface is amorphized by the high-dose C I/I, the grain size of the Ni-silicide film of the w/o CIA samples is smaller than that of the CIA samples. Furthermore, the R_s values of the w/o CIA samples decrease with increasing grain size at higher silicide formation temperatures. For the w/o CIA samples with a dose of $5x10^{15}$ cm^{-2}, the effect of grain growth dominates the R_s values at the temperature range of 500-800 °C, as shown in Fig. 2-8. However, the agglomeration and phase transformation dominate the R_s values at 850 °C, as shown in Fig. 2-11(d) and 2-12, respectively. In Table 2-2, we summarize the agglomeration and phase transformation temperatures of all samples. It is clear that the agglomeration and phase transformation temperatures of the NiSi film are raised to 800 °C as the C I/I dose is equal to $1x10^{15}$ cm^{-2}. As the C I/I dose is increased to $5x10^{15}$ cm^{-2}, the agglomeration and phase transformation temperatures of the NiSi film can be further raised up to 850 °C.

Figure 2-13 shows the R_s values of the TNS samples and control2 samples as a function of annealing temperature at a constant annealing time of 30 sec. For thinner Ni-silicide films, the agglomeration mechanism plays an important role in the thermal degradation of the Ni-silicide film. Figure 2-14 and 2-15 show the plan-view SEM micrographs of the TNS samples and control2 samples, respectively. The control2 samples agglomerate at a temperature as low as 500 °C, however, the agglomeration temperature of the TNS samples keeps at 800 °C. Therefore, C atoms in Si can effectively suppress the agglomeration phenomenon of the Ni-silicide film, especially for thinner Ni-silicide films. At silicide formation temperature of 500 °C, the R_s value

of the TNS samples is higher than that of the control2 samples due to the existence of C atoms in the Ni-silicide film. During silicide formation at 600-800 °C, the R_s values of the control2 samples are much higher than those of the TNS samples because of severe agglomeration, as shown in Fig. 2-15(b), 2-15(c), and 2-15(d).

Figure 2-16 shows the measured R_s values as a function of silicide formation temperature with As I/I energy at 35 keV. The C5As35 samples have slightly higher R_s values at a lower silicide formation temperature (≦ 700 °C) owing to the larger number of C atoms within the Ni-silicide film. Figure 2-17, 2-18, and 2-19 display SEM images of the C0As35, C1As35, and C5As35 samples, respectively. The R_s values of the C0As35 samples increase from 700 °C due to the agglomeration. Many broken holes in the NiSi film can be seen in Fig. 2-17(b). On the other hand, few holes can be observed at 750 °C in the C1As35 samples, as shown in Fig. 2-18(c), and a continuous Ni-silicide film without any holes is obtained even at 800 °C in the C5As35 samples, as shown in Fig. 2-19(d). Hence, it is confirmed that sufficient C atoms can effectively suppress the agglomeration of the Ni-silicide film.

To understand the reason for the increased R_s values of the C1As35 samples at 750 °C and the C5As35 samples at 800 °C, XRD analysis was used to identify the Ni-silicide phase. The XRD spectra of the C1As35 and C5As35 samples are shown in Fig. 2-20 and 2-21, respectively. In Fig. 2-20, it is observed that the $NiSi_2$(400) phase appears at 750 °C in the C1As35 samples, and the NiSi(304) phase coexists in the Ni-silicide film at the same time. Furthermore, the NiSi(304) phase disappears, and only the $NiSi_2$(400) phase can be detected at 800 °C. In the C5As35 samples, the $NiSi_2$(400) phase does not occur until 800 °C, as shown in Fig. 2-21. According to these observations, it is clear that increasing the C I/I dose to $5x10^{15}$ cm^{-2} can retard the phase transformation of the NiSi film. In summary, performing the C I/I process

with a higher C dose of $5x10^{15}$ cm^{-2} is a feasible method for enhancing the thermal stability of the NiSi film even if As dopants exist.

Figure 2-22 shows the measured R_s values as a function of silicide formation temperature with As I/I energy at 85 keV, and the corresponding SEM images and XRD spectra are shown in Fig. 2-23 and 2-24, respectively. The information revealed from these figures is similar to that discussed previously. Moreover, the phase transformation temperature of the C0As85 samples is 750 °C while that of the C0As35 samples is 700 °C. On the basis of the experimental results of Ahmet *et al.* [14], we consider that the higher As I/I energy results in fewer As dopants within the NiSi film. Thus, the phase transformation temperature of the C0As85 samples is 50 °C higher than that of the C0As35 samples.

According to Table 2-2, it is clear that C I/I with a dose of $1x10^{15}$ cm^{-2} can raise the agglomeration and phase transformation temperatures of the Ni-silicide film to 750 °C. By increasing the C I/I dose to $5x10^{15}$ cm^{-2}, the phase transformation temperature of the Ni-silicide film can be further raised to 800 °C, and the agglomeration temperature becomes higher than 800 °C. The C I/I process successfully enhances the thermal stability of the Ni-silicide film by at least 100 °C.

2.3.2 The C PIII samples

Figure 2-25 shows the cross-sectional TEM image of the C PIII sample implanted only with C ions at 3 kV for 5 min. A-27-nm-thick implantation-induced amorphous Si layer is clearly observed. Furthermore, the 4-nm-thick diamond-like carbon (DLC) film is simultaneously deposited on the Si substrate surface during the C PIII process [15]. The input-voltage pulse waveform of the C PIII process is not a perfect square wave, which produces many low energy ions or neutral radicals during

the rising time and falling time of a square wave. While the energy of ions or neutral radicals in the CH_4 plasma environment is smaller than 100 eV, they would accumulate and deposit on the Si substrate surface to form the DLC film. The effect of the DLC layer on the formation of Ni silicide will be discussed later.

Figure 2-26 shows the measured R_s values of the C PIII samples as a function of silicide formation temperature for 30 sec. The R_s values of the C3K1M samples show abnormal high values as the silicide formation temperature is equal to or lower than 700 °C. Based on the diffraction peaks of XRD analysis at the temperature range from 500 °C to 700 °C, as shown in Fig. 2-27, it does not contain any detected Ni-silicide phase. In other words, Ni silicide can not be formed owing to the existence of the DLC film. The DLC film acts like the blocking layer between the Ni film and the Si substrate surface to stop the formation of the Ni-silicide film. Ni atoms need higher silicide formation temperature ($\geqq$ 800 °C) to break through the DLC film and react with the Si substrate. Therefore, we can observe the diffraction peaks of the $NiSi_2$ phase at the temperature range from 800 °C to 900 °C, as shown in Fig. 2-27. However, the R_s values of the C3K1M samples are still high owing to severe agglomeration, even if the Ni-silicide film is successfully formed at 800-900 °C. Figure 2-28 displays the plan-view SEM images of the C3K1M samples. $NiSi_2$ islands can be clearly observed, which cause the high R_s values at 800-900 °C, as shown in Fig. 2-28 (d) and 2-28(e). The severe agglomeration at 800 °C could be explained by insufficient C atoms at the Ni-silicide grain boundary and Ni-silicide/Si interface.

On the contrary, the R_s values of the C5K1M samples are normal at low silicide formation temperature. It represents the Ni-silicide formation is successful and not affected by the DLC film. The different experimental results of the C3K1M samples and the C5K1M samples are attributed to the thickness of the DLC film. The lower

input voltage pulse of 3 kV results in the thicker DLC film [15]. The XRD spectra of the C5K1M samples also show different patterns from those of the C3K1M samples, as shown in Fig. 2-29. Figure 2-29 indicates the NiSi film is already formed at 600 °C, and the NiSi phase transforms into the $NiSi_2$ phase at 700 °C. Figure 2-30 shows the agglomeration of the Ni-silicide film of the C5K1M samples occurs at 700 °C. It could be attributed to insufficient C atoms at the Ni-silicide grain boundary and Ni-silicide/Si interface. Although the C PIII dose may be increased by increasing the implantation time, the thickness of the DLC film is also increased to prohibit implantation.

2.4 Conclusions

In conclusion, we have investigated the effect of C I/I on the thermal stability of the NiSi film. Adding C into NiSi significantly enhances the NiSi thermal stability. Improved efficiency depends on the quantity of the C I/I dose. For the CIA samples implanted with a dose of $5x10^{15}$ cm^{-2}, the sustainable process temperature can be improved from 700 °C to 850 °C with the tradeoff of ~10 % increase of the R_s values. Furthermore, it is verified that the C I/I process, regardless of whether As dopants exist, is indeed useful for improving the thermal stability of the NiSi film at high temperatures. Our experimental results show that the agglomeration and phase transformation temperatures increase from 700-750 °C to 800 °C at least.

We also study the influence of the CPIII technology on the formation of the Ni-silicide film. The deposition of the DLC film during the C PIII process plays an important role in forming the Ni-silicide film. When the implantation voltage is equal to 3 kV, the DLC film will become a block layer between the Ni film and the Si substrate and prevent the formation of Ni silicide. Therefore, the silicide formation

temperature must be increased to 800-900 °C to form the Ni-silicide film. When the implantation voltage is increased to 5 kV, the Ni-silicide film can be normally formed at 500 °C. We find that the C3K1M and C5K1M samples exhibit poor thermal stability of NiSi due to insufficient implanted C atoms at the Ni-silicide grain boundary and Ni-silicide/Si interface. A tradeoff exists between the C PIII dose and the thickness of the DLC film. As the C PIII process is applied in the future, the impact of the DLC film must be carefully considered, or the appropriate etching technology must be developed to remove the DLC film.

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Table 2-1 Summary of substrate types, experimental splits, and their corresponding notations.

<table>
<tr><th>Notations</th><th>Substrate type</th><th>C I/I</th><th>CIA</th><th>As I/I and annealing</th><th>Ni thickness</th><th>Silicide formation</th></tr>
<tr><td>CIA</td><td rowspan="3">6-inch (100)-oriented phosphorus-doped (P-doped)</td><td>30-40 keV/ $1x10^{15}$-$5x10^{15}$ cm^{-2}</td><td>1050 °C/ 30 sec</td><td rowspan="3">----------</td><td rowspan="9">25 nm</td><td rowspan="3">500-850 °C/ 30 sec</td></tr>
<tr><td>w/o CIA</td><td>30-40 keV/ $1x10^{15}$-$5x10^{15}$ cm^{-2}</td><td>----------</td></tr>
<tr><td>control1</td><td>----------</td><td>1050 °C/ 30 sec</td></tr>
<tr><td>C5As35</td><td rowspan="10">6-inch (100)-oriented boron-doped (B-doped)</td><td rowspan="2">40 keV/ $5x10^{15}$ cm^{-2}</td><td rowspan="6">1100 °C/ 30 sec</td><td>35 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike</td><td rowspan="6">1st: 300 °C/ 1hr
2nd: 500-800 °C/ 30 sec</td></tr>
<tr><td>C5As85</td><td>85 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike</td></tr>
<tr><td>C1As35</td><td rowspan="2">40 keV/ $1x10^{15}$ cm^{-2}</td><td>35 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike</td></tr>
<tr><td>C1As85</td><td>85 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike</td></tr>
<tr><td>C0As35</td><td rowspan="2">----------</td><td>35 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike</td></tr>
<tr><td>C0As85</td><td>85 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike</td></tr>
<tr><td>TNS</td><td>7 keV/ $5x10^{15}$ cm^{-2}</td><td>1050 °C/ 30 sec</td><td rowspan="4">----------</td><td rowspan="2">10 nm</td><td rowspan="4">500-900 °C/ 30 sec</td></tr>
<tr><td>control2</td><td>----------</td><td>----------</td></tr>
<tr><td>C3K1M</td><td>3 kV/1 min</td><td rowspan="2">900 °C/ 15 sec</td><td rowspan="2">15 nm</td></tr>
<tr><td>C5K1M</td><td>5 kV/1 min</td></tr>
</table>

Table 2-2 Summary of the agglomeration and phase transformation temperatures of all samples.

Notations	C I/I condition	Agglomeration temperature (°C)	Phase transformation temperature (°C)
CIA	30 keV/1x10^{15} cm^{-2}	800	800
	40 keV/1x10^{15} cm^{-2}	800	800
	30 keV/5x10^{15} cm^{-2}	850	850
	40 keV/5x10^{15} cm^{-2}	> 850	> 850
w/o CIA	30 keV/1x10^{15} cm^{-2}	800	800
	40 keV/1x10^{15} cm^{-2}	800	800
	30 keV/5x10^{15} cm^{-2}	850	850
	40 keV/5x10^{15} cm^{-2}	850	> 850
control1	----------	700	750
C5As35	40 keV/5x10^{15} cm^{-2}	> 800	800
C5As85		> 800	800
C1As35	40 keV/1x10^{15} cm^{-2}	750	750
C1As85		750	750
C0As35	----------	700	700
C0As85		700	750
TNS	7 keV/5x10^{15} cm^{-2}	800	----------
control2	----------	500	----------
C5K1M	5 kV/1 min	700	700

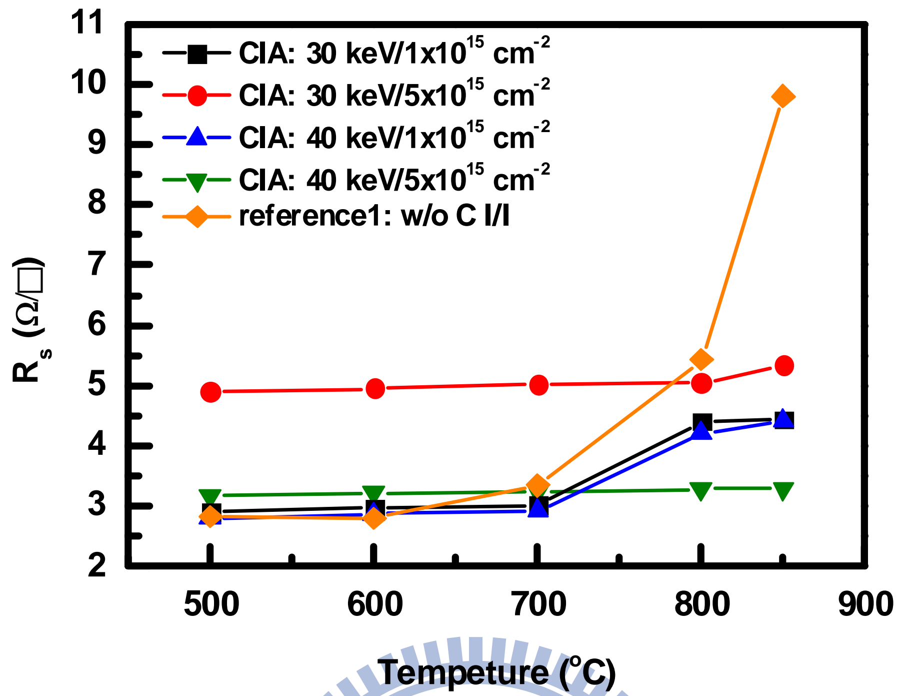

Fig. 2-1 R_s values of the CIA samples and controll samples as a function of annealing temperaure for 30 sec.

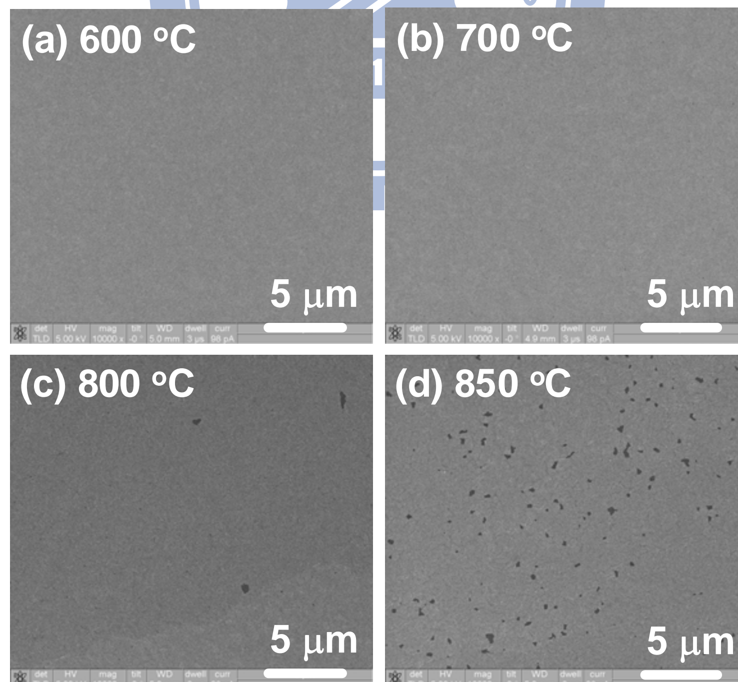

Fig. 2-2 Plan-view SEM micrographs of the CIA samples implanted at 40 keV with a dose of $1x10^{15}$ cm^{-2}: (a) 600 °C, (b) 700 °C, (c) 800 °C, and (d) 850 °C.

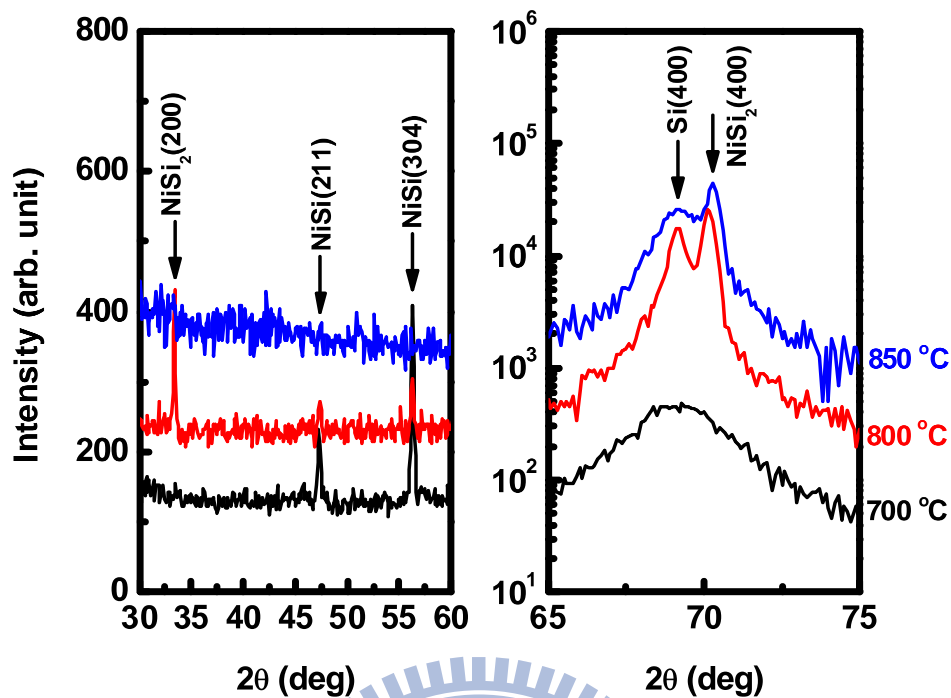

Fig. 2-3 XRD spectra of the CIA samples implanted at 40 keV with a dose of $1x10^{15}$ cm^{-2}. The silicide formation temperatures are labeled in the figure.

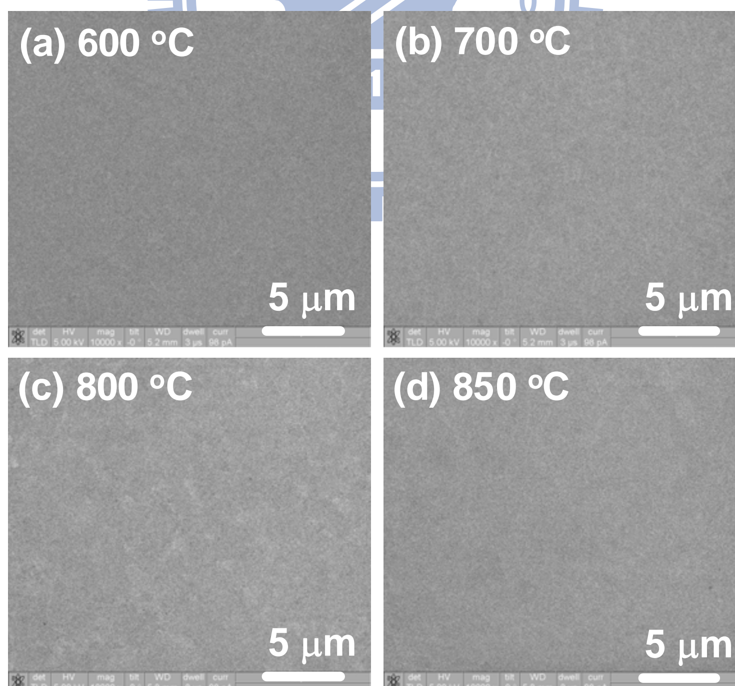

Fig. 2-4 SEM micrographs of the CIA samples implanted at 40 keV with a dose of $5x10^{15}$ cm^{-2} with different silicide formation temperatures: (a) 600 °C, (b) 700 °C, (c) 800 °C, and (d) 850 °C.

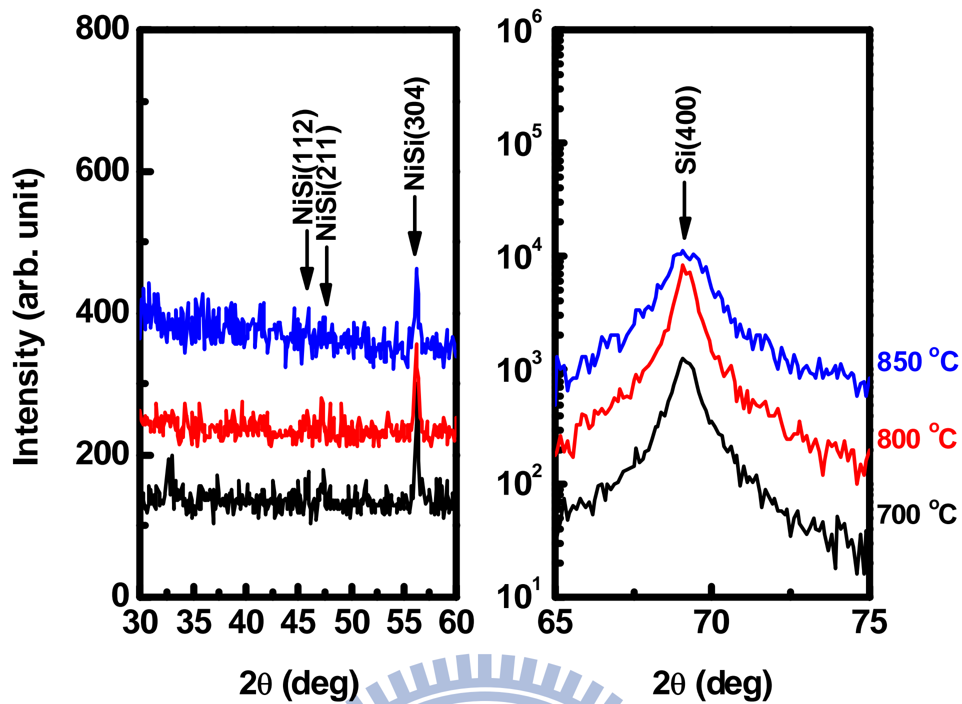

Fig. 2-5 XRD spectra of the CIA samples implanted at 40 keV with a dose of $5x10^{15}$ cm^{-2}. The silicide formation temperatures are labeled in the figure.

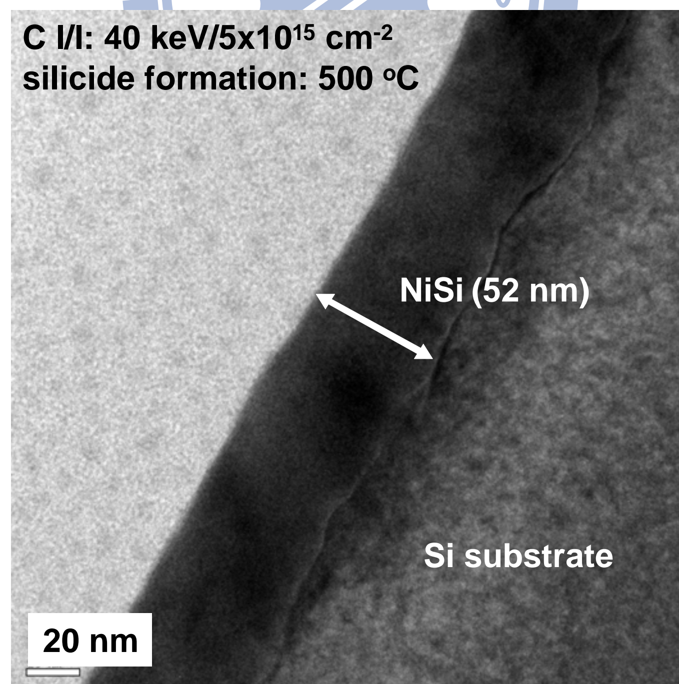

Fig. 2-6 Cross-sectional TEM image of the CIA sample implanted at 40 keV with a dose of $5x10^{15}$ cm^{-2} after silicide formation at 500 °C for 30 sec.

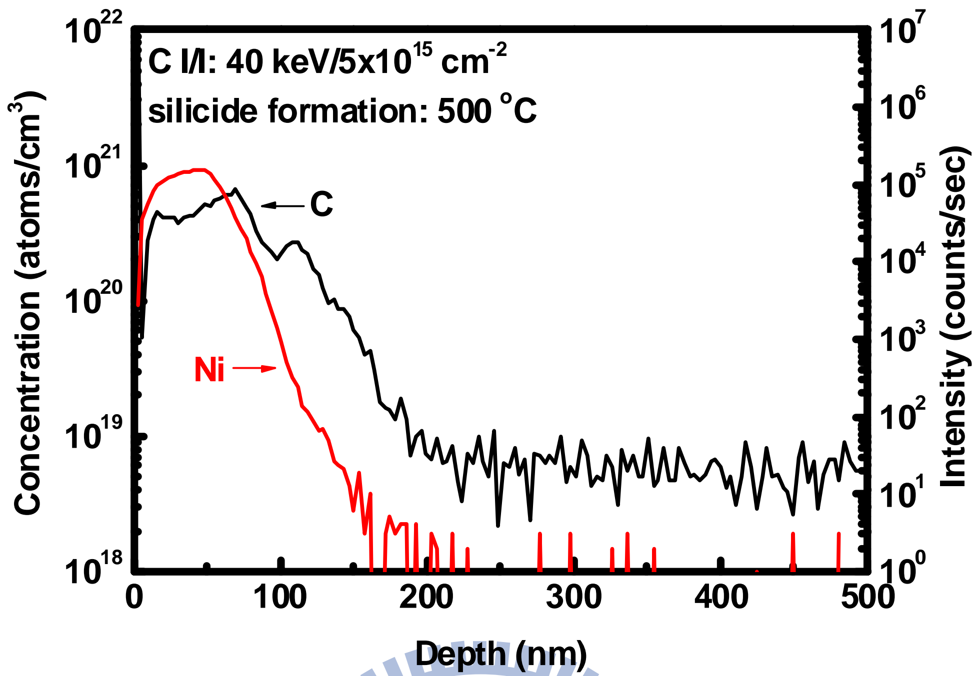

Fig. 2-7 SIMS depth profile of the CIA sample implanted at 40 keV with a dose of $5x10^{15}$ cm^{-2} after silicide formation at 500 °C for 30 sec.

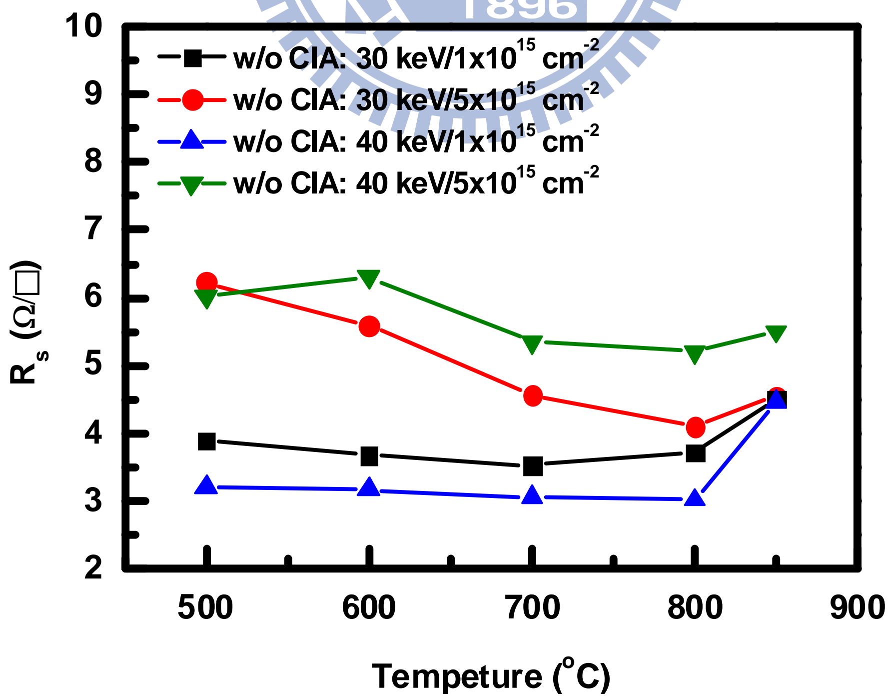

Fig. 2-8 R_s values of the w/o CIA samples as a function of annealing temperaure for 30 sec.

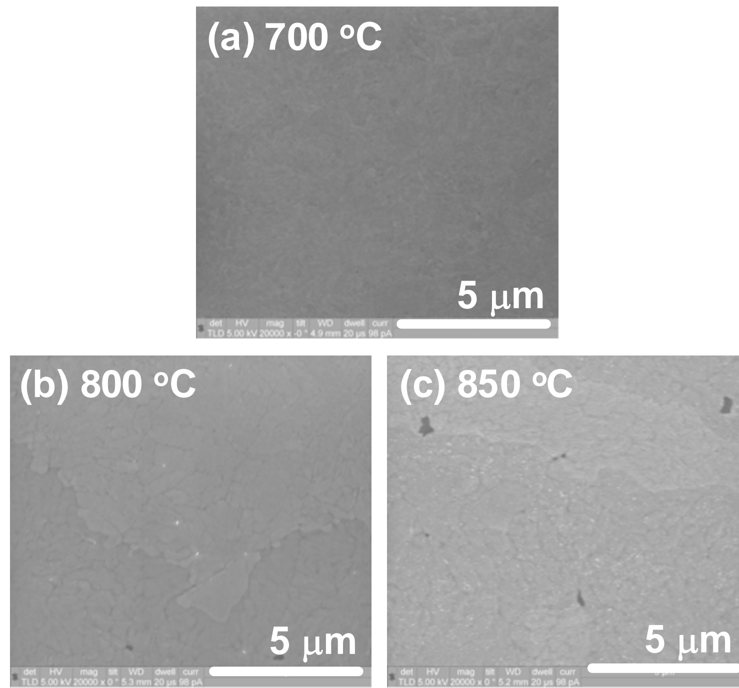

Fig. 2-9 SEM micrographs of the w/o CIA samples implanted at 30 keV with a dose of 1×10^{15} cm^{-2} with different silicide formation temperatures: (a) 700 °C, (b) 800 °C, and (c) 850 °C.

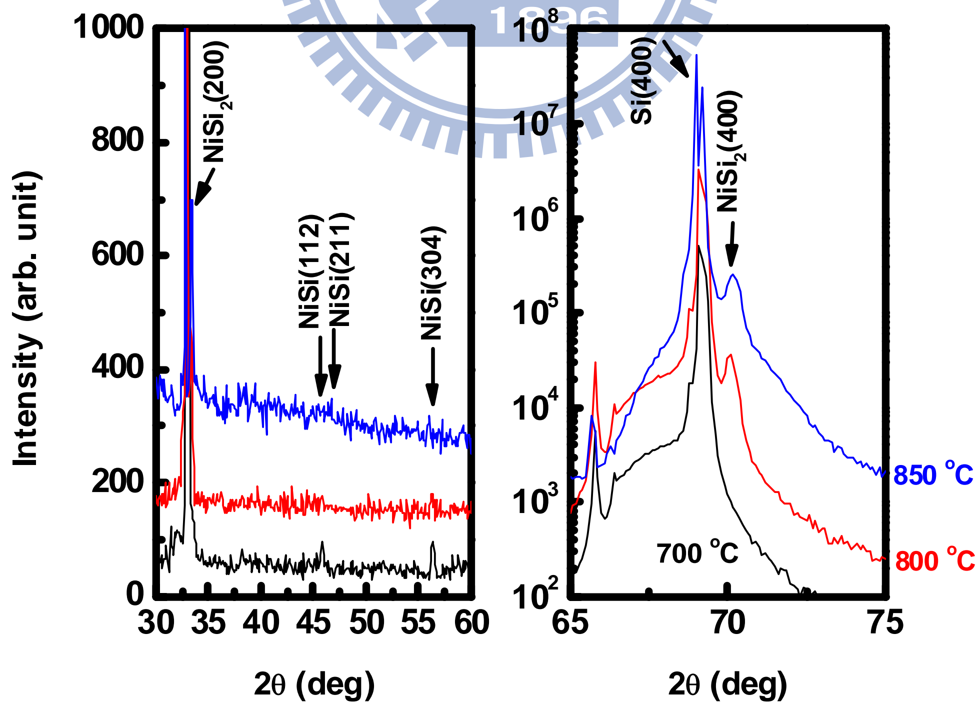

Fig. 2-10 XRD spectra of the w/o CIA samples implanted at 30 keV with a dose of 1×10^{15} cm^{-2}. The silicide formation temperatures are labeled in the figure.

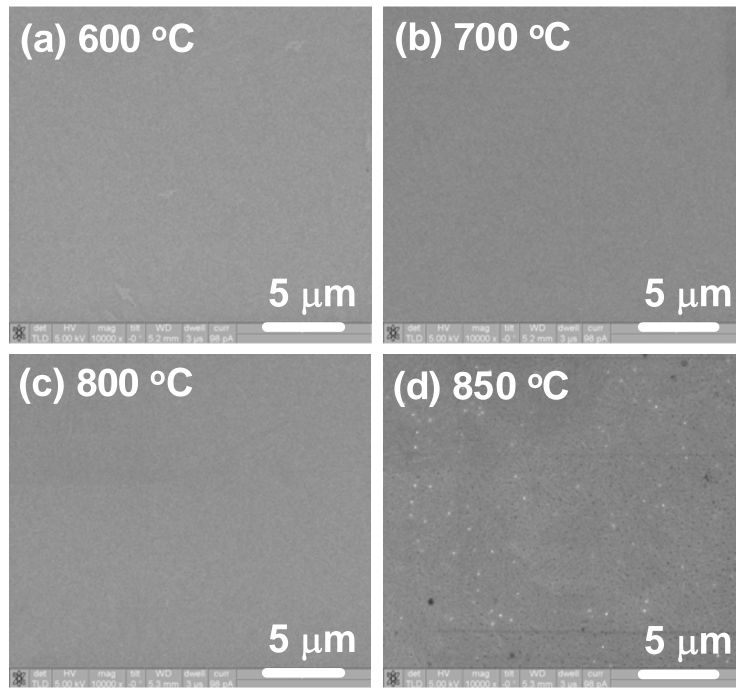

Fig. 2-11 SEM micrographs of the w/o CIA samples implanted at 30 keV with a dose of $5x10^{15}$ cm^{-2} with different silicide formation temperatures: (a) 600 °C, (b) 700 °C, (c) 800 °C, and (d) 850 °C.

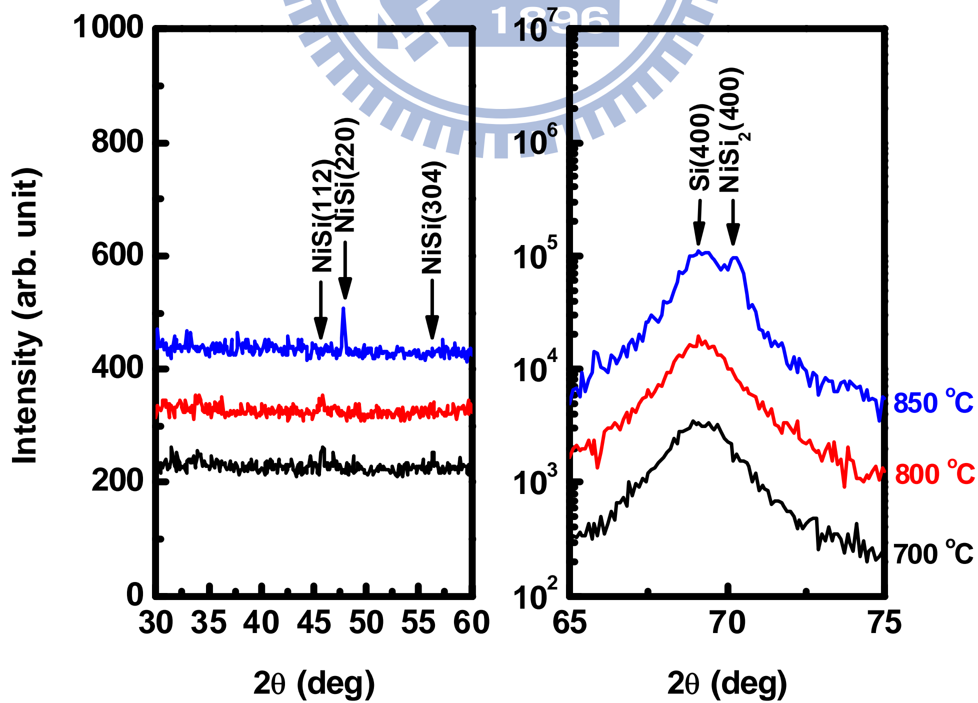

Fig. 2-12 XRD spectra of the w/o CIA samples implanted at 30 keV with a dose of $5x10^{15}$ cm^{-2}. The silicide formation temperatures are labeled in the figure.

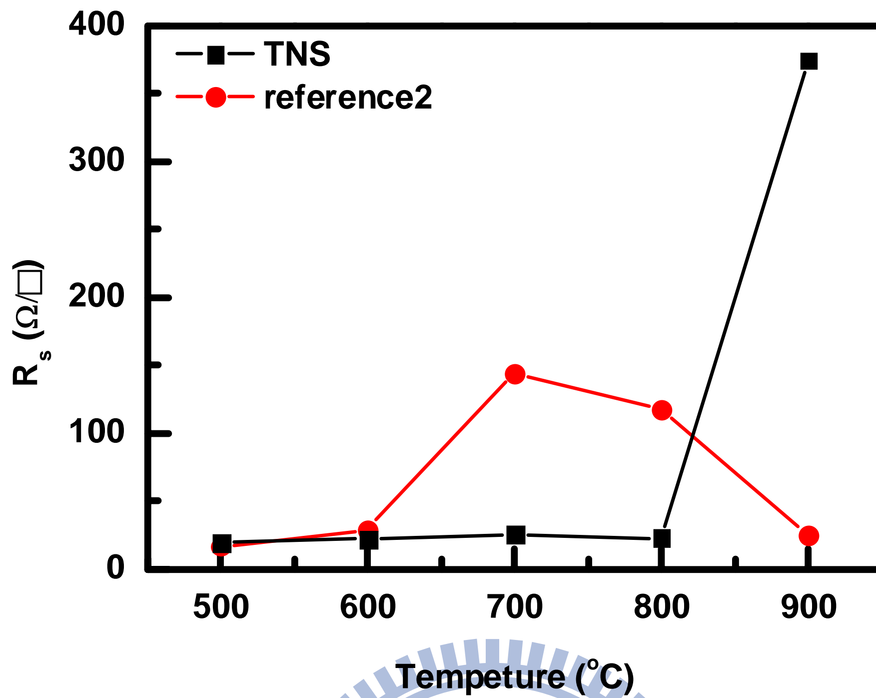

Fig. 2-13 R_s values of the TNS samples and control2 samples as a function of annealing temperaure for 30 sec.

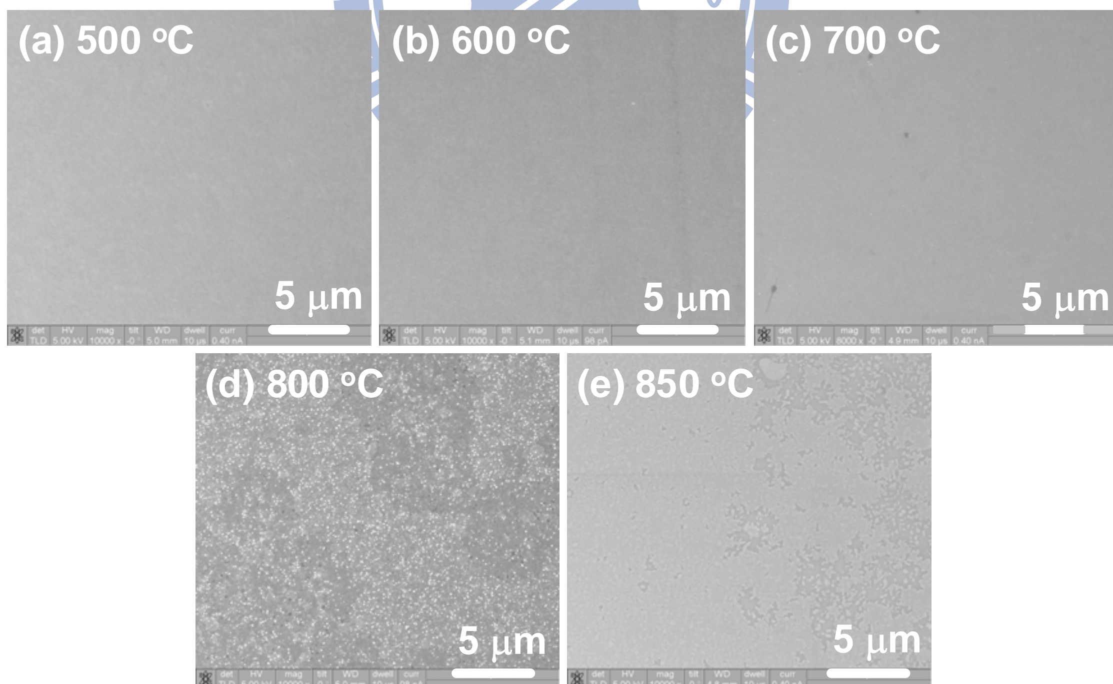

Fig. 2-14 SEM micrographs of the TNS samples implanted at 7 keV with a dose of $5x10^{15}$ cm^{-2} with different silicide formation temperatures: (a) 500 °C, (b) 600 °C, (c) 700 °C, (d) 800 °C, and (e) 850 °C.

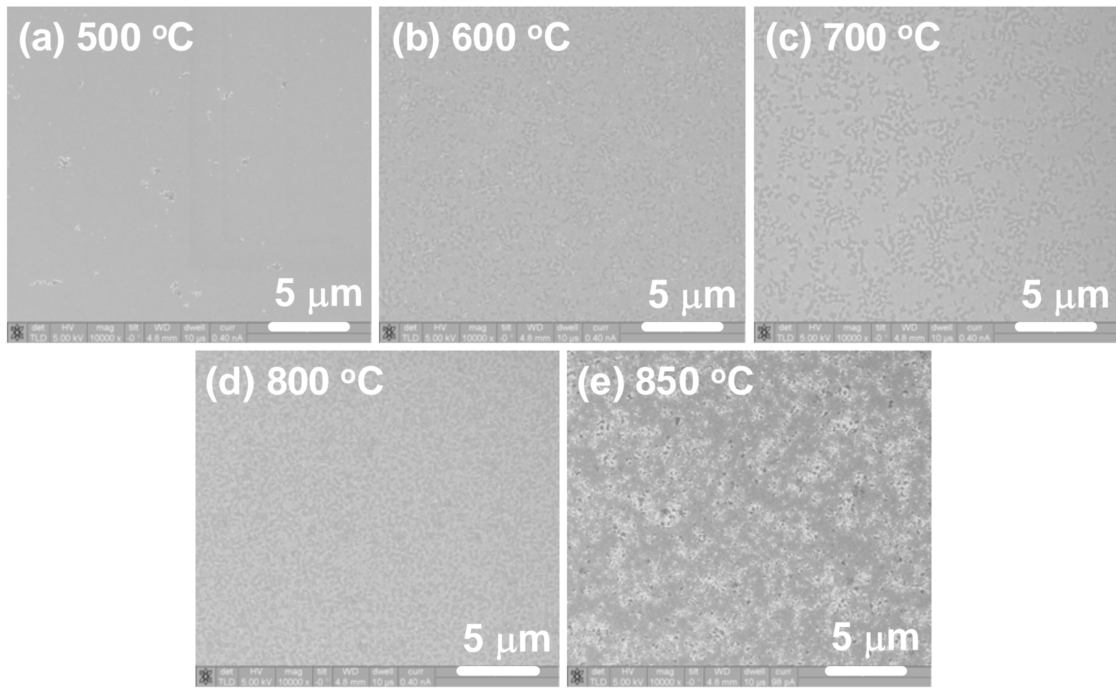

Fig. 2-15 SEM micrographs of the control2 samples with different silicide formation temperatures: (a) 500 °C, (b) 600 °C, (c) 700 °C, (d) 800 °C, and (e) 850 °C.

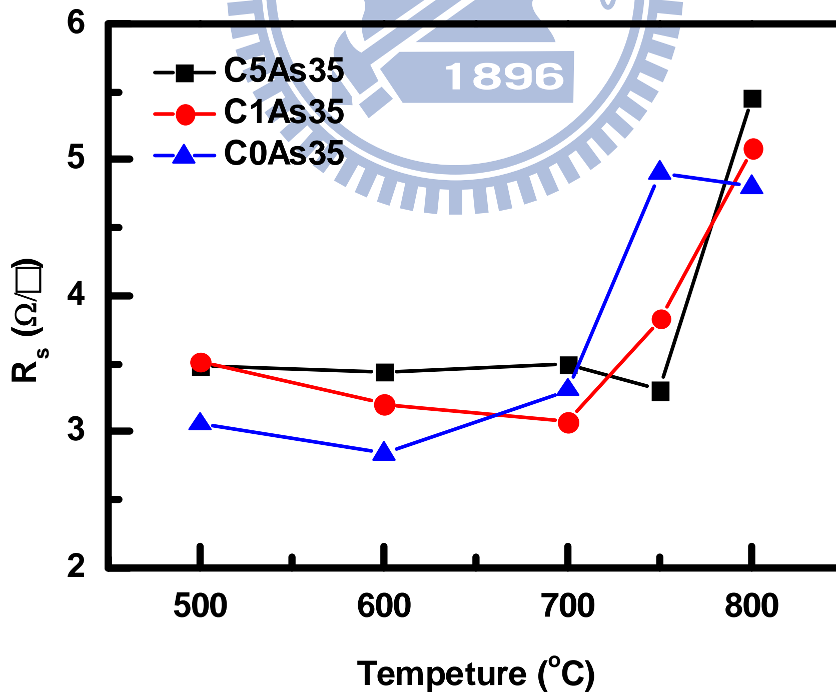

Fig. 2-16 R_s values as a function of silicide formation temperature with As I/I energy at 35 keV and different C I/I doses.

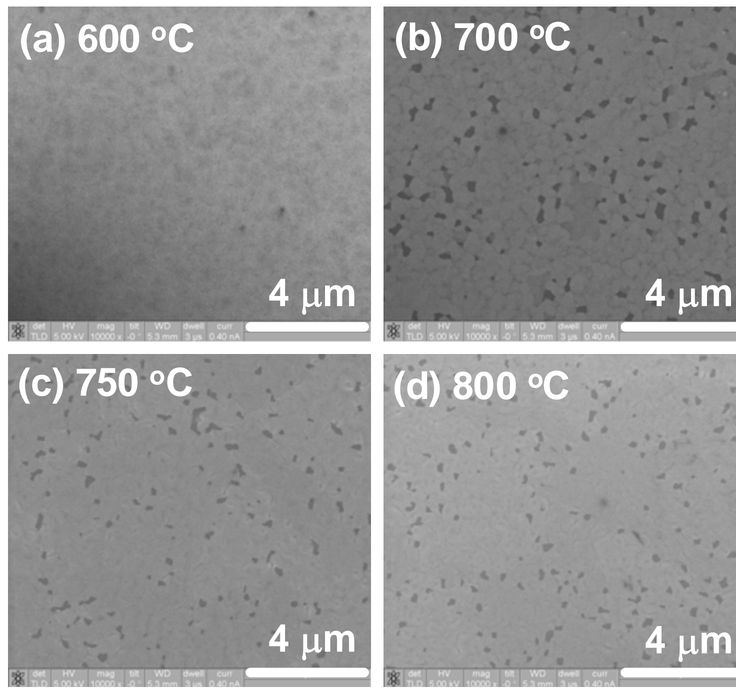

Fig. 2-17 SEM micrographs of the C0As35 samples with different silicide formation temperatures: (a) 600 °C, (b) 700 °C, (c) 750 °C, and (d) 800 °C.

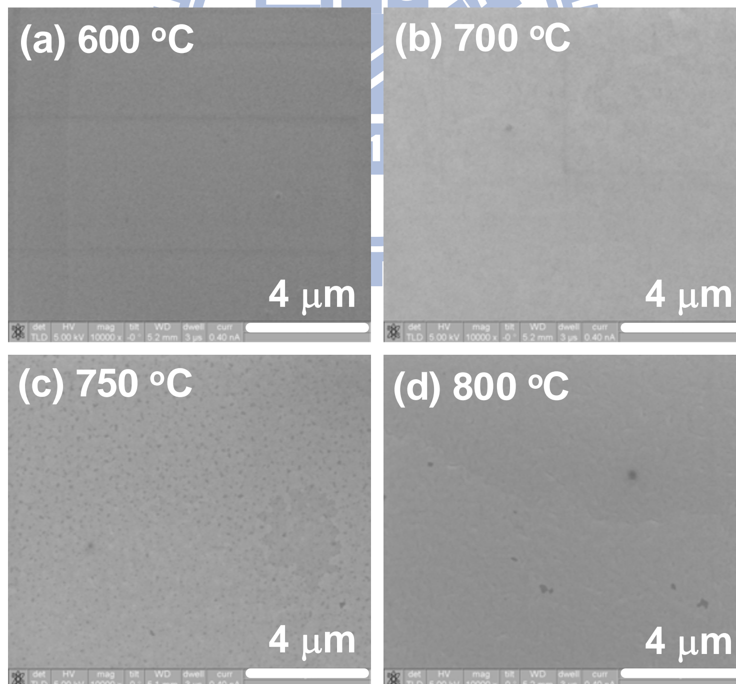

Fig. 2-18 SEM micrographs of the C1As35 samples with different silicide formation temperatures: (a) 600 °C, (b) 700 °C, (c) 750 °C, and (d) 800 °C.

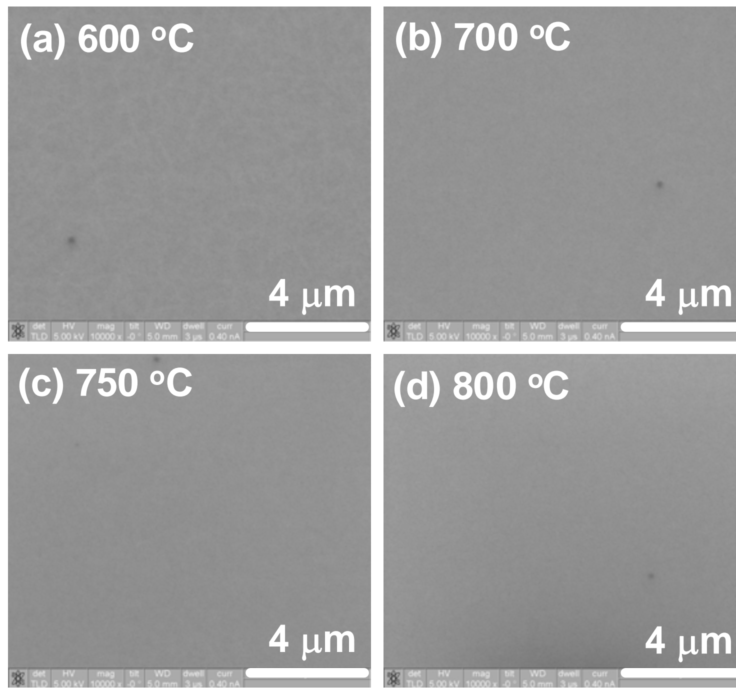

Fig. 2-19 SEM micrographs of the C5As35 samples with different silicide formation temperatures: (a) 600 °C, (b) 700 °C, (c) 750 °C, and (d) 800 °C.

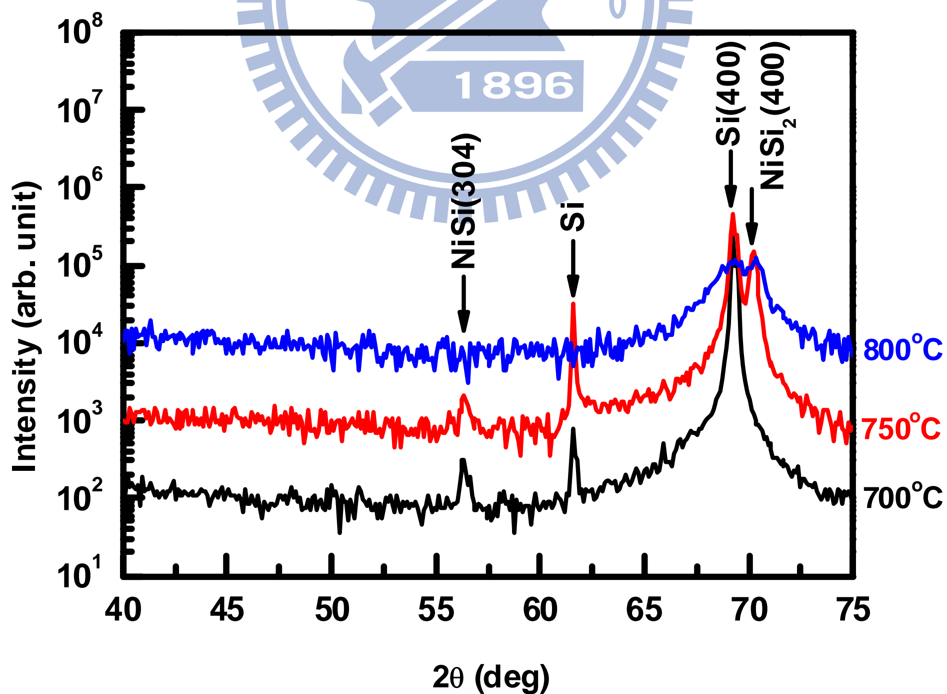

Fig. 2-20 XRD spectra of the C1As35 samples. The silicide formation temperatures are labeled in the figure.

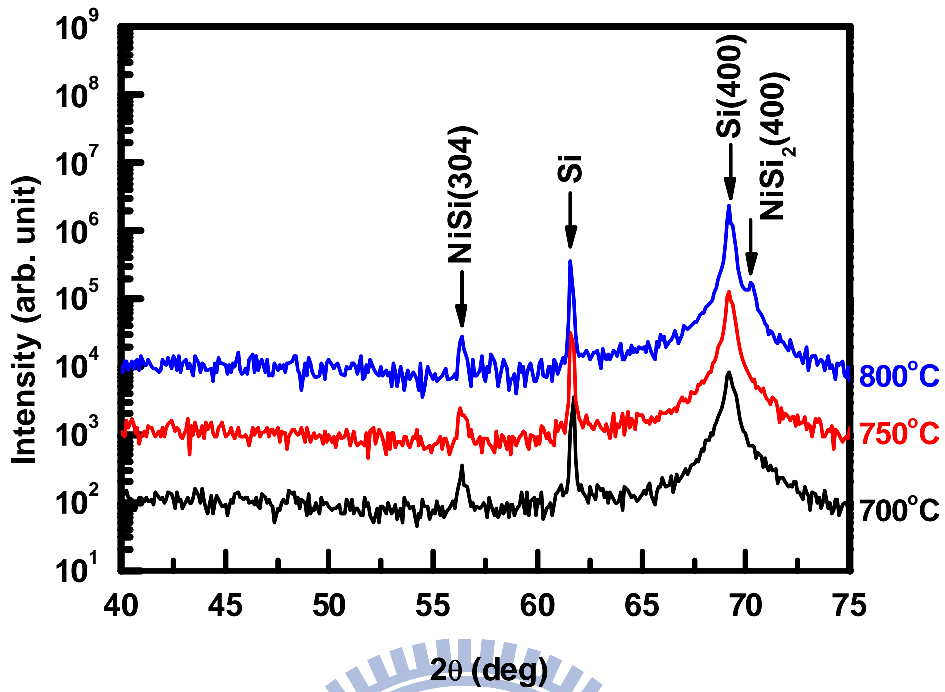

Fig. 2-21 XRD spectra of the C5As35 samples. The silicide formation temperatures are labeled in the figure.

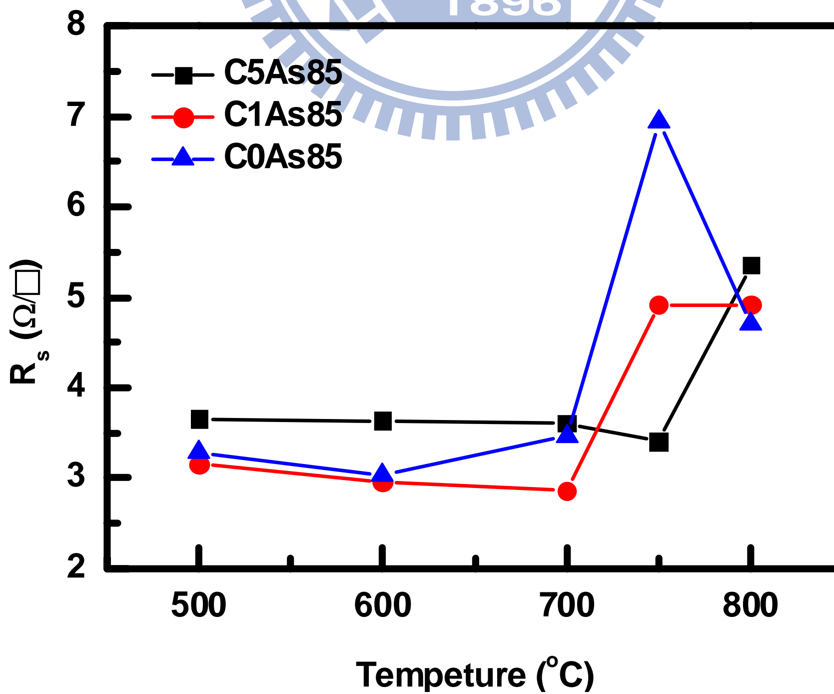

Fig. 2-22 R_s values as a function of silicide formation temperature with As I/I energy at 85 keV and different C I/I doses.

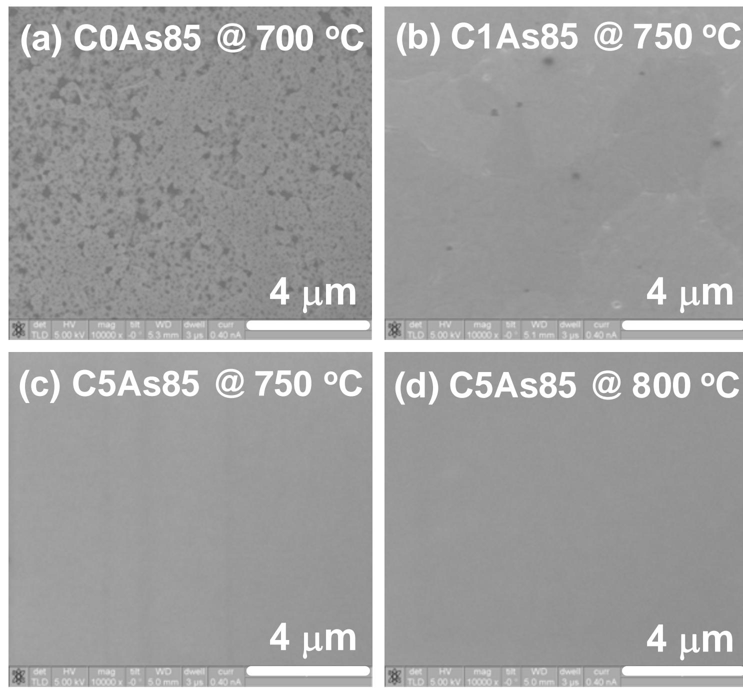

Fig. 2-23 SEM micrographs at the agglomeration temperature with As I/I energy at 85 keV and various C I/I doses: (a) C0As85 at 700 °C, (b) C1As85 at 750 °C, (c) C5As85 at 750 °C, and (d) C5As85 at 800 °C.

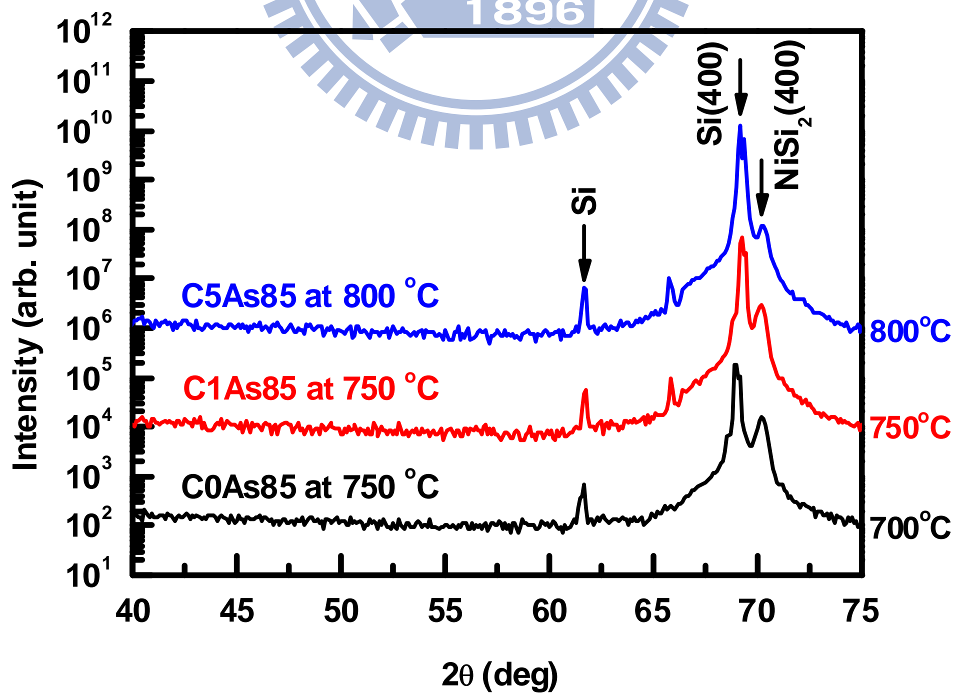

Fig. 2-24 XRD spectra at the phase transformation temperature with As I/I energy at 85 keV and various C I/I doses.

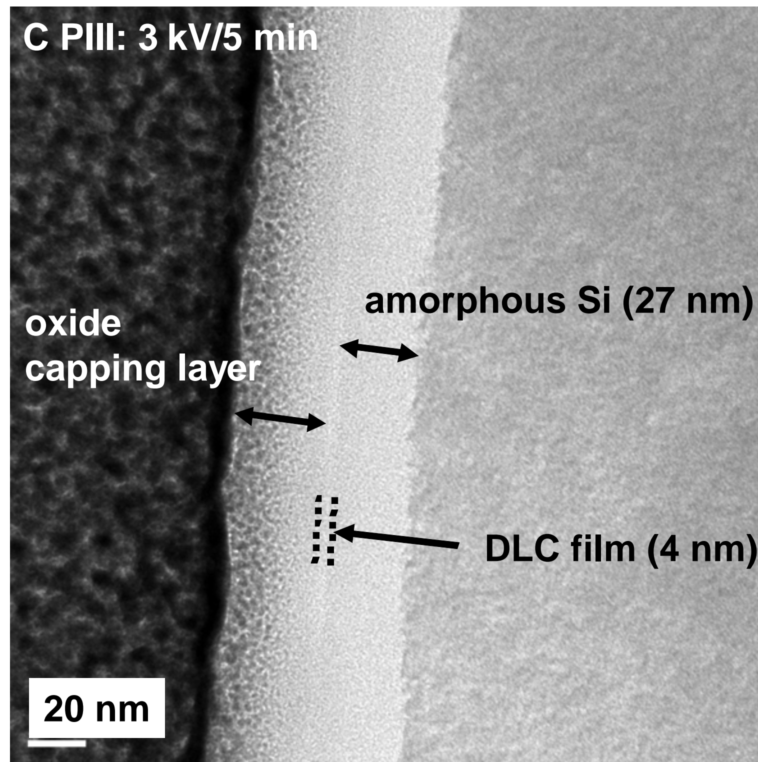

Fig. 2-25 Cross-sectional TEM image of the C PIII sample implanted at 3 kV for 5 min.

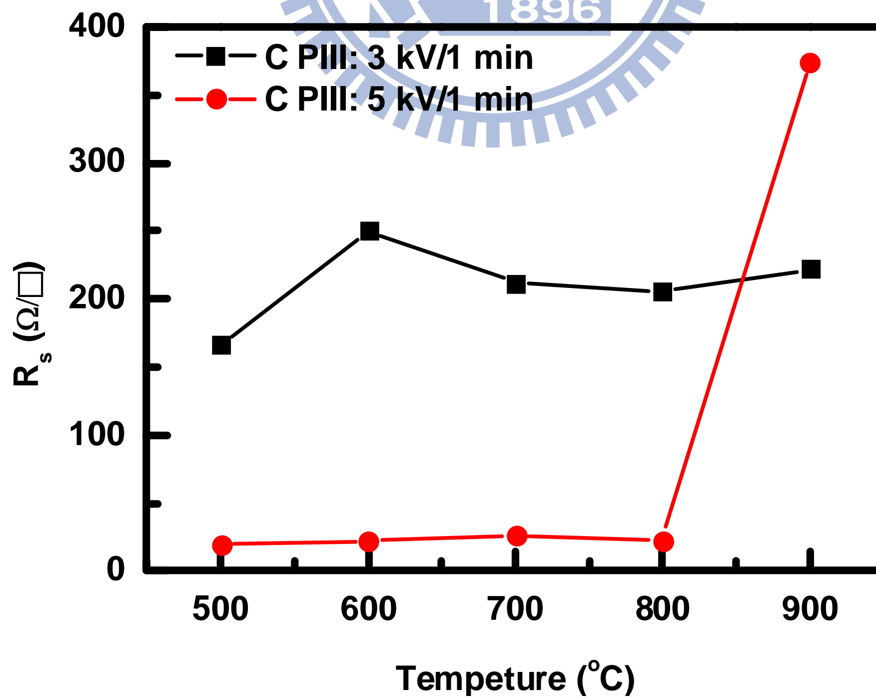

Fig. 2-26 R_s values of the C3K1M and C5K1M samples as a function of annealing temperaure for 30 sec.

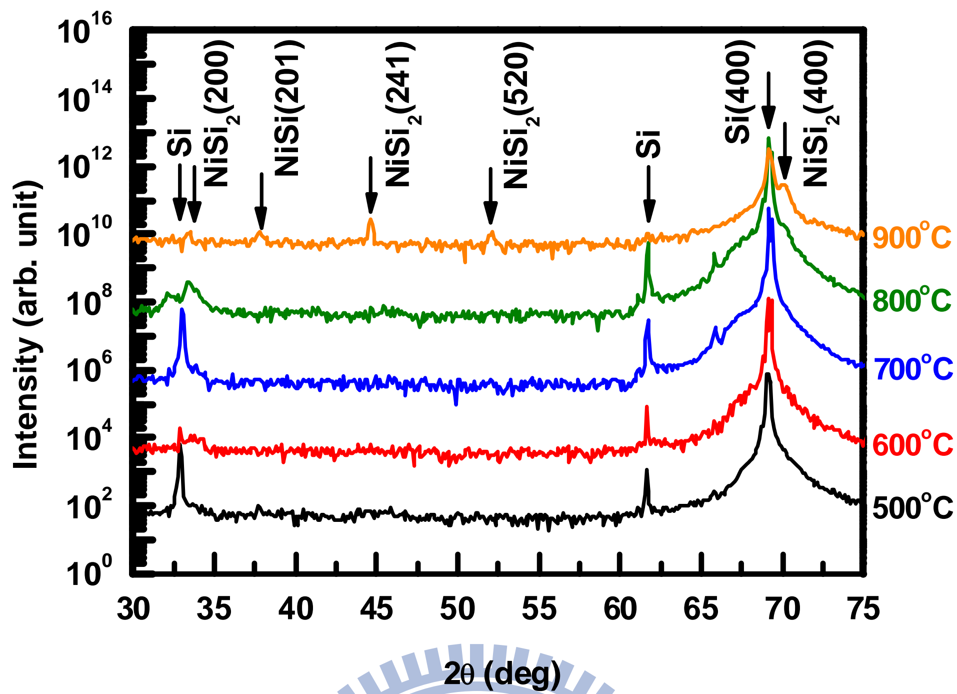

Fig. 2-27 XRD spectra of the C3K1M samples. The silicide formation temperatures are labeled in the figure.

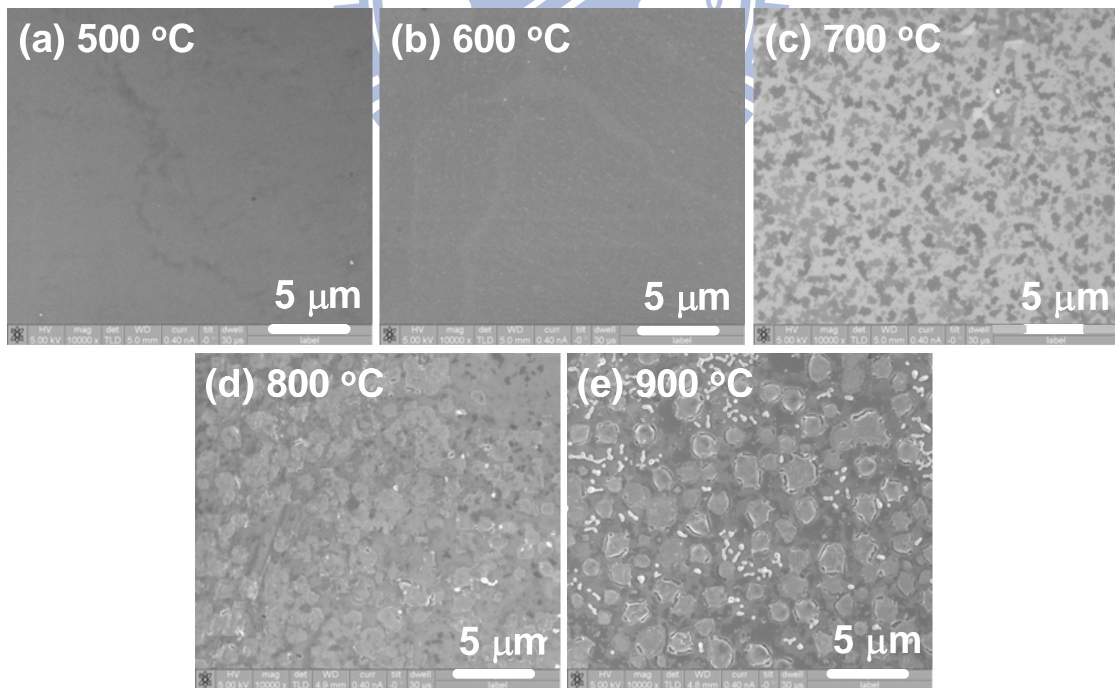

Fig. 2-28 SEM micrographs of the C3K1M samples with different silicide formation temperatures: (a) 500 °C, (b) 600 °C, (c) 700 °C, (d) 800 °C, and (e) 900 °C.

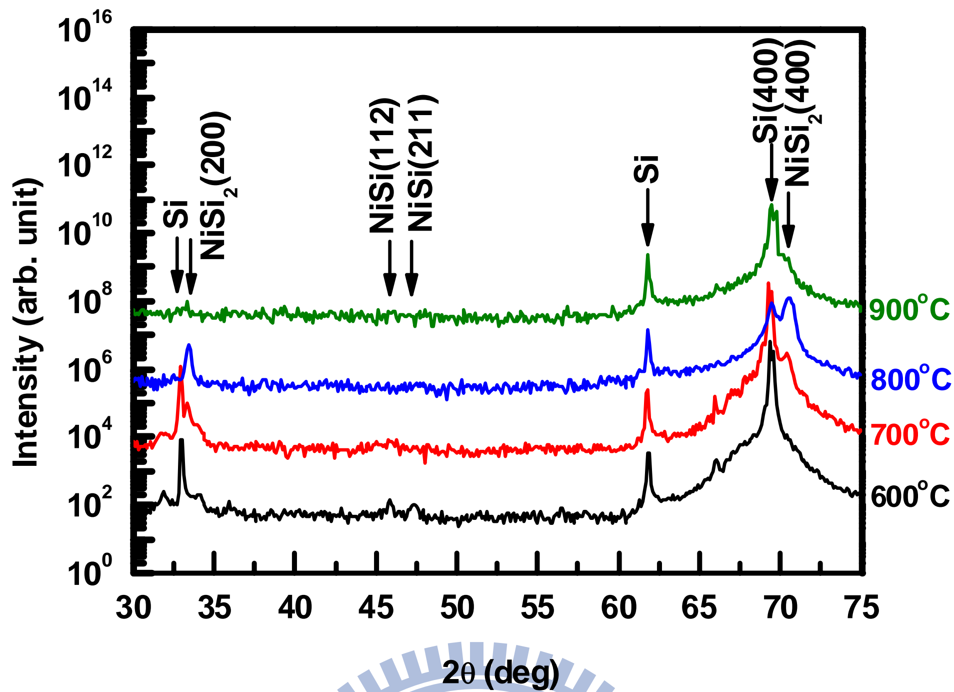

Fig. 2-29 XRD spectra of the C5K1M samples. The silicide formation temperatures are labeled in the figure.

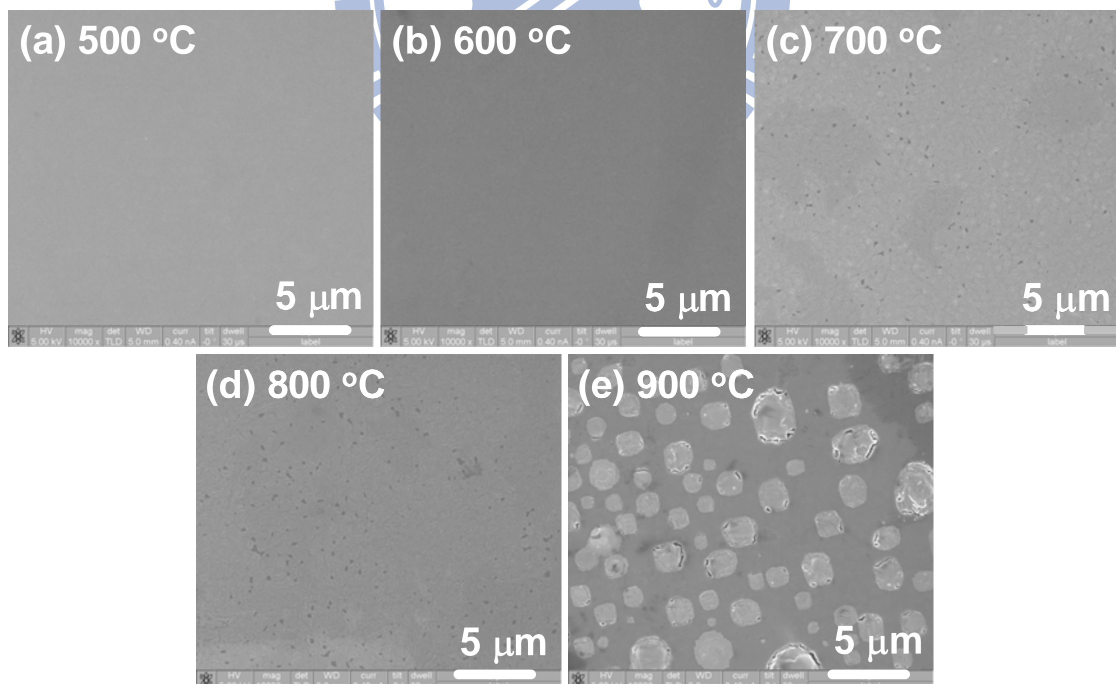

Fig. 2-30 SEM micrographs of the C5K1M samples with different silicide formation temperatures: (a) 500 °C, (b) 600 °C, (c) 700 °C, (d) 800 °C, and (e) 900 °C.

Chapter 3

Electrical Characteristics of Nickel-Silicide-Contacted Junctions with Carbon Ion Implantation

3.1 Introduction

For sub-100-nm technology nodes, a self-aligned Ni silicide technology is useful to reduce the S/D parasitic resistance in MOSFETs owing to several advantages [1]. The scaling of the junction depth is essential to control the SCE of MOSFETs. Therefore, the relatively thin silicide S/D contacts having good high-temperature stability are required for ultra-shallow S/D junctions. In chapter 2, we have demonstrated that the thermal stability of the NiSi/Si structure can be improved by high-dose C I/I. In the past, the advantages and disadvantages of C atoms in Si were extensively researched. Many studies focused on ultra-shallow junction formation by co-implanting C ions into the Si substrate [2-5]. Carbon atoms can act as traps and capture Si self-interstitials to form C-Si complexes, and ultra-shallow junctions are achieved by eliminating the interstitial-assisted dopant diffusion. However, the corresponding junction characteristics were not reported in these papers. Only a few papers reported the C-doped pn junction characteristics [6-8]. S. Lombardo *et al.* found that C-Si complexes belonged to neutral scattering centers and recombination-generation centers in the Si band gap. In addition, an interstitial C

atom is another deep-level center in Si [8]. Once the C-Si complexes and interstitial C atoms locate within the junction depletion region, the C-doped junction characteristics deviate from the ideal characteristics [6, 8]. C. F. Tan *et al.* reported that doping C atoms into Si can reduce junction leakage owing to the elimination of secondary defects [7]. Therefore, C atoms in Si have strong effects on the electrical characteristics of ultra-shallow junctions.

The impact of the C I/I process on the current-voltage (I-V) characteristics of the Ni-silicide-contacted Schottky junctions has not been previously reported and will be discussed later in this chapter. Moreover, the I-V characteristics of the Ni-silicide-contacted n^+/p shallow junctions have not been studied in detail. In this chapter, we demonstrate and discuss the trade-off between the thermal stability of the NiSi film and the I-V characteristics of the Ni-silicide-contacted n^+/p shallow junction. Some methods of fabricating the Ni-silicide-contacted n^+/p shallow junctions with both good thermal stability and excellent I-V characteristics are proposed.

3.2 Junction Fabrication

The C-doping effects on the electrical characteristics of the Ni-silicide-contacted Schottky and n^+/p shallow junctions are both investigated in this study. N-type and p-type (100)-oriented Si prime wafers were used for the Schottky and n^+/p shallow junctions, respectively. After typical local-oxidation-of-silicon (LOCOS) isolation, a 70-nm-thick screen oxide layer was thermally grown. Next, C ions were implanted through the screen oxide at 40 keV to a dose of $1x10^{15}$ cm^{-2} or $5x10^{15}$ cm^{-2}. The projected ion range of C ions is 58.7 nm under the Si substrate surface, which is slightly deeper than the final NiSi/Si interface. Then, the C I/I defects were eliminated by an RTA in N_2 ambient at 1050 °C (Schottky junctions) or 1100 °C (n^+/p shallow

junctions) for 30 sec. Junctions without C I/I were also prepared as reference. After etching the screen oxide by DHF solution, for the n^+/p shallow junctions, As ions were implanted at 35 keV or 85 keV to a dose of $5x10^{15}$ cm^{-2} followed by a 1050 °C spike annealing process in N_2 ambient. The lower As I/I energy of 35 keV results in more dopants within the Ni-silicide film and a shallower junction depth. After removing the native oxide by DHF solution, a 25-nm-thick Ni layer and a 5-nm-thick TiN capping layer were sequentially deposited on all junctions by a sputtering system followed by a one-step (Schottky junctions) or two-step (n^+/p shallow junctions) annealing process to form Ni silicide [9]. The one-step annealing process was performed at 500 °C for 30 sec. The first annealing step of the two-step annealing process was performed at 300 °C for 60 min. After that, the TiN capping layer and unreacted Ni of all junctions were selectively removed by using piranha solution (H_2SO_4:H_2O_2= 3:1). The second annealing step was performed at the temperature range of 500-800 °C for 30 sec. Finally, a 500-nm-thick Al layer was deposited on the wafer backside by a sputtering system to complete the fabrication of all junctions. The main process flow of the Ni-silicide-contacted n^+/p shallow junctions is illustrated in Fig. 3-1. The notations used to identify different junctions along with their fabrication conditions are summarized in Table 3-1. The I-V characteristics of the Ni-silicide-contacted Schottky and n^+/p shallow junctions were measured by a precision semiconductor parameter analyzer of model Agilent 4156C.

3.3 Results and Discussion

Typical I-V characteristics of the pure and C I/I Schottky junctions are shown in Fig. 3-2. It is clearly observed that both of the junction forward and reverse currents increase with an increase in the C I/I dose. The measurement results imply the

Schottky barrier height (SBH) of the NiSi/n-type Si interface gradually decreases with an increase in the C I/I dose. Due to the low substrate doping concentration (~1×10^{15} cm^{-3}) and high SBH, the forward I-V characteristics of the pure Schottky junction obey the thermionic model. Hence, the extracted SBH of the pure Schottky junction is 0.66 eV by using the conventional forward I-V method [10].

For the C I/I Schottky junctions, even if the depletion width at lower reverse-bias voltages (0 V > V_R > -1 V) greatly exceeds the distribution range of C atoms, the reverse-bias currents still increase exponentially. Therefore, the increased reverse-bias currents are not the thermal generation currents via the C-related deep levels. In addition, the forward-bias ideality factors (n) deviate from the unity. We consider that the measured currents of the C I/I Schottky junctions are composed of the thermionic emission and tunneling currents. The conventional forward I-V method does not take into account the tunneling mechanism. Hence, it is not suitable for SBH extraction. By considering the thermionic-field emission (TFE) model combined with the image force barrier lowering and series resistance effects, a new procedure to extract the SBH has recently been proposed [11]. After setting the doping concentration and SBH, the theoretical reverse I-V characteristics are calculated in MATLAB. The doping concentration and actual SBH can be estimated by comparing the theoretical and measured reverse I-V curves. As the C I/I dose is equal to 1×10^{15} cm^{-2}, the doping concentration and actual SBH at the NiSi/n-type interface are 8.97×10^{16} cm^{-3} and 0.599 eV, respectively. When the C I/I dose is increased to 5×10^{15} cm^{-2}, the doping concentration is raised to 1.65×10^{17} cm^{-3} and actual SBH is reduced to 0.484 eV. The increased doping concentration and image force lowering of the barrier could be attributed to the n-type doping effect of C atoms [6].

Figure 3-3 shows the I-V characteristics of the Ni-silicide-contacted n^+/p shallow junction with As I/I energy at 35 keV. The junction area is 6.25×10^{-4} cm^2. Both the C1As35 and C5As35 junctions exhibit the lowest leakage current at the silicide formation temperature of 500 °C. The lowest leakage value is approximately 10 nA/cm^2 at a reverse bias of 3 V, and this value is close to that of the junction without silicide. For the C0As35 and C1As35 junctions, the leakage current increases with increasing silicide formation temperature. However, the junctions with a C I/I dose of 5×10^{15} cm^{-2} exhibit very different reverse leakage current behavior. For the C5As35 junctions, when the silicide formation temperature increases to 600 °C, the leakage current abruptly increases by 3 orders of magnitude. Then, the leakage current decreases as the silicide formation temperature increases to 700 °C and 750 °C, but increases again as the silicide formation temperature increases to 800 °C. Figure 3-4 and 3-5 show statistics of the junction leakage current at a reverse bias of 3 V for the Ni-silicide-contacted n^+/p shallow junctions with As I/I at 35 and 85 keV, respectively. The silicide formation temperature dependences of the junction leakage current described above are confirmed to be universal behavior. The same leakage current dependence on the silicide formation temperature and C I/I dose can also be found at an As I/I energy of 85 keV, as shown in Fig. 3-5.

It has been reported that the formation of Ni-silicide spikes penetrating into the Si substrate can cause a severe leakage problem [12]. In this work, three mechanisms are considered to have an effect on the junction leakage current. The first one is the agglomeration of the Ni-silicide film. Agglomeration causes an increase in interface roughness at the Ni-silicide/Si contact, and the junction leakage current may increase owing to structural damage. The second is the diffusion of Ni atoms. The many defects produced by the high-dose I/I process form the diffusion path. Ni atoms can

rapidly diffuse via these defects during silicide formation. As Ni atoms diffuse toward the junction depletion region and form deep levels, the junction leakage current increases. The third is the phase transformation from the NiSi phase to the $NiSi_2$ phase. When the phase transformation occurs, the thickness of the silicide film becomes double that of the NiSi film. Thus, the Ni-silicide/Si interface becomes closer to the junction depletion region. Agglomeration can easily damage the junction depletion region, and more Ni atoms can arrive at the junction depletion region to contribute to the junction leakage current. Agglomeration and the phase transformation occur at a high silicide formation temperature and depend on the silicide formation temperature and C I/I dose. The agglomeration and phase transformation temperatures of all junctions have been studied in chapter 2 and summarized in Table 2-2. In addition to the silicide formation temperature, the effect of the diffusion of Ni atoms is also related to the number of I/I defects, which depends on the C I/I dose.

For the reasons mentioned above, the deeper junction has fewer Ni atoms within the junction depletion region. Moreover, the agglomeration and phase transformation also have less impact on the deeper junction. Hence, by comparing Fig. 3-4 and 3-5, it can be seen that the leakage current at an As I/I energy of 85 keV is much lower than that at 35 keV at a high silicide formation temperature.

When the C I/I dose is zero or equal to $1x10^{15}$ cm^{-2}, the number of defects is not large enough to form a long diffusion path for Ni atoms. Fewer Ni atoms can arrive at the junction depletion region. Hence, the agglomeration and phase transformation dominate the junction leakage current mechanism, and the junction leakage current increases with silicide formation temperature. Because the C1As35 and C1As85 junctions have better thermal stability of the Ni-silicide film, both junctions exhibit a

lower leakage current than the C0As35 and C0As85 junctions with silicide formation temperatures of 700 °C and 750 °C.

On the other hand, when the C I/I dose increases to 5×10^{15} cm^{-2}, it generates many remnant defects, and Ni atoms can diffuse very rapidly via these defects. Therefore, the diffusion of Ni atoms dominates the junction leakage current mechanism. The leakage currents of the C5As35 and C5As85 junctions are similar to that of the C0As35 junction at 500 °C, as can be observed by comparing Fig. 3-4 and 3-5. This indicates that most of the defects generated by a high C I/I dose were annihilated by RTA at 1100 °C for 30 sec. Figure 3-6(a) and 3-6(b) show the SIMS depth profiles of C, As, and Ni atoms of the C5As85 and C0As85 samples with the silicide formation temperature at 600 °C, respectively. The different surface NiSi thicknesses of these two junctions is due to the thickness variation of the as-deposited Ni films. Hence, all of the depth profiles were measured from the NiSi/Si interface, which is defined as the intersection of the Ni and As depth profiles. Rucker *et al.* reported that substitutional C atoms can enhance As dopant diffusion, but the diffusion enhancement effect ends when most of the C atoms precipitate [13]. In the case of our C5As85 samples, C atoms were incorporated by I/I, and this process produced a large number of Si interstitials. It is well known that C atoms can trap Si interstitials to eliminate secondary defects during high-temperature annealing [14]. Hence, C atoms combine with Si interstitials and precipitate to form immobile clusters during high-temperature annealing. Compared with the epitaxial Si:C layer in Rucker *et al.*'s experiment, most of the C atoms are not located at substitutional sites in our C5As85 samples. Therefore, no As diffusion enhancement is observed upon comparing Fig. 3-6(a) with Fig. 3-6(b). It is observed that the Ni depth profile of the C5As85 sample has an apparent hump whose position coincides with the peak of the

C depth profile. The distance between As and Ni atom depth profiles measured at an As atom concentration of $1x10^{18}$ cm^{-3} is indicated in Fig. 3-6(a) and 3-6(b). The Ni distribution of the C5As85 sample is about 15 nm closer to the n^+/p junction than that of the C0As85 sample. This implies that the C5As85 junction has more Ni atoms within the junction depletion region owing to the dissolution and diffusion of Ni atoms toward the junction depletion region along the many defects induced by C I/I with a dose of $5x10^{15}$ cm^{-2} during silicide formation. This explains why the C5As35 and C5As85 junctions unexpectedly exhibit the highest leakage current at 600 °C. We consider that the Ni-silicide formation process can generate more and more vacancies injecting into the Si substrate at a higher temperature [15]. Some residual defects can be combined and removed by these vacancies, so that fewer Ni atoms can diffuse into the junction depletion region. Therefore, the junction leakage current decreases as the silicide formation temperature increases to 700 °C and 750 °C. Finally, the increase in the leakage current again at 800 °C is a result of the agglomeration and phase transformation of the Ni-silicide film.

To suppress the diffusion of Ni atoms, we propose two solutions. One method is to ensure that the C distribution is shallower than the junction depletion region by introducing a lower C I/I energy. Thus, a higher concentration of C atoms near the Si substrate surface can be obtained. We predict that this will further enhance the thermal stability of the Ni-silicide film. Furthermore, defects are far away from the junction, thus reducing the leakage current. The other method is to eliminate the defects as completely as possible. Raising the thermal budget of RTA or developing other annealing processes is a feasible solution to eliminate these defects.

3.4 Conclusions

We have investigated the impact of C I/I on the Ni-silicide-contacted Schottky and n^+/p shallow junctions for the first time. The incorporation of C is Si could lower the SBH of the Ni-silicide-contacted Schottky junction owing to the n-type doping effect of C atoms. The leakage current mechanisms of the Ni-silicide-contacted n^+/p shallow junctions are also explained in detail in this chapter. Good thermal stability of the Ni-silicide film and better junction I-V characteristics cannot be obtained at the same time. A higher C I/I dose of $5x10^{15}$ cm^{-2} causes numerous defects, and Ni atoms diffuse very rapidly along these defects into the junction depletion region. Therefore, the leakage current suddenly increases owing to the existence of deep levels, i.e., Ni atoms.

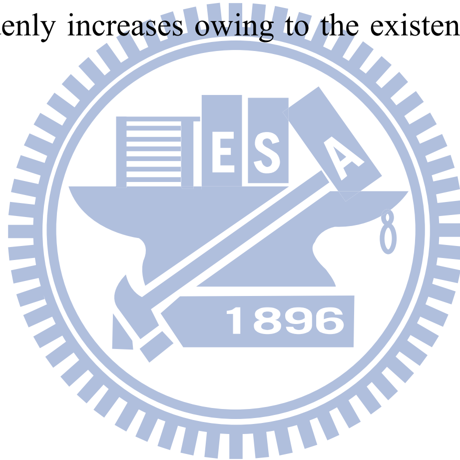

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Table 3-1 Notations and fabrication conditions of the Ni-silicide-contacted Schottky and n^+/p shallow junctions.

Notations	**C I/I**	**CIA**	**As I/I and annealing**	**Ni thickness**	**Silicide formation**
C I/I	40 keV/ $1x10^{15}$-$5x10^{15}$ cm^{-2}	1050 °C/30 sec	----------	25 nm	500 °C/ 30 sec
pure	----------				
C5As35	40 keV/ $5x10^{15}$ cm^{-2}	1100 °C/30 sec	35 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike		1st: 300 °C/1 hr 2nd: 500-800 °C/ 30 sec
C5As85			85 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike		
C1As35	40 keV/ $1x10^{15}$ cm^{-2}		35 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike		
C1As85			85 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike		
C0As35	----------		35 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike		
C0As85			85 keV/ $5x10^{15}$ cm^{-2} 1050 °C/spike		

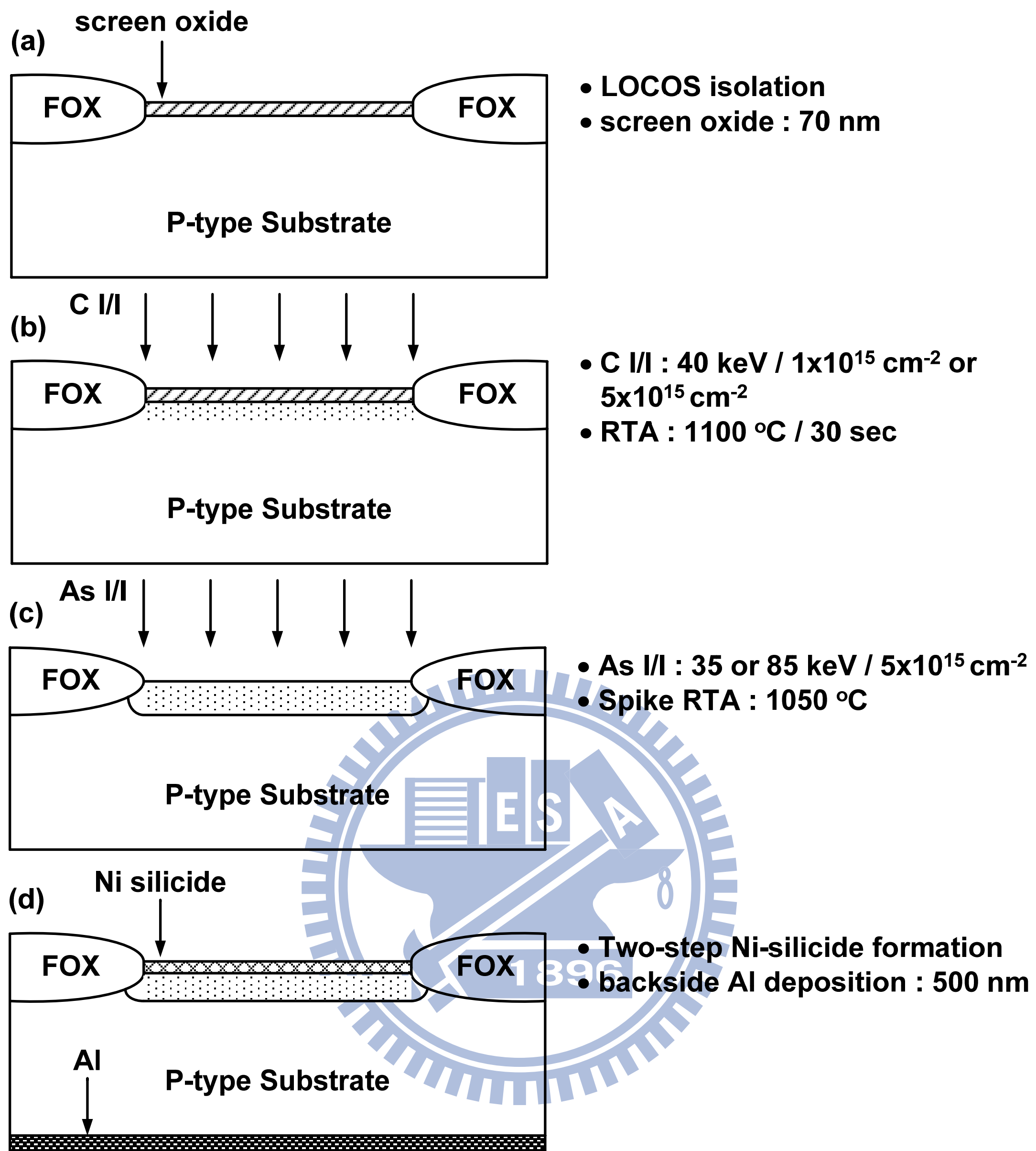


Fig. 3-1 Main process flow of the Ni-silicide-contacted n^+/p shallow junction: (a) after LOCOS isolation and screen oxide growth, (b) after C I/I and annealing, (c) after As I/I and activation, and (d) the final structure.

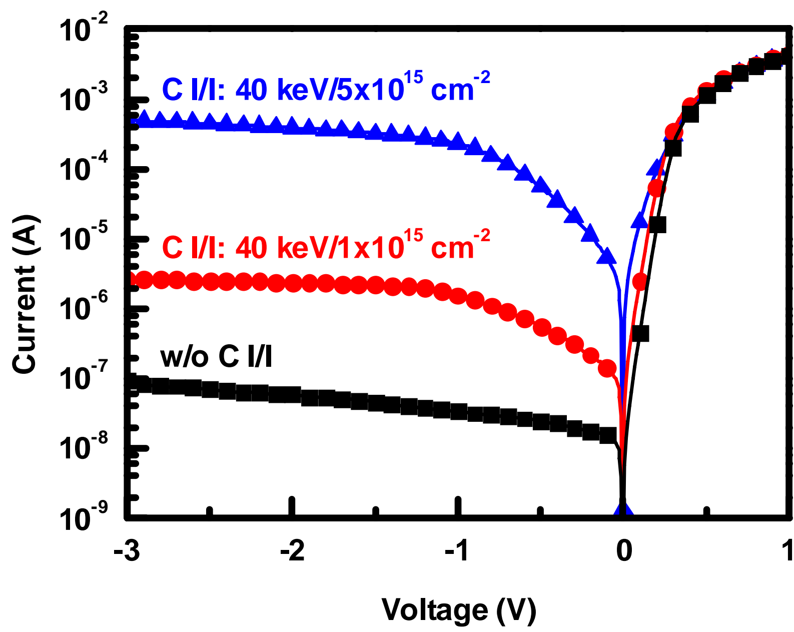
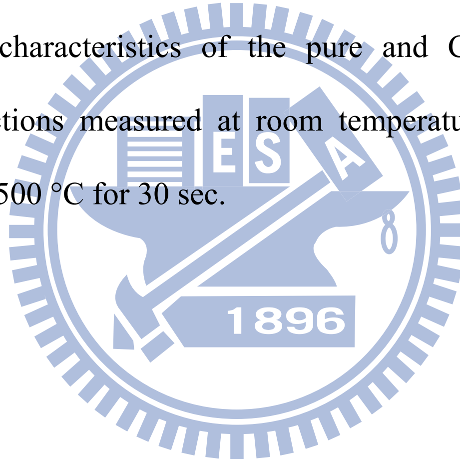


Fig. 3-2 Typical I-V characteristics of the pure and CIA Ni-silicide-contacted Schottky junctions measured at room temperature. Silicide formation is carried out at 500 °C for 30 sec.



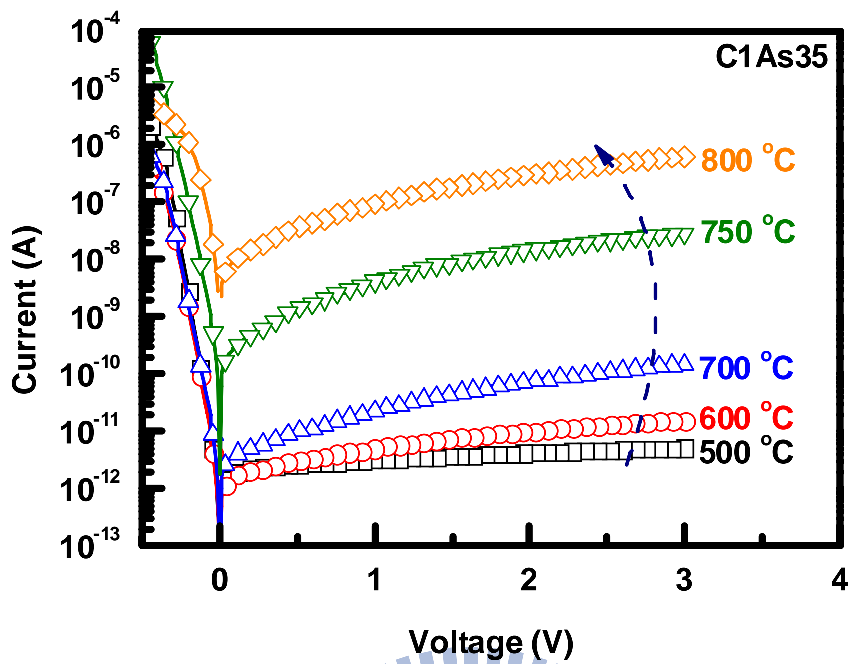


Fig. 3-3 (a) Silicide formation temperature dependences of leakage current characteristics of the C1As35 junctions.

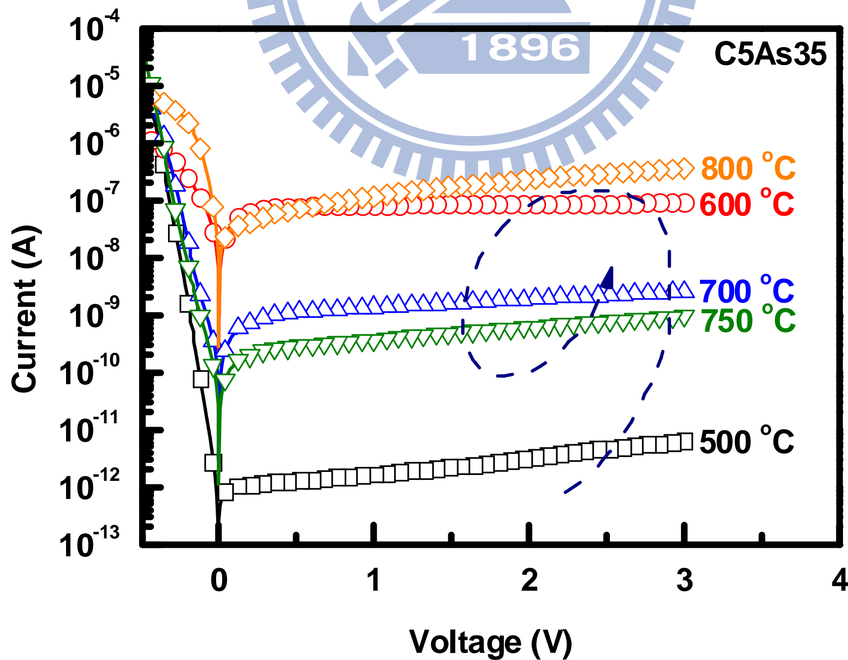


Fig. 3-3 (b) Silicide formation temperature dependences of leakage current characteristics of the C5As35 junctions.

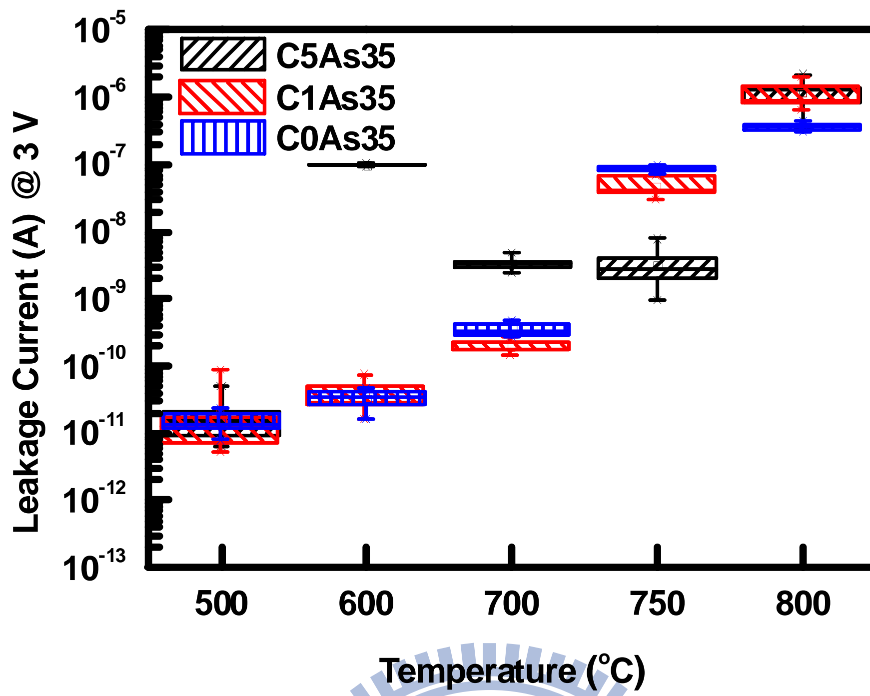


Fig. 3-4 Statistics of the reverse-bias junction leakage current at 3 V for the Ni-silicide-contacted n^+/p shallow junctions with As I/I at 35 keV.

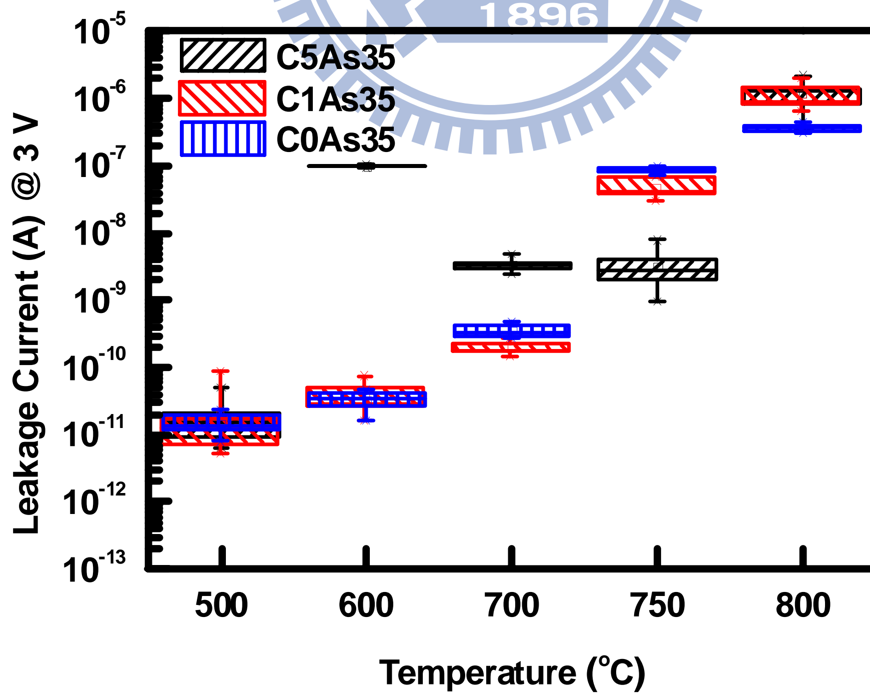


Fig. 3-5 StatStatistics of the reverse-bias junction leakage current at 3 V for the Ni-silicide-contacted n^+/p shallow junctions with As I/I at 85 keV.

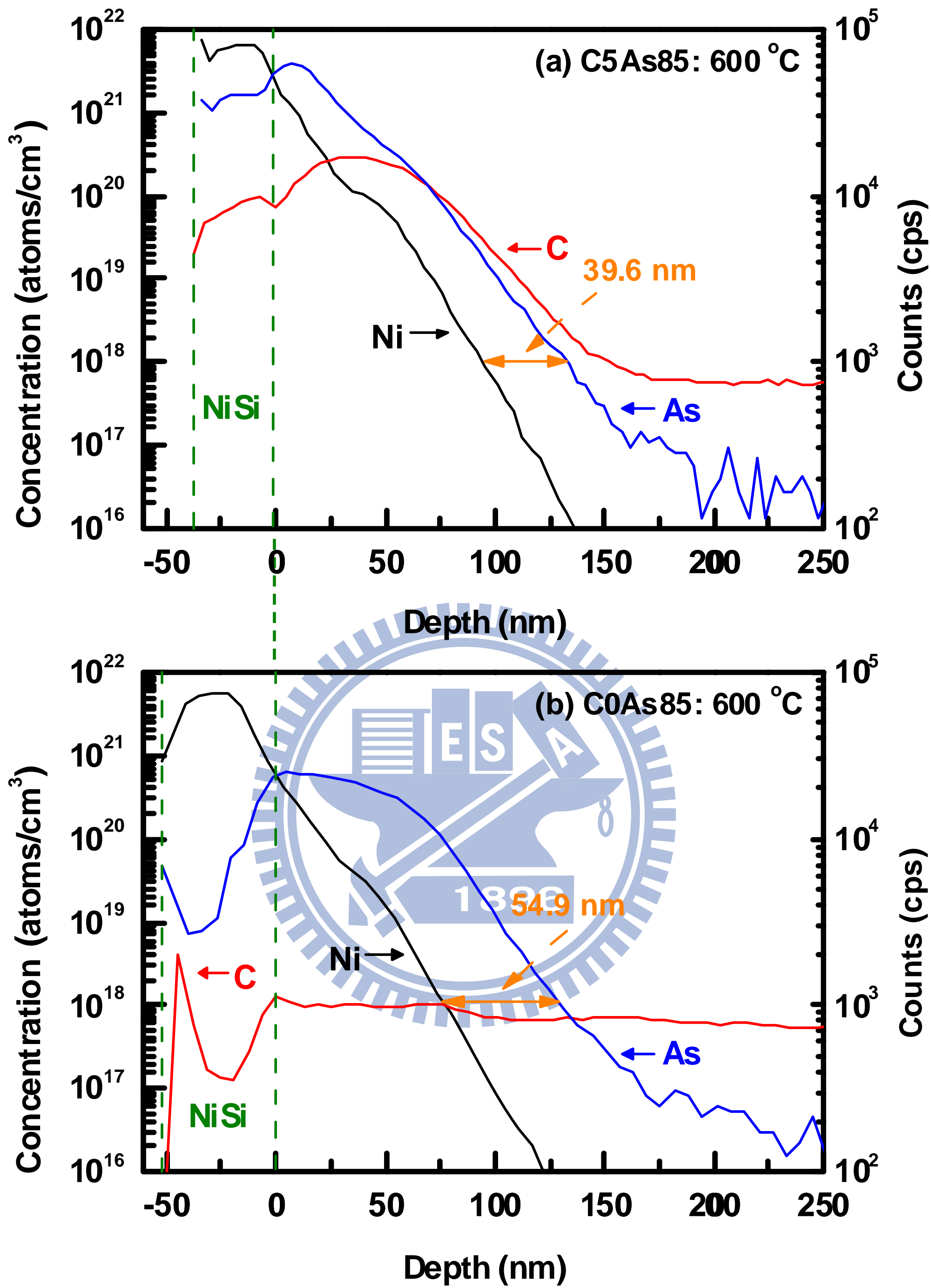


Fig. 3-6 SIMS depth profiles of C, Ni, and As of the (a) C5As85 and (b) C0As85 samples with silicide formation temperature at 600 °C.

Chapter 4

Formation of Silicon-Carbon Alloys Using Low-Temperature Carbon Ion Implantation and Solid Phase Epitaxy

4.1 Introduction

Strain engineering has been proposed to enhance the transistor performance below the sub-90-nm technology node and is actually applied to mass-produced integrated circuit wafers in the early 2000s [1]. Silicon-germanium (SiGe) S/D and a compressive contact etch stop layer (CESL) are both utilized to create uniaxial compressive stress in the Si channel of p-type field-effect transistors (PFETs) and increase the hole mobility [2]. Similarly, forming a tensile CESL over n-type field-effect transistors (NFETs) can produce uniaxial tensile stress along the channel and enhance the electron mobility [1-2]. Furthermore, in 2004, K. W. Ang *et al.* first reported that SiC S/D stressors can also introduce lateral tensile stain and has been regarded as a new candidate material for strained Si NFETs [3]. For SiC S/D stressors, there are still many technical challenges that must be overcome before becoming a high-performance strained Si technology. The equilibrium solid-solubility of C in Si at the melting point temperature is only $3.5\text{x}10^{17}$ am^{-3} [4]. Therefore, when C atoms are incorporated into Si, most of them prefer to occupy interstitial sites rather than locate at substitutional lattice sites in thermal equilibrium. C interstitials in Si can

substantially degrade the electron mobility and increase the leakage current [5-6], so interstitial C concentration (C_{int}) should be reduced in strained Si NFETs with SiC S/D stressors. It is well known that the electron mobility enhancement is increased with an increase of uniaxial tensile stress. In other words, to achieve high electron mobility without significant device degradation, high C_{sub} is necessary. On the other hand, the experimental results indicate C atoms and n-type dopants compete with each other to locate in substitutional Si lattice sites during annealing [7]. The deactivation effect of n-type dopants induced by substitutional C atoms results in the high R_s values and can partially compensate the effects of strain in the SiC layer. Therefore, the C_{sub} value should be carefully considered in device design, and sufficiently high C_{sub} and acceptably low R_s are both required for SiC S/D stressors.

Two main methods have been employed to fabricate heavily doped SiC alloy. One is the combination of a Si recess etch and a selective SiC epitaxy [3, 8]. The other one is implanting C ions into Si followed by SPE regrowth [7, 9-11]. The advantages and disadvantages of these two methods are compared in Table 4-1. Although the in-situ P-doped $Si_{0.979}C_{0.021}$ S/D stressors has been successfully grown by using an Epsilon reduced-pressure chemical vapor deposition epitaxial deposition tool [8], the use of selective epitaxy of the SiC film will lead to increase process cost and complexity. In addition, its low throughput and non-repeatable performance are needed to overcome [11]. On the contrary, the C ion implantation process is relatively low-cost and easier than a selective epitaxial process. Hence, monomer C and cluster C implants have been extensively studied in recent years [7, 9-11]. After co-implantation of C ions and n-type dopants into the Si substrate with the high implantation dose, the surface of the single-crystalline Si substrate becomes amorphous. The amorphous layer thickness and the degree of amorphous phase are

correlated to the substitutional C percentage [11]. Partial amorphization will result in incomplete recrystallization during the SPE process, and thus low C_{sub} is obtained. Hence, for the monatomic C ion implantation with light ion bombardment, it usually needs a pre-amorphization implantation (PAI) to confirm the occurrence of total amorphization. When compared with monomer C ions, cluster C ions are heavy enough to self amorphize the Si surface during the ion implantation process. SPE is well known to incorporate elements into Si at concentrations beyond their solid solubility limits, and its regrowth begins to occur from the end-of-range (EOR) implant damage region. After ion implantation, SPE annealing is carried out to from highly supersaturated and metastable highly doped SiC S/D stressors [7, 9-11]. Q. Zhou *et al.* used a low-temperature RTA technique to achieve high C_{sub} of 1.5 % after SPE regrowth at 700 °C for 120 sec [9]. S. M. Koh et al. proposed a novel high-temperature millisecond anneal (MSA), pulsed laser annealing (PLA), to obtain high C_{sub} of 1.1 % [10]. To the best of our knowledge, low-temperature C ion implantation has never been reported for SiC formation. In this chapter, we focus on the monatomic C ion implantation at a low temperature of -15 °C. Low-temperature C ion implantation can prevent self-annealing during implantation, so total amorphization of the Si surface layer can be easily obtained. Then, three different SPE annealing technologies including RTA, furnace annealing, and PLA, are performed to recrystallize the amorphous Si layer. The influence of different implantation and annealing conditions on the C_{sub} and R_s values is discussed in this work.

4.2 Sample Fabrication

To study the effect of C ion implantation on SiC formation, monatomic C ions were implanted into a p-type Si substrate with different implantation energies, doses,

and temperatures. The implantation energy varied from 3 keV to 9 keV, and the implantation dose was $5x10^{15}$ cm^{-2} or $8x10^{15}$ cm^{-2}. The sample holder kept at either -15 °C or 5 °C during ion implantation. Then, the P ion implantation condition was fixed at 17 keV to a dose of $5x10^{15}$ cm^{-2} for all samples. P ions are chosen to dope the surface of the Si substrate instead of commonly used As ions for two reasons. As compared to P-doped SiC S/D stressors, As-doped SiC S/D stressors have the lower effective C_{sub} and higher R_s values owing to an increased stress compensation effect and C-induced deactivation of n-type dopants [12]. Three different SPE annealing technologies were individually used to activate C atoms and P dopants and annihilate implantation defects, as described below. The RTA process in N_2 ambient was utilized at temperature range from 650 °C to 850 °C and for time period range from 90 sec to 180 sec. Furnace annealing was performed in N_2 ambient at medium temperature of 750 °C for 1 hr to reveal the effect of increasing SPE annealing time. The PLA process was carried out in a vacuum environment (~$2x10^{-2}$ Torr) to melt and recrystallize the amorphous Si surface in millisecond time range. The wave length of the KrF laser beam is 248 nm, and its pulse duration is 30 nsec. The laser spot size is 23 mm by 1.8 mm, and its energy density distribution is semi-Gaussian shape. The constant energy is distributed along the longer axis, and the Gaussian energy distribution with the pre-set value of the peak energy is along the shorter axis. Multiple laser pulses with the repetition rate of 40 Hz were employed in the range of 10 to 20 pulses with the laser energy density ranging from 200 to 540 mJ/cm^2. Before performing the laser processing step, a 50-nm-thick tetra-ethoxy-silane (TEOS) oxide was deposited on the amorphous Si surface by plasma-enhanced chemical vapor deposition (PECVD). The TEOS oxide capping layer can minimize C out-diffusion and act as the antireflective layer.

The implant damage region before and after SPE regrowth was inspected using cross-sectional transmission electron microscope (XTEM). The depth profile analysis of C atoms and P dopants was performed via SIMS. The R_s values were measured with the four-point probe. High-resolution x-ray diffraction (HRXRD) was carried out to determine the C_{sub} value of the recrystallized SiC film. The C_{sub} values can be calculated from the HRXRD rocking curve, and its computational process can be observed in reference [13].

4.3 Results and Discussion

4.3.1 Incomplete Recrystallization and P Redistribution

Figure 4-1 and 4-2 show the SIMS depth profile and XTEM image of the sample implanted with C (7 keV/5x10^{15} cm^{-2} at -15 °C) and P (17 keV/5x10^{15} cm^{-2}) ions, respectively. The R_p of C at 7 keV is about 27.7 nm below the Si surface, and the maximum C-implanted concentration of 2.68 % is achieved at this position. The distribution of P atoms is slightly shallower than that of C atoms under this implantation condition. After co-implantation, the 49-nm-thick amorphous Si layer is formed on the surface of the Si substrate. Total amorphization and a sharp amorphous/crystal (*a/c*) interface are clearly observed. After RTA annealing at 750 °C for 120 sec, the SIMS depth profile and XTEM image are changed and are shown in Fig. 4-3 and 4-4, respectively. The RTA-annealed C depth profile is almost identical to the as-implanted C depth profile, but significant change in the P depth profile is detected after RTA annealing. The abnormal redistribution of P atoms will be discussed later. According to Fig. 4-4, we find that the amorphous Si layer is not completely recrystallized during the RTA annealing, and the thickness of the recrystallized SiC region is 27 nm. It has been reported that the presence of a high

concentration of C in Si raises the SPE temperature and retards the SPE growth rate owing to the high stress level [14-15]. SPE regrowth stops near the C-implanted R_p, and the retardation phenomenon of the SPE rate is also confirmed by an XTEM micrograph of the sample implanted only with C (7 keV/5x10^{15} cm^{-2} at -15 °C) ions and annealed at 750 °C for 120 sec, as shown in Fig. 4-5. If the SPE-annealing time increases to 1 hr, the recrystallization front can pass through the C-rich region and further propagates towards the Si surface at different rates at different locations, as shown in Fig 4-6. We consider that the non-uniform SPE rate results from the variation of the local stress. Therefore, the highly defective regrown layer with uneven thickness is formed after furnace annealing at 750 °C for 1 hr.

To investigate the change in the P distribution before and after post-RTA annealing, their SIMS depth profiles of the P concentration are compared in Fig. 4-7. In the P profile tail region, the as-implanted P distribution is almost the same as the RTA-annealed P distribution because the interstitial-assisted mechanism of P diffusion is suppressed by the presence of C atoms [16]. C atoms can trap Si interstitials to form C/I clusters and reduce the self-Si-interstitial concentration. Although the EOR defect is still formed during the RTA annealing at 750 °C, it does not dissolve to produce a large amount of self-Si interstitials. However, comparing the P distribution profiles near the Si surface, the P concentration obviously reduces in the recrystallized SiC region and increases in the amorphous Si region. The impurity redistribution phenomenon arising from low-temperature crystallization of amorphous Si has been reported previously and is associated with the solubility in the regrowing phase, the segregation coefficient at the moving *a/c* interface, and the interface velocity [17-18]. The segregation coefficient (κ) of the impurity is defined as the ratio of solid solute concentration to liquid solute concentration at the melting point of Si.

The reported κ value of P dopants is 0.35, which means that P dopants prefer to stay within the amorphous Si region rather than the recrystallized Si region during SPE regrowth [19]. Furthermore, R. Duffy *et al.* also reported the greater impurity redistribution arises from retarded crystallization [17]. While the *a/c* front propagates to higher C concentration, the P diffusivity in the amorphous Si region is higher than the velocity of the *a/c* front owing to the retardation of the SPE rate induced by substitutional C atoms. Therefore, P dopants have sufficient time to diffuse out of the recrystallized SiC region and are relocated at the amorphous Si surface. Hence, the large magnitude of P redistribution is observed, and significant reductions in the P concentration and activation result in the high R_s values of the recrystallized SiC film.

4.3.2 Substitutional C Concentration and Sheet Resistance

The R_s values of various samples with different implantation energies, doses, temperatures, and annealing conditions are summarized in Table 4-2. Figure 4-8 shows the HRXRD rocking curves as a function of the implantation energy. The diffraction angle of the SiC peak is higher than that of the Si (004) peak because the lattice constant (a) of SiC is smaller than that of Si (a_{Si}= 0.543 nm). The C ion implantation is performed at 5 °C with a dose of $5x10^{15}$ cm^{-2}. After RTA annealing at 700 °C for 120 sec, both of the R_s and C_{sub} values continuously increase with increasing the implantation energy from 3 keV to 7 keV, as shown in Fig. 4-8. The C_{sub} value of 0.973 % is obtained as the implantation energy is at 7 keV, but its R_s value increases to 270.5 Ω/□. The high R_s value is attributed to the incomplete recrystallization and the reductions of the P concentration and activation as mentioned before. As the implantation energy is increased from 3 keV to 7 keV, the increased overlap between the C and P doping profiles results in the higher R_s values. The C_{sub}

value is highly associated with the amorphous layer thickness and the degree of amorphization. The thicker amorphous layer and total amorphization can cause the higher C_{sub} value after SPE regrowth. Hence, the higher C_{sub} value can be obtained with higher energy implantation of C. If the implantation energy is increased from 7 keV to 9 keV, the extracted C_{sub} value is saturated at 1.047 %, as shown in Fig. 4-9. Its implantation and annealing condition are labeled in the figure.

Next, we discuss the effect of the C implantation dose on the R_s and C_{sub} values. Figure 4-10 compares the HRXRD rocking curves of the RTA-annealed samples with two different implantation doses. A further increasing in the C implantation dose increases the thickness of the amorphous layer and the degree of amorphization. Therefore, the high C_{sub} value is expected to be obtained with increasing the C ion dose of $8x10^{15}$ cm^{-2}, but the ratio of substitutional to total C concentration is decreased. An increase in substitutional C concentration is accompanied by an increase in interstitial C concentration. From Fig. 4-10, the SiC peak becomes broader with much lower intensity with increasing the C ion dose to $8x10^{15}$ cm^{-2}. The decreased peak intensity suggests that the recrystallized SiC region has the poor crystal quality. The local change in the recrystallization rate induced by high C concentration can lead to a large number of crystal defects, such as dislocations, stacking faults, and twins [20]. The highest R_s value of 391 Ω/□ in Table 4-2 provides another evidence for the poor crystal quality. Hence, for obtaining the higher quality SiC layer, the C implantation dose should not exceed $5x10^{15}$ cm^{-2}.

Figure 4-11 shows the implantation temperature dependence of the HRXRD rocking curves of the RTA-annealed samples. The XTEM image of the sample implanted with C (7 keV/$5x10^{15}$ cm^{-2} at 5 °C) and P (17 keV/$5x10^{15}$ cm^{-2}) ions is shown in Fig. 4-12. Similar to Fig. 4-2, total amorphization is also reached at the

implantation temperature of 5 °C. Its amorphous-layer thickness is 49 nm, the same as that presented in Fig. 4-2. However, as compared to Fig. 4-2, the *a/c* interface shown in Fig. 4-12 reveals rough and low contrast. Therefore, after SPE annealing at 750 °C for 120 sec, the C_{sub} value of the RTA-annealed sample implanted at -15 °C is slightly higher than that of the RTA-annealed sample implanted at 5 °C. The highest C_{sub} value of 1.046 % can be achieved by using a low-temperature C ion implantation technology at -15 °C.

Figure 4-13 presents the annealing temperature dependence of the HRXRD spectra of the RTA-annealed samples for fixed annealing time of 120 sec. The C_{sub} value continuously increases from 0.88 % to 1.027 % until the annealing temperature is increased to 750 °C. Moreover, the crystal quality of the recrystallized SiC region, as well as the R_s values listed in Table 4-2, can be improved by thermal annealing at higher temperatures. Nevertheless, once the annealing temperature exceeds 750 °C, the SiC peak is gradually close to the Si peak. Because most of the substitutional C atoms diffuse into the interstitial sites at higher temperatures, the C_{sub} value decreases and even near zero at 850 °C. Therefore, the annealing temperature of 750 °C is suitable for SiC formation. Figure 4-14 presents the annealing time dependence of the HRXRD spectra of the RTA-annealed samples annealed at a fixed temperature of 750 °C. Further annealing results in the metastable state towards thermal equilibrium. Hence, the C_{sub} value will slightly decrease with little increase in the annealing time. Too much thermal budget will cause the metastable state returns to thermal equilibrium, as shown in Fig. 4-15. When additional RTA annealing at the higher temperature of 1000 °C for 1 sec or furnace annealing at 750 °C for prolonged annealing time of 1 hr is performed, no obvious SiC peak can be observed.

The R_s values of the PLA-annealed samples with differing laser energy density and number of incident laser pulses are summarized in Table 4-3. Lower laser energy and a small number of incident laser pulses are insufficient to totally recrystallize the amorphous Si layer, so the R_s values higher than 1000 Ω/□ are measured. Increasing energy density and number of incident laser pulses can activate P dopants and reduce the R_s values. However, their HRXRD rocking curves indicate no C atoms are located at substitutional sites, as shown in Fig. 4-16. These HRXRD experimental results do not correspond to the previously reported experimental HRXRD data under similar experimental conditions [10, 21]. The possible reason is explained as follows. Since PLA was carried out in a low vacuum environment (~$2x10^{-2}$ Torr= 2.666 Pa), there is still residual oxygen (O) in the chamber. It has been reported that O can interact with vacancy (V) to form the V-O defect in a 10^{-4} Pa working pressure during high-energy pulsed laser irradiation with multiple pulses [22]. The V-O defects can react with the substitutional C atoms to form CO complexes and volatile carbon oxides [22]. Therefore, to obtain the high C_{sub} values, the PLA process must be performed in an oxygen-free environment to prevent C precipitation.

4.4 Conclusions

In this chapter, the SiC alloy is successfully fabricated by using the low-temperature C ion implantation followed by RTA annealing. The highest C_{sub} value of 1.046 % can be obtained via process optimization. For SiC S/D stressors, the C-implanted concentration in Si should be carefully optimized. It is useless to dope excess C atoms in Si because most of them will occupy interstitial sites instead of substitutional sites to form generation and scattering centers. Furthermore, the excess C-implanted concentration will result in incomplete recrystallization during the SPE

process and significant reductions of the P concentration in the recrystallized SiC region. Both of them cause an increase in the R_s values of the recrystallized SiC region. The critical amorphization dose decreases with decreasing implantation temperature, so the low-temperature C ion implantation only needs a lower implantation dose to achieve self amorphization without using PAI or heavier C cluster ions. A lower implantation dose can also help reduce the excess C-implanted concentration and C_{int}. Therefore, if the implantation temperature can be further reduced to lower temperature, the low-temperature C ion implantation has the potential to simultaneously achieve high C_{sub} with high substitutional-to-total C ratio and low R_s. After SiC formation, it is important to note that the high thermal budget process should be avoided to eliminate C precipitation in Si.

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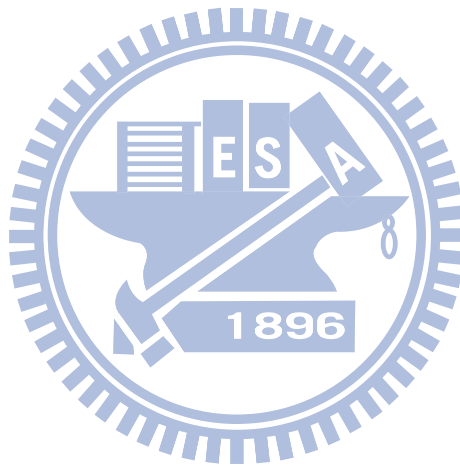


Table 4-1 Comparison of two fabricating methods of SiC S/D stressors.

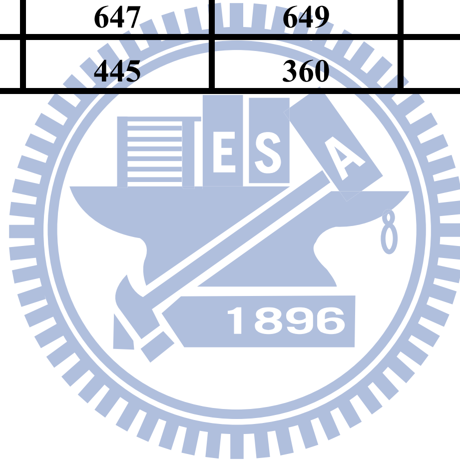
Fabrication method	Si recess etch and selective SiC epitaxy	C ion implantation and SPE
Throughput	low	high
Process complexity	complex	easy
Process cost	high	low
Highest reported C_{sub}	2.3 % [8]	2.2 % [11]
Design stressor shape	yes	no
Doping method	in-situ doping	ion implantation

Table 4-2 Summary of the R_s (Ω/□) values of the RTA-annealed and furnace-annealed samples with different implantation energies, doses, temperatures, and annealing conditions.

C I/I \ SPE	650 °C/ 120 sec	700 °C/ 120 sec	750 °C/120 sec 750 °C/1 hr	800 °C/ 120 sec	850 °C/ 120 sec
3 keV/5x10^{15} cm^{-2} (5 °C)	139.5	134.7	----------	----------	----------
5 keV/5x10^{15} cm^{-2} (5 °C)	185.5	177.9	----------	----------	----------
7 keV/5x10^{15} cm^{-2} (5 °C)	292	270.5	258 242.8	238	173
C I/I \ SPE	**750 °C/ 90 sec**	**750 °C/ 120 sec**	**750 °C/ 150 sec**	**750 °C/ 180 sec**	**750 °C/120 sec & 1000 °C/1 sec**
7 keV/5x10^{15} cm^{-2} (-15 °C)	267	255	247	241	125
7 keV/8x10^{15} cm^{-2} (-15 °C)	----------	391	----------	----------	213
9 keV/5x10^{15} cm^{-2} (-15 °C)	----------	327	----------	----------	132

Table 4-3 Summary of the R_s (Ω/□) values of the PLA-annealed samples with different laser energy densities and number of incident laser pulses. Before PLA annealing, these samples were implanted with C (9 keV/$5x10^{15}$ cm^{-2} at -15 °C) and P (17 keV/$5x10^{15}$ cm^{-2}) ions.

Laser energy (mJ/cm^2)	10 pulses	15 pulses	20 pulses
200	----------	----------	high R_s (non-measureable)
240	----------	----------	high R_s (non-measureable)
300	----------	----------	high R_s (non-measureable)
340	----------	----------	high R_s (non-measureable)
400	226900	234400	1125
440	41500	11240	738
500	647	649	383
540	445	360	328



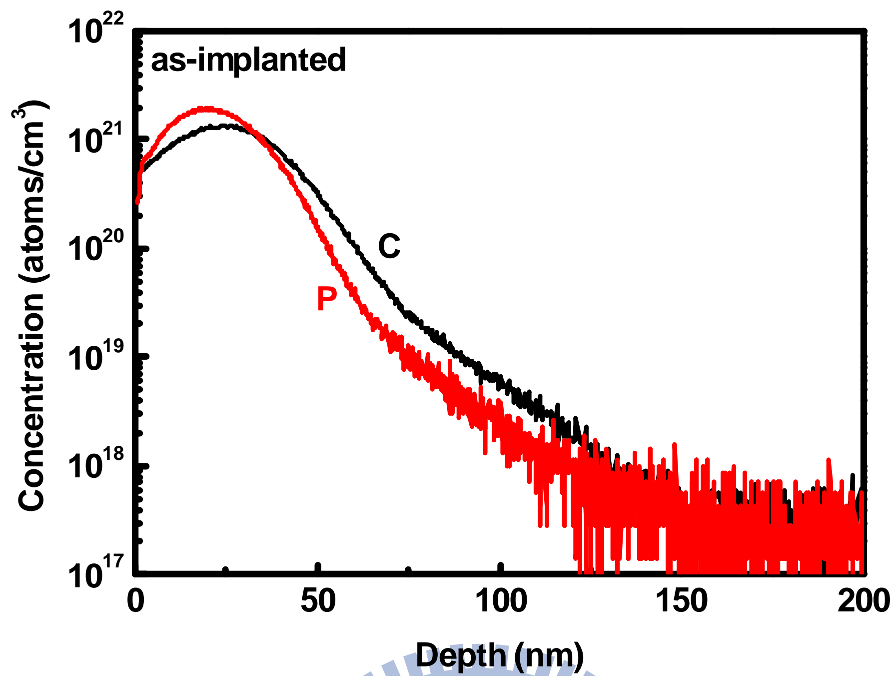


Fig. 4-1 SIMS depth profile of the as-implanted sample implanted with C (7 keV/5x10^{15} cm^{-2} at -15 °C) and P (17 keV/5x10^{15} cm^{-2}) ions.

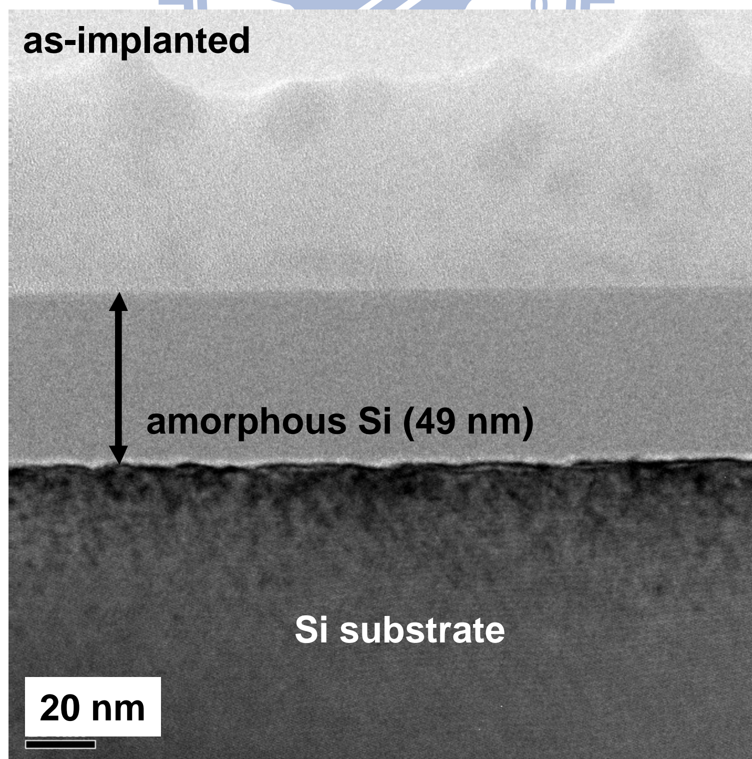


Fig. 4-2 XTEM image of the as-implanted sample implanted with C (7 keV/5x10^{15} cm^{-2} at -15 °C) and P (17 keV/5x10^{15} cm^{-2}) ions.

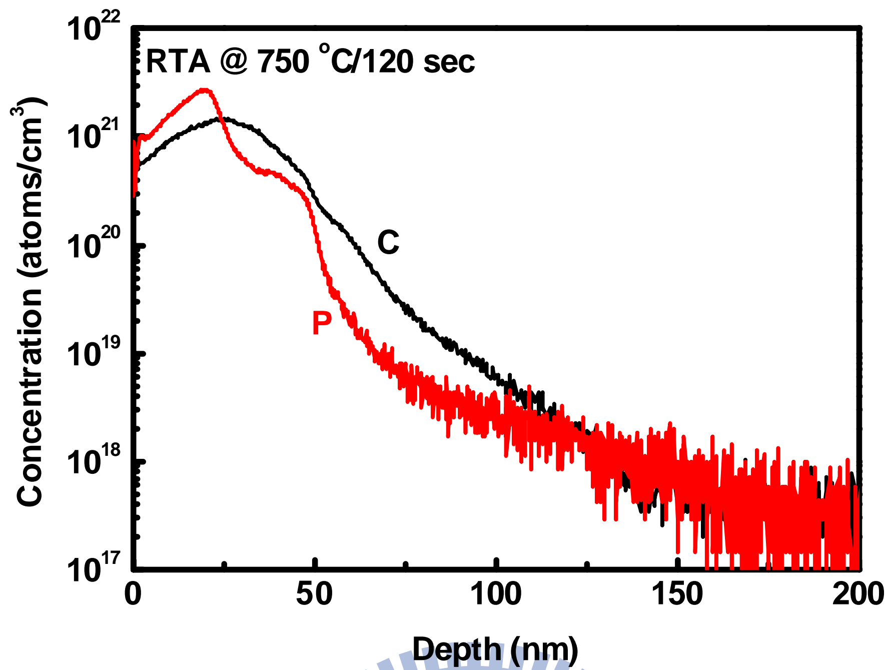


Fig. 4-3 SIMS profile of the RTA-annealed (750 °C/120 sec) sample implanted with C (7 keV/5x10^{15} cm^{-2} at -15 °C) and P (17 keV/5x10^{15} cm^{-2}) ions.

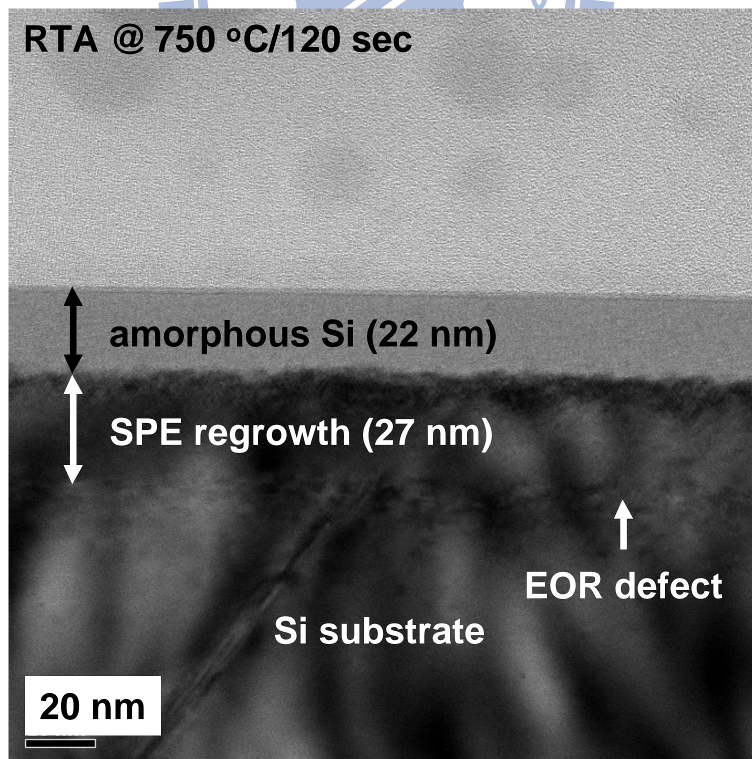


Fig. 4-4 XTEM image of the RTA-annealed (750 °C/120 sec) sample implanted with C (7 keV/5x10^{15} cm^{-2} at -15 °C) and P (17 keV/5x10^{15} cm^{-2}) ions.

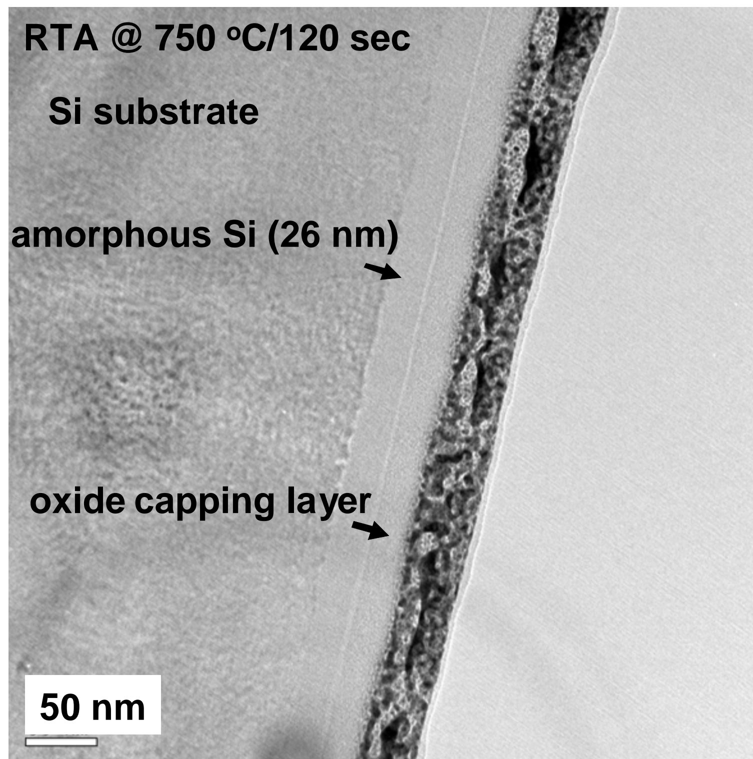


Fig. 4-5 XTEM image of the RTA-annealed (750 °C/120 sec) sample implanted only with C (7 keV/5x10^{15} cm^{-2} at -15 °C) ions.

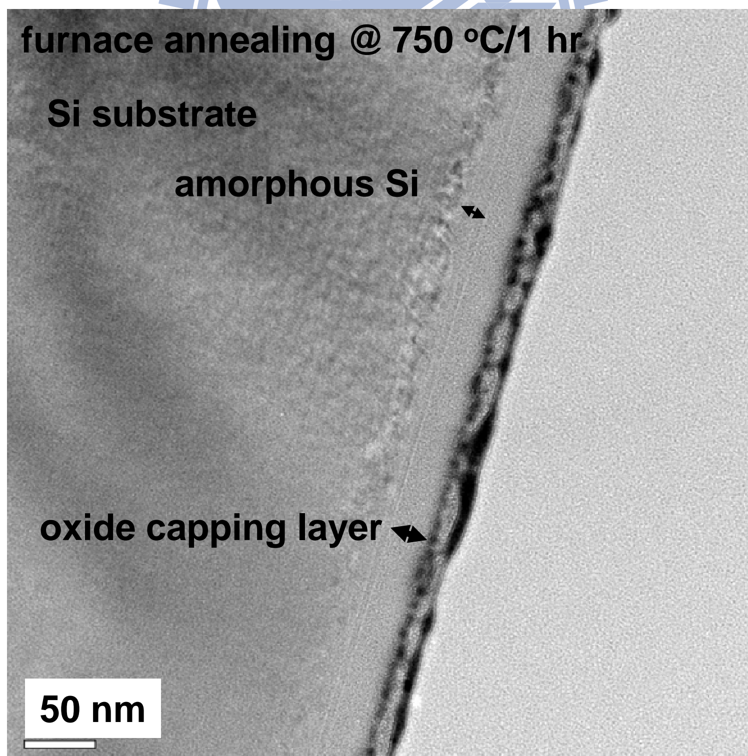


Fig. 4-6 XTEM image of the furnace-annealed (750 °C/1 hr) sample implanted with C (7 keV/5x10^{15} cm^{-2} at -15 °C) and P (17 keV/5x10^{15} cm^{-2}) ions.

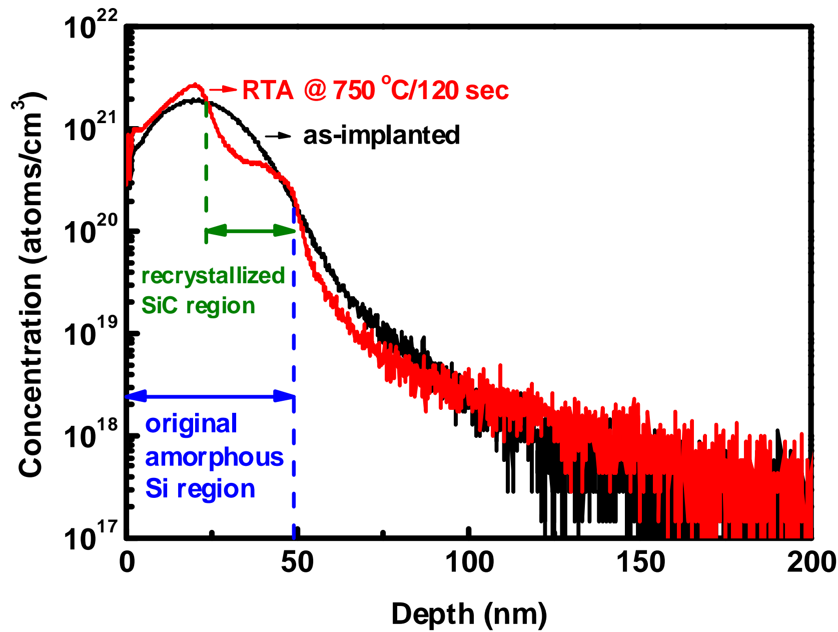


Fig. 4-7 Comparison of the SIMS profiles of the as-implanted and RTA-annealed (750 °C/120 sec) samples implanted with C (7 keV/5x10^{15} cm^{-2} at -15 °C) and P (17 keV/5x10^{15} cm^{-2}) ions.

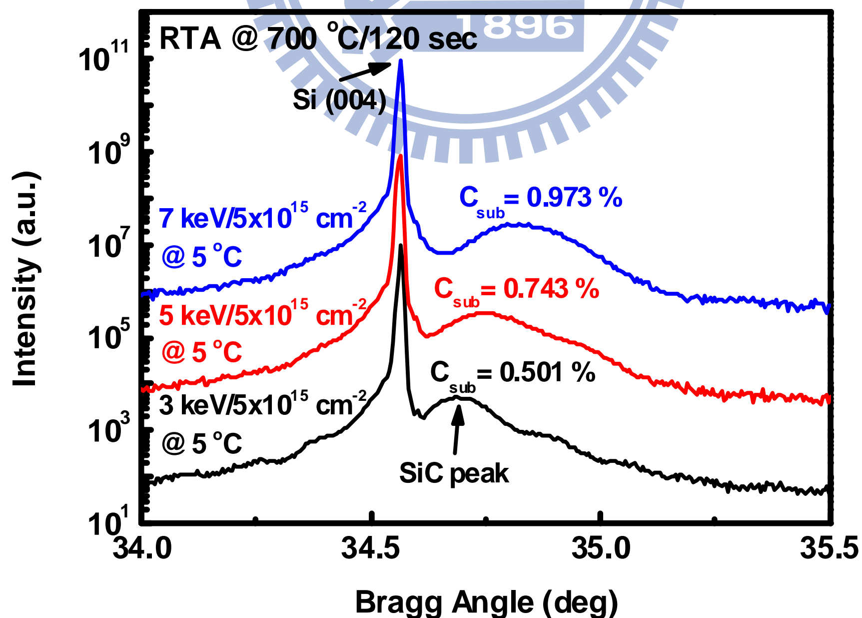


Fig. 4-8 Energy dependence of the HRXRD rocking curves of the RTA-annealed (700 °C/120 sec) samples implanted with C and P (17 keV/5x10^{15} cm^{-2}) ions.

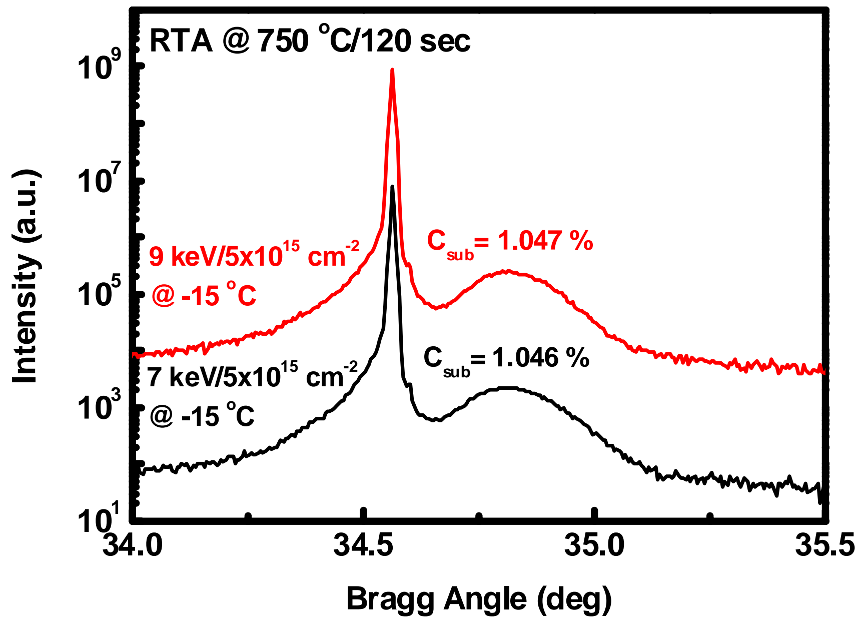


Fig. 4-9 Energy dependence of the HRXRD rocking curves of the RTA-annealed (750 °C/120 sec) samples implanted with C and P (17 keV/5x10^{15} cm^{-2}) ions.

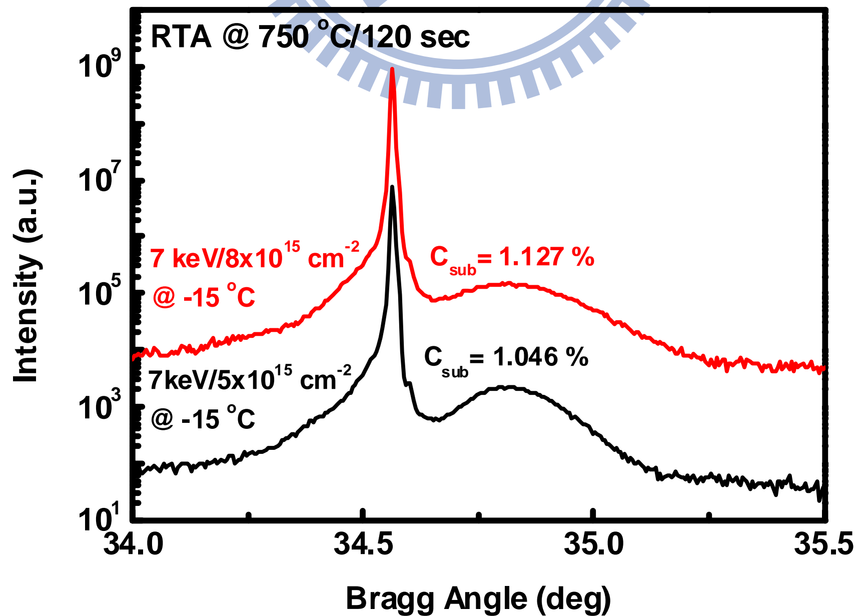


Fig. 4-10 Dose dependence of the HRXRD rocking curves of the RTA-annealed (750 °C/120 sec) samples implanted with C and P (17 keV/5x10^{15} cm^{-2}) ions.

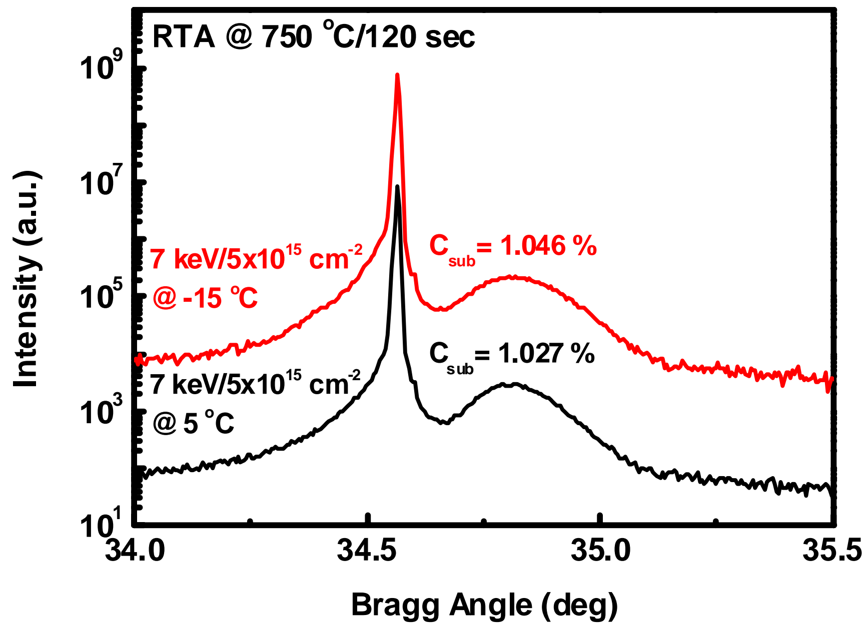


Fig. 4-11 Implantation temperature dependence of the HRXRD rocking curves of the RTA-annealed (750 °C/120 sec) samples implanted with C and P (17 keV/5×10^{15} cm^{-2}) ions.

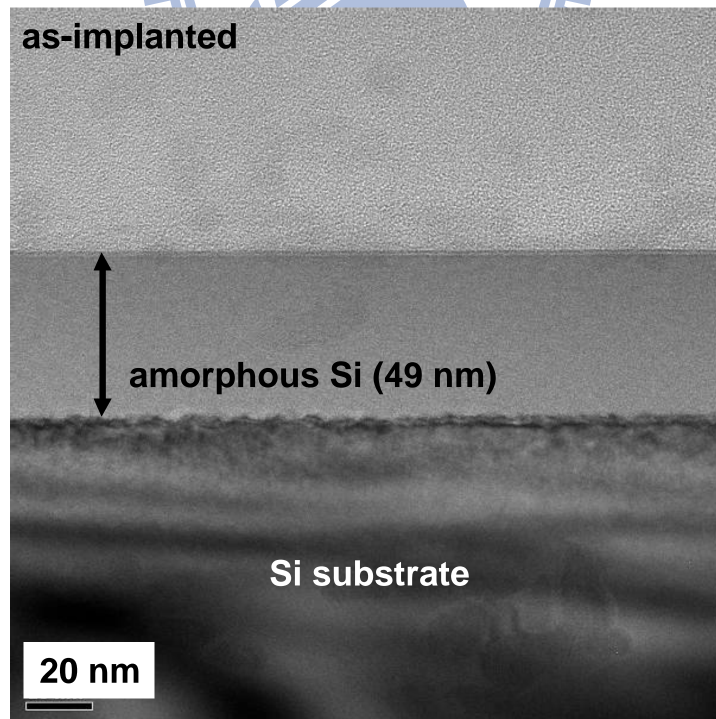


Fig. 4-12 XTEM image of the as-implanted sample implanted with C (7 keV/5×10^{15} cm^{-2} at 5 °C) and P (17 keV/5×10^{15} cm^{-2}) ions.

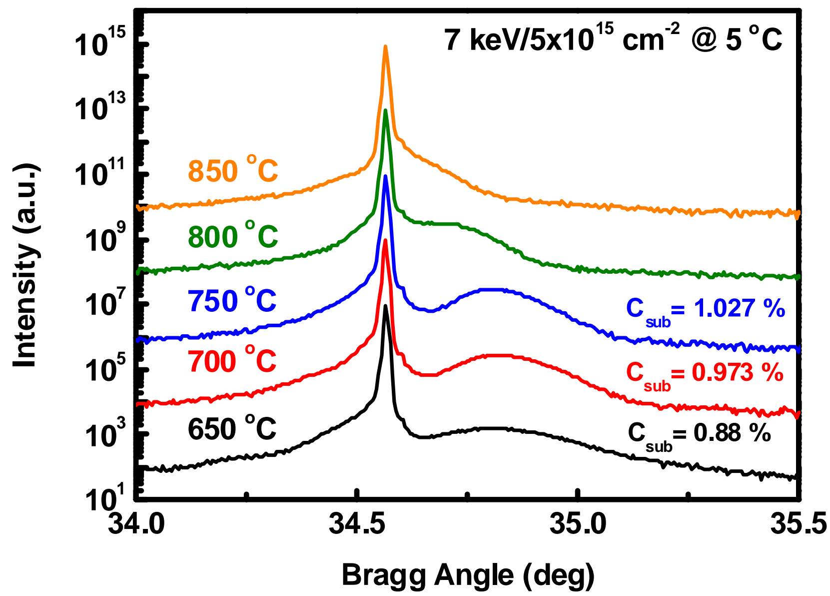


Fig. 4-13 HRXRD spectra of the RTA-annealed samples implanted with C and P (17 keV/5x10^{15} cm^{-2}) ions after RTA annealing at various temperatures for 120 sec.

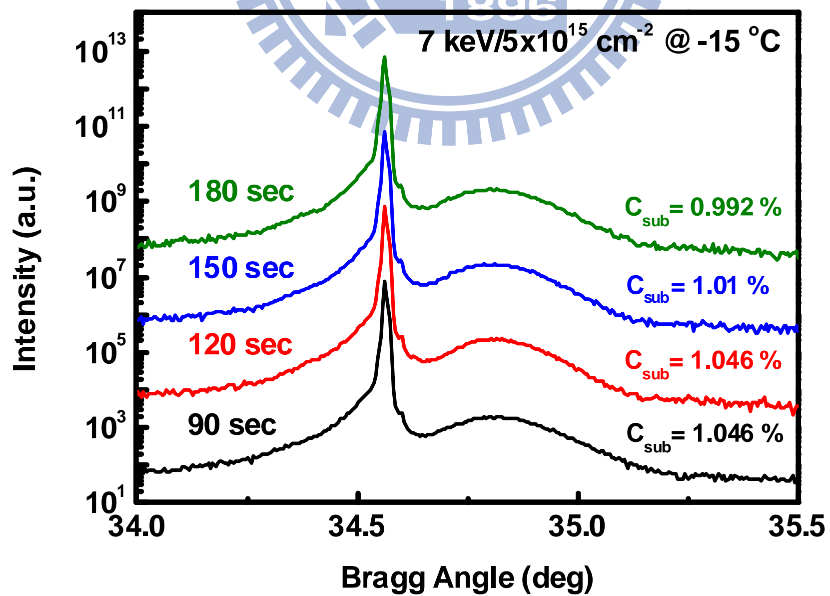


Fig. 4-14 HRXRD spectra of the RTA-annealed samples implanted with C and P (17 keV/5x10^{15} cm^{-2}) ions after RTA annealing at 750 °C for different annealing time.

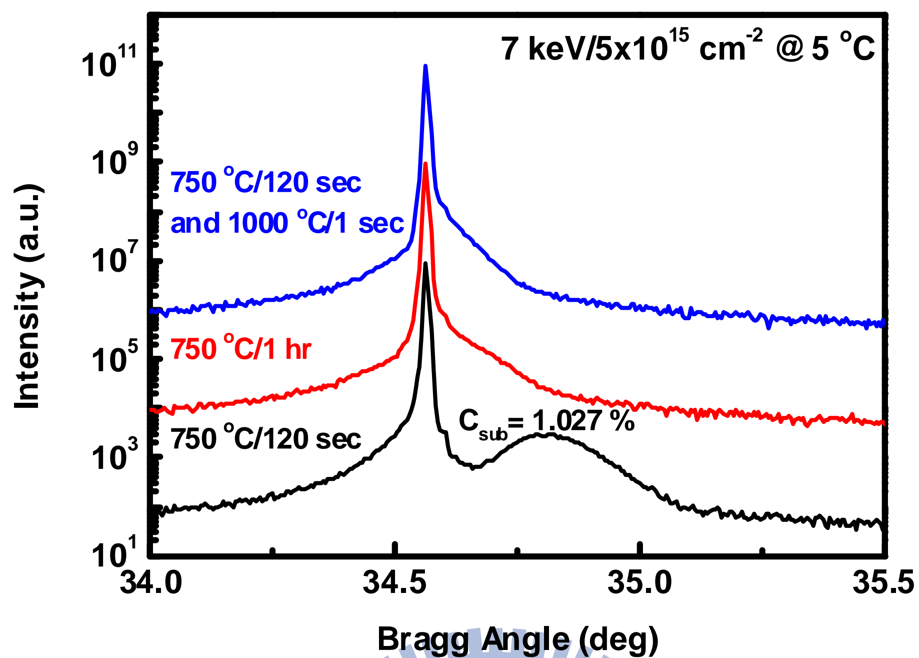


Fig. 4-15 HRXRD spectra of the RTA-annealed and furnace-annealed samples implanted with C and P (17 keV/5x10^{15} cm^{-2}) ions.

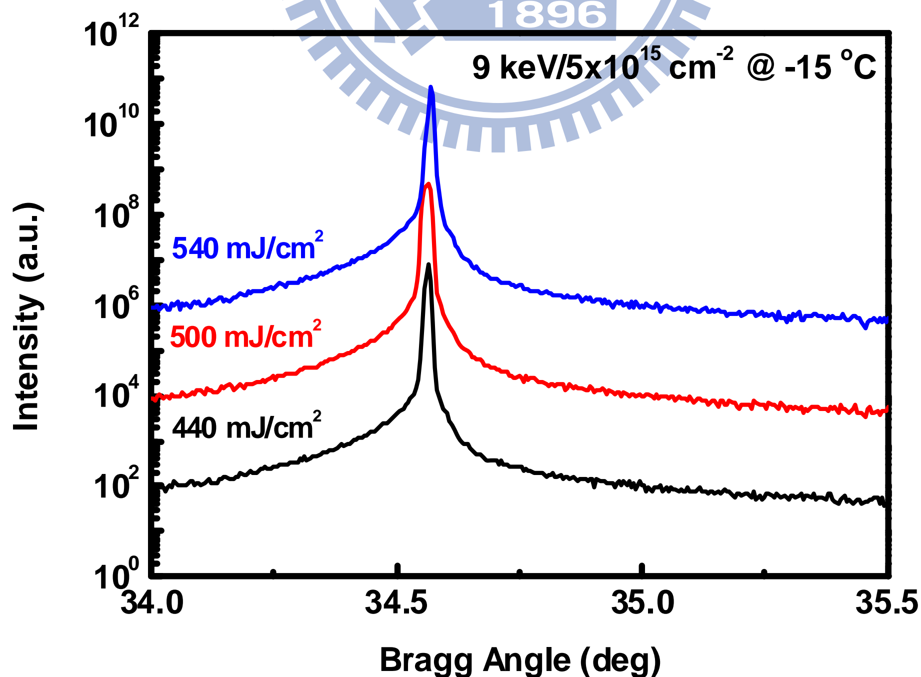


Fig. 4-16 HRXRD spectra of the PLA-annealed samples implanted with C and P (17 keV/5x10^{15} cm^{-2}) ions.

Chapter 5

Fabrication and Electrical Characteristics of Gate-All-Around Poly-Si Nanowire Thin-Film Transistors

5.1 Introduction

Low temperature poly-Si TFTs have been studied for several years and successfully used as pixel and driving IC in AM-LCDs and AM-OLED displays [1-2]. However, in order to apply poly-Si TFTs to SOP display, their device characteristics are needed to be further improved. Furthermore, 3D IC and 3D Flash memory have several advantages for relaxing device scaling down issues [3-4], which could be realized by using the poly-Si TFT technology. Therefore, for these applications, high-performance poly-Si TFTs are required.

To achieve high performance, poly-Si TFTs with various fabrication processes and device structures have been extensively investigated to reduce grain-boundary defects of the poly-Si film and eliminate SCEs. Large-grain poly-Si TFTs are extensively researched by different recrystallization technologies including ELA and MILC instead of conventional SPC [5-6]. Large-grain poly-Si TFTs with low grain-boundary defect density can enhance the carrier mobility and suppress the leakage current. Furthermore, it is well known that the NH_3 plasma treatment process is able to reduce grain-boundary defects and effectively improve the device

characteristics of poly-Si TFTs [7]. Various poly-Si NW TFTs with different multi-gate structures were proposed by many researchers [8-11]. The main advantage of these device structures is suppressing SCEs by increasing the control ability of the gate electrode. The device parameters of several high-performance poly-Si TFTs published in recent years are summarized in Table 5-1 [5-6, 10-13]. Although great progress has been achieved, the device performance of poly-Si TFTs is still poorer than that of the devices fabricated on single crystalline Si. This chapter will review these high-performance poly-Si TFTs and discuss advantages and disadvantages of them. Based on these discussions, the aim of this study is to achieve high-performance poly-Si TFTs by structural engineering.

Furthermore, the L_G of most of the published poly-Si TFTs is usually larger than or equal to 1 μm, so the short-channel behavior of poly-Si TFTs is not clear. As poly-Si TFTs are applied in the 3D IC or 3D Flash memory technology in the future, L_G scaling of poly-Si TFTs should be achieved simultaneously for high layout efficiency as logic or memory devices. Therefore, the device characteristics of poly-Si TFTs with the ultra-short L_G must be investigated. Although the poly-Si NW TFT with L_G down to 20 nm and the omega-shaped gate electrode has been reported, the switching characteristics are poor [11]. In this chapter, we successfully fabricate the smallest GAA poly-Si NW TFT with L_G of 30 nm. Good electrical characteristics are obtained by the poly-Si NW, GAA, and MSB S/D structures [14]. Short-channel and narrow-width characteristics of our fabricated devices are investigated. The current transport mechanism is clarified by high-temperature measurements. Finally, the effect of the NH_3 plasma treatment on the device characteristics is also discussed.

5.2 Structural Engineering

In this section, we first discuss how to achieve high-performance poly-Si TFTs by structural engineering, which can be divided into three parts: (a) recrystallization techniques, (b) short-channel characteristics, and (c) driving capability.

(a) Recrystallization techniques

Reducing the number of the grain boundary in the poly-Si channel region is the basic strategy to achieve high performance. Therefore, several recrystallization techniques including the SPC, ELA, and MILC technologies were studied to enlarge the grain size of the poly-Si channel film [5-6]. The comparison of these recrystallization techniques are listed in Table 5-2. For large-area poly-Si TFTs, the device characteristics of the ELA and MILC poly-Si TFTs are superior to those of the SPC poly-Si TFTs because of their larger grain size and fewer grain boundaries throughout their channel regions [5-6]. However, the ELA process has two drawbacks, such as its high initial cost and process complexity [15]. The MILC grains contain small amounts of metal contamination and high intragrain defect density, which can deteriorate the device characteristics [16]. In addition to the enlargement of the grain size, device scaling also helps reduce the number of the grain boundary in the poly-Si channel region. If the active device area is compatible with the average grain size, it is possible to have few grain boundaries in the poly-Si channel region. Hence, despite using SPC technology, good device characteristics may still be obtained by device scaling. SPC crystallization technology is a promising technique due to its simplicity, low cost, excellent uniformity, and large-area capacity [17]. In this work, we use the SPC crystallization technology instead of other grain-enhancement techniques to investigate the effect of device scaling on the device characteristics of poly-Si TFTs.

(b) Short-channel characteristics

Most high-performance poly-Si TFTs have L_G lager than 1 μm to avoid SCEs, so excellent subthreshold swing (S.S.) and drain-induced-barrier-lowering (DIBL) values can be obtained [5-6, 12]. To reduce L_G while keeping good SCEs, the natural length (λ) concept of conventional Si MOSFETs is introduced into poly-Si TFTs [18]:

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{NC_{ox}} T_{Si}} = \sqrt{\frac{\varepsilon_{Si}}{N\varepsilon_{ox}} T_{Si} T_{ox}} \text{ ,} \qquad (5\text{-}1)$$

where C_{ox} is the gate capacitance per unit area. ε_{ox} and ε_{Si} are the relative permittivity of the gate dielectric and the Si channel region, respectively, and T_{ox} and T_{Si} are the physical thickness of the gate dielectric and the Si or poly-Si channel region, respectively. The value, N, means the number of the gate electrodes. The physical meaning of λ is the extension of the electric field lines from the drain electrode in the Si channel region. In addition to an increase of the number of the gate electrodes, reducing the poly-Si film thickness and EOT also results in shorter λ. If λ is 5 to 10 times smaller than L_G, SCEs can be well controlled. The device characteristics of poly-Si NW TFTs with the multi-gate structures were investigated [10-11]. As L_G scales from 400 nm to 100 nm, SCEs can be effectively eliminated. Moreover, the high-κ gate dielectric extensively used in conventional Si MOSFETs was also integrated into poly-Si TFTs to reduce the EOT and eliminate SCEs [12-13]. Reference [13] using the HfO_2 gate dielectric also reveals good SCEs as L_G is scaled down to 100 nm. The ultra-short-channel characteristics (L_G < 100 nm) of poly-Si TFTs have seldom been reported in the literature but become very important for device scaling in the future. In this work, the ultra-thin and narrow poly-Si body, the multi-gate structure, and the HfO_2 gate dielectric are completely integrated together

on our ultra-short-channel poly-Si NW TFTs, thus good short-channel characteristics can be demonstrated by structural engineering.

(c) Driving capability

Some driving current (I_{ON}) values listed in Table 5-1 are still lower than 100 μA/μm due to their relatively long L_G ($L_G \geqq 1$ μm), unless the drain electrode is intentionally biased at higher voltages to raise their I_{ON} values. Therefore, for low-voltage operation, the driving capability of poly-Si TFTs is needed to be improved. The linear-region drain-to-source current (I_{DS}) equation of poly-Si TFTs deduced by J. Levinson *et al.* is shown below [19]:

$$I_{DS} = \mu_{EFF} \frac{W}{L_G} \exp\left(\frac{-V_B}{\kappa_B T}\right) C_{ox} (V_{GS} - V_{TH}) V_{DS}, \quad (5\text{-}2)$$

where μ_{EFF} is the field-effect mobility, W is the physical channel width, V_B is the effective grain-boundary barrier height, κ_B is Boltzmann's constant, T is absolute temperature, and V_{GS}, V_{TH}, and V_{DS} are the gate, threshold, and drain voltages, respectively. Based on the Levinson's current model, the high driving capability can be obtained by increasing μ_{EFF} and C_{ox} or decreasing L_G, V_B, and V_{TH}. Various grain-enhancement technologies mentioned before can effectively raise μ_{EFF} and lower V_B and V_{TH}. Similarly, EOT scaling not only suppresses SCEs but also enhances the driving capability. The L_G scaling, i.e. device scaling, is another direct method to enhance the driving capability. However, L_G scaling may degrade the driving capability if the parasitic S/D resistance effect occurs. Once the ultra-thin poly-Si film thickness and/or the poly-Si NW channel are adopted to suppress SCEs, the parasitic series resistance effect is more apparent. The standard self-aligned Ni-silicide process used in the current Si MOSFETs can be applied in poly-Si TFTs to relax the series resistance issue [20]. For our ultra-short-channel poly-Si NW TFTs,

the fully-Ni-silicided S/D is successfully formed during the MSB S/D process. Therefore, the high driving capability can also be achieved by structural engineering.

5.3 Device Fabrication

Figure 5-1 shows the main process flow and the schematic diagram of the GAA poly-Si NW TFTs integrated with the MSB S/D. This simple and CMOS-compatible process flow is described in detail below. First, a 150-nm-thick SiO_2 was thermally grown on a 6-inch (100)-oriented p-type Si substrate with a resistivity of 0.5-100 Ω-cm. Then, an 18-nm-thick amorphous Si film was deposited by a LPCVD system as an active channel layer. The amorphous Si film was recrystallized by a SPC annealing at 600 °C for 24 hr in N_2 ambient, and the active area composed of the poly-Si NW channel and S/D pad regions was defined by a top-down fabrication technology including electron-beam lithography (EBL), photoresist (PR) trimming [21], and reactive ion etching (RIE).

A simple method was used to fabricate the GAA structure. The wet oxide, whose length, width, and depth are 1 μm, 1 μm, and 70 nm, under the poly-Si NW channel was removed by EBL and buffer oxide etchant (BOE) wet etching and named the oxide opening region. Hence, the poly-Si NW channel was suspended from the wet oxide. Next, after the standard RCA cleaning process, a 30-nm-thick TEOS gate oxide and a 200-nm-thick in-situ phosphorus-doped poly-Si gate were sequentially deposited followed by a RTA at 1000 °C for 10 sec in N_2 ambient. The gate dopant activation process at 1000 °C for 10 sec can be replaced by 600 °C for 12 hr to reduce the thermal budget in 3D IC applications. We consider that the device characteristics can still be retained because of the rather thick gate oxide of our poly-Si NW TFTs. In this study, the GAA structure is only formed as the W is smaller than or equal to 200

nm. Devices with channel width wider than 200 nm belong to the planar-gate structure. Figure 5-2(a) shows the cross-sectional TEM micrograph along the gate direction. The poly-Si NW channel is completely surrounded by the TEOS gate oxide and the poly-Si gate, and the darker area under the poly-Si NW channel contains grains of the poly-Si gate with different orientations. Figure 5-2(b) is an enlarged cross-sectional view of Fig. 5-2(a). The final T_{Si} over the oxide opening region is reduced to 8 nm owing to the several cleaning processes, and the width of the narrowest channel is 35 nm. After patterning the poly-Si gate, a 20-nm-thick SiO_2 and a 20-nm-thick silicon nitride (Si_3N_4) were continuously deposited and etched to form a double spacer.

To reduce the series resistance of the poly-Si NW's S/D region, the MSB S/D was used on our poly-Si NW TFTs [14]. After removing the remnant TEOS oxide and/or native oxide on the poly-Si gate and S/D regions by DHF solutions, the composite Ni (6 nm)/TiN (10 nm) films was sequentially deposited by a PVD system. A low temperature and two-step Ni-silicidation process was used to form NiSi [14]. The first step was performed at 300 °C for 4 min in an ultra-high vacuum (UHV) environment to form di-nickel silicide (Ni_2Si) at the poly-Si gate and S/D regions. The purpose of the first annealing step is to avoid excessive lateral Ni-silicide encroachment. Then, the un-reacted Ni film was selectively removed by the mixture solution of H_2SO_4 and H_2O_2. The second step was performed by a RTA at 500 °C for 30 sec in N_2 ambient, and the Ni_2Si phase transformed into the low-resistivity NiSi phase. The SBH between the poly-Si NW channel and the NiSi S/D can be modified by an ITS technique followed by a drive-in annealing [14]. Phosphorus ions (P^+) were implanted into the NiSi S/D at 10 keV to a dose of $5x10^{15}$ cm^{-2}, then a furnace annealing at 600 °C for 30 min in an UHV environment was employed to form the

n-type S/D extension (SDE). The implanted dopants diffused out from the NiSi S/D and piled-up at the interface between the poly-Si NW channel and the NiSi S/D. The maximum process temperature of the MSB S/D process is 600 °C, so it is suitable for the poly-Si TFT application. Figure 5-3(a) displays the cross-sectional TEM micrograph along the channel direction. The shortest L_G is 30 nm, and the fully Ni-silicided S/D is successfully fabricated. The average grain size of the poly-Si channel inspected by plan-view TEM is about 55 nm, as shown in Fig. 5-3(b). The channel area of the smallest GAA poly-Si NW TFT is smaller than the average poly-Si grain size, so there are few grain boundaries in the ultra scaling channel region.

Finally, a-300 nm-thick passivation layer is a TEOS oxide formed by PECVD and deposited on all devices. After contact hole opening, a-500 nm-thick Al film was deposited and patterned to form the contact pads and finish the device fabrication. For the NH_3-passivated devices, after recording the fresh I-V characteristics, a NH_3 plasma treatment at 300 °C for 5 min was performed to passivate the grain-boundary defects in the poly-Si channel region. Therefore, the smallest GAA poly-Si NW TFT with NH_3 plasma treatment can be considered as the single-crystal-like logic device. During the NH_3 plasma treatment process, the RF power and the NH_3 flow rate were set to 200 W and 700 sccm, respectively. The transfer and output characteristics of the devices were measured with a HP 4156C semiconductor parameter analyzer. The device parameters are extracted from the transfer characteristics at a V_{DS} of 0.05 V. The linear-region V_{TH} (the n-type MSB device) is defined by the maximum transconductance (G_{mmax}) method. The constant-current V_{TH} (the Schottky barrier (SB) device) is defined as the V_{GS} at which $I_{DS}= W_{EFF}/L_G x10$ nA, where $W_{EFF}= 2x(W+T_{Si})$.

The maximum and minimum values of the I_{DS} within one I_{DS}-V_{GS} curve are designated as the I_{on} and I_{off}, respectively.

5.4 Results and Discussion

5.4.1 Process Consideration

(a) PR trimming

After electron-beam exposure and development, the minimum PR linewidth inspected by in-line SEM is about 50 nm owing to the resolution limit of the electron-beam system, as shown in Fig. 5-4(a). To obtain the narrowest poly-Si NW pattern, the PR ashing technique is employed in a low temperature oxygen (O_2) plasma environment to decrease the PR stripping rate and reduce the minimum PR linewidth further. The PR patterns were trimmed by O_2-plasma at an RF power of 900 W. Furthermore, the process temperature and the O_2 flow rate were set to 60 °C and 2400 sccm, respectively. The ashing time was varied to control the final PR linewidth. The PR ashing rate in the vertical or lateral direction was estimated by measuring the change in the PR thickness or linewidth before and after the PR ashing process. The average vertical ashing rate is around 0.5 nm/sec, and this value is slow enough for good linewidth control. The average lateral ashing rate and standard deviation are 0.549 nm/sec and 0.065 nm/sec, respectively. Figure 5-4(a) and 5-4(b) show the PR pattern before and after the PR ashing process. The minimum PR linewidth decreases from 51 nm to 32 nm after 40 sec O2-plasma ashing. The well-ashed line is observed with uniform shape, and the line edge roughness (LER) is not influenced by the PR ashing process. Over-ashing results in LER degradation and/or broken line, as shown in Fig. 5-5(a) and 5-5(b), respectively. As the ashing time increases to 140 sec, the line shape of the pre-ashed 80-nm-wide line becomes non-uniform or even broken.

The narrowest PR linewidth of the entire wire is 27 nm, as shown in Fig. 5-5(a). After completing the PR ashing process, the PR patterns were then transferred to the poly-Si film by RIE.

(b) Silicidation

For the metal S/D technology, the Ni-silicide film should have low-resistivity NiSi phase and good thermal stability to reduce the S/D series resistance, especially for the ultra-thin Ni-silicide film [22]. After completing the device fabrication, the final Ni-silicide film thickness is 8 nm near the poly-Si NW channel and 19 nm at S/D pad regions, as shown in Fig. 5-3(a) and 5-6, respectively. Formation of low-resistivity NiSi S/D is confirmed with XRD analysis, as shown in Fig. 5-7. However, the agglomeration phenomenon occurs at the NiSi S/D, as shown in Fig. 5-8. The R_s value of the agglomerated ultra-thin NiSi film measured by the four-point probe method is up to 163 Ω/□. Figure 5-9 shows the atomic force microscope (AFM) image of the NiSi S/D. The height difference between point and point in the AFM image is 19 nm and nearly equal to the NiSi film thickness. On the contrary, the surface morphology of the Ni-silicide film on the poly-Si gate region is still smooth owing to the thick Ni-silicide film, as shown in Fig. 5-8. The low thermal budget of the MSB S/D process still results in the agglomeration of the ultra-thin NiSi film.

The C I/I technology mentioned in chapter 2 can be used to enhance the thermal stability of the ultra-thin NiSi film, especially for the agglomeration issue. Therefore, before the NiSi S/D formation, C ions were implanted into the S/D region at 1 keV to a dose of $5x10^{15}$ cm^{-2}. Then, the same two-step Ni-silicidation process, as mentioned before, was performed to form NiSi, but the first step annealing time was prolonged from 4 min to 25 min. The reaction rate at 300 °C for the formation of Ni_2Si is slowed owing to the existence of a large amount of C atoms. After the NiSi MSB S/D

formation, the C-doped NiSi film is still smooth without any agglomeration, as shown in Fig. 5-10.

5.4.2 Basic SB and MSB Device Characteristics

While the NiSi S/D connects with the poly-Si NW channel, the metal-to-semiconductor contact provides an interfacial SB. Figure 5-11(a) and 5-11(b) present the transfer and output characteristics of the smallest SB device with L_G/W= 30 nm/35 nm, respectively. The ambipolar transport characteristics are clearly observed owing to the mid-gap NiSi S/D. The sub-linear phenomenon in the output characteristics indicates the high SBH at the source side. Therefore, the SBH should be tuned to achieve high-performance device characteristics.

Various methods have been proposed to lower the SBH between a metal and a semiconductor, such as introducing an interfacial dipole [23], using low barrier silicides [24], passivating dangling bonds [25], and inserting a thin interfacial insulating layer [26]. In this work, we adopt the ITS technique followed by a drive-in annealing to adjust the SBH and form the n-type MSB S/D [14]. The width of the source-side Schottky barrier of the n-type MSB device becomes thin enough for electron tunneling owing to the thin and high concentration SDE layer. The source-side Schottky barrier is almost transparent to electron conduction, so high I_{ON} can be obtained. On the other hand, as the n-type MSB device is biased in the off-state, the width of the drain-side Schottky barrier becomes thick enough to prevent hole tunneling leakage currents. Figure 5-12(a) and 5-12(b) present the typical transfer and output characteristics of the smallest n-type MSB device with L_G/W= 30 nm/35 nm, respectively. Comparing with the electrical characteristics of the SB device, we find that the n-type MSB device exhibits better performance including higher I_{ON}, lower

leakage currents (I_{OFF}), lower V_{TH}, and steeper S.S.. The ambipolar conduction behavior transforms to unipolar channel operation. Due to the thin poly-Si channel, our GAA poly-Si NW device can be regarded as a planar fin or a double-gate ultra-thin body (UTB) device. The aspect ratio (T_{Si}/W) of the smallest MSB device with L_G/W= 30 nm/35 nm is 0.229, which is much higher than that of the conventional planar poly-Si TFT ($T_{Si}/W << 0.1$). The channel electric potential can be tightly controlled by the GAA poly-Si gate electrode even if the rather thick gate oxide. Therefore, the transfer characteristics of the smallest n-type MSB device show good switch performance. Furthermore, from the output characteristics, the sub-linear phenomenon also disappears, which indicates that the I_{ON} is no longer limited by the source-side Schottky barrier.

5.4.3 Effect of the S/D Series Resistance

As the technology node continuously scales down to sub-100 nm, the S/D series resistance becomes a serious problem and results in the I_{ON} degradation [27]. Therefore, many studies focus on the metal S/D technology [24]. For the n-type MSB device with the ultra-short L_G of 30 nm, to investigate the S/D series resistance effect on its device turn-on characteristics, the external loading method (ELM) proposed by S. T. Hsu is adapted to extract the parasitic S/D resistance [28]. The major advantage of this method is that it requires only single device and dc-voltage sweep measurements for the parameter extraction. The equivalent circuit diagram is depicted in Fig. 5-13. During the measurement, the source terminal of the n-type MSB device is connected to an external load resistor. The linear-region transfer characteristics are measured with different external load resistance (R_L), as shown in Fig. 5-14. There is a serious degradation in the I_{ON} with high R_L. The S/D series resistance can be

extracted from these transfer characteristics, and the parameter extraction process is described below. The I_{DS} of conventional Si MOSFETs in the linear region is expressed by:

$$I_{DS} = \frac{W}{L_G}\mu C_{ox}\left(V_{GS} - V_{TH} - \tfrac{1}{2}V_{DS}\right)V_{DS}, \tag{5-3}$$

where μ is carrier mobility.

In addition to R_L, the S/D series resistance (R_S and R_D) is also considered into the equivalent circuit, as shown in Fig. 5-13. Assuming the device is biased in the linear region, the voltage drop across the resistors is proportional to the I_{DS} flowing through them. Therefore, the actual gate-to-source voltage (V'_{GS}) and drain-to-source voltage (V'_{DS}) across the n-type MSB device is smaller than the bias V_{GS} and V_{DS}. If we consider the equivalent circuit containing three resistors, the I_{DS} of conventional Si MOSFETs in the linear region is modified and given by:

$$\begin{aligned} I_{DS} &= \frac{W}{L_G}\mu C_{ox}\left(V'_{GS} - V_{TH} - \tfrac{1}{2}V'_{DS}\right)V'_{DS} \\ &= \frac{W}{L_G}\mu C_{ox}\left\{\left[V_{GS} - I_{DS}(R_S + R_L) - V_{TH}\right] - \tfrac{1}{2}\left[V_{DS} - I_{DS}(R_S + R_D + R_L)\right]\right\}\left[V_{DS} - I_{DS}(R_S + R_D + R_L)\right] \end{aligned} \tag{5-4}$$

As we choose the suitable external load resistors to satisfy the inequality (5-5), equation (5-4) can be simplified and rearranged to equation (5-6):

$$V_{GS} - V_{TH} - \tfrac{1}{2}V_{DS} >> \tfrac{1}{2}I_{DS}\left|R_D - R_S - R_L\right|, \tag{5-5}$$

$$\frac{1}{I_{DS}} = \frac{R_T + R_L}{V_{DS}} + \frac{1}{\frac{W}{L_G}\mu C_{ox}\left(V_{GS} - V_{TH} - \tfrac{1}{2}V_{DS}\right)}, \tag{5-6}$$

where $R_T = R_S + R_D$ represents the total external resistance of the device. By plotting $1/I_{DS}$ versus R_L with V_{GS} as a parameter (shown in Fig. 5-15), the x-axis intersection gives R_{L0} which can be expressed as follows:

$$-R_{L0} = R_T + \left(\frac{W}{L_G}\mu C_{ox}\right)^{-1}\left(V_{GS} - V_{TH} - \frac{1}{2}V_{DS}\right)^{-1} \tag{5-7}$$

Next, by plotting $-R_{L0}$ as a function of $(V_{GS}-V_{TH}-0.5V_{DS})^{-1}$, the slope and y-axis intersection gives carrier mobility and R_T, respectively. Figure 5-16 shows the extracted results of the n-type MSB device with L_G/W= 30 nm/35 nm. Although the ultra-thin NiSi film has agglomerated in S/D pad regions (shown in Fig. 5-17), the extracted S/D series resistance of 0.299 kΩ-μm is still lower than that of the conventional device with T_{Si}= 40 nm reported in reference [29]. Furthermore, the extracted electron mobility is 33.8 cm^2/V-sec. This value is close to the field-effect electron mobility of 28.9 cm^2/V-sec calculated from the G_{mmax}. After excluding the S/D series resistance effect, the field-effect electron mobility is raised to 31.2 cm^2/V-sec. We consider that the parasitic S/D resistance is originated from the unagglomerated NiSi NW regions instead of the agglomerated NiSi S/D pad regions. Therefore, even if the agglomeration of the NiSi S/D pad regions takes place, it has less effect on the n-type MSB device with the ultra-short L_G of 30 nm.

For large-area poly-Si TFTs crystallized by SPC, the carrier conduction is restricted by the scattering at the grain boundary. By reducing the grain-boundary defect density with device scaling, we expect that the low carrier mobility can be improved owing to the decrease in grain-boundary scattering. However, according to the extracted results, the field-effect electron mobilities of many different devices with the same W of 35 nm are almost independent of L_G. Even if the active device area is smaller than the average poly-Si grain size, the extracted electron mobility of the smallest n-type MSB device with L_G/W= 30 nm/35 nm is 33.8 cm^2/V-sec. This value is only slightly higher but close to that of large-area poly-Si TFTs crystallized by SPC and could be explained as follows. First, we discuss the influence of Coulomb

scattering induced by the charged interface states. The effective interface state density (N_{it}) near the poly-Si/SiO_2 interface can be estimated from the equation shown below [30]:

$$N_{it}=\left[\left(\frac{S.S.}{\ln 10}\right)\left(\frac{q}{\kappa T}\right)-1\right]\left(\frac{C_{ox}}{q}\right) \quad (5\text{-}8)$$

The N_{it} value of the n-type MSB device with L_G/W= 30 nm/35 nm is 1.703×10^{12} cm^{-2}, which is about two orders of magnitude higher than that of conventional Si MOSFETs. Therefore, the high density of the interface states can capture electrons during device operation. The trapped electrons located at the interface can act like charged scattering centers and thus lower the electron mobility. For our GAA poly-Si NW TFTs, the poly-Si body is thin enough that the entire channel is close to the interface and strongly affected by scattering centers at the interface. Furthermore, it has been reported that surface roughness scattering dominates with decreasing the Si layer thickness owing to the high geometrical confinement of the electrons [31]. Surface roughness scattering is related to the magnitude of the transverse electrical field and dominates at high V_{GS}. Therefore, Coulomb scattering and surface roughness scattering should both be taken into account due to the increase of electron confinement originated from the UTB structure. The low electron mobility can be attributed to the combination of these two scattering effects. For poly-Si NW TFTs, the interface trap density at the poly-Si/SiO_2 interface and surface roughness should be reduced to improve the carrier mobility.

5.4.4 Short-Channel and Narrow-Width Characteristics

Figure 5-18(a), 5-18(b), and 5-18(c) show the statistics of the V_{TH}, DIBL, and I_{ON} values of the n-type MSB devices with fixed W= 35 nm and various L_G,

respectively. The I_{ON} value is normalized by the effective channel width (I_{DS}/W_{EFF}) and defined as the device is biased at V_{GS}-V_{TH}= 5 V and V_{DS}= 1 V. Each solid square in these three figures presents the average value calculated from ten devices with the same dimension. The V_{TH} roll-off phenomenon occurs as L_G is smaller than 100 nm, and the average DIBL value as L_G= 30 nm is around twice lager than that as L_G= 160 nm owing to a-30nm-thick TEOS gate oxide. These results imply that the SCE can be further improved by reducing the gate oxide thickness. The I_{ON} continuously increases with decreasing L_G, which means that the S/D series resistance effect is not apparent. The average I_{ON} value as L_G= 30 nm can achieve up to 288 μA/μm. We consider that the considerable device-to-device variation is mainly originated from the non-uniform encroachment of Ni silicide onto the poly-Si channel region. Excessive Ni-silicide encroachment can lead to low V_{TH} and high DIBL and I_{ON} values.

Figure 5-19(a), 5-19(b), and 5-19(c) show the statistics of the V_{TH}, DIBL, and I_{ON} values of the n-type MSB devices with fixed L_G= 30nm and various W, respectively. As W is much larger than T_{Si}, the GAA structure can also be regarded as a double-gate (top and bottom gates) structure. Therefore, the V_{TH} and DIBL values are less dependent on W. However, the two sides of the GAA structure become more efficient as W is reduced to 35 nm. In addition to the top- and bottom-gate electrodes, gate stacks can further tightly control the channel potential via the two sides of the GAA structure so that the V_{TH} and DIBL values obviously decrease as W= 35 nm. We find that the I_{ON} continuously decreases as W gradually increases. This phenomenon could be explained by the corner effect in GAA poly-Si NW TFTs. Due to field crowding at the corner, the enhanced electric fields will induce more charge in the inversion layer. The corner effect is more obvious with the decrease in W. Therefore, the increased inversion-layer carrier density results in the I_{ON} enhancement.

5.4.5 Temperature-Dependent Transfer Characteristics

For poly-Si TFTs, the grain-boundary traps in the poly-Si channel region can capture the carriers induced by the V_{GS} and then form the grain-boundary potential barriers. The higher the grain-boundary trap density, the greater the potential barrier at the grain boundary. When the carriers drift or diffuse along the channel direction, the grain-boundary potential barriers plays an important role for current transport. Source-side carriers having sufficient thermal energy can surmount the source potential barrier and the grain-boundary potential barriers and thus arrive at the drain electrode. Therefore, the current transport mechanism in the poly-Si channel region is considered as a thermionic emission process. For large-area and small-grain poly-Si TFTs, current transport is highly temperature dependent owing to their higher effective grain-boundary barrier height. The temperature-dependent transfer characteristics of the n-type MSB device with L_G/W= 5 μm/5 μm are shown in Fig. 5-20(a). The I_{OFF} and S.S. obviously increase but the V_{TH} decreases with the increase of the measurement temperature, which indicates that the current transport mechanism in the weak inversion region is dominated by thermionic emission. The temperature-dependent and V_{GS}-independent I_{OFF} results from the junction leakage currents. The temperature dependences of these parameters observed in the weak inversion region are similar with those found in conventional Si MOSFETs. According to Fig. 5-20(b) and 5-20(c), the I_{ON} of the n-type MSB device with L_G/W= 5 μm/5 μm also increases with the increase of the measurement temperature, so the current transport mechanism in the strong inversion region is still dominated by thermionic emission. This phenomenon can be explained by the continued existence of the grain-boundary potential barriers in both weak and strong inversion regimes. However, the current transport mechanism of the conventional Si MOSFETs biased in

the strong inversion region will transfer from thermionic emission to drift-diffusion model because there are no grain boundaries existing in the single-crystalline Si channel. The source potential barrier is eliminated under the influence of the V_{GS}, so the drift-diffusion current becomes the main mechanism of current transport and decreases with the increase of the measurement temperature owing to the degradation of the phonon-limited mobility. Therefore, the temperature dependence of the thermionic emission mechanism is opposite to that of the drift-diffusion mechanism. The only different temperature-dependent trend between large-area poly-Si TFTs and conventional Si MOSFETs is the I_{ON} so that we can study the influence of the grain-boundary potential barriers within the poly-Si channel by temperature measurements.

Next, the current transport mechanism of small-area poly-Si TFTs is discussed. Figure 5-21(a) shows the temperature-dependent transfer characteristics of the smallest n-type MSB device with L_G/W= 30 nm/35 nm. Figure 5-21(b) and 5-21(c) show the temperature-dependent I_{ON} with V_{DS}= 0.05 and 1 V, respectively. It is well known that the number of the grain boundary in the poly-Si channel region can be significantly reduced by decreasing the gate area. Furthermore, the effective grain-boundary potential barrier heights can be lowered by the double-gate and ultra-thin channel structures [32]. Therefore, for the I_{ON} with V_{DS}= 0.05 V, as the measuring temperature is increased to 375 K, the thermionic emission mechanism is replaced by the drift-diffusion mechanism. Furthermore, the drain-induced grain barrier lowering (DIGBL) effect is more apparent at V_{DS}= 1 V, so the grain-boundary potential barriers almost disappear under this bias condition. The temperature-dependent transfer characteristics are the same as those of conventional Si MOSFETs, as shown in Fig. 5-21(c). Therefore, the smallest n-type MSB device

with L_G/W= 30 nm/35 nm can be considered as a single-crystal-like device. Figure 5-22 is a plot of the transconductance as a function of the V_{GS} for various measuring temperature. The G_{mmax} value decreases with increasing the measuring temperature owing to the electron mobility degradation caused by phonon scattering. Furthermore, it is clear from Fig. 5-22 that the surface roughness scattering dominates another scattering mechanism and degrades the electron mobility at high V_{GS}.

5.4.6 Effect of NH_3-Plasma Treatment

It is well known that the NH_3-plasma passivation can effectively improve the device characteristics of poly-Si TFTs because the grain-boundary defects of the poly-Si film and the interface states at the poly-Si/SiO_2 interface are passivated by hydrogen and nitrogen [7]. The decrease in the grain-boundary scattering results in an increase in carrier mobility and the I_{ON}. The V_{TH} and S.S. are also improved, as well as the I_{OFF} originating at the grain-boundary defects. Therefore, in order to further improve the device performance, the NH_3-plasma treatment process is performed on our GAA poly-Si NW TFTs.

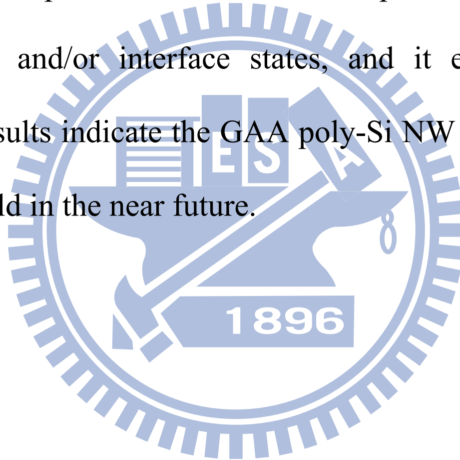
Figure 5-23(a) compares the transfer characteristics of the smallest n-type MSB device with L_G/W= 30 nm/35 nm before and after the NH_3 plasma passivation. After the NH_3-plasma treatment process, the transfer characteristics of the n-type MSB device are drastically improved and has excellent performance compared to those of the non-NH_3-passivated n-type MSB device. The V_{TH}, S.S., and DIBL values decrease to 0.97 V, 224 mV/Dec., and 0.895 V/V, respectively. Before the NH_3-plasma treatment process, grain-boundary barriers play important role on current transport and the barriers close to the drain electrode can be reduced more effectively as the V_{DS} increases. Therefore, the DIBL effect is apparent. After the NH_3-plasma

treatment process, the grain-boundary barriers are lowered. The transport of electrons becomes dominated by the source-to-channel barrier, and the drain electric field has less influence on the source-to-channel barrier lowering owing to the GAA structure. Therefore, the DIBL effect can be improved. The I_{on}/I_{off} current ratio is raised to $5x10^7$ at V_{DS}= 1V. We believe that the V_{TH}, S.S., DIBL, and I_{ON} values could be further improved by scaling EOT to get better gate controllability. The severe gate-induced-drain-leakage (GIDL) off-state currents may result from the excess encroachment of Ni silicide. Figure 5-23(b) shows the typical output characteristics of the NH_3-passivated n-type MSB device with L_G/W= 30 nm/35 nm. The normalized I_{ON} (I_{DS}/W_{EFF}) at V_{GS}-V_{TH}= 5 V and V_{DS}= 1 V is 187 μA/μm. If normalized to the drawn channel width, the driving current can be as high as 459 μA/μm. As we compared the device characteristics of the NH_3-passivated n-type MSB device with the state-of-the-art poly-Si TFTs listed in references [8-11], our device shows the best driving current value due to the ultra-short L_G and fully Ni-silicided S/D.

5.5 Conclusions

The smallest workable GAA poly-Si NW TFT with the ultra-short L_G of 30 nm has been successfully demonstrated. Thanks to the UTB and GAA structures, the channel electric potential can be well controlled by the gate electrode in spite of a rather thick TEOS gate oxide. The MSB S/D structure reduces the thermal budget and also helps the control of SCEs and reduction of parasitic resistance. Although the grain-boundary defect density can be reduced with device scaling, the electron mobility is still limited by other scattering mechanisms. Owing to the UTB device structure, Coulomb scattering and surface roughness scattering can have a very strong influence on the electron mobility. The high density of interface traps at the

poly-Si/SiO_2 interface and significant surface roughness results in low electron mobility. As a result, low interface trap density and control of surface roughness of poly-Si are both needed to improve the electron mobility for poly-Si NW TFTs with the ultra-short L_G. From the transfer characteristics of the smallest GAA poly-Si NW TFT measured at various temperatures, it reveals that the on-state current transport mechanism of poly-Si TFTs is no longer limited by thermionic emission and transforms to drift-diffusion transport. The influence of grain-boundary barrier height on the turn-on behavior of the smallest GAA poly-Si NW TFT is ignored at V_{DS}= 1 V, so the smallest GAA poly-Si NW TFT can be regarded as the single-crystal-like device. The additional NH_3 plasma treatment was adopted to effectively passivate the grain boundary defects and/or interface states, and it exhibits excellent device characteristics. These results indicate the GAA poly-Si NW TFT would be promising for the 3D IC or SOP field in the near future.



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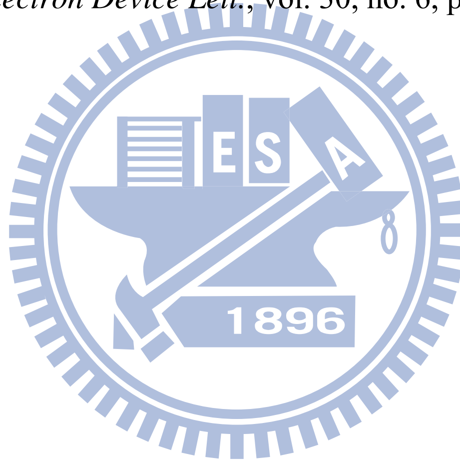


Table 5-1 Summary of main device parameters of the state-of-the-art high-performance poly-Si TFTs.

Reference #	**[5]**	**[6]**	**[10]**	**[11]**	**[12]**	**[13]**	**This work**
Crystalliza -tion technique	ELA	MILC	SPC	NONE	SPC	SPC	**SPC**
Gate dielectric	SiO_2 (8nm)	SiO_2 (40nm)	SiO_2 (20nm)	SiO_2 (1.7nm)	Pr_2O_3 (18nm)	HfO_2 (27.7nm)	**HfO_2 (10nm)**
Gate structure	Single gate	Single gate	Tri-gate	Ω-shaped	Single gate	Single gate	**Ω-shaped**
L_G/W	10μm/10 μm	1μm/45 nm	400nm/8 nm	100nm/14 nm	10μm/10 μm	100nm/1 μm	**40nm/20 nm**
I_{ON} (μA/μm)	~2	80	145	40	~0.2	136	**275**
S.S. (mV/Dec.)	78	260	100	79	253	280	**248**
DIBL (mV/V)	~0	256	10	78	~128	~0	**760**

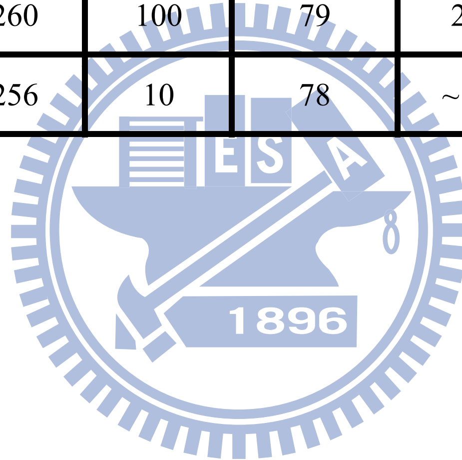
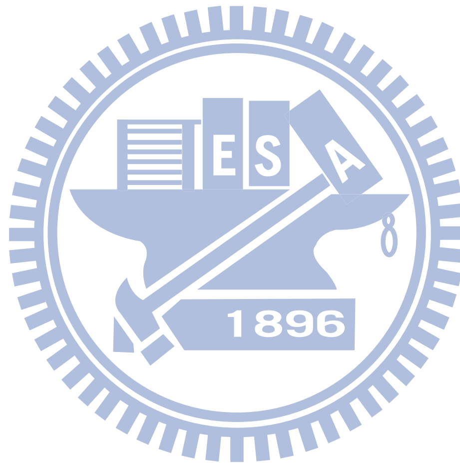


Table 5-2 Comparison of various crystallization techniques.

	SPC	ELA	MILC
Grain size	**< 0.1 μm**	**0.3-0.6 μm**	**> 0.6 μm**
Grain orientation	**random**	**random**	**{1 1 0}**
Grain boundary location	**non-controllable**	**controllable**	**controllable**
Advantages	**1. simplicity** **2. low cost** **3. uniformity** **4. large area capacity**	**1. low-temperature process**	**1. low-temperature fabrication (500-550 °C)** **2. low cost** **3. batch process**
Disadvantages	**1. high crystallization temperature (600 °C)**	**1. high initial cost** **2. high process complexity**	**1. metal contamination** **2. high intragrain defect density**



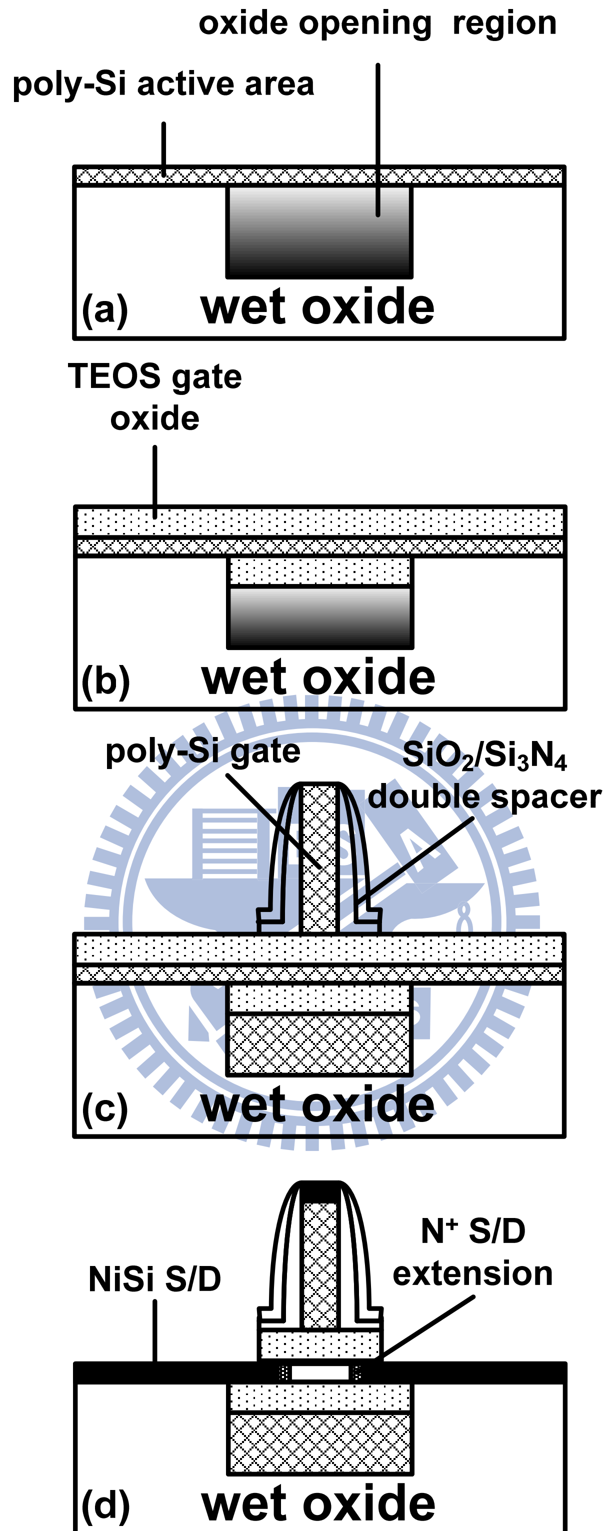


Fig. 5-1 Main process flow of the GAA poly-Si NW TFT integrated with the MSB S/D: (a) after the oxide opening region definition, (b) after the TEOS gate oxide deposition, (c) after a double spacer formation, and (d) the final device structure.

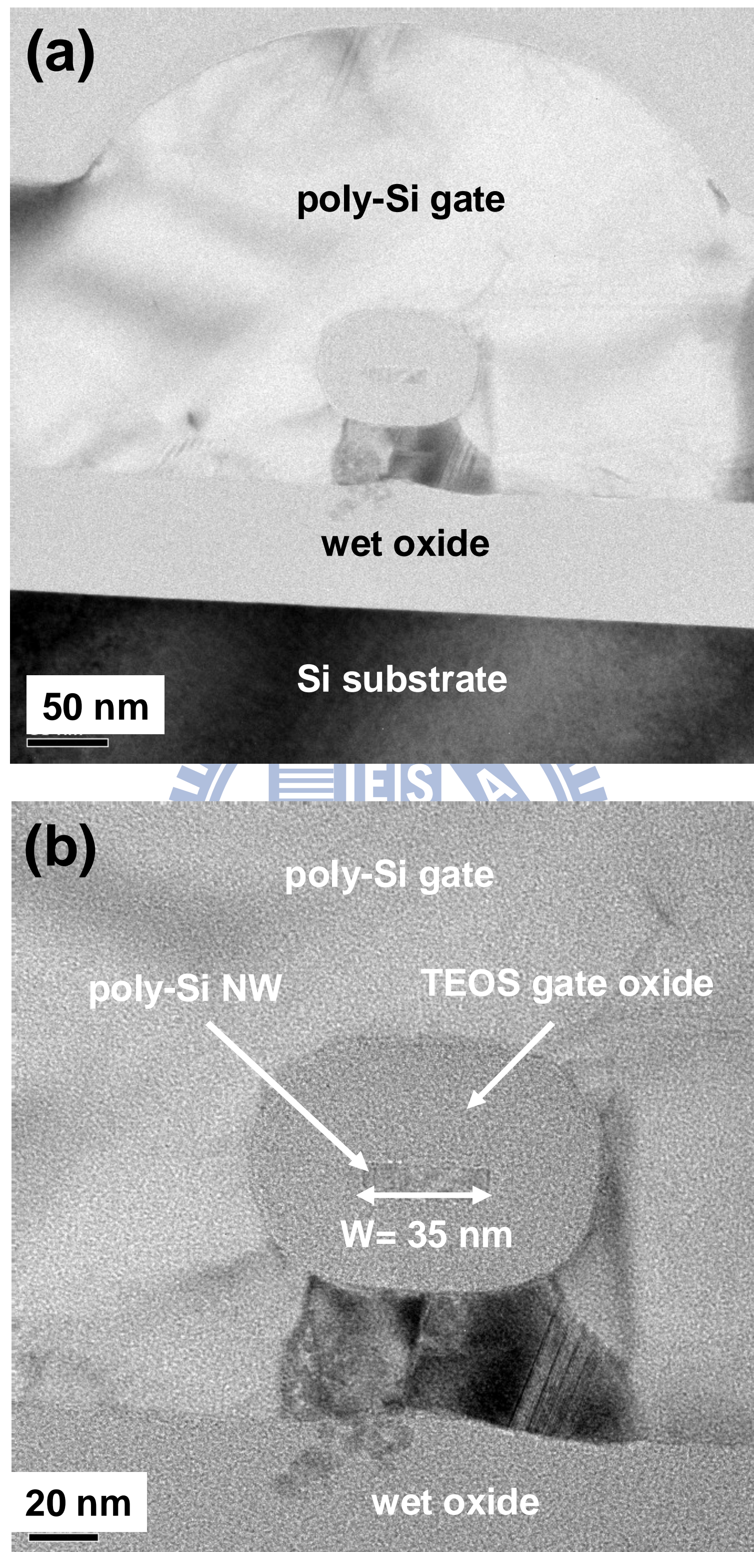
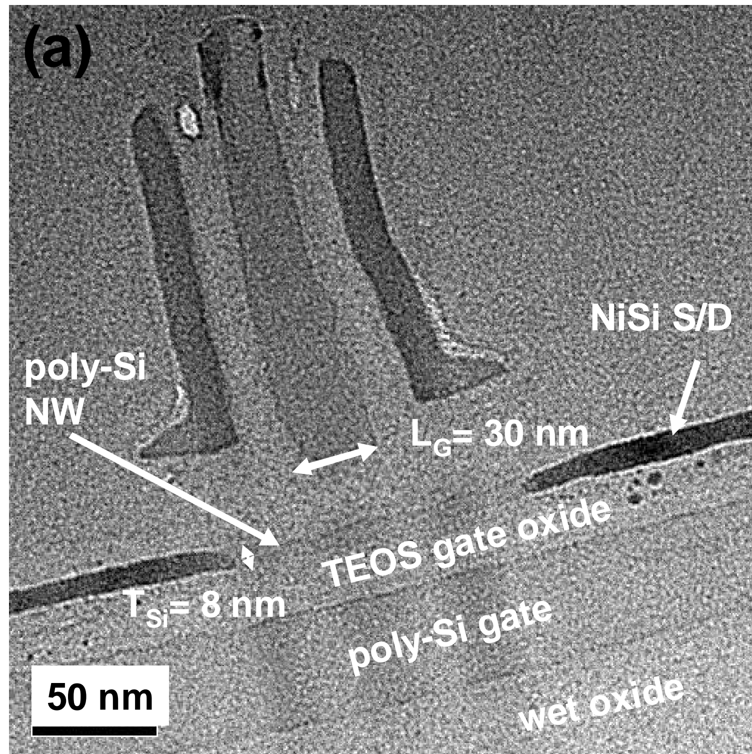


Fig. 5-2 (a) Cross-sectional TEM image of the GAA poly-Si NW TFT along the gate direction with L_G/W= 200 nm/35 nm. (b) Enlarged cross-sectional view of (a).



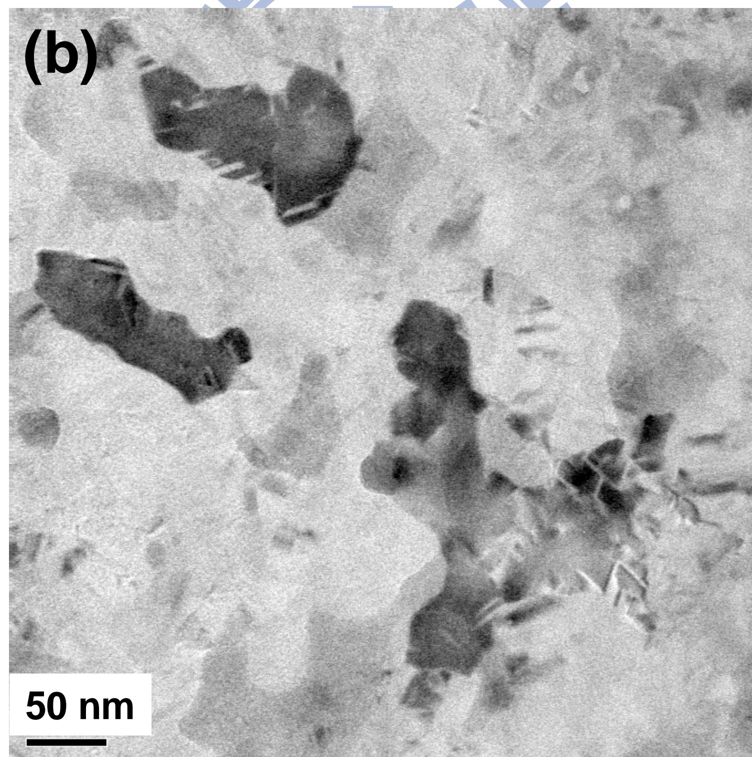


Fig. 5-3 (a) Cross-sectional TEM image of the GAA poly-Si NW TFT along the channel direction with L_G/W= 30 nm/35 nm. (b) Plan-view TEM of the ultra-thin poly-Si channel.

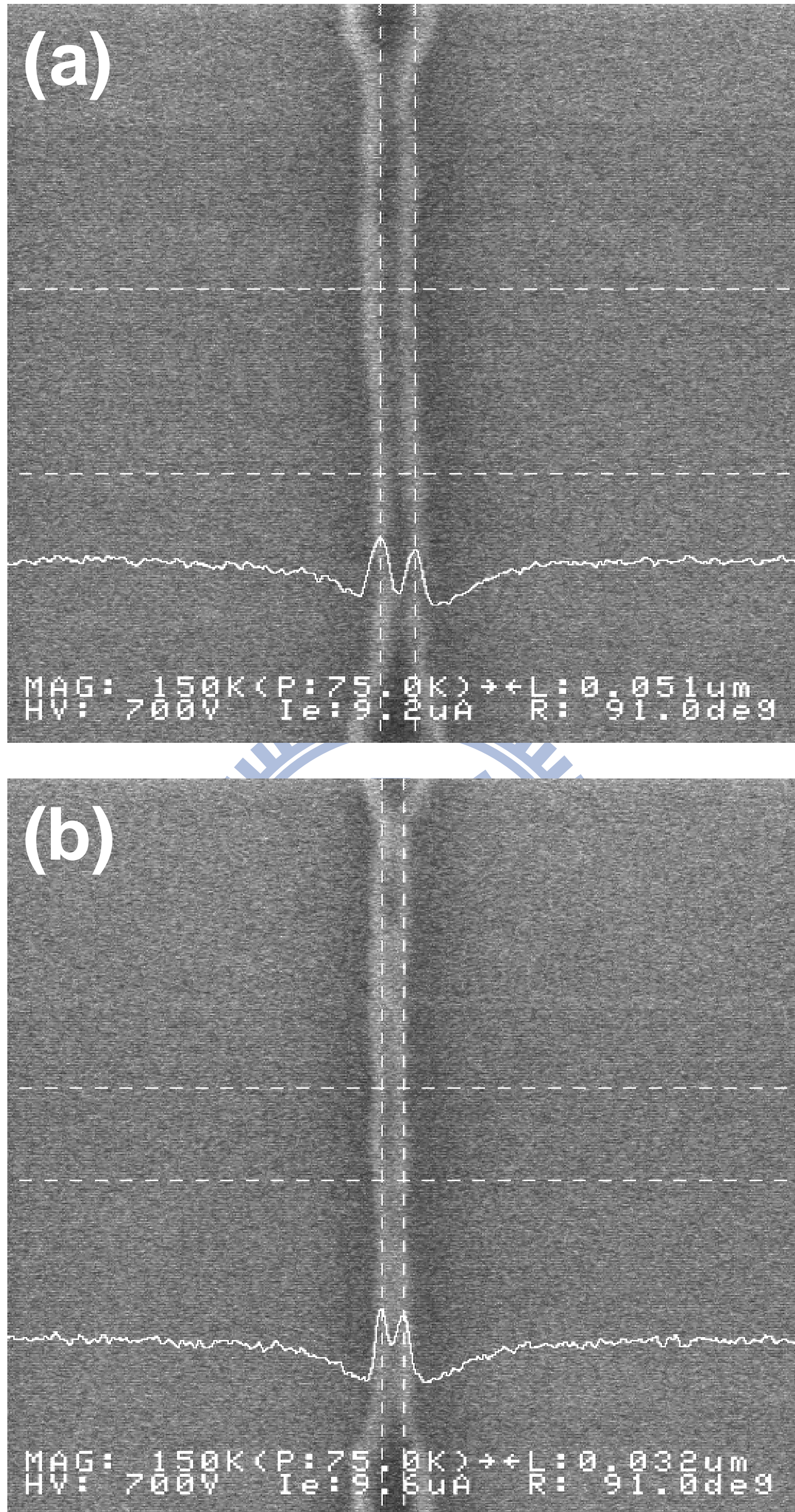
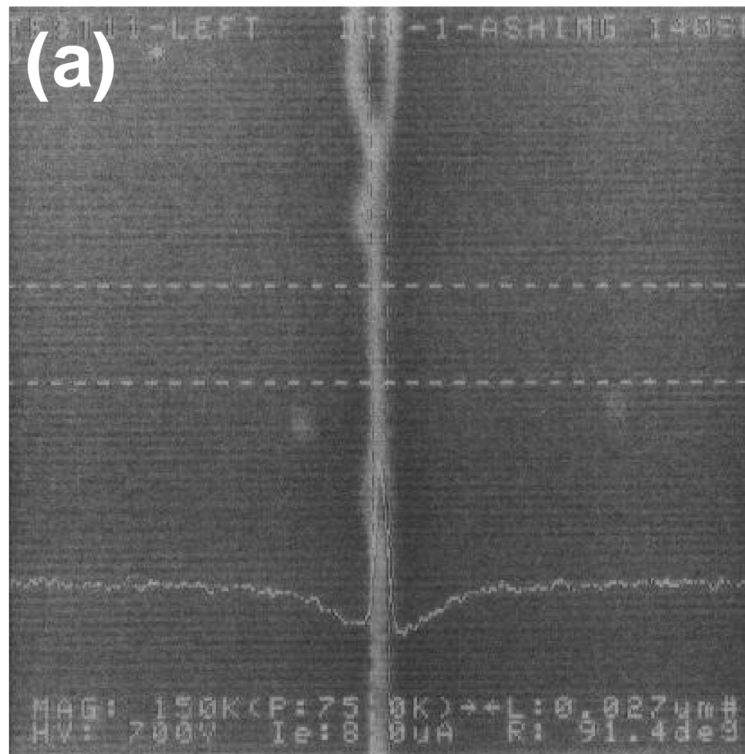


Fig. 5-4 Top-view SEM image of the active area: (a) after EBL and (b) after the PR ashing process with the ashing time of 40 sec.



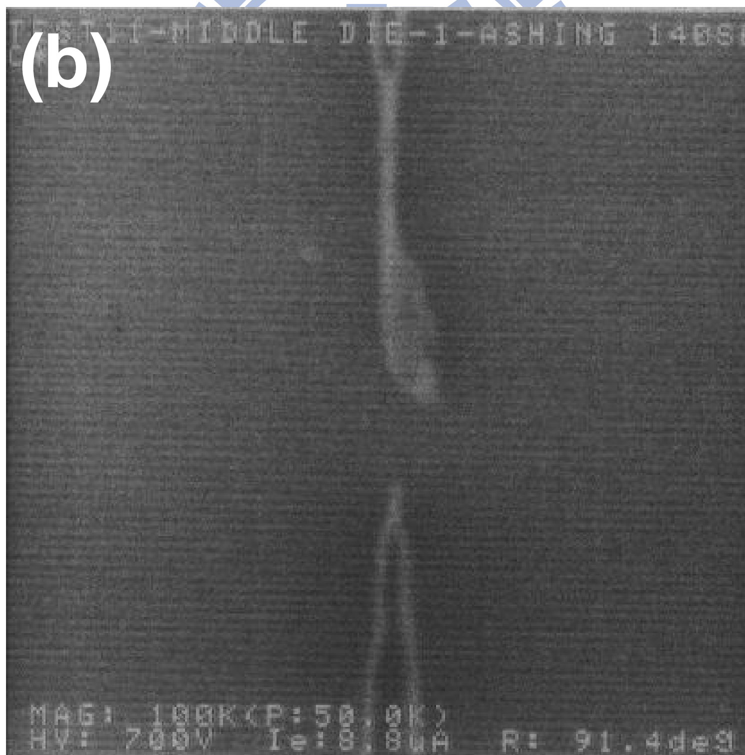


Fig. 5-5 Top-view SEM image of the active area after the PR ashing process with the ashing time of 140 sec: (a) LER degradation and (b) the broken line.

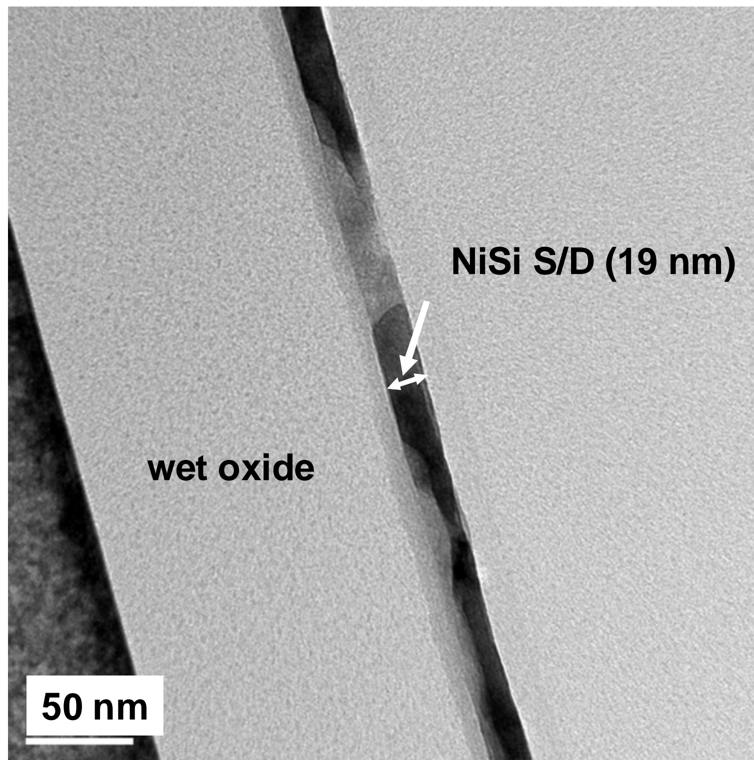


Fig. 5-6 Cross-sectional TEM image of the NiSi film at S/D pad regions.

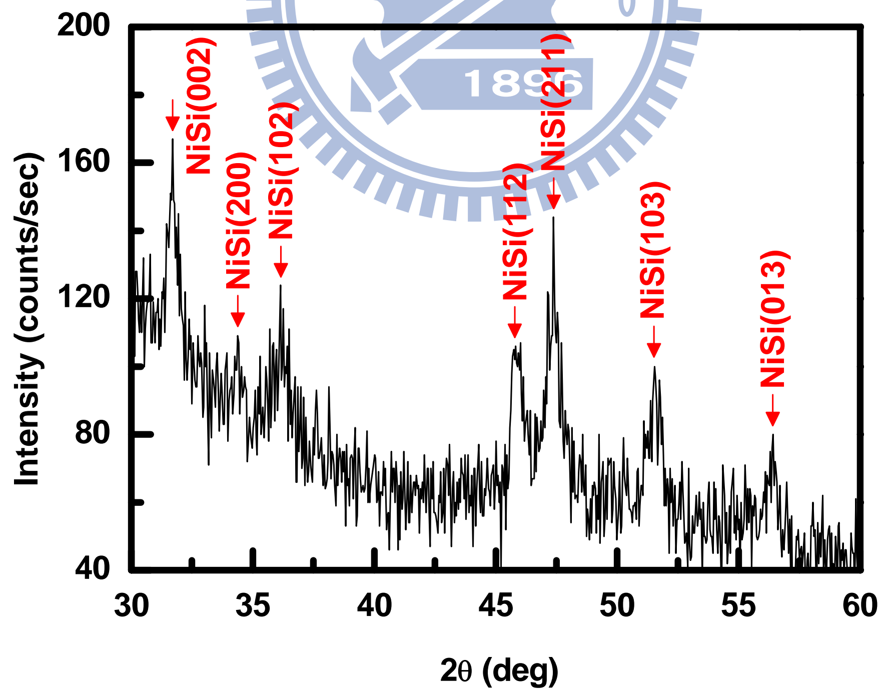


Fig. 5-7 XRD spectra of the NiSi film on SiO_2/Si substrate after completing the device fabrication.

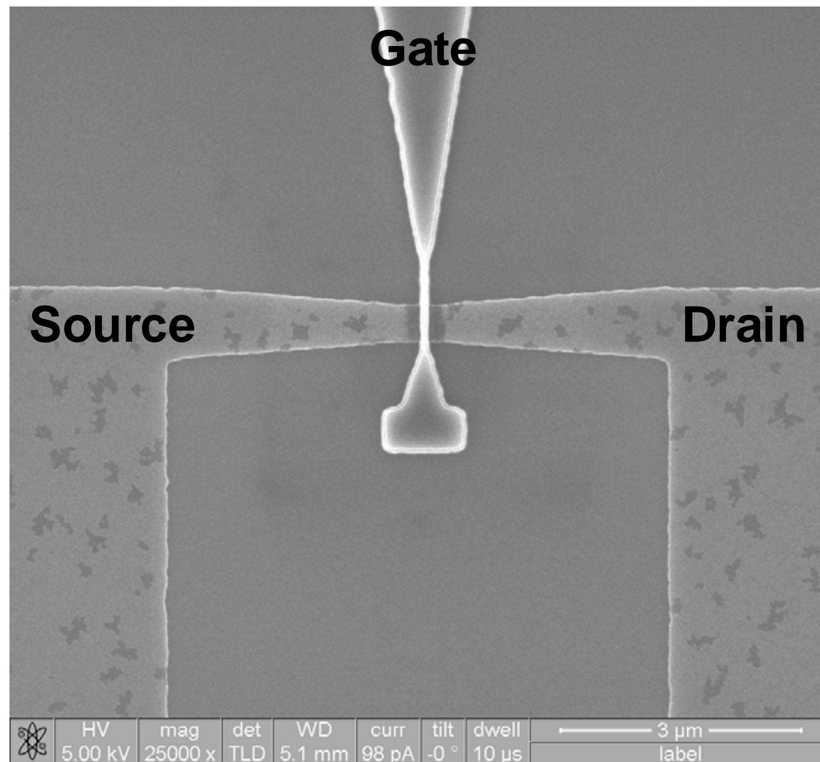


Fig. 5-8 Top-view SEM image of the fabricated poly-Si NW TFT with L_G/W= 30 nm/500 nm.

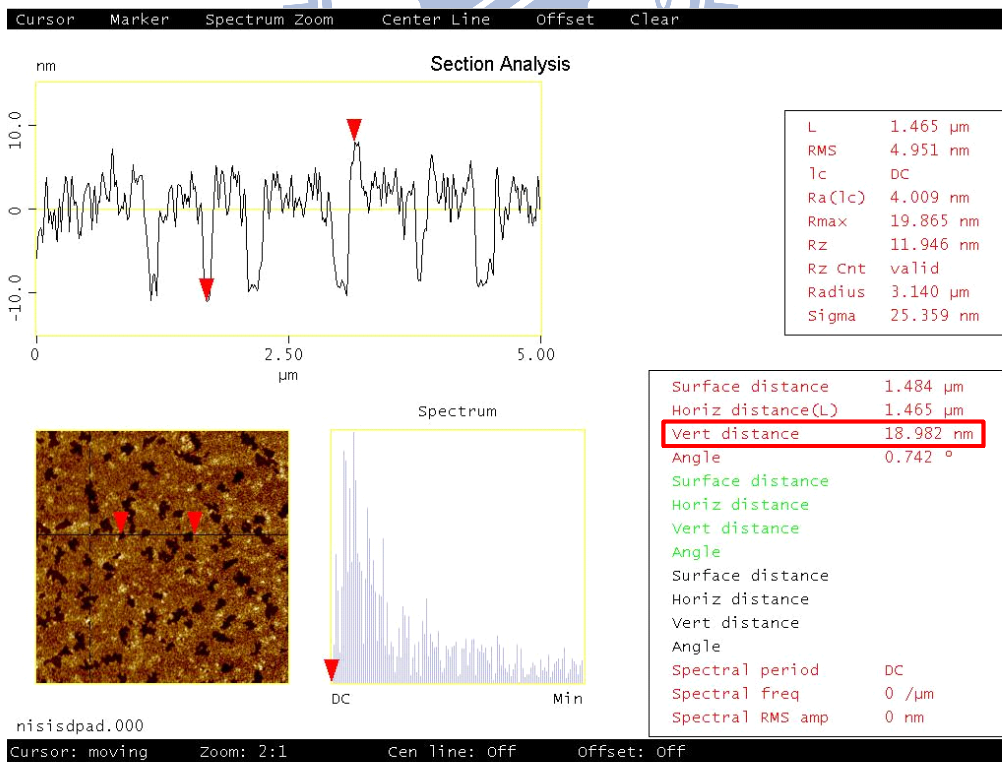


Fig. 5-9 AFM image of the NiSi film at S/D pad regions.

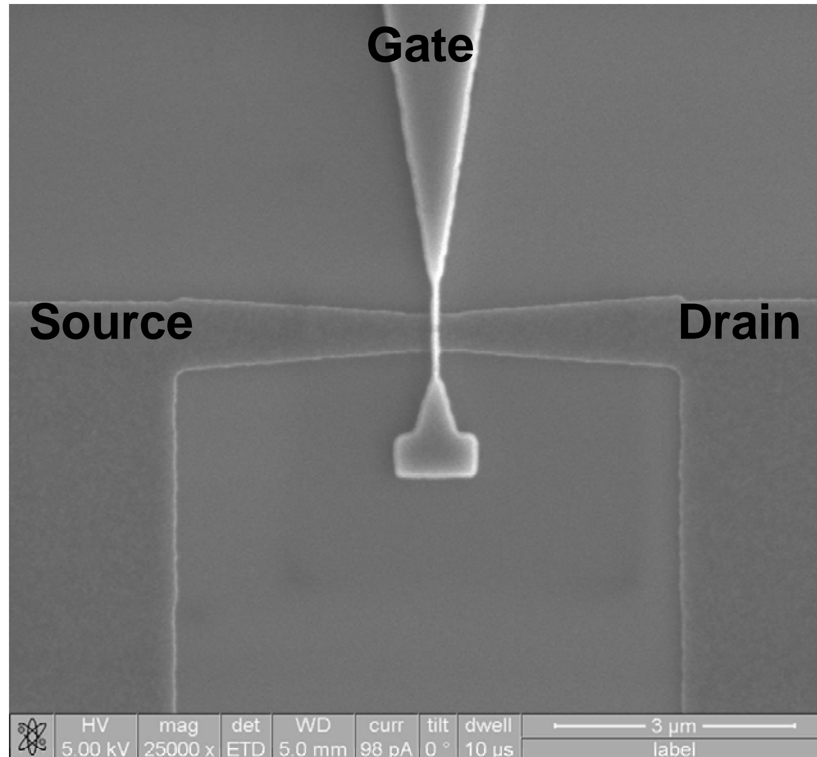


Fig. 5-10 Top-view SEM image of the NiSi film at S/D pad regions implanted with C ions at 1 keV to a dose of $5x10^{15}$ cm^{-2}.

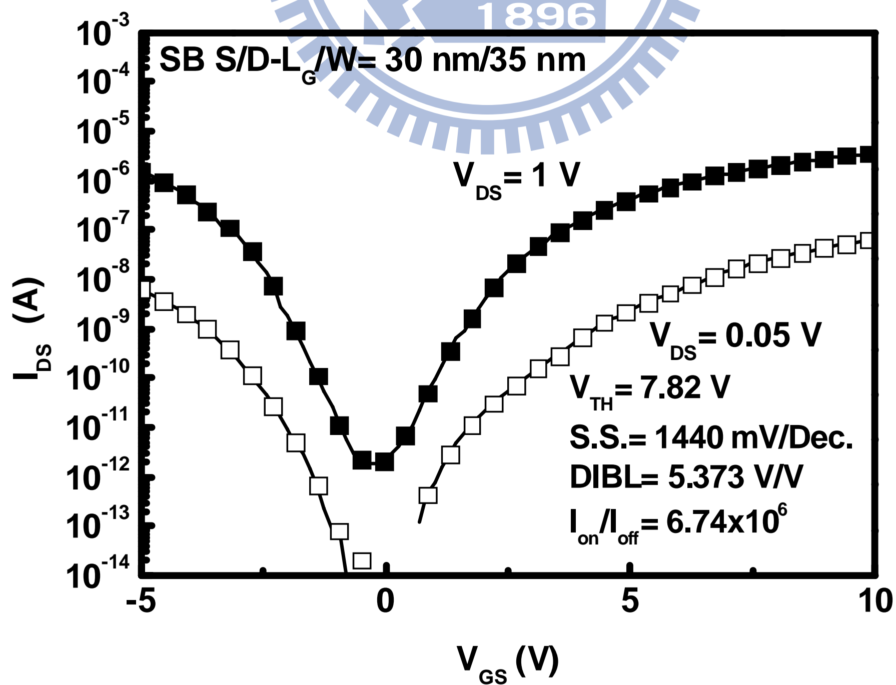


Fig. 5-11 (a) Transfer characteristics of the smallest SB device with L_G/W= 30 nm/35 nm.

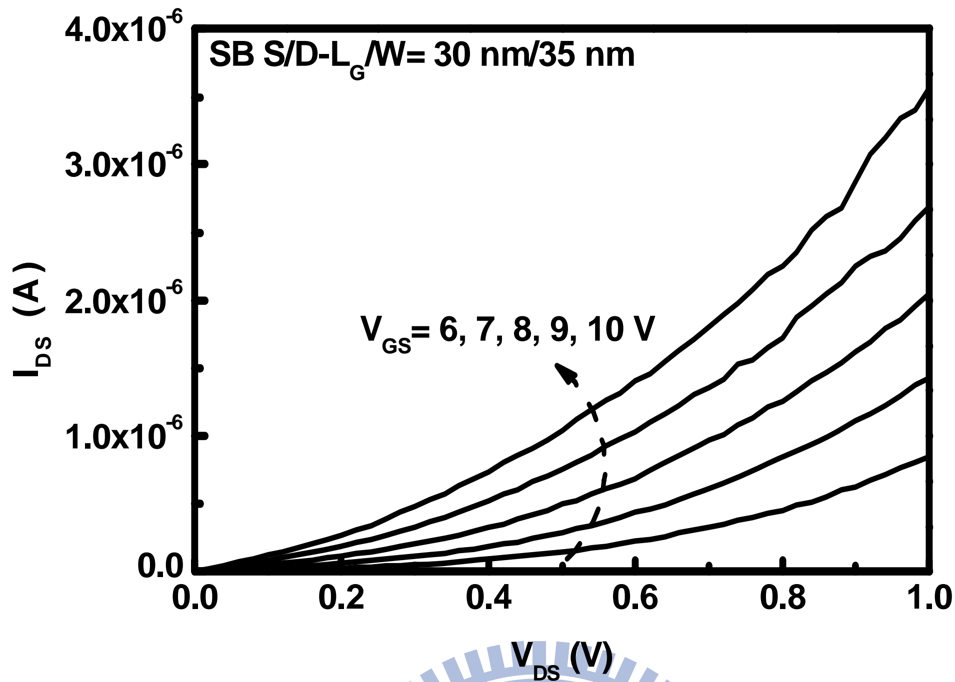


Fig. 5-11 (b) Output characteristics of the smallest SB device with L_G/W= 30 nm/35 nm.

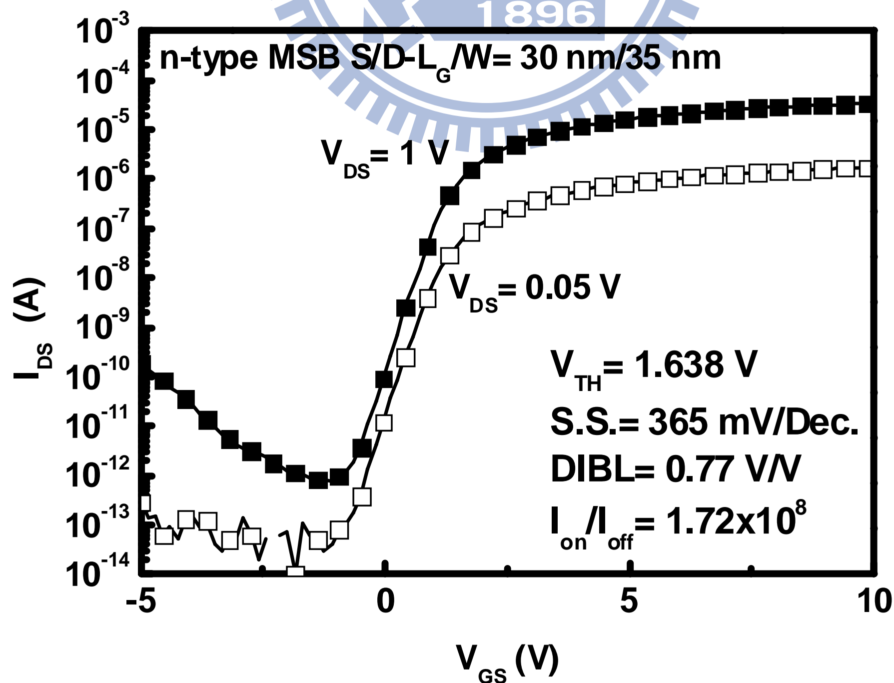


Fig. 5-12 (a) Transfer characteristics of the smallest n-type MSB device with L_G/W= 30 nm/35 nm.

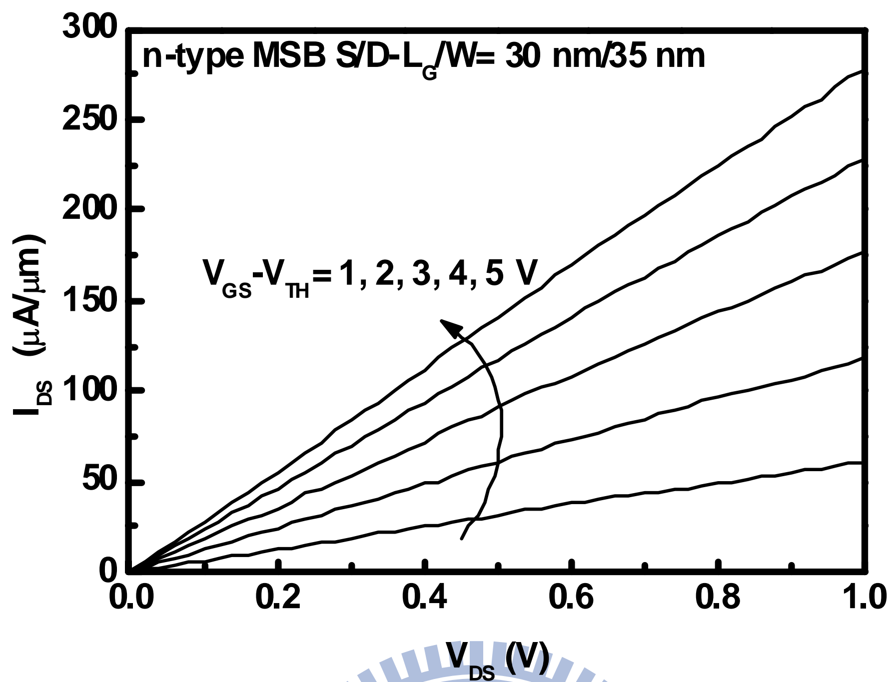


Fig. 5-12 (b) Output characteristics of the smallest n-type MSB device with $L_G/W=$ 30 nm/35 nm.

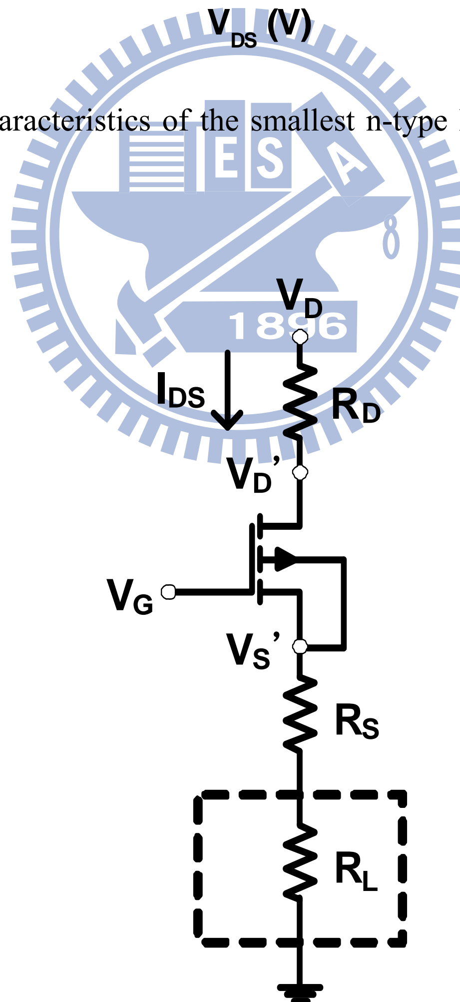


Fig. 5-13 Equivalent circuit diagram of the ELM.

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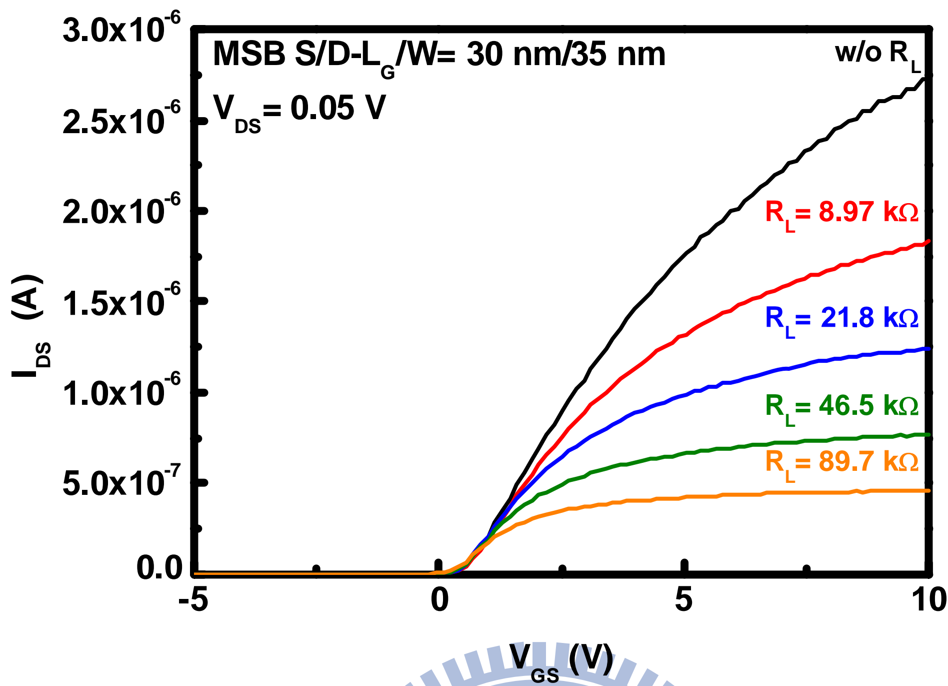

Fig. 5-14 Linear-region transfer characteristics with different external load resistors of the smallest n-type MSB device with L_G/W= 30 nm/35 nm.

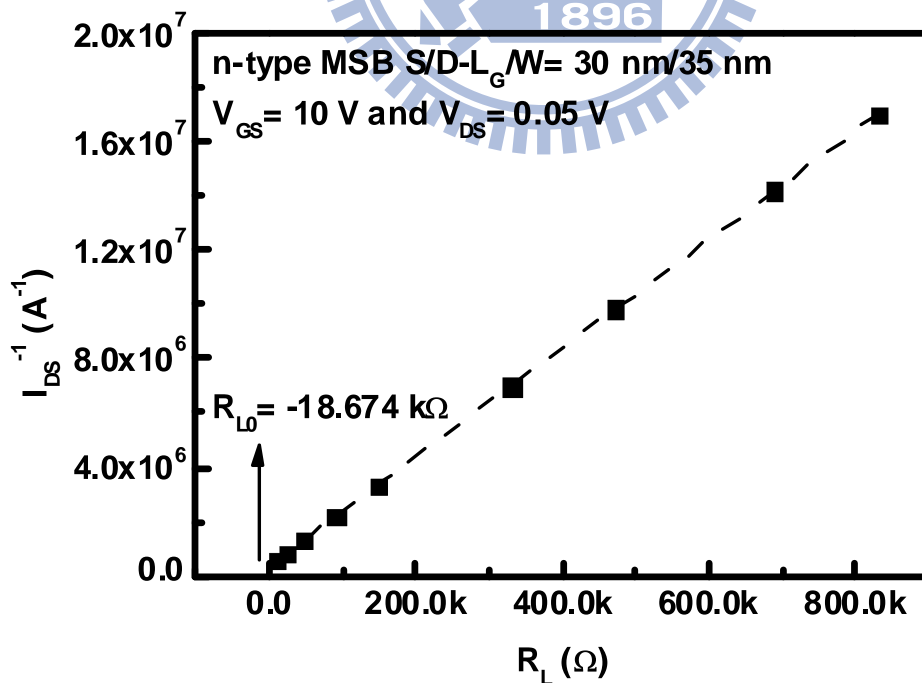

Fig. 5-15 $1/I_{DS}$ versus R_L plot of the smallest n-type MSB device with L_G/W= 30 nm/35 nm.

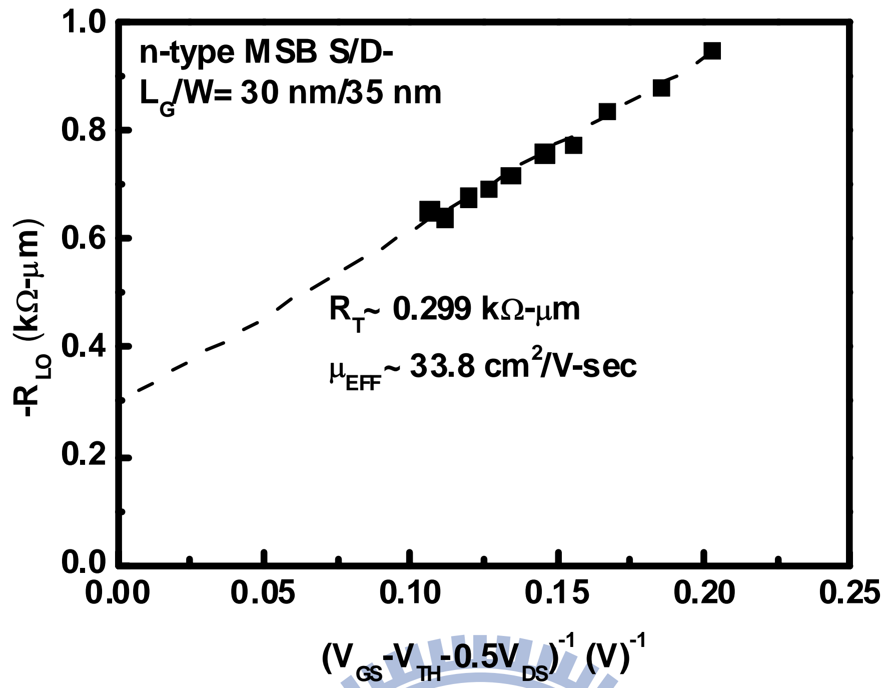

Fig. 5-16 $-R_{L0}$ versus $(V_{GS}-V_{TH}-0.5V_{DS})^{-1}$ plot of the smallest n-type MSB device with L_G/W= 30 nm/35 nm.

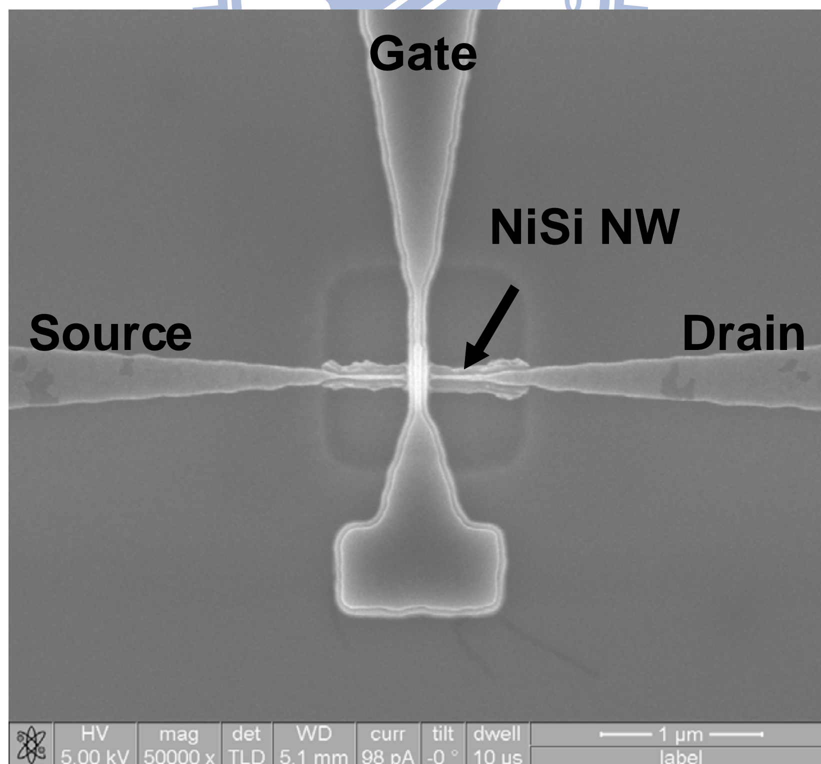

Fig. 5-17 Top-view SEM image of the fabricated poly-Si NW TFT with L_G/W= 30 nm/35 nm.

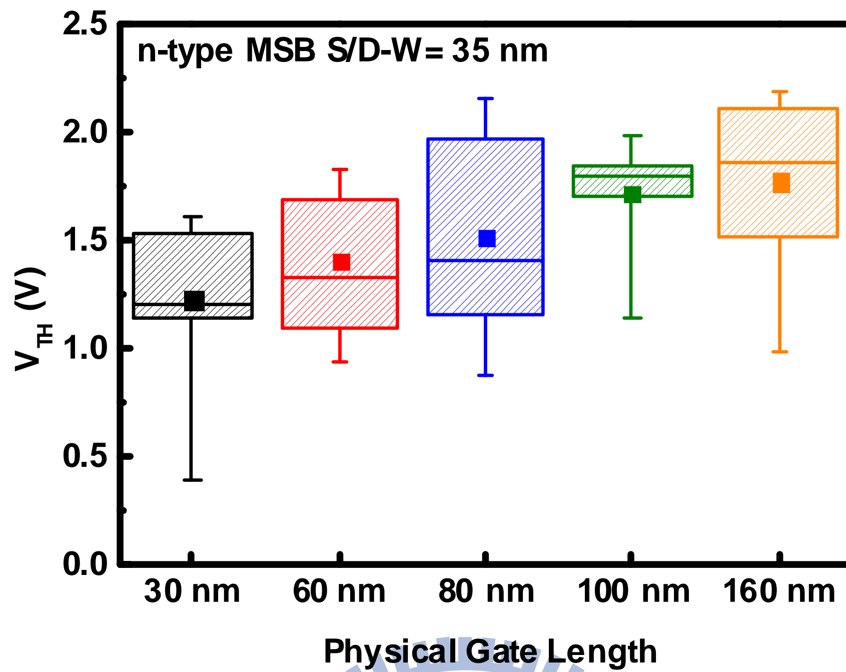

Fig. 5-18 (a) Statistics of the V_{TH} values of the n-type MSB devices with fixed W= 35 nm and various L_G.

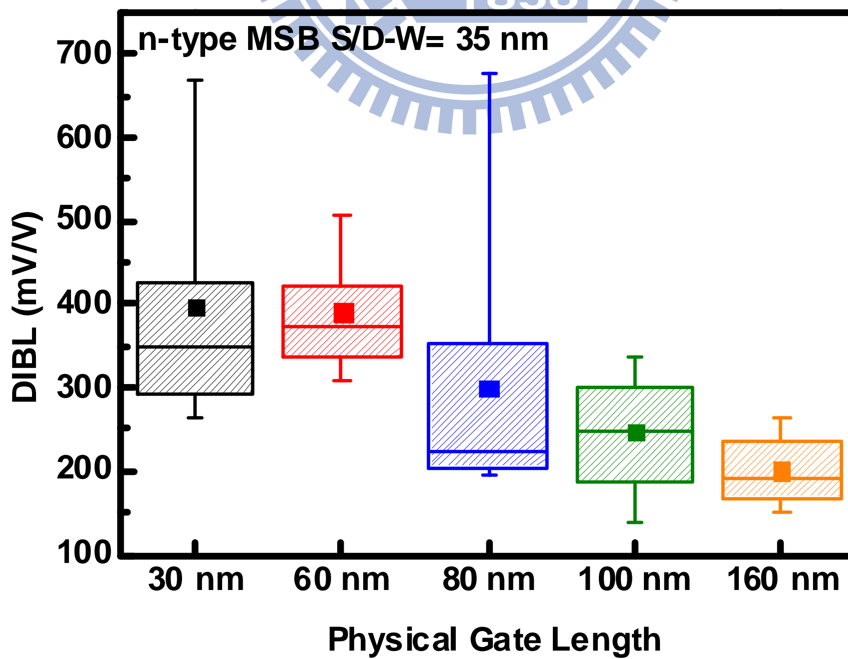

Fig. 5-18 (b) Statistics of the DIBL values of the n-type MSB devices with fixed W= 35 nm and various L_G.

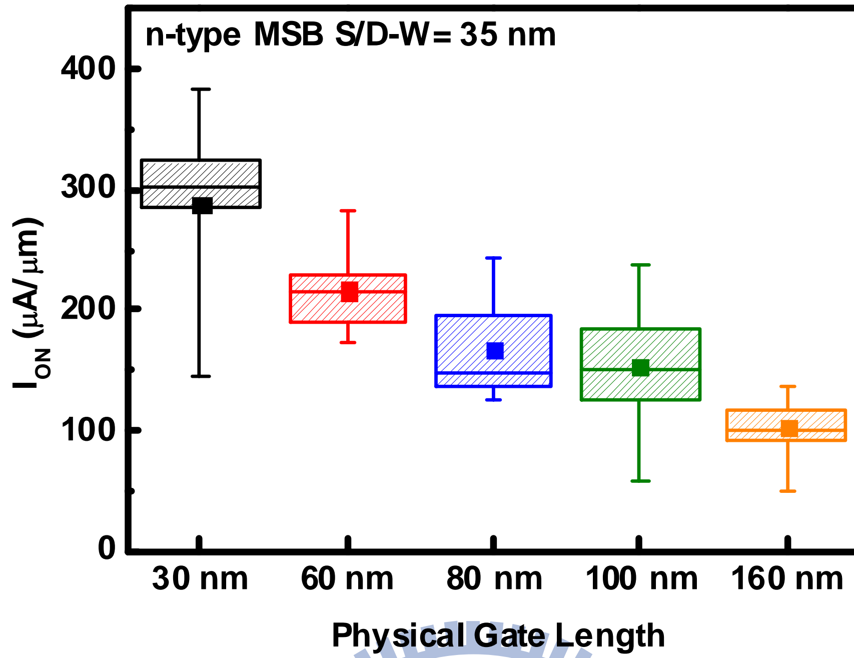

Fig. 5-18 (c) Statistics of the I_{ON} values of the n-type MSB devices with fixed W= 35 nm and various L_G.

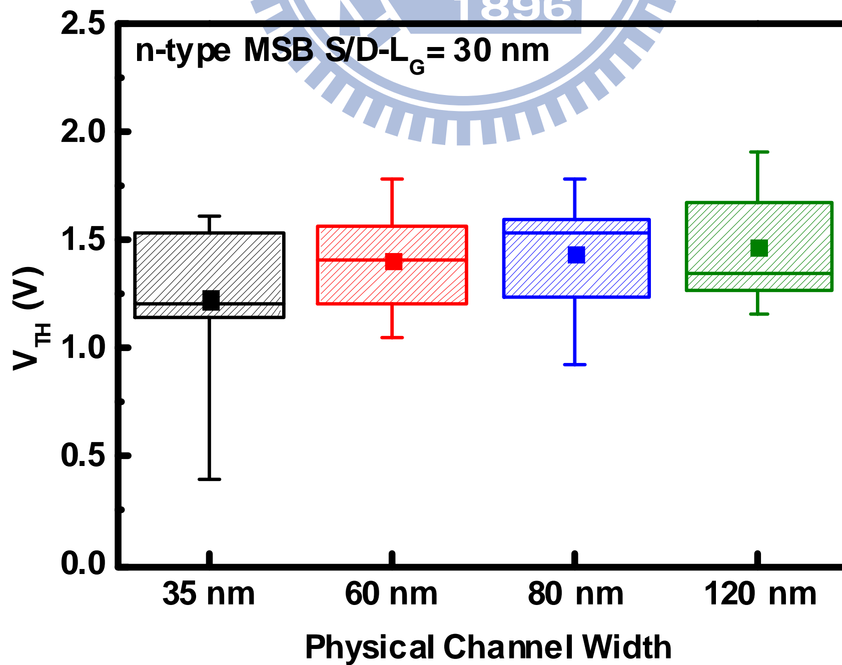

Fig. 5-19 (a) Statistics of the V_{TH} values of the n-type MSB devices with fixed L_G= 30 nm and various W.

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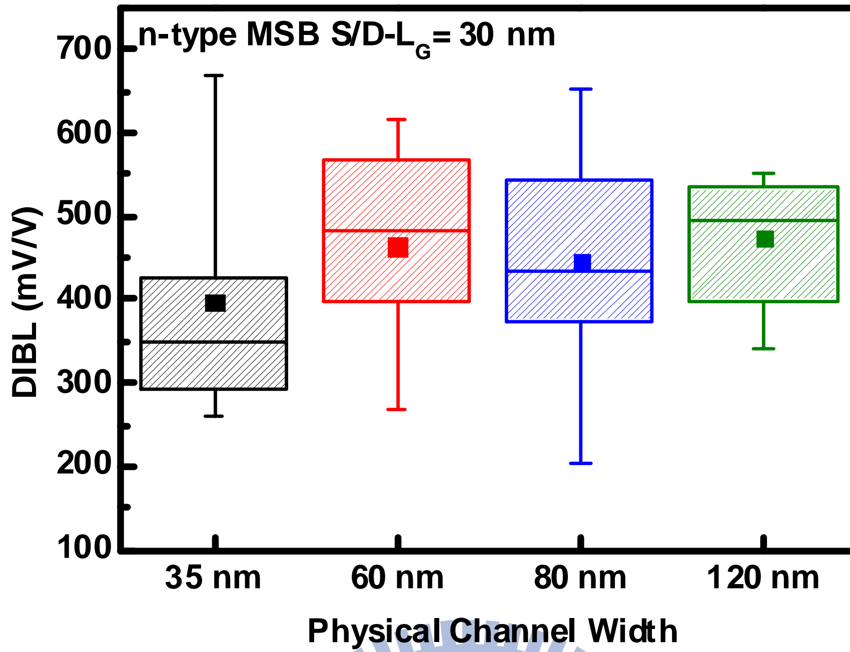


Fig. 5-19 (b) Statistics of the DIBL values of the n-type MSB devices with fixed L_G= 30 nm and various W.

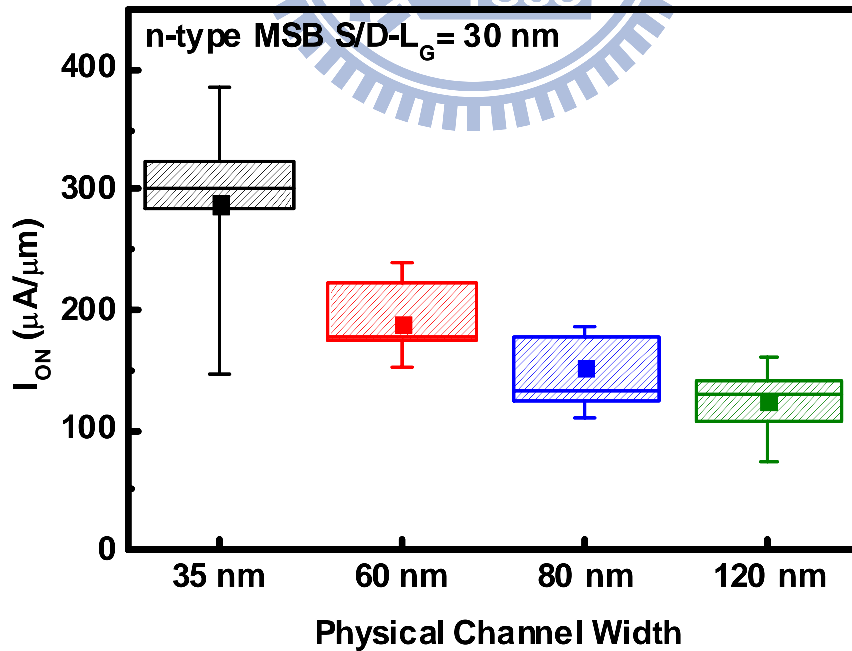


Fig. 5-19 (c) Statistics of the I_{ON} values of the n-type MSB devices with fixed L_G= 30 nm and various W.

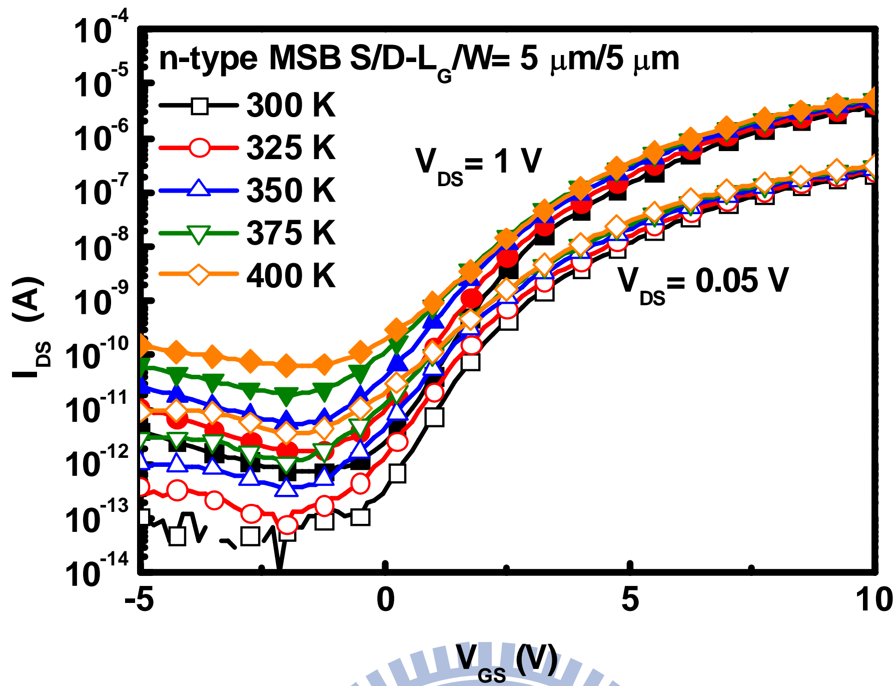


Fig. 5-20 (a) Temperature-dependent transfer characteristics of the n-type MSB device with L_G/W= 5 μm/5 μm.

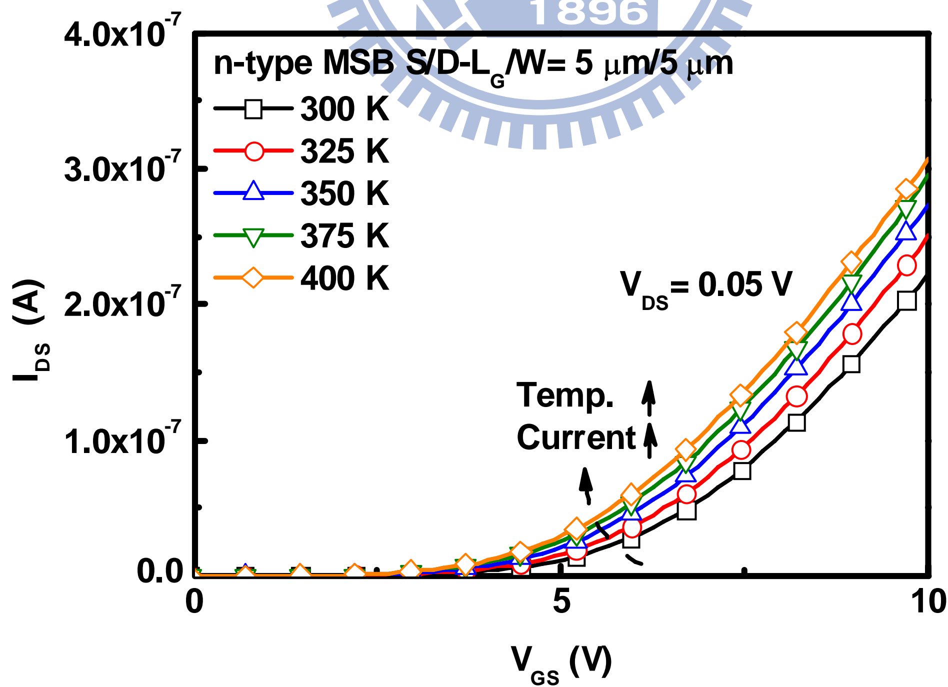


Fig. 5-20 (b) Temperature-dependent transfer characteristics (linear scale) of the n-type MSB device with L_G/W= 5 μm/5 μm biased at V_{DS}= 0.05 V.

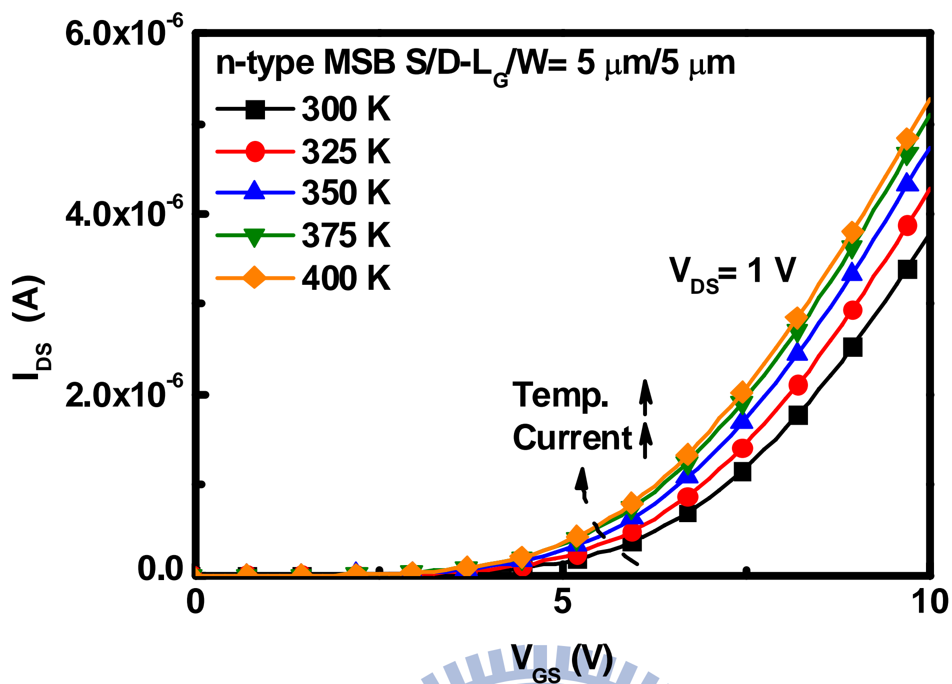


Fig. 5-20 (c) Temperature-dependent transfer characteristics (linear scale) of the n-type MSB device with $L_G/W= 5\ \mu m/5\ \mu m$ biased at $V_{DS}= 1$ V.

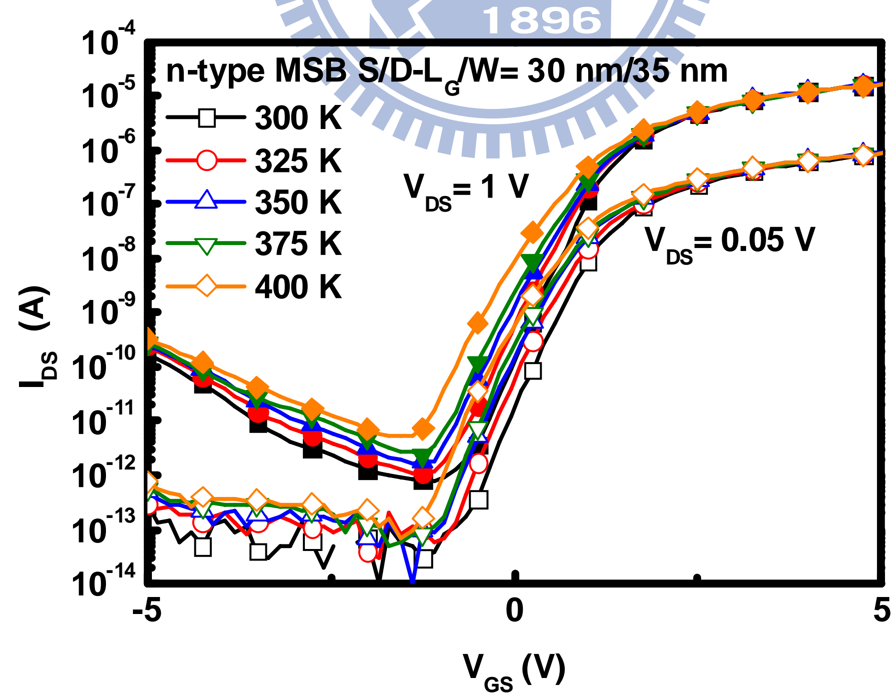


Fig. 5-21 (a) Temperature-dependent transfer characteristics of the smallest n-type MSB device with $L_G/W= 30$ nm/35 nm.

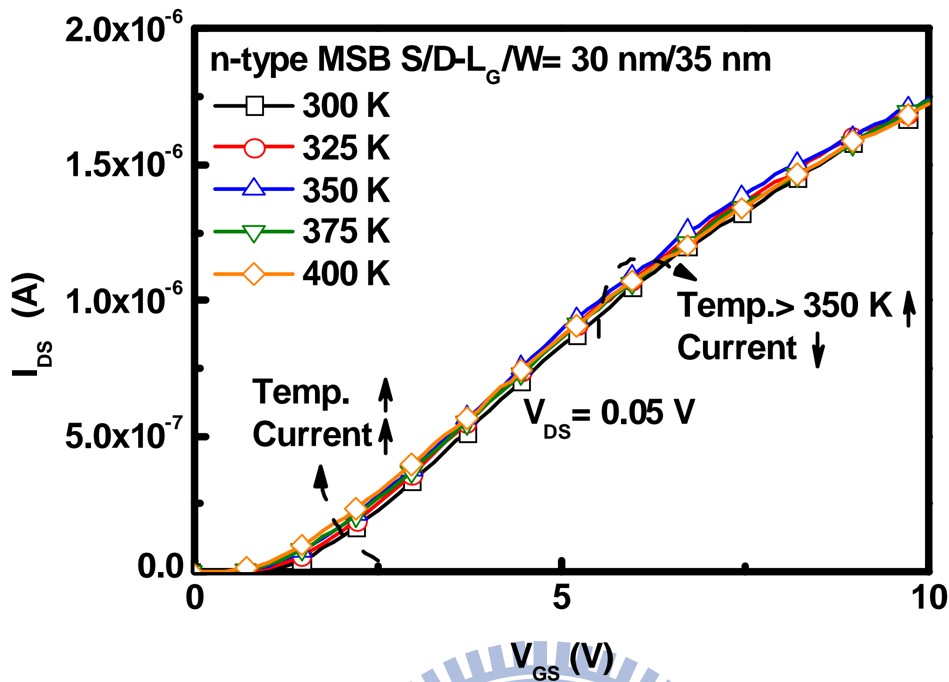


Fig. 5-21 (b) Temperature-dependent transfer characteristics (linear scale) of the n-type MSB device with L_G/W= 30 nm/35 nm biased at V_{DS}= 0.05 V.

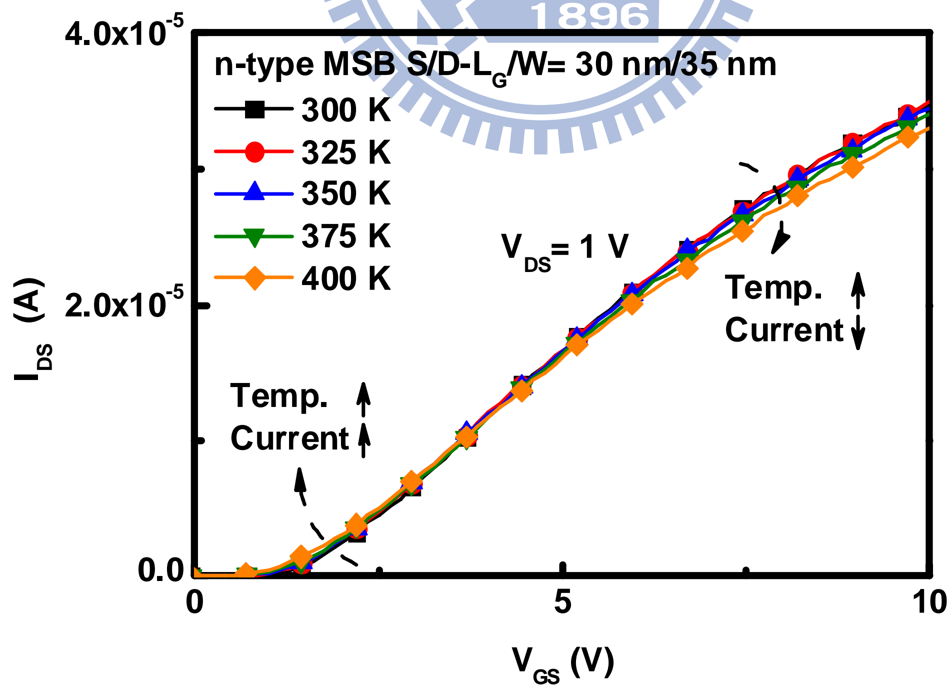


Fig. 5-21 (c) Temperature-dependent transfer characteristics (linear scale) of the n-type MSB device with L_G/W= 30 nm/35 nm biased at V_{DS}= 1 V.

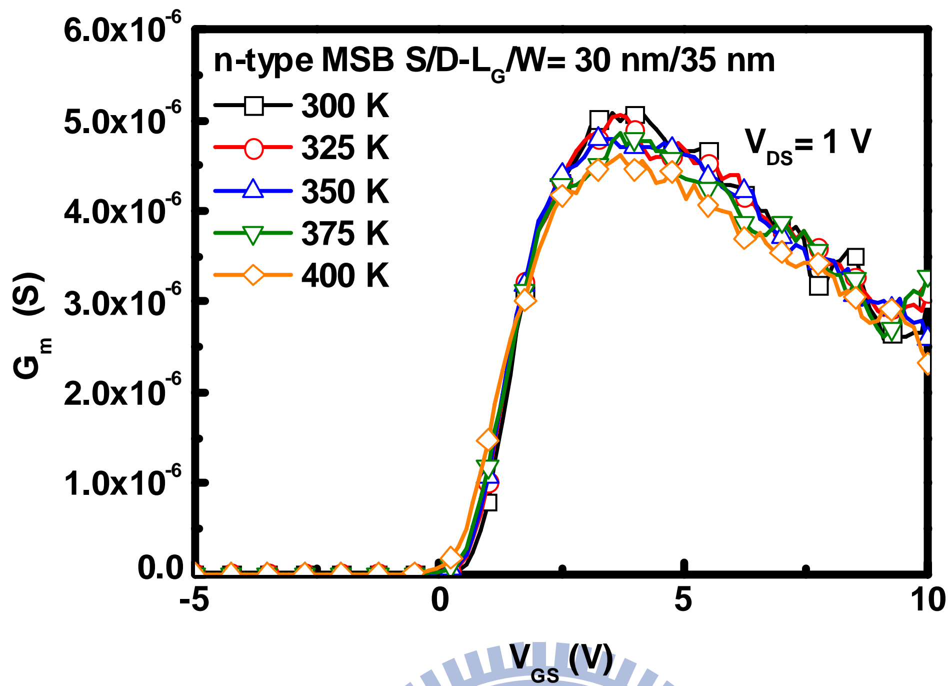


Fig. 5-22 Temperature-dependent transconductance characteristics of the n-type MSB device with L_G/W= 30 nm/35 nm biased at V_{DS}= 1 V.

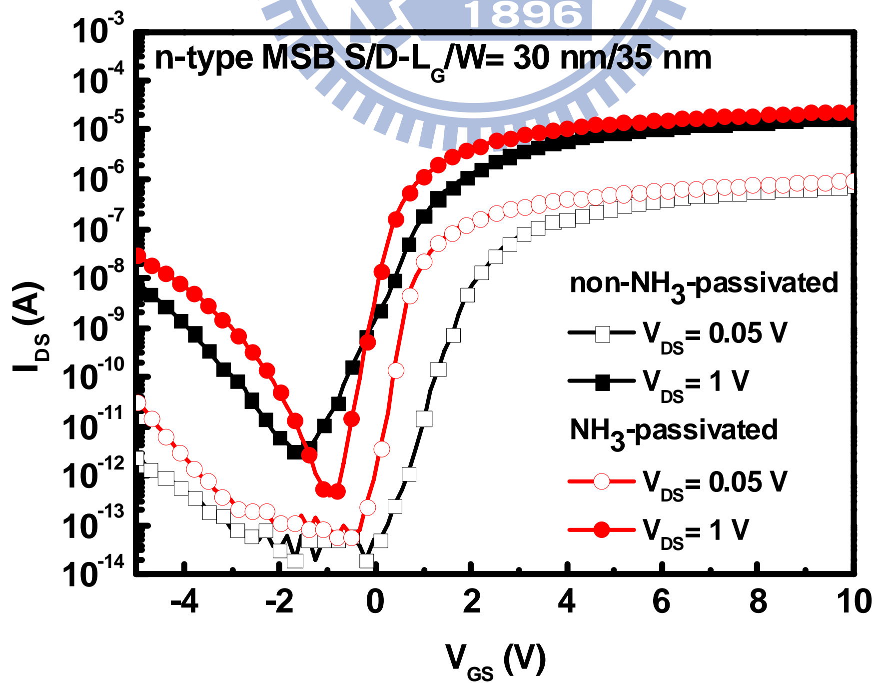
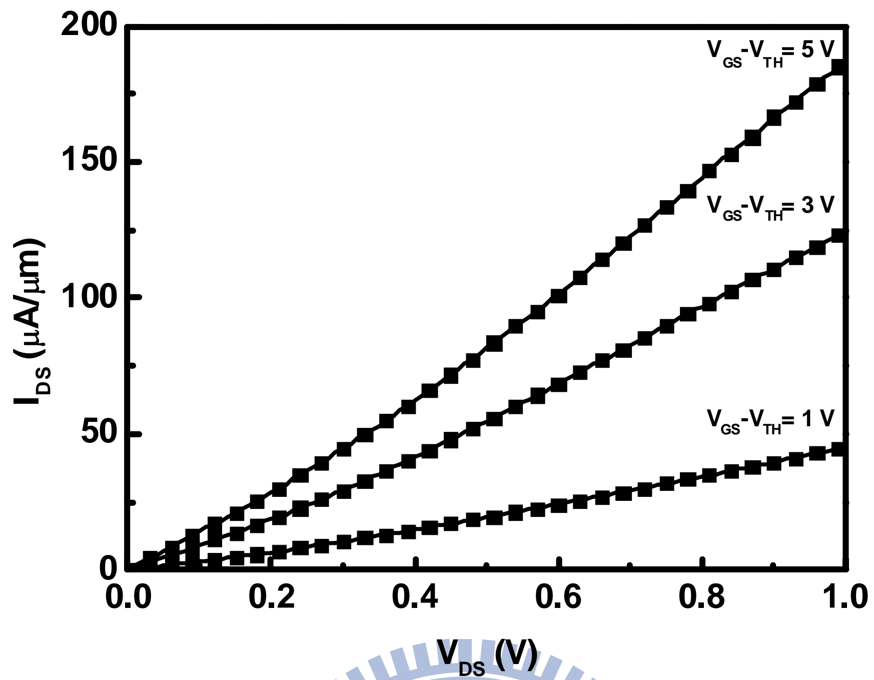


Fig. 5-23 (a) Transfer characteristics of the smallest n-type MSB device with L_G/W= 30 nm/35 nm before and after the NH_3 plasma passivation.



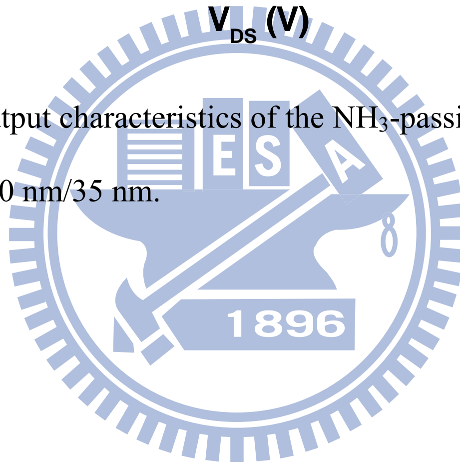


Fig. 5-23 (b) Typical output characteristics of the NH_3-passivated n-type MSB device with L_G/W= 30 nm/35 nm.

Chapter 6

Fabrication and Electrical Characteristics of Poly-Si Nanowire Thin-Film Transistors with the High-κ Gate Dielectric

6.1 Introduction

The high driving capability and low-operation voltage are necessary for high-performance poly-Si TFTs. In chapter 5, we have successfully demonstrated the smallest GAA poly-Si NW TFTs with the high driving capability. However, its high V_{TH} and S.S. values are not suitable for low-voltage operation. For conventional poly-Si TFTs, the SiO_2 gate dielectric is usually formed by a PECVD technique. The CVD SiO_2 is used as the gate dielectric instead of thermal SiO_2 because enhanced grain-boundary oxidation leads to non-uniform thermal oxidation along the poly-Si channel. In addition, thermal oxidation at high temperature is not compatible with the low-temperature poly-Si TFT process. The quality of CVD SiO_2 is worse than that of thermal SiO_2, so the gate dielectric thickness of CVD SiO_2 must be thick enough to prevent high gate leakage currents. Thicker CVD SiO_2 gate dielectric results in the higher V_{TH} and S.S. values. Therefore, in this chapter, we focus on the scaling of the EOT by using the high-κ gate dielectric. In recent years, poly-Si TFTs with various high-κ gate dielectrics, such as HfO_2 and praseodymium oxide (Pr_2O_3), have been proposed to reduce the EOT [1-2], but the gate electrodes they used are close to planar

structures. In this study, the HfO_2 gate dielectric and the novel omega-shaped gate structure are both integrated into poly-Si NW TFTs for the first time. We investigate the short-channel characteristics of poly-Si NW TFTs with L_G down to 40 nm.

Furthermore, we also use the UTB structure to achieve high performance. Most research on SOI MOSFETs with the UTB structure has shown excellent electrical characteristics [3-4], so the concept of the UTB structure could be easily extended to poly-Si TFTs. Several studies also indicate reducing the channel thickness of poly-Si TFTs can also achieve higher I_{ON}, lower I_{OFF}, steeper S.S., and lower V_{TH} [5-6]. One issue of the ultra-thin T_{Si} is the degradation of its film quality. After the SPC process, the thinner poly-Si film consists of the smaller grain size and thus higher grain-boundary trap density [5]. Therefore, the channel thickness of the published SPC poly-Si TFTs is just thinned to 20 nm [7]. The other issue of poly-Si TFTs with the ultra-thin channel thickness is the high parasitic resistance at the S/D regions. Both of these issues degrade the driving capability of poly-Si TFTs, so the metal S/D is also used in our study to alleviate the concerns of high parasitic S/D resistance. Hence, the low V_{TH} and steep S.S. values and the high driving capability can be simultaneously obtained via the optimization of the device structures and process technologies.

The SHE in SOI MOSFETs has been studied for many years [8-9], and it can reduce carrier mobility and the corresponding decrease of the I_{ON} owing to Joule heating. Joule heating is proportional to the square of current density, so the SHE of high-performance poly-Si TFTs should be considered due to their high current driving capability. In this work, pulsed I-V measurements are used, for the first time, to observe the self-heating phenomenon of our high-performance poly-Si NW TFTs with various active area sizes.

6.2 Device Fabrication

Figure 6-1 shows the key fabrication steps of poly-Si NW TFTs combined with the HfO_2 gate dielectric, and its detailed process flow is described below. This device is called device A. The process steps before the gate dielectric deposition are the same as those described in section 5.3. After the standard RCA cleaning process, a metal-organic CVD (MOCVD) system was used to deposit a 10-nm-thick HfO_2 gate dielectric (T_{HfO2}= 10 nm) at 500 °C. A 200-nm-thick un-doped amorphous-Si film was sequentially deposited by a LPCVD system and etched to define the gate pattern, and the omega-shaped gate structure was formed owing to the recessed and undercut etching of the buried SiO_2 by several cleaning steps. Then, a double spacer consisting of a 20-nm-thick TEOS SiO_2 and a 20-nm-thick Si_3N_4 was formed by a PECVD system and RIE. Phosphorous ions were implanted into the amorphous-Si gate electrode at 60 keV to a dose of $5x10^{15}$ cm^{-2}. This ion implantation process also amorphize the HfO_2 gate dielectric at the S/D regions so that it can be removed easier. After removing the HfO_2 layer by a mixture of 95% isopropyl alcohol (IPA) and 5% HF [10], the implanted dopants in the gate electrode were activated in N_2 ambient at 600 °C for 12 hr. To reduce the S/D series resistance, the metal S/D was fabricated by a low-temperature process. After removing the native oxide on the phosphorus-doped poly-Si gate and S/D regions by DHF solutions, an 8-nm-thick Ni film was evaporated by electron-beam evaporation. Next, a two-step Ni-silicidation process was employed to form the n-type MSB S/D (as described in section 5.3) [11]. Some devices underwent a sintering process in forming gas (95 % N_2 and 5 % hydrogen (H_2)) at 400 °C for 30 min. Finally, PECVD oxide passivation, contact-hole patterning, Al metallization steps were performed to complete device fabrication. In

addition, the MOS capacitor with an area of 50x50 μm^2 was fabricated by using the same process flow to extract the EOT and the κ value of the HfO_2 gate dielectric.

Figure 6-2(a) shows the device structure along the channel direction inspected by a TEM. The L_G, T_{Si}, and T_{HfO2} are 40 nm, 10 nm, and 10 nm, respectively. The fully Ni-silicided S/D is successfully fabricated. Figure 6-2(b) shows an enlarged view of Fig. 6-2(a), and it also can be seen that the HfO_2 gate dielectric has been crystallized during the annealing processes. Furthermore, a 3-nm-thick amorphous interfacial oxide layer (T_{IL}) forms between the HfO_2 gate dielectric and the poly-Si NW channel during the gate dopant activation at 600 °C for 12 hr. The narrowest W observed by a TEM is 20 nm, as shown in Fig. 6-3(a). The encroachment of the gate electrode under the poly-Si NW channel forms an omega-shaped gate structure. Figure 6-3(b) shows the cross-sectional TEM image of the near GAA device with L_G/W= 1 μm/200 nm. The poly-Si channel can be surrounded by the HfO_2 gate dielectric, but highly non-conformal deposition of HfO_2 is clearly observed. Therefore, for the GAA devices, high gate leakage currents arising from the ultra-thin HfO_2 gate dielectric at the backside poly-Si channel are measured. Atomic layer deposition (ALD) has the merits of better step coverage and thickness controllability [12], so it can be used to replace MOCVD and deposit the HfO_2 gate dielectric.

For comparison, the other two n-type MSB devices named device B and device C were also fabricated by using the process flow described in section 5.3 and [13], respectively. The active layer thickness and the gate dielectric thickness of all n-type MSB devices are listed in Table 6-1. A HP 4156C semiconductor parameter analyzer and a HP 4284A inductance-capacitance-resistance (LCR) meter were used to perform the I-V and capacitance-voltage (C-V) measurements, respectively. Pulsed I-V measurements were performed using the Agilent B1530A, the waveform

generator/fast measurement unit (WGFMU), which enables high speed I-V measurement with high resolution.

6.3 Results and Discussion

6.3.1 Basic MSB Device Characteristics

To investigate the intrinsic gate-to-channel controllability without the influence of the SCE, the non-sintered transfer characteristics of three n-type MSB devices (device A, B, and C) with L_G/W= 5 μm/10 μm are compared in Fig. 6-4. The linear-region V_{TH} is defined as the V_{GS} at which the I_{DS} equals to (W/L_G)x10 nA at a V_{DS} of 0.05 V. The DIBL value is calculated from the difference in V_{TH} at V_{DS}= 0.05 V and 0.5 V. The device key parameters including the V_{TH}, S.S., and DIBL values are extracted and listed in Table 6-1. By comparing the device key parameters of the device B to those of the device C, it is observed that the scaling of the T_{Si} and T_{ox} can effectively improve the gate-to-channel controllability. The effective grain-boundary trap density (N_t) of the device B is measured by Levinson's method [14], as shown in Fig. 6-5. According to the current model in the linear region developed by Levinson *et al.*, Levinson's method measures the N_t within the thickness of the surface inversion channel, which is independent of the thickness of the poly-Si film. For device B with the ultra-thin T_{Si} of 8 nm, the N_t value is $5.266\text{x}10^{12}$ cm^{-2}. This N_t value is comparable to that of the SPC poly-Si TFTs with the thicker T_{Si} [15]. Moreover, the I_{OFF} of the device B is smaller than that of the device C owing to the thinner T_{Si}. As the TEOS SiO_2 gate dielectric is replaced by the HfO_2 gate dielectric to further reduce the EOT, the device A exhibits the best transfer characteristics among these three n-type MSB devices. The S.S. and DIBL values can be further improved to 606 mV/Dec. and 2.283 V/V, respectively, but the GIDL effect is more apparent in the off state as the

result of the stronger electric filed between the gate electrode and the drain electrode. The grain-boundary defects at the drain-side depletion region could also enhance the trap-assisted tunneling of the valence band electrons. It should be noted that gate leakage currents do not dominate when the device A operates at the off-state region.

Figure 6-6 compares the transfer characteristics before and after forming gas sintering of the n-type MSB device combined with the HfO_2 gate dielectric. The L_G/W is equal to 90 nm/20 nm. Before the sintering process, the V_{TH}, S.S., and DIBL values are 2.561 V, 253 mV/Dec., and 0.459 V/V, respectively. It is indicated that the SCE can be greatly suppressed by the structure of the HfO_2 gate dielectric, the ultra-thin poly-Si NW, and the omega-shaped gate structure. After utilizing the 400 °C forming gas sintering process to passivate the grain-boundary defects and the poly-Si/interfacial oxide interface states, the V_{TH}, S.S., and DIBL values decrease to 1.162 V, 113 mV/Dec., and 0.254 V/V, respectively. The extremely high I_{on}/I_{off} current ratio of 2.52×10^7 is obtained at V_{DS}= 1 V. It has been reported that H_2 in the HfO_2 gate dielectric can form H^+ state to contribute positive fixed charges [16], so it results in the negative V_{TH} shift after the sintering process.

Figure 6-7 show the transfer and output characteristics of the n-type MSB device combined with the HfO_2 gate dielectric after the sintering process, respectively. The L_G/W is equal to 40 nm/20 nm, respectively. The V_{TH}, S.S., and DIBL values are -0.413 V, 248 mV/Dec., and 0.760 V/V, respectively. The calculated λ value (see section 5.2) of this work is 6.9 nm, which is 5.8 times smaller than L_G of 40 nm. Hence, good S.S. and DIBL values can be both obtained. Furthermore, although the HfO_2 gate dielectric has been crystallized, gate leakage currents are still low due to the formation of the amorphous interfacial oxide layer and the ultra-small gate area. From the output characteristics, the normalized I_{ON} (I_{DS}/W_{EFF}) at V_{GS}-V_{TH}= 3 V and

V_{DS}= 1 V is as high as 549 μA/μm, which exceeds the record value in section 5.4.2 with the even lower V_{GS}-V_{TH} value of 3 V. The I_{on}/I_{off} current ratio is $3.19x10^6$ at V_{DS}= 0.05 V. This ratio is not very high because the thinner EOT results in higher GIDL current, but it is an acceptable value especially for TFTs.

Assuming the dielectric constant of the interfacial oxide layer is 3.9, the κ and EOT values extracted from the MOS capacitor are 22.2 and 4.76 nm, respectively. A very thick interfacial oxide layer of 3 nm can greatly increase the EOT of the gate dielectric even if the κ value of the HfO_2 gate dielectric is high enough and close to the previously reported value [2]. The thermal stability of an HfO_2/poly-Si gate stack should be improved in order to further reduce the EOT and enhance the gate-to-channel controllability. Several methods have been proposed to raise crystallization temperature of the HfO_2 film and eliminate the formation of the interfacial oxide layer between the HfO_2 film and the Si substrate [17-18].

6.3.2 Self-Heating Effect

The SHE is related with the thermal conductivity of the substrate and power dissipation. The thermal conductivity of Si is 155 W/m-K at 300 K, so Joule's heat generated inside the bulk device can be transferred to the Si substrate. However, the thermal conductivity of SiO_2 is only 1.4 W/m-K, which is two orders of magnitude smaller than that of Si. Since poly-Si TFTs or SOI MOSFETs are fabricated on a glass or SOI substrate, the accumulated Joule heat can not be dissipated via the buried SiO_2 layer during device operation and then causes an increase in the device temperature. In recent years, the effect of the electrical-current-induced Joule self-heating on the device characteristics is studied by device simulation or electrical measurement (pulsed I-V and ac conductance methods) [8, 19-20]. These results indicate that the

device temperature can substantially increase with an increase of the power density dissipated in the device. The I_{ON} values of the dc I-V characteristics are smaller than those of the pulsed I-V characteristics due to the phonon-limited mobility reduction induced by the SHE, especially for the high driving capability. From our previous discussion, we have fabricated high-performance poly-Si NW TFTs with the superior current driving capability. Furthermore, for high-level applications in the future, poly-Si TFTs will be operated under pulsed bias in the real condition. Therefore, the influence of the self-heating phenomenon on their turn-on characteristics should be investigated by the pulsed I-V measurements.

For the pulsed I-V measurement system of the model Agilent B1530A, it has a remote-sense and switch unit (RSU) to perform dc measurements by the source monitor unit (SMU), a WGFMU for pulsed I-V measurement, and a wave monitor function by the V monitor. The schematic diagram of the pulsed I-V measurement system is shown in Fig. 6-8(a). The gate and drain terminals of the device are connected to the WGFMU channel 1 and WGFMU channel 2, respectively. During the pulsed I_{DS}-V_{GS} measurement, the gate bias is a pulsed sweep, and the drain bias is a constant voltage. The WGFMU channel 1 forces the pulsed gate bias, and the WGFMU channel 2 simultaneously senses the I_{DS}. Figure 6-8(b) shows the definition of the pulse waveform. In addition to the basic pulse parameters, the measurement delay time and the averaging time are necessary to confirm the measurement accuracy. The base voltage is set to the V_{GS} at which the device is biased at the turn-off state.

Figure 6-9(a) shows an example of the voltage waveform monitored by the V monitor as a function of time. The pulse width and period are set to 1 μsec and 2 μsec, respectively. The rise and fall times are both 100 nsec. The pulsed gate bias sweeps from -0.5 V to 1.5 V, and the constant drain bias is 1 V. It is reasonable that the

measured voltage value sensed with an oscilloscope is ten times smaller than the actual applied voltage owing to the voltage attenuator within the V monitor. Figure 6-9(b) shows an enlarged view of Fig. 6-9(a), and the output waveform corresponds to the user-defined waveform. Overshoot and oscillation phenomena of the pulsed gate bias are not observed, therefore, the accurate output waveform is confirmed by an Agilent infiniium DSO80204B oscilloscope. Furthermore, in addition to the gate voltage waveform monitored by the V monitor, we also simultaneously measure the gate voltage waveform by another external probe to observe if the resistance-capacitance (RC) time constant delay of the gate pad would alter the waveform, as shown in Fig. 6-10(a) and 6-10(b). The pulsed gate bias sweeps from 0 V to 4 V, and other pulse parameters are the same as those of Fig. 6-9(a). According to Fig. 6-10(b), the RC time constant delay of the gate pad is almost zero and can be neglected in practice.

Before measuring the SHE of our high-performance poly-Si NW TFTs, we measure the SHE of the bulk MOSFET and SOI MOSFET at first. The pulse width and period are set to 1 μsec and 2 msec, respectively. The rise and fall times are both 100 nsec. The measurement delay time and the averaging time are set to 200 nsec and 700 nsec, respectively. Therefore, the turn-on time is 0.9 μsec while the turn-off time is 1.9988 msec. In other words, the device has 1.9988 msec to dissipate the heat produced during the turn-on time of 0.9 μsec. To study the SHE, the dc I-V characteristics of the device are also measured and compared with its pulsed I-V characteristics. Figure 6-11(a) and 6-11(b) show the measurement results of the n-type bulk MOSFET with a poly-Si/oxynitride gate stack and p-type SOI MOSFET with a poly-Si/SiO_2 gate stack, respectively. Obviously, the SHE does not occur in the n-type bulk MOSFET with L_G/W= 75 nm/1 μm owing to the high-thermal-conductive Si

substrate. The pulsed I-V characteristics are the same as the dc I-V characteristics even if the driving current density is as high as 1322 μA/μm at V_{GS}= 1.904 V and V_{DS}= 1.2 V. On the contrary, for the p-type SOI MOSFET with L_G/W= 1 μm/10 μm, the SHE occurs and becomes apparent as the driving current density is only equal to 138.4 μA/μm at V_{GS}= -4 V and V_{DS}= -7 V. The relative current amplitude is defined as the current difference between pulsed I-V and dc I-V measurements divided by the current of the pulsed I-V measurement. The relative current amplitude of the p-type SOI MOSFET is 4.28 % at V_{GS}= -4 V and V_{DS}= -7 V. According to these measurement results, we consider that the pulsed I-V measurement system is reliable to study the self-heating phenomenon. These pulse parameters are fixed to execute the next pulsed I-V measurements.

Next, we study the SHE in our n-type NH_3-passivated poly-Si NW TFTs with a poly-Si/TEOS oxide stack. The detailed process flow has been described in chapter 5. Figure 6-12 compares the pulsed I-V and dc I-V curves of the n-type poly-Si NW TFT with L_G/W= 300 nm/1 μm. The SHE does not take place because the I_{ON} of 30 μA/μm is not high enough to produce Joule heating. Therefore, the SHE can only be observed in high-performance poly-Si TFTs with the higher driving capability. Figure 6-13 and 6-14 show the pulsed I-V and dc I-V curves of the n-type poly-Si NW TFT with L_G/W= 30 nm/35 nm and L_G/W= 30 nm/120 nm, respectively. For these two figures, as the I_{ON} is smaller than 50 μA/μm, the pulsed I-V and dc I-V curves totally overlap with each other. When the SHE occurs with high I_{ON}, the pulsed I-V curve gradually deviates from the dc I-V curve. From Fig. 6-13, we observe that the pulsed I-V curve shows higher I_{ON} than those of the dc I-V curve, which is similar to that observed in SOI MOSFETs. At V_{GS}= 9.09 V and V_{DS}= 1 V, the pulsed current is 4.5 % higher than the dc current. However, according to Fig. 6-14, we find that the I_{ON} measured

by the pulsed I-V technique at V_{GS}= 8.9 V and V_{DS}= 1 V is about 5.21 % lower than in the dc measurement. The reason why the SHE results in different dc I-V behaviors is related to the current transport mechanism in poly-Si TFTs described in 5.3.6. For the n-type poly-Si NW TFT with L_G/W= 30 nm/35 nm, it can be regarded as a single-crystal-like device, and its current transport mechanism is the drift-diffusion current. Therefore, when Joule heating raises the temperature of the device during the dc I-V measurement, its I_{ON} values decrease due to the phonon-limited mobility degradation. On the other hands, the I_{ON} of the n-type poly-Si NW TFT with L_G/W= 30 nm/120 nm is governed by thermionic emission over the grain-boundary barrier. Hence, its I_{ON} values increase with an increase of the device temperature induced by Joule heating. As a result, the on-current transport mechanism in poly-Si TFTs plays an important role in the Joule heating process. Figure 6-15 and 6-16 show the pulsed I-V and dc I-V curves of n-type poly-Si NW TFTs with different pulse width. It is reasonable that their pulsed I-V curves are close to their dc I-V curves with increasing the pulse width. Our high-performance poly-Si NW TFT with L_G/W= 30 nm/35 nm can operate at high switching speeds without the driving capability degradation. Figure 6-17 compares the pulsed I-V and dc I-V curves of the n-type poly-Si NW TFT combined with the HfO_2 gate dielectric, and its L_G/W is equal to 40 nm/20 nm, respectively. The highest I_{ON} value of 945 μA/μm can be obtained at V_{GS}= 4 V and V_{DS}= 1 V. In addition to the SHE, we also observe the I_{DS} fluctuation in the pulsed I-V measurement. The I_{DS} fluctuation with discrete levels can be attributed to oxide traps or interface traps in the gate stack, which is called RTN. Figure 6-18 shows an example of the RTN signal observed in the n-type poly-Si NW TFT combined with the HfO_2 gate dielectric. Its detailed physical mechanism is discussed in chapter 7.

6.4 Conclusions

The smallest poly-Si NW TFT combined with the HfO_2 gate dielectric is demonstrated for the first time. The SCE is well controlled owing to the structure of the HfO_2 gate dielectric, the ultra-thin poly-Si NW, and the omega-shaped gate structure. The gate controllability could be further enhanced by scaling the EOT. Moreover, the S/D parasitic resistance can be reduced by the Ni-silicided S/D. Therefore, the high-performance poly-Si NW TFT, especially for the ultra-high driving capability of 549 μA/μm, can be achieved without using the MILC and the ELA technology. Furthermore, as the device size of the poly-Si TFT continuously scales down, the SHE starts to occur due to a high driving capability. The relationship between the SHE and the on-current transport mechanism of poly-Si TFTs has been investigated in this chapter. If the on-current transport mechanism of poly-Si TFTs is dominated by thermionic emission above the grain-boundary potential barrier, the I_{ON} degradation can be observed during the pulsed I-V measurement. This phenomenon is commonly seen in large-area and small-grain poly-Si TFTs. On the contrary, for small-area and large-grain poly-Si TFTs, once its on-current transport mechanism is transformed into the drift-diffusion model, its SHE phenomenon is the same as that observed in SOI MOSFETs.

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Table 6-1 Comparison of three n-type MSB poly-Si TFTs.

Device ID	**A**	**B**	**C**
Poly-Si channel thickness	**10 nm**	**8 nm**	**45 nm**
Grain-boundary trap density	**5.266×10^{12} cm^{-2}**	**5.266×10^{12} cm^{-2}**	**9.907×10^{12} cm^{-2}**
Gate dielectric	**HfO_2 (10 nm)**	**SiO_2 (25 nm)**	**SiO_2 (45 nm)**
V_{TH} (V)	**4.784**	**4.557**	**10.68**
S.S. (mV/Dec.)	**606**	**933**	**1637**
DIBL (V/V)	**2.283**	**3.143**	**5.384**

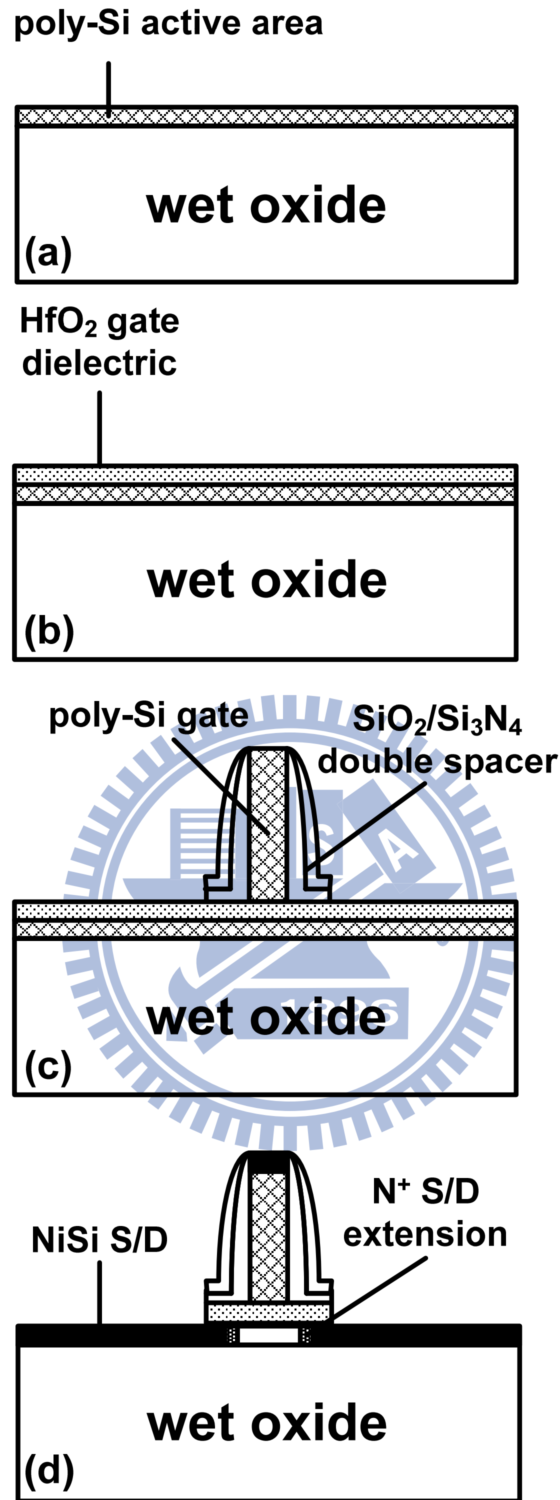

Fig. 6-1 Main process flow of the n-type poly-Si NW TFT combined with the HfO_2 gate dielectric: (a) after the active area definition, (b) after the HfO_2 deposition, (c) after a double spacer formation, and (d) the final device structure.

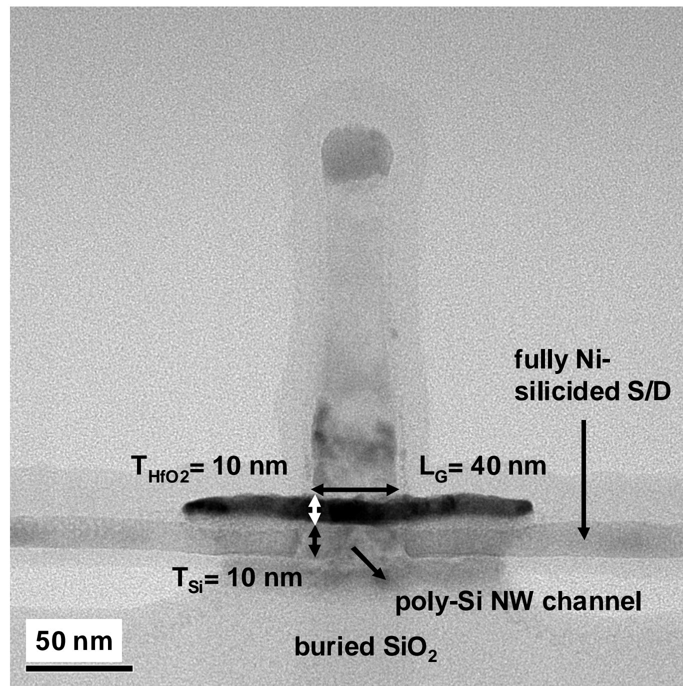

Fig. 6-2 (a) Cross-sectional TEM image along the channel direction of the n-type poly-Si NW TFT combined with the HfO_2 gate dielectric with L_G/W= 40 nm/20 nm.

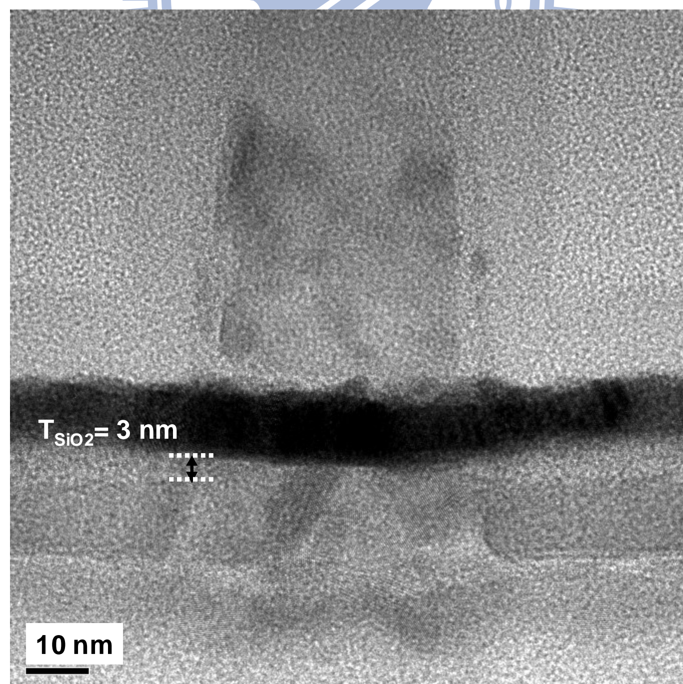

Fig. 6-2 (b) Enlarged view of Fig. 6-2(a) showing a-3 nm-thick amorphous interfacial oxide layer between the HfO_2 gate dielectric and the poly-Si NW channel.

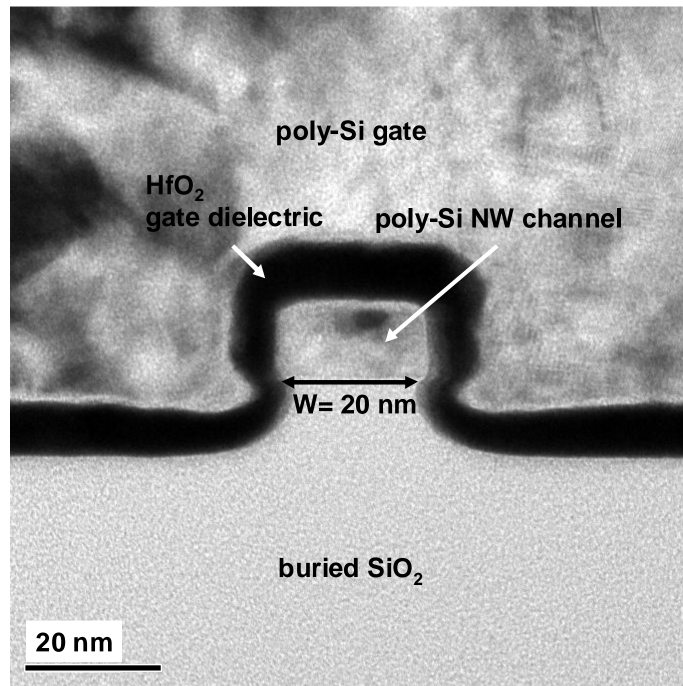

Fig. 6-3 (a) Cross-sectional TEM image along the gate direction of the n-type poly-Si NW TFT combined with the HfO_2 gate dielectric with L_G/W= 40 nm/20 nm.

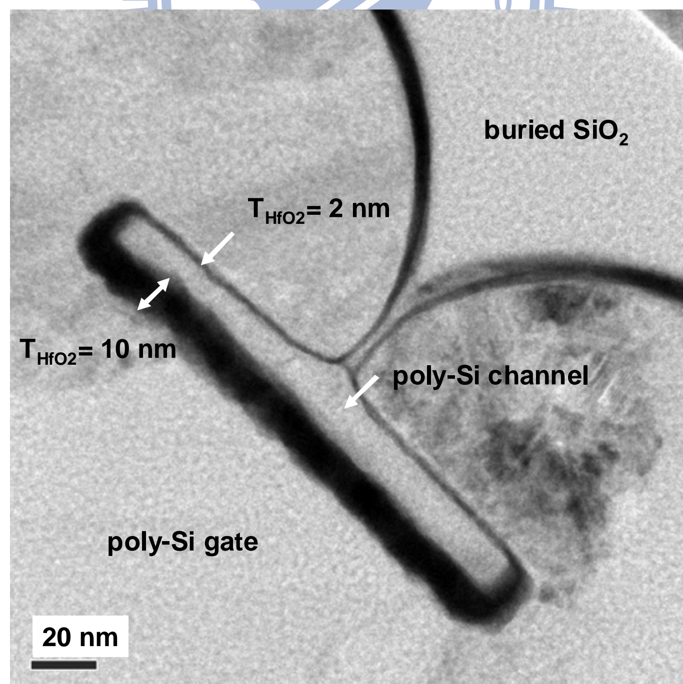

Fig. 6-3 (b) Cross-sectional TEM image of the near GAA device with L_G/W= 1 μm/200 nm.

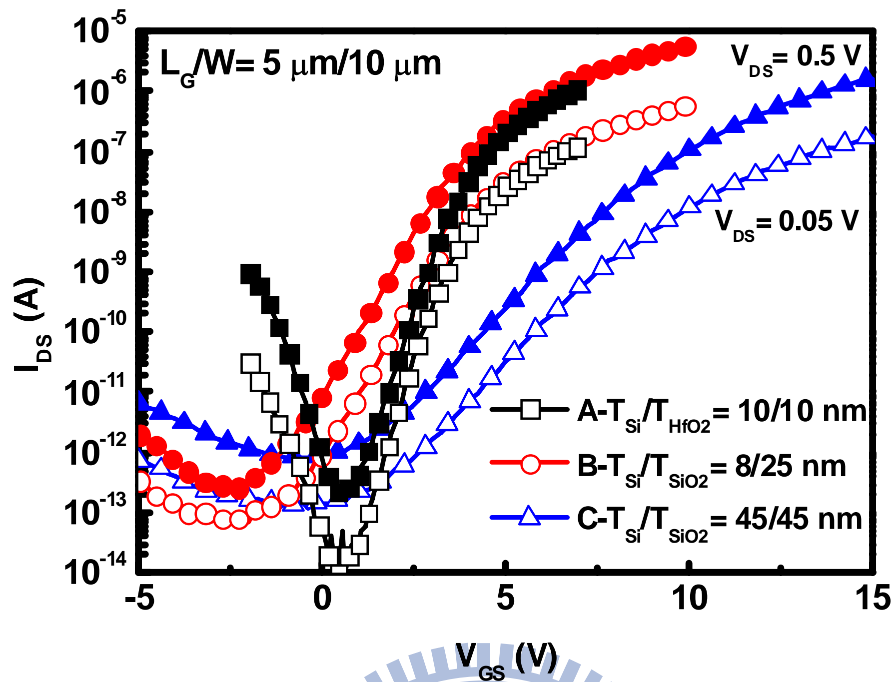

Fig. 6-4 Comparison of the typical non-sintered transfer characteristics of the device A, device B, and device C with L_G/W= 5 μm/10 μm.

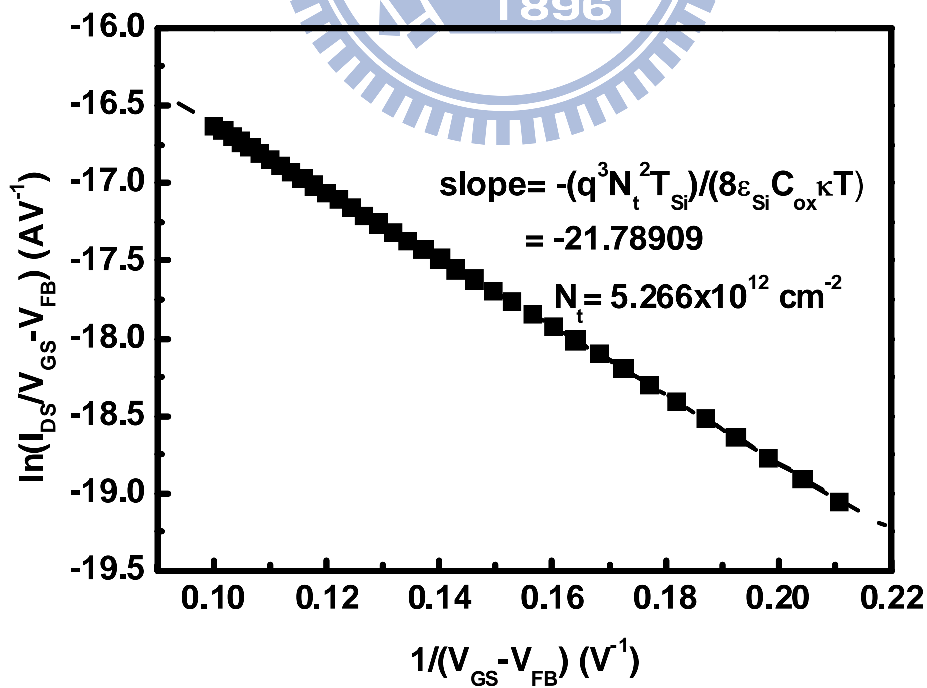

Fig. 6-5 Plot of ln(I_{DS}/V_{GS}) versus (1/ V_{GS}) and the effective grain-boundary trap density of the device B.

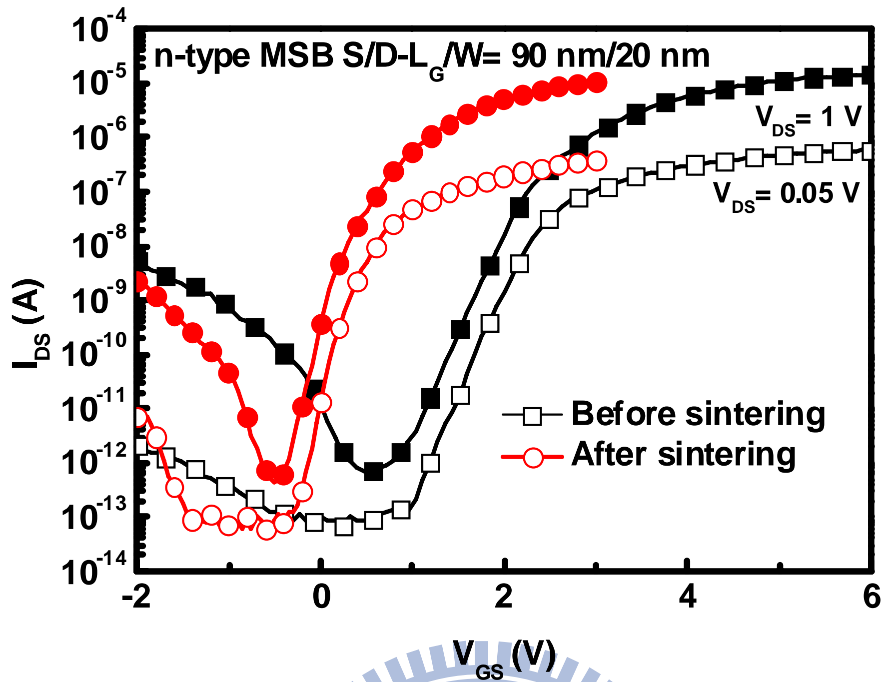

Fig. 6-6 Non-sintered and sintered transfer characteristics of poly-Si NW TFTs combined with HfO_2 gate dielectric, and their L_G/W= 90 nm/20 nm.

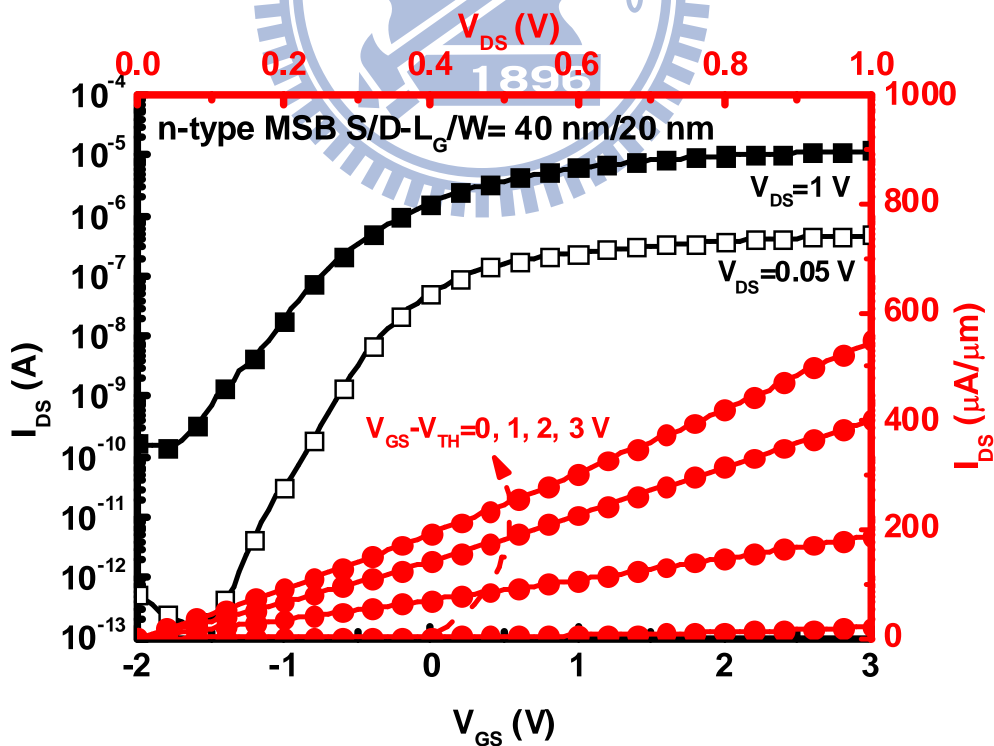

Fig. 6-7 Typical sintered transfer and output characteristics of poly-Si NW TFTs combined with HfO_2 gate dielectric, and their L_G/W_G = 40 nm/20 nm.

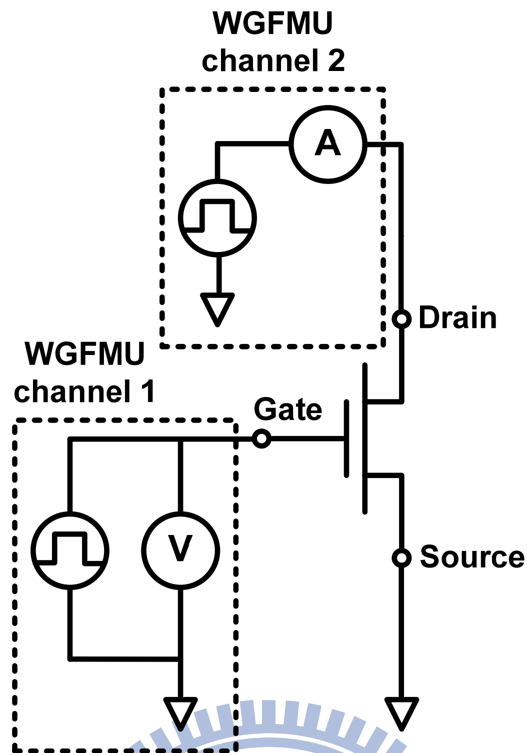

Fig. 6-8 (a) Connection of pulsed I-V measurements using the WGFMU channel 1 and WGFMU channel 2.

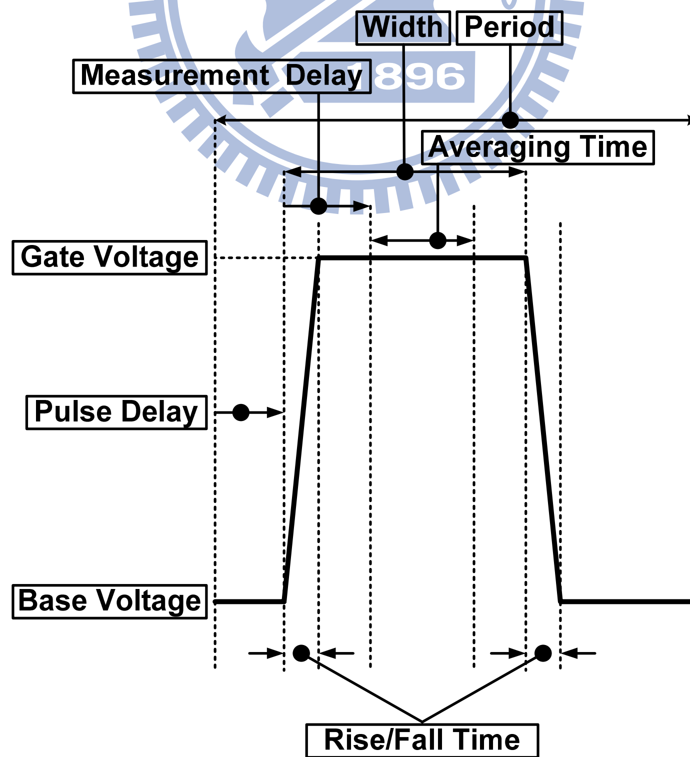

Fig. 6-8 (b) Timing chart of the pulse waveform with the definition of the pulse parameters.

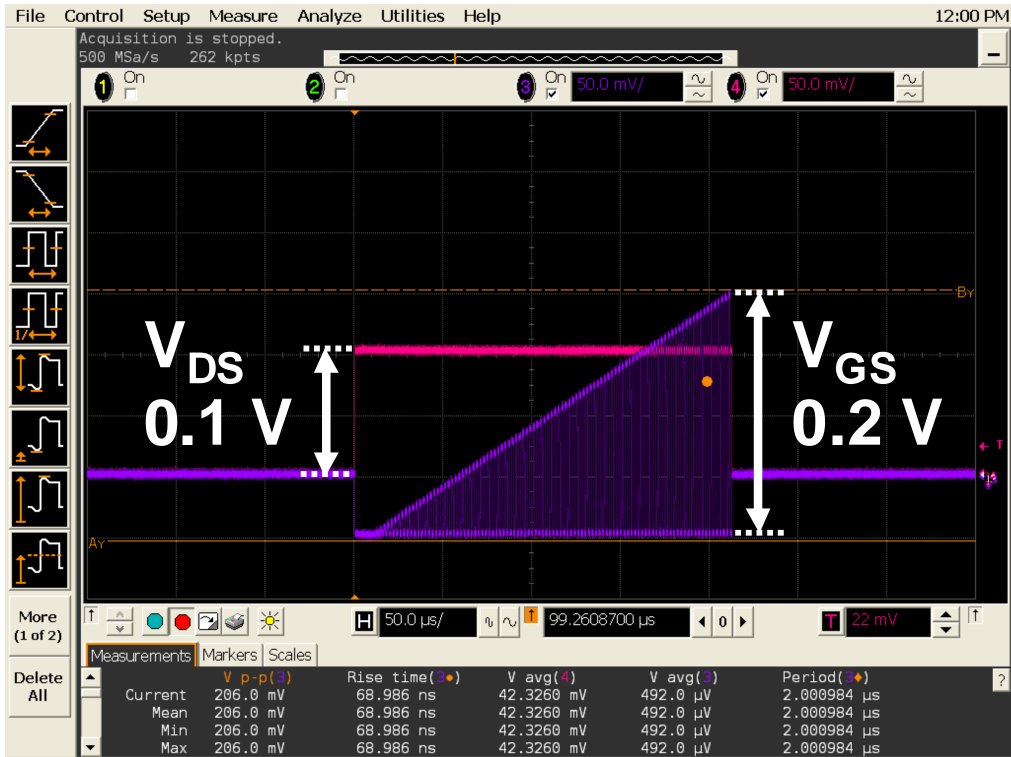

Fig. 6-9 (a) Example of the monitored voltage waveform as a function of time. The gate bias is a pulsed sweep, and the drain bias is a constant voltage.

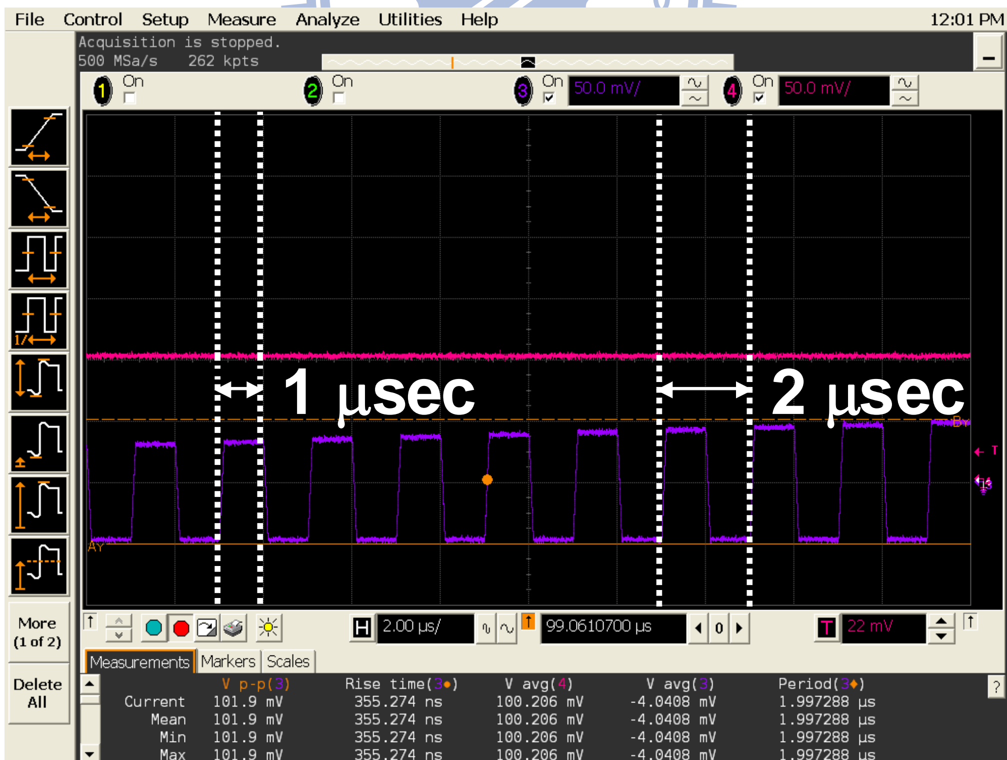

Fig. 6-9 (b) Enlarged view of 6-9(a) showing the output waveform corresponds to the user-defined waveform.

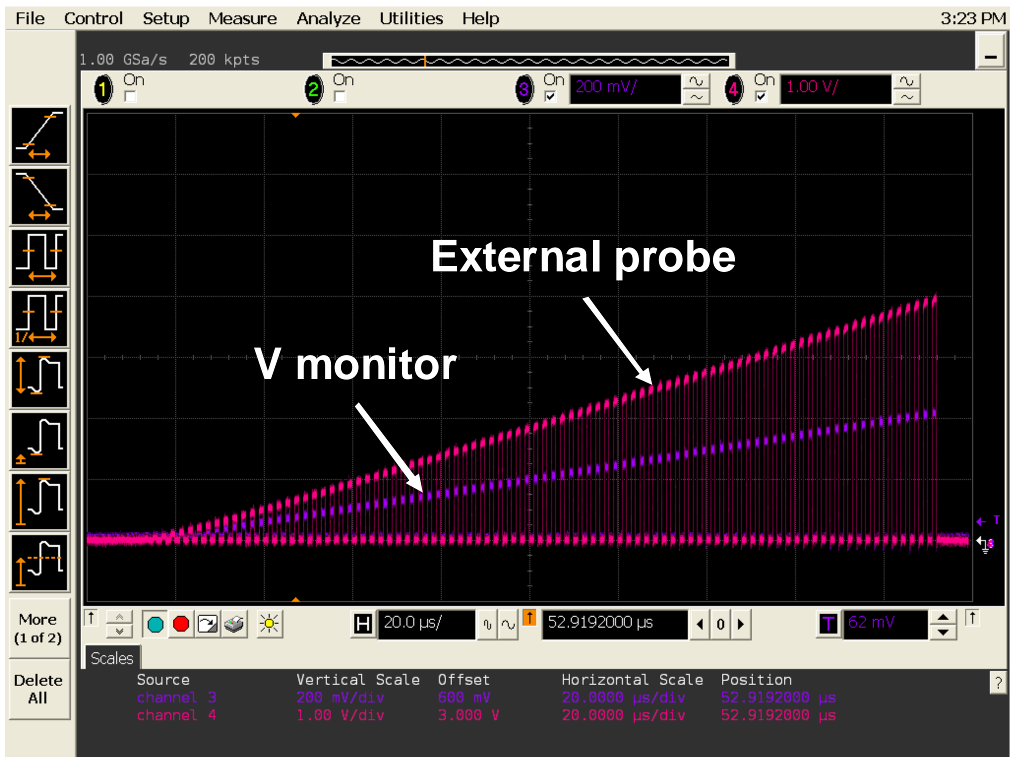

Fig. 6-10 (a) Gate voltage waveforms monitored by the V monitor and the external probe as a function of time.

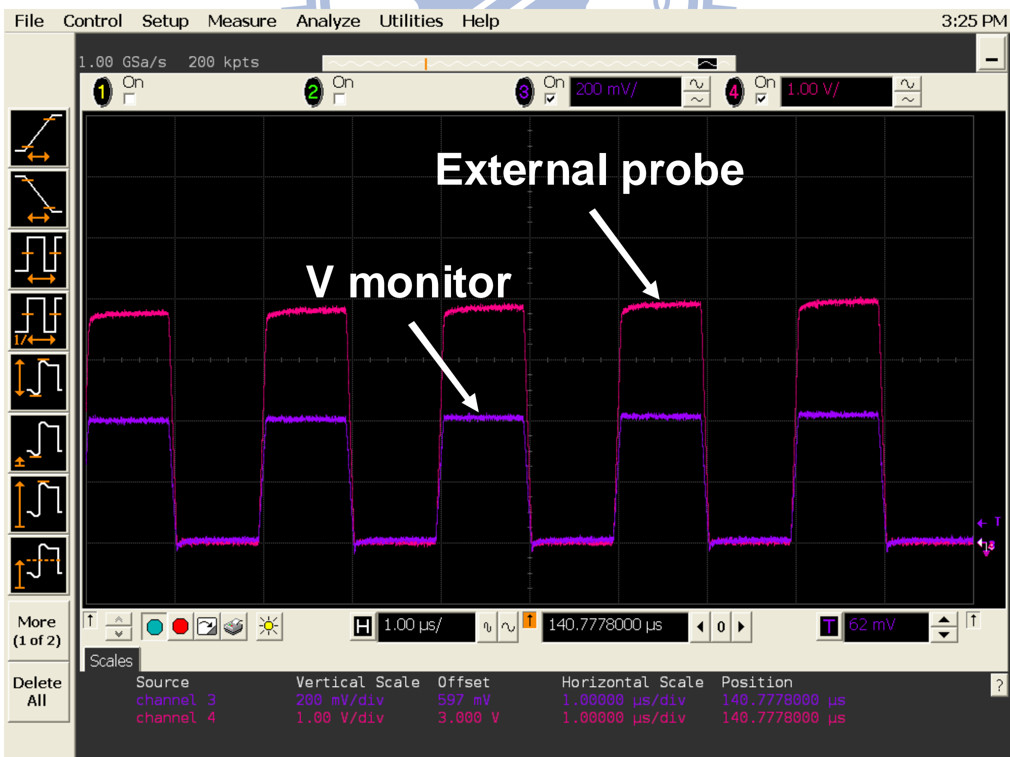

Fig. 6-10 (b) Enlarged view of 6-10(a) showing the RC time constant delay of the gate pad can be neglected during pulsed I-V measurements.

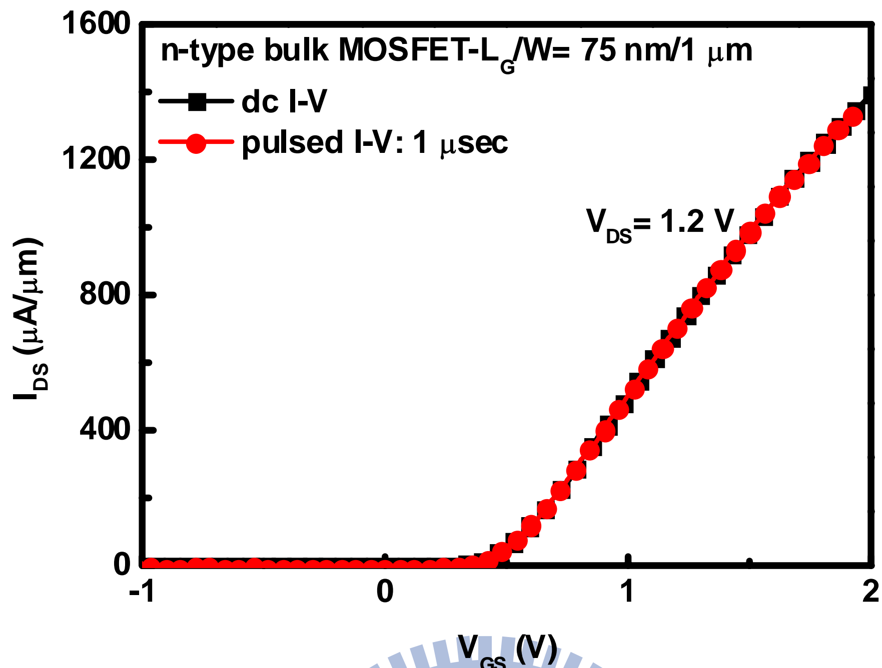

Fig. 6-11 (a) Pulsed I-V and dc I-V curves of the n-type bulk MOSFET with L_G/W= 75 nm/1 μm.

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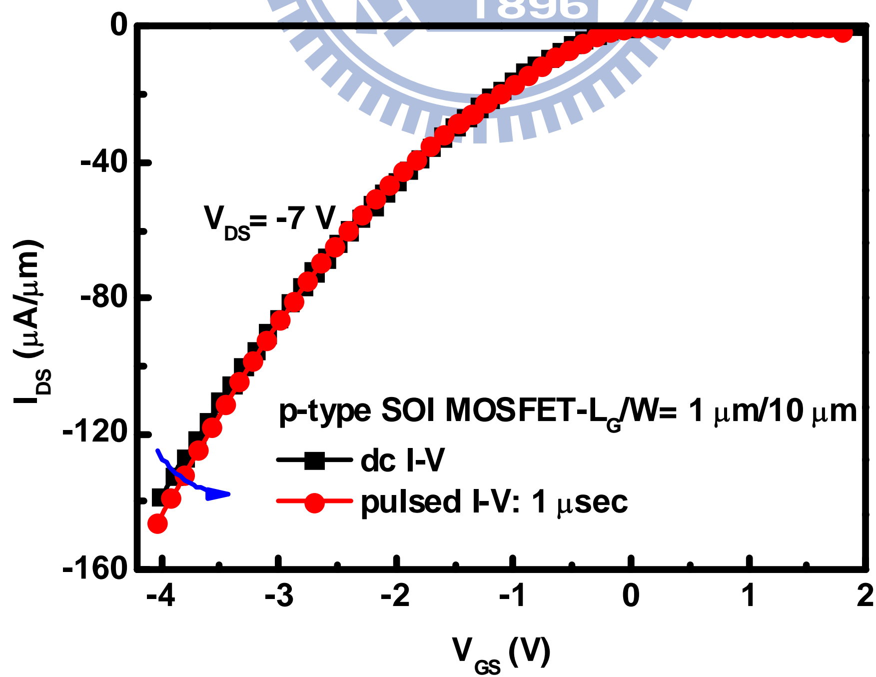


Fig. 6-11 (b) Pulsed I-V and dc I-V curves of the p-type SOI MOSFET with L_G/W= 1 μm/10 μm.

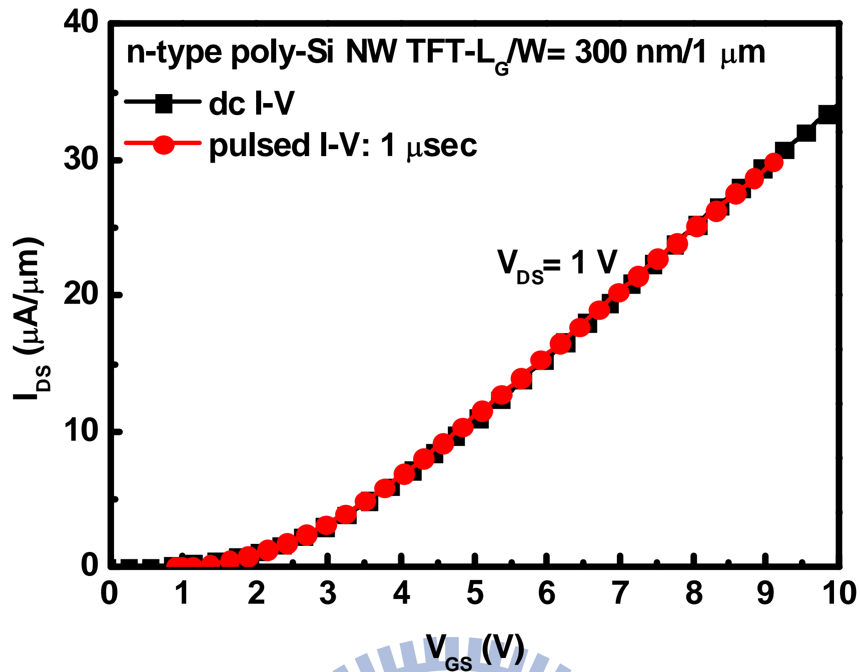


Fig. 6-12 Pulsed I-V and dc I-V curves of the n-type poly-Si NW TFT with L_G/W= 300 nm/1 μm.

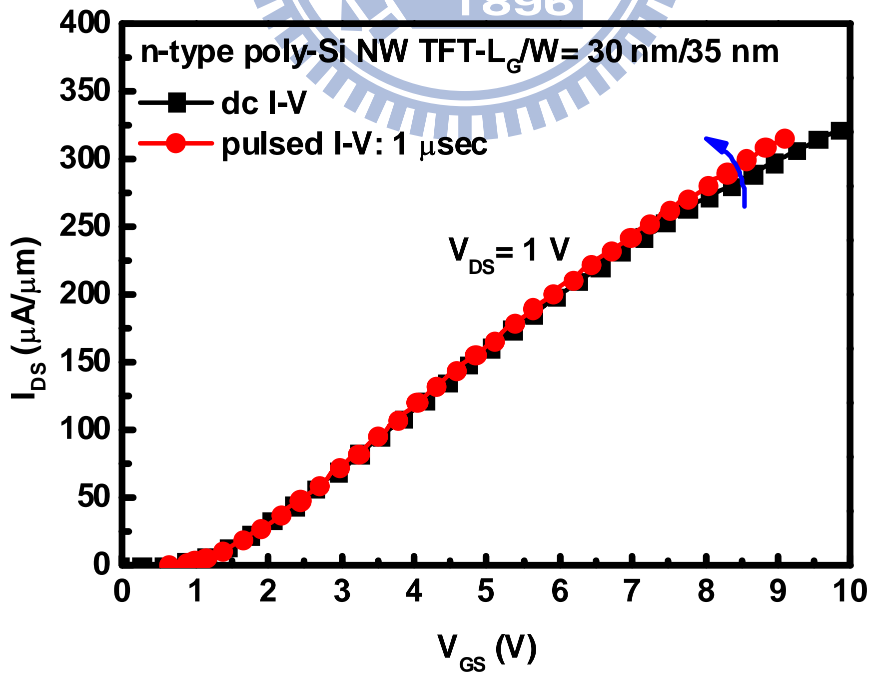


Fig. 6-13 Pulsed I-V and dc I-V curves of the n-type poly-Si NW TFT with L_G/W= 30 nm/35 nm.

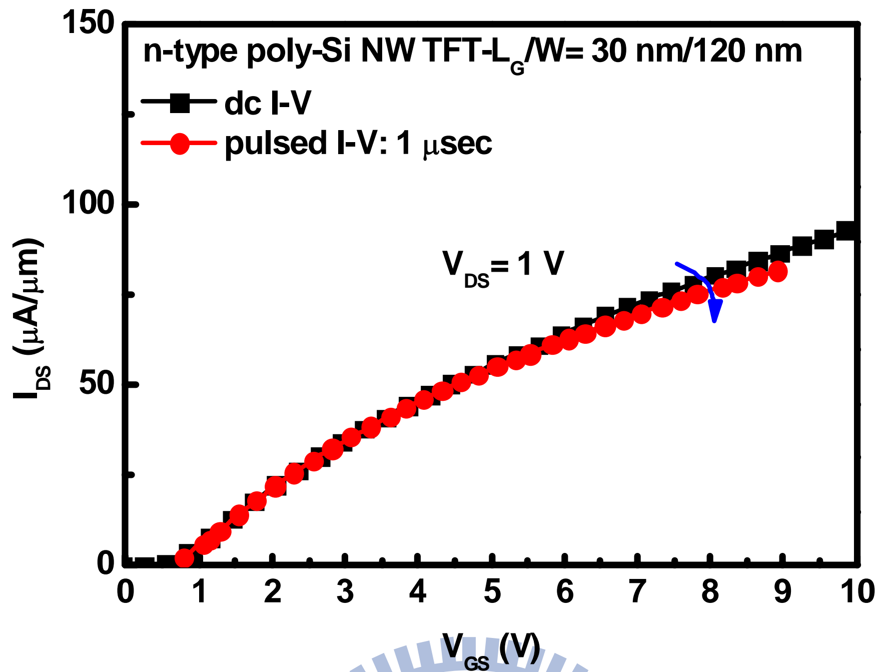


Fig. 6-14 Pulsed I-V and dc I-V curves of the n-type poly-Si NW TFT with L_G/W= 30 nm/120 nm.

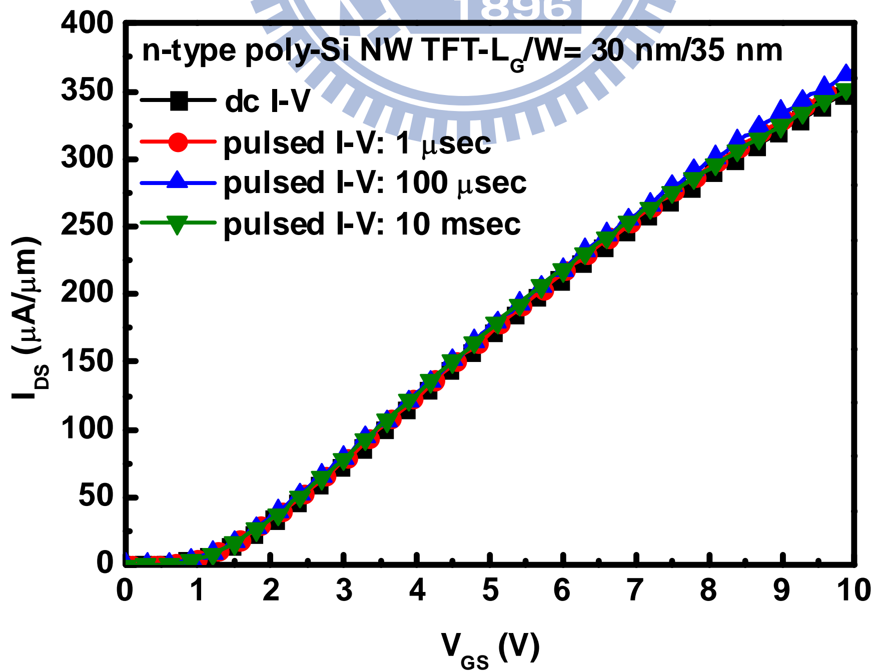


Fig. 6-15 Pulsed I-V curves with different pulse width of the n-type poly-Si NW TFT with L_G/W= 30 nm/35 nm.

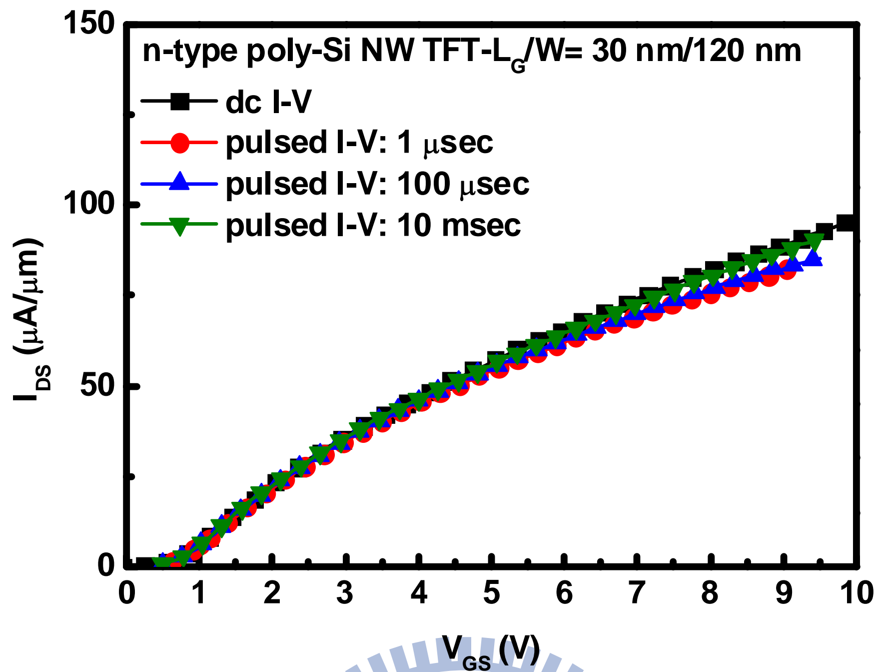


Fig. 6-16 Pulsed I-V curves with different pulse width of the n-type poly-Si NW TFT with L_G/W= 30 nm/120 nm.

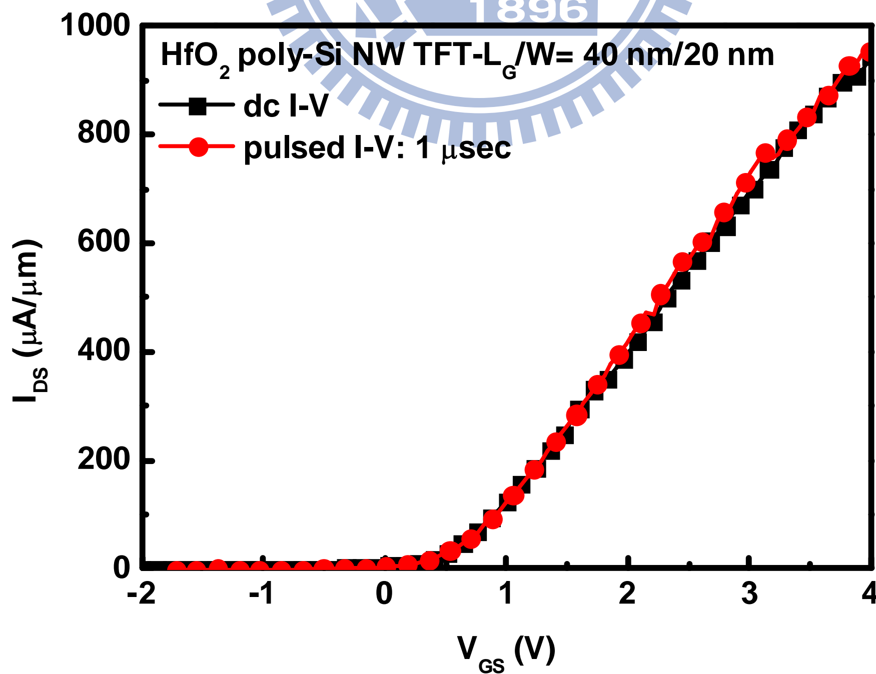


Fig. 6-17 Pulsed I-V and dc I-V curves of the n-type poly-Si NW TFT combined with the HfO_2 gate dielectric, and its L_G/W is equal to 40 nm/20 nm.

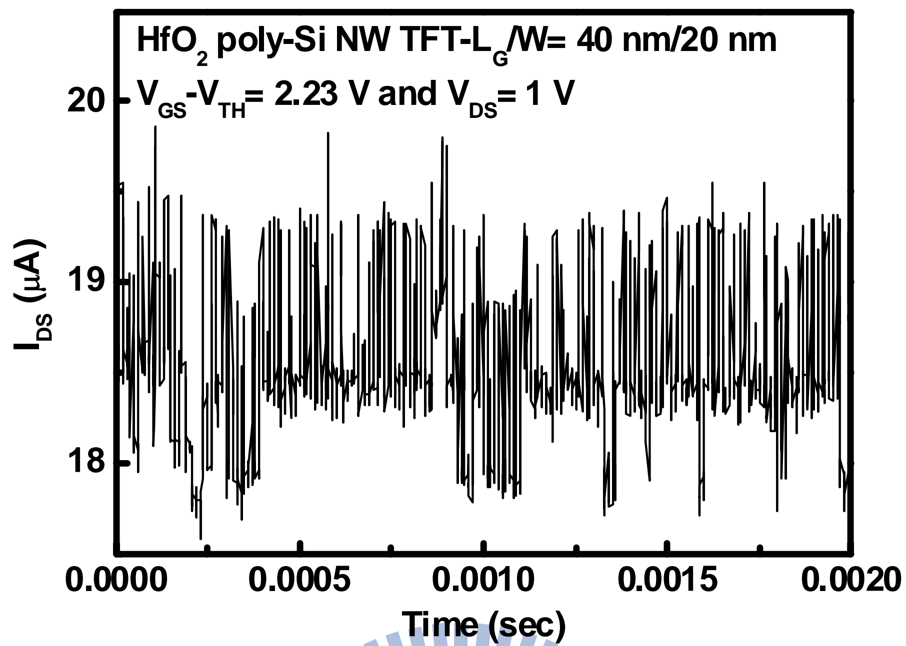


Fig. 6-18 Example of the RTN signal observed in the n-type poly-Si NW TFT with the HfO_2 gate dielectric, and its L_G/W is equal to 40 nm/20 nm.

Chapter 7

Random Telegraph Noise in Small-Area Poly-Si Nanowire Thin-Film Transistors

7.1 Introduction

The impact of L_G scaling (L_G < 100 nm) on poly-Si NW TFTs with different multi-gate structures has been studied in chapter 5 and 6. These devices exhibit excellent I-V characteristics and good short-channel characteristics. Recent successes in fabricating small-area poly-Si NW TFTs have opened up the possibility of producing the poly-Si-based 3D IC and 3D stackable TFT Flash memories in the future. Therefore, the noise properties of small-area poly-Si NW TFTs should also be simultaneously considered, especially for application in analog IC. LFN, 1/*f* noise, is the main noise component for these highly scaled devices since it increases as the reciprocal of the gate area [1]. The LFN in large-area poly-Si TFTs has been deeply investigated by several researchers [2-6]. On poly-Si TFTs, the carrier number fluctuation model as in single-crystalline MOSFETs was first proposed to explain the measured low-frequency 1/*f*-type noise spectra [2-3]. In this model, the spectra density of the drain current (I_D) noise is caused by the dynamic trapping and detrapping of free carriers into slow oxide traps [2]. However, C. A. Dimitriadis *et al.* found that only the carrier number fluctuation model was not adequate to explain all experimental noise data of their poly-Si TFTs, especially in the low I_D region [4]. They considered that the power spectrum of the I_D noise is also caused by the

grain-boundary potential barrier fluctuation owing to the dynamic trapping and detrapping of free carriers at the grain boundary. Therefore, according to the derivation model, the spectral dependence of the I_D noise deviated from the pure $1/f$ behavior and showed a $1/f^{\gamma}$ ($\gamma < 1$) law at higher frequencies [5]. Furthermore, the carrier number fluctuation model modified with correlated mobility fluctuation has been used to explain the higher excess noise in poly-Si TFTs [6-7]. According to the literature review, we conclude that the I_D noise arises from carrier number fluctuation and mobility fluctuation, which is similar to single-crystalline MOSFETs except that carrier number fluctuation is also originated from grain-boundary traps.

To the best of our knowledge, the LFN in small-area poly-Si NW TFTs has never been published previously. RTN is a LFN component and has been considered as the origin of LFN [8]. The RTN can be observed in several semiconductor devices as the device size continues to shrink, such as single-crystalline MOSFETs and junction field effect transistors (JFETs) [8-9]. The RTN in single-crystalline MOSFETs is related to carrier capture and emission processes by one or a few gate oxide traps (or interface states) [10-11], as illustrated in Fig. 7-1. It has become a main issue on sub-100-nm CMOS devices and flash memories [12-13]. The V_{TH} variation due to RTN affects the stability of SRAM and the MLC operation of Flash memory. In this work, we study the two-level and complex I_D-RTN of nano-scale n-type GAA poly-Si NW TFTs with the TEOS gate oxide for the first time. Furthermore, the influence of surface potential fluctuations induced by grain-boundary traps on the giant RTN relative amplitude is also discussed. Finally, we propose the carrier number fluctuation model induced by the grain-boundary trap, called the CNFGB model, and attempt to identify the origin of the fast-trap related RTN by high-temperature measurements.

The detailed process flow of the n-type GAA poly-Si NW TFTs used in this chapter has been described in chapter 5. The key parameters of all devices are listed in Table 7-1. The RTN measurements for different V_{GS} and a fixed V_{DS} of 1 V were done on these high-performance devices at room temperature. The fastest sampling rate of Agilent B1530A is 100 MHz, which enables the observations of the I_D switching with time resolution up to 10 nsec.

7.2 Results and Discussion

7.2.1 Two-Level I_D-RTN

The two-level I_D-RTN is typically seen in the time domain and frequently reported owing to the analysis convenience. Figure 7-2 shows an example of the two-level I_D-RTN of the device A. The histogram of the I_D distribution is shown in Fig. 7-3(a). The random switching between two discrete levels, the high-current and low-current levels, in the I_D is clearly observed. This observation means that only a single trap is active to repeatedly trap and detrap the channel electrons. When an acceptor-type trap captures a channel electron, the low I_D level arises from the reduced carrier density and the increased carrier scattering, and vice versa. As a two-level I_D-RTN signal results from a single acceptor-type trap, the capture time (τ_c) and the emission time (τ_e) are defined as the duration time of the high-current level and the low-current level, respectively, as shown in Fig. 7-2. The RTN amplitude (ΔI_D) is related to carrier number and mobility fluctuations, and its definition is also shown in Fig. 7-3(a). According to commonly used analysis methods proposed by Z. Celik-Butler [14], we can calculate the average capture time ($\langle\tau_c\rangle$), the average

emission time (<τ_e>), and the RTN relative amplitude ($\Delta I_D/I_D$) from the raw data presented in Fig. 7-2.

The time-domain signal can be transformed into the frequency domain via Fourier transformation. As a two-level RTN signal is transformed into the frequency domain, the Lorentzian type of power spectrum ($S_I(f)$) can be obtained. Its general form is shown below [14]:

$$S_I(f) = \frac{\kappa}{1+\left(f/f_0\right)^2}, \qquad (7\text{-}1)$$

where $\kappa = \frac{4\tau^2 \Delta I_D^2}{\langle\tau_e\rangle + \langle\tau_c\rangle}$, $f_0 = \frac{1}{2\pi\tau}$, and $\frac{1}{\tau} = \left(\frac{1}{\langle\tau_e\rangle} + \frac{1}{\langle\tau_c\rangle}\right)$. Figure 7-3(b) shows the Lorentzian-type noise power spectral density (PSD) of the device A biased at V_{GS}-V_{TH}= -0.43 V and V_{DS}= 1 V. The corner frequency (f_0) is 1.82×10^{-1} Hz, and the PSD is approximately proportional to the reciprocal of the square of the frequency.

Figure 7-4 shows the I_D waveform of the device A biased in the weak inversion region at different V_{GS}. The V_{DS} is fixed at 1 V. According to the time scale (the *x* axis) in Fig. 7-4, we can find that the transition time between the two current levels is on a time scale of a few seconds. Therefore, the single active trap existing within the device A belongs to a slow trap. The <τ_c> and <τ_e> values of the device A are calculated and plotted as a function of V_{GS}-V_{TH} in Fig. 7-5. The <τ_c> value decreases from 8.149 to 1.506 sec with increasing V_{GS}-V_{TH}. On the other hand, the <τ_e> value increases from 0.925 to 2.254 sec with increasing V_{GS}-V_{TH}. Therefore, the single active trap is identified as an acceptor-type trap. Furthermore, according to the observations of RTN in single-crystalline MOSFETs, the <τ_c> and <τ_e> values for a slow trap are in the range of 0.1 to 1 sec, and the slow trap is considered as a gate oxide trap near the Si/gate-oxide interface [15]. It is reasonable to observe RTN

caused by the gate oxide trap in small-area poly-Si NW TFTs since the quality of the TEOS gate oxide is worse than that of the conventional thermally grown gate oxide. Therefore, the RTN phenomenon in small-area poly-Si NW TFTs could arise from the slow gate oxide trap. Furthermore, it should be noted that the slow trap can also be observed in the strong inversion region.

The position of the slow gate oxide trap can be extracted by the V_{GS} dependence of $\ln(\langle\tau_c\rangle/\langle\tau_e\rangle)$, and its conventional expression can be derived as follows [16]:

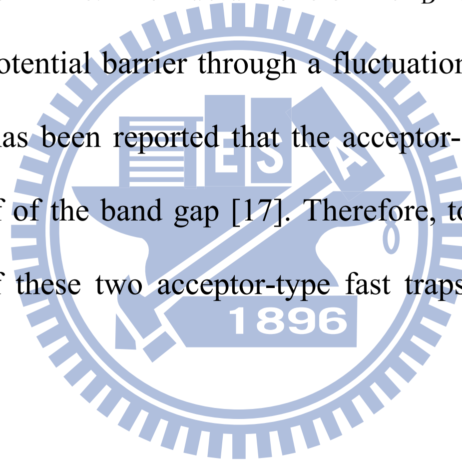
$$\frac{d\left(\ln\frac{\langle\tau_c\rangle}{\langle\tau_e\rangle}\right)}{dV_{GS}} \cong -\frac{q}{\kappa_B T}\times\frac{\chi_T}{T_{ox}}, \qquad (7\text{-}2)$$

where χ_T is the trap position located away from the poly-Si/gate-oxide interface. The position of the gate oxide trap is extracted from the slope of $\ln(\langle\tau_c\rangle/\langle\tau_e\rangle)$ vs. V_{GS} plot (right y axis) and is found to be 4.55 nm by using equation (7-2). This high value of χ_T results in long capture and emission times.

In addition to the slow gate oxide trap, the RTN can also arise from the fast trap [11]. We also observe the two-level I_D-RTN caused by a single fast trap. Figure 7-6(a) shows an example of the two-level I_D-RTN observed in the device B. The transition times of the device B are much shorter than those of the device A, which indicates the single active trap is a fast trap instead of a slow trap. Figure 7-6(b) shows the PSD of the device B biased at V_{GS}-V_{TH}= 1.26 V and V_{DS}= 1 V, and its PSD is close to a Lorentzian-type spectrum with f_0=2.37x10^3 Hz. The f_0 value is consistent with the observed switching times of the device B. Figure 7-7 shows the I_D waveform of the device B biased in the strong inversion region with different V_{GS} and a fixed V_{DS} of 1 V. Figure 7-8 shows the V_{GS}-V_{TH} dependence of the $\langle\tau_c\rangle$ and $\langle\tau_e\rangle$ values of the device B, which indicates that the fast trap is also acceptor-type. The fast trap can also

be observed in both device C and device D biased in the weak inversion region, as shown in Fig. 7-9 and Fig. 7-10, respectively. Figure 7-11 shows the V_{GS}-V_{TH} dependence of the $<\tau_c>$ and $<\tau_e>$ values of the device C and device D, respectively, and these two fast traps are also acceptor-type.

In single-crystalline MOSFETs, the acceptor-type fast trap is regarded as the process-induced interface state at the Si/gate-oxide interface [11]. It is reasonable to observe the acceptor-type interface state as the Fermi level moves toward the conduction band edge. However, for small-area poly-Si TFTs, grain-boundary traps within the poly-Si channel region may also result in the RTN phenomenon just like LFN in large-area poly-Si TFTs. The fluctuations of the I_D result from the fluctuations of the grain-boundary potential barrier through a fluctuation of the charge trapped at the grain boundary. It has been reported that the acceptor-like grain-boundary traps locates at the upper half of the band gap [17]. Therefore, to clarify the difference in the RTN mechanism of these two acceptor-type fast traps, we derive the CNFGB model in section 7.2.3.



7.2.2 Complex I_D-RTN

When more than one trap is active, the complex I_D-RTN can be observed. A very high $\Delta I_D/I_D$ value can also result from the complex I_D-RTN. Figure 7-12 shows an example of the complex I_D-RTN pattern observed in the device E. Multi-level current switching is clearly observed, showing that RTN arises from more than one trap. Moreover, the histograms in Fig. 7-13 show six major peaks and reveal that three traps are simultaneously active. It is difficult to analyze the six-level complex I_D-RTN signal and characterize the property of each individual trap. Therefore, the four-level complex I_D-RTN signal shown in Fig. 7-14 of the device F is analyzed in this section.

From Fig. 7-15, the I_D switching between four discrete current levels is clearly observed, which means two fast traps are both active at the same time. In the device F, the active trap with shorter time constants is called the faster trap, and the other active trap with longer time constants is named as the fast trap. The high I_D level and low I_D level labeled in Fig. 7-16 and 7-17 represent the fast trap is empty or filled, respectively. According to Fig. 7-16 and 7-17, the $<\tau_c>$, $<\tau_e>$, and ΔI_D values for the faster trap are almost the same whether the fast trap is empty or filled. Therefore, we conclude that these two fast traps are independent in the device.

7.2.3 Carrier Number Fluctuation Model

The $\Delta I_D/I_D$ expression of single-crystalline MOSFETs can be written as [18]:

$$\frac{\Delta I_D}{I_D} = -\frac{1}{W \times L_G}\left(\frac{1}{N} \pm \alpha\mu\right), \tag{7-3}$$

where N is the carrier density and α is the scattering coefficient. The first term on the right-hand side of equation (7-3) presents the carrier number fluctuation induced by the slow gate oxide trap or the fast interface state. The second term corresponds to mobility fluctuation.

Next, we derive the CNFGB model. The linear-region I_D equation of poly-Si TFTs deduced by J. Levinson *et al.* is shown below [19]:

$$I_D = \mu\frac{W}{L_G}\exp\left(\frac{-qV_B}{\kappa T}\right)C_{ox}\left(V_{GS} - V_{TH}\right)V_{DS} = \mu\frac{W}{L_G}\exp\left(\frac{-qV_B}{\kappa T}\right)\left(qNt_{ch}\right)V_{DS}, \tag{7-4}$$

$$V_B = \frac{Q_T^2}{8q\varepsilon_{Si}N}, \tag{7-5}$$

$$N = \frac{C_{ox}\left(V_{GS} - V_{TH}\right)}{qt_{ch}}, \tag{7-6}$$

where Q_T is the grain-boundary trapped charge per unit area, N is the channel inversion charge per unit volume, and t_{ch} is the channel thickness. The fluctuation of the I_D results from the fluctuation of the grain-boundary potential barrier via the charge trapping/detrapping at the grain boundary, so ΔI_D can be expressed as follows:

$$\Delta I_D = \frac{\Delta I_D}{\Delta V_B} \times \frac{\Delta V_B}{\Delta Q_T} \times \Delta Q_T \tag{7-7}$$

The $\frac{\Delta I_D}{\Delta V_B}$ and $\frac{\Delta V_B}{\Delta Q_T}$ terms can be obtained from equation (7-4) and equation (7-5) by using differential techniques. Hence, equation (7-7) can be rewritten as follows:

$$\Delta I_D = \frac{-q}{\kappa T} \times I_D \times \frac{Q_T}{4q\varepsilon_{Si}N} \times \Delta Q_T \tag{7-8}$$

If we assume that only one grain-boundary trap is active within the poly-Si channel region for the two-level I_D-RTN signal, the ΔQ_T term is thus equal to $\frac{1}{W \times L_G}$. Therefore, equation (7-8) can be rearranged to obtain the CNFGB model, as shown below:

$$\frac{\Delta I_D}{I_D} = \frac{-q}{\kappa T} \times \frac{Q_T}{4\varepsilon_{Si}N} \times \frac{1}{W \times L_G} \tag{7-9}$$

The complete expression of the $\Delta I_D/I_D$ must include the mobility fluctuation term. The mobility fluctuation model induced by the grain-boundary trap results from Coulomb scattering at the grain boundary, as well as Coulomb scattering at the Si/gate-oxide interface. Therefore, the mobility fluctuation term of equation (7-3) is added into equation (7-9) and the current fluctuation model becomes:

$$\frac{\Delta I_D}{I_D} = -\frac{1}{W \times L_G}\left(\frac{q}{\kappa T} \times \frac{Q_T}{4\varepsilon_{Si}N} \pm \alpha\mu\right) \tag{7-10}$$

According to equation (7-10), we can find that the carrier number fluctuation term is inverse proportional to the absolute temperature. However, the carrier number fluctuation term in equation (7-3) is independent of the absolute temperature. Therefore, we can identify the fast grain-boundary trap and the fast interface state by measuring the $\Delta I_D/I_D$ values of the poly-Si TFT biased in strong inversion at different temperatures. Although mobility fluctuation also depends on the measurement temperature, it becomes less significant at high V_{GS}. When the device is biased in the strong inversion region, the screening effect of the inversion layer charge can exclude the contribution of number fluctuation.

The three active traps in the device B, device C, and device D are all fast traps. For the device C and device D, their RTN phenomena are only observed in the weak inversion region, so their trap types are indistinguishable from observable RTN behaviors. On the contrary, the RTN phenomenon of the device B can be observed in the strong inversion region. Therefore, the temperature-dependent RTN measurements were only performed on the device B. The $\Delta I_D/I_D$ values at 300 K and 350 K are shown in Fig. 7-18. The V_{TH} value is defined by the G_{mmax} method. At different temperatures, the V_{GS}-V_{TH} value is fixed to obtain the same carrier density. In this figure, the rectangular and triangular marks represent the measurement results at 300 K and 350 K, respectively. The circular marks represent the $\Delta I_D/I_D$ values at 350 K calculated from the values at 300 K according to the equation (7-10) but omitting the contribution of the number fluctuation. The $\Delta I_D/I_D$ values indeed decreases with increasing the measurement temperature and nearly corresponds to the prediction equation (7-10). Since we neglect the contribution of the number fluctuation, the calculated $\Delta I_D/I_D$ values are slightly higher than the measured $\Delta I_D/I_D$ values, especially for low V_{GS}-V_{TH} values. In fact, the mobility fluctuation is also slightly

dependent on the measurement temperature, and Fig. 7-19 shows the V_{GS}-V_{TH} dependence of the transconductance (G_m) value of the device B at 300 K and 350 K. According to this figure, once the biased V_{GS}-V_{TH} value is high enough, we can neglect the contribution of number fluctuation. The calculated result is gradually close to the measured result. Therefore, we consider that the active trap in the device B is the grain-boundary trap instead of the interface state. In other words, the grain-boundary trap could also result in the RTN phenomenon as the device size scales down to nanoscale.

Figure 7-20 compares the $\Delta I_D/I_D$ values of some devices as a function of V_{GS}-V_{TH}. According to equation (7-3) and equation (7-10), all of them have high $\Delta I_D/I_D$ values higher than 1 % owing to their ultra-small gate area [15]. Moreover, the entire channel can be effectively affected by the active trap because of the ultra-thin poly-Si body. The $\Delta I_D/I_D$ values decrease with the increase of V_{GS} due to the increase of the charges in the inversion layer and the screening of the trapped charges. We also find that the $\Delta I_D/I_D$ values of the device A are higher than those of the device C because of device area scaling. Furthermore, in weak inversion, it is notable that the $\Delta I_D/I_D$ values of the non-passivated device D are about two times higher than those of the passivated device C. The only difference in the process flow between the device C and device D is the NH_3 plasma treatment process. The device C can be regarded as the single-crystal-like device after applying the NH_3-plasma treatment. In contrary to the device C, there are still a few grain-boundary traps distributed in the poly-Si channel region of the device D. It has been confirmed that surface potential fluctuation caused by random discrete dopants can significantly increase the $\Delta I_D/I_D$ values as the device is biased in the weak inversion region [20]. Similarly, for poly-Si TFTs, surface potential fluctuation in the poly-Si channel region can result from

grain-boundary traps as well as random discrete dopants. As the poly-Si TFT is biased in the weak inversion region, the channel electrons select the current path with a lower effective grain-boundary potential barrier height to conduct from the source to drain electrodes [21]. Consequently, the effective conducting width is narrower than the device width. Once the RTN trap locates near the current path, it will produce RTN with high $\Delta I_D/I_D$ values. The effect of surface potential fluctuations induced by grain-boundary traps can be suppressed by using the NH_3 plasma treatment process, so the $\Delta I_D/I_D$ values of the device C is around two times smaller than those of the device D.

7.3 Conclusions

In this chapter, the RTN phenomenon of small-area poly-Si NW TFTs is investigated for the first time. The CNFGB model is proposed which attempts to distinguish between the fast grain-boundary trap and the fast interface state. If the RTN phenomenon induced by the fast trap occurs in the strong inversion region, we can identify the fast grain-boundary trap and the fast interface state by measuring the $\Delta I_D/I_D$ values at different temperatures. Since RTN is a single trap or few traps phenomenon, it is seldom observed on the long-channel or non-passivated poly-Si TFTs. However, the RTN phenomenon can be easily observed on the nano-scale poly-Si TFTs in either weak inversion or strong inversion region owing to device area scaling. The RTN phenomenon could also result from the process-induced slow oxide trap. Very high $\Delta I_D/I_D$ values arise from ultra-small gate area and/or multiple active traps. Furthermore, to explain the highest $\Delta I_D/I_D$ values of the GAA poly-Si NW TFT without the NH_3 plasma passivation, we consider that the effect of surface potential fluctuations induced by grain-boundary defects in the poly-Si channel region.

High-temperature measurement results are shown to prove the accuracy of the CNFGB model. Therefore, RTN of the high-performance small-area poly-Si NW TFTs would be a serious concern for 3D IC and 3D stackable TFT Flash memories. It is necessary to improve the quality of the gate oxide and reduce the interface states at the poly-Si/gate-oxide interface and grain-boundary traps within the poly-Si channel region.

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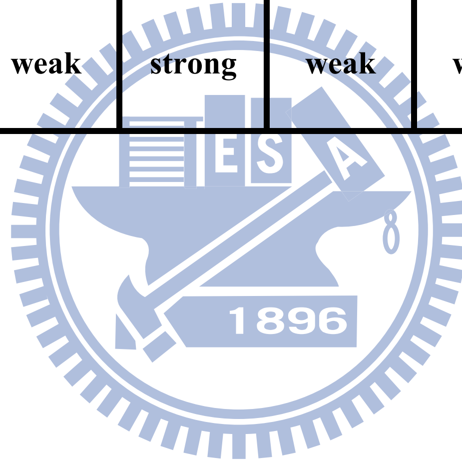
Table 7-1 Key parameters of all devices biased at V_{DS}= 1 V. All devices have the same gate oxide thickness of 25 nm and poly-Si channel thickness of 8 nm.

Device ID	A	B	C	D	E	F
Gate length (L_G)	30 nm	60 nm	60 nm	60 nm	60 nm	60 nm
Nanowire width (W)	35 nm	35 nm	35 nm	35 nm	35 nm	35 nm
V_{TH} (V)	1.241	1.348	1.519	3.058	1.527	1.536
Subthreshold swing (mV/Dec.)	202	150	163	434	161	194
NH_3 plasma treatment	Yes	Yes	Yes	No	Yes	Yes
Number of active traps	one	one	one	one	three	two
Trap type (slow/fast trap)	slow	fast	fast	fast	fast	fast
Detect the RTN signal in strong/weak inversion	weak	strong	weak	weak	strong	weak and strong



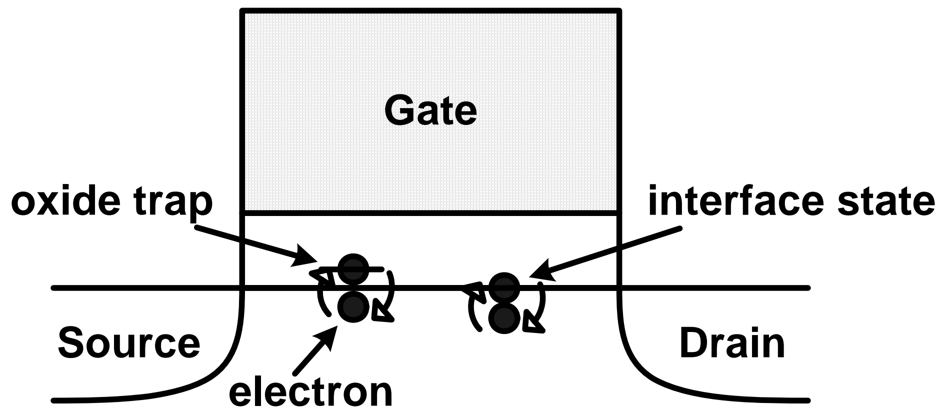


Fig. 7-1 Illustration of electron trapping and detrapping by the oxide trap and interface state.

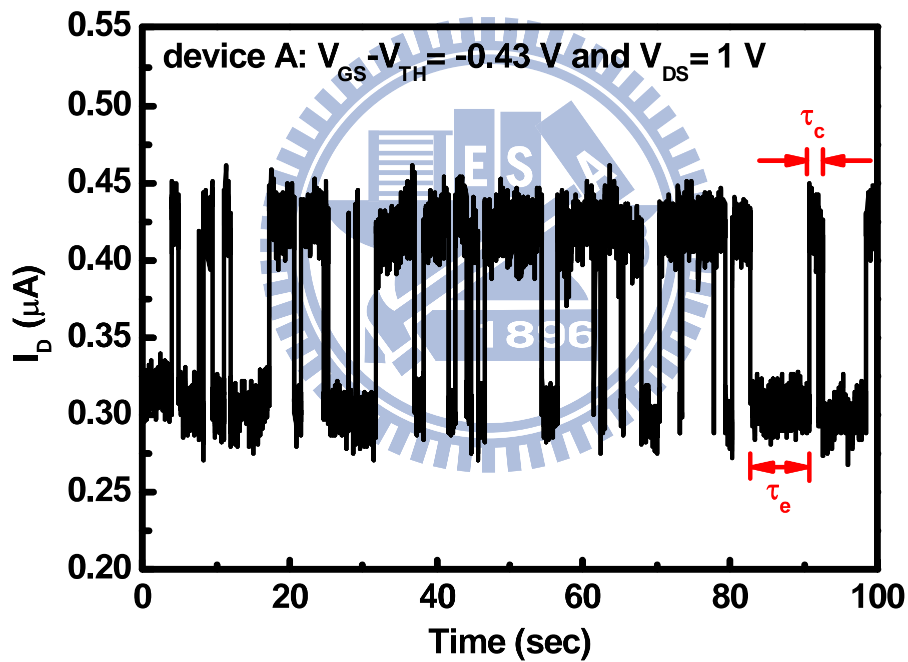


Fig. 7-2 Example of the two-level I_D-RTN observed in the device A. The definition of the capture time (τ_c), the emission time (τ_e), and the RTN amplitude (ΔI_D) are labeled.

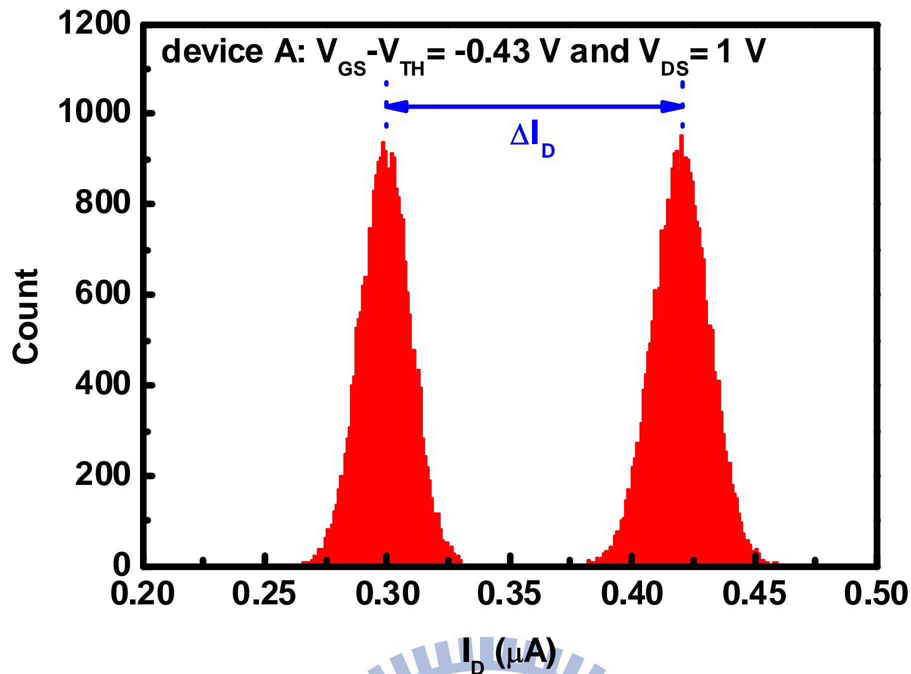


Fig. 7-3 (a) Histogram of the time-domain data of the device A biased at V_{GS}-V_{TH}= -0.43 V and V_{DS}= 1 V.

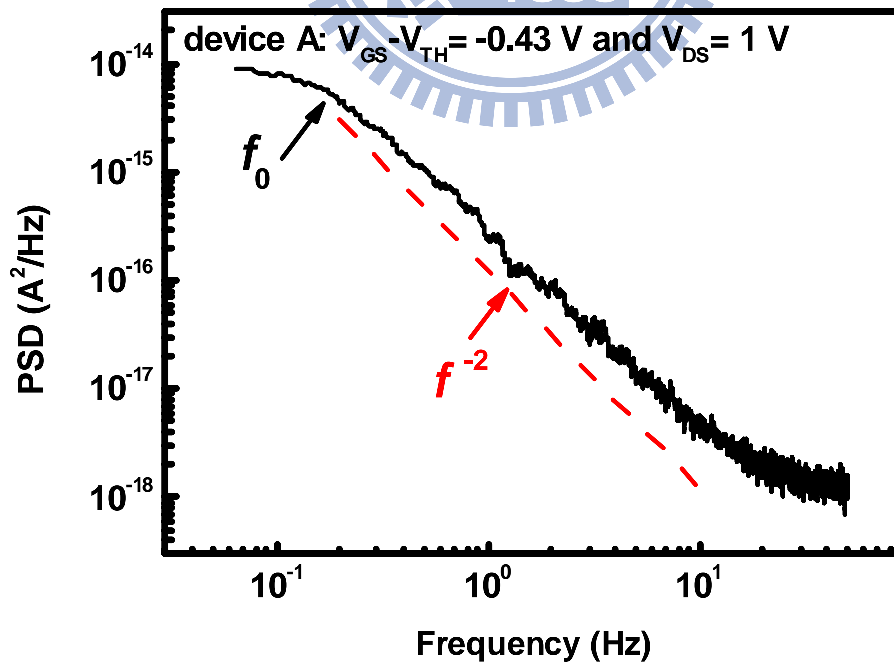


Fig. 7-3 (b) PSD of the device A biased at V_{GS}-V_{TH}= -0.43 V and V_{DS}= 1 V.

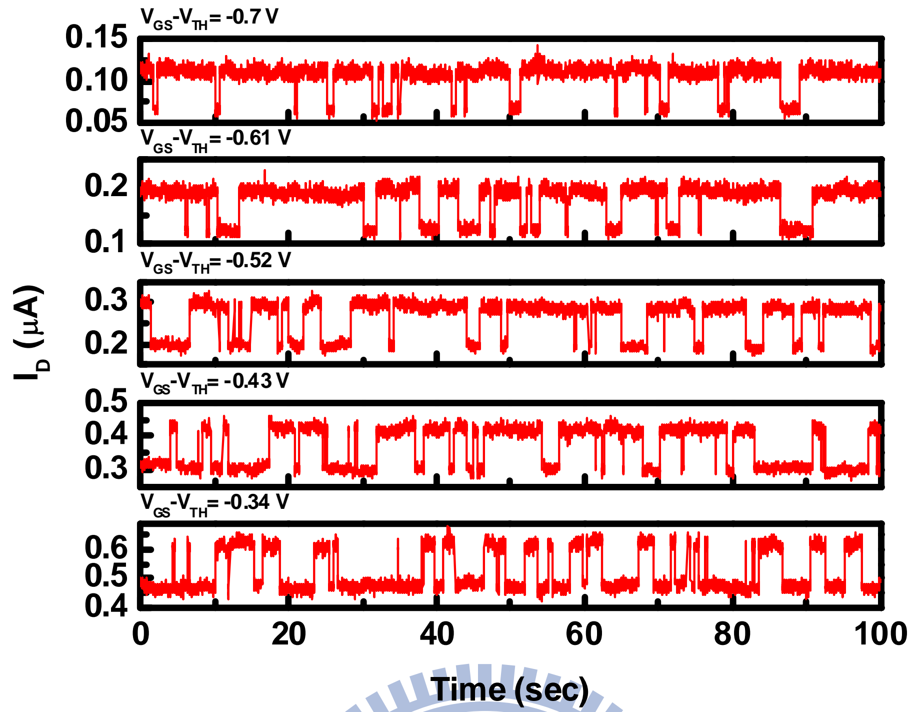


Fig. 7-4 I_D waveform of the device A with different V_{GS} and a fixed V_{DS} of 1 V.

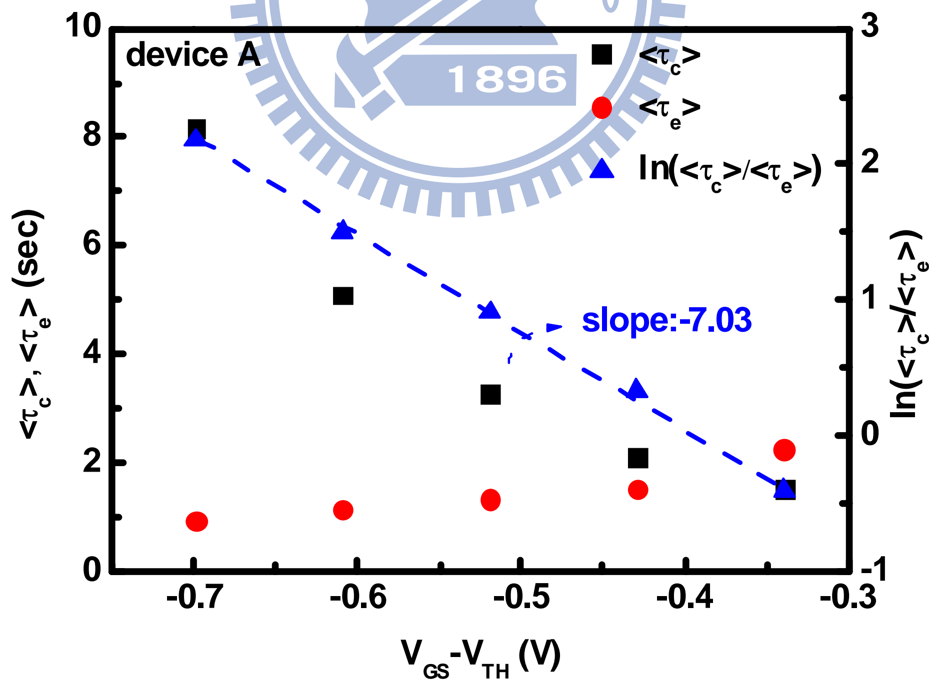


Fig. 7-5 $\langle\tau_c\rangle$, $\langle\tau_e\rangle$, and $\ln(\langle\tau_c\rangle/\langle\tau_e\rangle)$ values of the device A as a function of V_{GS}-V_{TH}.

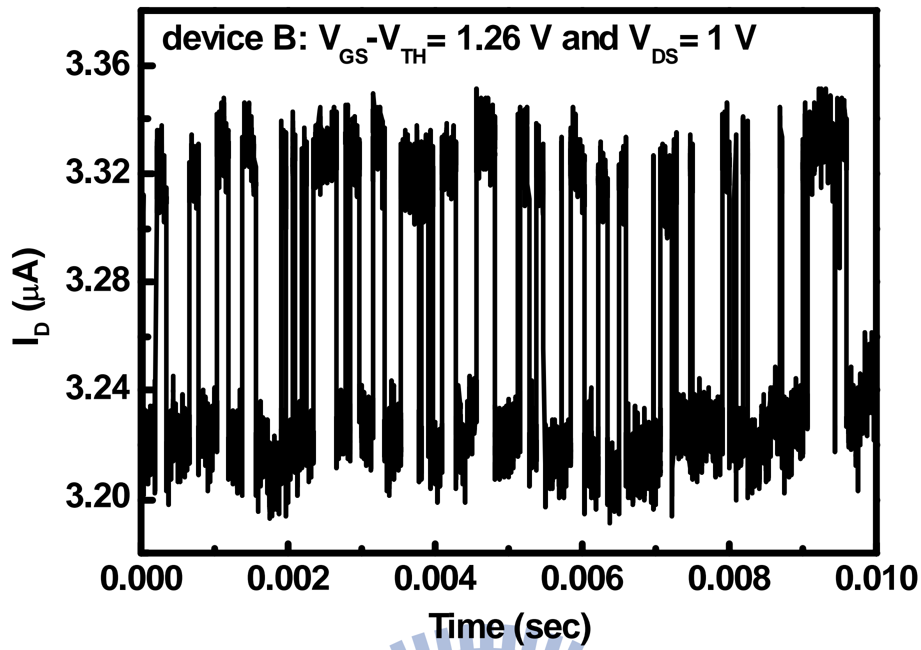


Fig. 7-6 (a) Example of the two-level I_D-RTN observed in the device B.

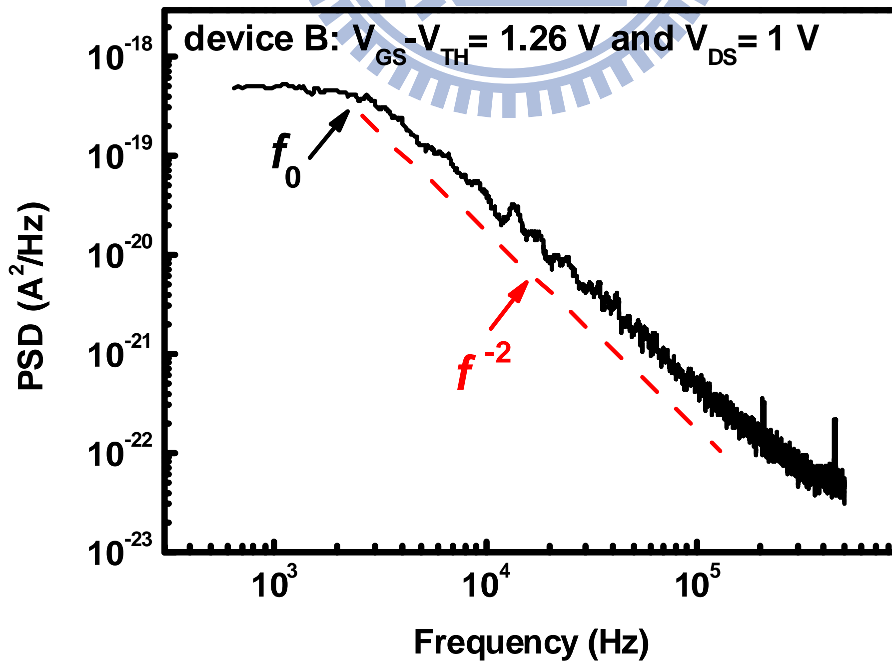


Fig. 7-6 (b) PSD of the device B biased at V_{GS}-V_{TH}= 1.26 V and V_{DS}= 1 V.

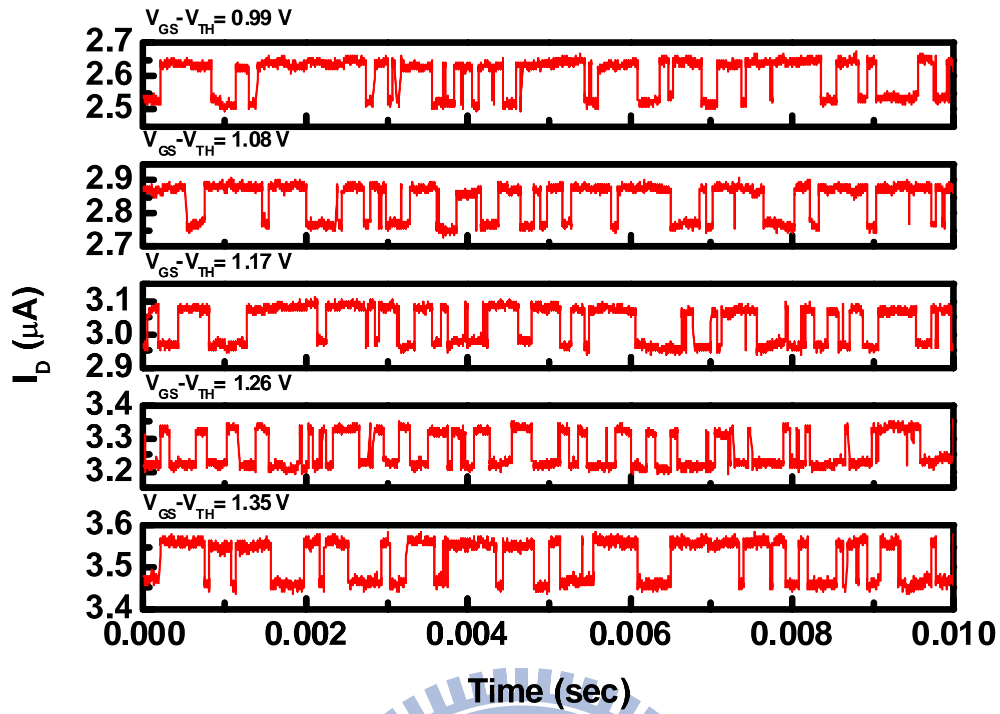


Fig. 7-7 I_D waveform of the device B with different V_{GS} and a fixed V_{DS} of 1 V.

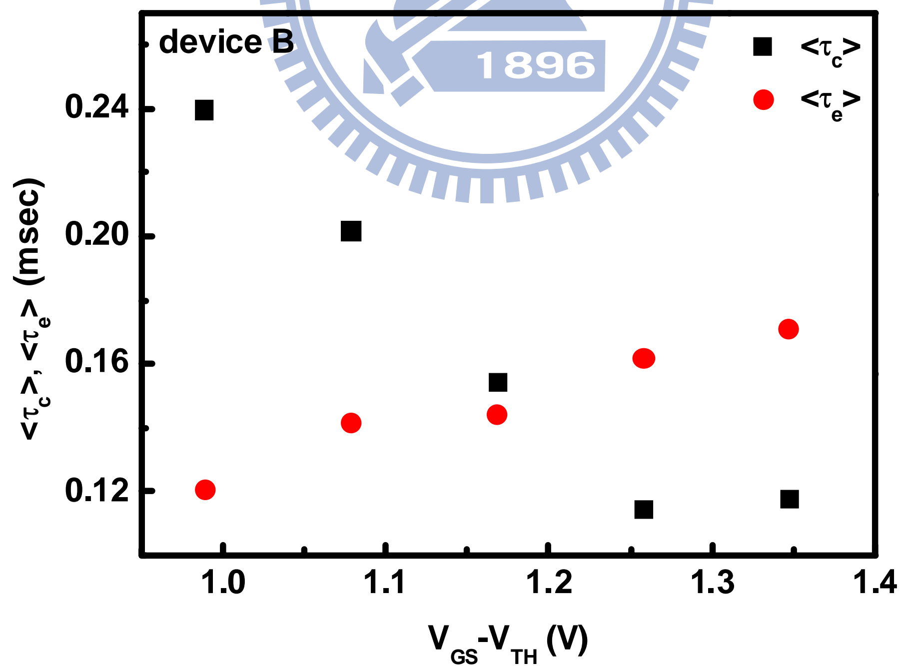


Fig. 7-8 $<\tau_c>$ and $<\tau_e>$ values of the device B as a function of V_{GS}-V_{TH}.

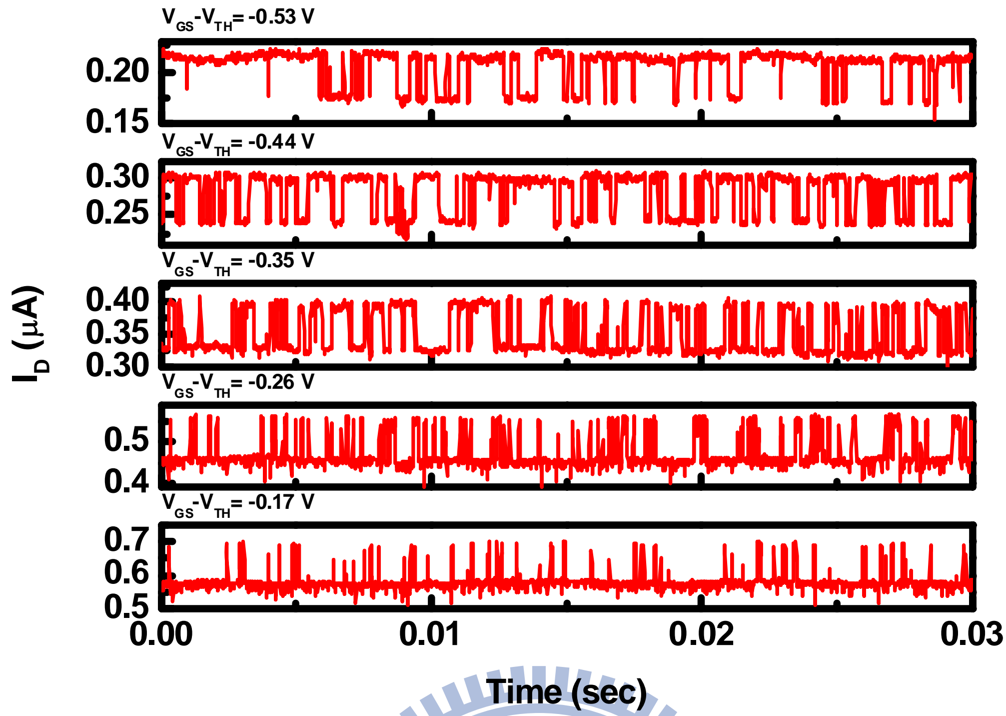


Fig. 7-9 I_D waveform of the device C with different V_{GS} and a fixed V_{DS} of 1 V.

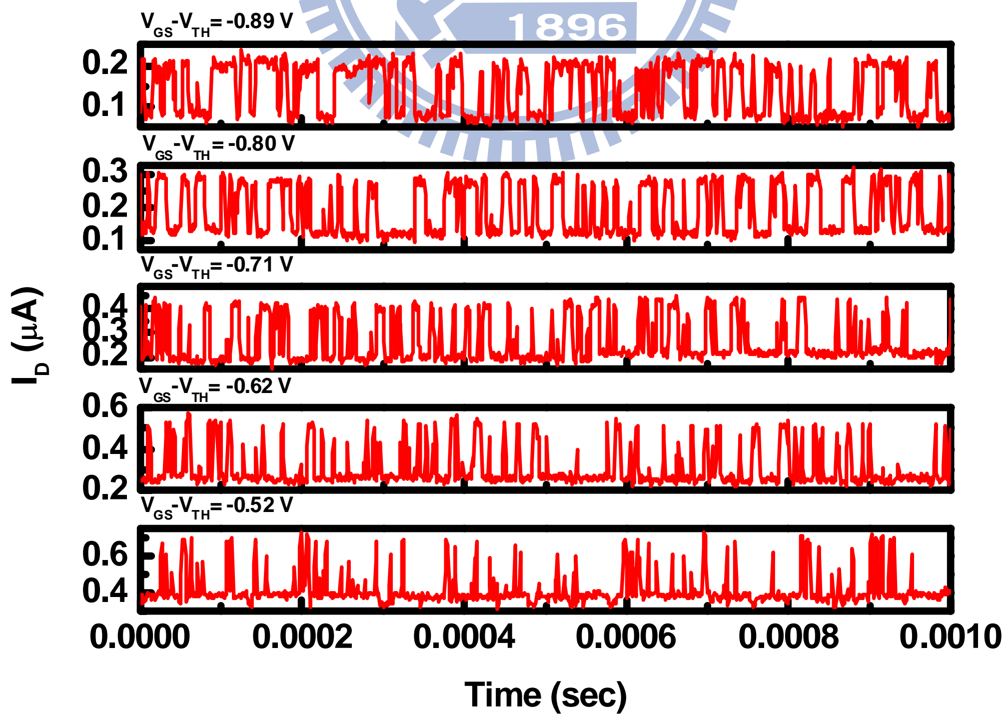


Fig. 7-10 I_D waveform of the device D with different V_{GS} and a fixed V_{DS} of 1 V.

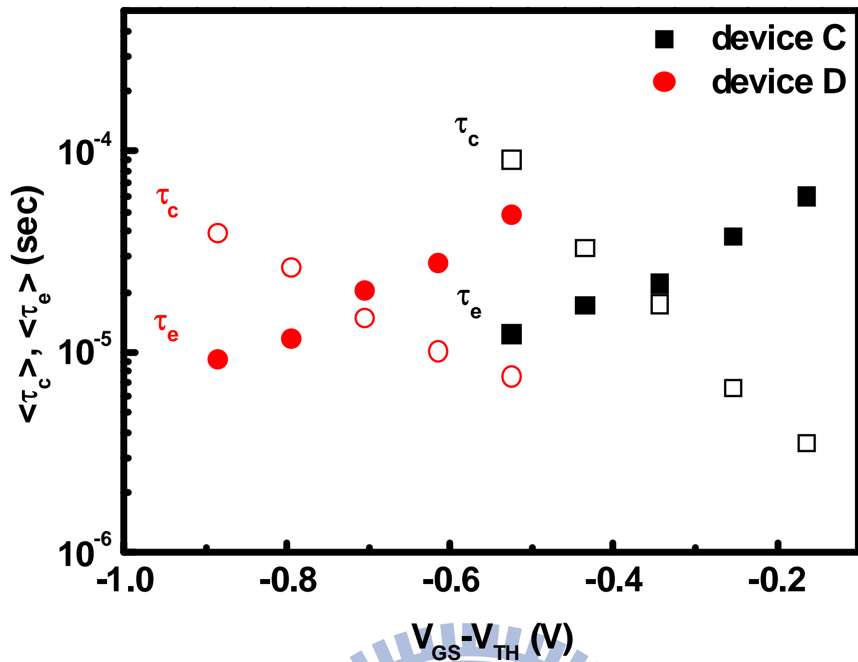


Fig. 7-11 $<\tau_c>$ and $<\tau_e>$ values of the device C and device D as a function of V_{GS}-V_{TH}.

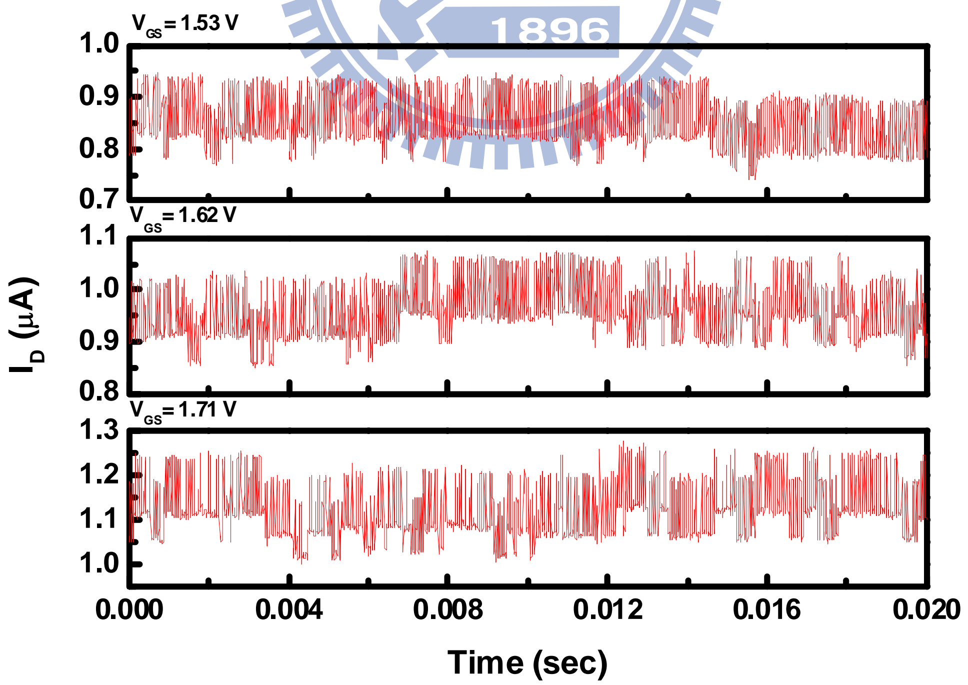


Fig. 7-12 Examples of the complex I_D waveform seen in the device E with different V_{GS} and a fixed V_{DS} of 1 V.

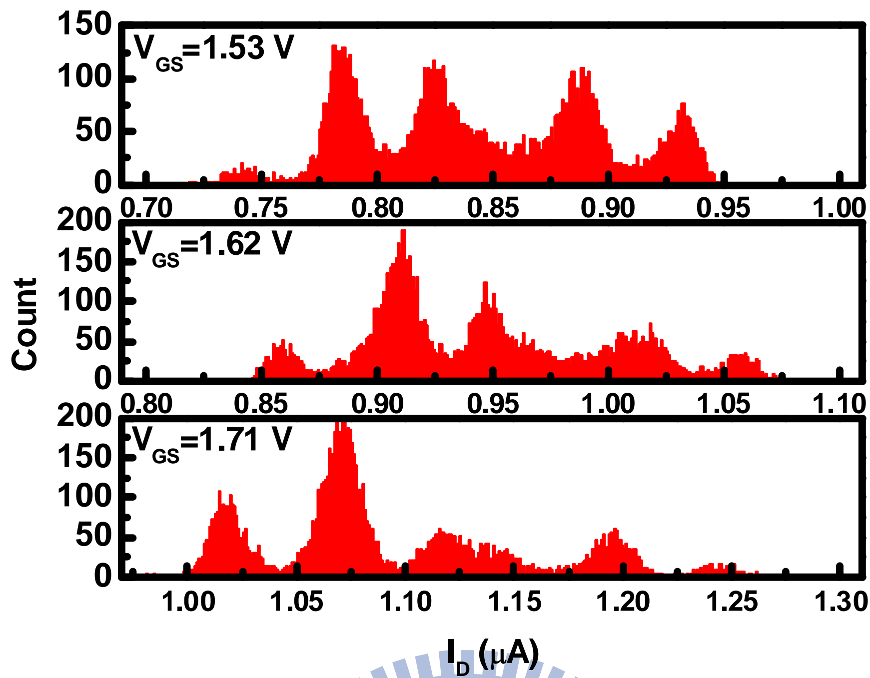


Fig. 7-13 Histograms of the time-domain data shown in Fig. 7-12.

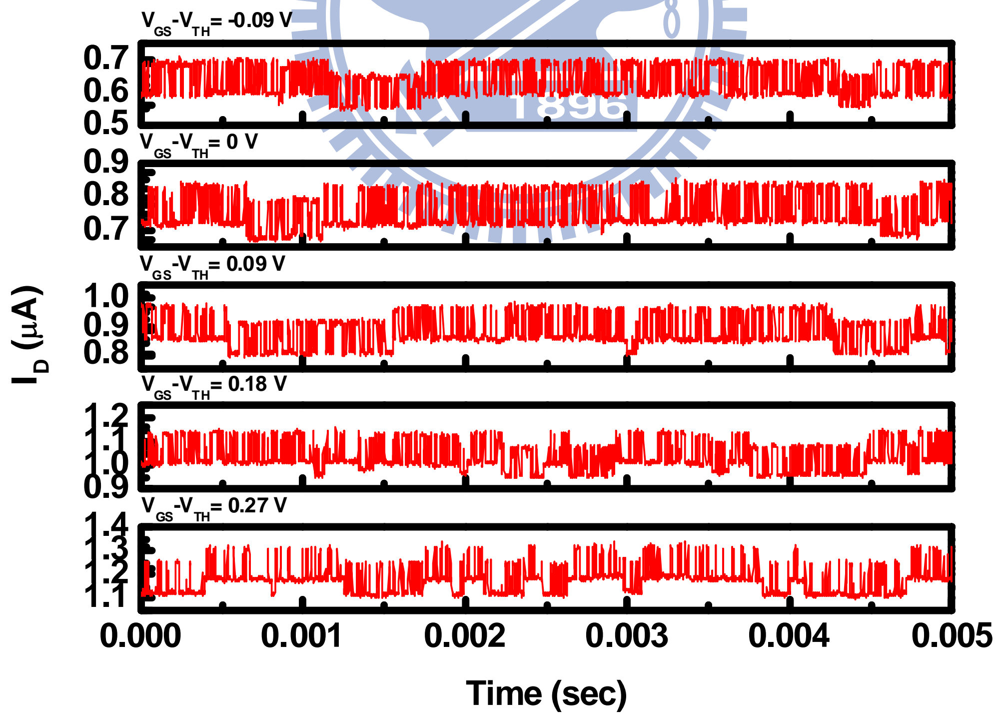


Fig. 7-14 I_D waveform of the device F with different V_{GS} and a fixed V_{DS} of 1 V.

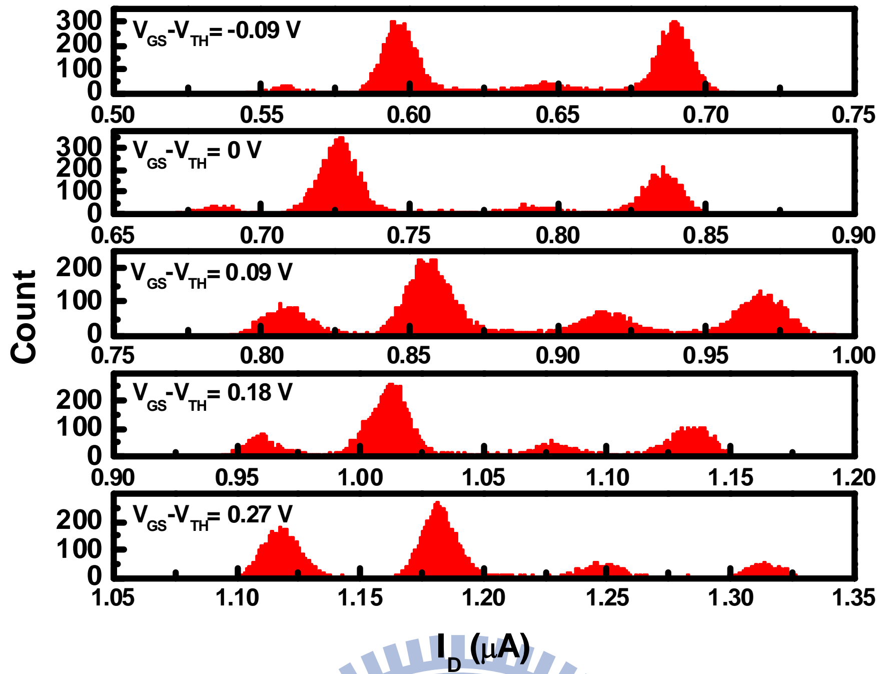


Fig. 7-15 Histograms of the time-domain data shown in Fig. 7-14.

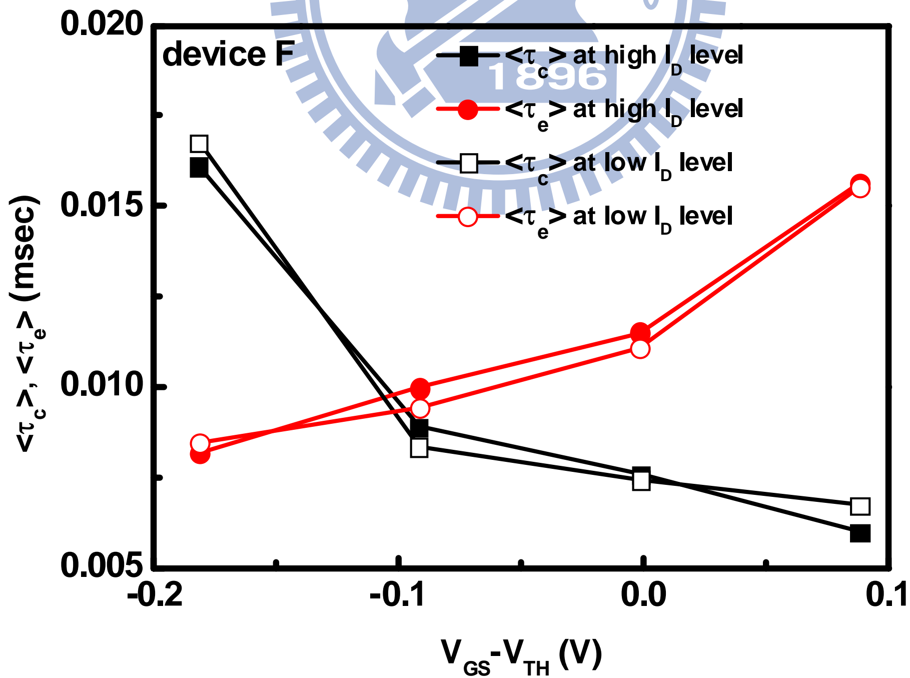


Fig. 7-16 $<\tau_c>$ and $<\tau_e>$ values of the faster trap of the device F as a function of V_{GS}-V_{TH} for the high I_D level and low I_D level, respectively.

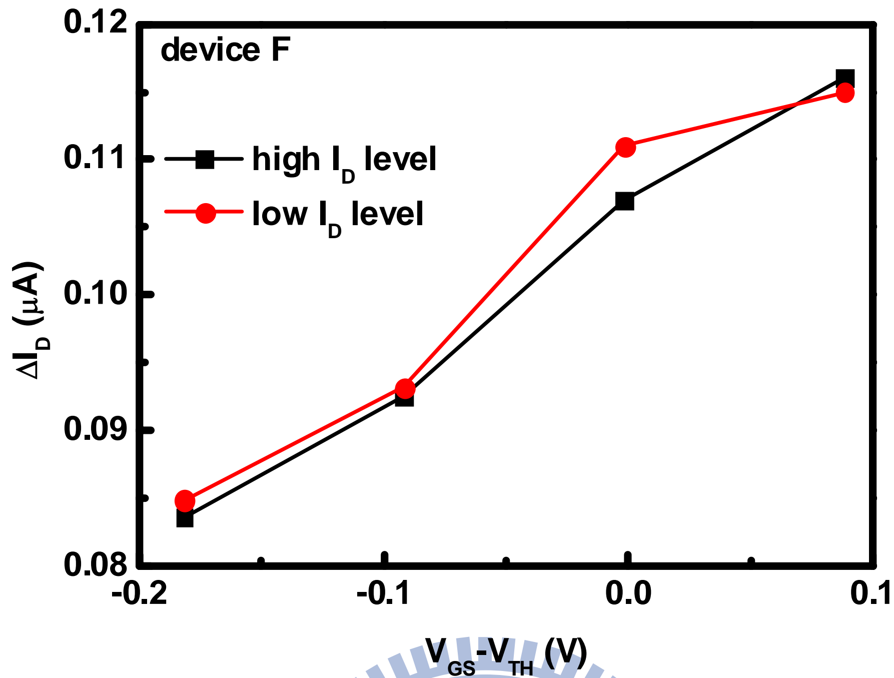


Fig. 7-17 ΔI_D values resulting from the faster trap as a function of V_{GS}-V_{TH} at the high I_D level and low I_D level.

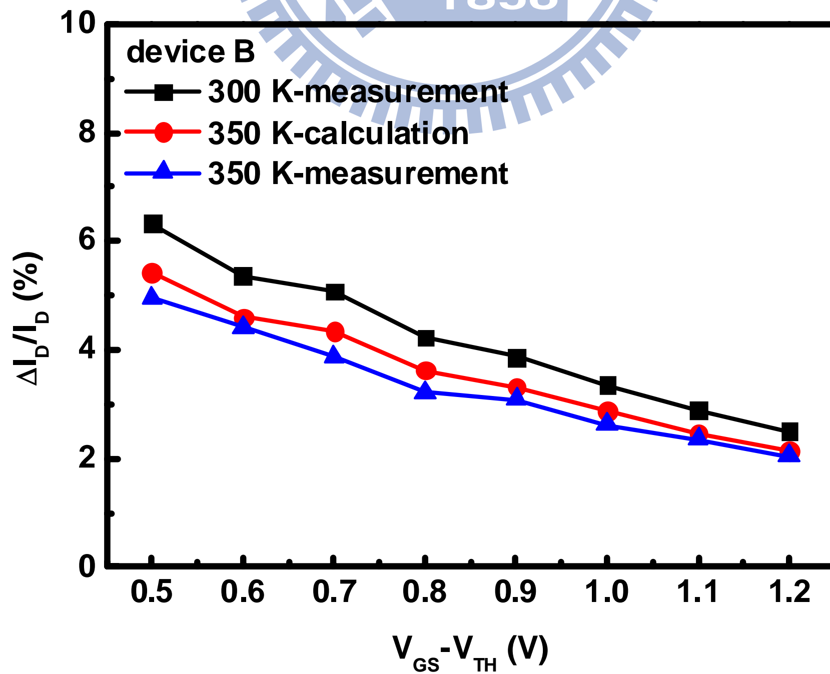


Fig. 7-18 $\Delta I_D/I_D$ values at 300 K and 350 K of the device B as a function of V_{GS}-V_{TH}.

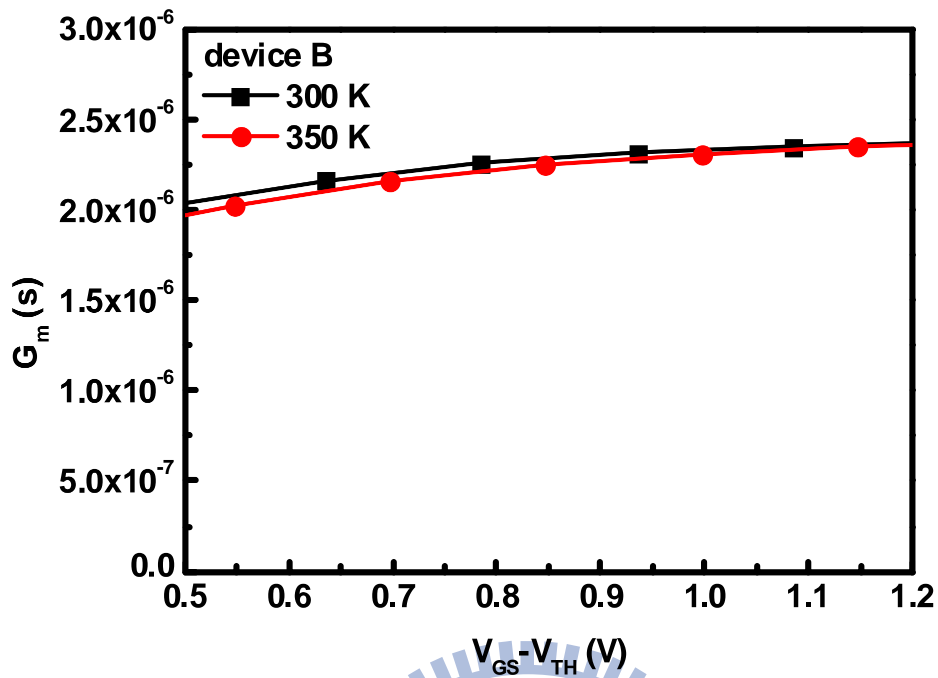


Fig. 7-19 V_{GS}-V_{TH} dependence of the G_m value of the device B at 300 K and 350 K.

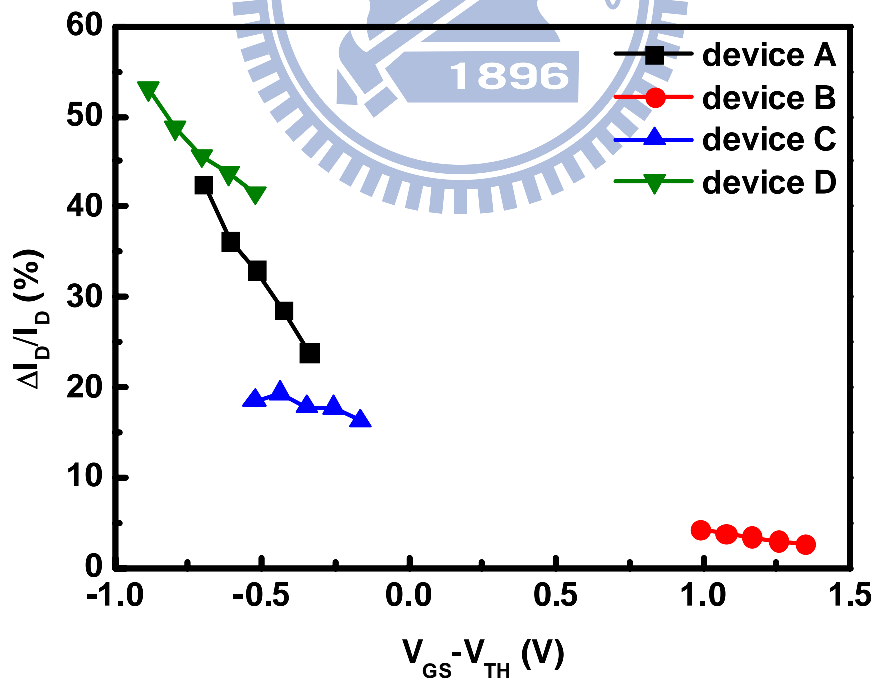


Fig. 7-20 Comparison of the $\Delta I_D/I_D$ values of some devices as a function of V_{GS}.

Chapter 8

Conclusions and Future Recommendations

8.1 Conclusions

In the first part of this dissertation, we study the impact of the C I/I process on the thermal stability of the NiSi film (chapter 2), the I-V characteristics of the Ni-silicide-contacted junctions (chapter 3), and the formation of the SiC film (chapter 4). Then, for applying poly-Si TFTs in 3D IC, their device characteristics and reliability issues are important and discussed in the second part. In chapter 5 and 6, high-performance poly-Si NW TFTs are demonstrated by structural engineering. Next, in chapter 7, the RTN phenomenon in small-area poly-Si NW TFTs is studied for the first time. The main results and conclusions are summarized as follows:

First, in chapter 2, the thermal stability of the NiSi film can be improved by the C I/I method. C atoms segregate to the NiSi grain boundary and NiSi/Si interface during silicide formation and then modify the grain-boundary and interfacial energies. Sufficient C atoms can effectively enhance the NiSi thermal stability in spite of thin Ni-silicide films (~20 nm) or the co-existence of As dopants. When the C I/I dose is equal to $5x10^{15}$ cm^{-2}, the agglomeration and phase transformation temperatures shown in Table 2-2 can be increased to 800 °C at least. Furthermore, the PIII technology is proposed to implant C ions into the Si substrate surface. During implantation, the DLC film is simultaneously deposited on the Si substrate surface. For the C3K1M samples, the formation of Ni silicide is prevented by the thick DLC film at low

temperatures (500-700 °C). For the C5K1M samples, although the Ni-silicide film is successfully formed at 500 °C, agglomeration and phase transformation simultaneously occur at a temperature as low as 700 °C. This result can be explained by insufficient C atoms at the NiSi grain boundary and NiSi/Si interface.

Then, in chapter 3, the SBH between NiSi and n-type Si could be modulated by the n-type doping effect of carbon. For the Ni-silicide-contacted n^+/p junctions, the magnitude of the junction leakage current is related to the thermal stability of the Ni-silicide film and the diffusion of Ni atoms. As the C I/I dose is equal to zero or $1x10^{15}$ cm^{-2}, due to the thermal degradation of the Ni-silicide film, the junction leakage currents increase with an increase in the silicide formation temperature. Although the thermal stability of the NiSi film can be improved with the C I/I dose of $5x10^{15}$ cm^{-2}, anomalously high junction leakage currents are attributed to the rapid diffusion of Ni atoms via extra defects. Hence, for the C I/I process, there exists a tradeoff relationship between enhancing the NiSi thermal stability and reducing junction leakage.

In chapter 4, the low-temperature C I/I technology followed by SPE annealing is used to form the SiC film. By optimizing the C I/I and SPE annealing conditions, the highest C_{sub} value of 1.046 % can be achieved. However, the presence of excess C atoms in Si results in retardation of the SPE rate, so incomplete recrystallization is observed. Another interesting phenomenon is that the P redistribution profile after SPE regrowth. We find that P atoms have sufficient time to diffuse out of the recrystallized region by the slowing down of the regrowth rate. Incomplete recrystallization and P redistribution both result in the high R_s values. After SiC formation, a high-thermal budget process should be avoided because the metastable SiC alloy will return to thermal equilibrium state.

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In chapter 5, we successfully fabricate high-performance GAA poly-Si NW TFTs with L_G= 30 nm. The GAA structure, the ultra-thin and narrow poly-Si body, and the MSB S/D are integrated together in poly-Si TFTs for the first time. High driving capability and good short-channel and narrow-width characteristics can be simultaneously achieved by structural engineering. The different current transport mechanisms between large-area and small-area poly-Si TFTs are characterized. The current transport mechanism of the GAA poly-Si NW TFT with L_G= 30 nm transforms from thermionic emission into the drift-diffusion model at V_{DS}= 1 V. By using NH_3 plasma treatment to passivate grain-boundary defects and interface states, the device characteristics can be further improved. These experimental results indicate poly-Si TFTs with the highly-scaled dimension are suitable for 3D IC applications.

In chapter 6, the HfO_2 gate dielectric is first introduced into poly-Si NW TFTs. Excellent low-voltage device characteristics can be demonstrated by EOT scaling. As the L_G/W is equal to 40 nm/20 nm, the normalized I_{ON} at V_{GS}-V_{TH}= 3 V and V_{DS}= 1 V is as high as 549 μA/μm. The SHE in our high-performance poly-Si TFTs is investigated. The SHE does not occur in large-area poly-Si TFTs due to the low driving capability. Two SHE phenomena can be observed in small-area poly-Si TFTs with the high driving capability, which is associated with the different current transport mechanisms. Thermionic emission and drift-diffusion currents are positively and negatively proportional to temperature, respectively. If the current transport is dominated by thermionic emission, the I_{ON} of the dc I-V measurement is higher than that of the pulsed I-V measurement. On the other hand, if the current transport is dominated by the drift-diffusion model, the I_{ON} of the dc I-V measurement is lower than that of the pulsed I-V measurement.

Finally, in chapter 7, the interesting phenomenon called RTN is observed in small-area poly-Si TFTs for the first time. The new carrier number fluctuation model, called the CNFGB model, is derived and used to distinguish between the grain-boundary and interface traps. By high-temperature measurements, we prove that the RTN phenomenon can also arise from the grain-boundary trap. Furthermore, the RTN signal caused by the gate oxide trap can also be detected. Very high $\Delta I_D/I_D$ values could be attributed to device scaling, multiple active traps, and/or surface potential fluctuations induced by grain-boundary traps. Therefore, if nano-scale poly-Si TFTs are actually applied to 3D IC or 3D stackable TFT Flash memories, the oxide, interface, and grain-boundary trap densities should be reduced by new advanced process technologies.

8.2 Future Works

There are several topics and suggesions worthy of note for future research and listed below:

1. For SiC formation, the C I/I process can be performed at lower implantation temperatures (for example, -100 °C). It prevents excess C atoms introduced by the I/I process. Therefore, two main problems, incomplete recrystallization and P redistribution phenomena after SPE annealing, could be resolved. High substitutional-to-total C ratio and low R_s could both be obtained in the recrystallized SiC region. The C I/I process results in increased junction leakage and dopant deactivation, which should be resolved by future research.
2. Once small-area poly-Si TFTs are applied in 3D IC, device variation will become a main issue and should be suppressed. Although our fabricated devices exhibit high performance, they also exhibit a serious device-to-device variation. In

addition to L_G variation, NW linewidth variation, and the variation of the lateral Ni-silicide growth rate commonly seen in single-crystalline MOSFETs, device-to-device variation in poly-Si TFTs also results from random grain boundary character distribution. Therefore, the recrystallization of poly-Si should be improved to control the grain size, grain orientation, and grain-boundary location.

3. Although the self-heating phenomenon of poly-Si TFTs related to the device size has been characterized, detailed thermal analysis is unknown and can be carried out using analytical modeling and numerical simulations. Heat transfer and temperature distribution in the poly-Si channel region can affect the device performance. Special thermal design considerations should be made.
4. Owing to the ultra-thin and narrow poly-Si body, surface roughness and high density of interface and oxide traps result in severe mobility degradation. Therefore, new process technologies should be developed to obtain smooth poly-Si/dielectric interface and better gate oxide quality. Moreover, the RTN phenomenon can also be eliminated by reducing the oxide, interface, grain-boundary trap densities.
5. Stress measurements can be performed on our short-channel poly-Si NW TFTs to study the reliability issues and discuss the degradation mechanism.
6. To further improve the device performance of our poly-Si NW TFTs, the strained Si technology commonly used on MOSFETs can be used. For example, poly-Si NW TFTs are measured under uniaxial mechanical stress induced by a three-point bending machine. Effects of bending stress on device characteristics and reliability issues can be investigated.

7. In order to observe significant quantum effects, our small-area GAA poly-Si NW TFTs can be cooled to the cryogenic temperature of liquid helium (4 K).

Publication List

Journal Paper:

1. B. Y. Tsui and **C. M. Lee**, "Thermal Stability of Nickel Silicide and Shallow Junction Electrical Characteristics with Carbon Ion Implantation," *Jpn. J. Appl. Phys.*, vol. 49, p. 04DA04, 2010.
2. **C. M. Lee** and B. Y. Tsui, "A High-Performance 30-nm Gate-All-Around Poly-Si Nanowire Thin-Film Transistor With NH_3 Plasma Treatment," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 683-685, 2010.
3. **C. M. Lee** and B. Y. Tsui, "High Performance Poly-Si Nanowire Thin-Film Transistors using the HfO_2 Gate Dielectric," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 327-329, 2011.

Conference Paper:

4. **C. M. Lee**, B. Y. Tsui, and G. L. Luo, "Improvement of Nickel Silicide Thermal Stability by Carbon Ion Implantation," in *15th Symposium on Nano Device Technology*, 2008.
5. **C. M. Lee** and B. Y. Tsui, "Impact of Carbon Ion Implantation on the Thermal Stability of Nickel Silicide and Shallow Junction," in *Ext. Abst. SSDM*, 2009, pp. 328-329.
6. **C. M. Lee** and B. Y. Tsui, "A 30 nm Gate-All-Around Poly-Si Nano Wire Thin-Film Transistor," in *Proc. VLSI-TSA*, 2010, pp. 28-29.
7. **C. M. Lee**, T. H. Lo, B. Y. Tsui, Y. C. Li, W. F. Tsai, and C. F. Ai, "Effect of carbon plasma immersion ion implantation on the thermal stability of nickel silicide film," in *18th International Conference on Ion Implantation Technology*, 2010.
8. **C. M. Lee**, C. F. Lien and B. Y. Tsui, "Achieving High-Performance Poly-Si TFTs by Structural Engineering," in *International Nanoelectronics Conference*, 2011.

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博士論文題目：

碳摻雜製程與高性能多晶矽奈米線薄膜電晶體之研究

A Study on Carbon Doping Technology and High-Performance Poly-Si Nanowire TFTs