國立交通大學

電子工程學系 電子研究所

博 士 論 文

快閃式記憶體和金氧半電晶體元件中單一電荷所導致的可靠性議題研究

Single Charge Phenomena in Scaled Memory and CMOS Devices

研 究 生：馬煥淇

指導教授：汪大暉 教授

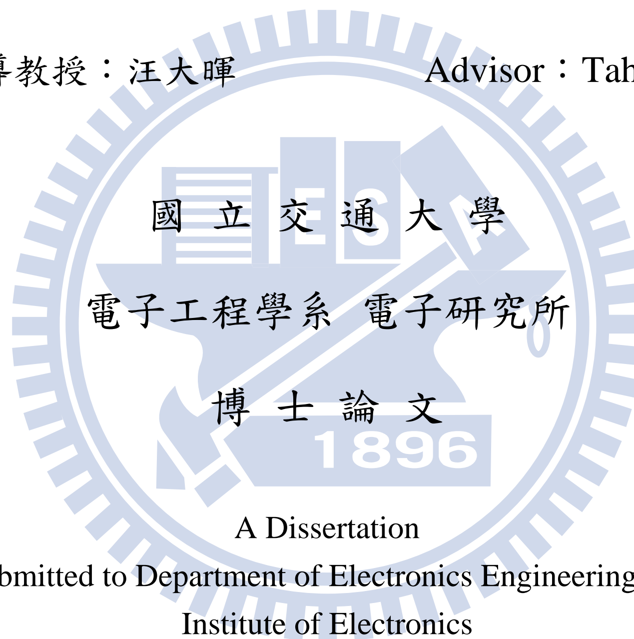
中 華 民 國 一 〇 〇 年 一 月

快閃式記憶體和金氧半電晶體元件中單一電荷所導致的可靠性議題研究

Single Charge Phenomenon in Scaled Memory and CMOS Devices

研 究 生：馬煥淇　　　　Student：Huan-Chi Ma

指導教授：汪大暉　　　　Advisor：Tahui Wang



國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

A Dissertation
Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering

January 2011
Hsinchu, Taiwan, Republic of China

中華民國一〇〇年一月

快閃式記憶體和金氧半電晶體元件中單一電荷
所導致的可靠性議題研究

學生：馬煥淇　　　　　　　　　指導教授：汪大暉 博士

國立交通大學　電子工程學系　電子研究所

摘　　要

本篇論文主要探討在以氮化矽(SiN)為電荷儲存之快閃式記憶元件以及高介電閘極材料(high-k)金氧半電晶體元件中，單一電荷引致的可靠性議題研究。隨著高介電閘極的採用，其元件在加壓後的電流不穩定狀態之研究的重要性也逐漸增加。另外，隨著元件不斷地微縮，數顆載子散逸流失以及隨機電報雜訊(RTN)對於通道電流會造成顯著的影響，而隨機電報雜訊對浮動閘極快閃式元件操作的影響近來已廣泛地被討論，但是，隨機電報雜訊對於氮化矽快閃記憶體操作的影響只有少數論文提及，因此，本論文前半段的研究著重於氮化矽快閃記憶體中的隨機電報雜訊，在氮化矽快閃記憶體元件中，吾人基於隨機電報雜訊開發新穎一種方法來分析注入電荷的分布，並且深入討論隨機電報雜訊於浮動閘極與氮化矽快閃記憶體元件操作的不同影響之原因，接著，討論氧化鉿量子點快閃記憶體電荷流失機制，而本論文後半段，提出雙極電荷散逸模型來解釋在高介電閘極電晶體施加電壓溫度後所引致的電流轉彎實驗現象。

第一章中，說明隨著元件不斷微縮，單一載子北補捉/釋放所造成的隨機電報雜訊及少數載子散逸流失現象對元件通道電流會造成顯著的影響，並且對於隨

機電報雜訊對於浮動閘極快閃記憶體操作之可靠性議題快速地回顧，另外，亦對量子點快閃記憶體材料作一精簡回顧。

第二章中，吾人研發一新穎方法來偵測小面積 SONOS 快閃記憶體沿著通道的表面電位變化，這個新方法是藉由結合缺陷位置萃取技術和底層二氧化矽缺陷所產生的隨機電報雜訊(Random Telegraph Noise)來達成。吾人使用這個新方法來驗證 SONOS 快閃記憶體中通道熱電子(Channel Hot Electron)的寫入電荷分佈和通道引發二次電子射入的電荷分佈之不同。此外，這個方法也被應用在觀察通道熱電子寫入和能帶到能帶穿隧產生之熱電洞(Band-to-Band Tunneling Hot Hole)抹除電荷分佈的不對稱現象。最後，亦利用此方法研究對於氮化矽記憶元件資料流失的機制，而我們藉由量測在寫入電子流失時電流的變化，推論出寫入電子是經由垂直方向經由底部氧化層穿遂流失。

在第三章中，我們研究了氮化矽快閃式記憶體(SONOS Flash Memory)中的寫入載子對隨機電報雜訊(Random Telegraph Noise)之振幅的影響。同時，我們對浮動閘極快閃式記憶體(Floating Gate Flash Memory)、氮化矽快閃式記憶體做了測量與模擬的工作。我們發現氮化矽記憶元件在資料寫入後隨機電報雜訊振幅分布與寫入前不同，而浮動閘極記憶元件在資料寫入前後有相同的隨機電報雜訊振幅。兩者的不同歸因於在氮化矽快閃記憶體中，隨機且分離的寫入載子造成的電流路徑滲透作用。

第四章探討高介電材料量子點快閃記憶體元件資料流失的機制。吾人分別在不同溫度下量測資料流失速度。相較於氮化矽快閃記憶體元件，高介電材料量子點快閃記憶體元件資料流失速度有強烈的溫度正相關性，無法以是適於氮化矽快閃記憶體的 Frenkel-Poole 激發理論解釋。吾人提出一種新的電荷流失機制：藉由熱激發穿隧機制，成功解釋其電荷流失的強烈溫度關係。

第五章中，研究高介電閘極(HfSiON) pMOSFETs 在施加負電壓溫度後所導致的不穩定現象，以單電子散逸量測技術針對施加負電壓大小、量測電壓大小及施加溫度作仔細的討論，在某特定條件下，加壓後電流將從退化變化為增益模式，吾人提出雙極電荷散逸模型來解釋負電壓溫度加壓所致之汲極電流的此轉彎(turn around)現象。其原因為在不同的施加電壓溫度及量測電壓下，加壓電流的電洞與電子成分不相同所致。

最後於第六章，吾人將對本論文做個總結。

關鍵字: 隨機電報雜訊，先進互補式金氧半電晶體，氮化矽快閃式記憶元件，浮動閘極快閃記憶體，負電壓溫度引致不穩定，高介電閘極氧化層，單電荷散逸，雙極電荷散逸模型，橫向電荷分佈，垂直電荷流失機制，橫向電荷流失機制，熱電子注入，熱電洞注入，滲透路徑，不均勻通道電位分佈

1896

Single Charge Phenomena in Scaled Memory and CMOS Devices

Student: Huan-Chi Ma   Advisor: Dr. Tahui Wang

Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

ABSTRACT

This thesis will focus on the reliability issues of single charge phenomenon in nonvolatile flash memory device and advanced gate dielectrics CMOS device. A novel technique based on random telegraph signal (RTS) is proposed to characterize the program/erase charge profile and retention in SONOS device. Besides, the different program charge effect between floating gate (FG) and SONOS flash device is investigated. Furthermore, staircase-like post- negative bias temperature (NBT) current instability is investigated by a computer-automated measurement circuit, which minimizes the switching delay between stress and measurement.

In Chapter 1, single electron induced current fluctuation in sub-micron FETs will be introduced. First, trapping and detrapping of individual oxide defects has been readily measured in CMOS device and nonvolatile memory. Second, the phenomena of drain current steps due to individual defects in NBTI relaxation

transients will be described. Also, the impact of single charge induced current variation will be pointed out. The application of nano-crystals in nonvolatile memory will be made a short introduction.

In Chapter 2, a new RTS-based method is proposed to characterize the lateral distribution of injected charge in program and erase states in a NOR-type SONOS flash memory. The concept of this method is to use RTS to extract an interface trap position in the channel and then to use the interface trap and RTS as internal probe to detect a local channel potential change resulting from injected charge during program/erase. The lateral width of the injected charge induced channel potential barrier is shown to be around 20nm in channel hot electron (CHE) program by this method. We also find that channel initiated secondary electron (CHISEL) program has a broader injected charge distribution than CHE program. A mismatch of CHE program electrons and band-to-band tunneling erase holes is observed. The polarity of a program-state charge distribution is examined along the channel within 10-20 program/erase cycles. Nitride charge retention loss is observed by using this method.

To expound the different program charge effect between FG flash and SONOS flash, in Chapter 3, RTN in planar SONOS cells and floating-gate cells in erase state and program state are measured, respectively. We find that a SONOS cell has a wide spread in RTN amplitudes after programming while a floating gate cell has identical RTN amplitudes in erase and program states at the same read current level. A 3D atomistic simulation is performed to calculate RTN amplitudes. Our result shows that the wide spread of program-state RTN amplitudes in a SONOS cell is attributed to a current-path percolation effect caused by random discrete nitride charges.

In Chapter 4, the charge retention loss mechanism in a hafnium oxide (HfO_2) dielectric dot flash memory is investigated. The temperature and time dependence of a charge loss induced gate leakage current in a large area cell are measured directly. We find that the charge loss is through a top oxide in the cell and the stored charge emission process exhibits an Arrhenius relationship with temperature, as opposed to linear temperature dependence in a SONOS flash memory. A thermally activated tunneling front model is proposed to account for the charge loss behavior in a HfO_2 dot flash memory.

In Chapter 5, bipolar charge detrapping induced current instability in HfSiON gate dielectric pMOSFETs after negative bias and temperature stress is studied by using a fast transient measurement technique. Both single electron and single hole emissions are observed, leading to post-stress current degradation and recovery, respectively. The NBT stress voltage and temperature effect on post-stress current evolution is explored. Clear evidence of electron and hole trapping in NBT stress is demonstrated. A bipolar charge trapping/detrapping model and charge detrapping paths based on measured charge emission times are proposed. Finally, conclusions are made in Chapter 6.

Keywords: Random Telegraph Signal, SONOS, Floating-gate Flash, NBTI, high-k dielectric, Single charge emission, Bipolar charge detrapping model, Lateral charge distribution, Lateral charge loss mechanism, Vertical charge loss mechanism, Hot electron programming, Percolation path, non-uniform channel potential

ACKNOWLEDGEMENT

First of all, I would like to express my deepest gratitude to my advisor Prof. Tahui Wang for his continuous guidance and encouragement. Without his teaching, I cannot complete my dissertation.

I also show my appreciation to all of my committee for their suggestions and comments.

During my study, many important persons have influenced me. Mr. S. H. Ku, Mr. C. T. Chan and J. W. Wu have taught me a lot of invaluable knowledge; special thanks are given to Mr. C. J. Tang and Mr. C. C. Cheng for sharing experience together. In particular, the assistance in measurement from Mr. C. H. Lee, Mr. Y. P. Chao, Mr. Y. L. Chou, Mr. J. P. Chiu, Mr. T. Y. Lin, Mr. Y. T. Chung and Mr. C. W. Lee are also greatly appreciated. I am also indebted to the Wang and Chung group members of Emerging Device and Technology Lab, who had made life fun.

Finally, I would present the deepest love to my parents. Their love is the most important power supporting me. This dissertation is dedicated to them.

謝誌

首先，這本博士論文的完成，必須感謝我的指導老師汪大暉教授。他有深厚的理論基礎，再加上細心與耐心的指導態度，使得我很容易從他的隻字片語中學習到新的知識及觀念。從討論中吸取汪老師的思考模式及獨到的見解，已成為我學習獨立思考的不二法門。

在論文的研究上必須感謝許多曾經指導過我的許多學長，及一起參與研究的同學及學弟。首先感謝古紹泓及詹前泰學長在我剛進研究生活的指導與鼓勵；感謝鄭志昌學長及唐俊榮同學在研究領域上的協助及討論。同時，我也感謝在李智雄學弟，趙元鵬學弟，周佑亮學弟，邱榮標學弟，林東陽學弟及鐘岳庭學弟在實驗執行上的幫助。此外，感謝許智維同學，李冠成學弟，薛至宸學弟，吳致融學弟，許家源學弟，林彥君學妹，李致維學弟以及前瞻元件與技術實驗室所有成員，他們為我的博士生涯增色許多。

最後，我要感謝我的父母、家人及女友小儀，在攻讀博士班期間給我的鼓勵與支持，有他們在背後無怨無悔的付出與關心，讓我毫無顧忌的專注於論文研究，使得這本博士論文得以順利完成。這本論文，獻給他們。

1896

Contents

Chinese Abstract		i
English Abstract		iv
Acknowledgement		iix
Contents		x
Figure Captions		xiii
Table Captions		xix
List of Symbols		xx
Chapter 1	**Introduction**	1
1.1	Background	1
1.2	Description of the Problem	2
1.3	Organization of the Dissertation	4
Chapter 2	**A Novel Random Telegraph Signal Method to Study Program/Erase Charge Lateral Spread and Retention Loss in a SONOS Flash Memory**	9
2.1	Preface	9
2.2	Device Description and Measurement Setup	12
2.3	Measurement Result and Discussion	12
	2.3.1 Extraction of an Interface Trap Position	12
	2.3.2 CHE Program Charge Lateral Profile	14
	2.3.3 CHE versus CHISEL programming	15
	2.3.4 CHE Program/BTBT Erase Charge Mismatch	15
	2.3.5 Program Charge Retention Loss	16
2.4	Summary	20

Chapter 3 Program Charge Effect on Random Telegraph Noise Amplitude in Floating Gate and SONOS Flash Memory 40

3.1 Preface 41

3.2 Device Description and Measurement Setup 41

3.3 Results and Discussions 41

3.3.1 Comparison of the Erase- and Program-state RTN in a FG and SONOS Cell 41

3.3.2 Statistics Results of Erase-state and Program-state in FG and SONOS devices 42

3.3.3 3D Atomistic Simulation of RTN 43

3.4 Summary 44

Chapter 4 Charge Retention Loss in a HfO_2 Dot Flash Memory via Thermally Assisted Tunneling 55

4.1 Preface 55

4.2 Device Description and Measurement Setup 56

4.3 Results and Discussions 56

4.3.1 Gate Leakage in HfO_2 dots memory and SONOS 56

4.3.2 Thermally Activated Tunneling Front Model 57

4.4 Summary 57

Chapter 5 Study of Post-NBT Stress Current Instability Modes in HfSiON Gate Dielectric pMOSFETs by Measurement of Individual Trapped Charge Emissions 64

5.1 Preface 64

5.2 Device Structure and Measurement Setup 65

5.3 Results and Discussions 65

5.3.1 Evidence of Holes and Electrons Detrapping in Post-NBT Stress Current 65
5.3.2 Stress V_g and temperature effect on Post-NBT Current Instability 66
5.3.3 Measurement V_g Dependence on Post-NBT Current Instability 67
5.3.4 Bipolar Charge Detrapping Model 68
5.4 Summary 68

Chapter 6 Conclusions 80

References 82
Vita 96
Publication List 97

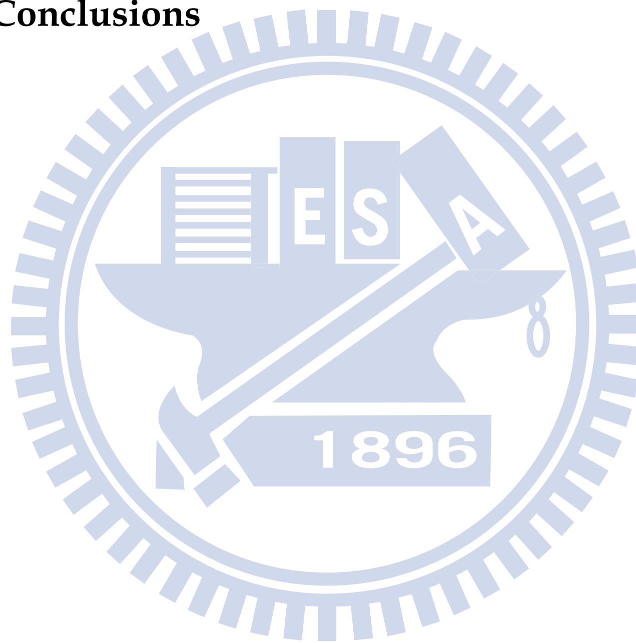


FIGURE CAPTIONS

Chapter 1

Fig. 1.1 A typical step-like "quantum jump" observed in channel current during NBTI recovery in a SiO_2 pMOSFET. 5

Fig. 1.2 A two-level RTS waveform resulting from electron emission and capture at oxide trap. τ_c and τ_e are electron emission time and capture time. ΔI_d is RTS amplitude. 6

Fig. 1.3 Estimation of threshold voltage shift as a function of process node [1.30] 7

Fig. 1.4 (a) Noise distributions of 90nm, 70nm, 50nm flash memory technologies [1.31] and (b) Measured V_{th} distribution of a 4-level MLC with level enlarged [1.30]. 8

Chapter 2

Fig. 2.1 Illustration of a two-level RTS waveform resulting from electron emission and capture at an interface trap. c and e are electron emission time and capture time. The trap position is x_t from the drain junction. The channel potential right below the trap is denoted by V_{ts}. 21

Fig. 2.2 Gate voltage dependence of average capture time in RTS at two drain voltages, V_{ds}=0.05V and 0.3V. The lateral shift of these two curves corresponds to ΔV_{ts}. 22

Fig. 2.3 Cumulative trap position distribution along the channel. L=0.1μm is the channel length and x_t is the distance of a trap from the drain. 23

Fig. 2.4 RTS patterns at three program ΔV_t=0.3V, 0.9V and 1.2V in a CHE program cell. The RTS measurement condition is V_{gs}=3.5V and V_{ds}=0.05V. x_t =0.2L. 24

Fig. 2.5 Average capture time (τ_c) and emission time (τ_e) versus program ΔV_t in an x_t =0.2L cell. 25

Fig. 2.6 Ratio $\langle\tau_c\rangle/\langle\tau_e\rangle$ and a local surface potential change ($\Delta\varphi_s$) at the trap position (x_t =0.2L) versus program ΔV_t. The local potential change is calculated from Eq. (2). 26

Fig. 2.7 Evolutions of $\langle\tau_c\rangle/\langle\tau_e\rangle$ with program ΔV_t at four different trap positions x_t=0.03L, 0.05L, 0.2L and 0.3L. 27

Fig. 2.8 Channel potential energy distribution extracted from RTS. The CHE program window is ΔV_t=0.6V. The width of the potential energy barrier is about 20nm. 28

Fig. 2.9 Comparison of $\langle\tau_c\rangle/\langle\tau_e\rangle$ evolutions with program ΔV_t in CHE and CHISEL program. A substrate bias of -2V is applied in CHISEL program. 29

Fig. 2.10 $\langle\tau_c\rangle/\langle\tau_e\rangle$ versus program ΔV_t during CHE program and BTBT hot hole erase. The device has a trap at 0.05L from the drain. The inset shows the $\langle\tau_c\rangle/\langle\tau_e\rangle$ in a log scale. 30

Fig. 2.11 $\langle\tau_c\rangle/\langle\tau_e\rangle$ versus program ΔV_t during CHE program and BTBT hot hole erase. The device has a trap at 0.3L from the drain. 31

Fig. 2.12 Illustration of program/erase charge distributions in the channel. The stars represent interface traps. The program electrons at x_t=0.05L are completely compensated, but some far electron at x_t=0.3L are not compensated by erase holes. 32

Fig. 2.13 $\langle\tau_c\rangle/\langle\tau_e\rangle$ in a program-only cell versus bake time. The x_t is 0.03L. The bake temperature is 120℃. The program ΔV_t is 1V. 33

Fig. 2.14 Program-state and erase-state $\langle\tau_c\rangle/\langle\tau_e\rangle$ at different P/E cycles. The x_t is 0.05L. The $\langle\tau_c\rangle/\langle\tau_e\rangle$ in fresh state is also shown in the figure. The program ΔV_t is 1V. 34

Fig. 2.15 Program-state $\langle\tau_c\rangle/\langle\tau_e\rangle$ is plotted against gate stress time. The program ΔV_t is 1V. The gate stress voltage is Vg=-5V. The trap position x_t is 0.05L. RTS waveforms immediately after program and after 4-second gate stress are shown in the inset of the figure. 35

Fig. 2.16 (a) Read current variation with cumulative gate stress time in program state. The P/E cycle number is 33. (b) Experimental setup for read current measurement. The measurement consists of two alternating phases, a gate stress phase and a read phase. In gate stress, a negative gate voltage (-3.5V) is applied to accelerate nitride charge loss. The sampling rate is 10kHz. The program ΔV_t is 2V. 36

Fig. 2.17 Step-like drain current during retention time in a SONOS NAND cell with uniform FN program/erase. 38

Chapter 3

Fig. 3.1 An illustration of random potential induced percolation effect (fromRTN [3.7]) in FG cell. 45

Fig. 3.2 RTN amplitude versus drain current in a FG flash cell in three P/E cycles. The V_t window is 1V. The drain voltage in measurement is 0.7V and the gate voltage is varied. 46

Fig. 3.3 RTN amplitude versus drain current in a SONOS cell in three P/E cycles. The V_t window is 1V. The drain voltage in measurement is 0.7V and the gate voltage is varied. 47

Fig. 3.4 Measured RTN waveform and I_d versus V_g plot (a) in erase-state and (b) in program-state of a SONOS cell. Electron trapping at an interface trap is manifested by a current discontinuity in the I_d-V_g plot 48

Fig. 3.5 An illustration of two different program charge storage characteristic resulting distinct outcome of percolation path. Continuous distribution in FG flash and random discrete distribution in SONOS flash. 49

Fig. 3.6 Measured program-state RTN amplitude versus erase-state RTN amplitude in 40 FG flash cells. The RTN amplitude is measured at I_d=500nA @V_d=0.7V. The device dimension is W/L=0.11μm/0.09μm. The program window is 1V or 2V. 50

Fig. 3.7 Measured program-state RTN amplitude versus erase-state RTN amplitude in 45 planar SONOS cells. The RTN amplitude is measured at I_d=500nA @V_d=0.7V. The SONOS cells have W/L=0.09μm /0.08μm, a 2.8nm tunnel oxide, a 6nm SiN and a 6nm top oxide. 51

Fig. 3.8 Simulation flowchart of 3D atomistic simulation for RTN amplitude at program state and erase state for FG and SONOS flash. 52

Fig. 3.9 Simulated RTN amplitude versus drain current in a FG flash cell. Program-state and erase-state have the same placement of substrate random dopants. The RTN trap is placed in the middle of the device. 53

Fig. 3.10 Simulated RTN amplitude versus drain current in a planar SONOS cell. Program-state and erase-state have a fixed placement of substrate dopants. Ten different sets of random program charges are simulated. An RTN amplitude due to number fluctuation is calculated with continuous substrate doping and program charges. 54

Chapter 4

Fig. 4.1 Measured gate leakage current at V_g=0V versus time in a HfO_2 dot flash memory cell (500μm×500μm). The temperature is from 25℃ to 125℃. The device is programmed to a threshold window of 3V. 60

Fig. 4.2 Comparison of temperature dependence of a gate leakage current in a HfO_2 dot flash and in a SONOS flash at t=3s. 61

Fig. 4.3 Arrhenius plot of the gate leakage current in a HfO2 dot flash memory. The retention time is 0.5s and 5s. The extracted activation energy is 0.19eV. 62

Fig. 4.4 (a) Illustration of charge loss through a top oxide trap in a HfO_2 dot flash. (b) Energy band diagram and thermally assisted tunneling of a trapped charge. 63

Chapter 5

Fig. 5.1 Voltage waveforms applied to the gate and the drain during NBT stress and measurement (relaxation) phases. A high-speed electronic switch is used to minimize a delay between stress and measurement. 69

Fig. 5.2 Post-stress current evolution with measurement (relaxation) time in (a) a small area device (W/L=0.18/0.08μm) and (b) a large area device (W/L=10/0.32μm). The NBT stress voltage is -3.0V. The measurement voltages are V_g/V_d=-1.2V/-0.2V and temperature is 25°C. The pre-stress current is shown in (a) for comparison. Both current degradation and recovery are obtained in the measurement period. 70

Fig. 5.3 Linear drain current change versus NBT stress time. ΔI_d is measured immediately after stress. Three stress voltages, V_g =-2.8V, -2.6V and -2.0V are applied. Electron trapping into pre-existing high-k traps is demonstrated by a positive ΔI_d at a high stress $|V_g|$. 71

Fig. 5.4 Drain current evolution after a low V_g (=-2V) stress in (a) a small area device and (b) a large area device. Only hole detrapping are found at a low stress V_g. The measurement voltages are V_g/V_d=-1.2V/-0.2V and temperature is 25°C. 72

Fig. 5.5 Illustration of a band diagram and carrier flows in a high-k pMOSFET under $-V_g$ stressing. In a charge separation measurement, the electron stress current (I_e) flows from the substrate to the gate and the hole stress current (I_h) flows from the source/drain to the gate. 73

Fig. 5.6 Stress voltage dependence of electron injection current (I_e) and hole injection current (I_h). A charge separation technique is used to measure I_e and I_h. (a) T= 25°C and (b) T= 100°C. 74

Fig. 5.7 Post-stress current evolutions with measurement time for two different stress temperatures, T= 25°C and 80°C. The stress voltage is -2.2V. The turn-around characteristic is observed only at T= 80°C. Note that the Id measurement is biased in subthreshold region that Id is larger at a higher temperature. 75

Fig. 5.8 Typical post-stress current evolution patterns. (a) measurement V_g=-0.85V and (b) V_g=-1.0V. The longest electron detrapping time (τ_e) and the shortest hole detrapping time (τ_h) are indicated. The trend is that both τ_e and τ_h increase with measurement $|V_g|$. 76

Fig. 5.9 Average τ_e and τ_h are plotted against measurement V_g. We repeated measurement of each data point ten times by charge re-filling to take an average. Only the longest electron detrapping time and the shortest hole detrapping time (as shown in Fig. 8) are plotted in the figure. 77

Fig. 5.10 Illustration of the energy band diagram in relaxation phase. (a) Trapped electron emission to the gate, and (b) trapped hole emission to the substrate. 78

Fig. 5.11 Arrhenius plot of the τ_e and τ_h versus temperature (a) trapped electrons and (b) trapped holes. The extracted activation energy is 0.2eV for electrons and 0.14eV for holes. 79

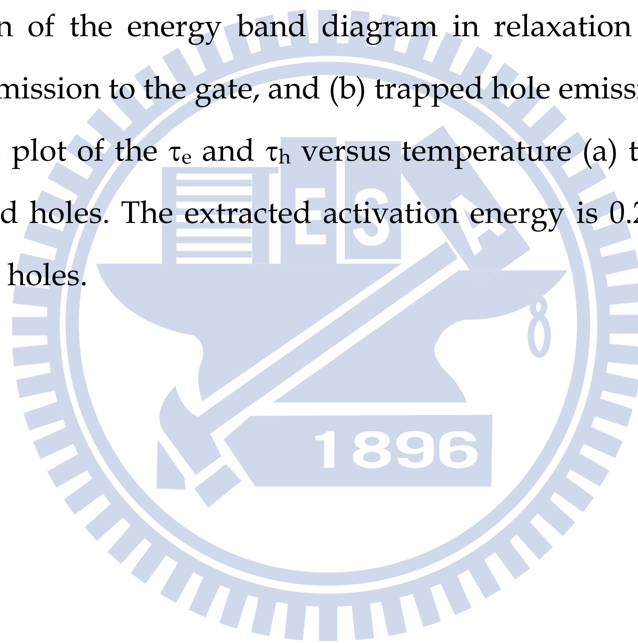
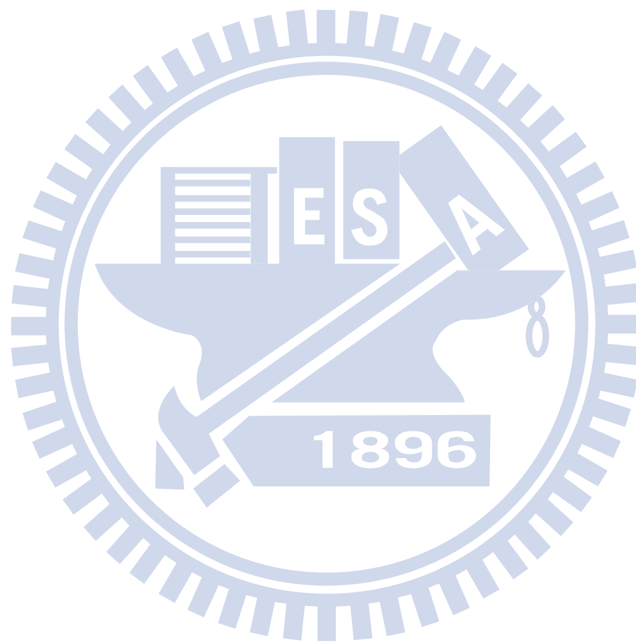


Table Captions

Table 2.1 Dependence of program-state V_t retention loss on retention time, P/E cycles, gate stress polarity and temperature from the vertical charge loss model (in a FP emission limited condition) and from experimental results. 39



LIST OF SYMBOLS

E_a	Activation energy
E_T	Trap energy
E_F	Fermi level
F	Electrical field in nitride
I_e	Electron stress current
I_h	Hole stress current
I_d	Drain current
L	Channel length
m_e	Electron effective mass in SiO_2
N	P/E cycle number
N_{ox}	Oxide trap density
N_t	Trap density in top oxide
n_e	Electron concentration in the channel right below the trap
n_t	Trapped charge density in silicon nitride
Q_s	Stored charge in the HfO_2 dot
Q_{ox}	Negative trapped charge in the bottom oxide
T	Absolute temperature
t	Measurement time
t_{ox}	The oxide thickness
V_t	Threshold voltage
V_g, V_d, V_s	Gate, drain, and source voltage
V_{ts}	Channel potential at the trap position
W	Channel width
x	Distance between a HfO_2 trap and a top oxide trap

x_t — Distance of the trap from drain edge

α_{ox} — Coefficient of tunneling probability through SiO_2

ΔI_d — RTN amplitude

ΔV_t — Program window

$\Delta \varphi_s$ — Local potential change at the trap position

ε_{ox} — Dielectric constant of SiO_2

ϕ_b — Barrier height between the SiO_2 and Si_3N_4 for electrons

σ — RTN amplitude distribution standard deviation

σ_t — Trap cross section

τ_e, τ_c — Electron emission time and capture time

$\tau_e(FP)$, $\tau_c(FP)$ — Frenkel-Poole emission time and capture times

τ_{eff} — Effective time for nitride trapped charge at the emission front to escape from the ONO film

τ_{ox} — Oxide tunneling time

υ_{th} — Thermal velocity

$<\tau_c>,<\tau_e>$ — Average time of the capture time and emission tim

Chapter 1

Introduction

1.1 Backgrounds

In order to maintain the scaling roadmap, high permittivity (high-k) material is introduced to replace SiO_2 to solve the gate leakage problem. Bias temperature stress induced current instability in SiO_2 and high-k based gate dielectric CMOS was reported to be mainly issue on DC performance [1.1]-[1.8]. With the shrinkage of device dimension to atomic levels, variation between devices occurred due to the effects such as random dopant fluctuation [1.9]-[1.15]. Similarly, the effect of a single charge induced current fluctuation on a typical device can be quite significant.. In ultra small area device, the trapping of even a single carrier will potentially cause functional errors in digital logic circuits and memories. The effect of few carriers trapping has also become a major reliability issue in bulk MOSFETs. MOSFET degradation associated to trapping of carriers in stress-generated defects in the gate dielectric has become a matter of growing concern [1.16]-[1-21]. Fig. 1.1 illustrates multiple carriers were detrapping in negative bias stressed device [1-22]

Flash memory is a non-volatile computer data storage technology that can be electrically programmed, erased and read for many times and won't be lost after cutting off the power. It is primarily used in memory cards, USB flash drives, and solid-state drives for general storage and transfer of data between computers and other digital products. With respect to charge storage devices, two state-of-art techniques attract great attention. (a) Floating gate (FG) devices: charge is stored in a thin conducting or semiconductor layer. (b) Charge trapping devices: Charge is stored in the traps at the interface and bulk of insulator, such as SONOS

device [1.23]. With the advanced VLSI processing, the effect of a single electron on a typical device can be quite significant. Such effects will eventually cause fundamental scaling and reliability problems. Random telegraph noise (RTN) phenomenon arising from electron emission and capture at an interface trap site [1.24]-[1.27] has been recognized as a new scaling concern in flash memory [1-28]-[1-33]. Typical two-level RTN pattern is shown in Fig. 1.2. Vt fluctuations originated from a large-amplitude RTN tail will cause a read error and become a prominent issue in designing a multilevel-cell (MLC) flash memory in 45nm technology node and beyond as shown in Fig. 1.3[1-30]. Fig. 1.4(a) shows that the worst case of RTN induced Vt shift is over 0.3V in 50 nanometer technology node [1-31]. Fig. 1.4(b) tells us that such large RTN tail may cause a read error in multilevel-cell flash memory application and requires the use of error code correction.

Another category of discrete charge storage flash memories are to use nano-crystals as storage nodes. Many different types of nano-crystals from semiconductors (Si, Ge) to metals (W, Au) have been proposed [1-34], [1-35]. Recently, a HfO_2 dielectric dot flash memory with hot electron program/hot hole erase was presented with superior characteristics in terms of a large memory window, fast P/E speed, and long charge retention time [1-36]. As compared to semiconductor/metal dots, electrons in a dielectric dot are stored in trap states rather than conduction states. Because trapped electrons have a very sharp wave-function distribution in space, size quantization effect is not expected for the programmed electrons in a dielectric dot.

1.2 Description of the Problem

Negative bias temperature instability (NBTI) has been recognized as a major

reliability concern in ultra-thin dielectric pMOSFETs. Compared to SiO2 gate dielectric, the NBTI in high-k has been less explored. We employ the fast transient measurement technique to reduce the post-stress transient effect due to charge trapping/detrapping in high-k dielectric.

Two-bits/cell NOR-type SONOS flash memory has been realized by storing bit charges in two sides of a channel by channel hot electron (CHE) program and band-to-band tunneling (BTBT) hot hole erase. The control of program/erase charge lateral distributions of each bit is a major thrust to improve cell performance and scalability. Many attempts have been made in the past to characterize a trapped charge lateral profile in a SONOS cell. Two lateral profiling techniques were often used, a charge pumping (CP) method and an inverse I-V modeling approach. The CP current is too small to be measured. The inverse I-V modeling requires the knowledge of a two-dimensional device doping profile and does not yield a unique solution. The technique to characterize the charge profile, which is suitable for a small area cell and does not need a 2D numerical device simulation, is needed. Since RTN is very sensitive to a local potential change near the trap, it can be used as internal probe to detect a variation in a trapped charge density during program, erase and retention.

In recent years, RTN issues in FG flash device are intensively studied. Less works were done on RTN issues in charge trapping memory, i.e. SONOS. Especially, the difference dependence on program charge between FG and SONOS has never shown in the report until. The program charge effects on RTN amplitudes in floating gate flash and SONOS flash were investigated in detail.

1.3 Organization of the Dissertation

The scope of this thesis mainly focuses on reliability concerns of NBTI in high-k gate dielectric and RTN in nitride-based storage memory, which are schematically illustrated in Fig. 1.4. Following the introduction, the characterization of post-NBTI current instability in HfSiON gate dielectric pMOSFETs is demonstrated in Chapter 2. Bipolar charge detrapping model is proposed and successfully applied to explain the experimental result. Described in Chapter 3 is a novel RTN-based technique for direct characterization of program/erase charge lateral distribution and retention mechanism in silicon nitride. In the chapter 4, we will investigate program charge effects on RTN amplitudes in floating gate flash and SONOS flash. The RTN measurement is performed in planar SONOS cells and floating-gate cells in erase state and program state, respectively. A SONOS cell has a wide spread in RTN amplitudes after programming while a floating gate cell has identical RTN amplitudes in erase and program states at the same read current level. Our result shows that the wide spread of program-state RTN amplitudes in a SONOS cell is attributed to a current-path percolation effect caused by random discrete nitride charges. In Chapter 5, the charge loss mechanism in a hafnium oxide (HfO_2) dielectric dot flash memory is investigated. The temperature and time dependence of a charge loss induced gate leakage current in a large area cell are discussed. A thermally activated tunneling front model is proposed to account for the charge loss behavior in a HfO_2 dot flash memory. Finally, conclusions are drawn in Chapter 6.

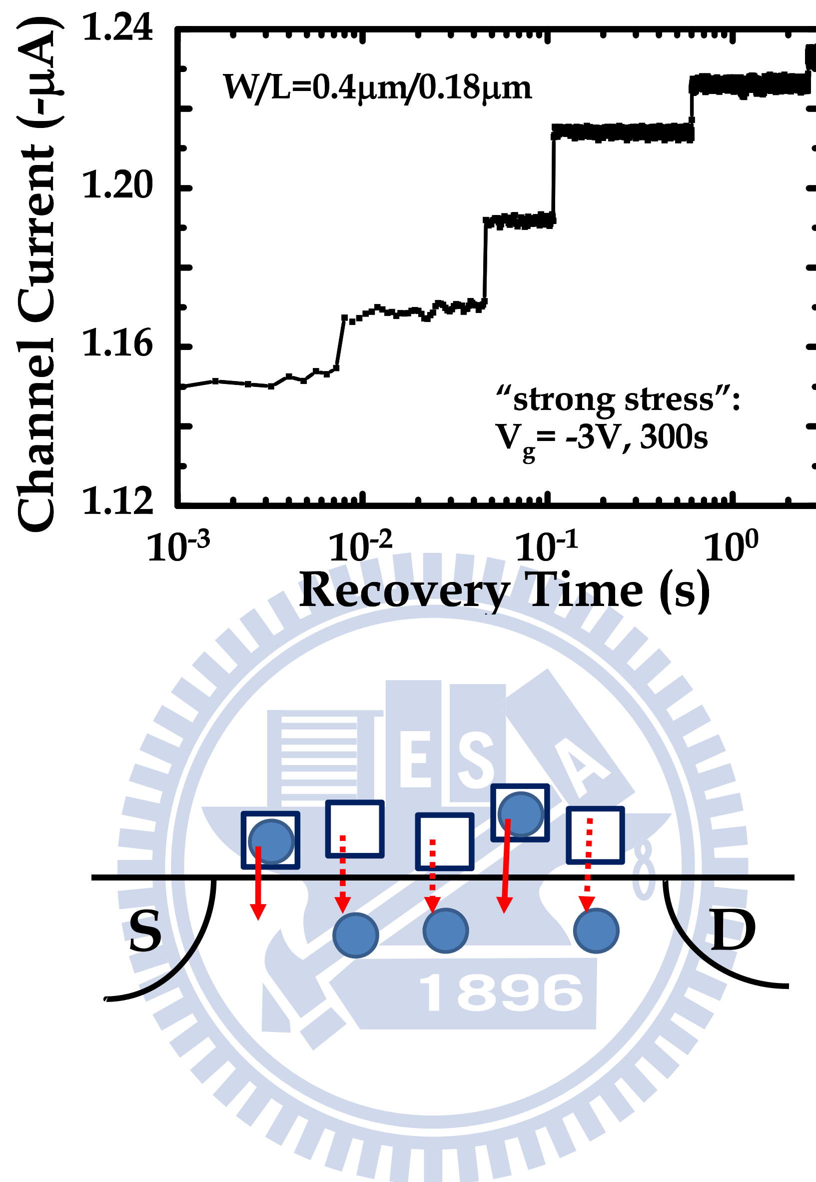


Fig. 1.1 A typical step-like "quantum jump" observed in channel current during NBTI recovery in a SiO_2 pMOSFET.

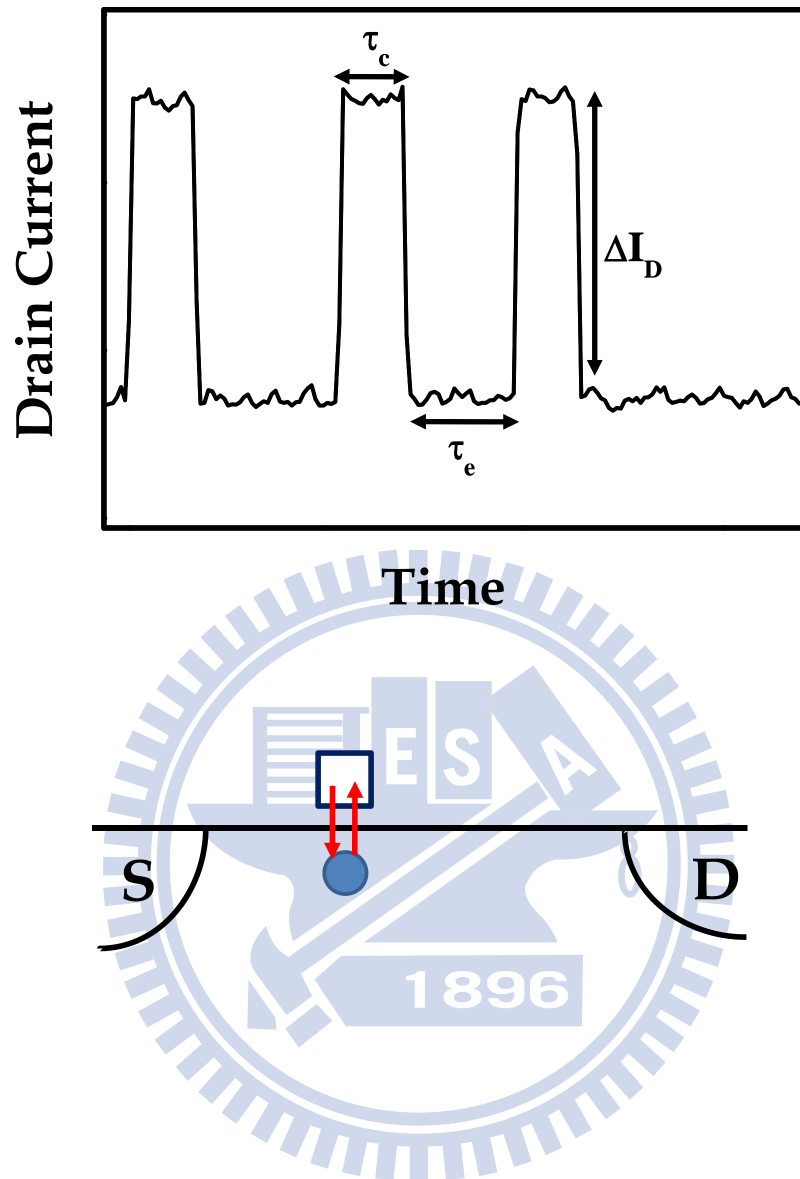


Fig. 1.2 A two-level RTS waveform resulting from electron emission and capture at oxide trap. τ_c and τ_e are electron emission time and capture time. ΔI_d is RTS amplitude.

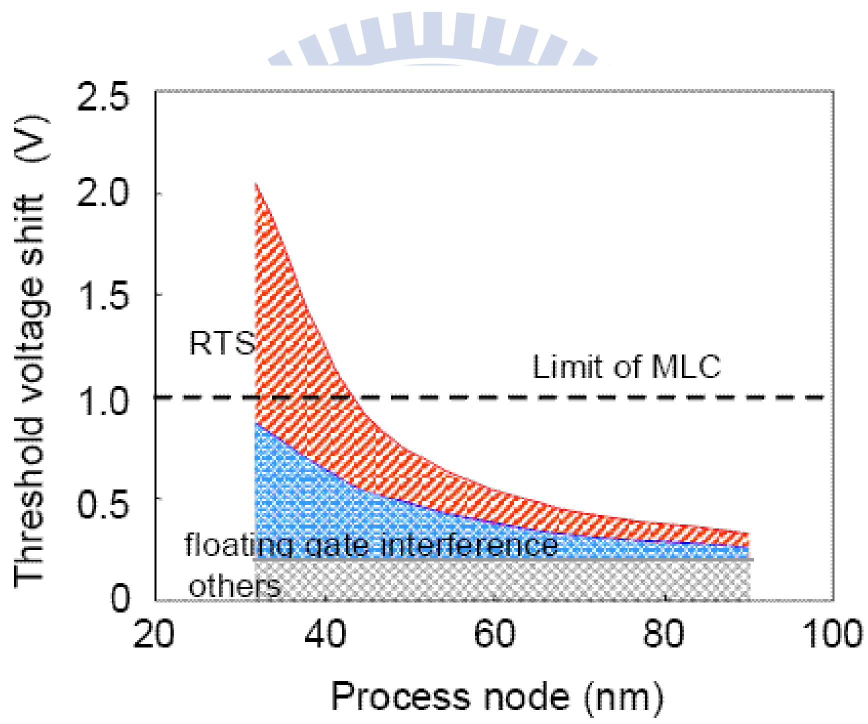


Fig. 1.3 Estimation of threshold voltage shift as a function of process node [1.30]

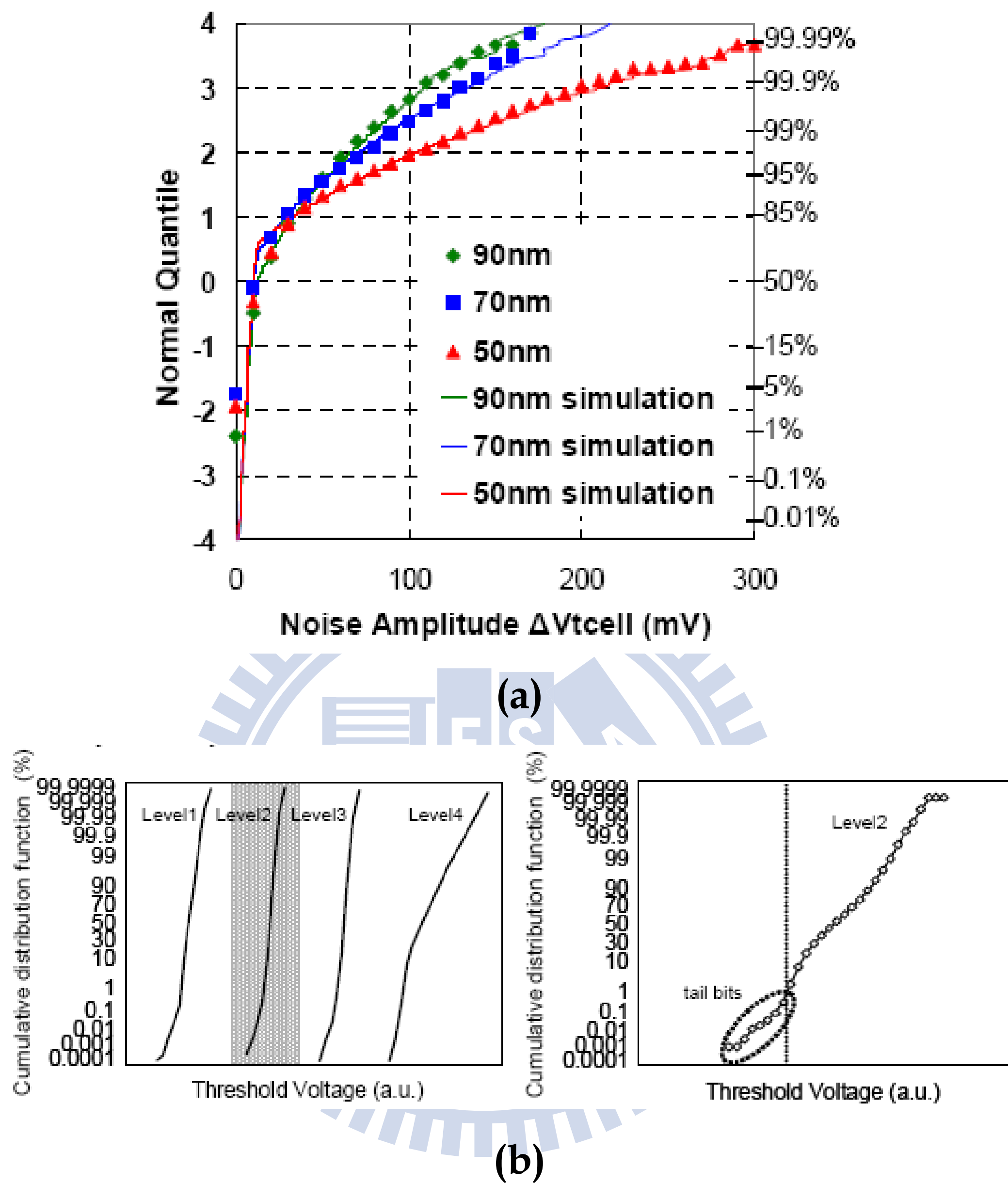


Fig. 1.4 (a)Noise distributions of 90nm, 70nm, 50nm flash memory technologies [1.31] and (b)Measured V_{th} distribution of a 4-level MLC with level enlarged [1.30].

Chapter 2

A Novel Random Telegraph Signal Method to Study Program/Erase Charge Lateral Spread and Retention Loss in a SONOS Flash Memory

2.1 Preface

Nitride-based trapping storage flash memory has received much attention recently because of its immunity from stress-induced leakage current and the coupling of floating gates in conventional flash memory [2.1]. Two-bits/cell NOR-type SONOS flash memory has been realized by storing bit charges in two sides of a channel by channel hot electron (CHE) program and band-to-band tunneling (BTBT) hot hole erase [2.2]. The control of program/erase charge lateral distributions of each bit is a major thrust to improve cell performance and scalability [2.3]. Many attempts have been made in the past to characterize a trapped charge lateral profile in a SONOS cell [2.4]-[2.9]. Two lateral profiling techniques were often used, a charge pumping (CP) method [2.7] and an inverse I-V modeling approach [2.4]. The CP method provides a direct measurement result, but has the following drawbacks. First, the profiling method is based on an assumption that interface traps have a uniform distribution along the channel [2.10]. This assumption is not true in certain device process conditions, for example, pocket implanted cells in a buried diffusion bit-line array, where interface traps are distributed near the source/drain junctions of a cell. Second, a charge pumping current is hardly sensed in a small area

SONOS cell due to a few interface traps in a cell. Third, the CP profiling technique is applicable only when a charge density increases monotonically along the channel [2.6]. For a two-pole charge profile in erase state, the CP method is not appropriate. On the other side, the inverse I-V modeling is an indirect method. A charge lateral distribution is extracted from a two-dimensional device simulation by fitting simulated subthreshold and GIDL characteristics to measurement results. The inverse I-V modeling also suffers from some limitations. First, it requires the knowledge of a two-dimensional device doping profile in device simulation. A specific shape of a program/erase charge distribution is usually given in priori in simulation, for example, a rectangular charge packet or a Gaussian-like charge distribution [2.4]-[2.5]. Second, the method does not yield a unique solution. The simulated width of a program-state charge distribution varies considerably in literature, from 20-40nm in [2.4]-[2.6] to 85nm in [2.11]. In this work, we will propose a new charge profiling technique based on random telegraph signal. This technique is very sensitive to injected electrons or holes in program/erase operation and charge loss during retention. Moreover, this technique is suitable for a small area cell and does not need a 2D numerical device simulation.

Random telegraph signal in the channel current of a SONOS cell arises from electron emission and capture at a SiO_2/Si interface trap. Recently, it has been recognized as a major scaling concern in flash memories [2.12] since Vt fluctuations originated from a large amplitude RTS will cause a read error in a multilevel-cell flash memory [2.13]-[2.14]. On the other hand, since RTS is very sensitive to a local potential change near the trap, it can be used as internal probe to detect a variation in a trapped charge density during program, erase and retention. The waveform of RTS

may exhibit two-level or multi-level switching in a current, depending on the number of traps in a device. For simplicity, only devices with two level RTS (single interface trap) are chosen in this work. In this way, we can measure trap emission time and capture time clearly. In this work, we determine a trap position in the channel from RTS, and then use the trap and RTS as internal probe to detect a local potential change due to injected program/erase charge or charge retention loss. A program charge lateral profile is obtained by collecting the measured potential changes in devices with different trap positions. By using this method, we compare the width of the charge distributions by CHE program and by CHISEL [2.15] program. A misalignment between CHE program electrons and BTBT erase holes will be characterized. Finally, mechanisms of program-state V_t retention loss will be re-examined by using this technique.

In this work, a novel random telegraph signal (RTS) method is proposed to characterize the lateral distribution of injected charge in program and erase states in a NOR-type SONOS flash memory. The concept of this method is to use RTS to extract an interface trap position in the channel and then to use the interface trap and RTS as internal probe to detect a local channel potential change resulting from injected charge during program/erase. By using this method, the lateral width of the injected charge induced channel potential barrier is shown to be around 20nm in channel hot electron (CHE) program. Our method also confirms that channel initiated secondary electron (CHISEL) program has a broader injected charge distribution than CHE program. A mismatch of CHE program electrons and band-to-band tunneling erase holes is observed. The polarity of a program-state charge distribution is examined along the channel within 10-20 program/erase cycles.

Nitride charge retention loss is observed by using this method.

2.2 Device Description and Measurement Setup

Measurements were carried out on SONOS flash cells with an ONO thickness of 8.5nm (top oxide), 7nm (nitride) and 5.5nm (bottom oxide), respectively. The channel width and length are W/L=0.11μm/0.1μm. The CHE program condition is V_{gs}=8V and V_{ds}=3.7V. The BTBT hot hole erase is at V_{gs}=-4V and V_{ds}=5V. RTS is measured at a small V_{ds} that the device is operated in the linear region and the channel electric field is uniform.

2.3 Results and Discussions

2.3.1 Extraction of an Interface Trap Position

Typical two-level RTS waveform is shown in Fig. 2.1. The average electron capture time $<\tau_c>$, as illustrated in Fig. 1, can be expressed below,

$$<\tau_c>=\frac{1}{n_e \sigma_t \upsilon_{th}} \quad (1)$$

where σ_t is a trap cross-section, υ_{th} is a thermal velocity and n_e is an electron concentration in the channel right below the trap. n_e is a function of a gate overdrive, i.e. $n_e=f(V_{gs}-V_{ts})$, where V_{ts} is the channel potential at the trap position and is equal to $(1-x_t/L)V_{ds}$. x_t is the distance of the trap from the drain edge and L is the channel length, as shown in Fig. 2.1. It should be mentioned that a uniform channel electric field is assumed here. A pocket implant may induce a non-uniform electric field. This

non-uniform electric field effect, however, can be reduced by using a larger gate overdrive voltage in RTS measurement.

An interface trap position (x_t) in the channel can be extracted in a way similar to [2.16]. Two different drain voltages (V_{ds}=0.05V and 0.3V) are used in RTS and $<\tau_c>$ measurement. Since τ_c depends on the electron concentration n_e, or a voltage drop between the gate (V_{gs}) and the channel right below the trap (V_{ts}), the amount of the lateral shift of these two curves (ΔV_{ts}) in Fig. 2.2 is equal to the difference of the voltages at the point of the trap (x_t), raised by the two drain voltages. Therefore, the trap position in the channel can be extracted from $\Delta V_{ts}/\Delta V_{ds}=1-x_t/L$. In this work, the RTS extraction is conducted in more than 150 fresh cells. For simplicity, we only record devices with two-level RTS (i.e., a single trap). The cumulative trap position distribution along the channel is shown in Fig. 2.3. In fresh SONOS cells, more process-induced interface traps are found near the source/drain junctions. With the information of a trap position in each device, we choose devices with appropriate trap positions as internal probes to investigate program/erase charge lateral spread. The local channel potential at the trap position can be extracted from the ratio $<\tau_c>$ to $<\tau_e>$ in RTS according to the following equation.

$$\frac{\langle \tau_c \rangle}{\langle \tau_e \rangle} = g \exp\left(\frac{E_T - E_F}{kT}\right) \qquad (2)$$

and

$$\frac{\left.\frac{\langle\tau_c\rangle}{\langle\tau_e\rangle}\right|_{prog}}{\left.\frac{\langle\tau_c\rangle}{\langle\tau_e\rangle}\right|_{fresh}} = \exp\left(\frac{q\Delta\varphi_s}{kT}\right) \quad (3)$$

where g is a degeneracy factor [2-17]. E_T is the trap energy and $\Delta\varphi_s$ is a local potential change at the trap position due to injected program charge. Note that Eq. (3) still holds even though a phonon-assisted transition process is considered.

2.3.2 CHE Program Charge Lateral Profile

To profile the lateral charge distribution by CHE programming, four SONOS cells are used with a respective trap position at x_t=0.03L, 0.05L, 0.2L and 0.3L from the drain junction. Fig. 2.4 shows RTS traces of the channel current at three program ΔV_t(=0.3V, 0.9V, 1.2V) in the x_t=0.2L cell. The RTS measurement is fixed at V_{gs}=3.5V and V_{ds}=0.05V. The device is in strong inversion at the measurement biases. Fig. 3.5 shows measured average capture time $<\tau_c>$ and emission time $<\tau_e>$ versus program ΔV_t. The minimum integration time is 0.5ms and the total sampling period is 10s. The observed trends in the $<\tau_c>$ and $<\tau_e>$ versus program ΔV_t are similar to previous results [2.18]. The ratio of average capture time to emission time $<\tau_c>/<\tau_e>$ and a corresponding surface potential change ($\Delta\varphi_s$) at x_t from Eq. (2) are plotted in Fig. 2.6. As more electrons are injected into the nitride layer, the conduction band-edge at x_t and the trap level move upward with respect to the Fermi level. Thus, the $<\tau_c>/<\tau_e>$ ratio increases with ΔV_t. The measured $<\tau_c>/<\tau_e>$ versus ΔV_t in the four cells are shown in Fig. 2.7. For a x_t closer to the drain junction, for example, the x_t=0.03L cell,

the τ_c/τ_e ratio increases more rapidly with ΔV_t, implying a higher program charge density at the trap position x_t=0.03L. In contrast, the τ_c/τ_e remains almost unchanged in the x_t=0.3L cell, which means the injected program charge does not reach the trap point during program. The surface potential energy change along the channel for a program window of ΔV_t=0.6V is presented in Fig. 2.8. The program charge induced potential barrier is within 30nm. Our result is consistent with most of published results from the inverse I-V method [2.4-2.6] and from Monte Carlo simulation [2.6], [2.19].

2.3.3 CHE versus CHISEL programming

To compare the width of injected charge by CHE and CHISEL program [2.18], a SONOS cell having a trap at x_t=0.2L is used. The device is programmed by CHE first. The ratio of τ_c/τ_e versus a program ΔV_t is recorded. Then, the device is erased and re-programmed by CHISEL. In CHISEL program, a substrate bias of -2V is applied. Fig. 2.9 shows the evolution of τ_c/τ_e with ΔV_t by CHE and CHISEL. The τ_c/τ_e ratio increases more quickly by CHISEL than by CHE. This means that the local channel potential at x_t=0.2L is affected by injected charge earlier in CHISEL program as ΔV_t increases. In other words, the program charge has a broader distribution in CHISEL than in CHE program at the same program ΔV_t. Our findings here are consistent with the result in [2.20]

2.3.4 CHE Program/BTBT Erase Charge Mismatch

In this section, we discuss the lateral misalignment between CHE program electrons and BTBT erase holes. To this purpose, we choose two devices with a trap

located at the position of 0.05L and 0.3L, respectively, from the drain junction. The two devices are programmed by CHE and then erased by BTBT hot holes. Fig. 2.10 and Fig. 2.11 show the evolution of the τ_c/τ_e during program and erase in the two devices. The τ_c/τ_e increases with a program ΔV_t and then decreases during erase. In Fig. 10, our monitor point is at x_t=0.05L in the channel. The τ_c/τ_e curves during program and erase match reasonably well, suggesting that program electrons at 0.05L can be totally neutralized by erase holes. To examine the charge polarity in erase state, the τ_c/τ_e near ΔV_t=0V is re-drawn in a log scale in the inset of Fig. 2.10. The erase-state τ_c/τ_e is actually lower than its value in a fresh state. This result provides evidence of hole accumulation near the drain junction in erase state. This phenomenon becomes more pronounced in an over-erased cell, i.e., ΔV_t<0V. On the contrary, in Fig. 2.11 where the monitor point is at x_t=0.3L, the τ_c/τ_e ratio is significantly above its original value after a P/E cycle. The larger τ_c/τ_e value after one P/E cycle implies the existence of some residual program electrons at x_t=0.3L although the cell has been erased to its original V_t. Combining the results in Figs. 2.10 and 2.11, the charge distributions in program and in erase are depicted in Fig. 2.12. A misalignment of injected erase holes and program electrons [2.11], [2.21] is concluded. The erase holes have a narrower spatial distribution than CHE program electrons.

2.3.5 Program Charge Retention Loss

Two types of models have been published to explain the observed program-state V_t retention loss in a SONOS cell. The first one is nitride charge vertical loss through P/E cycling induced oxide traps [2.22]-[2.26]. The second type of the models explains the V_t retention loss by lateral redistribution of nitride charges

in program state [2.27]-[2.30]. The possibility of program electron lateral movement [2.30] is explored by the RTS method in Fig. 2.13. The cell has only one-time program and then is subject to high temperature bake. The trap position is at 0.03L from the drain. The result shows that the τ_c/τ_e remains the same during the bake, indicating that the program electron concentration is unchanged. Another explanation for a program-state V_t loss is nitride trapped hole lateral migration. A three-pole electron-hole-electron distribution in program state has to be assumed in the hole lateral migration models [2.27]-[2.29]. We use the RTS method to examine the charge polarity along the channel in program state. The trap position (monitor point) in measured devices spreads from the drain junction to 0.4L into the channel. We measured program-state and erase-state RTS at different P/E cycles. Fig. 2.14 shows the program-state and erase-state τ_c/τ_e versus P/E cycles in an x_t=0.05L device. At other x_t, the τ_c/τ_e dependence on P/E cycle has a similar feature and the result is not shown here. The cycle number in Fig. 2.14 is 16. The reason is that RTS becomes unclear at more P/E cycles due to new interface trap creation. In our monitored range of P/E cycles, program-state τ_c/τ_e is always above its original value, showing a negative charge polarity in all the measured cells. We do not find any evidence of positive charge (hole) accumulation in program state. Although there is no sign of hole accumulation within 10-20 P/E cycles. However, we would like to point out that a program-state charge profile may vary with operation biases, device doping profile and P/E cycling conditions [2.29]. Although there is no sign of hole accumulation within 10-20 P/E cycles in the present cycling and bias conditions, we still observe an apparent charge retention loss in these cells under a gate stress condition (V_g=-5V) in Fig. 2.15. The τ_c/τ_e ratio decreases with gate stress time. RTS traces immediately after

program and after 4 seconds gate stress are presented in the inset of Fig. 2.15. The τ_c/τ_e ratio decreases with gate stress time in Fig. 2.15. Since hole accumulation and lateral movement have been excluded in the cell, the observed decrease of the τ_c/τ_e is attributed to charge vertical loss, i.e, stored electron emission through the bottom oxide. Fig. 2.16(a) shows the read current variation versus gate stress time in a 33 P/E cycled cell. The setup for this measurement is shown in Fig. 2.16(b) [2.14]. An electronic switch is used to record gate stress time accurately. The sampling rate is 10kHz, which enable the observation of read current switching with time resolution up to 0.1ms. Both RTS and long-term nitride charge escape are both observed. Individual nitride charge loss is manifested by a long-term abrupt increase of a read current. During two consecutive nitride charge escapes, RTS is observed. It should be stressed that the "average" read current level remains constant between two consecutive nitride charge escapes. This stepwise evolution characteristic provides an evidence of the vertical charge loss. In Fig. 2.17, the retention result is shown in a uniform FN program/erase NAND SONOS cell. In such a device, charge lateral movement should be excluded. But we still observe a clear step-wise current evolution during retention. The feature is pretty much the same as Fig. 2.16(a). These jumps can be explained by a single charge vertical loss plus the percolation effect. If the charge lateral migration is dominant, the current evolution should be "GRADUAL" rather than "ABURPT" since the ΔI_d due to single-step charge hopping in the lateral direction should be very small.

One major argument in [2.28] against the vertical loss model is "the bottleneck of the carrier loss is either the tunneling or the Frenkel-Poole detrapping". This argument is incorrect since they do not consider the re-capture of nitride conduction

band electrons into nitride traps before tunneling out through the bottom oxide. By taking into account the re-capture process, we showed [2.31] that even in the Frenkel-Poole (FP) emission limited condition (i.e., Frenkel-Poole emission time longer than oxide tunneling time) the nitride charge retention time can be approximated by

$$\tau(retention) = \frac{\tau_{\mathrm{e}}(FP) + \tau_{\mathrm{c}}(FP)}{\tau_{\mathrm{c}}(FP)}\tau_{ox} \sim \exp\left(\frac{E_T - q(qF/\pi\varepsilon)^{1/2}}{kT}\right)\tau_{ox} \tag{3}$$

where τ_e(FP) and τ_c(FP) are the Frenkel-Poole emission and capture times. τ_{ox} is an oxide tunneling time, or more specifically, positive oxide trapped charge (hole) assisted tunneling time. F is an electric field in nitride. Other variables have their usual definitions. The above equation can well explain many salient features of the observed program-state V_t retention loss, for example, log dependence on retention time [2.22],[2.26],[2.35] and P/E cycle number ([2.35], Fig. 2.9 in [2.33]), negative dependence on gate stress voltage polarity [2.23],[2.26],[2.34], positive dependence on retention temperature [2.22],[2.26],[2.27]. The comparison of the model predictions from Eq. (4) and experimental results is summarized in Table 2.1. It should be remarked that trap anneal effect during high temperature bake is not considered in Eq. (4). Thus, a deviation between the model and measurement results in the temperature dependence is expected. Although the charge vertical loss model can explain the above measurement results well, other V_t retention loss mechanisms may co-exist in different operation bias or device process conditions.

Finally, we would like to remark that the above RTS measurement is limited to

a low P/E number because of cycling induced new interface trap creation. The RTS measurement result in Fig. 14 does not exclude the possibility of hole accumulation and thus a dipole formation in a heavily cycled cell, or in other device process conditions [2.29].

2.4 Summary

We have demonstrated a novel RTS method to characterize program and erase charge lateral spread in a SONOS flash memory without the need to know a doping profile. In the RTS method, the τ_c/τ_e is very sensitive to program/erase/retention charges. It exhibits an exponential dependence on a local potential, as compared to a linear dependence in the CP method. The RTS method can provide a better resolution than a charge pumping method or an inverse I-V modeling approach. A mismatch between program electrons and erase holes is shown by this method. Read current instability due to nitride charge vertical loss and random telegraph noise is directly observed.

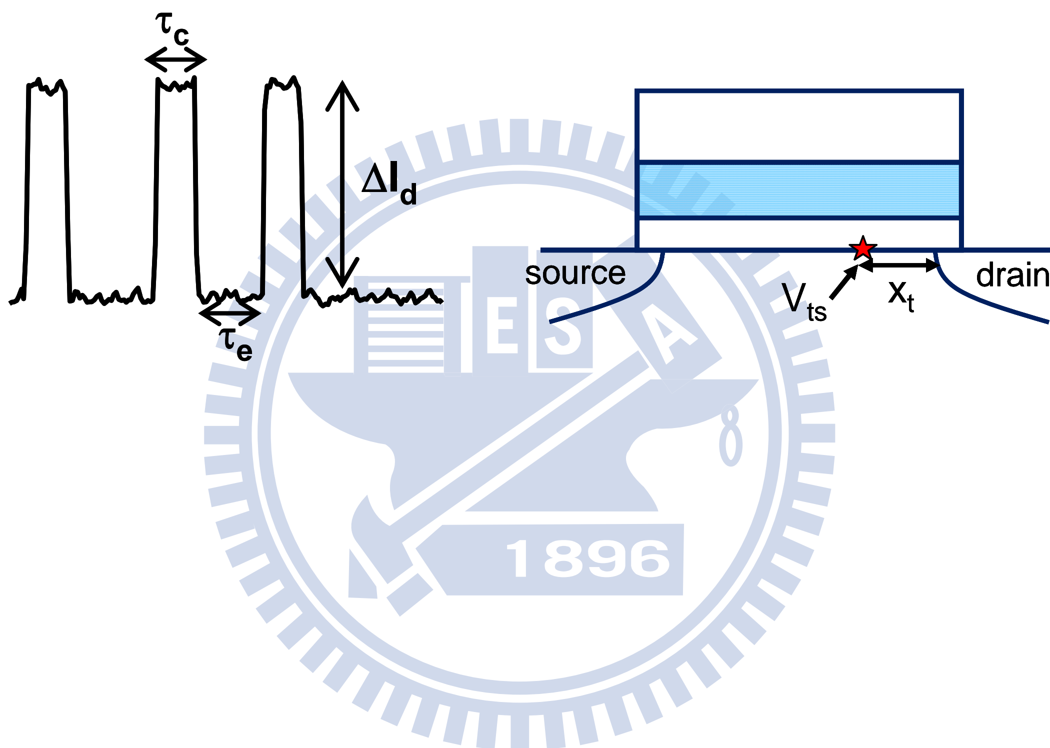


Fig. 2.1 Illustration of a two-level RTS waveform resulting from electron emission and capture at an interface trap. τ_c and τ_e are electron emission time and capture time. The trap position is x_t from the drain junction. The channel potential right below the trap is denoted by V_{ts}.

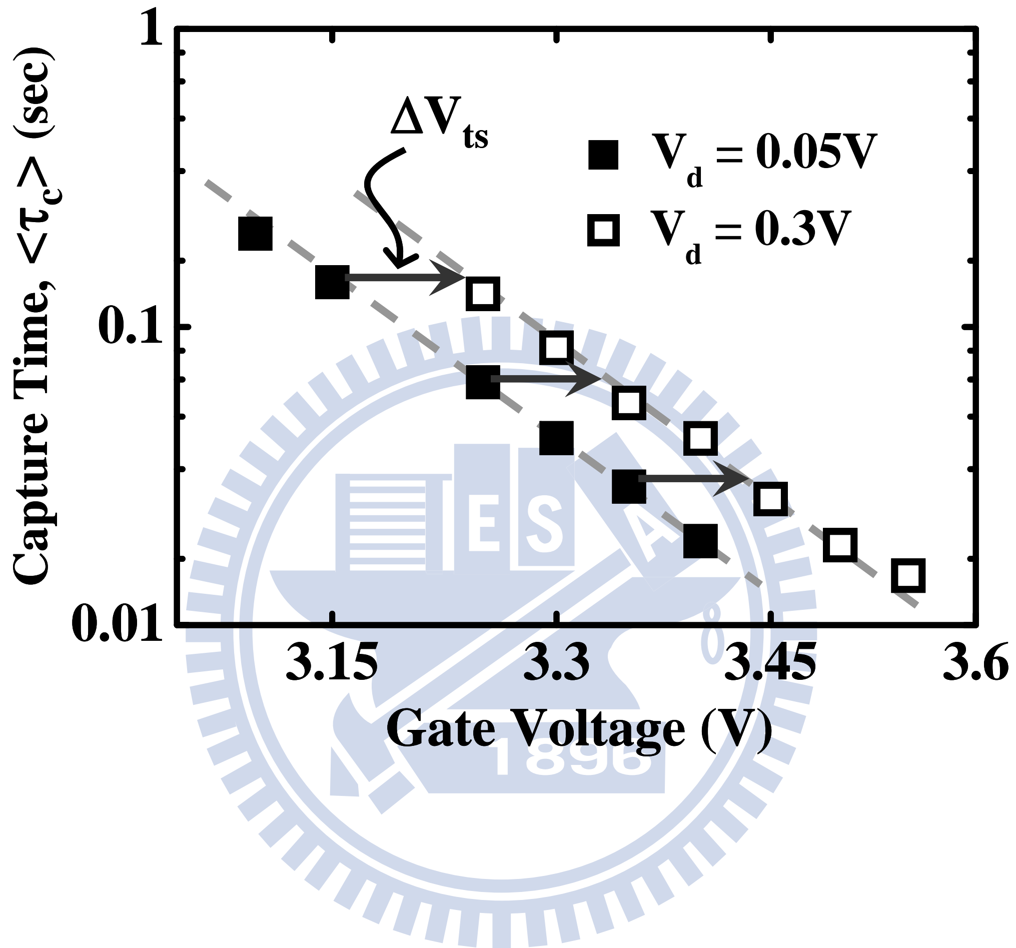


Fig. 2.2 The gate voltage dependence of average capture time in RTS at two drain voltages, V_{ds}=0.05V and 0.3V. The lateral shift of these two curves corresponds to ΔV_{ts}.

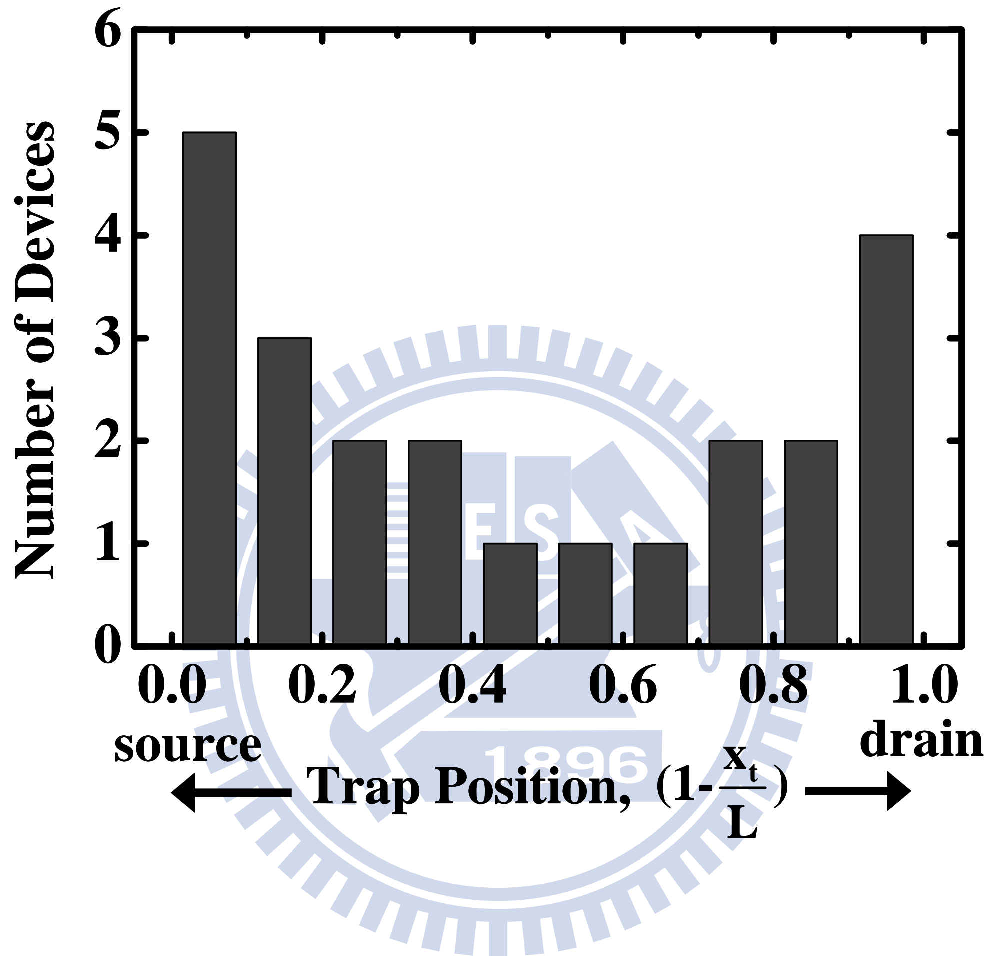


Fig. 2.3 Cumulative trap position distribution along the channel. L=0.1μm is the channel length and x_t is the distance of a trap from the drain.

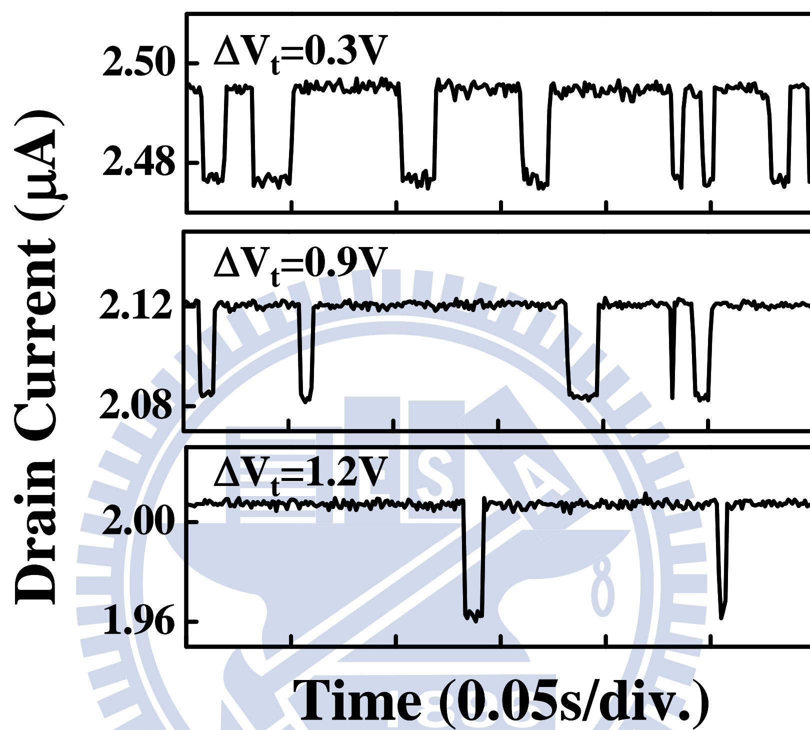


Fig. 2.4 RTS patterns at three program ΔV_t=0.3V, 0.9V and 1.2V in a CHE program cell. The RTS measurement condition is V_{gs}=3.5V and V_{ds}=0.05V. x_t =0.2L.

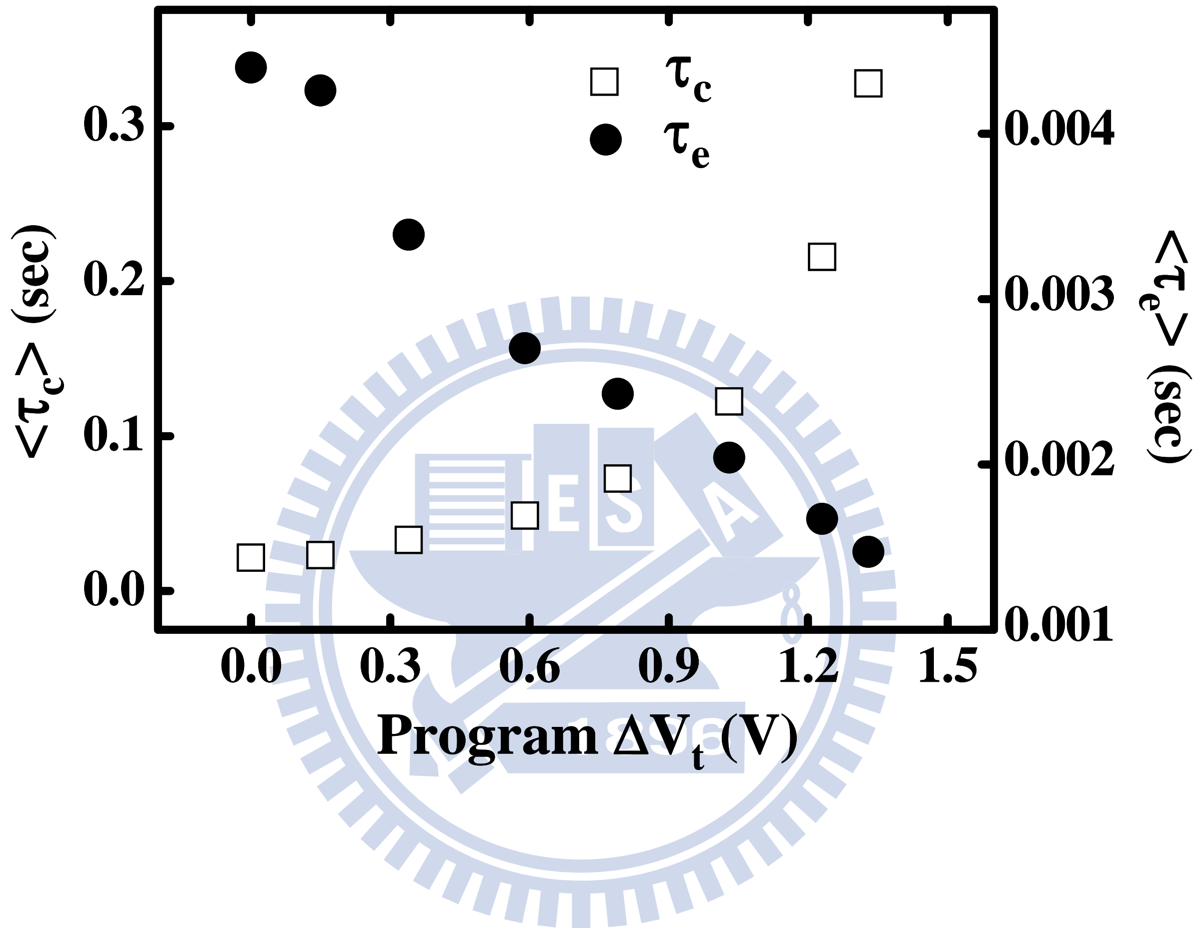


Fig. 2.5 Average capture time (τ_c) and emission time (τ_e) versus program ΔV_t in an x_t =0.2L cell.

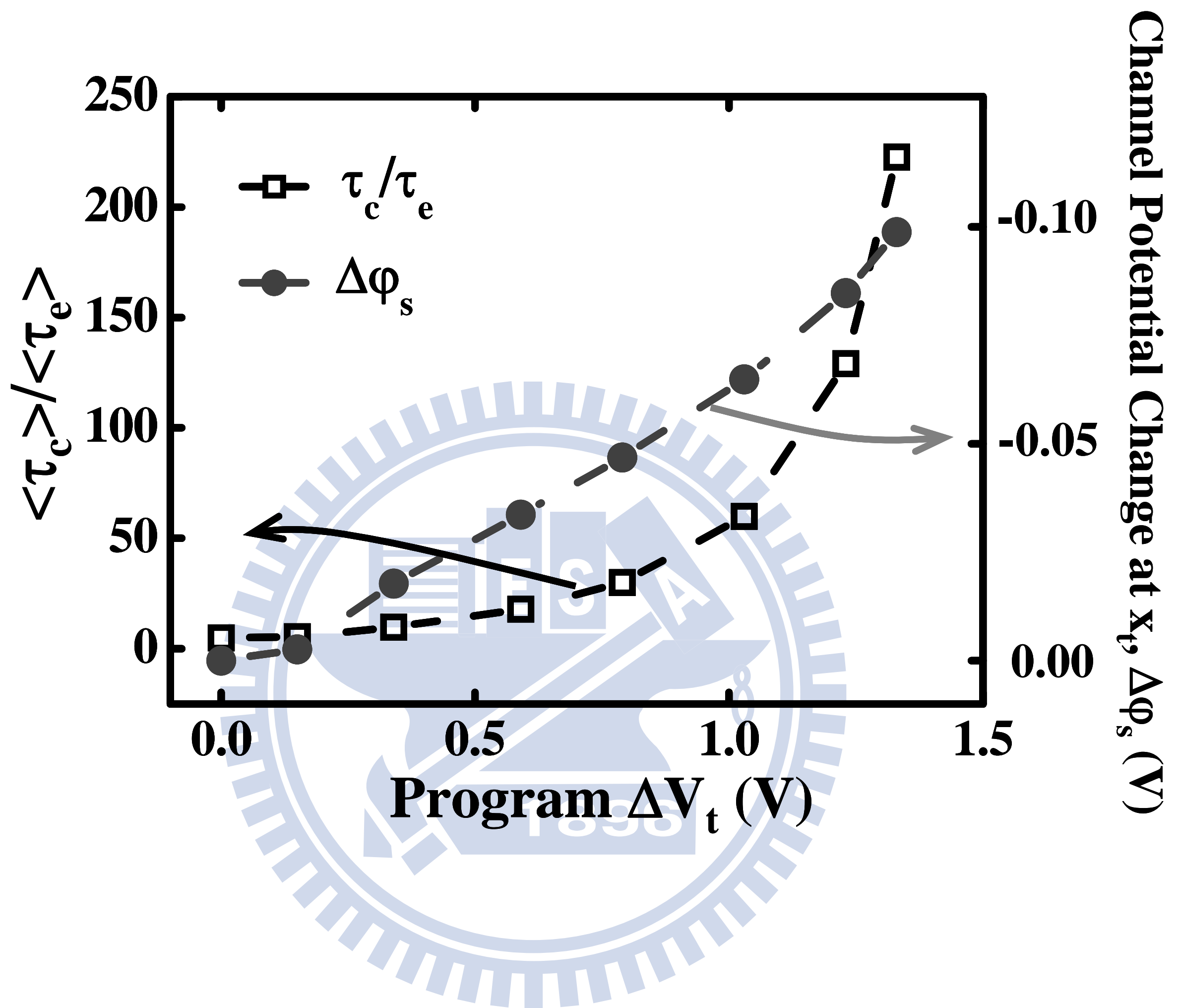


Fig. 2.6 The ratio $<\tau_c>/<\tau_e>$ and a local surface potential change ($\Delta\varphi_s$) at the trap position (x_t =0.2L) versus program ΔV_t. The local potential change is calculated from Eq. (2).

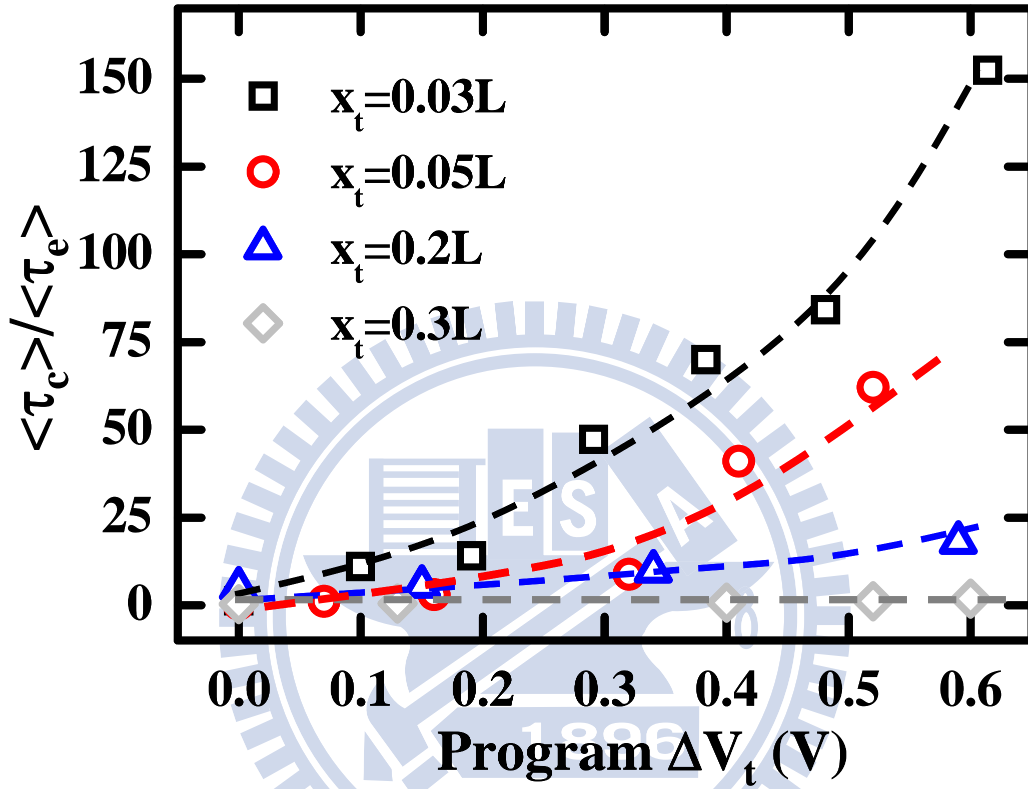


Fig. 2.7 Evolutions of $<\tau_c>/<\tau_e>$ with program ΔV_t at four different trap positions x_t=0.03L, 0.05L, 0.2L and 0.3L.

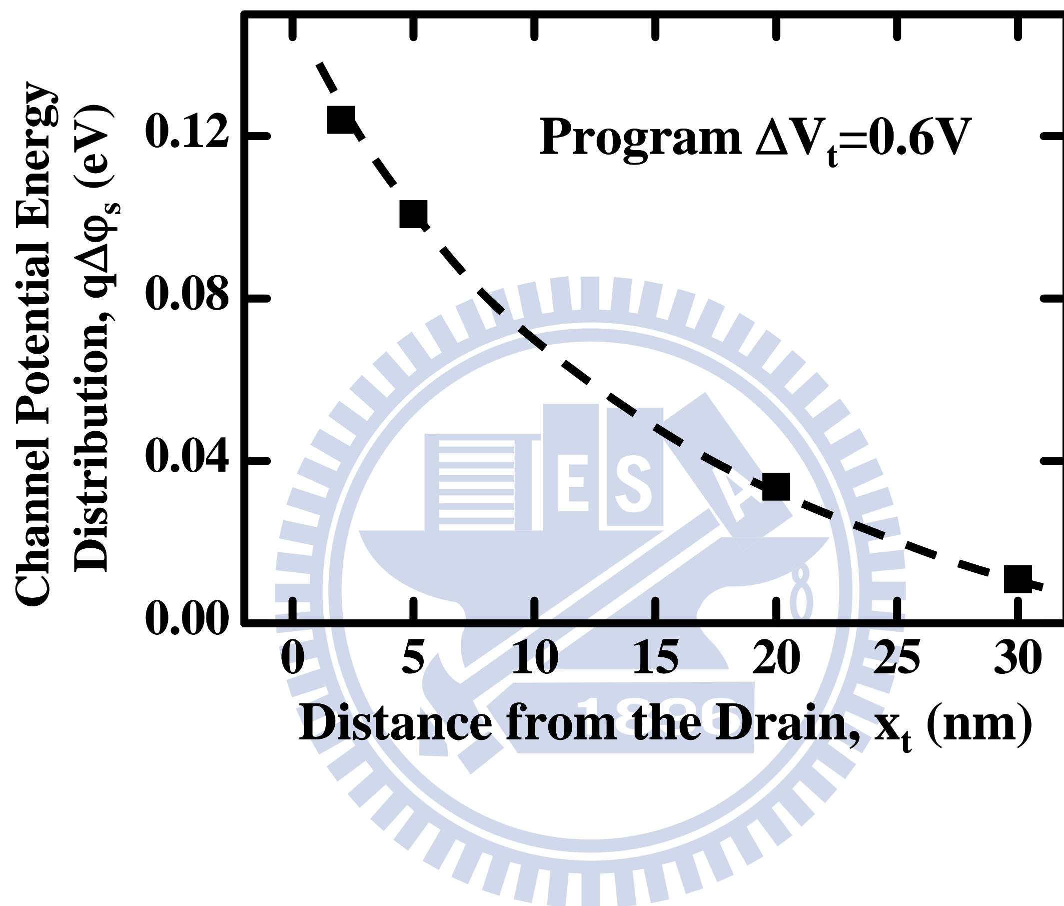


Fig. 2.8 The channel potential energy distribution extracted from RTS. The CHE program window is ΔV_t=0.6V. The width of the potential energy barrier is about 20nm.

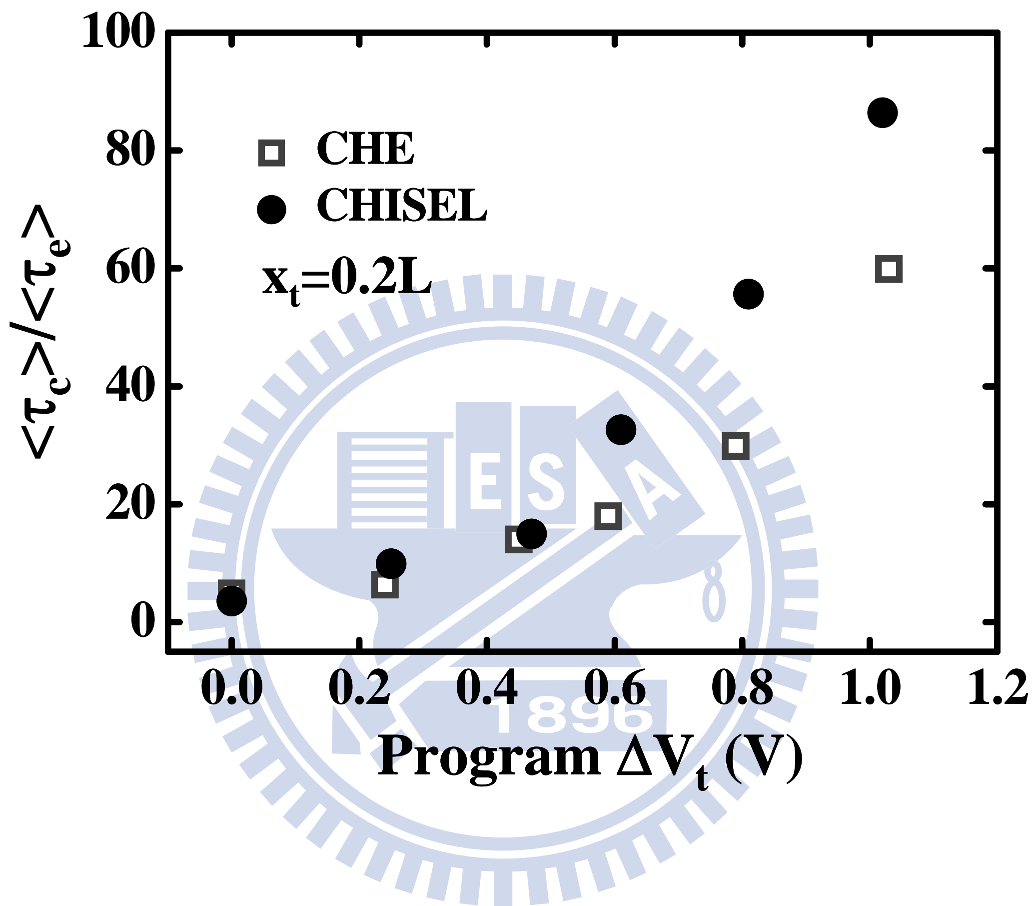


Fig. 2.9 Comparison of $<\tau_c>/<\tau_e>$ evolutions with program ΔV_t in CHE and CHISEL program. A substrate bias of -2V is applied in CHISEL program.

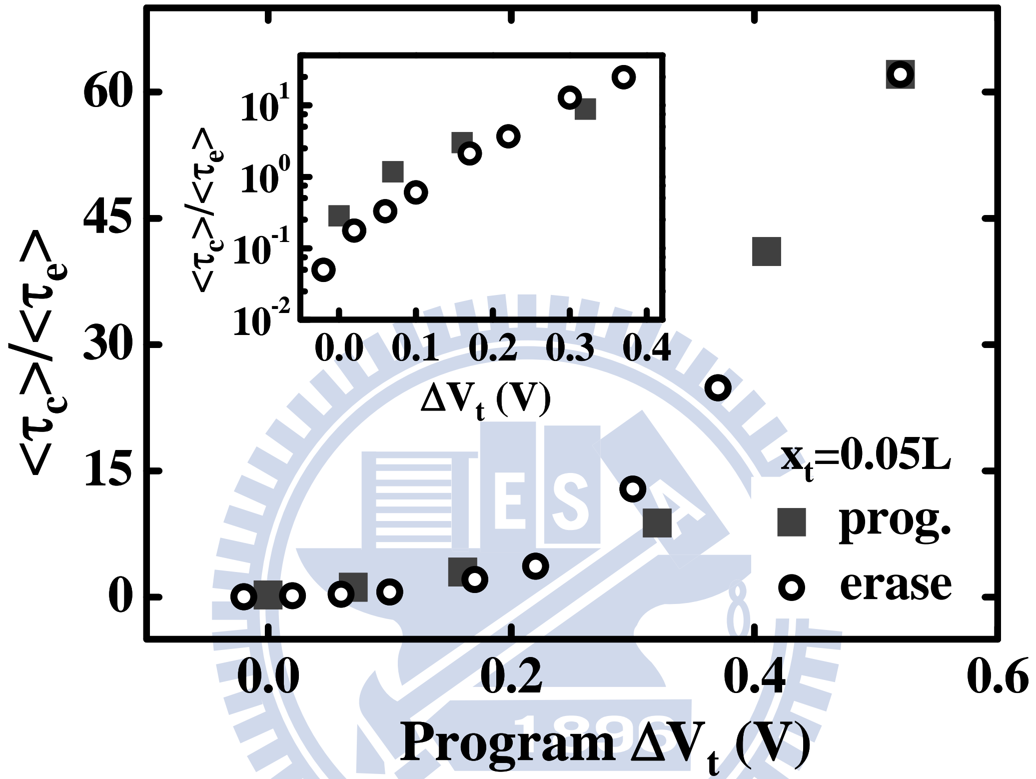


Fig. 2.10 The <τ_c>/<τ_e> versus program ΔV_t during CHE program and BTBT hot hole erase. The device has a trap at 0.05L from the drain. The inset shows the <τ_c>/<τ_e> in a log scale.

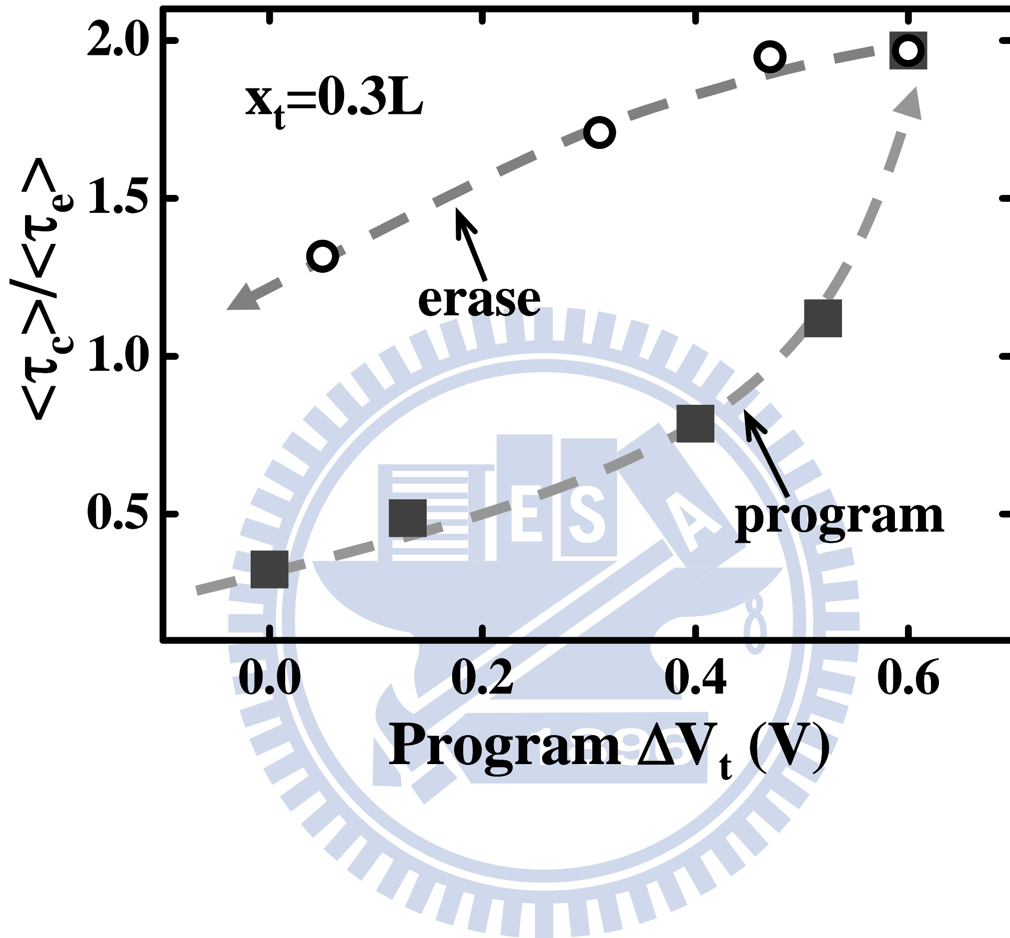


Fig. 2.11 The $<\tau_c>/<\tau_e>$ versus program ΔV_t during CHE program and BTBT hot hole erase. The device has a trap at 0.3L from the drain.

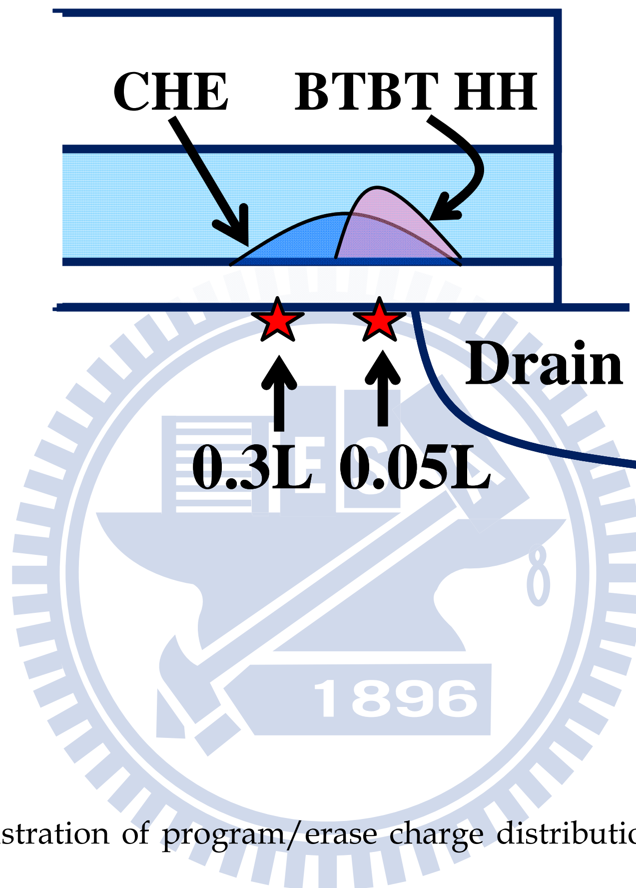


Fig. 2.12 Illustration of program/erase charge distributions in the channel. The stars represent interface traps. The program electrons at x_t=0.05L are completely compensated, but some far electron at x_t=0.3L are not compensated by erase holes.

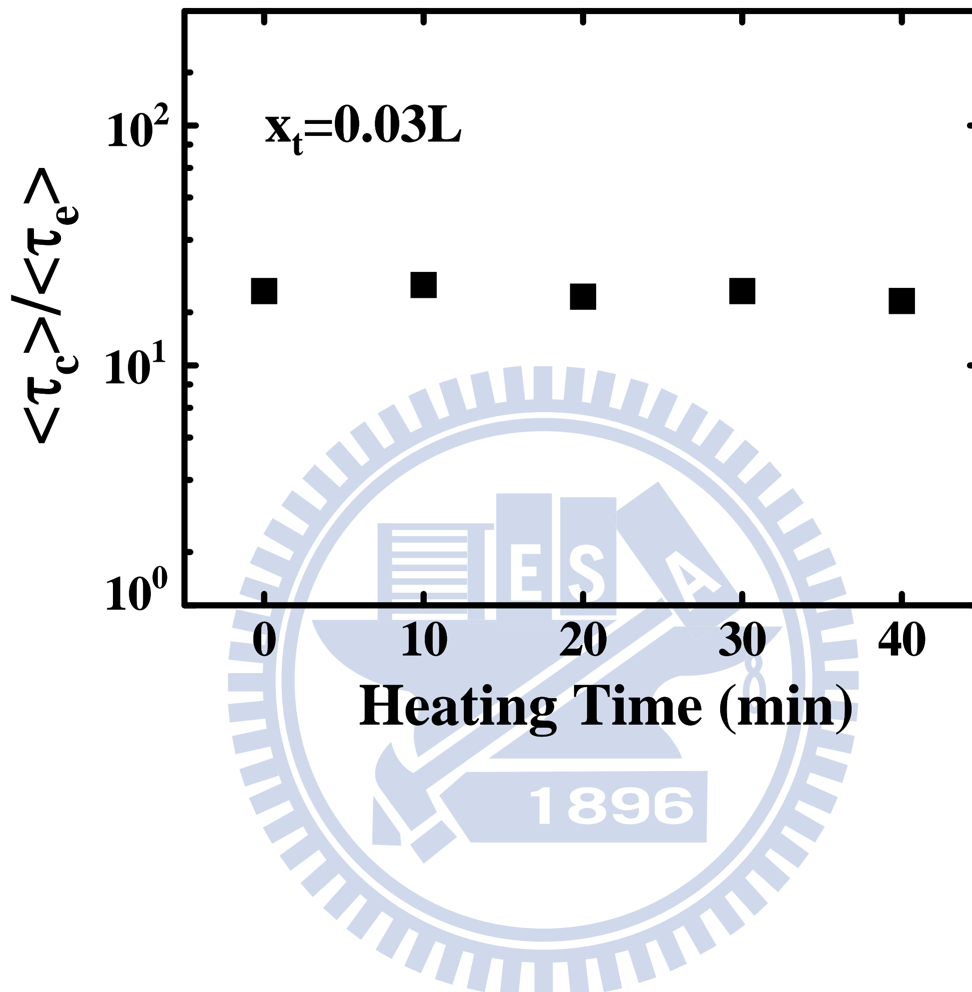


Fig. 2.13 The <τ_c>/<τ_e> in a program-only cell versus bake time. The x_t is 0.03L. The bake temperature is 120℃. The program ΔV_t is 1V.

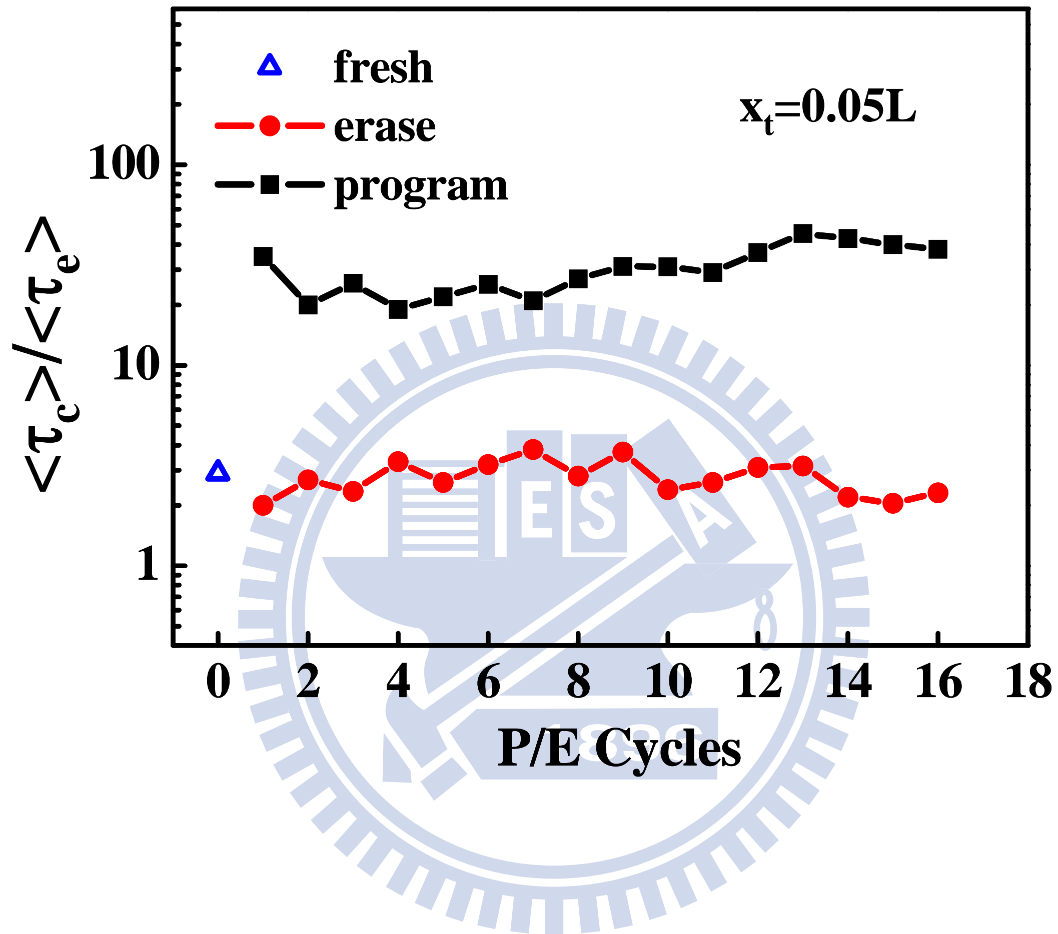


Fig. 2.14 Program-state and erase-state $<\tau_c>/<\tau_e>$ at different P/E cycles. The x_t is 0.05L. The $<\tau_c>/<\tau_e>$ in fresh state is also shown in the figure. The program ΔV_t is 1V.

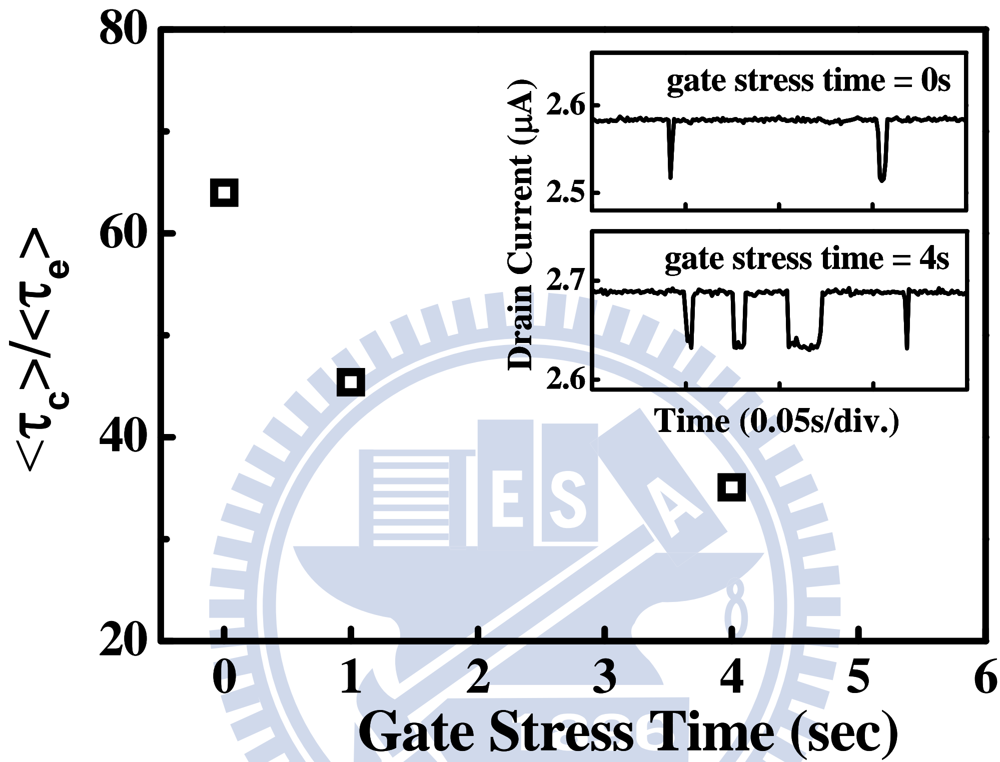


Fig. 2.15 Program-state $<\tau_c>/<\tau_e>$ is plotted against gate stress time. The program ΔV_t is 1V. The gate stress voltage is Vg=-5V. The trap position x_t is 0.05L. RTS waveforms immediately after program and after 4-second gate stress are shown in the inset of the figure.

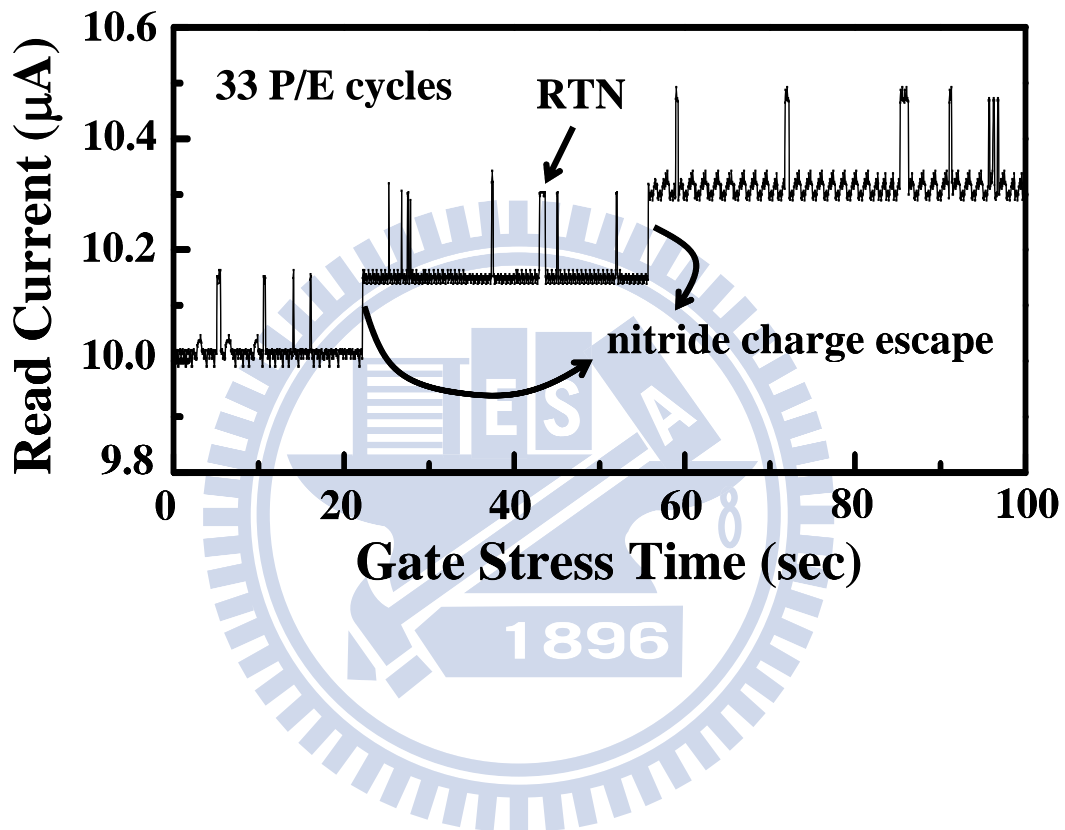


Fig. 2.16(a) Read current variation with cumulative gate stress time in program state. The P/E cycle number is 33.

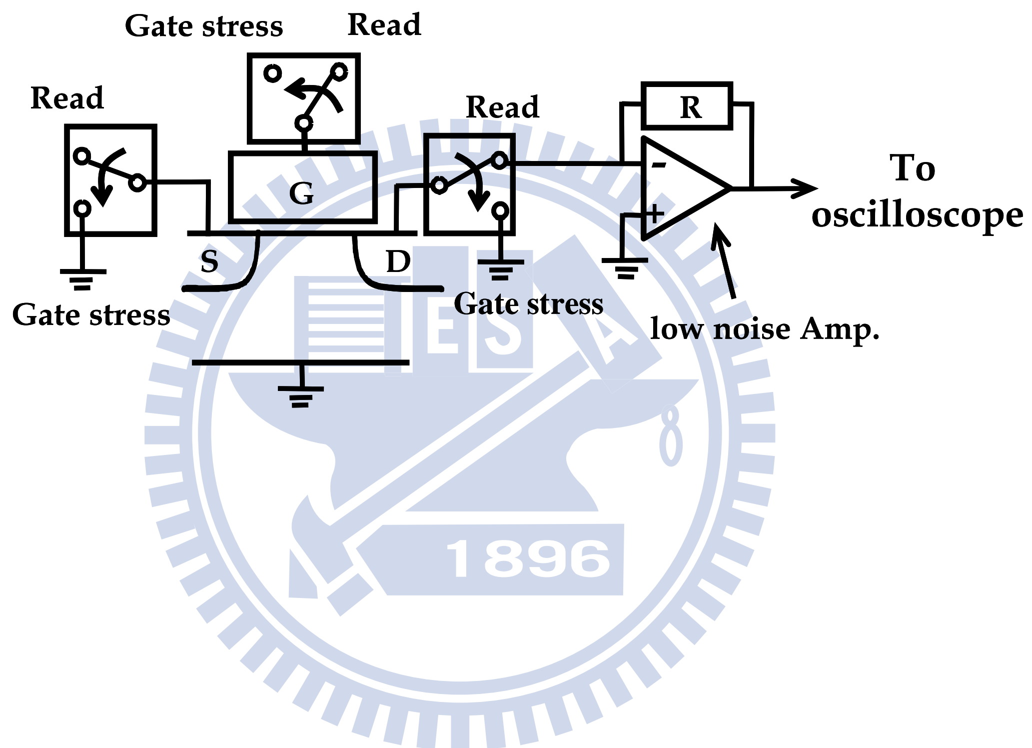


Fig. 2.16(b) Experimental setup for read current measurement. The measurement consists of two alternating phases, a gate stress phase and a read phase. In gate stress, a negative gate voltage (-3.5V) is applied to accelerate nitride charge loss. The sampling rate is 10kHz. The program ΔV_t is 2V

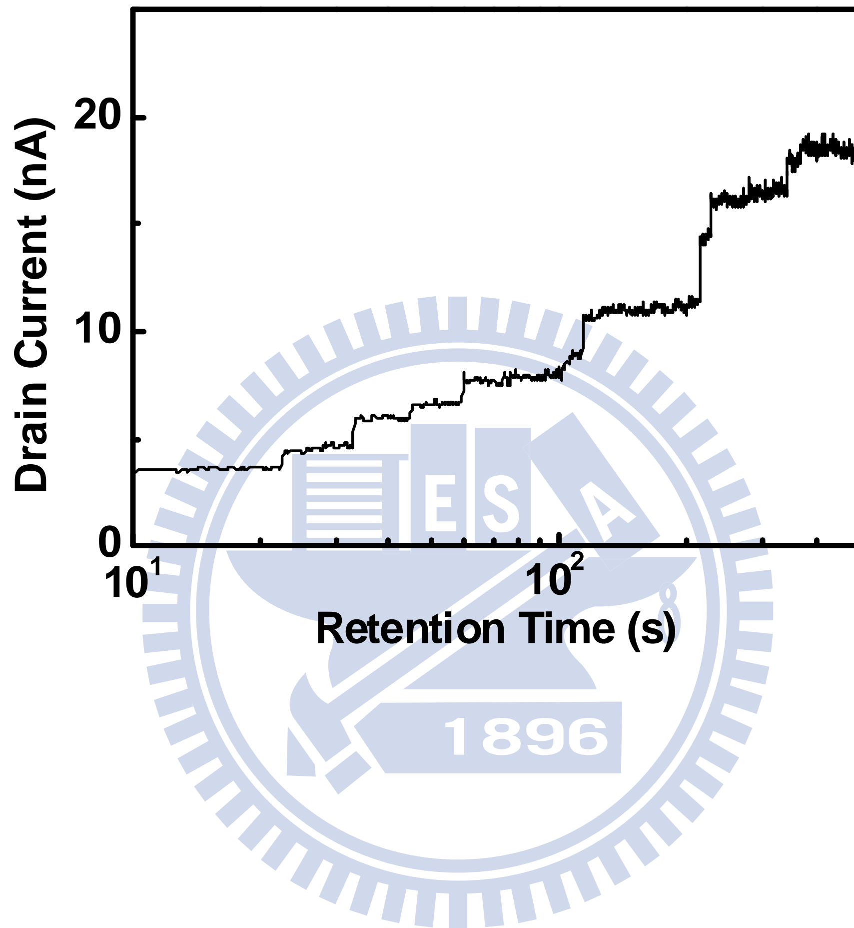


Fig. 2.17 Step-like drain current during retention time in a SONOS NAND cell with uniform FN program/erase.

program-state retention loss (ΔV_t)	retention time (t)	P/E cycle number (N)	gate stress (V_g)	bake temp. (T)
vertical charge loss model (FP emission limited, Eq.(4))	$\Delta V_t \sim \log(t)$	$\Delta V_t \sim \log(\tau_{ox}^{-1})$ $\sim \log(N_{ox})$ $\because N_{ox} \sim t_{stress}^{n} \sim N^{n}$ [32] $\therefore \Delta V_t \sim \log(N)$	**negative V_g polarity dep.**	$\Delta V_t \sim T$
experimental result	**log dep. [22,26,35]**	**log dep. [33(Fig.9),35]**	**negative V_g polarity dep. [23,26,34]**	**positive temp. dep. [22,26,27]**

Table 2.1 Dependence of program-state V_t retention loss on retention time, P/E cycles, gate stress polarity and temperature from the vertical charge loss model (in a FP emission limited condition) and from experimental results.

Chapter 3

Program Charge Effect on Random Telegraph Noise Amplitude in Floating Gate and SONOS Flash Memory

3.1 Preface

Random telegraph noise (RTN) arising from electron emission and capture at an interface trap site has been recognized as a new scaling constraint in flash memories [3.1]-[3.4]. V_t fluctuations originated from a large-amplitude RTN tail will cause a read failure and become a prominent issue in designing a multilevel-cell (MLC) flash memory in 45nm technology node and beyond [3.3], [3.4]. Recently, a statistical model based on a three-dimensional Monte Carlo simulation [3.5], [3.6] has shown that the amplitudes of RTN and thus the V_t fluctuations exhibit an exponential distribution, i.e., $f(\Delta V_t)=\exp(-\Delta V_t/\sigma)/\sigma$ [3.4]. In a floating-gate (FG) flash memory, a RTN tail is attributed to a current-path percolation effect due to random dopants in substrate, as shown in Fig. 3.1, and σ is dependent on a substrate doping concentration. Unlike a FG flash cell, where program charges are stored in a conducting poly-silicon and have a continuous distribution, program charges in a SONOS cell are stored in silicon nitride traps. Because of the nature of random nitride charge trapping, a current percolation path in a SONOS cell is formed by both substrate dopants and program charges.

In this chapter, we will investigate program charge effects on RTN amplitudes in floating gate flash and SONOS flash. We measure RTN in 45 planar SONOS cells and 40 floating-gate cells in erase state and program state, respectively. We find that

a SONOS cell has a wide spread in RTN amplitudes after programming while a floating gate cell has identical RTN amplitudes in erase and program states at the same read current level. A 3D atomistic simulation is performed to calculate RTN amplitudes. Our result shows that the wide spread of program-state RTN amplitudes in a SONOS cell is attributed to a current-path percolation effect caused by random discrete nitride charges.

3.2 Device Description and Measurement Setup

The SONOS cell has a 6nm top oxide, a 6nm nitride layer, and a 2.8nm bottom oxide. The device area is $0.09\times0.08\mu m^2$. The FG cell has W/L=0.11μm/0.09μm and a tunnel oxide thickness of 8nm. Uniform FN injection is employed for program and erase. The program V_t window is chosen to be 1V for MLC application.

3.3 Results and Discussions

3.3.1 Comparison of the Erase- and Program-state RTN in a FG and SONOS Cell

In order to characterize the different dependence of RTN on program charge effect in a FG and SONOS device, we measured single-trap RTN relative amplitudes ($\Delta I_d/I_d$) versus drain current in both FG cell and SONOS flash cell. In RTN measurement, the drain voltage is 0.7V, and the gate voltage varies such that the drain-current ranges from 50nA to 2uA. The erase-state and program-state RTN amplitudes versus the drain current in three P/E cycles in FG flash cell are shown in Fig. 3.2. Program-state and erase-state RTN have almost identical amplitudes at the same read current level. This result implies that program charges in a FG cell do not have an effect on RTN amplitudes. In other words, they do not alter a current

percolation path caused by random dopants. Fig. 3.3 shows measured erase-state and program-state RTN amplitudes in a SONOS cell in three consecutive P/E cycles. The program-state RTN varies from cycle to cycle, suggesting that program charges play an important role in current percolation paths. The measured RTN waveforms and the I_d-V_g are shown in Fig. 3.4. Two-level current switching is observed, showing that RTN arises from a single interface trap and no additional traps are created during P/E cycles. Fig. 3.5 illustrates the different dependence of current percolation paths on program charges in FG and SONOS cell respectively.

3.3.2 Statistics Results of Erase-state and Program-state in FG and SONOS devices

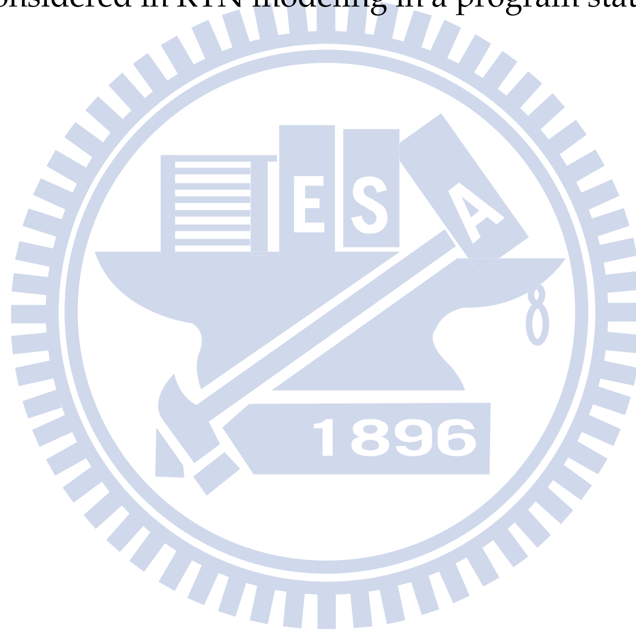
To confirm the different program charge effects in FG and SONOS devices, we also measured single-trap RTN relative amplitude ($\Delta I_d/I_d$) in 40 FG flash cells and 45 SONOS flash cells, then we perform a bit-by-bit tracking plot of program-state RTN amplitude versus erase-state RTN amplitude. RTN amplitudes in erase-state and in program-state are traced in each cell at the same read current level of 500nA. In FG flash cells, all the dots are almost lay on the straight line with the slope=1, as shown in Fig. 3.6. We changed the program V_t window from 1V to 2V and the result remains the same. Program-state and erase-state RTN have the same amplitudes in each FG cell. Again, this result implies that the current percolations caused by substrate dopants are not altered after programming. As a contrast, a distinctly different feature is obtained in a SONOS flash cell. Fig. 3.7 shows program-state RTN versus erase-state RTN in 45 SONOS cells. The RTN amplitudes spread in a wide range after programming and are almost independent of erase-state RTN. It is deduced that program charge effect on RTN is significant in SONOS cells.

3.3.3 3D Atomistic Simulation of RTN

To evaluate a nitride trapped charge effect on RTN, we performed a 3D atomistic simulation with random discrete program charges and substrate dopants. The simulation flowchart is shown in Fig. 3.8. Two different program charge storage characteristics, continuous charge and discrete charge, in FG and SONOS cell have to be taken into account respectively. In a FG cell simulation, only substrate dopants are randomly placed, and program charges have a continuous distribution. An equi-potential condition in a FG is obtained in the simulation. We calculate the change of the drain current due to trapping/detrapping of an interface charge placed in the center of the device. Fig. 3.9 shows our simulated RTN in program-state and erase-state have the same amplitude, which is in agreement with our measured result. The simulated RTN amplitudes in a SONOS cell are shown in Fig. 3.10. Ten different sets of random nitride charges having a similar program-state V_t are simulated. The number of nitride electrons in simulation is 180. In all simulations (program-state or erase state), a fixed placement of random substrate dopants is used. The RTN amplitude due to a number fluctuation effect is simulated by assuming continuous substrate doping and program charge distributions for reference. The program-state and erase-state RTN amplitudes are much larger than the current variation due to number fluctuation. This suggests that the large-amplitude RTN results from a percolation effect. In Fig. 3.10, we observe a wide spread in program-state RTN amplitudes in a SONOS cell since each set of program charges results in a different current percolation path. The large spread of program-state RTN amplitudes from cycle to cycle in Fig. 3.3 can be also realized.

3.4 Summary

Read failure due to a large amplitude RTN tail is an urgent issue in flash memory scaling. Random program charge effects in a planar SONOS cell on RTN have been characterized and simulated. In a FG cell, the RTN tail is mainly attributed to random substrate dopants while in a SONOS cell the percolation path and thus the amplitude of RTN are determined by both substrate dopants and program charges. Our simulation shows that random program charges have a large effect on RTN. This effect has to be considered in RTN modeling in a program state of a MLC SONOS.



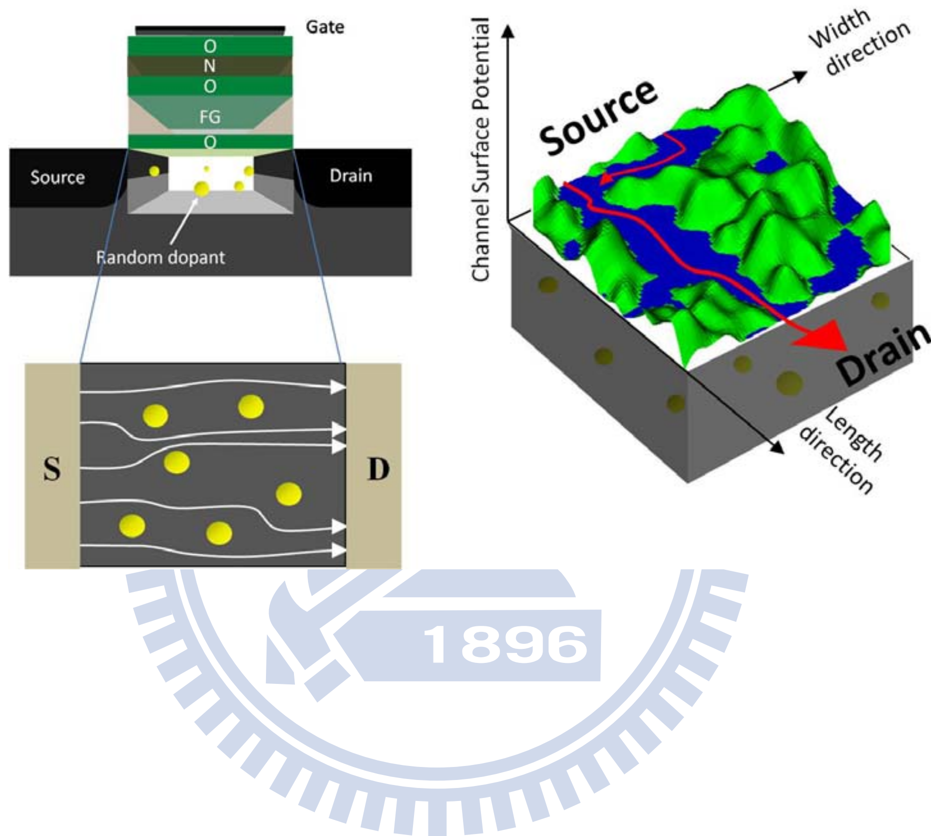


Fig. 3.1 An illustration of random potential induced percolation effect (from [3.7]) in FG cell.

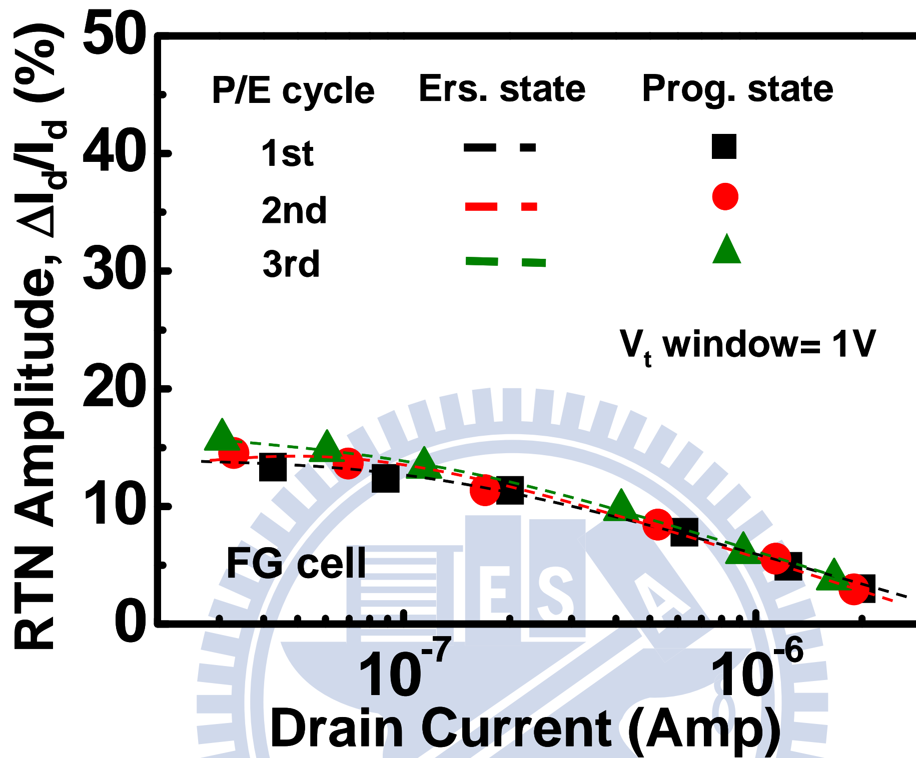


Fig. 3.2 RTN amplitude versus drain current in a FG flash cell in three P/E cycles. The V_t window is 1V. The drain voltage in measurement is 0.7V and the gate voltage is varied.

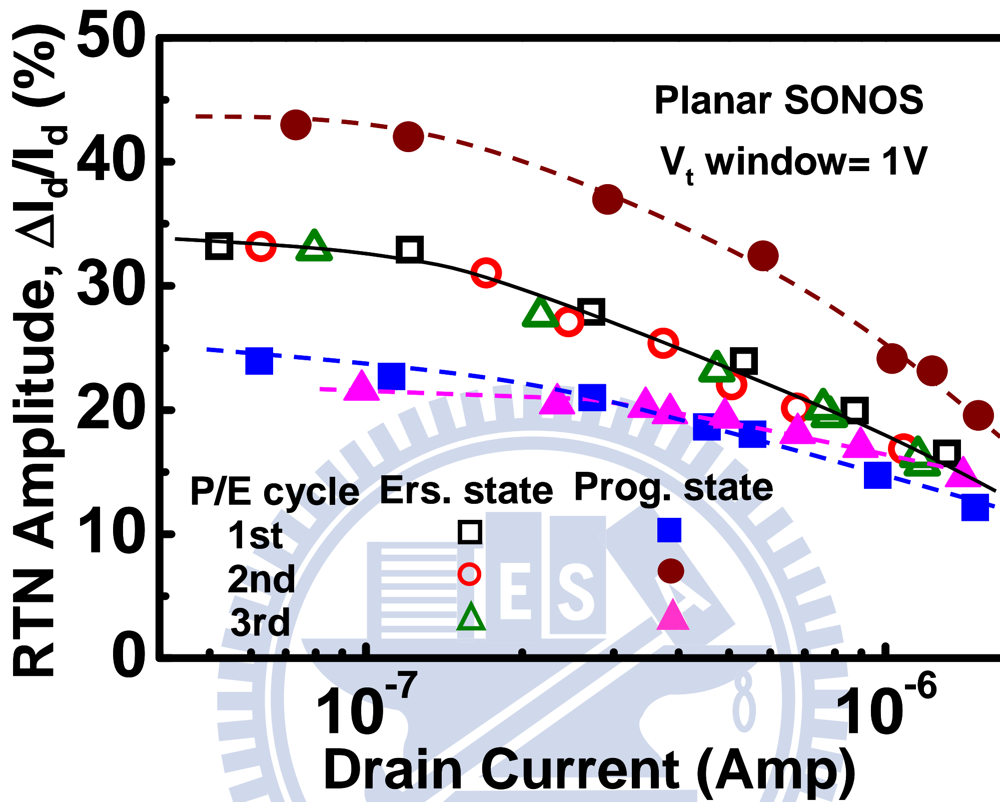


Fig. 3.3 RTN amplitude versus drain current in a SONOS cell in three P/E cycles. The V_t window is 1V. The drain voltage in measurement is 0.7V and the gate voltage is varied.

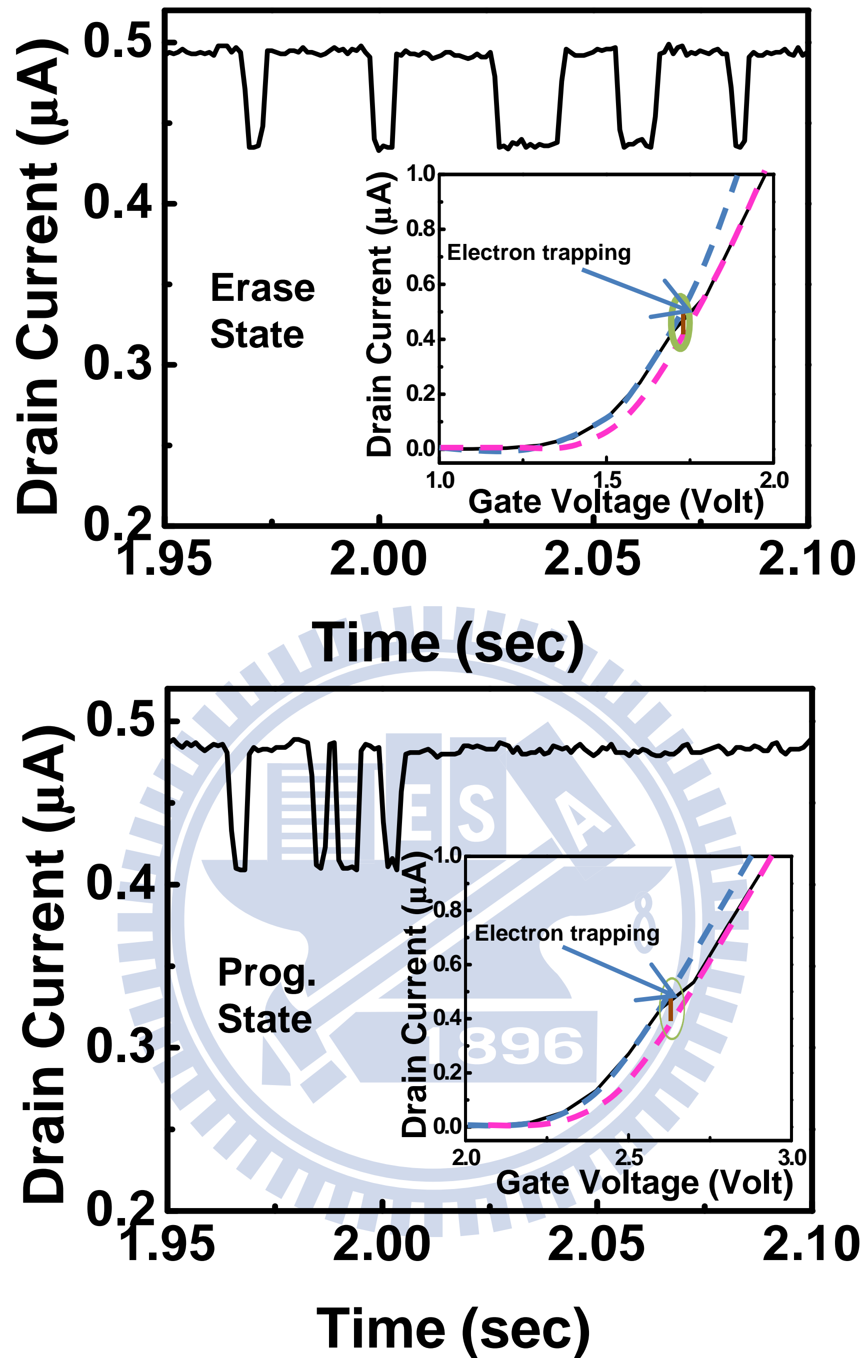


Fig. 3.4 Measured RTN waveform and I_d versus V_g plot (a) in erase-state and (b) in program-state of a SONOS cell. Electron trapping at an interface trap is manifested by a current discontinuity in the I_d-V_g plot

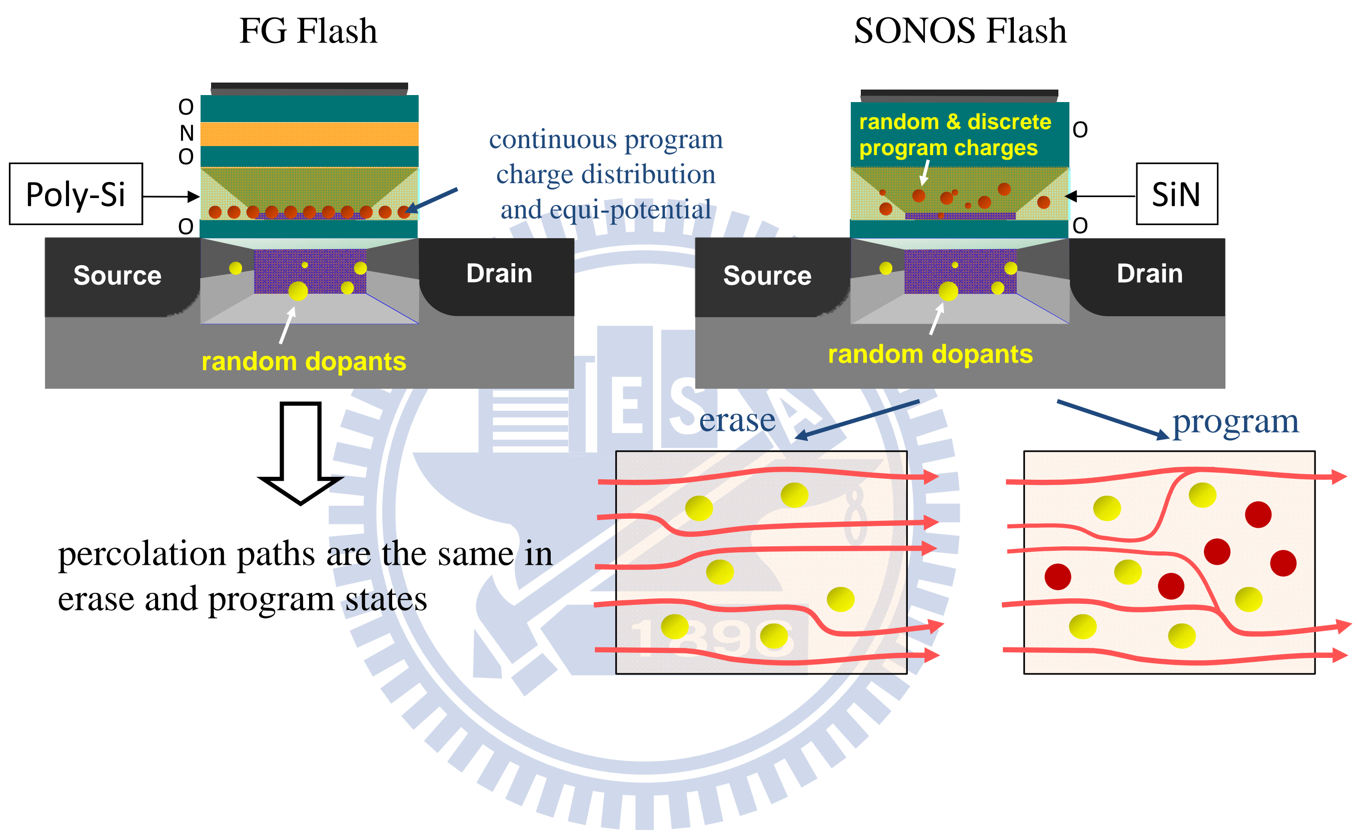


Fig. 3.5 An illustration of two different program charge storage characteristic resulting distinct outcome of percolation path. Continuous distribution in FG flash and random discrete distribution in SONOS flash

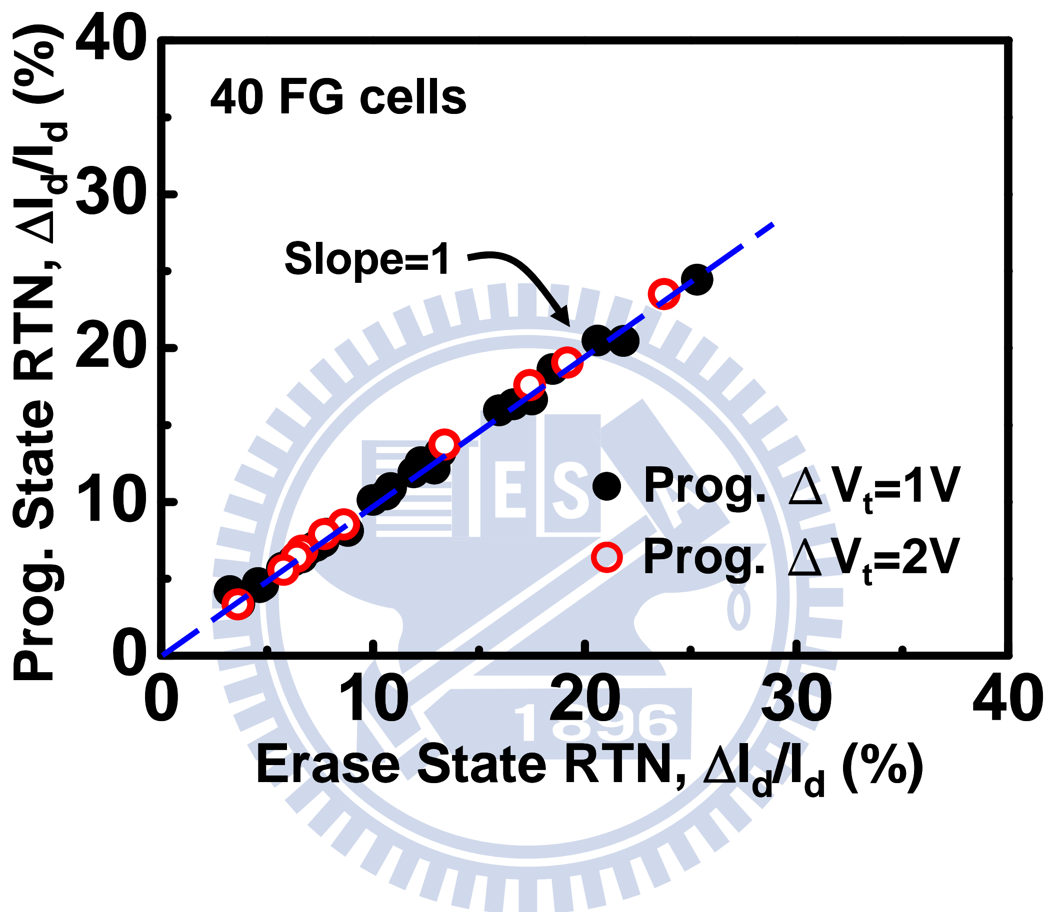


Fig. 3.6 Measured program-state RTN amplitude versus erase-state RTN amplitude in 40 FG flash cells. The RTN amplitude is measured at I_d=500nA @V_d=0.7V. The device dimension is W/L=0.11μm/0.09μm. The program window is 1V or 2V.

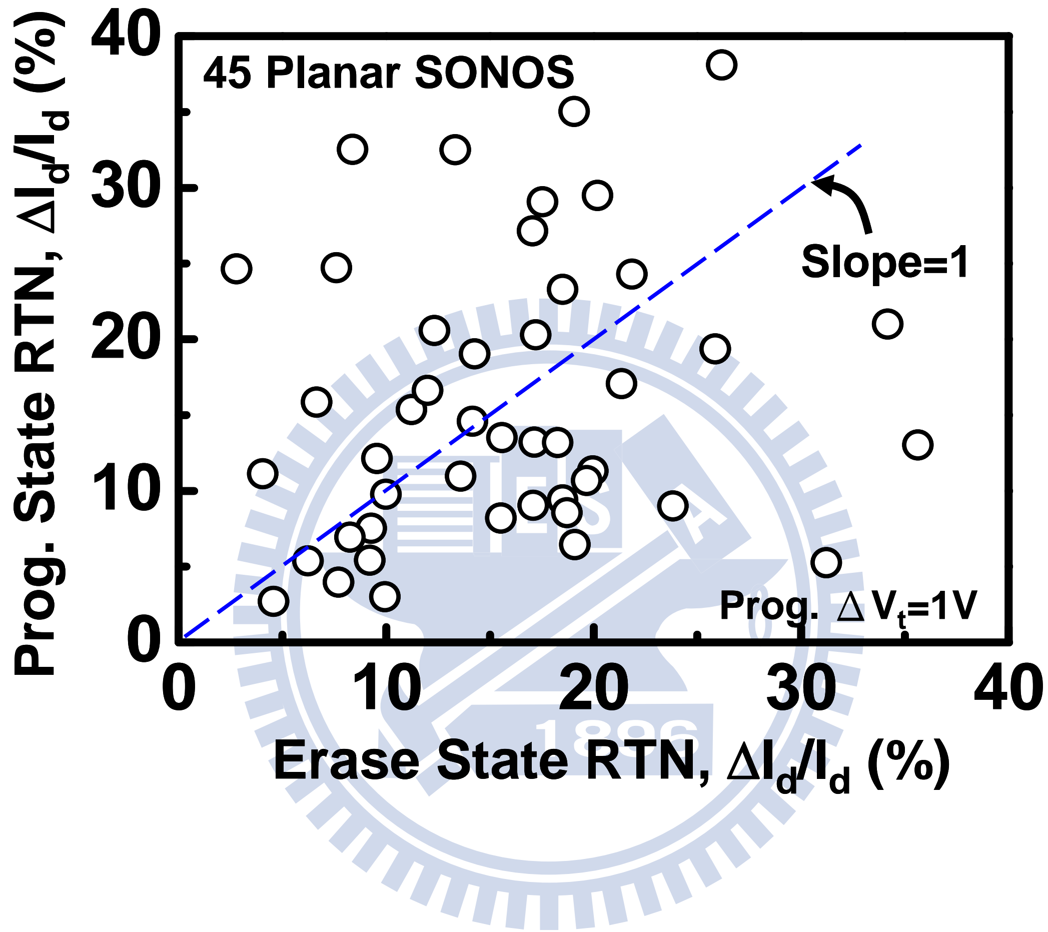


Fig. 3.7 Measured program-state RTN amplitude versus erase-state RTN amplitude in 45 planar SONOS cells. The RTN amplitude is measured at I_d=500nA @V_d=0.7V. The SONOS cells have W/L=0.09μm /0.08μm, a 2.8nm tunnel oxide, a 6nm SiN and a 6nm top oxide.

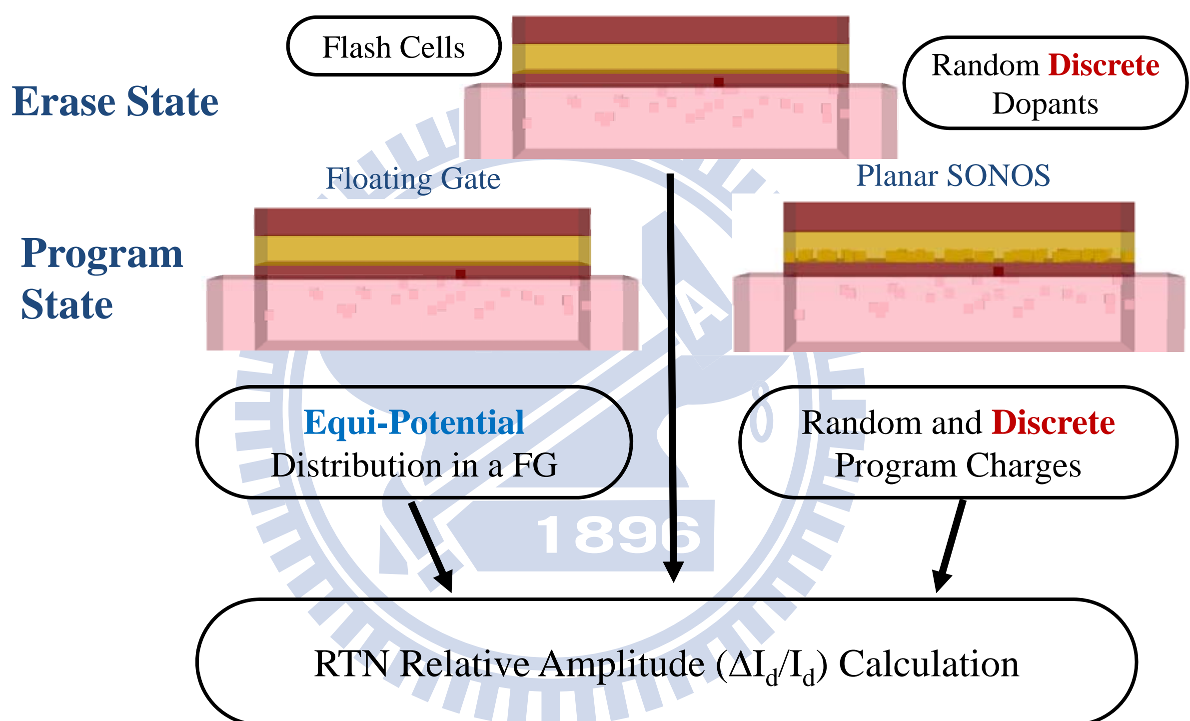


Fig. 3.8 Simulation flowchart of 3D atomistic simulation for RTN amplitude at program state and erase state for FG and SONOS flash.

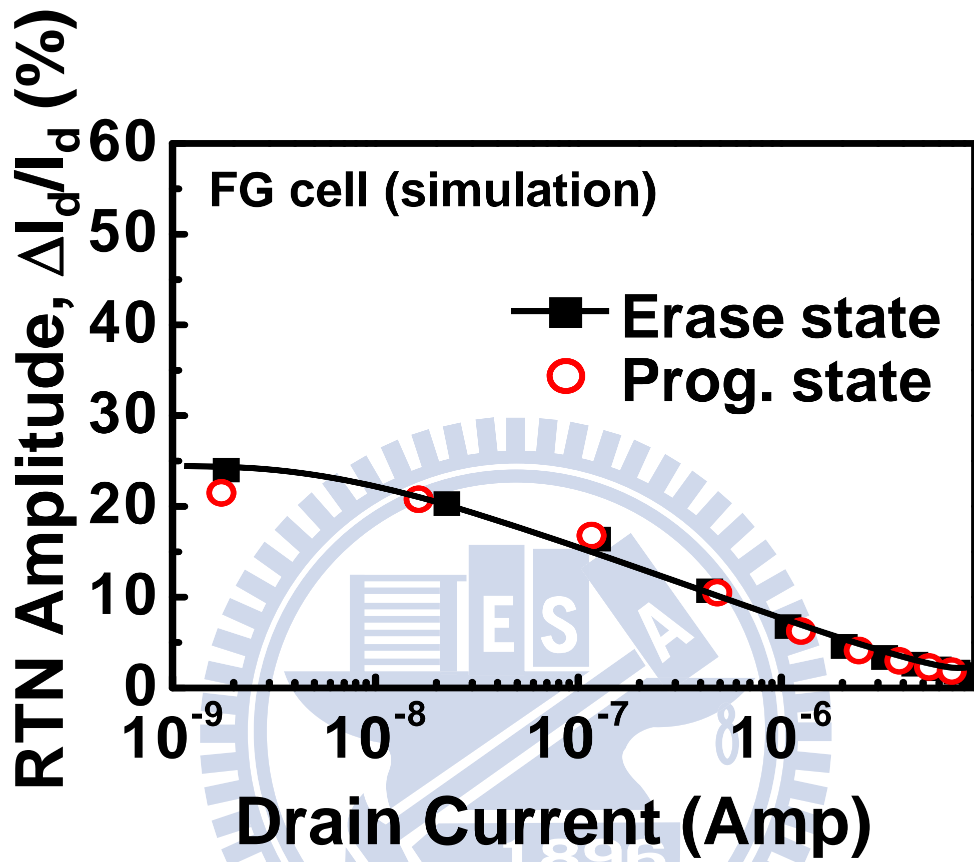


Fig. 3.9 Simulated RTN amplitude versus drain current in a FG flash cell. Program-state and erase-state have the same placement of substrate random dopants. The RTN trap is placed in the middle of the device.

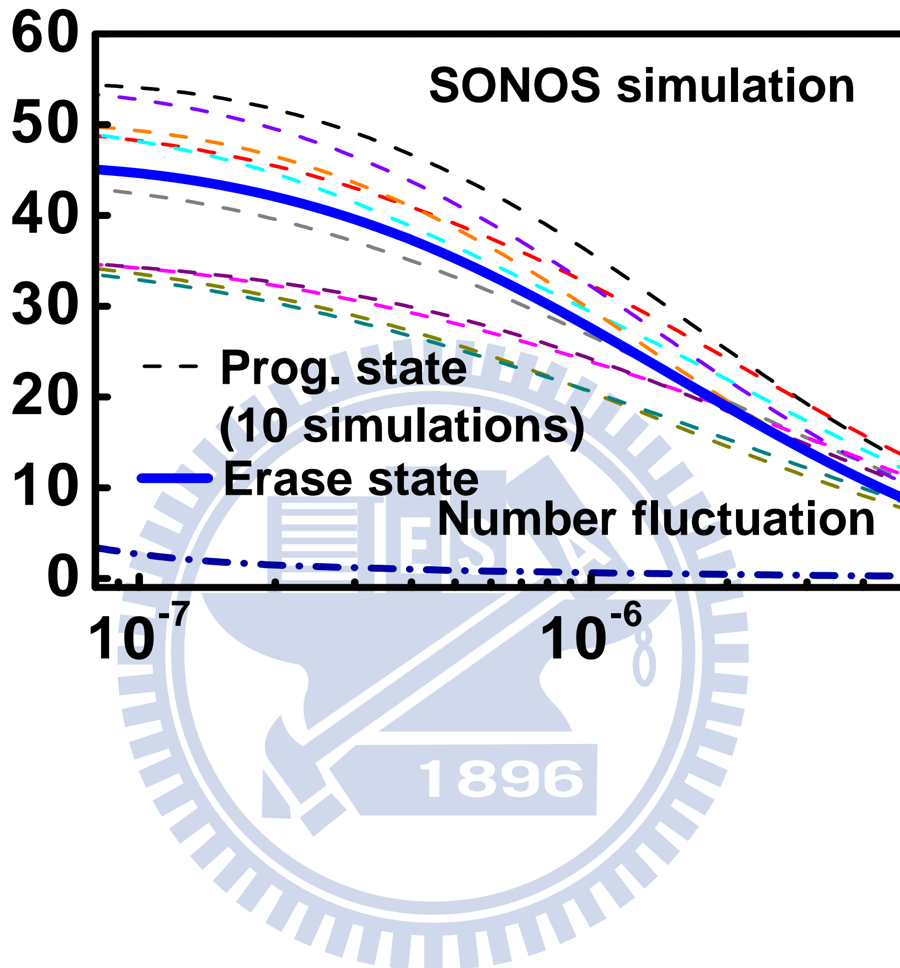


Fig. 3.10 Simulated RTN amplitude versus drain current in a planar SONOS cell. Program-state and erase-state have a fixed placement of substrate dopants. Ten different sets of random program charges are simulated. An RTN amplitude due to number fluctuation is calculated with continuous substrate doping and program charges.

Chapter 4

Charge Retention Loss in a HfO_2 Dot Flash Memory via Thermally Assisted Tunneling

4.1 Preface

Flash memory cells employing discrete charge storage nodes have received much interest for their better cell scalability [4.1]-[4.5]. To improve program/erase (P/E) speed and data retention properties in these cells, a lot of efforts have been made with regard to charge storage media. For instance, various trapping materials have been studied in a SONOS-type flash memory [4.2]. Another category of discrete charge storage flash memories are to use nano-crystals as storage nodes. Many different types of nano-crystals from semiconductors (Si, Ge) to metals (W, Au) have been proposed [4.3, 4.4]. Recently, a HfO_2 dielectric dot flash memory with hot electron program/hot hole erase was presented with superior characteristics in terms of a large memory window, fast P/E speed, and long charge retention time [4.5]. As compared to semiconductor/metal dots, electrons in a dielectric dot are stored in trap states rather than conduction states. Because trapped electrons have a very sharp wave-function distribution in space, size quantization effect is not expected for the programmed electrons in a dielectric dot. In this work, we will explore the charge retention loss mechanism in a HfO_2 dielectric dot cell. We fabricate a large area cell to measure a charge loss induced gate leakage current directly. The temperature and the retention time dependence of the gate leakage current is characterized. In addition, we measure a high-voltage stress induced gate leakage current in a SONOS cell for comparison. A thermally activated tunneling front model is developed for

charge retention loss in a HfO_2 dot flash memory.

In this chapter, the charge loss mechanism in a hafnium oxide (HfO_2) dielectric dot flash memory is investigated. We measure the temperature and time dependence of a charge loss induced gate leakage current in a large area cell directly. We find that (i) the charge loss is through a top oxide in the cell and (ii) the stored charge emission process exhibits an Arrhenius relationship with temperature, as opposed to linear temperature dependence in a SONOS flash memory. A thermally activated tunneling front model is proposed to account for the charge loss behavior in a HfO_2 dot flash memory.

4.2 Device Description and Measurement Setup

The HfO_2 nano-crystal memory used in this work has a 8 nm top oxide, a 10nm intermediate oxide layer with embedded HfO_2 dots, and a 6nm bottom oxide. The dot size is 5-8nm. In order to measure a charge loss induced gate leakage current directly, the device has a dimension of $500\times500\mu m^2$. The fabrication process and device characteristics were published in [4.5]. A Fowler-Nordheim (FN) stress is performed at V_g=-19V for 2000s. Uniform negative FN injection is employed to put electrons into the HfO_2 dots. The program V_t window is 3V. On the other side, a SONOS cell used for comparison has a 9 nm top oxide, a 6 nm silicon nitride, and a 6 nm bottom oxide. The capacitor area is also 500×500 μm^2. Uniform FN programming is performed after a FN stress at V_g=-20V for 2500s.

4.3 Results and Discussions

4.3.1 Gate Leakage in HfO_2 dots memory and SONOS

The program-state gate leakage current versus retention time at different temperatures is shown in Fig. 4.1. Some distinguished features in the gate current of the two cells are observed. First, the gate leakage current is positive in a HfO_2 dot flash (flowing into the gate) but is negative in a SONOS cell (measured result not shown here). The direction of the gate current flow indicates the escape of programmed electrons through a top oxide in the HfO_2 cell. Second, the gate current in both SONOS [4.6] and HfO_2 dot flash cells exhibits 1/t time dependence. The 1/t characteristic can be derived either from a tunneling front model [4.7] or from a Frenkel-Poole (FP) emission model [4.8]. In order to distinguish these two models, we compare the temperature dependence of the gate current in the two cells in Fig. 2. The charge detrapping current in the SONOS cell obeys a linear dependence on temperature, which is expected from the FP emission model, i.e, $I_g \propto kT/t$ [4.8]. The gate leakage current in the HfO_2 cell, however, deviates from a linear relationship apparently. In Fig. 4.3, we replot the temperature dependence of the gate current in the HfO_2 cell in Arrhenius coordinates at t=0.5s and 5s. An Arrhenius relationship is obtained with activation energy of 0.19eV. The Arrhenius dependence excludes the possibility of the FP emission. Instead, the observed temperature and the time dependence in the HfO_2 cell can be well accounted for by thermally activated tunneling through traps in a top oxide.

4.3.2 Thermally Activated Tunneling Front Model

Fig. 4.4 illustrates the stored charge loss process in a HfO_2 cell. Based on the WKB approximation, the tunneling time for an electron from a HfO_2 trap to a top

oxide trap (assumed to be a limiting step in a charge loss process) can be formulated as [4.9, 4.10]

$$t^{-1} = N_t \nu_{th} \sigma_t \exp(-\alpha_{ox} x) \tag{4-1}$$

and

$$\alpha_{ox} = \frac{2\sqrt{2 m_e q \phi_b}}{\hbar}$$

where N_t is the trap density in the top oxide, x is the distance between a HfO_2 trap and a top oxide trap, σ_t is a trap cross-section ,ν_{th} is the thermal velocity, ϕ_b is the barrier height between the SiO_2 and the Si_3N_4 for electrons and other variables have their usual definition. Since we do not observe significant dependence of the gate leakage current on stress time, N_t is suspected to be pre-existing traps. Assuming the stored charges have a uniform distribution in x, we can derive the time and the temperature dependence of the gate current based on a tunneling front model,

$$\begin{aligned} I_g &= A Q_s \exp\left(\frac{-E_a}{kT}\right)\frac{dx}{dt} \\ &= \frac{A Q_s}{\alpha_{ox} t}\exp\left(\frac{-E_a}{kT}\right) \end{aligned} \tag{4-2}$$

where $Q_s \exp(-E_a/kT)$ represents the activated charge density in HfO_2 for tunneling. E_a is the activation energy of trapped charges and A is the cell area.

4.4 Summary

We investigate the charge loss mechanism in a HfO_2 dot flash cell by characterizing a charge loss induced gate leakage current. The Frenkel-Poole emission model is not suitable for charge loss in the cell. A thermally activated tunneling front model is proposed. Our model can well explain the measured temperature and the retention time dependence of a gate leakage current.

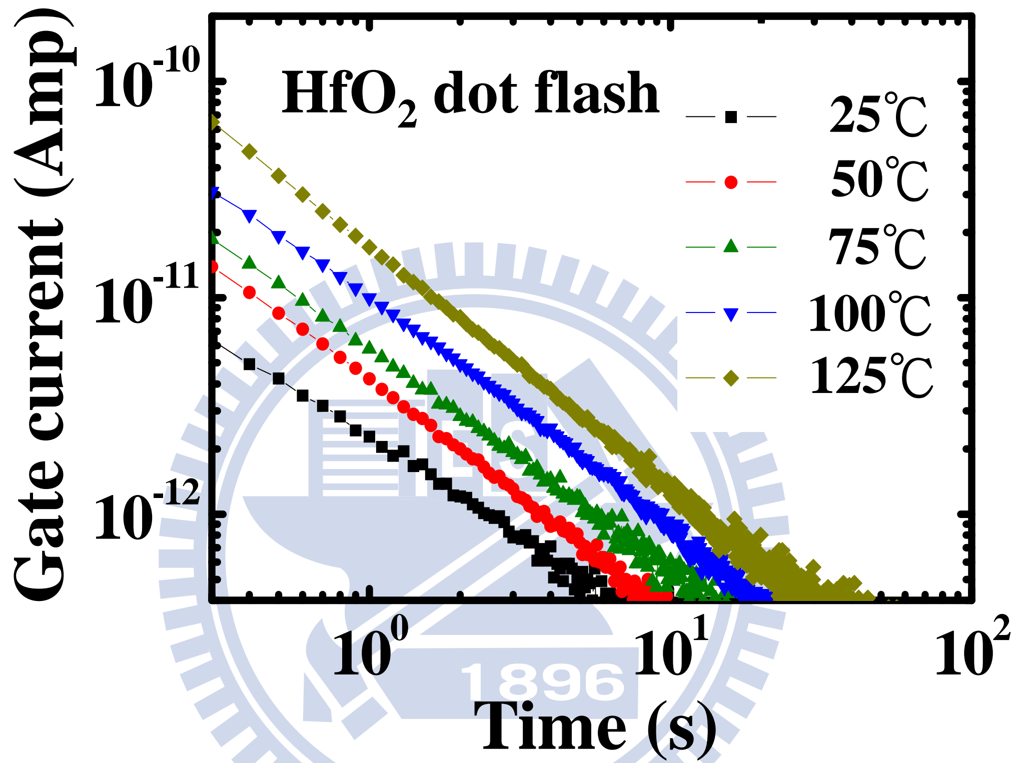


Fig. 4.1 Measured gate leakage current at V_g=0V versus time in a HfO_2 dot flash memory cell (500μmx500μm). The temperature is from 25℃ to 125℃. The device is programmed to a threshold window of 3V.

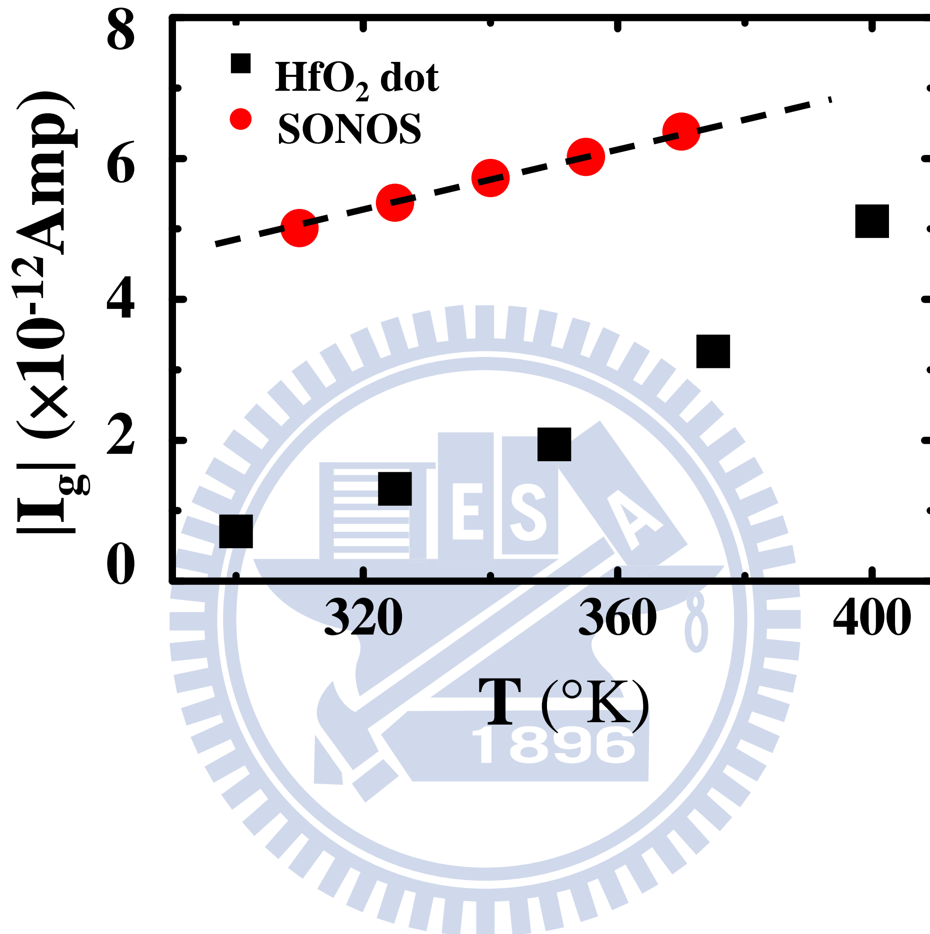


Fig. 4.2 Comparison of temperature dependence of a gate leakage current in a HfO_2 dot flash and in a SONOS flash at t=3s.

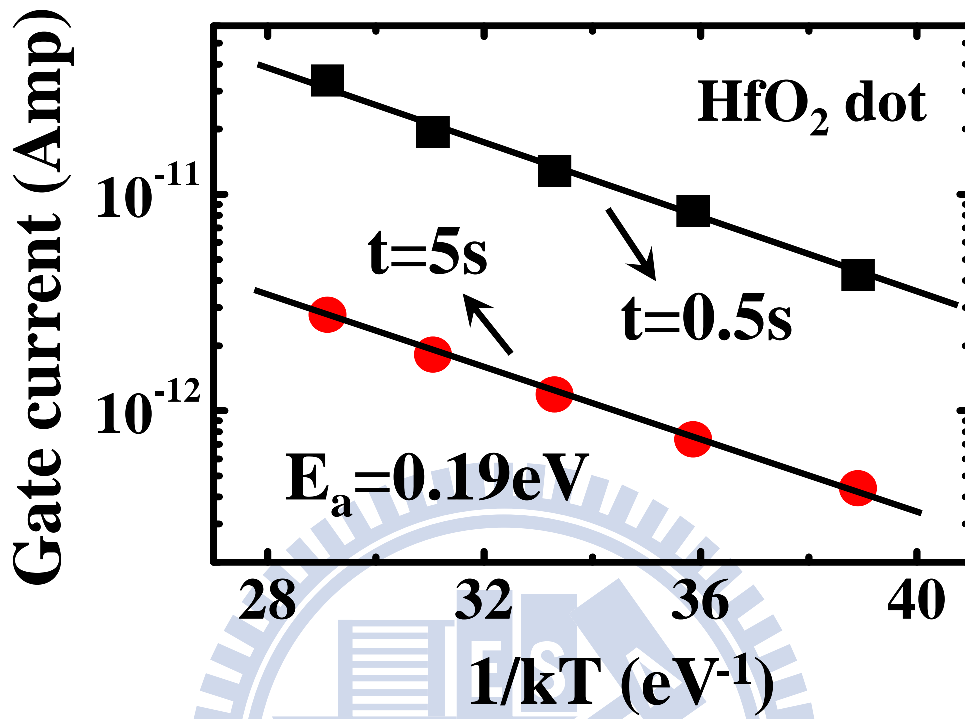


Fig. 4.3 Arrhenius plot of the gate leakage current in a HfO2 dot flash memory. The retention time is 0.5s and 5s. The extracted activation energy is 0.19eV.

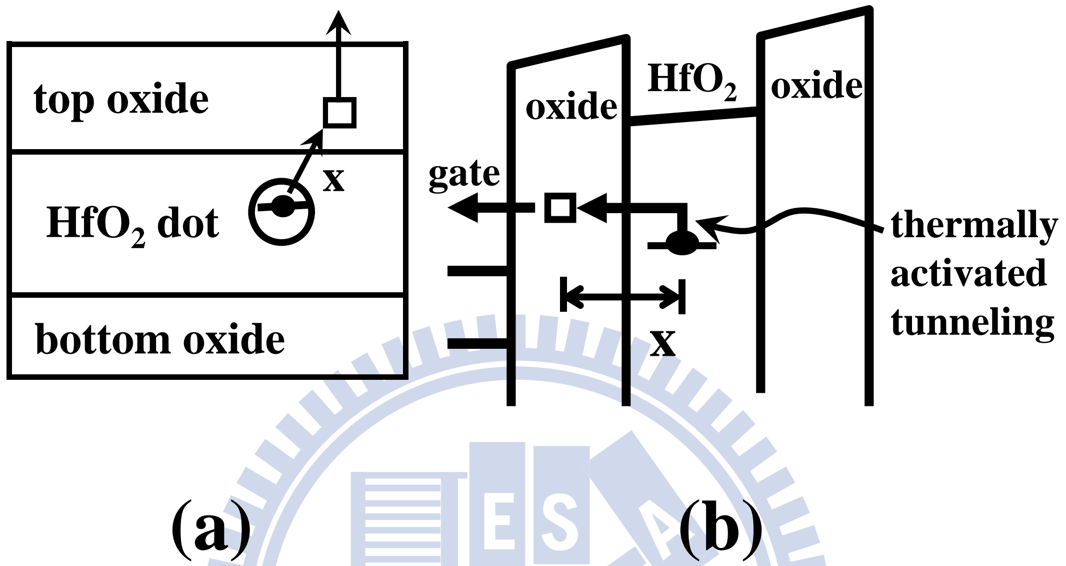


Fig. 4.4 (a) Illustration of charge loss through a top oxide trap in a HfO_2 dot flash. (b) Energy band diagram and thermally assisted tunneling of a trapped charge.

Chapter 5

Study of Post-NBT Stress Current Instability Modes in HfSiON Gate Dielectric pMOSFETs by Measurement of Individual Trapped Charge Emissions

5.1 Preface

Negative bias–temperature (NBT) instability has been recognized as a major reliability concern in ultra-thin gate dielectric pMOSFETs. Recent studies have shown electron trapping in NBTI in SiON and high-k gate dielectric pMOSFETs [5.1-5.4]. In this work, we are focused on post-stress current evolution in HfSiON gate dielectric pMOSFETs due to bipolar charge detrapping. Two post-stress current evolution modes, recovery mode and degradation mode, are observed, depending on a NBT stress condition. A physical model based on bipolar charge trapping/detrapping is proposed to explain the observed instability modes. A small area device is used to measure individual trapped electron and hole emissions directly. A fast transient measurement technique is employed to characterize charge emission times. The description of the measurement setup can be found in [5.5], [5.6].

In this work, bipolar charge detrapping induced current instability in HfSiON gate dielectric pMOSFETs after negative bias and temperature stress is studied by using a fast transient measurement technique. Both single electron and single hole emissions are observed, leading to post-stress current degradation and recovery, respectively. The NBT stress voltage and temperature effect on post-stress current

evolution is explored. Clear evidence of electron and hole trapping in NBT stress is demonstrated. A bipolar charge trapping/detrapping model and charge detrapping paths based on measured charge emission times are proposed.

5.2 Device Description and Measurement Setup

The devices used here are p-type MOSFETs with a poly-silicon electrode and a HfSiON-SiO_2 gate stack. The transistors have an effective oxide thickness (EOT) of 1.7nm, a gate length of 0.08~10μm, and a gate width of 0.16~100μm. NBT stress at V_g=-2.0V to -3.2V is performed. The linear drain current is measured at V_d=-0.2V and V_g=-0.7V to -1.2V. The voltage waveforms in NBT stress phase and in measurement (relaxation) phase are depicted in Fig. 5.1.

5.3 Results and Discussions

5.3.1 Evidence of Holes and Electrons Detrapping in Post-NBT Stress Current

The drain current evolution after NBT stress at V_g =-3.0V is shown in Fig. 5.2. In a small area device (Fig. 5.2(a)), single-electron detrapping and single-hole detrapping are both observed, which are manifested by a step-like decrease and increase in the drain current. The pre-stress drain current is also plotted as a reference. In a large area device (Fig. 5.2(b)), the bipolar charge detrapping is exhibited by a turn-around characteristic of the post-stress current versus measurement time. Notably, trapped electron emission usually has shorter detrapping times and thus one may fail to observe it in a conventional NBT measurement setup using Agilent 4156 due to a switching delay. Our findings here are different from the result in a SiON pMOSFET in Ref. [5.3] that hole detrapping is

faster than electron detrapping.

5.3.2 Stress V_g and temperature effect on Post-NBT Current Instability

Hole trapping is usually observed in NBT stress in pMOSFET's, but electron trapping is strongly affected by stress voltage and temperature. Fig. 5.3 shows the NBT induced ΔI_d versus stress time at different stress V_g. The stress V_g ranges from -1.6V (result not shown here) to -2.8V. ΔI_d was taken immediately after stress. At a large stress V_g, ΔI_d initially increases with stress time and then decreases, featuring a turn-around characteristic in Fig. 5.3. The transition time for the ΔI_d changing from enhancement mode to degradation mode is mostly within seconds in the bias range of interest. This feature provides evidence of electron trapping in the stress. In contrast, at a smaller stress V_g (for example, -2V), ΔI_d decreases monotonically with stress time, indicating that holes are the dominant injected charges.

In Fig. 5.4, we monitor the current evolution after a low V_g (-2V) stress. Unlike Fig. 5.2 (a high V_g stress), the post-stress current exhibits a recovery mode and only hole detrapping is found. The stress V_g dependence can be explained by the fluence of injected carriers during stress. Fig. 5.5 shows the band diagram and carrier flows in a high-k pMOSFET under -V_g stressing. We use a charge separation technique to measure the electron stress current (I_e) and the hole stress current (I_h) respectively (Fig. 5.6). The electron stress current increases drastically with $|V_g|$ and exceeds the hole stress current at a high stress $|V_g|$, thus explaining a large electron rate at a high stress $|V_g|$.

In addition to a high stress voltage, a high stress temperature also favors electron trapping. Fig. 5.6(b) shows the electron and hole stress currents at an

elevated temperature (T=100°C). Note that, as compared to the hole stress current, the electron stress current is enhanced to a larger extent at a higher temperature (Fig. 5.6). As a result, electron trapping is more sensitive to temperature than hole trapping. Fig. 5.7 shows the post-stress current evolution in a large area device for two different stress temperatures, T=25°C and 80°C. The stress V_g is -2.2V. The electron detrapping phenomenon (turn-around behavior) is obtained only at a higher stress temperature.

5.3.3 Measurement V_g Dependence on Post-NBT Current Instability

The electron and hole detrapping paths can be inferred from the dependence of their emission times on measurement V_g. Two measurement V_g, -0.85V and -1V, are used in Fig. 5.8. A high stress V_g of -3.2V is chosen to ensure electron trapping and hole trapping during NBT stress.

Typical post-stress current evolution patterns are shown in Fig. 5.8. In Fig. 5.9, we plot the electron and hole detrapping times ($<\tau_e>$ and $<\tau_h>$) versus measurement V_g. For simplicity, we only record the longest τ_e and the shortest τ_h. The ten measurements of the τ_e and the τ_h at each V_g in the same device were repeated by charge re-filling to take an average. The charge re-filling has the same voltage as NBT stress, but has a much shorter re-filling time (0.1sec). It is believed that no additional traps are created by the re-filling. Both electron and hole emission times increase with measurement $|V_g|$. Since a negative Vg exerts a repulsive force on a negative trapped charge, the positive dependence of the τ_e on $|V_g|$ implies trapped electron emission to the gate. Likewise, the positive dependence of the τ_h on $|V_g|$ suggests trapped hole emission to the substrate.

5.3.4 Bipolar Charge Detrapping Model

The energy band diagram and charge detraping paths in relaxation are drawn in Fig. 5.10. Thermally assisted tunneling for trapped charge emission is adopted [5.5]. The activation energy of trapped charges can be extracted from an Arrhenius plot of the τ_e and τ_h versus temperature (Fig. 5.11). The extracted activation energy is 0.20eV for trapped electrons and 0.14eV for trapped holes.

5.4 Summary

Post-NBT stress current instability due to electron detrapping and hole detrapping in a high-k gate dielectric pMOSFET has been explored. Post-stress current recovery and degradation modes are observed. Our study shows that electron trapping is more likely to occur as NBT stress voltage and temperature increase. The presence of electron trapping complicates the modeling and characterization of NBTI. In order to extrapolate a reliable NBTI lifetime, electron trapping effects should be carefully considered in voltage/temperature accelerated stress.

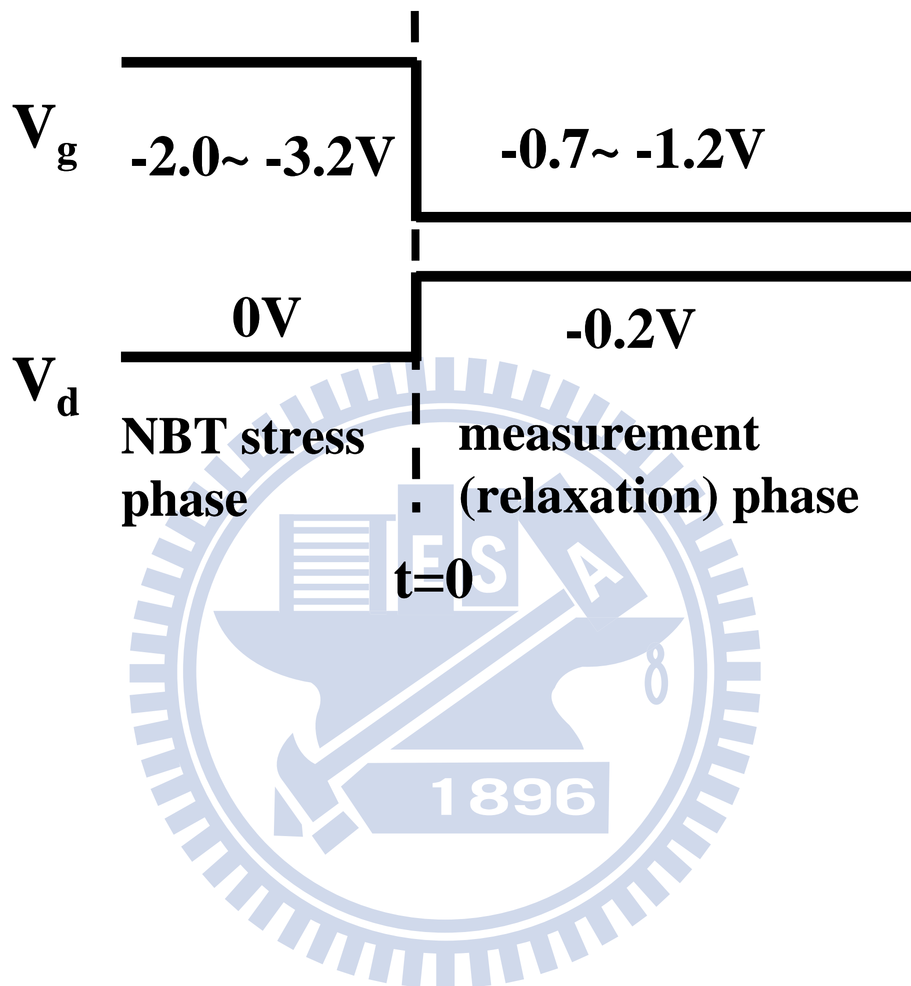


Fig. 5.1 Voltage waveforms applied to the gate and the drain during NBT stress and measurement (relaxation) phases. A high-speed electronic switch is used to minimize a delay between stress and measurement.

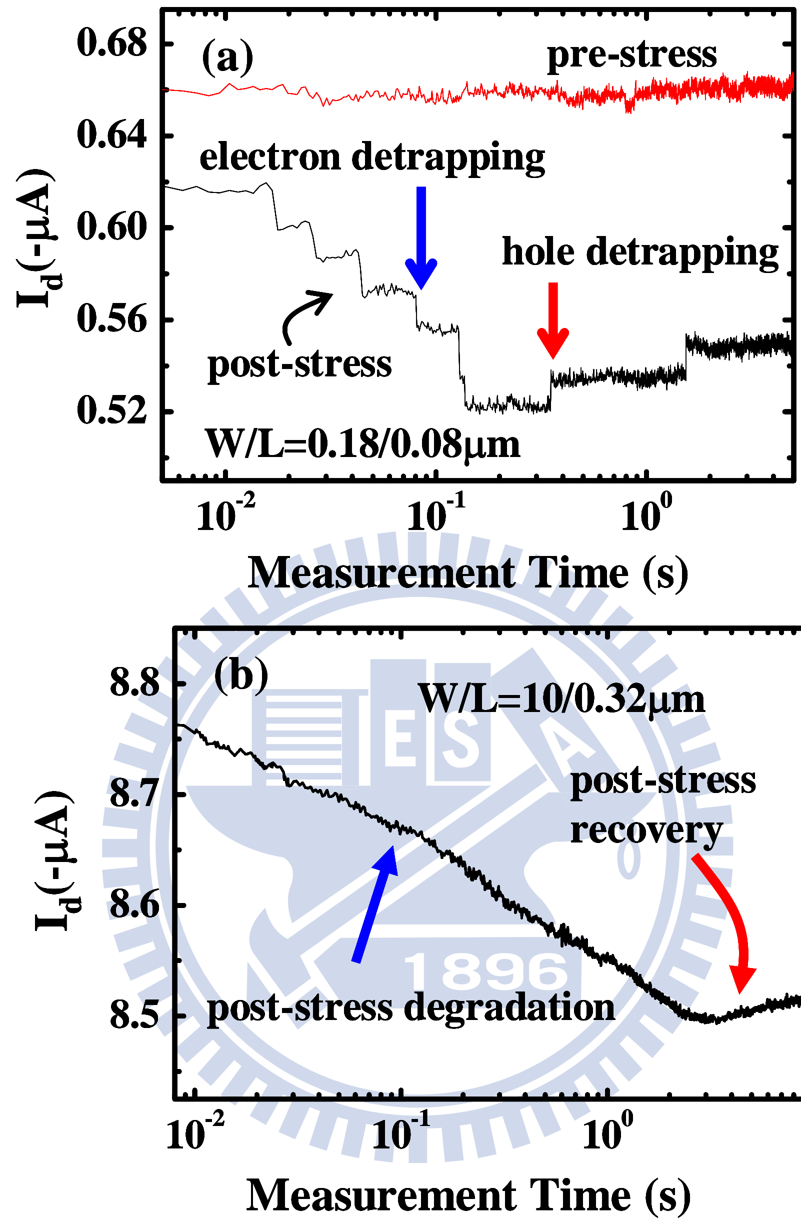


Fig. 5.2 Post-stress current evolution with measurement (relaxation) time in (a) a small area device (W/L=0.18/0.08μm) and (b) a large area device (W/L=10/0.32μm). The NBT stress voltage is -3.0V. The measurement voltages are V_g/V_d=-1.2V/-0.2V and temperature is 25°C. The pre-stress current is shown in (a) for comparison. Both current degradation and recovery are obtained in the measurement period.

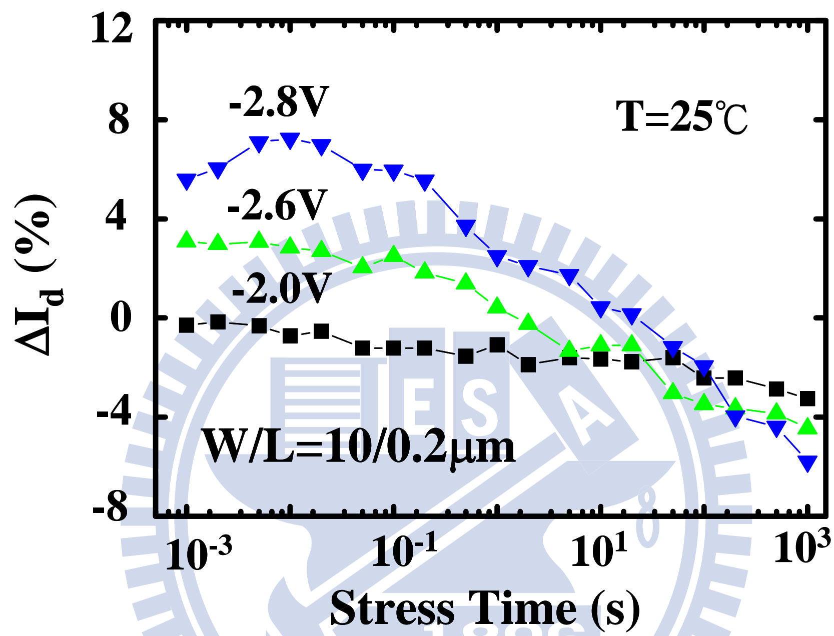


Fig. 5.3 Linear drain current change versus NBT stress time. ΔI_d is measured immediately after stress. Three stress voltages, V_g =-2.8V, -2.6V and -2.0V are applied. Electron trapping into pre-existing high-k traps is demonstrated by a positive ΔI_d at a high stress $|V_g|$.

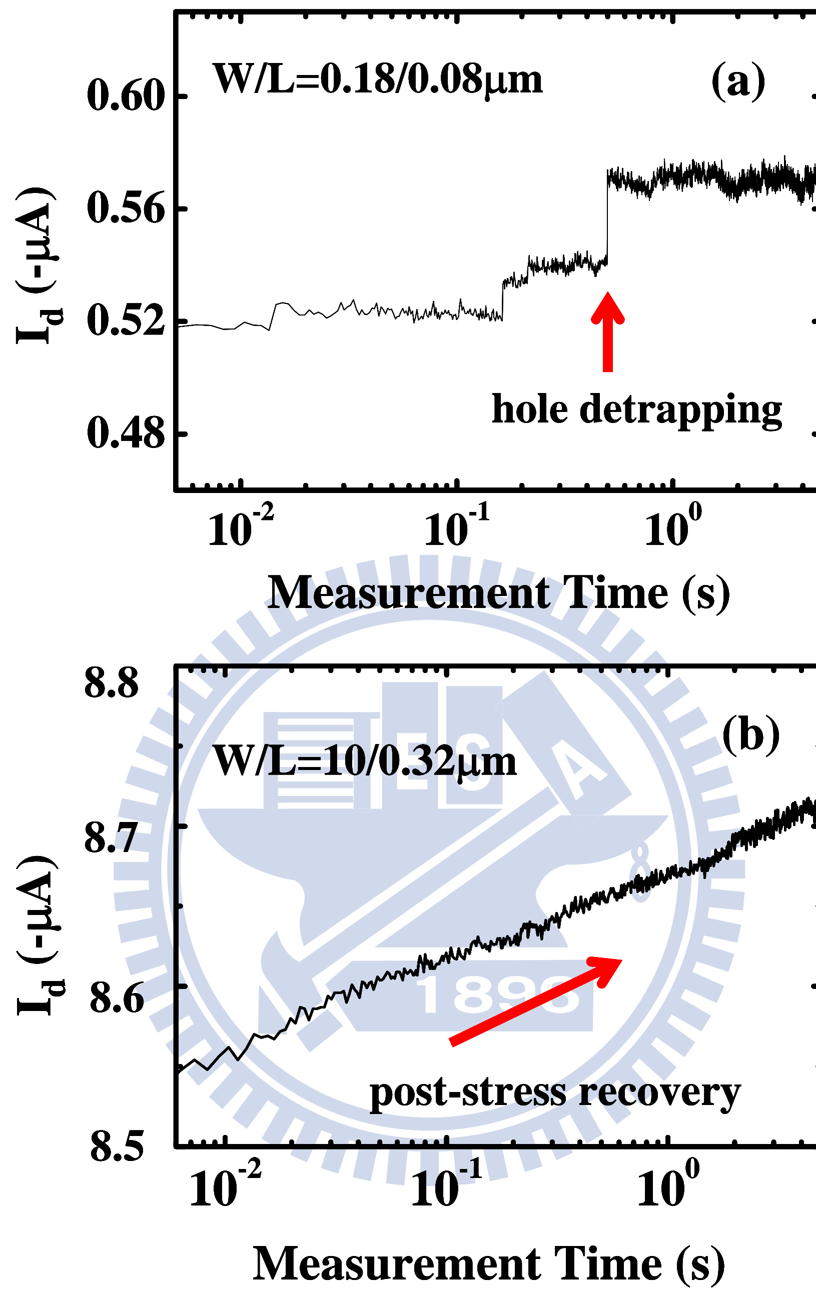


Fig. 5.4 Drain current evolution after a low V_g (=-2V) stress in (a) a small area device and (b) a large area device. Only hole detrapping are found at a low stress V_g. The measurement voltages are V_g/V_d=-1.2V/-0.2V and temperature is 25°C.

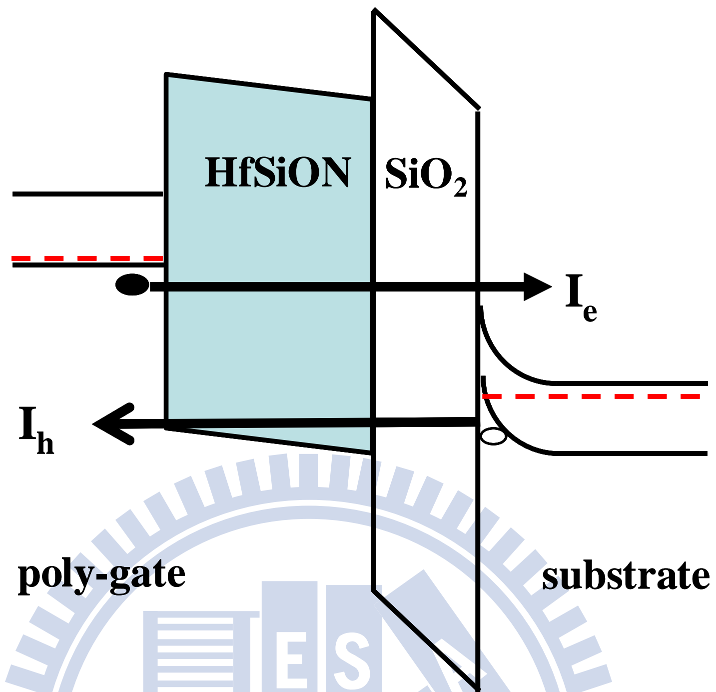


Fig. 5.5 Illustration of a band diagram and carrier flows in a high-k pMOSFET under -V_g stressing. In a charge separation measurement, the electron stress current (I_e) flows from the substrate to the gate and the hole stress current (I_h) flows from the source/drain to the gate.

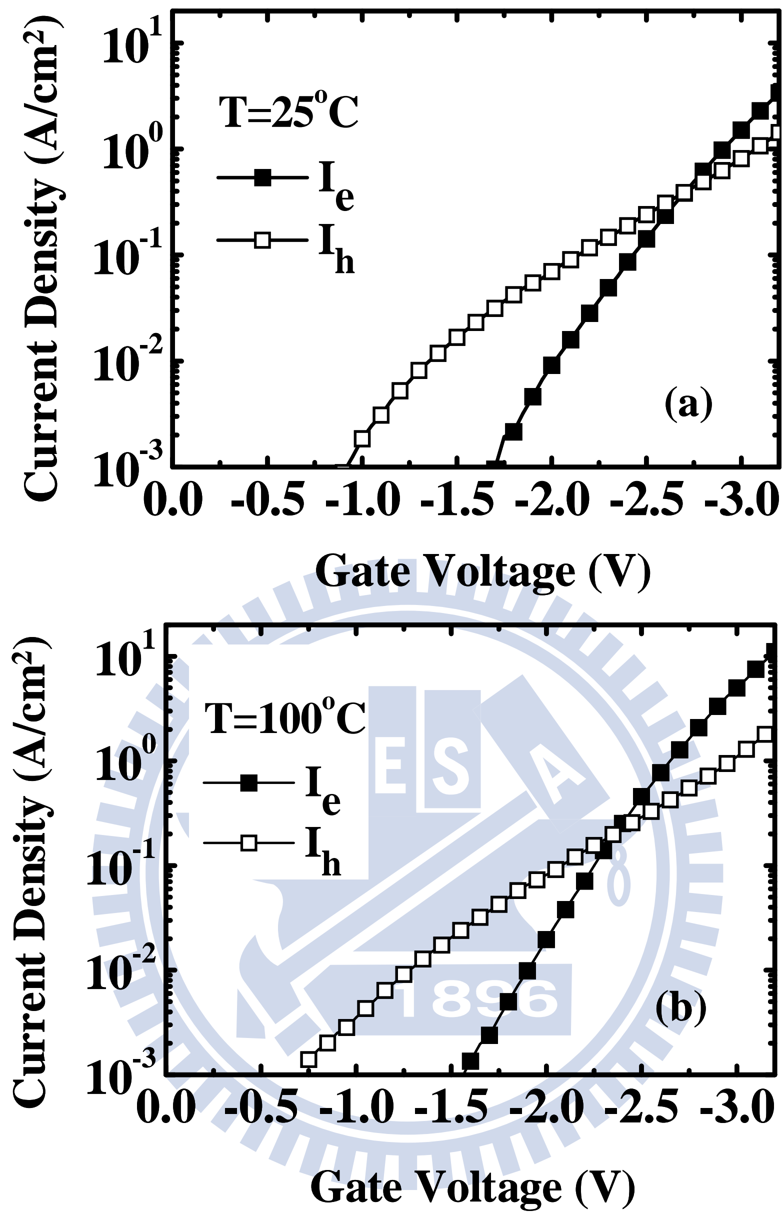


Fig. 5.6 Stress voltage dependence of electron injection current (I_e) and hole injection current (I_h). A charge separation technique is used to measure I_e and I_h. (a) T= 25°C and (b) T= 100°C.

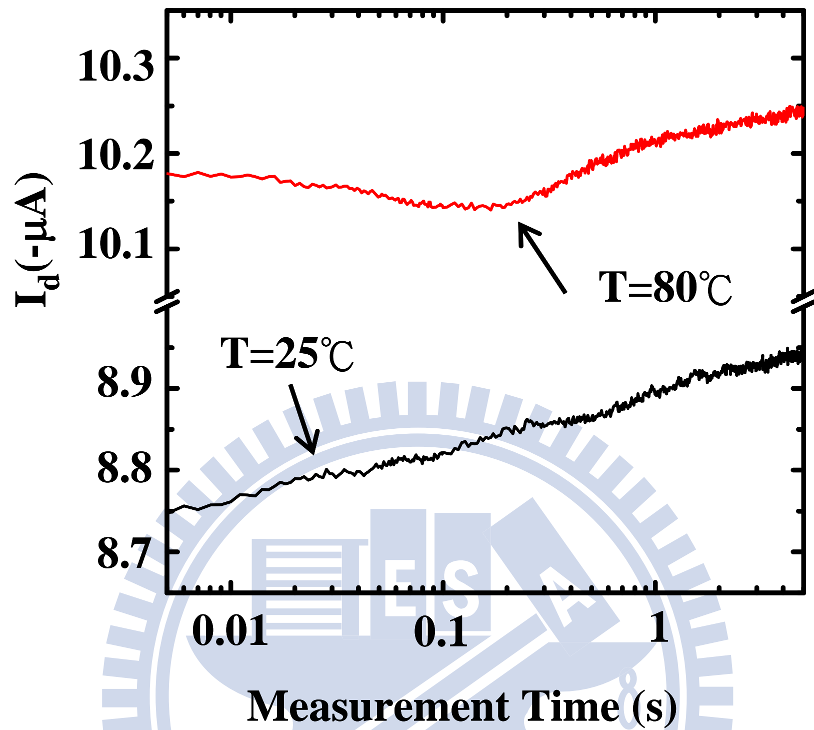


Fig. 5.7 Post-stress current evolutions with measurement time for two different stress temperatures, T= 25°C and 80°C. The stress voltage is -2.2V. The turn-around characteristic is observed only at T= 80°C. Note that the Id measurement is biased in subthreshold region that Id is larger at a higher temperature.

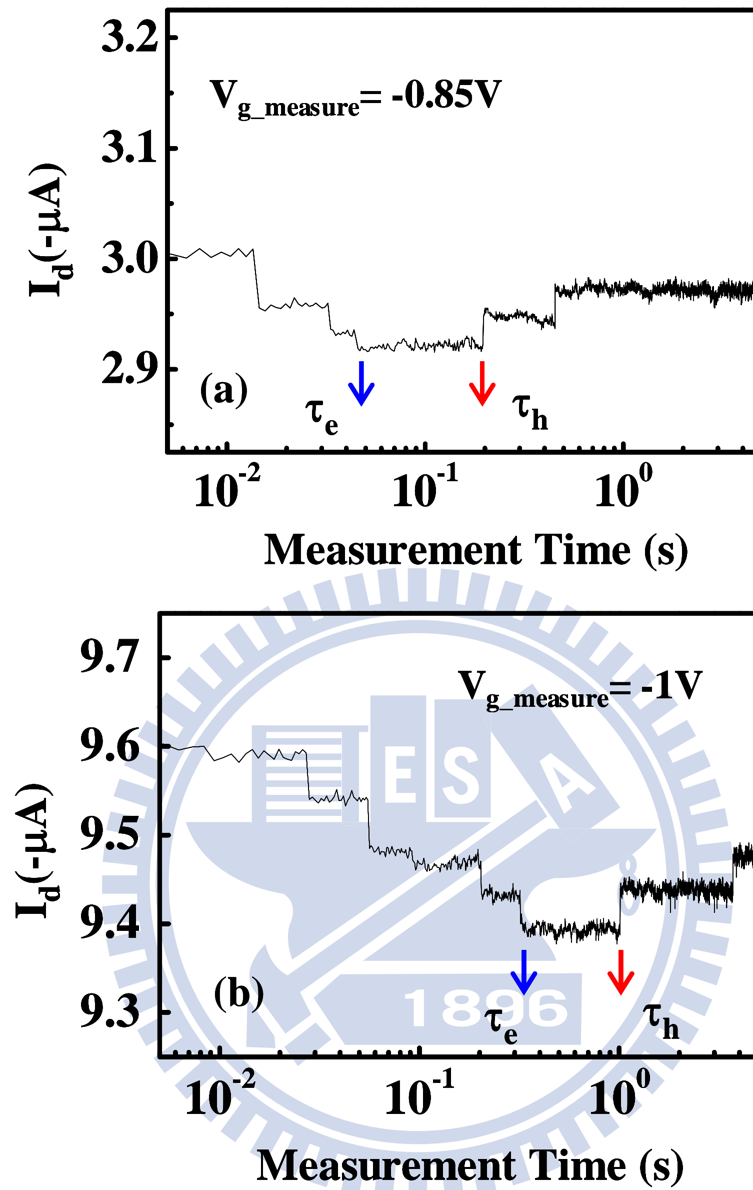


Fig. 5.8 Typical post-stress current evolution patterns. (a) measurement V_g=-0.85V and (b) V_g=-1.0V. The longest electron detrapping time (τ_e) and the shortest hole detrapping time (τ_h) are indicated. The trend is that both τ_e and τ_h increase with measurement $|V_g|$.

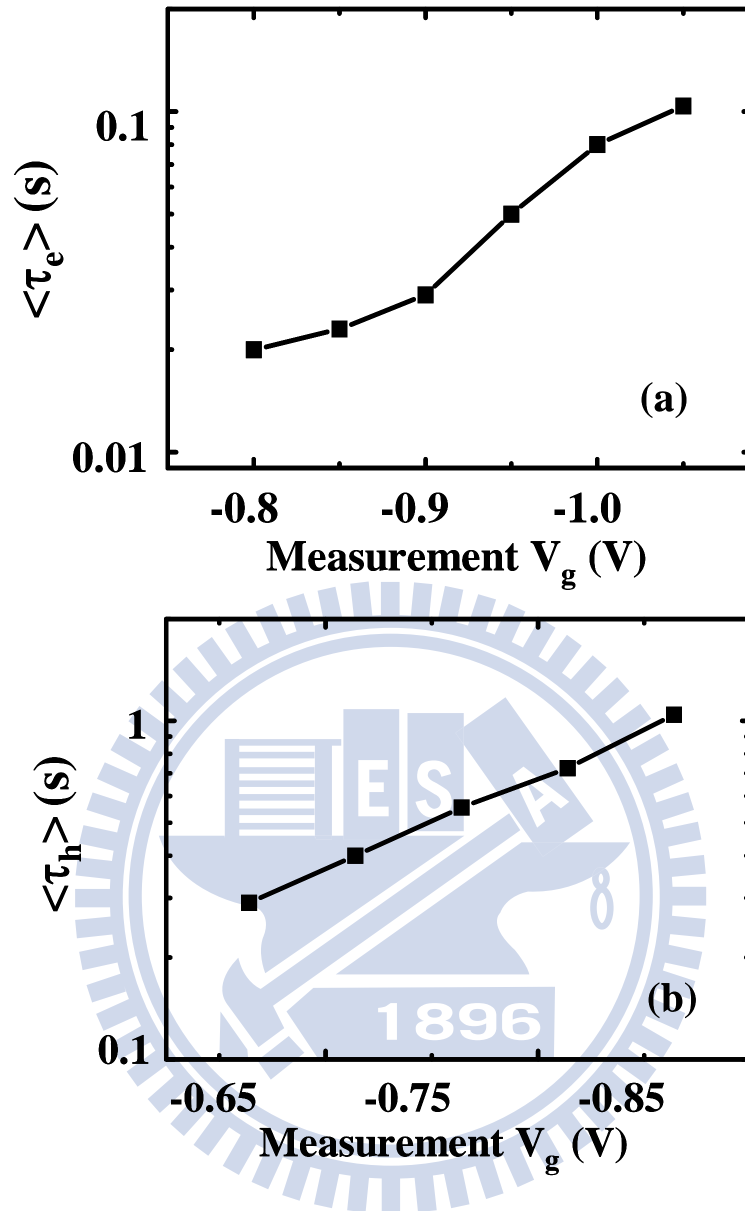


Fig. 5.9 Average τ_e and τ_h are plotted against measurement V_g. We repeated measurement of each data point ten times by charge re-filling to take an average. Only the longest electron detrapping time and the shortest hole detrapping time (as shown in Fig. 8) are plotted in the figure.

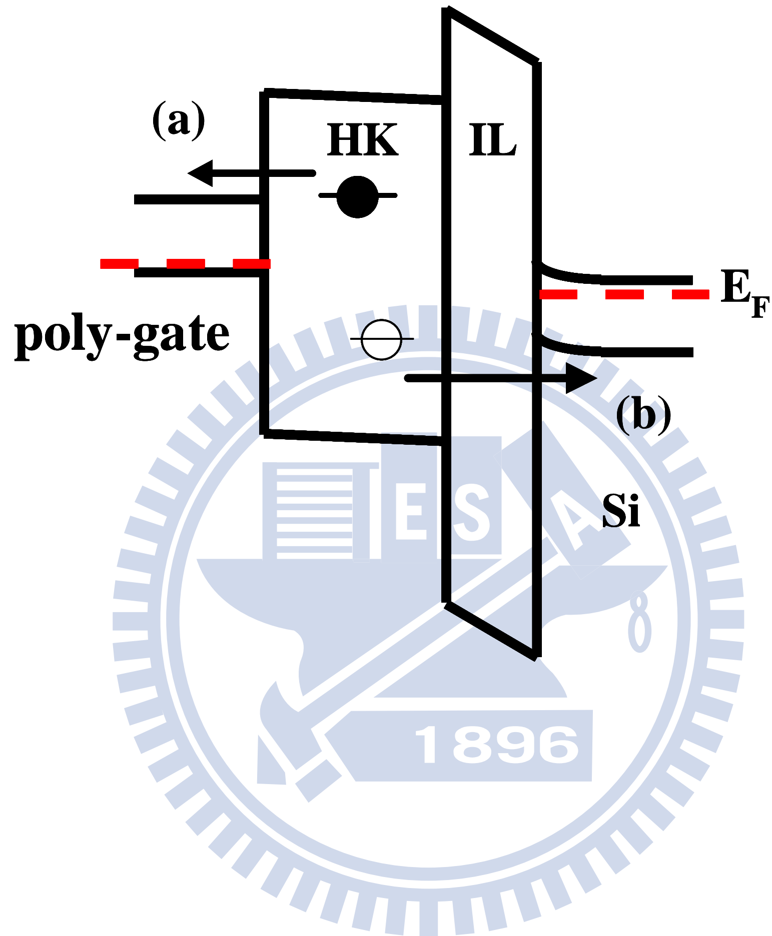


Fig. 5.10 Illustration of the energy band diagram in relaxation phase. (a) Trapped electron emission to the gate, and (b) trapped hole emission to the substrate.

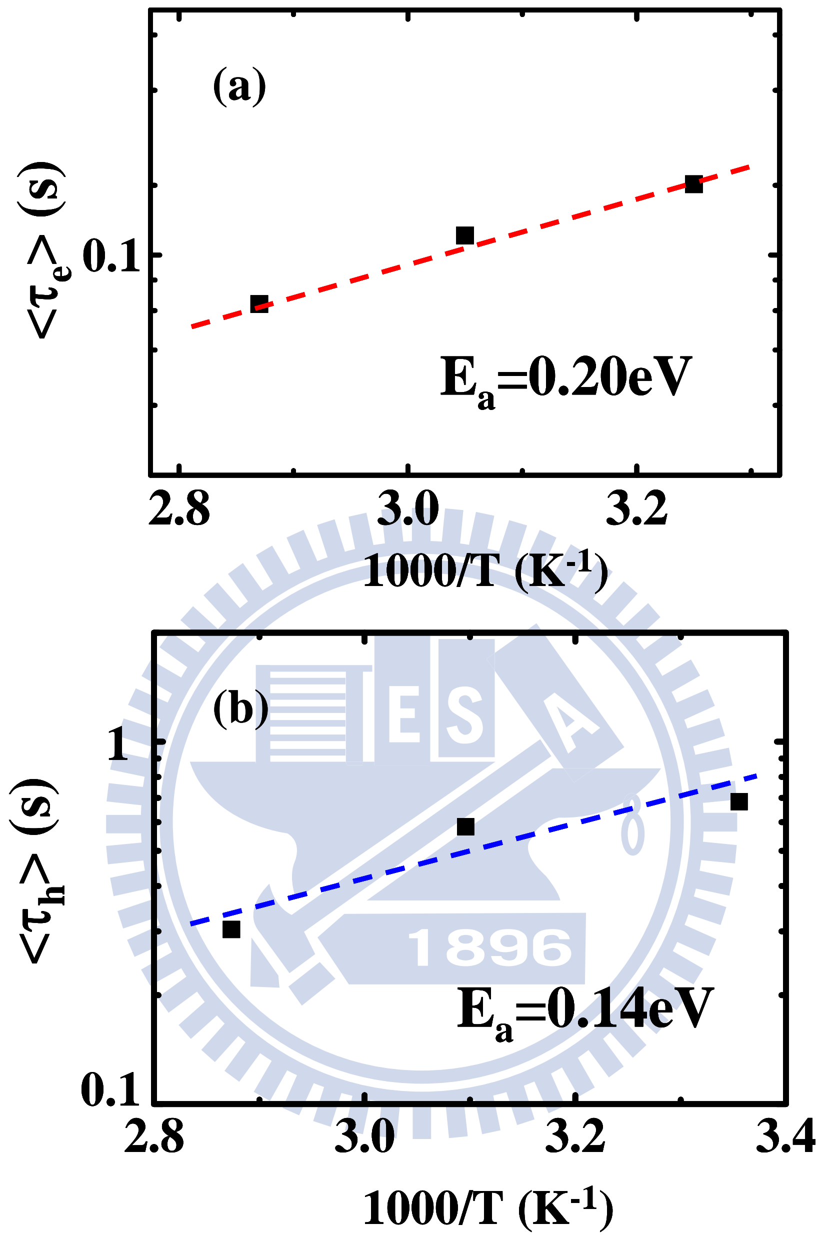


Fig. 5.11 Arrhenius plot of the τ_e and τ_h versus temperature (a) trapped electrons and (b) trapped holes. The extracted activation energy is 0.2eV for electrons and 0.14eV for holes.

Chapter 6

Conclusions

In short, this dissertation has involved the reliability issues in high-k gate dielectric pMOSFETs and charge trapping storage Flash memory. The subjects that have been comprehensively discussed including the post-NBTI behavior in high-k pMOSFETs, a novel RTS-based technique to characterize injected charge in SONOS flash cell, program charge effect on RTN amplitude in a flash cell, and retention mechanism in HfO_2 dot flash memory. Contributions of each subject in this work are summarized as follows.

First, post-NBT stress current instability due to electron detrapping and hole detrapping in a high-k gate dielectric pMOSFET has been explored. Post-stress current recovery and degradation modes are observed. Our study shows that electron trapping is more likely to occur as NBT stress voltage and temperature increase. The presence of electron trapping complicates the modeling and characterization of NBTI. In order to extrapolate a reliable NBTI lifetime, electron trapping effects should be carefully considered in voltage/temperature accelerated stress.

Next, a novel RTS method is proposed to characterize program and erase charge lateral spread in a SONOS flash memory without the need to know a doping profile. In the RTS method, the τ_c/τ_e is very sensitive to program/erase/retention charges. It exhibits an exponential dependence on a local potential, as compared to a linear dependence in the CP method. The RTS method can provide a better resolution than

a charge pumping method or an inverse I-V modeling approach. A mismatch between program electrons and erase holes is shown by this method. Read current instability due to nitride charge vertical loss and random telegraph noise is directly observed.

Read failure due to a large amplitude RTN tail is an urgent issue in flash memory scaling. Random program charge effects in a planar SONOS cell on RTN have been characterized and simulated. In a FG cell, the RTN tail is mainly attributed to random substrate dopants while in a SONOS cell the percolation path and thus the amplitude of RTN are determined by both substrate dopants and program charges. Our simulation shows that random program charges have a large effect on RTN. This effect has to be considered in RTN modeling in a program state of a MLC SONOS.

Finally, the charge loss mechanism in a HfO_2 dot flash cell is investigated by characterizing a charge loss induced gate leakage current. The Frenkel-Poole emission model is not suitable for charge loss in the cell. A thermally activated tunneling front model is proposed. Our model can well explain the measured temperature and the retention time dependence of a gate leakage current.

References

Chapter 1

[1.1] C. Shen, M. F. Li, X.P. Wang, H. Y. Yu, Y. P. Feng, A. T.-L. Lim, Y. C. Yeo, D.S.H. Chan, and D. L. Kwong, "Negative U traps in HfO2 gate dielectrics and frequency dependence of dynamic BTI in MOSFETs," *IEDM Tech. Dig.*, pp.733-736, 2004

[1.2] S. Rangan, N. Mielke, and E. C. C. Yeh, "Universal recovery behavior of negative bias temperature instability," *IEDM Tech. Dig.*, pp. 341-344, 2003

[1.3] M. Denias, A. Bravaix, V. Huard, C. Parthasarathy, G. Ribes, F. Perrier, Y. Rey-Tauriac, and N. Revil, "On-the-fly characterization of NBTI in ulra-thin gate oxide pMOSFET's," *IEDM Tech. Dig.*, pp.109-112, 2004

[1.4] R. Degraeve, A. Kerber, P. Roussell, E. Cartier, T. Kauerauf, L. Pantisano, and G. Groseneken, "Effect of bulk trap density on HfO_2 reliability and yield," *IEDM Tech. Dig.* ,pp. 935-938, 2003

[1.5] V. Huard and M. Denias, "Hole trapping effect on methodology for DC and AC negative bias temperature instability measurements in pMOS transistors," *Proc. Int. Reliab. Phys. Symp.*, pp. 40-45, 2004

[1.6] T. Yang, M. F. Li, C. Shen, C. H. Ang, C. Zhu, Y. C. Yeo, G. Samudra, S. C. Rustagi, M. B. Yu, and D. L. Kwong, "Fast and slow dynamic NBTI components in p-MOSFET with SiON dielectric and their impact on device life-time and circuit application", *VLSI Tech. Symp.*, pp. 92-93, 2005

[1.7] S. Zafar, A. Callegari, E. Gusev, and M. V. Fischetti, "Charge trapping in high K gate dielectric stacks," *IEDM Tech. Dig.* pp. 517-520, 2002

[1.8] M. Houssa, M. Aoulaiche, S. Van Elshocht, S. De Gendt, G. Groeseneken, and M. H. Heyns, "Impact of Hf content on negative bias temperature instabilities in HfSiON-based gate stacks," *Appl. Phys. Lettl* vol. 86, pp. 173509, 2005

[1.9] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub 0.1 μm MOSFETs: a 3D "atomistic" simulation study," *IEEE Trans. Electron Devices*, vol. 45, pp. 2505-2513, Dec, 1998

[1.10] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya and G. Slavcheva, "Simulation of Intrinsic Parameter Fluctuations in Decananometer and Nanometer-Scale MOSFETs," *IEEE Trans. Electron Devices,* vol. 50, pp. 1837-1852, 2003

[1.11] H. P. Tuinhout, "Impact of parametric mismatch and fluctuations on performance and yield of deep-submicron CMOS technologies," in *Proc. ESSDERC,* 2002, pp. 95-101

[1.12] H. Aikawa, "Variability aware modeling and characterization in standard cell in 45 nm CMOS with stress enhancement technique," in *VLSI Tech. Symp.*, 2008, pp.90-91

[1.13] K. Ishimaru, "45 nm/32 nm CMOS challenge and perspective," in *Proc. ESSDERC,* 2007, pp. 32-35

[1.14] B. Cheng, S. Roy, G. Roy, F. Adamu-Lema, and A. Asenov, "Impact of intrinsic parameter fluctuations in decanano MOSFETs on yield and functionality of SRAM cells," *Solid State Electron.,*, vol. 49, pp. 740-746, May 2005

[1.15] D. Reid, C. Millar, G. Roy, S. Roy, and A. Asenov, "Analysis of Threshold Voltage Distribution Due to Random Dopants: A

100000-Sample 3-D Simulation Study," *IEEE Trans. on Elec. Dev.*, vol. 56, pp. 2255-2263, Oct. 2009

[1.16] V. Huard, C. Pathasarathy, C. Guerin, T. Valentin, E. Pion, M. Mammasse, N. Planes, and L. Camus, "NBTI degradation: From transistor to SRAM arrays," in *Proc. Int. Rel. Symp.*, 2008, pp. 289-300

[1.17] S. E. Rauch, "Review and reexamination of reliability effects related to NBTI statistical variations," *IEEE Trans. Device Mater. Rel.*, vol. 7, no. 4, pp. 524-530, Dec. 2007

[1.18] B. Kaczer, T. Grasser, J. Martin-Martinez, E. Simeon, M. Aoulaiche, P. J. Roussel, and G. Groeseneken, "NBTI from the perspective of defect states with widely distributed times," in *Proc. Int. Rel. Phys. Symp.*, 2009, pp. 55-60,

[1.19] B. Kaczer, T. Grasser, P. J. Roussel, J. Franco, R. Degraeve, L.-A. Ragnarsson, E. Simeon, G. Groeseneken, and H. Reisinger, "Origin of NBTI variablility in deeply scaled pFETs," in *Proc. Int. Rel. Phys. Symp.*, 2010, pp. 26-32

[1.20] B. Kaczer, P. J. Roussel, T. Grasser, and G. Groeseneken, "Statistical of Multiple Trapped Charges in the Gate Oxide of Deeply Scaled MOSFET Devices-Application to NBTI," *IEEE Elec. Dev. Lett.*, vol. 31, pp. 411-413, May, 2010

[1.21] M. F. Bukhori, S. Roy, and A. Asenove, "Simulation of Statistical Aspects of Charge Trapping and Related Degradation in Bulk MOSFETs in the Presence of Random Discrete Dopants," *IEEE Trans. Elec. Dev.*, vol. 57, pp. 795-803, Apr. 2010

[1.22] C. T. Chan, H. C. Ma, C. J. Tang, and Tahui Wang, "Investigation of

Post-NBTI Stress Recovery in pMOSFETs by Direct Measurement of Single Oxide Charge De-trapping," *VLSI Tech. Dig.*, pp. 90-91, 2005

[1.23] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A Novel Localized Trapping, 2-bit Novolatile Memory Cell," *IEEE Electron Device Lett.*, vol. 21, pp. 543-545, Nov. 2000

[1.24] M. H. Tsai, H. Muto, and T. P. Ma, "Random telegraph signals arising from fast interface states in metal-SiO_2-Si transistors", *Appl. Phys. Lett.* vol. 61, pp. 1691, Oct. 1992

[1.25] K. Kandiah, M. O. Deighton, and F. B. Whiting, "A physical model for random telegraph signal currents in semiconductor devices", *J. Appl. Phys.* vol.66, pp. 937, July 1989

[1.26] M. J. Kirton and M. J. Uren, "Noise in solid state microstructure: A new perspective on individual defects, interface states, and low frequency noise," *Adv. in Phys.*, vol. 38, pp. 367-468, 1989

[1.27] H. Muller and M. Schulz, "Conductance modulation of submicrometer metal-oxide-semiconductor field-effect transistors by single electron trapping," *J. Appl. Phys.*, vol. 79, no. 8, pp. 4178-4186, Apr. 1996

[1.28] N. Tega, H. Miki, T. Osabe, A. Kotabe, K. Otsuga, H. Kurata, S. Kamohara, K. Tokami, Y. Ikeda, and R. Yamada, "Anomalously Large Threshold Voltage Fluctuation by Complex Random Telegraph Signal in Floating Gate Flash Memory," in *IEDM Tech. Dig.*, pp. 491 -494, 2006

[1.29] P. Fantini, A. Ghetti, A. Marinoni, G. Ghidini, A. Visconti, and A. Marmiroli, "Giant Random Telegraph Signals in Nanoscale Floating-Gate Devices," *IEEE Electron Device Lett.*, Vol.28, pp. 1114 - 1116, 2007

[1.30] H. Kurata, K. Otsuga, A. Kotabe, S. Kajiyama, T. Osabe, Y. Sasago, S. Narumi, K. Tokami, S. Kamohara, and O. Tsuchiya, "The Impact of Random Telegraph Signals on the Scaling of Multilevel Flash Memories," in *VLSI Circuit Symp.*, pp. 112 - 113, 2006

[1.31] K. Fukuda, Y. Shimizu, K. Amemiya, M. Kamoshida, and C. Hu, "Random Telegraph Noise in Flash Memories-Model and Technology Scaling," in *IEDM Tech. Dig.*, pp. 169 - 172, 2007

[1.32] A. S. Spinelli, C. M. Compagnoni, R. Gusmeroli M. Ghidotti and A. Visconti, "Investigation of the Random Telegraph Noise Instability in Scaled Flash Memory Arrays," *Jpn. J. Appl. Phys.* vol. 47, no. 4, pp. 2598–2601, 2008

[1.33] S. H. Gu, C. W. Li, Tahui Wang, W. P. Lu, K. C. Chen, Joseph Ku, and Chih-Yuan Lu, "Read Current Instability Arising from Random Telegraph Noise in Localized Storage, Multi-Level SONOS Flash Memory," *IEDM Tech. Dig.*, pp. 487-490, 2006

[1.34] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chen, and D. Buchanan, "Volatile and nonvolatile memories in silicon with nano-crystal storage," in *IEDM Tech. Dig.*, pp. 521, 1995

[1.35] R. Muralidhar, R. F. Steimle, M. Sadd, R. Rao, C. T. Swift, E. J. Prinz, J. Yater, L. Grieve, K. Harber, B. Hradsky, S. Straub, B. Acred, W. Paulson, W. Chen, L. Parker, S. G. H. Anderson, M. Rossow, T. Merchant, M. Paransky, T. Huynh, D. Hadad, K.-M. Chang, and B. E. White, Jr., "A 6 V embedded 90 nm silicon nanocrystal nonvolatile memory," in *IEDM Tech. Dig.*, 2003, pp. 601–605

[1.36] Y. H. Lin, C. H. Chien, C. T. Lin, C. W. Chen, C. Y. Chang, T. F. Lei,

"High performance multi-bit nonvolatile HfO2 nanocrystal memory using spinodal phase separation of hafnium silicate," in *IEDM Tech. Dig.*, pp. 1080-1082, 2004

Chapter 2

[2.1] M. H. White, D. Adams and J. Bu, "On the Go with SONOS," *IEEE Circuits and Devices Magazine*, vol. 16, p.22, Jul. 2000

[2.2] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," *IEEE Electron Device Lett.*, vol. 21, pp. 543-545, Nov. 2000

[2.3] Y. W. Chang, T. C. Lu, S. Pan, and C. Y. Lu, "Modeling for the Second Bit Effect of a Nitride-Based Trapping Storage Flash EEPROM Cell under Two-Bit Operation," *IEEE Electron Device Lett.*, vol. 25, pp. 95–97, Feb. 2004.

[2.4] E. Lusky, Y. Shacham-Diamand, I. Bloom and B. Eitan "Characterization of Channel Hot Electron Injection by the Subthreshold Slope of NROM Device," *IEEE Electron Device Lett.*, vol. 22, pp. 556-558, Nov. 2001

[2.5] M.Y. Liu, Y.W. Chang, N.K. Zous, I. Yang, T.C. Lu, Tahui Wang, W.C. Ting, Joseph Ku, and Chih-Yuan Lu, "Temperature Effect on Read Current in a Two-bit Nitride-based Trapping Storage Flash EEPROM Cell," *IEEE Electron Device Lett.*, vol. 25, pp. 495-497, Jul. 2004

[2.6] P.R. Nair, P. Bharath Kumar, R. Sharma, S. Kamohara and S. Mahapatra "A Comprehensive Trapped Charge Profiling Technique for SONOS Flash EEPROMs", in *IEDM Tech. Dig.*, pp. 403-406, 2004

[2.7] S. H. Gu, Tahui Wang, W. P. Lu, W. Ting, Y. H. Joseph Ku, and C. Y. Lu, "Characterization of Programmed Charge Lateral Distribution in a Two-bit Storage Nitride Flash Memory Cell by Using a Charge Pumping Technique," *IEEE Trans. Electron, Devices,* pp.103-108, Jan. 2006.

[2.8] M. Rosmeulen , L. Breuil , M. Lorenzini , L. Haspeslagh , J. Van Houdt and D. De Meyer "Characterization of the Spatial Charge Distribution in Local Charge-Trapping Memory Devices Using the Charge-Pumping Technique," *Solid State Electron*, vol. 48, pp. 1525-1530, Sep. 2004.

[2.9] A. Padovani, L. Larcher and P. Pavan, "Hole Distributions in Erased NROM Devices; Profiling Method and Effects on Reliability," *IEEE Trans. Electron Devices*, vol. 55, pp. 343–349, Jan. 2008

[2.10] C. Chen and T. P. Ma, "Direct Lateral Profiling of Hot-Carrier-Induced Oxide Charge and Interface Traps in Thin Gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 45, pp. 512–520, Feb. 1998

[2.11] S. Jeon, J. H. Han, J. Lee, S. Choi, H. Hwang, and Chungwoo Kim, "Impact of metal work function on memory properties of charge-trap flash memory devices using fowler-nordheim P/E mode," *IEEE, Elect. Dev. Lett.*, vol.27, pp. 486-488, 2006

[2.12] H. Kurata, K. Otsuga, A. Kotabe, S. Kajiyama, T. Osabe, Y. Sasago, S. Narumi, K. Tokami, S. Kamohara, and O. Tsuchiya, "The Impact of Random Telegraph Signals on the Scaling of Multilevel Flash Memories," in *Proc. Symp. VLSI Circuits Dig.*, 2006, pp. 140–141

[2.13] K. Fukuda, Y. Shimizu, K. Amemiya, M. Kamoshida, and C. Hu, "Random Telegraph Noise in Flash Memories—Model and Technology Scaling," in *IEDM Tech. Dig.*, 2007, pp. 169–172.

[2.14] S.H. Gu, C.W. Li, Tahui Wang, W.P. Lu, K.C. Chen, Joseph Ku, and C.Y. Lu, "Read Current Instability Arising from Random Telegraph Noise in Localized Storage, Multi-Level SONOS Flash Memory," in *IEDM Tech. Dig.*, pp.487-490, 2006

[2.15] Jeff D. Bude, Mark R. Pinto, and R. Kent Smith, "Monte Carlo Simulation of the CHISEL Flash Memory Cell," *IEEE Trans. Electron Devices*, vol. 47, no.10, pp. 1873 - 1881, Oct. 2000

[2.16] P. Restle, "Individual Oxide Traps as Probes into Submicron Devices," *Appl. Phys. Lett.*, vol.53, pp. 1862, Nov. 1988

[2.17] Sze and Ng, "Physics of Semiconductor Devices", third edition, Wiley, 2007, pp. 22

[2.18] J. W. Wu, J. W. You, H. C. Ma, C. C. Cheng, C. F. Hsu, C. S. Chang, G. W. Huang, Tahui Wang, "Excess Low-Frequency Noise in Ultrathin Oxide n-MOSFETs Arising from Valence-Band Electron Tunneling," *IEEE Trans. Electro, Devices*, vol. 52, no. 9, pp. 2061-2066, Sep. 2005

[2.19] C.J. Tang, C.W. Li, Tahui Wang, S.H. Gu, P.C. Chen, Y.W. Chang, T.C. Lu, W.P. Lu, K.C. Chen, and C.Y. Lu, "Characterization and Monte Carlo Analysis of Secondary Electrons Induced Program Disturb in a Buried Diffusion Bit-line SONOS Flash Memory," in *IEDM Tech. Dig.*, pp.173-176, 2007.

[2.20] L. Avital, A. Padovani, L. Larcher, I. Bloom, R. Arie, P. Pavan, and B. Eitan, "Temperature monitor: A new tool to profile charge distribution in NROM memory devices," in Proc. IRPS, 2006, pp. 534–540.

[2.21] A. Shappir, Y. Shacham-Diamand, E. Lusky, I. Bloom, and B. Eitan,"Lateral charge transport in the nitride layer of the NROM non-volatile memory device," Microelectron. Eng., vol. 72, no. 1–4, pp. 426–433, Apr. 2004.

[2.22] W. J. Tsai, N. K. Zous, C. J. Liu, C. C. Liu, C. H. Chen, T. Wang, S. Pan, C.-Y. Lu, and S. H. Gu, "Data Retention Behavior of a SONOS Type Two-Bit Storage Flash Memory Cell," in *IEDM Tech. Dig.*, 2001, pp. 719-722

[2.23] L. Breuil, L. Haspeslagh, P. Blomme, M. Lorenzini, D. Wellekens, J. De

Vos, J. Van Houdt, "Comparative Reliability Investigation of Different Nitride Based Local Charge Trapping Memory Devices," in *Proc. IRPS*, pp. 181-185, 2005

[2.24] H.T. Lue, Y.H. Hsiao, Y.H. Shih, E.K. Lai, K.Y. Hsieh, R. Liu and Chih-Yuan Lu, "Study of Charge Loss Mechanism of SONOS-type Devices Using Hot-Hole Erase and Methods to Improve the Charge Retention, " in *Proc. IRPS*, pp. 523-529, 2006

[2.25] P. Kumar, E. Murakami, S. Kamohara and S. Mahapatra, "Endurance and Retention Characteristics of SONOS EEPROMs operated Using BTBT Induced Hot Hole Erase," in Proc. IRPS, pp. 699-700, 2006

[2.26] G. Tempel, R. Hagenbeck and M. Strassburg, "Quantitative Model for Data Retention Loss at NROM Nitride Charge Trapping Devices after Program/Erase Cycling," in *Proc. Non-Volatile Semiconductor Memory Workshop*, pp.78-80, 2006

[2.27] M. Janai, B. Eitan, A. Shappir, E. Lusky, I. Bloom, and G. Choen, "Data Retention Reliability Model of NROM Nonvolatile Memory Products," *IEEE Trans. Device Mater. Rel.*, vol. 4, no. 3, pp. 404–415, Sep. 2004.

[2.28] A. Furnémont, M. Rosmeulen, K. Van der Zanden, J. Van Houdt, K. De Meyer and H. Maes, "Root Cause of Charge Loss in a Nitride-Based Localized Trapping Memory Cell," *IEEE Trans. Electron Device*, vol. 54, pp. 1351–1359, Jun. 2007

[2.29] A. Shapira, Y. Shur, Y. Shacham-Diamond, A. Shappir and B. Eitan, "Unified Retention Model for Localized Charge Trapping Nonvolatile Memory Device," *Appl. Phys. Lett.*, vol. 92, 133514, Apr. 2008

[2.30] David Fuks, Arnold Kiv, Yakov Roizin, Micha Gutman, Rachel

Avichail-Bibi, and Tatyana Maximova, "The Nature of HT Vt Shift in NROM Memory Transistors", *IEEE Trans. Electron Device*, vol. 53, pp. 304–313, Jun. 2006

[2.31] S.H. Gu, Tahui Wang, W.P. Lu, Y.H. Joseph Ku, and C.Y. Lu, "Numerical Simulation of Bottom Oxide Thickness Effect on Charge Retention in SONOS Flash Memory Cells with Fowler-Nordheim Programming," *IEEE Trans. Electron Devices*, pp.90-97, Jan. 2007

[2.32] B. Doyle, M. Bourcerie, J. Marchetaux, and A. Boudou, "Interface State Creation and Charge Trapping in the Medium-to-High Gate Voltage Range During Hot-Carrier Stressing of n-MOS Transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 744–754, Mar. 1990

[2.33] W. J. Tsai, N. K. Zous, H. Y. Chen, Lenvis Liu, C.C. Yeh, Sam Chen, W. P. Lu, Tahui Wang, Joseph Ku, and Chih-Yuan Lu, "Investigation of Charge Loss in Cycled NBit Cells via Field and Temperature Accelerations," in *IEEE International Integrated Reliability Workshop*, pp. 693-694, 2006

[2.34] P. Zisman, Y. Roizin, and M. Gutman, "Vt Drift of Cycled Two-Bit microFLASH Cells," in *Solid State Devices and Materials,* pp. 228-229, 2003

[2.35] I. Bloom, P. Pavan, and B. Eitan, "NROM™— A New Nonvolatile Memory Technology: from Device to Products," *Microelectron. Eng.*, vol. 59, pp. 213-223, 2001

Chapter 3

[3.1] N. Tega, H. Miki, T. Osabe, A. Kotabe, K. Otsuga, H. Kurata, S.

Kamohara, K. Tokami, Y. Ikeda, and R. Yamada, "Anomalously Large Threshold Voltage Fluctuation by Complex Random Telegraph Signal in Floating Gate Flash Memory," in *IEDM Tech. Dig*., 2006, pp. 491–494

[3.2] P. Fantini, A. Ghetti, A. Marinoni, G. Ghidini, A. Visconti, A. Marmiroli, "Giant Random Telegraph Signals in Nanoscale Floating-Gate Devices," *IEEE Trans. Electron Device Letters*, vol. 28, no.12, pp. 1114-1116, Dec. 2007

[3.3] H. Kurata, K. Otsuga, A. Kotabe, S. Kajiyama, T. Osabe, Y. Sasago, S. Narumi, K. Tokami, S. Kamohara, and O. Tsuchiya, "The Impact of Random Telegraph Signals on the Scaling of Multilevel Flash Memories," *VLSI Circuits Symp. Dig*., 2006, pp. 112 -113

[3.4] K. Fukuda,Y. Shimizu, K. Amemiya, M. Kamoshida ,and Chenming. Hu "Random Telegraph Noise in Flash Memories: Model and Technology Scaling," in *IEDM Tech. Dig*., 2007, pp. 169–172

[3.5] A. Ghetti, M. Bonanomi, C.M. Compagnoni, A.S. Spinelli, A.L. Lacaita, and A. Visconti, "Physical Modeling of Single-trap RTS Statistical Distribution in Flash Memories," in *IEEE-IRPS 2008*, pp. 610-615

[3.6] A. Asenov, R. Balasubramaniam, A. R. Brown, and J. H. Davies, "RTS Amplitudes in Decananometer MOSFETs: 3-D Simulation Study," *IEEE Trans. Electron Devices*, vol. 50, no.3, pp. 839-845, Mar. 2003

[3.7] http://www.ibiblio.org/e-notes/Perc/contour.htm

Chapter 4

[4.1] M.H. White, D. Adams and J. Bu, "On the Go with SONOS," *IEEE Circuits and Devices Magazine*, Vol. 16, pp.22-31, 2000.

[4.2] Y.N. Tan, W.K. Chim, W.K. Choi, M.S. Joo, T.H. Ng and B.J. Cho, "High-k HfAlO charge trapping layer in SONOS-type nonvolatile memory device for high speed operation," in *IEDM Tech. Dig.*, pp.889-892, 2004

[4.3] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chen, and D. Buchanan, "Volatile and nonvolatile memories in silicon with nano-crystal storage," in *IEDM Tech. Dig.*, pp. 521, 1995

[4.4] R. Muralidhar, R. F. Steimle, M. Sadd, R. Rao, C. T. Swift, E. J. Prinz, J. Yater, L. Grieve, K. Harber, B. Hradsky, S. Straub, B. Acred, W. Paulson, W. Chen, L. Parker, S. G. H. Anderson, M. Rossow, T. Merchant, M. Paransky, T. Huynh, D. Hadad, K.-M. Chang, and B. E. White, Jr., "A 6 V embedded 90 nm silicon nanocrystal nonvolatile memory," in *IEDM Tech. Dig.*, 2003, pp. 601–605

[4.5] Y. H. Lin, C. H. Chien, C. T. Lin, C. W. Chen, C. Y. Chang, T. F. Lei, "High performance multi-bit nonvolatile HfO2 nanocrystal memory using spinodal phase separation of hafnium silicate," in *IEDM Tech. Dig.*, pp. 1080-1082, 2004

[4.6] S.H. Gu, C.W. Hsu, Tahui Wang, W.P. Lu, Y.H. Joseph Ku, and Chih-Yuan Lu, "Numerical Simulation of Bottom Oxide Thickness Effect on Charge Retention in SONOS Flash Memory Cells," *IEEE Trans. Electron Devices*, vol. 54, pp. 90-97, 2007

[4.7] D. J. Dumin and J. Maddux, "Correlation of stress-induced leakage current in thin oxides with trap generation inside the oxides," *IEEE Trans. Electron Devices*, vol. 40, pp. 986-993, 1993

[4.8] D. J. Dumin and J. Maddux, "Correlation of stress-induced leakage

current in thin oxides with trap generation inside the oxides," *IEEE Trans. Electron Devices*, vol. 40, pp. 986-993, 1993

[4.9] L. Lundkvist, I. Lundstrom and C. Svensson, "Discharge of MNOS structures," Solid-St. Electron., vol.16, pp. 811-823, 1973

[4.10] Y. Hu and M. White, "Charge retention in scaled SONOS nonvolatile semiconductor memory devices-modeling and characterization," *Solid-St. Electron.*, vol.36, pp. 1401-1416, 1993

Chapter 5

[5.1] C. J. Tang, H. C. Ma, C. T. Chan, T. Wang, and H. C.-H. Wang, "NBT stress induced anomalous drain current instability in HfSiON pMOSFETs arising from bipolar charge trapping," *Proc. Int. Conf. Solid State Devices Mater.*, 2006, pp. 366–367

[5.2] Campbell, J.P., Cheung, K.P., Suehle, and J.S. Oates, A., "The fast initial threshold voltage shift: NBTI or high-field stress," *IEEE Int. Reliability Phys. Symp.*, 2008, pp. 72-78

[5.3] Campbell, J.P., Cheung, K.P., Suehle, and J.S. Oates, A., "Electron trapping: An unexpected mechanism of NBTI and its implications," in *VLSI Symp. Tech. Dig.*, 2008, pp. 76-77

[5.4] C. J. Tang, H. C. Ma, T. Wang, C. T. Chan, and C. S. Chang, "Bipolar charge trapping induced anomalous negative bias-temperature instability in HfSiON gate dielectric pMOSFETs," *IEEE Trans. Device and Materials Reliability*, vol. 7, no. 4, pp. 518-523, Dec. 2007

[5.5] T. Wang, C.T. Chan, C.J. Tang, C.W. Tsai, Wang, H.C.-H, M.H. Chi, Tang, D.D., "A novel transient characterization technique to investigate

trap properties in HfSiON gate dielectric MOSFETs-from single electron emission to PBTI recovery transient," *IEEE Trans. Electron Devices*, vol. 53, pp. 1073-1079, May, 2006

[5.6] C.T. Chan, C.J. Tang, T. Wang, H.C.H. Wang, and D.D. Tang, "Positive bias and temperature stress induced two-stage drain current degradation in HfSiON nMOSFET's, " in *IEDM Tech. Dig.*, pp.571-574, 2005

學經歷表 Vita

姓名/Name	：	馬煥淇 Huan-Chi Ma	**性別/Sex**	：	男 Male
生日/DOB	：	1981/01/11	**籍貫**	：	台南市

學歷/Education：

國立台南第一高級中學 1996.09-1999.06
National Tainan First Senior High School

國立交通大學電子工程學系 1999.09-2003.06
Dept. of Electronics Engineering, NCTU

國立交通大學電子工程研究所碩士班 2003.09-2005.06
M. S. Program, Dept. of Electronics Engineering, NCTU

國立交通大學電子工程研究所博士班 2005.09-2011.01
Ph. D. Program, Dept. of Electronics Engineering, NCTU

經歷/Experience：

固態物理助教
Solid-State Physics

博士論文題目/Ph. D. Dissertation：

快閃式記憶體和金氧半電晶體元件中單一電荷所導致的可靠性議題研究

Single Charge Phenomenon in Scaled Memory and CMOS Devices

Publication List

(a) Journal Papers

3.

A類國際性期刊論文

(1) H. C. Ma, Y. L. Chou, J. P. Chiu, Y. T. Chung, T. Y. Lin, Tahui Wang, Y. P. Chao, K. C. Chen, and Chih-Yuan Lu, "A Novel Random Telegraph Signal Method to Study Program/Erase Charge Lateral Spread and Retention Loss in a SONOS Flash Memory" accepted and to be published in *IEEE Trans. on Electron Devices(TED)*

3.

A類國際性期刊論文

(2) H. C. Ma, Y. L. Chou, J. P. Chiu, Tahui Wang, S. H. Ku, N. K. Zou, Vincent Chen, W. P. Lu, K. C. Chen, and Chih-Yuan Lu, "Program Trapped Charge Effect on Random Telegraph Noise Amplitude in a Planar SONOS Flash Memory Cell," *IEEE Elect. Dev. Lett.(EDL)*, Vol. 30, pp.1188-1190, 2009

3.

A類國際性期刊論文

(3) Tahui Wang, H. C. Ma, C. H. Li, Y. H. Lin, C. H. Chien and T. F. Lei, "Charge Retention Loss in a HfO_2 Dot Flash Memory via Thermally Assisted Tunneling," *IEEE Elect. Dev. Lett.(EDL)*, Vol. 29, pp.109-110, 2008

(4) C. J. Tang, H. C. Ma, Tahui Wang, C. T. Chan, and C. S. Chang, "Bipolar Charge Trapping Induced Anomalous Negative Bias-Temperature Instability in HfSiON Gate Dielectric pMOSFETs," *IEEE Trans. on Device and Materials Reliability (Invited paper)*, Vol. 7, pp.518-523, 2007

(5) J. W. Wu, J. W. You, H. C. Ma, C. C. Cheng, C. S. Chang, G. W. Huang, and Tahui Wang, "Excess Low-Frequency Noise in Ultrathin Oxide n-MOSFETs Arising from Valence-Band Electron Tunneling," *IEEE Trans. on Electron Devices(TED)*, vol. 52, pp. 2061-2066, 2005

(6) J. W. Wu, J. W. You, H. C. Ma, C. C. Cheng, C. S. Chang, G. W. Huang, and Tahui Wang, "Valence-band tunneling induced low frequency noise in ultrathin oxide (15A) n-type

metal-oxide-semiconductor field effect transistors," *Appl. Phys. Lett.* Vol. 85, 1827930, 2004

(b) Conference Papers

1. 國際會議論文

(7) H. C. Ma, J. P. Chiu, C. J. Tang and Tahui Wang, "Investigation of Post-NBT Stress Current Instability Modes in HfSiON Gate Dielectric pMOSFETs by Measurement of Individual Trapped Charge Emissions," *Proc. Int. Reliab. Phys. Symp. (IRPS)*, Montreal, Canada, pp.51-54, 2009

(8) Y. L. Chou, J. P. Chiu, H. C. Ma, Tahui Wang, Y. P. Chao, K. C. Chen, and Chih-Yuan Lu, "Use of Random Telegraph Signal as Internal Probe to Study Program/Erase Charge Lateral Spread in a SONOS Flash Memory," *Proc. Int. Reliab. Phys. Symp. (IRPS)*, pp.960 – 963, Anaheim, U.S.A., 2010

(9) J. P. Chiu, Y. L. Chou, H. C. Ma, Tahui Wang, S. H. Ku, N. K. Zou, Vincent Chen, W. P. Lu, K. C. Chen, and Chih-Yuan Lu, "Program Charge Effect on Random Telegraph Noise Amplitude and Its Device Structural Dependence in SONOS Flash Memory," *IEEE International Electron Device Meeting(IEDM)*, Baltimore, U.S.A., pp.843-846, 2009

(10) C. J. Tang, H. C. Ma, C. T. Chan, Tahui Wang, and H. C.-H. Wang, "NBT Stress Induced Anomalous Drain Current Instability in HfSiON pMOSFETs Arising from Bipolar Charge Trapping," *International Conference on Solid State Devices and Materials (SSDM)*, pp. 366-367 , Yokohama, Japan, 2006

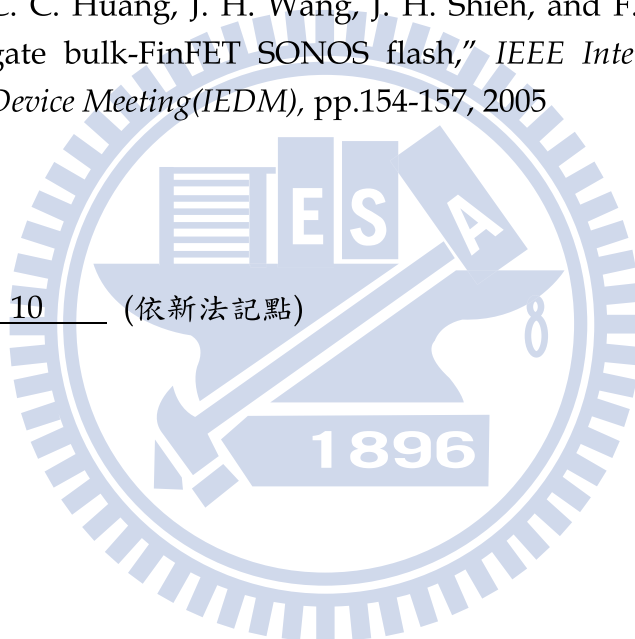
(11) C. T. Chan, H. C. Ma, C. J. Tang, and Tahui Wang, "Investigation of Post-NBTI Stress Recovery in pMOSFETs by Direct Measurement of Single Oxide Charge De-Trapping," *VLSI Tech. Dig. (VLSI), Kyoto, Japan,* pp. 90-91, 2005
(Best Student Paper Award)

(12) C. T. Chan, C. J. Tang, C. H. Kuo, H. C. Ma, C. W. Tsai, H. C.-H.

Wang, M. H. Chi, and Tahui Wang, “Single-electron Emission of Traps in HfSiON as High-k Gate Dielectric for MOSFETs,” *Int. Reliab. Phys. Symp. (IRPS)* , pp. 41-44, San Jose, U.S.A., 2005

(13) J. W. Wu, J. W. You, H. C. Ma, C. C. Cheng, C. F. Hsu, G. W. Huang, C. S. Chang, and Tahui Wang, ”Low Frequency Noise Degradation in Ultra-thin Oxide (15A) Analog n-MOSFETs Resulting from Valence-Band Tunneling,” *Proc. Int. Reliab. Phys. Symp. (IRPS)*, pp. 260-264, San Jose, U.S.A., 2005

(14) J. R. Hwang, T. L. Lin, H. C. Ma, T. C. Lee, T. H. Chung, C. Y. Chang, S. D. Liu, B. C. Perng, J. W. Hsu, M. Y. Lee, C. Y. Ting, C. C. Huang, J. H. Wang, J. H. Shieh, and F. L. Yang, “20nm gate bulk-FinFET SONOS flash,” *IEEE International Electron Device Meeting(IEDM)*, pp.154-157, 2005



著作總點數：10 (依新法記點)