國立交通大學

電子工程學系 電子研究所

博士論文

前瞻非揮發性電阻式記憶體元件之製作與特性研究

Fabrication and Characterization of FeO_x Based Resistive Random Access Memory

研 究 生：馮立偉

指導教授：張俊彥 教授

中華民國九十九年十一月

前瞻非揮發性電阻式記憶體元件之製作與特性研究

Fabrication and Characterization of FeO_x Based Resistive Random Access Memory

研究生：馮立偉　　Student：Li-Wei Feng

指導教授：張俊彥　　Advisor：Chun-Yen Chang

國立交通大學

電子工程學系 電子研究所

博士論文

A Dissertation
Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering

November 2010
Hsinchu, Taiwan, Republic of China

中華民國九十九年十一月

前瞻非揮發性電阻式記憶體元件之製作與特性研究

研究生：馮立偉　　　　**指導教授：張俊彥 院士**

國立交通大學

電子工程學系暨電子研究所

摘要

隨著數位行動生活的到來，非揮發性記憶體在可攜式電子產品，如：手機、數位相機跟筆記型電腦扮演著重要的角色。以傳統浮閘(Floating gate)記憶體為基本元件之非揮發性固態半導體記憶體是現今非揮發性記憶體的主流，但是它有著許多缺點，包含：高的操作電壓、低的操作速度與較差的耐久力，且隨著尺寸微縮的趨勢下，面臨了難以解決之難題，即儲存在懸浮閘極中之電荷，因穿遂氧化層過薄而隨時間漸漸流失，造成資料流失，如此瓶頸，加快了下世代非揮發性記憶體之研究腳步。其一類預期能取代傳統浮閘記憶體的非揮發性元件者為電阻式非揮發性記憶體(RRAM)，主要是由於其製程簡單且與動態隨機存取記憶體(DRAM)製程相似，可以被整合到半導體的後段製程。電阻式記憶體擁有高速、非揮發性與低電壓操作的特性等優點。故本論文所研究之主題，將針對電阻式性記憶體這類型之非揮發性記憶體原件觀念為主，而提出一以鐵原素為製程基礎之一系列具簡易製程方式的記憶體原件之備製，並探討其元件之原理與特性，以及更進一步地提供改良其元件特性之製備方式：對此鐵原素電阻式性記憶體而言，

我們提供了一種利用氧化鐵電極的表面之方式，來獲得一層具備阻值轉態特性的薄氧化鐵薄膜，因為阻值轉態特性的存在主要與非完全化學當量組成的過渡金屬氧化物的存在相關，是故藉由氧化鐵電極表面所獲得之薄氧化鐵薄膜的最大優勢為其本身所具備之不完全化學組成之氧化層成分，而能利用以提供較佳的電阻式記憶體特性。另一方面，藉由鉑(Pt)元素於鐵電極的參雜而製成的鉑化鐵(FePt alloy)合金，而能間接控制鐵電極的氧化與擴散，以利於進一步地探討其特性與原理。就其基本轉態原理之推測上，我們藉由不同極性之高壓施加而於電極上所產生之不同特性之泡泡現象(Bubble Effect)，以及元件電阻值對不同元件電極面積之關係分析，來更進一步來間接地佐證此氧化鐵之阻值轉態現象的機制。甚者，我們亦於此兩組含鐵電極之元件，研究於不同的後續熱退火製程處理之特性，發現藉由退火處理能有效地降低形成電壓、操作電壓以及其電性參數之變異性，而能獲得更佳的電阻式記憶體特性，其原因也藉由X光光電子能譜儀(XPS)，穿透式電子顯微鏡(TEM)，X光粉晶繞射儀(XRD)分析來討論；我們更藉由做不同退火處理樣本之電性結果的統計分析，來釐清其更深入的機制。此外，我們亦發現藉由設定量測時之電流限流限制條件與電壓掃描限制條件之設定，而能任意調整此氧化鐵薄膜其所具有的阻值狀態，能達到具多重阻值位階之特性，以利於成為高儲存資料密度之運用；同樣地，此不同電流限流與電壓掃描限制條件下之電性結果統計分析，亦能對這尚未完全明瞭的電阻轉態機制，進一步地來輔助此元件轉態機制之確認。最後對全文作一總結，並對未來可行的研究工作做一建議。

Fabrication and Characterization of FeO_x Based Resistive Random Access Memory

Student: Li-Wei Feng **Advisor: Dr. Chun-Yen Chang**

Department of Electronics Engineering & Institute of Electronics,
National Chiao Tung University

Abstract

With the arrival of Digital Age, nonvolatile memory (NVM) plays an important role in portable electronic products, such as the mobile phone, digital camera, and notebook computer. Floating gate composed nonvolatile memories have been widely applied in electronic devices in recent years, but it has many drawbacks, including high operation voltage, low operation speed, and poor endurance. Moreover, as the device dimensions are continuously scaled down, the floating gate composed memory faces the challenge of thin tunneling oxide that causes an unsatisfactory retention time. Consequently, resistive random access memory (RRAM) is one promising candidate to substitute for conventional floating gate memory. As for RRAM, the digital data can be stored in two memory states with high and low resistivities, ON-state and OFF-state, respectively. The two memory states can be easily switched by voltage biases or pulses, which enhance the possibility of the application in circuit level. Therefore, the topic of this thesis discusses this advanced nonvolatile memory devices by fabricating and characterizing iron-based RRAM devices and, furthermore, proposes the methods to improve the characteristics of the proposed devices for NVM applications. The proposed iron-based RRAM device was fabricated by a structure of $TiN/SiO_2/FeO_x/Fe$, where the FeO_x is a thin transition layer at the SiO_2/Fe interface and produced spontaneously during the plasma-enhanced tetraethyl orthosilicate oxide deposition process due to the ease of oxidation of iron atoms. The basic idea of the proposed structure is that the resistive switching effect is associated with the existence of nonstoichiometric materials, so the thin FeO$_x$ transition layer produced by partially oxidizing the iron electrode surface exhibits a richer nonstoichiometry property because of containing the compositions varied from Fe-rich FeO$_x$ (close to Fe electrode) to oxygen-rich FeO$_x$ (close to SiO$_2$ layer). Moreover, in order to clarify the detailed mechanism of resistive switching effects, a method of adding platinum (Pt) into Fe electrode, which affects oxidation and diffusion characteristics of Fe layer, was also proposed by a TiN/SiO$_2$/FeO$_x$/FePt structure. In addition, observation of bubble effects occurred at the top electrode after biasing highly opposite polarity voltage stresses as well as the electrode area dependence of resistance values also provides another indirect method to clarify the mechanism of resistive switching effects.

Moreover, the influence of thermal annealing treatments on the FeO$_x$ resistance switching behaviors was also researched because of the thermal sensitivity of the iron oxide layer. The distinct reduction of memory switching parameters in forming voltage, set/reset voltages, and even their dispersions was obtained after annealing. The cause was also discussed by XPS, TEM, and XRD analyses. Additionally, statistical electrical results, including set/reset current, set/reset voltage and set/reset power, also help for understanding the mechanism of resistive switching effects.

Furthrmore, multiple resistance states were easily observed to obtain in our proposed FeO$_{\mathrm{x}}$-contained structure by justifying the sweeping voltage during the reset process region and the compliance current during the set process region, which allow more bits to be stored per cell for application. Moreover, extraction of statistical results, such as set/reset voltage, set/reset current and set/reset power, further provides

more details to clarify the mechanism of the FeO_x-contained resistive switching behaviors.In the final part of this dissertation, the conclusions and the suggested future works are presented.

誌謝

從歷歷在目之初至新竹念研究所之時，轉眼間便就到了該好好寫此篇夾在博士論文內之致謝之際，但此當中，卻又矛盾地充滿著一日三秋所感受到的喜、怒、哀、樂，與悲、歡、離、合，確如人飲水般，讓我充實的體會了一遍。而此一切的一切，著實都是因為有著的大家幫忙與協助始得以完成，是故希望能藉由此篇致謝，來拙劣地敘述出我內心所存著無限感謝的一小部分。

首先，很感謝的是我親愛的父母親，正因有你們從小到大無悔付出的養育，而讓我得以獲得此次寶貴求學進修之機會與經驗；同時，也很感謝在此求知過程中，不辭辛勞地給予諄諄教誨的指導老師張俊彥導師，不管是專業領域、或是待人處事上的栽培與教導，正深深地影響著之後我所需要的一切。我人生中正因有你們如貴人般在旁的提攜與指導，才有我如今一切的我，因此除了感謝還是感謝。我也要感謝口試委員張鼎張教授、鄭晃忠教授、龔正教授、吳永俊教授、詹益仁組長、高明哲副組長與崔秉钺教授的指導與提醒，讓論文的內容更趨完善。

同時，也很感謝在課業與實驗上指導與幫忙的學長姐們、同學們以及學弟妹們，雖然我知道這種概括的寫法很簡略，但對你們感謝之心，卻正如此無法一一明列名子般之無以細數的多，而得以讓我能在學業方面順利修完課程，在實驗方面也得到很多寶貴的經驗與研究成果：學長姐當中，又想特別再次提出幾位對我直接影響重大而得鄭重感謝的人，包括陳紀文、楊宗熹、吳永俊、涂峻豪、陳世青、陳怡誠、陳致宏、郭柏儀學長等等，以及幾位跟我共同切磋的好同學，包括林昭正、陳弘斌、鄭兆欽、揚哲育、何武陵等等，學弟妹方面，包括涂博閔、王派璿、薛培堃、翁麗雯、陳弘根、李勝凱、蔡佳州、江培維、莊凱麟、張耀峰、張哲榮、林聖錡、陳緯仁、胡志瑋、王信淵、蔡侑廷、陳仕承、張冠張、陳敏甄、俞詠騰，尤書鴻，與實驗室優秀的助理等等，感謝你們一路上的陪伴與幫忙，讓我能完成這個修業學程。

最後還是在一次謝謝指導老師張俊彥老師的幫忙與指導，讓我重新認清自己的缺點，也讓我體驗到自己能力的渺小，體驗到仍有很多東西該學該做，我想這種課外的指導才是我這次學習中最有價值的東西。

2010.11

立偉

Contents

§ Chapter 1

Introduction

§ Chapter 2

Basic Principles of Resistive Switching Nonvolatile Memory

§ Chapter 3

Characteristics of thin-FeO_x-contained Resistive Switching Memory

A. Basic Characteristics

3.1. Resistive Switching Effects on a thin FeO_x Transition Layer Produced at the Oxide/iron Interface of Ti/TiN/SiO_2/Fe-contented Electrode Structures

B. Thermal Annealing Effects

3.2. Annealing Effects on the Resistive Switching Characteristics of the Ti/TiN/SiO_2/FeO_x/FePt and Ti/TiN/SiO_2/FeO_x/Fe Structures

C. Multi-Level Effects

3.3. Tunable Resistance Switching Characteristics in a thin FeO_x-transition Layer by Controlling Sweeping Voltage and Compliance Current

§ Chapter 4

※ Appendix ※

Characteristics of Titanium-based Nanocrystal Nonvolatile Memories

A.1 Formation and Composition of Titanium Oxinitride Nanocrystals Synthesized via Nitridizing Titanium Oxide

A.2 Low-temperature-synthesized Memory Characteristics of Titanium-based Nanocrystal Nonvolatile Memories by Germanium Doping

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Appendix Figure Captions

Table Captions

Chapter 1

Introduction

1.1 Overview of Nonvolatile Memory

In 1960's, due to the high cost, large volume, and high power consumption of the magnetic-core memory, the electronic industries urgently needed a new kind of memory device to replace the magnetic-core memory. In 1967, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory at Bell Labs [1.1]. Because of exhibiting several advantages, such as fast read access time, better kinetic shock resistance than hard disk and, most importantly, compatibility with the current complementary-metal-oxide-semiconductor (CMOS) process, the stacked-gate FG device structure, as shown in Fig. 1-1, becomes the mainstream nonvolatile memory (NVM) device in last few decades and is widely used in both standalone and embedded memories.

The basic operation of a FG device is that charges are injected from the silicon substrate across the tunneling oxide and stored in the floating gate by applying an appropriate gate voltage. Then, the stored charges can cause a threshold-voltage shift, and the device is at a high-threshold state (programmed). For a well-designed memory device, the stored charge can maintain in floating gate over 100 years without external power [1.1]. Moreover, the most widespread FG memory array organization is the so-called Flash memory, which has a byte-selectable write operation combined with a sector “flash” erase, and has created a huge industry of portable electronic systems, such as MP3 player, PDA, Notebook, and flash driver. Besides, the flash memory can be further classified into two types, NOR and NAND flash memories, according to their functions and advantages [1.2]. NOR Flash offers faster read speed and random access capabilities, making it suitable for code storage in devices such as PDA and cell phone. In contrast to NOR flash, the NAND memory, which offers faster write/erase capability and higher density is typically used for storing large quantities of data.

In spite of such a huge commercial success, conventional FG devices have their limitations. The most prominent one is the issue on scaling down of the tunnel oxide. According to the 2007 International Technology Roadmap for Semiconductors (ITRS) flash memory [1.3], tunnel oxide thickness must be more than 6-nm to assure enough retention time, as shown in Fig. 1-2. This basic limitation on tunnel oxide leads to a high programming/erasing voltage and low operation speed for the device. If tunnel oxide were scaling to below 2-nm, the programming/erasing voltage could be reduced to smaller than 4V. Although the thin tunnel oxide can effectively enhance the programming/erasing speed and reduce operation voltage, the thick oxide is required to guarantee the ten years retention time. Furthermore, after endurance test, traps can generate in tunnel oxide, which might induce a leak path in the tunnel oxide and results in the stored charge loss. These difficult trade-off problems hinder the scaling.

To overcome the scaling limits of the conventional FG structure, not only the charge based storage technology, such as nanocrystal NVM devices [Appendix], but also the non-charge based storage technology is researched to be the candidates for the next generation of NVMs, such as phase-change memory (PCM), magnetoresistive random access memory (MRAM), and resistive random-access memory (RRAM), exhibiting the reproducible changes of electrical resistance. RRAM, especially, has the potential to become the front runner among other non-volatile memories. Compared to PRAM, RRAM operates at a faster timescale (switching time can be less than 10 ns), while compared to MRAM, it has a simpler, smaller cell structure (less than $8F^2$ MIM stack). Compared to flash memory and racetrack memory, a lower voltage is sufficient and hence it can be used in low power applications. Moreover, ITRI has recently shown that RRAM is scalable below 30 nm. It is believed that if a filament is responsible, it would not exhibit direct scaling with cell size.

1.1.1 Resistive Random Access Memory Devices

Resistive random access memory (RRAM) is also one of possible candidates for the next generation nonvolatile memory devices. RRAMs use of the resistance changes as different memory states. By electrical field or current effects, the conductivity could be switched between high and low resistance reproducibly, so such the bistable resistance states could be represented to different digital states as a memory device. The advantages of RRAM are with high cell density array, high operation speed, low power consumption, high endurance and lower scale limit. Moreover, RRAMs have the features of nonvolatility, long retention time, and non-destructive readout.

The basic structure for RRAM is made up of only metal-insulator-metal (M-I-M), which could be further integrated into 1D1R (a diode and a resistor) or 1T1R (a transistor and a resistor) structures [1.4-1.5]. The top and bottom electrodes could be made by metals or conducting transition metal oxides [1.4], the choice of which would impact on the resistive switching properties because of their different crystallinities, work functions and ability of oxygen gettering [1.6-1.8]. On the other hand, the main character of resistive switching is the insulator layer sandwiched between the electrodes. The insulator for the M-I-M structure may be not really insulating, but also semiconducting, depending on its composition and stoichiometry [1.9]. The insulator would be called "resistance switching layer" in the following sections. The different quality connected with different deposition methods would also affects the resistive switching characteristics [1.10].

Resistive switching phenomena have been discovered in many materials and now the research mainstream is concentrated on groups of binary oxides, such as TiO_2 [1.11], ZrO_2 [1.12], NiO [1.13], Al_2O_3 [1.14], Cu_xO [1.15], Fe_2O_3 [1.16], ZnO [1.17], HfO_2 [1.8], SiO_2 [1.18, 1.19] and MoO_x [1.20], perovskite oxides, such as Cr-doped $SrTiO_3$ [1.10], Cr-doped $SrZrO_3$ [1.21], and $Pr_{0.7}Ca_{0.3}MnO_3$ [1.22], manganites, and organic/polymers. Of note, the binary oxides adopted in RRAM application are candidates or have been widely used in other field of CMOS devices. Thus, the compatibility with modern CMOS process would not be a serious issue. Moreover, these binary oxides have such simple element components that it could be easier to control the proportion of metal and oxygen composition.

1.2 Motivation

As mentioned above, because of facing the scaling limits of the conventional FG structure, works on researching the most probable candidate for the next generation of NVMs are studied in this dissertation, i.e. non-charge based storage structure. For non-charge storage structure, resistive switching effects on a thin FeO_x transition layer produced at the oxide/iron interface of TiN/SiO_2/Fe-contented electrode structures are demonstrated. It is because that the switching effect of FeO_x was proposed as a redox reaction between nonstoichiometric compounds of iron oxides, which takes place locally near the electrode region. In addition, because of the ease of oxidation of iron atoms, we provided a method to produce a nonstoichiometric FeO_x layer, the critical resistance switching layer, near the electrode region simply for RRAM applications by depositing a plasma-enhanced tetraethyl orthosilicate oxide onto the Fe-contented electrode to form a $SiO_2/FeO_x/$ Fe-contented electrode structure. Moreover, thermal annealing effects and multi-level effects of such a FeO_x transition layer are also studied at the same time.

1.3 Organization of the dissertation

This dissertation is divided into four chapters. The contents in each chapter are described as follows.

In chapter 1, general background of resistive switching nonvolatile memory devices is introduced.

In chapter 2, operation method of resistive switching nonvolatile memory devices is briefly described as well as their basic physical characteristic and mechanism. Furthermore, reliability discussions are also mentioned in this chapter.

In chapter 3, memory characteristic researches on thin-FeO_x-contained resistive switching memories, where the thin FeO_x layer is a produced at the interface between oxide/iron transition region by a Fe-contented-electrode of an Metal-Insulator-Metal structure, i.e. a sandwiched TiN/SiO_2/Fe/Pt or TiN/SiO_2/FePt structures, are studied, including three main sections: (a) Basic characteristics to demonstrate resistive switching effects on a thin FeO_x transition layer produced at the interface of SiO_2/Fe and SiO_2/FePt structures, including resistive switching properties, insulator thickness effects, area size effects, and bubble effects; (b) Thermal annealing effects to demonstrate improvements of resistance switching characteristics in a thin FeO_x-transition-contained structure as well as the mechanism by discussing the reliability and statistic characteristics; and (c) Multi-level effects to demonstrate tunable resistance switching characteristics in a thin FeO_x-transition layer by controlling sweeping voltage and compliance current.

Finally, the summarization of all experimental results in this dissertation and the suggestions for the future work are presented in chapter 4.

Besides, in the appendix, memory characteristic researches on titanium-based nanocrystal nonvolatile memories, titanium oxinitride nanocrystals synthesized via nitridizing titanium oxide, are demonstrated, including formation, composition, and electric properties. In addition, research on lowering the synthesis temperature of Titanium-based nanocrystal by Germanium doping for nonvolatile memory application is also demonstrated.

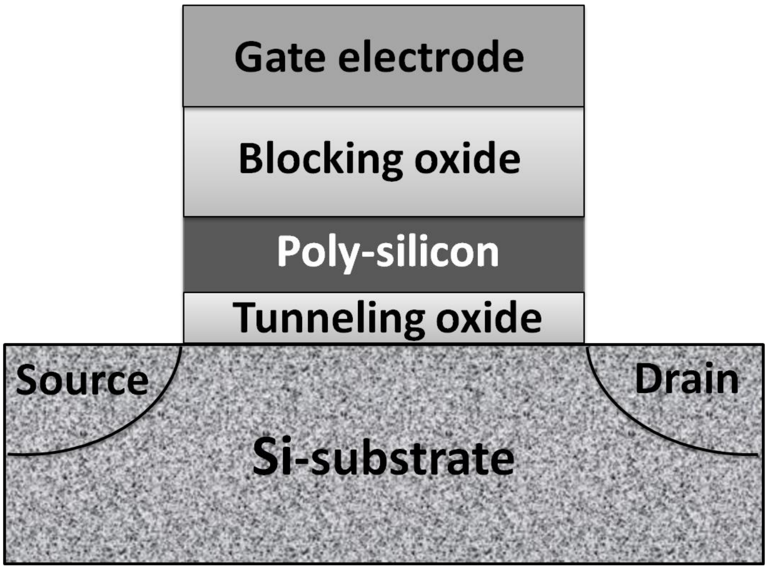
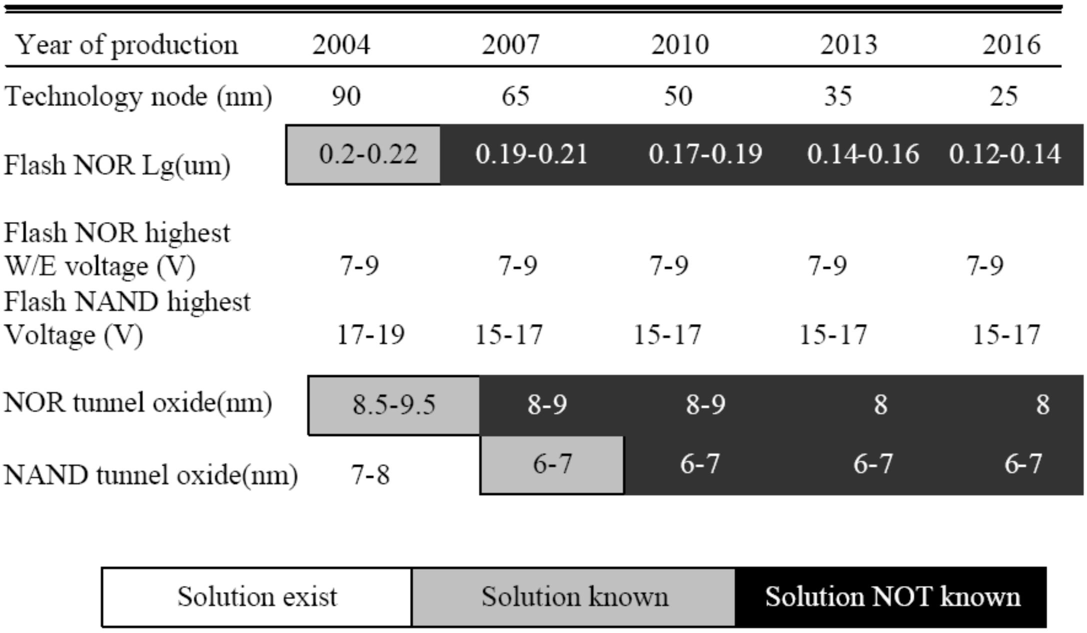


Fig. 1-1 Structure of a conventional floating-gate nonvolatile memory device. The floating-gate device is constructed by the MOSFET device with a modified gate stack (tunnel oxide/floating gate/blocking oxide/gate electrode), where the floating gate is fabricated by an electronically continuous poly-silicon layer and is employed as the charge storage media.



Year of production	2004	2007	2010	2013	2016
Technology node (nm)	90	65	50	35	25
Flash NOR Lg(um)	0.2-0.22	0.19-0.21	0.17-0.19	0.14-0.16	0.12-0.14
Flash NOR highest W/E voltage (V)	7-9	7-9	7-9	7-9	7-9
Flash NAND highest Voltage (V)	17-19	15-17	15-17	15-17	15-17
NOR tunnel oxide(nm)	8.5-9.5	8-9	8-9	8	8
NAND tunnel oxide(nm)	7-8	6-7	6-7	6-7	6-7

Solution exist	Solution known	Solution NOT known

Fig. 1-2 Tunnel oxide and operation voltage scaling predicted by the 2007 International Technology Roadmap for Semiconductors.

Chapter 2

Basic Principles of Nonvolatile Resistive Switching Memory

2.1 Material Sources of Resistive Switching Memory

Resistance switching in metal-insulator-metal (M-I-M) structures has been a long standing problem in materials and device physics for 40 years. To date, many materials with resistance switching characteristics have been widely demonstrated, which could be simply grouped into perovskite oxides, such as Cr-doped $SrTiO_3$ [2.1], Cr-doped $SrZrO_3$ [2.2], and $Pr_{0.7}Ca_{0.3}MnO_3$(PCMO) [2.3] $La_{1-X}Ca_XMnO_3$ (LCMO), transition metal oxides, such as FeO_x [2.4], ZrO_x [2.5], TiO_2 [2.6], NiO [2.7] , Cu_xO [2.8], HfO_2 [2.9] and $(Pr,Ca)MnO_3$ [2.10], organic polymer materials [2.11], solid-state electrolyte (programmable metallization cell), such as $Cu:SiO_2$, $Ag:TiO_2$, $Cu:Ta_2O_5$, Ag:CuS, and Ag:GeSe, rare-earth metal oxide, such as Gd_2O_3 [2.12], CeO_2 [2.13] and even SiO_2 [2.14], Al_2O_3 [2.15]. However, the resistance switching mechanisms are not well understood and identified yet. Therefore, more and more researches on resistance switching are still investigated recently.

2.2 Operation Characteristics of Resistive Switching Memory

Figure 2-1, for example, shows (a) a typical unipolar and (b) a bipolar current-voltage operation characteristic of an initial-stated (as-prepared sample) resistive switching memory for (1) forming, (2) reset, and (3) set processes [2.16, 2.35]. It is found that after the forming process, which is required to initiate the resistive switching properties of oxide films, a basic writing/erasing operation (or named set/reset process) of bistable resistive switching in one cell could be achieved by DC sweeping or pulse modes. First, if the resistance state of a RRAM cell is held in a high resistance state (HRS), the current of the cell would increase during DC bias sweeping over a threshold voltage (or a switching voltage). Then, the resistance exchanges from the HRS to a low resistance state (LRS), which is defined as a process of “set”. Furthermore, when DC bias sweeps again, the LRS would switch back to a HRS, associated with an enormously current drop after a switching voltage. Then, the resistance exchanges from the LRS to a HRS again, which is defined as a process of “reset”. On the other hand, for reading operation, the bias should not exceed the switching voltage to keep the expected “set” or “reset”, preventing the memory state from variation.

Details of forming voltage, unipolar, bipolar characteristics and even circuit realization will discuss in the next sections. Of note, in order to unify the operation parameters in the following text, the “set” and “reset” would be used to describe the switching operation; “V_{set}”, “V_{reset}”, “R_{LRS}” and “R_{HRS}” would be used to describe the set voltage, reset voltage, the resistance at low resistance state (LRS) and the resistance at high resistance state (HRS), respectively. The V_{set} and V_{reset} represent the voltage where set and reset processes begin to occur, and R_{LRS} and R_{HRS} were measured at V = 0.2 V for LRS and HRS, respectively.

2.2.1 Forming Process

Before the resistive switching characteristics are observed to exhibit, a “forming process” or a “conditioning process” is necessary to activate the resistive memory devices, i.e. the first transition of resistive switching materials from highly insulating to a more conductive state. The forming process needs a high-voltage stress ($V_{forming}$) applied on the pristine device to change the local microstructure or morphology of the RRAM device and form the conduction paths (also named inner conducting filaments), which is equivalent to dielectric breakdown reported by Kinoshita et al., between top and bottom electrodes. For short, the forming process is similar to soft breakdown, leading to the conducting paths (filaments) composed of clusters of point defects as shown in figure 2-2 [2.18] and figure 2-3 [2.19]. The stoichiometry and the thickness of the resistive memory film have been reported to have influences on $V_{forming}$ [2.18]. The forming process, according to previous studies [2.19-2.21] could be considered as a high-voltage process that drives the migration of oxygen ion, oxygen vacancies, or anode material to modify the anode region or the whole memory device. It should also be noted that both the polarity of the forming voltage seems to induce a LRS for the unipolar device, which was considered as typical soft breakdown of the insulator. However, for the bipolar device, it was reported by by J Joshua Yang, et al. that the electric field polarity repels the growing vacancy channels from touching the top electrode—the Schottky-like barrier is not heavily reduced after forming and the post-forming state is OFF. In other words, the conducting channel penetrates the bulk film but *not* the Schottky-like interface region [2.35]. Therefore, the forming process could induce the bipolar device to either a LRS or a HRS, depending on which side the interface barrier is.

2.2.2 Unipolar (or Nonpolar)

Figure 2-4 shows a typical unipolar *I-V* plot under DC sweep operation. Unipolar means the operation of switching is independent on the polarity of the voltage and current signal. In unipolar system, the low-resistance state (ON state) is switched (“turn OFF”) into the high-resistance state (OFF state) by sweeping to over a reset voltage, which needs to be below the set voltage and with the compliance current condition (1→2 or 1’→2’). On the other hand, the unipolar system in its high-resistance state (OFF state) is switched (“to turn ON”) into the low-resistance state (ON state) by sweeping to over a set voltage (3→4 or 3’→4’). It should be noted that this operation requiring same voltage polarities to switch, whether positive on/positive off or negative off/negative on. Because we could switch device resistance with the same or reversed voltage polarity in unipolar resistive switching, therefore the unipolar switching is also called nonpolar resistive switching. The unipolar resistive switching is thought to be the fuse/antifuse of conduction paths or filaments. The unipolar switching usually has much larger resistance change than the bipolar switching, and this makes it much easier to read the memory state. In addition, devices using unipolar switching can be potentially integrated in higher density. This type of switching behavior has been observed in many highly insulating oxides, such as binary metal oxides.

2.2.3 Bipolar

Figure 2-5 shows a typical bipolar *I-V* plot under DC sweep operation. Bipolar means the operation of the set to the ON state occurs at one voltage polarity, and the reset to the OFF state take place on reversed voltage polarity, i.e. this operation requiring different voltage polarities to switch, whether negative on/positive off or negative off/positive on. In figure 2-4, for example, the low-resistance state (ON state) is switched (“turn OFF”) into the high-resistance state (OFF state) by a negative voltage sweeping to over a reset voltage (1→2→3). On the other hand, the bipolar system in its high-resistance state (OFF state) is switched (“turn ON”) into the low-resistance state (ON state) by a positive voltage sweeping to over the set voltage (4→5→6). The mechanism of bipolar resistive switching is considered to be the migration of anions. This type of resistive switching behavior occurs with many semiconducting oxides, such as complex perovskite oxides.

2.2.4 Circuit Realization

In the real circuits, it is the pulse mode switching that is the practical operation method due to fast operation speed and lower power consumption. Ideally, operation sequences of set/reset voltage pulses and the corresponding respondent current for unipolar and bipolar switching are schematically shown in figure 2-6(a) and (b), respectively [2.22]. For example, the waveforms of set and reset process to operate a RRAM device were demonstrated in figure 2-7(a) and (b), respectively [2.7]. The other example is also shown in figure 2-8 [2.23]. The pulse heights and widths for set and reset must take a balance. The larger the pulse height is, the shorter the pulse width is needed. The reading pulses with small pulse heights are also designed in order not to vary the memory states.

For simplicity, a layout of the RRAM array structure is schematically illustrated in figure 2-9, which contains the word lines crossed with the bit lines. For realization applications, the 1D1R (1 diode and 1 resistor) or the 1T1R (1 transistor and 1 resistor) structure must be used to prevent misreading as shown in figure 2-10 and figure 2-11, respectively. I. G. Baek *et al.* [2.7] reported that if a cell is in high resistance state and its neighboring cells are in low resistance state, it will be misread as low resistance state due to the leakage current path around its neighboring cells as shown in figure 2-12 [2.24]. Hence, a rectifying element is required for each cell in an array to limit the current paths. The minimum sizes for the 1D1R and the 1T1R structures are $4F^2$ and $6F^2$ respectively, and these structures would meet the requirement for high density arrays.

2.3 Basic Conducting mechanisms of Resistive Switching Memory

Based on conductivity, transition metal oxides could be insulator, semiconductor or metal depending on the composition of the oxide materials. Hence the conducting mechanisms may vary because of their different physics and chemistry characteristics. The most discussed materials in RRAM application generally belong to insulator or semiconductor according to the constitution and stoichiometry, and the electron conduction mechanisms mostly involved are Ohmic conduction, space charge limited current, Schottky emission, Frenkel-Poole emission and Tunneling. Furthermore, the current fitting procedure would give insight into the conduction mechanisms.

2.3.1 Ohmic conduction

Ohmic conduction takes place when the injected carrier density is far less than the thermally-generated carrier density. Generally, it applies to the condition of low electric field region in which thermally-generated carriers are dominant in conduction. The current-voltage characteristics follow Ohm's law that the current passing through a resistor from one terminal to the other is proportional to the voltage drop across the two points. In addition, the temperature effect is also described in Ohmic conduction behavior. Due to the electron and phonon scattering effects, the conductivity rises with increasing temperature for conduction in semiconductor, while with decreasing temperature for metal conduction. The following is the expression for Ohmic conduction:

$$J = aV\exp\left(\frac{c}{T}\right)$$

where a (and c) is constant, and V is the applied voltage.

2.3.2 Space charge limited current

The mechanism of space charge limited current (SCLC) is attributed to defects and usually exists in the dielectric stressed by high electric fields. After charge injection from an electrode, the space charge may form if the charge carriers are trapped and distributed over a region of area without being neutralized. The further flow of charge carriers would be impeded by this space charge region. It should be noted that the injected carriers are mostly electrons. As for conductive media, the trapped carriers are able to be neutralized or screened rapidly; therefore the space charge region would not form.

The complete trapped controlled SCLC mechanism is composed of two stages [2.6], trap-unfilled SCLC and trap-filled SCLC, both can be written as the following expression:

$$J = \left(\frac{\theta}{\theta+1}\right)\frac{9}{8}\varepsilon_r\varepsilon_0\mu\frac{V^2}{L^3}$$

where J is the current density, θ is the ratio of free electron to trapped electron, N_C is the effective density of states in the conductive band, Nt is the number of emptied electron traps, ε_0 is the permittivity of free space, ε_r is the static dielectric constant, μ is the electron mobility, V is the applied voltage and L is the film thickness. At first stage, the traps are not filled with charges and the formula can be rewritten with θ <<1 as the following:

$$J = \theta\frac{9}{8}\varepsilon_r\varepsilon_0\mu\frac{V^2}{L^3}$$

As the voltage increases, the majority of traps are occupied by the injected carriers, and the current-voltage characteristics can be again rewritten with θ >>1:

$$J = \frac{9}{8}\varepsilon_r \varepsilon_0 \mu \frac{V^2}{L^3}$$

2.3.3 Schottky emission

Schottky emission is mainly attributed to the Schottky contact of the metal-insulator interface. For the carriers to transport, they must jump across the barrier height of one of the interfaces, travel through the dielectric film, and eventually reach the other side. It is the thermionic emission that enables the carriers (mostly electrons) to overcome the interface barrier height. Therefore temperature is the key factor that energetic carriers (hot carriers) are easier to jump across the barrier. The formula of Schottky emission is expressed as below:

$$J = A^{*}T^{2}\exp\left(\frac{-q\left(\phi_b - \sqrt{qV/4\pi\varepsilon_r\varepsilon_0 d}\right)}{kT}\right)$$

where A* denotes Richardson constant, Φ_b is the Schottky barrier height, ε_0 is the permittivity of free space, ε_r is the dynamic dielectric constant, V is the external applied voltage and d is the insulator thickness.

2.3.4 Frenkel-Poole emission

Frenkel-Poole emission is pretty much similar to Schottky emission mechanism. The main differences are that Frenkel-Poole emission describes the process for carriers to overcome the barriers resulted from the defect states in the dielectric material, and the barrier lowering is twice as large as that in Schottky emission mechanism. Temperature is also crucial for this carrier transportation process, while electric field plays a more important role in this mechanism than in Schottky emission, which suggests that field effects have greater impact on defect-related behavior. The current-voltage relationship can be written as the following formula:

$$J = BV \exp\left(\frac{-q(\phi_t - \sqrt{qV/4\pi\varepsilon_r\varepsilon_0 d}}{kT} \right)$$

where B is a material-related constant, Φ_t is the trap level, and other parameters are the same as those in Schottky emission.

2.3.5 Tunneling

Tunneling is the most common conduction mechanism through insulators under high fields. The tunnel emission is a result of quantum mechanism by which the electron wave function can penetrate through a potential barrier. It has the strongest dependence on applied voltage but is essentially independent of the temperature. Tunneling mechanism can be divided into direct tunneling and Fowler-Nordheim tunneling where carrier tunnel through a partial width of the barrier. The current-voltage relationship can be written as the following formula:

$$\mathrm{J} \propto \xi_{\mathrm{i}}^{2} \exp\left[-\frac{4\sqrt{2\mathrm{m}^{*}}(\mathrm{q}\phi_{\mathrm{B}})^{3/2}}{3\mathrm{q}\hbar\xi_{\mathrm{i}}} \right] \propto \mathrm{V}^{2} \exp\left(\frac{-\mathrm{b}}{\mathrm{V}}\right)$$

where ξ_i is the electric field in insulator, m^* is the effective mass, ϕ_B is the berrier height, and V is the applied voltage.

2.4 Switching Characteristics and Models of Resistive Switching Memory

The major possible models having been proposed by other research groups are sorted partially as two parts, one is filament-type resistance switching and the other is interface-type resistance switching [2.16]. The two models may be applied for some combinations of electrodes and oxide materials. However, these models are mainly derived by indirect observation or electrical measurements, but the switching mechanisms are not still well known because of having less direct and striking evidences to prove.

2.4.1 Filament-type resistive switching

The filament-type model comes from the nature of oxide breakdown and integrity that defects existing in an oxide bulk, such as the interstitials, oxygen vacancies and metals constitute the leakage current path, indicated in figure 2-13 [2.25]. This model has been proposed since 1970’s and is one of the earliest models in resistive switching mechanism [2.26, 2.27]. Recently, since nonvolatile memories have obtained a lot of attention, the further and more detailed studies have been realized to investigate the possible mechanisms. Among these proposed models, it is almost the filament-type model that prevails in many of binary oxide films, such as TiO_2 [2.6], ZrO_2 [2.5], NiO [2.7] and Cu_xO [2.8] and even in solid electrolyte, such as Ag-Ge-S shown in figure 2-14 [2.28]. The most obvious evidences for the filament-type model are conductive atomic force microscopy (CAFM) mapping results at low resistance state. C-AFM is one of the power tools to study the local conductivity throughout the film. B. J. Choi *et. al.* and J. Y. Son *et. al.* reported that by scanning the film surface with CAFM, only several conductive points exist and account for the current conduction, as shown in figure 2-15 [2.29] and figure 2-16 [2.30]. Fortunately, K. Fujiwara *et. al.* reported the observation of the a filamentary conducting path in a CuO film between Pt electrodes by Scanning electron microscope as shown in figure 2-17, providing the experimental reality of the conducting filament for the filament-type model [2.31]. Generally, the switching transformation of the filament-type model between the LRS and HRS is naively considered to be an abrupt transformation, causing the correspondence of abrupt-changed current from LRS (or HRS) and HRS (or LRS) during the voltage sweeping. Moreover, the filament-type model could also be affirmed by the independent electrode area relationship to resistance values (both the HRS and LRS).

As shown in figure 2-18, the resistance of NiO memory cells is almost independent of the area, suggesting that resistive switching is a local phenomenon, i.e. the filament-type phenomenon [2.32].

2.4.2 Interface-type resistance switching

The interface-type resistance switching model is wide-spreading especially in the material system of PCMO [2.33] and Nb;STO [2.34]. This model can be further classified into two types in accordance with the type of semiconductor, the n-type semiconductor and p-type semiconductor. As shown in figure 2-19 [2.16], when the number of oxygen vacancies in the oxide layers is reduced, the Ti/PCMO/SRO cells converted to a LRS and the SRO/Nb:STO/Ag cells converted into a HRS. It is because that in p-type oxide semiconductors, oxygen vacancies are considered to be an acceptor scavenger. Therefore, the reduction in oxygen vacancies at the interfaces upon annealing may cause the depletion layer to become narrower in PCMO, resulting in a decrease in the contact resistance. On the other hand, since an oxygen vacancy acts as an effective donor in n-type oxide semiconductors, the reduction in the number of oxygen vacancies may cause the depletion layer to become wider in Nb:STO, resulting in an increase in the contact resistance. For example, the schematic for p-type semiconductor (Ti/PCMO/SRO cell) is illustrated in figure 2-20 [2.16].

Generally, the switching transformation of the interface-type resistance switching model between the LRS and HRS is also naively considered to be an smooth and gradual transformation, causing the correspondence of gradual-changed current from LRS (or HRS) and HRS (or LRS) during the voltage sweeping. Moreover, the interface-type resistance switching model could also be affirmed by the dependent electrode area relationship to resistance values (both the HRS and LRS). As shown in figure 2-18, the resistance of Nb-doped $SrTiO_3$ memory cells depends linearly on the area, suggesting that the resistive switching takes place over the entire area of the interface, i.e. the interface-type resistance switching phenomenon.

2.5 Reliability: Retention and Endurance

Unlike to logic IC, nonvolatile memory is more concerned with reliability than performance. The reliability includes two parts, retention and endurance. Both reliability tests are very important for nonvolatile memory application in the portable electronic productions market and they are also a kind of specifications to define the charge loss phenomena during a long-term usage. In general, nonvolatile memory must be able to bear 100K-1M program/erase operation cycles (endurance), and can keep the stored data at least 10-year long (retention).

Because non-charge-based nonvolatile memory is related to the complex chemical reactions, such as redox between nonstoichiometric compounds, diffusion of ions, and phase change of materials, deviation of the operation voltage and variation of high and low resistance state values are the most concerned reliability issues for a RRAM device. Moreover, different materials could exhibit different resistive switching mechanisms. To date, therefore, RRAM reliability could be discussed case by case, depending on what kind of material and mechanism it is. In general, there are still some required specifications for nonvolatile memory applications introduced as following:

(a) Retention

For nonvolatile memory, the data information must be conserved over than ten years. This means that the charge loss rate have to be as low as possible. One possible origin of charge loss is through the degradation of the film materials, which may be responsible for time and temperature dependent on retention behavior of nonvolatile memory devices. The retention capability of nonvolatile memories are usually examined by using accelerated tests that usually adopt screening electric fields and hostile environments at high temperature.

(b) Endurance

Endurance is a number of erase/write operations. Generally speaking, Flash products are specified for 10^6 erase/program cycles. Nevertheless, the endurance requirement may be relaxed with the increase of memory density for the other applications. The endurance requirement is relaxed to 100K cycles for 256 MB memory. In the higher density, a certain cell in a block has less possibility to be written and erased since the memory operation on the cell is repeated after using up the whole memory blocks. The endurance requirement is sufficient for the user to take 700 photos with a 1MB size every day for 10 years.

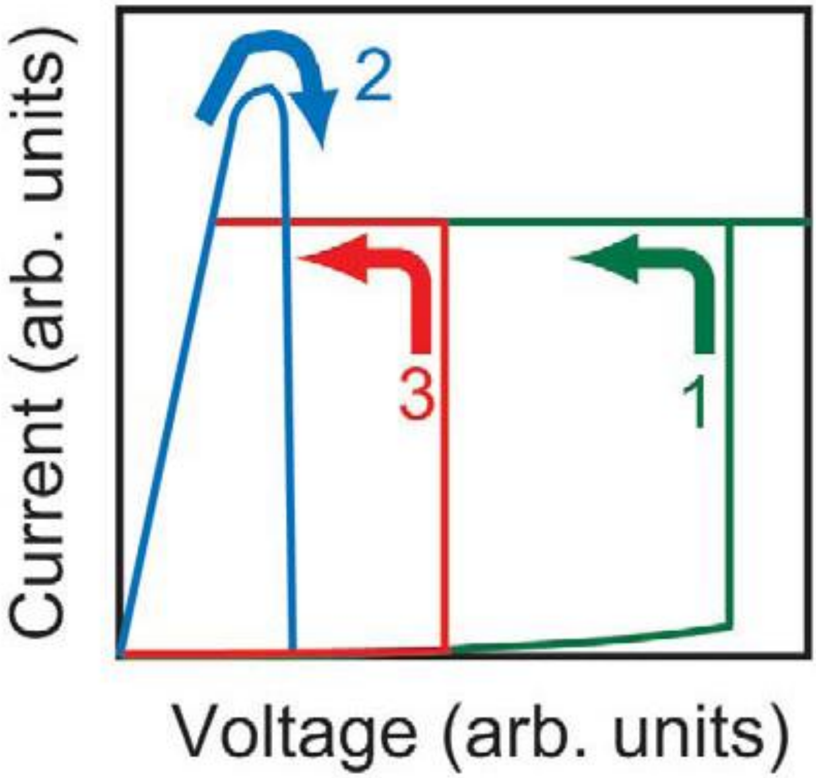


Fig. 2-1(a) A typical unipolar current-voltage operation characteristic of an initial-stated (as-prepared sample) resistive switching memory for (1) forming, (2) reset, and (3) set processes. [2.16]

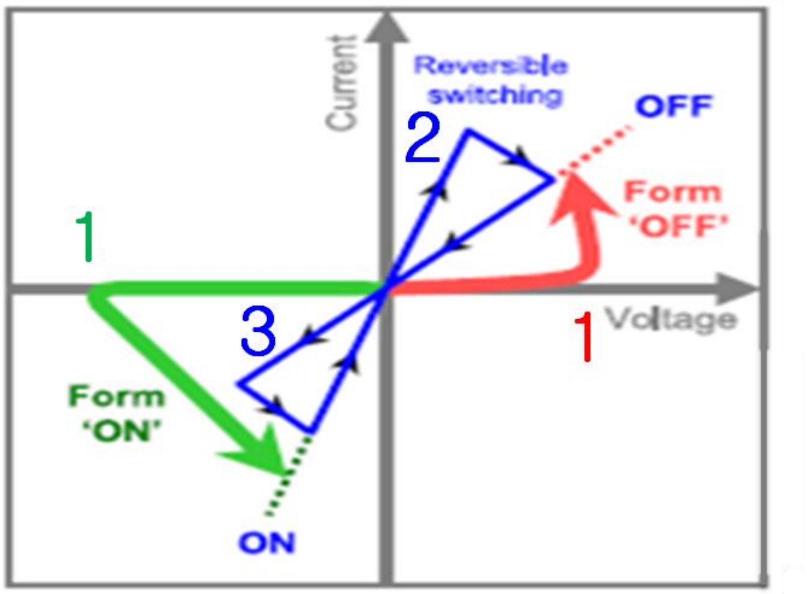


Fig. 2-1(b) A typical bipolar current-voltage operation characteristic of an initial-stated (as-prepared sample) resistive switching memory for (1) forming, (2) reset, and (3) set processes. [2.35]

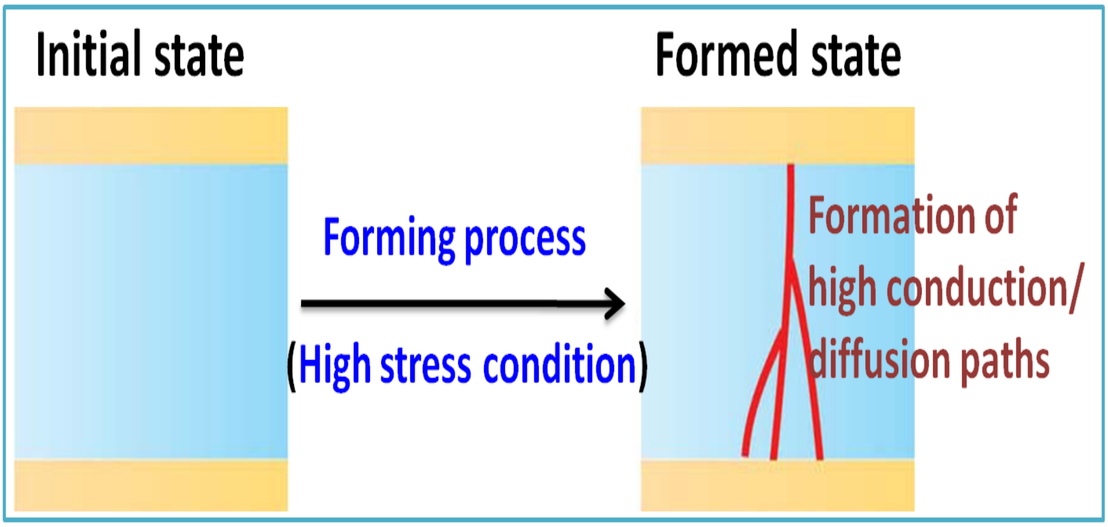


Fig. 2-2 Schematics of an initial state (as-prepared sample) and a formed state after the forming process. [2.16]

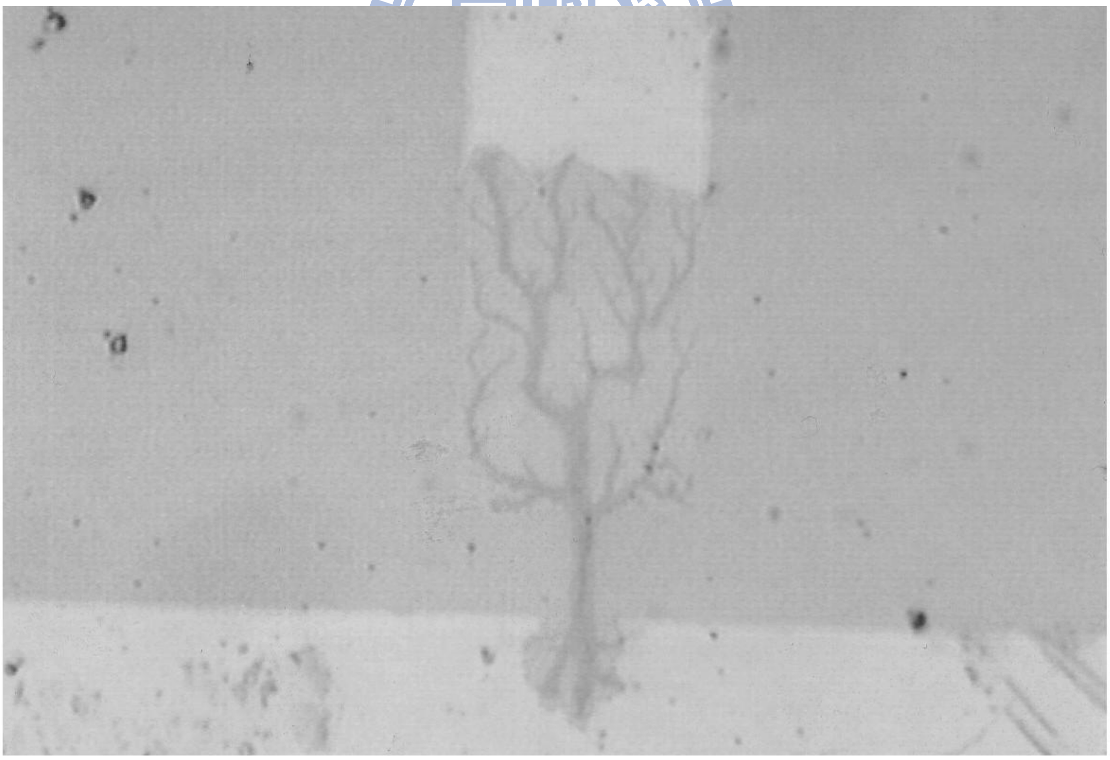


Fig. 2-3 Optical image from the filamentary region. This is a typical breakdown filament. [2.17]

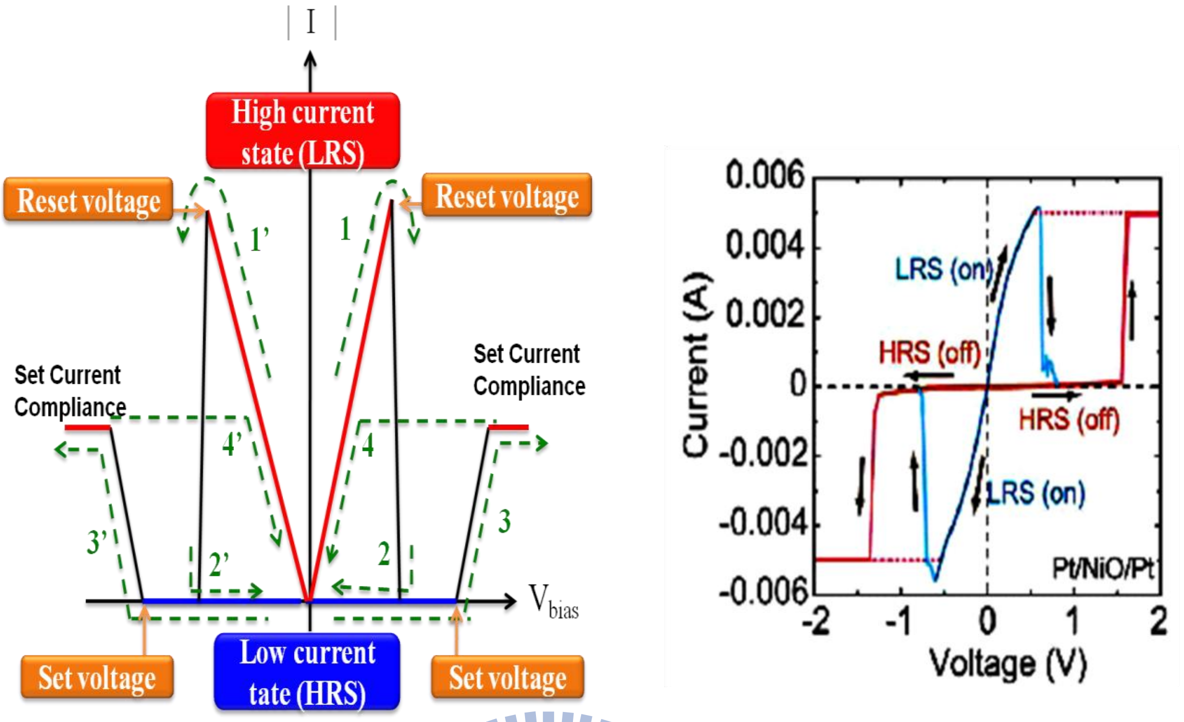


Fig. 2-4 Typical unipolar I-V curves of RRAM switching in voltage sweeping mode [2.16].

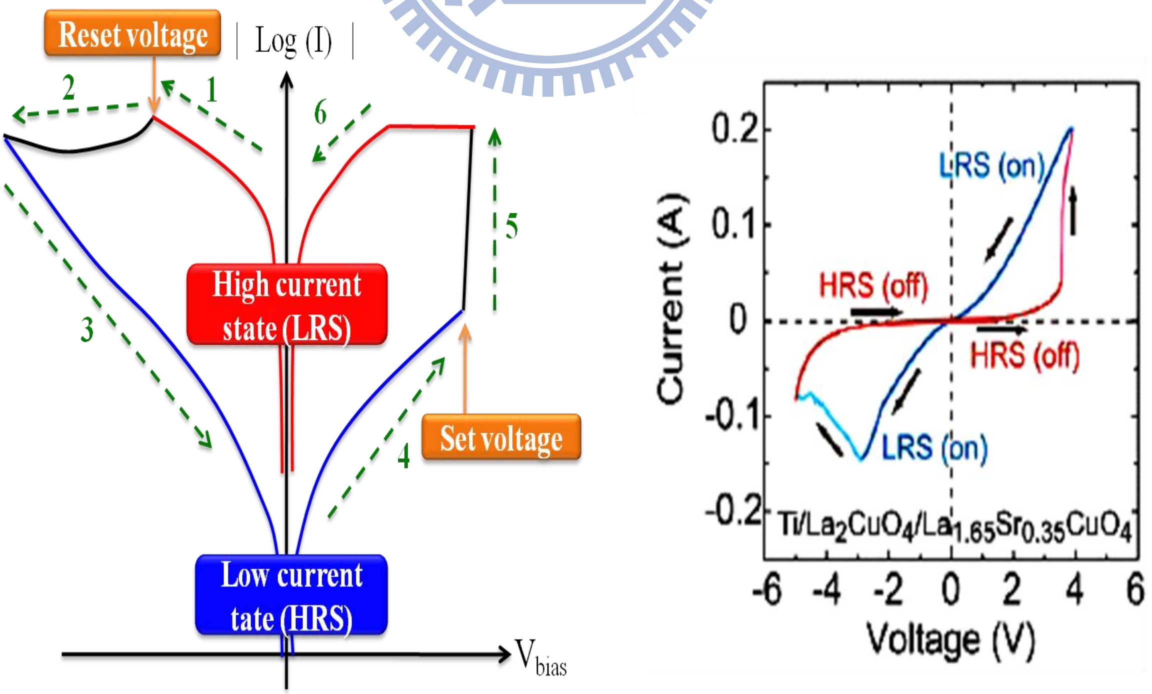


Fig. 2-5 Typical bipolar I-V curves of RRAM switching in voltage sweeping mode. [2.16].

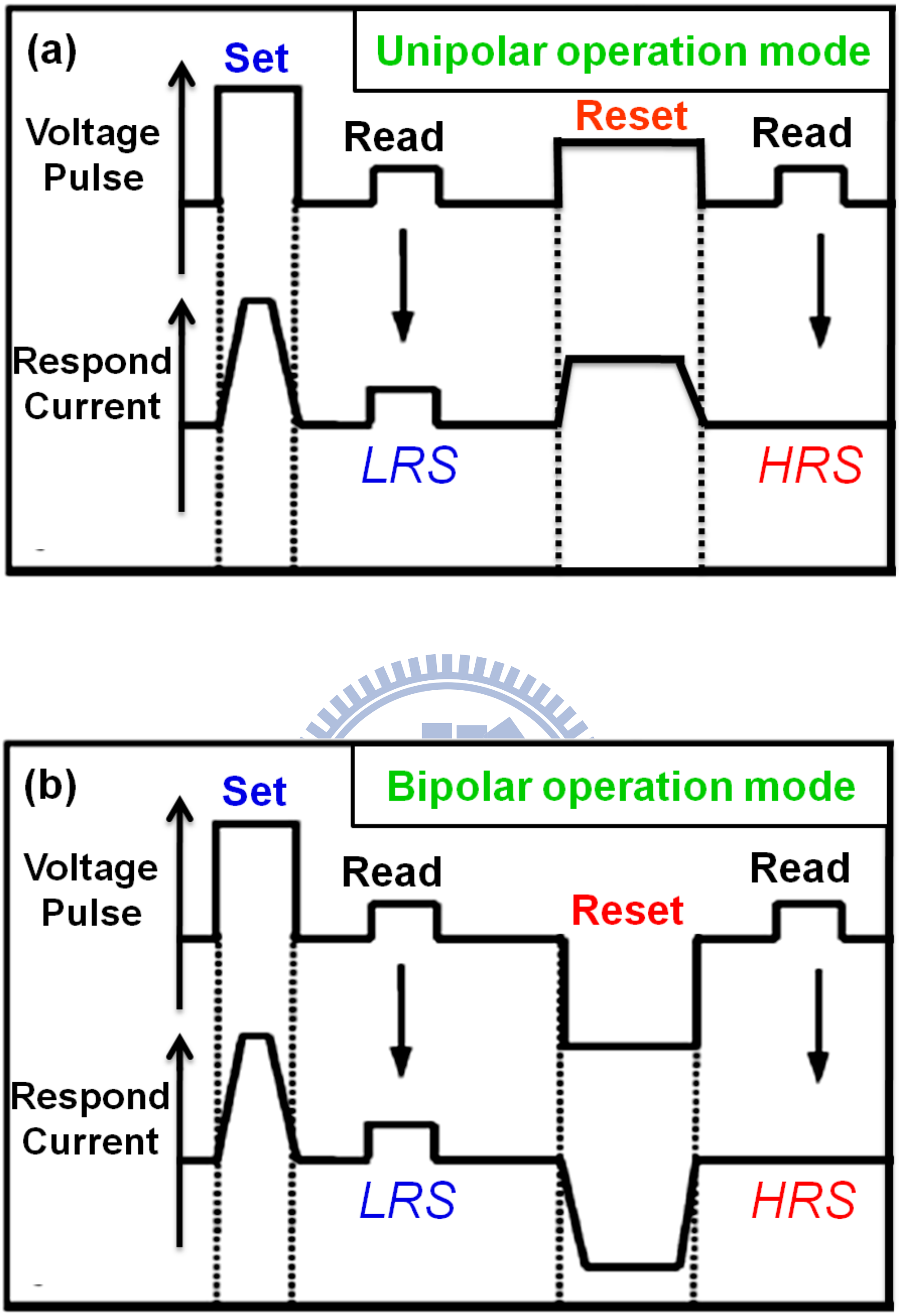


Fig. 2-6 Schematic operation sequences of set/reset voltage pulses and the corresponding respondent current for (a) unipolar and (b) bipolar switching. [2.22]

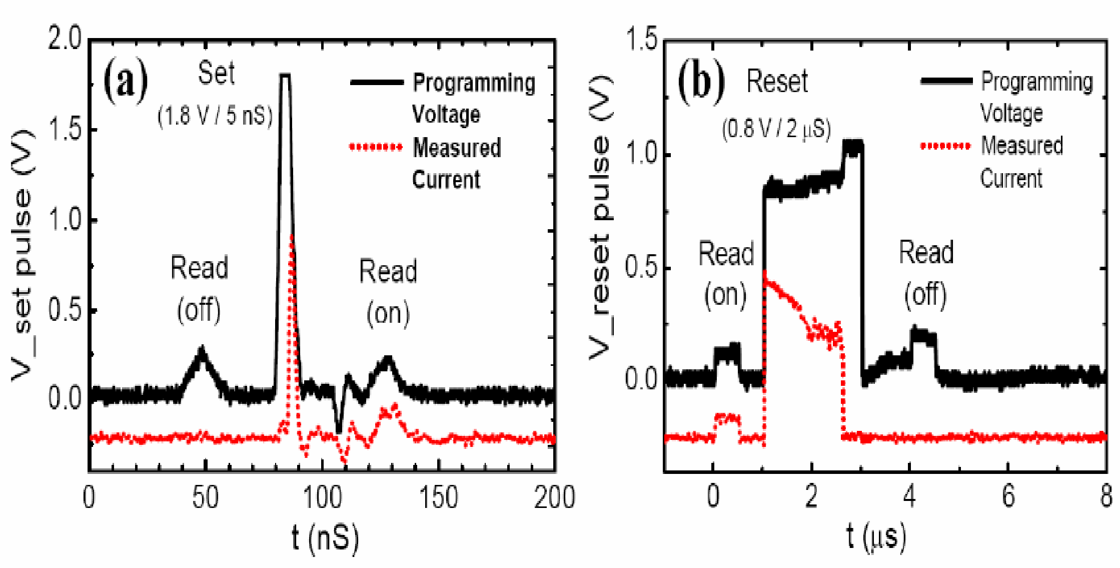


Fig. 2-7 Switching dynamics monitored with programming and reading pulses. Pulse waveforms and transition for (a) set process and (b) reset process [2.7].

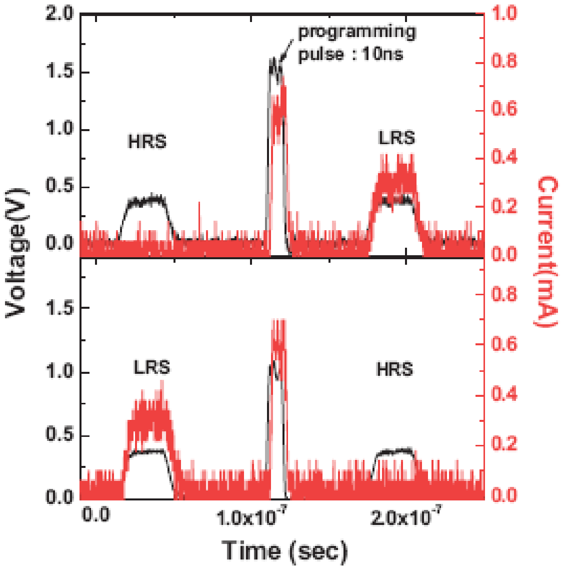


Fig. 2-8 (a) Characteristic 0.4 V monitoring pulses with the programming pulse in between (black line), and switching from HRS to LRS induced by a single 1.5 V pulse with a 10 ns duration (red line). (b) Switching from LRS to HRS driven by a single reset 1 V pulse with a 10 ns duration. [2.23]

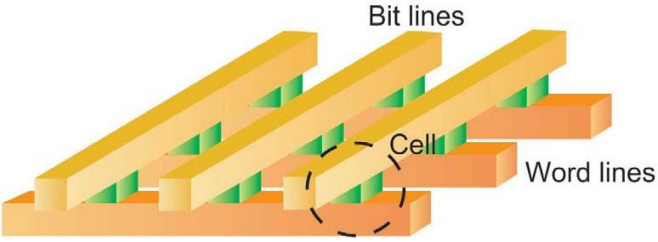


Fig. 2-9 Conceptual schematic of a RRAM memory array layout [2.16].

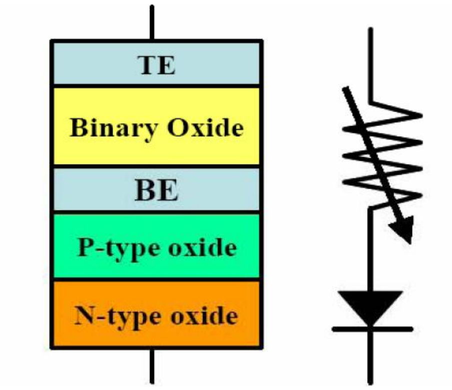


Fig. 2-10 Conceptual schematic cell unit composed of 1D1R structure [2.7].

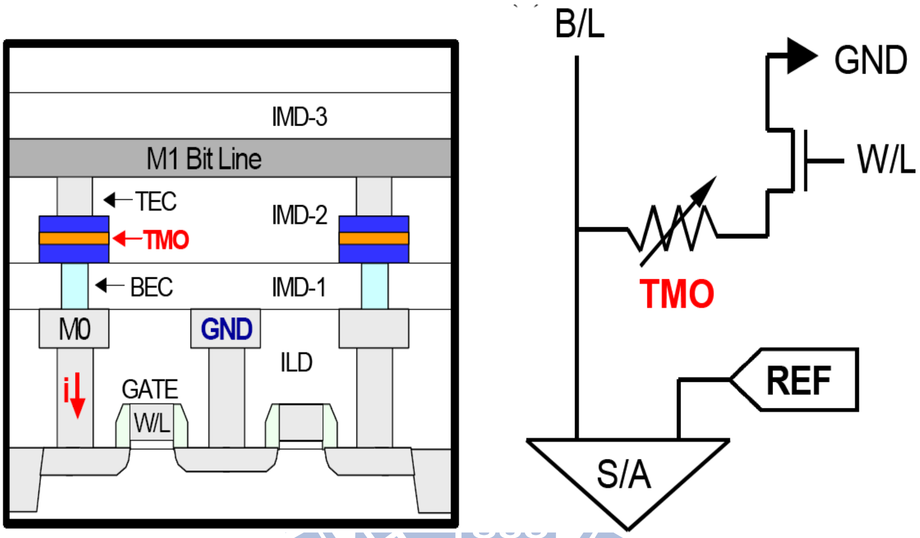


Fig. 2-11 Cross-sectional schematic and basic circuit diagram of cell unit composed of 1T1R structure [2.18].

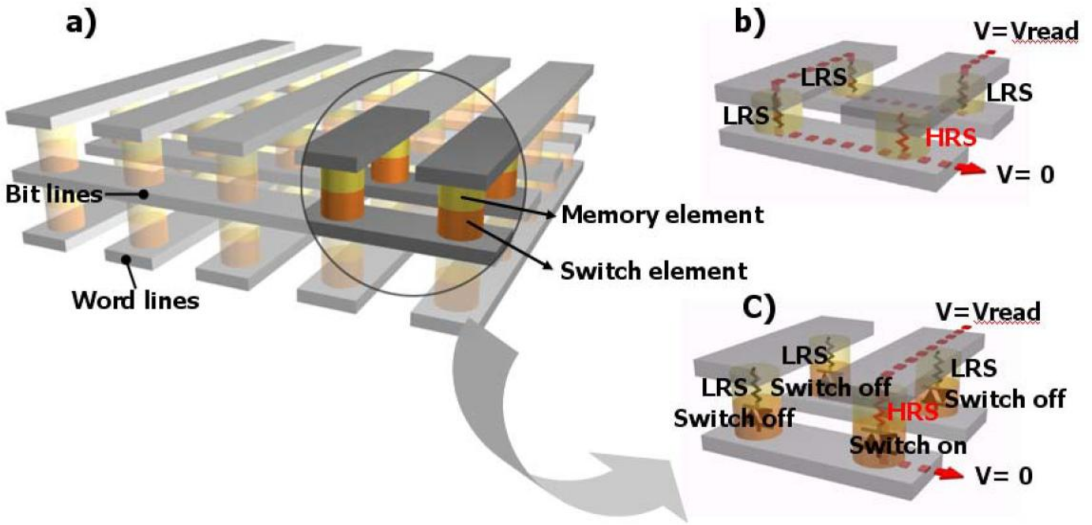


Fig. 2-12 (a) Generalized cross-point structure with memory and switching elements. (b) Reading interference without switch elements. (c) Rectified reading operation with switch elements [2.24].

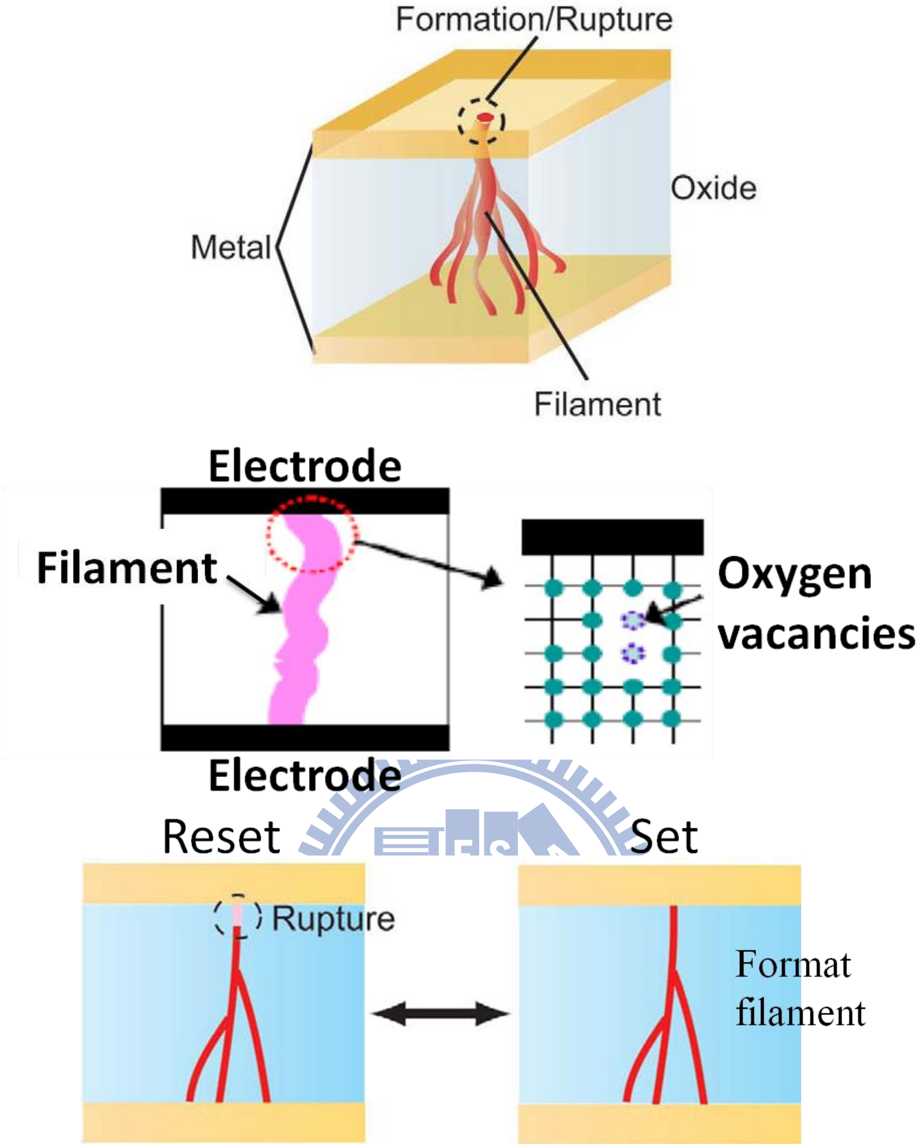


Fig. 2-13 Schematic of the filament in an oxide [2.16, 2.25].

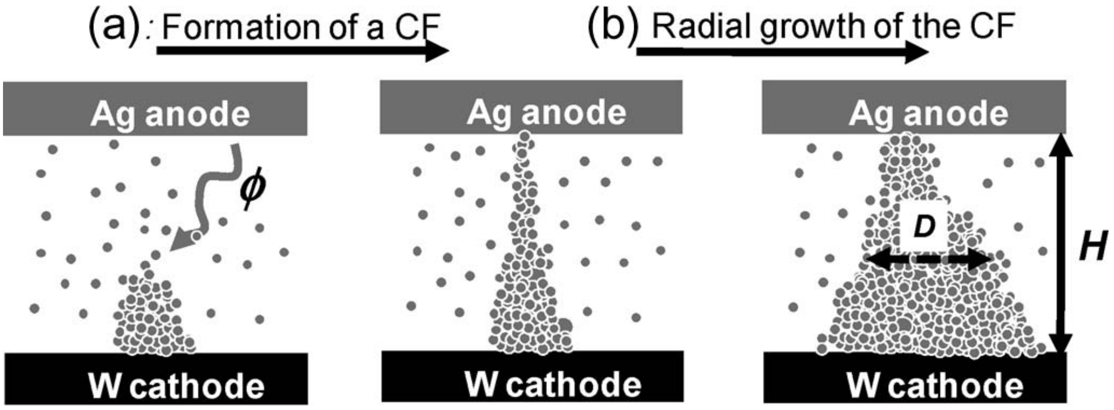


Fig. 2-14 Schematic of (a) the initial formation of a conductive filament, and (b) radial growth of the CF. Both stages of the programming operation are driven by electrochemical reactions at the electrodes and ion migration. [2.28]

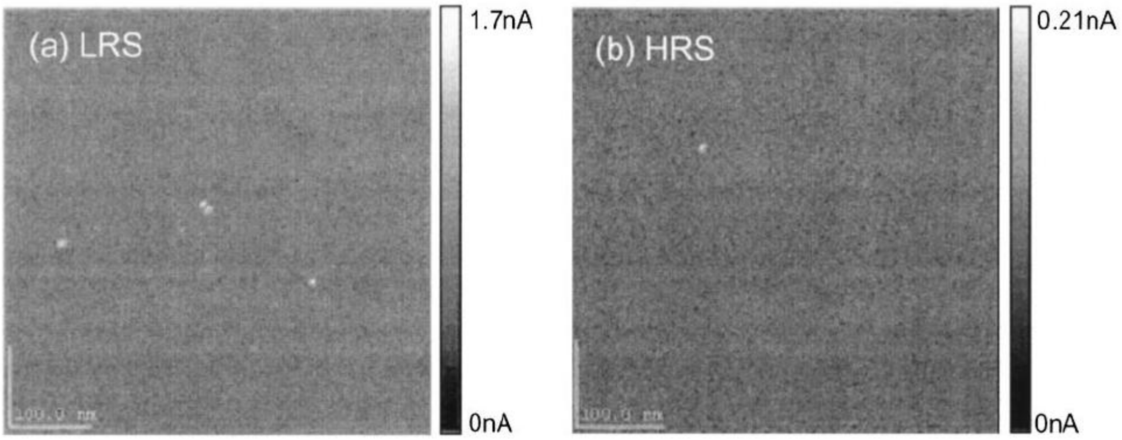


Fig. 2-15 Conductivity mapping results of the (a) low resistance and (b) high resistance state TiO_2 films, using conductive AFM (CAFM). The bright spots represent the conducting points [2.29].

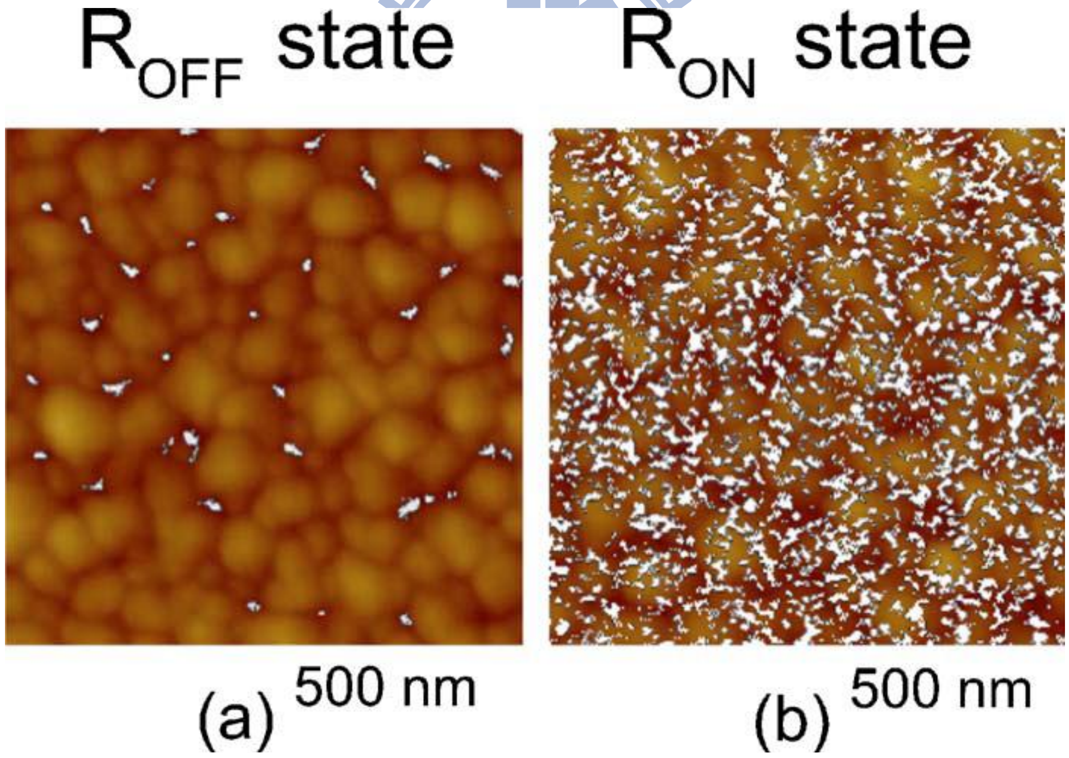


Fig. 2-16 (a) The CAFM image of the NiO thin film for the Roff state corresponding to 100 switching cycles. The bias voltage of 0.1 V was used for the CAFM measurement. (b) The CAFM image of the NiO thin film for the Ron state corresponding to 100 switching cycles. [2.30]

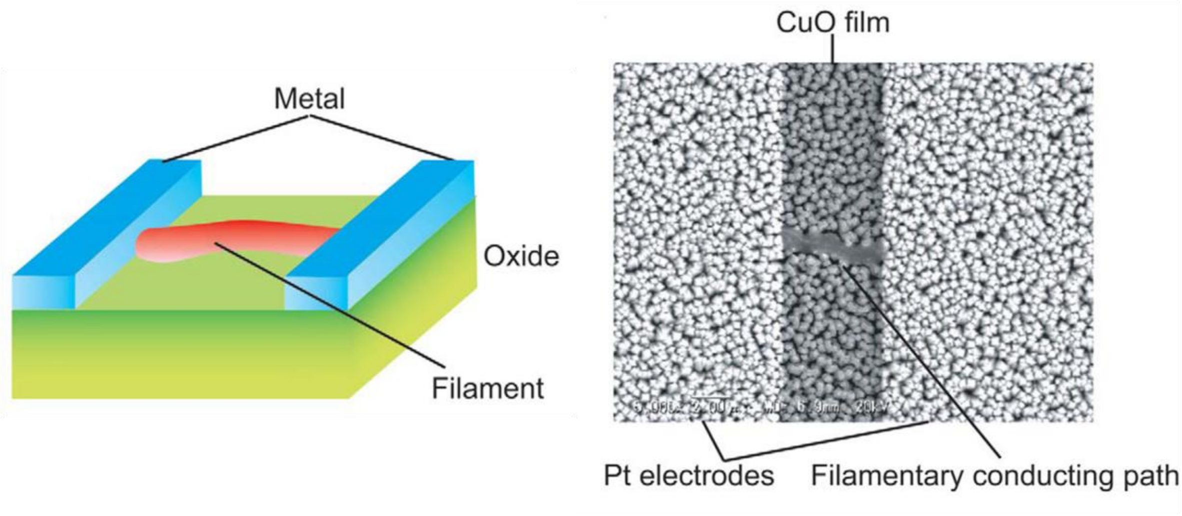


Fig. 2-17 Illustration of a filamentary conducting path in a lateral planar configuration. (b) Scanning electron microscope image of a filamentary conducting path in a CuO film between Pt electrodes. (2.31)

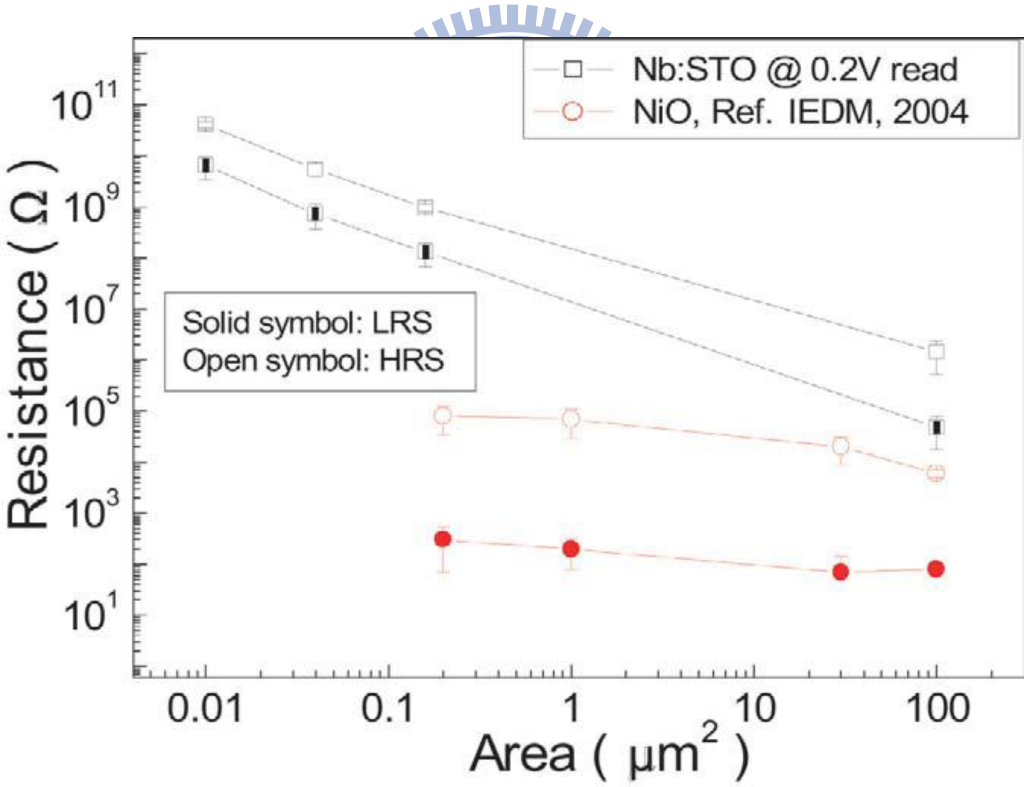


Fig. 2-18 5 Area dependence of resistance values in high and low resistance states for Nb-doped $SrTiO_3$ (Nb:STO) and NiO memory cells. The resistance of Nb:STO memory cells depends linearly on the area, suggesting that the resistive switching takes place over the entire area of the interface. The resistance of NiO memory cells is almost independent of the area, suggesting that resistive switching is a local phenomenon. [2.32]

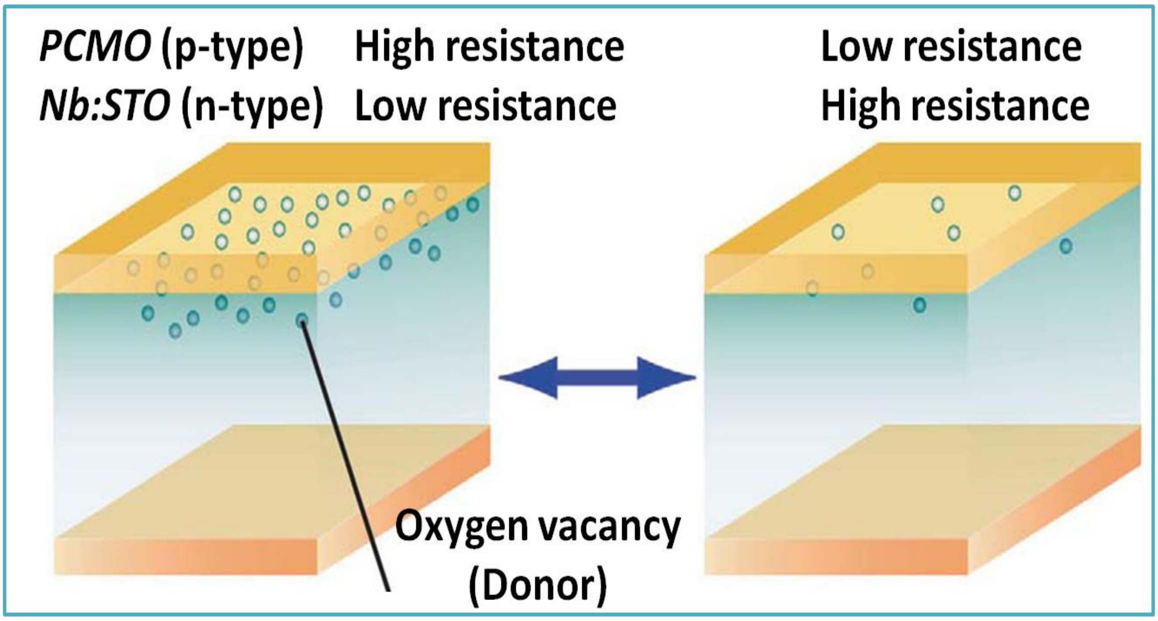


Fig. 2-19 Schematics of the changes in the oxygen vacancy density in the vicinity of the interface. The resistance states of the memory cells are possibly determined by the oxygen vacancy density [2.16].

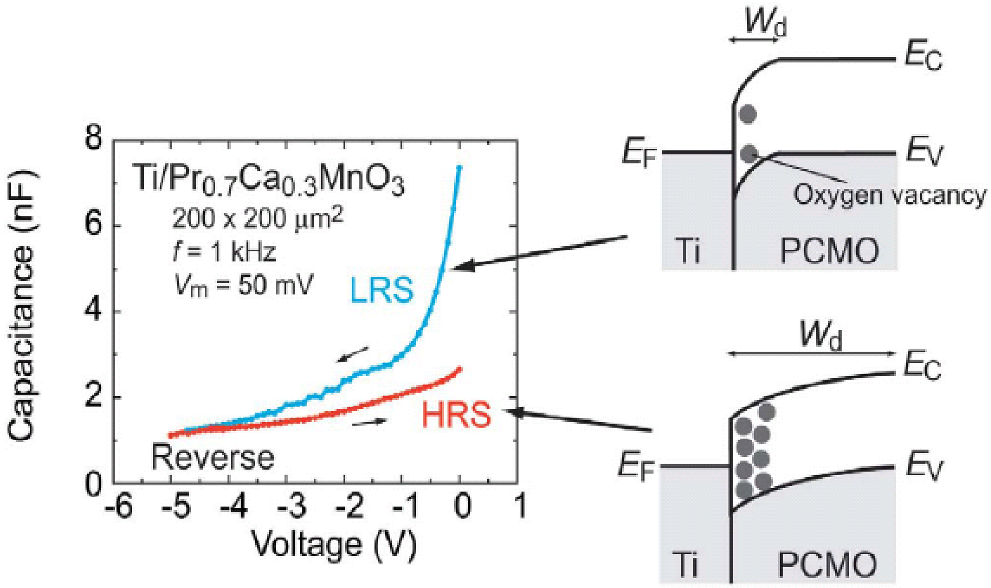


Fig. 2-20 Band diagram with the conditions of p-type semiconductor for on state (LRS) and off state (HRS), respectively [2.16].

Chapter 3

Characteristics of thin-FeO$_x$-contained resistive switching memories

A. Basic Characteristics

3.1 Resistive switching effects on a thin FeO$_x$ transition layer produced at the oxide/iron interface of Ti/TiN/SiO$_2$/Fe-contented electrode structures

3.1.1 Introduction

Resistance random access memory (RRAM) is one of the most potential candidates for the next generation of non-volatile memory [3.1] due to its excellent advantages of high cell density array, high operation speed, low power consumption, and high endurance [3.2-3.4]. Therefore, there have been many studies of binary metal oxides with resistance switching characteristics, such as FeO$_x$ [3.5], ZrO$_x$ [3.6], TiO$_2$ [3.7], NiO [3.8], Al$_2$O$_3$ [3.9], Cu$_x$O [3.10], and HfO$_2$ [3.11] in a metal-insulator-metal (M-I-M) structure due to, in a word, the inevitable existence of nonstoichiometry in every oxide thin film [3.12]. Among these insulators, the switching effect of FeO$_x$ was proposed as a redox reaction between non-stoichiometric compounds of iron oxides, which takes place locally near the electrode region [3.13]. From the point of view of fabrication, almost the binary metal oxides were fabricated by sputtering method. Though binary metal oxides have the advantage of a simple fabrication process compared with ternary or quaternary oxide films, the dominant parameter that has to be considered for the application of binary metal oxides is that the nonstoichiometric oxides show low device yield due to the difficulty to control the composition of non-stoichiometric compounds [3.14, 3.15]. It is because that variation of the composition of a non-stoichiometry is so sensitive that it is easily changed due to the machine inaccuracy. For example, if the amount of oxygen in the chamber is larger, caused from the residue oxygen/moisture in the chamber or the variation of O_2 gas flow rate, it could be easy to form stoichiometric metal oxides instead of the non-stoichiometric compounds. Therefore, it seems difficult to control the composition of non-stoichiometric compounds well by sputtering.

Therefore, we provided a method to produce a non-stoichiometric FeO_x layer, the critical resistance switching layer, near the electrode region simply for RRAM applications by depositing a plasma-enhanced TEOS (Tetraethyl Orthosilicate) oxide onto the Fe-contented electrode to form a SiO_2/FeO_x/Fe-contented electrode structure. It is because of the ease of oxidation of iron atoms that surface of the Fe-contented electrodes could be oxidized spontaneously and incompletely under the PE-TEOS deposition surroundings. Therefore, a “complete” non-stoichiometric compounds, containing the compositions varied from Fe-rich FeO_x (close to Fe electrode) to oxygen-rich FeO_x (close to SiO_2 layer), can easily be produced in the FeO_x transition region. Moreover, in our proposed method, fabrication of the non-stoichiometric compounds was actually related to the step of the PE-TEOS oxide deposition process, i.e. a chemical vapor deposition ambient. Therefore, the factors to affect the fabrication are the temperature of the substrate and the gas flows. Generally, the deposition condition of CVD is in the surface-reaction controlled case, which is dependent on the substrate temperature instead of the gas flow. Most important of all, the diffusion of Fe atoms is also related to the temperature of the substrate, which can be easily controlled accurately instead of the gas flow technically. So, our proposed method seems to provide a better advantage to composite the non-stoichiometric compounds well. Additionally, this oxide layer can act as a supplier of oxygen ions for the switching requirement [3.13]. Furthermore, we also discussed effects of Fe content in the transition region on RRAM behaviors by utilizing Fe and FePt alloy electrodes while the control sample fabricated with only Pt metal as the electrode was also prepared concurrently. Besides the observations of the resistance switching effects of the SiO_2/FeO_x/Fe-contented electrode structure, characterization of the resistance switching mechanism was also examined by discussing the insulator thickness effects, the area size effects, and even the bubble effects.

3.1.2 Experiment

After thermal oxidation of P-type (100) silicon wafers, a 50-nm-thick Pt layer and a 50-nm-thick Fe layer were deposited sequentially as a bottom electrode by DC magnetron sputtering of a Pt target and a Fe target, respectively. For comparison, a 50-nm-thick FePt layer, whose composition of $Fe_{0.73}Pt_{0.27}$ was examined by Inductively Coupled Plasma Mass Spectroscopy, was co-sputtered with Fe and Pt targets. On the other hand, a 50-nm-thick Pt layer was also prepared as the control sample. Then, a ~50-nm-thick SiO_2 layer was deposited on the bottom electrodes by plasma enhanced chemical vapor deposition system with a substrate temperature of 300 ℃ and a working pressure of ($TEOS+O_2$) gases at 300 mTorr. Finally, a 20-nm-thick TiN layer and a 80-nm-thick Ti layer were sputtered sequentially as a top electrode and patterned in a square area with side length of 100 μ m on the SiO_2 films. Illustrations of the proposed process flows and device structures are shown in figure 3-1 (a), figure 3-1 (b), and figure 3-1 (c). For material analyses, auger electron spectroscopy (AES) and transmission electron microscopy (TEM) were carried out using a VG microlab 350 and a Philips Tecnai-20 Systems, respectively. Furthermore, x-ray photoelectron spectroscopy (XPS) was also carried out using the Microlab 350 with a monochromatized Al Kα X-rays source (1486.6 eV; 300 W). For surface topography analyses, Atomic Force Microscopy (AFM) and Scanning Electron Microscopy (SEM) were carried out using a Veeco Dimension 3100 Scanning Probe Microscope and a HITACHI S-4000, respectively. Additionally, for electrical analyses, Keithley 4200 semiconductor characterization system is used to measure the current-voltage (*I*-*V*) characteristics of the fabricated devices.

3.1.3 Results and discussion

(a) Material Examinations and Analyses

Figure 3-2 (a), figure 3-2 (b), and figure 3-2 (c) show cross-sectional TEM of the Ti/TiN/SiO_2/FeO_x/Fe/Pt, the Ti/TiN/SiO_2/FeO_x/Pt, and the Ti/TiN/SiO_2/FeO_x/FePt structures, respectively. Besides the thickness of each layer can be confirmed, it was further observed that there was a thin grey layer of about 5 nm in thickness between SiO_2 and FePt layer, associated with the FeO_x transition region due to the ease of oxidation of iron atoms under the PE-TEOS deposition surroundings.

(b) Resistance Switching Effects

Figure 3-3 (a), figure 3-3 (b), and figure 3-3 (c) show current versus voltage (*I*-*V*) characteristics of the Ti/TiN/SiO_2/FeO_x/Fe/Pt, Ti/TiN/SiO_2/FeO_x/Pt and

$Ti/TiN/SiO_2/FeO_x/FePt$ structures for 50 cycles of switching, respectively. Driving voltage was biased on the bottom electrode while the top electrode was ground and the compliance current was limited to 5 mA during sweeping voltage. Obviously, resistive switching effects are observed only in the structures with a Fe-contained electrode, except the control sample: Bipolar switching is observed for both of the $Ti/TiN/SiO_2/FeO_x/Fe/Pt$ and $Ti/TiN/SiO_2/FeO_x/FePt$ structures: by sweeping the voltage to positive values, the current begins to decrease gradually at a reset voltage (V_{reset}) and finally reaches a high-resistance state (HRS). On the other hand, the current increases suddenly at a set voltage (V_{set}) to return a low-resistance state (LRS) while sweeping the voltage to negative values. The resistance ratios of HRS to LRS for both the structures are ~50 times larger than the requirement of memory for sensing. Of note, prior to the measurements, an electroforming process, i.e. an abrupt increase of leakage current with increase of biasing voltage, were required. Moreover, in order to clarify the composition difference of the iron oxide transition layer, as shown in figure 3-4, Fe $2p_{3/2}$ XPS spectra of the FeO_x transition region of the $Ti/TiN/SiO_2/FeO_x/FePt$ structure after (a) a set process (in an “ON” state) and (b) a reset process (in an “OFF” state) were also analyzed under the same Ar sputter etching time of 350 sec form top surface of PE-TEOS oxide. It is observed that compared to the “OFF” state, the “ON” state show a higher iron oxide composition, FeO, Fe_2O_3, and Fe_3O_4, near the transition region. Therefore, it is further confirmed that the "set" and the "reset" process do change the valence state of iron oxide, which shows a redox of the transition layer during the "set" and the "reset" operations. Figure 3-5 (a) and figure 3-5 (b) show the electroforming process of the Ti/TiN/SiO_2/FeO_x/Fe/Pt and Ti/TiN/SiO_2/FeO_x/FePt structures. It was observed that electroforming voltages of both the structures were carried out in a certain voltage region between 25 and 27 V (for most of cells), corresponding to the electric field of 5.31 ~ 5.74 MV/cm calculated from the actual SiO_2 thickness of 47 nm detected by transmission electron microscopy. Of note, the forming electric field is small but close to the dielectric strength of SiO_2 (normally 10 MV/cm). This result may associate the forming process with dielectric breakdown in the slightly Fe-doped oxide. It is because that a relatively much thicker SiO_2 layer was existed in the proposed structure than the FeO_x layer. Therefore, such a good insulator needs a larger voltage to breakdown, inducing the breakdown of such the thin FeO_x layer to become unobvious and ignorable. In additionally, Fig. 3-5 (c) shows the forming process of the Pt/SiO_2/Pt structure. it is noted that the current characteristics between -20 V~ -25 V region in TiN/SiO_2/Pt structure is different from the others structures with a Fe-contained electrode, which is suggested to the existence of a FeO_x layer and associated to the Stress-Induced Leakage Current from the FeO_x layer. Although the

TEM pictures show a nice and SiO_2 layer, this contamination of SiO_2 interface region near the FePt electrode by inter-diffusion could also be simply inspected by the AES results, which show a slightly diffusion of Fe and Pt atoms into the SiO_2 region. In other words, the forming process of our proposed structure is dominated by the thicker sandwiched insulator, SiO_2, instead of the thin FeO_x layer because of their notable thickness difference. Moreover, in order to confirm that the switching effects in our *I-V* data result only from the FeO_x transition region, we have ascertained that employing Al metal or even tungsten conductive probe (a measurement tip directly on the SiO_2 insulator without a specific contact electrode area) as the top electrode onto the SiO_2/FeO_x/Fe/Pt stacked layers also shows resistance switching effects. Hence, it not only indicates that the top electrode materials exhibit non-dominant factor in our structure but also confirms that the switching effects is related to this transition region.

To further discuss the conduction mechanisms of the Ti/TiN/SiO_2/FeO_x/FePt sample, an *I-V* curve in negative and positive voltage ranges is replotted in a log-log scale as shown in figure 3-6 (a) and figure 3-6 (b), respectively. The slopes of LRS in both the positive and negative voltage ranges are close to 1, corresponding to the Ohmic behaviors. We suggests that in LRS, the transition region is composed of the low resistance phase of Fe_3O_4, though incompletely, so it presents a conductive property and follows the Ohm' law. On the other hand, the slopes of HRS are also close to 1 in the low voltage ranges in both the positive and negative voltage ranges, but the current begins to increase nonlinearly with voltages higher than ~2.8 V. This nonlinear region plotted in log-log scale can further be fitted to be a linear curve at ln(*I/V*) versus square root voltage plot as shown in the inset of figure 3-6 (b). In addition, a relationship between temperature and current has also been observed as shown in the inset of figure 3-6 (a). According to the report of *Ieda et al.* [3.17], the modified Pool-Frenkel equations showed that current follows Ohm' law at low electric fields and increases exponentially with the square root of the applied voltage at high fields as well as the temperature-dependent characteristics. Therefore, our observed *I-V* curves in HRS are in good agreement with the Pool-Frenkel behaviors. Because the conduction mechanism of Pool-Frenkel is related to trap sites in the insulating material, we suggests that in HRS, most of the non-stoichiometric transition region is composed of the high resistance phase, Fe_2O_3, while a residual of the other iron oxides phase act as the defect traps.

(c) Insulator Thickness Effects

At the beginning of our experiment, the choice of employing a 50-nm-thick SiO_2 layer was based on two reasons naively. One reason is that the thickness of the insulator materials reported in RRAM literatures is typically a few ten nanometers (40 nm~100 nm in our references) in order to observe the effects obviously, prevent a severe leakage current, improve the reliability of the device, and operate the device in a reasonable voltage range for observation. So we also sued the SiO_2 layer of ~50 nm in the beginning of study. The other reason is that a thicker SiO_2 layer could prevent the entire SiO_2 layer from the contamination of Fe atoms so that a FeO_x transition layer would form between a Fe layer and a SiO_2 layer obviously.

To confirm the correspondence of the resistance switching characteristics to the FeO_x transition region, a difference in insulator thickness, the SiO_2 layer, was also prepared for comparison. Experimentally, a thinner SiO_2 layer of ~22 nm was fabricated on the same Fe-contained-electrode structure. It is also observed that the resistance switching effects were exhibited in the thin-SiO_2-contained structure. However, it is noted that the necessary electric field for forming process in such a thin-SiO_2-contained sample was slightly reduced to ~5.01 MV/cm. The cause of this forming electric field reduce is suggested that the ratio of the Fe-slightly-doped SiO_2 region to the bulk SiO_2 layer increases as the thickness of SiO_2 layer decrease. So, a “more seriously” Fe-doped insulator was obtained in a sample with a thinner insulator layer, inducing the decrease of the forming electrical field. It should be noted that the smaller HRS of the thinner-SiO_2-contained structure was also observed. Simply, based on the Ohm's law, it is considered that the thinner insulator layer contributes a smaller resistance for the device. Besides, it could also be suggested that a thinner silicon dioxide layer provides less oxygen iron for the FeO_x transition layer to form an oxygen-rich Fe_2O_3 phase, which exhibits a higher resistance state, so that the inefficient HRS would be produced and cause a higher off state leakage current.

(d) Area Size Effects

To further understand the switching phenomenon of the Fe-contained-electrode structure, area size dependence of resistance values in high and low resistance states was also investigated by the Ti/TiN/SiO_2/FeO_x/FePt sample as shown in figure 3-7. Interestingly, it is observed that the resistance in HRS depends more obviously and more strongly on the electrode area size, suggesting that the resistive switching takes place over the entire area of the interface and associating with the interface-type resistance switching phenomenon. Otherwise, the resistance in LRS shows a slight dependence on the area size, suggesting that the main resistive switching characteristic of the LRS is combined with both an entire area phenomenon and a localized phenomenon and associating with the minority of interface-type resistance switching phenomenon and the majority of filament-type resistive switching phenomenon.

(e) Bubble Effects

Of note, by observing optical microscopy of the biased top metal pad (Ti/TiN), pits were obviously obtained after a high voltage sweep measuring as shown in figure 3-8. Moreover, different constructions of the pits were created at a Ti/TiN of an initial sample surface after high positive and negative voltage bias conditions as shown in figure 3-8 (the positive bias condition was applied by sweeping the voltage on the bottom electrode from 0 V to 30 V and the negative one was from 0 V to -30 V). Compared to a negative biasing condition [figure 3-9 (a)], a positive biasing condition was observed to induce complex pits with a darker regions on the Ti/TiN surface [figure 3-9 (b)], associated with the exposure of the Fe-contained electrode. In short, pits deeper into the FePt surface. To ensure that dark pits are deep pits, we checked the pit depth by a α -stepper to make sure the dark pits as deeper pits. Besides, we also analyzed the dark pit by atomic force microscope (AFM) system as shown in figure 3-10. In order to get more accurate information of the construction of a dark pit, the AFM was performed on the sample with a dark pit after stripping the top electrode by wet chemical etching. It was observed that a depth of a dark pit is about 50 nm, which is almost closed to the thickness of the SiO_2 layer. It is supposed that formation of the pits is due to severe gas expansion to burst the thin films, caused from the electrical Joule heating. In addition, XPS spectra of Fe-2$p_{3/2}$ were also utilized to examine the characteristics of the FeO_x transition region after a positive and a negative bias stress contidions. Figure 3-11 (a) and figure 3-11 (b) show XPS Fe-2$p_{3/2}$ spectra near the interface region of the SiO_2/(FeO_x)/FePt structure after a positive and a negative bias stress contidions. Besides experimentally confirming the existence of the non-stoichiometric iron oxides, including FeO, Fe_2O_3, and Fe_3O_4, near the Fe and the FePt electrode surfaces, where Fe $2p_{3/2}$ features for metallic Fe at 707.3 eV, FeO at 709.8 eV, Fe_3O_4 at 710.4 eV and Fe_2O_3 at 711.4 eV were assigned. [3.16]. Most important of all, it is observed that a higher oxidized phase of the iron oxide exhibits in the positive-stressed condition than the negative-stressed condition, inferring the migrating element of the device is oxygen ion instead of oxygen vacancy. Therefore, an explanation for different constructions of the pits on the Ti/TiN surface is proposed: under a voltage bias condition, the O^{2-} ions of the oxide materials drift toward the anode to evolve O_2 gas, as schematically shown in figure 3-12. Moreover, electrical Joule heating also occurs severely at higher applied voltages (and higher current densities). Therefore, as applying a high positive bias on the Fe-contained electrode (anode), oxygen ions in the SiO_2 layer drifted toward the SiO_2/Fe-contained interface region to evolve the oxygen gas in small size randomly as soon as the large oxygen gas was accumulated and grown by engulfing neighbors. Of note, the drifting trace of the oxygen ions might be properly by the way of diffusion path produced by forming process. Then, the evolved O_2 gas expands to burst the SiO_2 and Ti/TiN layers to cause such the deeper pits due to an efficiently Joule heating [figure 3-12 (a)], especially when the main current flow is conducted by a thin conductive filament, causing a severe Joule heating effect locally to burst our structures. On the other hand, as applying a negative bias on the Fe-contained electrode (cathode), the evolved O_2 gas drifts torward the Ti/TiN/SiO_2 interface to burst [figure 3-12 (b)] Ti/TiN layers only so that shallower pits were created. Therefore, it is suggested that the O^{2-} ions is the major voltage-controlled migration elements in our proposed structure.

On the other hand, the formation of the oxygen irons is also related to the formation of oxygen vacancies with the chemical relationship as follows:

$$V_o^{2+} + O^{2-} \longleftrightarrow O$$

Therefore, the role of oxygen vacancies could also play an important role in the resistance switching. Oxygen vacancies could be regarded as donors to provide electrons in iron oxide. In addition, for an intrinsic n-type Fe_2O_3 semiconductor iron oxide layer, the addition of oxygen vacancies caused from the biased voltage, where oxygen vacancy is a sort of positive charge carrier, could also contribute to the conductivity of the Fe_2O_3 layer to transfer the HRS into a LRS during a “set process”. Moreover, the existence of oxygen vacancies could also help the band bending of the n-type Fe2O3 semiconductor upward severely to cause a tunneling path for conducting carriers to transport, which also causing the lowing of the HRS.

Therefore, according to the area dependence results, insulator thickness results, and the bubble effect results, the possible switching model of the Fe-electrode-contained RRAM structure was proposed as shown in figure 3-13. As shown in figure 3-13 (a), normally, the forming process mainly causes the breakdown of the insulator, inducing the conducting filaments inside both the SiO_2 and the FeO_x region. When the proposed structure was performed to a “reset” process, the bias-controlled oxygen ions drifts toward the FeO_x region to oxidize this transition region (or recover the FeO_x to a high-oxidized iron oxide state, i.e. Fe_2O_3, which also exhibits a high resistivity). Therefore, the resistive switching phenomenon during “set” was dominated by the filament-type resistive switching as shown in figure 3-13 (b). On the other hand, when a “set” process was performed, it is also suggested that the domination of the resistive switching phenomenon of the Fe_2O_3 region prefers to a fast breakdown rather than a slow chemical reduction as shown in figure 3-13 (c).

(f) Fe-contented Electrode Effects

First of all, it is noted that definitions of the “Set Current” and “Set Voltage” are the values of the current and voltage detected at the beginning of the resistance switching from a HRS to a LRS, respectively. The “Set Power” is defined as the product of “Set Current” and “Set Voltage” .Similarly, definitions of the “Reset Current” and “Reset Voltage” are the values of the current and voltage detected at the beginning of the resistance switching from a LRS to a HRS, respectively. The “Reset Power” is defined as the product of “Reset Current” and “Reset Voltage”.

For comparing the effects on the different Fe-contented electrode, *I-V* characteristics of the Ti/TiN/SiO_2/FeO_x/Fe/Pt, and Ti/TiN/SiO_2/FeO_x/FePt structures were shown concurrently in figure 3-14 as well as statistical comparison of set/reset voltages (V_{set}/V_{reset}), set/reset current (I_{set}/I_{reset}) and set/reset power (P_{set}/P_{reset}) in figure 3-15. It is observed that not only the mean values of V_{set}, V_{reset}, P_{set} and P_{reset} but also the variances of V_{set} (ΔV_{set}) and V_{reset} (ΔV_{reset}) in the Ti/TiN/SiO_2/FeO_x/FePt structure are smaller than those in the Ti/TiN/SiO_2/FeO_x/Fe/Pt structure. In order to clarify the difference, AES depth profile of Fe and O near SiO_2/FeO_x/Fe/Pt and SiO_2/FeO_x/FePt stacked layer region were also examined, as shown in figure 3-16. It is observed that the SiO_2/Fe sample is with a relatively Fe-rich composition in the transition region as well as a longer Fe diffusion profile into the SiO_2 layer. In addition, the O element also diffuses severely into the Fe electrode. It indicated that addition of Pt into Fe electrode can not only restrain the out-diffusion of Fe atom but also resist the oxidation of the electrode itself because platinum is chemically unreactive. Moreover, because the switching mechanism of iron oxides was explained by a redox reaction between the Fe_3O_4 phase (with lower resistance) [3.18] and Fe_2O_3 phase (with higher resistance) [3.19], i.e. these non-stoichiometric phases are easily oxidized or reduced into each other according to the electric-field-controlled movement of O^{2-} ions, the improvement of the dispersions in the Ti/TiN/SiO_2/FeO_x/FePt structure may result from the decrease of effective thickness of the FeO_x region due to the electromigration of O^{2-} into FeO_x layer [3.20]. Additionally, the transition region with more Fe composition and/or thickness in the Ti/TiN/SiO_2/FeO_x/Fe/Pt structure may exhibit more random and non-uniform conducting paths, so the variances of the switching voltages to cause the formation or rupture of the conducting paths were also enlarged [3.21, 3.22].

Retention characteristics of the Ti/TiN/SiO_2/FeO_x/Fe/Pt and Ti/TiN/SiO_2/FeO_x/PtFe structures were measured at room temperature as shown in figure 3-17. After the sweeping process to cause a set or reset state, then, the current of LRSs or HRSs in the both samples is recorded at 0.2 V reading voltage with an interval. The reading of the resistance state is nondestructive, and no electrical power is needed to maintain the resistance within a given state (LRS or HRS).

3.1.4 Conclusion

In conclusion, we have demonstrated the reproducible resistance switching characteristics on a FeO_x transition layer produced by oxidizing the surface of the FePt electrode under a PE-TEOS depositing surroundings in a $Ti/TiN/SiO_2/FeO_x/FePt$ structure. Confirmation of the resistive switching effects provided by the FeO_x layer was carried out by replacing the top and bottom electrodes materials, such as Pt, Al, and even W measurement probe. Moreover, reduction of the Fe amount in the transition region improves the dispersion of memory switching parameters such as V_{set}, V_{reset}, P_{set}, P_{reset}, ΔV_{set} and ΔV_{reset} by utilizing a $Ti/TiN/SiO_2/FeO_x/FePt$ structure. Characteristics of the non-stoichiometric FeO_x transition layer were confirmed and examined by auger electron spectroscopy, transmission electron microscopy, and x-ray photoelectron spectroscopy analyses. The resistance ratio of HRS to LRS of the structure was ~50 times. Moreover, the role of the silicon oxide layer was experimentally demonstrated to act as a supplier of oxygen ions for the switching requirement by biasing high voltage bias conditions.

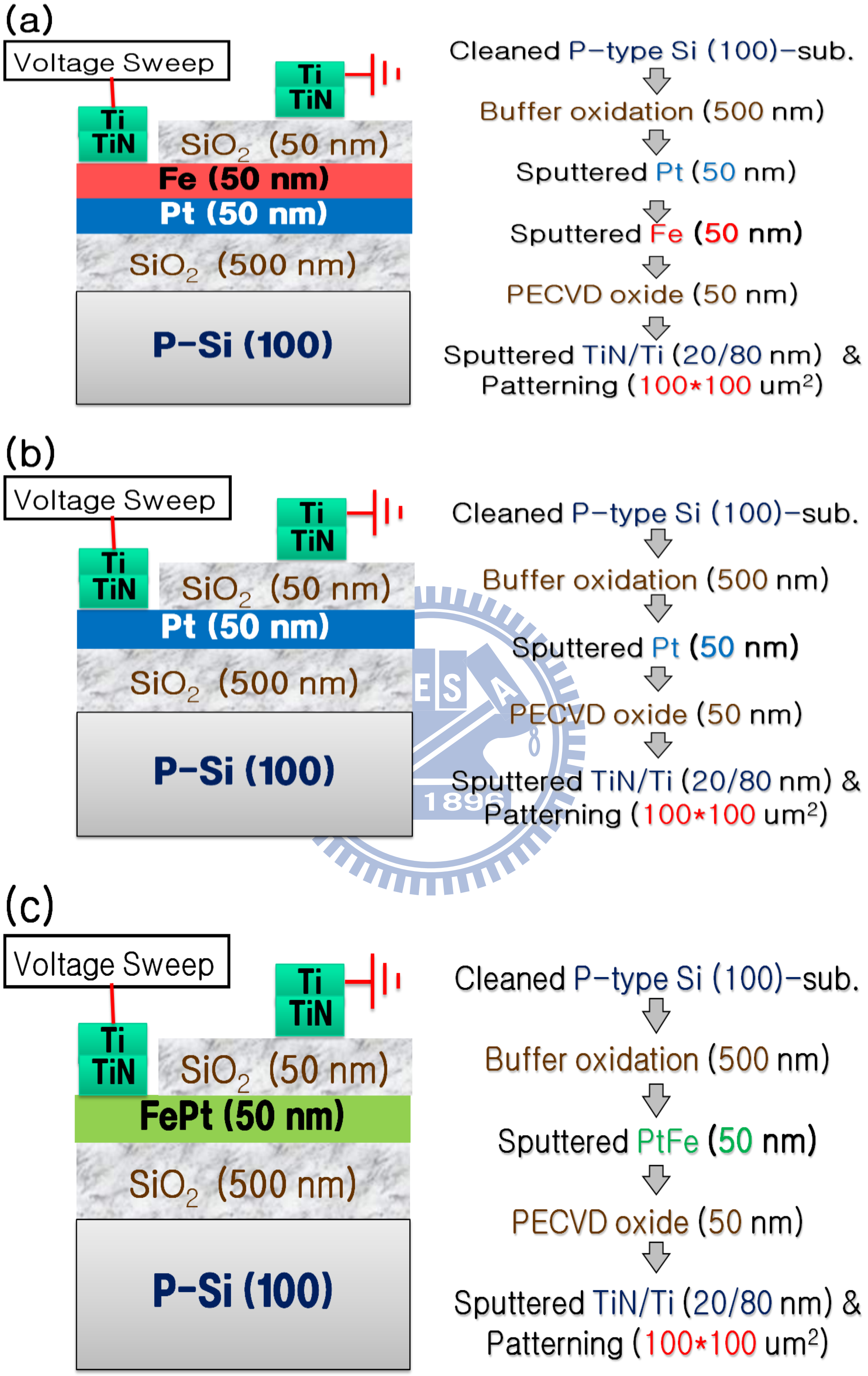


Fig. 3-1 Illustrations of the (a) Ti/TiN/SiO_2/FeO_x/Fe/Pt, (b) Ti/TiN/SiO_2/FeO_x/Pt, and (c) Ti/TiN/SiO_2/FeO_x/FePt device structures and their process flows.

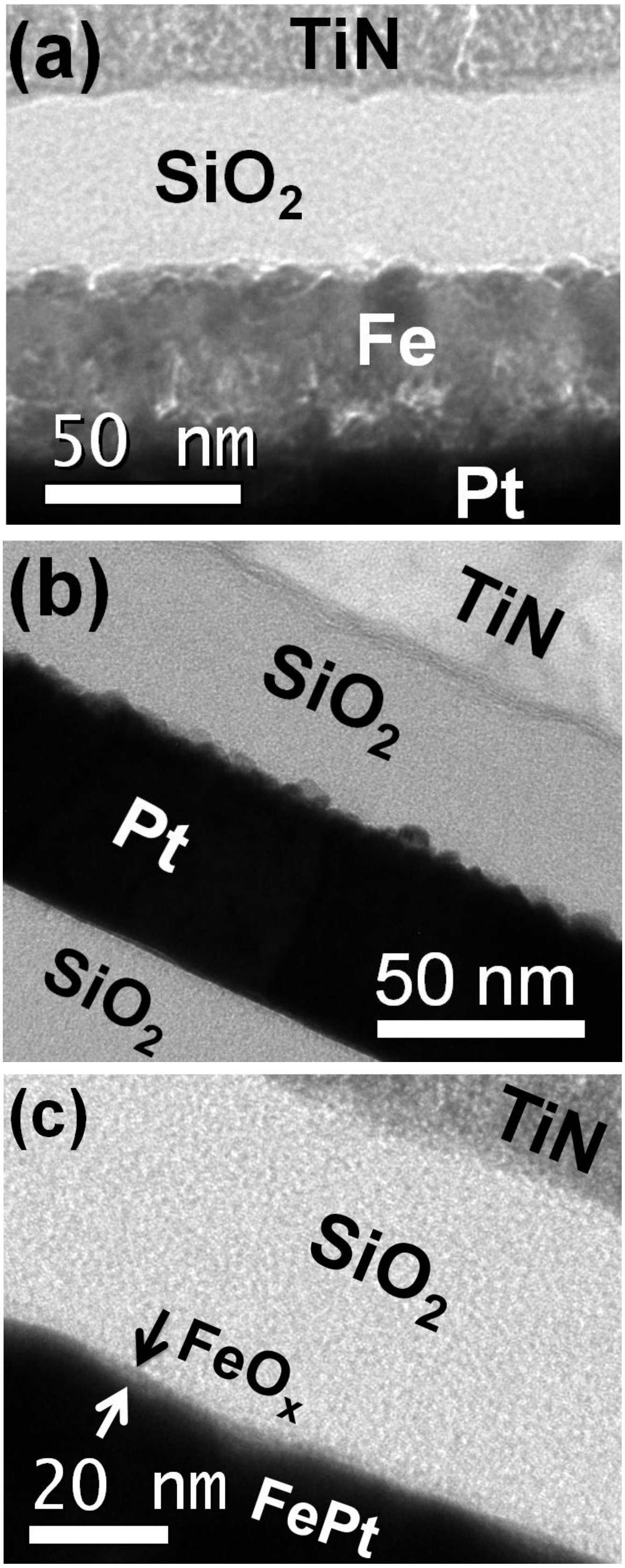


Fig. 3-2 Cross-sectional TEM of the proposed (a) Ti/TiN/SiO_2/FeO_x/Fe/Pt, (b) Ti/TiN/SiO_2/FeO_x/Pt, and (c) Ti/TiN/SiO_2/FeO_x/FePt device structures.

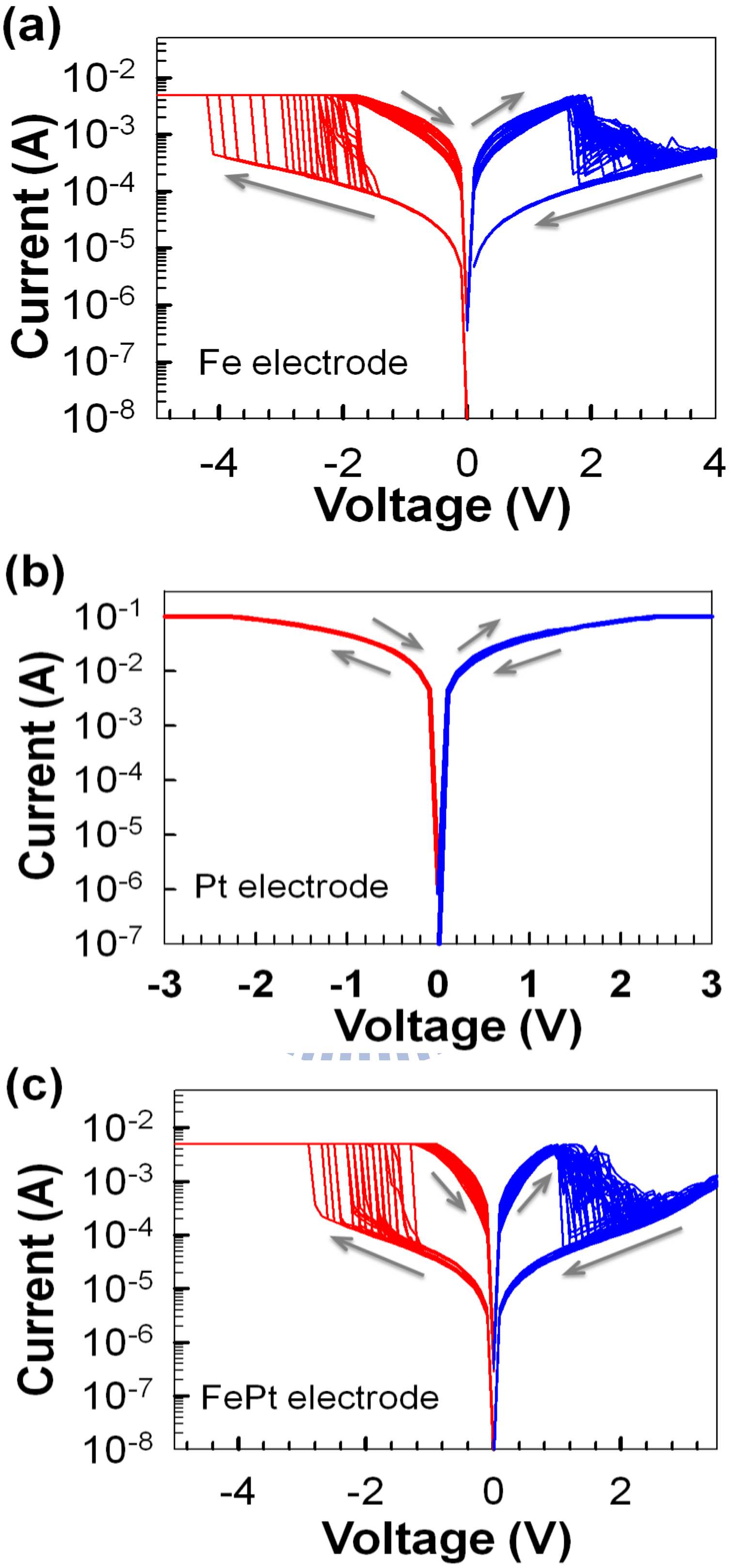


Fig. 3-3 50 cycles of bipolar switching behaviors of the (a) Ti/TiN/SiO_2/FeO_x/Fe/Pt, (b) Ti/TiN/SiO_2/FeO_x/Pt, and (c) Ti/TiN/SiO_2/FeO_x/FePt structures with compliance current 5 mA. The arrows indicate voltage sweeping directions.

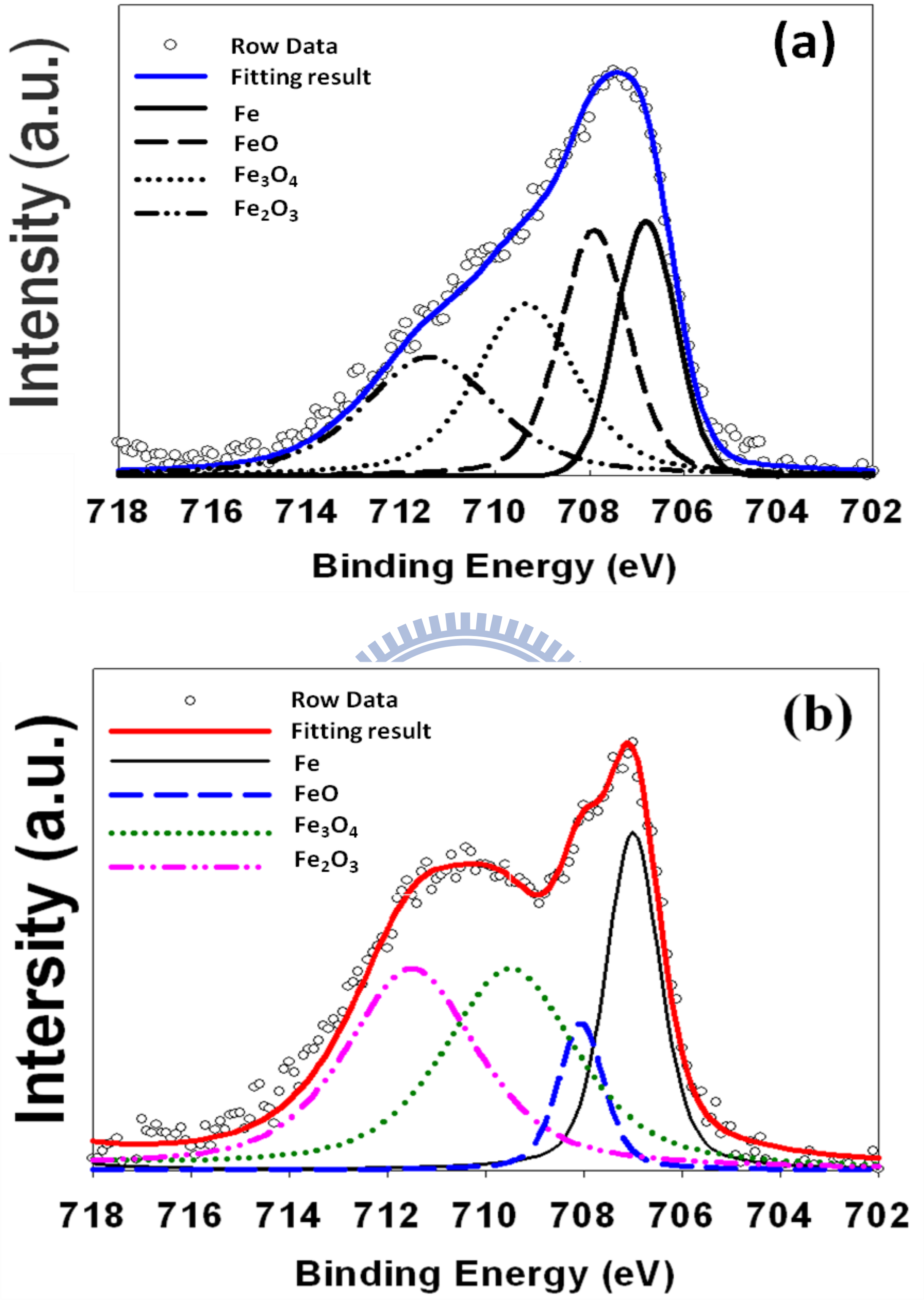


Fig. 3-4 Fe 2p3/2 XPS spectra of the FeOx transition region of the Ti/TiN/SiO2/FeOx/FePt structure after (a) a set process (in an “ON” state) and (b) a reset process (in an “OFF” state) under the same Ar sputter etching time of 350 sec form top surface of PE-TEOS oxide.

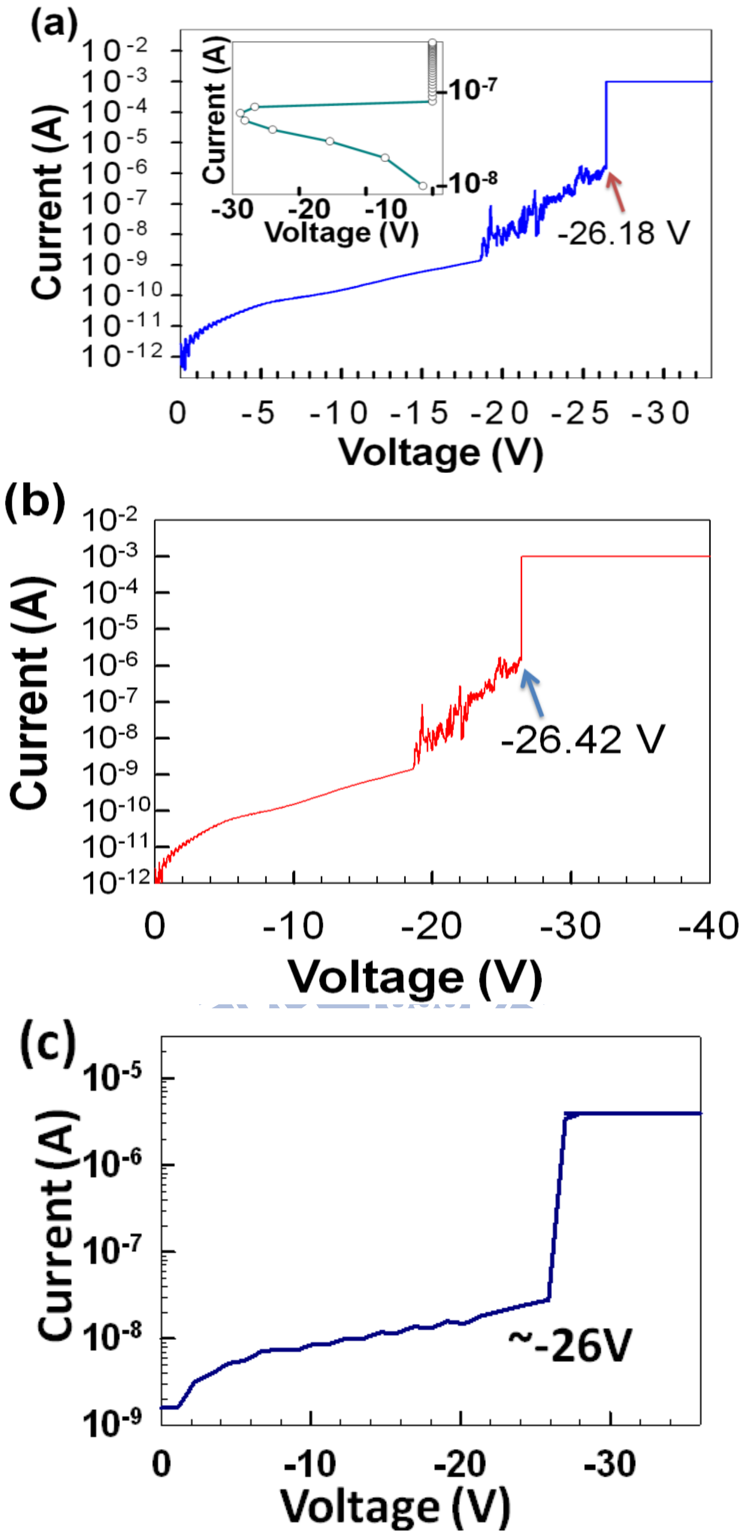


Fig. 3-5 *I*-*V* characteristics of forming process on the (a) Ti/TiN/SiO_2/FeO_x/Fe/Pt and (b) Ti/TiN/SiO_2/FeO_x/FePt structures for *V*-sweep measurement. In addition, the inset of (a) also shows the *I*-*V* characteristics of the forming process for *I*-sweep measurement. Fig. (c) also shows the forming process of the Pt/SiO_2/Pt structure.

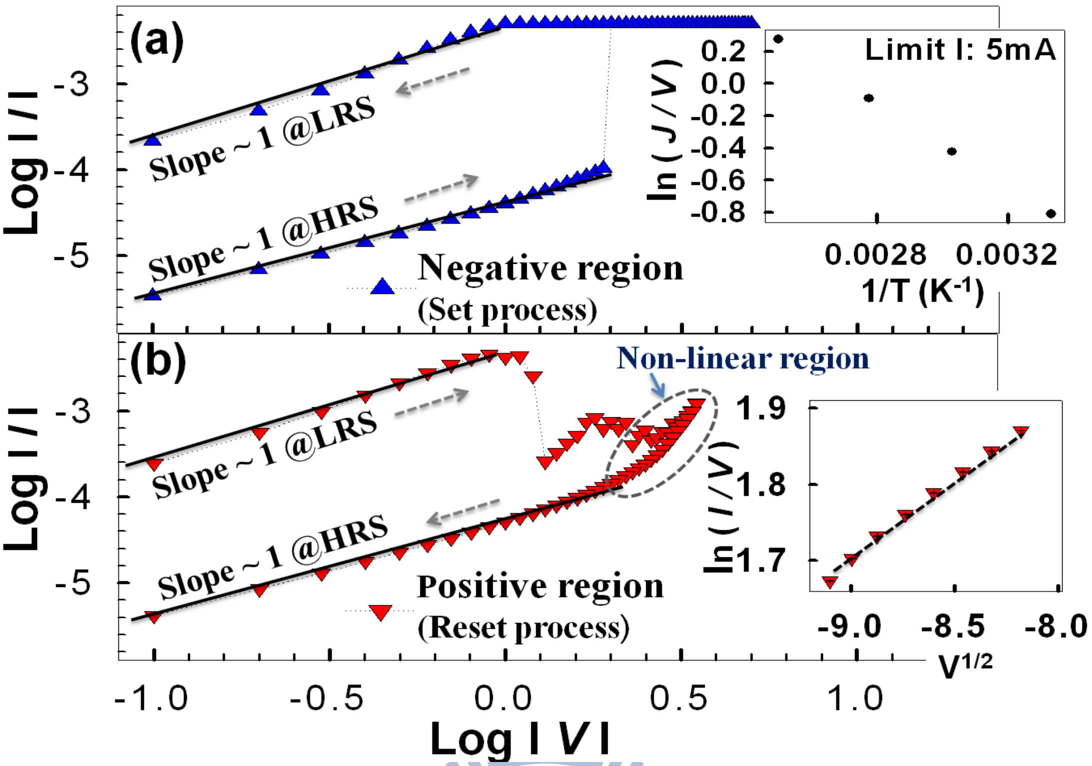


Fig. 3-6 Linear fitting results of log-log scale in (a) negative voltage region and (b) positive voltage region for the Ti/TiN/SiO_2/FeO_x/FePt structure. The insets of (a) and (b) show a plot of current vs temperature and a plot of ln(I/V) vs $V^{1/2}$ at voltage higher than +2.8 V in HRS, respectively. The arrows indicate voltage sweeping directions.

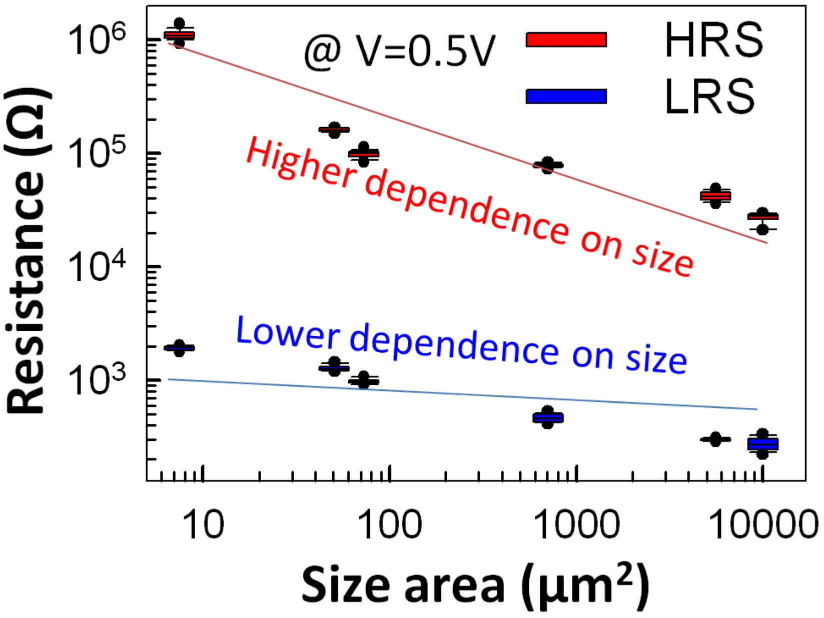


Fig. 3-7 Electrode area dependence of resistance values in high and low resistance states for a Ti/TiN/SiO_2/FeO_x/FePt structure.

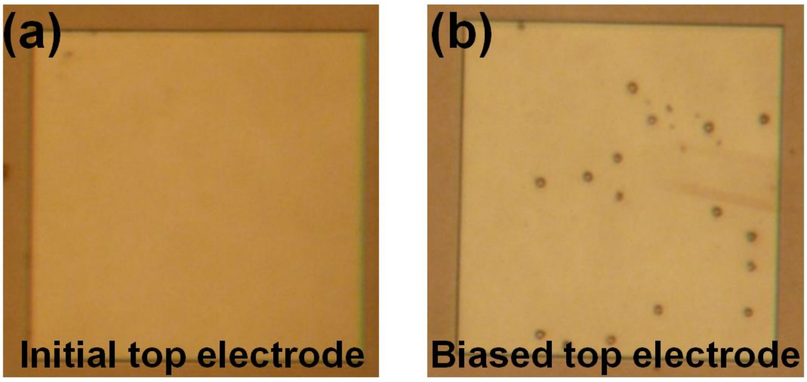


Fig. 3-8 OM images of a Ti electrode surface (a) before and (b) after a higher voltage stress biasing.

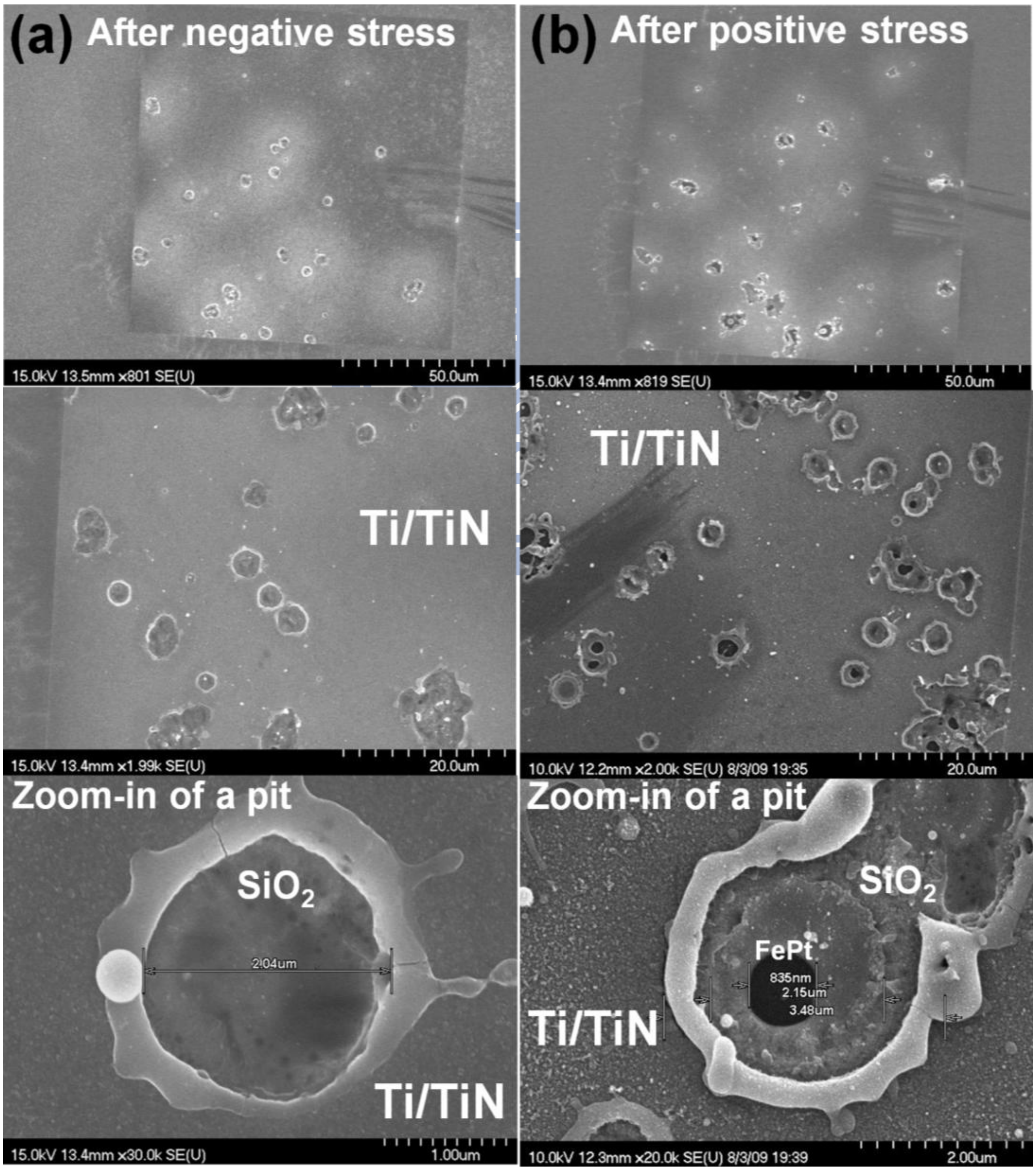
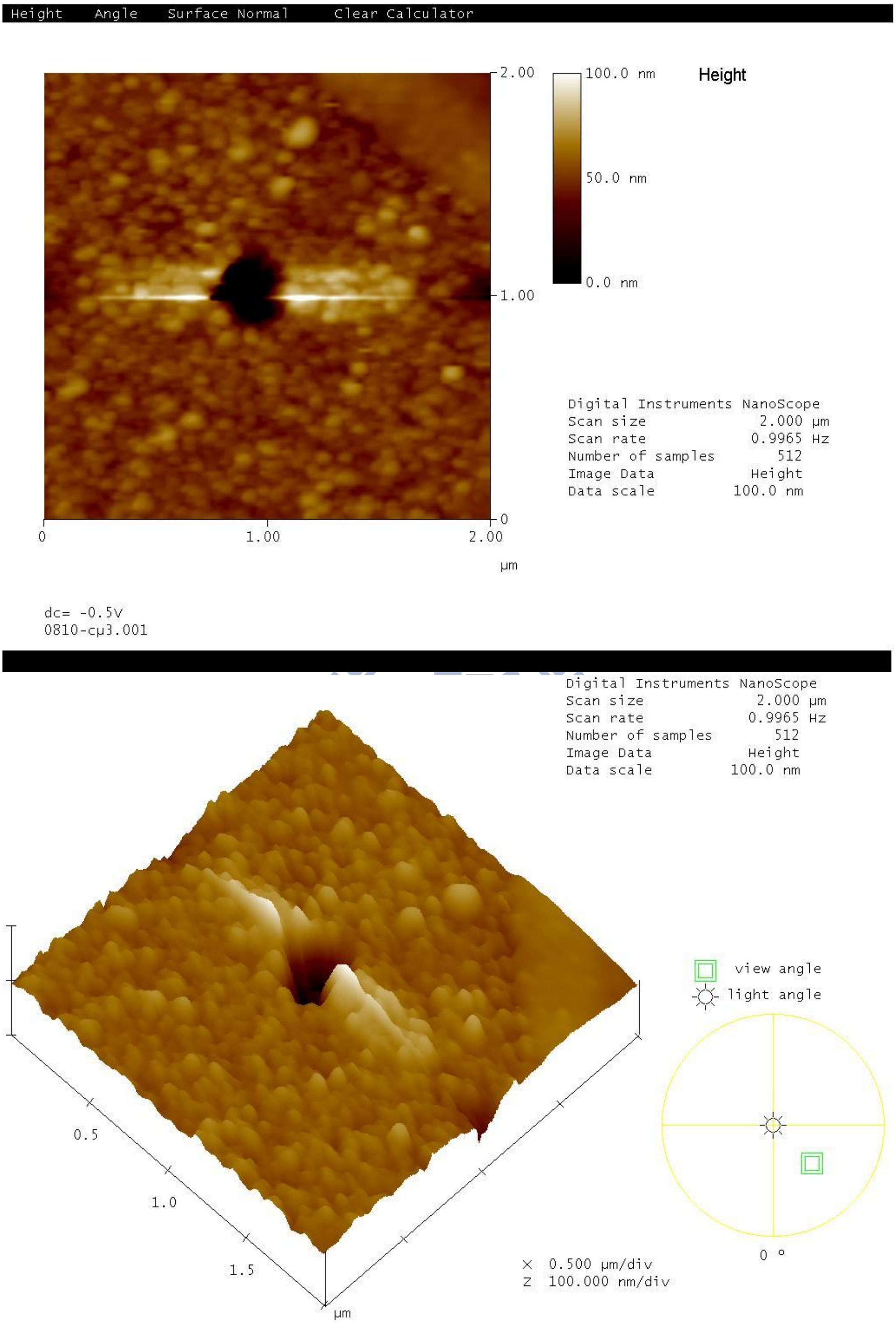


Fig. 3-9 SEM images of the Ti/TiN electrode surface after (a) negative stress and (b) positive stress conditions.



Digital Instruments NanoScope
Scan size 2.000 µm
Scan rate 0.9965 Hz
Number of samples 512
Image Data Height
Data scale 100.0 nm

dc= -0.5V
0810-cµ3.001

Digital Instruments NanoScope
Scan size 2.000 µm
Scan rate 0.9965 Hz
Number of samples 512
Image Data Height
Data scale 100.0 nm

X 0.500 µm/div
Z 100.000 nm/div

Fig. 3-10 AFM image of the sample with a dark pit after stripping the top electrode by wet chemical etching.

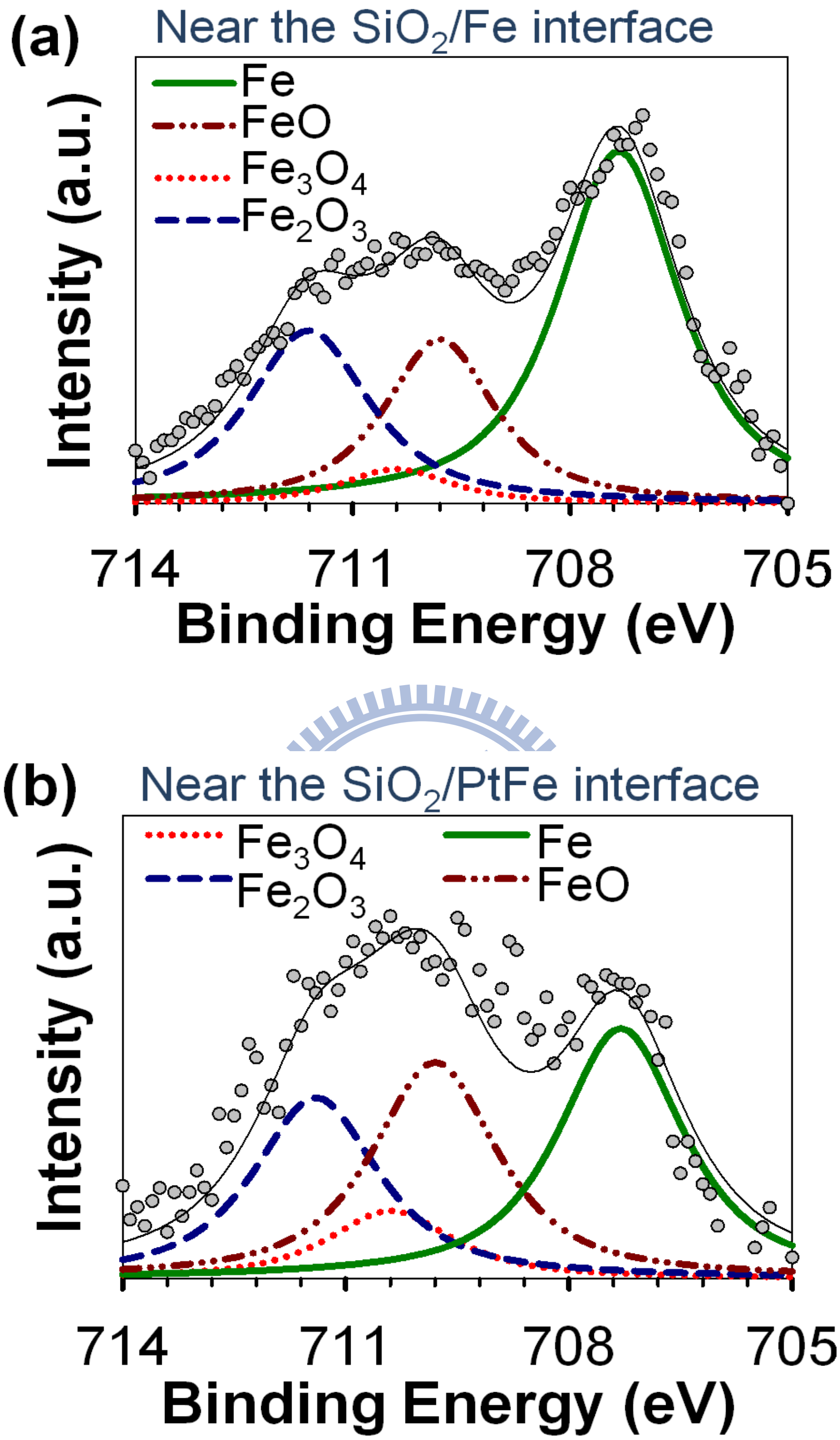
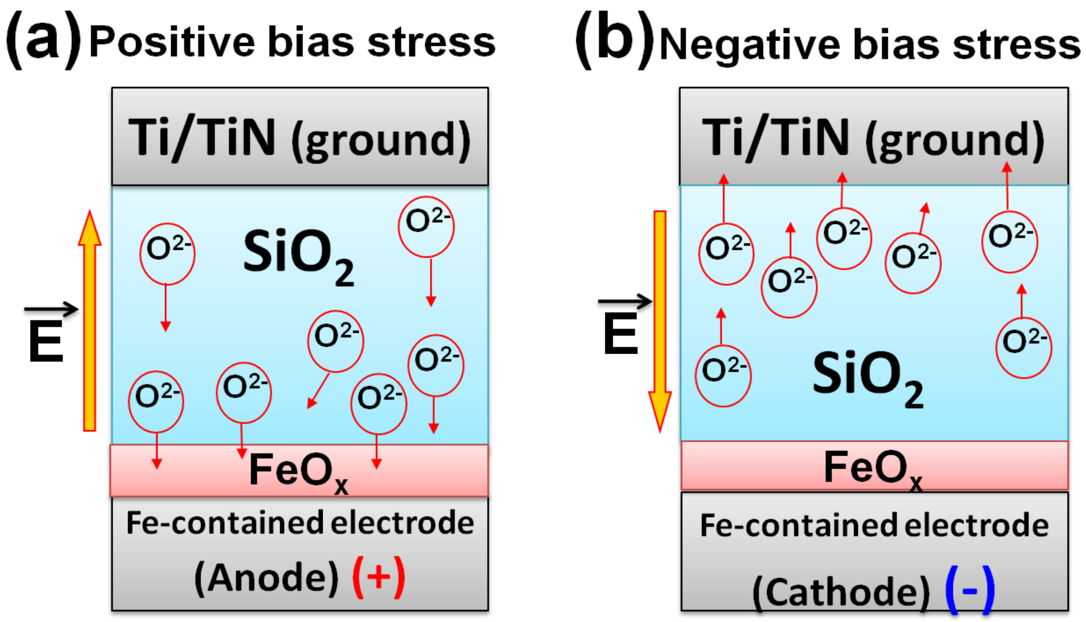


Fig. 3-11 Fe $2p_{3/2}$ XPS spectra of the FeO_x transition region in the (a) Ti/TiN/SiO_2/FeO_x/Fe/Pt and (b) Ti/TiN/SiO_2/FeO_x/FePt structures. Fe $2p_{3/2}$ features for metallic Fe at 707.3 eV, FeO at 709.8 eV, Fe_3O_4 at 710.4 eV and Fe_2O_3 at 711.4 eV were assigned.



$$3Fe_2O_3\,(HRS) + 2e^- \Longleftrightarrow 2Fe_3O_4\,(LRS) + O^{2-}$$

Fig. 3-12 Schematic pictures of the electromigration of O^{2-} in a sandwiched structure of Ti/TiN/SiO_2/FeO_x/Fe-contained electrode during (a) negative stress and (b) positive stress conditions.

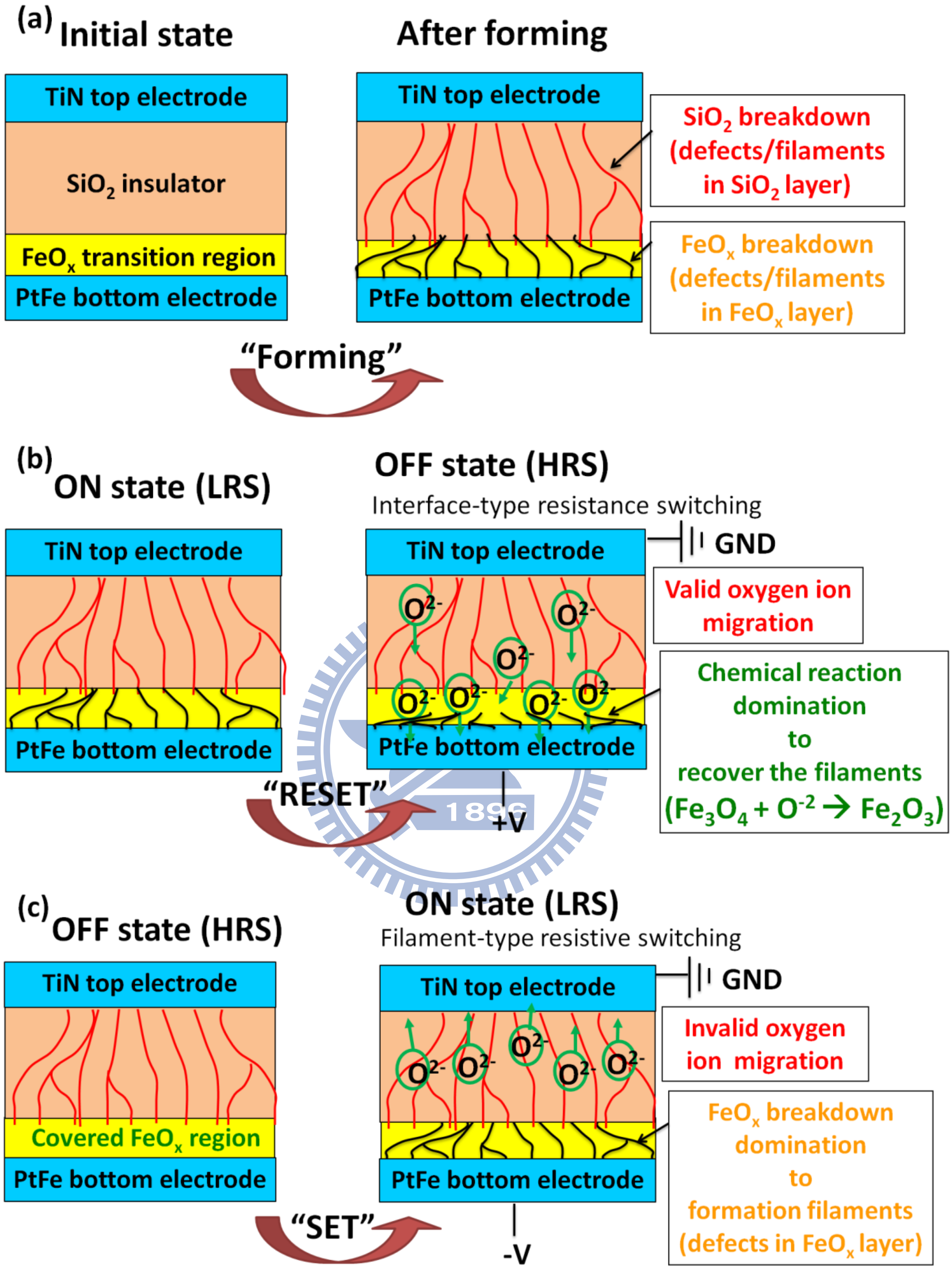


Fig. 3-13 Proposed switching model of the Fe-electrode-contained RRAM structure for (a) an initial state to a formed state, (b) a “set” state to a “reset” state, and (c) a“reset” state to a “set” state.

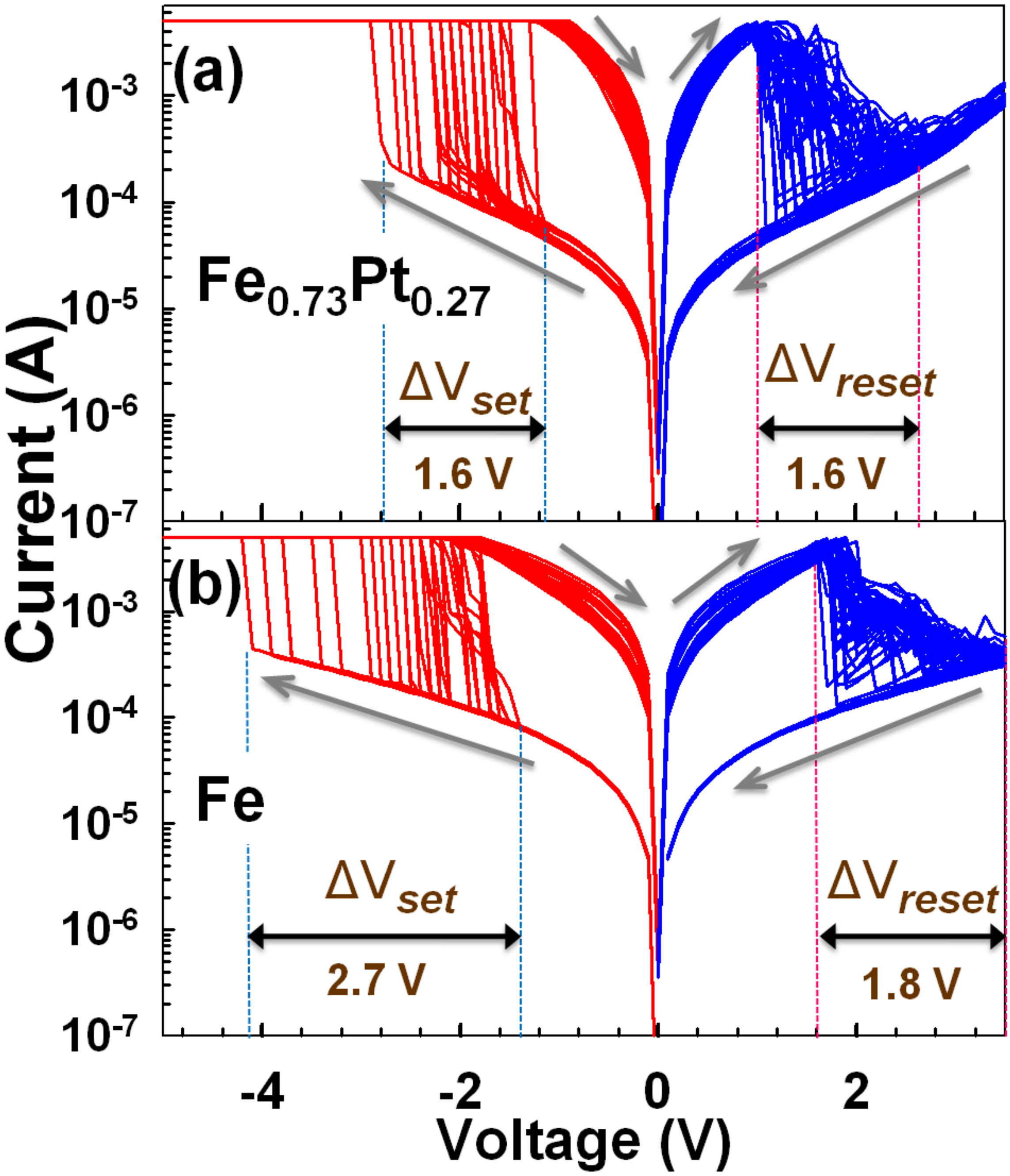


Fig. 3-14 Comparison of 50-cycle bipolar switching behaviors between the (a) Ti/TiN/SiO_2/FeO_x/FePt and (b) the Ti/TiN/SiO_2/FeO_x/Fe/Pt structures.

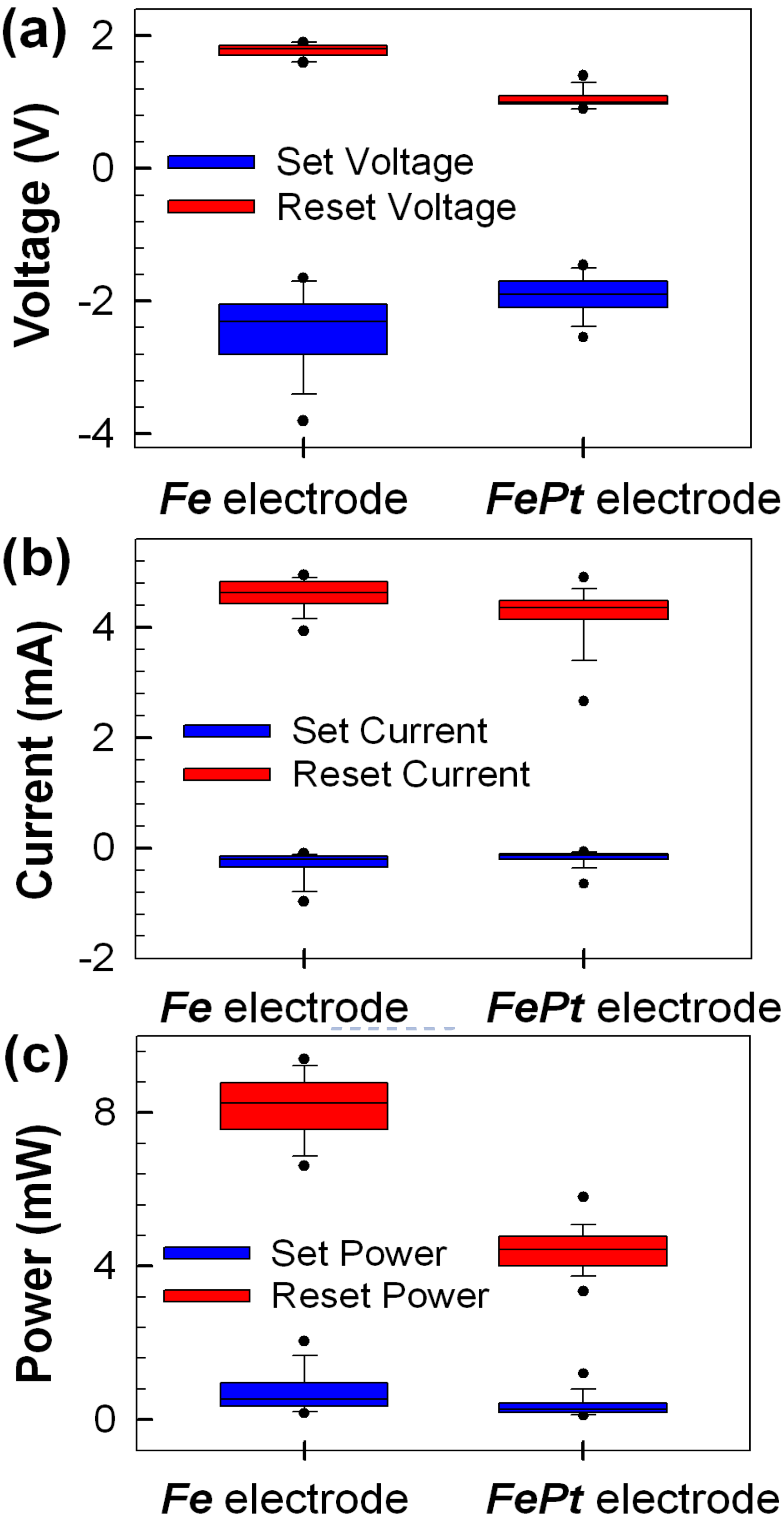


Fig. 3-15 Statistical comparison of (a) set/reset voltages, (a) set/reset current, and (c) set/reset power between the Ti/TiN/SiO_2/FeO_x/FePt and the Ti/TiN/SiO_2/FeO_x/Fe/Pt structures.

electrode	Set Voltage (V)	Reset Voltage (V)	Set Current (mA)	Reset Current (mA)	Set Power (mW)	Reset Power (mW)
Fe	-2.3	1.8	-0.2	4.6	0.54	8.25
FePt	-1.9	1.0	-0.1	4.3	0.25	4.45

Table 3-1 Comparison of the mean value of Set & Reset voltage, Set & Reset current and Set & Reset power between the FePt-contained and Fe-contained structures.

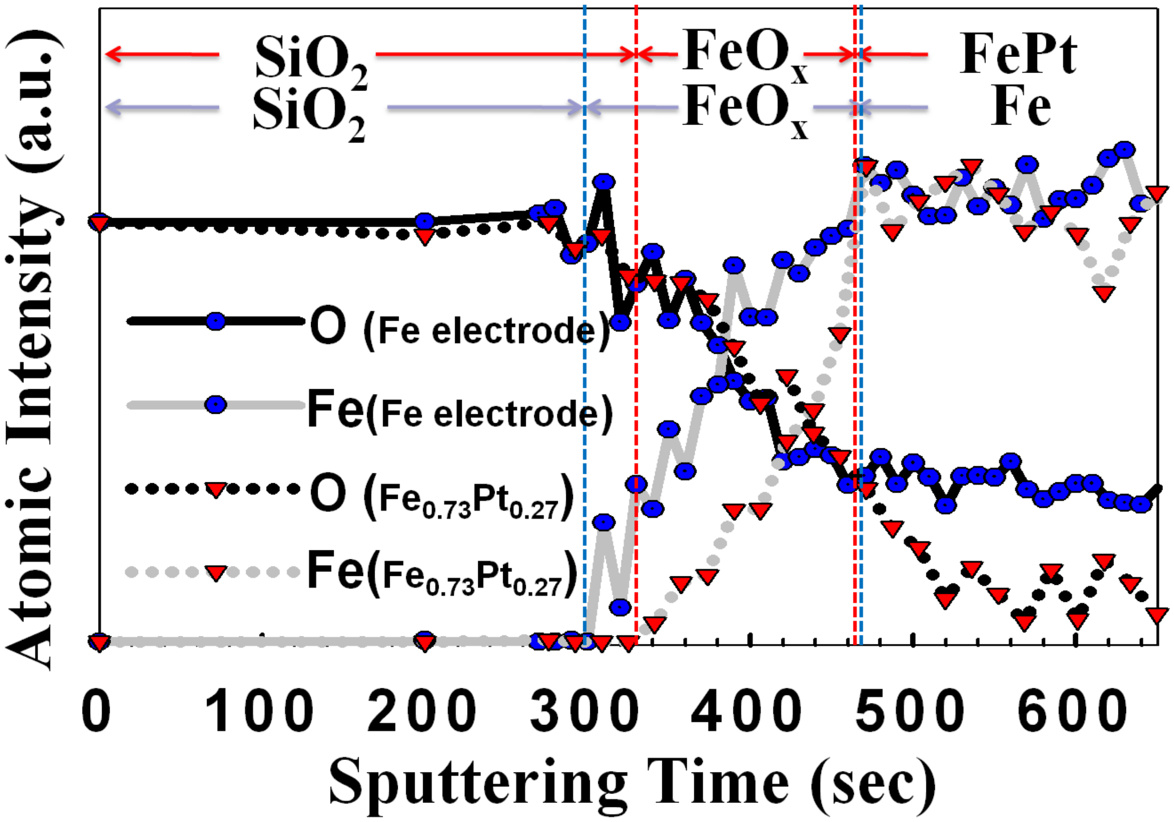


Fig. 3-16 Comparison of AES depth profiles of Fe and O between a SiO_2/FePt and a SiO_2/Fe/Pt stacked layers.

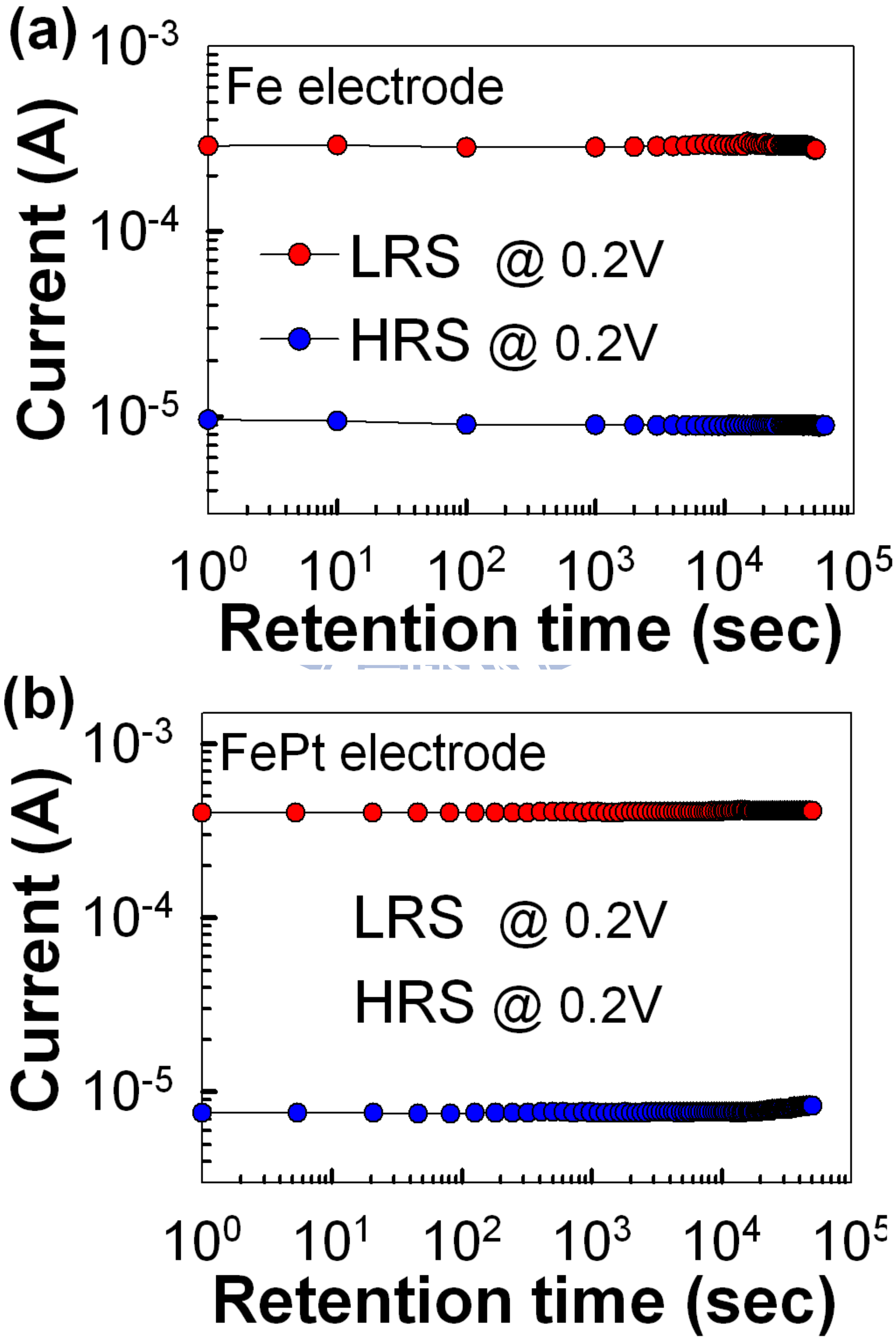


Fig. 3-17 Electrical retention characteristics of the (a) Ti/TiN/SiO_2/FeO_x/Fe/Pt and (b) the Ti/TiN/SiO_2/FeO_x/FePt structures.

Thermal Annealing Effects

3.2 Annealing effects on the resistive switching characteristics of the Ti/TiN/SiO_2/FeO_x/FePt and Ti/TiN/SiO_2/FeO_x/Fe structures

3.2.1 Introduction

Many materials with resistance switching characteristics including perovskite oxides, such as Cr-doped $SrTiO_3$ [3.23], Cr-doped $SrZrO_3$ [3.24], and $Pr_{0.7}Ca_{0.3}MnO_3$ [3.25], and transition metal oxides, such as HfO_2 [3.11], FeO_x [3.12], ZrO_x [3.26], and Al_2O_3 [3.27], have been widely investigated. Compared to ternary or quaternary oxide materials, binary transition metal oxides have the advantages of simpler fabrication process and higher compatibility with complementary metal-oxide semiconductor process. Therefore, in our previous report [3.28], a simple method to fabricate a FeO_x-based RRAM device with good characteristics was proposed in sandwich structure of Ti/TiN/SiO_2/FeO_x/Fe-contained electrode, where the FeO_x transition layer was produced spontaneously by depositing a plasma-enhanced TEOS (Tetraethyl Orthosilicate) oxide onto the Fe-based electrode due to the ease of oxidation of Fe-contented electrode under a PE-TEOS deposition surroundings.

On the other hand, it was reported that an annealing treatment could transform the phases and crystallinity of the FeO_x structure [3.5], which plays an important role in the switching characteristics of the FeO_x material. Additionally, an annealing treatment also drives a further diffusion of Fe atoms from Fe-contented electrode into the SiO_2 layer. So, an annealing treatment could directly affect the switching behaviors of a FeO_x-transition-layer-contained device and would be help for investigating the characteristics of the switching mechanism clearer. Therefore, annealing treatments on the $Ti/TiN/SiO_2/FeO_x/FePt$ and $Ti/TiN/SiO_2/FeO_x/Fe$ structures were investigated.

3.2.2 Experiment

The resistance switching memory devices were prepared through the following processes. After thermal oxidation of P-type (100) silicon wafers, a 50-nm-thick $Fe_{0.73}Pt_{0.27}$ layer and a Fe/Pt layer were deposited as a bottom electrode by DC magnetron. Then, a ~50-nm-thick SiO_2 layer was deposited on both the bottom electrodes by plasma enhanced chemical vapor deposition system with a substrate temperature of 300 °C and a working pressure of $(TEOS+O_2)$ gases at 300 mTorr. A 20-nm-thick TiN and a 80-nm-thick of Ti were sputtered sequentially as the top electrode and patterned in a square area with side length of 100 μm on the SiO_2 film. Finally, rapid thermal annealing (RTA) treatments at 600 °C for different intervals of 30 sec (denoted as “RTA-30 sec sample”), and 60 sec (denoted as “RTA-60 sec sample”), and a furnace annealing (FA) treatment at 600 °C for 30 min (denoted as

FA-30 min sample) were performed in argon ambient. For a comparison, the control sample made without the annealing treatment (denoted as "as-deposited sample") was also prepared under the same process. Keithley 4200 semiconductor characterization system is used to measure the current-voltage (*I*-*V*) characteristics of the fabricated devices. Illustrations of the proposed process flows and device structures are shown in figure 3-18and figure 3-19. In addition, transmission electron microscopy (TEM) was carried out using a Philips Tecnai-20 Systems and x-ray diffraction (XRD) was carried out using a PANalytical X'Pert Pro (MRD) with a monochromatized Cu Kα; λ= 0.154 nm. Furthermore, x-ray photoelectron spectroscopy (XPS) was also carried out using the Microlab 350 with a monochromatized Al Kα X-rays source (1486.6 eV; 300 W).

3.2.3 Results and discussion

(a) Material Examinations and Analyses

Two parts of analytical results of the structures with Fe and FePt electrodes were discussed separately.

First, for the Ti/TiN/SiO_2/FeO_x/FePt structure:

Figure 3-20 (a), figure 3-20 (b), figure 3-20 (c) and figure 3-20 (d) show cross-sectional TEM images of the as-deposited, RTA-30 sec, RTA-60 sec and

FA-30 min samples, respectively. A more obvious transition region at the SiO_2 and FePt interface was observed in the sample with a longer thermal annealing time, contributed from a serious diffusion of iron atoms. Besides, severe roughness at the SiO_2/FePt interface was obtained.

Figure 3-21 depicts comparisons of x-ray diffraction (θ -2θ) data among the as-deposited, RTA-60 sec and FA-30 min samples. It is observed that not only the distinct enhancement of FePt peak intensities but also the additional peaks of Fe_2O_3 (222), Fe_2O_3 (332), and Fe_2O_3 (622) appear [3.29] after annealing treatments.

Figure 3-22 (a), figure 3-22 (b) and figure 3-22 (c) show x-ray photoelectron spectroscopy depth profiles of Fe-*2p* on the as-deposited, RTA-60 sec and FA-30 min samples, respectively. An Ar sputter etching into the SiO_2 layer was performed for collecting the XPS data at various depths and the etching times of the spectra as shown in figure 3-22 are from bottom to top 300, 320, 340, and 360 sec. Though the existence of the non-stoichiometric iron oxides, FeO, Fe_2O_3, and Fe_3O_4, are observed in all the samples, higher Fe-O bonds intensities in the thermal-treated samples are detected at shorter Ar sputter etching times as compared to the as-deposited sample, implying that deeper diffusion of Fe atoms into SiO_2 layer. In addition, larger amounts of Fe_2O_3 and Fe_3O_4 bonds can be obtained after annealing, especially for the RTA-60 sec sample. Therefore, the XPS results show that a thicker and more intense FeO_x binding layer was produced after annealing, which is also with correspondence to XRD results. Of note, in the FA-30 min sample, Fe-Fe binding intensity becomes higher than Fe-O binding with Ar sputter etching, which is suggested that larger amounts of SiO_2-diffused iron atoms were not oxidized effectively due to insufficient present of excess oxygen.

(b) Resistance Switching Effects

Figure 3-23 (a), figure 3-23 (b), figure 3-23 (c) and figure 3-23 (d) show current versus voltage (*I*-*V*) characteristics of the as-deposited, RTA-30 sec, RTA-60 sec and FA-30 min samples for 50 cycles of switching, respectively. Under the same measuring method mentioned above, driving voltage was biased on the bottom electrode while the top electrode was ground and the compliance current was limited to 5 mA during sweeping voltage. Bipolar switching is observed for all of the annealed samples: by sweeping the voltage to positive values, the current begins to decrease gradually at a V_{reset} and finally reaches a HRS. On the other hand, the current increases suddenly at a V_{set} to return a LRS while sweeping the voltage to negative values. In addition, it is noticed that besides a reduction in operation voltages (V_{set} and V_{reset}), the variances of V_{set} and V_{reset} were also improved as the annealing time increasing. According to the proposed switching mechanism of iron oxides explained by a redox reaction of FeO_x [3.30] between the Fe_3O_4 phase (with lower resistance [3.18]) and Fe_2O_3 phase (with higher resistance [3.19]), therefore, we suggests that the improved crystallinity of the FeO_x film, i.e. been already existed crystalline phases of Fe_2O_3 structure in the RTA sample, could cause the ease of such iron oxide phase transformations between Fe_3O_4 and Fe_2O_3 so as to reduce the operation voltages. Then, the ΔV_{set} and ΔV_{reset} would also decrease relatively with the reduction of the V_{set} and V_{reset}. Of note, prior to the measurements, an electroforming process were also required for all the annealed samples. However, it is obtained that the forming voltage decreases intensively while the annealing time increasing: after a 600 ℃ annealing for 60 sec, the forming electric field of the as-deposited sample were reduced from 5.74 MV/cm to 0.13 MV/cm and further to 0.08 MV/cm while the annealing time increasing to 30 min, which nearly means formless requirement. It could be associated with the more severe diffusion of Fe atoms, which are regarded as impurities for the insulator, into the SiO_2 layer. Therefore, the soft breakdown electric field dropped obviously, with corresponding to the TEM and XPS results of a severe Fe diffusion.

(c) Statistic Characteristics

First of all, definitions of the “Set Current” and “Set Voltage” are the values of the current and voltage detected at the beginning of the resistance switching from a

HRS to a LRS, respectively. The “Set Power” is defined as the product of “Set Current” and “Set Voltage” .Similarly, definitions of the “Reset Current” and “Reset Voltage” are the values of the current and voltage detected at the beginning of the resistance switching from a LRS to a HRS, respectively. The “Reset Power” is defined as the product of “Reset Current” and “Reset Voltage”.

Additionally, *I-V* characteristics of all the annealed samples were shown concurrently for comparison in figure 3-24 as well as statistical comparison of set/reset voltages (V_{set}/V_{reset}), set/reset current (I_{set}/I_{reset}) and set/reset power (P_{set}/P_{reset}) in figure 3-25 and figure 3-26. For set process region [figure 3-25], it is observed that not only the mean value of V_{set}, but also the variance of V_{set} becomes smaller with longer annealing time as shown in figure 3-25 (a). In figure 3-25 (b), it is observed that the set current increases with annealing time except the RTA-60 sec sample. Moreover, with the exception of the RTA-60 sec sample, the set power nearly maintains constant in spite of annealing treatment [figure 3-25(c)]. According to the results of the abrupt increase of current from HRS to LRS and the constant maintenance of the set power, defined by the production of the set voltage and set current, the set process of the device is regarded as agglomeration of conducting filament with a necessary of heating condition. Furthermore, for the RTA-60 sec sample, the slight reduction of the set current and the set power was suggested to the existence of larger Fe-O bonds in the FeO_x transition layer without a severe diffusion of effective-oxidized Fe atoms. On the other hand, for reset process region [figure 3-26], it is also observed that both the mean value of V_{reset} and its variance becomes smaller with longer annealing time as shown in figure 3-26 (a). In figure 3-26 (b), however, it is observed that the reset current remains constant in spite of the annealing treatments. Besides, the reset power slight decrease with increase the annealing time [figure 3-26 (c)]. According to the results of the gradual decrease of current from LRS to HRS and the constant maintenance of the reset current, the reset process of the device is regarded as chemical reaction of conducting filament oxidation with a necessary of sufficient current intensity.

(d) Reliability Characteristics

Figure 3-27 shows the retention performance of the as-deposited, the RTA-60 sec and the FA-30 min samples under 0.2 V reading voltage at room temperature. The readout of LRS and HRS is performed after applied -4 V / 3 V for the as-deposited sample, -2 V / 2 V for the RTA-60 sec sample and -2 V / 1.2 V for the FA-30 min sample for a short time, respectively. Then the current of LRSs or HRSs in the as-deposited and the RTA samples is recorded at 0.2 V reading voltage with an interval. The reading of the resistance state is nondestructive, and no electrical power is needed to maintain the resistance within a given state (LRS or HRS). As can be seen in figure 3-27, LRSs and HRSs currents of both the samples are kept stable for more than 6×10^4 sec, confirming the nonvolatile nature of the device. Based on an extrapolation, although the retention decay of the as-deposited sample is more serious, however, both the two resistance states of both the samples are good enough to be maintained over 10-years for nonvolatile memory applications. In addition, figure 3-28 also shows their retention performance under 0.2 V reading voltage at 85 ℃. It is observed that retention property of the as-deposited sample becomes unstable at higher measuring temperature, which also confirms the chemical reaction characteristic of FeO_x resistive switching behavior due to the higher chemical activity at higher temperature surroundings. However, exhibition of more stable retention characteristics was observed in the thermal-treated samples, which may associate with the crystallinity of the FeO_x film. Of note, higher HRS and LRS current were also observed due to the severe diffusion of the ion atoms into SiO_2 layer.

Second, for the $Ti/TiN/SiO_2/FeO_x/Fe/Pt$ structure:

In order to confirm the annealing effect results discussed above, therefore, we also studied the annealing effects by a $Ti/TiN/SiO_2/FeO_x/Fe/Pt$ structure. Figure 3-29 (a), figure 3-29 (b), figure 3-29 (c) and figure 3-29 (d) show current versus voltage

(*I*-*V*) characteristics of the as-deposited, RTA-30 sec, RTA-60 sec and FA-30 min samples for 50 cycles of switching, respectively. Under the same measuring method mentioned above, driving voltage was biased on the bottom electrode while the top electrode was ground and the compliance current was limited to 5 mA during sweeping voltage. Bipolar switching is also observed for all of the annealed samples. It is noticed that besides a reduction in operation voltages (V_{set} and V_{reset}), the variances of V_{set} and V_{reset} were also improved as the annealing time increasing. Additionally, *I-V* characteristics of all the annealed samples were shown concurrently for comparison in figure 3-30 as well as statistical comparison of set/reset voltages (V_{set}/V_{reset}), set/reset current (I_{set}/I_{reset}) and set/reset power (P_{set}/P_{reset}) in figure 3-31 and figure 3-32. The almost similar phenomena in the set process region [figure 3-31] and reset region [figure 3-32] were also observed in the Ti/TiN/SiO_2/FeO_x/Fe/Pt structure, including reduction of V_{set}, V_{reset} and P_{reset}, increase of I_{set} and nearly constant maintenance of I_{reset} and P_{reset}. According to the similar statistical results of the Ti/TiN/SiO_2/FeO_x/FePt and the Ti/TiN/SiO_2/FeO_x/Fe/Pt structure, therefore, it could also be affirmed that the source of the resistive switching mechanism is contributed from the common-existed Fe atoms.

3.2.4 Conclusion

Annealing effects on reproducible resistance switching characteristics of a Ti/TiN/SiO_2/FeO_x/FePt structure as well as a Ti/TiN/SiO_2/FeO_x/Fe/Pt structure with a 600 ℃ annealing for 30 sec, 60 sec and 30 min were investigated. The annealing testing results demonstrate the improvements of the switching parameters, such as forming voltage, V_{set}, V_{reset},ΔV_{set} and ΔV_{reset},. According to the x-ray diffraction, transmission electron microscopy and x-ray photoelectron spectroscopy depth profiles analyses, exhibition of better crystallinity of the FeO_x film with a wider Fe-diffused region is suggested to provide an effective iron oxide phase transformation region for resistance switching, which gives rise to better behaviors of resistance switching.

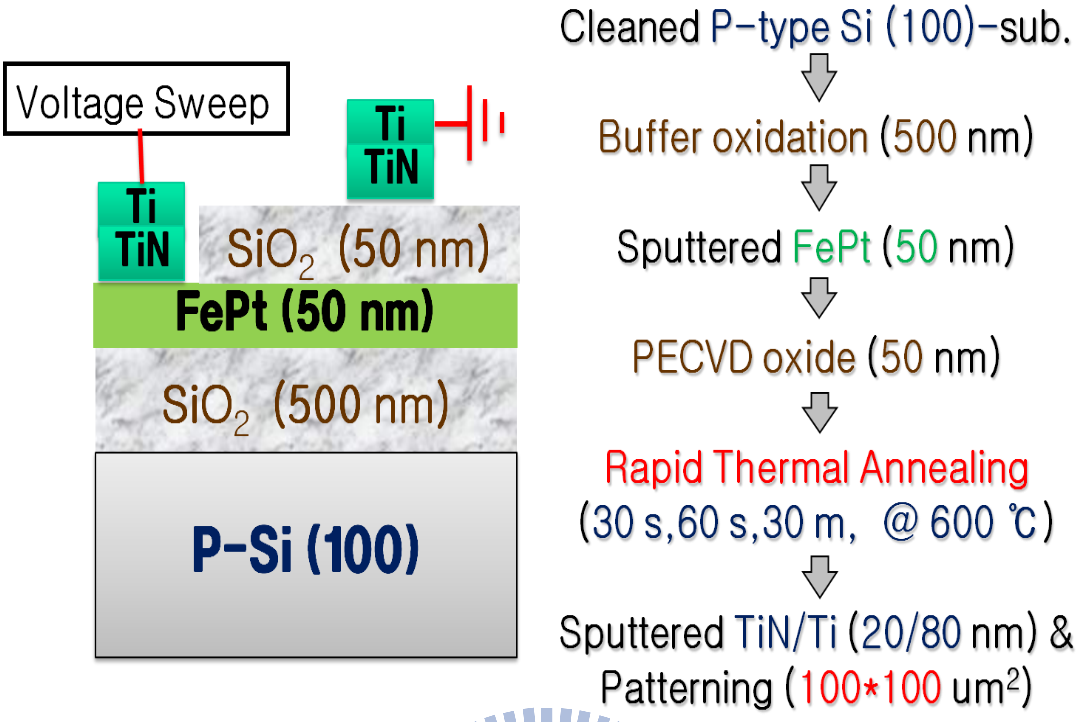


Fig. 3-18 Illustrations of the annealed Ti/TiN/SiO_2/FeO_x/FePt device structures and their process flows.

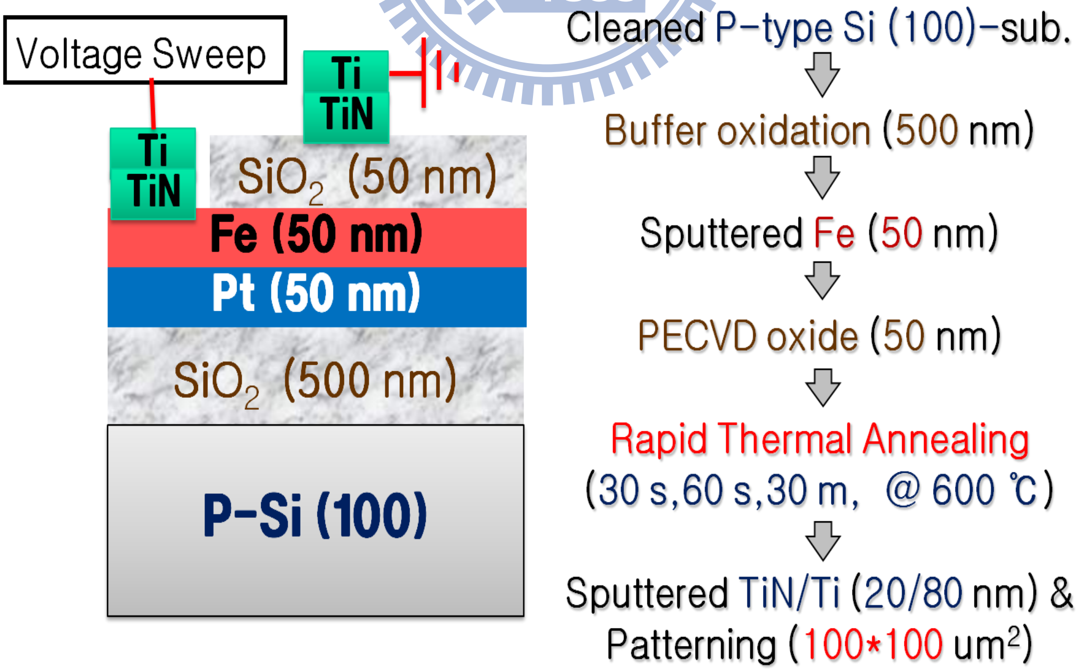


Fig. 3-19 Illustrations of the annealed Ti/TiN/SiO2/FeOx/Fe/Pt device structures and their process flows.

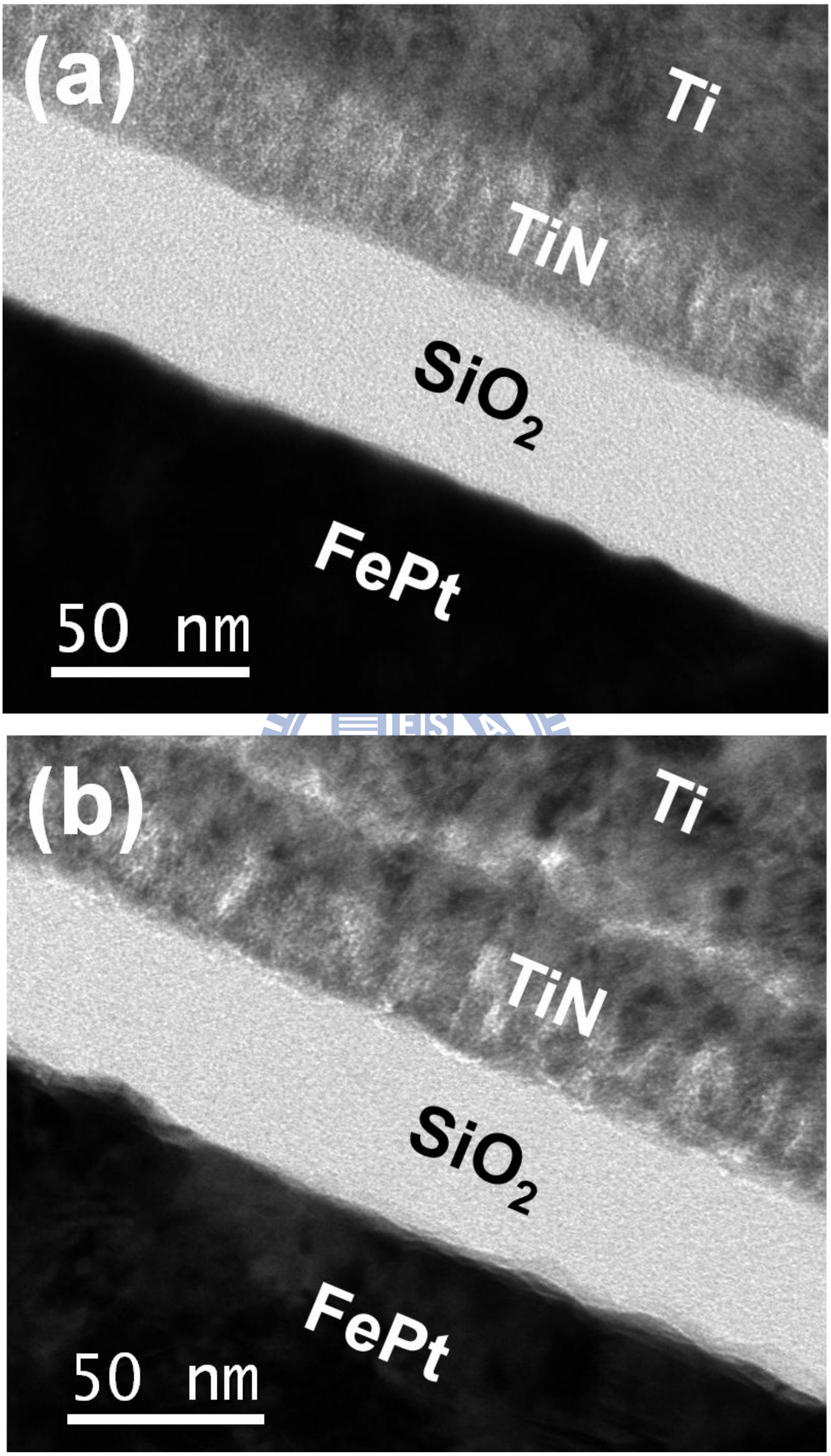


Fig. 3-20 (a) & (b) Cross-sectional TEM of the Ti/TiN/SiO_2/FeO_x/FePt structures (a) without (as-deposited condition) and (b) with a thermal treatment of RTA-30 sec.

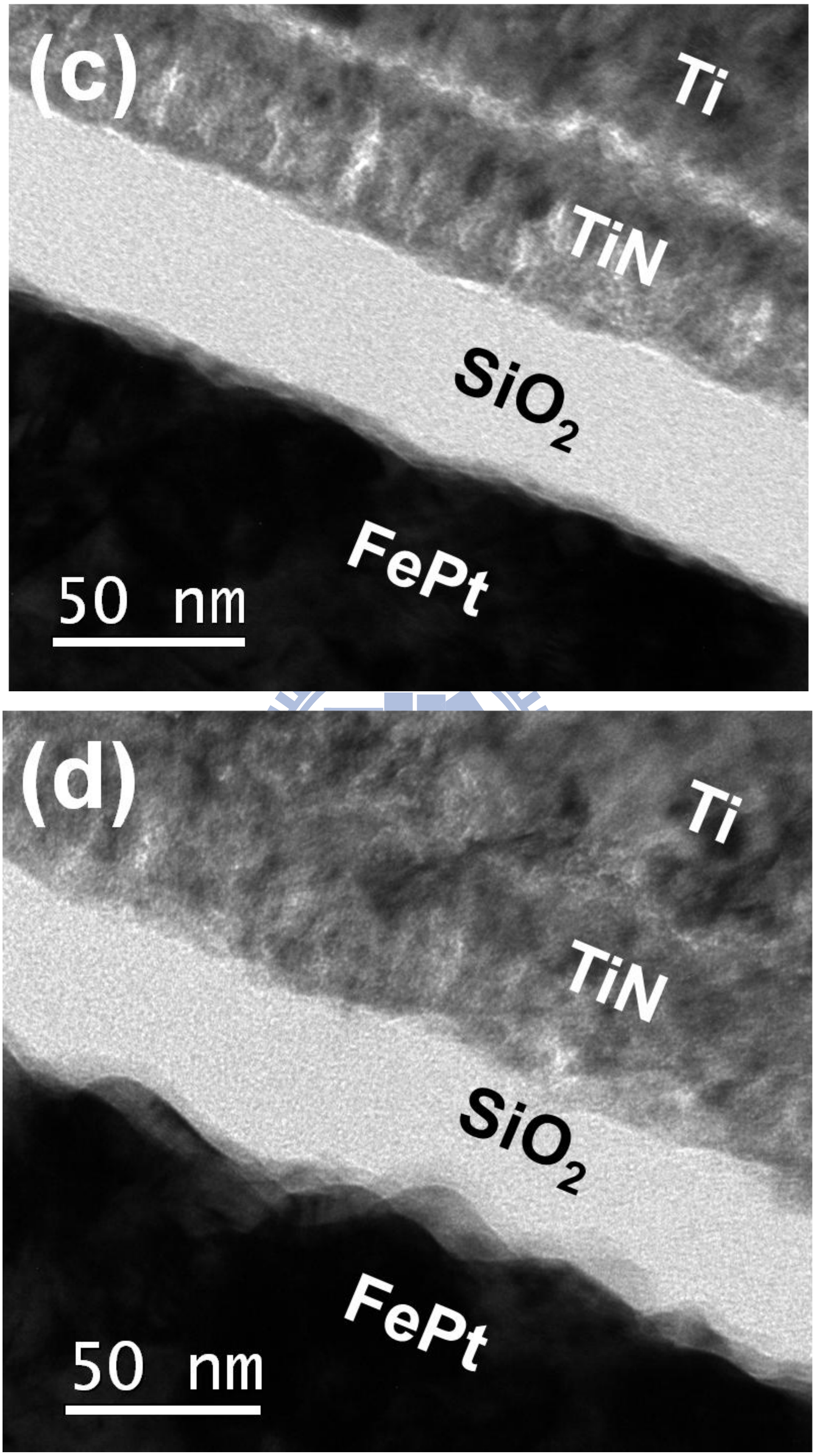


Fig. 3-20 (c) & (d) Cross-sectional TEM of the Ti/TiN/SiO_2/FeO_x/FePt structures with a thermal treatment of (c) RTA-60 sec and (d) FA-30 min at 600 ℃.

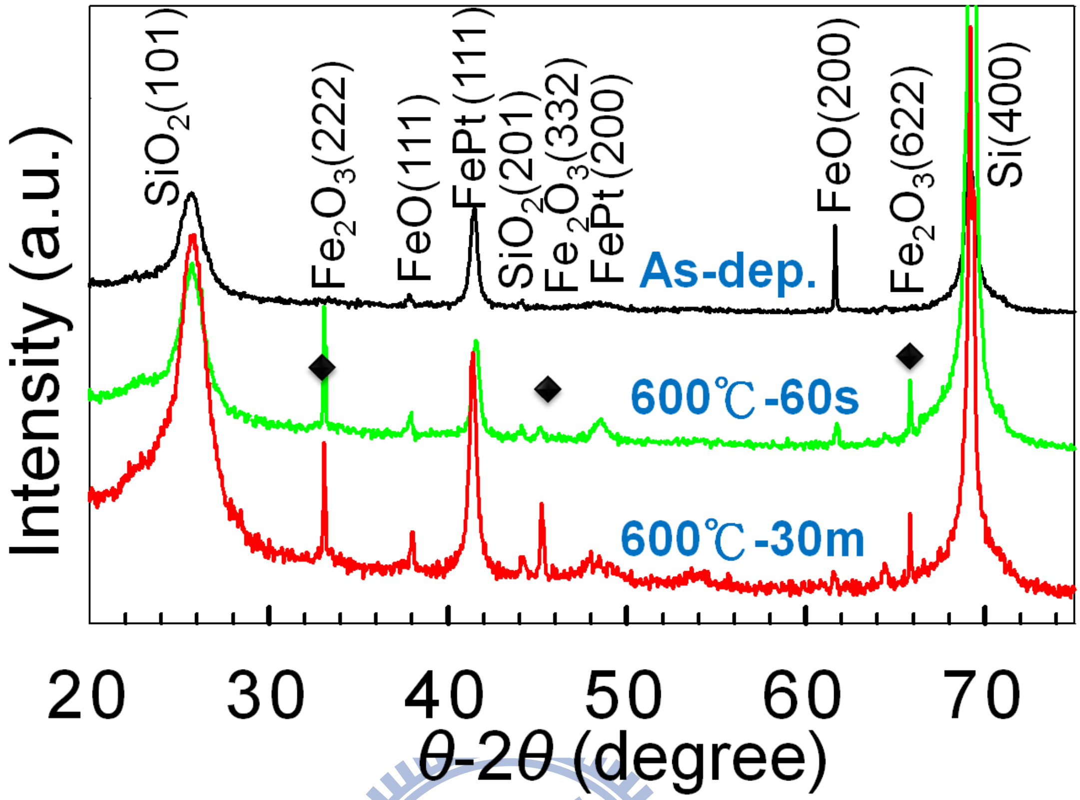


Fig. 3-21 XRD θ-2θ scan results for the TiN/SiO_2/FeO_x/FePt structures without (as-deposited condition) and with a thermal treatment of RTA-60 sec, and FA-30 min at 600 ℃. Symbol (◆) indicates the additional diffraction peaks appeared only in the thermal-treated samples and contributed from the crystallinity of FeO_x phases.

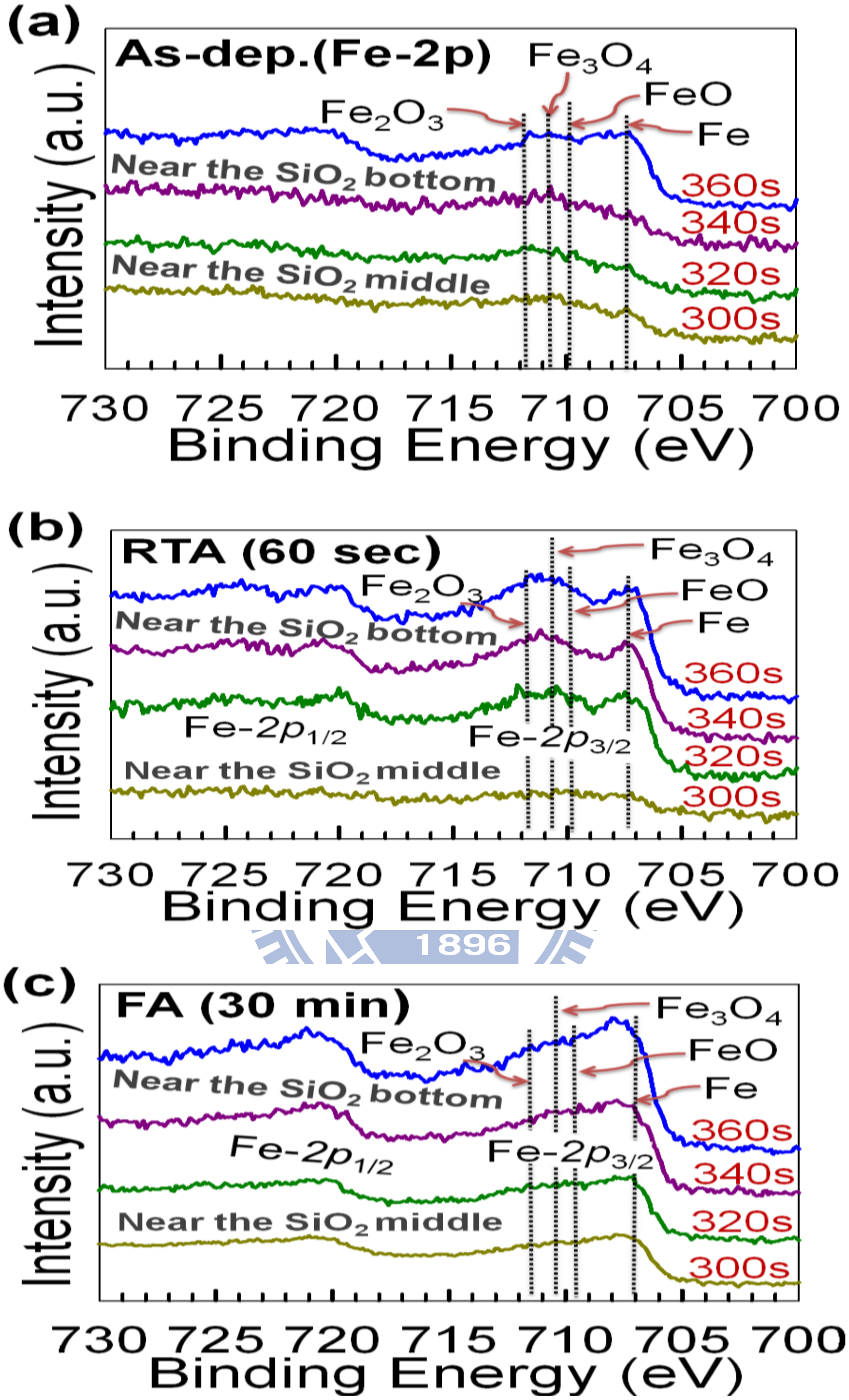


Fig. 3-22 XPS depth profiles of Fe-*2p* on the $SiO_2/FeO_x/FePt$ structures (a) without (as-deposited condition) and with a thermal treatment of (b) RTA-60 sec and (c) FA-30 min at 600 ℃. The depth profiles are obtained by an Ar sputter etching in the SiO_2 layer, collecting the XPS data at various depths. The etching times of the spectra are from bottom to top 300, 320, 340, and 360 sec.

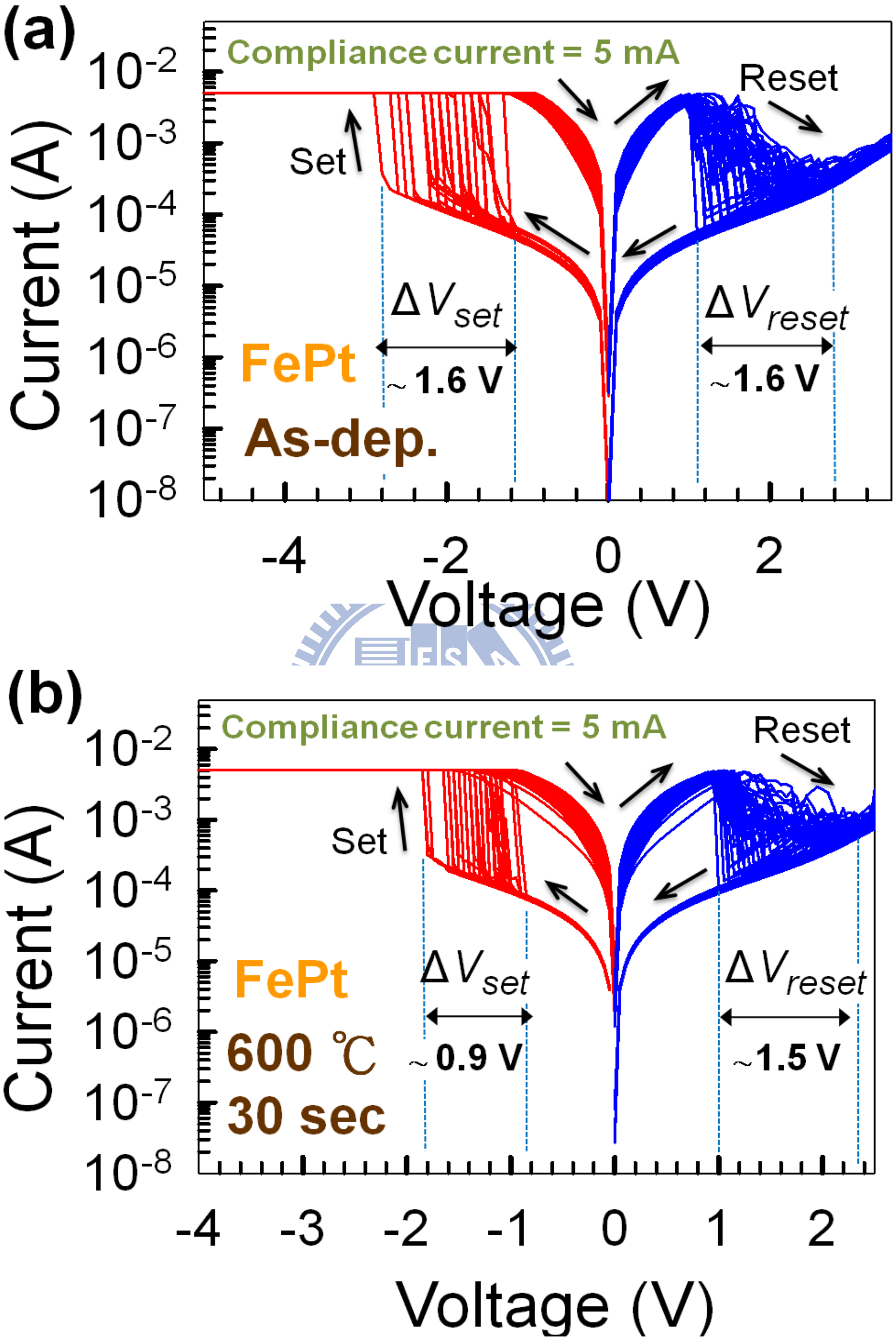


Fig. 3-23(a) & (b) 50-cycle bipolar switching behaviors of the Ti/TiN/SiO_2/FeO_x/FePt structures (a) without (as-deposited condition) and (b) with a 600 ℃-RTA for 30 sec.

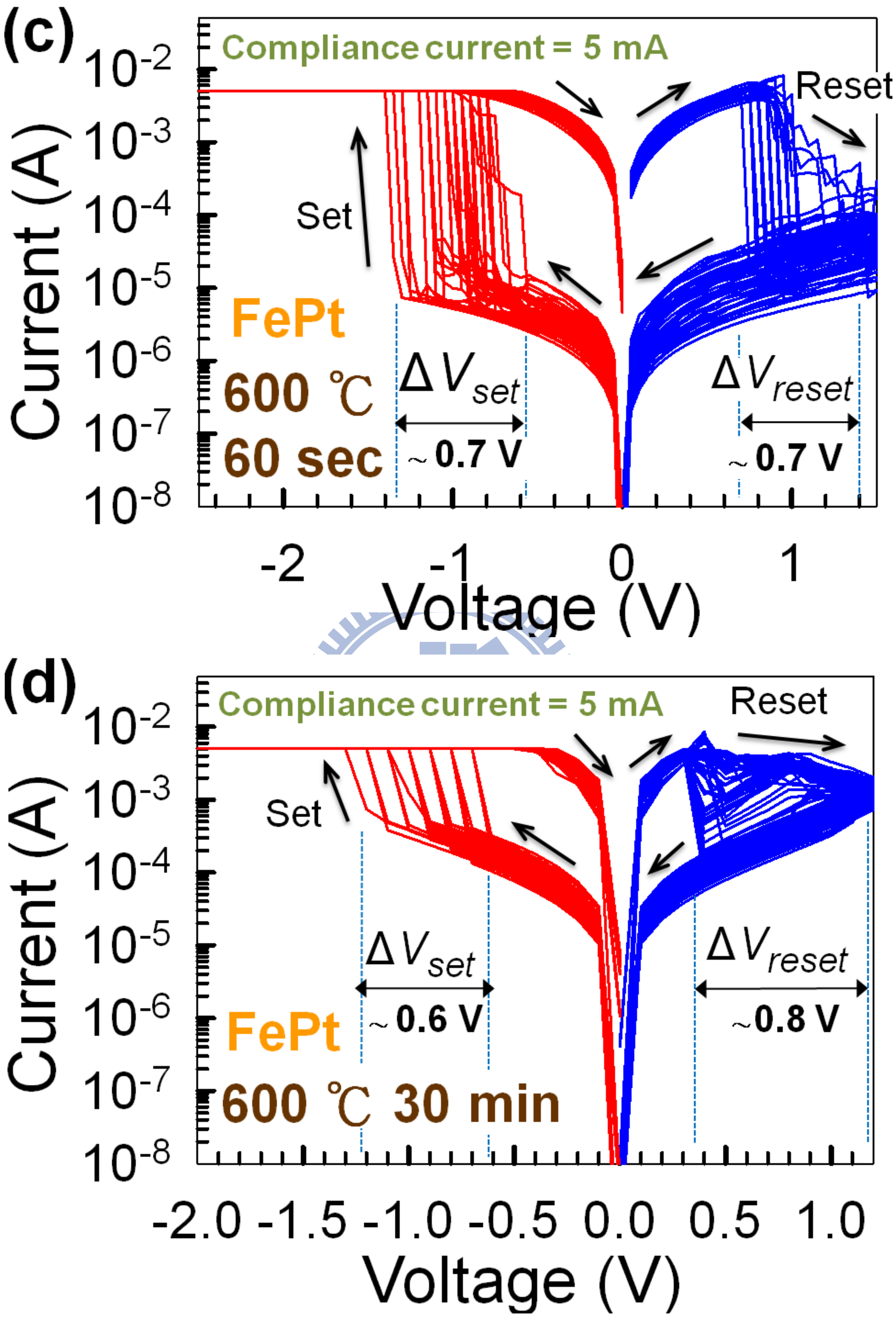


Fig. 3-23(c) & (d) 50-cycle bipolar switching behaviors of the Ti/TiN/SiO_2/FeO_x/FePt structures with a (c) 600 ℃-RTA for 60 sec and (d) 600 ℃-FA for 30 min.

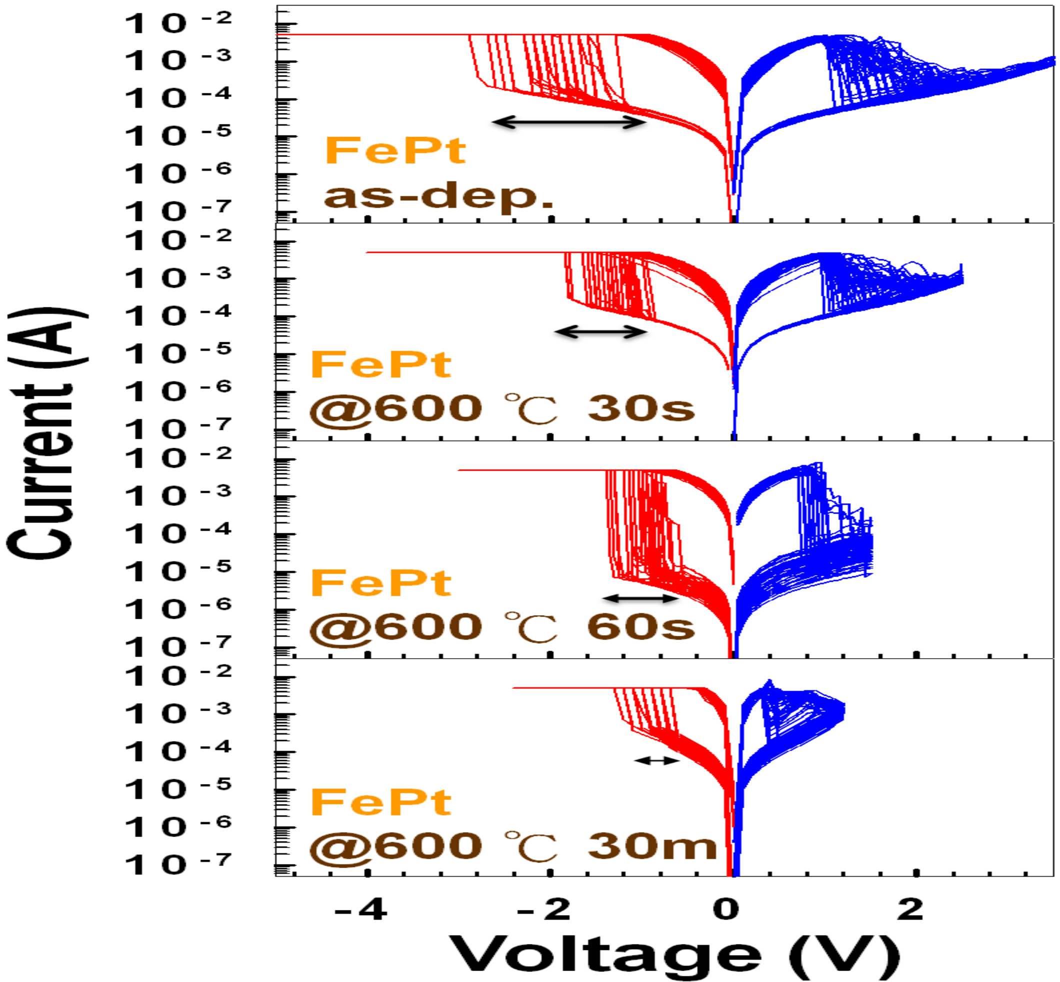


Fig. 3-24 All *I-V* comparisons of the Ti/TiN/SiO_2/FeO_x/FePt structure with different thermal-treated conditions.

600 ℃	**V_{set} (V)**	**V_{reset} (V)**	**I_{set} (mA)**	**I_{reset} (mA)**	**P_{set} (mW)**	**P_{reset} (mW)**	**Forming Voltage**
As-dep.	-1.9	1.0	0.133	4.40	0.26	4.45	~26 V
30 sec	-1.2	1.0	0.175	4.44	0.23	4.33	~1.3 V
60 sec	-0.9	0.8	0.018	3.96	0.16	3.01	~0.6 V
30 min	-0.8	0.3	0.349	4.47	0.29	1.39	~0.37 V

Table 3-2 Comparison of the mean value of Set & Reset voltage, Set & Reset current, Set & Reset power and forming voltage of the Ti/TiN/SiO_2/FeO_x/FePt structure between different annealing conditions.

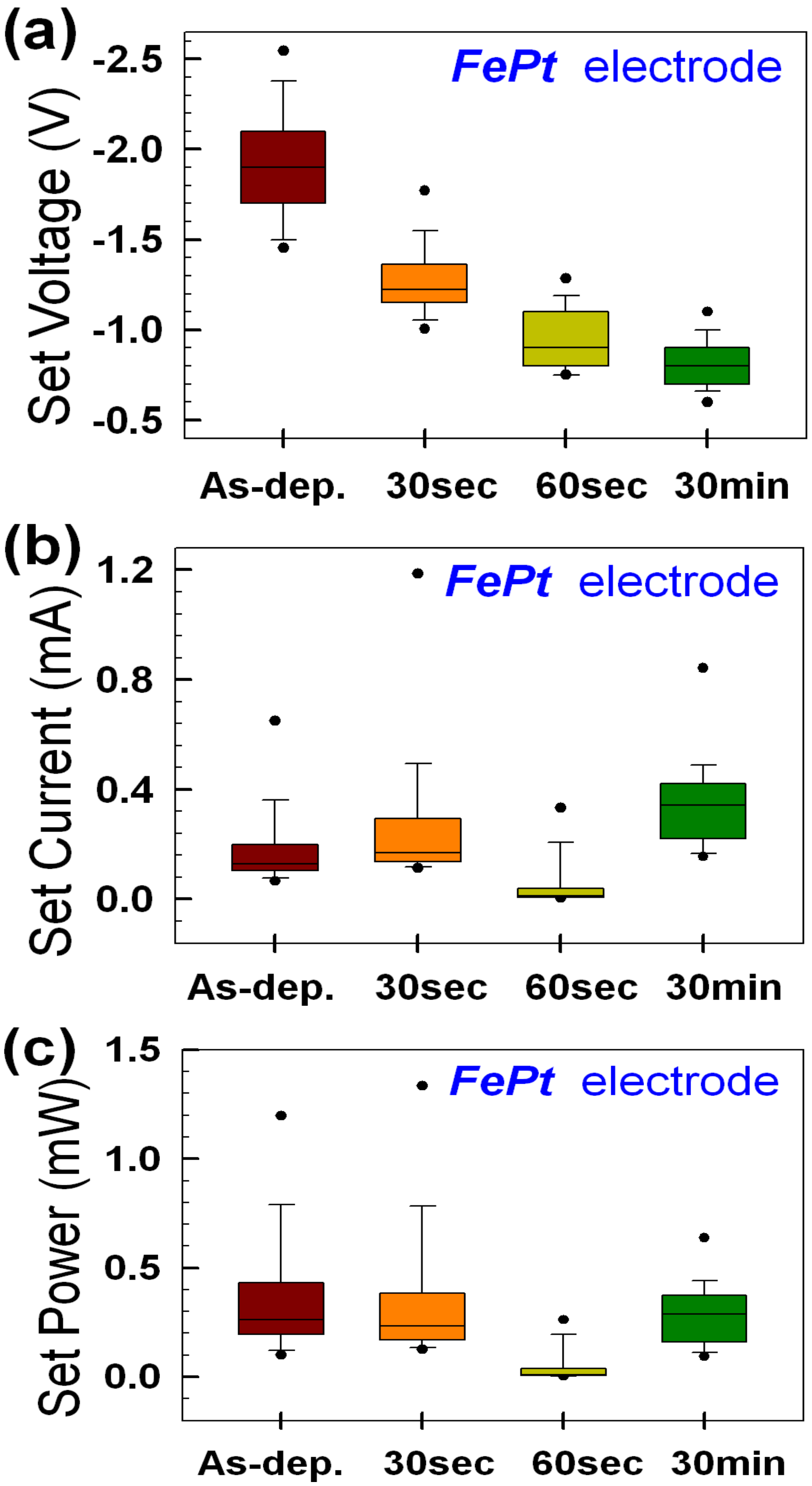


Fig. 3-25 Statistical comparisons of (a) set voltage, (b) set current, and (c) set power for the different thermal-treated Ti/TiN/SiO_2/FeO_x/FePt structures.

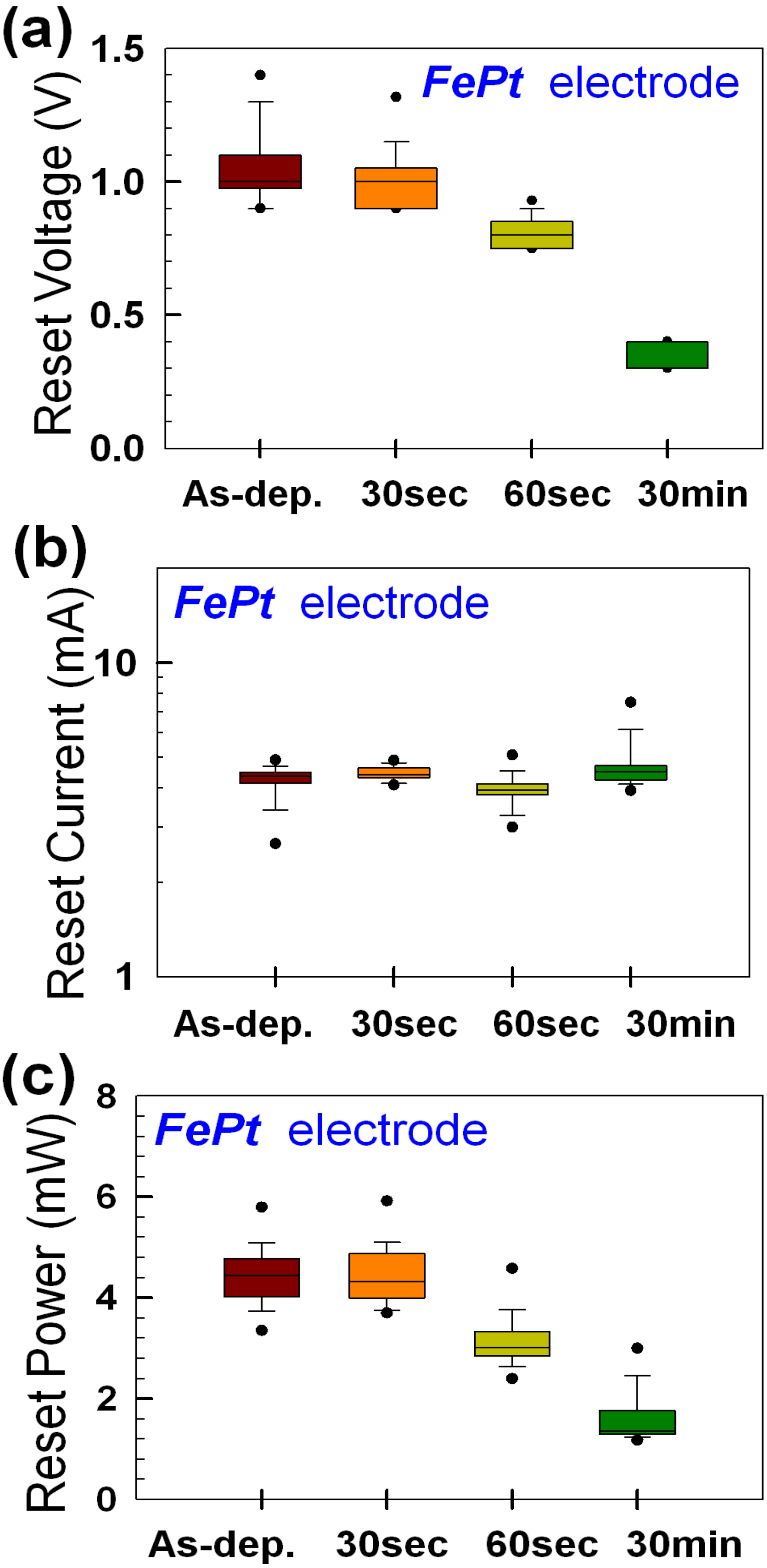


Fig. 3-26 Statistical comparisons of (a) reset voltage, (b) reset current, and (c) reset power for the different thermal-treated Ti/TiN/SiO_2/FeO_x/FePt structures.

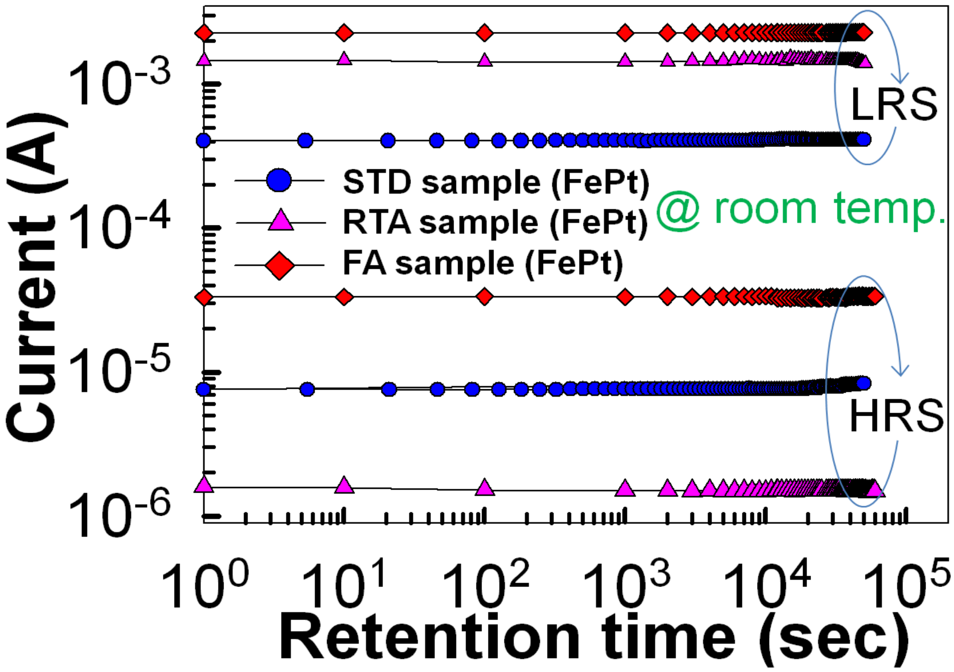


Fig. 3-27 Room-temperature retention comparisons of the Ti/TiN/SiO_2/FeO_x/FePt structures without (as-deposited condition) and with a thermal treatment of RTA-60 sec and FA-30 min at 600 ℃.

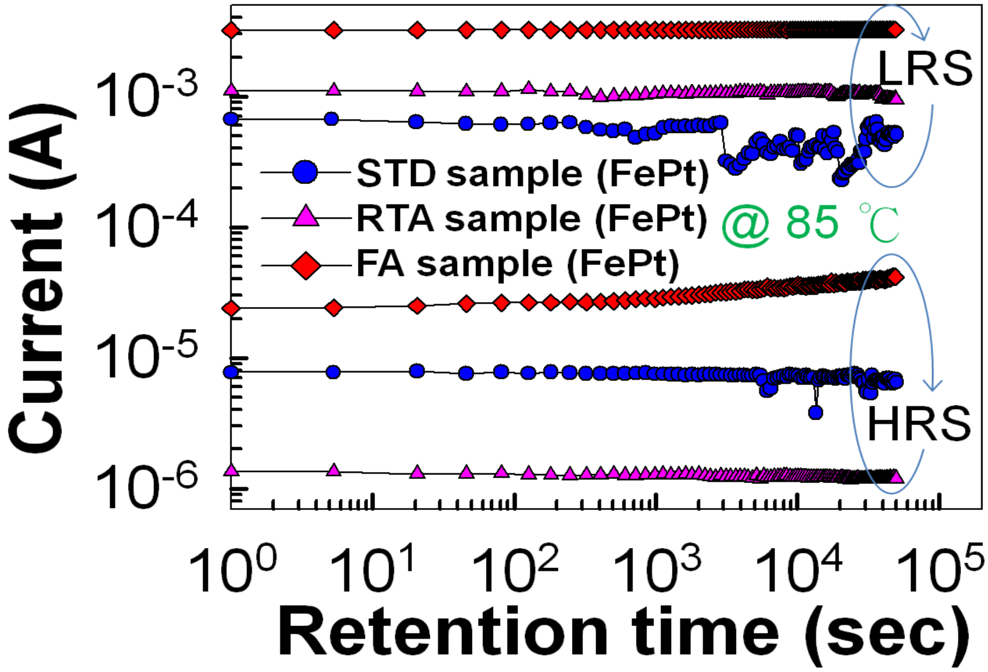


Fig. 3-28 85 ℃ retention comparisons of the Ti/TiN/SiO_2/FeO_x/FePt structures without (as-deposited condition) and with a thermal treatment of RTA-60 sec and FA-30 min at 600 ℃.

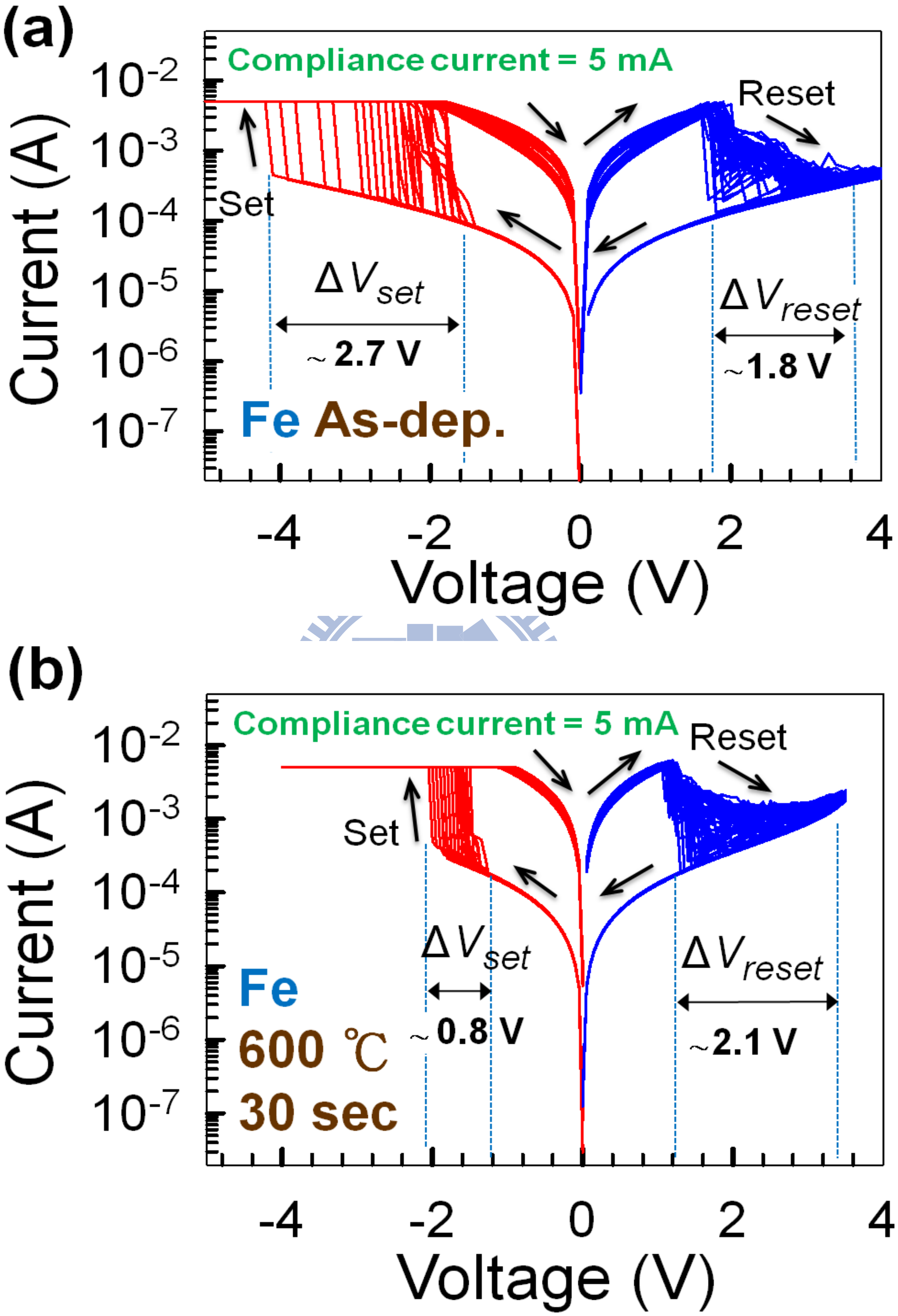


Fig. 3-29 (a) & (b) 50-cycle bipolar switching of the Ti/TiN/SiO_2/FeO_x/Fe/Pt structures (a) without (as-deposited condition) and (b) with a 600 ℃-RTA for 30 sec.

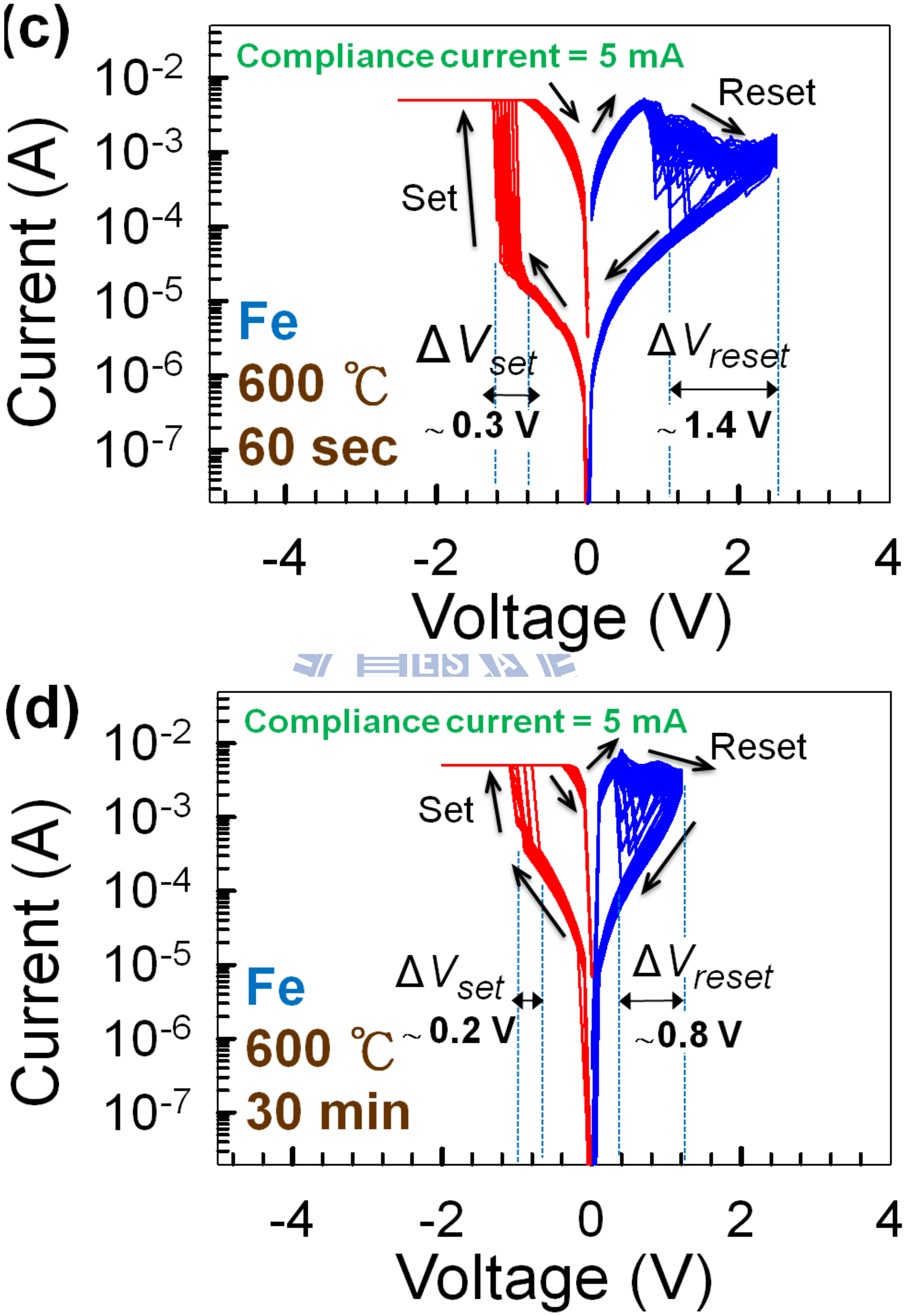


Fig. 3-29 (c) & (d) 50-cycle bipolar switching of the Ti/TiN/SiO_2/FeO_x/Fe/Pt structures with a (c) 600 ℃-RTA for 60 sec and (d) 600 ℃-FA for 30 min.

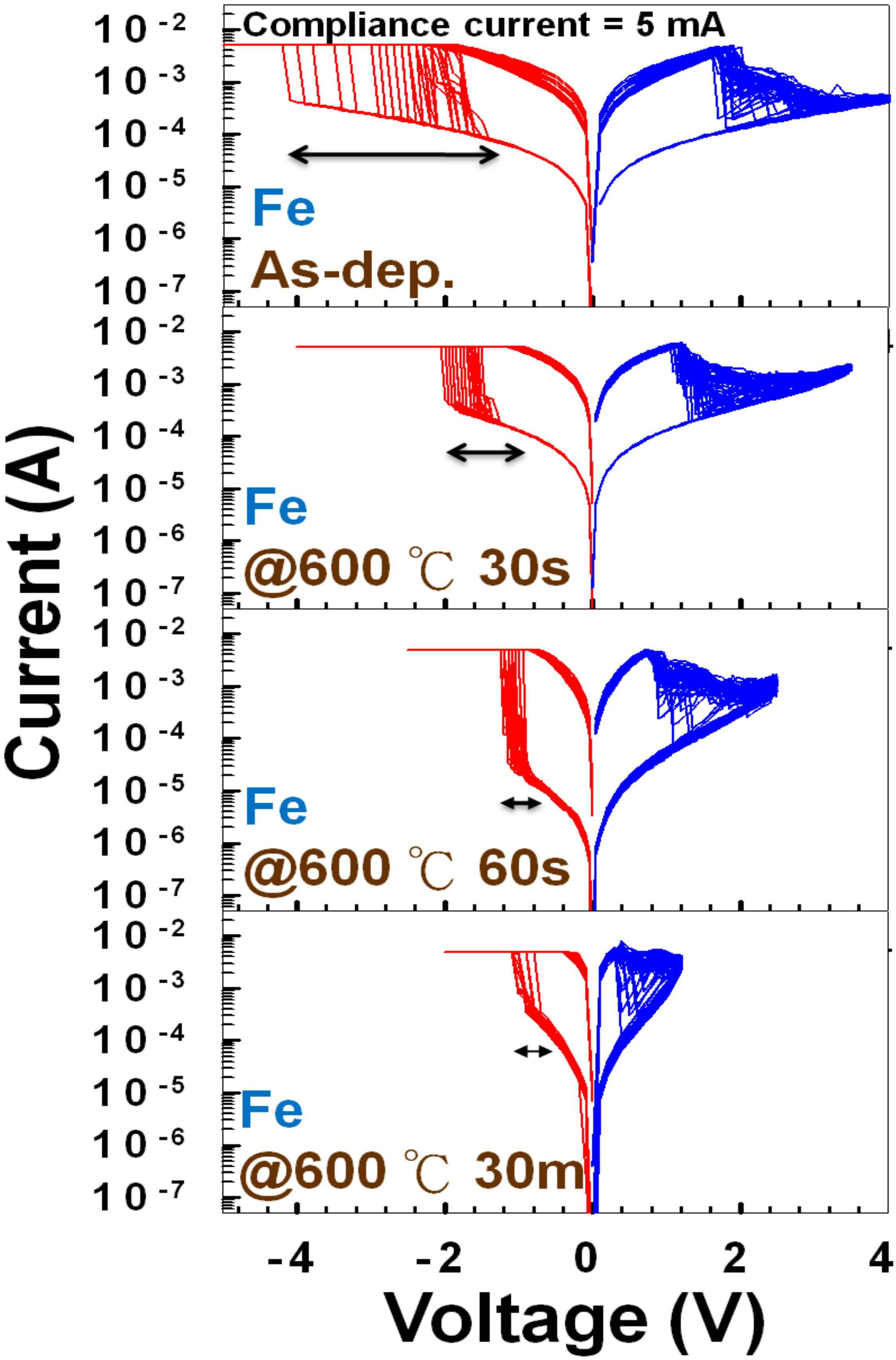


Fig. 3-30 All *I-V* characteristics comparison of the Ti/TiN/SiO_2/FeO_x/Fe/Pt structures with different thermal-treated conditions.

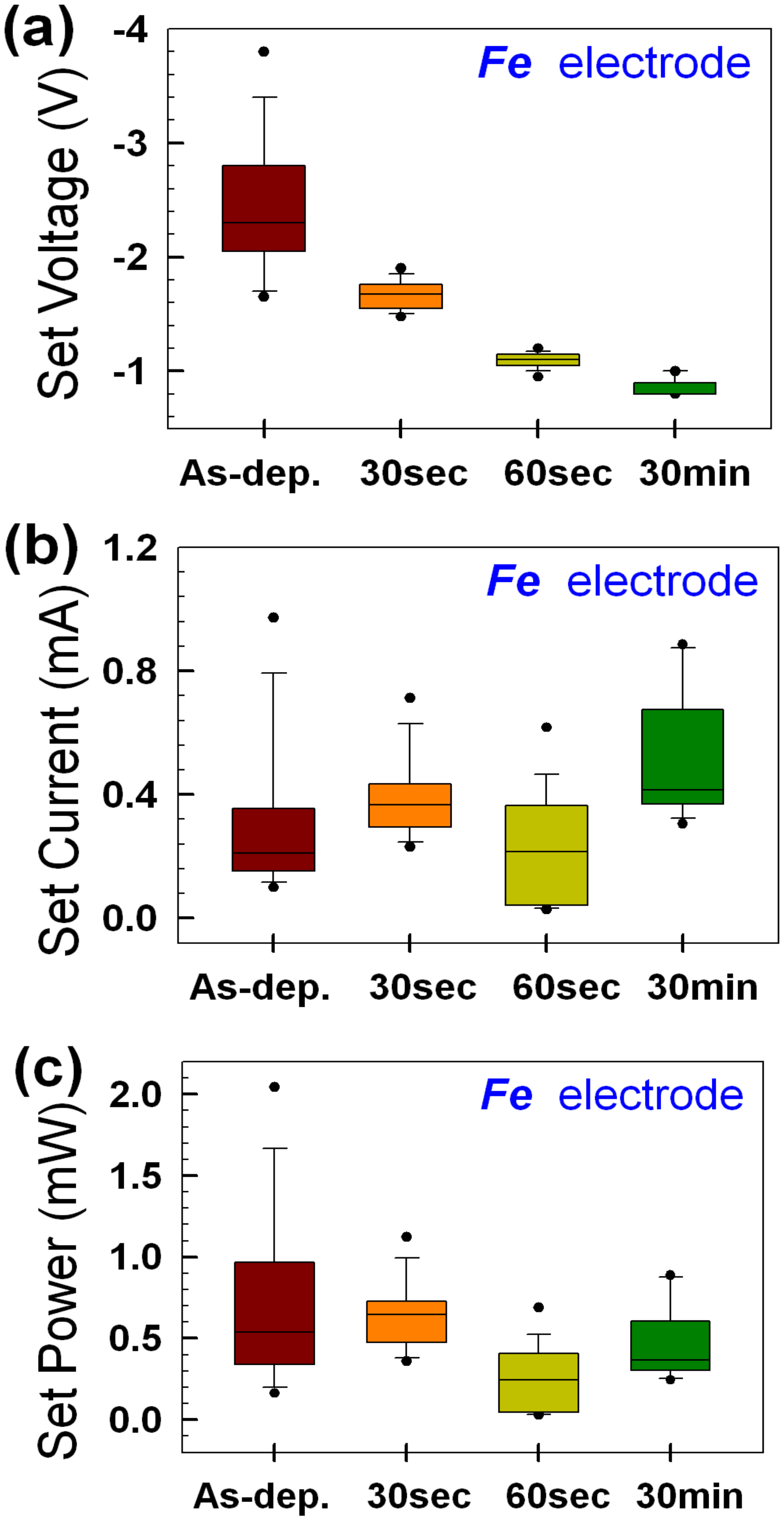


Fig. 3-31 Statistical comparisons of (a) set voltages, (b) set current, and (c) set power for the different thermal-treated Ti/TiN/SiO_2/FeO_x/Fe/Pt structures.

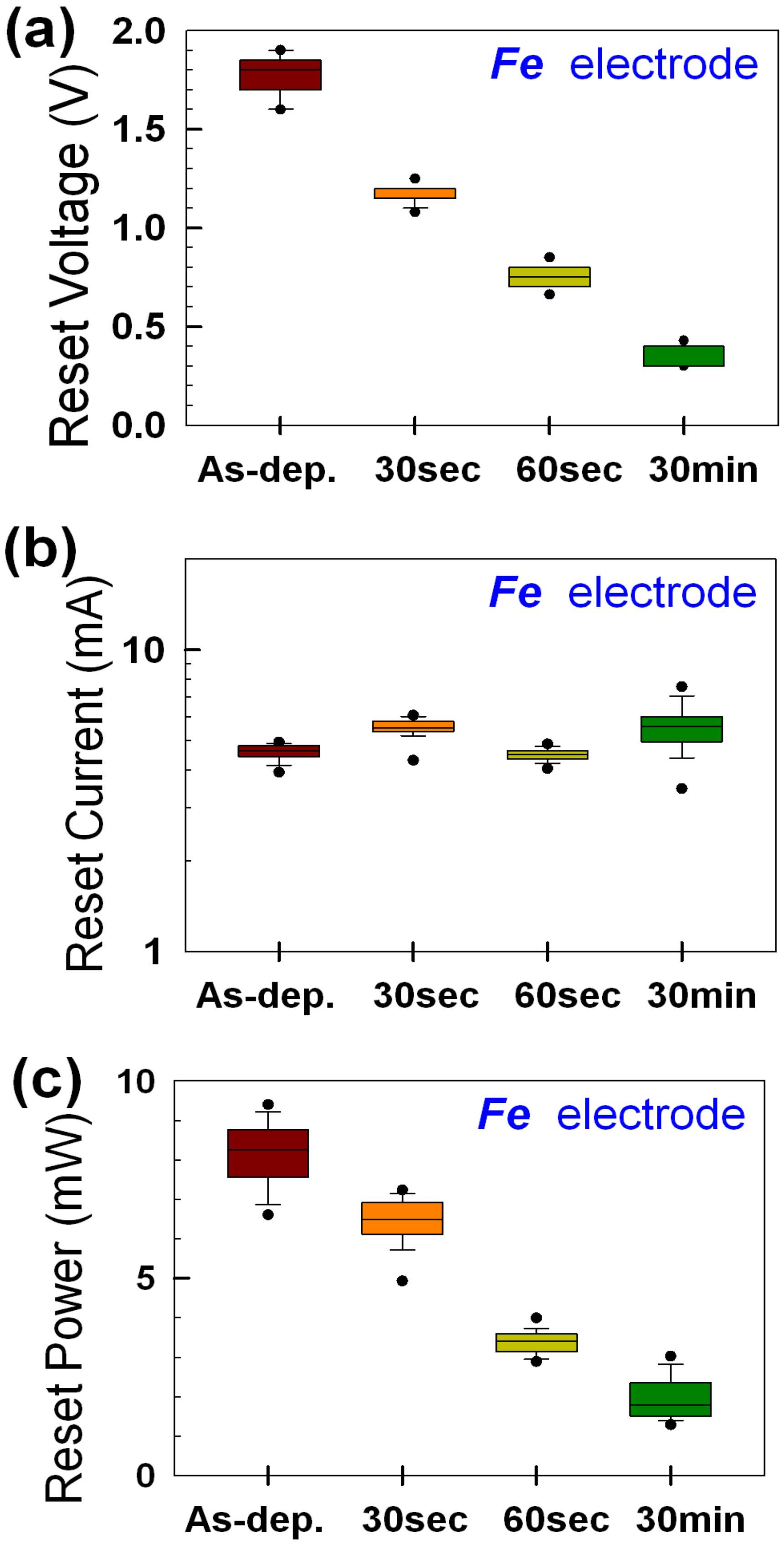


Fig. 3-32 Statistical comparisons of (a) reset voltages, (b) reset current, and (c) reset power for the different thermal-treated Ti/TiN/SiO_2/FeO_x/Fe/Pt structures.

B. Multi-Level Effects

3.3 Tunable resistance switching characteristics in a thin FeO_x-transition layer by controlling sweeping voltage and compliance current

3.3.1 Introduction

In electronics, a multi-level cell is a memory element capable of storing more than a single bit of information. For example, if a multi-level cell stores four states per cell, so the four states yield two bits of information per cell. Therefore, a multi-level cell provides the advantage of less cost per megabyte of storage to manufacture for economical productions.

Basing on the same concept, phenomenon of exhibiting multiple resistance states were also examined in our proposed FeO_x-contained resistive switching device. Fortunately, observation of multiple resistance states is easy to obtain by justifying the sweeping voltage during the reset process region and the compliance current during the set process region so as to allow more bits to be stored per cell in the Fe-electrode-contained structure for a wide and practical application. Moreover, extracting the statistical results, set/reset voltage, set/reset current and set/reset power, in different sweeping voltages and compliance currents conditions also further provides more details to clarify the mechanism of the FeO_x-contained resistive switching behaviors.

3.3.1 Experiment

The resistance switching memory devices were prepared through the same processes mentioned above. After thermal oxidation of P-type (100) silicon wafers, a 50-nm-thick Fe and a 50-nm-thick Pt layer were deposited sequentially as a bottom electrode by DC magnetron. Then, a ~50-nm-thick SiO_2 layer was deposited by plasma enhanced chemical vapor deposition system with a substrate temperature of 300 ℃ and a working pressure of (TEOS+O_2) gases at 300 mTorr. A 20-nm-thick TiN and a 80-nm-thick of Ti were sputtered sequentially as the top electrode and patterned in a square area with side length of 100 μm on the SiO_2 film. Finally, a rapid thermal annealing treatment at 600 ℃ for 60 sec was performed in argon ambient. Keithley 4200 semiconductor characterization system is used to measure the current-voltage (*I*-*V*) characteristics of the fabricated devices.

It is noted that definitions of the “On Current” and “Off Current” are the values of the current measured in the LRS and HRS with a voltage bias of 0.2 V, respectively. The “On/Off Current ratio” is defined as the ratio of On Current” to “Off Current”. In addition, definitions of the “Set Current” and “Set Voltage” are the values of the current and voltage detected at the beginning of the resistance switching from a HRS to a LRS, respectively. The “Set Power” is defined as the product of “Set Current” and “Set Voltage” .Similarly, definitions of the “Reset Current” and “Reset Voltage” are the values of the current and voltage detected at the beginning of the resistance switching from a LRS to a HRS, respectively. The “Reset Power” is defined as the product of “Reset Current” and “Reset Voltage”

3.3.1 Results and discussion

(a) Compliance Current Effects

Figure 3-33 shows continuous bipolar switching behaviors of the 600 ℃-60 sec annealed Ti/TiN/SiO_2/FeO_x/Fe/Pt structure under a series of compliance current limitations, 0.3 mA, 0.5 mA, 0.8 mA, 1 mA, 3 mA, 5 mA, 8 mA, and 10 mA, during set voltage sweeping. It is obviously observed that the resistive state of the FeO_x material could be easily tunable by controlling the compliance current. In addition, statistics of “On current”, “Off current”, and “On/Off current ratio” with different compliance currents were also extracted and shown in figure 3-34. The “On current” was defined as the LRS current measured at 0.2 V voltage bias and the “Off current“ was defined as the HRS current measured at 0.2 V voltage bias as well. The “On current” increases with the increase of compliance current instead of the nearly constant maintained “Off current”, and, therefore, the “On/Off current ratio” increases with the increase of the compliance current. It is suggested that higher compliance current could provide higher power for the resistive switching material without limiting the phase transformation from HRS to LRS, so a lower resistive state was reached to exhibit a larger “On current”. Moreover, statistics of set/reset voltage, set/reset current and set/reset power with compliance currents were also studied and shown in figure 3-35 and figure 3-36. Almost of the reset parameters, such as set voltage, set current and set power, increase with the compliance current except the set voltage at higher compliance current conditions of 8 mA and 10 mA [figure 3-35]. The cause of the reset parameters increase was naturally suggested to the severe phase transformation of LRS (in other word, further “turn on”) so that larger reset current as well as reset power was required to recover from LRS to HRS. The sudden drop of the reset voltage at a higher sudden compliance current condition was supposed that the reset process is dominated by the reset current, so the lower reset voltage was required to obtain a larger current especially when the resistive state are quite low. On the other hand, the compliance current was, however, independent to the set parameters, including set voltage, set current and set power, as shown in figure 3-36. It is because that the set parameters are mainly affected and controlled by the HRS, which exhibits neglect variation under different compliance current conditions.

(b) Stopped Sweeping Voltage effects

Figure 3-37 shows continuous bipolar switching behaviors of the Ti/TiN/SiO_2/FeO_x/Fe/Pt structure with the 600 ℃-60 sec treated condition under a series of stopping voltage, 1.25 V, 1.5 V, 1.75 V, 2 V, 2.25 V, 2.5 V, and 2.75 V, in reset region. The stopping voltage is defined as the maximum value of positively sweeping voltage. It is obviously observed that the resistive state of the FeO_x material could be easily tunable by controlling the stopping voltage. In addition, statistics of On current, Off current, and On/Off current ratio with different stopping voltages were also extracted and shown in figure 3-38. The Off current decreases and then saturates with the increase of stopping voltage instead of the nearly constant maintained On current, and, therefore, the On/Off current ratio increases and finally saturates with increasing the stopping voltage. It is suggested that higher stopping voltage could provide more complete recover from LRS to HRS, so a higher resistive state was reached to exhibit a smaller Off state current. Moreover, statistics of set/reset current, set/reset current and set/reset power with compliance currents were also studied and shown in figure 3-39 and figure 3-40.

For set parameters, it is observed that set voltage, which slightly increases with increasing stopping voltage, was in contrast to the set current, which decreases with stopping voltage. However, the set power was calculated to slightly reduce due to the more rapid decrease of set current [figure 3-39]. According to these results, it is suggested that the major fact affecting the set process for a higher resistance state is dependent on larger set voltage, which is correspondent to the different electrode results of Fe and FePt.

On the other hand, the influence of stopping voltage was, however, independent to the reset parameters, including reset voltage, reset current and reset power, as shown in figure 3-40. It is because that the reset parameters are mainly associated with the LRS, which exhibits neglect variation under different compliance current conditions. Therefore, the stopping voltage affects how low the resistive state recovers.

3.3.1 Conclusion

Multi-level resistance switching characteristics in a thin FeO_x-transition layer were studies by controlling the maximum sweeping voltage during reset process and the maximum current compliance during set process. It is observed that the compliance current value mainly influences the LRS and is nearly independent to the HRS. On the other hand, the HRS is mainly influenced by the stopping voltage instead of the LRS.

(a)

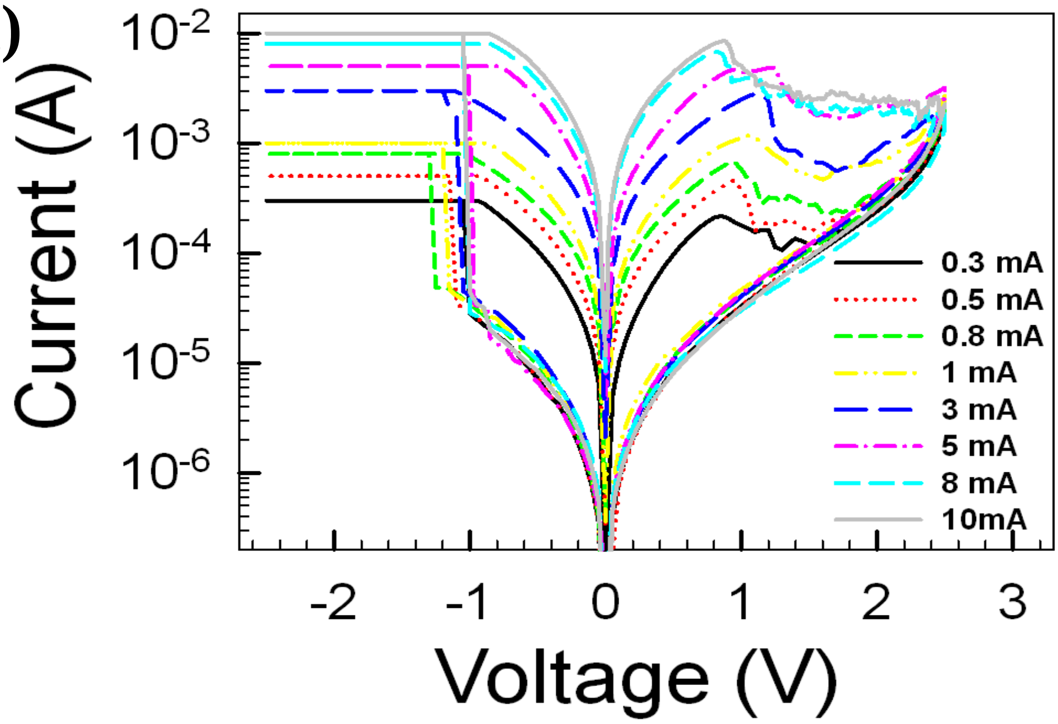


Fig. 3-33 (a) Continuous bipolar switching behaviors of the 600 ℃-60 sec treated Ti/TiN/SiO_2/FeO_x/Fe/Pt structure under a series of compliance current limitations.

(b)

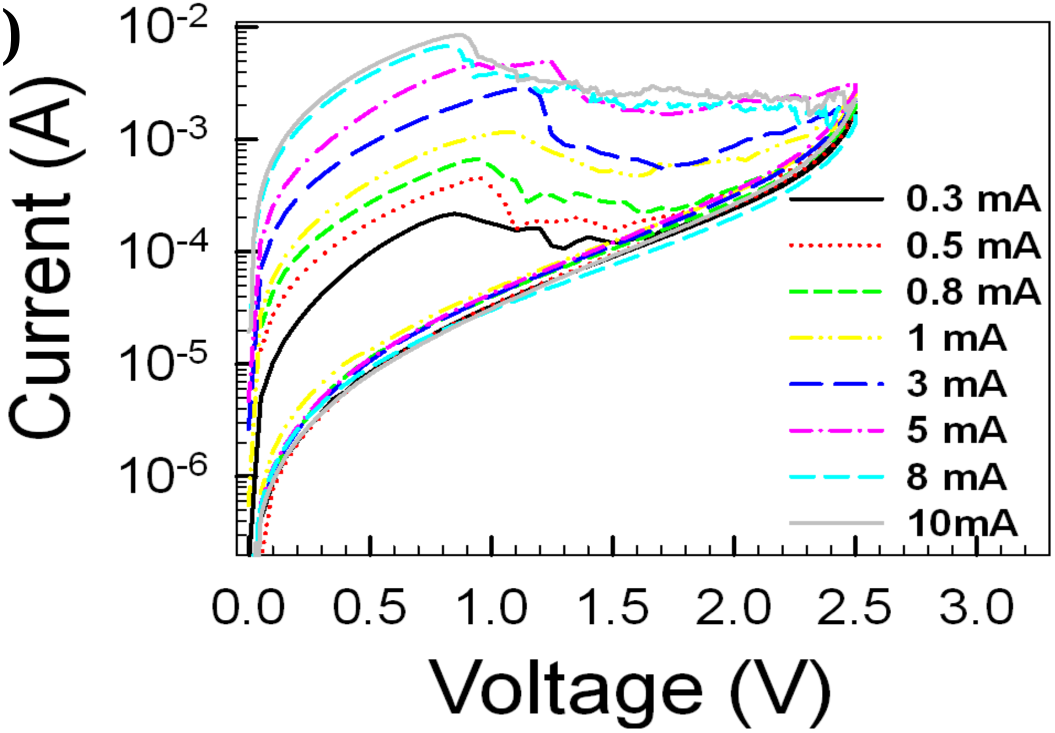


Fig. 3-33 (b) Enlarged replot of Fig. 3-29(a) for continuous reset region under a series of compliance current limitations in the reset region.

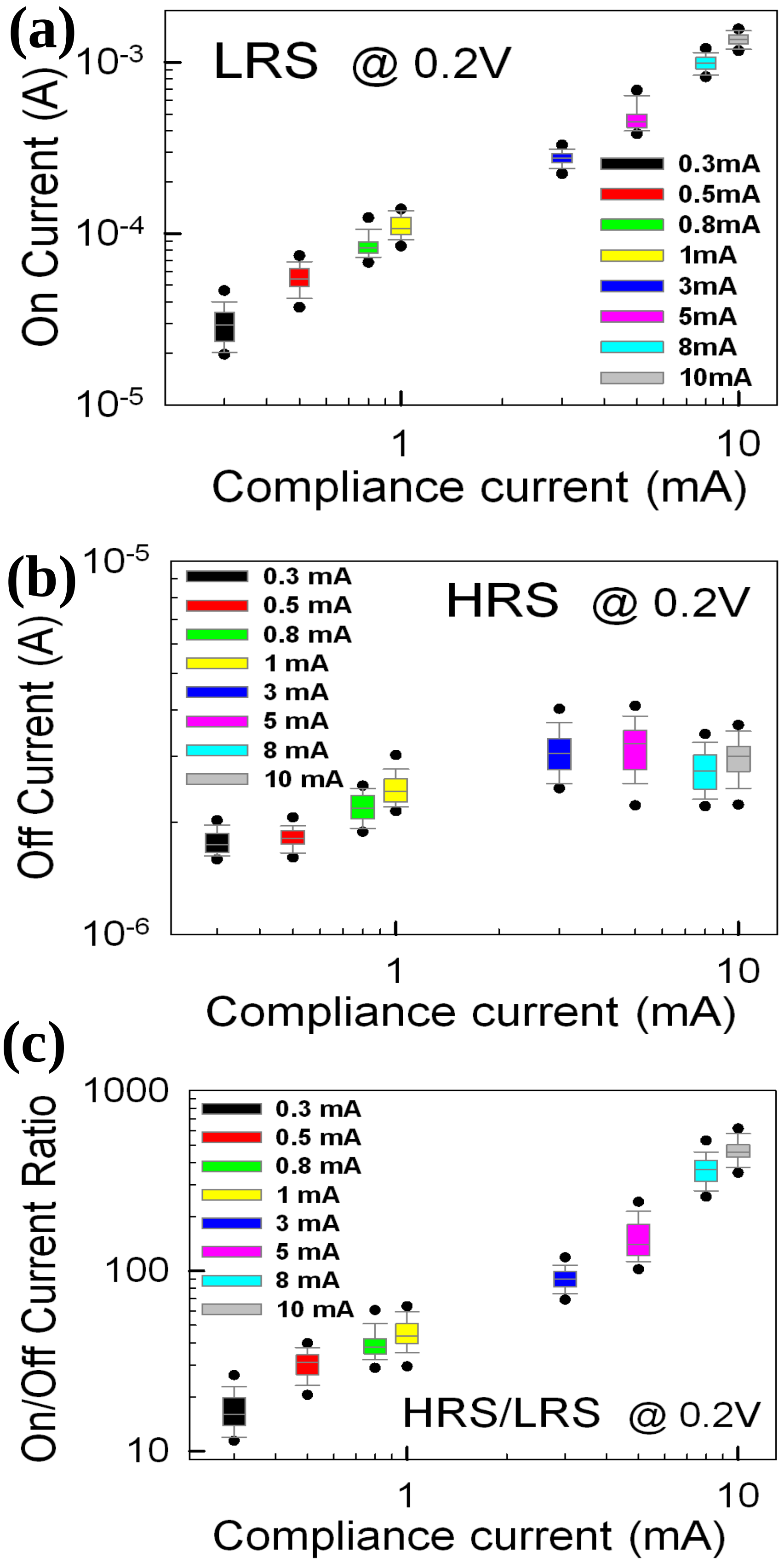


Fig. 3-34 Statistics of (a) On current, (b) Off current, and (c) On/Off current ratio for the 600 ℃-60 sec treated Ti/TiN/SiO_2/FeO_x/Fe/Pt structure with compliance currents.

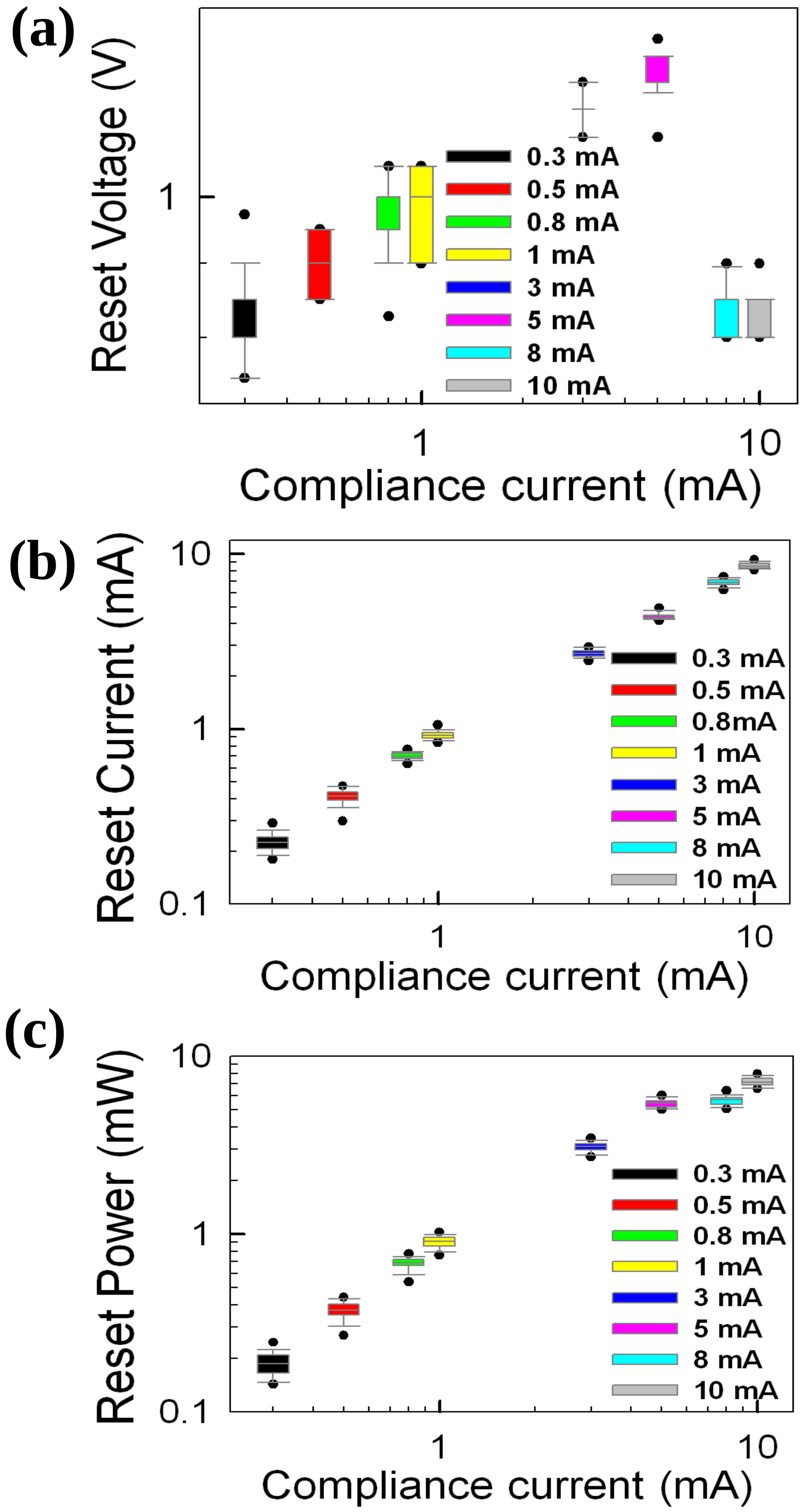


Fig. 3-35 Statistics of (a) reset current, (b) reset current, and (c) reset power for the 600 ℃-60 sec treated Ti/TiN/SiO_2/FeO_x/Fe/Pt structure with compliance currents.

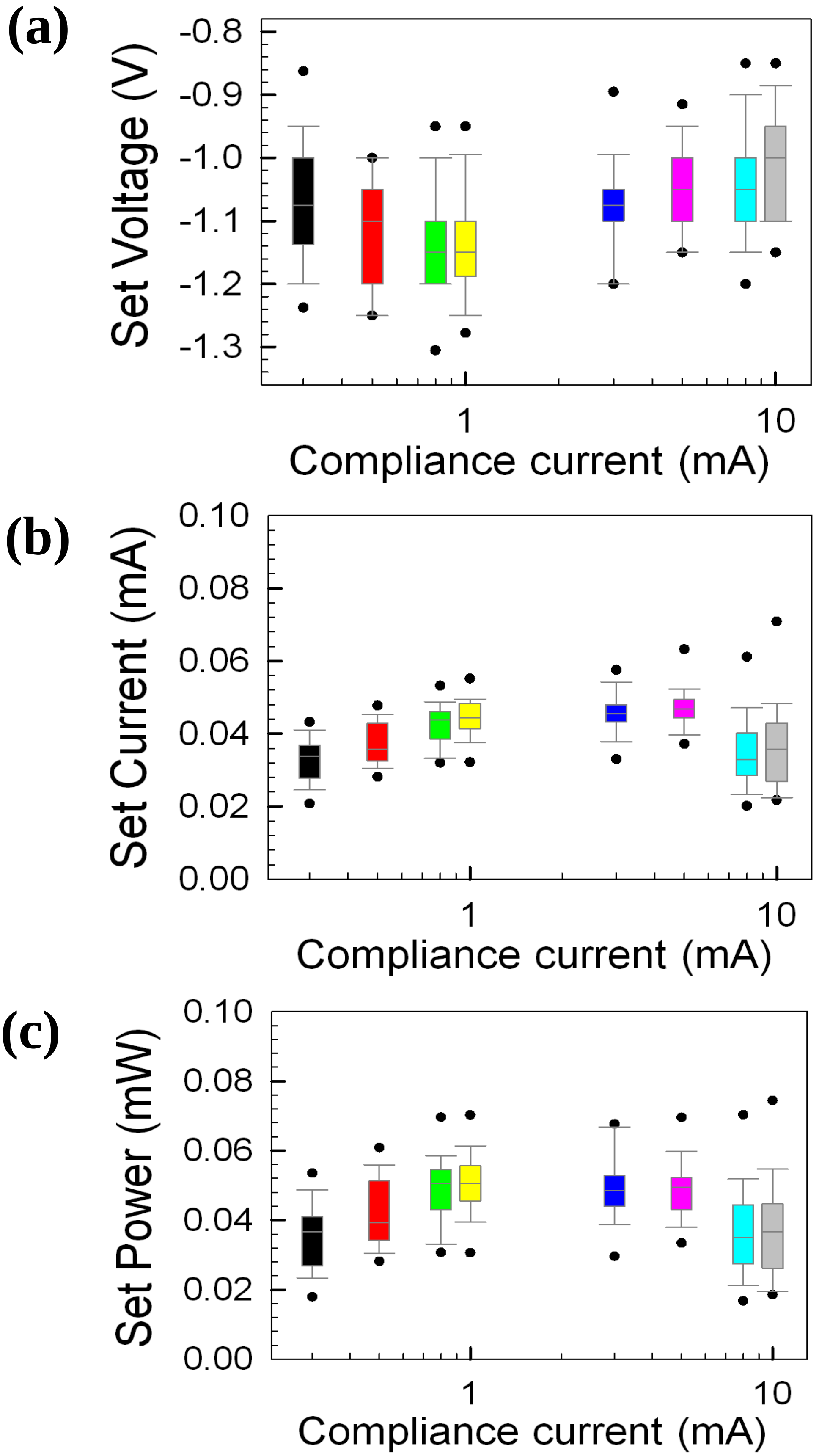


Fig. 3-36 Statistics of (a) set voltage, (b) set current and (c) set power for the 600 ℃ -60 sec treated Ti/TiN/SiO_2/FeO_x/Fe/Pt structure with compliance currents.

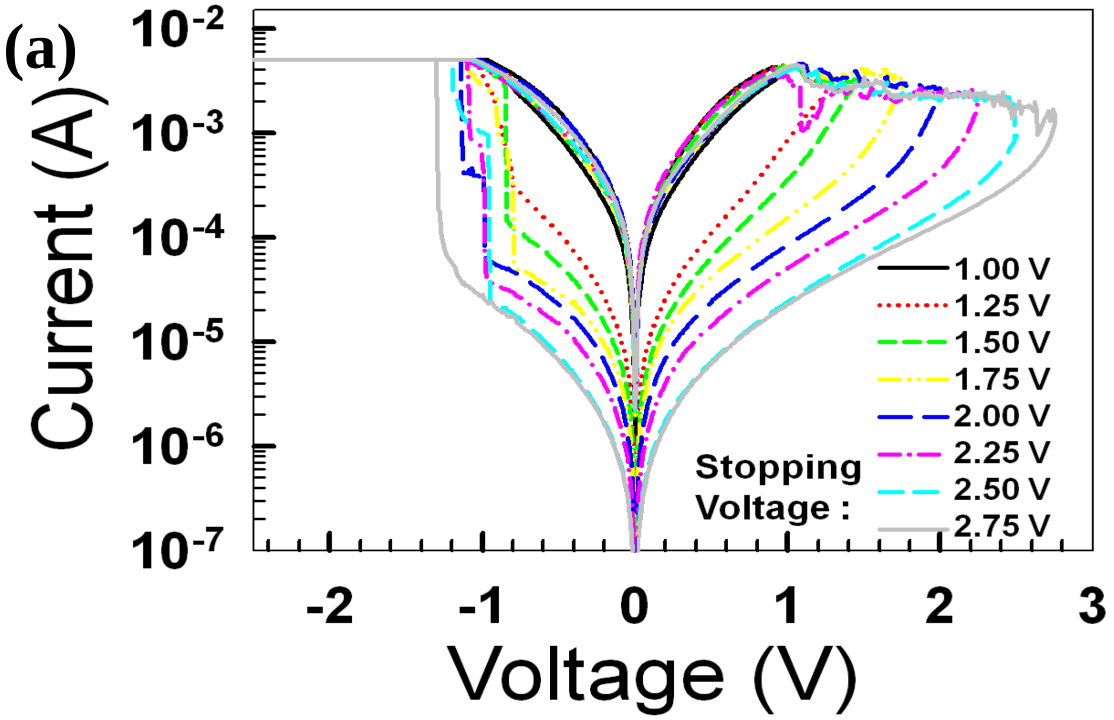


Fig. 3-37 (a) Continuous bipolar switching behaviors of the 600 ℃-60 sec treated Ti/TiN/SiO_2/FeO_x/Fe/Pt structure under a series of stopping voltage in reset region.

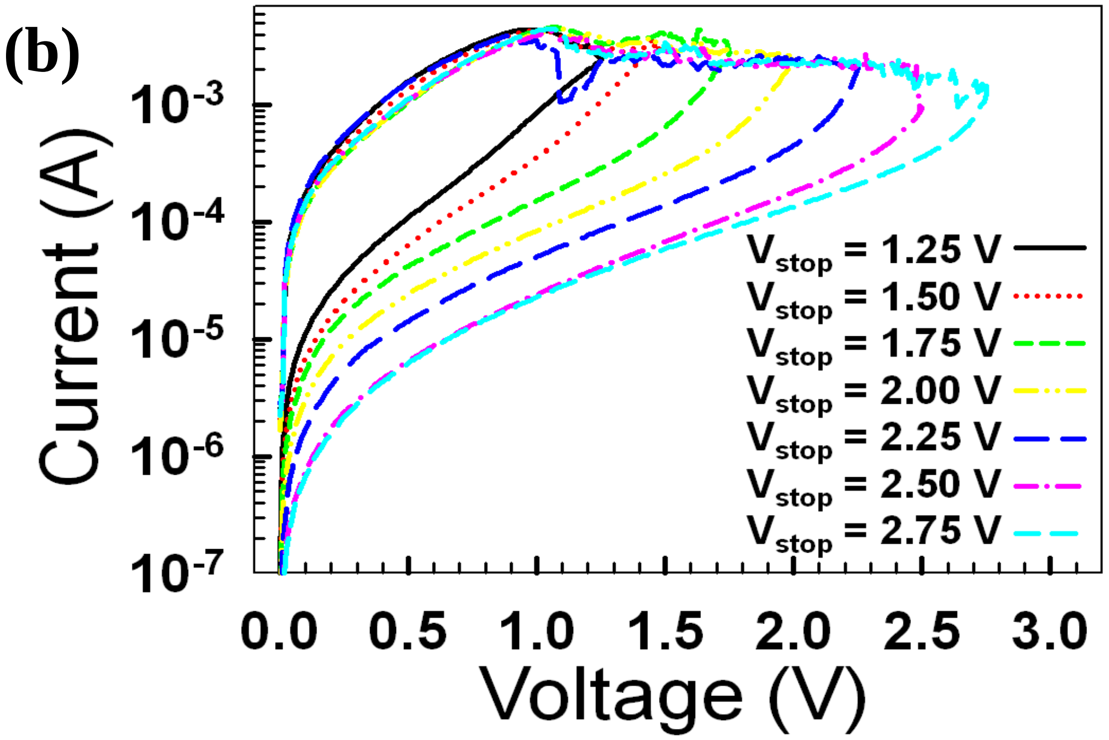


Fig. 3-37 (b) Enlarged replot of Fig. 3-29(a) for continuous reset region under a series of stopping voltage in the reset region.

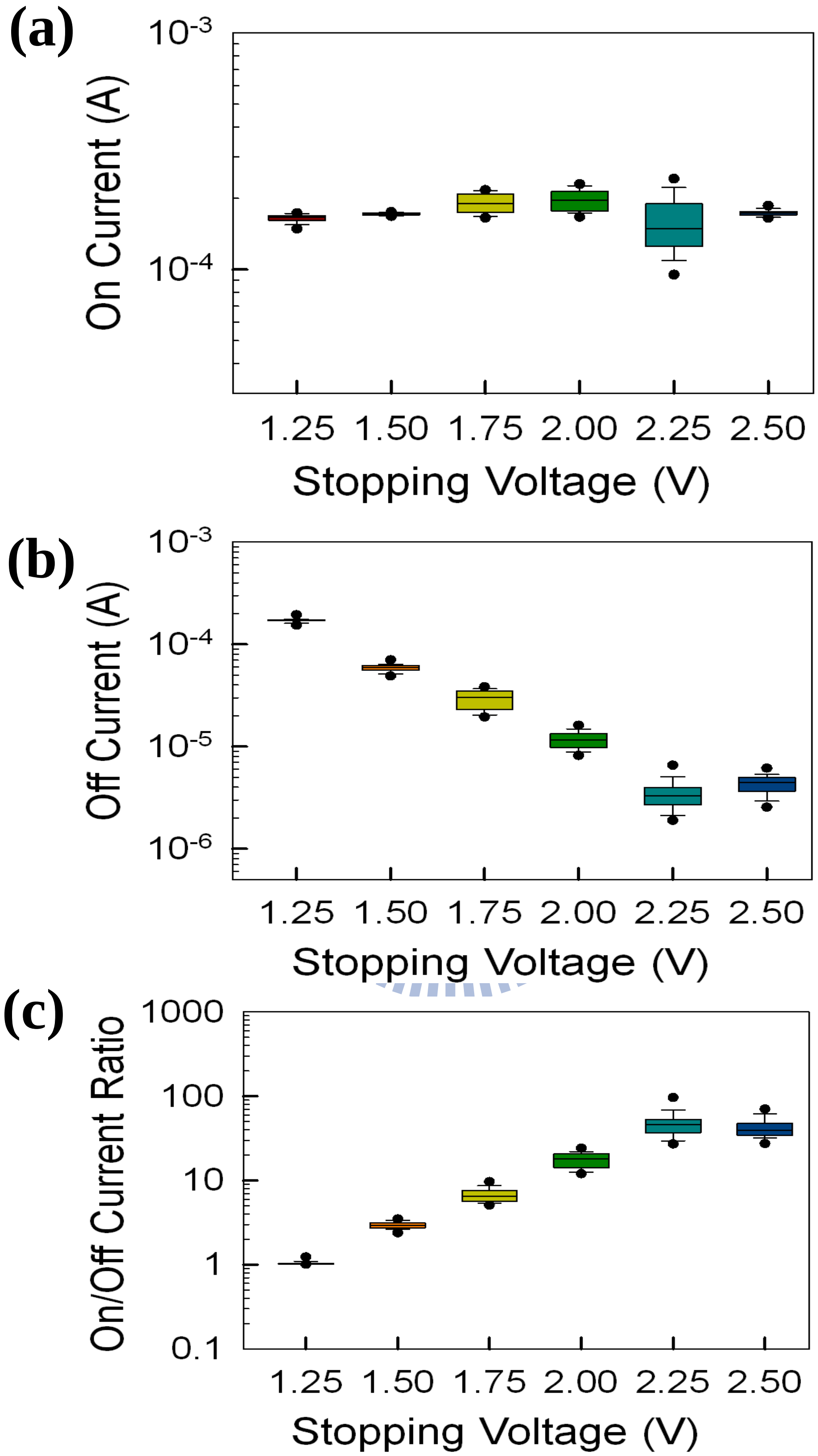


Fig. 3-38 Statistics of (a) On current, (b) Off current, and (c) On/Off current ratio for the 600 ℃-60 sec treated Ti/TiN/SiO$_2$/FeO$_x$/Fe/Pt structure with different stopping voltages in the reset region.

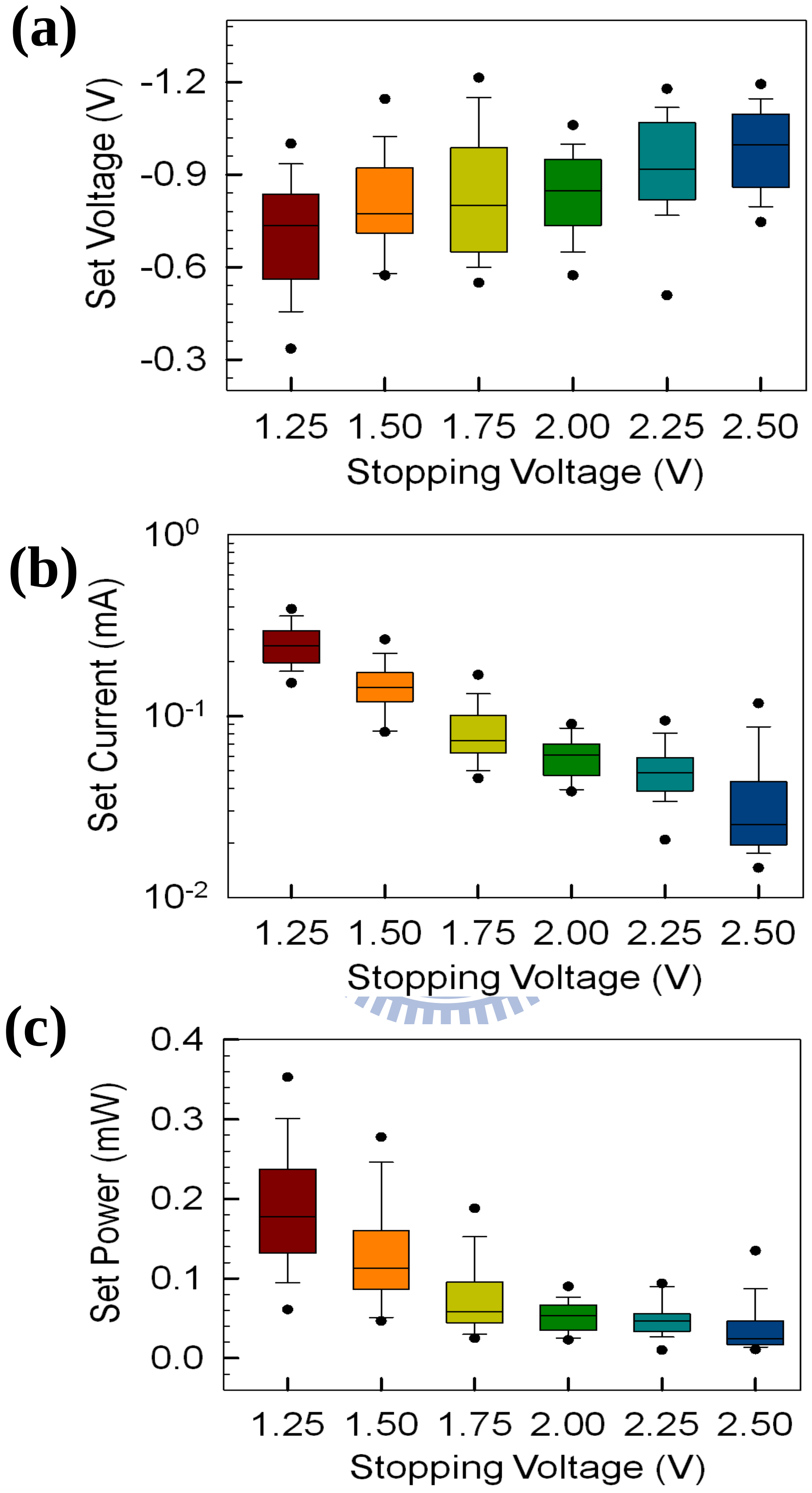


Fig. 3-39 Statistics of (a) set voltage, (b) set current and (c) set power for the 600 ℃ -60 sec treated Ti/TiN/SiO_2/FeO_x/Fe/Pt structure with different stopping voltages in the reset region.

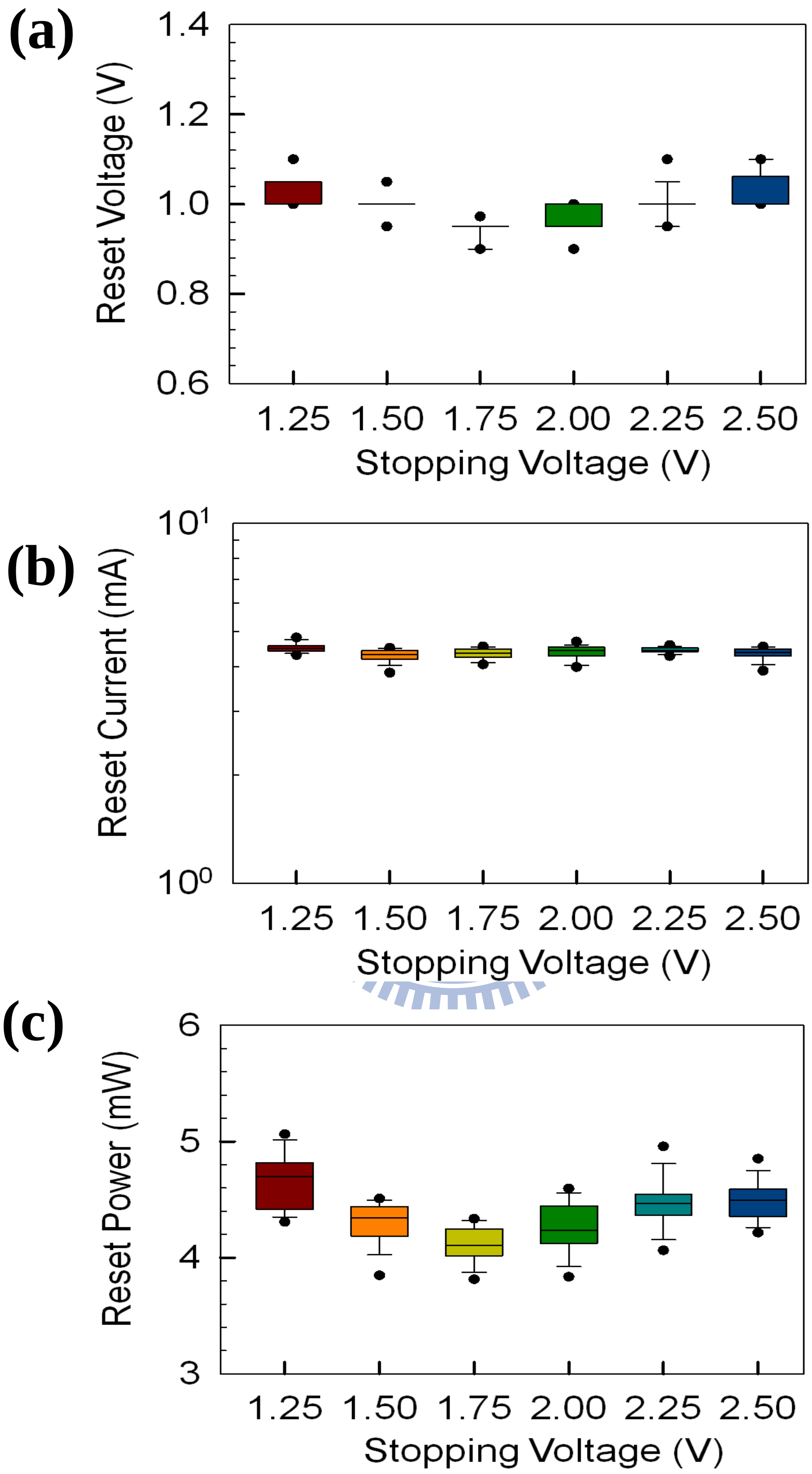


Fig. 3-40 Statistics of (a) reset voltage, (b) reset current and (c) reset power for the 600 ℃-60 sec treated Ti/TiN/SiO_2/FeO_x/Fe/Pt structure with different stopping voltages in the reset region.

Chapter 4

Conclusion

Non-charge based storage technology was researched to be the candidate for the next generation of nonvolatile memory in this dissertation. Stable and reproducible resistance switching effects were demonstrated on a relatively thin FeO_x layer in the $TiN/SiO_2/FeO_x/$ $Fe_{0.73}Pt_{0.27}$ and the $TiN/SiO_2/FeO_x/Fe/Pt$ structures produced by oxidizing the surface of a FePt electrode during a plasma-enhanced Tetraethyl Orthosilicate oxide deposition process. Characteristics of the non-stoichiometric FeO_x transition layer were examined by Auger electron spectroscopy, transmission electron microscopy, and X-ray photon emission spectra analyses. Addition of Pt into Fe electrode, i.e. the $TiN/SiO_2/FePt$ structure, was observed to improve the data dispersion of switching parameters, associating with the decrease of Fe content inside the FeO_x layer. In addition, characteristics of the forming process as well as the current transport characteristics after forming process were discussed. Moreover, current-voltage fitting data shows that current transport mechanism is governed by Ohm’ law in low voltage region and Pool-Frenkel behavior in high voltage region, consisting with FeO_x phase transition characteristics. Furthermore, the role of the silicon oxide layer was also experimentally demonstrated to act as an additional supplier of oxygen ions for the switching requirement by biasing high voltage bias conditions.

Besides, thermal treatment effects on the resistive switching characteristics were also demonstrated on the Ti/TiN/SiO_2/FeO_x/FePt and the Ti/TiN/SiO_2/FeO_x/Fe/Pt structures, including bipolar switching behaviors, retention, and statistics of set and reset power characteristics. It is found that besides the distinct reduction of memory switching parameters in forming voltage, set/reset voltages, and their dispersions, the retention characteristic measured at higher temperature is also enhanced after annealing. The effects of annealing on improving the resistance switching properties are examined by tunneling electron microscope, X-ray diffraction and X-ray photon-emission spectra depth profile results and discussed from the point of diffusion phenomena and chemical composition of the transition layer. In addition, statistics of the set and reset power consumption results were also studied for clarifying switching mechanism of the FeO_x-contained structures.

Also, multi-level resistance switching characteristics of the thin FeO_x-transition layer were studies by controlling the maximum sweeping voltage during reset process and the maximum current compliance during set process. It is obtained that the LRS is mainly influenced by the compliance current value, which is nearly independent to the HRS. On the other hand, the HRS is mainly influenced by the stopping voltage instead of the LRS.

Future work

In our future work, there are still several researches needed to be studied further, described as follows:

First part is combination of our proposed Fe-based RRAM with MOSEFT transistor for real circuit operation study.

Second part is small size fabrication of a sub-micro or a deep-sub-micro dimension.

Third part is AC measurement characteristics of our proposed Fe-based RRAM, such as pulse measurement, and switching time measurement.

The fourth part is yield statistics, such as cumulative probability and die-to-die uniformity characteristics.

The final part is optimization of performance by adjusting the thickness of the Fe-contained electrode /SiO2 as well as the deposition surroundings of PECVD-TEOS oxide, such as adjusting the plasma treatment condition, deposition pressure and the gas flow.

Prospects

Compared to present technology of RRAM, our proposed Fe-based RRAM structure is with the advantages of simpler fabrication process and higher uniformity. It is because that most of the fabrications of RRAM are by the directly deposition a resistance switching layer. However, most importantly, it is reported that the resistance switching effects are strongly related to the existence of non-stoichiometric compounds for chemical reaction mechanism. Therefore, it is very difficult to control the non-stoichiometric compounds uniformly and well. So, it could result in a larger variation wafer-to-wafer and lot-to-lot. On the other hand, in our proposed structure, the most important advantage is that the formation of the non-stoichiometric compounds is by producing a transition layer of an oxidized iron electrode surface, containing the compositions varied from Fe-rich FeO_x (close to Fe electrode) to oxygen-rich FeO_x (close to SiO_2 layer).

Another prospect is to clearly understand the mechanism of RRAM further, which is important and helpful for the future researches and studies.

References

Chapter 1

[1.1] D. Kahng and S. M. Sze, *Bell Syst. Tech, J.*, **46**, 1288 (1967).

[1.2] P. Pavan, R. Bez, P. Olivo and E. Zanoni, *Proc. IEEE*, **85**, 1248 (1997).

[1.3] "International Technology Roadmap for Semiconductors, 2007 update" at http://public.itrs.net/Files/2007Update/Home.pdf.

[1.4] I.G. Baek, D.C. Kim, M.J. Lee, H.J. Kim, E.K. Yim, M.S. Lee, J.E. Lee, S.E. Ahn, S. Seo, J.H. Lee, J.C. Park, Y.K. Cha, S.O. Park, H.S. Kim, I.K. Yoo, U.I. Chung, J.T. Moon, and B.I. Ryu, *Tech. Dig. – Int. Electron Devices Meet.*, p. 750 (2005).

[1.5] Qi Liu, Weihua Guan, Shibing Long, Rui Jia, Ming Liu, and Junning Chen, *Appl. Phys. Lett.*, **92**, p. 012117, Jan. (2008).

[1.6] S. Seo, M. J. Lee, D. H. Seo, E. J. Jeoung, D. S. Suh, Y. S. Joung, I.K. Yoo, I.R. Hwang, S.H. Kim, I.S. Byun, J.S. Kim, J.S. Chio, and B.H. Park, *Appl. Phys. Lett.*, **85**, p. 5655, Dec. (2004).

[1.7] C.B. Lee, B.S. Kang, A. Benayad, M.J. Lee, S.E. Ahn, K.H. Kim, G. Stefanovich, Y. Park, and I. K. Yoo, *Appl. Phys. Lett.*, **93**, p. 042115, (2008).

[1.8]]H.Y. Lee, P.S. Chen, T.Y. Wu, Y.S. Chen, C.C. Wang, P.J. Tzeng, C.H. Lin, F. Chen, C.H. Lien, and M.J. Tsai, IEEE IEDM Tech. Dig., p.297 (2008).

[1.9] X. Wu, P. Zhou, J. Li, L.Y. Chen, H. B. Lv, Y.Y. Lin, and T.A. Tang, *Appl. Phys. Lett.*, **90**, p. 183507, (2007).

[1.10] B.J. Choi, D.S. Jeong, S.K. Kim, C. Rohde, S. Choi, J.H. Oh, H.J. Kim, C.S. Hwang, K. Szot, R. Waser, B. Reichenberg, and S. Tiedke, *J. Appl. Phys.*, **98**, p. 033715, Aug. (2005).

[1.11] B.J. Choi, Seol Choi, K.M. Kim, Y.C. Shin, C.S. Hwang, S.Y. Hwang, S.S.

Cho, S. Park, and S.K. Hong, *Appl. Phys. Lett.*, **89**, p. 012906, Jul. (2006).

[1.12] C.Y. Lin, C.Y. Wu, C.Y. Wu, T.C. Lee, F.L. Yang, Chenming Hu, and T.Y. Tseng, *IEEE Electron Device Lett.*, **28**, pp. 366, May. (2007).

[1.13] D.C. Kim, S. Seo, S.E. Ahn, D.S. Suh, M.J. Lee, B.H. Park, I.K. Yoo, I.G. Baek, H.J. Kim, E.K. Yim, J.E. Lee, S.O. Park, H.S. Kim, U-In Chung, J.T. Moon, and B.I. Ryu, *Appl. Phys. Lett.*, **88**, p. 202102, May. (2006).

[1.14] I. Emmer, *Thin Solid Films*, **20**, p. 43, Jan. (1974).

[1.15] R. Dong, D.S. Lee, W.F. Xiang, S.J. Oh, D. J. Seong, S.H. Heo, H.J. Choi, M.J. Kwon, S.N. Seo, M.B. Pyun, M. Hasan, and Hyunsang Hwang, *Appl. Phys. Lett.*, **90**, p. 042107, Jan. (2007).

[1.16] S. Muraoka, K. Osano, Y. Kanzawa, S. Mitani, S. Fujii, K. Katayama, Y. Katoh, Z. Wei, T. Mikawa, K. Arita, Y. Kawashima, R. Azuma, K. Shimakawa, A. Odagawa, and T. Takagi, *Tech. Dig. – Int. Electron Devices Meet.*, p. 779 (2007).

[1.17] D. Lee, D.K. Hwang, M. Chang, Y. Son, D.J Seong, D. Choi, and H. Hwang, *IEEE Non-Volatile Semiconductor Memory Workshop*, p. 86 (2006).

[1.18] Christina Schindler, Sarath Chandran Puthen Thermadam, Rainer Waser, and Michael N. Kozicki, IEEE Trans. Electron Devices, **54**, pp. 2762, Oct. (2007).

[1.19] I.S. Park, K.R. Kim, S. Lee, and J. Ahn, *Jpn. J. Appl. Phys.*, **46**, No. 4B, p. 2172 (2007).

[1.20] Lee D, Seong D-j. Jo I., Xiang F, Dong R, Oh S and Hwang H., *Appl. Phys. Lett.*, **90**, p. 122104 (2007).

[1.21] H. Sim, D. Choi, D. Lee, S. Seo, M. J. Lee, I. K. Yoo, and H. Wang, IEEE Electron Device Lett. **26**, 292 (2005).

[1.22] S.Q. Liu, N.J. Wu, and A. Ignatiev, Appl. Phys. Lett. **76**, 2749 (2000).

Chapter 2

[2.1] B.J. Choi, D.S. Jeong, S.K. Kim, C. Rohde, S. Choi, J.H. Oh, H.J. Kim, C.S. Hwanga, K. Szot, R. Waser, B. Reichenberg, S. Tiedke, J. Appl. Phys. 98, 033715 (2005).

[2.2] H. Sim, D. Choi, D. Lee, S. Seo, M,J, Lee, I.K. Yoo, H. Wang, IEEE electron Device Lett. 26, 292 (2005).

[2.3] S.Q. Liu, N.J. Wu, A. Ignatiev, Appl. Phys. Lett. 76, 2749 (2000).

[2.4] S.B. Lee and S. C. Chae, S. H. Chang and C. Liu, Jour. of the Korean Appl. Phys. Society, 51, 96 (2007).

[2.5] X. Wu, P. Zhou, J. Li, L.Y. Chen, H.B. Lv, Y.Y. Lin, and T.A. Tang, Appl. Phys. Lett., 90, p. 183507, (2007).

[2.6] Christina Rohde, Byung Joon Choi, Doo Seok Jeong, Seol Choi, Jin-Shi Zhao, and Cheol Seong Hwang, Appl. Phys. Lett., 86, p. 262907, Jun. (2005).

[2.7] I.G. Baek, D.C. Kim, M.J. Lee, H.J. Kim, E.K. Yim, M.S. Lee, J.E. Lee, S.E. Ahn, S. Seo, J.H. Lee, J.C. Park, Y.K. Cha, S.O. Park, H.S. Kim, I.K. Yoo, U.I. Chung, J.T. Moon, and B.I. Ryu, Tech. Dig. – Int. Electron Devices Meet., p. 750 (2005).

[2.8] R. Dong, D.S. Lee, W.F. Xiang, S. J. Oh, D.J. Seong, S.H. Heo, H.J. Choi, M.J. Kwon, S.N. Seo, M.B. Pyun, M. Hasan, and Hyunsang Hwang, Appl. Phys. Lett., 90, 042107, Jan. (2007).

[2.9] H.Y. Lee, P.S. Chen, T.Y. Wu, Y.S. Chen, C.C. Wang, P.J. Tzeng, C.H. Lin, F. Chen, C.H. Lien, and M.J. Tsai, IEEE IEDM, 297 (2008).

[2.10] S.Q. Liu, N.J. Wu, and A. Ignatiev, Appl. Phys. Lett. 76, 2749 (2000).

[2.11] T.W. Hickmott, J.Appl. Phys. 33, 3669 (1962).

[2.12] X. Cao, X.M. Li, X.D. GAo, W.D. Yu, X.J. Liu, Y.W. Zhang, L.D. Chen, and

X.H. Cheng, J. Appl. Phys. 106, 073723, (2009).

[2.13] Y. Lin, D.Y. Lee, S.Y. Wang, C.C. Lin, and T.Y. Tseng, Surf. Coat. Technol. 203, 480 (2008).

[2.14] C. Schindler, S.C.P. Thermadam, R. Waser, and M. N. Kozicki, IEEE Trans. Electron Devices, 54, 2762, (2007).

[2.15] C.Y. Lin, C.Y. Wu, C.Y. Wu, C. Hu, and T.Y. Tseng, J. Electrochem. Soc. 154, G189 (2007).

[2.16] Akihito Sawa, 11, p. 28 (2008).

[2.17] A. Avila, R. Asomoza, Solid-State Electronics, 44, 17 (2000).

[2.18] I.G. Baek, M.S. Lee, S. Seo, M.J. Lee, D.H. Seo, D.S. Suh, J.C. Park, H.S. Kim, I.K. Yoo, U.I. Chung and J.T. Moon, Int. Electron Devices Meet. Tech. Dig., p. 587 (2004).

[2.19] C.B. Lee, B.S. Kang, M.J. Lee, S.E. Ahn, G. Stefanovich, W.X. Xianyu, K.H. Kim, J.H. Hur, H.X. Yin, Y. Park, I.K. Yoo, J.-B. Park and B.H. Park, Appl. Phys. Lett. **91**, p. 082104 (2007).

[2.20] A. Odagawa, Y. Katoh, Y. Kanzawa, Z. Wei, T. Mikawa, S. Muraoka and T. Takagi, Appl. Phys. Lett. **91**, p. 133503 (2007).

[2.21] M. Janousch, G.I. Meijer, U. Staub, B. Delley, S.F. Karg and B.P. Andreasson, Adv. Mater. **19**, p. 2232 (2007).

[2.22] N. Xu, L.F. Liu, X. Sun, X.Y. Liu, D.D Han, Y. Wang, R.Q. Han, J.F. Kang, and B. Yu, Appl. Phys. Lett, 92, 232112 (2008).

[2.23] S.E. Ahn, M.J. Lee, Y.s. Park, B.S. Kang, C.B. Lee, K.H. Kim, Sunae Seo, D.S. Suh, D.C. Kim, Jihyun Hur, Wenxu Xianyu, Genrikh Stefanovich, Huaxiang Yin, I.K. Yoo, J.H. Lee, J.B. Park, I.G. Baek, and B.H. Park, Adv. Mater. , 20, 924 (2008).

[2.24] M.J. Lee, Y. Park, B.S. Kang, S.E. Ahn, C. Lee, K. Kim, Wenxu. Xianyu, G.

Stefanovich, J.H. Lee, S.J. Chung, Y.H. Kim, C.-S. Lee, J.B. Park, I.G. Baek, and I.K. Yoo, Tech. Dig. – Int. Electron Devices Meet. p. 767 (2007).

[2.25] Masashi Kawasaki, Akihito Sawa, and Yoshnori Tokura, Int. Conf. Solid State Devices Mater., 286 (2006).

[2.26] J. E. Ralph, and J. M. Woodcock, J. Non-Cryst. Solids, 7, 236, Apr. (1972).

[2.27] I. Emmer, Thin Solid Films, 20, p. 43, Jan. (1974).

[2.28] Ugo Russo, Deepak Kamalanathan, Daniele Ielmini, Andrea L. Lacaita, and Michael N. Kozicki, IEEE electron Device, 56, 5, MAY (2009).

[2.29] R. Dong, D.S. Lee, W.F. Xiang, S. J. Oh, D.J. Seong, S.H. Heo, H.J. Choi, M.J. Kwon, S.N. Seo, M.B. Pyun, M. Hasan, and Hyunsang Hwang, Appl. Phys. Lett., 90, p. 042107, Jan. (2007).

[2.30] J. Y. Son and Y.H. Shin, Appl. Phys. Lett, 92, 222106 (2008).

[2.31] K. Fujiwara and H. Takagi, University of Tokyo (2008), unpublished data.

[2.32] Hyunjun Sim, Hyejung Choi, Dongsoo Lee, Man Chang, Dooho Choi, Yunik son, Eun-Hong Lee, Wonjoo Kim, Yoondong Park, In-Kyeong Yoo, and Hyunsang Hwang, IEDM Tech. Dig., 758 (2005).

[2.33] A. Sawa, T. Fujii, M. Kawasaki, and Y. Tokura, Appl. Phys. Lett. **85**, 4073 (2004).

[2.34] T. Fujii, M. Kawasaki, A. Sawa, H. Akoh, Y. Kawazoe, and Y. Tokura, Appl. Phys. Lett. **86**, 012107 (2005).

[2.35] J. J. Yang, F. Miao, M. D. Pickett, D. A. A. Ohlberg, D. R. Stewart, C. N. Lau, and R. S. Williams, Nanotechnology 20, 215201 (2009).

Chapter 3

[3.1] I.G. Baek, M.S. Lee, S. Seo, M.J. Lee, D.H. Seo, D.S. Suh, J.C. Park, S.O. Park, H.S. Kim, I.K. Yoo, U.I. Chung, and J.T. Moon, Tech. Dig. IEDM, 587 (2004).

[3.2] Kozicki M N, Park M and Mitkova M, IEEE Trans. Nanotechnol. **4**, 331 (2005).

[3.3] Terabe K, Hasegawa T, Nakayama T and Aono M, Nature, **433**, 47 (2005).

[3.4] Y. Watanabe, J. G. Bednorz, A. Bietsch, C. Gerber, D. Widmer, A. Beck, and S. J. Wind, Appl. Phys. Lett. **78**, 3738 (2001).

[3.5] S.B. Lee and S. C. Chae, S. H. Chang and C. Liu, Jour. of the Korean Appl. Phys. Society, **51**, 96 (2007).

[3.6] D.S. Lee, H.J. Choi, H.J. Sim, D.H. Choi, H.S. Hwang, M.J. Lee, S.A. Seo and I.K. Yoo, IEEE Electron Device Lett. **26**, 719 (2005).

[3.7] K.M. Kim, B.J. Choi, D.S. Jeong, and C.S. Hwang, Appl. Phys. Lett. 89, 162912 (2006)

[3.8] S. Seo, M.J. Lee, D. H. Seo, E.J. Jeoung, D.S. Suh, Y.S. Joung, and I.K. Yoo, I.R. Hwang, S.H. Kim, I.S. Byun, J.S. Kim, J.S. Choi, and B.H. Park, Appl. Phys. Lett. **85**, 5655 (2004).

[3.9] C.Y. Lin, C.Y. Wu, C.Y. Wu, C. Hu, and T.Y. Tseng, J. Electrochem. Soc. 154, G189 (2007).

[3.10] R. Dong, D.S. Lee, W.F. Xiang, S.J. Oh, D.J. Seong, S.H. Heo, H.J. Choi, M. J. Kwon, S. N. Seo, M.B. Pyun, M. Hasan, and Hyunsang Hwang, Appl. Phys. Lett. **90**, 042107 (2007).

[3.11] H.Y. Lee, P.S. Chen, T.Y. Wu, Y.S. Chen, C.C. Wang, P.J. Tzeng, C.H. Lin, F. Chen, C.H. Lien, and M.J. Tsai, IEEE IEDM, 297 (2008).

[3.12] I.H. Inoue, S.Yasuda, H. Akinaga, and Takagi, Phys. Review B, **77**, 035105 (2008).

[3.13] S. Muraoka, K. Osano, Y. Kanzawa, S. Mitani, S. Fujii, K.Katayama, Y. Katoh, Z. Wei, T. Mikawa, K. Arita, Y. Kawashima, R. Azuma, K. Kawai, K. Shimakawa, A. Odagawa, and T. Takagi, IEEE IEDM, 227 (2007).

[3.14] X. Wu, P. Zhou, J. Li and L. Y. Chen, H. B. Lv, Y. Y. Lin, and T. A. Tang, Appl. Phys. Lett. **90**, 183507 (2007).

[3.15] D.S. Lee, D.J. Seong, H.J. Choi, I. Jo, R. Dong, W. Xiang, S. Oh, M. Pyun, S.O. Seo, Seongho Heo, Minseok Jo, D.K. Hwang, H. K. Park, M. Chang, M. Hasan, and H. Hwang, Tech. Dig. - Int. Electron Devices Meet. 2006, 346733.

[3.16] L. Y. Zhao, K. R. Eldridge, K. Sukhija, H. Jalili, N. F. Heinig, and K. T. Leung, Appl. Phys. Lett. **88**, 033111 (2006).

[3.17] M. Ieda, G. Sawa, and S. Kato, J. Appl. Phys. **42**, 3737 (1971).

[3.18] H. Yanagihara, M. Hasegawa, E. Kita, Y. Wakabayashi, H. Sawa, and K. Siratori, J. Phys. Soc. Jpn. 75, 054708 (2006).

[3.19] S. Kumari, C. Tripathi, A. P. Singh, D. Chauhan, R. Shrivastav, S. Dass, and V. R. Satsangi, Curr. Sci. 91, 1062 (2006).

[3.20] C. B. Lee, B. S. Kang, M. J. Lee, S. E. Ahn, G. Stefanovich, W. X. Xianyu, K. H. Kim, J. H. Hur, H. X. Yin, Y. Park, and I. K. Yoo, J.-B. Park, B. H. Park, Appl. Phys. Lett. **91**, 082104 (2007).

[3.21] D.C. Kim, S. Seo, S.E. Ahn, D.-S. Suh, M.J. Lee, B.-H. Park, I.K. Yoo, I.G. Baek, H.-J. Kim, E.K. Yim, J.E. Lee, S.O. Park, H.S. Kim, U-In Chung, J.T. Moon, and B.I. Ryu, Appl. Phys. Lett. **88**, 202102 (2006).

[3.22] J. J. Yang, F. Miao, M. D. Pickett, D. A. A. Ohlberg, D. R. Stewart, C. N. Lau, and R. S. Williams, Nanotechnology 20, 215201 (2009).

[3.23] B.J. Choi, D.S. Jeong, S.K. Kim, C. Rohde, S. Choi, J.H. Oh, H.J. Kim, C.S. Hwanga, K. Szot, R. Waser, B. Reichenberg, S. Tiedke, J. Appl. Phys. **98,** 033715 (2005).

[3.24] H. Sim, D. Choi, D. Lee, S. Seo, M,J, Lee, I.K. Yoo, H. Wang, IEEE electron Device Lett. **26**, (2005), 292.

[3.25] S.Q. Liu, N.J. Wu, A. Ignatiev, Appl. Phys. Lett. **76**, 2749 (2000).

[3.26] D.S. Lee, H.J. Choi, H.J. Sim, D.H. Choi, H.S. Hwang, M.J. Lee, S.A. Seo, and I.K. Yoo, IEEE Electron Device Lett. **26**, 900 (2005).

[3.27] C.Y. Lin, C.Y. Wu, C.Y. Wu, Chenming Hu, and T.Y. Tseng, Journal of The Electrochemical Society, **154** G189-G192 (2007).

[3.28] L.W. Feng, C.Y. Chang, Y.F. Chang, W.R. Chen, S.Y. Wang, P.W. Chiang, and T.C. Chang, Appl. Phys. Lett. **96**, 052111 (2010).

[3.29] Ikeda, Y., Takana. M., Bando. Y., Bull. Inst. Chem. Res., Kyoto Univ., **64**, 249 (1986).

[3.30] S. Muraoka, K. Osano, Y. Kanzawa, S. Mitani, S. Fujii, K.Katayama, Y. Katoh, Z. Wei, T. Mikawa, K. Arita, Y. Kawashima, R. Azuma, K. Kawai, K. Shimakawa, A. Odagawa, and T. Takagi, Tech. Dig. - Int. Electron Devices Meet. (2007), 227.

Appendix

Introduction to Nanocrystals Nonvolatile Memories

Nanocrystals (NCs) nonvolatile memory device is still based on the charge storage technology, containing distributed charge storage centers so that stored charges can be suppress their lateral migration. Therefore, even if an intrinsic defect or extrinsic defect chain exists in the tunnel oxide, they can only influence a few trapping centers allowing aggressive scaling of tunnel oxide. In recent years, NCs nonvolatile memory devices have also received attention due to their higher energy state density, stronger coupling with the device channel, a wide range of available work functions, and strong charge confinement. Therefore, it can be applied for ultralow-power and high-density memories with long retention time, due to strong quantum confinement of charges in the NCs.

NC nonvolatile memories, first introduced in the early 1990s, are one particular implementation of that concept. As compared to conventional stacked gate NVM devices, the main advantage contributed from the NC charge storage structure is the potential to use a thinner tunnel oxide without sacrificing nonvolatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds. This claim of improved scalability results not only from the distributed nature of the charge storage, which makes the storage more robust and fault-tolerant, but also from the beneficial effects of Coulomb blockade. Quantum confinement effects (bandgap widening; energy quantization) can be exploited in sufficiently small NC geometries (sub-3 nm dot diameter) to further enhance the memory’s performance.

Besides, there are other important advantages from NC NVM devices. First, NC memories use a more simplified fabrication process as compared to conventional stacked-gate FG NVM’s by avoiding the fabrication complications and costs of a dual-poly process. Further, due to the absence of drain to FG coupling, NC memories suffer less from drain induced barrier lowering (DIBL) and therefore have intrinsically better punchthrough characteristics. One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time. Alternatively, it allows the use of shorter channel lengths and therefore smaller cell area (i.e., lower cost). Finally, NC memories are characterized by excellent immunity to stress induced leakage current (SILC) and oxide defects due to the distributed nature of the charge storage in the NC layer.

In aspects of practical fabrication, four important parameters should also be taken care: (1) Tunnel oxide thickness. The oxide thickness must be well controlled and uniformity must be good enough to prevent the threshold voltage variation from cell to cell. (2) The quality of blocking oxide. The quality of the oxide must ensure that the carrier cannot tunnel from gate electrode to NC layer. (3) The density of NC and (4) the size of NC. Larger NC size provides high program/erase efficiency because the larger size of NC suffers from smaller quantum confinement and coulomb blockade effects. However, it is desirable to reduce the NC size to achieve a high density of NC on the channel for a uniform devices array. Therefore, there is a trade-off in the NC size. A typical target of density is 10^{12} cm^{-2}, which requires NC size of about 5-nm.

Memory characteristics of Titanium-based nanocrystals nonvolatile memories

A.1 Formation and composition of titanium oxinitride nanocrystals synthesized via nitridizing titanium oxide

A.1.1 Introduction

In the past few years, portable electronic devices have significantly impacted the markets of consumer electronics. Because of the low working voltage and non-volatility, the flash memory based on the floating-gate structure is widely employed [A.1]. However, the most prominent one for floating-gate structure in recent industry is the limited potential for continued scaling of the device structure. Therefore, in recent years, NCs nonvolatile memory (NVM) devices with discrete charge trapping centers have been extensively studied and discussed on different materials, such as metal NCs, semiconductor NCs [A.2-A.4] and even high-κ dielectric NCs [A.5-A.7], due to their grand potency for achieving high program/erase speed, low programming voltage, low-power performance and excellent retention and disturb characteristics [A.8-A.10]. Among these materials, titanium nitride (TiN) [A.11-A.12] and titanium oxide (TiO_2) [A.13] NCs have received increasing attentions for NVMs applications due to their advantages of high electrical conductivity(TiN)/high dielectric constant(TiO_2), larger memory window, easy fabrication, low cost, good heat stability, and especially excellent compatibility with CMOS process. Therefore, in this study, titanium oxinitride (TiN_xO_y) NCs were also investigated for application aspects of NVMs because TiN_xO_y is a kind of materials with a wide range ranking from a conductor (TiN) to an insulator (TiO_2) by a tunable N/O ratio. On the other hand, there are many preparation methods for a TiN_xO_y film in past reports, such as a reactive sputtering of Ti in an oxygen/nitrogen atmosphere, oxidative annealing of TiN [A.14], and metalorganic chemical vapor deposition [A.15-A.16]. In this study, another simple technique to synthesize TiN_xO_y in NCs structures was also proposed via treating a magnetron co-sputtered thin film of titanium (Ti) and silicon dioxide (SiO_2) with a rapid thermal annealing in nitrogen (N_2) ambient.

A.1.2 Experiment

Illustration of the proposed process flows and device structures is shown in figure A-1. After the standard Radio Corporation of America (RCA) clean process (SC1: NH_4OH (ammonium hydroxide) + H_2O_2 (hydrogen peroxide) + H_2O, SC2: HCl + H_2O_2 + H_2O, and HF dip) of a p-type silicon (100) wafer [A.17], a ~6-nm-thick tunnel oxide examined by the TEM observation was thermally grown by a dry oxidation process at 875 °C. Then, a ~15-nm-thick Ti-based charge trapping layer was deposited by RF and DC magnetron co-sputtering with SiO_2 and Ti targets, respectively. The sputtering chamber was initially evacuated to a base pressure of 2.1×10^{-4} Pa and the working pressure was maintained at 0.61 Pa in argon ambient at room temperature. The RF power of the SiO_2 target was fixed at 100 W while the DC power of the Ti target was fixed at 50 W. Then, annealing treatments with different temperature conditions up to 900 °C were performed for 1 min in N_2 (6N purity) ambient at a pressure of 3×10^{3} Pa. It is noted that a base-pressured evacuation about 5×10^{-4} Pa was also performed before the annealing process and the surroundings during raising and cooling the annealing temperature is filled with N_2 ambient. Subsequently, a blocking oxide in thickness of 40 nm was deposited by the plasma enhanced chemical vapor deposition system at 300 °C. Finally, a 500-nm-thick aluminum (Al) gate electrode was deposited by thermal evaporation and patterned by shadow mask with a pad radius of 0.4 mm to form a capacitor structure for electrical measurement. The schematic diagram of device structure is shown in the inset of figure 1(a). TEM and XPS were adopted for the microstructure analysis, and chemical material analysis of NCs, respectively. Note that the XPS analyses were carried out using a Microlab 350 with a monochromatized Al Kα X-rays source (1486.6 eV; 300 W) and the XPS data were adopted from the annealed samples before capping the blocking oxide. The TEM samples was prepared by force ion beam milling and analyzed by a Philips Tecnai-20 System. In addition, electrical characteristics, including the capacitance-voltage (C-V) hystereses, and retention characteristics were performed by a HP4284 Precision LCR Meter with high frequency of 1 MHz.

A.1.3 Results and Discussion

To observe the phase separation after the different annealing conditions, TEM images analyses were performed. figure A-2 shows the cross-sectional TEM images of the Ti/SiO_2 co-sputtered samples with the different annealing temperatures of (a) 500 ℃, (b) 700 ℃, and (c) 900 ℃ in N_2 ambient for 1 min. In figure A-2 (a), a continuous trapping layer structure was still observed after an annealing treatment of 500 ℃. However, when the annealing temperature was increased to 700 ℃, the trapping layer was observed to segregate partially and incompletely as shown in figure A-2 (b). Furthermore, after the 900 ℃-annealing treatment, observation of clear NCs dots structure was confirmed obviously as well as the NCs density of $\sim 6.2\times 10^{10}$ cm^{-2} was estimated roughly by figure A-2 (c). Besides, the surroundings of the NCs were most possibly consisted of SiO_2 according to the brighter contrast to NCs, which is also correspondent with the XPS results. Note that the expansion of the NCs size with a ~20 nm in diameter was also observed, which could be caused from the severely thermal diffusion of the trapping layer within such a high annealing temperature.

Figure A-3 shows comparisons of XPS for O-1s, N-1s, and Ti-2p on the Ti/SiO_2 co-sputtered samples with the different annealing temperatures of 500 ℃, 700 ℃, and 900 ℃ in N_2 ambient. Energy calibration, necessary because of charging effects was performed using the adventitious carbon C 1s peak at 284.7 eV. In O-1s spectrum, the main peak signal for Ti-O binding at 530 eV was observed in the 500 ℃-annealed sample [A.18]. Ti atom is easily oxidized since TiO_2 is a thermodynamically stable phase, and hence, the trace O_2 existing in co-sputtering process or the absorbed O_2 on the wafer surface during wafer transportation (air exposure) is enough to cause the formation of Ti-O bonding during the rapid annealing process [A.19, A.20]. As the annealing temperature was increased to 700 ℃, the peak signal at 532.6 eV, referred to Si-O binding, enhances obviously while the intensity of the Ti-O peak decreases relatively [A.21]. Furthermore, after the 900 ℃-annealing treatment, the Si-O peak begins to dominate instead of the Ti-O bond. The increase of Si-O bonds and the decrease of Ti-O bonds with increasing the annealing temperature are associated with the formation of silicon dioxide around the NCs, inferred from the TEM results, and the partial replacement of Ti-O bonds by Ti-N bonds as well. In N-1s spectrum, observations of peak signals around 400 eV and 402 eV in the samples with the 500

℃ and 700 ℃ annealing temperatures were related to molecularly chemisorbed γ-N_2, which is caused from a small amount of N_2 molecules incorporated into the TiO_2 lattice [A.22]. As the annealing temperature was increased to 900 ℃, a peak signal at 397 eV is observed obviously, which is contributed from the formation of atomic β-N [A.22]. Moreover, occurrence of a positive shift of +1 V in binding energy compared to normal Ti-N bond (396 eV) confirms the formation of titanium oxinitride bindings due to the existence of higher electronegative oxygen atoms. According to the reference of 21, it is noted that TiN dissolution and TiO_x formation is thermodynamically favoured; however, observation of the reverse of this process is presumably driven by the excess of N2 on the co-sputtered thin film in our experiment. In Ti-2p spectrum, two detectable principal peaks closed to 464 and 458 eV in the samples with the 500 ℃ and 700 ℃ annealing temperatures are referred to Ti^{4+}-$2p_{1/2}$ and Ti^{4+}-$2p_{3/2}$, which are contributed from titanium dioxide bonds [A.23]. Detection of these bonds is also correspondent with the results of O-1s spectrum due to the existence of the thermodynamically stable phase of TiO_2. However, a significant broadening of the Ti-2p lines on the lower binding energy side occurs in the sample with the 900 ℃ annealing temperature due to the formations of Ti^{3+} and Ti^{2+} bindings [A.24] as well as the Ti-Si binding at 459 eV [A.25]. The observation of Ti^{3+} and Ti^{2+} peaks also confirms the occurrence of nitridizing TiO_2.

Figure A-4 shows C-V characteristics of different gate voltage sweeping regions on the Ti/SiO_2 co-sputtered samples with the annealing treatments of (a) 500 ℃, (b) 700 ℃, and (c) 900 ℃. As shown in figure A-4 (a), no threshold voltage shifts occurs while the sample was treated at 500 ℃. Moreover, the C-V curve shifts along the negative voltage axis, which is associated with the existence of positive fixed charge in the TiO_2 layer. Therefore, this infers that a blanket TiO_2 layer exhibits no programmable/erasable charge trapping centers for NVM applications. As the annealing temperature was increased to 700 ℃ [figure A-4 (b)], small threshold voltage shifts begin to exhibit due to the occurrence of partial and incomplete segregation in the trapping layer. Furthermore, after the 900 ℃-annealing condition [figure A-4 (c)], outstanding threshold voltage shifts of ~2 V, ~5 V, and ~8 V are exhibited to increase with increasing the gate voltage sweeping regions of 3 / -3 V, 5 / -5 V, and 7 / -7 V, respectively. Especially, a threshold voltage shift of 1 V is easily achieved under a small sweeping voltage range of 2 V / -2 V. Explicit observation of the threshold voltage shift is mainly contributed to the formation of well-separated NCs structures instead of the continuous trapping layer structure, which could result the stored carrier charge in a lateral leak. This indicates that the TiN_xO_y NCs provide excellent characteristics to act as charge storage centers for NVMs applications, especially exhibiting a potential for low power operation device applications. In addition, observation of the counterclockwise hysteresis loops of the C-V curves indicates the phenomenon of substrate injection of carriers through the tunneling oxide, which is preferable to gate injection through the blocking oxide.

Figure A-5 shows charge loss characteristic of the TiNxOy NCs capacitor with the annealing treatment of 900 ℃. After a initially-programmed/erased bias condition of +5 V/ -5 V for 1 sec, the threshold voltage shift still remains about 2.2 V after 10^7 sec by extrapolation, indicating excellent charge storage characteristic of TiN_xO_y NCs for NVM applications.

A.1.4 Conclusion

In this study, material analyses and the formation of TiN_xO_y NCs fabricated by co-sputtering titanium and silicon dioxide targets with different annealing conditions in N_2 ambient were investigated. A 900 ℃-annealing treatment induced the well-separated NCs structure and nitridation of the titanium oxide to format the TiN_xO_y NCs, which provides high electrical performance for NVM applications. A significant C-V hysteresis of threshold voltage shift in 1 V is observed under the low operating voltage of +2 V / -2 V voltage sweeping. The retention characteristics were also tested to be robust.

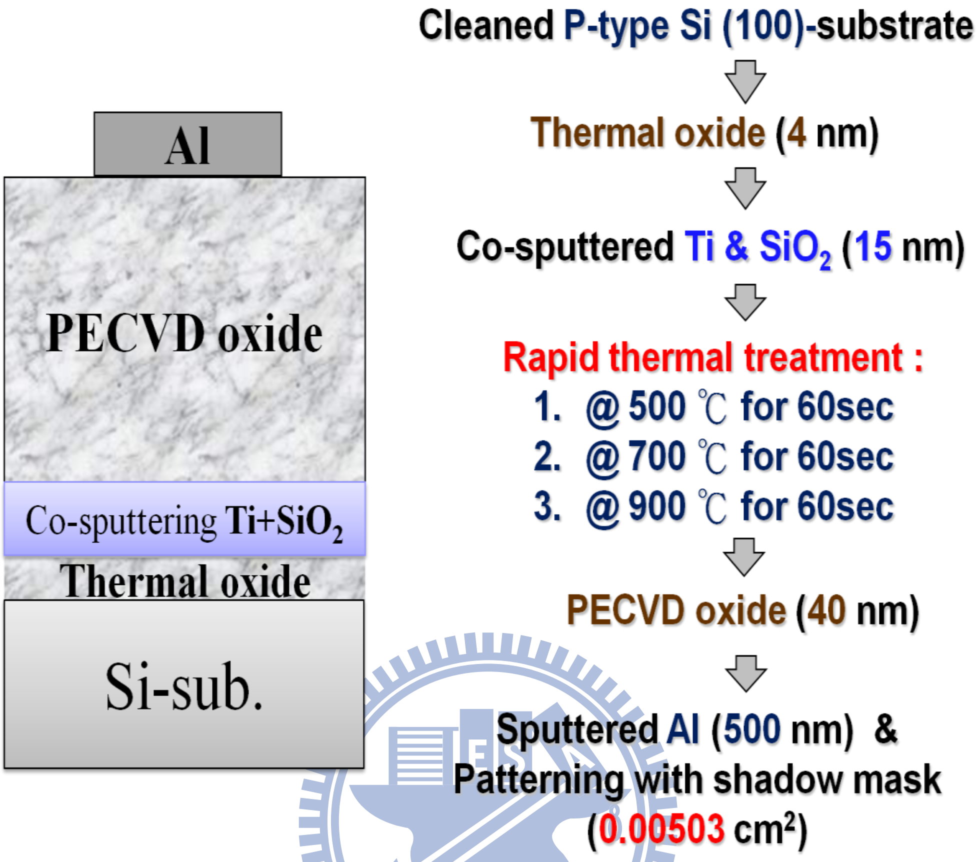


Fig. A-1 Illustration of the proposed titanium oxinitride nanocrystals device structure and process flows.

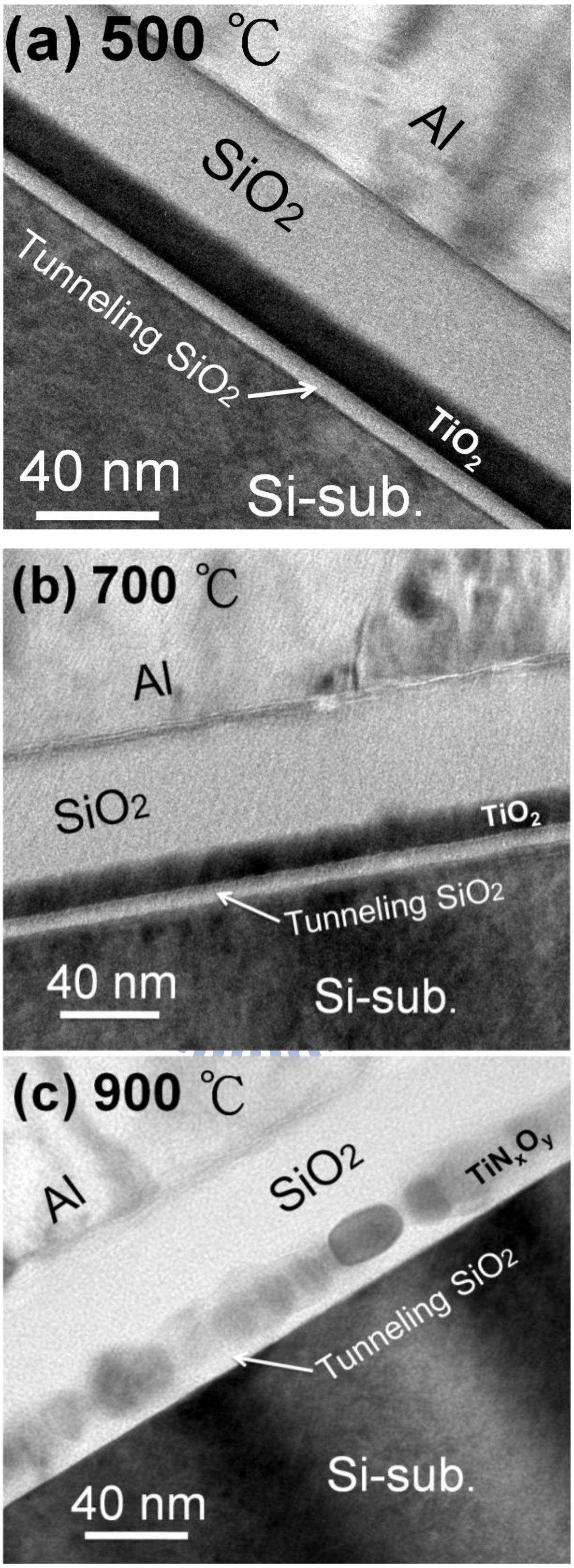


Fig. A-2 Cross-sectional TEM of the Ti-SiO_2 co-sputtered samples with rapid annealing treatments of (a) 500 ℃, (b) 700 ℃, and (c) 900 ℃ in N_2 ambient for 1 min.

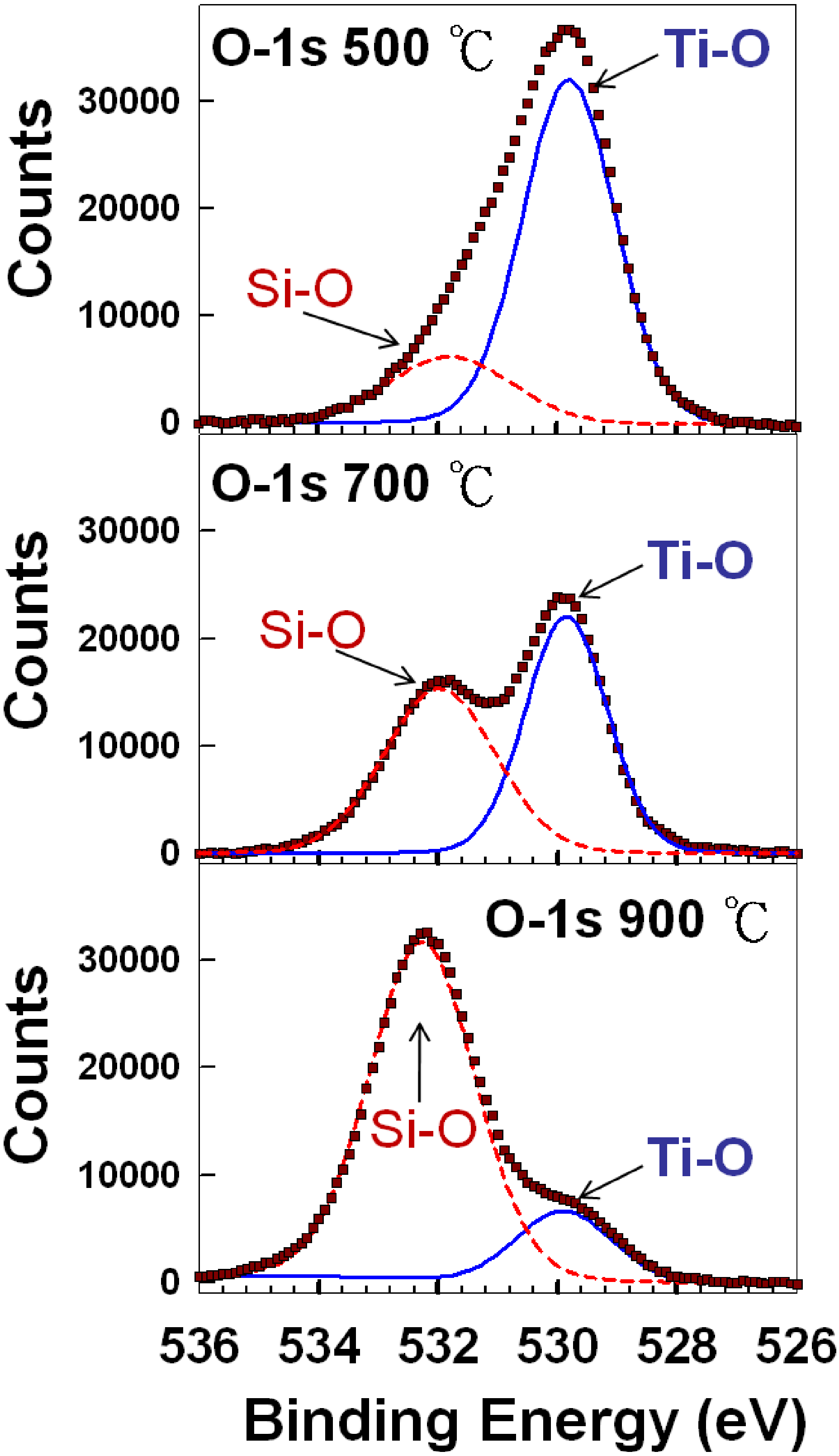


Fig. A-3(a) XPS spectra of O-1s on the Ti-SiO_2 co-sputtered samples with different annealing treatments of 500 ℃, 700 ℃, and 900 ℃ in N_2 ambient.

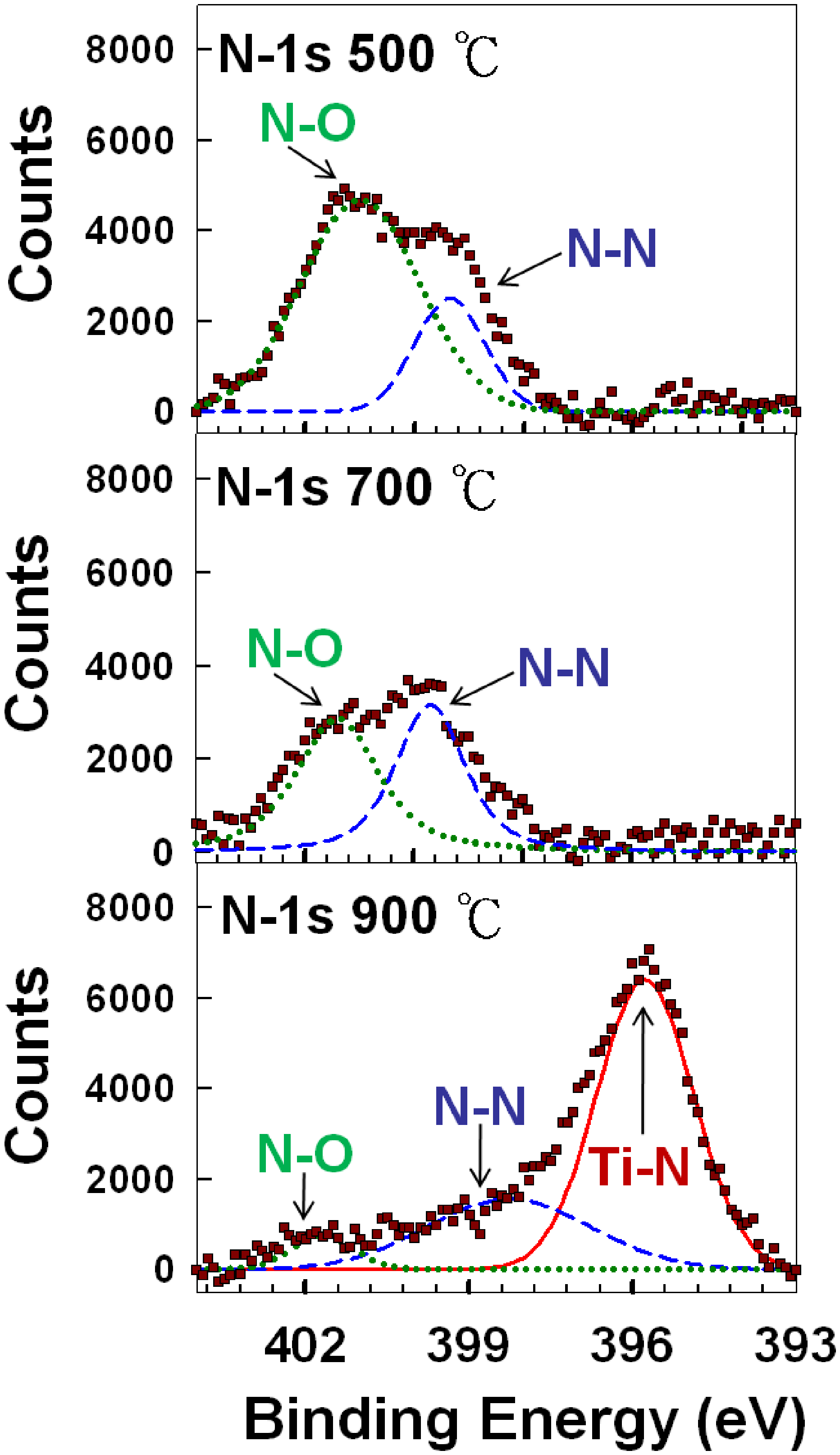


Fig. A-3(b) XPS spectra of N-1s on the Ti-SiO_2 co-sputtered samples with different annealing treatments of 500 ℃, 700 ℃, and 900 ℃ in N_2 ambient.

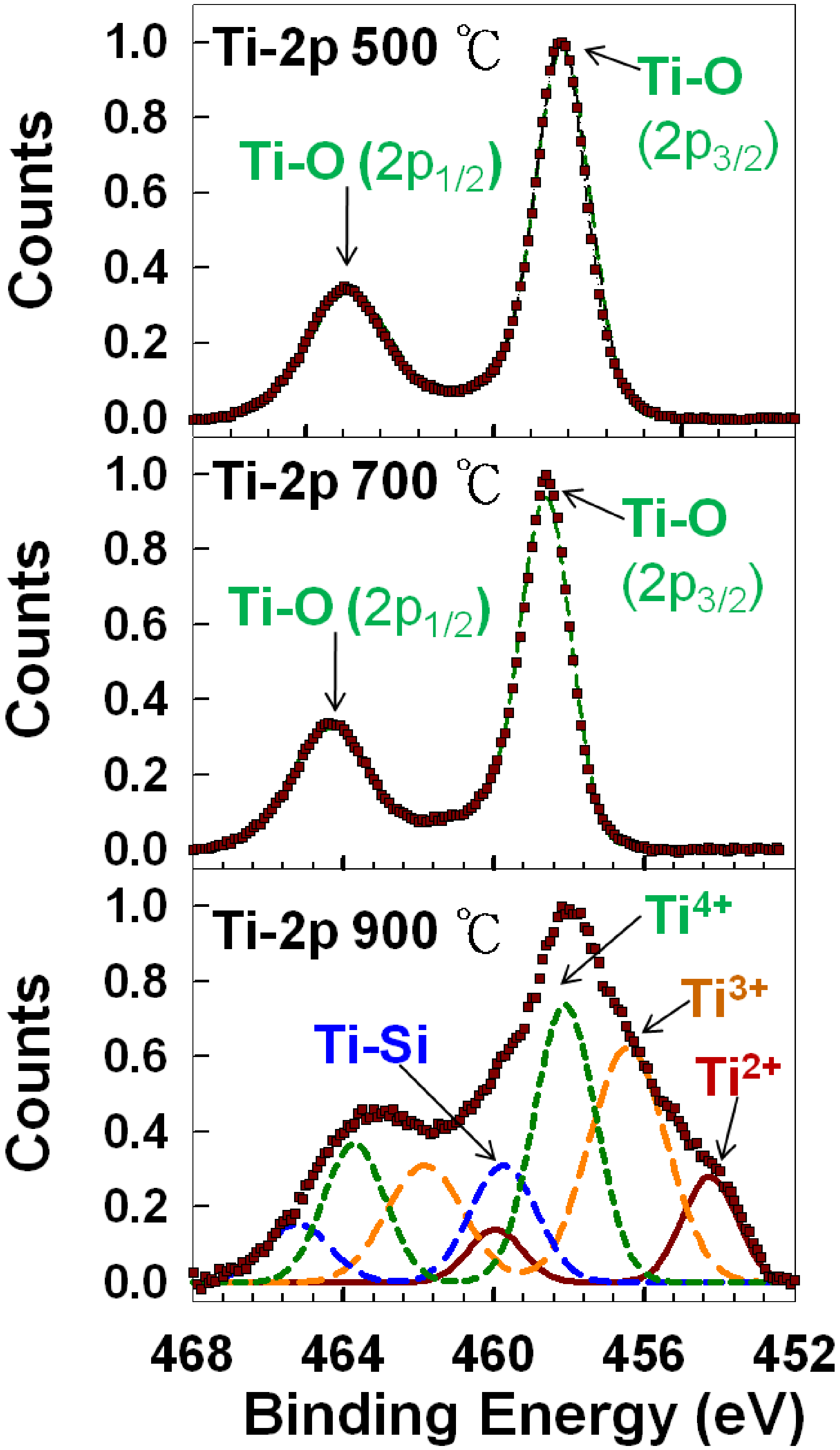


Fig. A-3(c) XPS spectra of Ti-2p on the Ti-SiO_2 co-sputtered samples with different annealing treatments of 500 ℃, 700 ℃, and 900 ℃ in N_2 ambient.

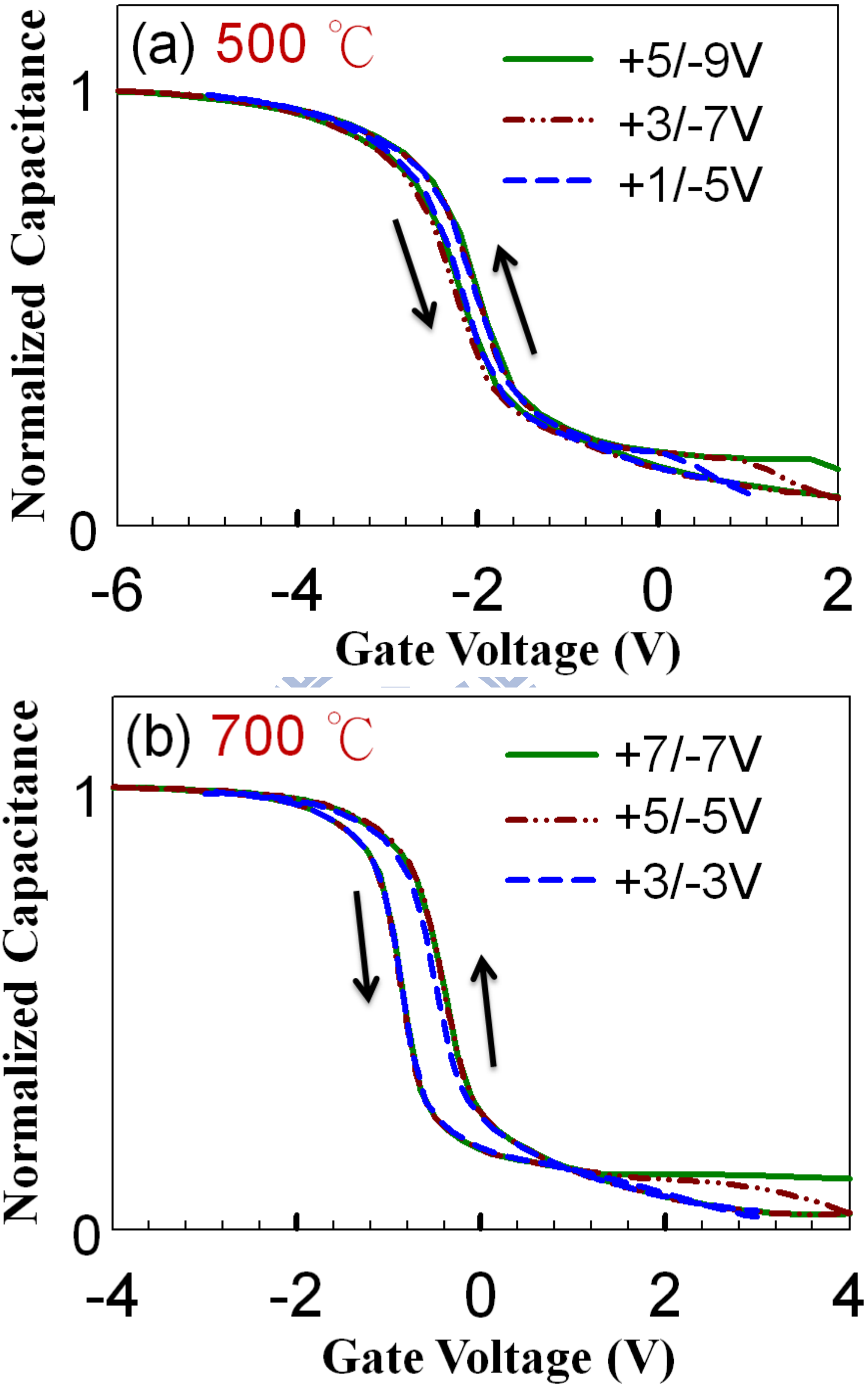


Fig. A-4(a) & (b) *C*-*V* characteristics of different gate voltage sweeping regions on the Ti-SiO_2 co-sputtered samples with rapid annealing treatments of (a) 500 ℃ and (b) 700 ℃, and in N_2 ambient.

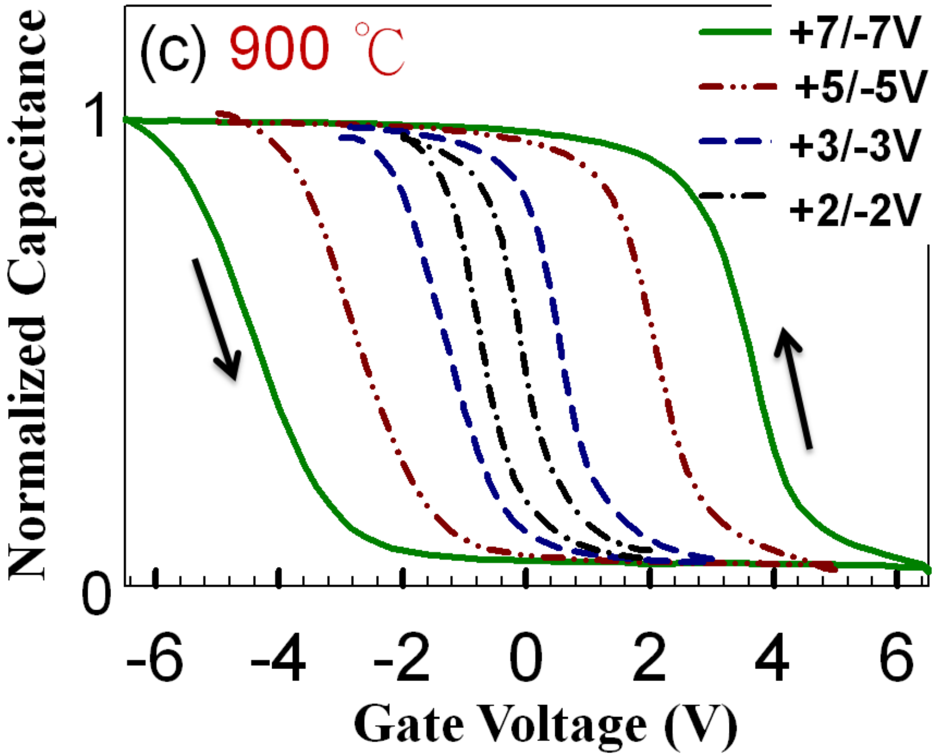


Fig. A-4(c) *C-V* characteristics of different gate voltage sweeping regions on the Ti-SiO$_2$ co-sputtered sample with rapid annealing treatment of 900 ℃ in N$_2$ ambient.

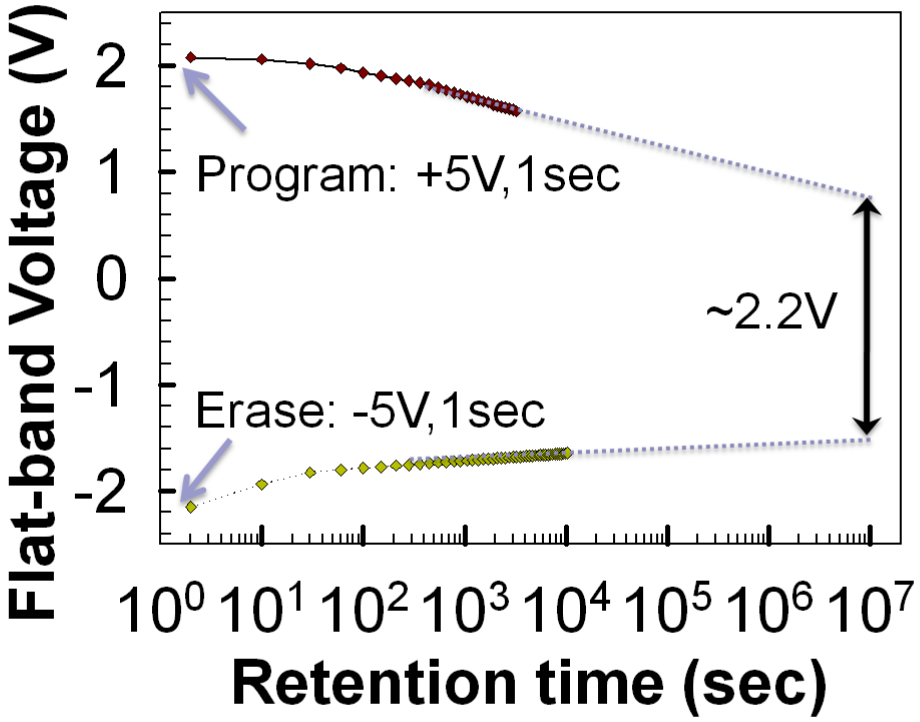


Fig. A-5 Charge loss characteristic of the TiN$_x$O$_y$ NCs capacitor with an annealing treatment of 900 ℃ in N$_2$ ambient.

A.2 Low-temperature-synthesized Memory characteristics of Titanium-based nanocrystals nonvolatile memories by Germanium doping

A.2.1 Introduction

Compared to comentional floating-gate nonvolatile memory (NVM) devices, NVMs with metal nanocrystals (NCs) as the floating storage node have received much attention due to their higher energy state density, stronger coupling with the device channel, wider range of available work functions, and stronger charge confinement [B.1-A.3] It can be applied for ultralow-power and high-density memories with long retention time, due to strong quantum confinement of charges in the NCs. Among them, titanium (Ti)-based NCs, such as titanium nitride (TiN) and titanium oxide (TiO_2) [B.4-B.7], were one of the excellent materials for NVM applications due to advantages of easy-fabricated property, low cost, good heat stability, and excellent compatibility with complementary metal-oxide-semiconductor process. However, a requirement of the fabrication temperature to exhibit NVM characteristics in all reports was higher than 900℃ at least. Such a high temperature process does not suit for low temperature process applications, for example, fabrications on a glass substrate, and so on. On the other hand, according to the investigations, presence of germanium (Ge) in Ti silicide film affects obviously not only the phase formation temperature but also its morphological stability. It means that a low-resistance Ti germanosilicide phase can be formed at a lower temperature than Ti silicide [B.8]. In addition, a poor morphological stability could be obtained due to the lowering of agglomeration temperature of Ti silicide with Ge composition [B.9-B.11]. So, incorporation of Ge into titanium silicide seems to provide a desirable trend to format Ti-based NCs at a relatively low temperature. In this study, therefore, we researched the temperature dependence of formation of Ti-based NCs with composition of Ge as well as the chemical and electrical characteristics for NVM applications.

A.2.2 Experiment

After the standard RCA clean process of a p-type silicon (100) wafer, a 4-nm-thick thermal oxidation layer was grown to be the tunneling oxide layer. Then, a ~10-nm-thick Ti-based germanosilicide layer was deposited to act as a charge tapping layer by co-sputtering $TiSi_2$ and Ge targets in Argon ambient at a pressure of 7.6 mTorr. The applied direct current powers on $TiSi_2$ and Ge targets were fixed at 100 W and 50 W, respectively. Then, a thin silicon dioxide layer of 10 nm was deposited by plasma enhanced chemical vapor deposition before annealing treatments (denoted as "10 nm-pre-capped sample") in order to reduce a possible contamination on the trapping layer during atmospheric exposure. For comparison, the other set of sample with a thicker pre-capped oxide of 20 nm (denoted as "20 nm-pre-capped sample") was also prepared in order to further discuss thermal desorption phenomena of the charge trapping layer during the subsequent annealing process. After encapsulation of the thin oxide layers, a rapid temperature annealing (RTA) was carried out at different temperature conditions of 400 ℃, 500 ℃ and 600 ℃ for 2 min to compare and recognize the temperature-related formation characteristics of NCs. After the annealing treatments, once again a 30-nm-thick and a 20-nm-thick silicon oxide layer were deposited on the 10 nm-pre-capped and 20 nm-pre-capped samples, respectively. So, a total 40 nm-thick oxide layer, including the pre-capped oxide, was produced to act as the blocking oxide. Finally, a 500-nm-thick Al gate electrode was deposited and patterned by shadow mask to form a capacitor structure for electrical measurements. On the other hand, the control samples without Ge composition in charge trapping layer, i.e. only a 10-nm-thick $TiSi_2$ as the trapping layer, were also fabricated with the same process conditions for comparison. The microstructure and chemical material analyses were adopted by transmission electron microscopy (TEM) and x-ray photoelectron spectroscopy (XPS), respectively. In addition, capacitance-voltage (C-V) hysteresis and electrical retention characteristics were performed by a HP4284 Precision LCR Meter with high frequency of 1 MHz. Figure A-6 shows the illustration of the proposed titanium-based NCs device structure with germanium doping and process flows.

A.2.3 Results and discussion

Figure A-7 shows cross-sectional TEM of the 10-nm-pre-capped samples with the annealing treatments of (a) 400 ℃, (b) 500 ℃, and (c) 600 ℃ as well as the 20-nm-pre-capped sample with the annealing treatment of (d) 600 ℃. It was observed that a blanket Ti-based germanosilicide film was still maintained even after the 400 ℃ annealing as shown in figure A-7 (a). However, after the 500 ℃ annealing, the

Ti-based germanosilicide film began to agglomerate and format NCs structure incompletely as shown in figure A-7 (b). Furthermore, after the 600 ℃ annealing, well-separated NCs structures were obtained as shown in figure A-7 (c) and figure A-7 (d). It was noted that by comparing between figure A-7 (c) and figure A-7 (d) which were with the same annealing condition, expansion of the NCs size as well as decrease of the NCs contrast to SiO_2 was observed evidently in the 10-nm-pre-capped sample [figure A-7 (c)]. These phenomena could be caused from an ineffective protection of the Ti-based germanosilicide layer against Ge thermal desorption, which was confirmed by the XPS results discussed below. In contrast, the 20-nm-pre-capped sample was observed to exhibit better crystallization due to the existence of Ge to reduce the phase formation temperature.

Figure A-8 (a), figure A-8 (b), and figure A-8 (c) show XPS of the 10-nm-pre-capped samples with different annealing conditions for O-*1s*, Si-*2p*, and Ti-*2p*, respectively. It is noted that all the XPS data were adopted from the annealed samples only with the pre-capped oxide layer after argon milling of the pre-capped oxide. In O-*1s* spectrum [figure A-8 (a)], it was observed that the main peak signal for Si-O bonding [B.12] is intact in the samples annealed at 400℃, and 500℃, and shifts toward higher binding energy in the sample annealed at 600℃, associating with the formation of more complete Si-O bonding [B.13]. It could be contributed to the formation of more stoichiometric and more condensed silicon oxide separated from the trapping layer due to the agglomeration of Ti-based germanosilicide NCs after a high temperature treatment. In Si-*2p* spectrum [figure A-8 (b)], a peak signal at 102.7 eV related to Si-O [B.14] bonding was observed in the sample annealed at 400 ℃. Additionally, another peak signal at 99.6 eV, corresponding to Si-Si binding [B.15], appears in the sample annealed at 500 ℃ and increases slightly in the sample annealed at 600 ℃. Besides, the Si-O peak also shifts toward higher binding energy of 103.1 eV after the 600 ℃ annealing, which also consists with the O-*1s* due to the more complete Si-O bonding. In Ti-*2p* spectrum of figure A-8 (c), Ti-O peak signals referred to TiO_2 [B.16] were detected and after all annealing conditions. Ti atom is easily oxidized since TiO_2 is a thermodynamically stable phase, and hence, the trace O_2 in RTA ambiance or the absorbed O_2 on the wafer surface during wafer transportation (air exposure) is enough to format Ti-O bonding during high temperature annealing [B.17-B.19]. In addition, after the 500 ℃ and 600 ℃ annealing, one more peak referred to Ti-O-Si bonding was observed [B.20]. In Ge-2p spectra [figure B-8 (d)], it was observed that not only Ge peak signal but also considerable GeO, and GeO_2 peak signals were exhibited in the sample annealed at 400 ℃, which is similar to Ti atoms and contributed to the ease of oxidation of Ge atoms in the present of O_2 ambient [B.16]. After the 500 ℃ annealing, the Ge-Ge binding dominates significantly instead of the Ge-O bindings. According to the XPS results of Si and Ge signals, the appearance of Si-Si and Ge-Ge bonds could be related to formation of Si-Ge [B.21] and contributed from the Si-Ge precipitates [B.22, B.23]. Moreover, since the enthalpy of $TiSi_2$ formation is larger than that of $TiGe_2$ [B.13, B. 24], there is a tendency for Si to replace Ge in Ti-Si-Ge compounds [B.25]. Such a replacement accompanies the formation of germanium-rich Si-Ge precipitates and then causes the remarkable Ge-Ge signals. It is noted that peak signals related to the elemental Ge were only observed obviously in the 10-nm-pre-capped samples after the 400℃ and 500℃ annealing but severely decreased after the 600℃ annealing. From the point of view of quantitative XPS analysis, the atomic concentration ratio of Ge-*2p*/Ti-*2p* was reduced obviously from 3.62 in the 500℃-annealed sample to 0.41

in the 600℃-annealed sample, consisting with the TEM contrast results discussed above. In order to further confirm the binding characteristics at the 600℃-treated condition, an analysis of the Ge-*2p* XPS spectra was also carried out on the 20-nm-pre-capped sample. Particular exhibition of large amount of non-stoichiometric germanium oxide was observed in the 20-nm-pre-capped sample after the 600℃ annealing. Production of the unneglectable GeO might be caused from oxidation of the precipitated Ge during the 600 ℃-annealed process. In addition, it has been reported that the GeO phase is too thermodynamically unstable to sublime at such annealing conditions [B.26, B.27]. Therefore, occurrence of the severe decrease of Ge element in the 10-nm-pre-capped sample after the 600 ℃ annealing is also indirectly confirmed to thermal desorption due to sublimation of the formatted GeO phase. According to the XPS results, therefore, the NCs the charge trapping layer are mainly composed of titania-germanosilicide after the 500℃ annealing and mainly titania-germanium oxide after the 600℃ annealing.

Figure A-9 shows a comparison of high frequency C-V characteristics on the 10-nm-pre-capped samples with the annealing treatment of (a) 400 ℃, (b) 500 ℃, and (c) 600 ℃. As shown in figure A-9 (a), nearly no flat band voltage shift (ΔV_{th}) was observed with gate bias voltage sweeping in the sample after the 400 ℃ annealing, which is mainly due to a continuous structure of the charge trapping layer. When the annealing temperature was increased to 500 ℃ [figure A-9 (b)], large ΔV_{th} of ~1.8 V, ~4 V, and ~6.1 V was obtained while the gate voltage was swept in the range between 3 / -3 V, 5 / -5 V, and 7 / -7 V, respectively. In addition, the observed counterclockwise hysteresis loops indicate that charge carriers were injected from the silicon substrate through the tunnel oxide. However, when the 600 ℃ annealing condition was performed, the ΔV_{th} reduces severely as shown in figure A-9 (c). By contrast, figure A-9 (d) also shows C-V characteristics of the 20-nm-pre-capped sample after the 600 ℃ annealing. Again, exhibition of ΔV_{th} of ~0.6 V, ~1.2 V, and ~3.8 V were observed under the gate voltage sweeping ranges of 3 / -3 V, 5 / -5 V, and 7 / -7 V, respectively. On the other hand, the control samples, whose charge trapping layer was only composed of $TiSi_2$, show no flat band voltage shifts after the 400 ℃, 500 ℃ or 600 ℃ annealing conditions (not showed here). Additionally, Ge NCs reported in past researches for NVMs applications [B.28-B.30] were almost fabricated above such temperatures. According to the discussions above, therefore, we could suggest that the exhibition of memory effects is strongly associated with the addtion of Ge in Ti-based NCs instead of the only Ge or TiO_2 NCs.

Figure A-10 shows a comparison of retention characteristics between the 10-nm-pre-capped sample annealed at 500 ℃ and the 20-nm-pre-capped one annealed at 600 ℃. After both the devices were operated to the condition with a nearly the same memory window of ~3.5V, the memory windows of 10 nm-capped sample and the 20 nm-capped sample still retained ~1.30 V and ~1.75 V after 10^4 sec, respectively. Better retention characteristic was exhibited in the sample with a higher temperature treatment, associating with better separation of the charge storage NCs.

A.2.4 Conclusion

In conclusion, the memory effects of the Ti-based NCs fabricated by annealing the co-sputtered thin film with a titanium silicide and a germanium targets were demonstrated at a relatively low fabrication temperature of 500 ℃ due to the presence of Ge atoms. However, as the annealing temperature was increased to 600 ℃, thermal desorption of Ge atoms occurred and degraded the electrical characteristic of threshold voltage shift severely. An effective approach to suppressing such the thermal desorption at 600 ℃ was proposed by depositing a efficient pre-capped oxide layer (20 nm here) on the trapping layer before annealing treatments. By annealing the efficiently encapsulated NVMs device at 600 ℃, therefore, better crystallization and separation of the Ti-based NCs would obtain and result in the exhibition of a better electrical retention performance, compared to the 500 ℃ -annealed one.

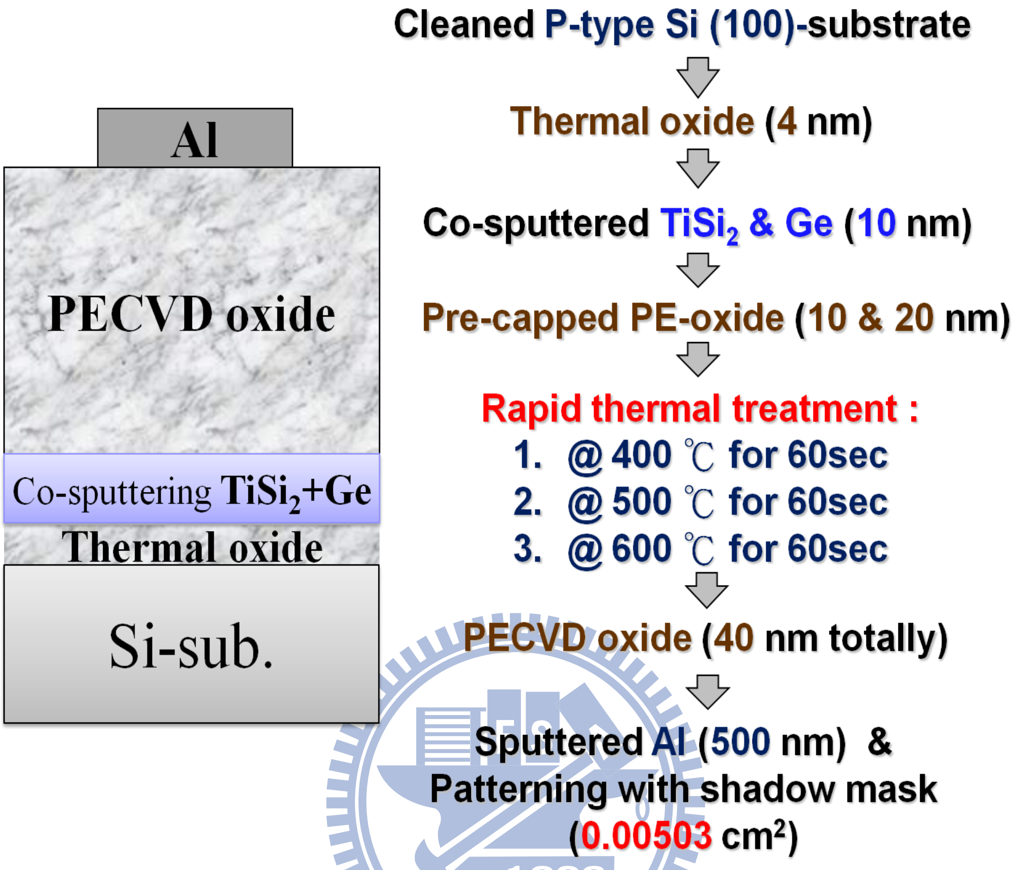


Fig. A-6 Illustration of the proposed titanium-based nanocrystals device structure with germanium doping and process flows.

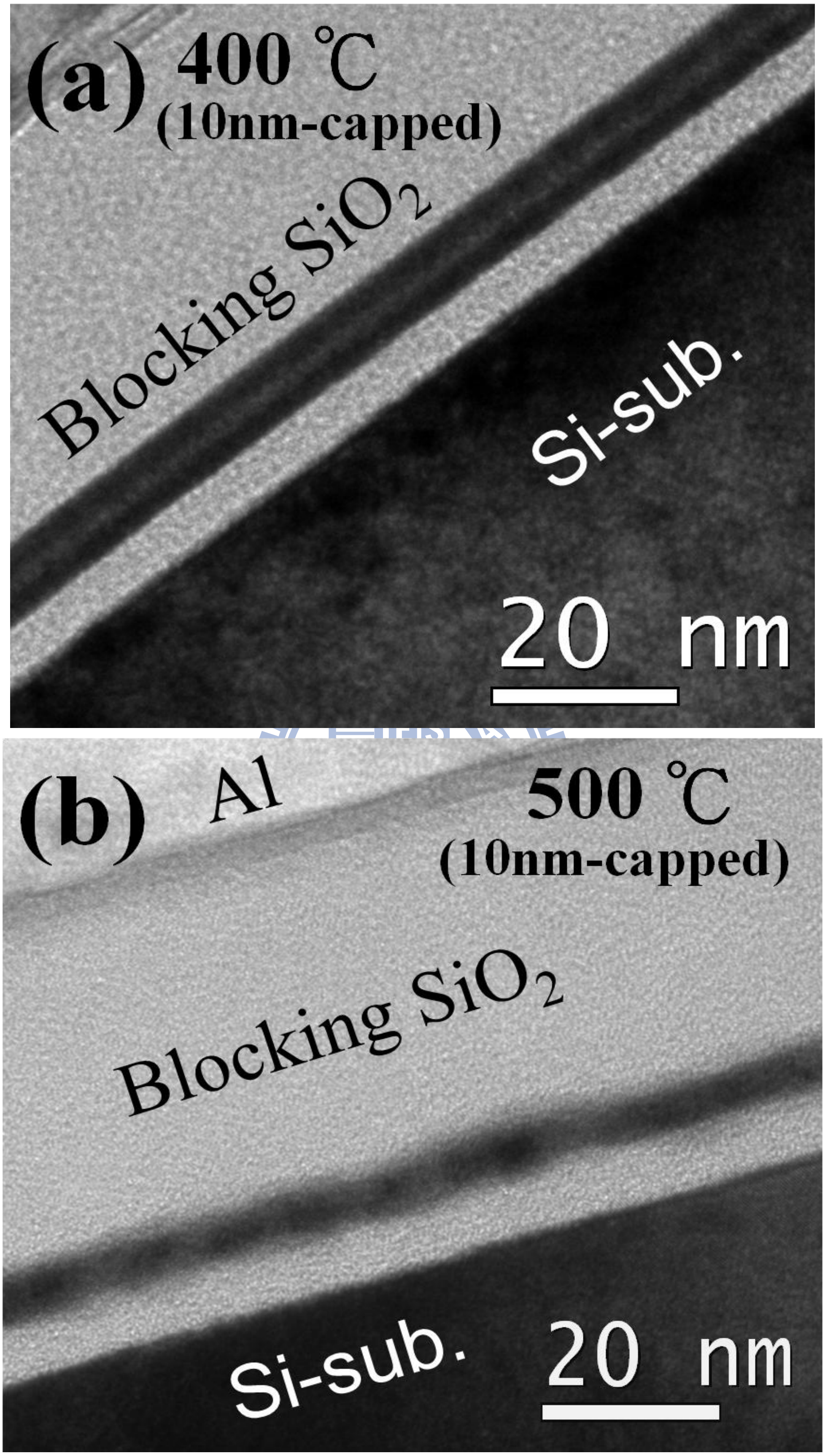


Fig. A-7 (a) & (b) Cross-sectional TEM of the 10-nm-pre-capped samples after annealed at (a) 400 ℃ and (b) 500 ℃.

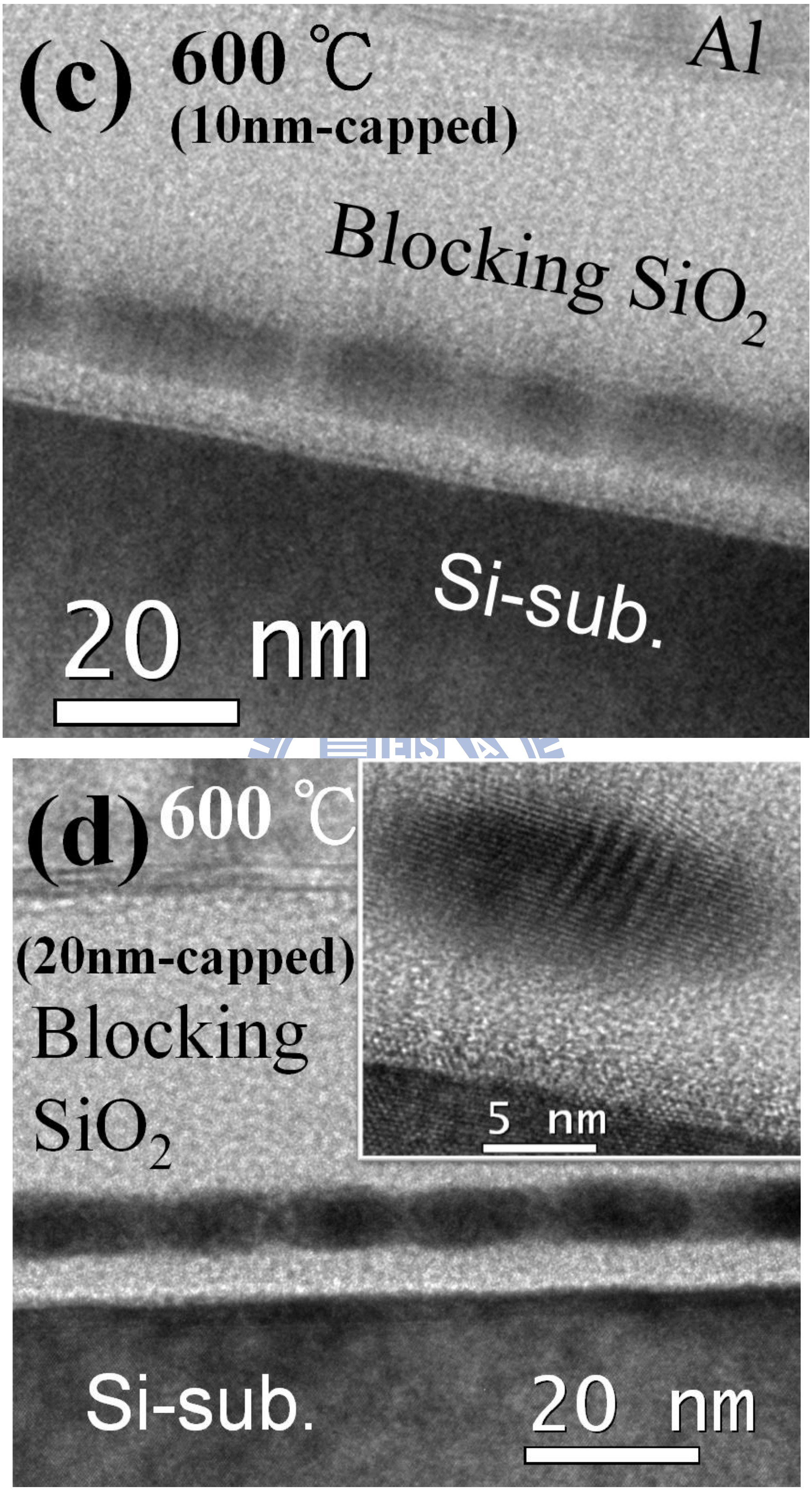


Fig. A-7 (c) & (d) Cross-sectional TEM of the 10-nm-pre-capped and the 20-nm-pre-capped samples after annealed at 600 ℃.

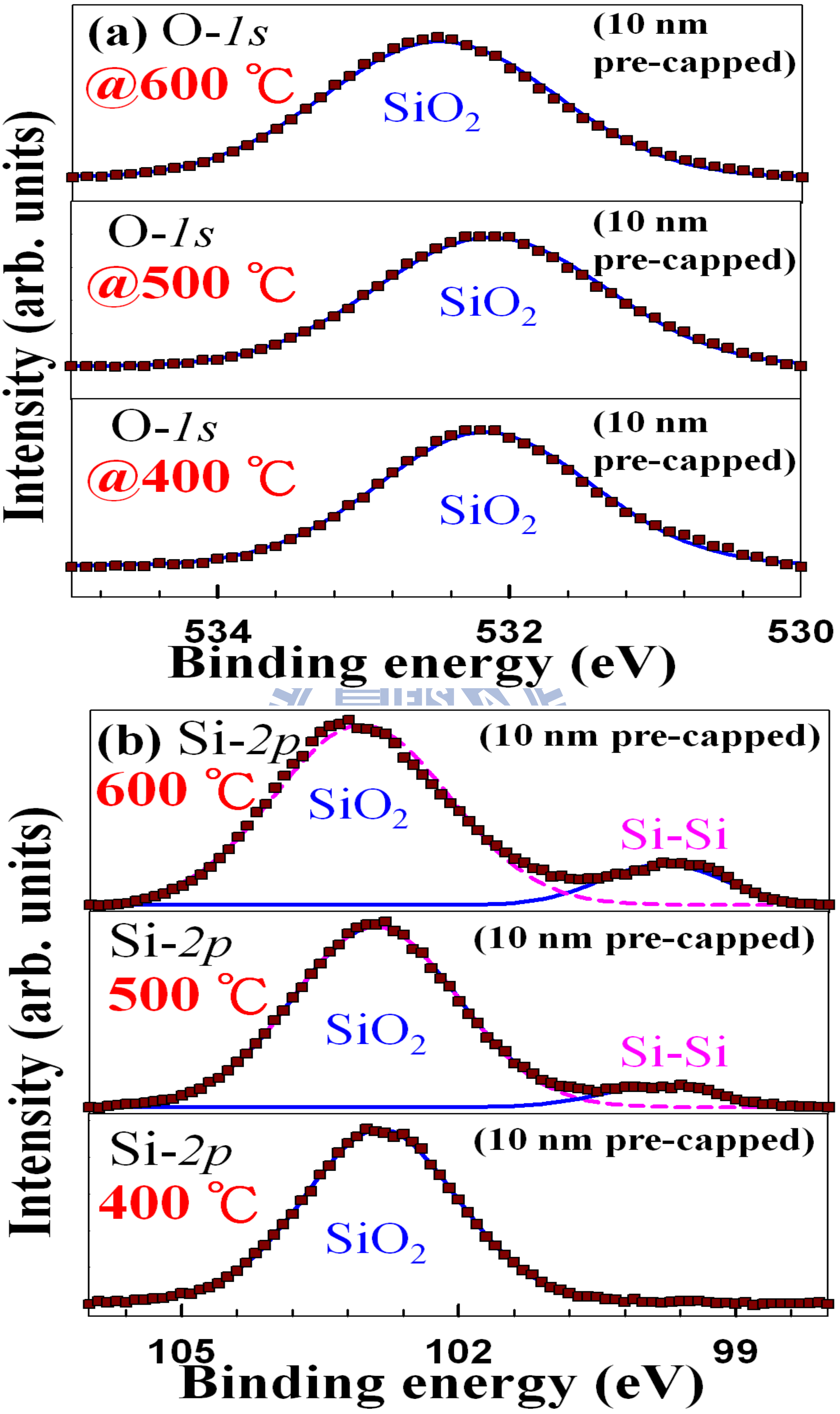


Fig. A-8 (a) & (b) XPS spectra of the 10-nm-pre-capped samples annealed at 400℃, 500℃, and 600℃ for (a) O-*1s* and (b) Si-*2p*.

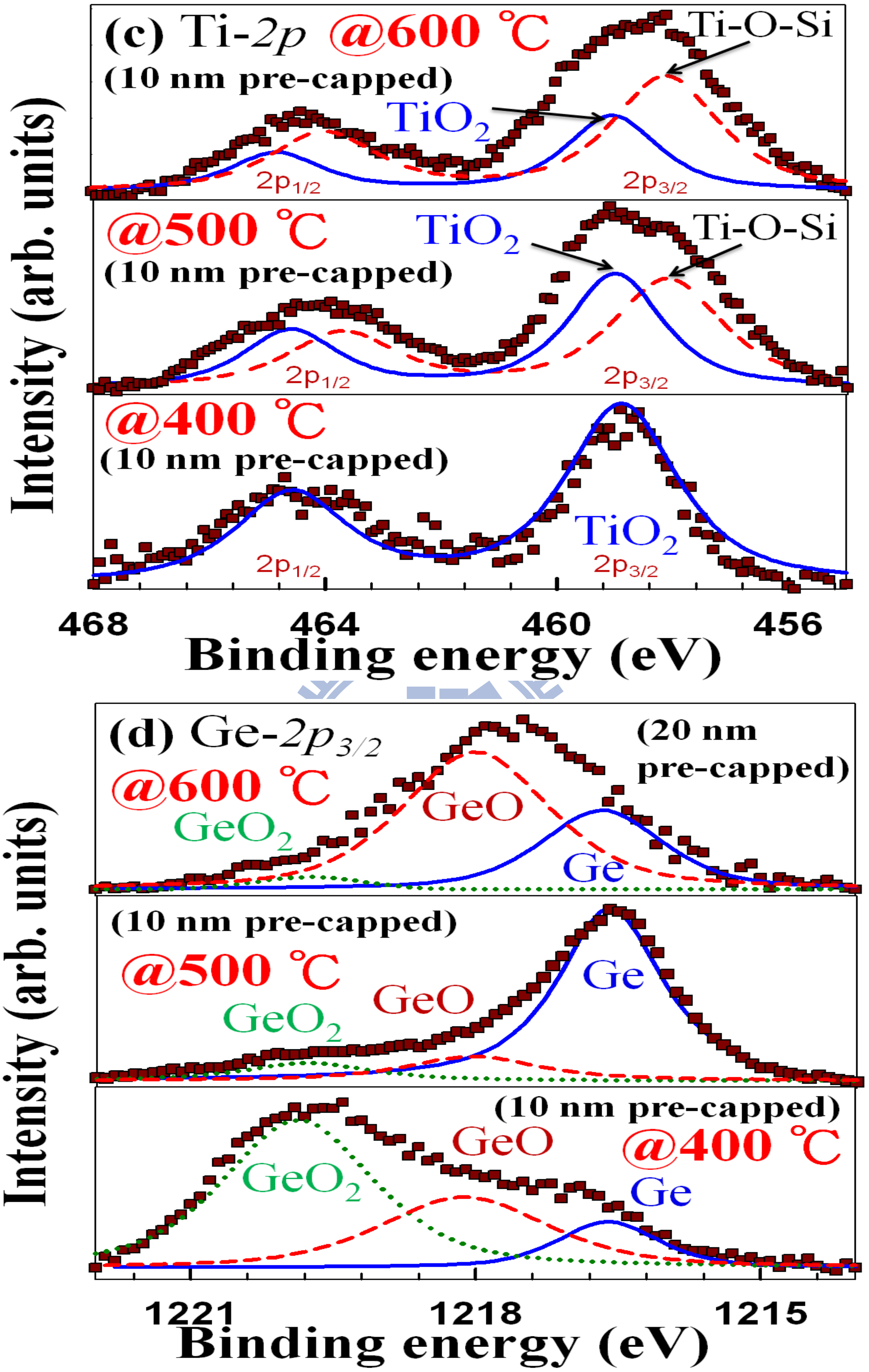


Fig. A-8 (c) & (d) XPS spectra of the 10-nm-pre-capped samples annealed at 400℃, 500℃, and 600℃ for (c) Ti-*2p* and (d) Ge-2p with the exception of 600℃-treated Ge signals, which was analyzed in the 20-nm-pre-capped sample.

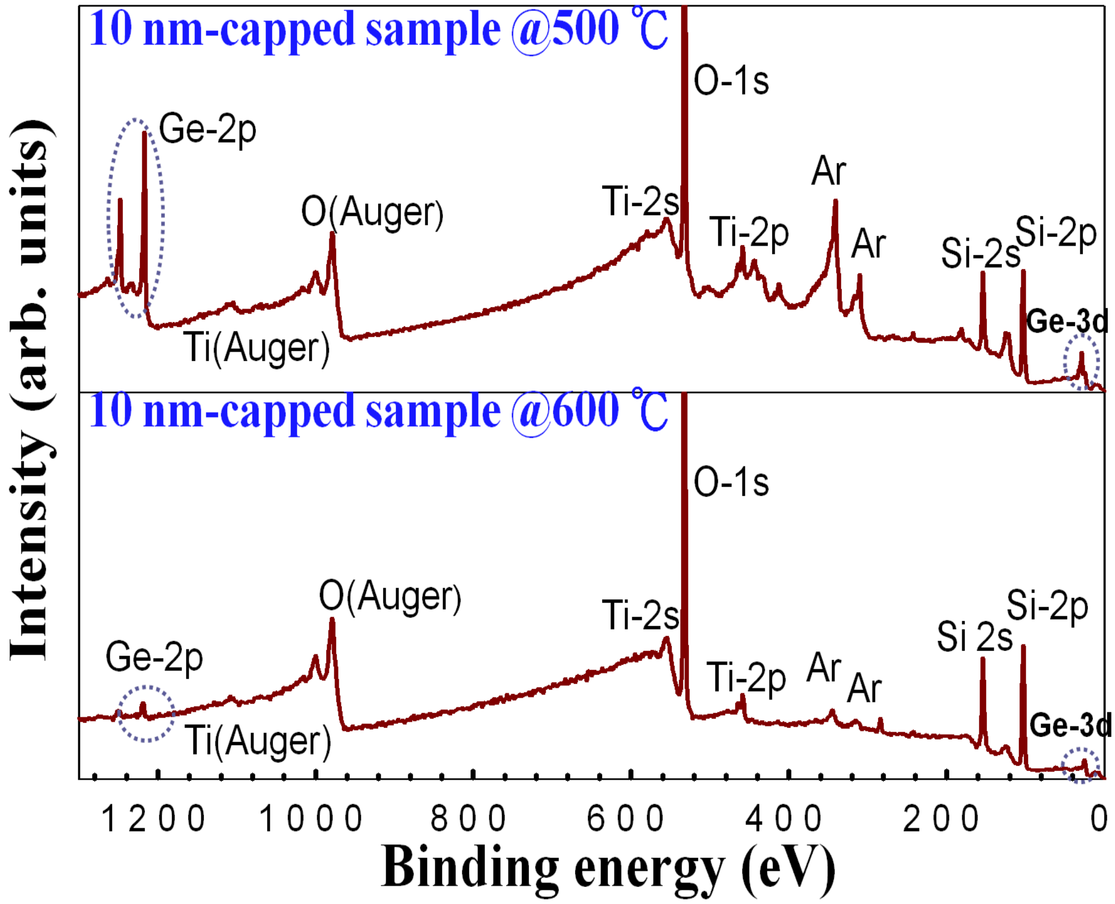


Fig. A-8(e) XPS overall region on the Ti-based germanosilicide samples with the 500 ℃ and 600 ℃ annealing, detected with Ar ion milling of the 10 nm-thick pre-capped oxide.

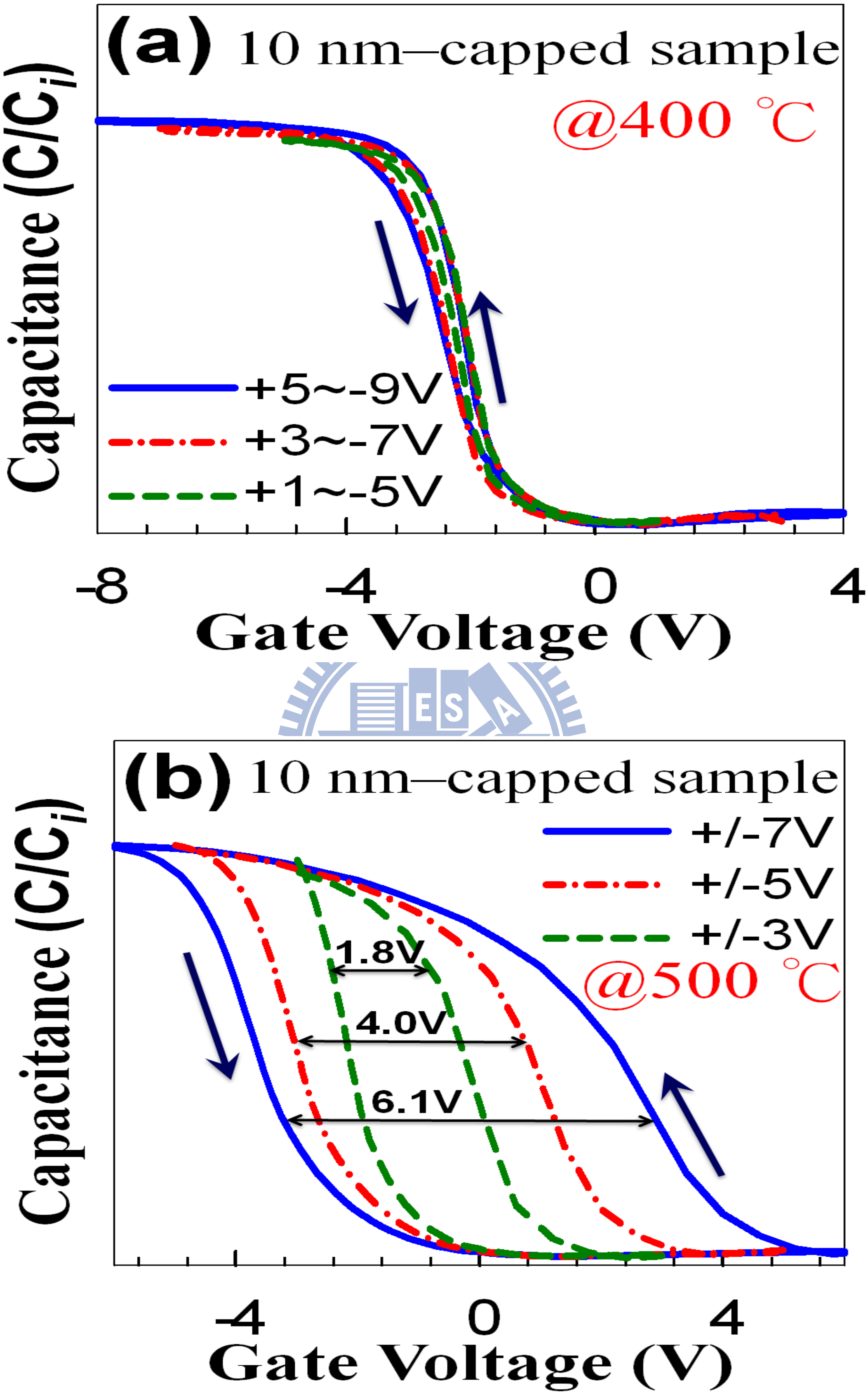


Fig. A-9 (a) & (b) Comparison of high frequency *C-V* characteristics on the 10 nm-pre-capped samples with the thermal treatments of (a) 400 ℃ and (b) 500 ℃.

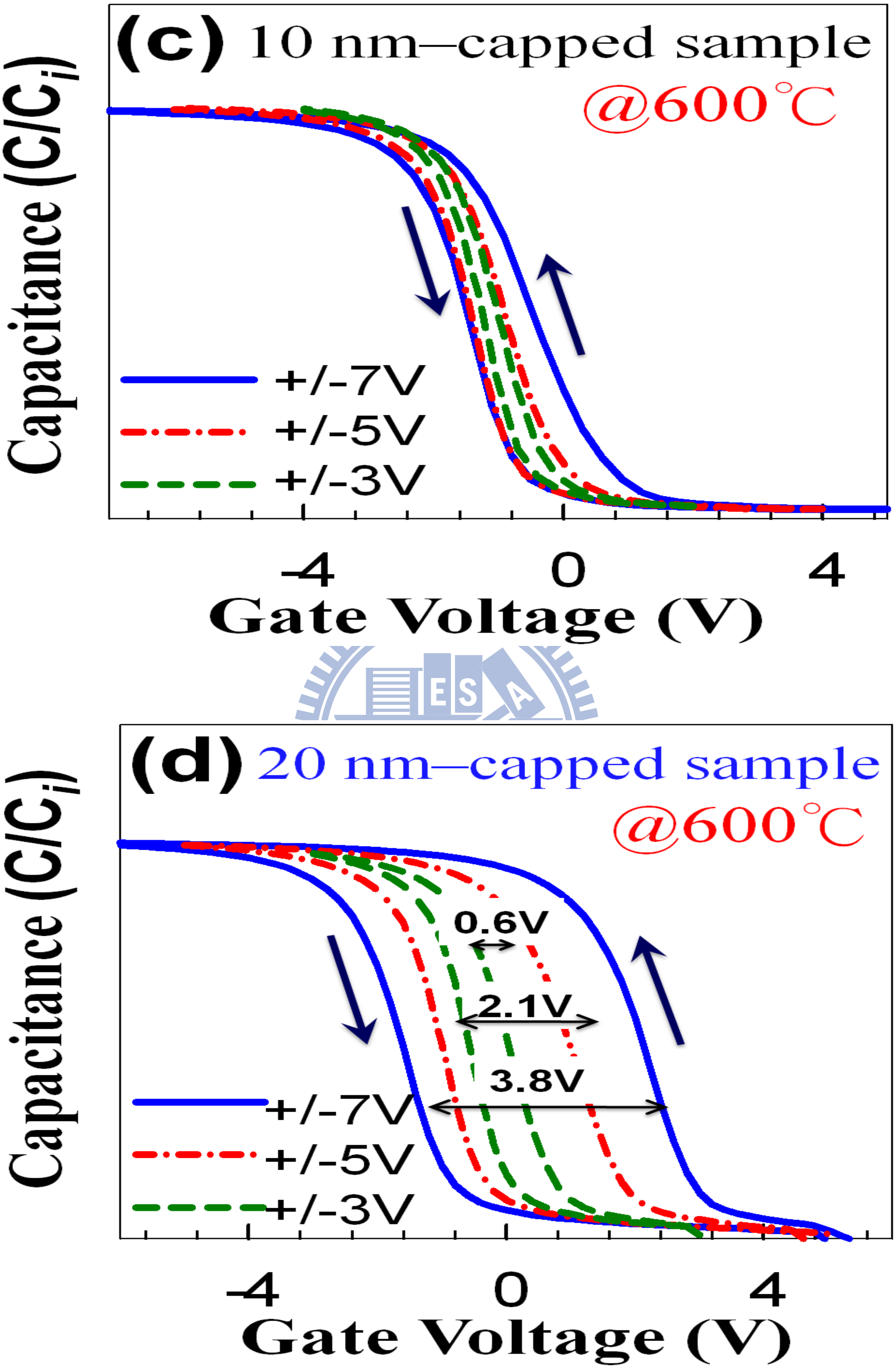


Fig. A-9 (c) & (d) Comparison of high frequency *C*-*V* characteristics on (c) the 10 nm-pre-capped and (d) the 20 nm-pre-capped samples with the 600 ℃ annealing.

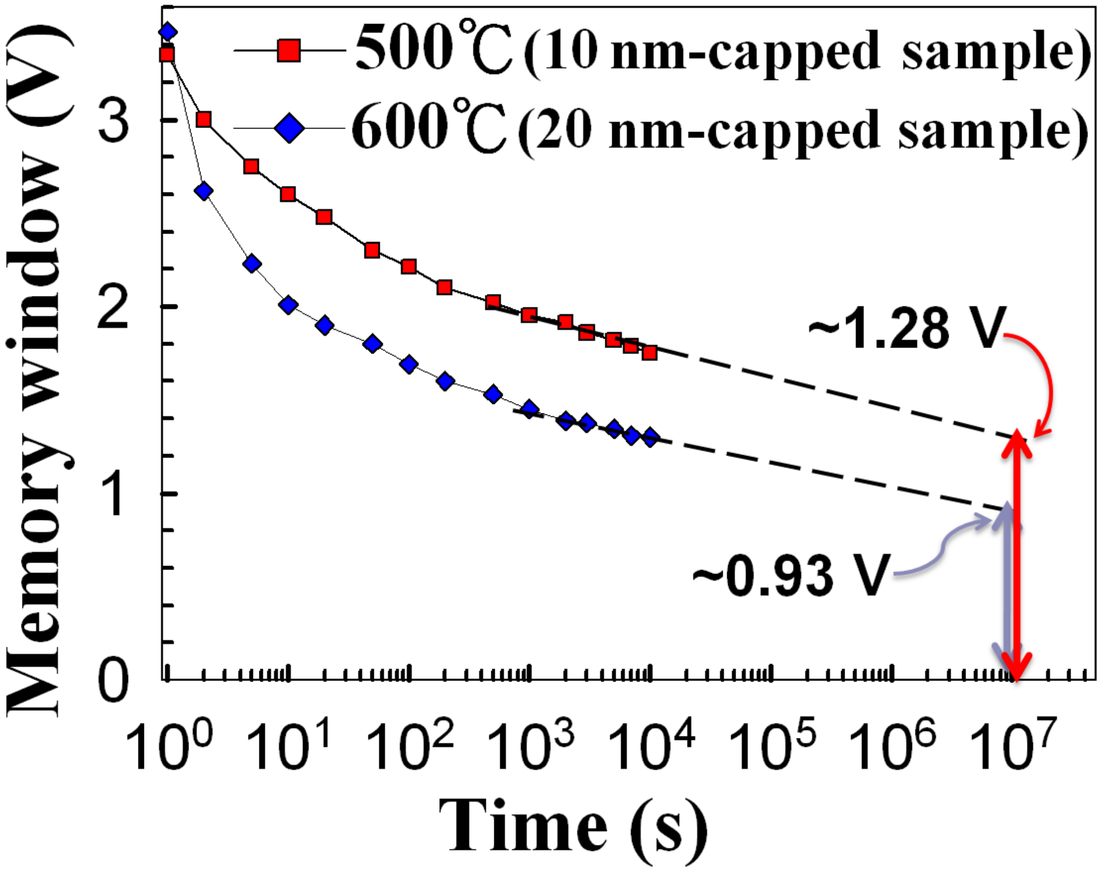


Fig. A-10 Comparison of retention characteristics between the 10 nm-pre-capped memory capacitor sample with the 500 ℃ annealing and the 20 nm-pre-capped one with the 600 ℃ annealing.

Appendix References

Chapter A.1

[A.1] D. Kahng, S.M. Sze. Bell Syst. Tech. Journal, **46**, p. 1288 (1967).

[A.2] F.M. Yang, T.C. Chang, P.T. Liu, P.H. Yeh, Y.C. Yu, J.Y. Lin, S.M. Sze, and J.C. Lou , Appl. Phys. Lett. **90**, 132102 (2007).

[A.3] C.H. Chen, T.C. Chang, I.H. Liao, P.B. Xi, C.T. Tsai, P.Y. Yang, Joe Hsieh, Jason Chen, U.S. Chen, and J.R. Chen, Appl. Phys. Lett. **91**, 232104 (2007).

[A.4] W.R. Chen, T.C. Chang, Y.T. Hsieh, S.M. Sze, and C.Y. Chang, Appl. Phys. Lett. **91**, 102106 (2007).

[A.5] S.M. Yang, C.H. Chien, J.J. Huang, and T.F. Lei, Appl. Phys. Lett. **91**, 262104 (2007).

[A.6] Y.H. Lin, C.H. Chien, C.T. Lin, C.Y. Chang, and T.F. Lei, IEEE Trans. Electron Devices **53**, 782 (2006).

[A.7] H.C. You, F.H. Ko, and T.F. Lei, J. Electrochem. Soc. 153, F94 (2006).

[A.8] R. Muralidhar, R.F. Steimle, M. Sadd, R. Rao, C.T. Swift, E.J. Prinz, J. Yater, L. Grieve, K. Harber, B. Hradsky, S. Straub, B. Acred, W. Paulson, W. Chen, L. Parker, S. G. H. Anderson, M. Rossow, T. Merchant, M. Paransky, T. Huynh, D. Hadad, K.-M. Chang, and B. E. White, Jr., IEDM Tech. Dig., p. 26.2.1 (2003).

[A.9] Chungho Lee, Gorur-Seetharam, A., Kan, E.C., IEDM Technicd Digest, p. 22.6.1 (2003).

[A.10] T. Baron, B. Pelissier, L. Perniola, F. Mazen, J.M. Hartmann and G. Rolland, Appl. Phys. Lett. **83**, p. 1444 (2003).

[A.11] Sangomoo choi, Seok-Soon Kim, Man Chang, Hyunsang Hwang, Sanghun

Jeon and Chungwoo Kim, Appl. Phys. Let. **86**, 123110 (2005).

[A.12] S. Mailap, P.J. Tzeng, H.Y. Lee, C.C. Wang, T.C. Tien, L.S. Lee, and M.J. Tsai. Appl. Phys. Let. 9 (2007).

[A.13] C.H. Lin, C.-C. Wang, P.J. Tzeng, Siddheswar MAIKAP, H.Y. Lee, L.S. Lee, and M.J. Tsai. Jpn. J. Appl. Phys. **46**, No. 4B, p.2523 (2007).

[A.14] Takeshi MORIKAWA, Ryoji ASAHI, Takeshi OHWAKI, Koyu AOKI and Yasunori TAGA, Jpn. J. Appl. Phys. **40**, p. L 561 (2001).

[A.15] Songwang Yang and Lian Gao. J. Am. Ceram. Soc. **87**, p.1803 (2004).

[A.16] J. Guillota, F. Fabreguetteb, L. Imhoffa, O. Heintza, M. C. Marco de Lucasa, M. Sacilottib, B. Domenichinia, S. Bourgeois. Appl. Surf. Sci. **177**, p.268 (2001).

[A.17] J. D. Plummer, M. D. Deal, and P. B. Griffin, Text Book: Silicon VLSI Technology Fundamentals Practice and Modeling.

[A.18] H. Noda, K. Oikawa, T. Ogata, K. Matsuki and H. Kamada: Nippon Kagaku Kaishi, **8**, 1084 (1986) [in Japanese].

[A.19] C. H. Lin, C. C. Wang, P. J. Tzeng, C. S. Liang, W. M. Lo, H. Y. Li, L. S. Lee, S. C. Lo, Y. W. Chou, and M. J. Tsai, Jpn. J. Appl. Phys., Part 1 45, 3036 (2006).

[A.20] J. M. Wang, W. G. Liu, and T. Mei, Ceram. Int. 30, 1921 (2004).

[A.21] T.L. BARR, Journal Phys. Chem., **10**, p.760 (1990).

[A.22] N.C. Saha and H.G. Tompkins, J. Appl. Phys. **72**, 3072 (1992).

[A.23] S. Petigny, H. Mostefa-Sba, B. Domenichini, E. Lesniewska, A. Steinbrunn, S. Bourgeois, Surf. Sci. 410, 250 (1998).

[A.24] Yang W Y, Iwakuro H, Yagi H, Kuroda T and Nakamura S 1984 *Jpn. J. Appl.* Phys. 23 (1560).

[A.25] Yang W Y, Iwakuro H, Yagi H, Kuroda T and Nakamura S 1984 Jpn. J. Appl. Phys. 23 (1560).

Chapter A.2

[B.1] T. C. Chang, P. T. Liu, S. T. Yan, and S. M. Sze, Electrochem. Solid-State Lett. **8**, G71 (2005).

[B.2] T. C. Chang, S. T. Yan, C. H. Hsu, M. T. Tang, J. F. Lee, Y. H. Tai, P. T. Liu, and S. M. Sze, Appl. Phys. Lett. **84**, 2581 (2004).

[B.3] P. H. Yeh, C. H. Yu, L. J. Chen, H. H. Wu, P. T. Liu, and T. C. Chang, Appl. Phys. Lett. **87**, 193504 (2005).

[B.4] Sangomoo choi, Seok-Soon Kim, Man Chang, Hyunsang Hwang, Sanghun Jeon and Chungwoo Kim, Appl. Phys. Let. **86**, 123110 (2005).

[B.5] S. Mailap, P.J. Tzeng, H.Y. Lee, C.C. Wang, T.C. Tien, L.S. Lee, and M.J. Tsai. Appl. Phys. Let. **91**, 043114 (2007).

[B.6] Cha-Hsin Lin, Ching-Chiun Wang, Pei-Jer Tzeng, Siddheswar MAIKAP, Heng-Yuan Lee, Lurng-Shehng Lee, and Ming-Jinn Tsai. Jpn. J. Appl. Phys. **46**, 4B, 2523 (2007).

[B.7] L.W. Feng, C.Y. Chang, T.C. Chang, C.H. Tu, P.S. Wang, Y.F. Chang, M.C. Chen, and H.C. Huang, Appl. Phys. Let. 95, 262110 (2009).

[B.8] B. UMAPATHI, S. DAS, S.K. LAHIRI, and S. KAL. Journal of Electronic

Materials, **30**, 17 (2001).

[B.9] D.B. Aldrich, Y.L. Chen, D.E. Sayers, R.J. Nemanich, S.P. Ashburn, and M.C. Ozturk, J. Appl. Phys. **77**, 5107 (1995).

[B.10] N. Boutarek and R. Madar, Appl. Surface Sci. **73**, 209 (1993).

[B.11] O. Thomas, F.M. d'Heurle, and S. Delage, J. Mater. Res. **5**, 1453 (1990).

[B.12] G. MINK - G. VARSANYI - I. BERTOTI - J. GRABIS - J. VAIVADS - T. MILLERS - T. SZEKELY, Surface and Interface Analysis, **12**, 527 (1988).

[B.13] R. Alfonsetti, G. De Simone, L. Lozzi, M. Passacantando, P. Picozzi and S. Santucci, Surface and Interface Analysis, **22**, 89 (1994).

[B.14] Liang-Po Chen, Yuen-Chang Chan, Shoou-Jinn Chang, Guo-Wei Huang and Chun-Yen Chang, Jpn. J. Appl. Phys. **37**, L 122 (1998).

[B.15] Finster J. Surf. Interface Anal. **12**, 309 (1988).

[B.16] H. Noda, K. Oikawa, T. Ogata, K. Matsuki and H. Kamada: Nippon Kagaku Kaishi, **8**, 1084 (1986) [in Japanese].

[B.17] C. H. Lin, C. C. Wang, P. J. Tzeng, S. Maikap, H.-Y. Lee, L. S. Lee, and M. J. Tsai, Jpn. J. Appl. Phys., Part 1 **46**, 2523 (2007).

[B.18] C. H. Lin, C. C. Wang, P. J. Tzeng, C. S. Liang, W. M. Lo, H. Y. Li, L. S. Lee, S. C. Lo, Y. W. Chou, and M. J. Tsai: Jpn. J. Appl. Phys. 45,3036 (2006).

[B.19] J. M. Wang, W. G. Liu, and T. Mei: Ceram. Int. 30, 1921 (2004).

[B.20] W. X. Xu, Shu Zhu, X. C. Fu, Applied Surface Science 136, 194 (1998).

[B.21] Zheng Youdou, Zhang Rong, Hu Liquan, Mo Shuiyuan, Li Xuenin and Zhong Peixin, Physica Scripta. **41**, 1041 (1990).

[B.22] D. B. Aldrich, F. M. d'Heurle, D. E. Sayers, and R. J. Nemanich, Phys. Rev. B **53**, 16279 (1996).

[B.23] W.R. Chen , T.C. Chang , P.T. Liu , C.H. T , J.L. Yeh, Y.T. Hsieh , R.Y. Wang , C.Y. Chang, Surface & Coatings Technology **202**, 1333 (2007).

[B.24] F. R. deBoer, R. Boom, W. C. M. Mattens, A. R. Miedema, and A. K. Niessen, Cohesion in Metals-Transition Metal Alloys North-Hollan, Amsterdam, **1**, 127 (1988),.

[B.25] James E. Burnette, Robert J. Nemanich,a! and Dale E. Sayers. Journal of Appl. Phys. **97**, 113521 (2005).

[B.26] Y. Pauleau and J.-C. J. Remy, J Less-Common Met, **42**, 199 (1975).

[B.27] Jungwoo Oh, and Joe C. Campbell, Journal of Electronic Materials, **33**, 364 (2004).

[B.28] X. B. Lu, P. F. Lee, and J. Y. Dai, Appl. Phys. Lett. **86**, 203111 (2005).

[B.29] S. Duguay, J. J. Grob, A. Slaoui, Y. Le Gall, and M. Amann-Liess, Jour. of Appl. Phys. **97**, 104330 (2005).

[B.30] T. H. Ng, W. K. Chim, W. K. Choi, V. Ho, L. W. Teo, A. Y. Du and C. H. Tung, Appl. Phys. Lett. **84**, 4385 (2004).

Vita 簡 歷

姓名： 馮立偉 (Li-Wei Feng)

出生日期：民國 69 年 10 月 08 日 (1980/10/08)

住址：830 高雄縣鳳山市五福里福德街 143 巷 36 號 7 樓

學歷：

國立中山大學 物理系 學士班

(1999.09-2003.6)

國立交通大學 電子工程研究所 碩士班

(2003.09-2005.6)

國立交通大學 電子工程研究所 博士班

(2005.09-迄今)

論文題目：

前瞻非揮發性電阻式記憶體元件之製作與特性研究

Fabrication and Characterization of FeO_x Based Resistive Random Access Memory

Publication List（著作目錄）

International Journals:

[1]. Chun-Hao Tu, Ting-Chang Chang, Po-Tsun Liu, Hsiao-Wen Zan, Ya-Hsiang Tai, **Li-Wei Feng**, Yung-Chun Wu, Chun-Yen Chang "Improvement of reliability for polycrystalline thin-film transistors using self-aligned fluorinated silica glass spacers" ELECTROCHEMICAL AND SOLID STATE LETTERS, **8** , 8, G209 (2005).

[2]. Yung-Chun Wu, Hung-Bin Chen, **Li-Wei Feng**, Ting-Chang Chang, Po-Tsun Liu, Chun-Yen Chang "Reliability Study on Tri-Gate Nanowires Poly-Si TFTs under DC and AC Hot-Carrier Stress" 2007 7TH IEEE CONFERENCE ON NANOTECHNOLOGY, **1-3,** 767 (2007).

[3]. Chun-Hao Tu, Ting-Chang Chang, Po-Tsun Liu, Che-Yu Yang, **Li-Wei Feng**, Chia-Chou Tsai, Li-Ting Chang, Yung-Chun Wu, Simon M. Sze, Chun-Yen Chang "Improved performance of F-ions-implanted poly-Si thin-film transistors using solid phase crystallization and excimer laser crystallization" JOURNAL OF DISPLAY TECHNOLOGY, **3**, 1, 45, MAR (2007).

[4]. Shih-Ching Chen, Ting-Chang Chang, Po-Tsun Liu, Yung-Chun Wu, Chin-Cheng Ko, Sidney Yang, **Li-Wei Feng**, S. M Sze, Chun-Yen Chang, Chen-Hsin Lien, "Pi-shape gate Polycrystalline Silicon Thin-Film-Transistor for Nonvolatile Memory Applications ", APPLIED PHYSICS LETTERS, **91**, 21, 213101**,** NOV 19 (2007).

[5]. Shih-Ching Chen, Ting-Chang Chang, Po-Tsun Liu, Yung-Chun Wu, Jing-Yi Chin, Ping-Hung Yeh, **Li-Wei Feng**, S. M. Sze, Chun-Yen Chang, Chen-Hsin Lien "Nonvolatile Si/SiO$_2$/SiN/SiO$_2$/Si type polycrystalline silicon thin-film-transistor memory with nanowire channels for improvement of erasing characteristics" APPLIED PHYSICS LETTERS, **91**, 19, 193103, NOV 5 (2007).

[6]. Yung-Chun Wu, Ting-Chang Chang, Po-Tsun Liu, **Li-Wei Feng** "Degradation behaviors of trigate nanowires poly-si TFTs with NH3 plasma passivation under hot-carrier stress", ELECTROCHEMICAL AND SOLID STATE LETTERS, **10**, 8, H235, (2007).

[7]. Chun-Hao Tu, Ting-Chang Chang, Po-Tsun Liu, Che-Yu Yang, **Li-Wei Feng**, Yung-Chun Wu, Simon M. Sze, Chun-Yen Chang, "Performance enhancement of excimer laser crystallized poly-Si thin film transistors with fluorine implantation

technology” THIN SOLID FILMS, **516**, 10, 3128, MAR 31 (2008).

[8]. **Li-Wei Feng**, Ting-Chang Chang, Po-Tsun Liu, Chun-Hao Tu, Yung-Chun Wu, Che-Yu Yang and Chun-Yen Chang, “Application of fluorine doped oxide (SiOF) spacers for improving reliability in low temperature polycrystalline thin film transistors”, THIN SOLID FILMS, 517, 3, 1204 (2008).

[9]. **Li-Wei Feng**, Chun-Yen Chang, Ting-Chang Chang, Chun-Hao Tu, Pai-Syuan Wang, Yao-Feng Chang, Min-Chen Chen, and Hui-Chun Huang “Role of germanium in the reduced temperature dependence of Ti-based nanocrystals formation for nonvolatile memory applications”, APPLIED PHYSICS LETTERS **95**, 262110 (2009).

[10]. Chao-Cheng Lin, Ting-Chang Chang, Chun-Hao Tu, Wei-Ren Chen, **Li-Wei Feng**, Simon M. Sze, Tseung-Yuen Tseng, Sheng-Chi Chen, Jian-Yang Lin “Improvement of Charge-Storage Characteristics of Mo Nanocrystal Memory by Double-Layer Structure”, JOURNAL OF THE ELECTROCHEMICAL SOCIETY, **156**, 4, H276 (2009).

[11]. **Li-Wei Feng**, Chun-Yen Chang, Yao-Feng Chang, Ting-Chang Chang,Shin-Yuan Wang, Shih-Ching Chen, Chao-Cheng Lin, Shih-Cheng Chen and Pei-Wei Chiang,“Improvement of resistance switching characteristics in a thin FeOx transition layer of TiN/SiO_2/FeO_x/FePt structure by rapid annealing”, APPLIED PHYSICS LETTERS **96**, 222108 (2010).

[12]. **Li-Wei Feng**, Chun-Yen Chang, Yao-Feng Chang, Wei-Ren Chen, Shin-Yuan Wang, Pei-Wei Chiang and Ting-Chang Chang,“A study of resistive switching effects on a thin FeO_x transition layer produced at the oxide/iron interface of TiN/SiO_2/Fe-contented electrode structures”, APPLIED PHYSICS LETTERS **96**, 052111 (2010).

[13]. **Li-Wei Feng**, Yao-Feng Chang, Chun-Yen Chang, Ting-Chang Chang, Shin-Yuan Wang, Pei-Wei Chiang, Chao-Cheng Lin, Shih-Ching Chen, Shih-Cheng Chen, “Reproducible resistance switching effects of a relatively thin FeO_x layer produced by oxidizing the surface of a FePt electrode in a metal-oxide-metal structure”, THIN SOLID FILMS, (2010).

International Conference:

[1]. **L.W. Feng**, Chun-Yen Chang, Ting-Chang Chang, Yao-Feng Chang, Shin-Yuan Wang, Pei-Wei Chiang, Chao-Cheng Lin, ” Reproducible resistance switching

effects of a relatively thin FeOx layer produced by oxidizing the surface of a FePt electrode in a metal-oxide-metal structure", International Conference on Metallurgical Coatings and Thin Films", April 26 –30, (2010).

[2]. **Li-Wei Feng**, Chun-Yen Chang, Ting-Chang Chang, Chun-Hao Tu, Pai-Syuan Wang, Der-Shin Gan, New-Jin Ho, Hui-Chun Huang, Min-Chen Chen, "Formation of Titanium Germanosilicide nanocrystals for nonvolatile memory applications", International Conference on Metallurgical Coatings and Thin Films", April 27 – May 1st, (2009).

[3]. **Li-Wei Feng**, Chun-Yen Chang, Ting-Chang Chang, Chun-Hao Tu, Pai-Syuan Wang, Der-Shin Gan, New-Jin Ho, Hui-Chun Huang, Min-Chen Chen, "Study on Titanium oxinitride nanocrystals synthesized via magnetron sputtering and rapid thermal nitridation for nonvolatile memory applications" , International Conference on Metallurgical Coatings and Thin Films", April 27 – May 1st, (2009).

[4]. **Li-Wei Feng**, Ting-Chang Chang,Po-Tsun Liu,Chun-Hao Tu, Yung-Chun Wu, Che-Yu Yang, Chun-Yen Chang, "Application of Fluorine Doped Oxide (SiOF) Spacers for Improving Reliability in Low Temperature Polycrystalline Thin Film Transistors", International Conference on Metallurgical Coatings and Thin Films, April 28-May 2, (2008).

[5]. **Li-Wei Feng**, Ting-Chang Chang, Po-Tsun Liu, Shih-Ching Chen, Yung-Chun. Wu, Chun-Yen Chang, High performance nano-structure poly-crystalline thin film transistor with a O/N/O stacked gate dielectric, International Electron Devices and Materials Symposia, December 7-8, (2006).