國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

新穎反轉式及無接面多閘極多晶矽奈米線薄膜電晶體特性與應用的探討

An Investigation on the Characteristics and Applications of Novel Multiple-Gated Inversion-Mode and Junctionless Polycrystalline Silicon Nanowire Thin-Film Transistors

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中 華 民 國 一百零一 年 三 月

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摘要

本篇論文研究獨立雙閘極(independent double-gated)多晶矽奈米線薄膜電晶體操作於低汲極(drain)偏壓時，雙閘控制模式相對於單閘控制模式而言有較佳輸出電流的主要原因。實驗數據以及理論分析結果顯示，當多晶矽奈米線元件操作於雙閘模式控制之下，對於通道中晶粒邊界與缺陷所造成之位能障(grain-boundary potential barrier)具有較佳的調控能力，因而可獲得相較單閘操作下為佳的元件特性。

另一方面，本研究也探討將獨立雙閘極機制應用於 SONOS 記憶體元件中的可能性。由於獨立雙閘極 SONOS 記憶體元件具有兩個可以獨立操作的閘極，所以有兩種讀取模式可供選擇。論文中分析了兩種不同讀取模式對感測窗口大小(memory window)特性的影響。本論文製作的元件採用的雙閘極介電層分別為二氧化矽以及二氧化矽-氮化矽-二氧化矽堆疊層。當選用具二氧化矽-氮化矽-二氧化矽堆疊層為閘介電層之閘極當驅動閘極(driving gate)時，SONOS 記憶體元件具有比較大的感測窗口，但是，其大小與施加於輔助閘極的偏壓無關。根據這些分析，

本研究提出了幾種以無摻雜或重摻雜矽薄膜為通道且具獨立雙閘極之先進非揮發性記憶體結構，其主要特徵為具有一共用輔助閘來增進性能。

除了獨立雙閘極多晶矽奈米線薄膜電晶體外，運用全包覆式閘極(gate-all-around)無接面(junctionless)多晶矽奈米線薄膜電晶體的電流-電壓(I-V)量測，我們也發展了一個可用於檢測重磷摻雜多晶矽奈米線通道的活化摻雜濃度(active doping concentration)、遷移率(mobility)及分布於閘極介電層與通道間的表面二氧化矽閘極介電層電荷密度(interface oxide charge density)的量測方法。利用此方法獲得的重磷摻雜多晶矽奈米線通道特性分析結果與實施於平面無接面薄膜電晶體的電容-電壓(C-V)量測分析結果相當一致。相較於對重磷摻雜多晶矽塊材進行霍爾量測(Hall measurement)所獲得的分析結果，上述兩個方法皆顯示較低的活化摻雜濃度以及大量負的表面二氧化矽閘極介電層電荷密度。其主要原因推估為磷於二氧化矽閘介電層與多晶矽通道間介面的偏析(segregation)現象。

此外，考慮到無接面場效電晶體的實際應用，本研究也發展了一個理論模型，可用於描述雙閘極無接面場效電晶體的臨界電壓(threshold voltage)與次臨界電流(subthreshold current)。其計算結果顯示，此模型可以準確的描述雙閘極無接面場效電晶體導通通道長度從 100 nm 微縮至 22 nm 時，元件呈現的臨界電壓下降效應(threshold voltage roll-off effect) 。

除了探討一般的無接面場效電晶體，考量蕭特基位障(Schottky-barrier)電晶體於非揮發性記體元件的應用潛力，本研究也提出了一種新穎的非對稱蕭特基位障電晶體。此非對稱元件具備了蕭特基位障於源極(source)端，然而，其導通通道與汲極皆為重 n 型摻雜。計算結果顯示，其非對稱的特性使得此蕭特基位障電晶體顯示出單極(unipolar)的傳輸特性以及低的漏電流，但是其位於源極端的蕭特基位障也劣化了元件的輸出電流以及操作於擬次界區(pseudo-subthreshold region)的次臨界擺幅(subthreshold swing)。而此次臨界擺幅的劣化可藉由薄化導通通道以及閘

極介電層來獲得改善。除此之外，本研究也提出了修正的微縮長度(scaling length)“λ”概念，來描述導通通道以及閘極介電層的厚度對位於擬次界區的次臨界擺幅所產生的影響。

最後，本論文在全包覆式閘極反轉模式 (inversion-mode)多晶矽奈米線元件常溫量測中發現獨特的低於 60 mV/dec 的次臨界擺幅現象。其主要原因推估與下面兩項描述相關。第一、trap-assisted band to band tunneling (BTBT) current 於汲極端產生了大量的電洞，其中部分被擷取於晶粒邊界之缺陷所造成之能階狀態中。第二、後續當元件操作於次臨界區(subthreshold region)時，擷取的電洞被中和。然而，我們的量測數據顯示，當元件通道長度逐漸微縮或者包覆式閘極遭單閘取代時，此獨特現象將逐漸消失。

關鍵字：奈米線, 獨立雙閘極, 全包覆式閘極, 多晶矽, 薄膜電晶體, SONOS, 無接面, 蕭特基位障, SONOS, 低於 60 mV/dec 的次臨界擺幅。

An Investigation on the Characteristics and Applications of Novel Multiple-Gated Inversion-Mode and Junctionless Polycrystalline Silicon Nanowire Thin-Film Transistors

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Abstract

In this dissertation, we study the characteristics of independent double-gated (IDG) polycrystalline silicon (poly-Si) nanowire (NW) thin-film transistors (TFTs) with focus on the physical mechanism responsible for the superior output current under double-gated (DG) mode of operation over that under single-gated (SG) mode at a small drain voltage. The experimental data and theoretical analysis identify that the root cause is related to the more efficient modulation of grain boundary barrier height of poly-Si channels under DG mode of operation.

On the other hand, the feasibility of applying such IDG scheme to silicon–oxide–nitride–oxide–silicon (SONOS) flash memory is also explored. Two

different read modes can be adopted in such IDG poly-Si NW SONOS device with the two independent control gates. Special attention is paid to the analysis of memory window under different read modes. The fabricated device has oxide and oxide-nitride-oxide (ONO) stack as dielectrics for the two independent gates, respectively. Our analysis and experimental data show that a larger memory window is obtained when the gate with ONO stack as dielectrics is used as the driving gate. Moreover, the memory window of this mode is essentially independent of the bias applied to the auxiliary gate. Based on this finding, several novel IDG Flash structures with undoped or heavily doped silicon channels and a common auxiliary gate are proposed.

Next, based on the measured *I-V* characteristics of gate-all-around (GAA) poly-Si NW junctionless (J-less) TFTs, we develop a methodology capable of extracting the values of active doping concentration, mobility, and interface fixed charge density of the *in situ* phosphorous-doped poly-Si NW channel. The experimental results show lower value of active doping concentration as compared to that obtained from Hall measurements performed on blanket thin films. Moreover, a highly negative interface oxide fixed charge density is found as well. These measured properties of the heavily doped poly-Si NWs are compared with the results of C-V measurements performed on planar J-less transistors with an ultra-thin channel. Close agreement is obtained between

these two schemes. Segregation of phosphorous at gate oxide/NW interface is postulated to be the responsible mechanism for the observed phenomena.

In this dissertaton, we also develop an analytical model of threshold voltage (V_{th}) and subthreshold current for DG J-less transistors by solving the two-dimensional Poisson's equation. The V_{th} roll-off effect of DG J-less transistors with channel length from 100 to 22 nm can be well described through the proposed model as the channel thickness is thinned to 8 nm.

In addition, we also propose a new asymmetric n-channel SB transistor (ASSBT) which features SB only on the source side, while the channel and drain are both n^+ doped. Our calculation results show that such a device exhibits unipolar behavior and low off-state leakage current owing to the elimination of SB originally presenting on the drain side. However, aggravated subthreshold swing (SS) in the pseudo-subthreshold region and degraded output current are found because of the SB source. Based on the calculation results, the aggravated SS can be improved by thinning the thickness of silicon channel or gate oxide. A modified form of scaling length (λ) concept is introduced to describe the impacts of structural parameters and gate configurations on the SS characteristics in the pseudo-subthreshold region.

Finally, we report, for the first time, an abnormal phenomenon showing sub-60

mV/dec SS found in GAA inversion-mode (IM) poly-Si NW TFTs at room temperature. The responsible physical mechanism related to the trapping of excessive holes generated by the high trap-assisted band-to-band tunneling (BTBT) current and later recombination of these trapped holes when operating in the subthreshold regime is suggested. Moreover, the experimental data also indicate that such an unexpected phenomenon is relieved or even negligible with the decrease of channel length or the replacement of GAA configuration by a single-gated one.

Keywords: nanowire (NW), independent double-gated (IDG), gate-all-around (GAA), polycrystalline silicon (Poly-Si), thin-film transistor (TFT), silicon-oxide-nitride-oxide-silicon (SONOS), junctionless (J-less), Schottky-barrier (SB), sub-60 mV/dec SS.

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林　哲　民
誌於風城交大
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Chapter 1

Introduction

1-1 Overview of Nanowire Technology

Moore's law predicts the path at which the dimensions of transistors keep scaling down [1.1] for two important reasons. One is improving the speed of transistors to provide more efficient electronic products and the other is increasing the density of transistors on an integrated circuit to reduce the cost. Nowadays, the semiconductor industry has entered into the nano-scale era. As the device is shrunk down to such an aggressively scaled regime, dimensionality and size would play a critical role in determining the material characteristics, which are very different to those in the bulk materials. For example, the differences between interactions of electrons with two-dimensional (2D), one-dimensional (1D), and zero-dimensional (0D) systems are quite significant. In all of the aforementioned low-dimensional structures, 1D systems, such as nanowire (NW), would be the most spotlighted because it is the smallest dimensional structure that can efficiently transport mobile carriers, and thus could be utilized as a modal test platform to fundamentally understand the impacts of

dimensionality and size on electrical properties [1.2]. A NW is defined as a stripe-shaped material with cross-sectional diameter or feature sizes smaller than 100 nm. NWs inherently feature a large surface-to-volume ratio, one major factor that boosts the prosperous research activities conducted for many potential applications related to NWs in the past two decades, such as NW-based field-effect transistors (FETs) [1.3], switch devices [1.4], memory devices [1.5], nanowire probes [1.6], and sensors [1.7]. In this thesis, we pay special attention to the applications of NWs on FETs and memory devices. For FETs, to serve as the conducting channel of the devices, a NW with a large surface-to-volume ratio enables the high gate coupling efficiency, and thus improves the controllability from the gate to the conduction channel, to prevent the penetration of the drain lateral electric field; therefore, shows great immunity to short-channel effects (SCEs) [1.8]. For memory devices, compared to the conventional planar bulk devices, the adoption of NW also provides high programming/erasing efficiency as well as low operating voltage, and thus, power consumption can be efficiently saved [1.5].

1-1.1 Bottom-up and Top-down Approaches

The route of making nanowires can be roughly divided into two approaches, namely, top-down and bottom-up. For bottom-up approach, a number of methods, such as vapor-liquid-solid (VLS) [1.9], solid-liquid-solid (SLS) [1.10], molecular beam

epitaxy (MBE) [1.11], oxide-assisted growth [1.12] and so on, have been developed for a long while. As a matter of fact, bottom-up approach can also be applied to prepare NWs of other materials in addition to Si, such as III-V and II-VI compounds [1.13]. However, Si is still the most popular material in nowadays electronic industry. Therefore, next, we focus on the introduction of the preparation of silicon NW by bottom up approach.

Among the reported bottom-up approaches, VLS technique is the most prominent to synthesize silicon NWs. In 1964, silicon NWs synthesized by VLS have been proposed by Wager and Ellis in their classical article [1.14]. The growing mechanisms of a silicon NW by VLS method is schematically shown in Fig. 1-1, in which a liquid metal-Si alloy cluster, such as Au-Si, is exposed in a gaseous silicon precursor such as silane (SiH_4) and acts as the energetically favored site for absorption of gaseous silicon precursor on silicon substrate. The metal-Si alloy cluster supersaturates and grows a 1D silicon NW with feature size limited by the diameter of the liquid metal-Si alloy cluster. Although VLS method takes advantages of easiness and cheapness, the contamination of metal would be a potential concern. This can be addressed by oxide-assisted growth method, because it is free from the metal contamination; however, numerous defects contained in NWs limit the application in nanoelectronics [1.12]. For SLS, it also faces the challenge that the requirement to melting the catalyst is below the solvent boiling

point [1.10]. Moreover, regarding the practical application, the most serious issue for NWs prepared by bottom-up approach is how to be precisely aligned and positioned. On the other hand, top-down approach, usually employs advanced lithographic techniques, such as deep UV steppers [1.15] and electron beam (EB) writers [1.16], to generate NW patterns. In this regard, these tools typically use optical means to tightly control the alignment and positioning of the patterned structures. However, these cutting-edge lithography tools suffer from high-cost, and are usually not affordable by academic organizations. In addition, low throughput would be another serious issue for EB writing. Another candidate is nanoimprint [1.17] by impressing a reliable mode with sub-100-nm features into the resist, and then doing the pattern transfer to the underlying material by an anisotropic etching. However, most of the modes with sub-100-nm features are also defined by EB or complicated processing.

1-1.2 Approaches Developed by Our Group

Recently, our group have also proposed and demonstrated several innovative top-down procedures to fabricate poly-Si NWs. These methods adopt either the spacer etching technique [1.8], [1.18]~[1.20] or formation of nano-scale cavities for a poly-Si film to be embedded [1.21]~[1.22]. Feature size of the fabricated NWs can be precisely determined by carefully controlling the etching time for forming the side-wall spacers or

the cavities. For the latter approach, the nano-scale cavities are formed at the sidewalls of a protruding structure by selectively etching a sacrificial layer sandwiched between two nitride layers. The sacrificial layer can be an *in stiu* doped poly-Si or an oxide prepared by low-pressure chemical vapor deposition (LPCVD). The selective etching of the poly-Si is dry etching in nature and performed in a transformer-coupled plasma (TCP) reactor [1.21] with SF_6-based chemistry, while the etching of the oxide layer is done in a dilute HF solution [1.22]. Because of the adoption of top-down approach, these methods avoid the concerns encountered in the bottom-up approach, such as poor control of precise alignment and position, but maintain the inherent advantages of top-down approach. Throughout the fabrication, no expensive lithography tools (G-line or I-line only) are needed for the preparation of nano-scale poly-Si NWs. Therefore, these methods are simple and cost-effective. Moreover, they are reliable, reproducible as well as compatible with today's standard processing technologies, and thereby, suitable for practical manufacturing. Through a slight modification done in the process sequence, several kinds of multi-gated (MG) architectures, including Tri-gate [1.22], Gate-all-around (GAA) [1.22], inverse-T (IT) double-gate (DG) [1.23], independent double-gate (IDG) [1.24], can be easily incorporated in the device fabrication, as compiled in Fig. 1-2. These proposed MG poly-Si NW thin-film transistors (TFTs) have indeed shown the features of high on/off current ratio and low sub-threshold swing (SS)

[1.18]~[1.24]. Furthermore, the potentials to serve as an SONOS flash memory with excellent programming/erasing efficiency [1.22] as well as a sensor with high sensitivity [1.25] have also been demonstrated. In some of the previous works [1.23]~[1.24], devices with an independent double-gated (IDG) configuration were fabricated and characterized. Interesting performance enhancement under double-gated mode of operation as well as the feasibility in the application of SONOS flash memory have been reported [1.26]. On the other hand, the configuration of GAA has been employed to investigate the device characteristics of novel junctionless (J-less) transistors [1.27].

1-2 Overview of Multiple-Gated Devices

A successful design of metal-oxide-semiconductor field-effect transistors (MOSFETs) means the delivery of maximum driving output current (I_{on}) and the maintenance of acceptable off-current (I_{off}). Although a lower threshold voltage (V_{th}) is desired to achieve a higher output current, unfortunately, a greatly enhanced I_{off} is usually accompanied. This is an inevitable trend encountered as shrinking the feature size of MOSFETs [1.28]. Therefore, how to well control the V_{th} roll-off in aggressively-scaled MOSFETs is an important task to address. In terms of device architecture, the suppression of V_{th} roll-off of a conventional bulk planar MOSFET can be achieved by the scaling of gate oxide thickness (t_{ox}) as well as source and drain (S/D)

junction depth (X_j) and maximum depletion region width ($W_{dep,max}$) [1.29]~[1.30]. However, all of them are limited by some constraints. For $t_{ox,}$ the limitation is power consumption resulting from the unacceptable increment of gate leakage current with an ultra-thin gate oxide [1.31]~[1.32]. Replacing high-κ (κ: dielectric constant) materials for the gate dielectrics can mitigate such issue because the adoption of high-κ materials can further scale the equivalent oxide thickness (EOT) while keeping a sufficiently thick physical oxide thickness to suppress the gate leakage current [1.33]~[1.35]. However, the employment of high-κ dielectrics is facing a number of challenges and thus very difficult to be realized in practical production lines. These challenges include the inevitable existence of an interfacial layer which makes the actual EOT scaling difficult than expected [1.36], and mobility degradation due to the severe trapped charge-related scattering [1.37]~[1.38]. With respect to X_j, in the past two decades, numerous studies have been proposed to form extra shallow junctions, such as solid-phase epitaxial re-growth (SPER) [1.39] as well as plasma doping [1.40]~[1.41]. However, the accompanied concern is that too shallow an Xj leads to a high external parasitic resistance, and thus, degrading the output current [1.42]. Regarding $W_{dep,max}$, a shallow $W_{dep,max}$ can be achieved by the increment of channel doping concentration. However, the carrier mobility will be aggravated if the channel doping concentration is too high [1.43]~[1.44]. In short, all of the strategies listed above

are seriously limited; therefore, the employment of new three-dimensional (3D) device architectures to replace conventional bulk MOSFETs seems urgently needed. The first multi-gate (MG) device, called XMOS featuring double-gate (DG) configuration, was proposed by T. Sekigawa and Y. Hayashi in 1984 [1.45]. Five years later, the first fabricated DG device, called "fully Depleted Lean-channel TrAnsistor (DELTA)," was proposed and reported by D. Hisamoto *et al.* in 1989 [1.46]. About a decade later, D. Hisamoto and his colleagues [1.47] proposed a similar DG structure dubbed "folded channel transistor" built on an SOI substrate. This structure is a forerunner of the now famous FinFET structure [1.48]. Following these pioneering works, a number of versions of MG devices, such as tri-gate [1.49]~[1.50], omega-gate [1.51]~[1.53], Π -gate [1.54]~[1.55], gate-all-around (GAA) [1.56] were subsequently proposed and investigated. Fig. 1-3 compiles all of the cross-sectional views of the aforementioned MG devices. Nowadays, MG devices have been regarded as one of the most promising candidates for succeeding the conventional bulk planar CMOS because of the following advantages [1.57]: (1) Strong immunity against SCEs, (2) low junction leakage current (due to greatly reduced junction area), and (3) compatibility with today's standard CMOS manufacturing. Actually, MG FinFET devices are no longer just candidates for succeeding the planar CMOS. In mid-2011, Intel had announced that the tri-gated body-tied Si-fin structure would be employed in the next 22nm-node microprocessors

[1.58].

Next, we briefly elaborate the root causes why MG devices can mitigate the SCEs and promise the continuity of scaling sown. For a fully-depleted (FD) MG device, the SCEs is closely related to a parameter, Φ_{min}, which is the minimum potential through the whole conduction channel along the direction from source to drain. A sufficiently high potential barrier between S/D (*i.e.*, a small enough Φ_{min}) is desired to avoid the occurrence of punch-through or drain-induced barrier lowering (DIBL) in the channel. In addition, the $x_{min,}$ which corresponds to the location where the Φ_{min} occurs, serves as another index to approximately measure the SCEs. Here the x-direction is from source to drain and x = 0 is located at the drain/source junction. Therefore a smaller x_{min} means the location of Φ_{min} is closer to the source side, implying that more electric field encroachment from drain to the channel, and thus worse SCEs [1.59].

Next, we further introduce the concept of electrostatic scaling length, denoted as λ, which is contained in the relation between the Φ_{min} and x_{min} and is helpful for us to comprehend the SCEs of MG devices. For an FD SG device, the Φ_{min} and x_{min} can be expressed as [1.59]

$$x_{\min} \approx \frac{1}{2}L_g - \frac{\lambda}{2}\ln(\frac{\phi_d}{\phi_s}), \tag{1.2-1}$$

and

$$\Phi_{\min} \approx 2\sqrt{\phi_s \phi_d}\, e^{(-L_G/2\lambda)}, \tag{1.2-2}$$

respectively. L_g is the effective channel. ϕ_s and ϕ_d are the electric potentials at the source and drain (S/D) regions, respectively, if we assume that the doping concentrations of the S/D regions are heavy enough and no drop in electric potential occurs in the S/D regions. λ is defined as [1.59]~[1.60]

$$\lambda = \sqrt{(\varepsilon_{si} / \varepsilon_{ox}) t_{ox} t_{si}}, \tag{1.2-3}$$

where ε_{si} and ε_{ox} are dielectric constants of silicon and oxide, respectively, t_{ox} is the thickness of gate oxide, and t_{si} is the thickness of the Si channel. According to the aforementioned statements, the SCEs of MG devices can be improved by decreasing both Φ_{min} and x_{min}. Based on Eqs. 1.2-1 ~ 1.2-3, it can be achieved by the reduction of the electrostatic scaling length λ with either a thinner t_{si} or t_{ox}. However, as mentioned above, the scaling of t_{ox} is limited. Fortunately, concerns regarding the scaling of t_{si} can be released by the employment of an MG configuration. For DG devices, any of the two gates only has to control half of the silicon channel; therefore, the term t_{si} in Eq. 1.2-3 can be replaced by $t_{si}/2$ and electrostatic scaling length is equal to [1.59]~[1.60]

$$\lambda = \sqrt{(\varepsilon_{si} / \varepsilon_{ox}) t_{ox} (t_{si} / 2)}\,. \tag{1.2-4}$$

This means that, compared to SG devices, DG devices only need twice thick channel thickness to attain the same immunity to SCEs. Similar concept can also be extended to quadruple-gate devices, which feature four control gates, and thus, electrostatic scaling

length can be expressed as [1.61]

$$\lambda = \sqrt{(\varepsilon_{si} / \varepsilon_{ox}) t_{ox} (t_{si} / 4)}. \quad (1.2\text{-}5)$$

In short, with the same t_{si}, Eqs. 1.2-3 ~ 1.2-5 indicate that an MG device with additional control gates features a shorter λ, which results in a smaller Φ_{min} and x_{min} and, thus, improving the SCEs. However, MG devices, such as tri-gate or quadruple-gate, usually suffer from the "corner effect" which results from the premature inversion forming in the corners of the channel of MG devices [1.62]. In particular, such premature inversion results in a undesirable non-uniform turning-on phenomenon and kink presenting in the I_D-V_G characteristics in subthreshold region [1.62]. Therefore, preserving the feature of suppressing V_{th} roll-off while avoiding the undesirable "corner effect," the ultimate MG configuration is with a cylindrical channel completely surrounded by a common gate. Namely, the inherently symmetrical GAA configuration provides theoretically the best gate controllability to the channel potential and eliminates the undesired corner effect [1.63].

1-3 Overview of Junctionless (J-less) Nanowire Transistors

As continuing to scale down planar bulk CMOS, one of the most serious issues is the provision of abrupt and low-resistance junctions by implantation [1.42]. However,

compared to the conventional planar bulk CMOS, this task is even more challenging for the construction of three-dimensional MG devices [1.64]. The reason is simple: The conduction channel is not restricted to planar structure anymore. Taking the FinFET as an example, the conduction is mainly along the surface of the vertical sidewalls of the fin channel [1.65]. Therefore, a fin with aggressively high aspect ratio is desired to increase the output current conducting through a fin. The fin aspect ratio is defined as the ratio of fin height to fin width. By a conventional low-energy vertical implantation, a fin with high aspect ratio is in no way to achieve conformally-doped S/D extensions (SDEs) from the top of a fin to the bottom, as shown in Fig. 1-4(a). This issue can be addressed by a two-pass implantation with large titled angle [1.66], as shown in Fig. 1-4(b). By tilting the implantation, the whole sidewalls of the fin can be uniformly doped. However, such a tilted implantation suffers from severe dopant loss [1.67]. Fig. 1-4(c) illustrates the different dopant loss mechanisms in the tilted implantation, including the ions scattered to the opposite side of the fin, to the buried oxide, out from the top of the fin, and backscattered out from the incident side surface of the fin [1.67]. Besides, owing to the shadowing effect stemming from the adjacent tall resist layer, as shown in Fig. 1-4(d) [1.68], the implantation angle is restricted to 10° in 32nm-node and beyond [1.69]. According the simulation results reported by L. Pelaz *et al.* [1.67], for the low-energy implants with such a small implantation angle, backscattering causes

significant dopant loss along the sidewall of a fin and consequently results in non-conformal SDEs [1.67]. This would degrade the external parasitic resistance [1.67]. Moreover, even in the best case (implantation angle $\alpha = 45^{\circ}$), the conformal doping ratio of a fin (as defined by $C_{max\_top}/C_{max\_sidewall}$, where C_{max_top} and $C_{max\_sidewall}$ are the maximum doping concentrations of the top and sidewall of a fin, respectively) can only be 2 [1.69]. In this regard, new doping techniques such as plasma doping [1.69]~[1.70] or vapor phase deposition [1.71] will be useful skills for the realization of conformally-doped SDEs of FinFETs. However, the process controllability of these conformal doping methods has yet to be proven in mass production. Sputter erosion of the fins represents another major issue in the case of plasma doping [1.70].

The above concerns associated with the formation of SDEs of the FinFET can be effectively lifted with a novel transistor named "junctionless (J-less) NW transistor" proposed recently[1.72]~[1.74]. J-less NW transistors have their channel doping of the same type to that of the S/D, a feature quite similar to that of an accumulation-mode transistor. The major difference between the two types of devices is the much heavier doping concentration ($> 10^{19}$ cm^{-3}) in the channel of J-less NW transistors. In other words, the doping concentration is more or less homogeneous across S/D and channel in J-less transistors and no abrupt p-n S/D junctions are present in J-less transistors. This is the reason why the constraints related to forming abrupt and uniform SDEs in

conventional inversion-mode (IM) devices can be released. Additional intriguing features associated with the J-less scheme include the reduction of the degradation of mobility from surface scattering [1.75], and 3) excellent performance for RF application [1.76].

The concept of J-less NW transistors became popular after the proposition by J. P. Colinge *et al.* in 2009 [1.72]. Actually, a similar concept can be traced back early to a paper proposed by S. Cristoloveanu *et al.* in 1992 [1.77], in which a transistor named "Point-Contact Pseudo-MOSFET" was proposed, featuring no S/D extensions as well. Actually, the original purpose of "Point-Contact Pseudo-MOSFET" was to serve as a test vehicle for a new methodology employed to determine the characteristics of as-grown SOI wafers.

Considering the heavily-doped channel ($1x10^{19}$~$1x10^{20}$ cm^{-3}), J-less transistors reported to this date usually feature an MG configuration and a NW channel in order to effectively turn off the conduction in the off-state. To maintain a reasonable threshold voltage (V_{th}), a gate electrode featuring a high work-function difference between gate electrode and conducting channel (typically about 1V) is employed [1.72]. Although, at first glance, the basic device characteristics of J-less NW transistors, such as I_D-V_G and I_D-V_D characteristics, are similar to those of IM transistors, their operation mechanisms are quite different owing to the particularity of the heavily-doped channel. Figures 1-5(a)

and (b) schematically compare the difference in transfer characteristics of fully-depleted SOI n-type IM and J-less NW transistors. As shown in Fig. 1-5(a) for an IM transistor, the device operated in the subthreshold region features weak inversion until the gate voltage reaches V_{th}. A further increase in gate voltage pushes the surface potential of the channel into the condition of strong inversion and a surface inversion layer is accordingly formed underneath the gate insulator [1.78]. On the other hand, as shown in Fig. 1-5(b) for an FD n-type J-less NW transistor, the body of the channel is depleted as gate voltage is below the threshold voltage. As gate voltage increases to V_{th}, the peak electron concentration increases and approaches N_D, the doping concentration of the channel. [1.79]. As gate voltage further increases, the portion of the quasi-neutral region (*i.e.*, region with $n = N_D$) in the channel increases and eventually the whole channel becomes neutral, corresponding to the flat-band condition, *i.e.*, $V_G = V_{FB}$. Next, Figs. 1-6(a) and (b) compare, respectively, the distribution of the electrons in the channel of n-type DG IM and J-less NW transistors as both devices are turned on. For J-less NW transistors, Fig. 1-6(b) depicts that most of the electrons are away from the interface between gate insulator and channel, thus reducing the scattering events occurring at the gate insulator/channel interface. This is in contrast to the situation shown in Fig. 1-6(a) for the IM device, and is helpful in promoting the field-effect mobility of J-less NW transistor [1.75]. However, the depleted channel space between transport carriers and

the gate insulator tends to increase the EOT of the J-less NW transistor [1.79]. It would become a potential concern of J-less NW transistors for further scaling.

In addition to serving as the basic building blocks for logic circuits, J-less NW transistors are also suitable to be applied in Flash memory technology, especially in future 3-D multi-stacking integration. With the adoption of the *in situ* doping process, the high thermal budget associated with the formation of implanted S/D junctions can be eliminated. Recently, several kinds of J-less-based Flash memory devices with acceptable memory characteristics, such as reasonable programming/erasing efficiency, endurance, and data retention, have been proposed and investigated [1.80]~[1.83]. In terms of NAND Flash memory application, one more advantage of J-less NW transistors is the superior low series resistance due to the heavy and homogenous doping concentration through S/D and channel. In nowadays aggressively-scaled NAND Flash memory, the S/D region of NAND Flash memory devices is sometimes undoped [1.84] and, thus, degrading the current flowing through the string of NAND Flash. It can be expected that such an issue can be much relaxed by the employment of J-less NW transistors due to the heavily-doped channel and S/D.

1-4 Overview of Schottky-barrier (SB) MOSFETs

A Schottky-barrier (SB) MOSFET is an MOSFET in which the doped silicon

source and/or drain is replaced with a metallic (typically silicided) source/drain. The concept of SB MOSFETs can be traced back to an early Japanese patent proposed by Nishi in 1966 [1.85]. Shortly, the first fabricated p-channel SB MOSFET utilizing PtSi for S/D was proposed in a paper reported by Lepselter and Sze in 1968 [1.86]. However, until 1980s', the first surge of SB MOSFETs has included the first introduction of fabricated n-channel SB MOSFETs [1.87] as well as the asymmetric SB MOSFETs [1.88] and the devices employing S/D channel interfacial layers [1.89]. Until now, state-of-the-art SB-MOSFETs have significantly advanced and been regarded as a potential candidate for aggressively scaled logic devices [1.90] and Flash memory devices [1.91].

For the application of logic circuits, one of the advantages of SB-MOSFETs is the low sheet resistance of the metallic S/D material. Nonetheless, a high contact resistance may present at the SB junction unless a silicide or metal with SB height (SBH) less than 0.1 eV or even a negative value is used [1.90]. In addition, for the scaling of conventional MOSFETs, in order to maintain a reasonable V_{th} roll-off, the implementation of complex techniques, such as shallow S/D extensions and halo implantation, is essential. In this regard, the depth of silicided S/D can be well and easily controlled by the deposited metal thickness as well as annealing temperature and duration; thus, greatly simplifying the fabricating process as compared with that of

conventional MOSFETs. Furthermore, the low process temperatures (typically below 600 ℃) promise the incorporation of high-κ dielectric and metal gate, considering the elimination of the general reliability issues associated with the high temperature annealing steps for activating the ultra-shallow S/D junctions [1.90]. In the meantime, such a low thermal budget is also helpful for better control in uniformity and reliability of device characteristics as applied in the fabrication of 3D integrated circuits [1.92].

On the other hand, in terms of the scaling in NOR-type Flash memory, one of the most challenging issues is the reduction of programming voltage applied to the drain side [1.93]. In order to achieve channel hot carrier programming, a voltage of more than 3.2 V from drain to source is essential in order to overcome the Si-to-SiO_2 barrier height [1.94]. The irretrievable punch-through effect resulting from such a high programming voltage limits the scaling of channel length [1.93]. In this regard, recently, the SB MOSFET-based non-volatile flash memory devices have drawn particular attentions because their Schottky barrier can strongly enhance the generation of hot carriers, and thus, a highly efficient source-side injected gate current can be generated at a relatively low drain voltage [1.91], [1.95]~[1.97]. Namely, a low-voltage but high-speed programming can be indeed achieved. Such a unique programming mechanism can be understood by the comparison of band diagrams of conventional and SB MOSFETs, as shown in Fig. 1-6. The intrinsic sharp band bending of SB MOSFETs at the source side

attributes to a large lateral electric filed, and therefore, the programming voltage applied to the drain side can be efficiently reduced [1.91].

Nevertheless, SB MOSFETs usually exhibit two drawbacks. One is the inferior on-state performance [1.98]~[1.100] and the other is the inherent ambipolar characteristics [1.101]. Regarding the degradation of output current, the root cause is that the SB presenting at the source junction impedes the current tunneling through the SB. The strategies used to increase the efficiency of transport current tunneling through SBH can be generally divided into two camps. The first camp focuses on the reduction of the SBH. Generally, the silicided S/D with SBH less than 0.1 eV or even a negative value is suggested to obtain comparable current drivability to that of the conventional MOSFETs [1.90]. To date, the reported lowest SBH is around 0.2 eV for PtSi, a suitable candidate for p-channel SB MOSFETs, and 0.27-0.36 eV for ErSi or YbSi, suitable candidates of n-channel devices [1.90]. These values are actually not low enough for practical demand. Moreover, the fabrication is more challenging for n-channel devices, since Er and Yb are both earth-rare materials and easy to get oxidized. Several schemes, such as dopant segregation technique [1.102], increasing the substrate doping [1.103] or inserting an ultra-thin (sub 1-nm regime) insulator between silicon and silide [1.104], were proposed and investigated to reduce the SBH. The aforementioned techniques can lower the effective SBH to about 0.1 eV and thus, have the potential to provide a

comparable driving current to that of conventional MOSFETs. Finally, the second camp comes up with the optimization of the architecture of SB MOSFETs. Two potential candidates are suggested. One is the use of an extra-thin channel [1.98]~[1.99] and the other is the adoption of an MG configuration [1.105]. For the former case, Si nanowires are promising to serve the purpose. Regarding the MG configurations, GAA has been indentified as an ideal MG one, which can provide the strongest control to the channel potential [1.63]. Actually, it has been convinced that the employment of Si nanowire combined with the GAA configuration can efficiently modulate the width of SBH, and thus, makes the SB more transparent and improves the injection of carriers through the SB [1.105].

Another major issue associated with the SB MOSFETs is the ambipolar conduction behavior which becomes significant as the SBH at the drain junction for minority carriers is not high enough. Such a bias-dependent minority-carrier current injecting through the drain-side SB may induce a large off-state GIDL (gate-induced drain leakage)-like current and form V-shaped I_D-V_G curves of the SB MOSFETs [1.106]. Such inherent ambipolar characteristic is urgently needed to be eliminated no matter for logic or memory devices. Certainly the large off-state leakage current would worsen the power consumption issue. For a flash memory device, such an ambipolar characteristic would make confusions as determining the storage state of an

SB-MOSFETs memory device because of the particular V-shaped I_D-V_G characteristics [1.107]. One of the feasible strategies to overcome such a concern is the adoption of asymmetric SB-MOSFETs [1.88]. This scheme replaces the metallic drain with an n^+ (p^+)-doped semiconductor junction for n-type (p-type) devices while retains the SB source. The ambipolar behavior is effectively suppressed and becomes unipolar owing to the elimination of the injection of minority carriers from the drain side. However, such approach suffers from more complex fabrication because one more mask and additional process steps are needed to form the asymmetric S/D structure [1.88]. Another approach, featuring an electrical drain extension induced by a metal field-plate (or a sub-gate) in a SB MOSFETs, was proposed by our group previously [1.106]. By applying a suitable voltage bias to the metal field-plate, the electrical drain extension in the active silicon layer can be induced and effectively suppressed the GIDL-like leakage current. Therefore, unipolar behavior can be successfully achieved. Although no extra mask is needed because metal field-plate (*i.e.*, sub-gate) could be formed during the metal interconnect step, this approach mainly suffers the degraded current drive due to the high parasitic resistance contributed by the electrical extensions.

1-5 Overview of Devices with Sub-60 mV/dec Subthreshold Swing (SS)

In the past two decades, several kinds of devices featuring sub-60 mV/dec subthreshold swing (SS) at room temperature were proposed and investigated, such as tunneling field-effect transistors (TFET) [1.108], impact-ionization metal-oxide-semiconductor field-effect transistors (I-MOS) [1.109], and silicon-on-insulator (SOI) devices caused by latch-up phenomenon [1.110]. All of their operational mechanisms are not thermionic emission, which dominates the operational mechanism in subthreshold region of conventional MOSFETs and thus, sub-60 mV/dec SS can be possibly achieved in these devices.

For n-channel TFET, which is basically a gated p-i-n diode under reverse biased as shown in Fig. 1-8, band-to-band tunneling is utilized as a source carrier injection mechanism to turn on the device. In the off-state, as the band diagram shown in Fig. 1-8(a), the potential barrier for valence-band electrons between source and the channel is so high so only a very small leakage current conducts. Next, as shown in Fig. 1-8(b), when gate voltage is sufficiently large so that the channel surface is inverted and a strong band bending develops across the source junction. Under such a condition, the strong field at the junction would trigger the band-to-band tunneling process, that is, an amount of electrons would tunnel from valence band in the source to conduction band in the channel. Since the above action is triggered all of a sudden when the gate voltage is increased, hence sub-60 mV/dec can be achieved.

For an n-channel I-MOS, as shown in Fig. 1-9, which is a partially-gated p-i-n diode under reversed biased. Different from TFET, the modulation of the breakdown voltage in the non-gated i-region is utilized to switch the device from the off- to on-state. In off-state, as shown in the band diagram (Fig. 1-9(a)), no sufficient energy can be provided to the electrons in the source side for impact-ionization. As a result, the off-state current of I-MOS is also limited by leakage current of the p-i-n diode under reversed bias. Next, as shown in Fig. 1-9(b), the gate voltage is increased to a condition that the electric field in the non-gated i-region is sufficiently large to cause significant impact ionization which may then lead a high conduction current. Therefore, a steep sub-60 mV/dec SS can be found. For latch-up phenomenon found in n-channel partially-depleted SOI devices, the root cause of sub-60 mV/dec SS depends on two feedback mechanisms. As shown in Fig. 1-10, when the applied bias condition is able to trigger impact ionization inside the channel, accumulated holes in the floating-body region would tend to forward bias the body-to-source diode, and thus, leading to a sudden lowering in threshold voltage. Consequently the drain current increases. Meanwhile, a parasitic n^+(drain)-p^+(accumulated holes)-n^+(source) BJT is also formed and breaks down the device; thus, sub-60 mV/dec SS can be achieved.

Recently, an unexpected sub-60 mV/dec SS is also found in our GAA poly-Si NW TFTs. However, the aforementioned mechanisms for TFET, IMOS, or latch up

phenomenon are all not suitable to explain the finding. Therefore, in this thesis, we comprehensively investigate such an interesting phenomenon and propose a qualitative model to explain it.

1-6 Motivation

Since Si NWs have shown great potential in a variety of applications and are attractive to serve as an ideal building block for future extremely-scaled electronics, it is worth developing a reliable and reproducible process to fabricate high-performance NW devices. To cope with the issues mentioned in Sec. 1-1-1 for either bottom-up or top-down approaches, our group (Advanced Device Technology Laboratory) has developed several innovative methods for fabricating poly-Si NW thin-film-transistors (TFTs) featuring several kinds of MG configurations, such as ITDG [1.20], IDG [1.21], and GAA [1.22]. All of them feature the following merits: (1) Easy and low-cost fabrication process, (2) precisely-controlled NW's size, (3) accurate positioning, (4) self-aligned source/drain and NW formation, and (5) compatibility with today's standard CMOS processing technologies. However, one of the potential concerns of poly-Si NW TFTs is the defects contained in the granular poly-Si channel, which provoke undesirable potential barriers and lead to deteriorated ON-state current drive. Our previous work indicates that the height of the unavoidable potential barrier provoked by

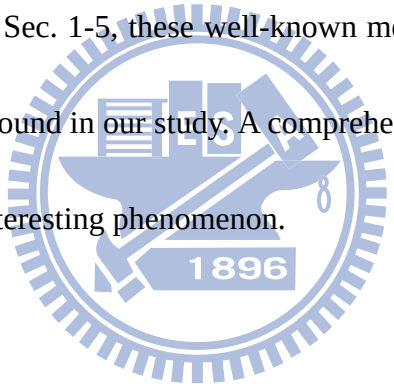
grain-boundary defects in the poly-Si channel can be efficiently modulated by MG control [1.23], although the associated mechanism is still not clear. In this thesis, the IDG poly-Si NW TFT featuring rectangular NW channels developed by our group [1.21] is utilized to study such phenomenon. Adoption of such a device is because of its regular shape of NW's cross section which makes the analysis easier and more accurate. In addition, it also can be applied to study the characteristics of IDG SONOS devices, which have shown promising potential to address the undesirble issue of "read disturb" in conventional singe-gate NAND Flash devices by reading the devices from a back-gate [1.111].

On the other hand, J-less transistors have also shown promising potential for deca-nanometer logic devices and flash memory devices, as stated in Sec. 1-3. Nonetheless, very few works were reported on extraction of electrical parameters and modeling of the J-less transistors. Therefore, we undertake studies to investigate the characteristics of J-less transistors, including the development of a novel methodology to extract the active doping concentration of heavily-doped NW channel of GAA J-less TFTs, as well as an analytical model of V_{th} and subthreshold current of DG J-less transistors.

As mentioned in Sec. 1-4, SB-MOSFETs possess several intriguing features, such as low parasitic resistance and low-temperature process. How to combine the

advantages pertaining to either J-less-transistors or SB-MOSFETs is an interesting topic and worth studying. In this regard, we propose and investigate a novel asymmetric SB MOSFETs featuring metallic silicided source and heavily doped channel and drain by the aid of TCAD.

Finally, an unexpected sub-60 mV/dec SS is found in GAA poly-Si NW TFTs at room temperature. Although there have been many reports on sub-60 mV/dec characteristics, such as TFET [1.108], I-MOS [1.109], latch-up effect [1.110] found in SOI devices, as reviewed in Sec. 1-5, these well-known mechanisms cannot be applied to explain the phenomenon found in our study. A comprehensive investigation is needed for understanding such an interesting phenomenon.



1-7 Thesis Organization

Eight chapters are contained in this dissertation. Background and motivation are described in Chapter 1. In Chapter 2, results and analysis regarding particular performance enhancement under DG control in IDG poly-NW TFTs are given. Chapter 3 models and experimentally verifies the unique read characteristics associated with the IDG poly-NW TFT SONOS devices. Chapter 4 firstly presents a novel methodology for extracting the carrier concentration and mobility of heavily-doped poly-Si NWs with J-less transistor structures. Chapter 5 develops an analytical model of V_{th} and SS for DG

J-less transistors. Chapter 6 comprehensively investigates the device characteristics of a novel n-type asymmetric Schottky-barrier transistor (ASSBT) with silicided Schottky-barrier source and heavily n-doped channel and drain. Chapter 7 comprehensively studies the abnormal Sub-60 mV/dec SS found in GAA poly-Si NW transistors. In Chapter 8, major achievements and summary are stated, and suggested future works are listed. Detailed content of the following chapters are specified as follows:

In Chapter 2, IDG poly-NW TFTs are adopted to experimentally and theoretically elucidate the root cause of device performance enhancement under double-gate control.

In Chapter 3, taking advantages of the more operational flexibilities provided by two independently-biased gates, IDG poly-NW TFTs can serve as a good test vehicle to study the reading characteristics of SONOS devices with various operation modes and investigate the potential of the IDG configuration in the related application.

In Chapter 4, the other architecture of poly-Si NW TFTs featuring GAA configuration is utilized to fabricate the novel GAA *in-situ* doped poly-Si NW J-less transistors. Moreover, this kind of J-less transistors is adopted to develop a new methodology to probe the active doping concentration and mobility of heavily *in-situ* phosphorous-doped poly-Si NWs.

In Chapter 5, an analytical model of V_{th} and subthreshold current for DG J-less

transistors is developed, which can precisely describe the V_{th} roll-off and subthreshold current even as the channel length is scaled to 22 nm.

In Chapter 6, a novel n-type asymmetric Schottky-barrier transistor (ASSBT) with silicided Schottky-barrier source and heavily n-doped channel and drain is investigated by the aid of 2D TCAD simulation tool [1.112]. The particular operational mechanisms shown in transfer characteristics are investigated. Moreover, as such devices are operated in the region where its operational mechanism is dominated by thermionic field-emission, a modified scaling length "λ" corresponding to the nature of thicker EOT of transistors featuring heavily-doped channel, as mentioned in Sec. 1-3, is employed to describe the degradation of SS.

In Chapter 7, GAA poly-Si NW TFTs are fabricated and characterized. Specifically, under specific applied drain and gate voltage biases, an interesting phenomenon related to sub-60 mV/dec SS is found. Trapping of the excessive holes during the off-state conduction in the poly-Si NW channels is proposed to be responsible for such a phenomenon.

Chapter 8 summarizes the results and contributions made in this dissertation and provides suggested items for future works.

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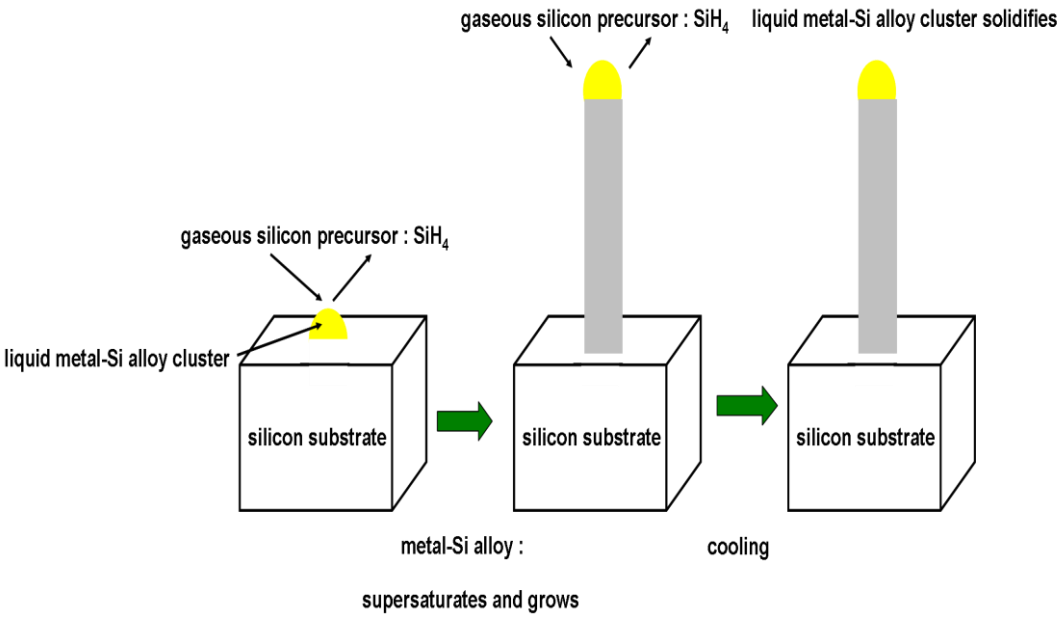


Fig. 1-1 Growth mechanism of silicon nanowires by means of vapor-liquid-solid (VLS) approach [1.14].

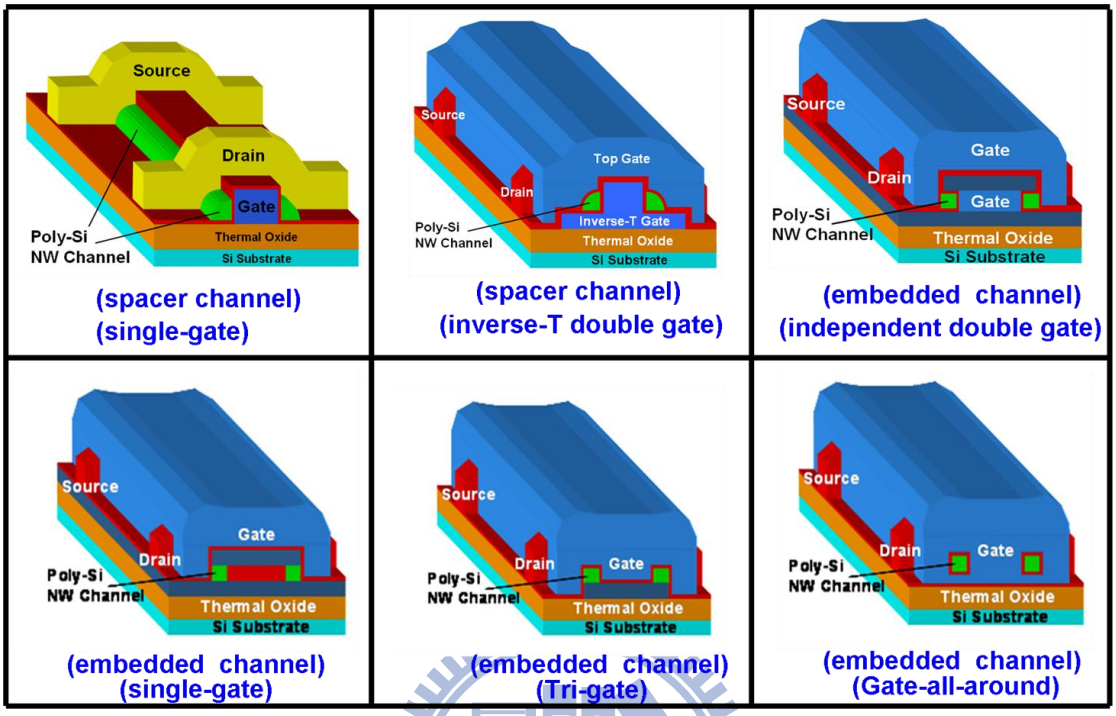


Fig. 1-2 Compilation of several kinds of multi-gated (MG) poly-Si nanowire (NW) thin-film-transistors (TFTs) developed by our group.

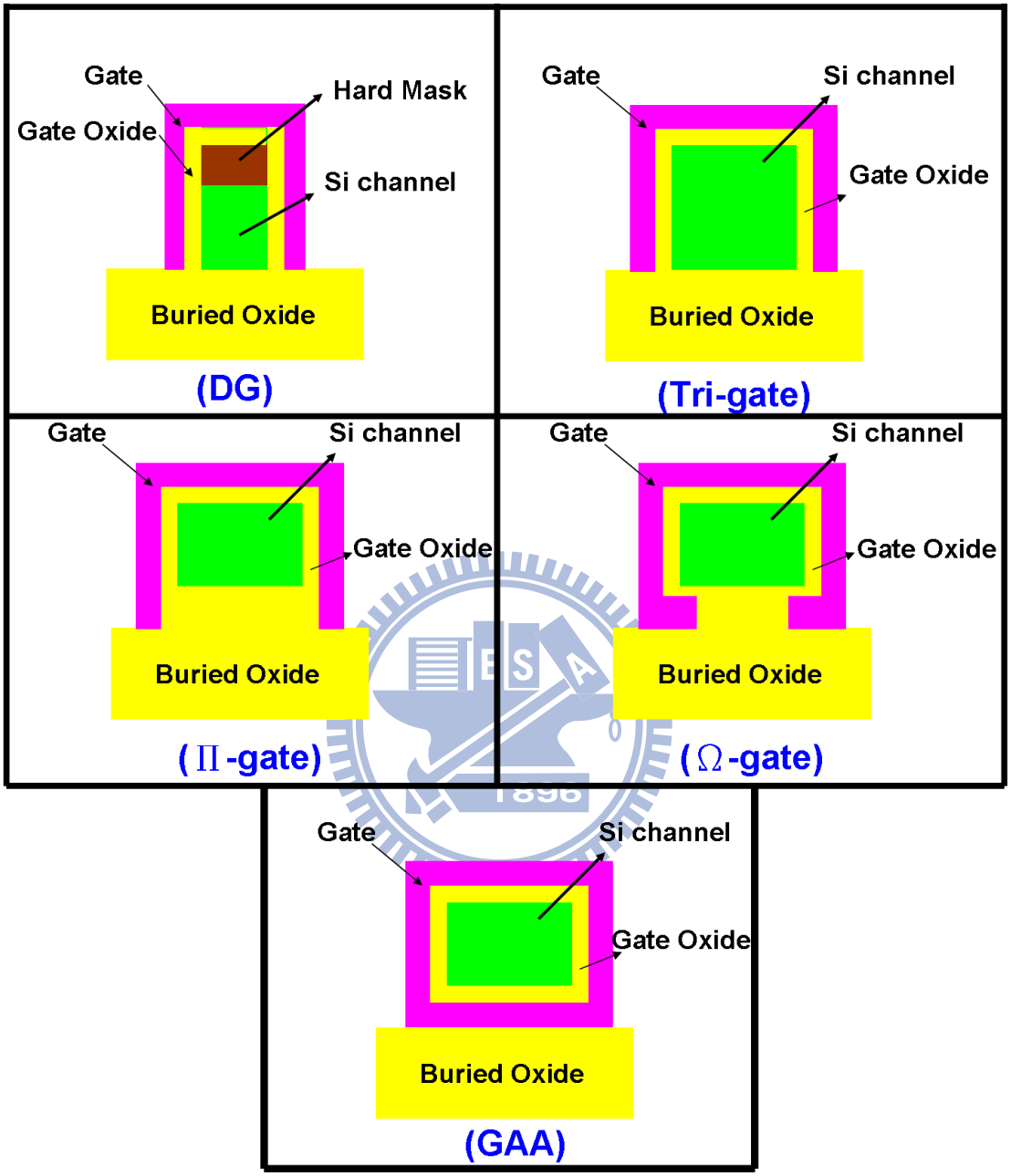


Fig. 1-3 Schematic cross-section of several kinds of multi-gated (MG) FinFETs, including DG, Tri-gate, Π-gate, Ω-gate, and GAA.

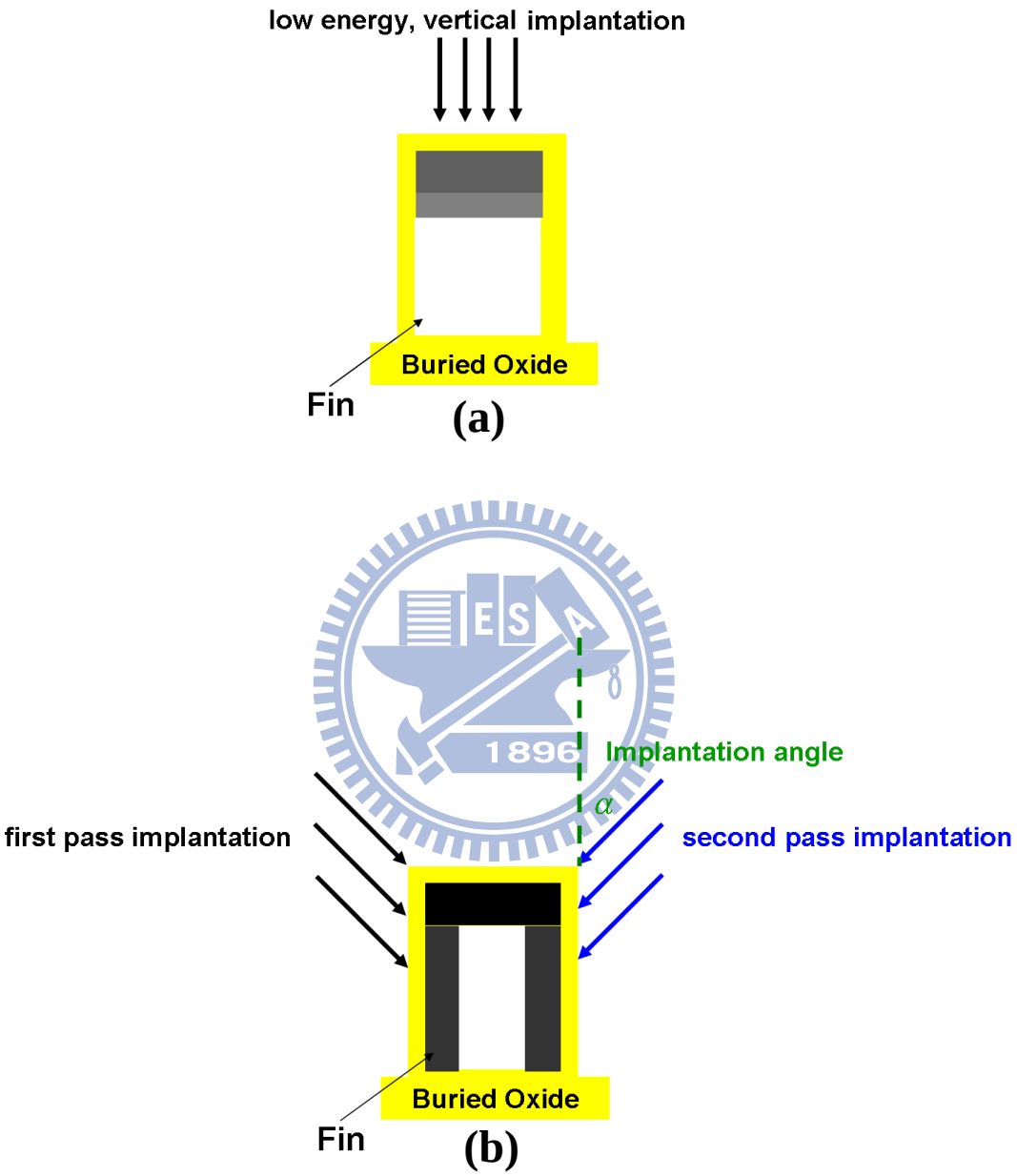
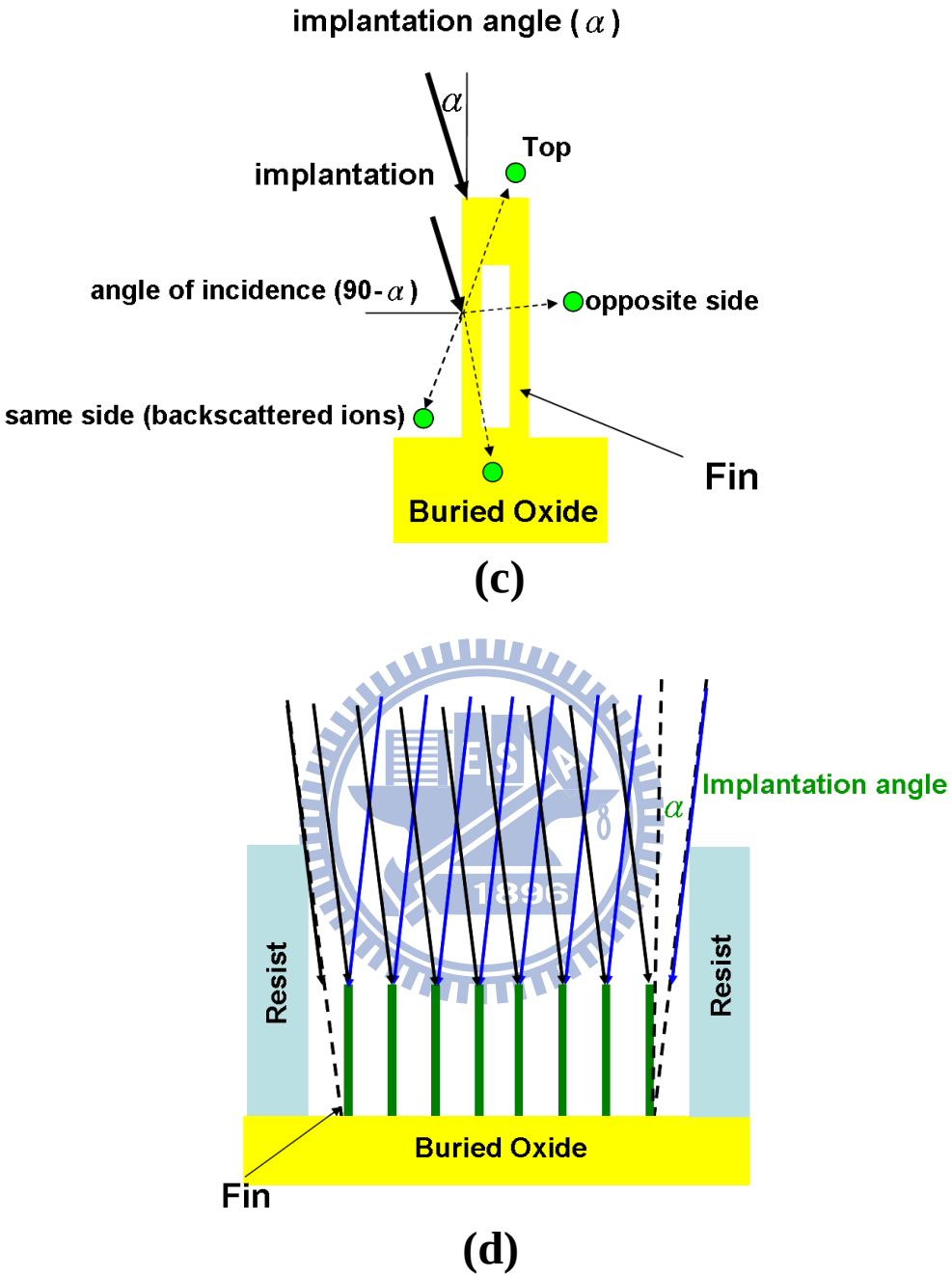


Fig. 1-4 Distribution of doping concentration in fin by (a) low-energy vertical implantation and (b) two-pass tilted implantations. The darker region means heavier doping concentration. (c) Different dopant loss mechanisms indicated by the dash arrowheads in the tilted implantation [1.67]. (d) Restriction of implantation angle owing to the shadowing issue due to the physical height of adjacent resist.



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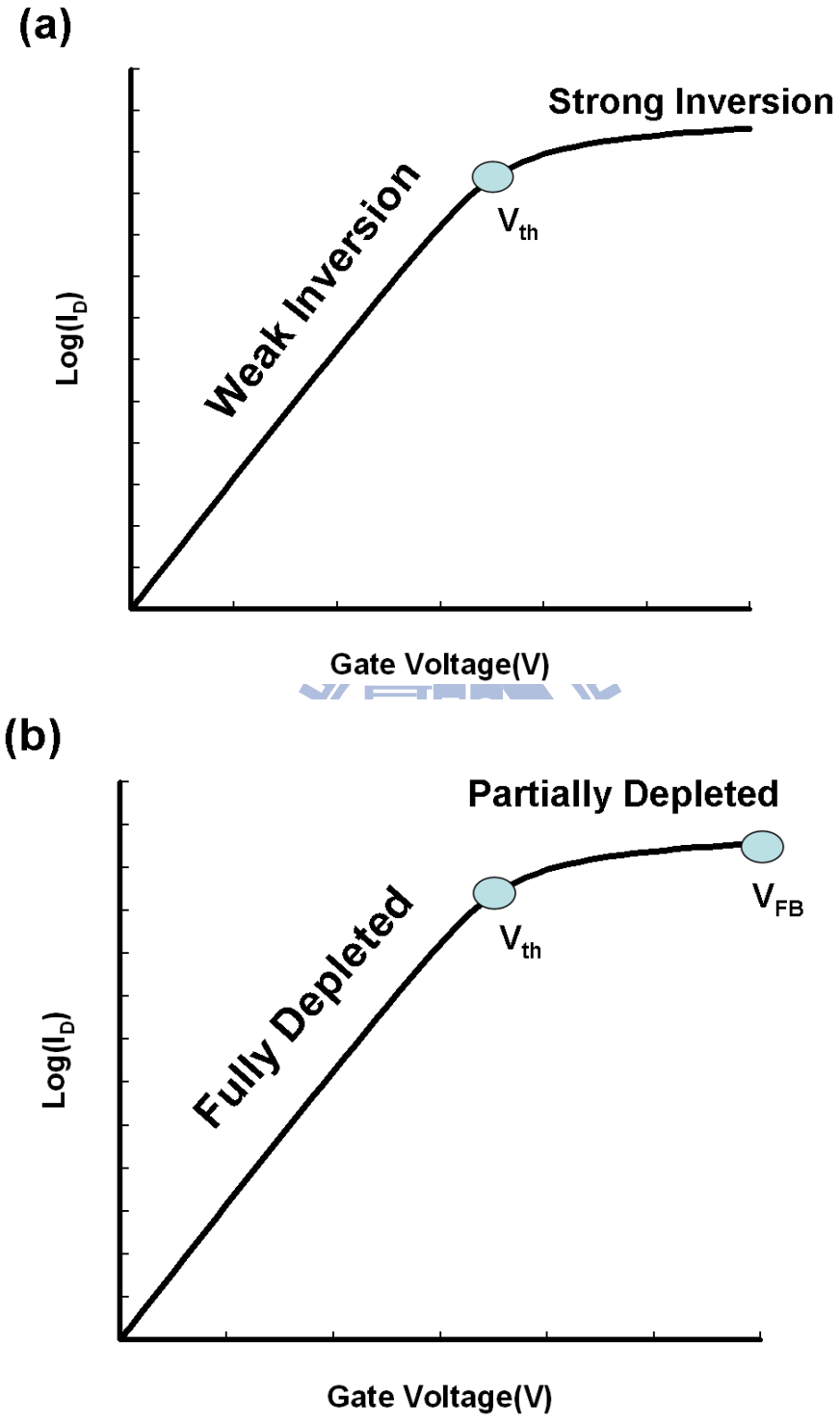

Fig. 1-5 Comparison of I_D-V_G characteristics of (a) n-type inversion-mode (IM) and (b) n-type junctionless (J-less) NW transistors [1.79].

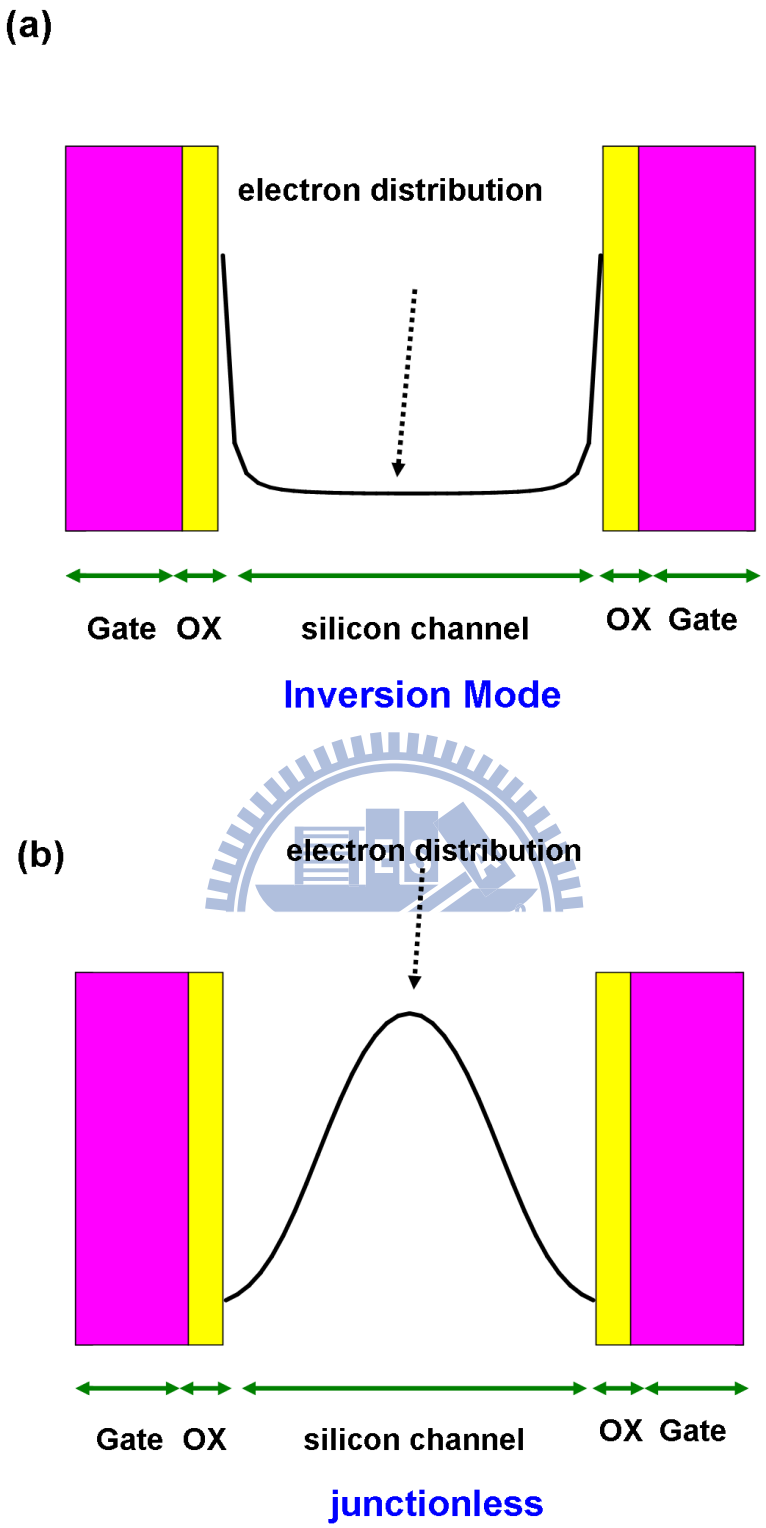

Fig. 1-6 Distribution of electron density in (a) DG n-type inversion-mode (IM) and (b) DG n-type junctionless (J-less) NW transistors along the direction perpendicular the carrier transport.

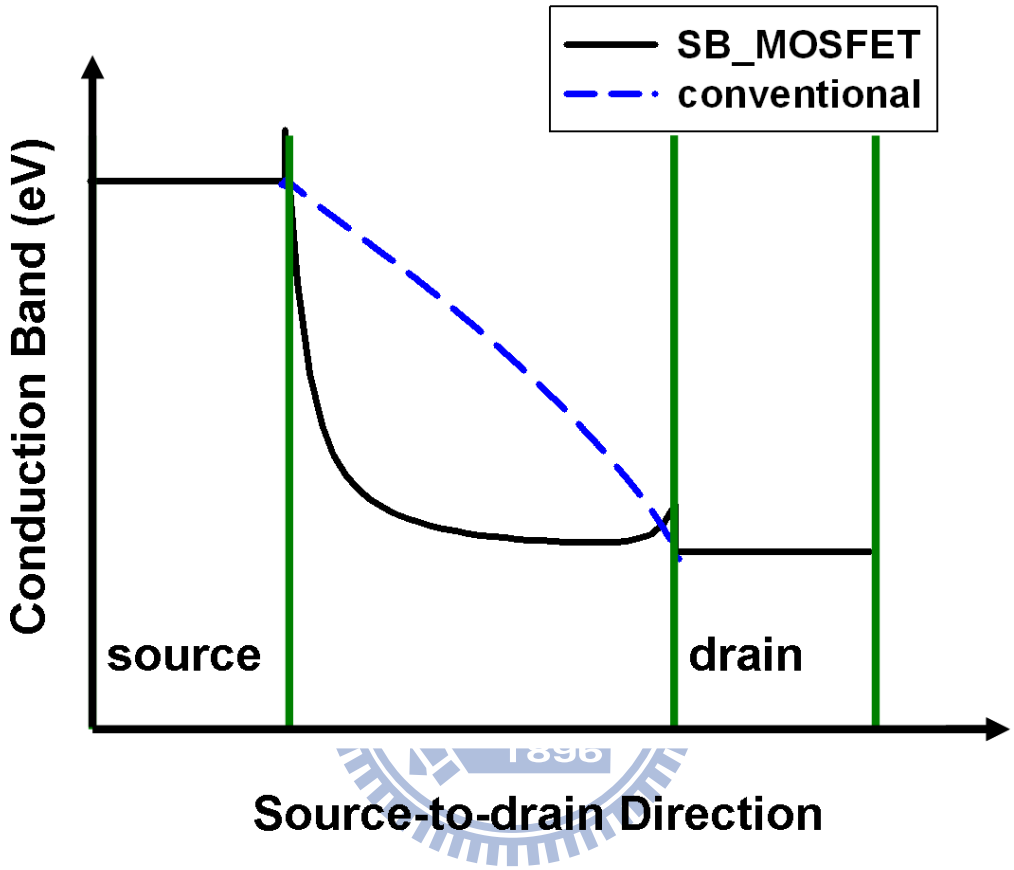

Fig. 1-7 Comparison of conduction band energy of SB and conventional MOSFETs. The particular abrupt drop near the source of the SB MOSFETs results in the efficient generation of hot carriers.

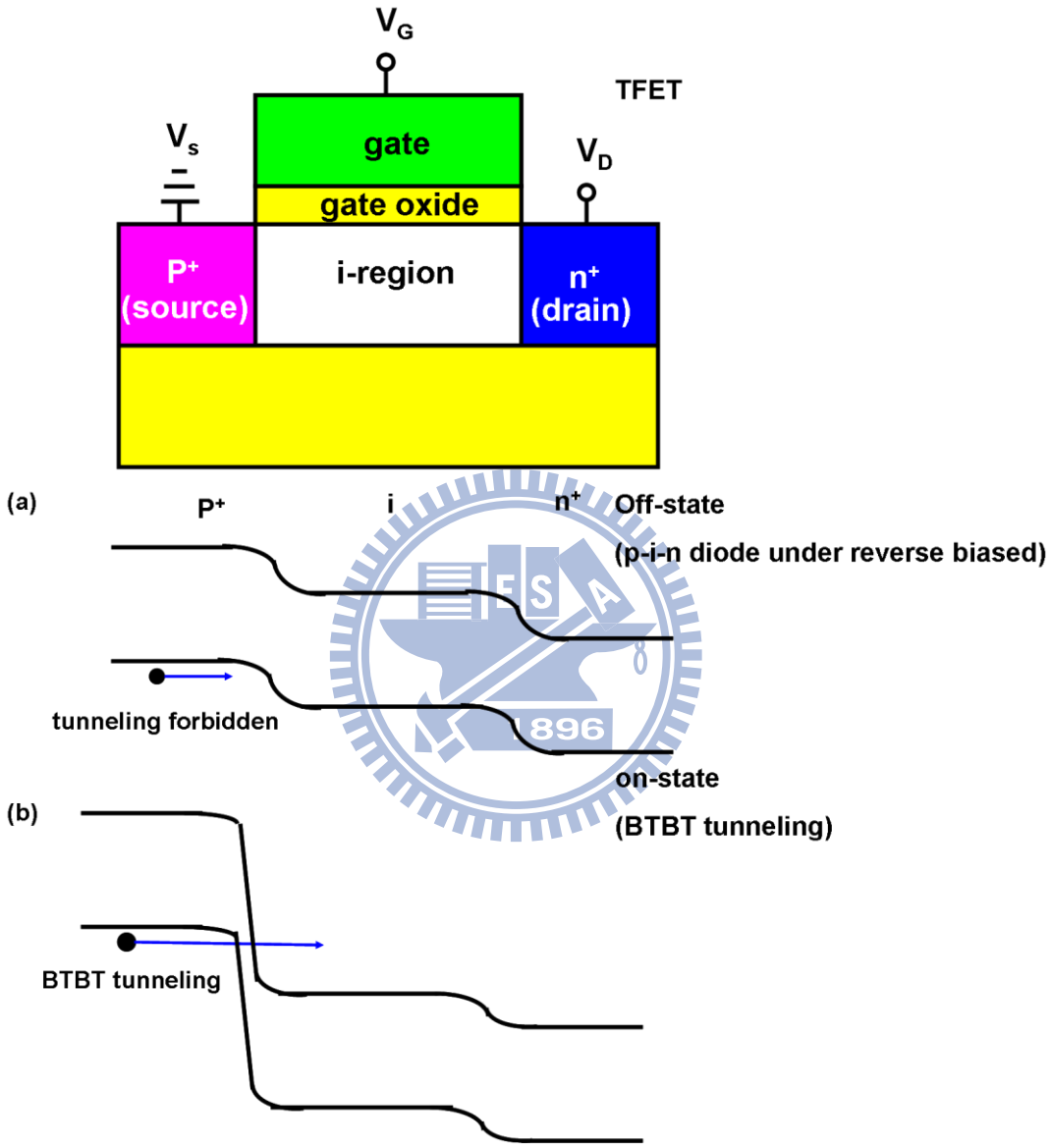

Fig. 1-8 Band diagrams of an n-channel TFET in (a) off and (b) on state, respectively.

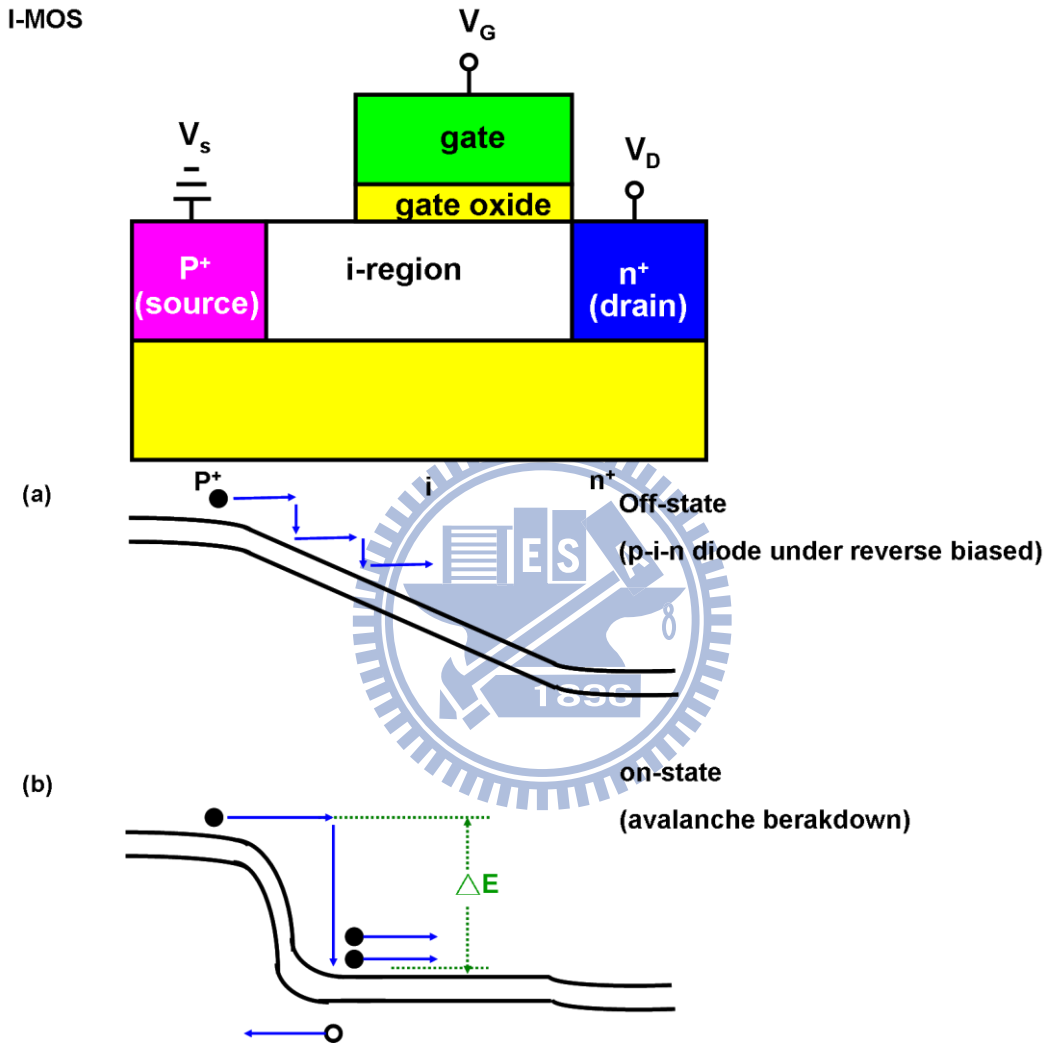

Fig. 1-9 Band diagrams of an n-channel I-MOS in (a) off and (b) on state, respectively.

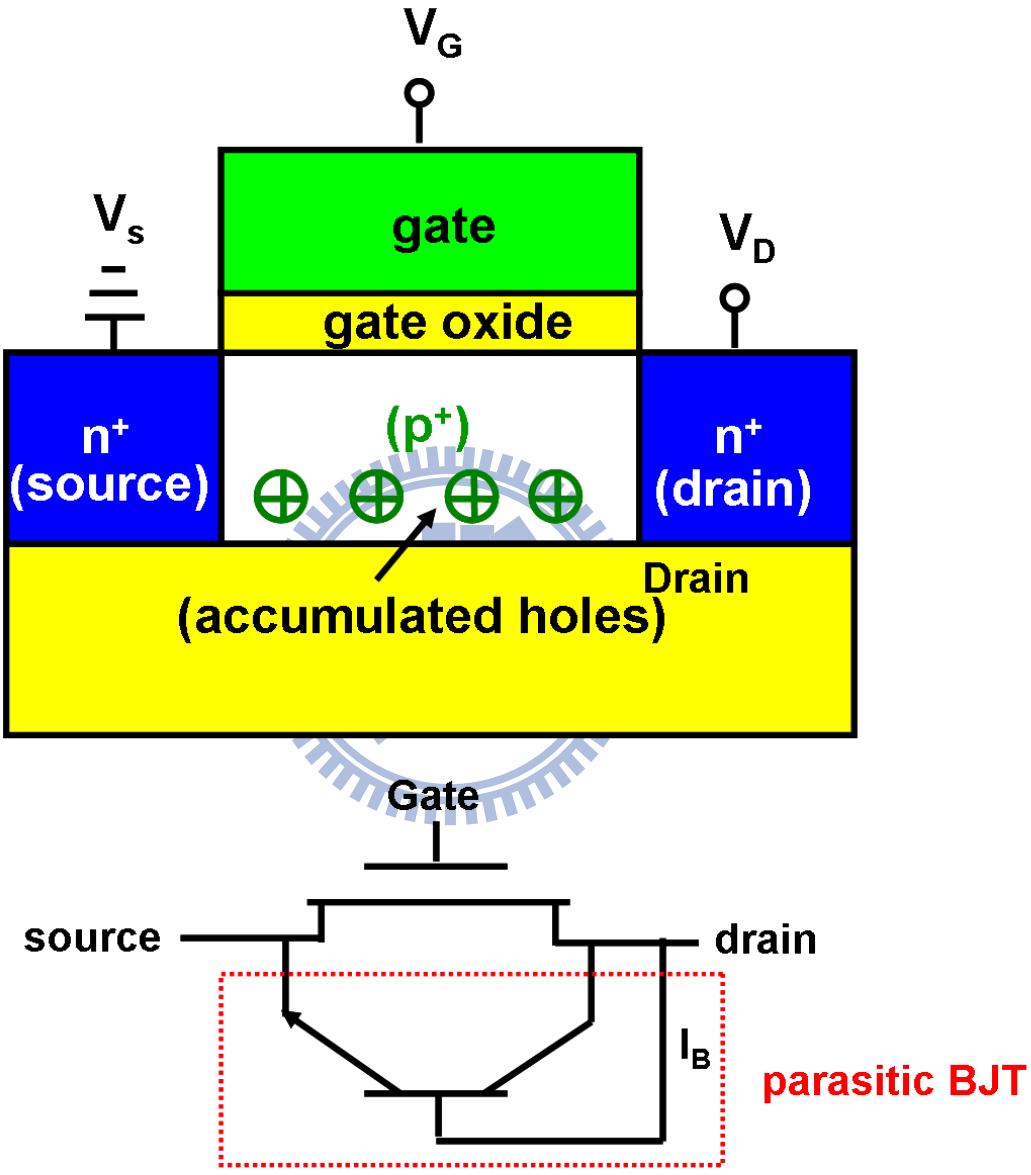

Fig. 1-10 Typical latch-up phenomenon found in SOI devices.

Chapter 2

Performance Enhancement of Poly-Si Nanowire (NW) Transistors with Independent Double-gated (IDG) Configuration

2.1 Introduction

Polycrystalline-silicon (poly-Si) thin-film transistors (TFTs) are widely applied in various fields such as active matrix liquid-crystal-displays (AMLCDs) and three-dimensional electronics [2.1]~[2.3] due to the low temperature and mature fabrication processes. However, as compared with the metal-oxide-semiconductor (MOS) transistors built on single crystalline silicon (c-Si), a large amount of defects contained in granular poly-Si channels would dramatically aggravate the device performance including high subthreshold swing (SS) as well as large OFF-state leakage current, and the degradation of output current [2.1]. A general strategy to cope with this issue is to improve the quality of granular poly-Si channels such as passivating the defects by a hydrogenation post-treatment [2.4], improving the crystallinity, and enlarging the grain size of poly-Si channels. The latter approach includes solid-phase crystallization (SPC) [2.5], metal-induced lateral crystallization (MILC) [2.6], and

excimer laser annealing (ELA) [2.7]. In addition, the employment of multi-gated (MG) configurations and poly-Si NWs as the conduction channel is also helpful [2.8]. The inherently small volume of poly-Si NWs can dramatically lower the number of defects contained in the channel. Besides, the intrinsic merit of large surface-to-volume ratio possessed by NWs combined with MG configurations can more efficiently modulate the potential barriers provoked by the grain-boundary (GB) defects in a poly-Si channel. Although there are a lot of theoretical studies devoted to analyzing the properties of the aforementioned gate-modulated potential barriers in traditional single-gated planar poly-Si TFTs [2.9]~[2.11], few reports related to the poly-Si-based devices featuring MG configuration and extra-thin NW channel are present. In this regard, an independent double-gated (IDG) NW TFT, developed by our group [2.8], is utilized to investigate the impact of different operation modes on the device characteristics in this work. Such an IDG poly-Si NW transistor can be operated under double-gated (DG) or single-gated (SG) modes of operation since the two control gates can be biased independently. Therefore, the efficiency of modulation to potential barriers under DG or SG modes of operation can be fairly compared in the same device. Moreover, such a device featuring its NW channels in a regular shape makes theoretical analysis more feasible.

2.2 Experiments

Figures 2-1(a)-(b) show the three-dimensional schematic structures as well as cross-sectional transmission electron microscopic (TEM) images and top view of the IDG poly-Si NW TFTs investigated in this chapter, respectively. As shown in Figs. 2-1(a)-(b), such devices feature a pair of poly-Si NW channels gated by two independent control-gates, therefore more flexibility can be provided in device operation. The fabrication flow of the transistors basically follows that described in our previous report [2.8]. Cross-sectional views of key steps along the A–B dashed line shown in Fig. 2-1(b) are depicted in Figs. 2-2(a)-(d), respectively. A first gate consisting of 100 nm-thick *in situ* doped n^+ poly-Si was sandwiched between two 50 nm-thick nitrides (Fig. 2-2(a)), followed by the formation of the cavities by laterally and selectively etching the *in situ* doped n^+ poly-Si in a transformer-coupled plasma (TCP) reactor (Fig. 2-2(b)). Afterwards, a 14nm-thick tetraethyl orthosilicate oxide layer was deposited to serve as the gate dielectric of the first gate, followed by the deposition of a 100nm-thick undoped amorphous-Si layer, both by low-pressure chemical vapor deposition (LPCVD). Next, an annealing step was performed at 600 ℃ in N_2 ambient for 24 hours to transform the amorphous-Si into poly-Si. After the source/drain (S/D) implantation, the undoped poly-Si layer was then patterned and etched to define the embedded NW channels and S/D regions simultaneously, as shown in Fig. 2-2(c). Finally, another 14nm-thick LPCVD TEOS oxide layer was deposited to serve as gate

dielectric of the second gate, followed by the deposition of 100nm-thick *in situ* doped n^+ poly-Si layer, which was then patterned to serve as the second gate electrode, as shown in Fig. 2-2(d). Next, we will introduce the measurement setup.

Electrical characteristics of the fabricated devices in this thesis are mainly characterized by an automated measurement setup consisting of an HP 4156 semiconductor parameter analyzer, an Agilent 8110A pulse generator, and a Visual Engineering Environment (VEE). These equipments integrated in the system are controlled by the interactive characterization software (ICS) program. The temperature was controlled at a stable value by the temperature-regulated hot-chuck.

2.3 Performance Enhancement under DG Control

Figures 2-3(a) shows the I_D-V_G characteristics of the IDG poly-Si NW TFT with channel length of 5 μm, operated in SG-1, SG-2, or DG modes of operation. The DG mode of operation denotes that both gate electrodes (first and second gates) are applied with the sweeping bias. For the SG-1 and SG-2 modes of operation, the sweeping gate voltage is applied to the first and second gate electrode, respectively, while the other gate is grounded. The comparison of the output characteristic under DG mode of operation with the sum of those under SG-1 and SG-2 modes of operation is shown in Fig. 2-3(b). It is interesting to see that the output current under DG mode of operation is

much larger than the sum of those under SG-1 and SG-2 modes of operation. As the device is operated in the region of high drain voltage (V_D), our previous work [2.12] indicates that this enhancement is mainly attributed to the "early saturation effect", and the limited saturation current under a SG mode is due to the lower saturation voltage. However, as a device is operated in the linear region (V_D is low), current enhancement is still observed while the above explanation is not applicable. Therefore, in the following sections, through our experimental and theoretical analysis, it is shown that a greater grain-boundary (GB) barrier lowering under DG mode of operation plays an important role in the aforementioned phenomenon. Before the end of this section, it is worth noting that as shown in Fig. 2-3(a), SG-1 mode has worse SS than that under SG-2 mode. According to our previous work [2.8], it is because that the conduction electrons need to surmount the extra barrier between source/drain and conduction channel arising from the offset (*i.e.*, ungated) regions during SG-1 mode of operation. In order to avoid the influence of such an extra barrier on the exploration of the grain-boundary (GB) barrier lowering under DG or single-gated (SG) modes of operation, major attention is paid on the device characteristics under SG-2 mode of operation as a comparison is made with that of DG mode in Sec. 2-6.

2.4 Experimental Analysis on the Double-gate

Modulated Barrier Lowering

According to the classic Levinson's model [2.10], the drain current and barrier height are related by the following equation:

$$I_D = \frac{W}{L} n\mu_0 e^{-\frac{V_B}{kT}} V_D, \quad (2\text{-}1)$$

where W and L are the width and length of the channel, respectively, n is the concentration of the induced electrons, μ_0 is the mobility of the electrons inside the grain, kT is the thermal energy, V_B is the barrier height, and V_D is the drain voltage. From Eq. 2-1, we can see that a lowering in V_B leads to more efficient thermionic emission and thus a higher drain current. To clarify this point, we extract the activation energy, which represents the effective V_B of the conduction electrons [2.9]~[2.11], from the I_D-V_G characteristics of a fabricated device measured at V_D = 0.1V and temperature ranging from 30°C to 90°C (see the inset shown in Fig. 2-4). The results are shown in Fig. 2-4 as a function of gate voltage. As expected, V_B decreases with increasing gate voltage due to the increase in carrier concentration. Moreover, V_B is much lower in the case of DG mode of operation. According to Eq. 2-1, such DG-induced barrier-lowering is very likely the major factor responsible for the larger I_D, as compared to that under SG mode of operation. The hypothesis is clarified with theoretical analysis detailed in the next section.

2.5 Theoretical Analysis

In order to theoretically analyze the DG-induced barrier lowing, the simplified two-dimensional structure with channel thickness of 20 nm, shown in Fig. 2-5, is applied to the two-dimensional TCAD simulation tool [2.13], featuring two independent n^+ poly-Si gates with the same gate oxide thickness of 14 nm. The *x*- and *y*- directions, shown in Fig. 2-5, are parallel and perpendicular to the source-to-drain direction, respectively. The position at depth $y = 0$ corresponds to the interface between top gate oxide and channel. In order to well describe the grain-boundary defects contained in the granular poly-Si channel, Fig. 2-5 is assumed to have a bamboo-like structure with the same GB traps and grain size of 30 nm. The grain size is chosen based on the results of previous transmission electron microscopic (TEM) characterization performed on the poly-Si films formed with solid-phase crystallization (SPC) scheme [2.14]. The capture and emission processes through GB traps are handled by the simulator using Shockley–Read–Hall recombination model and a conventional drift-diffusion method is used to model the carrier transport. Figures 2-6(a) and (b) depict the simulation results which can well describe the observed I_D-V_G and I_D-V_D characteristics of the fabricated devices. Note that "SG*2", shown in Fig. 2-6 (b) means double of the output current under SG-2 mode of operation. Next, the simulated barrier heights at channel depth y = 1, 3, and 5 nm are extracted and shown in Fig. 2-7. It can be seen that V_B is smaller for

the DG mode. Moreover, as y is closer to the interface, V_B becomes lower owing to a larger amount of induced electrons. However, the difference in V_B between the SG and DG modes increases with increasing *y*. This trend clearly evidences that more current conduction are available for the DG mode as observed experimentally in Fig. 2-4. It should be noted that such a coupling of the two separate gate biases occurs only as the channel body is sufficiently thin (in this case it is 20 nm).

Next, we will further demonstrate that the more efficient barrier lowering under DG modes results in significant thermionic emission enhancement. Here we define a parameter, thermionic emission factor (*TEF*), as follows:

$$TEF = \exp(\frac{-V_B}{kT}). \tag{2.2}$$

The effective *TEF* can be obtained by substituting the experimentally extracted V_B into Eq. 2-2. To verify the experimental data with simulation we employ the following relation:

$$TEF = \frac{\int_0^d n(y)\exp(\frac{-qV_B(y)}{kT})dy}{\int_0^d n(y)dy}, \tag{2.3}$$

where *d* is the channel thickness, *n(y)* and $V_B(y)$ are the simulated electron density and barrier height at depth *y*, respectively. In Eq. 2-3, *n(y)* serves as a weighting factor and a larger *n(y)* will contribute more to *TEF*. As shown in Fig. 2-8, the simulated results show excellent agreement with the trend found experimentally. In addition, as compared

with that in the SG mode of operation, the results also indicate that the enhancement in barrier lowering by the coupling of the two gate biases results in more efficient thermionic emission under DG mode of operation, and thus, leading to the improvement of I_D.

2.6 Summary

In this chapter, the physical mechanism responsible for the output current enhancement of poly-Si TFTs with ultra-thin channel under DG mode of operation is explored experimentally and theoretically under small drain voltage. The experimental data indicate that the potential barriers, which are provoked by the grain boundaries in the granular poly-Si channel, can be more efficiently lowered as the device is operated in DG mode. Such barrier-lowering leads to more efficient thermionic emission and consequently significantly improves output current. In addition to the experimental investigation, this interesting phenomenon is also verified from the theoretical analysis with the aid of a two-dimensional TCAD tool [2.13] and analytical expressions.

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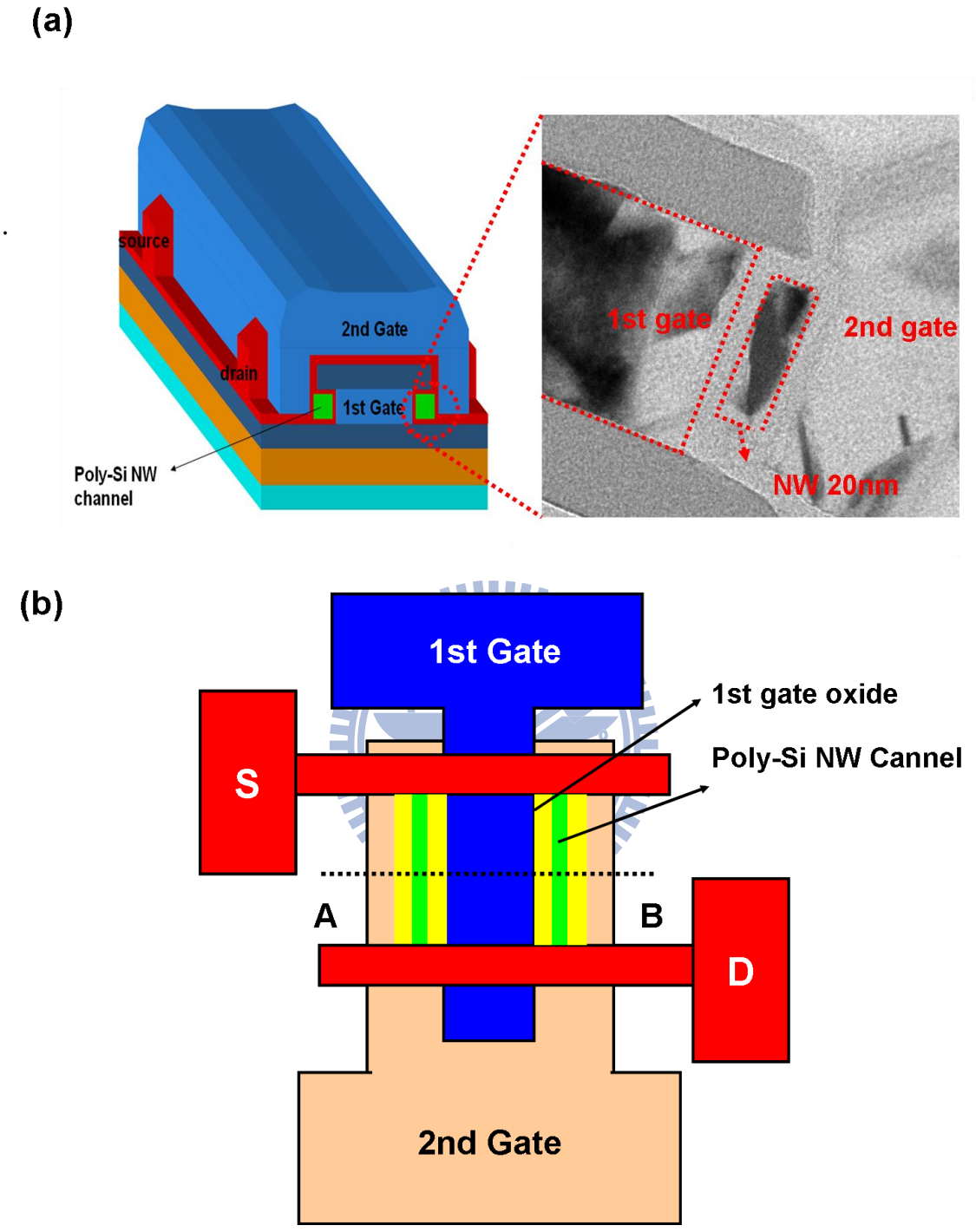

Fig. 2-1 (a) Stereo view as well as cross-sectional TEM image and (b) top view of the n-type IDG poly-Si NW TFTs investigated in this chapter, featuring two independently-biased gates and rectangular poly-Si NWs.

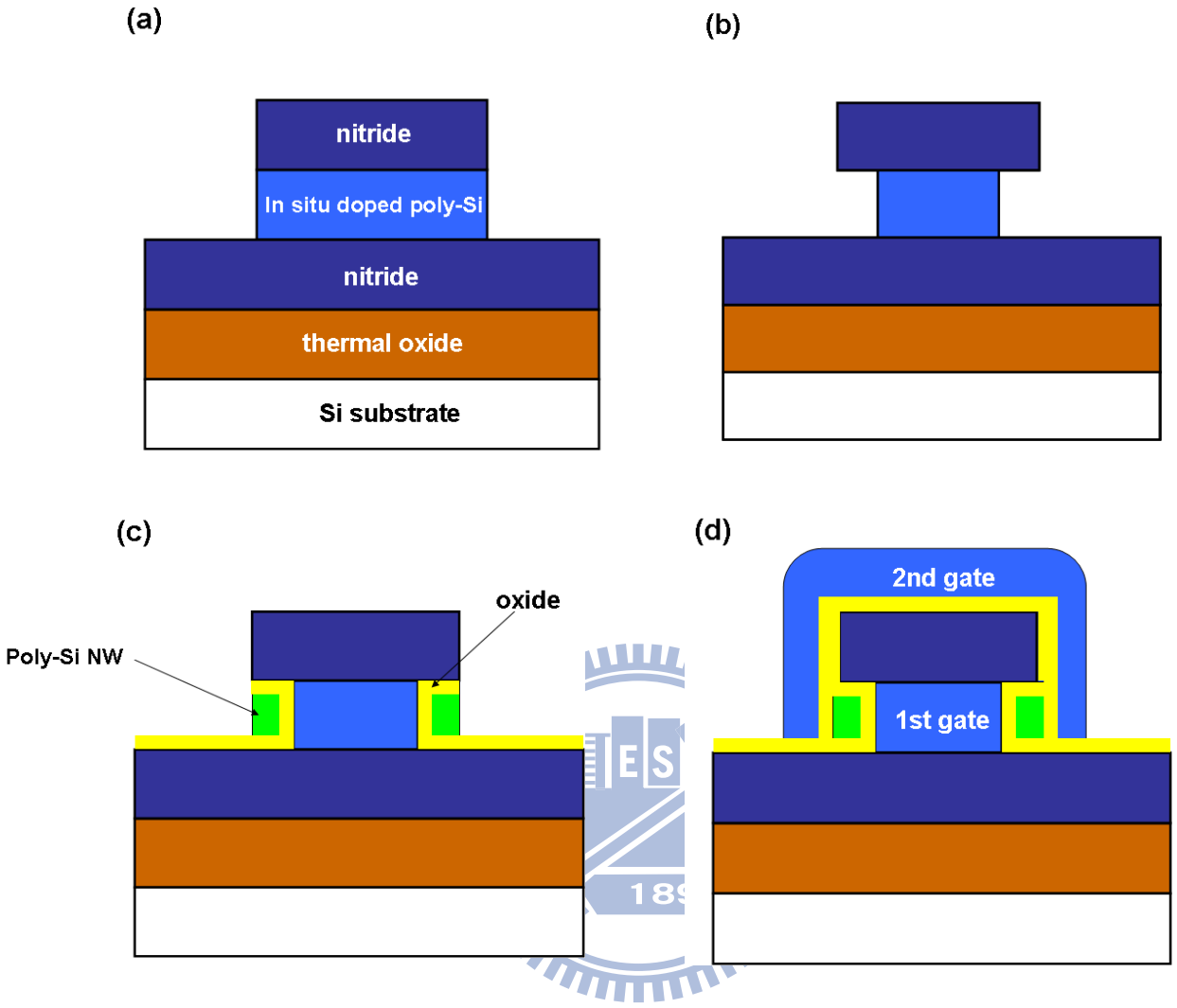

Fig. 2-2 (a)~(d) Key steps of fabrication flow of the IDG poly-Si NW TFTs investigated in this chapter.

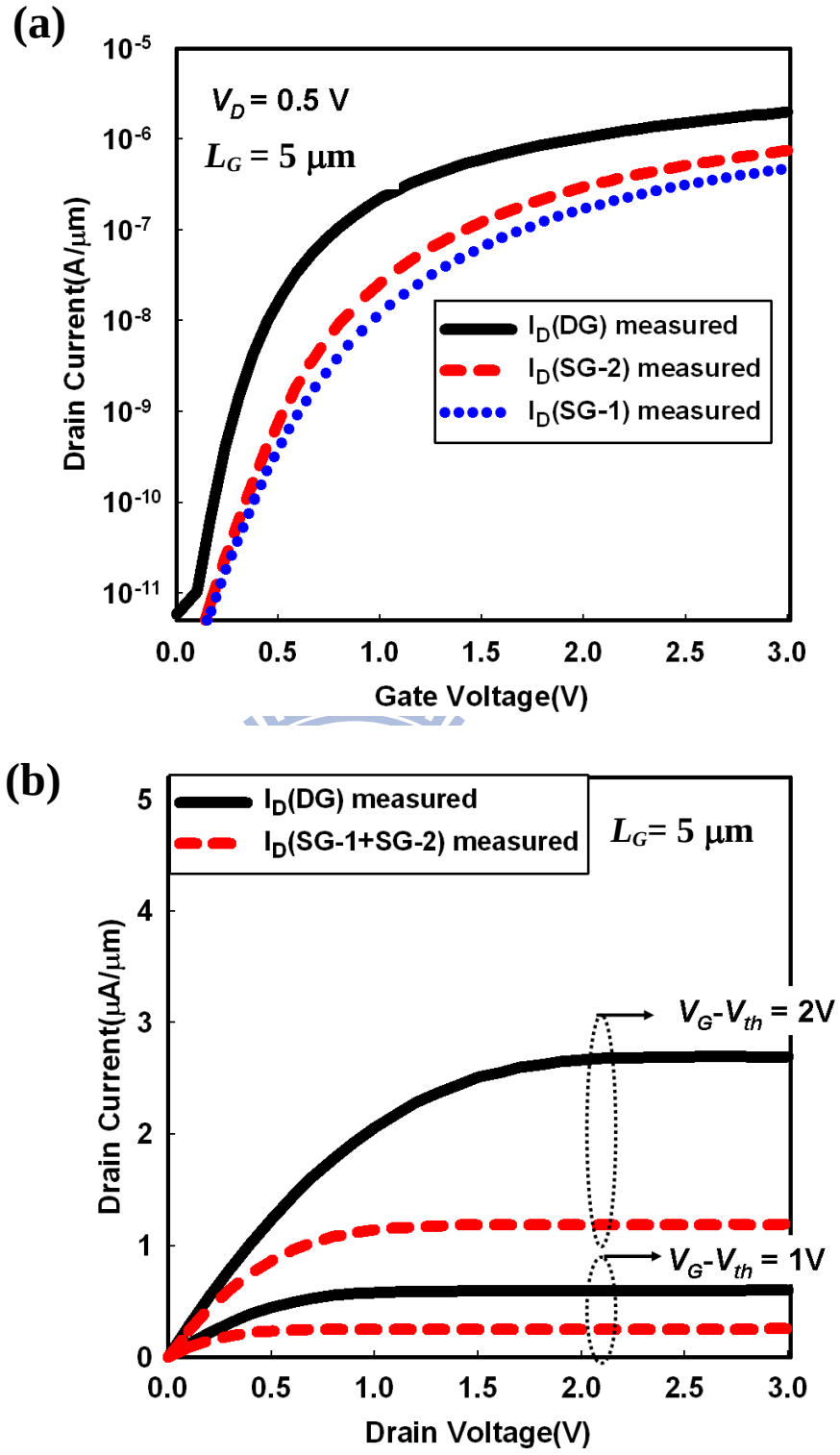

Fig. 2-3 (a) I_D-V_G and characteristic of the investigated IDG poly-Si NW TFT, featuring poly-Si channel thickness of 20 nm, gate oxide of 14 nm, and gate length of 5 μm under SG-1, SG-2, and DG modes of operation. (b) Comparison of the output characteristic under DG mode of operation with the sum of those under SG-1 and SG-2 modes of operation.

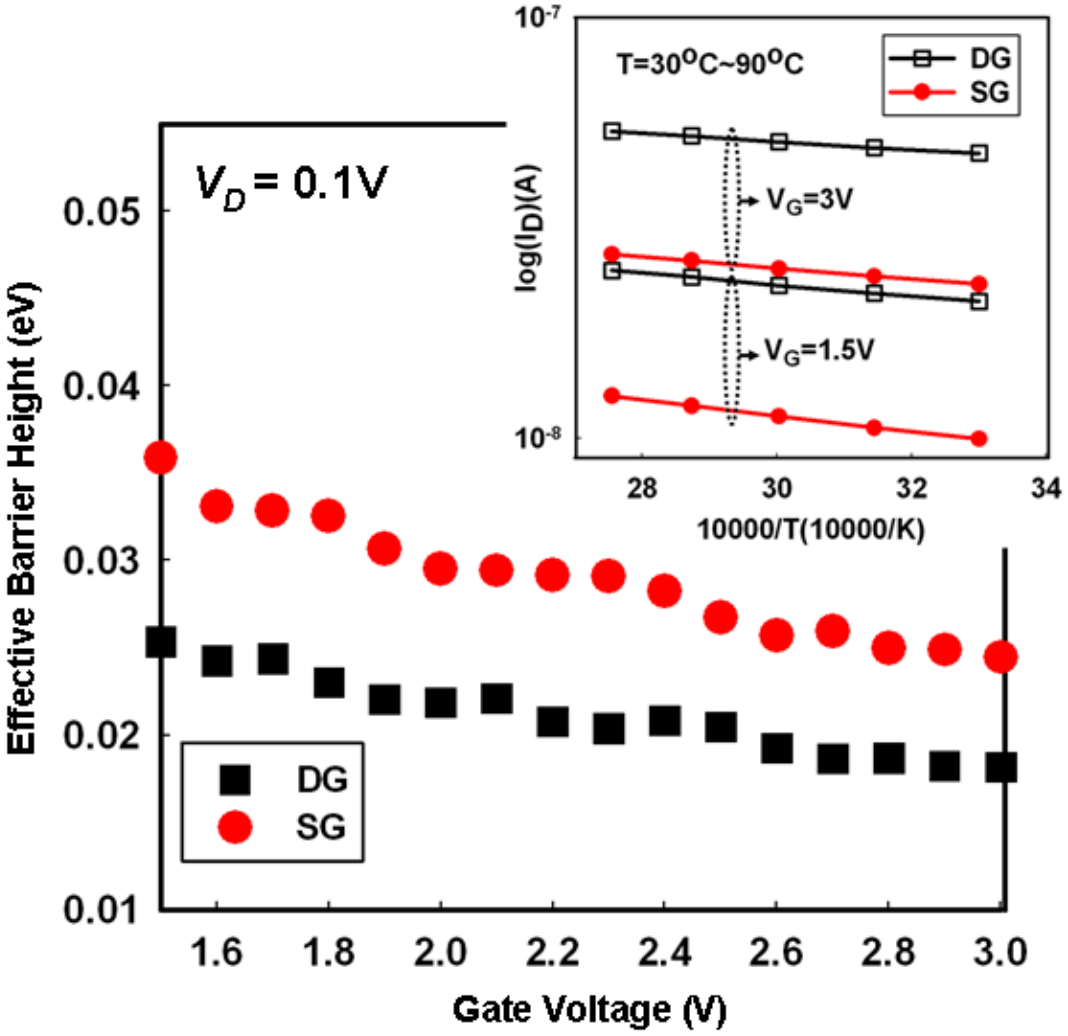

Fig. 2-4 Extracted V_B as a function of gate voltage for the device characterized in Fig. 2-3. The inset shows some of the log(I_D) vs. temperature (T) curves for extracting V_B. DG mode shows reduced V_B as compared with the SG mode.

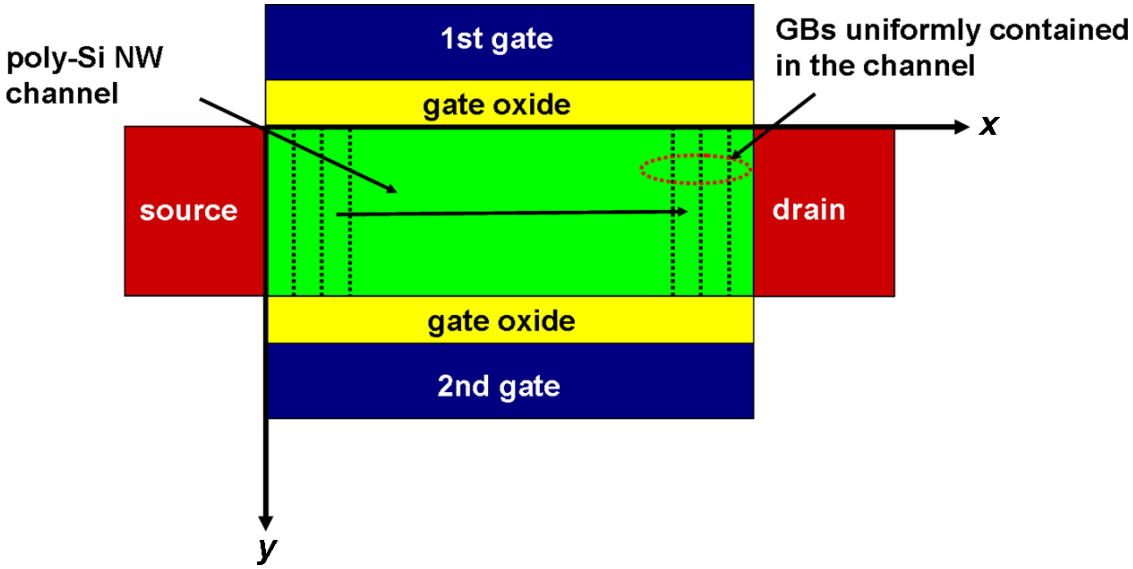

Fig. 2-5 Simplified 2D schematic illustration of the device applied in 2D TCAD simulation, featuring poly-Si channel thickness of 20 nm, gate oxide of 14 nm as well as gate length of 5μm and bamboolike structure corresponding to the granular channel of IDG poly-Si NW TFTs.

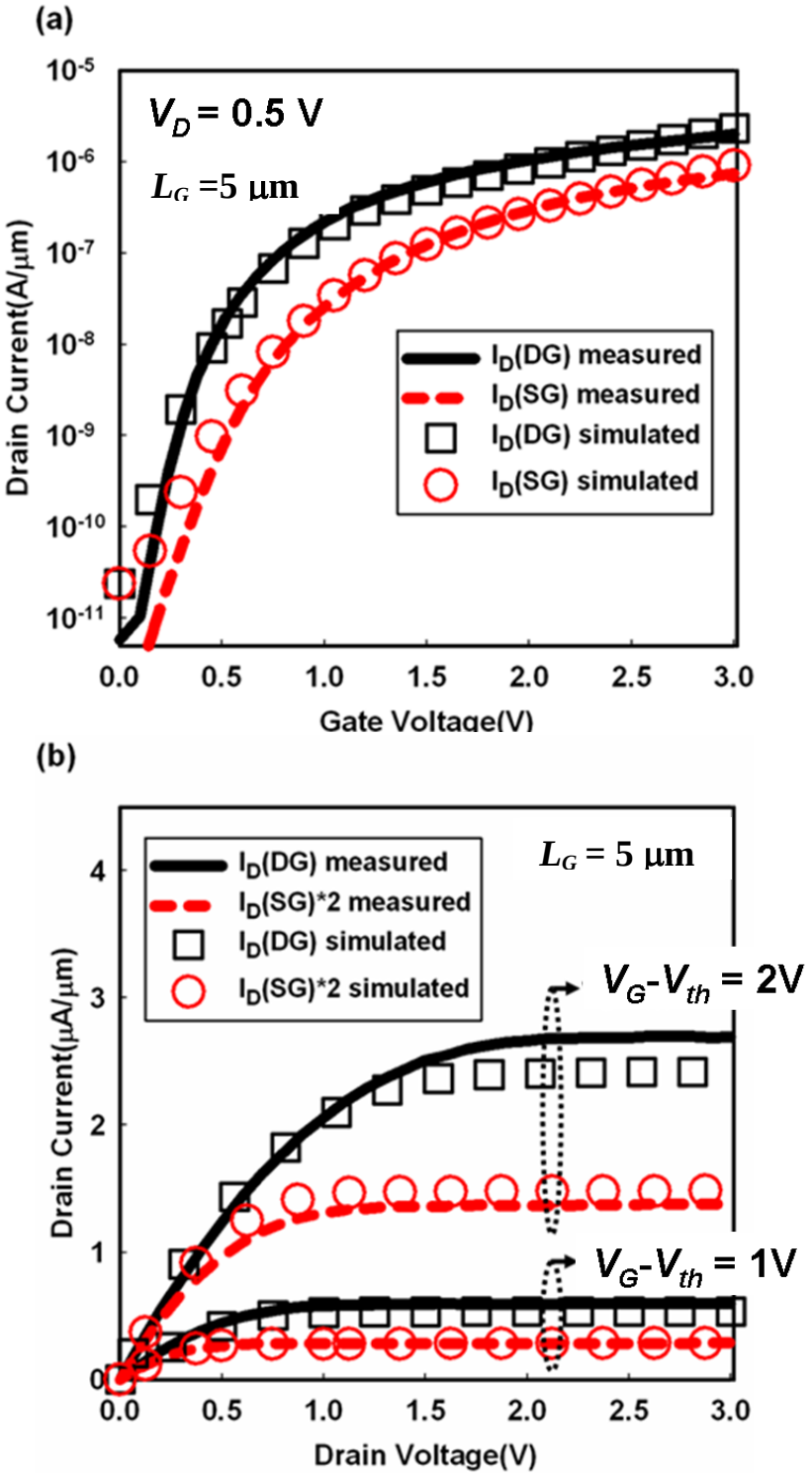

Fig. 2-6 The simulated (a) I_D-V_G and (b) I_D-V_D characteristics of the IDG poly-Si NW TFT under DG and SG modes of operation. Excellent agreements with those from experimental measurements shown in Fig. 2-3 are obtained.

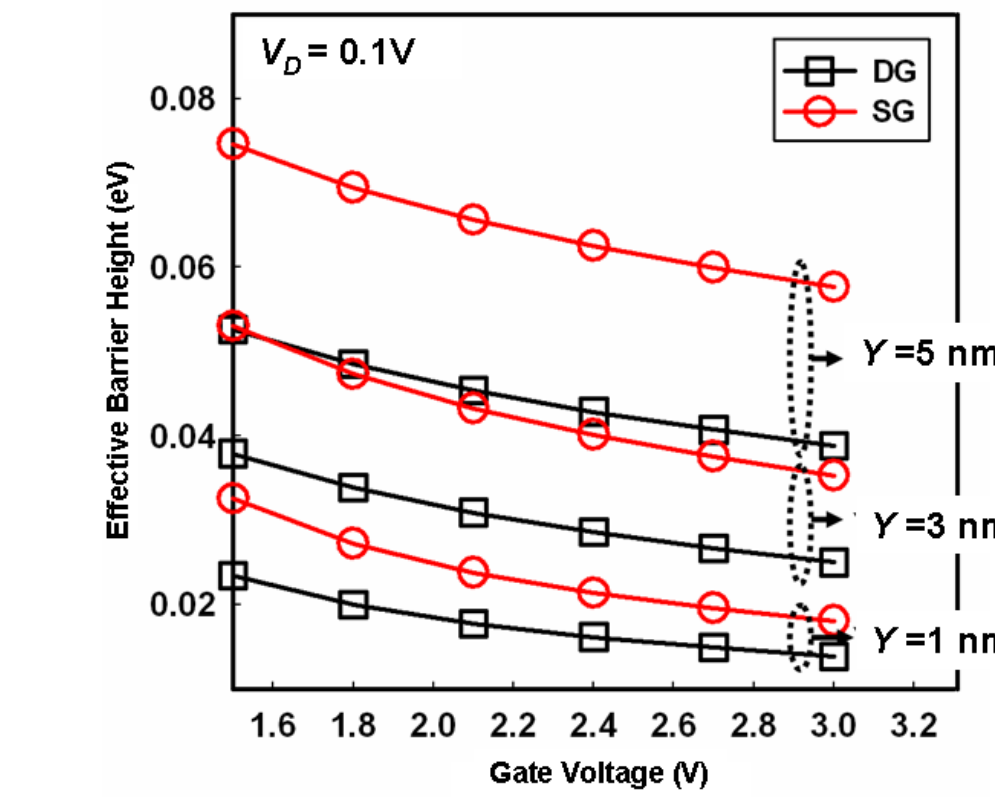

Fig. 2-7 The simulated V_B values at y = 1, 3, and 5 nm with simulated I_D-V_G and I_D-V_D characteristics shown in Fig. 2-6.

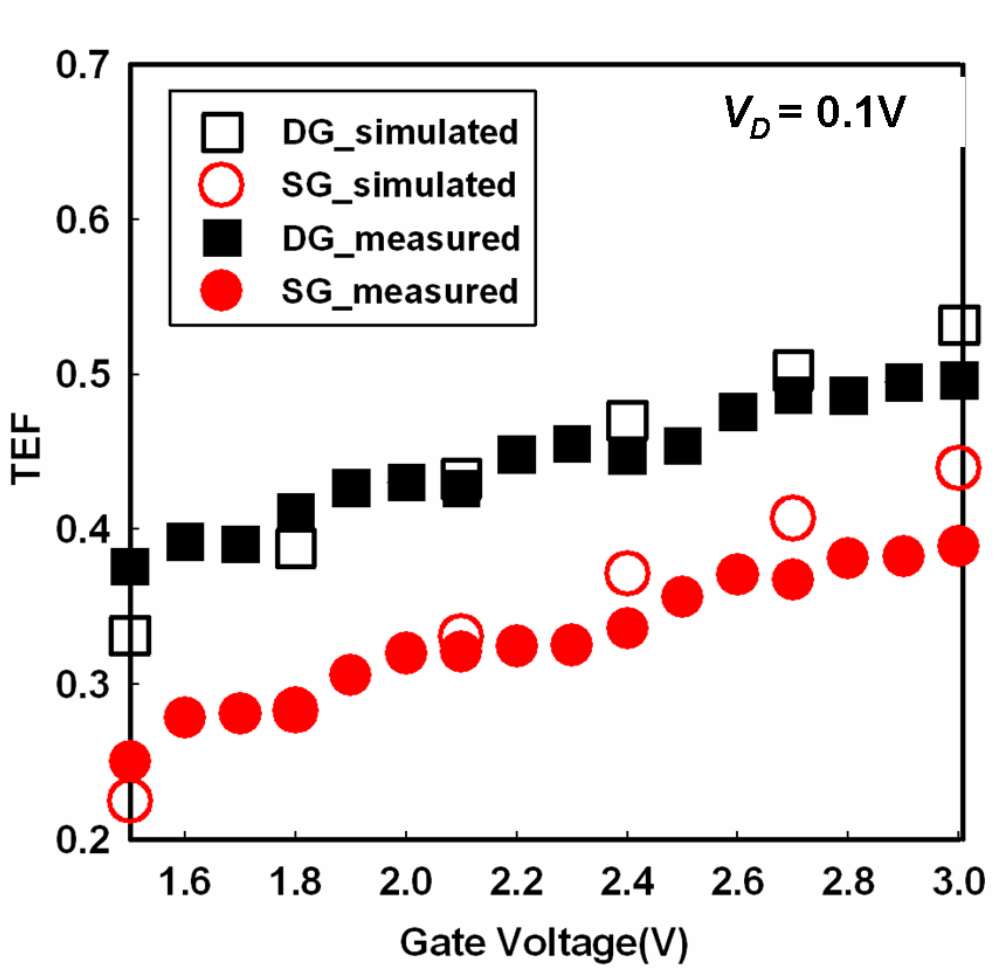

Fig. 2-8 Comparisons of experimental and simulated *TEF* under DG and SG modes of operation.

Chapter 3

Read Characteristics of Independent Double-Gated (IDG) Poly-Si Nanowire SONOS Devices

3-1 Introduction

Driven by the tremendous increase in the demand of portable electronic products, the non-volatile semiconductor flash memory market dominated by the floating-gate (FG) flash technology has been rapidly growing. However, other potential alternatives such as charge-trapping flash memories have also drawn particular renewed attentions because the minimization of floating-gate cells is strongly limited by the decreasing of gate coupling ratio as well as reliability issues caused by stress-induced leakage current (SILC) or interference of neighboring cells [3.1]~[3.4]. In the charge-trapping flash memory technologies, silicon-oxide-nitride-oxide-silicon (SONOS) scheme has been widely studied and reported [3.5]~[3.6]. Such a scheme adopts the sandwich architecture (*i.e.*, oxide/nitride/oxide) where the nitride layer replaces the FG as the charge storage medium. The discrete and isolated trapping centers provided by the nitride enable a SONOS flash memory device to exhibit a greater immunity against the

catastrophic failure due to the leakage current from a single defect located in the tunneling oxide and, thus, allowing the use of a thinner tunneling oxide [3.7]. In addition, compared to floating-gate flash memories, the reduction of stacking height makes SONOS flash memories less vulnerable to the interference from neighboring cells.

Most of the previous studies adopted a single-crystalline silicon layer as the conduction channel in a SONOS flash memory. However, considering the applications in 3D stackable technologies, the replacement of a single-crystalline silicon channel by a poly-Si one is a preferable choice in terms of the low deposition temperature (typically below 600 ℃). Certainly the potential concern is the inevitable defects contained in the ploy-Si channel. As mentioned in Chapter 2, such an issue can be efficiently addressed by the employment of poly-Si NW channels and MG configurations for more efficient modulation of the potential barriers caused by GB defects in poly-Si channel. In addition, the MG control, such as GAA configuration, can strengthen the electric field at the channel-to-gate dielectric interface and, thus, improve the programming/erasing (P/E) efficiency [3.8]. Although most of previous studies were focused on common MG gate architectures owing to the ease of process, SONOS flash memories featuring IDG configurations have also drawn a lot of attentions [3.9]~[3.10]. It is because the IDG configuration can offer more design flexibility pertaining to the two individually-biased

gates. In addition, it has been demonstrated that the “read-pass disturb” can be efficiently suppressed in IDG SONOS flash memory if the auxiliary gate (*i.e.*, the one without oxide/nitride/oxide layers to store data) is utilized as the read-passing gate [3.7]. Previously, by modifying the aforementioned novel IDG NW poly-Si TFT (shown in Chapter 2), our group has succeeded in fabricating an IDG poly-Si NW SONOS device, which shows greatly enhanced program/erase (P/E) speed if an appropriate IDG bias condition is applied and the channel is thin enough [3.11].

On the other hand, different read modes can be adopted in an IDG poly-Si NW SONOS device with the two feasible control gates. Nonetheless, their impact on the memory window is still not clear. Therefore, in this chapter, special attention is paid to the operation of different read modes and the impact on memory window. Both theoretical analysis and experimental clarification are conducted to comprehend the above topics. The organization of this chapter is as follows. The three-dimensional architecture of the investigated IDG poly-Si NW SONOS device and the cross-sectional transmission electron microscopic (TEM) image are shown in Sec. 3-2. Next, Section 3-3 introduces the theorectical background of threshold voltage (V_{th}) as a function of control gate bias in an IDG device. Next, based on that, the model of memory window under two read modes for an IDG SONOS device will be proposed in Sec. 3-4. Next, the experimental verification is provided in Sec. 3-5. Finally, in Sec. 3-5, based on the

analysis done in previous sections, an innovative IDG SONOS flash memory devices suitable for the future three-dimensional stacked flash memory technology is proposed to end Chapter 3.

3-2 Device Structure

The three-dimensional schematic structure as well as cross-sectional transmission electron microscopic (TEM) image and top view of the investigated IDG poly-Si NW SONOS device are shown in Figs. 3-1(a)-(b), respectively. As shown in the figures, its architecture is almost the same as the IDG poly-Si NW TFT investigated in Chapter 2 except for the replacement of the first-gate TEOS oxide by an oxide/nitride/oxide (ONO, 4nm/7nm/7nm) stack. As shown in Figs. 3-1(a) and (b), the IDG poly-Si NW SONOS device features a pair of poly-Si NW channels, gated by two independent control gates. Therefore, such a device can provide two kinds of read mode. In addition, the cross-sectional TEM image illustrates the rectangular NW channels with extra-thin thickness of 10 nm.

3-3 Effects of Auxiliary Gate Bias on V_{th} of the IDG Devices

This section introduces the theory governing the effects of the auxiliary gate bias

on the V_{th} of an n-channel IDG fully-depleted (FD) device driven by the opposite gate of the device. Figure 3-2 schematically depicts the structure of a n-channel IDG FD device. During measurements, the gate bias applied to the driving gate is swept to obtain the transfer characteristics while a fixed voltage is applied to the auxiliary (or V_{th}-control, control for short) gate. Figure 3-3 illustrates the simplified V_{th} characteristics of the device ($V_{th(dri)}$) as a function of the control gate bias ($V_{G(con)}$). According to the theory developed by Lim and Fossum [3.12]~[3.13], the V_{th} characteristics can be divided into three regions, as indicated in the figure. In regions I and III, the channel surface of the control-gate side are respectively accumulated and inverted. As a consequence, the V_{th} of the driving gate is pinned at $V_{th(dri),acc(con)}$ and $V_{th(dri),inv(con)}$, respectively, and can be expressed as

$$V_{th(dri),acc(con)} = V_{FB(dri)} + (1+\frac{C_{si}}{C_{ox(dri)}})2\phi_B - \frac{Q_{depl}}{2C_{ox(dri)}}, \quad (3\text{-}1)$$

$$V_{th(dri),inv(con)} = V_{FB(dri)} + 2\phi_B - \frac{Q_{depl}}{2C_{ox(dri)}}, \quad (3\text{-}2)$$

where $V_{FB(dri)}$ is the flat-band voltage of the driving gate, $C_{si} = \varepsilon_0\varepsilon_{si}/t_{si}$ is the silicon depletion capacitance, $Q_{depl} = qN_At_{si}$ is the total charges due to ionized dopants in the depleted Si film, $\phi_B = (kT/q)\ln(N_A/n_i)$ is the Fermi potential of Si channel, and $C_{ox(dri)} = \varepsilon_0\varepsilon_{ox}/t_{ox(dri)}$ is the gate oxide capacitance of the driving gate. In addition, N_A is the doping density in the silicon film, t_{si} is the thickness of silicon film, kT/q is the thermal energy,

and n_i is the intrinsic carrier concentration. In region II, the channel surface of the control-gate side is depleted and the $V_{th(dri)}$ can be adjusted by the applied $V_{G(con)}$. Boundaries of these regions are at $V_{G(con,acc)}$ and $V_{G(con,inv)}$, which represent the onsets of accumulated and inverted surface of control gate, respectively, and can be expressed as

$$V_{G(con,acc)} = V_{FB(con)} - \frac{C_{si}}{C_{ox(con)}} 2\phi_B - \frac{Q_{dep}}{2C_{ox(con)}}, \tag{3-3}$$

$$V_{G(con,inv)} = V_{FB(con)} + 2\phi_B - \frac{Q_{dep}}{2C_{ox(con)}}, \tag{3-4}$$

where $V_{FB(con)}$ and $C_{ox(con)} = \varepsilon_0\varepsilon_{ox}/t_{ox(con)}$ are the flat-band voltage of the control gate and oxide capacitance, respectively. As $V_{G(con)}$ increases from $V_{G(con,acc)}$ to $V_{G(con,inv)}$, the $V_{th(dri)}$ is linearly decreased from $V_{th(dri),acc(con)}$ to $V_{th(dri),inv(con)}$. Therefore, the V_{th} of driving gate in region II can be expressed as:

$$V_{th(dri),depl(con)} = V_{th(dri),acc(con)} - \left(\frac{C_{si}C_{ox(con)}}{C_{ox(dri)}(C_{si}+C_{ox(con)})}\right)(V_{G(con)} - V_{G(con,acc)}). \tag{3-5}$$

Furthermore, its slope is defined as the body-factor, β, which is expressed as

$$\beta = \frac{C_{si}C_{ox(con)}}{C_{ox(dri)}(C_{si}+C_{ox(con)})}. \tag{3-6}$$

3-4 Memory Window under Two Read Models in IDG Devices

In this section, based on the theory introduced in the above section, we consider

another situation shown in Fig. 3-4, which has two independent gates denoted as gate 1 (G1) and gate 2 (G2), and an amount of negative charges is contained in the gate oxide of G1. Since the two gates can be operated independently, two read modes can be applied. In mode I, the device is driven by G2 while G1 serves as the control gate to adjust $V_{th(dri).}$ The $V_{th2(dri)}$-$V_{G1(con)}$ characteristics in the mode I are shown in Fig. 3-5(a), where the solid and dashed lines are individually related to the cases with and without the aforementioned extra stored charges. Actually, the dashed line is the same as the one shown in Fig. 3-3. As can be seen in the figure, the $V_{th2(dri)}$-$V_{G1(con)}$ curve with the extra charges shows a parallel shift toward positive direction of the applied bias of G1, which severs as the control gate in mode I. This is because of the positive shift of the G1's flat-band voltage resulting from the incorporated fixed charges at the gate oxide of G1. Therefore, based on Eqs. 3-3 and 3-4, the voltages corresponding to the onsets of the accumulated and inverted surface of G1 with negative charges contained in the gate oxide of G1, denoted as $V(Q)_{G1(con,acc)}$ and $V(Q)_{G1(con,inv)}$, can be expressed as [3.14]

$$V(Q)_{G1(con,acc)} = V_{G1(con,acc)} - \frac{qQ}{C_{ox1}}, \tag{3-7}$$

$$V(Q)_{G1(con,inv)} = V_{G1(con,acc)} - \frac{qQ}{C_{ox1}}, \tag{3-8}$$

$$Q = = \frac{\int_{0}^{t_{ox1}} x\rho dx}{t_{ox1}}, \tag{3-9}$$

where t_{ox1}, x, and ρ individually denote the oxide thickness of G1, position, and charge density of the charges in the gate oxide of G1. The difference in V_{th} between the two characteristic curves in Fig. 3-5(a) is defined as the memory window. Due to the right shift caused by the incorporated charges, the memory window operated in the region between points A and B is shown in Fig. 3-5(b), which shows a linear relation with respective to the bias of control gate (V_{G1}). In addition, its slope is determined by the body-factor β (Eq. 3-6). Therefore, the memory window can be expressed as

$$\Delta V_{th} = \beta(V_{G1} - V_{G1(con,acc)}), \tag{3-10}$$

$$\beta(body-factor) = \frac{C_{si}C_{ox1}}{C_{ox2}(C_{si}+C_{ox1})}. \tag{3-11}$$

Next we examine the properties of mode II, in which G1 and G2 serve as the driving gate and control gate, respectively. In other words, the roles of G1 and G2 in the mode I are switched in the present case. The $V_{th1(dri)}$-$V_{G2(con)}$ characteristics in the mode II are shown in Fig. 3-6(a) where the solid and dashed lines are respectively related to the cases with or without negative charges contained in the gate oxide of G1. It should be noted that the extra fixed charges contained in the gate oxide of G1 have no influence on the surface conditions of channel gated by G2. This means the voltages correspond to the onsets of the accumulated and inverted surface of the channel gated with G2 remain unchanged. However, it indeed affects the threshold voltage as G1 serves as the driving gate. As a result, a parallel shift toward positive direction of the threshold

voltage (*y*-axis) is observed in Fig. 3-6(a). Furthermore, the associated threshold voltages with negative charges contained in the gate oxide of G1 in the mode II at the onsets of the accumulation and inversion of the channel gated with G2, $V(Q)_{th1(dri),acc2}$ and $V(Q)_{th1(dri),inv2}$, respectively, can be expressed as

$$V_{th1(dri),acc2(con)} = V_{th1(dri),acc2(con)} - \frac{qQ}{C_{ox1}}, \tag{3-12}$$

$$V_{th1(dri),inv2(con)} = V_{th1(dri),inv2(con)} - \frac{qQ}{C_{ox1}}. \tag{3-13}$$

Fig. 3-6(b) shows the memory window operated in the region betweens point A and B shown in Fig. 3-6(a) which has no dependence on the gate bias of the control gate owing to the upward parallel shift with the incorporation of electrons. The memory window is

$$\Delta V_{th} = -\frac{qQ}{C_{ox1}}, \tag{3-14}$$

which is proportional to the amount of charges incorporated.

3-5 Experimental Verification and Discussion

Next, the aforementioned fabricated IDG poly-Si NW SONOS TFT (Fig. 3-1(a)) is employed to explore the characteristics of the IDG SONOS devices and verify the theoretical model derived in Sec. 3-4. As can be seen in the cross-sectional TEM image

(Fig. 3-1(a)), the poly-Si NW channel is 10 nm in thickness, horizontally sandwiched by two independent gates denoted as the first and the second gates. In the following discussion, for simplicity, the first gate and its gate bias are denoted as the ONO-gate and $V_{G\text{-}ONO,}$ respectively, while the second gate and its gate bias as oxide-gate and $V_{G\text{-}O,}$ respectively. The device is programmed and erased using Fowler-Nordheim (FN) tunneling by applying a high gate bias to the ONO-gate while the oxide-gate, source and drain are grounded. As mentioned above, due to the flexibility offered by the IDG configuration, two read modes depending on the choice of driving gate are feasible. The I_D-V_G characteristics of programmed and erased states measured under modes I and II are shown in Figs. 3-7(a) and (b), respectively. The programming was executed with $V_{G\text{-}ONO}$ = 15V and $V_{G\text{-}O}$ = 0V for 5msec, and erasing was with $V_{G\text{-}ONO}$ = -12V and $V_{G\text{-}O}$ = 0V for 20msec. The memory window is defined as the V_{th} difference between the erased and programmed states. Figure 3-8 shows the results of memory window for the two read modes extracted from the data shown in Figs. 3-7(a) and (b). Figure 3-9 shows the simplified two-dimensional schematic SONOS structure with certain amount of electrons contained in the nitride layer. Detailed device parameters for the analysis are also included. In the figure, N_{eff} is the effective channel doping concentration resulting from the grain-boundary trapping centers in poly-Si film [3.15] and is estimated to be about 5×10^{17} cm^{-3} [3.16]. The difference of the present structure from that shown in

Fig. 3-4 is the replacement of the gate oxide of G1 by the ONO stack; thus, the analytical form of memory window given in Eq. 3-10 and Eq. 3-14 for mode I and mode II, respectively, can be applied if a modification in the oxide capacitance of G1 is made. The revised form, denoted as effective C_{ox1}, is expressed as

$$C_{ox1(eff)} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{oxt} + \frac{\varepsilon_{ox}}{\varepsilon_N} \times t_N + t_{oxb}}, \tag{3-15}$$

where t_{oxt}, t_N, and t_{oxb} are the thicknesses of tunneling oxide, nitride, and blocking oxide, respectively, and ε_N is the nitride dielectric permittivity. As the trapped electrons in the nitride layer shown in Fig. 3-9 is taken into account, Eq. 3-14 can be modified into the following form [3.17]

$$\Delta V_{th} = qQ_{tot}\left(\frac{t_{oxb}}{\varepsilon_0 \varepsilon_{ox}} + \frac{t_N - x_{mean}}{\varepsilon_0 \varepsilon_N}\right), \tag{3-16}$$

$$Q_{tot} = \int_0^{t_N} \rho \mathrm{d}x, \tag{3-17}$$

$$x_{mean} = \frac{1}{Q_{tot}} \int_0^{t_N} \rho x \mathrm{d}x, \tag{3-18}$$

where Q_{tot}, x_{mean}, and ρ are the total amount of trapped electrons, mean vertical position in the nitride, and charge density of trapped electrons, respectively. By substituting the device parameters shown in Fig. 3-9 to the above equations, the individual memory windows in mode I and II can be calculated. The theoretical results are shown and verified with the experimental data in Fig. 3-8. Since it is well-known that the charge centroid of the trapped electrons in the nitride layer is located close to

the middle of nitride as long as the programming time is sufficiently long. Therefore, the x_{mean} and Q_{tot} used in the above calculation are set to be 3.5 nm and 5 x 10^{12} cm^{-2}, respectively. As can be seen in Fig. 3-8, the calculated results well describe the measured memory windows extracted from the I_D-V_G characteristics shown in Figs. 3-7(a) and (b).

3-6 Innovative IDG SONOS Devices

The above theoretical analysis and experimental data indicate that the read operation of an IDG SONOS device prefers the mode with the ONO-gate serving as the driving gate and oxide-gate as the control gate. Such a read mode acquires a memory window which is larger than the other mode and independent of the bias applied to the control gate. Based on these features, we proposed a new SONOS flash structure shown in Fig. 3-10(a). Before describing its major features and advantages, we first review a previous structure developed by Walker [3.9] as shown in Fig. 3-10(b). The cell devices in such a structure also adopt an ONO-gate for charge storage and an oxide-gate underneath the channel. During read operation, the oxide-gates of the cells except for the one to be accessed are applied with a bias ($V_{read\text{-}pass}$) in order to reduce the parasitic series resistance. Such scheme can eliminate the necessity of applying a high bias to the ONO-gates of the cells neighboring the accessed cell. As a result, read-pass disturb can

be effectively suppressed. One major issue associated with such a structure is the alignment of top ONO-gate and bottom oxide-gate in the cell devices, making the fabrication complicated. Another major issue is the extra areas occupied by the contact holes of the serial bottom oxide-gates. These two issues can be addressed with the proposed scheme shown in Fig. 3-10(a), where the SONOS cells in the series string share a common bottom oxide-gate. During read operation the common bottom oxide-gate serves as the control gate and is applied with $V_{read\text{-}pass}$, while the top ONO-gate for the cell to be accessed is applied with V_{read}. The top ONO-gates of the neighboring cells are either floating or with a low voltage. Such a scheme is feasible, because based on the above analysis, the memory window is independent of the $V_{read\text{-}pass}$ applied to the bottom oxide-gate. With the present scheme, the merit of the previous structure shown in Fig. 3-10(b) in eliminating the read-pass disturb can be sustained, while two unique merits can be generated: 1) Easier fabrication due to elimination of the constraints stemmed from the precise alignment of the top and bottom gates, 2) less occupied areas owing to the replacement of the serial contact holes by a common bottom oxide-gate. However, in terms of the application in three-dimensional stackable flash memory technologies, the scheme shown in Fig. 3-10(a) also suffers from the high thermal budget associated with n^+ S/D regions. This issue can be addressed by anther new scheme shown in Fig. 3-11(a), where a novel junctionless (J-less) architecture is

adopted to replace the original undoped channel regions by a heavily doped one. As mentioned in Sec. 1-3, a J-less device features heavy and homogeneous doping concentration across source, channel, and drain and, thus, the original concerns related to the high thermal budget can be relaxed. In addition, low-pressure chemical vapor deposition (LPCVD) *in-situ* doped poly-Si film can be utilized to form such a heavily doped film in the J-less version. Such an implantation-free process can greatly simplify the complexity of device fabrication.

Finally, we briefly summarize some of the additional advantages of the proposed structure shown in Fig. 3-11(a): (i) Similar to the conventional DG structure [3.7][3.18], the common bottom-gate provides electrostatically enhanced short-channel effect control which is helpful for device scaling. (ii) The P/E efficiency can be improved as an appropriate bias is applied to the bottom control gate, as has been demonstrated in one of our previous work [3.11]. (iii) The fabrication involves mainly mature poly-Si preparation techniques and has the properties associated with implantation-free and low thermal budget, making it suitable for monolithic three dimensional integration. In addition, the concept is not restricted to the planar scheme shown in Fig. 3-11(a). If some modifications are made, the scheme can also be applied to the BiCS structures [3.19]~[3.20]. This is shown in Fig. 3-11(b), in which a scheme modified from BiCS is shown. In this structure, the inner and exterior gates sandwiching the vertical cylindrical

channel serve as the common oxide-gate and individual ONO-gate, respectively.

3-7 Summary

In this chapter, the characteristics of IDG poly-Si NW SONOS devices under two kinds of read mode are characterized. Theoretical analysis indicates that the memory window is independent of the bias applied to the control gate when the gate of charge storage side is used as the driving gate for sensing the V_{th}. Such predictions are confirmed with experimental results as well. Based on the above findings, novel schemes containing a string of J-less SONOS cell devices with planar or vertical channel and a common control gate are proposed for three-dimensional flash memory applications considering the feasibility of a simple and low-temperature process. In addition, such schemes can also retain the inherent merits associated with the IDG configuration, such as good control over the short-channel effects, improved P/E efficiency, and suppressed read disturb.

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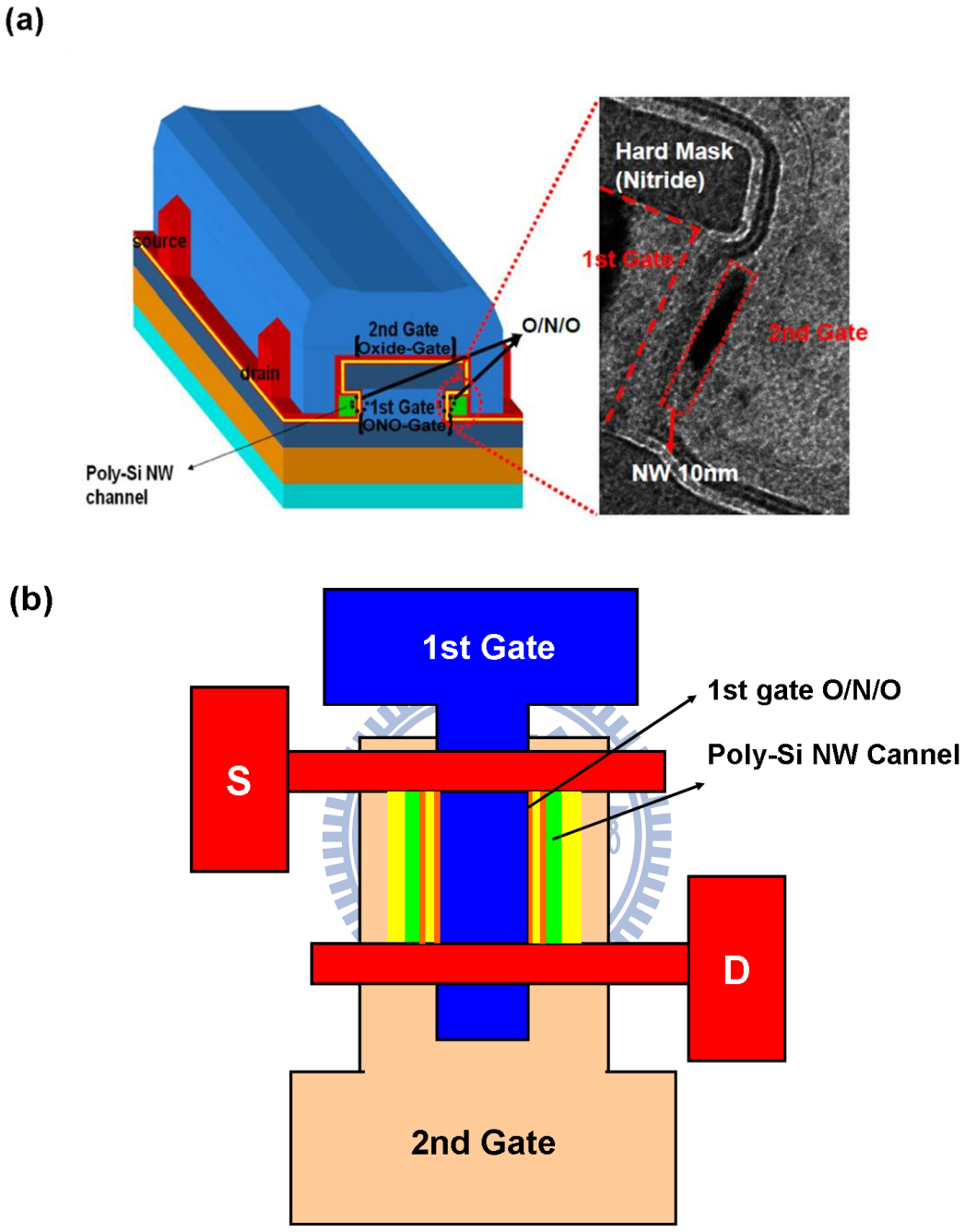

Fig. 3-1 (a) Stereo view as well as the cross-sectional TEM image and (b) top view of the n-type IDG poly-Si NW SONOS TFT characterized in Chapter 3. ONO and oxide are used as the gate dielectrics of the first and second gates, respectively.

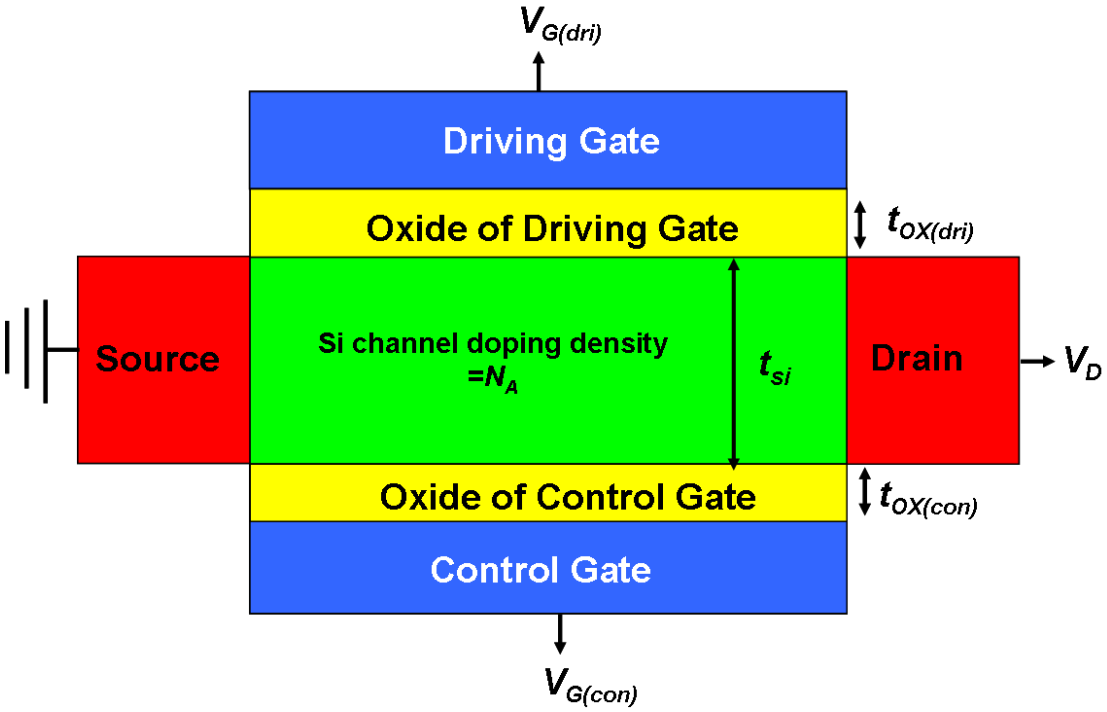

Fig. 3-2 Schematic structure of a typical n-type IDG device for analysis in Sec. 3-3.

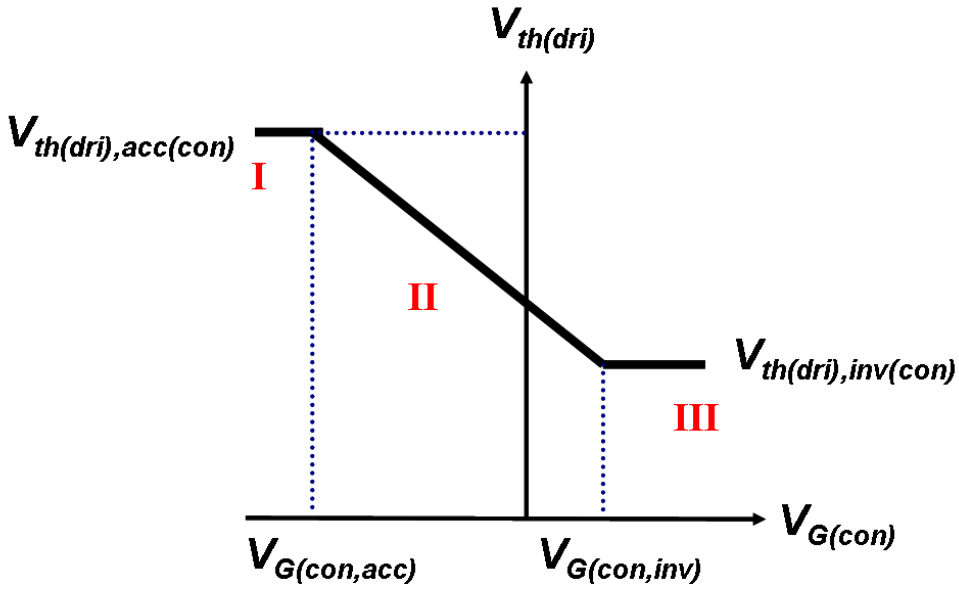

Fig. 3-3 $V_{th(dri)}$–$V_{G(con)}$ characteristics of a typical n-type IDG device. Three distinctly different regions corresponding to various channel surface conditions of the control gate side can be defined.

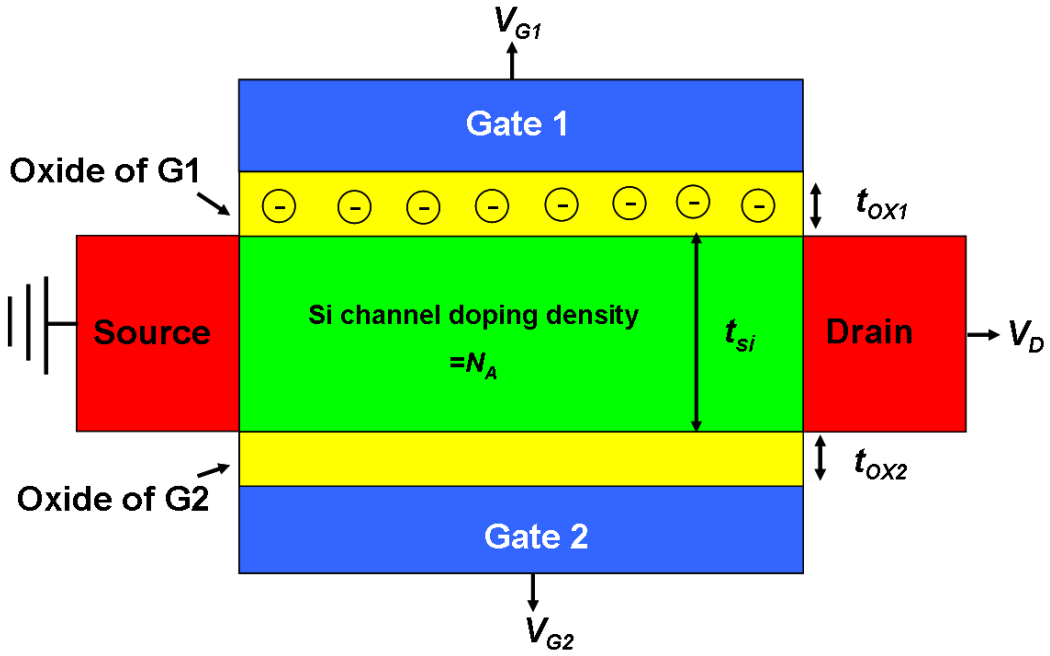

Fig. 3-4 Schematic structure of the n-type IDG devices with extra negative charges incorporated in the gate oxide of G1.

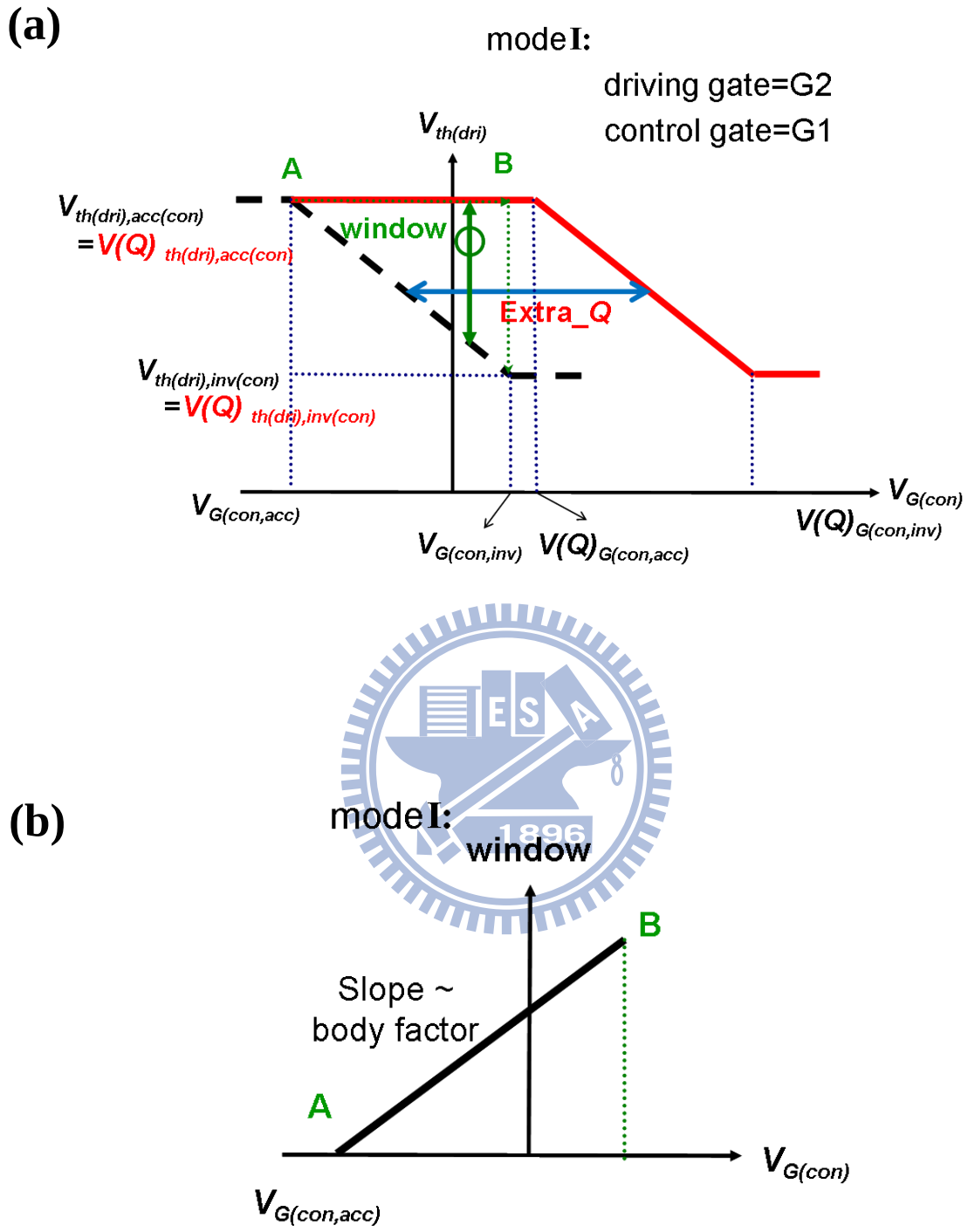

Fig. 3-5 (a) $V_{th(dri)}$ versus $V_{G(con)}$ characteristics and (b) memory window versus $V_{G(con)}$ read in mode I with or without extra charges incorporated.

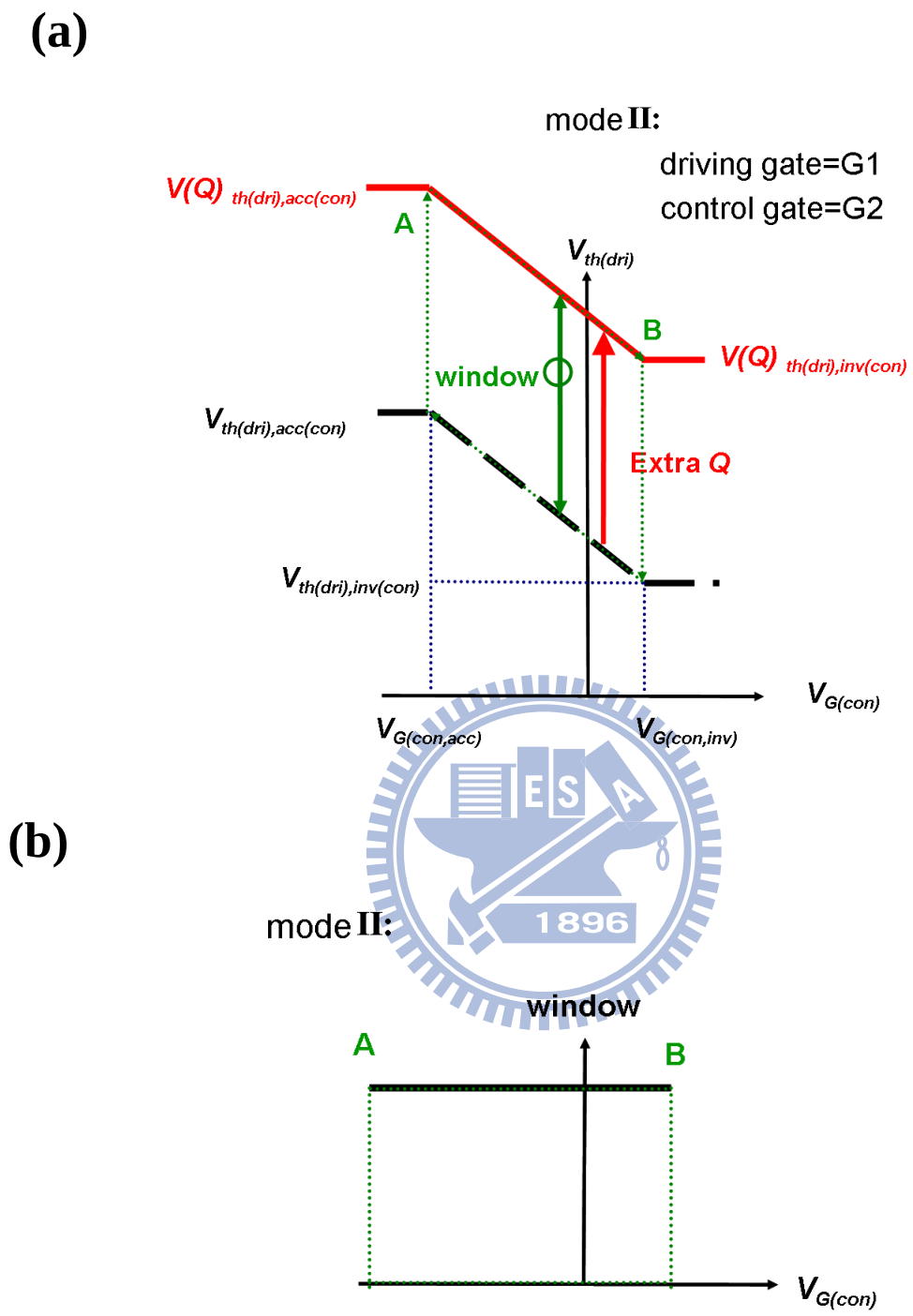

Fig. 3-6 (a) $V_{th(dri)}$ versus $V_{G(con)}$ characteristics and (b) memory window versus $V_{G(con)}$ read in mode II with or without extra charges incorporated.

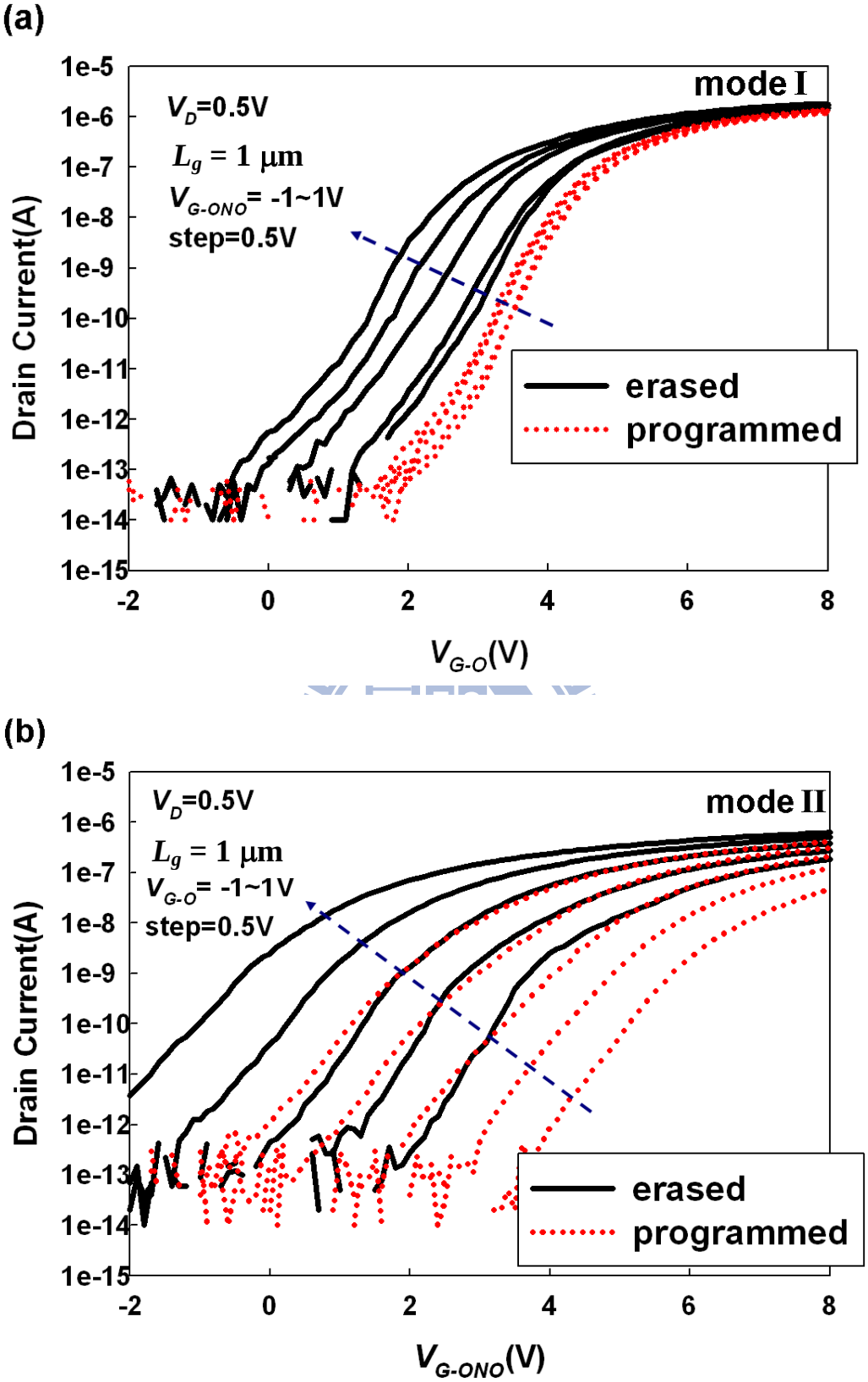

Fig. 3-7 Measured transfer characteristics of the programmed (dotted lines) and erased (solid lines) states in the IDG poly-Si NW SONOS TFT under (a) mode I and (b) mode II.

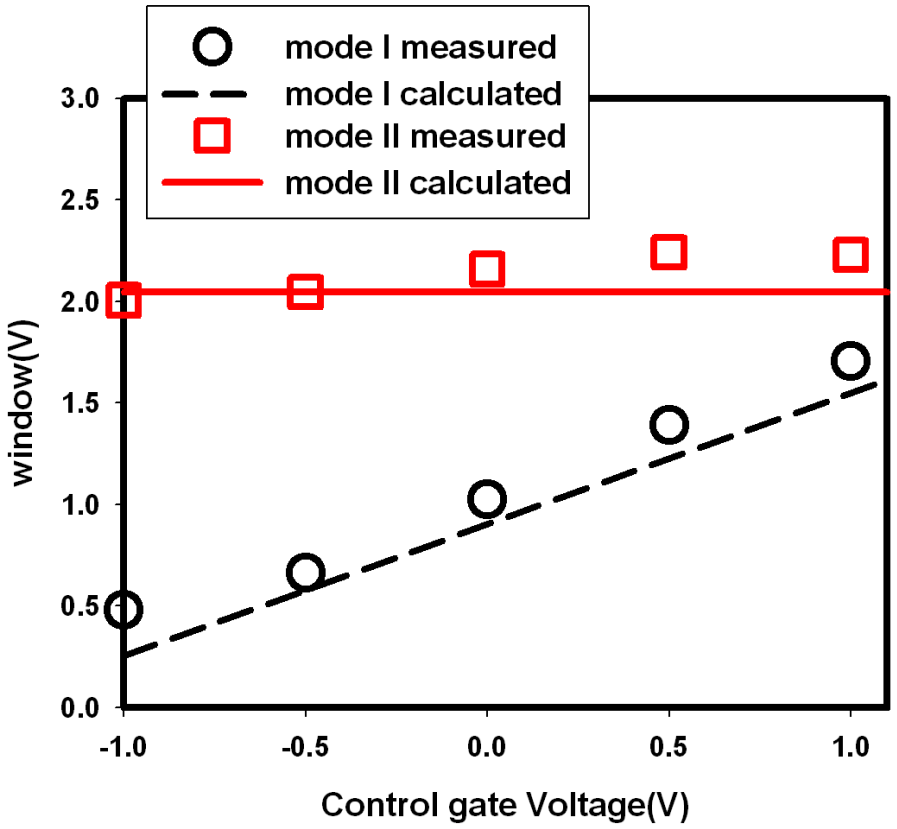

Fig. 3-8 Memory window as a function of control-gate bias read in modes I and II. The dash and solid lines refer to calculated results for modes I and II, respectively, and the circle and square symbols are the extracted results from the transfer characteristics shown in Figs. 3-7(a) and (b), respectively.

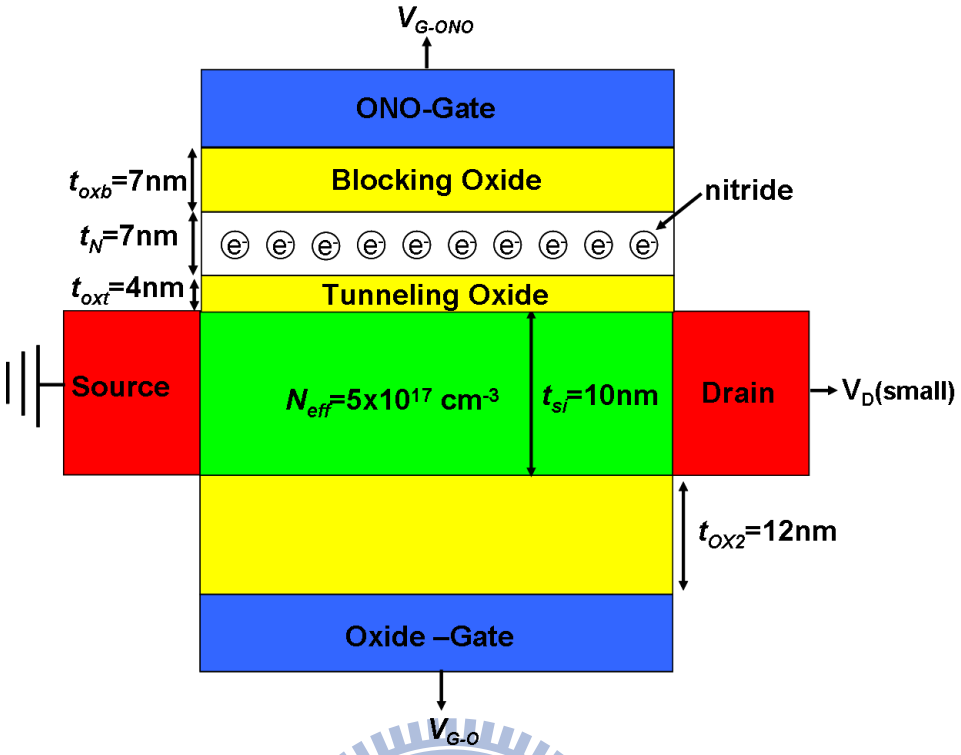

Fig. 3-9 Two-dimensional schematic structure of the n-type IDG poly-Si NW SONOS device, including detailed device parameters applied in the calculation.

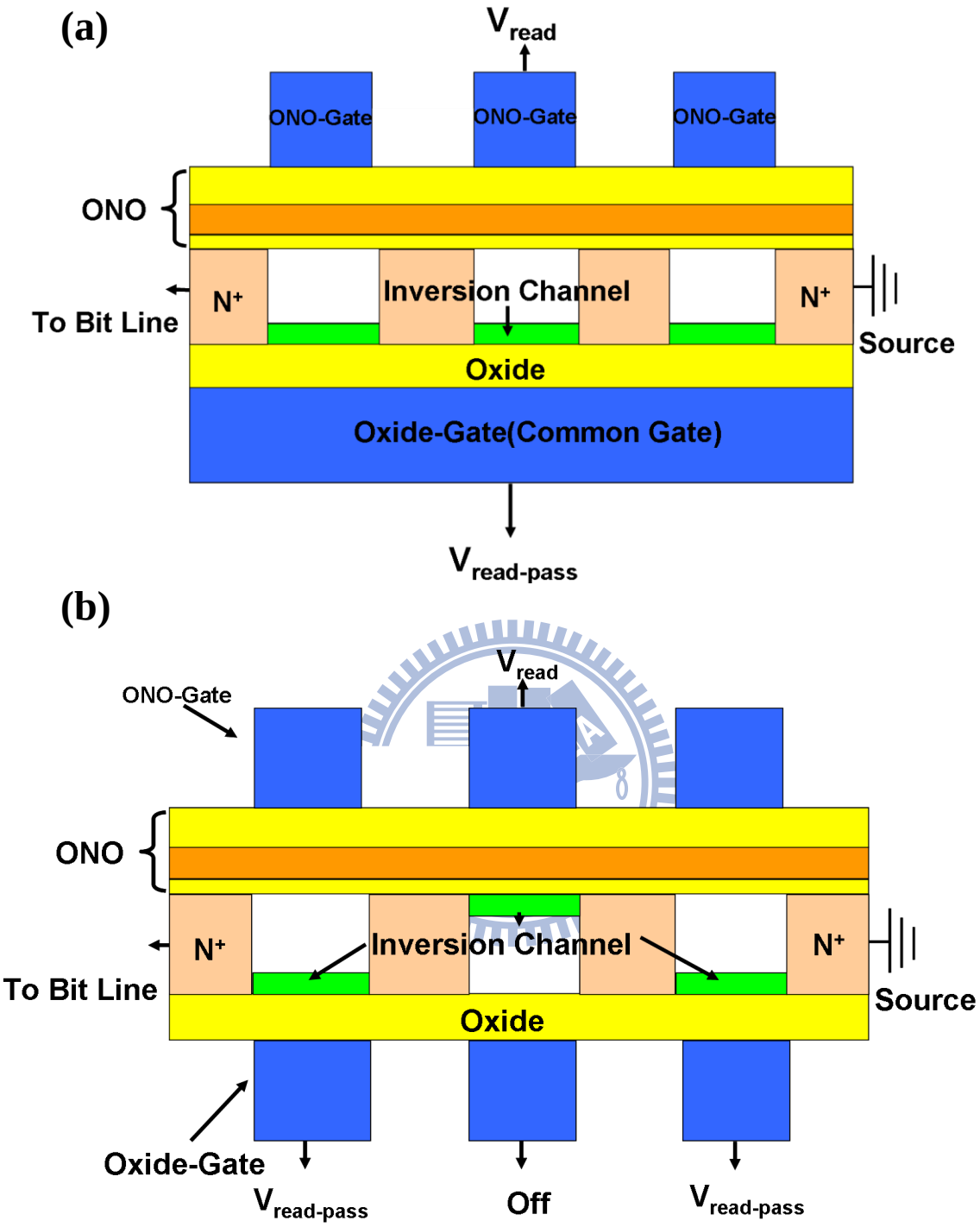

Fig. 3-10 (a) Proposed flash structure consisted of a series of IDG SONOS cell devices and a common control gate. (b) Previous structure consisted of a series string of IDG SONOS cell devices. Each cell has its own control gate.

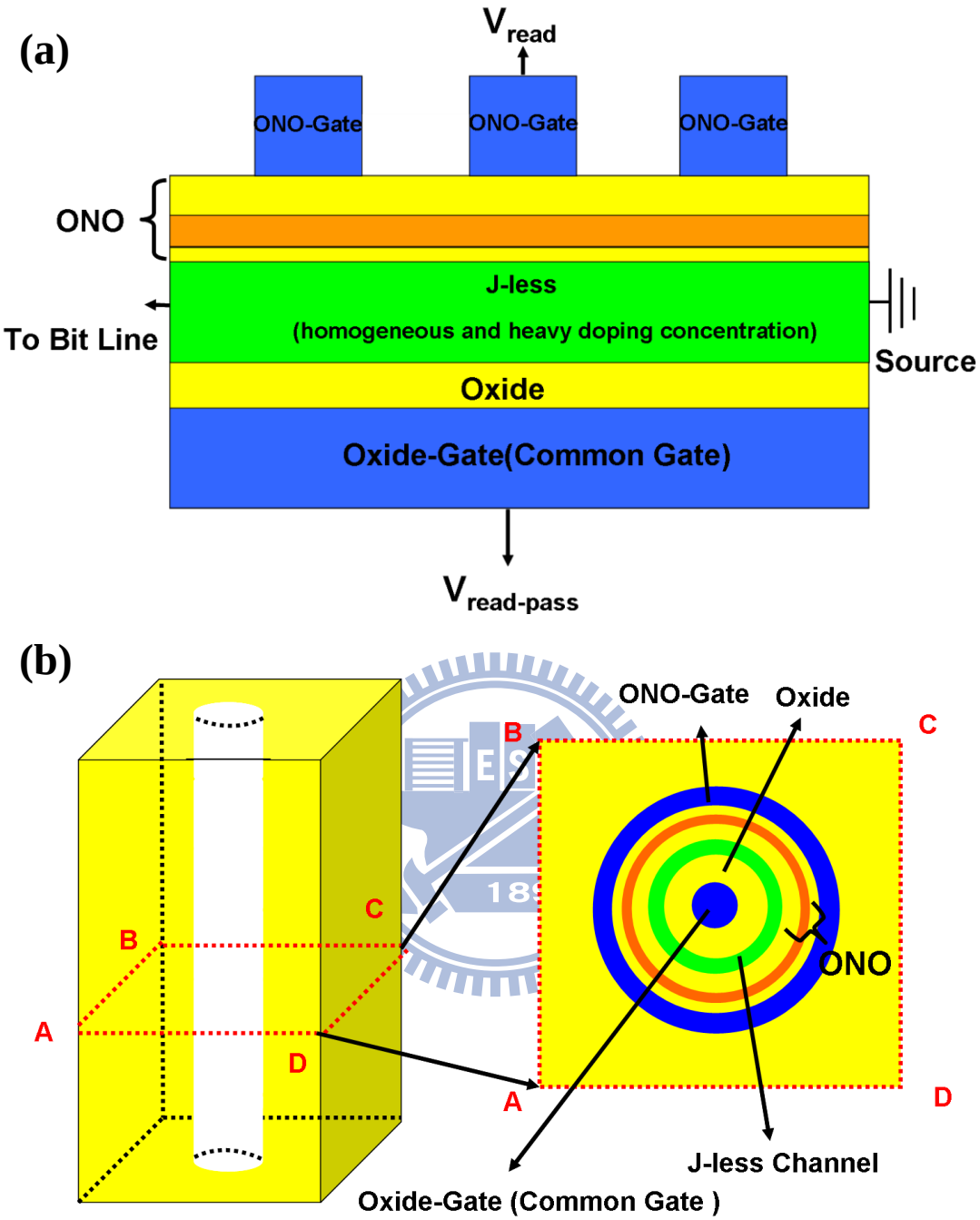

Fig. 3-11 A series of (a) IDG J-less SONOS cell devices and (b) three-dimensional IDG J-less SONOS cell devices with vertical channel. Both of them feature homogeneous and heavy doping concentration across source, channel, and drain.

Chapter 4

A New Methodology for Probing the Electrical Characteristics of Heavily Phosphorous-Doped Poly-Si Nanowires with Gated-All-Around (GAA) Junctionless (J-less) Structure

4-1 Introduction

As indicated in Sec. 1-3, several potential advantages, such as superior current drive [4.1], skipping altogether difficulties encountered in forming shallow and uniform S/D junctions [4.2]~[4.3], and higher cutting frequency for RF applications [4.4], have been demonstrated in junctionless (J-less) nanowire (NW) transistors. In order to efficiently shut off the leakage current, J-less NW transistors usually adopt heavily doped silicon NWs with aggressively scaled cross-sectional area as the conduction channels. Therefore, regarding further optimization of the device performance of J-less NW transistors, it is critical to develop a methodology to measure the values of active doping concentration and mobility of the heavily doped silicon NW channel. The measurement can be made by adopting conventional techniques like Hall measurement, four-probe technique and secondary ion mass spectrometry (SIMS) to characterize the

doping properties or mobility of poly-Si films. In this regard, there had been considerable efforts made in previous works [4.5]~[4.7]. However, these methods may not be appropriate for the poly-Si NW structure for the following two concerns: First, they do not take into account the effects associated with the fabrication and structures, like dopant segregation [4.8]. Second, as the feature size of the devices reaches to the nano-scale regime, the dimensionality and size of the poly-Si NW may show great impacts on their electrical properties [4.9]. Therefore, it is doubtful that the electrical properties determined from the bulk poly-Si films can really reflect those in poly-Si NWs. Although, in one of the previous works [4.10], the active doping concentration of *in situ* phosphorous-doped c-Si NWs was directly probed and studied, the value of mobility used in the analysis for extracting the carrier concentration was approximated by the result of the Hall measurement, leading one to question the accuracy of the analysis.

In this chapter, we propose a new methodology based on characterizing the performance of gated-all-around (GAA) J-less NW transistors with *in situ* phosphorous-doped poly-Si NWs channel. We'll show that this methodology is capable of extracting the major parameters, like the active doping concentration and mobility of the phosphorous-doped poly-Si NWs. Moreover, the interface fixed oxide charge density of the GAA *in situ* phosphorous-doped poly-Si NW J-less transistor can be

detected at the same time. The remaining part of this chapter is organized as follows: In Sec. 4-2, the fabrication process of the GAA *in situ* phosphorous-doped poly-Si NW J-less transistors is detailed. Next, in Sec. 4-3, we present the impacts of NW's cross-sectional area on the device characteristics and discuss the operation of the J-less devices, including the interesting leaky characteristics of the NW devices with a rather large cross-sectional area. Then, a theoretical model is detailed in Sec. 4-4 to establish the relations between the structural and electrical parameters. In Sec. 4-5, the methodology of parameter extraction, experimental verification, and discussion are given. Results of the major parameters extracted from the developed procedure are further discussed and compared to those from Hall or SIMS measurements in Sec. 4-6. Moreover, the results are also compared with those from C-V measurements performed on planar J-less transistors in Sec. 4-7. Finally, Sec. 4-8 summarizes the major contributions and observations of this chapter.

4-2 Device Fabrication

Details of the fabrication process of the GAA *in situ* phosphorous-doped poly-Si NW J-less transistor investigated in this chapter basically follow those presented in one of our previous works [4.1]. The key steps are shown in Figs. 4-1(a)~(f), respectively. First, a 50nm bottom nitride layer was deposited by low pressure chemical vapor

deposition (LPCVD) on silicon substrate capped with 200nm-thick wet oxide. Then a 30nm dummy TEOS oxide and a 30nm dummy-nitride layer (hard mask layer) were deposited (Fig. 4-1(a)). Next, the dummy nitride/TEOS gate stack was patterned by anisotropic reactive plasma etching (Fig. 4-1(b)). Diluted HF (DHF) etching was subsequently employed to laterally etch the TEOS oxide layer and form cavities underneath the nitride hard mask (Fig. 4-1(c)). Next, a 100nm *in situ* phosphorous-doped poly-Si film was deposited by a vertical LPCVD with SiH_4 of 0.49 slm and PH_3 of 15 sccm, followed by patterning and etching in a transformer-coupled plasma (TCP) reactor using Cl_2/HBr gases to define NW channels and S/D regions simultaneously (Fig. 4-1(d)). Then, nitride hard mask, dummy TEOS and bottom nitride were removed respectively by DHF and hot H_3PO_4 solutions (Fig. 4-1(e)). Finally, a LPCVD TEOS oxide layer of 18nm was deposited as the gate dielectric and a 150nm *in situ* doped poly-Si film which was sequentially deposited and patterned to serve as the gate electrode (Fig. 4-1(f)). The top view and cross-sectional view SEM images of a GAA *in situ* phosphorous-doped poly-Si NW J-less transistor (denoted as Device 4-A in this chapter) are shown in Figs. 4-2(a) and (b), respectively.

4-3 Impacts of the Cross-sectional Area of the NWs

From the cross-sectional SEM image shown in Fig. 4-2(b), it can be seen that

Device 4-A has a rectangular-shaped cross-section with area of 70×27 nm^2. Fig. 4-3 compares the transfer characteristics of Device 4-A with that of a device (denoted as Device 4-B). Device 4-B has a much smaller cross-sectional area of around 23×12 nm^2 [4.1] and almost identical process flow of Device 4-A except for the replacement of an *in situ* poly-Si gate by a TiN gate. It can be seen that the subthreshold characteristics and on/off current ratio can be dramatically improved by scaling down the size of poly-Si NW. Such a finding is reasonable considering the fact that the turning off of the channel conduction current of the J-less devices relies on the effective depletion of the channel [4.2]~[4.3]. In Device 4-A, owing to the rather large cross-sectional dimensions of the NW channels, the leakage along the core region of the NW would keep flowing even as a large negative gate voltage is applied. In contrast, thanks to the much reduced area, the whole channel is depleted for Device 4-B in the off regime, sharply off characteristics is thus resulted.

Although the Device 4-A with fatter poly-Si NW channels could not be turned off effectively, its transfer characteristics are cleverly analyzed in this thesis to acquire the active doping concentration and mobility of the *in situ* phosphorous-doped poly-Si NWs. Details about the methodology including theoretical analysis and experimental verification are elaborated in the next sections.

4-4 Theoretical Background

The cross-sectional view of the device along line A-A' shown in Fig. 4-2(a) is plotted in Fig. 4-4, where H, W, t_{ox}, n, and $X_{depl}(V_G)$ are the height, width, effective oxide thickness, active doping (or carrier) concentration, and depletion region width (as a function of gate voltage) of the heavily-doped poly-Si NW channel, respectively. In the following treatment, n is assumed to be uniform inside the poly-Si NW. X_{depl} is related to the applied bias condition and decreases with increasing n. Owing to the rather thick structure and the high channel doping, the investigated Device 4-A is partially depleted during off-state operation and X_{depl} is expected to be much smaller than both H and W. This allows us to use one-dimensional Poisson's Equation to calculate the electric potential in the depletion region shown in Fig. 4-4. The one-dimensional Poisson's equation along x-direction (Fig. 4-4) is expressed as

$$\frac{d^2\Phi_{1D}(x)}{dx^2} = \frac{-qn}{\varepsilon_{si}}, \tag{4-1}$$

where Φ_{1D} is the electric potential, ε_{si} is the dielectric constant of silicon, and q is the electric charge. In Fig. 4-4, x = 0 corresponds to the interface between top gate oxide and NW channel. The two boundary conditions applied for solving Eq. 4-1 are listed below

$$E(x = X_{depl}) = 0, \tag{4-2}$$

$$\Phi_{1D}(x = X_{depl}) = 0, \tag{4-3}$$

where $E(x = X_{depl})$ and $\Phi_{1D}(x = X_{depl})$ are the electric field and electric potential, respectively, at the edge of depletion region. By applying the two boundary conditions to solve Eq. 4-1, the solution of electric potential can be expressed as

$$\Phi_{1D}(x) = \frac{qnX_{dep}}{\varepsilon_{si}} x - \frac{qn(x^2 + X_{dep}{}^2)}{2\varepsilon_{si}}, \qquad 0 < x < X_{dep}. \tag{4-4}$$

To turn off an n-channel J-less transistor, the gate bias is decreased to increase X_{depl} and thus decreases the available area in the NW core for current conduction. Nonetheless, X_{depl} is limited by the maximum voltage drop in the heavily doped Si NW which is close to but smaller than the bandgap of Si. The maximum depletion width, $X_{depl,\,max}$, and the gate voltage as $X_{depl,\,max}$ is reached and the gate voltage corresponding to the reaching of $X_{depl,\,max}$, $V_{G,\,off}$, can be expressed as follows:

$$X_{depl,\max} = \sqrt{2\varepsilon_{si}[E_g / 2 + kT / q \ln(n / n_i)] / qn}), \tag{4-5}$$

$$V_{G,off} = V_{FB} - \frac{qnX_{depl,\max}}{C_{ox}} - (\frac{E_g}{2}) + \frac{kT}{q}\ln(\frac{n}{n_i}), \tag{4-6}$$

$$V_{FB} = \frac{E_g}{2} - \frac{kT}{q}\ln(\frac{n}{n_i}) - \frac{Q_{fix}}{C_{ox}}, \tag{4-7}$$

where V_{FB}, Q_{fix}, C_{ox}, n_i, E_g and kT/q are flat-band voltage, fixed charges at oxide/channel interface, gate oxide capacitance per unit area, intrinsic carrier concentration, silicon bandgap, and thermal energy at room temperature, respectively. As V_G is smaller than $V_{G,\,off}$, $X_{dep,\,max}$ is reached and retained. In other words, the device

operation changes from a gated resistor (as $V_G > V_{G,off}$) to an ungated one (as $V_G < V_{G,off}$) in which the current flow is conducted through the quasi-neutral core region with a conduction area not affected by the gate bias. Fig. 4-5 is the cross-section along the B-B' cutline in Fig. 4-2(a) showing the situation as $X_{depl,\ max}$ is reached. For a long-channel device operated at a low V_D, $X_{depl,\ max}$ should be quite uniform across the channel and, from Fig. 4-4, the area for the leakage current of the ungated resistor to conduct can be approximated as $H \times W - 2(H+W)X_{depl,\max} + 4X_{depl,\max}{}^2$. In addition, according to the previous work [4.5], the impact of grain boundary defects on the mobility of poly-Si films can be ignored as the doping is larger than 10^{19} cm^{-3}. In this study, the adopted poly-Si NWs are formed by heavily *in situ* phosphorous-doped poly-Si films; therefore, the effects associated with the grain boundary defects contained in poly-Si NW channel are not taken into account. Consequently, the resistance of the ungated resistor, *R*, can be expressed with the following form:

$$R = V_D / I_D = L / nq\mu(H \times W - 2(H+W)X_{depl,\max} + 4X_{depl,\max}{}^2), \qquad (4\text{-}8)$$

where μ is the effective mobility. *R* can be obtained from the information contained in the ungated operation regime, *i.e.*, $V_G < V_{G,off}$.

4-5 Experimental Verification and Discussion

Fig. 4-6 shows a flowchart which compiles the main procedures of our proposed

methodology related to the extraction of active doping concentration, interface fixed oxide charge density, and mobility of the *in situ* phosphorous-doped poly-Si NWs. The first part of the methodology is centered on the determination of active doping concentration and interface fixed oxide charge density. As shown in the flowchart in Fig. 4-6, active doping concentration can be determined by the $V_{G,\,off}$ and V_{FB} on the basis of Eqs. 4-5 and 4-6. In order to extract the $V_{G,\,off}$, we first perform the measurement of the I_D-V_G characteristics of Device 4-A in negative V_G regime at V_D ranging from 0.25 ~ 1.25 V with EOT value of 18 nm and channel length value of 5 μm. The results are shown in Fig. 4-7(a). In the figure, obviously two distinct regions divided with the dashed line shown can be identified. In one of the regions (*i.e.*, larger V_G), transport current is obviously related to the applied gate voltage, indicating that the device acts like a gated resistor [4.2]~[4.3]. In contrast, in the other region (*i.e.*, smaller V_G) the current is essentially independent of the gate bias. This confirms the inference made in the above section that $X_{depl,\,max}$ is reached as $V_G = V_{G,,off}$ and retained as $V_G < V_{G,\,off}$.

However, more precise determination of $V_{G,\,off}$ should be attained by plotting the transconductance (G_m) as a function of V_G, and the results are shown in Fig. 4-7(b). Since G_m is the differentiation of drain current to gate voltage, it suddenly drops to zero when the device transfers from gated- to ungated-resistor behavior. This transition indeed occurs in the figure, and $V_{G,\,off}$ can be extracted as the gate voltage when G_m

drops to zero, which is -9.1 V in this case. On the other hand, V_{FB} can also be determined as the gate voltage corresponding to the G_m peaks in Fig. 4-7(b). It is because that, as V_G is smaller than V_{FB}, X_{depl} exists and tends to increase the effective EOT of the gate dielectric. The additional EOT contributed by X_{depl} decreases with increasing V_G, one of the reasons responsible for the increase in G_m as $V_G < V_{FB}$. This mechanism sustains until V_{FB} is reached, resulting in the G_m peak. From Fig. 4-7(b), it is seen that the G_m peaks show a very weak dependence on the applied V_D, and the corresponding V_G (= 2.88 V) is determined to be V_{FB}. Owing to the values of $V_{G,off}$ (= -9.1 V) and V_{FB} (= 2.88 V), the active doping concentration (n) of the doped poly-Si NW can be extracted to be 1.18×10^{19} cm^{-3} according to Eq. 4-6. Furthermore, as shown in the flowchart in Fig. 4-6, a negative interface fixed charge density (Q_{fix}) of -3.25×10^{12} cm^{-2} can be extracted by inserting the determined values of active doping concentration and flatband voltage into Eq. 4-7.

Next, we move on to the second part of the methodology with emphasis on the determination of the mobility of *in situ* phosphorous-doped poly-Si NWs. As shown in the flowchart in Fig. 4-6, the mobility (μ) is determined by the resistance of the ungated resistor (R), active doping concentration (n), H, W, and L based on Eq. 4-8. As mentioned above, the extracted active doping concentration is equal to 1.18×10^{19} cm^{-3}. From the SEM image shown in Fig. 4-2(b), H and W of Device 4-A are 27 nm and 70

nm, respectively. In addition, a long channel (5 μm) device is employed in this study to avoid the interference caused by short channel effects (SCEs). Furthermore, for the purpose of the determination of R, I_D in Fig. 4-7(a) measured at V_G = -10 V is rep-plotted and shown as a function of V_D in Fig. 4-8. In this figure, it can be seen that the current is proportional to drain voltage and its slope, which is equal to $1/R$, is $4.5\text{x}10^{-7}$ (A/V). On the basis of these results and Eq. 4-8, the mobility of doped poly-Si NW of Device 4-A is determined to be 52.5 cm^2/V-sec. Note that, based on the extracted value of n, the estimated $X_{depl,\,max}$ is 11 nm which is much smaller than W (=70 nm) and H (=27 nm) of the NW and supports the assumption made for the derivation of Eq. 4-8. Besides, to further verify the accuracy of the methodology proposed in Fig. 4-7(b) for determining V_{FB}, we simulate the electric potential across the middle of the NW along the y-direction (see Fig. 4-4) under various gate bias conditions with a TCAD tool [4.11]. The detail information for the key parameters applied to the TCAD tool methodology is summarized in Table 4-I. On the other hand, owing to the focus on the electrostatic characteristics of GAA poly-Si NW J-less transistors, basic models, such as the Poisson's equation, continuity equation, drift-diffusion model, and constant mobility models, are applied to the TCAD tool. The simulation results are shown in Fig. 4-9. It can be seen that electric potential is almost flat at V_G = 2.88 V, confirming the feature of flat-band condition. It is worth noting that the negative value of Q_{fix} at n^+Si/oxide

interfaces is reported for the first time.

4-6 Comparisons with the Results of SIMS and HALL Measurements

Table 4-II lists the measured results from SIMS, Hall measurements, and the proposed methodology. Note that the carrier concentration measured from Hall measurements is smaller than the dopant concentration obtained from the SIMS analysis, indicating the occurrence of dopant precipitation and segregation. More importantly, the carrier concentration is further reduced in the NW sample. One possible explanation for this observation is the segregation of phosphorous atoms to the oxide interface from the poly-Si NW [4.8], [4.12]. The segregation of phosphorous is postulated to be also responsible for numerous interface oxide fixed charges found in last section, although its origin needs more efforts to unveil. In addition, a reduction in the concentration of phosphorous in the Si material may also explain the increase in the effective carrier mobility of the NW sample as compared with the Hall mobility.

4-7 Further Verification by C-V Measurements on N-channel Planar J-less Transistors

The main goal of this section is to further verify the results obtained with the above proposed methodology with C-V characterization. The C-V measurements were performed on planar n-channel J-less transistors with an *in situ* phosphorous-doped poly-Si film as the conduction channel [4.13]. In this regard, based on a theoretical derivation given in the next paragraph, the *n* and Q_{fix} of the *in situ* phosphorous-doped poly-Si channel films can be extracted from the C-V results. The deposition condition of the *in situ* phosphorous-doped poly-Si channel films is identical to that of the NWs mentioned in Sec. 4-2 (*i.e.*, SiH_4 of 0.49 slm and PH_3 of 15 sccm in vertical furnace). The architecture of the investigated n-channel planar J-less transistors with raised source/drain (S/D) is shown in Fig. 4-10. For the purpose of efficiently turning the devices off, extra-thin poly-Si films are employed as the conduction channel. Actually, three split conditions of *in situ* phosphorous-doped poly-Si film of thicknesses of 8, 10, and 12 nm were performed in this section. Details of the fabrication flow can be seen in our previous work [4.13]. Also depicted in Fig. 4-10, the high/low terminals in the C-V measurements are applied to gate and S/D, respectively. Fig. 4-11 shows the cross-sectional TEM image of a fabricated device with *in situ* phosphorous-doped poly-Si channel film of 10 nm.

Next, the theoretical background associated with the proposed methodology based on the C-V measurement is elaborated on. An n-channel J-less transistor becomes

partially-depleted (PD) as gate voltage is larger than V_{th} but smaller than V_{FB} [4.14]. In the PD region, the effective capacitance (C_{eff}) of a J-less transistor is equal to the series connection of gate oxide capacitance and that attributed by the depletion region in silicon channel, as shown in Fig. 4-12(a), and thus, can be expressed as

$$\frac{1}{C_{eff}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}, \tag{4-9}$$

$$C_{dep} = \frac{\varepsilon_{si}}{X_{dep}}, \tag{4-9(a)}$$

$$X_{dep} = -\frac{\varepsilon_{si}}{C_{ox}} + \sqrt{(\frac{\varepsilon_{si}}{C_{ox}})^2 - \frac{2\varepsilon_{si}(V_G - V_{FB})}{qn}}, \tag{4-9(b)}$$

$$\frac{1}{C_{eff}} = \sqrt{\frac{1}{C_{ox}^{\ 2}} - \frac{2(V_G - V_{FB})}{qn\varepsilon_{si}}}. \tag{4-9(c)}$$

In addition, as shown in Fig. 4-12(b), when gate voltage is equal to or larger than the flatband voltage, C_{eff} is equal to gate oxide capacitance

$$\frac{1}{C_{eff}} = \frac{1}{C_{ox}}. \tag{4-10}$$

since electrons begin to be accumulated at the interface between channel and gate oxide.

Two devices with feature sizes of W(gate width) x L(gate length) of 10x10 μm^2 and 20x20 μm^2 are employed for the C-V measurements in order to eliminate the parasitic capacitance components associated with the S/D and test pads. Fig. 4-13 shows

the measured C-V characteristics of the three spilt conditions with frequency of 100 kHz. From Fig. 4-13, it can be seen that the measured capacitance tends to get saturated as the gate voltage is sufficiently large, an indication that electrons start to accumulate at the interface between channel and gate oxide. Such characteristics allow the flat-band voltage to be extracted as the gate voltage at the onset of C_{ox}=$C_{eff.}$ Once V_{FB} is obtained, the value of Q_{fix} can be determined with Eq. 4-7. Next, as gate voltage decreases to the region (V_{th} < V_G < V_{FB}), the n-channel J-less transistor is operated in the PD region. Therefore, by applying the extracted values of V_{FB} and C_{ox} to Eq. 4-9 to fit the measured C-V characteristics in PD region, the active doping concentration (n) can be obtained as well.

The comparison of the evaluated and measured C-V characteristics in planar J-less transistors of channel thickness of 8, 10, 12 nm, are shown in Figs. 4-14(a)-(c), respectively. In the figures, it can be seen that the theoretical evaluation can well describe the measured data except for the region of V_G < V_{th}. It is because that, as V_G < V_{th}, the remaining neutral region in the bottom of the channel (see Fig. 13(b)) is too thin to serve as a ground plane. As a result, the parasitic capacitance components originating from the bulk-Si substrate would participate in the measurements and make the measured value significantly lower than that estimated with Eq. 4-9.

The results of the C-V characterization are summarized in Table 4-III. In the table,

the channel thickness is determined by TEM characterization, while other parameters are extracted using the aforementioned procedure. These results are in close agreement with those shown in Table 4-II obtained from the characterization of the GAA NW devices. Moreover, the high negative interface fixed oxide charge density found in GAA devices is confirmed with the C-V analysis.

4-8 Summary

In this chapter, a simple procedure without complicated or expensive measurement setup is proposed to extract the major electrical properties of *in situ* phosphorous-doped poly-Si NWs, including the effective active doping concentration, mobility, and interface fixed charge density. Principles of this methodology rely on the operation of a GAA J-less transistor with a rather thick NW's cross-sectional dimensions. Such a device exhibits an un-gated operation behavior as gate bias is sufficiently negative, *i.e.*, $V_G \leqq V_{G,\,off}$, which is clearly observed in the practical measurements. Moreover, the gate voltage corresponding to $V_{G,\,off}$ and V_{FB} can be precisely determined from the G_m-*vs.*-V_G plots. Mobility could also be determined from the characteristics of the GAA J-less transistor operated in the ungated-resistor region. The extracted carrier concentration is significantly lower than that obtained from Hall measurements performed on blanket thin films. Segregation of phosphorous at gate oxide/NW

interface is postulated to be the major reason for the observed disparity. We've also identified the presence of negative fixed charges at the oxide interface, which is likely related to the dopant segregation as well. Furthermore, these measured properties of the heavily doped poly-Si NWs are compared with the results of C-V measurements performed on planar J-less transistors with an ultra-thin channel. Close agreement in the extracted carrier concentrations and interface state densities is obtained between the two characterization schemes.

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Parameter	Value
H (height of the heavily-doped poly-Si NW channel)	27 nm
W (width of the heavily-doped poly-Si NW channel)	70 nm
EOT (effective oxide thickness)	18 nm
L (channel length of Device A)	5 μm
n (active doping concentration)	1.18×10^{19} cm^{-3}
μ (mobility)	52.5 (cm^2/V-sec)
Q_{fix}(interface oxide charge density)	-3.25 x 10^{12} cm^{-2}

Table. 4-I Detailed parameters applied to a two-dimensional TCAD tool for the calculation of electric potential distributions shown in Fig. 4-9.

	SIMS	Hall	Poly-Si NW
Test structure	**Blanket thin film (400 nm-thick)**	**Blanket thin film (400 nm-thick)**	**NW J-less transistor**
Dopant or Carrier Concentration (cm^{-3})	10^{20}	$7x10^{19}$	$1.18x10^{19}$
Fixed Oxide charges (cm^{-2})	X	X	$-3.25x10^{12}$
Mobility (cm^2/V-sec)	X	42.7	52.5

Table. 4-II Results of SIMS, Hall measurements and the proposed methodology for *in situ* phosphorous-doped poly-Si NWs.

Test structure (Planar J-less transistor)	**t_{ch} = 8 nm**	**t_{ch} = 10 nm**	**t_{ch} = 12 nm**
Dopant or Carrier Concentration (cm^{-3})	$1.7x10^{19}$	$2.2x10^{19}$	$2.2x10^{19}$
Fixed Oxide Charges (cm^{-2})	$-6.8x10^{12}$	$-6.5x10^{12}$	$-5.5x10^{12}$
t_{ox}(nm)	8	8	8.2
V_{FB}(V)	2.6	2.4	2

Table. 4-III Results of extracted active doping concentration, interface fixed oxide charge density, oxide thickness, and flatband voltages from planar J-less transistors with channel thickness of 8, 10, 12 nm, respectively, by C-V measurements.

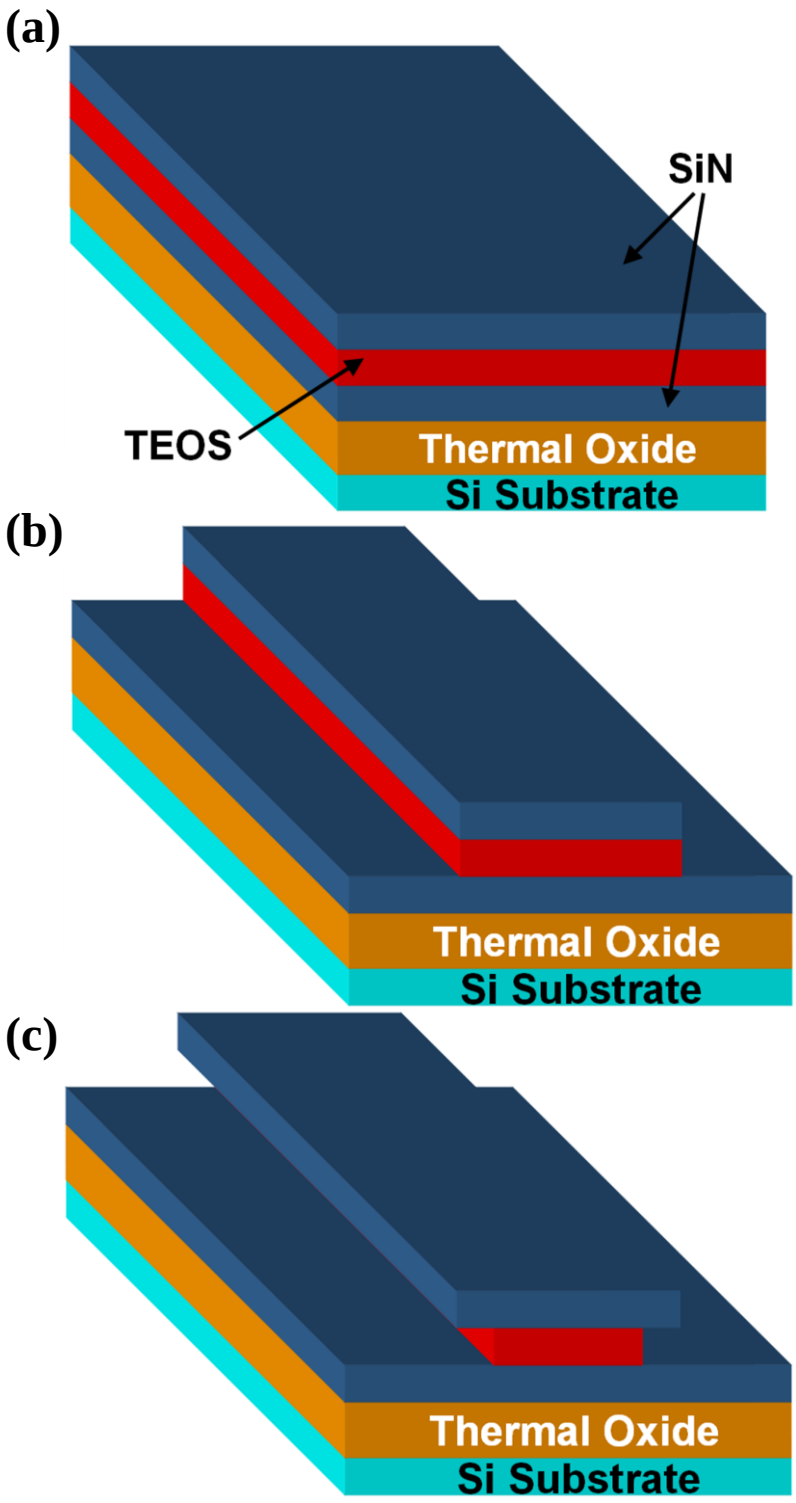

Fig. 4-1 (a)~(f) Key steps of the fabrication flow of the GAA poly-Si NW J-less transistors investigated in this chapter.

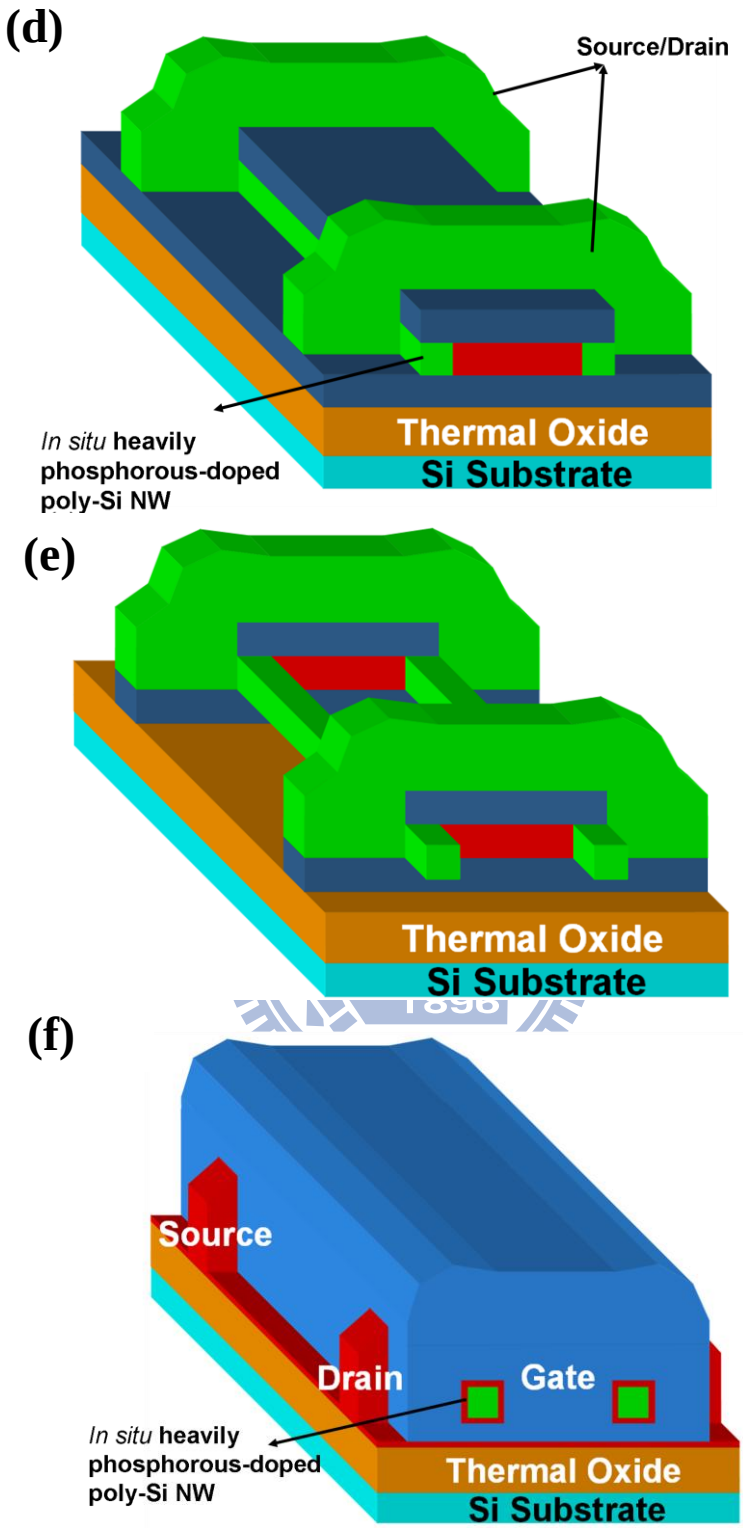

Fig. 4-1 (a)~(f) Key steps of the fabrication flow of the GAA poly-Si NW J-less transistors investigated in this chapter.

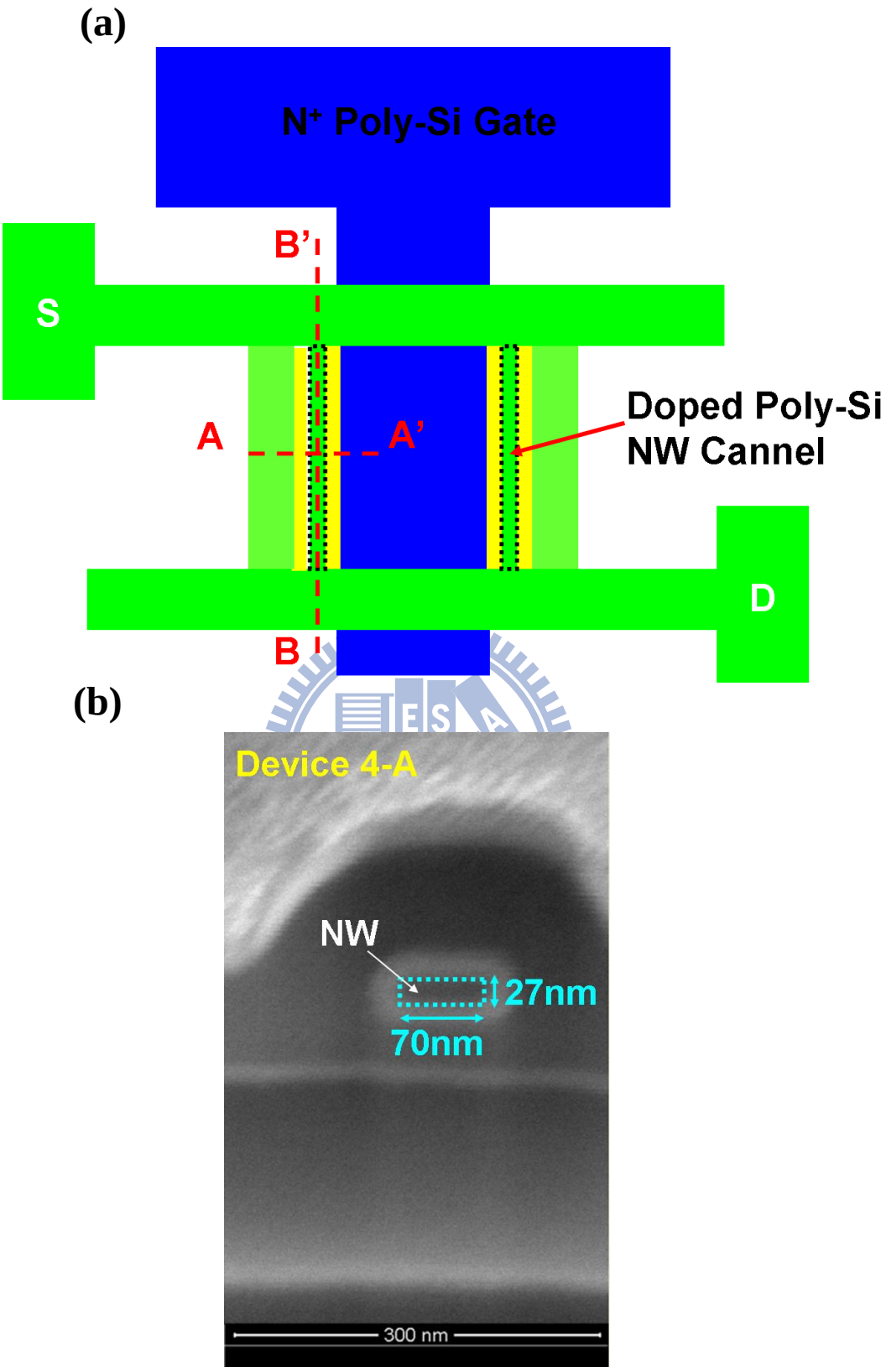

Fig. 4-2 (a) Top view and (b) cross-sectional SEM image of Device 4-A.

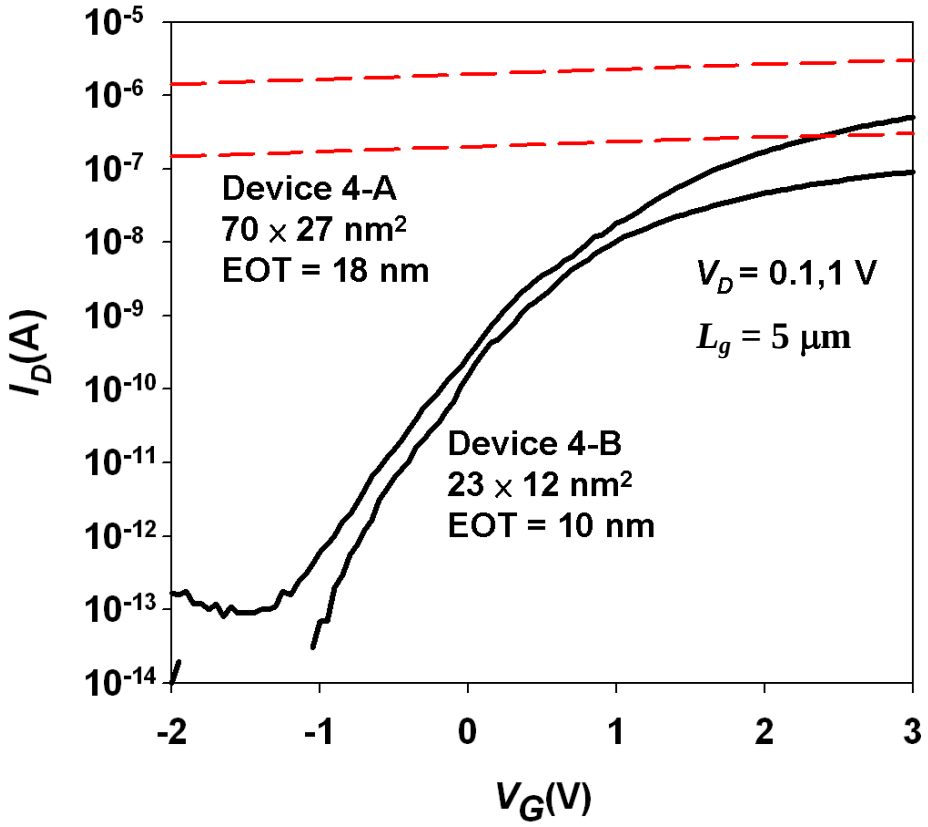

Fig. 4-3 I_D-V_G characteristics of Devices 4-A and -B. Device 4-B is with a much smaller cross-sectional area of around 23×12 nm^2 [4.1].

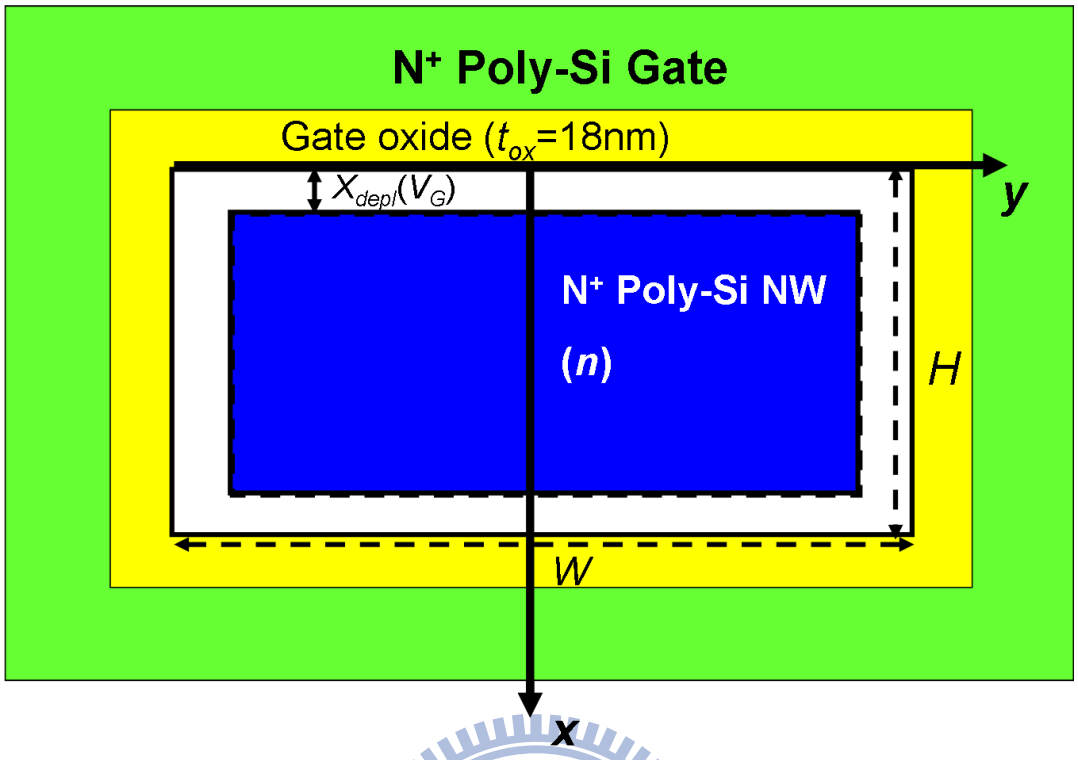

Fig. 4-4 Schematic illustration of the cross-sectional structure of the GAA J-less transistor as $V_G < V_{FB}$ along line AA' shown in Fig. 4-2(a).

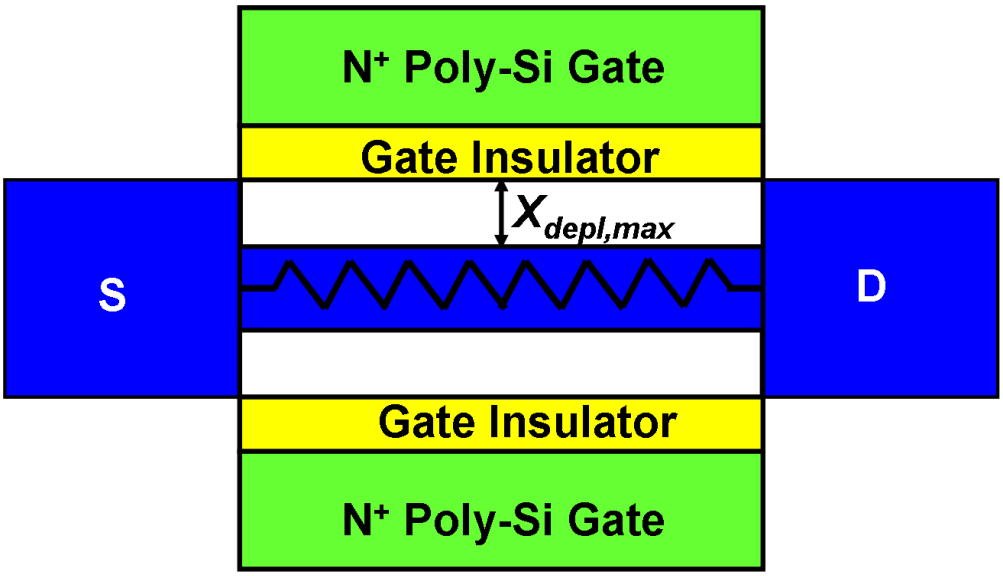

Fig. 4-5 Schematic illustration of the cross-sectional structure of the GAA J-less transistor as $V_G < V_{G,\,off}$ along line BB' shown in Fig. 4-2(b).

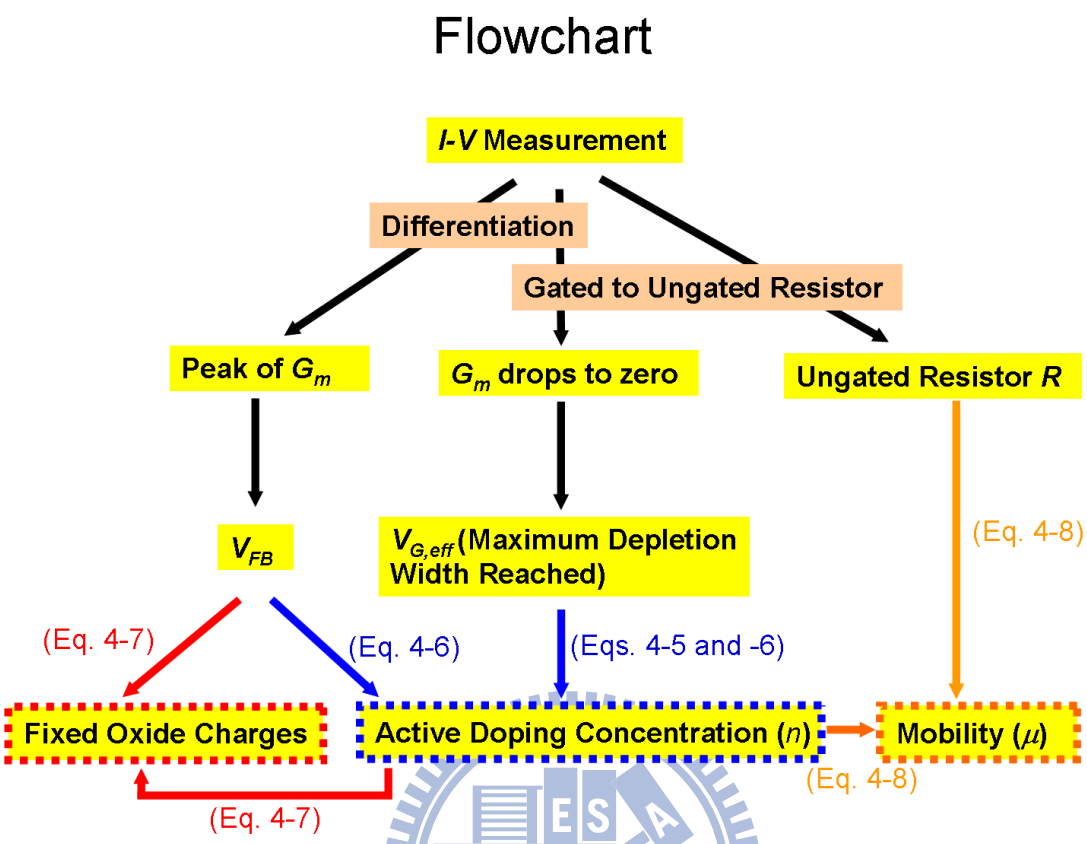

Fig. 4-6 The procedure flowchart detailing the proposed methodology for probing the active doping concentration as well as mobility, and interface fixed oxide charge density of the GAA poly-Si NW J-less transistor proposed in this chapter.

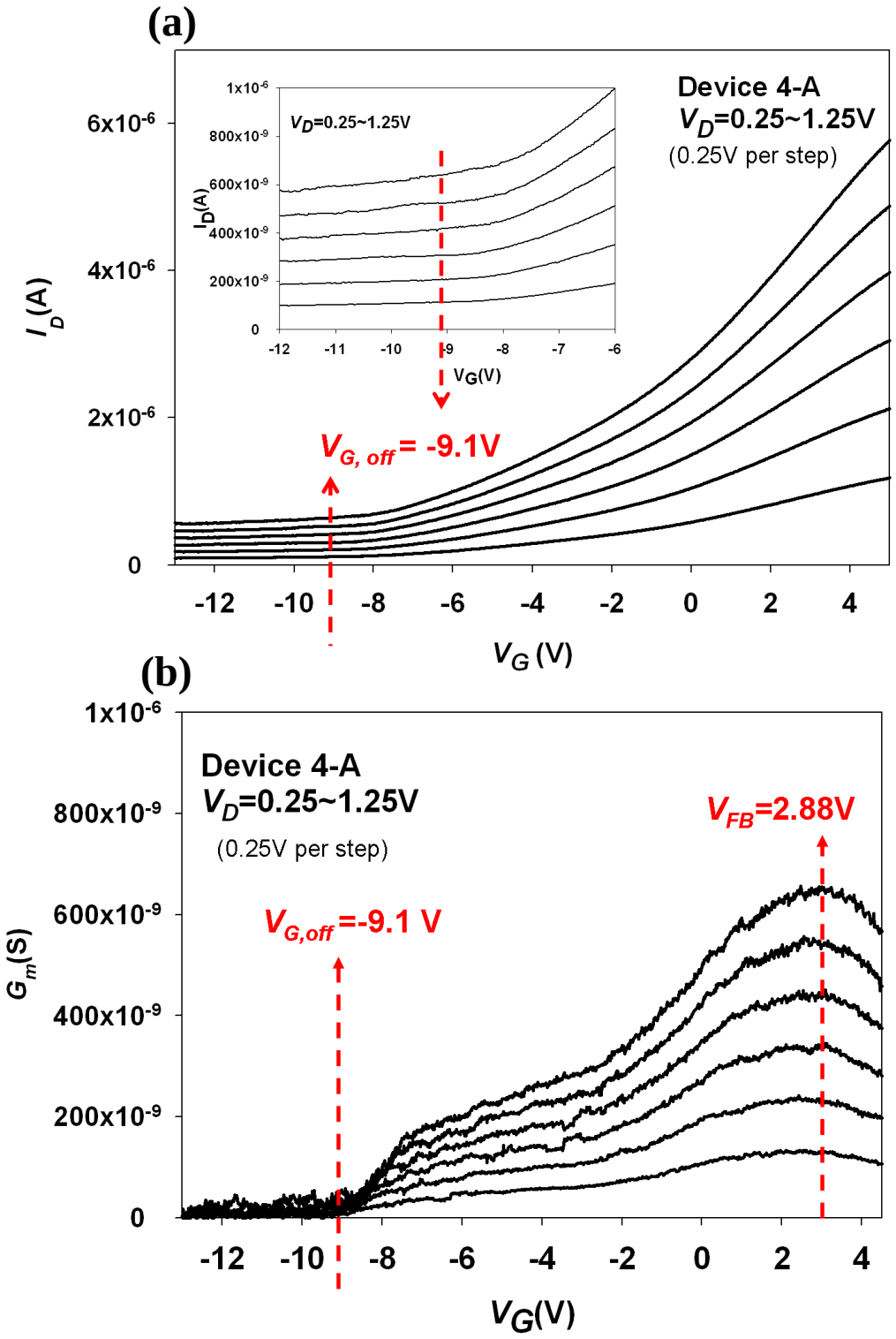

Fig. 4-7 (a) Transfer characteristics of Device 4-A measured at various V_D. The device behaves like an ungated resistor as V_G is smaller than -9.1 V. (b) G_m versus V_G measured at various V_D. $V_{G, off}$ and V_{FB} can be precisely determined from the plots.

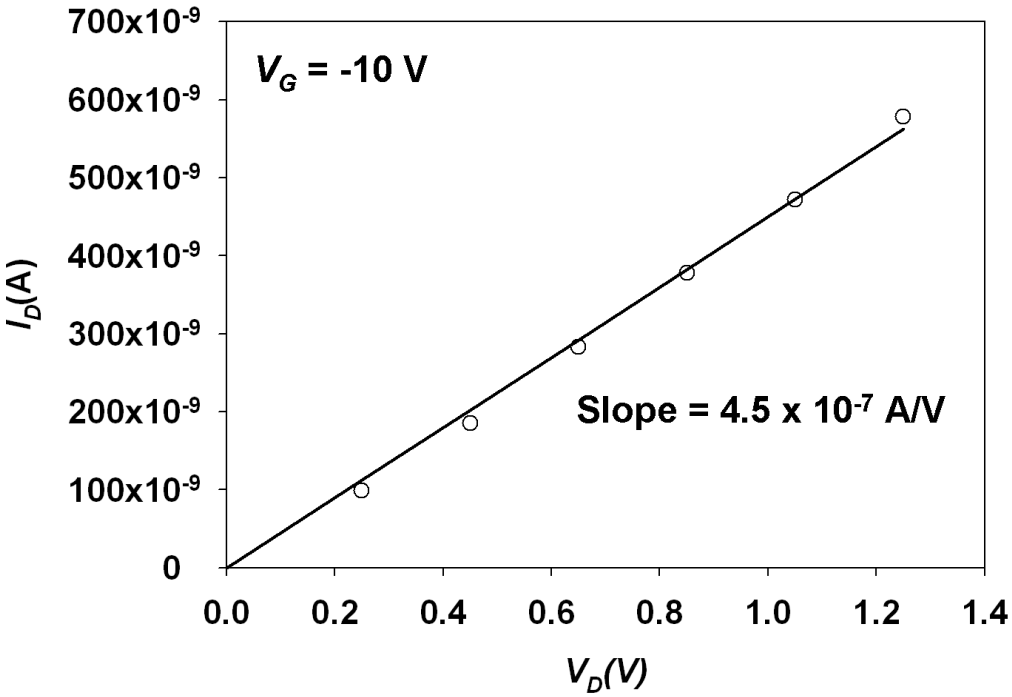

Fig. 4-8 I_D extracted from Fig. 4-7(a) at V_G = -10 V as a function of V_D.

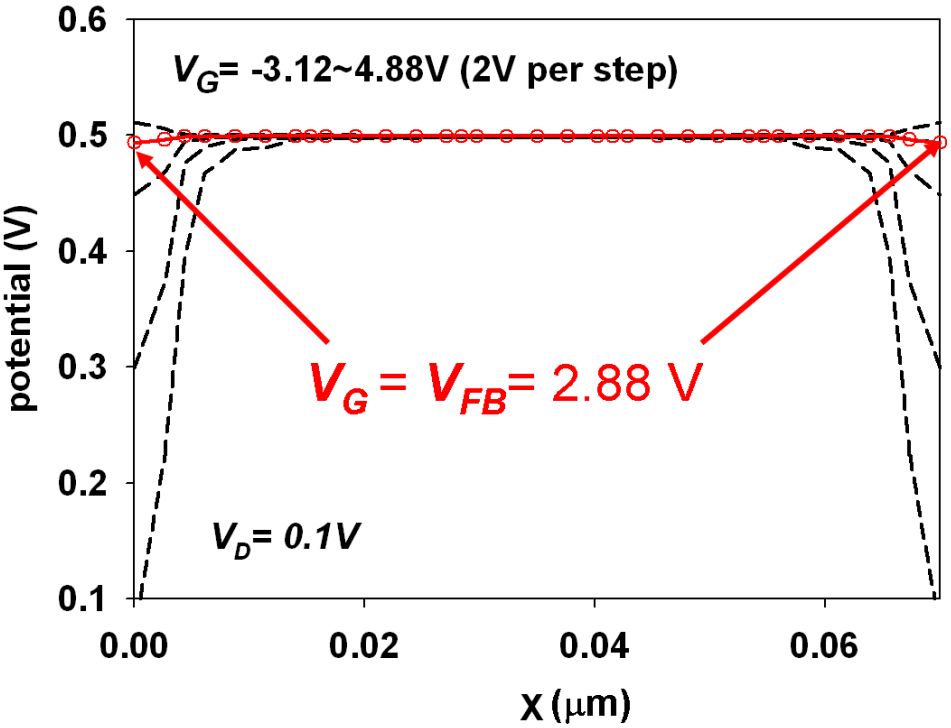

Fig. 4-9 Simulated electric potential distributions in the middle of the NW along *y*-axis at V_D = 0.1 V and various V_G. The result shown for V_G = 2.88 V confirms the flat-band condition.

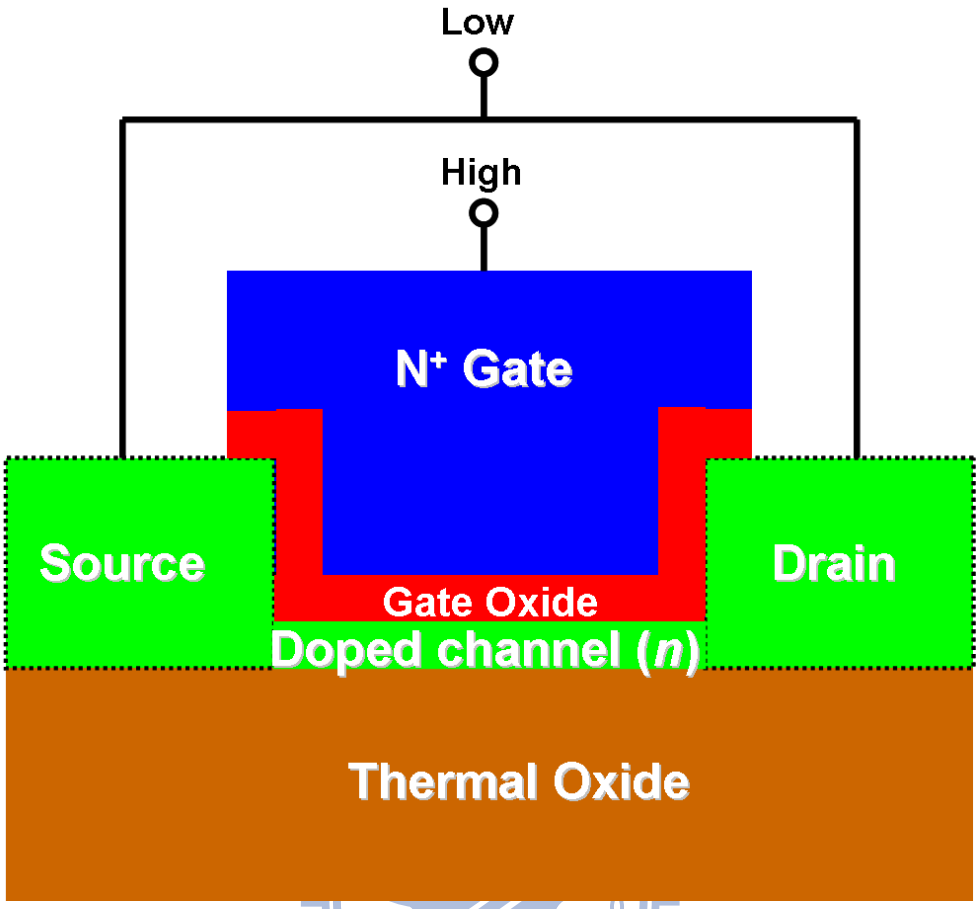

Fig. 4-10 Two-dimensional schematic structure of a planar J-less transistor featuring raised S/D. The high/low terminals are applied to gate and S/D electrodes, respectively, during C-V measurement.

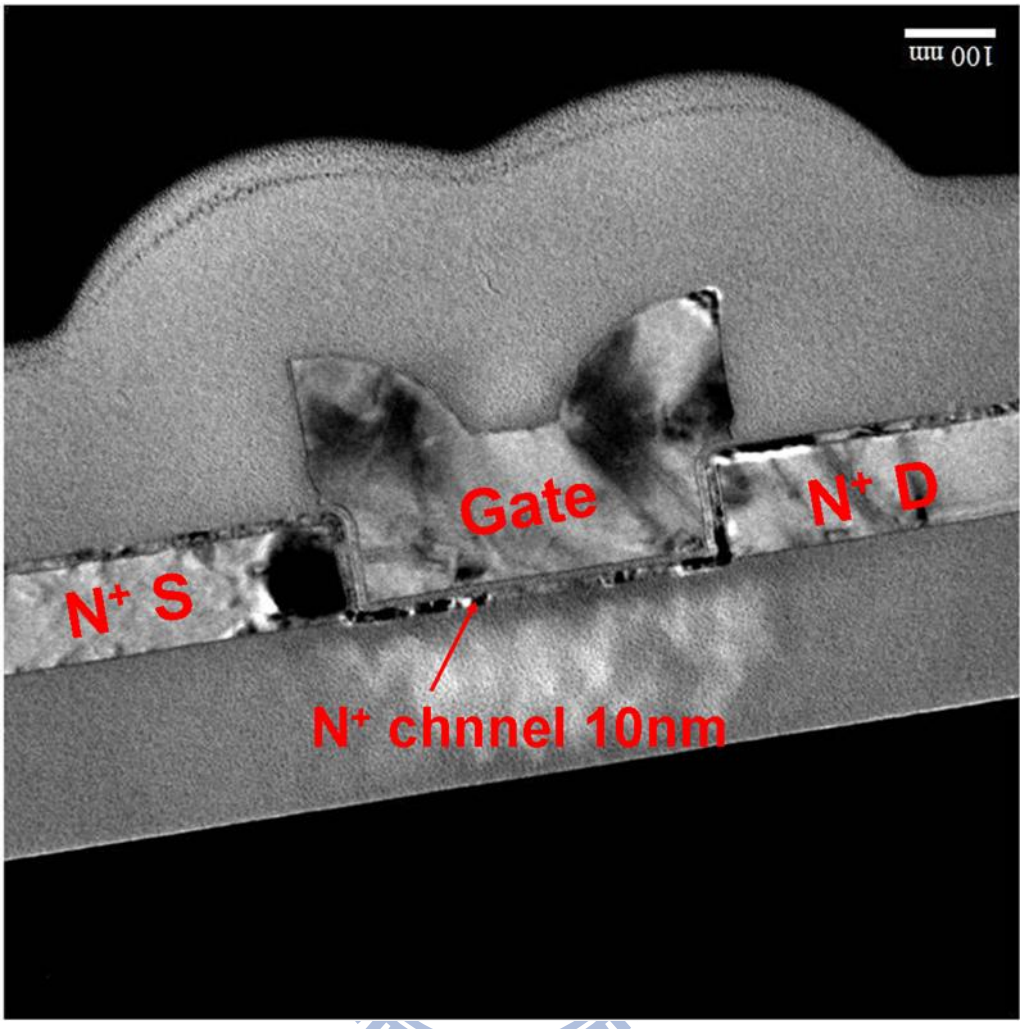

Fig. 4-11 Cross-sectional TEM image of a fabricated planar J-less transistor with *in situ* phosphorous-doped poly-Si channel film of 10nm in thickness.

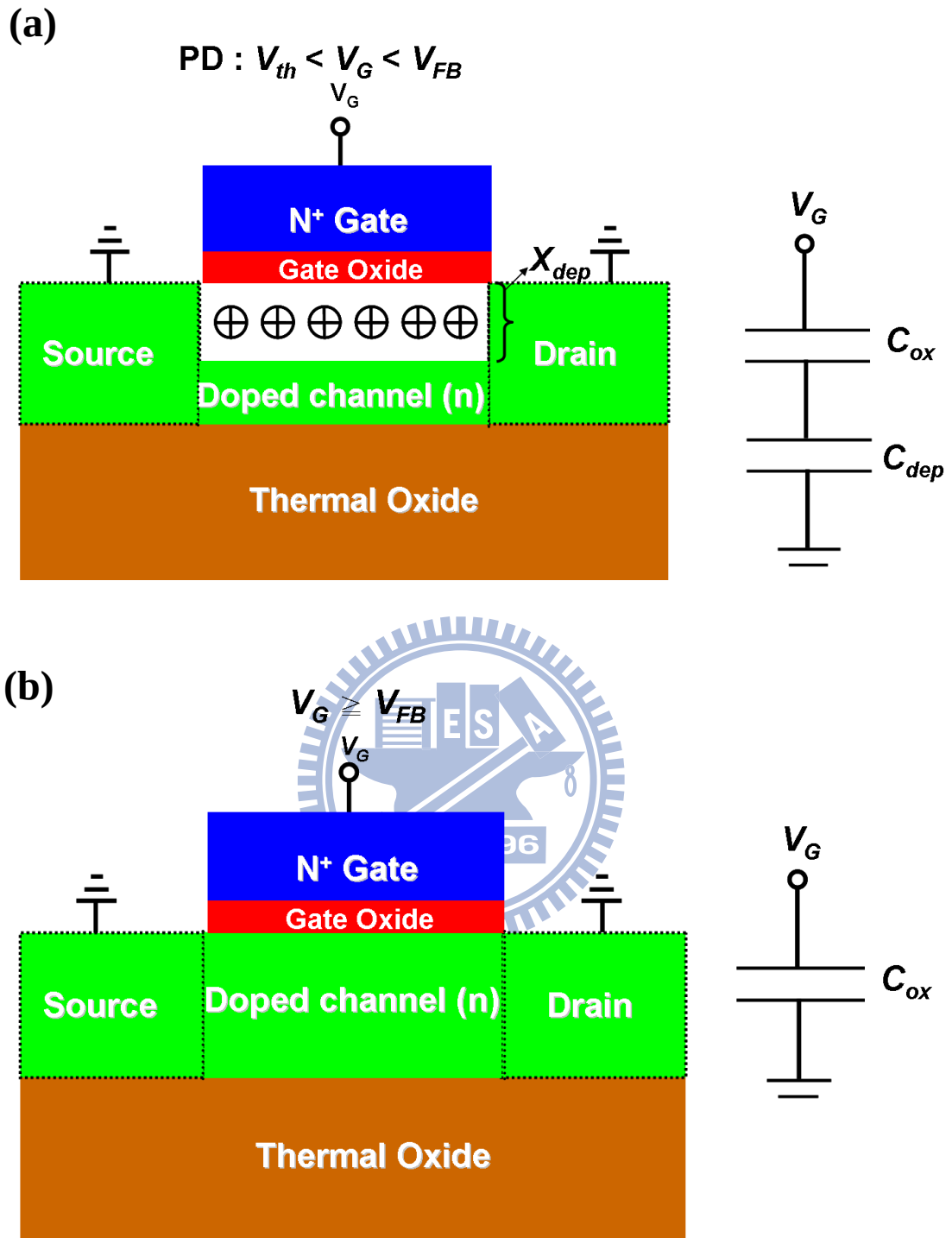

Fig. 4-12 (a) The schematic diagram as a J-less transistor is operated in PD region with effective capacitance equaling to the series connection of gate oxide capacitance (C_{ox}) and depletion region capacitance (C_{dep}) and (b) The schematic diagram of a J-less transistor with gate voltage larger than flatband voltage and effective capacitance equaling to C_{ox}.

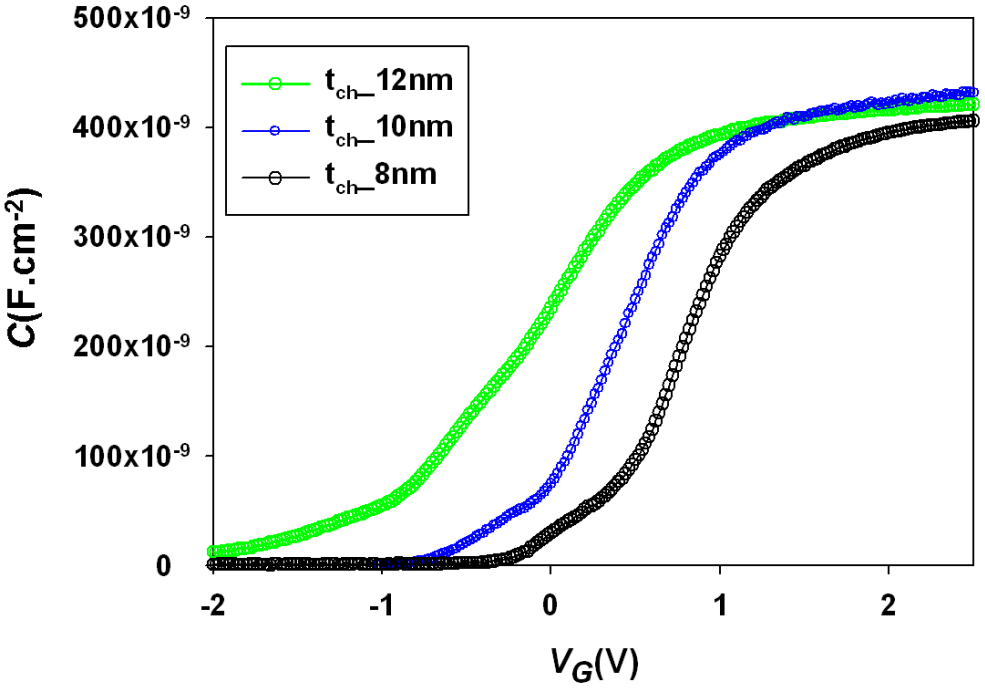

Fig. 4-13 The measured C-V characteristics of planar J-less transistors with channel thicknesses of 8, 10, 12 nm, respectively.

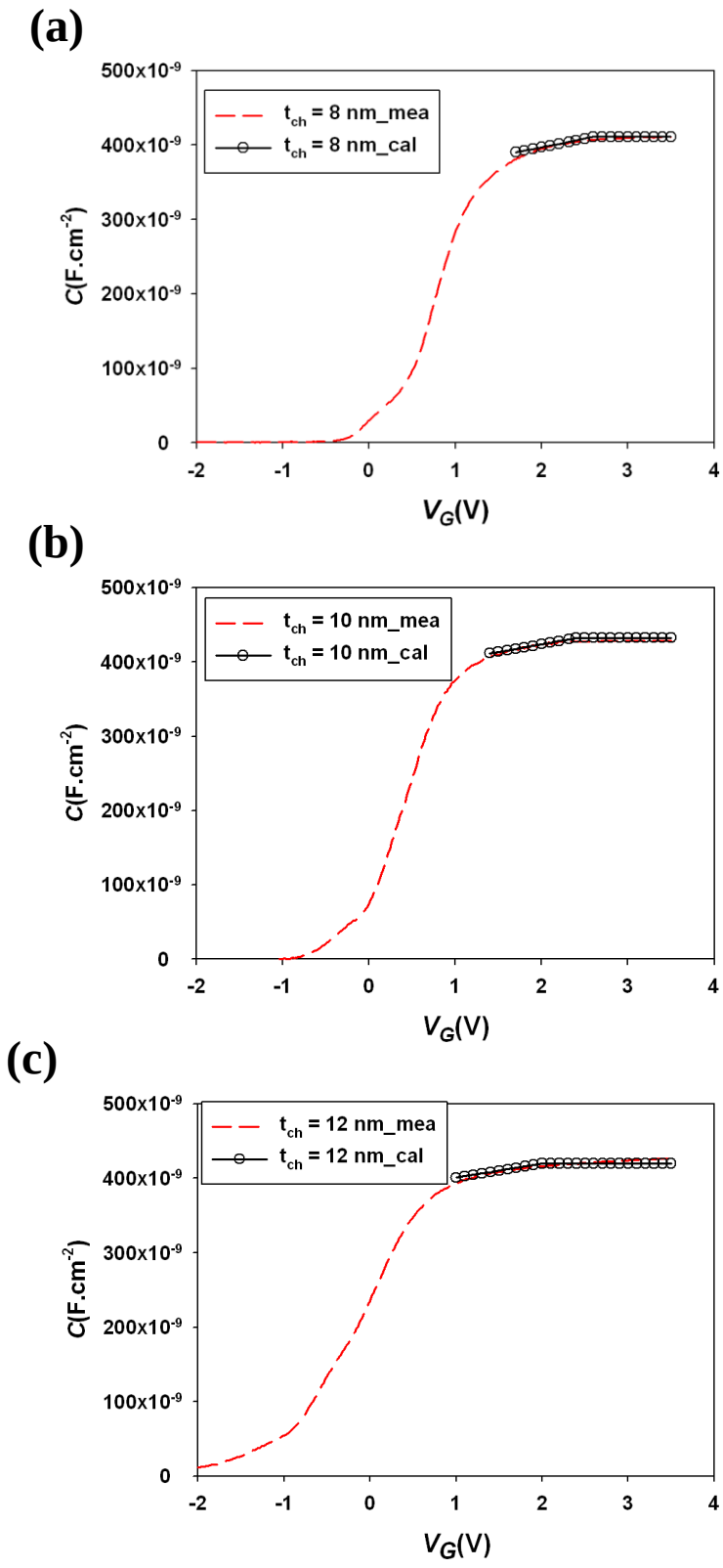

Fig. 4-14 Comparisons of the evaluated and measured C-V characteristics of planar J-less transistors with channel thickness of (a) 8, (b)10, (c)12 nm, respectively All of the results show that the theoretical calculation can well describe the experimental results shown in Fig. 4-13 in the region of V_G > V_{th}.

Chapter 5

Analytical Model of Threshold Voltage and Subthrshold Current for Fully-Depleted Double-gated (DG) Junctionless (J-less) Transistors

5-1 Introduction

As mentioned in the brief introduction in Sec. 1-3, Junctionless (J-less) transistors are of great potential for serving as the basic building blocks for logic circuits [5.1]~[5.4] or future 3-D multi-stacking NAND flash memories [5.5]~[5.6]. Regarding the practical applications, the development of an analytical model to describe the electrostatic characteristics of J-less transistors is essential because such an analytical model cannot only provide deep insights for engineers to design J-less transistors but also can serve as a spice model for circuit simulations.

Therefore, the purpose of this chapter is to develop an analytical model of threshold voltage (V_{th}) and subthreshold current for double-gated (DG) fully-depleted (FD) J-less transistors on the basis of solving the two-dimensional (2-D) Poisson's

equation. The organization of the remaining parts of this chapter is as follows. In Sec. 5-2, we derive an analytical model of the electric potential by solving the 2-D Poisson's equation. In Sec. 5-3, the subthreshold current and the subthreshold swing are calculated based on the derived 2-D electric potential. Then, in Sec. 5-4, we discuss the characteristics of V_{th} roll-off. Finally, the conclusions are present in Sec. 5-5.

5-2 Solution of 2-D Poisson's Equation

Figure 5-1 shows the schematic diagram of a DG FD J-less transistor. A P^+ poly gate is used in our calculation for a suitable value of V_{th}. The *x* and *y* axes directing the gate-to-gate and source-to-drain directions, respectively, are also shown in the figure with the origin set at the intersection of the source and front-gate oxide/channel interface. In the subthreshold region, the silicon film is fully depleted and the 2-D Poisson's equation can be written as

$$\frac{\partial^2 \Phi(x,y)}{\partial x^2} + \frac{\partial^2 \Phi(x,y)}{\partial y^2} = \frac{-qN_D}{\varepsilon_{si}}, \tag{5-1}$$

where Φ is the electric potential, ε_{si} is the dielectric constant of silicon, q is the electric charge, and N_D is the homogeneous active doping concentration across source, drain and channel regions. N_D is fixed at 1.5×10^{19} cm^{-3} in this work. The boundary conditions necessary to solve the 2-D Poisson's equation are listed below:

$$\Phi(t_{ch},y)+t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\partial\Phi(x,y)}{\partial x}\bigg|_{x=t_{ch}}=V_G-V_{FB}, \tag{5-2}$$

$$\Phi(0,y)-t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\partial\Phi(x,y)}{\partial x}\bigg|_{x=0}=V_G-V_{FB}, \tag{5-3}$$

$$\Phi(x,0)=V_s, \tag{5-4}$$

$$\Phi(x,L_g)=V_s+V_D. \tag{5-5}$$

In this chapter, the fixed oxide charges at oxide/silicon interfaces are neglected. In Eqs. 5-2~5-5, ε_{ox} is the dielectric constant of oxide. L_g, t_{ch}, and t_{ox} are the gate length, thickness of silicon channel film, and gate oxide thickness, respectively. V_G, V_D, and V_s are the applied voltages for the gate, drain and source, respectively. V_{FB} is the flatband voltage. To simplify the situation, we treat the gate oxide region as an equivalent Si region [5.7]~[5.8] by multiplying the gate oxide thickness by ($\varepsilon_{si}/\varepsilon_{ox}$). Then Eqs. 5-2 and 5-3 are converted into

$$\Phi(x,y)\big|_{x=t_{ch}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}}=V_G-V_{FB}, \tag{5-6}$$

$$\Phi(x,y)\big|_{x=-\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}}=V_G-V_{FB}. \tag{5-7}$$

Next, to solve Eq. 5-1, the 2-D Poisson's equation is separated into 1-D Poisson's equation and 2-D Laplace's equation as follows:

$$\frac{\partial^2\Phi_1(x)}{\partial x^2}=\frac{-qN_D}{\varepsilon_{si}}, \tag{5-8}$$

$$\frac{\partial^2\Phi_2(x,y)}{\partial x^2}+\frac{\partial^2\Phi_2(x,y)}{\partial y^2}=0, \tag{5-9}$$

$$\Phi(x,y)=\Phi_1(x)+\Phi_2(x,y), \tag{5-10}$$

where Φ_1 and Φ_2 are the solutions of the 1-D Poisson's and 2-D Laplace's equations, respectively. The 1-D solution Φ_1, which satisfies the two boundary conditions, Eqs. 5-6 and 5-7, can be expressed as

$$\Phi_1(x) = \frac{-qN_D}{2\varepsilon_{si}} x^2 + a_1 x + a_2, \tag{5-11}$$

$$a_1 = \frac{-2V_{FB} + \frac{N_D q t_{ox}{}^2 \varepsilon_{si}}{2\varepsilon_{ox}{}^2} + \frac{N_D q (t_{ch} + \frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}})^2}{2\varepsilon_{si}}}{t_{ch} + \frac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}}, \tag{5-11(a)}$$

$$\begin{aligned} a_2 &= \frac{(-V_{FB} + V_G + \frac{N_D q t_{ox}{}^2 \varepsilon_{si}}{2\varepsilon_{ox}{}^2})(t_{ch} + \frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}})}{t_{ch} + \frac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}} \\ &\quad + \frac{t_{ox}\varepsilon_{si}(-V_{FB} + V_G + \frac{N_D q (t_{ch} + \frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}})^2}{2\varepsilon_{si}})}{\varepsilon_{ox}(t_{ch} + \frac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}})} \\ &= V_G + a_3, \end{aligned} \tag{5-11(b)}$$

$$a_3 = \frac{(-V_{FB} + \frac{N_D q t_{ox}{}^2 \varepsilon_{si}}{2\varepsilon_{ox}{}^2})(t_{ch} + \frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}})}{t_{ch} + \frac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}} + \frac{t_{ox}\varepsilon_{si}(-V_{FB} + \frac{N_D q (t_{ch} + \frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}})^2}{2\varepsilon_{si}})}{\varepsilon_{ox}(t_{ch} + \frac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}})}. \tag{5-11(c)}$$

By using the separation method [5.9], the solution of the 2-D Laplace' equation Φ_2 can be expressed as

$$\Phi_2(x,y) = \sum_{n=1}^{\infty} \{G_n \sinh[\frac{n\pi}{t_{eff}} y] + H_n \sinh[\frac{n\pi}{t_{eff}}(L_g - y)]\} \times \sin(\frac{n\pi}{t_{eff}}(x + \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox})), \tag{5-12}$$

$$G_n = \frac{2}{n\pi}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}} y\right)\{(a_2 - V_D)\times(-1+\cos(n\pi)) +$$
$$\frac{2a}{(n\pi)^2 \varepsilon_{ox}}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}} y\right)[(n\pi t_{ox}\varepsilon_{si} + n\pi(t_{eff}\varepsilon_{ox} - t_{ox}\varepsilon_{si})\cos(n\pi) - t_{eff}\varepsilon_{ox}\sin(n\pi))] +$$
$$\frac{2qN_D}{(n\pi)^3 t_{eff}\varepsilon_{si}}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}} y\right)[\frac{(n\pi t_{ox}\varepsilon_{si})^2 t_{eff}}{\varepsilon_{ox}^2}(1-\cos(n\pi))$$
$$+\frac{2n\pi t_{eff}^2 t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}(n\pi\cos(n\pi) - \sin(n\pi)] +$$
$$t_{eff}^3[-2 + (2-(n\pi)^2)\cos(n\pi) + 2n\pi\sin(n\pi)]\}, \quad \text{(5-12(a))}$$

$$H_n = \frac{2}{n\pi}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}} y\right)\{a_2\times(-1+\cos(n\pi)) +$$
$$\frac{2a}{(n\pi)^2 \varepsilon_{ox}}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}} y\right)[(n\pi t_{ox}\varepsilon_{si} + n\pi(t_{eff}\varepsilon_{ox} - t_{ox}\varepsilon_{si})\cos(n\pi) - t_{eff}\varepsilon_{ox}\sin(n\pi))] +$$
$$\frac{2qN_D}{(n\pi)^3 t_{eff}\varepsilon_{si}}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}} y\right)[\frac{(n\pi t_{ox}\varepsilon_{si})^2 t_{eff}}{\varepsilon_{ox}^2}(1-\cos(n\pi))$$
$$+\frac{2n\pi t_{eff}^2 t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}(n\pi\cos(n\pi) - \sin(n\pi)] +$$
$$t_{eff}^3[-2 + (2-(n\pi)^2)\cos(n\pi) + 2n\pi\sin(n\pi)]\}, \quad \text{(5-12(b))}$$

$$t_{eff} = t_{ch} + 2\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox}, \quad \text{(5-12(c))}$$

where G_n and H_n are respectively determined by the boundary conditions, Eqs. 5-4 and 5-5, and Φ_2 is equal to zero at the top and bottom boundaries.

To verify the above-derived forms, we compare the calculated results with those of the TCAD simulation. With focus on the electrostatic characteristics of DG FD J-less transistors, basic models, such as the Poisson's equation, continuity equation, drift-diffusion, and constant mobility models, are applied to the 2D TCAD simulation tool "ISE TCAD Rel. 10.0 DESSIS" [5.10]. Figures 5-2(a) and (b) show such comparisons on the device with L_g of 100 and 22 nm, respectively. Note that A-A' and B-B' (see Fig. 5-1) refer to the perpendicular and parallel lines, respectively, with

respect to source-to-drain direction. Good agreements between the TCAD numerical simulation results and the analytical solutions of the electric potential along the two lines A-A' and B-B' are obtained. It should be noted that, in the long-channel case (L_g = 100 nm) shown in Fig. 5-2(a), in the middle of the channel (along the *y*-direction), the potential is nearly constant and close to its minimum value at $x = t_{ch}/2$. Results of the calculation indicate that Φ_2 is small and can be neglected in the middle region of a long-channel device and that the potential is mainly determined by Φ_1 in Eq. 5-10.

5-3 Subthreshold Current and Swing

With the analytical electric potential solution, the subthreshold current can be written as [5.7]

$$I_{DS} = \frac{q\mu W(kT/q)[1-\exp(-V_{DS}/kT)]}{\int_0^{L_g} dy \Big/ \int_0^{t_{ch}} n_i e^{q\Phi(x,y)/kT} dx}, \tag{5-13}$$

where μ, W, kT/q, and n_i are the effective carrier mobility, channel width, thermal voltage, and intrinsic carrier concentration, respectively. The subthreshold current is mainly limited by the potential minimum along the transport direction [5.9], which is assumed to be $\Phi(x, y_{min})$ located at $y = y_{min}$. The subthreshold current can then be simplified to

$$I_{DS} = \frac{q\mu W(kT/q)[1-\exp(-V_{DS}/kT)]}{\int_0^{L_g} \frac{dy}{\int_0^{t_{ch}} n_i e^{q\Phi(x,y_{\min})/kT} dx}}. \quad (5\text{-}14)$$

According to a previous work [5.9], two assumptions are made in our calculation. First, the first Fourier series term of Eq. 5-12 is sufficient to predict the electric potential at $y = y_{min}$. Second, $\sinh(x) \approx 0.5 \times \exp(x)$ can be used if $L_g\pi > t_{ch}$. Based on these two approximations, Eq. 5-12 can be simplified to

$$\Phi_2(x,y) = \sin[\frac{\pi}{t_{ch}}(x + \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox})] \times [G_1' \exp(\frac{(y-L_g)\pi}{t_{ch}}) + H_1' \exp(\frac{-y\pi}{t_{ch}})], \quad (5\text{-}15)$$

$$G_1' = \sinh[\frac{\pi}{t_{ch}} L_g] \times G_1, \quad (5\text{-}15(a))$$

$$H_1' = \sinh[\frac{\pi}{t_{ch}} L_g] \times H_1. \quad (5\text{-}15(b))$$

Furthermore, by setting $\partial\Phi_2(x,y)/\partial y = 0$, the location of channel potential minimum, y_{min}, can be expressed as

$$y_{\min} = \frac{L_g}{2} - \frac{t_{ch}}{2\pi} \ln(\frac{G_1}{H_1}). \quad (5\text{-}16)$$

Combining Eqs. 5-10, 5-14 and 5-16, the calculated subthreshold currents at L_g = 22 nm and 100 nm under V_D = 0.1 and 1 V are plotted in Figs. 5-3(a)-(d). Again, the calculated results are quite close to those of TCAD simulation. Figure 5-4 shows the subthreshold swing as a function of L_g ranging from 100 to 22 nm. The results are quite close to the theoretical limit of 60 mV/decade, owing to the ultra-thin silicon film (t_{ch} = 10 nm), and are also in good agreement with the results of TCAD simulation.

5-4 Threshold Voltage Roll-off

Although V_{th} can be directly extracted from the subthreshold current in Eq. 5-14 by the constant-current method, this approach cannot provide much physical insight into the operation of DG FD J-less transistors. Therefore, a simple analytical V_{th} model is addressed here. As discussed above, the subthreshold current is dominated by the electric potential minimum $\Phi(x, y_{min})$. Moreover, along the direction normal to the carrier transport direction, the subthreshold current is strongly related to the location where the maximum amount of conduction electrons passing through. The electric potential of this location is denoted as $\Phi(x_{max}, y_{min})$, where x_{max} is the depth from the front-gate oxide. Different from that of the traditional inversion-mode DG device in which $\Phi(x_{max}, y_{min})$ is situated close to the interface of the gate oxide and the silicon channel, the $\Phi(x_{max}, y_{min})$ of DG FD J-less transistor device is located in the middle of the silicon channel, as shown in Fig. 5-2. Therefore, in the following derivation, $\Phi(x_{max}, y_{min})$ is replaced with $\Phi(0.5\times t_{ch}, y_{min})$. Moreover, the electron density at $\Phi=\Phi(0.5\times t_{ch}, y_{min})$ is equal to

$$n_i e^{q\Phi(0.5\times t_{ch}, y_{\min})/kT}. \tag{5-17}$$

The V_{th} of the DG FD J-less transistor can be defined as:

$$V_{th} \equiv V_G \quad \text{when } \Phi(0.5\times t_{ch}, y_{\min}) = \left(\frac{kT}{q}\right)\ln\left(\frac{1}{M_{cri}}\frac{N_D}{n_i}\right), \tag{5-18}$$

where $M_{cri}\times n_i$ is the critical value of electron density which could be determined by

comparing the value of V_{th} in Eq. 5-17 with that obtained by the constant-current method for a long-channel device. Later, we will show that $M_{cri} \times n_i$ is typically about one or two orders in magnitude lower than the doping density (N_D). In the long-channel case, as has been pointed out in the end of Sec. 5-2 that $\Phi_2(x, y)$ in Eq. 5-10 can be neglected in the middle of a channel; therefore, solving the 1-D Poisson's equation is sufficient to predict the subthreshold current. Based on Eqs. 5-10 and 5-11, $\Phi(x_{max}, y_{min})$ can be simplified to

$$\Phi(0.5 \times t_{ch}, y_{\min}) = \Phi_1(\frac{t_{ch}}{2}) = \frac{-qN_D}{2\varepsilon_{si}}(\frac{t_{ch}}{2})^2 + a_1\frac{t_{ch}}{2} + a_2. \quad (5\text{-}19)$$

Combining Eqs. 5-11, 5-18, and 5-19, the V_{th} of a long-channel device can be expressed as

$$V_{th,long} = (\frac{kT}{q})\ln(\frac{1}{M_{cri}}\frac{N_D}{n_i}) - con1 - con2 - con3, \quad (5\text{-}20)$$

$$con1 = \frac{-qN_D}{2\varepsilon_{si}}(\frac{t_{ch}}{2})^2, \quad (5\text{-}20(a))$$

$$con2 = a_1 \times \frac{t_{ch}}{2}, \quad (5\text{-}20(b))$$

$$con3 = a_3. \quad (5\text{-}20(c))$$

For short-channel devices, only solving the 1D-Poisson's equation is not sufficient. Therefore, combined with Eqs. 5-16, 5-17, 5-18 and 5-20, the V_{th} of short-channel devices can be expressed as

$$V_{th,short} = \frac{V_{th,long}}{1-\frac{\pi}{8}\sin[\frac{\pi}{t_{ch}}(\frac{t_{ch}}{2}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox})]\times\exp(-\frac{\pi L_g}{2t_{ch}})} + \frac{-\frac{\pi}{8}con3+\{2(con4+con5+con6)-\frac{4V_D}{\pi}\}\sin[\frac{\pi}{t_{ch}}(\frac{t_{ch}}{2}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox})]\times\exp(-\frac{\pi L_g}{2t_{ch}})}{1-\frac{\pi}{8}\sin[\frac{\pi}{t_{ch}}(\frac{t_{ch}}{2}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox})]\times\exp(-\frac{\pi L_g}{2t_{ch}})},$$

(5-21)

$$con4 = \frac{2a(2t_{ox}\varepsilon_{si}-t_{eff}\varepsilon_{si})}{\pi\varepsilon_{ox}}, \quad \text{(5-21(a))}$$

$$con5 = \frac{2N_D q[(-4+\pi^2)t_{eff}^2 - \frac{2\pi^2 t_{eff}t_{ox}\varepsilon_{si}}{\varepsilon_{ox}} + \frac{2\pi^2 t_{eff}^2\varepsilon_{si}^2}{\varepsilon_{ox}^2}]}{\pi^3\varepsilon_{si}}, \quad \text{(5-21(b))}$$

$$con6 = \frac{-4(V_{bi}-V_D)}{\pi}. \quad \text{(5-21(c))}$$

Results of V_{th} estimated from Eq. 5-20 (for L_g = 100 nm) and Eq. 5-21 (for L_g < 100 nm) are shown in Fig. 5-5. By the constant-current method in which V_{th} is defined as the gate voltage at drain current of 300nA× W/L_g, a set of V_{th} values are also extracted by TCAD simulation and put together in the same figure for comparison. Note that, in the figure, the V_{th} of the transistor with L_g = 100 nm estimated with Eq. 5-20 is assumed to be the same as that extracted from constant-current method, and $M_{cri}\times n_i$ in Eq. 5-20 is consequently found to be equal to $\frac{1}{60}N_D$. It is seen that the simulated data actually coincide well with our analytical predictions. From Eq. 5-21, it is understood that V_{th} roll-off can be significantly improved by increasing the ratio of L_g/t_{ch} considering the $\exp(-\pi L_g / 2t_{ch})$ term in the denominators of the first and second terms of the equation. The V_{th} roll-off characteristics of the transistors with t_{ch}=8, 10, 12

and 15 nm measured at V_D = 0.1 and 1 V are shown in Figs. 5-6(a) and (b), respectively, in which delta_V_{th} is defined as the V_{th} difference between the short-channel transistors and that with L_g = 100 nm. As can be seen in the figures, the analytical model can well describe the trend of the enhanced V_{th} roll-off with increasing t_{ch}. Nonetheless, the difference between the analytical and simulation results in the short-channel regime becomes significant as t_{ch} increases. The reason for such deviation will be discussed later on.

Next, it is worth commenting on the value of $M_{cri} \times n_i$, which is actually the carrier concentration at $x = 0.5t_{ch}$ in the long-channel device at $V_G = V_{th}$. This value is typically much smaller than N_D, an indication of the fully depleted condition of the channel. However, it is not constant and is mainly dependent on t_{ch}, t_{ox}, and N_D. Since V_{th} is usually determined by the constant-current method, theoretically $M_{cri} \times n_i$ would decrease with increasing t_{ch} in order to turn off the additional contribution of current components conducted in the middle of the channel. Such a trend is shown in Fig. 5-7. $M_{cri} \times n_i$ is about $\frac{1}{60} N_D$ for t_{ch} = 10 nm and $\frac{1}{58} N_D$ for t_{ch} = 8 nm. Nonetheless, as t_{ch} is increased, the middle portion of the channel becomes difficult to deplete and eventually the device becomes partially depleted (PD) as t_{ch} is sufficiently thick. In the case shown in Fig. 5-7, the maximum t_{ch} under FD condition is 19 nm. When devices become PD, the quasi-neutral region in the channel would conduct an extremely high current that

can not be turned off by adjusting gate bias. In other words, the current level used to define V_{th} is screened out by the substantial leakage and loses its meaning in defining V_{th}. The essential role played by t_{ch} for the successful operation of J-less transistors is evident.

Figures 5-4 and 6 indicate that the differences in SS and delta_V_{th} between the results calculated by the analytical model and TCAD simulation become significant at a small L_g as t_{ch} is large. Such observation is attributed to the error in determining y_{min} using Eq. 5-16. In Fig. 5-8, the y_{min} values in the middle channel at $V_G = V_{th}$ and $V_D = 1$ V calculated by the analytical model and TCAD simulation are shown as functions of L_g. It is seen that y_{min} becomes closer to the source as the device becomes shorter, primarily due to the penetration of electric field with the applied drain voltage. At t_{ch} of 8 nm, the results obtained using analytical model are quite consistent with those of TCAD simulation. Nonetheless, the location of the y_{min} predicted by the analytical model is much closer to the source than that estimated by the TCAD simulation, implying that a much higher subthreshold leakage would conduct through the middle channel and thus worse SS and a high V_{th} roll-off. Such disparity indicates that the assumption made in acquiring Eq. 5-16 is not sufficient as t_{ch} is thick. As mentioned in Sec. 5-3 that only the first terms of the Fourier series in Eq. 5-12, *i.e.*, G_1 and H_1, are considered. This could greatly simplify the form for y_{min} but is not satisfactory as t_{ch} is thick. Fortunately, for

practical applications, t_{ch} should not be so thick considering the poor subthreshold characteristics (Fig. 5-9). The analytical model developed in this work is still useful for probing and designing J-less devices.

5-5 Summary

In this chapter, we've analytically modeled the subthreshold current and V_{th} roll-off characteristics of DG FD J-less transistors by solving the 2-D Poisson's equation. The calculated results of the derived analytical forms show good agreement with those of the numerical analysis by TCAD. With an ultra-thin silicon film ($t_{ch} \leqq 10$nm) and strong DG control, the subthreshold swing of DG FD J-less transistor is quite close to the theoretical limit of 60 mV/decade. The analytical forms for both long- and short-channel cases of V_{th} with useful physical insights are also derived. The V_{th} data estimated by these analytical forms also coincide well with those extracted by constant-current method except for those with too wide channel thickness owing to the inaccuracy during the determination of y_{min}.

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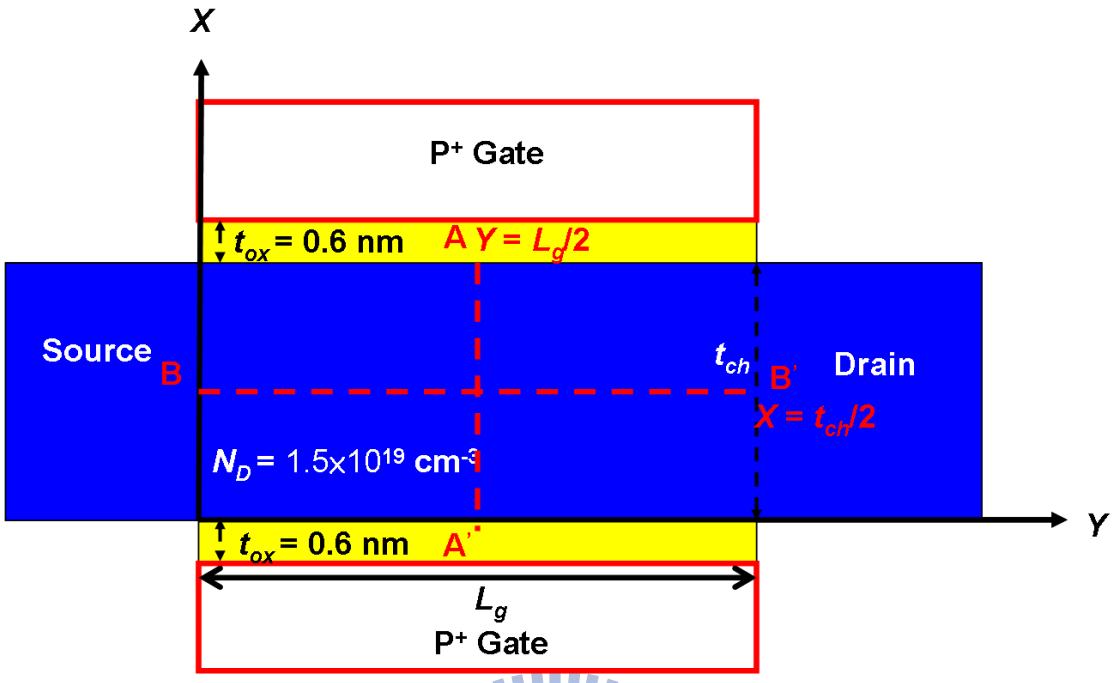

Fig. 5-1 Schematic diagram of the DG FD J-less transistor with P^+ polysilicon gate investigated in this work. t_{ch}, t_{ox}, and L_g are the silicon channel thickness, effective gate oxide thickness, and channel length, respectively. N_D = 1.5×10^{19} cm^{-3} is the homogeneous doping concentration across the source/drain and channel.

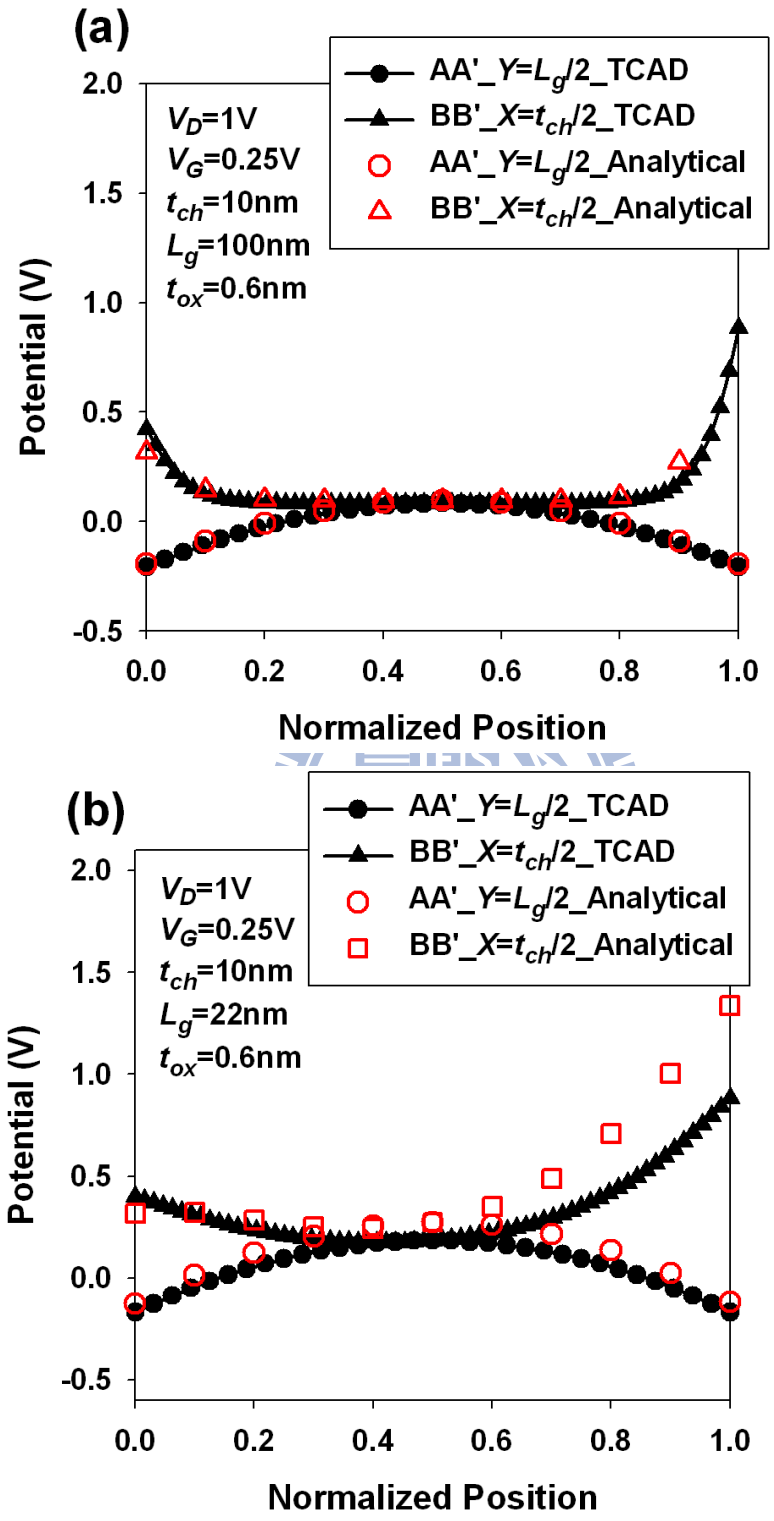

Fig. 5-2 Comparison of the analytical electric potentials and the TCAD simulation results for (a) long (L_g =100 nm) and (b) short (L_g =22 nm) channel devices.

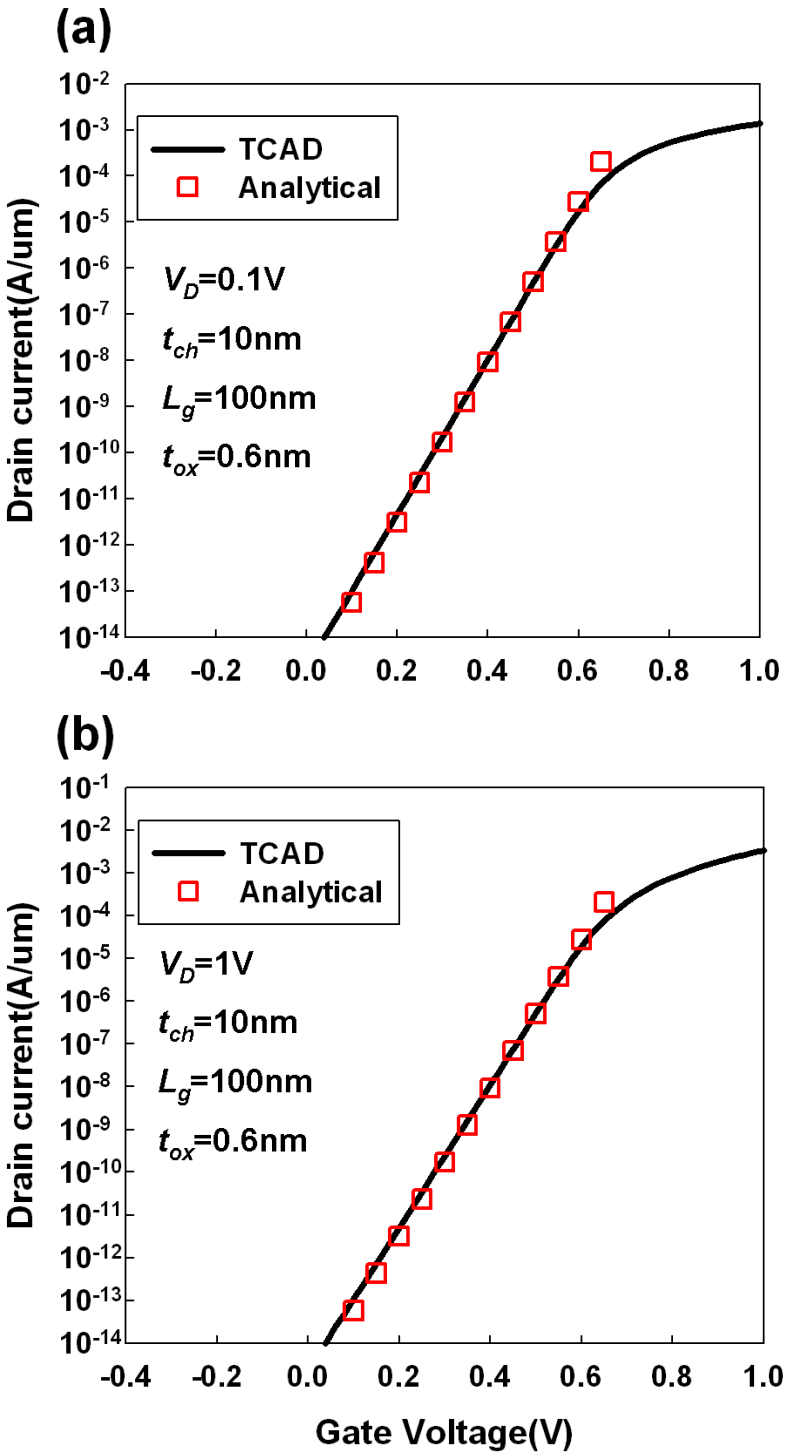

Fig. 5-3 Comparison of the analytical subthreshold currents and the TCAD simulation results for the long-channel device (L_g =100 nm) measured at (a) V_D = 0.1 and (b) 1V and the short-channel device (L_g =22 nm) measured at (c) V_D = 0.1 and (d) 1V.

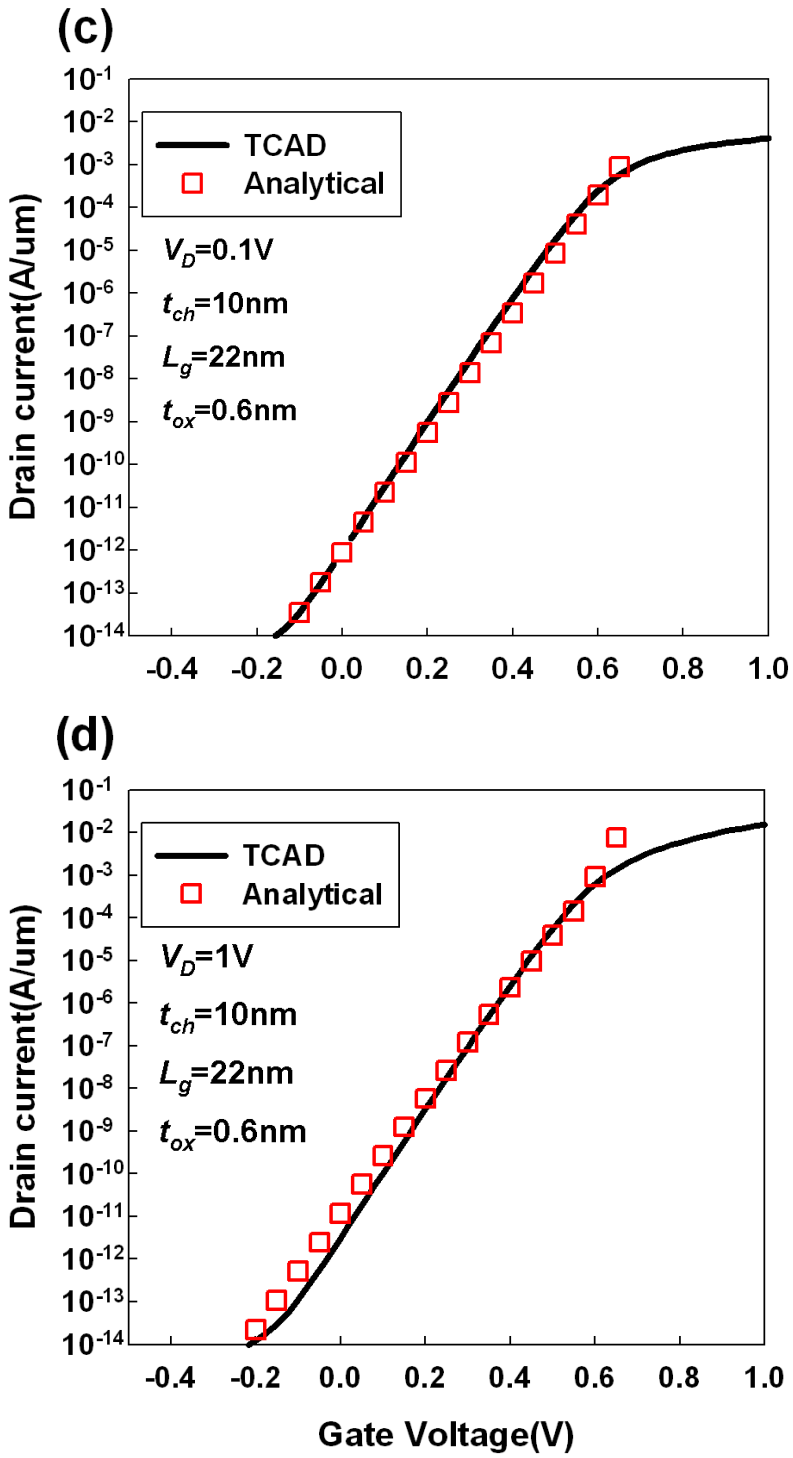

Fig. 5-3 Comparison of the analytical subthreshold currents and the TCAD simulation results for the long-channel device (L_g =100 nm) measured at (a) V_D = 0.1 and (b) 1V and the short-channel device (L_g =22 nm) measured at (c) V_D = 0.1 and (d) 1V.

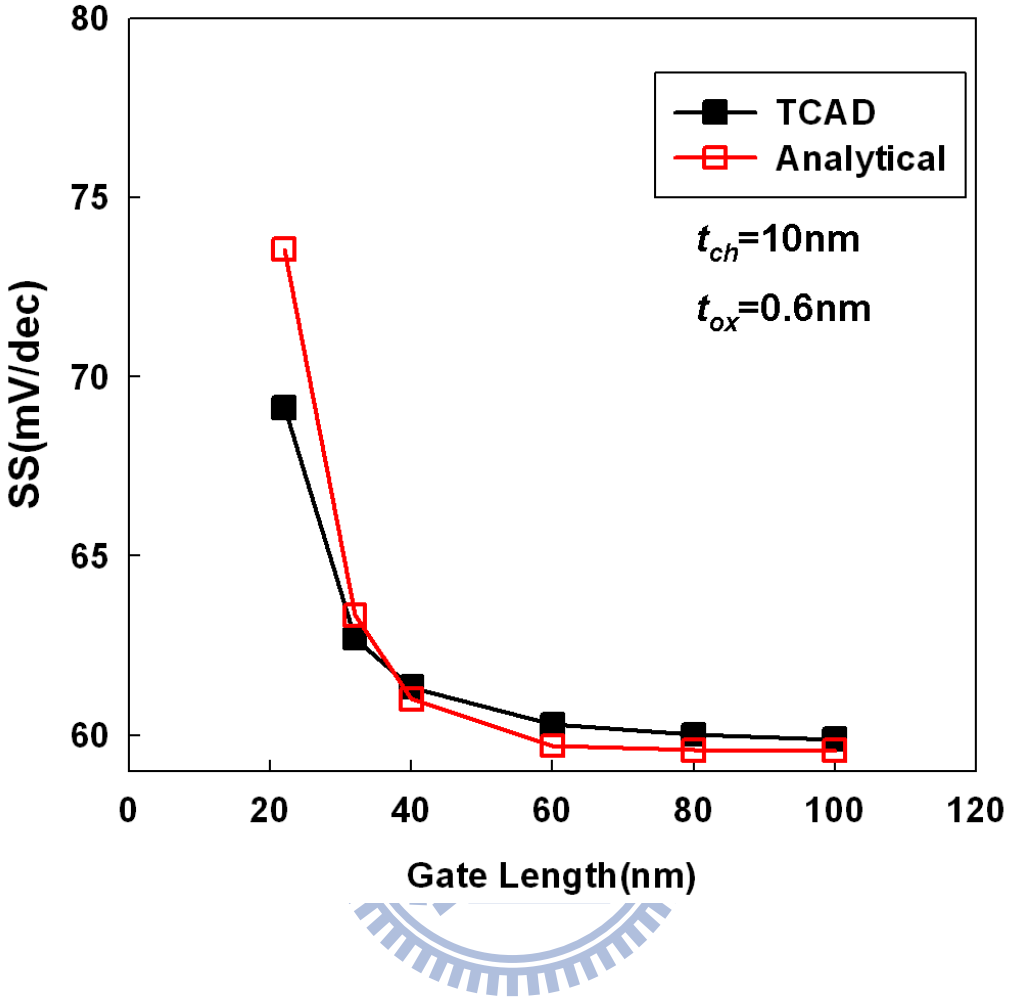

Fig. 5-4 Comparison of the analytical subthreshold swings for different channel lengths with the TCAD simulation results.

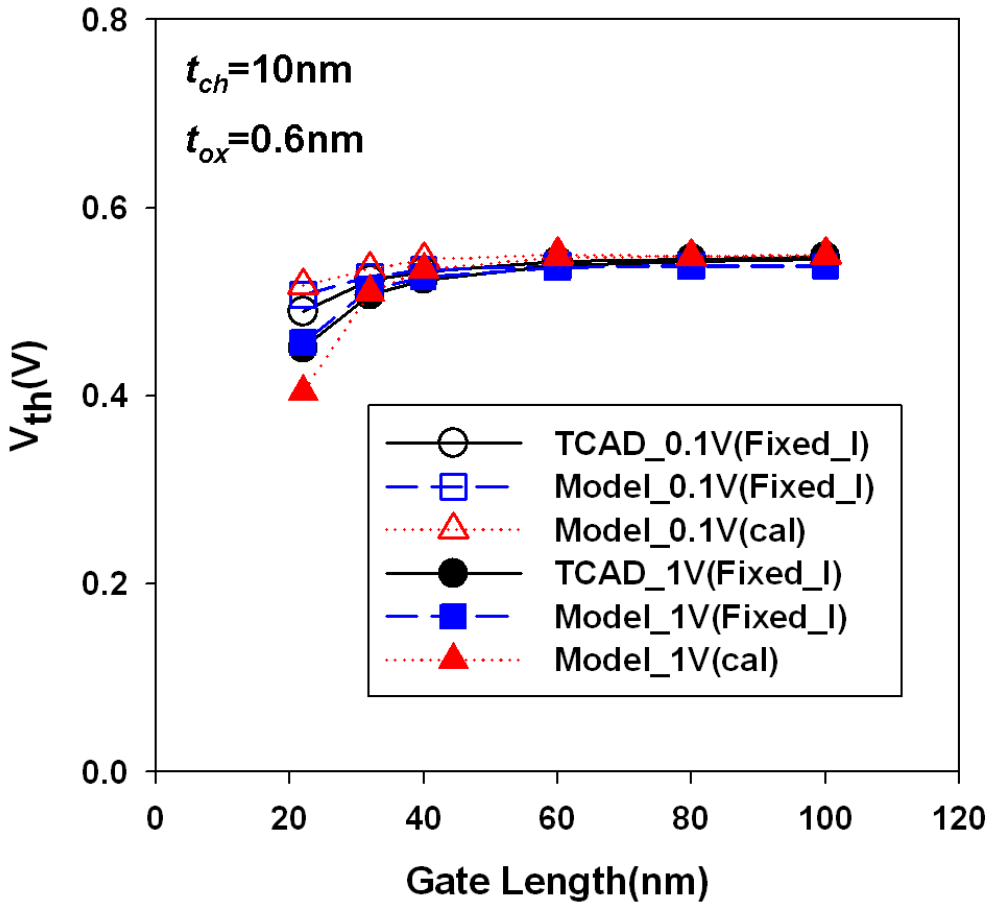

Fig. 5-5 Comparison of the analytical threshold voltages for different channel lengths with the TCAD simulation results.

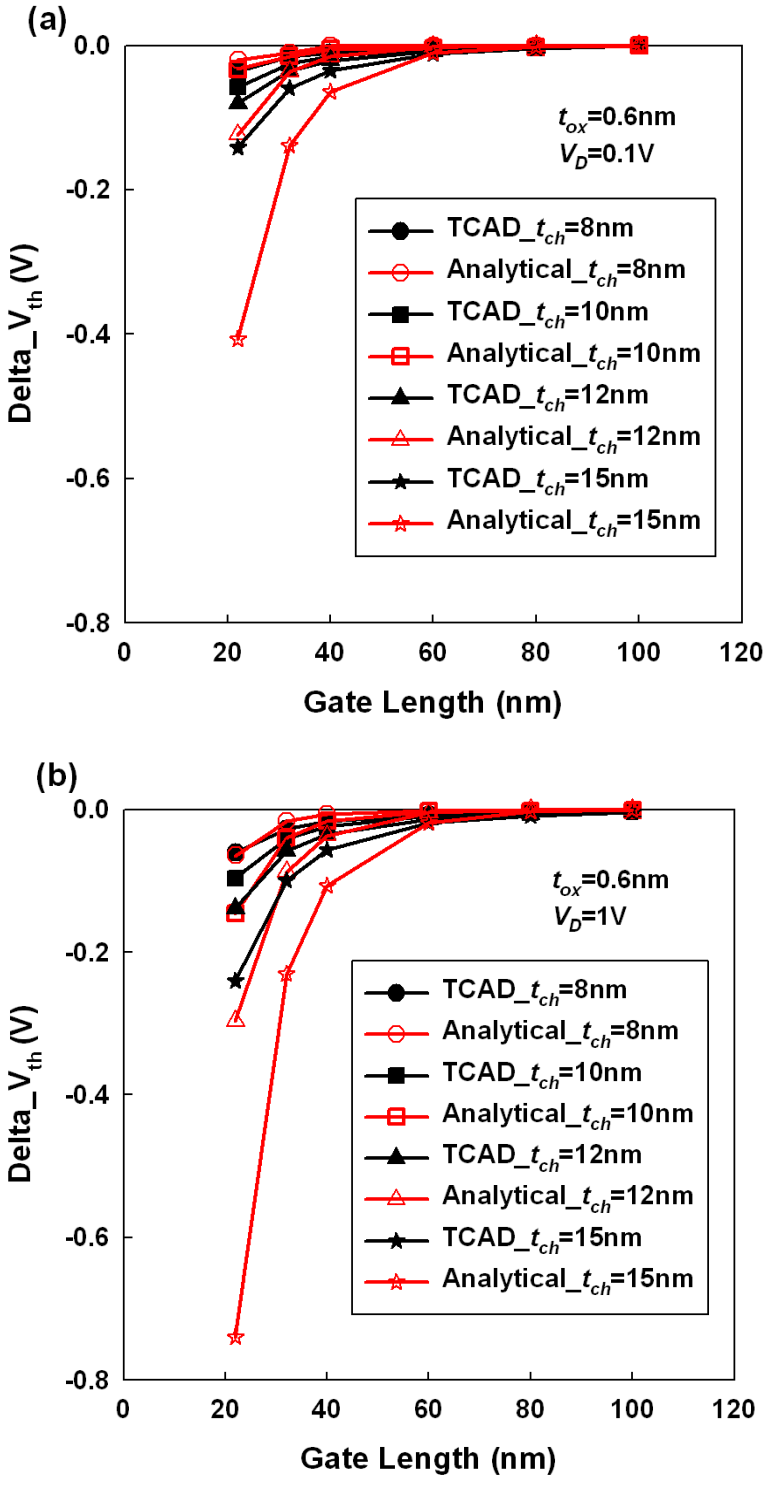

Fig. 5-6 Comparison of the analytical V_{th} roll-off for t_{ch} = 8, 10, 12 and 15 nm with the TCAD simulation results at V_D of (a) 0.1 V and (b) 1 V.

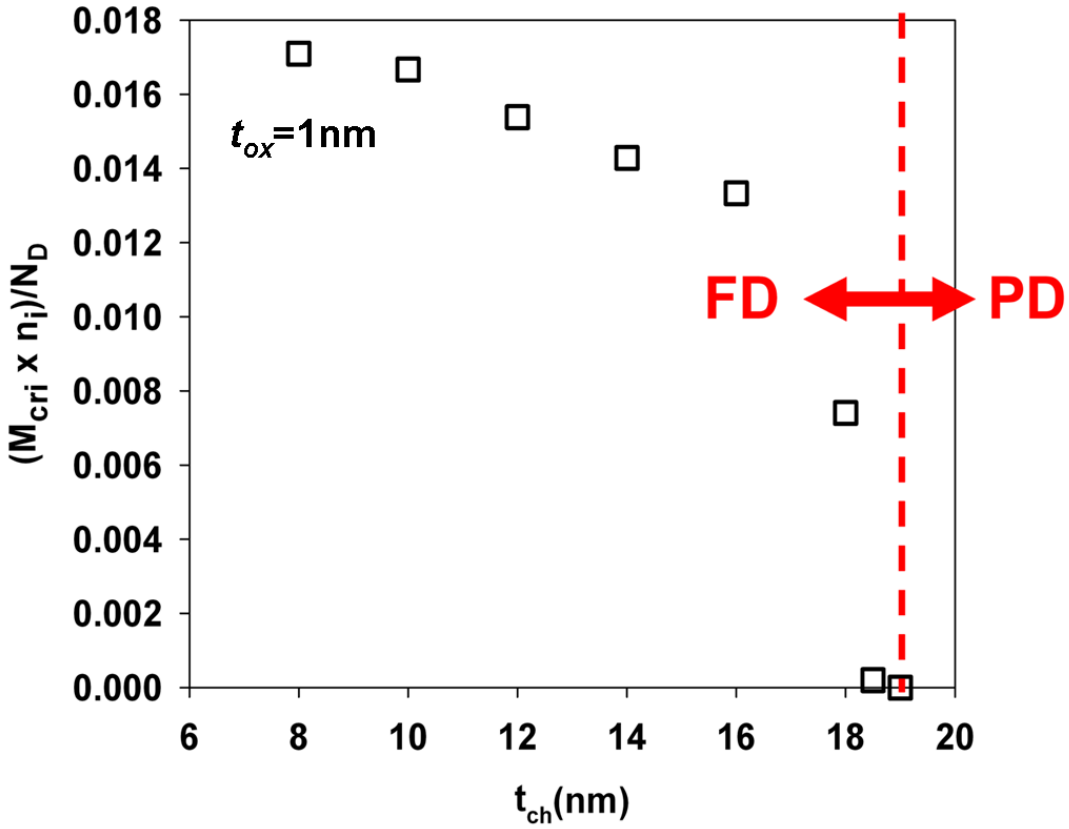

Fig. 5-7 $M_{cri} \times n_i/N_D$ versus t_{ch}. As t_{ch} is larger than 19 nm, the DG device becomes PD.

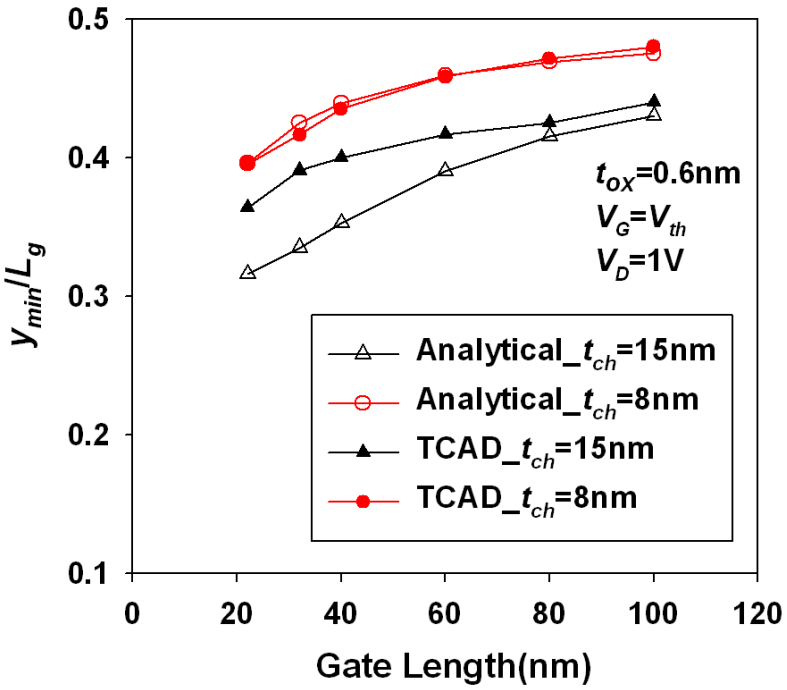

Fig. 5-8 Location of y_{min} estimated with Eq. 5-16 and TCAD simulation for devices with t_{ch} = 8 and 15nm. Smaller y_{min} means a location closer to the source.

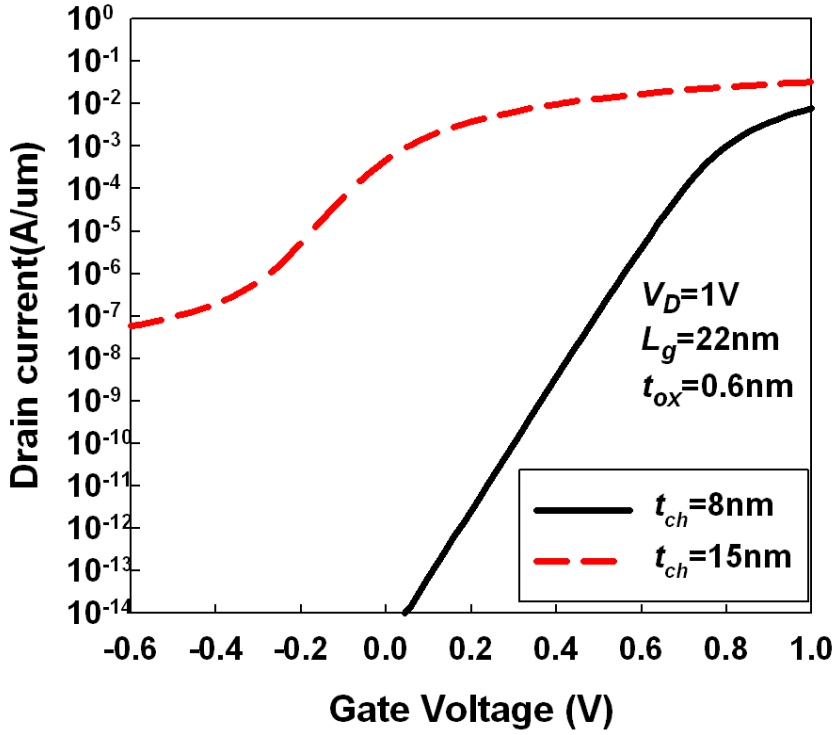

Fig. 5-9 Comparison of transfer characteristics of transistors with t_{ch} values of 8 and 15 nm and L_g of 22 nm, operating at V_D = 1 V. Note that the one with t_{ch} of 15 nm suffers from high leakage current.

Chapter 6

Characteristics of N-type Asymmetric Schottky-barrier Transistors (ASSBTs) with Silicided Schottky-barrier Source and Heavily N-type Doped Channel and Drain

6-1 Introduction

As mentioned in Sec. 1-4, Schottky-barrier (SB) transistors with source and drain (S/D) made of metallic silicides have shown intriguing properties in serving as a basic building block of the logic circuits [6.1]~[6.4] or non-volatile flash memories [6.5]. Regarding the applications of logic circuits, SB transistors possess the merits of easily-fabricated, abrupt, and shallow junctions which are formed with low-temperature process steps and exhibit low sheet resistance [6.1]~[6.4]. Regarding the applications of the non-volatile flash memories, low voltage but highly efficient programming can be achieved owing to the particularly high source-side injected gate current associated with the Schottky barrier [6.5].

However, a conventional symmetrical SB transistor (SSBT) with symmetrical SB S/D junctions usually suffers from a large off-state leakage current due to the inherent ambipolar characteristics [6.6]. So how to suppress the high leakage is an important task to address, which has been investigated in the past decade [6.7]~[6.8]. Possible approaches include the incorporation of an extra metal field-plate in SB transistors [6.7] or the employment of an asymmetric architecture [6.8] (*e.g.*, the replacing of the silicided drain by a doped one while maintaining the silicided source), as mentioned in Sec. 1.4.

On the other hand, junctionless (J-less) transistors have also shown great potentials for publications to the logic circuits [6.9]~[6.11] or non-volatile flash memories [6.12], especially in future three-dimensional (3-D) stacked NAND flash memories [6.13]. In this chapter, our objective is to combine the advantages pertaining to both ASSBT and J-less transistors, and propose a new asymmetric n-channel transistor (ASSBT) which features SB only on the source side, while the channel and drain are both n^+ doped. In other words, such a new structure eliminates the p-n drain junction in the previously-reported ASSBTs [6.8] and the drain is "junctionless-like". Our simulation results show that excellent on/off characteristics can be achieved with such a scheme. Moreover, in the final part of this chapter, an aggressive area-saving inverter is also proposed and explored based on such new ASSBTs.

6-2 Subthreshold Characteristics of ASSBT

Figures 6-1(a) and (b) show the simulated device structures of single-gated (SG) SSBT and the proposed ASSBT, respectively, both with a heavily n^+-doped-channel. The former is with symmetrical silicided SB source/drain while the latter has silicided SB formed only on the source side. Figure 6-1(b) indicates the proposed new ASSBT features junctionless-like drain and eliminates the p-n drain junction in the previously-reported ASSBTs [6.8]. Such a "junctionless-like" feature of the new ASSBT requires an ultra-thin channel in order to effectively switch off the current conduction of the device. Detailed parameters used for simulation of SSBT and ASSBT are listed in Table 6-I. The directions of *x* and *y* shown in Figs. 6-1(a) and (b) are parallel and perpendicular to the source-to-drain direction, respectively. A 2-D TCAD tool "DESSIS" [6.14] is employed in this work for the simulation analysis. The tunneling current conducting through the SB is handled by a non-local tunneling model with effective masses of $0.26m_0$ and $0.36m_0$ for electrons and holes, respectively. Figures 6-2(a) and 2(b) compare the calculated I_D-V_G characteristics of SSBT and ASSBT with gate length (L_g) of 100 and 22 nm, respectively. Similar to the traditional inversion-mode SB transistors, the SSBTs with a heavily n^+-doped channel show ambipolar behavior, *i.e.*, a large gate-induced drain leakage (GIDL)-like current is conducting in the off-state, resulting in low on/off current ratios. In contrast, the

ASSBTs show unipolar transfer characteristics with significantly reduced off-state current, owing to the suppression of hole current injecting from the drain side as gate voltage is sufficiently negative. Moreover, the on-state current of the ASSBT is also slightly improved, owing to the reduction of the drain resistance component.

6-3 Deep Insight into the Suthreshold Characteristics of ASSBT

Although the I_D-V_G characteristics of SB transistors with a heavily n^+-doped-channel look similar to the conventional inversion-mode SB transistors, as shown in Fig. 6-2(a) and (b), the physical mechanisms behind their operations are quite different. The most striking feature associated with the operation of the present devices is that the turn off of their operation relies on depleting the heavily n^+-doped-channel [6.10]. The dominant transport mechanism depends on the operation condition. To help understand the situations, a typical I_D-V_G curve of an ASSBT with an n^+-doped-channel is shown in Fig. 6-3, which is divided into three regions corresponding to different transport mechanisms. To elaborate on the mechanisms, electron density and electric potentials in the silicon channel along *y* direction near the source at x = 3 nm for various gate voltages are simulated, and the results are shown in Figs. 6-4, 6-5, and 6-6 for regions I, II and III, respectively. Moreover, the conduction band edge of the heavily

n^+-doped-channel along x direction at y = 1 nm in regions I, II, and III is also individually shown in Figs. 6-4(c), 6-5(c) and 6-6(c), respectively, to explain the impact of SB profile on the device operation. Region I is the subthreshold region and, as shown in Figs. 6-4(a) and (b), the carrier concentration is significantly reduced while the strength of electric field in the channel near the source is not high. The potential barrier for electrons in the source, as shown in Fig. 6-4(c), is much larger than the Schottky barrier height (SBH) at the source/channel interface. Thus, the injection of electrons from the source to the channel is mainly governed by the thermionic emission, similar to that of conventional MOS devices operated in the subthreshold regime. Moreover, by the aid of extra thin channel thickness (t_{ch} = 6 nm), a subthreshold swing (SS) close to ideal 60mV/dec is achieved. When gate voltage increases from region I to region II, which is also called the pseudo-subthreshold region, Figure 6-5(a) depicts the increment of carrier concentration accompanying with the rise of electric potential illustrated in Fig. 6-5(b). In addition, as shown in Fig. 6-5(c), the potential at the channel center is pushed down to a level lower than the top of the SB; thus, its operational mechanism is determined by the thermionic field emission, which is a combination of thermionic emission and tunneling current [6.15], as illustrated in Fig. 6-7. As can be seen in Fig. 6-5(c), the SBH is essentially not affected by the gate voltage when operated in this region, so does the thermionic emission current component. On the other hand, the

width of the barrier for the thermally activated electrons in the silicided SB source to tunnel through as well as the potential at the channel center (Φ_1 in Fig. 6-7) is effectively modulated by the gate voltage. As a result, the thermionic field emission (TFE) current dominates the conduction in region II, resulting in a larger SS.

As the gate voltage increases further and reaches beyond flat-band voltage, the device is switched from region II to region III (*i.e.*, the on-state) where a large number of electrons are accumulated near the interface between the channel and gate oxide as shown in Fig. 6-6(a). Under such a situation the tunneling barrier is so thin that the tunneling mechanism overwhelms the thermionic process. However, as gate voltage further increases, the tunneling width of the SB junction is not modulated effectively anymore, as illustrated in Fig. 6-6(c), so the transport current of ASSBT gradually saturates.

6-4 Impacts of t_{ch} and t_{ox} on the Transfer Characteristics of ASSBTs

In last section, we show that the ASSBT exhibits inferior SS in region II due to the inefficient modulation of the barrier height as well as the rather thick tunneling width of the SB junction. Since the SBH as high as 0.25 eV is difficult for the thermionic current to conduct, it is therefore desirable to enhance the capability of the gate bias in

modulating the tunneling width of the SB. In this section, we show how a thinner channel and/or a thinner effective gate oxide yield improvement of SS in region II. Figures 6-8(a) and (b) show the I_D-V_G characteristics of ASSBTs with various channel and gate oxide thicknesses, respectively. SS extracted from region II of the transfer curves for devices with channel thicknesses varying from 4 to 10 nm is plotted as a function of t_{ox} in Fig. 6-8(c). It can be seen that SS is improved as channel and gate oxide thickness become thinner. The decrease in SS with decreasing t_{ch} could be understood from the results shown in Fig. 6-5(b). In this figure, we can see that the modulation of the potential by the gate bias is weakened in a deeper position. A reduction in channel thickness could thus enhance the overall gate controllability in modulating the tunneling width of the SB. A reduction in oxide thickness may have the same effect, thus the SS is improved.

Similar trends were also observed in conventional inversion-mode SB transistors [6.16]~[6.18]. According to the previous study, the electrostatic problem of conventional fully-depleted inversion-mode SB MOSFETs could be solved by a simple 1-D differential equation, which is expressed as [6.17]~[6.18]

$$\frac{d^2\Phi(x)}{dx^2} - \frac{\Phi(x) - V_g + V_{bi}}{\lambda^2} = \frac{\rho_{tot}(x)}{\varepsilon_{si}}, \tag{6-1}$$

$$\lambda = \sqrt{t_{ch} t_{ox} \left(\frac{\varepsilon_{si}}{\varepsilon_{ox}}\right)}, \tag{6-2}$$

where x, $\Phi(x)$, V_{bi}, V_g, and ρ_{tot} are the direction from source to drain, electric

potential, build-in potential, applied gate voltage and mobile charges, respectively. λ is the scaling length and plays the role in describing how the potential variation is exponentially screened. According to Eqs. 6-1 and 2, decreases in t_{ch} and t_{ox} lead to a smaller λ, which would in turn reduce the tunneling width of the SB and improve SS. For heavily n^+-doped-channel ASSBT, the concept of scaling length "λ" is still suitable to describe the impact of t_{ch} and t_{ox} on SS while the device is operated in region II. However, a modification on λ is essential. From Fig. 6-5(a), it can be seen that the location of maximum electron concentration is deep into the channel. This is in contrast to the case of conventional inversion-mode SB transistors, and suggests that the effective gate oxide thickness is thicker for the n-type ASSBT with a heavily n^+-doped-channel. An empirical form for the modified λ can be expressed as:

$$\lambda = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ch} (\eta \frac{\varepsilon_{ox}}{\varepsilon_{Si}} t_{ch} + t_{ox.})}, \qquad (6\text{-}3)$$

where η is a fitting parameter used to reflect the effective thicker gate oxide. If no modification is done on the effective gate oxide thickness for heavily n^+-doped-channel ASSB transistor (*i.e.*, η=0), the plot of SS versus λ of heavily n^+-doped-channel ASSBTs with various t_{ch} and t_{ox} cannot be arranged in the same regression curve, as shown in Fig. 6-9(a). However, as shown in Fig. 6-9(b), as the above modified form for λ (η=0.3) is implemented, the concept of λ can work well again to reflect the influence of gate oxide and channel thickness on SS in region II. Because of the

broadening distribution of electron density between oxide/channel interface and bottom of channel as shown in Fig. 6-5(a), η must be a number between 1 and 0.

In order to further improve the SS of the ASSBT in region II, double-gated (DG) configuration is also investigated. Figure 6-10 plots the schematic 2-D structure of the DG ASSBT with a heavily n^+-doped-channel. The comparison of SS for DG and SG devices is shown in Fig. 6-11(a), where thicknesses of gate oxide and silicon channel vary from 0.6 to 1 nm and 4 to 10 nm, respectively. Due to the stronger gate control ability, significant improvement of SS is demonstrated with the DG configuration. Figure 6-11(b) shows the plot of SS versus λ of heavily n^+-doped-channel DG ASSBT, together with the results of devices with single gate (SG) configuration. It can be seen that both DG and SG configurations are arranged in the same regression curve, which means that the concept of λ works well regardless of the gate configurations. Note that t_{ch} in Eq. 6-3 is corrected to $t_{ch}/2$ for DG configuration.

6-5 A New Inverter Scheme Built by Dual Workfunction (DW) DG N- and P-type ASSBTs

The theoretical analysis in the above sections indicates that the newly proposed ASSBT could effectively suppress the high off-state leakage due to ambipolar conduction and therefore the associated issue of serious power consumption.

Furthermore, by the aid of DG configuration, the inferior SS attributed to the built-in SB could be significantly improved. However, the inappropriate threshold voltages of SG (Fig. 6-1(b)) and DG (Fig. 6-10) ASSBTs lead to a high leakage current at V_G = 0 V as shown in Fig. 6-13 and consequently unacceptable power consumption in practical circuit operation. In Fig. 6-13 the transfer characteristics of dual-workfuntion (DW) DG ASSBTs (Fig. 6-12) are also compared. Contrary to the aforementioned DG ASSBTs (Fig. 6-10) featuring both top and bottom gates of the same mid-gap workfunction, the DW DG N-type ASSBTs features top p^+-poly gate and bottom gate of mid-gap workfunction (4.5 eV). Therefore, the inappropriate threshold voltages of SG and DG ASSBTs can be adjusted by the top p^+ poly gate and consequently suppress the leakage current at V_G = 0 V, as shown in Fig. 6-13. Based on these features, we propose a new inverter built by DW DG ASSBTs, as shown in Fig. 6-14(a). In the scheme, the n- and p-type DW DG ASSBTs have a heavily n- and p-doped channel, respectively, and individually adopt the p^+- and n^+-poly gates as the top gate while sharing a common bottom gate with mid-gap workfunfion of 4.5 eV. Similar to the structure presented in a previous work [6.19] shown in Fig. 6-14(b), the area of isolation between the pair of devices is eliminated by directly connecting their drains and thus the overall area could be shrunk. In addition, compared to the structure shown in Fig. 6-14(b), the employment of the underlying common bottom gate can reduce the complexity of fabrication

associated with the misalignment between individual top and bottom gates. Detailed parameters used for the simulation of the new inverter shown in Fig. 6-14(a) are listed in Table 6-II. The results of the DC V_{in}-V_{out} characteristics and switching current are shown in Figs. 6-15(a) and (b), respectively. In addition, the AC output transient behavior with a load capacitance of 1 fF is also shown in Fig. 6-15(c). Figures 6-15(a)~(c) indicate that the proposed inverter (Fig. 6-14(a)) features good switching characteristics.

6-6 Summary

Through TCAD simulation, we've explored the operation of a novel n-type ASSBT with silicided SB source and n^+-doped channel and drain. As compared with the conventional SSBT equipped with symmetrical silicided SB S/D, the new ASSBT exhibits much reduced off-state current and improved on-current. The dominant conduction mechanisms of the ASSBT are also studied. In addition to the subthreshold and on-state regions, a pseudo-subthreshold region in which thermionic field emission conduction process dominates is identified. A reduction in either the channel or gate oxide thickness is helpful in reducing the SS of pseudo-subthreshold region. Furthermore, the concept of scaling length (λ) is adopted but with a modified empirical form to reflect the impacts of gate oxide and channel thicknesses on the characteristics

of the devices. Finally, a novel inverter composed of N- and P-type DW DG ASSBTs with common back-gate is proposed, featuring higher device density as well as good switching properties and simpler fabrication process.

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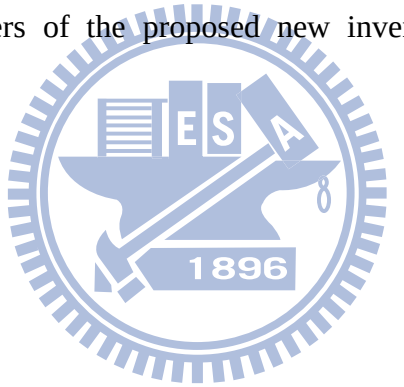
Parameter	Value
Gate work function (WF)	4.5 eV
Gate oxide thickness (t_{ox})	0.6 nm
Silicon thin film thickness (t_{ch})	6 nm
Doping concentration in drain	$1x10^{20}cm^{-3}$
Doping concentration in channel	$1x10^{19}cm^{-3}$
Schottky-barrier height (SBH)	0.25 eV

Table. 6-I Major parameters of SSBT and ASSBT used in simulations.

Parameter	Value
Gate work function of common bottom gate (WF)	4.5 eV
Gate oxide thickness (t_{ox})	6 nm
Silicon thin film thickness (t_{ch})	0.6 nm
Doping concentration in drain (N- & P-type device)	$1x10^{20}cm^{-3}$
Doping concentration in channel (N- & P-type device)	$1x10^{19}cm^{-3}$
Schottky-barrier height for N-type device (SBH_N)	0.25 eV
Schottky-barrier height for P-type device (SBH_P)	0.85 eV

Table. 6-II Major parameters of the proposed new inverter (Fig. 6-14(a)) used in simulations.



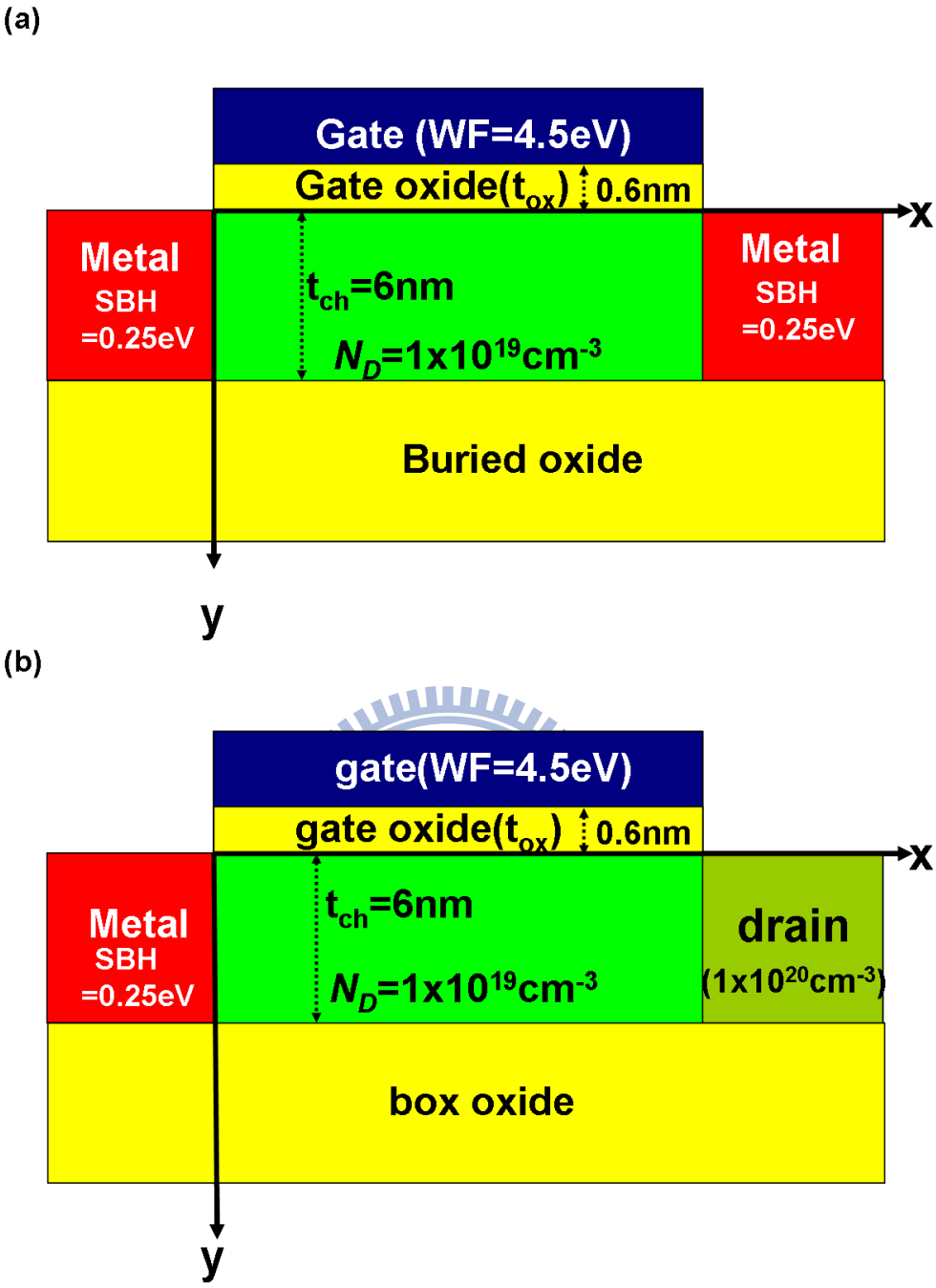


Fig. 6-1 Schematic diagrams of the (a) SSBT with silicided SB S/D and (b) ASSBT with silicided SB only on the source side investigated in this work. t_{ch} = 6 nm, t_{ox} = 0.6 nm, WF = 0.5 eV and SBH = 0.25 eV. Channel doping N_D=1 × 10^{19} cm^{-3}.

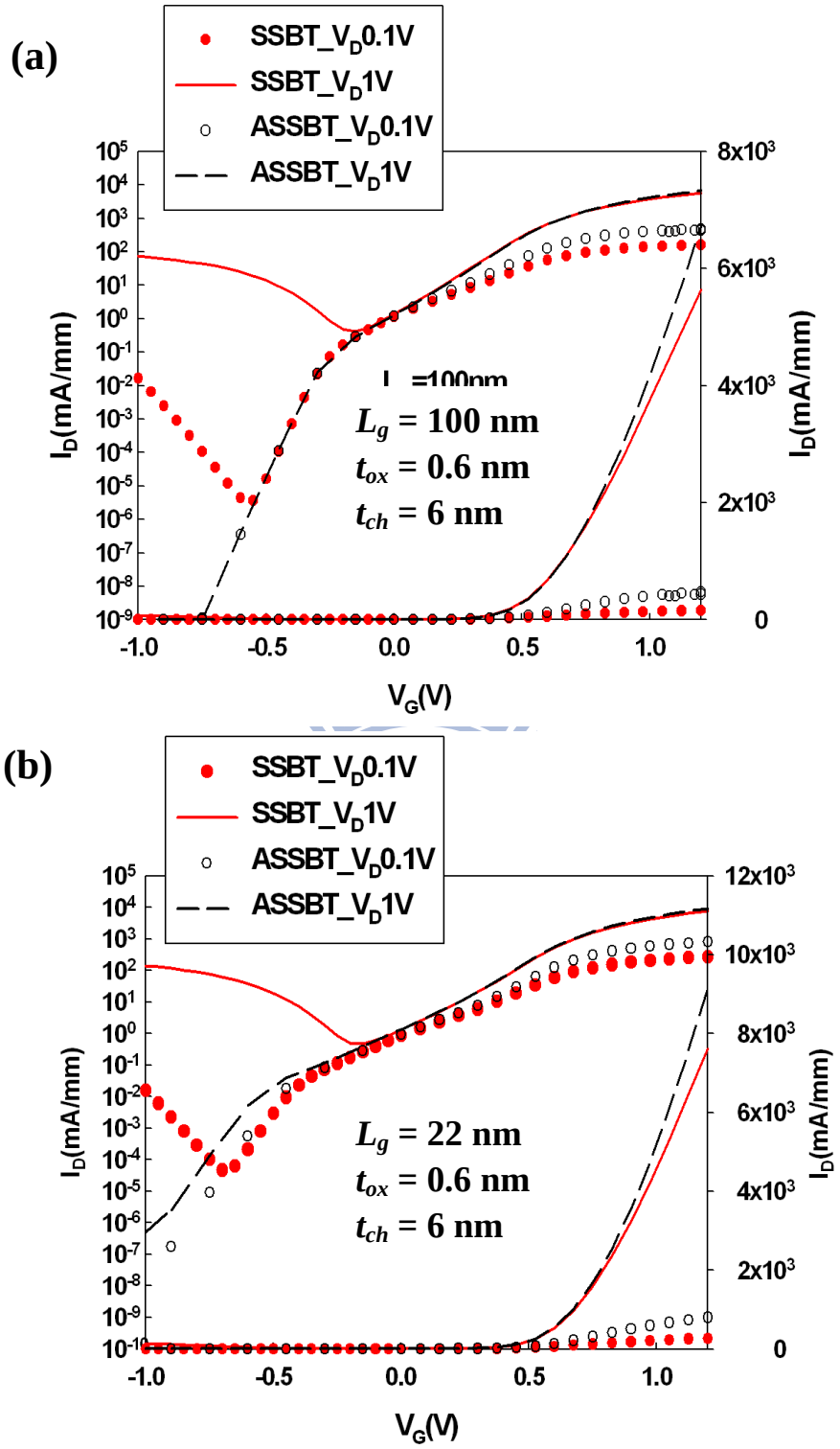


Fig. 6-2 Comparisons of the I_D-V_G characteristics of SSBT and ASSBT with channel length of (a) 100 nm and (b) 22 nm.

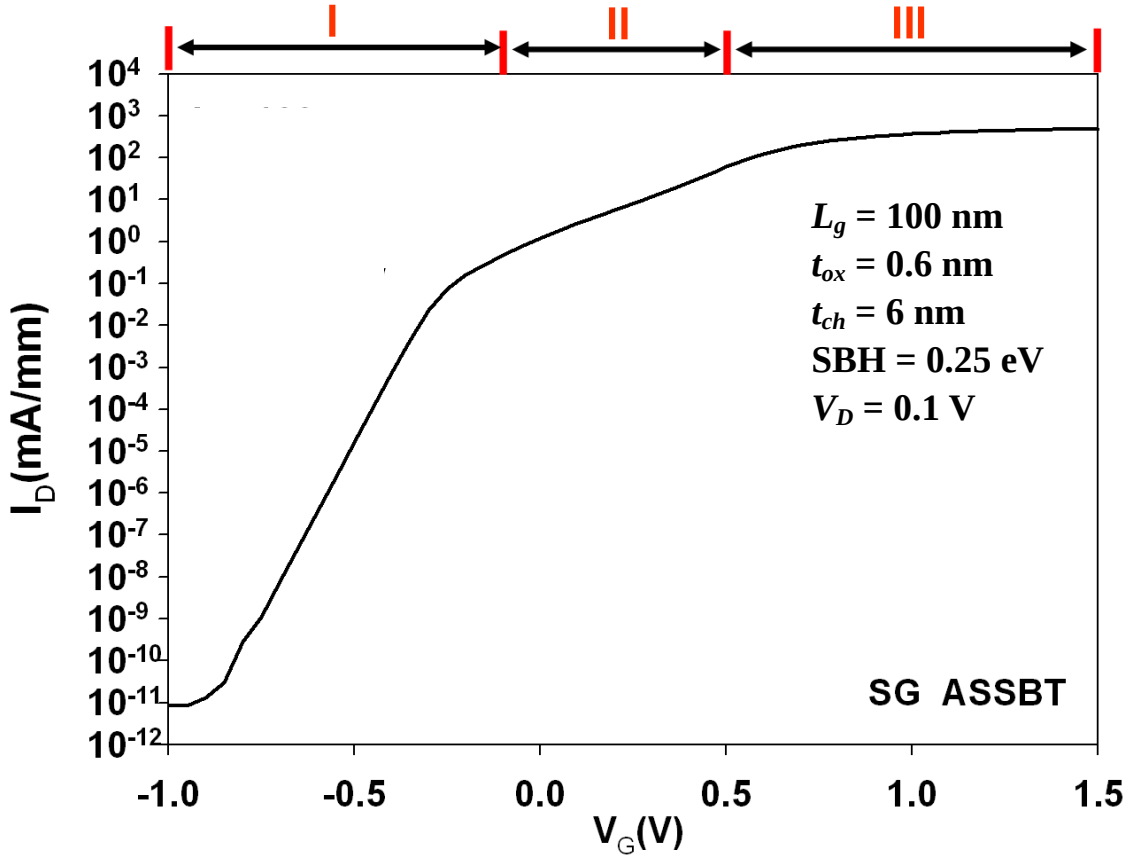


Fig. 6-3 Operation regions presented in the I_D-V_G characteristics of an ASSBT.

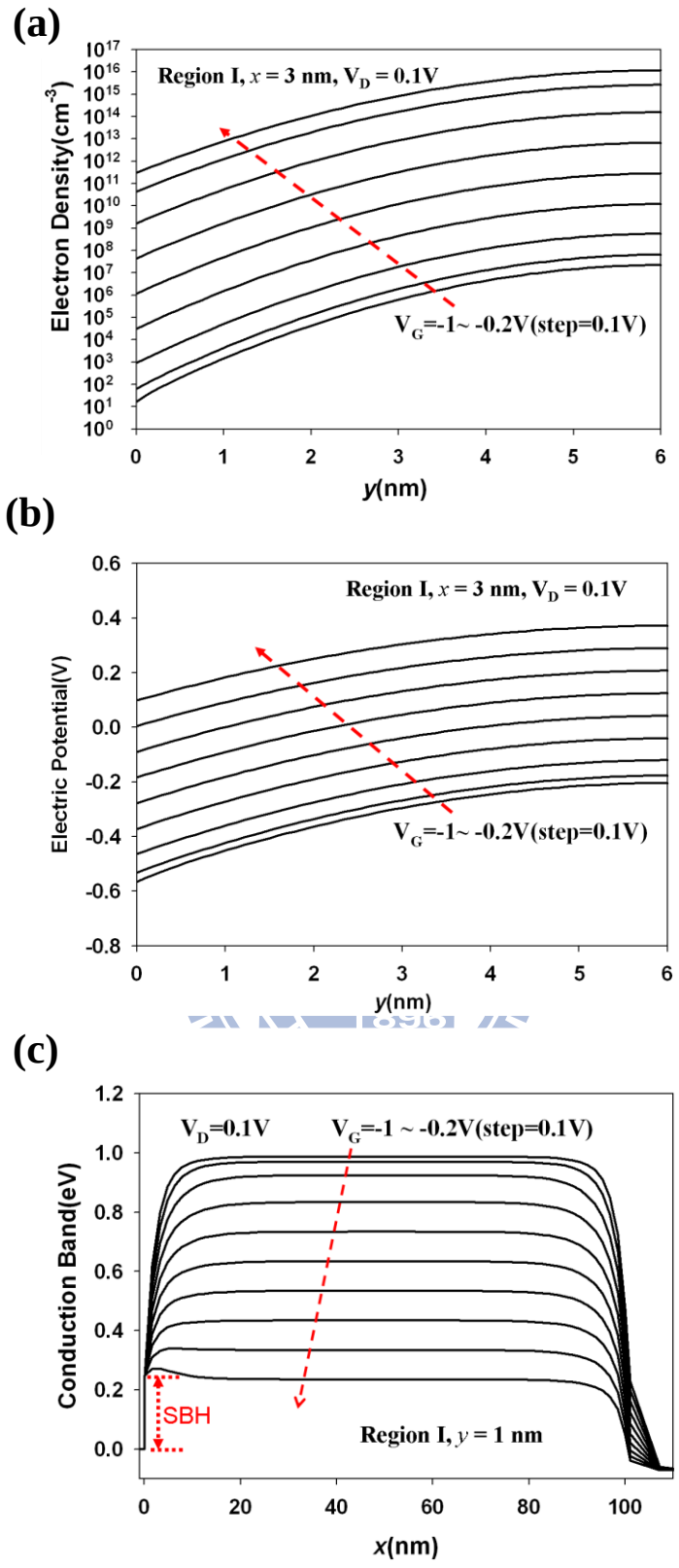


Fig. 6-4 (a) Electron density and (b) electric potential through the silicon channel along *y* direction at *x* = 3 nm, and (c) the potential diagram along *x* direction while the ASSBT is operated in region I.

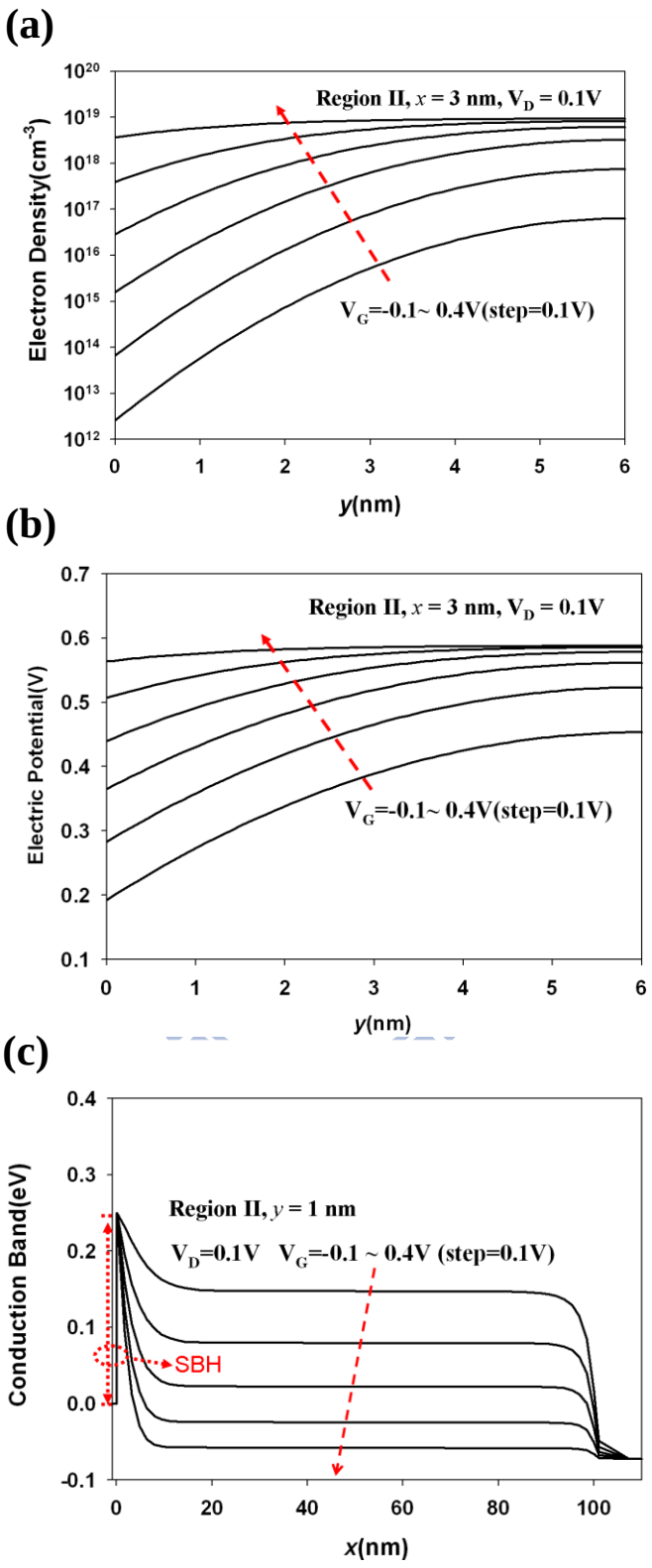


Fig. 6-5 (a) Electron density and (b) electric potential through the silicon channel along *y* direction at *x* = 3 nm, and (c) the potential diagram along *x* direction while the ASSBT is operated in region II.

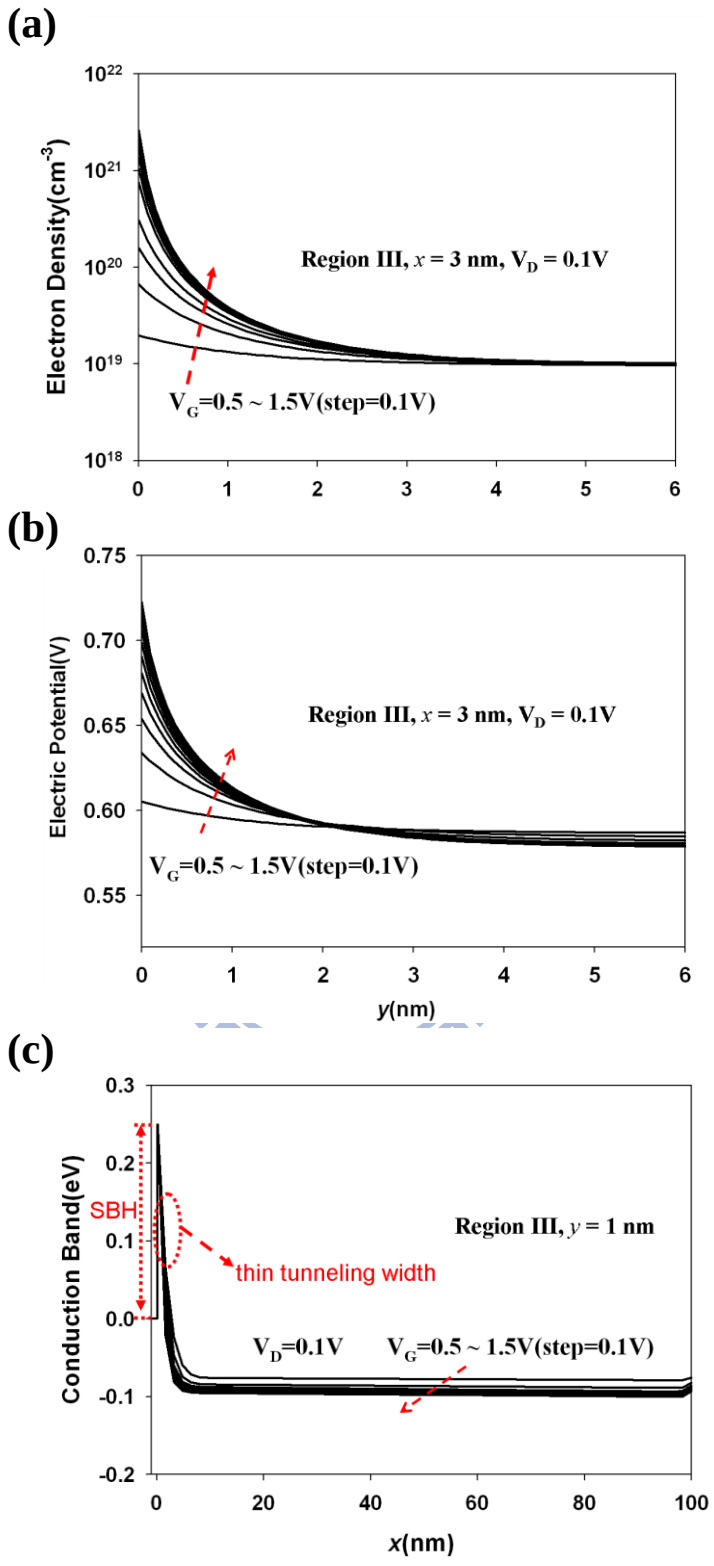


Fig. 6-6 (a) Electron density and (b) electric potential through the silicon channel along y direction at x = 3 nm, and (c) the potential diagram along x direction while the ASSBT is operated in region III.

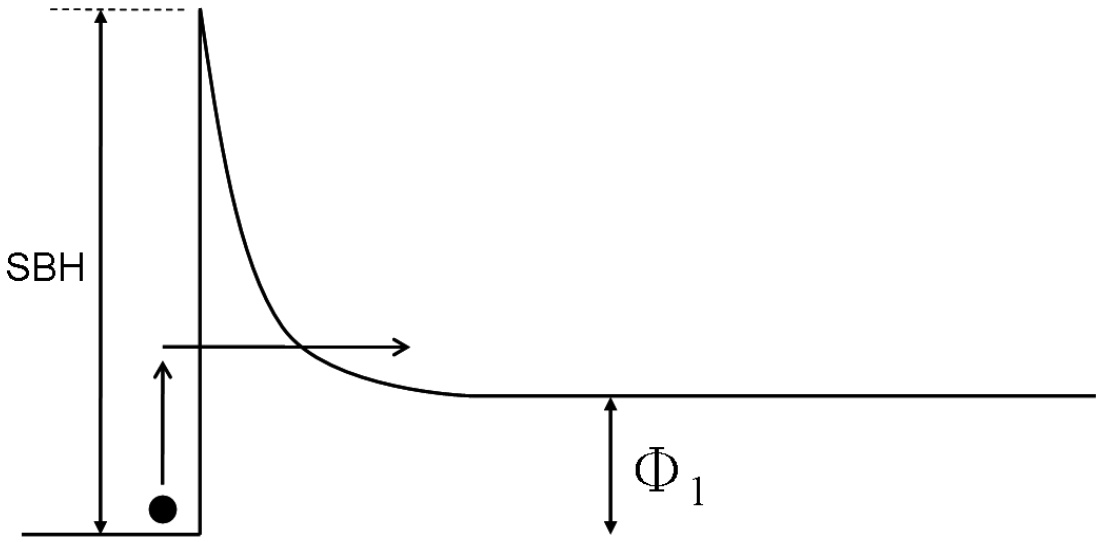


Fig. 6-7 Band diagram of the ASSBT operated in region II showing the thermionic field emission process.

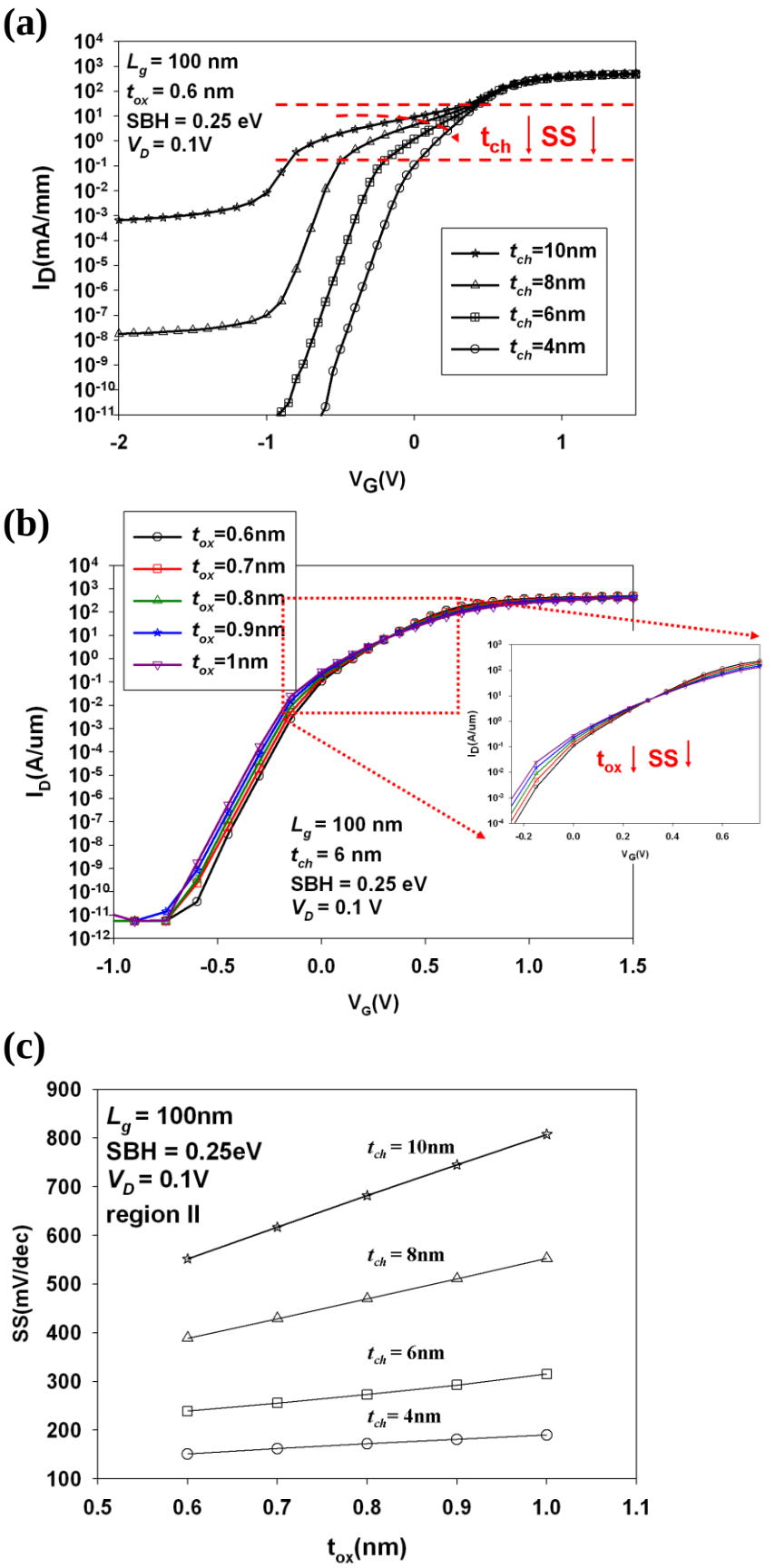


Fig. 6-8 I_D-V_G characteristics of ASSBTs with various (a) t_{ch} and (b) t_{ox}. (c) SS versus t_{ox} with t_{ch} as a parameter for ASSBTs operated in region II.

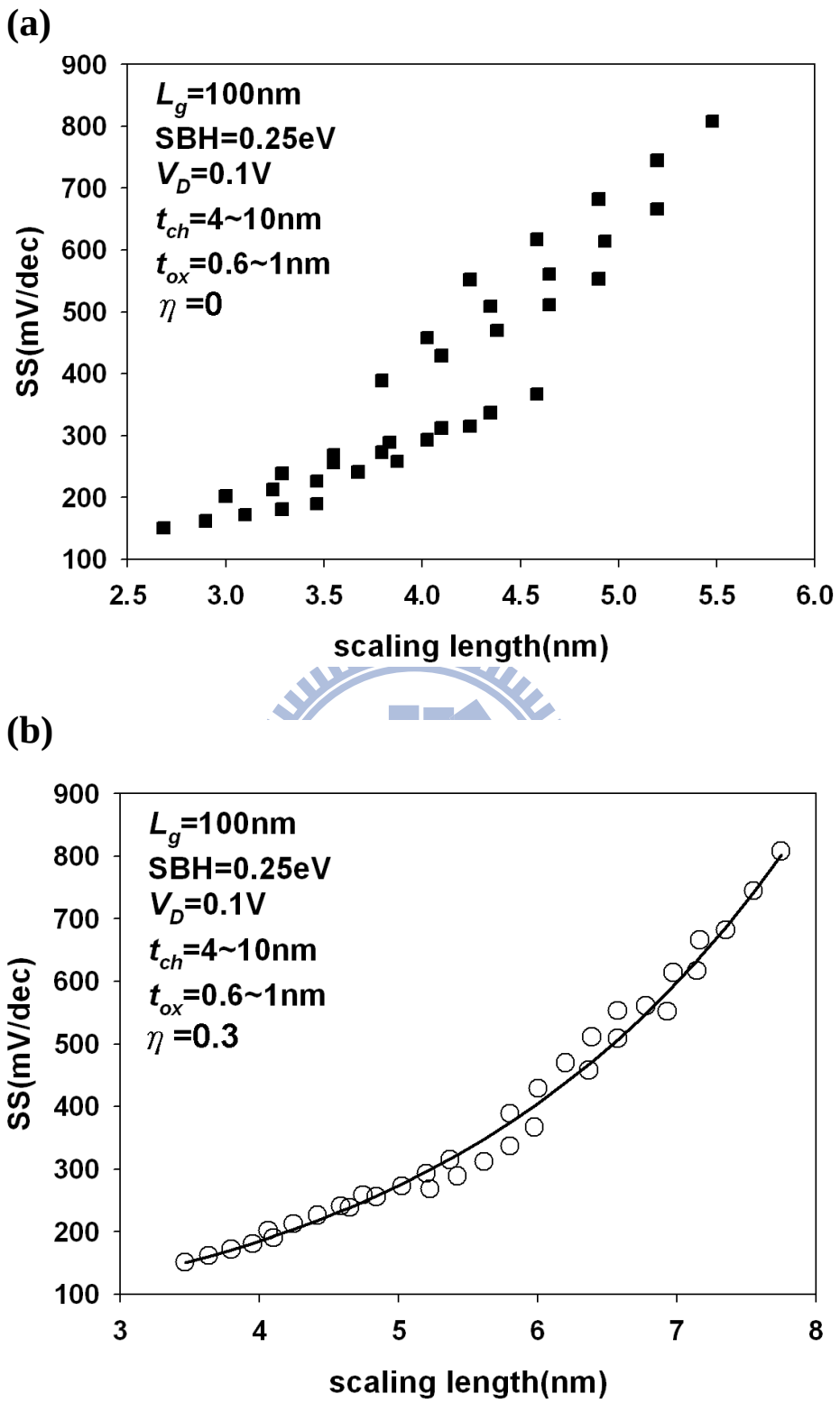


Fig. 6-9 The SS versus λ with (a) η = 0 and (b) η = 0.3. In (b), the data are described well by a fitting curve.

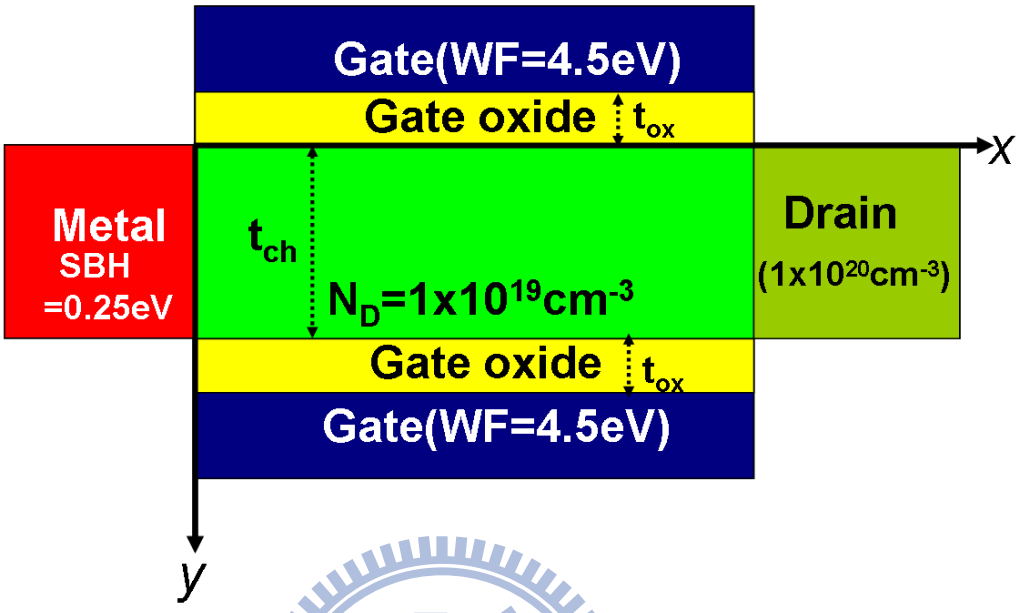


Fig. 6-10 Schematic diagram of the DG ASSBT with SBH=0.25eV.

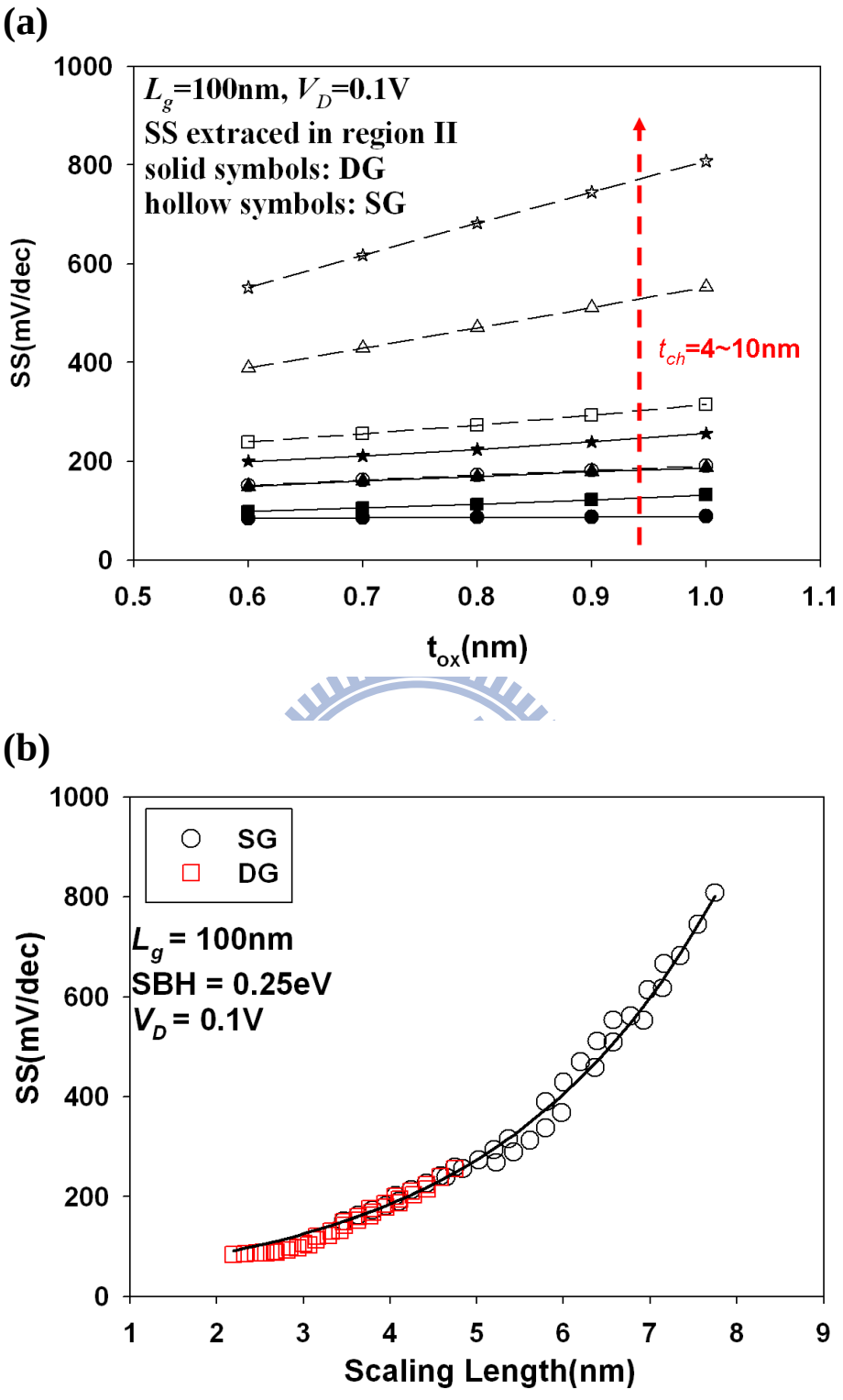


Fig. 6-11 (a) The comparison of SS for SG and DG ASSBTs with various t_{ch} and t_{ox}. (b) The SS versus λ for SG and DG ASSBTs with η = 0.3.

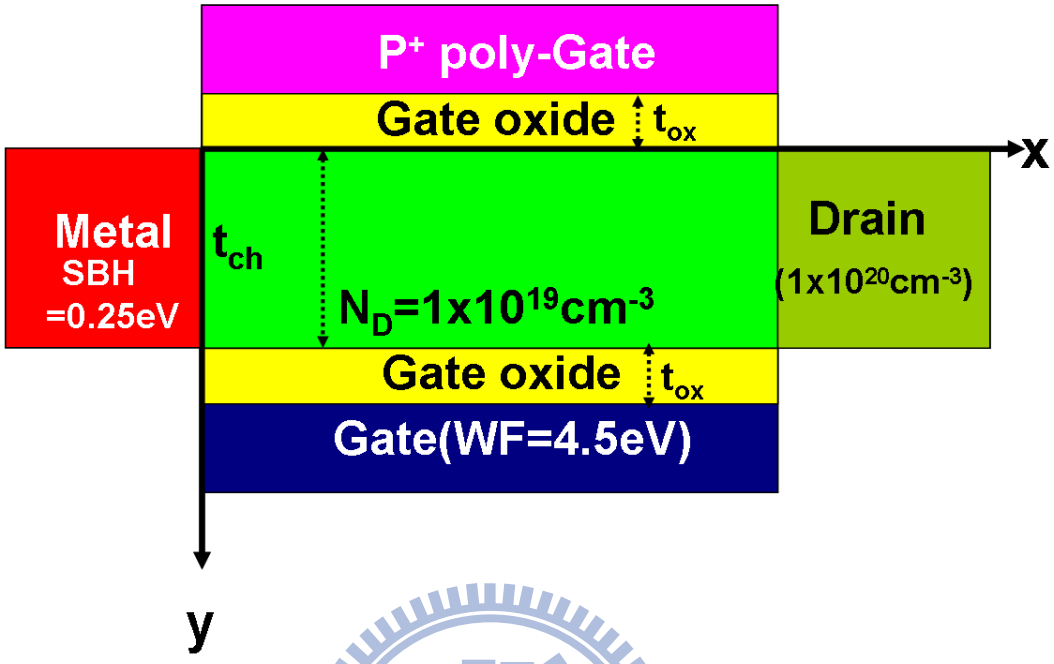


Fig. 6-12 Schematic diagram of the n-type dual-workfunction (DW) DG ASSBT with SBH = 0.25 eV.

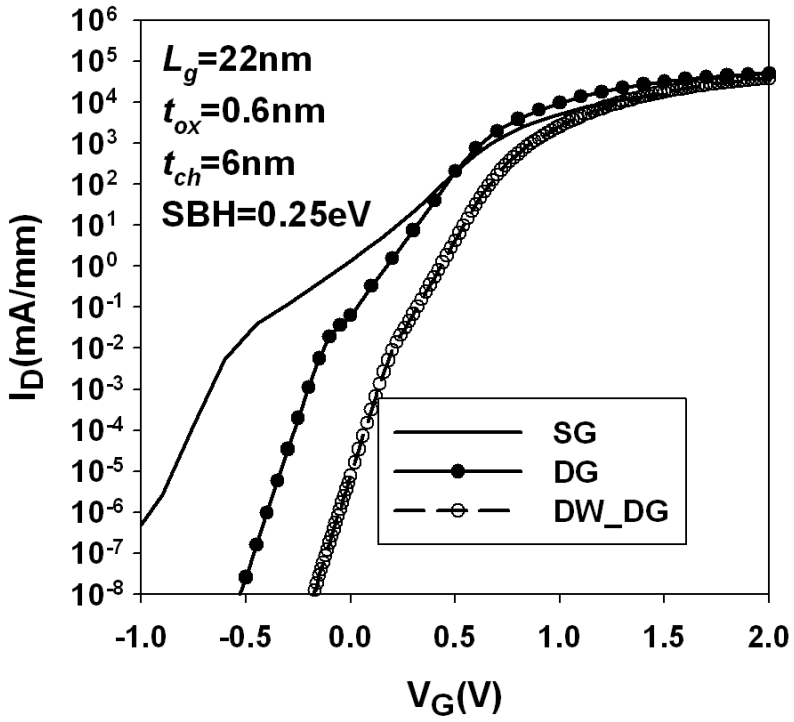


Fig. 6-13 Comparisons of the I_D-V_G characteristics of SG, DG, and DW DG ASSBTs with channel length of 22 nm.

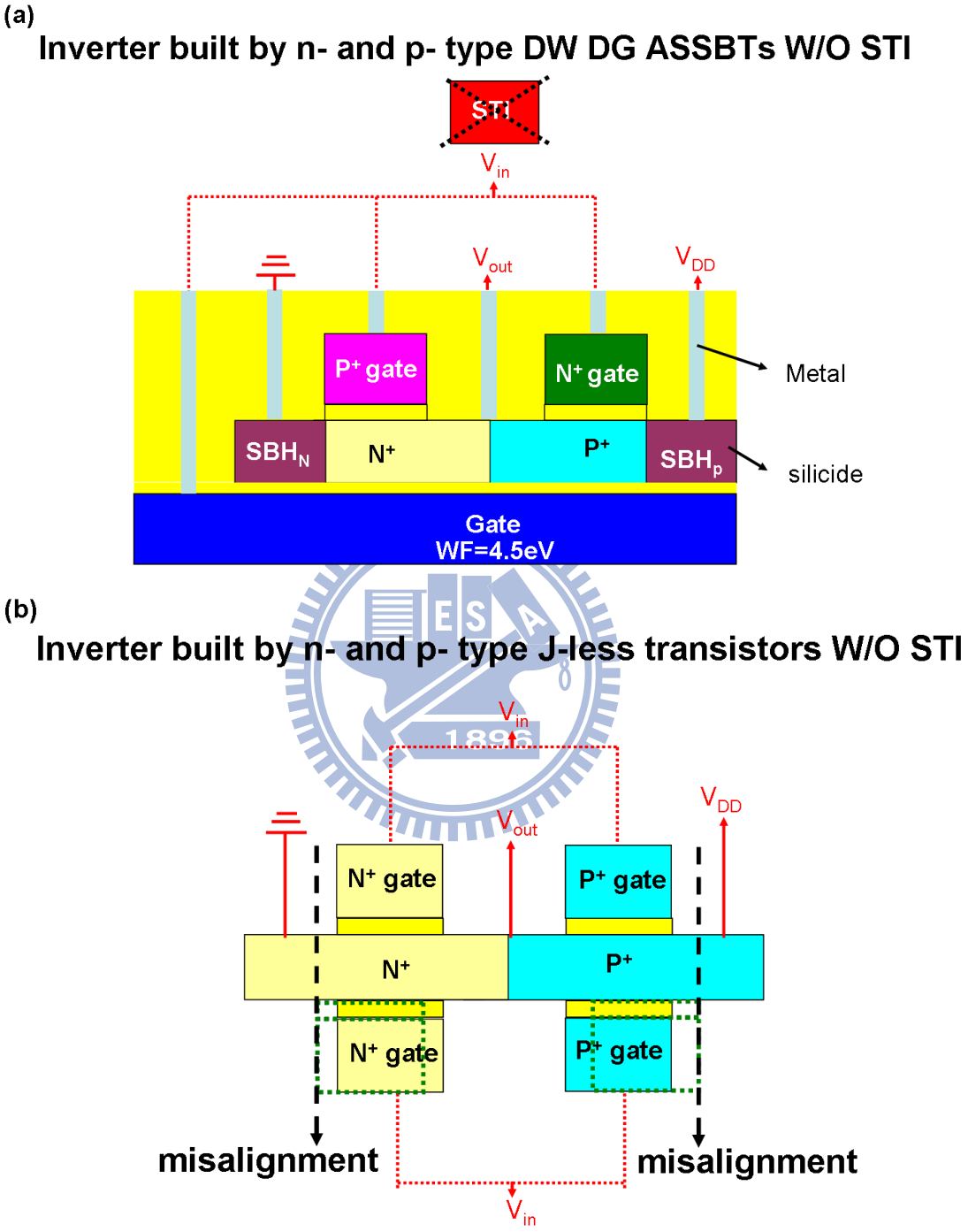


Fig. 6-14 Schematic diagram of (a) the proposed new inverter built by a pair of n- and p-type DW DG ASSBTs sharing a common back-gate with workfunction of 4.5 eV and (b) the inverter proposed in the previous study [6.19].

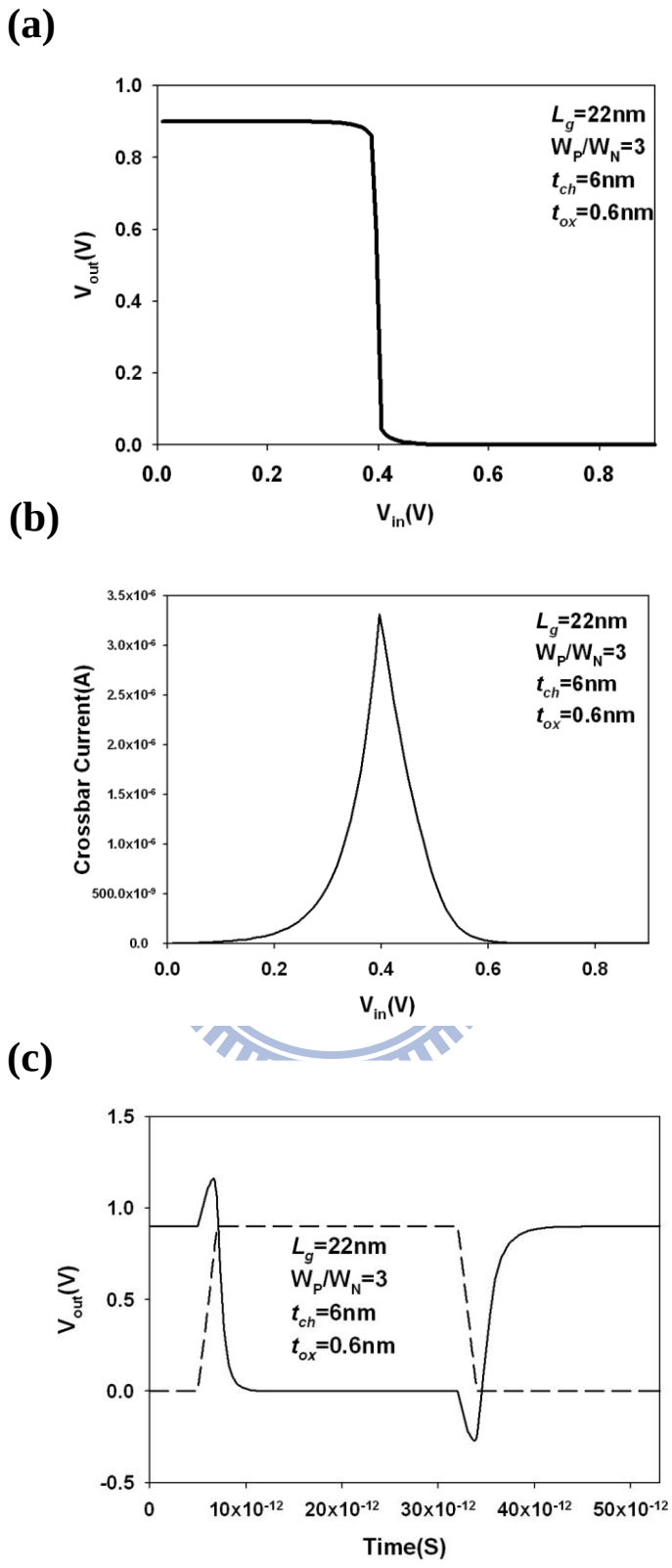


Fig. 6-15 (a)V_{in}-V_{out} characteristics, (b) switching current and (c) AC transient output voltage of the proposed new inverter (Fig. 6-14(a)).

Chapter 7

Mechanisms for Sub-60 mV/dec Subthreshold Swing (SS) Found in Gate-All-Around Polycrystalline Silicon Nanowire Thin-Film Transistors (TFTs)

7-1 Introduction

For a conventional MOSFET, as the device is switched from off- to on-state, thermionic emission dominates the conduction of carriers from source to drain. As a result, the ideal subthrshold swing (SS) of a conventional MOSFET is about 60 mV/dec at room temperature [7.1]. In this chapter, we report an unexpected sub-60 mV/dec SS found in Gate-all-around (GAA) poly-Si nanowire (NW) thin-film-transistors (TFTs).

As mentioned in Sec. 1-5, several kinds of devices featuring sub-60 mV/dec SS have been reported previously, such as tunneling field-effect transistors (TFET) [7.2]~[7.4], impact-ionization metal-oxide-semiconductor field-effect transistors (I-MOS) [7.5]~[7.7], and silicon-on-insulator (SOI) devices or TFTs with large grain

caused by latch-up [7.8]~[7.10]. However, all of their corresponding theories are not suitable to explain the abnormal sub-60 mV/dec SS characterized in this chapter. For TFET and I-MOS devices, both consist of a gated p-i-n diode and are operated under reverse biased and, thus, are structurally different from the GAA poly-Si NW TFTs investigated in this chapter. For the latch-up phenomenon found in n-channel SOI devices or TFTs with large grains, it is mainly related to the action of impact ionization process occurring in the channel and the resulted SS is usually smaller than 10 mV/dec while V_{th} is reduced with increasing drain voltage (V_D). These properties are contrary to what were observed in this chapter that SS is not so steep while V_{th} increases with increasing V_D.

Based on the preliminary check of the device characteristics, such an abnormal phenomenon observed in our study is postulated to be related to the trap-assisted band-to-band tunneling (BTBT) current. To confirm our postulation, more efforts have been conducted and the results and analysis are presented in this chapter. The rest of this chapter is organized as follows: First, Sec. 7-2 shows the architecture and fabrication process of the GAA poly-Si NW TFTs investigated in this chapter. Next, in Sec. 7-3, effects of major operation parameters, like the gate and drain voltages, on the electrical characteristics of the devices are studied. It is unambiguously shown that the occurrence of the abnormally low SS is accompanied by a high off-state leakage. A qualitative

model related to the hole-trapping in granular poly-Si channel is proposed in Sec. 7-4 to explain the findings observed in Sec. 7-3. Afterwards, the impacts from device structure, such as channel length and gate configuration, are examined in Sec. 7-5. Finally, the conclusion is summarized in Sec. 7-6.

7-2 Device Fabrication

Figures 7-1 (a) and (b) show the stereo structure and top view of the GAA poly-Si NW TFTs investigated in this chapter. The device fabrication flow basically follows that of GAA J-less poly-Si NW transistors described in Chapter 4 except for the step shown in Fig. 4-1(d). Specifically, the GAA ploy-Si NW TFTs studied in this chapter are conventional inversion-mode (IM) field-effect transistors, featuring undoped poly-Si NWs as the conduction channels. Therefore, the deposition of a 100 nm *in situ* phosphorous-doped poly-Si film in Fig. 4-1(d) is replaced by an undoped amorphous-Si (α -Si) one, followed by an annealing step performed at 600℃ in N_2 ambient for 24 hours to transform theα -Si into polycrystalline phase. The cross-sectional TEM image of a fabricated device is shown in Fig. 7-2, indicating the GAA poly-Si NW transistor investigated in this chapter features almost square cross-section of poly-Si NWs and the feature size of poly-Si NWs is about 20 nm.

7-3 Abnormal Subthreshold Characteristics of the GAA Poly-Si NW Transistors

The transfer characteristics of the long-channel GAA poly-Si NW TFT with channel length (L_g) of 5 μm are shown in Fig. 7-3(a) as a function of drain voltage (V_D). The threshold voltage (V_{th}) and SS extracted from Fig. 7-3(a) as a function of V_D are depicted in Figs. 7-3(b) and (c), respectively. Please note that, in this chapter, because we pay special attentions to the specific phenomenon related to the sub-60 mV/dec SS, the extracted SS depicted in all of the figures refers to the minimum value through the whole subthreshold region. In addition, V_{th} is defined as the gate voltage at which the drain current is equal to 30 nA × W/L_g. Figures 7-3(b) and (c) indicate that V_{th} dramatically increases while SS suddenly drops and even breaks the limit of 60 mV/dec at room temperature [7.1] as V_D is larger than 1 V. To gain more insights into the root cause of the observed abnormal trends, we carefully examine the transfer characteristics shown in Fig. 7-3(a) and find that the occurrences of the above phenomena as V_D > 1 V are accompanied by a significant rise in the off-state leakage. Such a leakage shows a strong dependence on the voltage difference between the V_G and V_D (*i.e.*, V_{GD}) and is attributed to the trap-assisted band-to-band tunneling (BTBT) current [7.12]~[7.13] occurring at the drain junction.

For further clarification, the transfer characteristics were characterized again by

varying the starting point of sweeping V_G at V_D of 3 V. The measured results are shown in Fig. 7-4(a). In addition, the extracted V_{th} and SS from the transfer characteristics shown in Fig. 7-4(a) are individually depicted in Figs. 7-4(b) and (c) as a function of the staring V_G in the measurements. As shown in Fig. 7-4(a), trap-assisted BTBT current remarkably increases when the starting V_G is smaller than 0.25 V, accompanied with a sudden increment of V_{th} and an abrupt drop of SS which could be smaller than 60 mV/dec, as shown in Figs. 7-4(b) and (c), respectively. Nonetheless, such a trap-assisted BTBT leakage disappears and the transfer curves become normal as the starting V_G is equal or larger than 0.5 V.

Next, we performed the measurements by first forward sweeing (FS) V_G from -1 to 2 V and then backward sweeping (BS) V_G from 2 to -1 V at V_D of 0.1 or 2 V. The measurement results are shown in Fig. 7-5, in which an abnormal increment of V_{th} and sub-60 mV/dec SS appear again in FS case at V_D of 2 V, owing to the high trap-assisted BTBT current again. However, such an abnormal phenomenon disappears in the BS case. The major difference between the FS and BS cases is that the trap-assisted BTBT current is present at the beginning of the FS measurement. Therefore, it is reasonable to postulate that the occurrence of the trap-assisted BTBT current generated at the beginning is the culprit to trigger the abnormal changes of V_{th} and SS. In addition, it is worth noting that, based on our previous work [7.14], the hysteresis window between

FS and BS measurement results shown in Fig. 7-5 is related to the electron trapping and de-trapping processes associated with the deep level traps in the grain boundaries of the poly-Si channel.

In short, results of the above-mentioned experimental measurements affirm the correlation of the high trap-assisted BTBT current with unconventional changes of V_{th} and SS. In the next section, a qualitative model is proposed to describe the above observations.

7-4 Proposed Mechanisms and Discussion

All of the above measured results suggest that the exclusivity reported in this work is related to the conduction of the high trap-assisted BTBT current at the beginning point during the I_D-V_G measurement. A closer look at trap-assisted BTBT current indicates that holes would be generated by the trap-assisted BTBT process and flow toward the source through the NW channels. Nonetheless, some of them would get trapped by the defects located in the grain boundaries of the poly-Si NWs near the source side if the channel length of transistor is long enough. These traps are mainly donor-like states located at the bottom half of silicon energy bandgap [7.15]. Such hole-trapping events would likely be responsible for the abnormal subthreshold characteristics of the characterized devices.

In the following we proposed a scenario to explain the findings presented in previous sections. Fig. 7-6 schematically shows the band diagram of GAA poly-Si NW TFT along the source-to-drain direction accounting for the hole-trapping process stated above. In the figure the channel potential near the source junction is raised as the generated holes are trapped wherein. The extent of the additional rise in channel potential (Φ_{SB} in Fig. 7-6) is related to the amount of trapped holes which is mainly determined by the magnitude of the trap-assisted BTBT current. As a result, a gate bias bigger than the case when no holes are trapped is needed to switch the device on in order to overcome the additional barrier height. This explains the monotonic increase of V_{th} with increasing V_D as V_D is larger than 1V shown in Fig. 7-3(b). As the starting V_G is larger than 0.25 V the aforementioned BTBT current is eliminated, and thus no hole-trapping would occur, the transfer curves shown in Fig. 7-4(b) thus become normal.

Devices' turn-on behavior, *i.e.*, the SS, is affected by the hole-trapping as well. Conventionally the conduction in subthreshold regime is mainly through thermionic emission of carriers from the source junction and the subthreshold swing is thus limited to 60 mV/dec [7.1]. Such a process is shown in Fig. 7-7 and denoted as the Process (1). In the same figure, an additional current component denoted as the Process (2) is also shown to explain the occurrence of steeper SS as the applied V_{GD} is high. This

component arises from the recombination of electrons injected from the source and the trapped holes in the channel. Neutralization of the trapped holes through this step quickly lowers the barrier height at the source junction. As a result, the thermionic emission [Process (1)] is greatly enhanced, thus conducting more current. Therefore SS is reduced, and can even reach a value smaller than the 60 mV/dec limit at room temperature, as confirmed in the measurements. The impacts from the structure of the device including channel length and gate configuration on the abovementioned phenomena are investigated in the next section.

7-5 Impacts of Channel Length and Gate Configuration on the Abnormal V_{th} and SS

In order to address the impact from channel length, I_D-V_G characteristics of GAA poly-Si NW TFTs with L_g of 2 and 0.4 μm were measured under various V_D. The results are depicted in Figs. 7-8(a) and (b) for devices with L_g of 2 and 0.4 μm, respectively. V_{th} and SS extracted from the two figures and the data shown in Figs. 7-3(b) and (c) for L_g of 5 μm are plotted together in Figs. 7-9(a) and (b), respectively, for comparison. From Figs. 7-9(a) and (b), two interesting phenomena can be found. First, the unexpected monotonic increase of V_{th} as V_D > 1 V shown by the devices with L_g of 5 μm disappears as the channel length is shorter. Second, the abrupt drop of SS as V_D > 1V shown by the

devices with L_g of 5 μm is relieved for devices with L_g of 2 μm and no sub-60 mV/dec data are recorded. Furthermore, as the channel length is scaled down to 0.4 μm, SS shows no clear dependence on V_D.

All of these phenomena can also be explained by the above qualitative model. As the channel length of GAA poly-Si NW TFTs is reduced, most of the holes generated by high trap-assisted BTBT current near the drain side can directly flow through NW channel into the source rather than trapped in the poly-Si NW. Thus, the amount of trapped holes is dramatically reduced as the channel is shortened and leads to the outcomes different from those observed in long-channel ones. As a result, as shown in Fig. 7-9(b), although SS still decreases with increasing V_D, values smaller than 60 mV/dec are not found for transistors with L_g shorter than 2 μm. Furthermore, as the channel is further scaled down to 0.4 μm, fewer holes are trapped wherein and, thus, the abnormal change of SS disappears altogether.

Next, we continue to investigate the impact of gate configurations on the transfer characteristics of GAA poly-Si NW TFTs with L_g = 5 μm. For this purpose, single-gated (SG) poly-Si NW TFTs were also fabricated. The fabrication process is identical to that of GAA poly-Si NW TFTs except for the step shown in Fig. 4-1(e). As shown in Fig. 7-10, by preserving the dummy nitride/oxide/nitride gate stack, which is originally removed in the GAA configuration, poly-Si NW TFTs with SG configuration can be

achieved. The cross-sectional TEM image of a SG poly-Si NW TFT is shown in Fig. 7-11, indicating that only one side of the poly-Si NW channel is controlled by the poly-Si gate.

Figure 7-12(a) depicts the I_D-V_G characteristics of the SG poly-Si NW device with L_g = 5 μm at various V_D. The V_{th} and SS extracted from Fig. 7-12(a) are shown in Figs. 7-12(b) and (c), respectively. It is seen in the figures that the measured results show distinctly different trends from those exhibited by the GAA poly-Si NW TFT with L_g of 5 μm, although high off-state leakage currents are still found in Fig. 7-12(a). This indicates that the gate configuration indeed plays an important role in the aforementioned phenomena. To help understand the situation, band diagrams of GAA and SG poly-Si NW TFTs near the source side perpendicular to source-to-drain direction are plotted in Figs. 7-13(a) and (b), respectively. Unlike the situation of the GAA device shown in Fig. 7-13(a), the trapped holes are located close to the un-gated side. Thus, impact of the raised potential by trapped holes (see Fig. 7-6) is dramatically weakened. Consequently, the above-mentioned abnormal trends regarding V_{th} and SS would disappear in the SG devices.

7-6 Summary

In summary, the abnormal increase in V_{th} and reduction in SS with increasing V_D

found in GAA poly-Si NW TFT are reported for the first time. A qualitative model related to the trapping of excessive holes generated by the high off-state current and later recombination of these trapped holes when operating in the subthreshold regime is suggested for explaining such particular phenomena. The experimental data also indicate that structural factors, such as channel length and gate configuration, play important roles in this phenomenon. As the devices are with a shorter channel length or controlled by an SG configuration, the abnormal phenomena found in the long channel (L_g = 5 μm) GAA ploy-Si NW TFTs are relieved or even negligible.

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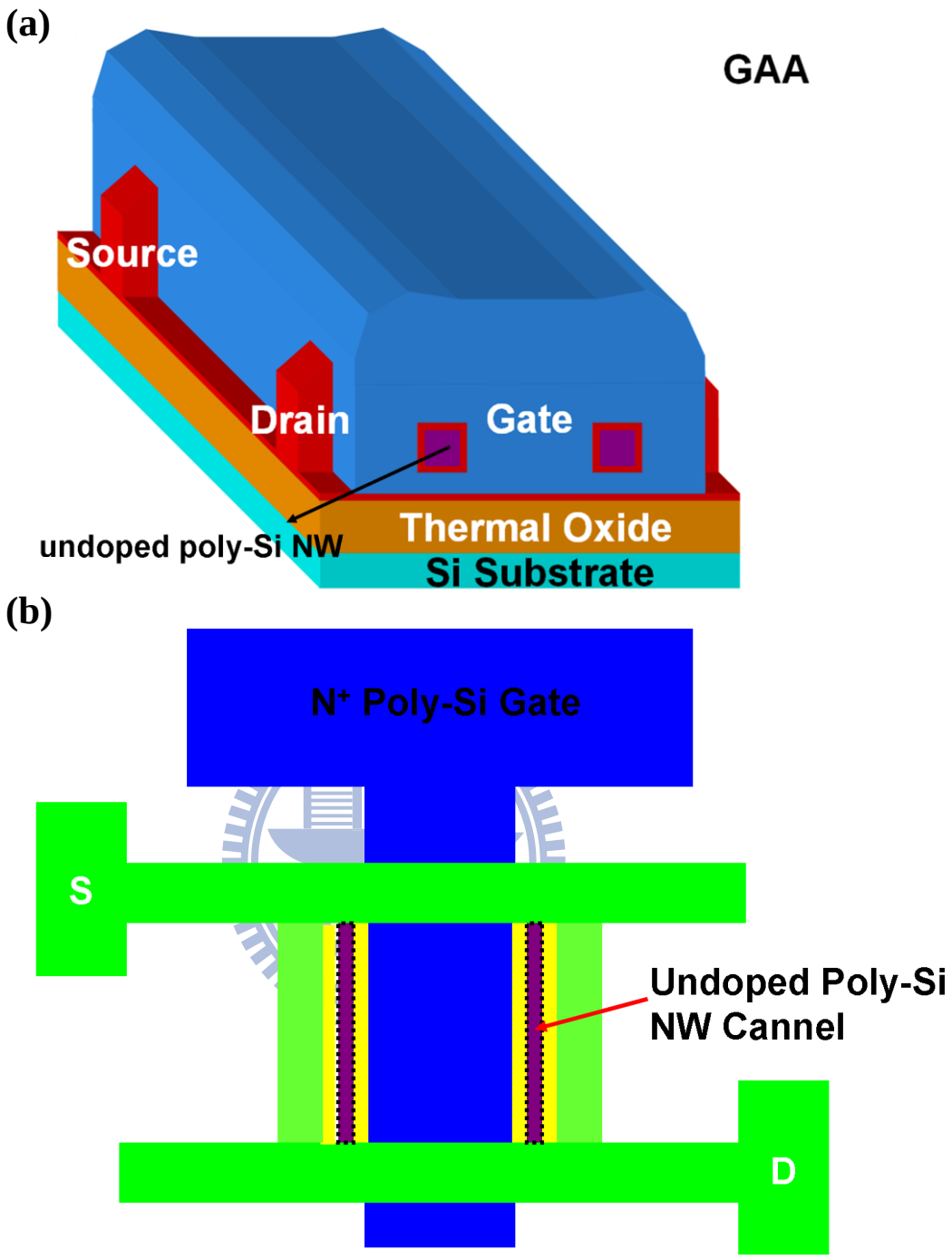

Fig. 7-1 (a) 3-D schematic structure and (b) top view of the GAA poly-Si NW TFT investigated in this study.

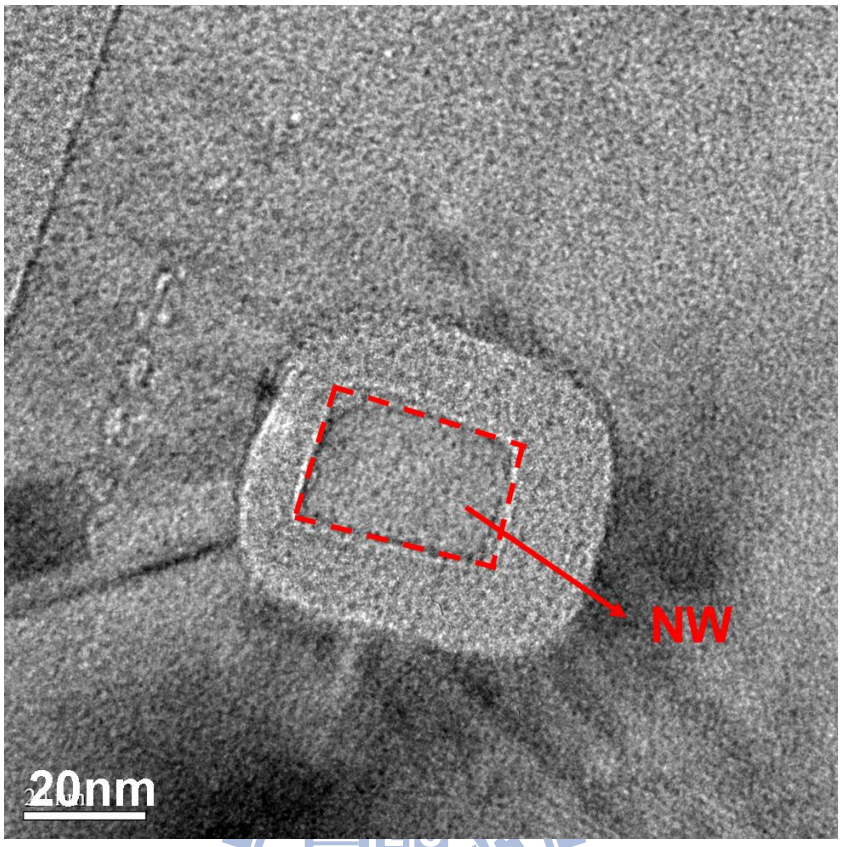

Fig. 7-2 Cross-sectional TEM image of a fabricated GAA poly-Si NW TFT.

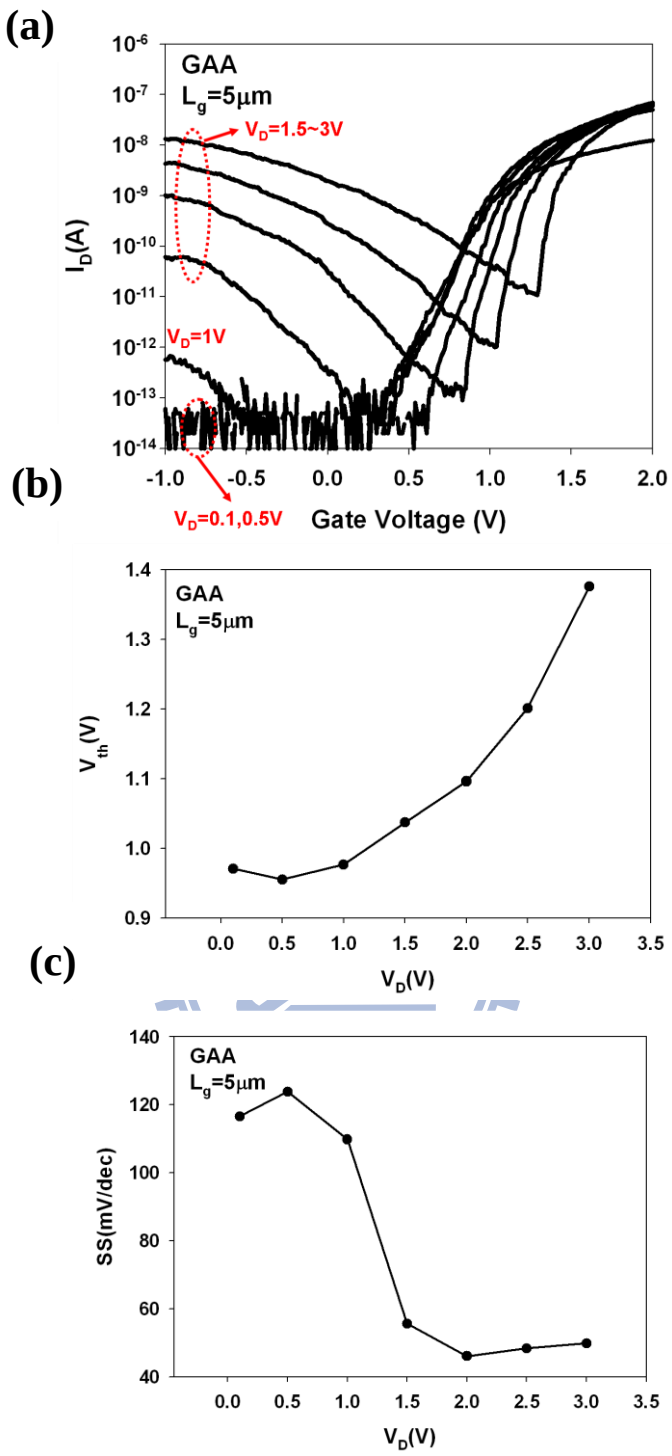

Fig. 7-3 (a) Transfer characteristics as well as (b) the extracted V_{th} and (c) SS of a GAA poly-Si NW TFT with L_g = 5 μm as a function of V_D.

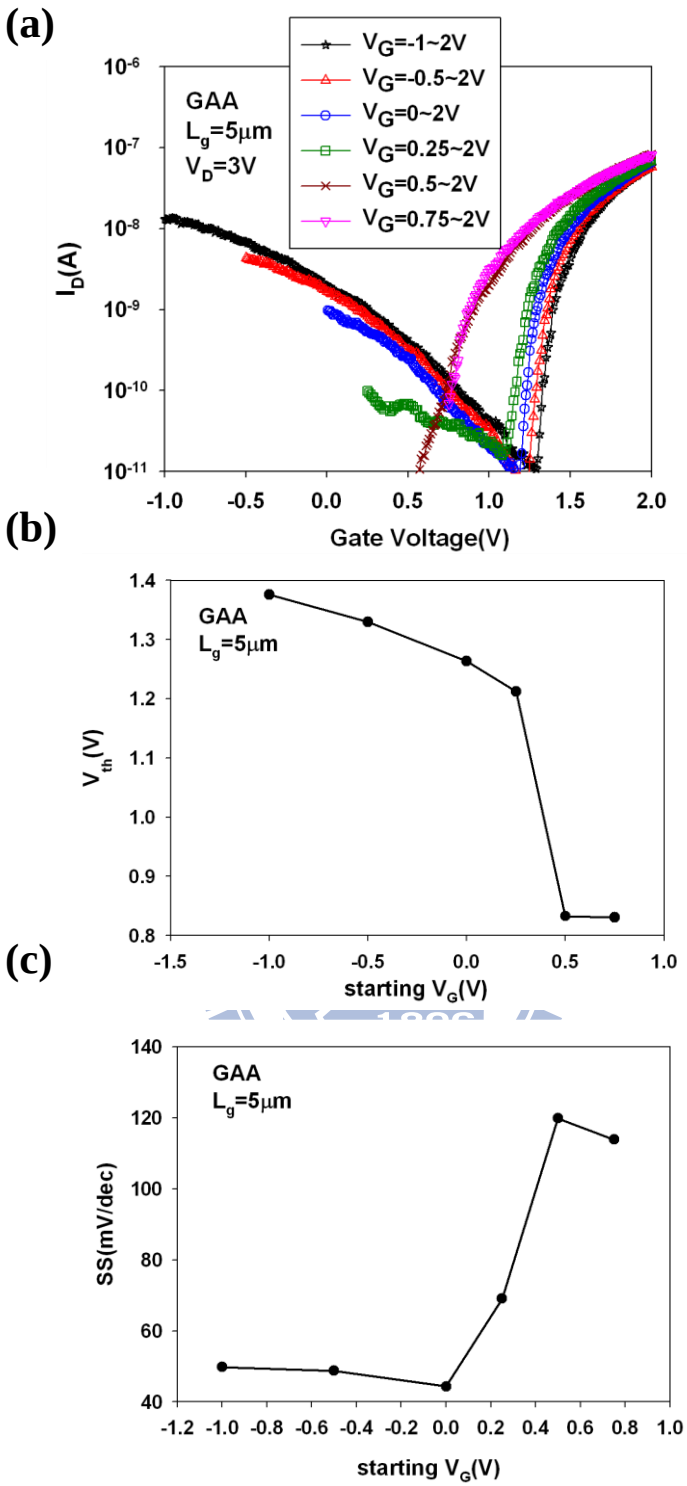

Fig. 7-4 (a) Transfer characteristics as well as (b) the extracted V_{th} and (c) SS of a GAA poly-Si NW TFT with L_g = 5 μm with different starting point of V_G while fixed V_D of 3V.

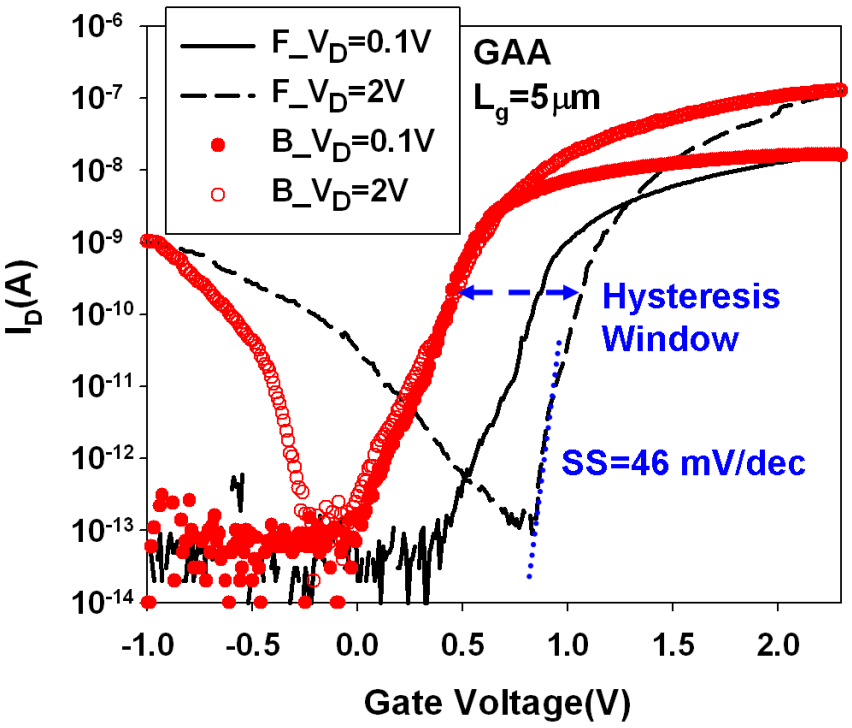

Fig. 7-5 I_D-V_G characteristics of a GAA poly-Si NW TFT with L_g = 5 μm at V_D = 0.1 and 2 V. The measurement first swept V_G from -1 to 2 V (Forward Sweeping) and then from 2 to -1 V (Backward Sweeping).

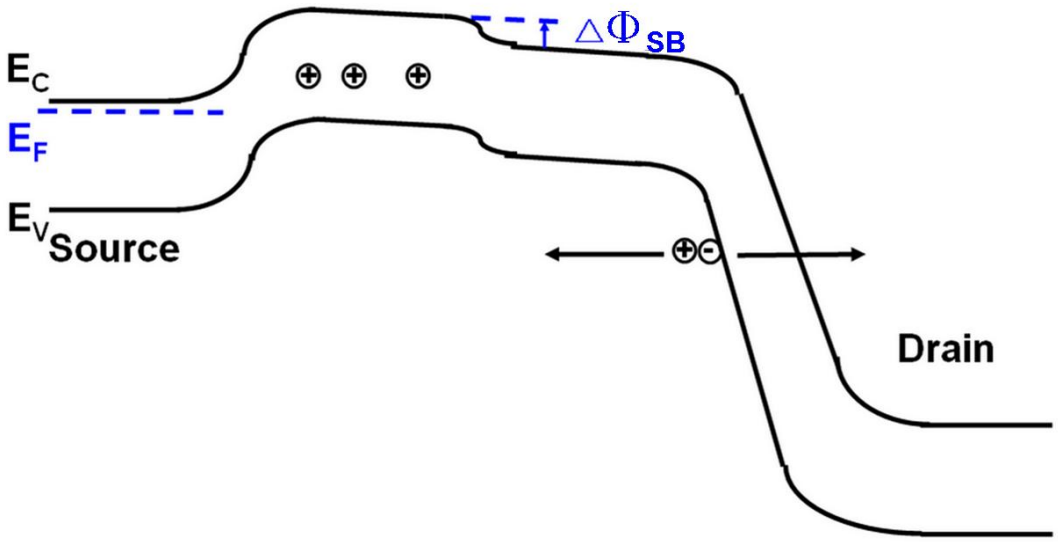

Fig. 7-6 Band diagrams along the poly-Si NW channel in the off-state, illustrating the generation of holes in the drain junction and the hole-trapping events in the channel near the source junction.

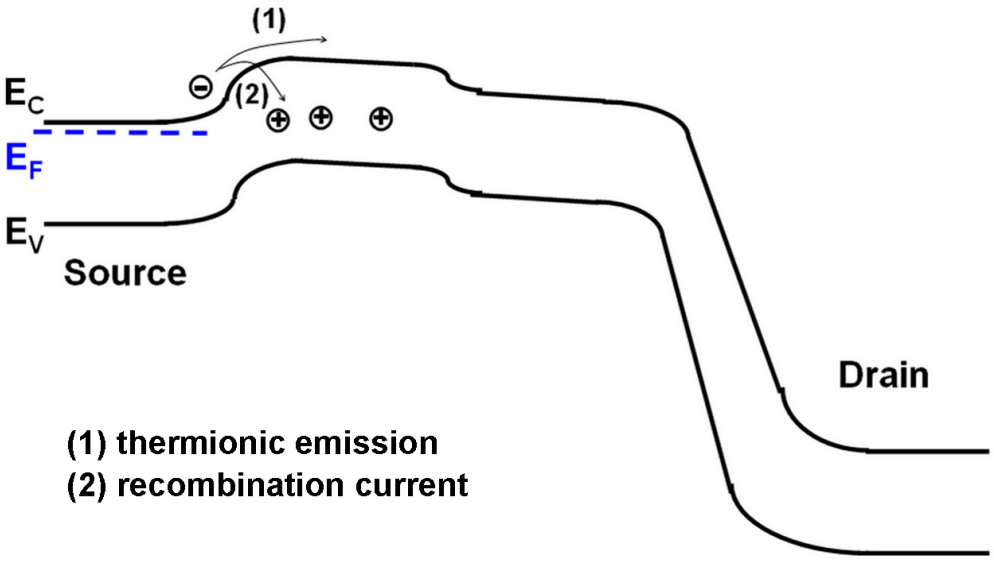

Fig. 7-7 Band diagrams along the poly-Si NW channel in the subthreshold regime, illustrating the thermionic emission (1) and the electron-hole recombination (2) processes.

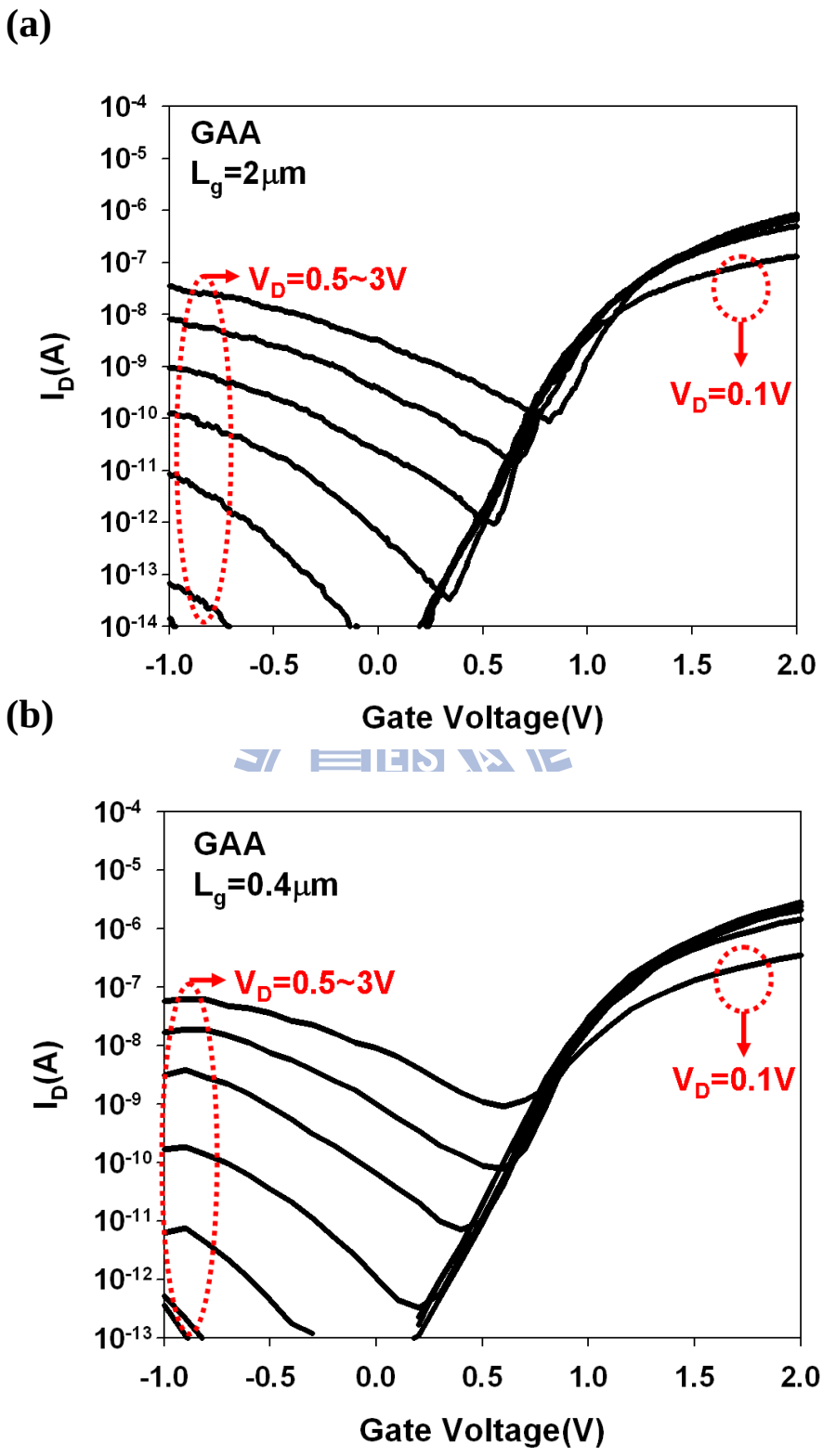

Fig. 7-8 I_D-V_G characteristics of GAA poly-Si NW TFTs with (a) L_g = 2 μm and (b) 0.4 μm as a function of V_D.

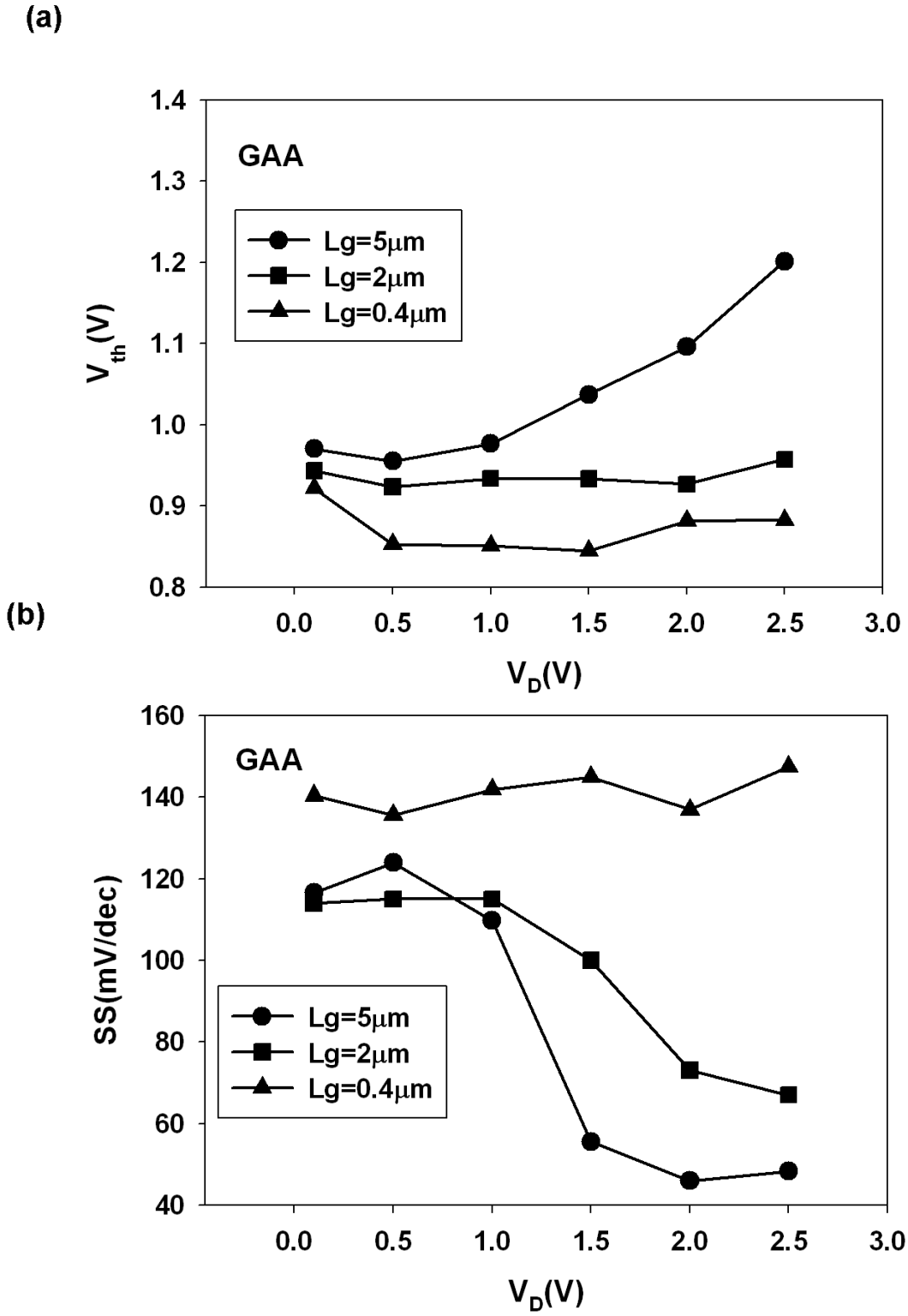

Fig. 7-9 (a) V_{th} and (b) SS of GAA poly-Si NW TFTs with L_g of 2 and 0.4 μm with various V_D, extracted from the transfer characteristics shown in Figs. 7-8 (a) and (b), respectively, to compare with those shown in the long channel (L_g = 5 μm) GAA poly-Si NW TFT.

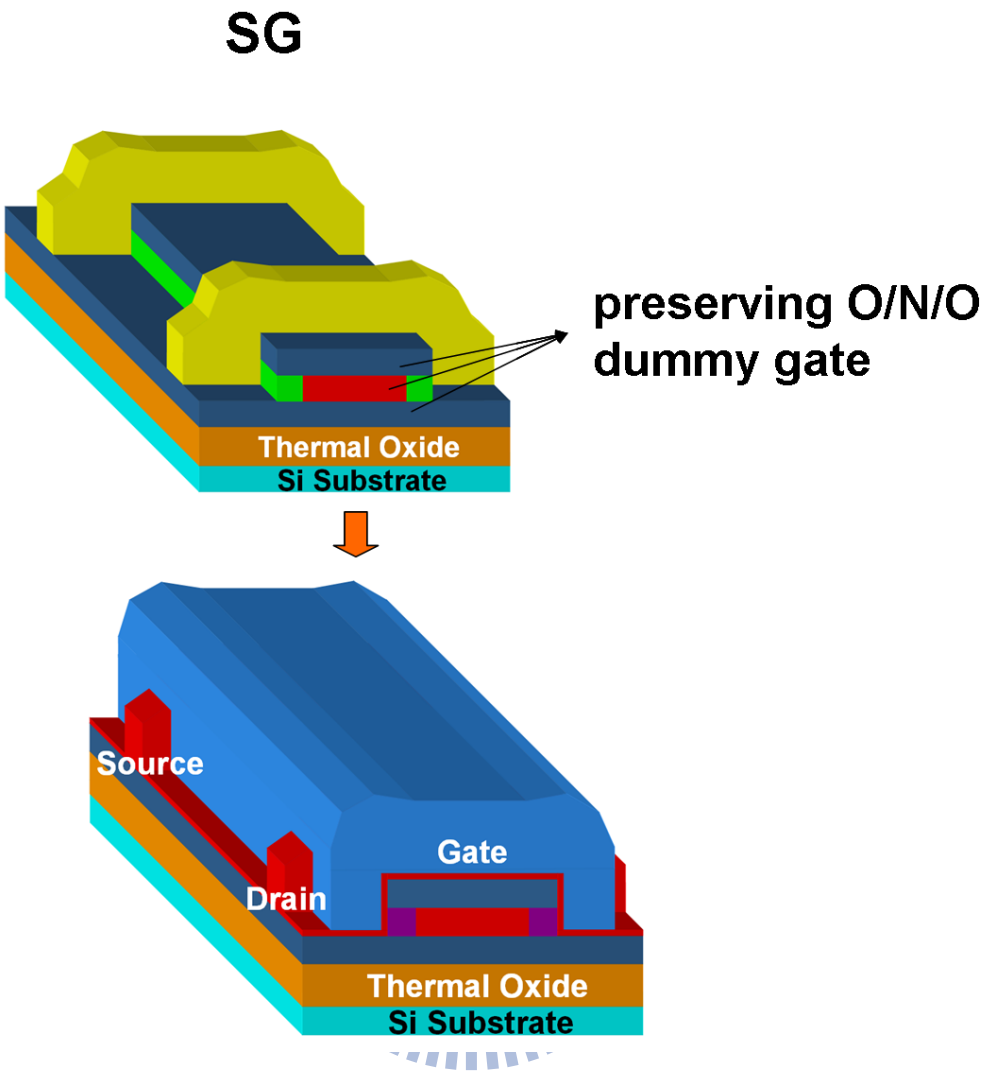

Fig. 7-10 Key steps and stereo structure of an SG poly-Si NW TFT.

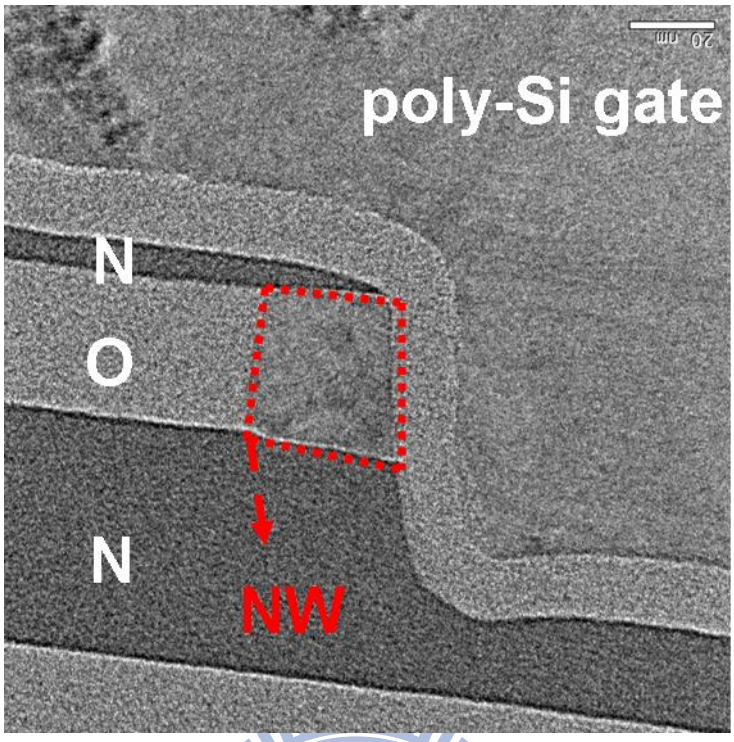

Fig. 7-11 Cross-sectional TEM image of an SG poly-Si NW TFT.

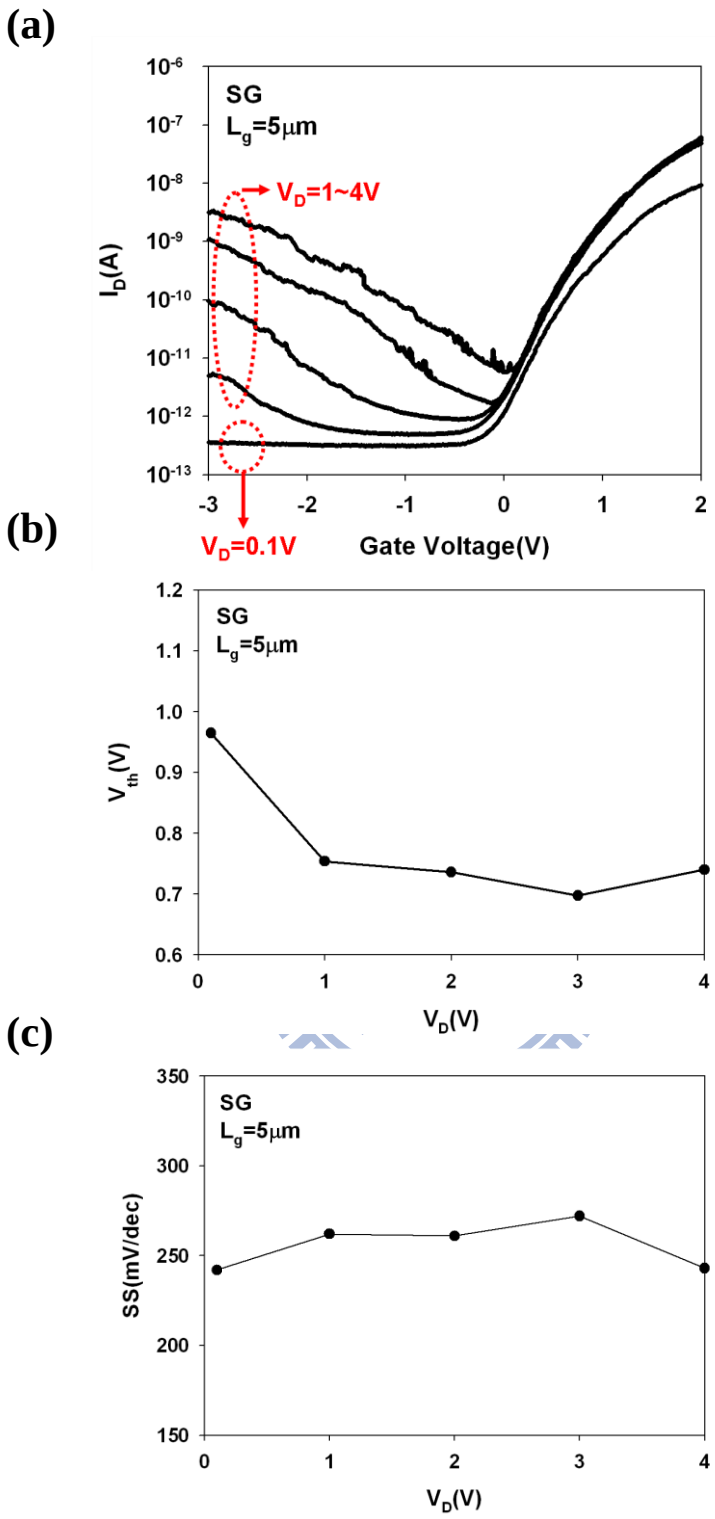

Fig. 7-12 (a) Transfer characteristics as well as (b) the extracted V_{th} and (c) SS of SG poly-Si NW TFT with L_g = 5 mm as a function of V_D.

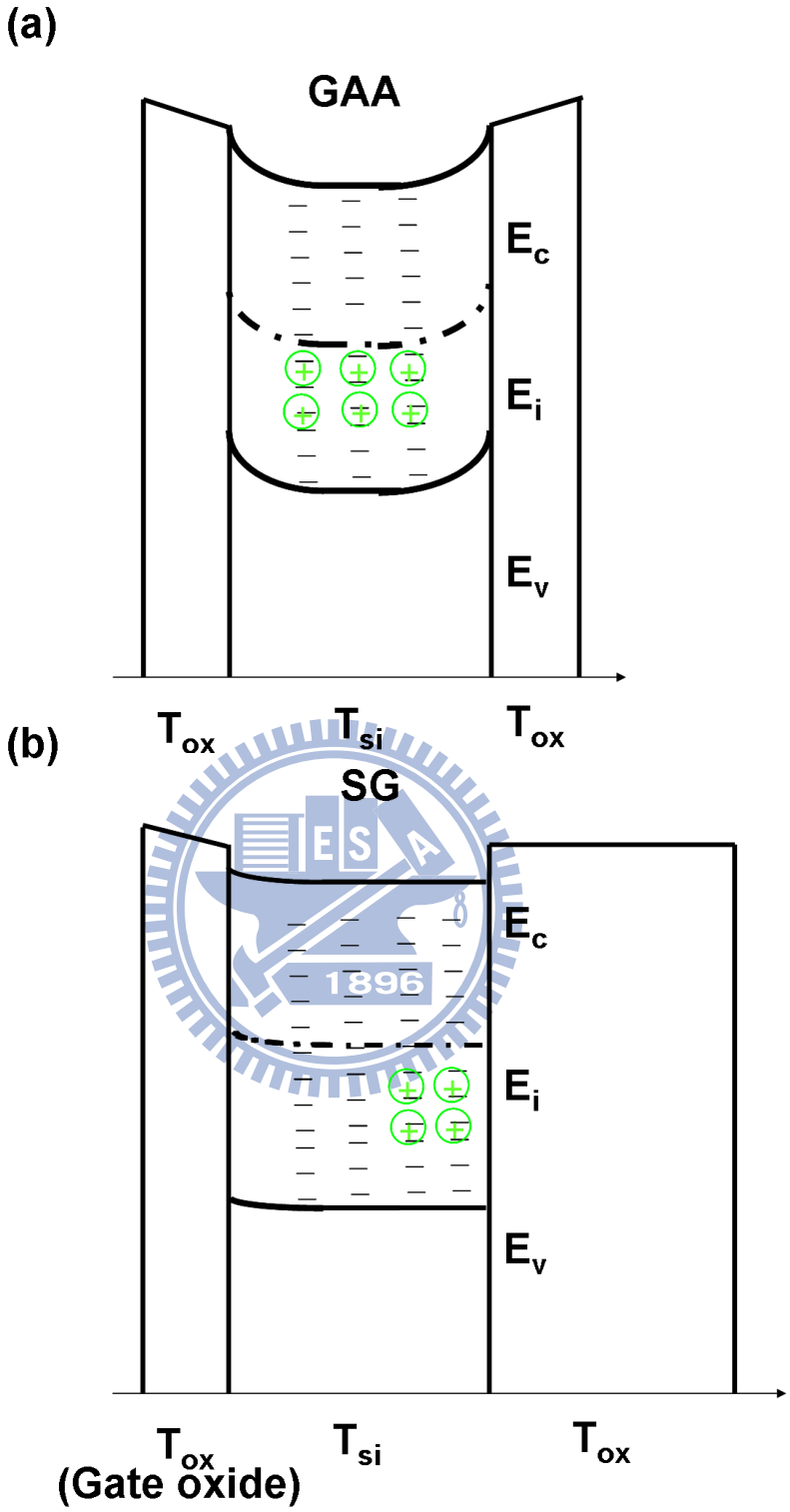

Fig. 7-13 Band diagrams of (a) GAA and (b) SG poly-Si NW transistors near the source side perpendicular to source-to-drain direction.

Chapter 8

Conclusions and Future Prospects

8.1 Conclusions

To sum up, as mentioned in Chapter 1, several approaches of manufacturing multi-gated (MG) poly-Si NW thin-film transistors (TFTs) have been proposed and demonstrated by our group. In this dissertation, we pay special attentions to two kinds of these approaches, *i.e.*, independent double-gated (IDG) and gated-all-around (GAA) configurations [8.1]~[8.2]. The IDG poly-Si NW TFT is adopted to explore the interesting performance enhancement under double-gated mode of operation as well as the feasibility in the application of IDG SONOS flash memory. The GAA configuration is employed to develop a novel methodology for probing the electrical characteristics of *in situ* phosphorous-doped poly-Si NW and investigation of the abnormal subthreshold characteristics at room temperature. We also develop an analytical model to describe the electrostatic characteristic of DG junctionless (J-less) transistors in subthreshold region. Moreover, we explore the device characteristics of asymmetric Schottky-barrier (SB)

transistors which feature SB only on the source side, while the channel and drain are both n^+ doped.

In Chapter 2, by the employment of IDG poly-NW TFTs, characteristics of poly-Si NW devices featuring IDG configuration are characterized and analyzed. Special attentions are paid to investigating the root cause of performance enhancement under DG mode of operation at a small drain voltage. It is attributed to the lower potential barriers provoked by the grain-boundary (GB) defects in a poly-Si channel as devices operated under DG mode of operation. This improves the injection efficiency of transport carriers though those potential barriers by thermionic emission. Consequently, a higher output current can be achieved.

In Chapter 3, the unique features of V_{th} window of IDG SONOS device under two different read modes are investigated. A derived model is clearly verified by the results of experimental measurements on fabricated IDG poly-Si NW SONOS TFTs. Based on the experimental and analytical analysis, several kinds of innovative SONOS NAND string with IDG configuration are proposed, featuring several merits, such as low thermal budget, low read disturb [8.3] and easier fabrication process. These approaches have potential to being applied to the future high-density 3D stackable non-volatile memory technology.

In Chapter 4, the approach of manufacturing GAA poly-Si NW TFTs is adopted to fabricate the J-less poly-Si NW transistors by replacing the original undoped poly-Si NW with an *in situ* phosphorous-doped poly-Si one as the conduction channel. Such a device features unique switching characteristics, which transfers from gated- to ungated-resistor as the gate voltage is sufficiently negative. Such a characteristic is utilized to develop a novel methodology capable of probing the basic electrical properties of *in situ* phosphorous-doped poly-Si NWs, such as active doping concentration and mobility. The experimental results indicate a lower active doping concentration than the SIMS value and unexpected large negative fixed charges presenting at the interface between gate oxide and poly-Si NW channel for the first time. The major reason is postulated to be related to the occurrence of phosphorous precipitation and segregation [8.4]~[8.5]. These results are also verified by the C-V measurements performed on the planar J-less transistors with the ultrathin *in situ* phosphorous-doped poly-Si film as the conduction channel.

In Chapter 5, an analytical model of V_{th} and subthreshold current for DG J-less transistors is proposed. Such a model provides good description of V_{th} roll-off and SS even with scaled gate length as short as 22 nm, if the thickness of conduction channel film is thin enough, say 8~10 nm. Therefore, it can offer deeper insights to optimize the device performance.

In Chapter 6, we combine the unique features of J-less transistor and Schottky-barrier (SB) transistors and propose an innovative asymmetric SB transistor (ASSBT) with silicided source as well as heavily doped channel and drain. Such a device features high on/off current ratio and unipolar characteristics. Considering the additional impacts of the silicon depletion region between gate oxide and quasi neutral region, a modified empirical form is proposed to describe the effects of channel thickness and gate oxide thickness to the subthreshold swing (SS) in pseudo-subthreshold region of this new ASSBT. The analytical data indicate that such a modified empirical form is also suitable for devices featuring DG configuration if half of the channel thickness is applied to the analytical expression of the scaling length (λ). Finally, we propose a novel inverter built by two dual-workfunction (DW) DG N- and P-type ASSBTs. Such an inverter features a simplified fabrication process as compared with the architecture proposed in a previous work [6.6] owing to the employment of a common back-gate. In addition, the merit of denser pattern attributed to the elimination of isolation revealed in the previous work is also preserved.

In Chapter 7, we report the particular phenomena associated with the abnormal dependence of SS and threshold voltage on the applied drain voltage and/or starting point of gate voltage in GAA poly-Si NW TFTs at room temperature for the first time. A qualitative model considering the numerous holes generated by high off-state current

and then trapped by the defects in poly-Si NW channel is proposed to explain the observations. The impacts from channel length and gate configuration are also explored.

8.2 Future Prospects

Notwithstanding the fact that several topics related to conventional IM and J-less IDG or GAA NW transistors have been studied in this dissertation, there are still a couple of aspects that need to be investigated aiming at further improvement of device performance and optimization for practical applications.

8-2.1 Three-Dimensional Integration of J-less Poly-Si NWTFTs and NVMs

As mentioned in Chapter 4, the proposed GAA J-less poly-Si TFTs with *in situ* phosphorous-doped poly-Si NW possess the merit of low temperature fabrication process. In addition, the complexity of process could be greatly simplified in such a device because of the skip of the implanted S/D, which is replaced by a heavily *in situ* phosphorous-doped poly-Si one formed simultaneously with the poly-Si NW channel. Such particularity makes it very attractive for the 3-D electronics integration or 3-D non-volatile memory (NVM), such as BiCS [8.7]~[8.8]. For NVM applications, it is also expected that the issue associated with read disturb can be relieved by the

employment of the IDG configuration [8.3]. Hence, it is interesting to combine the merits of the proposed J-less transistors and IDG configuration to develop an implantation-free J-less IDG NVM device. Moreover, for the purpose of achieving system-on-chip (SOC) or system-on-panel (SOP) [8.9], the topic of integrating the proposed implantation-free J-less NVMs and logic devices onto the same chip is also worth studying.

8-2.2 Metal-Oxide-Metal Field Effect Transistors (MOMFETs)

As mentioned in Sec. 1-3, although the employment of J-less transistors can relieve the difficulty in forming ultra-shallow S/D junctions and improve the output driving current, the output current is still degraded as carriers transport through the doped S/D to metallic silicide contacts. In this regard, further improvement can be expected if the heavily doped channel is replaced by a metallic silicide one.

Consequently, the original metal-oxide-semiconductor field-effect transistor (MOSFET) becomes a metal-oxide-metal field-effect transistor (MOMFET) owing to the fact that the semiconductor channel is replaced by a metallic one. However, one of the most serious issues is that a much thinner conduction channel than that adopted in J-less transistors for efficiently turning-off the metallic channel owing to the much higher carrier concentrations in the metallic silicide channel film, such as NiSi ($9 \times$

10^{22} cm^{-3}) [8.10] or $CoSi_2$(1×10^{21} cm^{-3}) [8.11]. On the other hand, the difficulty in controlling the phase of silicide channel film leads to the confusion of the type of conducting majority carriers. For example, both NiSi and CoSi are with n-type majority carriers [8.10]~[8.11]; however, those in $NiSi_2$ and $CoSi_2$ are both p-type [8.10]~[8.11].

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博士論文：新穎反轉式及無接面多閘極多晶矽奈米線薄膜電晶體特性與應用的探討

An Investigation on the Characteristics and Applications of Novel Multiple-Gated Inversion-Mode and Junctionless Polycrystalline Silicon Nanowire Thin-Film Transistors

Publication List

A. Journal Papers

1. H. C. Lin, C. H. Hung, W. C. Chen, **Z. M. Lin**, H. H. Hsu, and T. Y. Huang, "Origin of hysteresis in current-voltage characteristics of polycrystalline silicon thin-film transistors," *J. Appl. Phys*., vol. 105, no. 5, pp. 054502-1–054502-6, Mar. 2009.

2. W. C. Chen, H. C. Lin, **Z. M. Lin**, C. T. Hsu, and T. Y. Huang, "A study on low temperature transport properties of independent double-gated poly-Si nanowire transistors," *Nanotechnology*, vol. 21, no. 43, pp. 435201-1– 435201-7, Oct. 2010.

3. H. C. Lin, **Z. M. Lin**, W. C. Chen, and T. Y. Huang, "Read characteristics of independent double-gate poly-Si nanowire SONOS devices," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3771-3777, 2010.

4. **Z. M. Lin**, H. C. Lin, K. M. Liu, and T. Y. Huang, "Analytical model of subthreshold current and threshold voltage for fully depleted double-gated junctionless transistor," Jpn. J. Appl. Phys., vol. 51, p. 02BC14, 2012..

5. **Z. M. Lin**, H. C. Lin, and T. Y. Huang, "Characteristics of n-type asymmetric Schottky-barrier transistors (ASSBTs) with silicided Schottky-barrier source and heavily n-type doped channel and drain," submitted to *Japanese Journal of Applied Physics*.

B. Letter Papers

1. **Z. M. Lin**, H. C. Lin, W. C. Chen, and T. Y. Huang, "Insight into the performance enhancement of double-gated polycrystalline silicon thin-film transistors with ultrathin channel," *Appl. Phys. Lett*., vol. 96, no. 7, pp. 072108-072108-3, 2010.

2. C. J. Su, T. I. Tsai, Y. L. Liou, **Z. M. Lin**, H. C. Lin and T. S. Chao, "Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels" *IEEE Electron Device Lett*., vol. 32, no. 4, pp. 521-523, 2011.

C. Conference Papers

1. **Z. M. Lin**, H. C. Lin, and T. Y. Huang, "Simulation analysis of a double-gated

asymmetry Schottky-barrier transistor with heavily doped channel" *Int'l Electron Devices and Materials Symp*., Chungli, Taiwan, 2010.

2. **Z. M. Lin**, W. C. Chen, H. C. Lin, and T. Y. Huang, "A study on abrupt switching phenomena of independent double-gated poly-Si nanowire transistors under cryogenic operation," in *proceeding of International Symposium on VLSI Technology, Systems, and Applications*, pp. 38-39, Hsinchu, Taiwan, 2011.

3. **Z. M. Lin**, T. I. Tsai, T. Y. Huang, and H. C. Lin, "Fabrication and characterization of gate-all-around polycrystalline silicon nanowire thin-film transistors with sub-60 mV/decade subthreshold swing," *Int'l Electron Devices and Materials Symp*., Taipei, Taiwan, 2011.

4. **Z. M. Lin**, T. I. Tsai, T. Y. Huang, and H. C. Lin, "Fabrication and characterization of gate-all-around polycrystalline silicon nanowire thin-film transistors with sub-60 mV/decade subthreshold swing," *Int'l Electron Devices and Materials Symp*. Taipei, Taiwan, 2011.

   (Best Student Paper Award)

5. **Z. M. Lin**, H. C. Lin, K. M. Liu, and T. Y. Huang, "Modeling subthreshold current and threshold voltage of fully-depleted double-gate junctionless(J-less) Transistors," in *proceeding of International Conference on Solid State Devices and Materials*, pp. 100-101, Nagoya, Japan, 2011.

D. Patents

1. H. C. Lin, **Z. M. Lin**, "非揮發性記憶體陣列結構(Non-volatile memory cell array)," Taiwan and USA patents, pending.