國立交通大學

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博士論文

以噴射式大氣電漿在低溫下開發高品質二氧化矽應用在低電壓操作之有機薄膜電晶體之研究

High-Quality Silicon Dioxide Developed by Atmospheric Pressure Plasma Jet at Low Temperature for Low-Voltage OTFT Application

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指導教授：張國明 教授

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中文摘要

有機薄膜電晶體對許多研究者有很高的吸引力主要來自於它可以應用在可撓式顯示器以及可撓式電子。可撓式顯示器可以用在電子紙，這可以減少樹木的砍伐，而可撓式電子方面可以應用在人工皮膚、軟性感測器、RF-ID，雖然有機薄膜電晶體已經發展很長一段時間，但是在有機薄膜電晶體的發展上仍然存在一些問題，主要包含低的電子遷移率、不穩定性、低溫且低成本的製程、高操作電壓。在本論文中，由於塑膠基板不能承受高溫製程，低溫製程的開發變得越來越重要，就我們所知要得到高品質絕緣層通常需要高溫處理，因此開發低溫高品質的絕緣層將是非常困難的，製作絕緣層方法包含 PECVD、PVD 和溶液製程，PECVD 和 PVD 雖然廣泛被研究，但是都需要真空設備這將不利於大面積製作以及低成本的應用。溶液製程雖然符合低成本需求，但是容易在薄膜中形成孔洞而且為了去除薄膜裡的溶劑需要長時間的烘烤。

目前大多數的 OTFTs 都操作在高電壓約 -20 V~-40 V，這將會造成較高的功率損耗且不利於應用在攜帶式電子產品。所以如何降低操作電壓是非常之重要的，目前通常利用高介電係數材料以及較薄的絕緣層來當作閘極介電層，這可以增加單位面積的電容值去減少操作電

壓。

剛開始為了開發低溫且低成本製程，我們致力於利用大氣電漿技術去開發高品質二氧化矽薄膜當做有機薄膜電晶體絕緣層。因為大氣電漿可以操作在低溫下且適合大面積低成本製程的應用。在第二章我們分析溫度、流量、噴嘴距離、主要氣體對薄膜品質的影響。如我們期待的，我們利用大氣電漿在基板溫度約為 150 ^{O}C 下成功開發出高品質的二氧化矽薄膜，漏電流密度約為 2.53E-8 A/cm^2 在 0.5 MV/cm，目前大多數研究所發表的絕緣層漏電流密度約為 1E-8~5E-6 A/cm^2 at 0.5 MV/cm 且大多數不符合低溫低成本的製程，在第三章，為了減小操作電壓我們絕緣層厚度控制在約 10 nm 來增加絕緣層單位面積的電容值，我們成功的將所開發出來的高品質二氧化矽整合到低電壓操作的元件上，有機薄膜電晶體操作電壓小於 -2 V、截止電壓約為 -0.8 V、電子遷移率約為 0.66 cm^2/V-s、次臨界電壓約為 700 mV/decade，大多數研究者所發表出來的操作電壓通常大於 -20 V，我們在絕緣層品與元件特性有顯著的改善。

在我們成功沉積高品質絕緣層後，對二氧化矽做表面處理將有助於改善主動層的分子排列，這有助於電子遷移率的提升，但我們發現在做完表面處理後漏電流卻增加了，而這現象並沒有被討論過，且我們認識為這將會限制未來短通道有機薄膜電晶體的發展，為了瞭解這現象我們利用 top-contact 結構去討論表面處理對漏電流的影響在第四章。

High-Quality Silicon Dioxide Developed by Atmospheric Pressure Plasma Jet at Low Temperature for Low-Voltage OTFT

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Abstract

Organic thin film transistors (OTFTs) have lots of attraction for many researches because of their interesting and innovative applications on flexible display and flexible electronics. Flexible display could be used as an e-book which could reduce the use of woods. On the other hand, flexible electronics would be applied for artificial skin, flexible sensors, and RF-ID. Although OTFTs have been studied for a long time, there are still some issues influencing the development of OTFTs. These issues of OTFTs include low mobility, instability, low cost and temperature processes, and high operation voltage.

In this dissertation, we aim to develop low cost ant temperature processes of gate insulator and low-voltage OTFTs. Because the plastic substrate could not sustain high temperature processes, the development of low-temperature processed OTFTs is more and more important. As we known, to

gain good film quality with a low leakage current, a high-temperature insulator activation is required. Therefore, it is very difficult to develop low temperature processes for high-quality gate insulator. Fabricating approaches of gate insulator include PECVD, PVD, and solution processes. PECVD and PVD are widely used to deposit insulator but they need a vacuum system and higher cost which are not suitable for large area application of flexible display. Although solution processes could decrease the cost, this method easily forms the pin-hole and needs a long-time baking for solvent-free.

In most researches, OTFTs operated at high voltage about -20 V ~ -60 V which would lead to high power consumption. Because the high power consumption is not suitable for portable electronics, how to reduce the operation voltage of OTFTs would be urgent for flexible display and flexible electronics. Therefore, many researches utilized high-k material or thin insulator as gate dielectric, increasing capacitance of per unit area dielectric, to reduce the operation voltage.

In the beginning, we aim at the development of low cost and temperature processes. We are devoted to use atmospheric pressure plasma jet (APPJ) for depositing high quality silicon dioxide (SiO_2) as the gate insulator of OTFTs. Because APPJ could be operated at low temperature and atmospheric pressure, it is suitable for large area and low cost application. In chapter 2, we analyzed the influence of substrate temperature, flow rate, gap distance, and main gas on the quality of SiO_2. As we expected, a low leakage current density of 2.53 E-8 A/cm^2 at 0.5 MV /cm for SiO_2 deposited by APPJ at low temperature about 150 ^{O}C was demonstrated here. The leakage current density of most researches are between 1E-8~5E-6 A/cm^2 at 0.5 MV /cm and most of them are not suitable for low cost and temperature processes.

In order to reduce operation voltage of OTFTs, the thickness of SiO_2 was controlled about 10 nm to increase the capacitance of per unit area dielectric. Low-voltage OTFTs were successfully integrated with APPJ-SiO_2 which was described in chapter 3. These OTFTs showed a lower operation voltage about -2 V, a lower threshold voltage about -0.8 V, a good mobility 0.66 cm^2/V-s,

and a good subthreshold swing about 700 mV/decade. We got obviously improvement on the performance of gate insulator and OTFTs by using APPJ.

After we successfully deposited high quality silicon oxide, surface treatment on the silicon oxide could be used to improve ordering of active layer which would increase mobility of OTFTs. However, we found that the leakage current would increase with a surface treatment. We consider this phenomenon would limit the development of short channel OTFTs. In order to understand the phenomenon, we utilized top-contact structure to discuss the influence of the surface treatment on leakage current in chapter 4.

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Contents

Table Caption

Figure Caption

Chapter 1 Introduction

1.1 History & Application of OTFTs

Semiconductors have been widely used in various electronic devices. In addition, the invention of semiconductor transistor took replacement of traditional vacuum tube based electronics. Silicon is the dominate material in the use of high performance electronic chip from the end of 20th century and lead to the omnipresence of semiconductor microelectronics in our daily life. Organic semiconductor materials have been widely studied for the expectation of new applications, such as flexible light sources [1-5], flexible display [6-11], flexible electronics [12-14], and plastic solar cells [15-17]. In recent years, Flat panel displays (FPD) are growing quickly because flat panel displays are lighter, much thinner, and less power than traditional cathode ray tube (CRT). The development of flat panel display has made great progress in resolution, brightness, contrast ratio, viewing angle, response time, weight and so on. FPD are widely used in mobile phone, notebook, camera, and television and become more and more important for our life. Flexible displays are considered as the revolutionary product because it could be applied for e-paper, e-book, and large area screen which would decrease the use of woods, keep environment, and make our life colorful. Therefore, many national companies focus their investigation and development on the flexible display such as PVI, AUO, Fujitsu, Samsung Electronics, Sony, LG, and so forth. Figure 1-1 showed the pictures of the flexible display announced by LG. Recently, Sony Corporation announced that they developed a super-flexible 80 μm-thick, 4.1-in, 121 ppi, and OTFT-driven full color OLED display which can be wrapped around a thin cylinde at SID (Society for Information Display) 2010 International Symposium on May 27. Flexible display announced by Sony

Corporation was shown in Figure 1-2.

Organic thin film transistors (OTFTs) play an important role of flexible display and have been widely studied by many researchers. Pixel of active matrix organic light-emitting displays (AM-OLED) was shown in Figure 1-3. OTFTs could be used to charge the capacitor and drive the OLED in the pixel of AM-OLED and as a key component. In addition, OTFTs were also applied for flexible electronics, including ratio frequency identification smart card (RFID) and sensors such as pressure sensor, gas sensor, bio-sensor, and electronic artificial skin [18-23], shown in the Figure 1-4.

In the following sections, we would introduce the operation theory, fabrication methods, and major issues of OTFTs. Also, atmospheric pressure plasma jet (APPJ) with many advantages, applied for OTFTs fabrication would be introduced in the following sections, simultaneously.

1-1 Operation Theory of OTFTs

The structures of OTFTs mainly included two types of top contact (TC) and bottom contact (BC) [24-27], respectively, shown in Figure 1-5 (a) and (b). The structures of OTFTs have several variants. In general, an OTFT is composed of four parts – a metal electrode, an insulator, a thin channel layer, and the sourc/drain metal contacts. Each of these structures has its advantages and drawbacks. In the BC structure, source-drain electrodes deposited on insulator could be patterned by lithographic technology to get higher device density. However, source-drain electrodes could not be defined by lithographic technology in TC structure. This is because the organic semiconductor materials are much easier influenced by oxygen, water, organic solvent [28-29], and so on. Therefore, most TC structures need to pattern the source-drain electrodes by shadow mask but then decrease the densities of OTFT devices. In addition, TC

structures with lower contact resistance than BC structure could increase the mobility of OTFTs due to its channel material with better molecule ordering and larger grain size.

Transfer characteristics (I_D-VG) and output characteristics (I_D-V_D) of OTFTs are shown in the Figure 1-6 (a) and (b). These curves were measured on the pentacene-based OTFTs made with gold source and drain electrodes. The chemical structure of pentacene was also inserted in Figure 1-6 (a). Figure 1-7 shows the energy scheme which indicates the respective positions of the Fermi level of gold and the frontier orbitals (highest occupied molecular orbital, HOMO, and lowest unoccupied molecular orbital, LUMO) of pentacene. The LUMO level of pentacene is quite far away from the Fermi level of gold, so there is a substantial energy barrier for electrons. Therefore, electron injection is very difficult when a positive voltage is applied to the gate and source is connected with ground. In contrast, holes can be injected to the semiconductor from the source by applying a reverse gate voltage, since the Fermi level of gold is close to the HOMO level of pentacene. With increasing reverse gate voltage, the hole conductive channel forms at the interface between insulator and semiconductor. The hole charge could be driven from source to drain by applying negative voltage to the drain. It is a reason that pentacene is call as a p-type semiconductor. However, this concept is obviously different to the common p-type or n-type materials doped by implanting. In another words, when the source and drain electrodes can inject electrons into its LUMO level, an organic semiconductor will be a n-type material.

Generally, the gate voltage of OTFTs could induce the equal charges at both sides of gate insulator. These injected charge carriers increase as applying a reverse gate voltage and then generate a conductive channel with high conductance.. At low drain voltage, the current almost follows Ohm's law especially using high work function

source-drain metal material. Therefore, OTFTs are mainly controlled by gate and drain voltages. As the drain current approaches to the gate voltage, the channel gradually becomes pinch off. Then, the channel current becomes independent to drain bias which is called saturation region. The mobility of OTFTs was extracted in saturation region from the following equation:

$$I_{DS} = \left(\frac{WCi}{2L}\right)\mu(V_G - V_T)^2 \qquad [1]$$

Where W and L are the channel width and length, C_i is the insulator capacitance per unit area, V_G and V_D are the gate and drain voltage, and V_T is the threshold voltage that takes into account various potential drops through the gate-insulator-semiconductor structure. In the saturation region, μ can be calculated from the slope of the plot of $|I_D|^{1/2}$ versus V_G.

1-2 Major Issues for OTFT Development

Organic thin film transistor are expected to be applied for flexible display. In recent years, although the performance of OTFTs have great improvement, there are still some issues influencing the development of OTFTs. These issues of OTFTs mainly include low mobility, stability, and high operation voltage.

The mobility of organic thin film transistors is only about 0.001~10 cm^2/V-s, much lower than silicon-base MOSFET and polysilicon TFT. The mobility of OTFTs is dominated by organic material and ordering of organic material [30-32]. On the other hand, stability of organic semiconductor material is a serious problem. Electrical characteristics of OTFTs would be degraded by oxygen, moisture, and organic solvent

and so on [28, 29]. Some researchers believed that oxygen would diffuse into active layer and formed impurities in the organic semiconductor layer but these studies resulting from environment influence are not very clear. These environment factors may lead to the degradations of on current, threshold voltage shift, and subthreshold swing. It is well known that lithography processes such as organic solvent, photoresistor, water, exposure, and baking may degrade the performance of OTFTs. Therefore, there are many researchers focus on fabrication of capping layer [33, 34] and some of studies endeavor to overcome the issue of active layer tied to lithography processes[35, 37], which are important for the improvement on device performance and circuit density.

However, another pending problem of OTFTs is high operation voltage [38-41]. The high operation voltage would result in high active power consumption, not suitable for the low-power protable electronics. Active power consumption is on current multiplied by operation voltage. However, we could not decrease the on current because higher on current could increase operation speed to overcome RC time delay. Therefore, decreasing operation voltage is urgent for OTFTs. In order to keep the magnitude of on current and decrease operation voltage, increasing the capacitance per unit area is the one of the ways to obtain the goal. Capacitance is positive proportional to dielectric constant and negative proportional to thickness of insulator. Therefore, many studies used high-k material or thinner insulator as the gate insulator to decrease the operational voltage [11-16]. Gate insulator materials mainly consist of polymer, metal oxide, and nanocomposite. Polymer is suitable for low cost processes such as spin, inject, and print. However, the drawbacks of polymer include lower dielectric constant, longer baking time, and more holes pin-holes. Metal oxide materials usually have high dielectric constant such as HfO_2, Ta_2O_5, TiO_2, Al_2O_3, AlN, Si_3N_4 [42-45] and so on but these material often fabricated by CVD or PVD which is

high cost and low throughput processes for flexible electronics. Metal oxide material usually need a high temperature anneal to improve quality which is not suitable for plastic substrate. Plastic substrate usually could not sustain over 200 ^{o}C and the upper processing temperature of different kinds flexible substrate are shown in Figure 1-8.

1-4 Overview of Dissertation

Organic thin film transistors attracted many researchers and company to investigate and develop due to their future applications. Some main issues including low mobility, stability, and high operation voltage had been described above. In our work, we focus on developing and investigating low temperature and low cost processes to fabricate high quality silicon oxide as a gate insulator for OTFTs. Silicon dioxide is a kind of very cheap and rich resource in the world and used as main gate insulator for MOSFET. Band gap of silicon dioxide is about 9 eV which is good to be used as a gate insulator. In addition, good stability and reliability of silicon oxide were also proposed in many researches. The highest process temperature of OTFTs usually happened in gate insulator. So decreasing the processes temperature of gate insulator is very important for OTFTs due to the plastic substrate could not sustain high temperature. For the purpose of low cost and high throughput processes, atmospheric pressure plasma jet (APPJ) was utilized in this thesis. We controlled our processes temperature from room temperature to 200 ^{o}C. There are lot of advantages of APPJ such as low temperature, low cost, and high throughput.

Figure 1-9 shows the basic structure of atmospheric pressure plasma jet. Because APPJ could be operated in atmospheric pressure it is suitable for large area application which is very important for cost down.. Good quality of silicon oxide deposited by APPJ had been developed by us and leakage current density was

suppressed below 1~2E-8 A/cm^2 at 0.5 MV/cm in MIM structure. We controlled temperature, flow rate, gap distance, and main gas to improve the performance of silicon oxide which were all described in chapter 2. In addition, silicon oxide deposited with APPJ was successfully applied for the gate insulator of OTFTs. The thickness of our demonstrated silicon oxide is only 9 nm so the operation voltage of OTFTs was about -2 V. Threshold voltage is about 0.8 V, mobility is about 0.66 cm^2/V-s, and subthreshold swing is about 0.6 V/decade in our proposed OTFTs. The detail fabrication and discussion of OTFTs were described in chapter 3. We found that higher molecular ordering of organic semiconductor would influence the leakage current of OTFTs. Many studies used surface treatment to improve the molecular ordering of channel layer and increase the mobility of OTFTs. However, leakage current of OTFTs was also increased after improving molecular ordering and this drawback was ignored. We used to contact structure of OTFTs to investigate and discuss this problem in this chapter 4.

Figure 1-1 Flexible displays announced by LG.

Figure 1-2 Photo of OTFT-driven OLED display wrapped around a cylinder with 4 mm radius. (Sony Corp.)

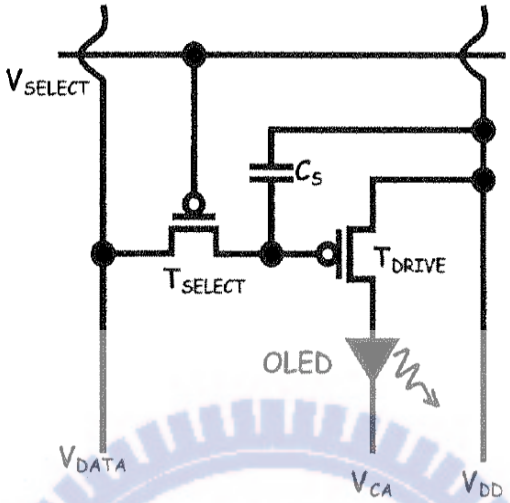

Figure 1-3 2T-1C OTFT driven OLED pixel design

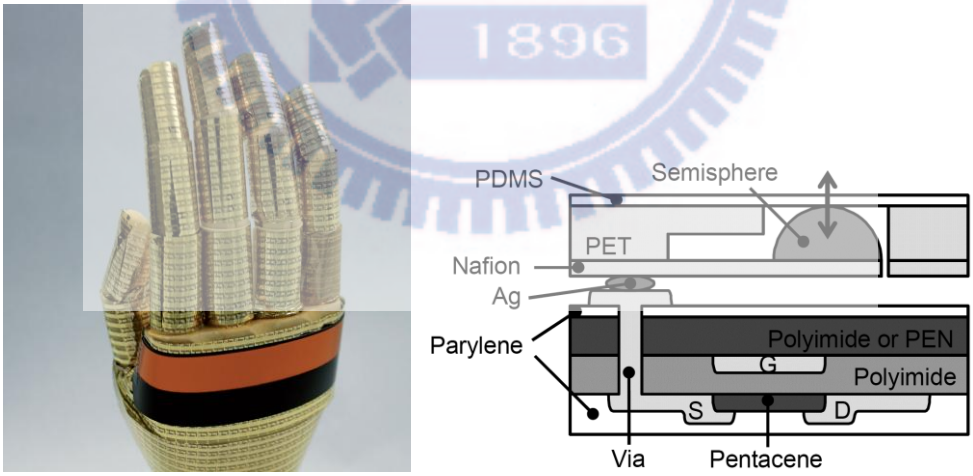

Figure 1-4 Electronic artificial skin integrated pressure and temperature sensors. Made by Prof. Takao Someya, University of Tokyo in Ref. [22].

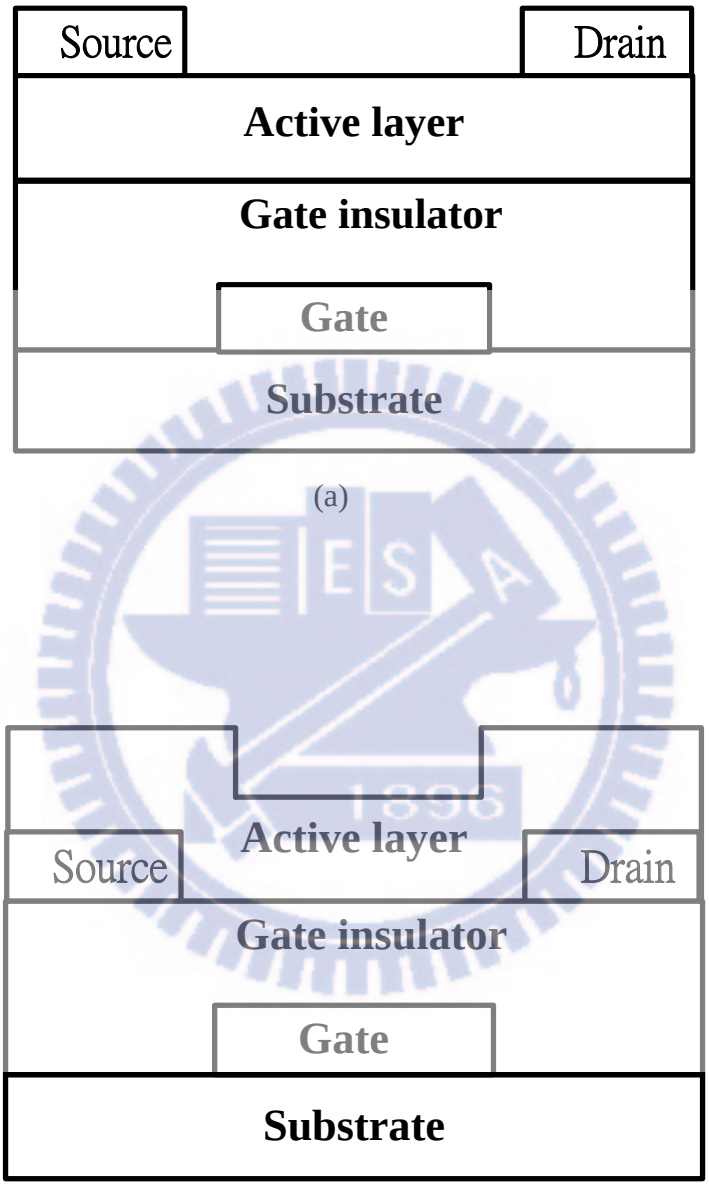

Figure 1-5 Top contact structure (a) and Bottom structure (b) of OTFTs

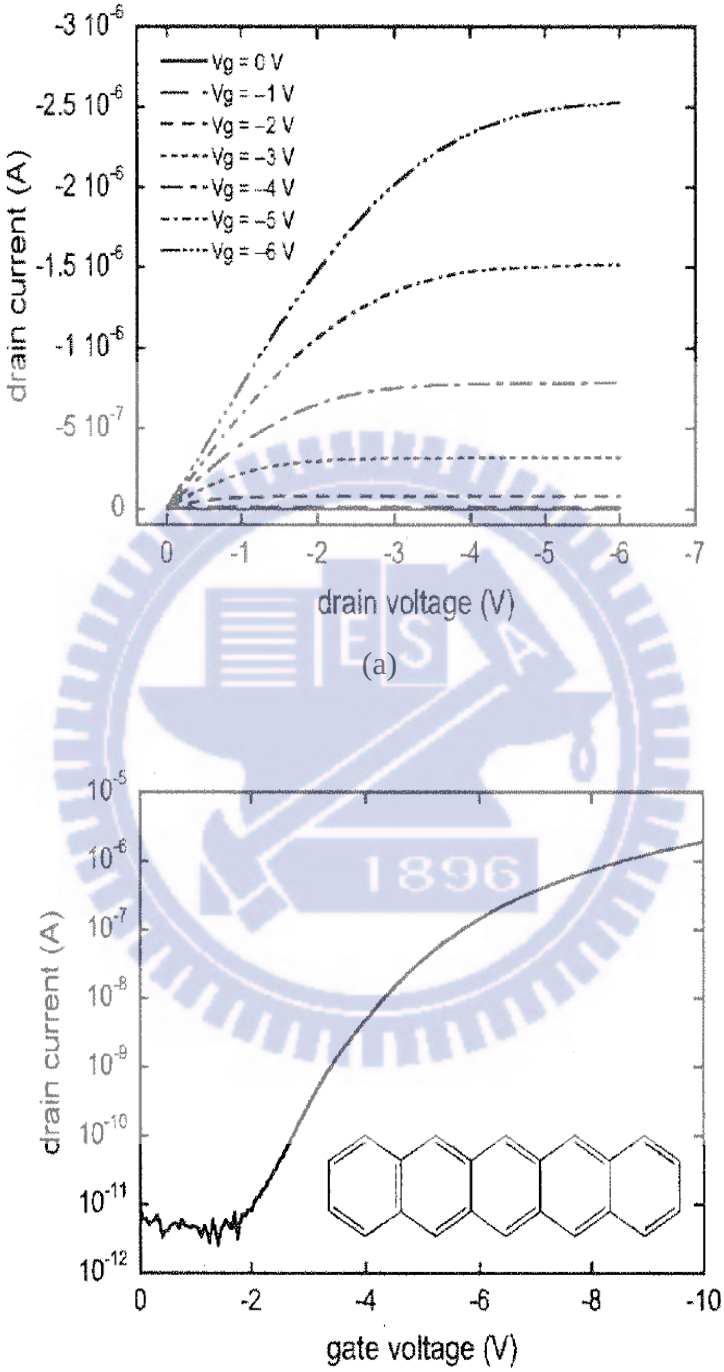

Figure 1-6 Output (a) and transfer (b) characteristics of a typical OTFT. The inset shows the molecular structure of pentacene, which serves as semiconductor in the device.

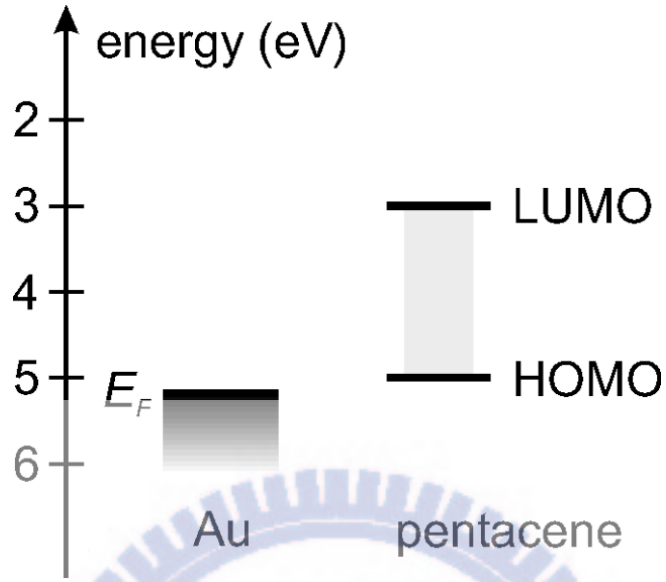

Figure 1-7 Schematic band diagram of gold and the energy of the frontier orbitals of pentacene. Data taken from Ref. 22.

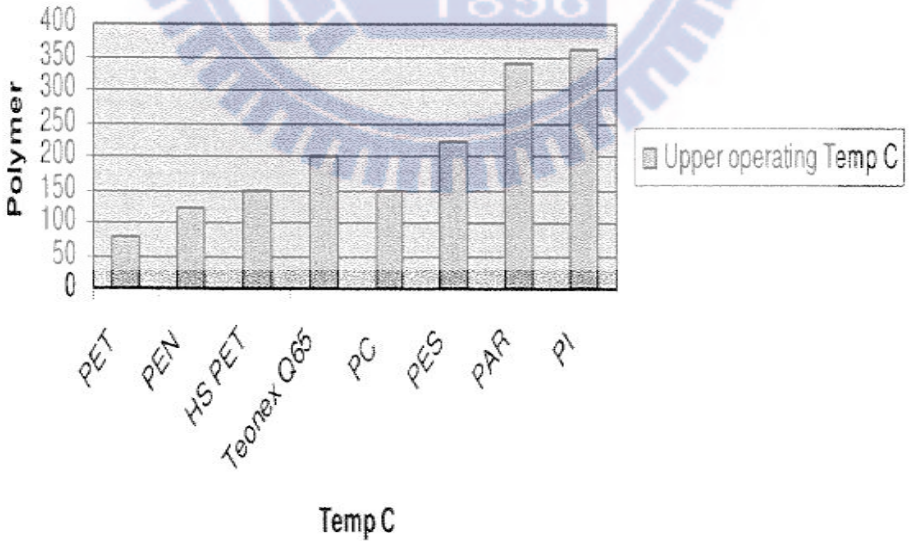

Figure 1-8 Upper processing temperature of flexible substrate.

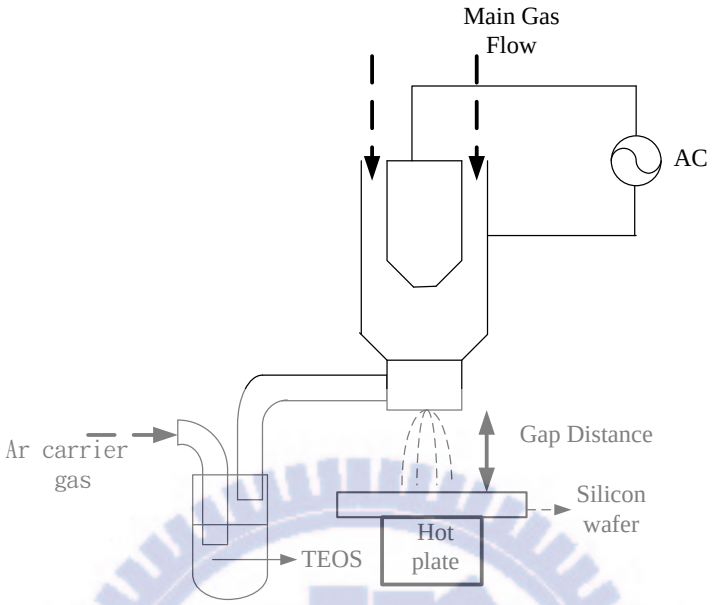

Figure 1-9 Schematic of the atmospheric-pressure plasma jet for the deposition of silicon oxide.

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Chapter 2

Factors for SiO2 Deposition by Atmospheric Pressure Plasma Jet

In this chapter, we aim at depositing high quality silicon oxide at low temperature by atmospheric pressure plasma jet (APPJ). First, we discussed the temperature influence on deposition of silicon oxide and defined the deposition temperature of silicon oxide. Second, because carrier gas's flow rate may influence the deposition rate and the quality of silicon oxide, we discuss the flow rate of carrier gas in section 2-2. We also found that the gap distance between nozzle and sample surface and main gas would influence the deposition rate and quality of silicon oxide, discussed in section 2-3 and 2-4, respectively. Leakage current density of silicon oxide was used to determine the quality of silicon oxide in these discussion. To improve surface morphology was also a problem for SiO_2 layer processed by APPJ. These pellets leading to large surface roughness would influence the characteristics of OTFTs. Fortunately, the pellets and surface roughness can be modified by controlling temperature, carrier gas's flow rate, gap distance, and main gas, discussed in following sections.

2.1 Effect of Growth Rate Influenced by Substrate Temperature on Different Substrate Materials

2.1.1 Introduction

Organic thin film transistors were usually to be fabricated on plastic substrate for

flexible electronics application. Because the plastic substrate can not sustain high temperature processes, the development of low-temperature processed OTFTs are more and more important. As we known, to gain good film quality with a low leakage current, a high-temperature insulator activation is required. Therefore, it is very important to investigate low temperature processes for high-quality gate insulator. In this study, we are devoted to use atmospheric pressure plasma jet for depositing gate insulator material because APPJ could be operated at atmospheric pressure and lower temperature, which was suitable for large area and low cost application [1,2]. Also, APPJ has been used for surface treatments on many kinds of applications [3-5]. In order to deposit high quality silicon oxide, we tuned parameters to optimize the conditions for film deposition. The film quality and deposition rate could be influenced by substrate temperature, proposed by many studies. In this section, we will investigate the effect of substrate temperature during process and find out the best condition for TFT device fabrication. As we expected, a low leakage current density of 1E-7 A/cm^2 at 0.5 MV /cm for silicon oxide deposited by low-temperature APPJ was demonstrated here.

2.1.2 Experiment

2-1-2-1 Silicon oxide MOS capacitors by APPJ

To simplify the process flow, the organic thin film transistors would be fabricated on silicon as a bottom substrate for basic electrical test [7-8]. The common metal insulator semiconductor (MIS) structure was utilized for the analysis of film quality deposited by APPJ and E-gun. First, a p-type silicon wafer used as the substrate was cleaned by RCA process to remove native oxide, particles, and contamination. Sequentially, the TEOS was introduced by a carrier gas of argon to deposit silicon

oxide in a atmospheric pressure plasma jet (APPJ) system. The plasma power was set around 560 W with an appropriate scanning rate to deposit silicon oxide under a room-temperature and atmospheric-pressure environment. We can control the thickness of silicon oxide by tuning the scanning times. Finally, a 500 nm thick aluminum metal was deposited by thermal coater as the top contact electrode. The top electrode was defined by a shadow mask with an area of 250μm x 250μm.

2-1-2-2 Silicon oxide MIM capacitors by APPJ systems

Metal insulator metal (MIM) structure was adopted in this experiment shown in Figure 2-1-1. First, the 500 nm thermal oxide was grown on the p-type silicon substrate for isolation and followed by the 300 nm aluminum layer as the bottom electrode. After bottom contact formation, silicon oxide was deposited by APPJ with different substrate temperatures of 25 ^{o}C, 100 ^{o}C, 150 ^{o}C, and 200 ^{o}C, respectively. Finally, the 300 nm aluminum layer were deposited for all samples by the shadow mask with a area of 250 μm x 250 μm.

2-1-2-3 Fabrication processes of organic thin film transistors (OTFTs)

The bottom contact structure was adopted to fabricate organic thin film transistor. The structure of organic thin film transistor was shown in Figure 2-1-2. The 500 nm thermal silicon dioxide was grown on the top of p-type silicon wafer as the isolation layer. Gate electrode with a 100 nm thick aluminum layer was deposited by thermal coater and Source/ Drain electrodes with 50 nm thick nickel layer were deposited by E-gun. After that, the gate insulator of Silicon oxide with 60 scanning times by APPJ under an atmospheric pressure at 150 ^{o}C was covered. The 50 nm pentacene material obtained from Aldrich was evaporated by thermal coater. During deposition of pentacene active layer, the substrate was heated to 70 ^{o}C at a pressure of $1x10^{-6}$ Torr.

2-1-3 Electrical measurements

Capacitance-Voltage (C-V) relationships were analyzed by HP 4284 LCR meter at 1MHz and the characteristics of Current-Voltage (I-V) were measured by HP4156 semiconductor parameter analyzer. All measurements were carried out at room temperature.

2-1-3 Results and Discussion

Organic thin film transistors are used for flexible electronics which could not sustain higher temperature processes. To understand the impact of substrate temperature for film deposition quality depending on surface morphology, thermodynamics and deposition rate, we choose different substrate temperatures to evaluate the insulator quality and gate leakage current of device.

Figure 2-1-3 shows leakage current density of silicon oxide deposited by APPJ. The leakage current density of silicon oxide deposited by APPJ (APPJ-SiO_2) is about 5E-7 A/cm^2 at E = 0.5 MV/cm. However, the deposition rate at room temperature for APPJ-SiO_2 insulator on aluminum electrode is almost zero, possibly ascribed to poor chemical reaction rate on aluminum substrate. As we known, the surface active energy is highly related to substrate temperature based on chemical vapor deposition dynamics. The equation of chemical reaction rate was shown in Eq. (2-1).

$$C.R. = A\exp(-E_a / kT) \qquad (2\text{-}1)$$

where A is a constant, Ea is active energy, T is substrate temperature, and k is

Boltzmann constant. According to chemical reaction mechanism, the surface reaction can occur easily for the case with a low active energy. Therefore, we can choose different material with a low active energy or lower the reaction barrier by increasing substrate temperature to improve the deposition quality. Here, the different metals including Ni, Ti, Ta, Pt, and Pd have been applied to be the bottom electrode of the MIM capacitor, but the deposition rate of SiO_2 (APPJ) at room temperature is still poor, close to zero. We also used different metal oxide (HfO_2, AlO_2O_3) as the buffered materials between SiO_2/electrode to decrease the active energy. However, the deposition quality is still poor.

To deposit silicon oxide on the metal by APPJ, we tried to increase the substrate temperature up to 100 ^oC, 150 ^oC, and 200 ^oC. We used aluminum as the bottom electrode for MIM structure. Figure 2-1-4 shows the thickness of APPJ-SiO_2 at different temperatures, indicating deposition rate increased with substrate temperature, like surface reaction control. To clarify the effect of temperature-dependence deposition, a fixed flow rate of 200 sccm was applied to concise our experiment design. The detail discussion on the influence of flow rate would be investigated in next section. Figure 2-1-5 shows the leakage current density of silicon oxide deposited by E-gun and APPJ, respectively. The optimized APPJ-SiO_2 at 150C presents a leakage current density of 1E-7 A/cm^2 at 0.5 MV/cm, much better than the silicon oxide deposited by E-gun with a leakage current of 4E-6 A/cm^2.

However, the SiO_2 deposition at room temperature is the future demand. The improvement of surface reaction between Si and bottom electrode is crucial important. Therefore, we deposited silicon oxide on Al electrode with an amorphous Si buffered layer at room temperature. Figure 2-1-6(a) and (b) show C-V and I-V characteristics of Al/SiO_2/amorphous Si/Al MIM structure, respectively. The good capacitance and leakage current characteristics for different scaling-times cases during demonstrate the

stable APPJ deposition process and reliable film quality. However, the experiment confirmed that the APPJ-SiO_2 film could be deposited on a-Si and SiO_2 substrate at room temperature since the active energy of a-Si and SiO_2 were lower than other materials. The experimental results support our previous assumption, which a lower surface active energy facilitate APPJ-SiO_2 deposition on Al electrode. As we mentioned before, the higher thermal budget and Si buffered layer can deposit SiO_2 successfully on Al electrode at room temperature, but the approach aided by buffered layer could increase the thickness variability and process complexity except for extra cost. In addition, we emphasized the importance of process temperature, since most plastic substrates could not sustain the temperature higher than 200 ^{o}C. The APPJ processed SiO_2 at 150 ^{o}C not only maintains a good deposition rate for throughput but also presents a good film quality which show the potential for low-temperature flexible electronic device fabrication.

After the above discussion, we have proposed approaches by using lower temperature control (<150C) and Si buffered layer to solve the issue of film deposition. Sequentially, the transistor characteristics will be discussed in the following part.

The drain current (I_D) versus drain-source voltage (V_{DS}) at varied gate voltages (V_{GS}) shown in Figure 2-1-7. The output characteristic of I_D versus V_{GS} was shown in Figure 2-1-8. The carrier mobility at the saturation region was calculated by the equation:

$$I_D = (W C_i / 2L)\mu(V_G - V_T)^2, \qquad [2]$$

C*i* is the capacitance per unit area of gate insulator in Eq (2). It correspond to a device with channel width W = 200 μm and length L = 100 μm.

The operational voltage was below -4 V for a EOT of 12.4 nm. The saturation mobility and the threshold voltage of the OTFT were about 0.066 $cm^2 V^{-1}s^{-1}$ and – 1.8 V, respectively. There are three possible reasons to explain why the mobility lower than pervious researches [14]-[17]. First, the grain size of the active layer would be affected by the roughness of the electrodes of source and drain due to bottom contact TFT structure. Secondly, poor oxide surface roughness could lead to the mobility degradation. In Figure 2-1-9, the roughness (RMS) of Al gate electrode was about 8.2 nm and a large RMS value of ~10.8 nm can be obtain after APPJ-SiO2 on the aluminum electrode. The uneven Al electrode could affect the roughness of following APPJ-SiO2. The contact angle of about 25 degree for APPJ-SiO2, showing hydrophilic characteristic on the oxide surface is another issue since the surface roughness and hydrophilic characteristics should be the main factors to influence the deposition of pentacene and then decrease the mobility of OTFT devices. To improve these issues, originated from bottom electrode with larger leakage current, we replaced Al (4.2eV) electrode by a higher work function Ni (5.1eV). Figure 2-1-10 shows the RMS of silicon oxide deposited at different temperatures on Al and Ni, respectively. The oxide on an evaporated Ni by E-gun has a RMS value of 2.2 nm, lower than that on Al. To reduce surface roughness of gate insulator and improve the gate leakage current, we used Ni as the bottom electrode of OTFT in the following experiment.

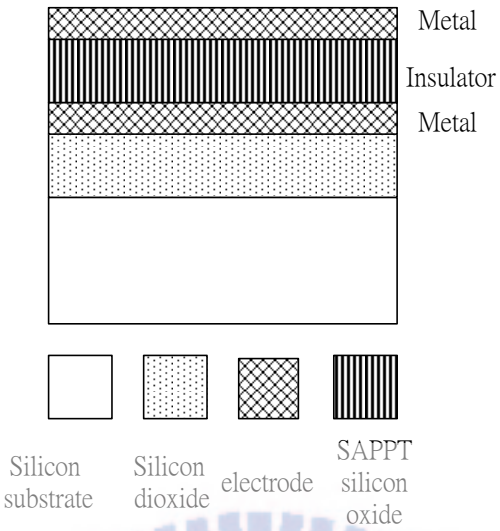


Figure 2-1-1 MIM structure for testing gate insulator's quality.

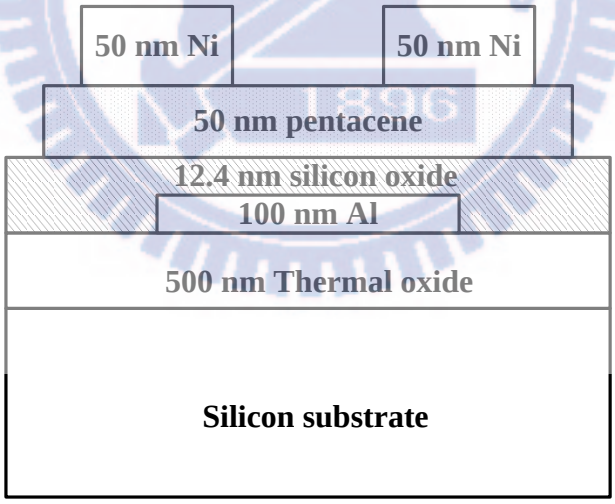


Figure 2-1-2 Scheme of the top contact structure of organic thin transistor

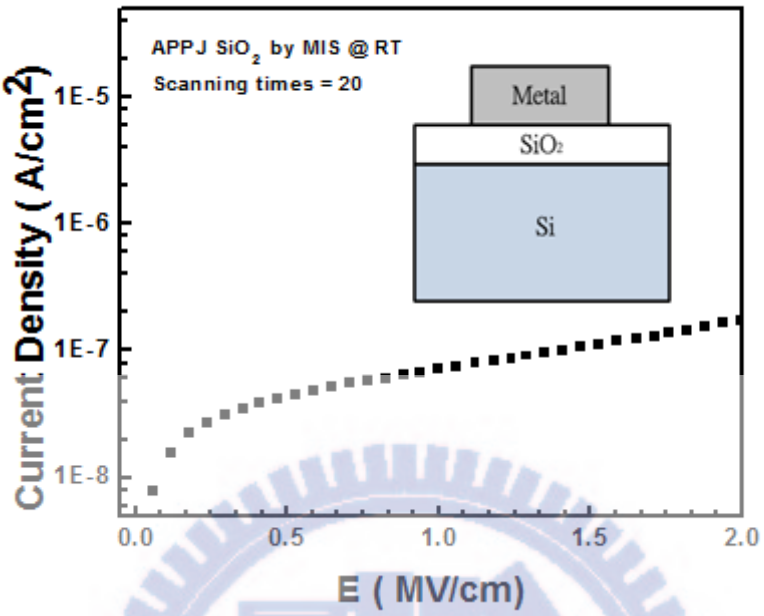


Figure 2-1-3 Leakage current density of silicon oxide deposited by APPJ and MIS structure.

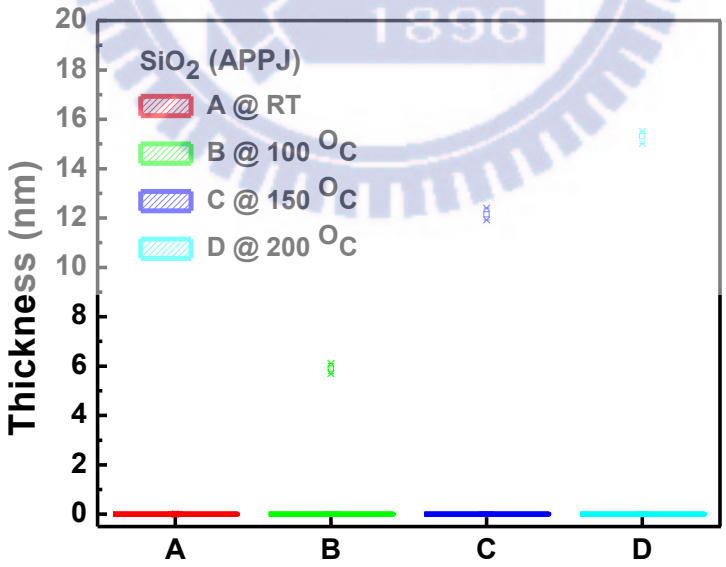


Figure 2-1-4 Thickness of silicon oxide with 60 times at different temperatures.

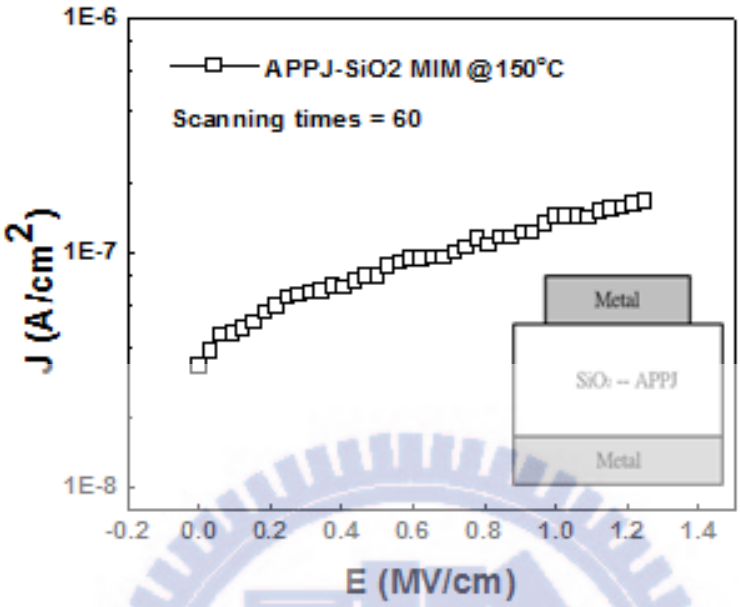
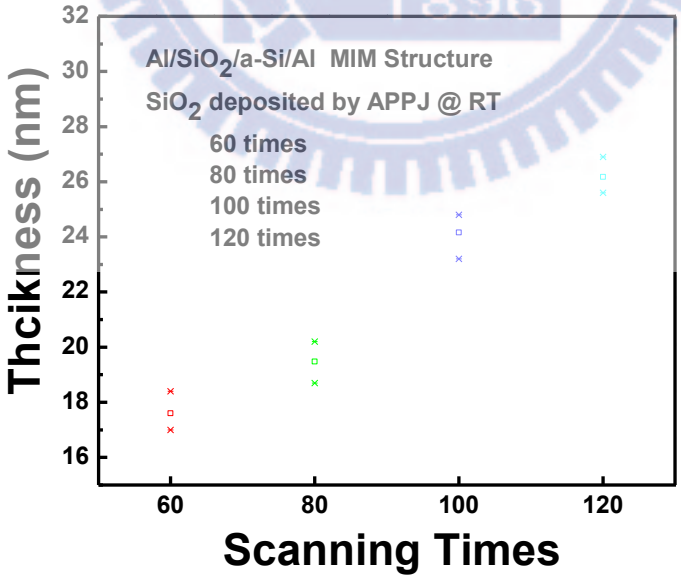
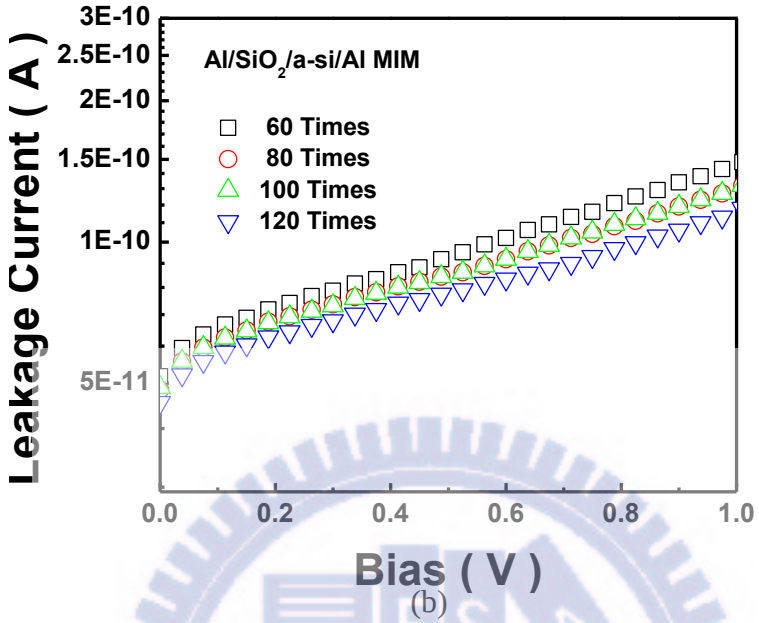


Figure 2-1-5 *J-E* of SiO_2 deposited by APPJ in MIM structure. Leakage current density of SiO_2 (APPJ), deposited at 150 ^{o}C, was about 1E-7 A/cm^2 at 0.5 MV/cm.



(a)



(b)

Figure 2-1-6 (a) Thickness of silicon oxide with a a-Si buffer layer at different scanning times. (b) I-V characteristic of SiO_2 using APPJ at different scanning times.

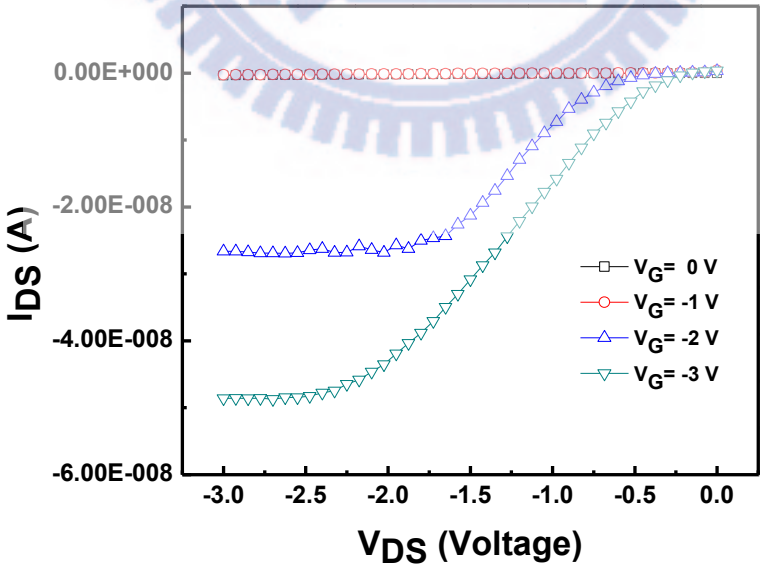


Figure 2-1-7 Scheme of the output characteristics of pentacene-based organic thin film transistor with a lower operation voltage about -3 V.

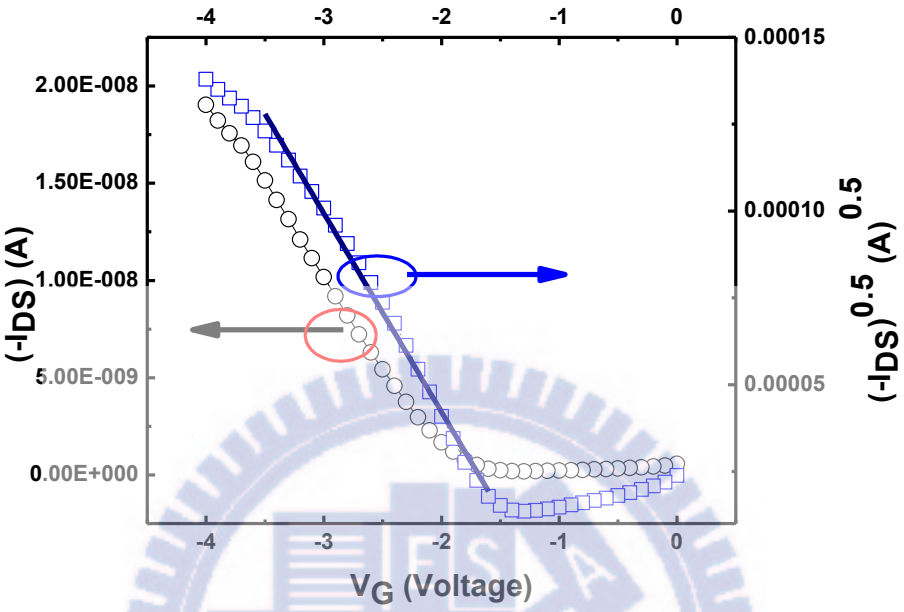


Figure 2-1-8 Scheme of transfer characteristics of penetacene-based organic thin film transistor with mobility about 0.066 cm^2/V-S.

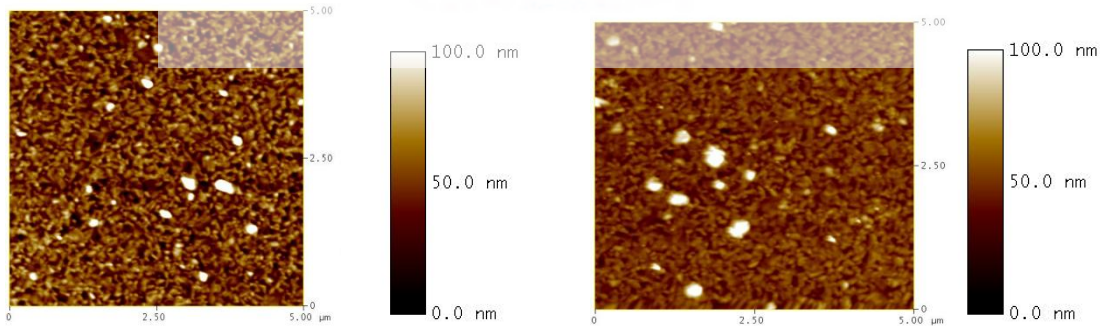


Figure 2-1-9 (a) AFM image of aluminum gate electrode with roughness about 8.7 nm.(b) AFM image silicon oxide (APPJ) deposited at 150 ℃ on the aluminum with the roughness around 10.8 nm

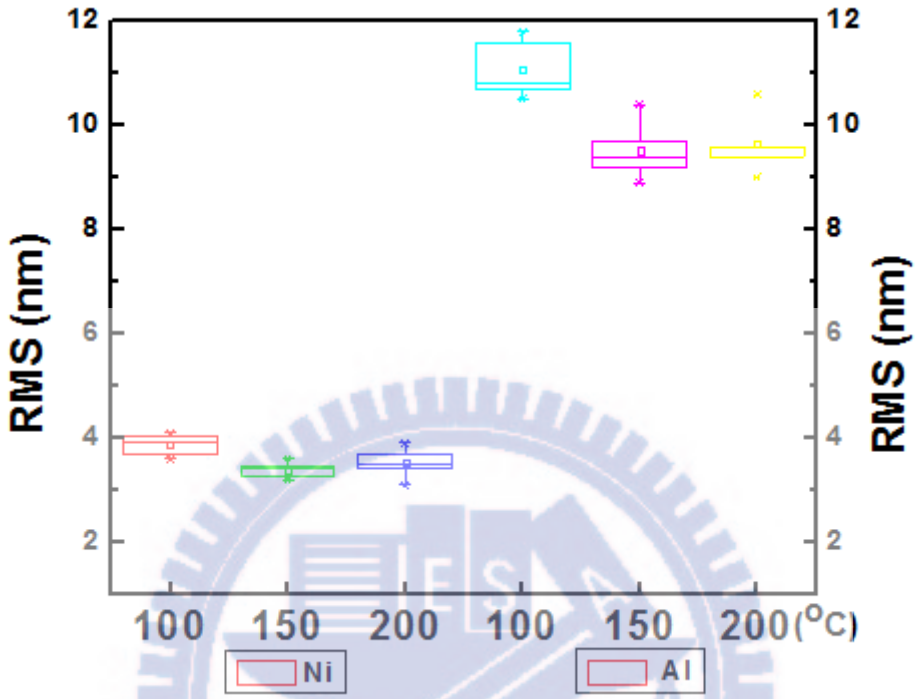


Figure 2-1-10 Scheme of the RMS of SiO_2 deposited at different temperatures separately on Al and Ni.

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2-2 The Effect Carrier Gas's Flow Rate on The Surface Morphology and Film Quality

Carrier gas's flow rate may be an influence factor for depositing SiO_2, discussed in many studies. In APPJ, flow rate would alter the concentration of the precursor at nozzle, influencing the deposition rate and the quality of silicon oxide. In this part, bubble method was utilized to carry the precursor into the plasma region and Ar was used as the carrier gas. The experimental detail was shown in Table 2-2-1. We selected substrate temperature at 150 ℃ because every experimental parameter must be suitable for plastic substrate. From Figure 2-2-1, we could obviously found that the leakage current density was increased with increasing the carrier gas's flow rate. When the gas flow rate was less than 100 sccm, the leakage current density could be suppressed below 2 E-8 A/cm^2 at 0.5 MV/cm. However, a larger leakage current of two order of magnitude (1E-6 A/cm^2) than optimized one was obtained as introducing an excess follow rate of > 200 sccm. From Figure 2-2-2, the thickness and roughness were increased with increasing the flow rate of carrier gas. The AFM plots of SiO_2 were also shown in Figure 2-2-3. The roughness of silicon oxide increased rapidly when the flow rate over 200 sccm. The rapid deposition rate would cause silicon oxide too loose to suppress leakage current. In addition, we used SEM to get the top view of silicon oxide surface shown in Figure 2-2-4 and found that these pellets on the silicon oxide surface was also increased obviously at higher flow rate. These pellets must be decreased because the surface roughness would scatter transport carriers which would decrease the mobility of OTFT. In addition, organic molecules

ordering and grain size would be degraded with high surface roughness [1-2] which would decrease the mobility of organic semiconductor. In our experiment, the roughness of silicon oxide could be reduced by decreasing the flow rate and the pellets also could be decreased, which would increase the possibility of application for OTFT. Figure 2-2-5 shows the XPS of silicon oxide deposited with different flow rates and the percentage of carbon existed in silicon oxide, shown in Table 2-2-2, was increased with increasing the flow rate. Some precursor may not be decomposed completely and then deposited on the surface of sample to form the impurities which may consist of C-H, C-O, and C-O-O in our demonstrated silicon oxide. This phenomenon may be more serious when the flow rate increases. CVD reactions are homogeneous, heterogeneous, or a combination of both. Homogeneous reactions nucleate in the gas phase and lead to particle formation. The greatest single problem in CVD technology. Most CVD processes are chosen to be heterogeneous reactions [3-4]. That is, they take place at the substrate surface rather than in the gas phase and form the desirable film deposit. In general, increasing temperature leads to increase film deposition rate, greater density, and improved structural perfection and crystallinity of the deposits. The quality of silicon oxide deposited by APPJ in this thesis was also improved with increasing temperature in lower flow rate. It is very important to control temperature and flow rate for depositing silicon oxide at heterogeneous reactions. Although silicon oxide deposited by APPJ in air may combined some particles or impurities, low leakage current density of insulator was obtained by well controlling temperature, flow rate, and other parameters of APPJ.

Table 2-2-1 The details of experimental parameters of silicon oxide deposited with different flow rates by APPJ.

Experimental parameters	
Main gas	CDA
Speed (mm/sec)	30
Gap distance (cm^2)	2.2
Scanning times	60
Ar flow rate (sccm)	60~300
Substrate temperature (℃)	150

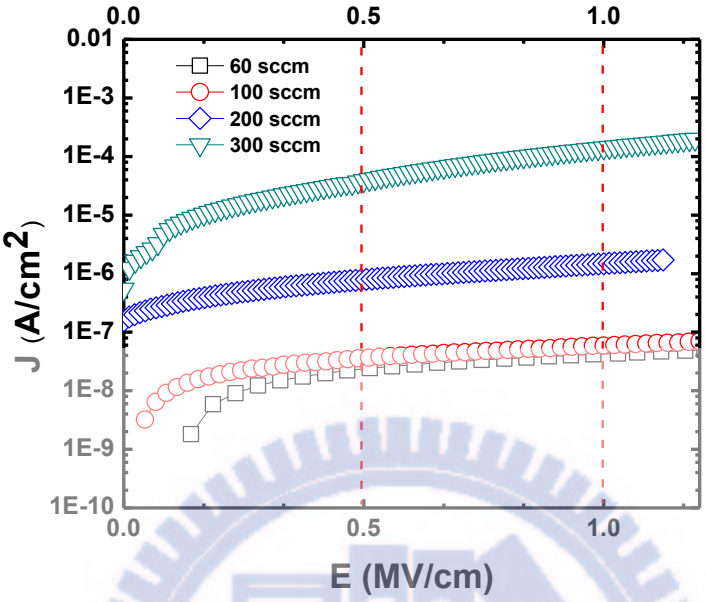


Figure 2-2-1 Plot of leakage current density versus electric field (*J-E*) of our APPJ-SiO_2 deposited with different carrier gas's flow rates.

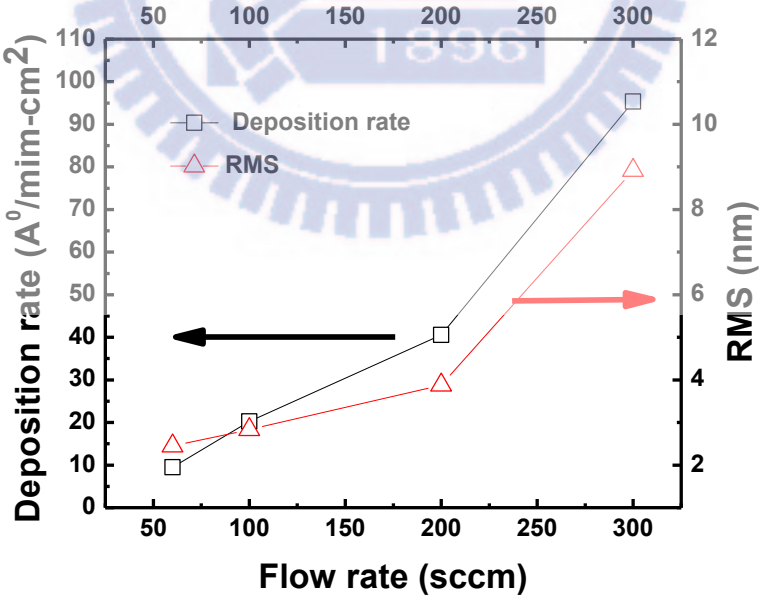
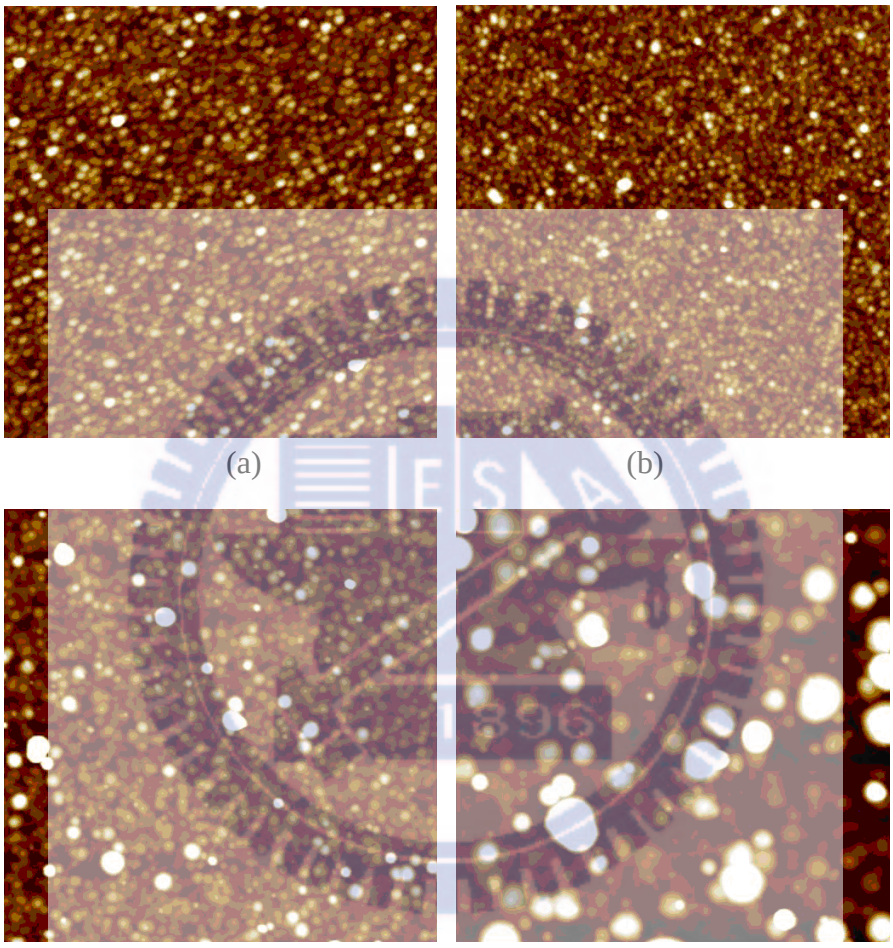


Figure 2-2-2 Deposition rate and RMS of silicon oxide deposited with different flow rates of atmospheric pressure plasma jet.



(a) (b)

(c) (d)

Figure 2-2-3 AFM images of silicon oxide fabricated with different Ar flow rates of APPJ. (a) 60 sccm (b) 100 sccm (c) 200 sccm (d) 300 sccm

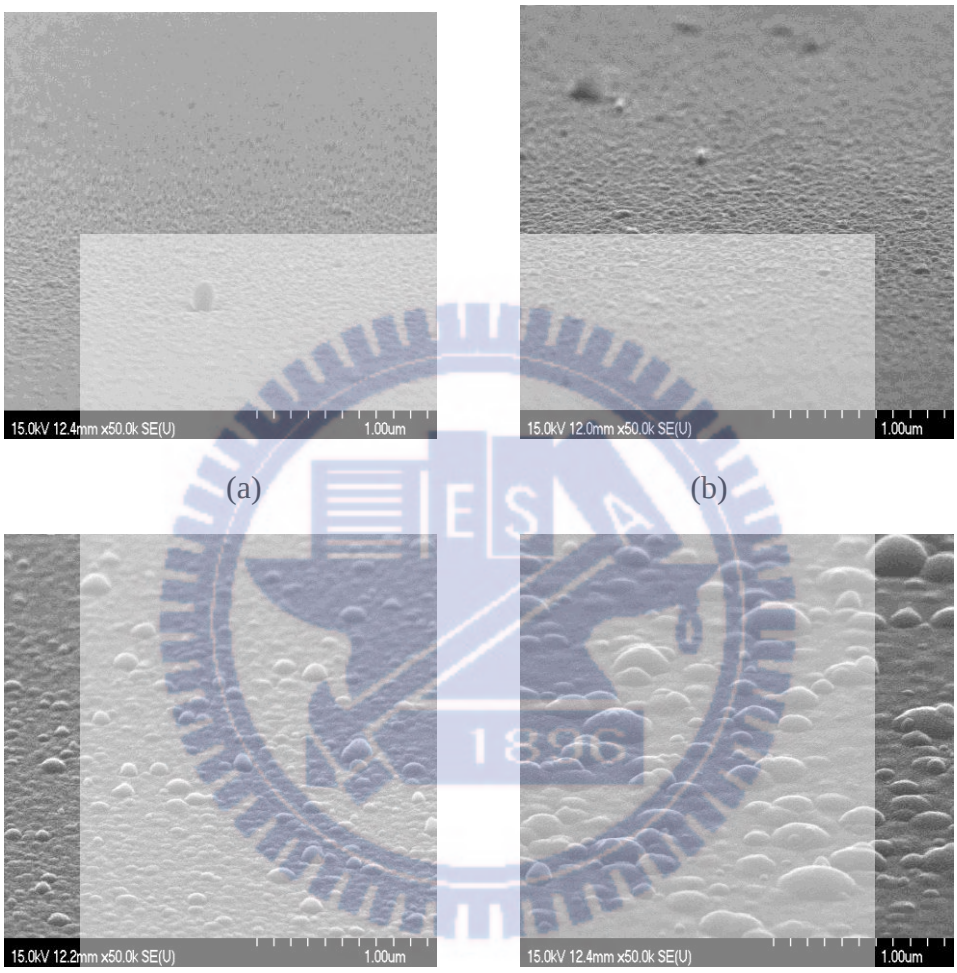


Figure 2-2-4 SEM images of silicon oxide fabricated with different Ar flow rates of atmospheric pressure plasma jet.
(a) 60 sccm (b) 100 sccm (c) 200 sccm (d) 300 sccm

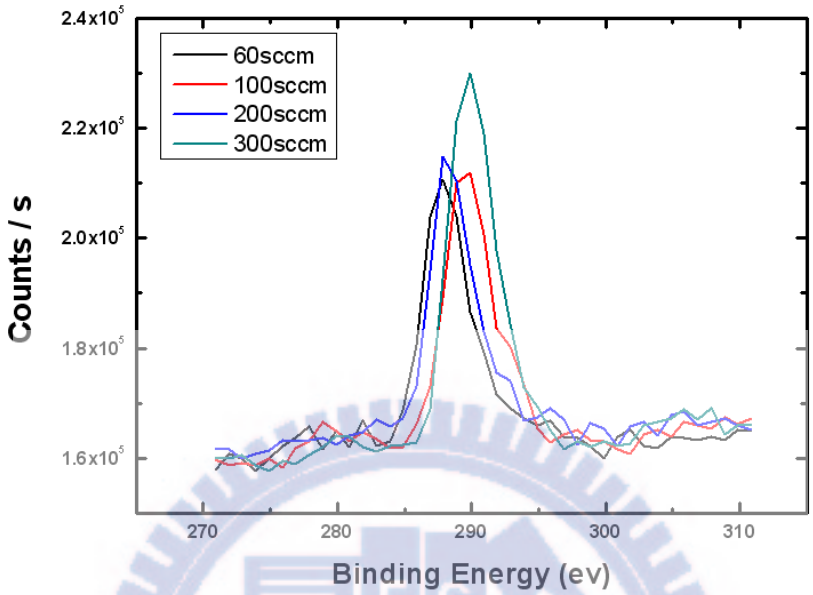


Figure 2-2-5 X-ray Photoelectron Spectroscopy spectra of SiO_2 (APPJ) deposited with different Ar flow rates.

Table 2-2-2 The concentration of carbon in silicon oxide, deposited with different flow rates, was analyzed by X-ray Photoelectron Spectroscopy.

	Name	Start BE	Peak BE	End BE	Height Counts	FWHM eV	Area (P) CPS.eV	Area (N)	At. %
60sccm	C1s	293.09	287.87	285.49	4786.72	1.99	11891.34	6543.55	3.81
100sccm	C1s	294.21	289.38	286.2	5041.63	2	12710.8	6995.36	4.1
200sccm	C1s	295.1	288.23	285.81	5267.28	1.96	14248.2	7840.72	4.52
300sccm	C1s	295.5	289.52	286.39	6606.53	1.71	18142.94	9985.05	5.87

Reference

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2-3 The Influence of Gap Distance on Deposition Rate and Film Leakage

In this section, we only focused the study on the gap distance from nozzle to sample surface, as shown in Figure 2-3-1. The detail of experimental parameters were shown in Table 2-3-1. CDA was used as the main gas to investigate the effect of gap distance on deposition process since the deposition rate for APPJ-SiO_2 with a main gas of CDA was more stable than the others (O_2, N_2). In Figure 2-3-2, the deposition rate of silicon oxide increasing with gap distance decreasing could be observed. This may be attributed to the higher species concentration near Al surface participate the film deposition at a small gap distance, which would increase the surface reaction probability and deposition rate.

In previous section of 2-1 and 2-2, we demonstrated the deposition rate would be influenced by temperature, increasing with substrate temperature due to a decrease of active energy. In addition, modifying species concentration by an appropriate flow rat to avoid the occurrence of homogeneous reactions during deposition is also important. As we known, the mean free path (MFP) of reactive species would be decreased in atmospheric pressure, compared to high vacuum environment. Also, the concentration of reactive species near the Al substrate would be decreased while the gap distance increases. In Figure 2-3-2, the deposition rate increase with gap distance deceasing but no film deposition process can be observed at an excess gap (>2.5cm), possibly caused by the lack of reactive species.

We concluded that the increase of deposition rate with gap distance may be attributed to two reasons. One is the concentration of reaction species and the other may be contributed from the “varied” fixed substrate temperature. Although the fixed substrate temperature of 150 ^{o}C has been applied in this experiment, the temperature near the substrate still possibly varied with changing the gap distance. We believed

that the additional thermal budget for the “fixed” substrate temperature is from the glowing plasma source. However, as the gap distance was decreased to 1.8 mm, the deposition rate decreased abruptly and the roughness increased. We suggested that the strong plasma flow would bombard the substrate surface with the decrease of gap distance, which may leave damages on the substrate surface to lower the deposition rate. In addition, we also think that some reactive species with high dynamic energies would be reflected and then formed nucleated particles in the air to fall on the substrate, which may lead to the large surface roughness. Fig. 2-3-3 shows the leakage current density versus electric field of silicon oxide deposited with atmospheric pressure plasma at different gap distances. We could found that the leakage current density of silicon oxide with a gap distance of 1.8 mm is the largest, suggesting that the plasma damage is major contribution in the leakage performance, as we described earlier.

The leakage current density and surface roughness for APPJ-SiO_2 with different gap distances have been summarized in Table 2-3-3. While the gap distance was decreased from 2 mm to 1.8 nm, the leakage current density can be lowered about 2 times. However, the large surface roughness (3.618 nm) could influence the coverage of organic layer and device mobility. In this study, we selected the gap distance of 2.2 mm as process parameter to fabricate gate insulator of OTFT because the condition has good insulator quality and an appropriate deposition rate.

According to the previous discussion, we consider that the concentration of ionization species would influence the deposition rate of APPJ-SiO_2 with various gap distances and oxide quality might be degraded at a small gap distance between nozzle and substrate (<2.0 mm).

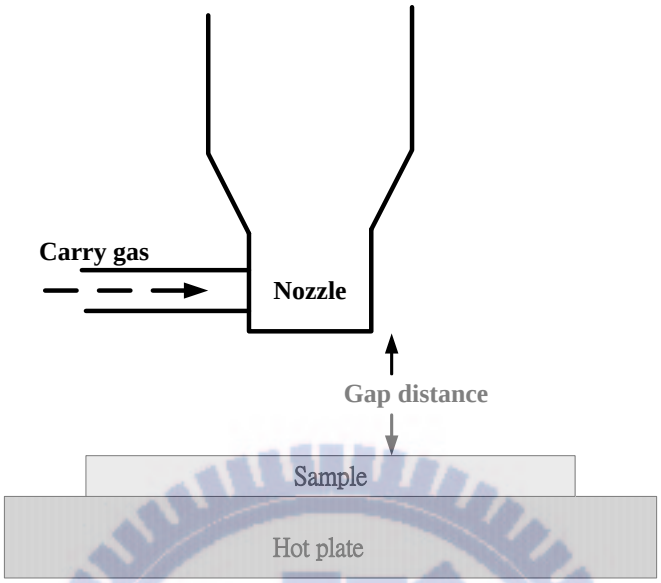


Figure 2-3-1 Schematic diagram of gap distance of APPJ. Gap distance means the distance from nozzle to the surface of sample.

Table 2-3-1 Experimental parameters of APPJ-SiO_2 deposited with different gap distances.

Experimental parameters	
Main gas	CDA
Speed (mm/sec)	30
Gap distance (cm)	1.8~2.5
Scanning times	60
Ar flow rate (sccm)	100
Substrate temperature (℃)	150

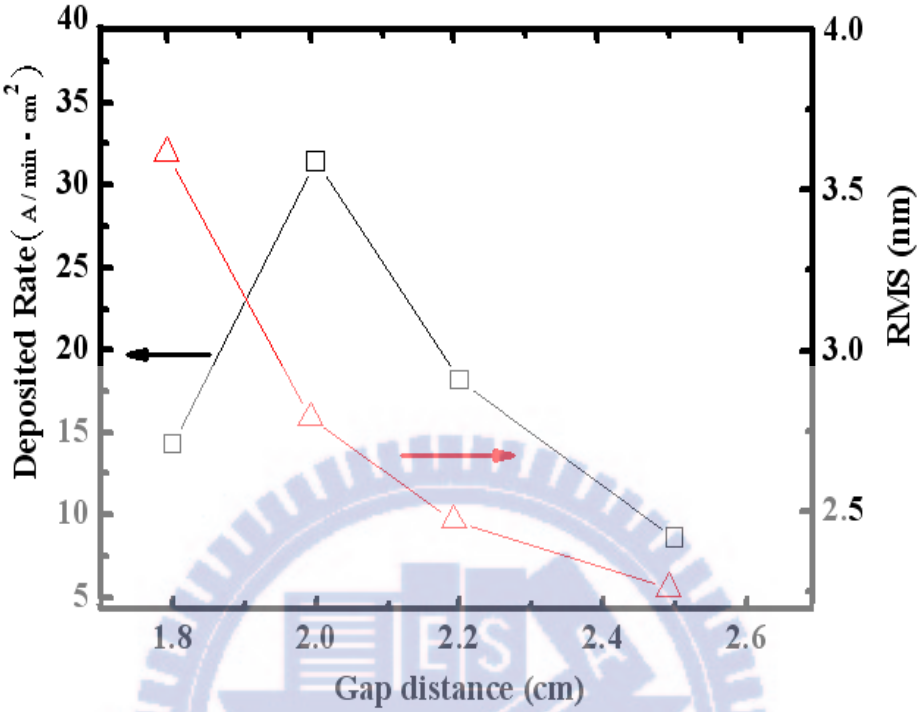


Figure 2-3-2 Deposition rate and RMS of APPJ-SiO_2 deposited with different gap distances.

Table 2-3-2 Thickness and deposition rate of APPJ-SiO_2 deposited with different gap distances.

Gap distance(cm) (CDA main gas)	Scanning times	Capacitance (nF/cm^2)	Thickness (Å)	Deposition rate (Å / min • cm^2)
1.8	60	161.2~159.3	67.2~71.4	14.28
2	60	57.17~54.94	151~157	31.4
2.2	60	97.93~94.74	88.3~91.5	18.2
2.5	60	201.43~199.84	42.9~43.1	8.6

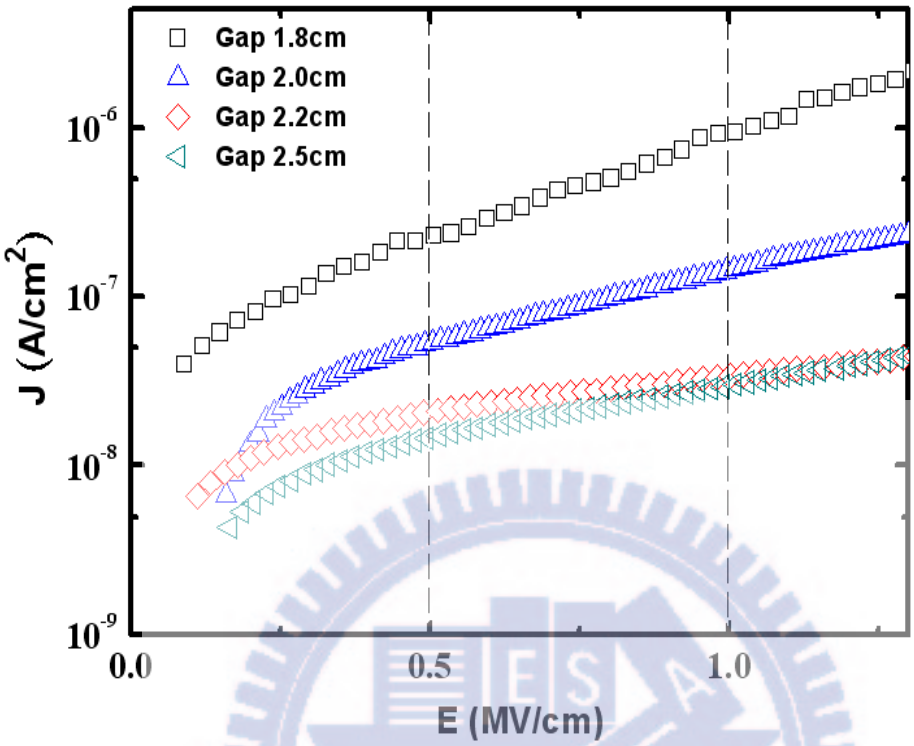


Figure 2-3-3 Leakage current density versus electric field of APPJ-SiO_2 with different gap distances.

Table 2-3-3 The leakage current density and surface roughness of silicon oxide deposited with different gap distances.

Gap distance (cm)	**Leakage current density (A/cm^2) at 0.5 MV/cm**	**Root Mean Square (nm)**
1.8	2.29E-7	3.618
2	5.34E-8	2.79
2.2	2.12E-8	2.47
2.5	1.46E-8	2.26

2-4 The Effect of Main Gas on The Deposition Rate and Electrical

Characteristics

2-4-1 Introduction

Main gas, used to generate plasma, is a key factor for precursor dissociation and film quality. During process, main gas was introduced into the high electric field region between anode and cathode to generate plasma source, including electrons, ions, metastable atoms. Under deposition process, deposition rate, hardness, and refraction index deposited with different main gases were widely studied. Some researches used low oxygen-ratio main gas to increase the deposition rate of silicon oxide [1]-[3], since oxygen could increase the dissociation of organic precursor. In this section, we would investigate the influence of different main gases on deposition rate, surface roughness, and leakage current of device.

2-4-2 Experiment

Main gas flow into the high electric field region between electrodes of APPJ was shown in Figure 2-4-1. In this section, we utilized oxygen, nitrogen, and CDA as the main gas for APPJ to decompose tetraethoxysilane (TEOS). The Metal-Insulator-Metal (MIM) capacitor was used to study electrical characteristics. First, a 500-nm-thick SiO_2 insulation layer was grown on the p-type silicon substrate by using a wet oxidation method at 1000 ^{o}C. Then, a 50-nm-thick Ni deposited by E-gun evaporator was used as bottom electrode and low temperature SiO_2 (APPJ) was deposited on it using different main gases including oxygen, nitrogen, and CDA for this experiment. After the formation of the low temperature SiO_2, a 50-nm-thick Ni was deposited on the SiO_2 (APPJ) by E-gun evaporator. The optimized substrate

temperature was about 150 ^{o}C. As for material analysis, the surface roughness and film compound were analyzed by AFM and XPS, respectively. The C-V and I-V characteristics were measured by HP4156 and HP4284, respectively.

2-4-3 Results and Discussion

Oxygen, nitrogen, and CDA were used to investigate the influence of different main gases on deposition rate and oxide quality. Silicon oxide was deposited at a gap distance of 2.2 mm under substrate temperature of 150 ℃. The detail experimental parameters were shown in table 2-4-1. However, the appropriate deposition rate and good oxide quality were dependent of the selection of gap distance and deposition temperature. The plot of leakage current density as a function of the electric field shown in Fig. 2-4-2 makes a comparison of silicon oxides fabricated by different main gas (N_2, O_2, CDA). Silicon oxide deposited by CDA with the best quality among these exhibits a low leakage current of 2.28 E-8 A/cm^2 at 0.5 MV/cm, compatible to other oxides processed at a low-temperature or under vacuum.

Some studies reported that the deposition rate of silicon oxide using the precursor of TEOS is dependent of the concentration of oxygen plasma, consist of oxygen atom, metastable oxygen, and ozone [4]. Furthermore, the deposition rate of silicon oxide with an oxygen main gas is the fastest since oxygen has better decomposition capability to TEOS precursor. The fast deposition rate may decrease the denseness of silicon oxide, thereby generate high leakage current density.

However, silicon oxide processed by a CDA main gas shows the best quality although the deposition rate is low. It is worth to note that the oxygen percentage in CDA is about 20 %, much higher than the main gas of nitrogen; nevertheless the deposition rate of CDA is the slowest. This may because the higher oxygen

percentage in nitrogen plasma has strong electronegativity, which decrease the electron density of plasma [5] and result in the decrease of the excited species. Although some researches [1-3] proposed that the deposition rate of silicon oxide was proportion to oxygen partial pressure but the percentage of below 2% was occupied by oxygen under total gas in these studies.

The use of main gas of pure nitrogen can generate a lot of ozone because the high density nitrogen plasma generated by APPJ could excite air to create ozone and excited oxygen atoms. Figure 2-4-3 shows the deposition rate and surface roughness of silicon oxide deposited by different main gas. The deposition rate of silicon oxide using oxygen and nitrogen as main gas is faster than CDA since oxygen and nitrogen could generate high concentration reaction species to increase the deposition rate. However, the high concentration reaction species may increase the nucleation possibility, which may fall down on the silicon oxide surface to form the pellets.

Table 2-4-2 shows the thickness and deposition rate of silicon oxide. Fig. 2-4-4 shows the AFM images of silicon oxide surface deposited with different main gases. The surface roughness silicon oxide deposited by nitrogen and oxygen was about 3.08 and 3.86 nm, respectively, larger than the silicon oxide with a CDA. Scanning electron microscopic (SEM) images of silicon oxide deposited with different kind main gas were presented in Fig. 2-4-5. We could find that the uniformity of silicon oxide with a main gas of CDA is better than that of oxygen. As seen in SEM, there are many pellets on the surface of silicon oxide with the main gases of oxygen and nitrogen.

To clarify the issues raised by the use of different main gas, we analysis the compound elements of the silicon oxide processed by different main gases. The XPS spectra for compound analysis of oxides was shown in Fig. 2-4-6. Silicon oxide using TEOS has a good stoichiometry, which the ratio of oxygen and silicon is close to 2.

However, there are lots of carbons impurities, remaining in silicon oxide film would lead to an unwanted leakage under bias. Although oxygen and nitrogen have strong capability for TEOS decomposition, more carbons residues than CDA are unacceptable. In a word, the oxygen and nitrogen as main gas may have a high risk on pre-nucleation in air and pellets formation during the period of precursor decomposition and surface reaction.

The leakage current density is plotted as a function of electric field on ln (J/T^2) – $E^{1/2}$ scales in Figure 2-4-7. Clearly, two transport mechanisms are observed in low and high fields of SiO_2 (CDA). The linear variations of the current density of SiO_2 (CDA) correspond to Schottky emission mechanism in the low electric field and shows Poole–Frenkel mechanism in the high field. However, leakage current curves of SiO_2 deposited by O_2 and N_2 only shows Poole–Frenkel mechanism. Because SiO_2 (CDA) has low surface roughness and high density, the Schottky barrier, suppressing leakage current in low electric field, could form between metal and SiO_2. These also could approve that SiO_2 (CDA) has higher quality than SiO_2 (O_2 or N_2).

Table 2-4-1 Experimental parameters of APPJ-SiO_2 deposited with different main gases

Experimental parameters	
Main gas	CDA, N_2, O_2
Speed (mm/sec)	30
Gap distance (cm)	2.2
Substrate temperature (℃)	150
Ar flow rate (sccm)	100
Scanning times	60 or 15 (N_2, O_2)

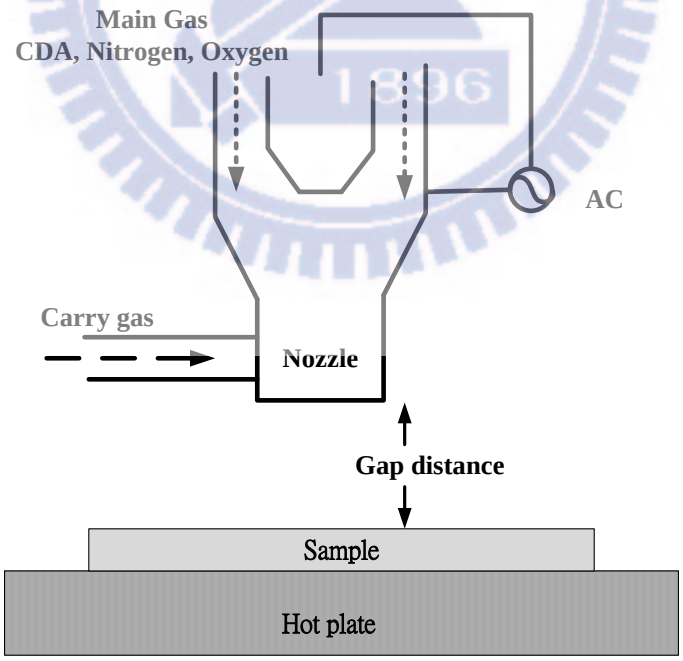


Figure 2-4-1 Main gas was introduced into the high electric field region between electrodes of APPJ for generating plasma.

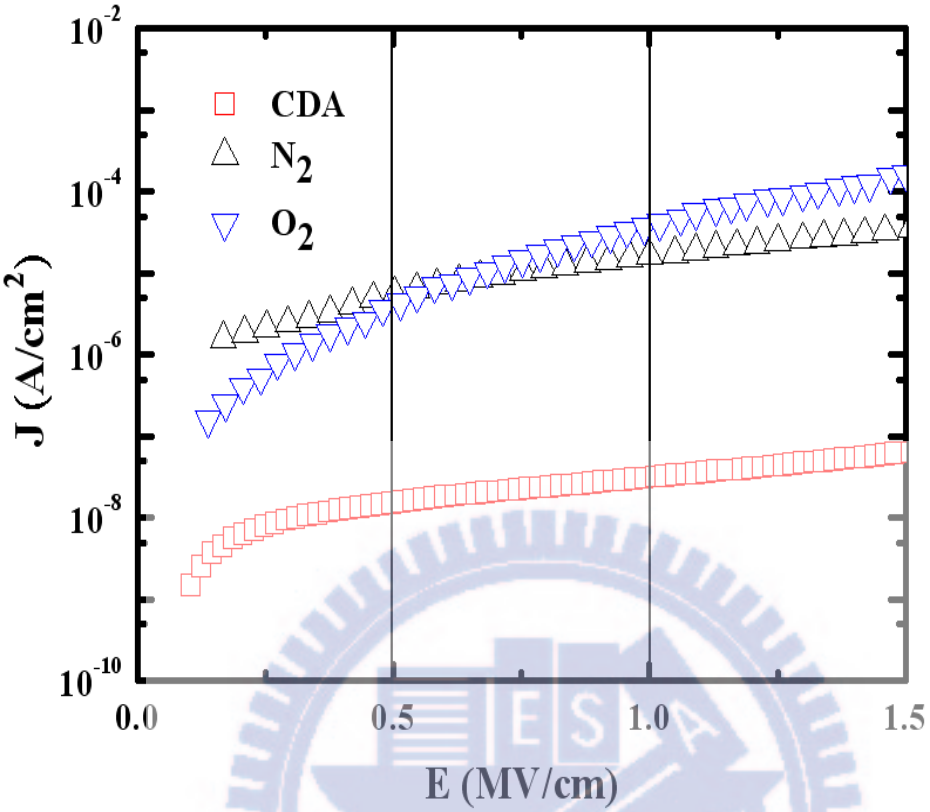


Figure 2-4-2 Electric field versus leakage current density of silicon oxide with different main gases of atmospheric pressure plasma jet.

Table 2-4-2 Leakage current density (A/cm2) of APPJ-SiO_2 at 0.5 MV/cm with different main gases.

Main gas	Leakage current density (A/cm^2) at 0.5 MV/cm
CDA	1.59E-08
N_2	5.54E-06
O_2	4.41E-06

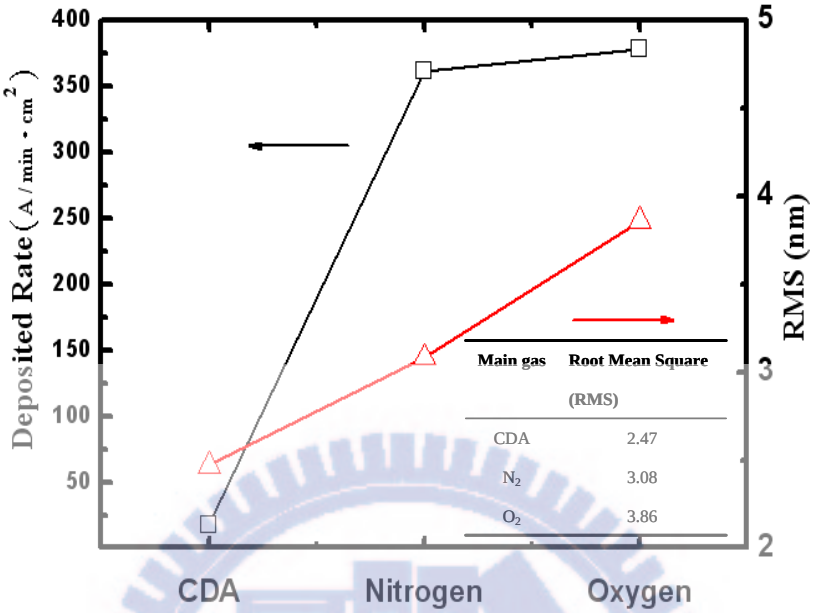
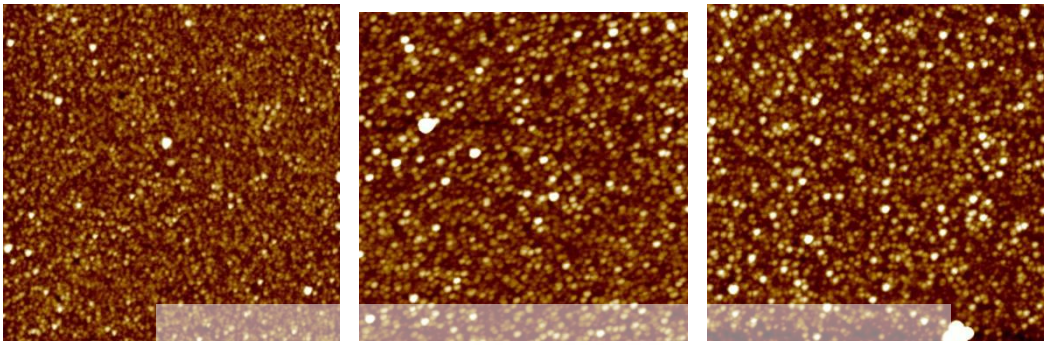


Figure 2-4-3 Deposition rate and surface roughness of silicon oxide deposited by different main gases.

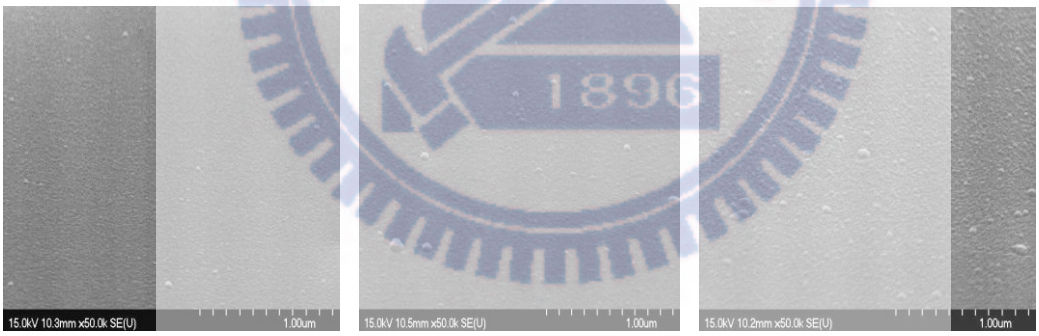
Table 2-4-3 Deposition rate and thickness of SiO_2 deposited with different main gases of atmospheric pressure plasma jet.

Main gas	Scanning times	Capacitance (nF/cm^2)	Thickness (Å)	Deposition rate (Å / min • cm^2)
CDA	60	97.93~94.74	88~91	18.2
Nitrogen	15	24.6~19.11	351~452	361.6
Oxygen	15	23.65~18.23	365~473	378.4



(a) CDA (b) N_2 (c) O_2

Figure 2-4-4 AFM images of silicon oxide fabricated with different main gases of atmospheric pressure plasma jet. (a) CDA (b) N_2 (c) O_2



(a) CDA (b) N_2 (c) O_2

Figure 2-4-5 SEM images of silicon oxide fabricated with different main gases of atmospheric pressure plasma jet. (a) CDA (b) N_2 (c) O_2

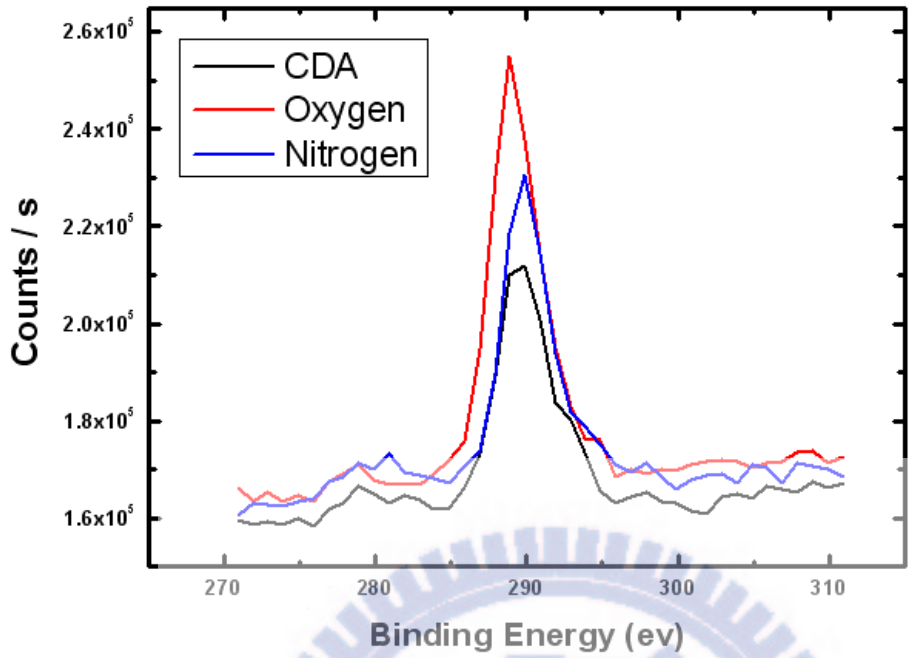


Figure 2-4-6 X-ray Photoelectron Spectroscopy survey spectra from silicon oxide fabricated with different main gases of atmospheric pressure plasma jet.

Table 2-4-4 Composition of silicon oxide fabricated with different main gases of atmospheric pressure plasma jet.

Name (At. %)	CDA	N_2	O_2
Si2P	33.12	32.8	31.13
O1s	62.45	62.13	61.38
N1s	0.33	0.32	0.63
Cls	4.1	4.75	6.86

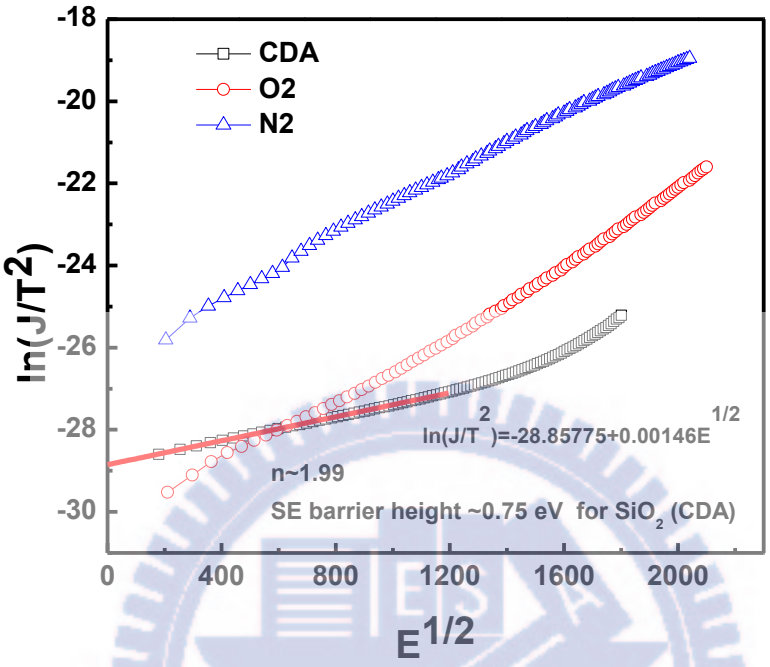


Figure 2-4-7 The leakage currents of silicon oxide deposited with different main gases are plotted as functions of electric field on ln (J/T^2) – $E^{1/2}$ scales. Using CDA as main gas could get lower leakage current.

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Chapter 3 Characterization and Discussion of Low-Voltage OTFT Devices with a Atmospheric-Deposited SiO_2

3-1 Introduction

OTFTs have been widely studied for a long time and some researches also used OTFTs to fabricate prototype of flexible display or flexible electronics. There are some main issues of OTFTs which have been extensively studied such as organic semiconductor materials, surface treatment, low temperature and low cost processes, source-drain contact resistance, and high operational voltage. We utilized APPJ to deposit silicon oxide at low temperature for low cost and temperature process. The thickness of our demonstrated silicon oxide is only about 9.08 nm which could obviously decrease the operation voltage of OTFTs. In addition, leakage current density of our proposed silicon oxide was only 2.13E -8 A/cm^2 at 0.5 MV/cm. Our proposed OTFTs shows a low subthreshold swing of only 0.66 V/dec, a low threshold voltage of -0.8 V, a low operation voltage of -2 V.

3-2 Experiment

In the previous sections, we focus on investigating and developing low temperature processes of high quality gate insulator by atmospheric pressure plasma jet. After estimating processes and quality of silicon oxide, silicon oxide deposited at low temperature about 150 ^{o}C, suitable carry gas's flow rate about 100 sccm and gap distance about 2.2 cm was applied as the gate insulator of OTFTs. The leakage current density of the demonstrated silicon oxide was suppressed about 2.13E-8 A/cm^2 at 0.5 MV/cm with MIM structure and the breakdown voltage was about 8 MV/cm which could be comparable with other researches about OTFTs [1-4]. Figure 3-1

shows the leakage current density and breakdown voltage of the proposed silicon oxide. Leakage current density of most researches were around 5E-6 ~ 1E-8 A/cm^2. Only few researches could deposit gate insulator at low temperature below 200 ^{o}C and meet low cost and high throughput processes. Additionally, the thickness of silicon oxide was control below 20 nm by us in our study in order to decrease the operation voltage. The operation voltage in many OTFTs studies are about -20 ~ -60 V [5-6] which would create higher active power consumption of OTFT. High power consumption is not appropriate for portable electronics. Ordering of organic semiconductor and the EOT of gate insulator are the main two points which would influence the operation voltage of OTFTs. Therefore, the demonstrated silicon oxide was only about 9 nm.

Finally, we integrated our proposed silicon oxide into pentacene-based organic thin-film transistors. Figure 3-2 shows the detail fabrication processes of OTFTs. The length and width of OTFTs were separately about 500 μm and 2000 μm. The bottom and top electrodes all used 50 nm Ni.

3-3 Results and Discussion

The I_D–V_D characteristics shown in Figure 3-3 are well behaved and suggest possible operation at -2 V, which has the advantage of reducing the power consumption ($I_D \times V_D$) in circuit operations. The transfer characteristics (I_D–V_G), as shown in Figure 3-4, enable the extraction of the mobility and V_T from the $|I_D|^{1/2}$ versus V_G plot. The device shows a lower operation voltage about -2 V, a lower threshold voltage about -0.8 V, a good mobility 0.66 cm^2/V-s, and a good subthreshold swing about 700 mV/decade. Table 3-1 shows the summarize the characteristics and processes of OTFTs studied by other researches about low

operation voltage or low temperature processes for comparing with this work. In deposition system, most researches used vacuum deposition system for fabricating their high-k material and subsequently processed with a high temperature annealing. Some researches utilized spinning technique to fabricated polymer or nanocomposite as gate insulator of OTFT but polymer or nanocomsite must bake for a long time. Our demonstrated silicon oxide was deposited at low temperature and atmospheric pressure by APPJ without annealing and shows good insulator quality. Our proposed OTFTs have lower operation voltage, subthreshold voltage, and subthreshold swing which are contributed by the thinner thickness, lower surface roughness, and higher quality gate insulator.

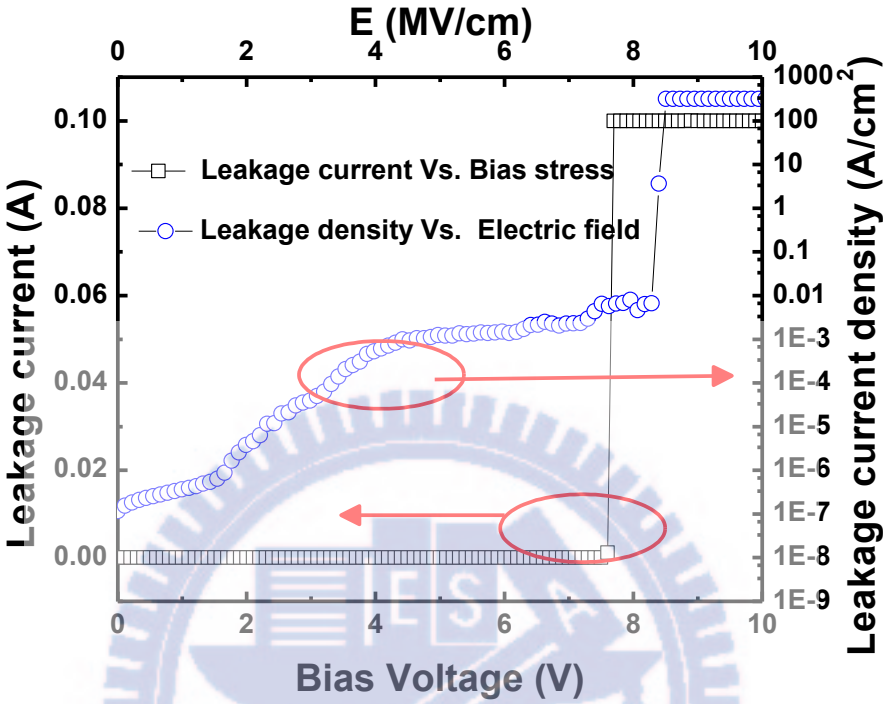
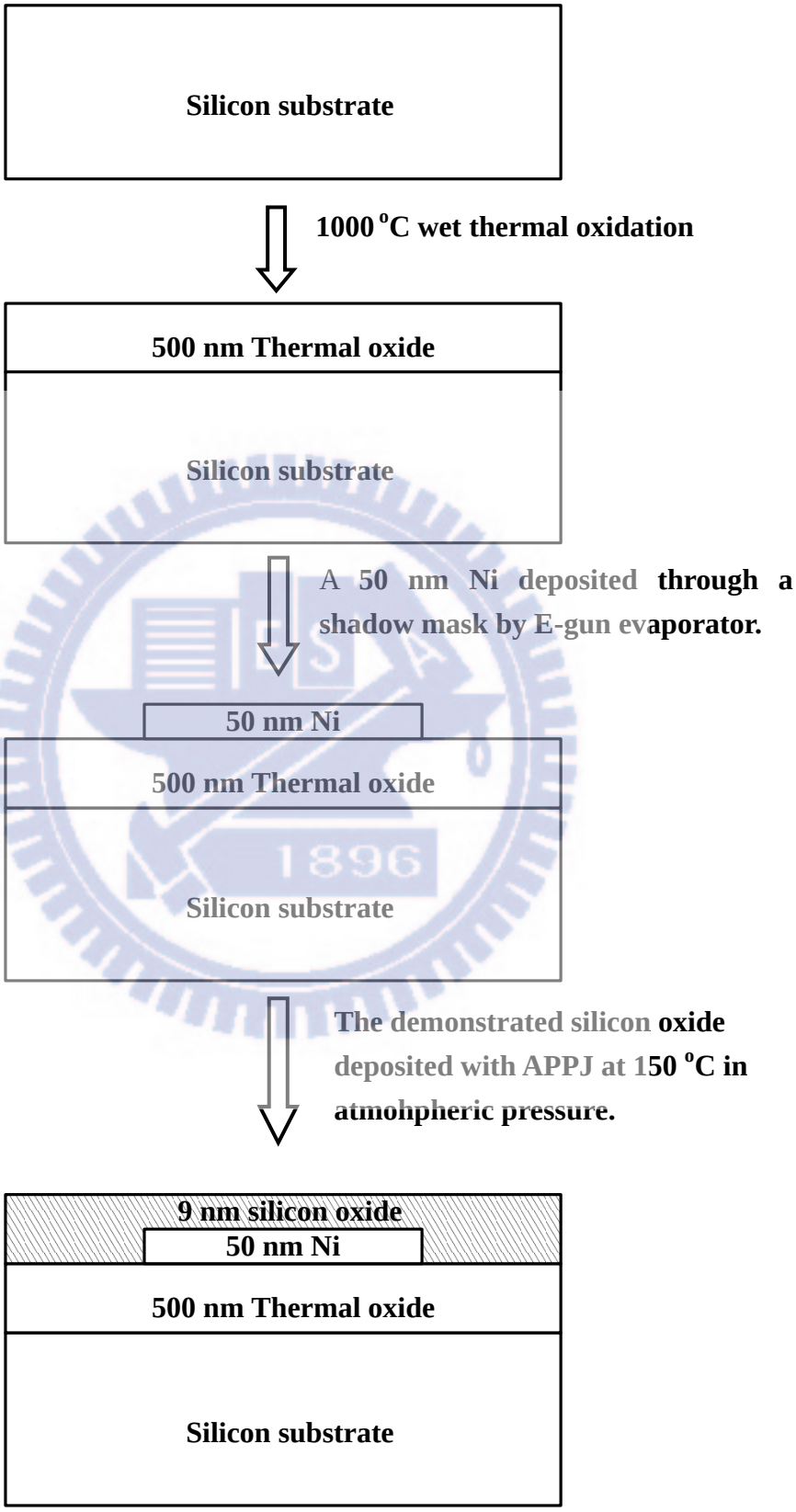


Figure 3-1 Leakage current density of silicon oxide showed the breakdown voltage was about 8 MV/cm.


Silicon substrate
1000 °C wet thermal oxidation
500 nm Thermal oxide
Silicon substrate
A 50 nm Ni deposited through a shadow mask by E-gun evaporator.
50 nm Ni
500 nm Thermal oxide
Silicon substrate
The demonstrated silicon oxide deposited with APPJ at 150 °C in atmohpheric pressure.
9 nm silicon oxide
50 nm Ni
500 nm Thermal oxide
Silicon substrate

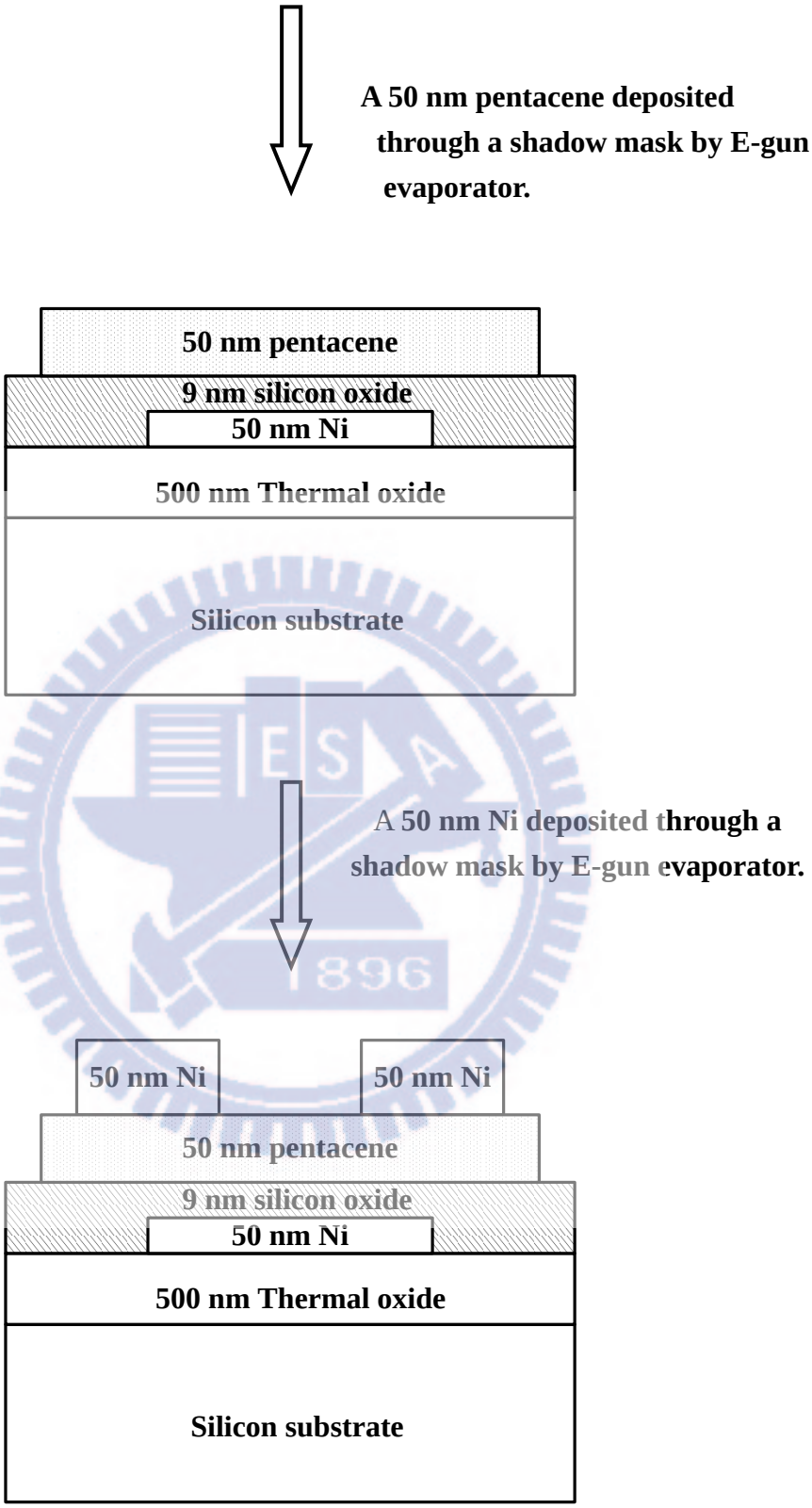


Figure 3-2 Fabrication processes of organic thin film transistors.

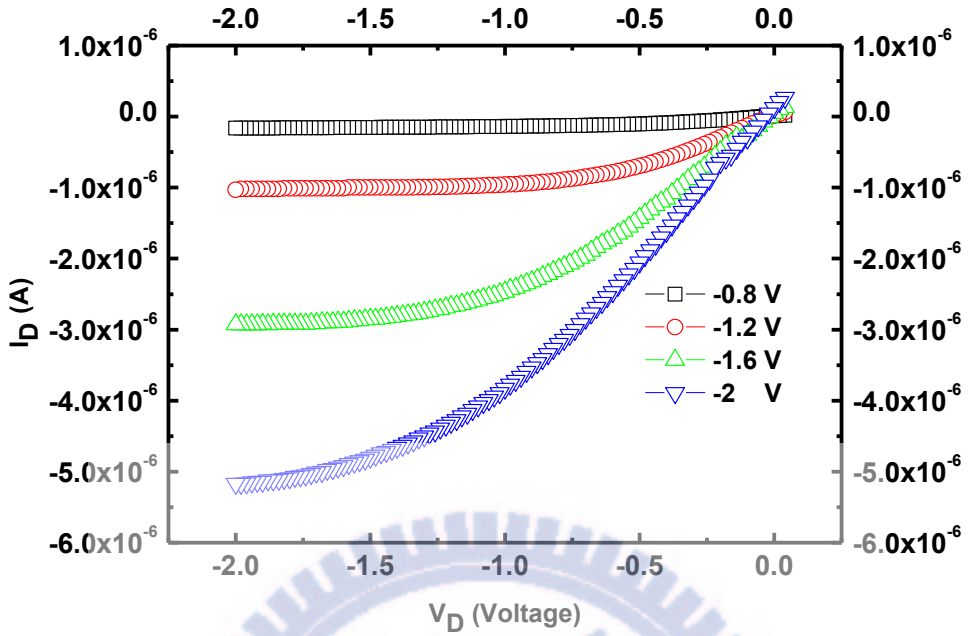


Figure 3-3 Output characteristics (I_D-V_{DS}) of OTFTs.

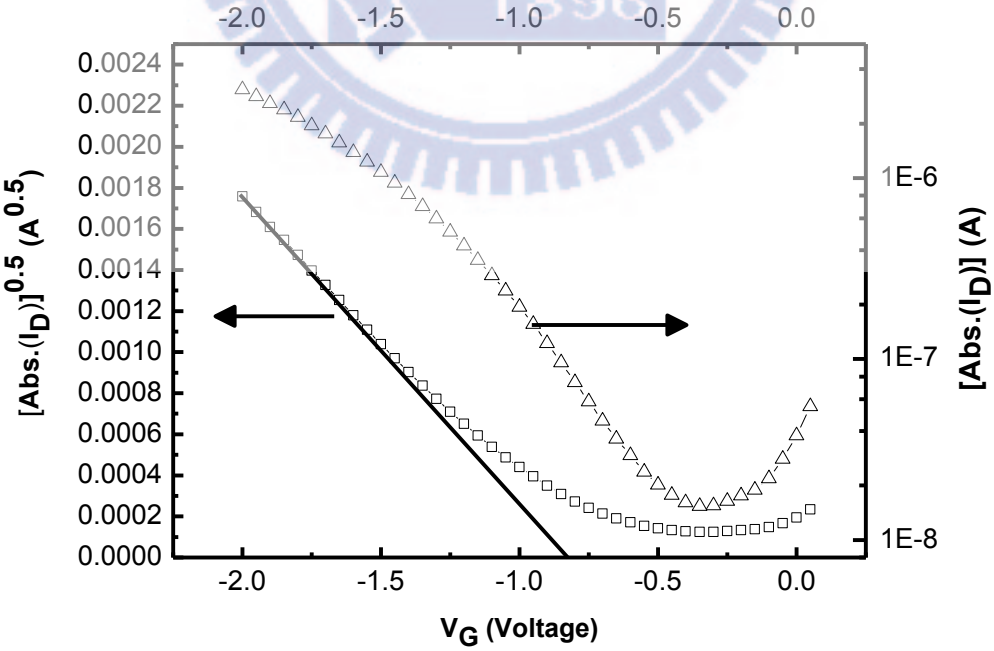


Figure 3-4 Transfer characteristics (I_D-V_G) and $|I_D|^{1/2}$-V_G of OTFTs.

Table 3-1：Comparison of this work with other researches about the characteristics of OTFTs fabricated at low temperature processes or operated at low voltage.

	Gate oxide material	Deposition method	Processes temperature (^{o}C)	Leakage current density (A/cm^2) at 0.5 MV /cm	Operation voltage (V)
Ref. [1] H. W. Zan et al.	AlN 2007 Organic Electronic	Sputter	150^{o}C	1E-8	-5
Ref. [2] Carmen Bartic et al.	Ta_2O_5 2002 Organic Electronic	E-gun	---------	1E-7~1E-8	-3
Ref. [3] F. C. Chen et al.	Nanocomposite 2004 Applied Physics Letters	spin	200 ^{o}C	1E-6~1E-7	-40
Ref. [4] Aber Chin et al	HfLaO 2008 IEEE	E-gun	350^{o}C	1E-7~1E-8	-2
In this work	Silicon oxide	APPJ	150 ^{o}C	2.53E-8	-2

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Chapter 4 The Investigation of Electrical Characteristic Dependent of Surface Hydrophobic Treatment

4-1 Introduction

In order to improve the performance of OTFTs, there are many methods could be used. You could improve about gate insulator quality, or the ordering of organic semiconductor material, contact resistance and so on. After we successfully deposited high quality silicon oxide, we could used surface treatment on the silicon oxide to improve ordering of active layer. However, the leakage current was increased after surface treatment. Therefore, we would discuss the influence of the surface treatment on leakage current in this section.

An appropriate hydrophobic treatment of gate insulator is the most general method to improve the mobility of OTFTs because the surface treatment could improve the molecular ordering of organic material [1-3]. In addition, after an appropriate surface treatment, the grain size of pentacene could become larger and the number of grain boundaries could be reduced, which could increase the mobility of OTFTs [3].

Leakage current would distort the electric characteristics and increase the power consumption of OTFTs. In general, the main leakage current of OTFTs consist gate leakage current and channel leakage current. Gnade et al. [4] had indicated that the positive drain leakage current of OTFTs, most came from non-channel leakage, would be reduced by patterning the active region of OTFTs.

Most researches of OTFTs often operated in high voltage because the thicker gate insulator could be used to suppress gate leakage current. However, the high operation voltage is not suitable for the portable applications of OTFTs because the active power consumption would be very large. Nowadays, the low operation voltage studies

are less and especially fabricated with low temperature processes. A high quality gate insulator fabricated with low temperature processes was urgent for OTFTs to reduce gate leakage current and power consumption. Therefore, how to reduce the static leakage current would be a problem in the development of OTFTs.

we analyzed the leakage current of OTFTs fabricated with and without a hydrophobic treatment of gate insulator. We found that the I_G and static source-drain leakage current would be increased after a hydrophobic treatment. In general, most researches only indicated the advantages of the surface treatment on gate insulator but did not point out the influence of surface treatment on leakage current. We would present the experimental results and discuss the reasons.

4-2 Experiment

All OTFTs were fabricated on silicon substrates with top contact structure, as shown in Fig. 4-1. A 30 nm silicon oxide thin film was grown with thermal dry oxidation at 950 ^{o}C as a gate insulator. Some samples were treated with HMDS by atmospheric pressure plasma. Following surface treatment, an active P3HT layer was spun-coated at 1500 rpm for 35s and baked on a hot plate at 130 ℃ for 3 min. The P3HT (with more than 98.5 % head-to-tail linkage) and highly pure solvent (xylene) were obtained from the Aldrich Chemical Company. Solutions of P_3HT in xylene were made with a weight concentration of 0.3 %, and filtered through a 0.2 μm pore PTFE filter. The source and drain electrodes, with a 60 nm thick Ni layer were deposited using E-gun apparatus. The channel length (L) and width (W) were 500 and the 2000 μm , respectively.

4-3 Results and Discussion

In our previous studies, we focused on surface treatment on gate insulator of OTFTs by HMDS. Figure 4-2 shows the transfer characteristics of OTFTs fabricated with various surface treatment. On current was increased obvious after various surface treatment. Table I shows the comparison of OTFTs with different surface treatment. Mobility and threshold voltage were improved with increasing contact angle. Larger contact angle indicated the surface of gate insulator was more hydrophobic which could increase the ordering of organic semiconductor molecular.

Figure 4-3 presents the UV-vis absorption spectra in the region of the π-π* absorption regioregular P_3HT. The figure shows that after the surface has been modified by APPJ, the absorption peak at 610 nm becomes stronger, also indicating increase in chain extension and chain alignment. Although the ordering could be improved after a surface treatment off current was also increased obviously.

However, we also could found the leakage current of OTFTs also was increased after surface treatment. Therefore, OTFTs fabricated with and without surface treatment were used for analyzing. Figure 4-4 (a) shows the I_{DS}-V_{DS} of OTFTs with and without surface treatment of gate insulator. Leakage current of OTFTs, mainly consists of gate leakage current and source-drain leakage current, has been studied in references [4]. The leakage current at V_{DS} = 0 V of the Figure 3-4 (a) was mainly contributed from gate leakage current because the positive I_{DS} leakage was cause by negative V_{GS} bias. The gate leakage current flows from drain electrode through active layer and gate insulator to silicon substrate which was shown in Figure 4-4 (b). However, when the drain voltage become more negative, the electric filed between drain and gate are decreased, and I_{DS} gradually turns to negative. Figure 4-5 (a) shows the I_{DS}-V_{GS} of OTFTs with and without surface treatment of gate insulator. Figure 4-5

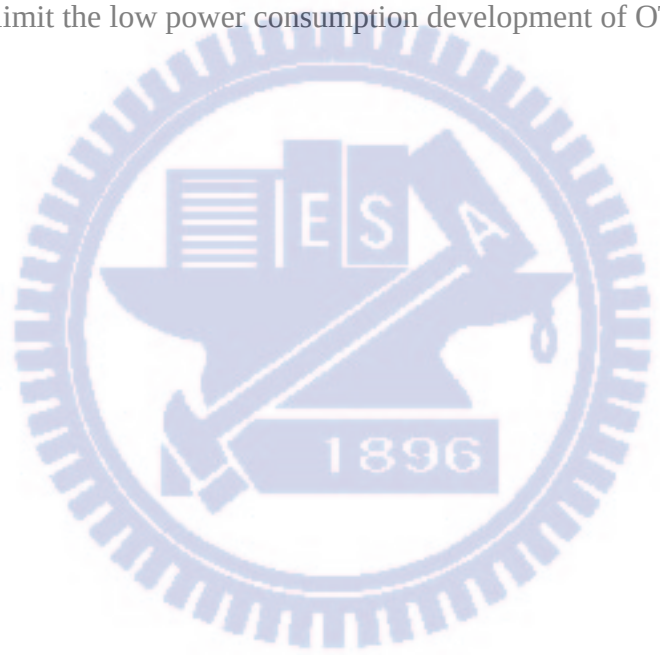
(b) shows static state condition of OTFTs which means V_G = 0 V and V_{DS} at high operation voltage. The analysis of I_G was shown in Figure 4-6 (a). After a surface treatment of gate insulator, I_G was increased. The measurement condition was shown in Figure 4-6 (b) which floating the drain electrode could avoid the influence of drain current. Many researches indicate that the ordering of organic semiconductor material would be improved when deposited on a hydrophobic treated gate insulator surface [2], [3]. We regard that the good ordering of organic material has higher mobility and this would decrease the resistance between drain and gate insulator, which could increase the gate leakage current. The mobility of OTFTs with and without surface treatment are 0.004 (cm^2/V-s) and 0.0023 (cm^2/V-s) respectively.

Figure 4-7 shows the output characteristics of OTFTs with and without defined active layer. The patterning active layer could suppress gate leakage current because the total leakage current area can be effectively decreased. The gate leakage current would be decreased with a patterned active layer and get high performance OTFTs. Using a thick thermal oxide could suppress gate leakage current but increased the operation voltage adversely. Moreover, the high thermal budget of thick oxide deposition was not suitable for flexible substrate. A high quality and low temperature processed gate insulator was necessary for OTFTs because it could decrease the gate leakage current and keep the good electrical characteristics of OTFTs.

On the other hand, I_{DS} measured at V_G floated was also increased obviously after surface treatment of gate insulator which was shown in Figure 4-8. V_G was floated to avoid the influence of gate leakage current on I_{DS}. When the channel resistance of OTFTs is comparable to the low schottky barrier of source-drain contact, the schottky contact could not effectively suppress the source drain leakage current, and the source drain leakage current would be increased with the decreased total resistance especially when the channel length was scaled down.

4-4 Conclusions

Surface treatment on gate insulator would improve the mobility of OTFTs because the ordering of organic material got better. However, the static leakage I_G and I_{DS} were also increased with the improvement of the order of organic material. Although the gate leakage current could be reduced by a high quality gate insulator and patterned active layer, static leakage current I_{DS} would still not be reduced. I_{DS} would be increased with the decreased channel length and more conductive channel at Off-state. These facts may limit the low power consumption development of OTFTs.



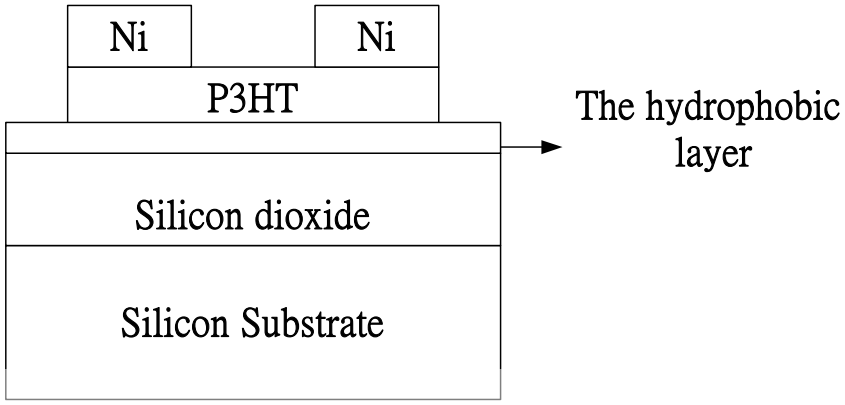


Figure 4-1 A cross-section plot of a top contact OTFT with surface treatment of gate insulator.

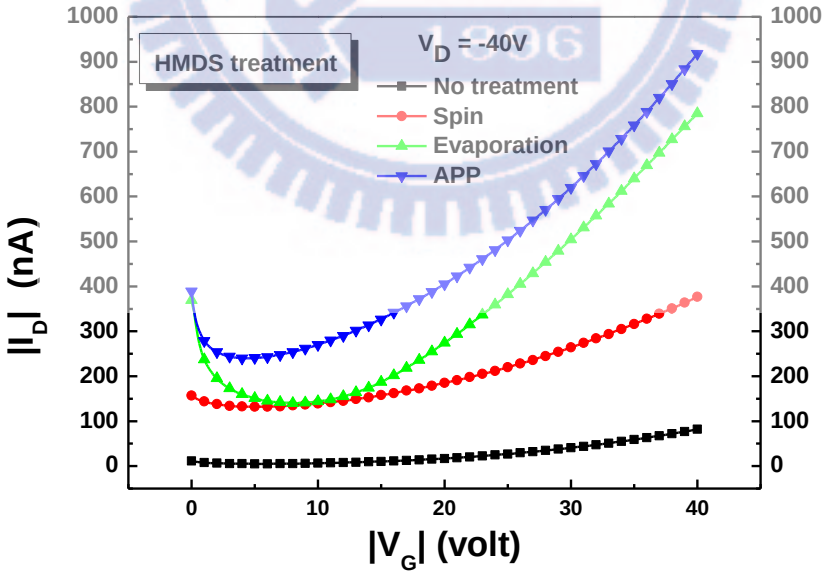


Figure 4-2 Transfer characteristics of OTFTs fabricated with various surface treatments.

TABLE 4-1. Electrical parameters of the OTFTs in this study.

Surface treatment	Contact angle	Surface roughness (nm)	Threshold voltage Vth (V)	Mobility μ_{sat} (cm^2/Vs)
No treatment	＜10°	1.58	-21.7	1.9×10^{-3}
Spin-coating	65.5°	0.895	-9.5	7.8×10^{-3}
Evaporated	75.3°	0.890	-12.0	2.2×10^{-2}
APP	90.5°	6.07	-8.3	2.6×10^{-2}

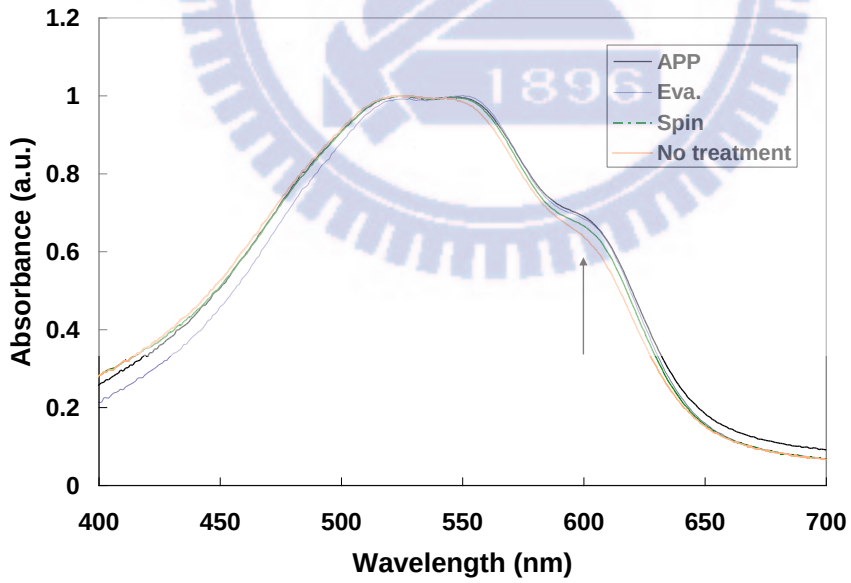


Figure 4-3 UV-vis absorption spectra of P_3HT films that are deposited on SiO_2 dielectric layers following various surface treatments , normalized to the maxima of the spectra.

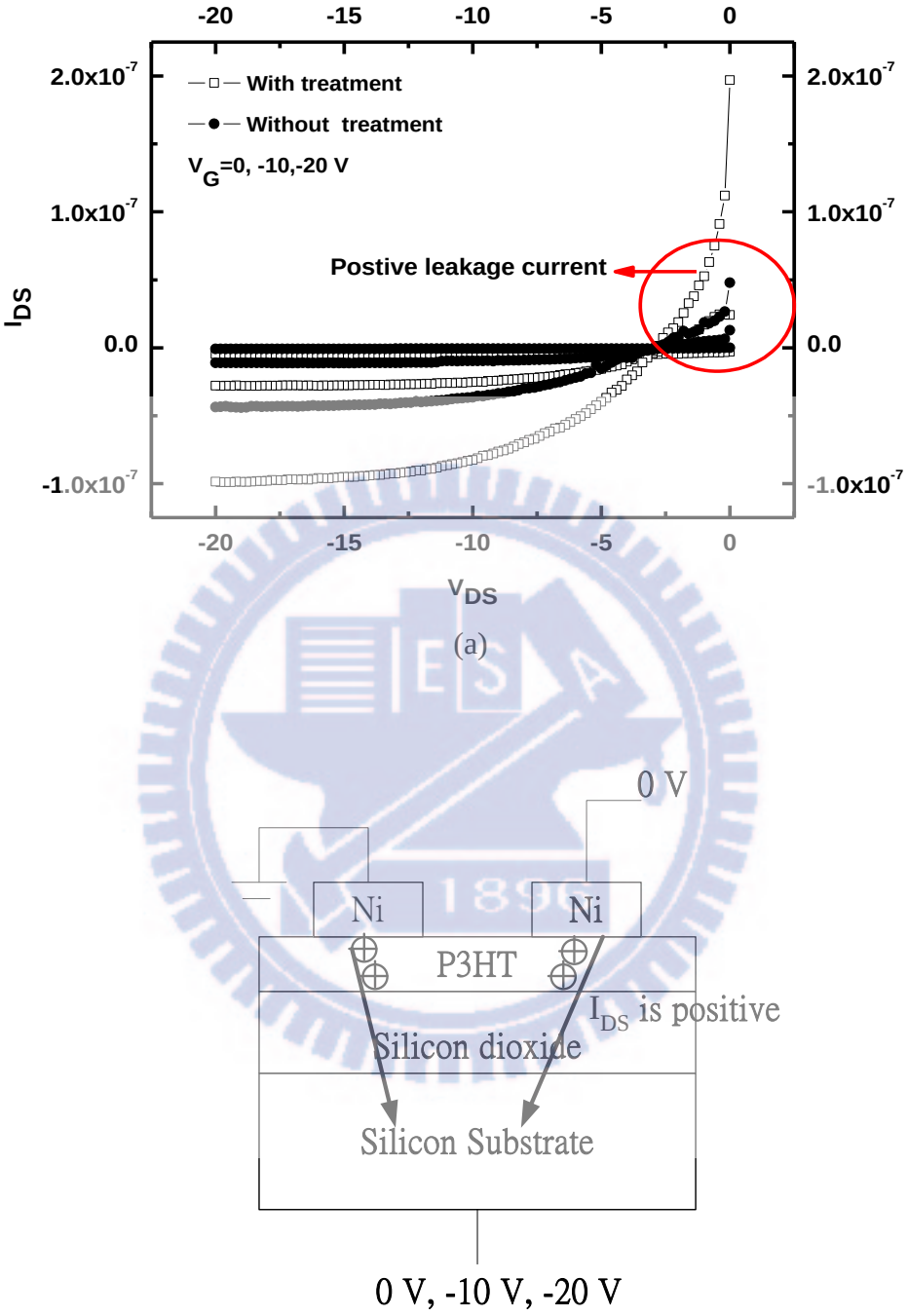


Figure 4-4 (a) I_{DS}-V_{DS} of OTFTs with and without surface treatment without patterning the active region. (b) A diagram of holes moving direction at source and drain are zero voltage.

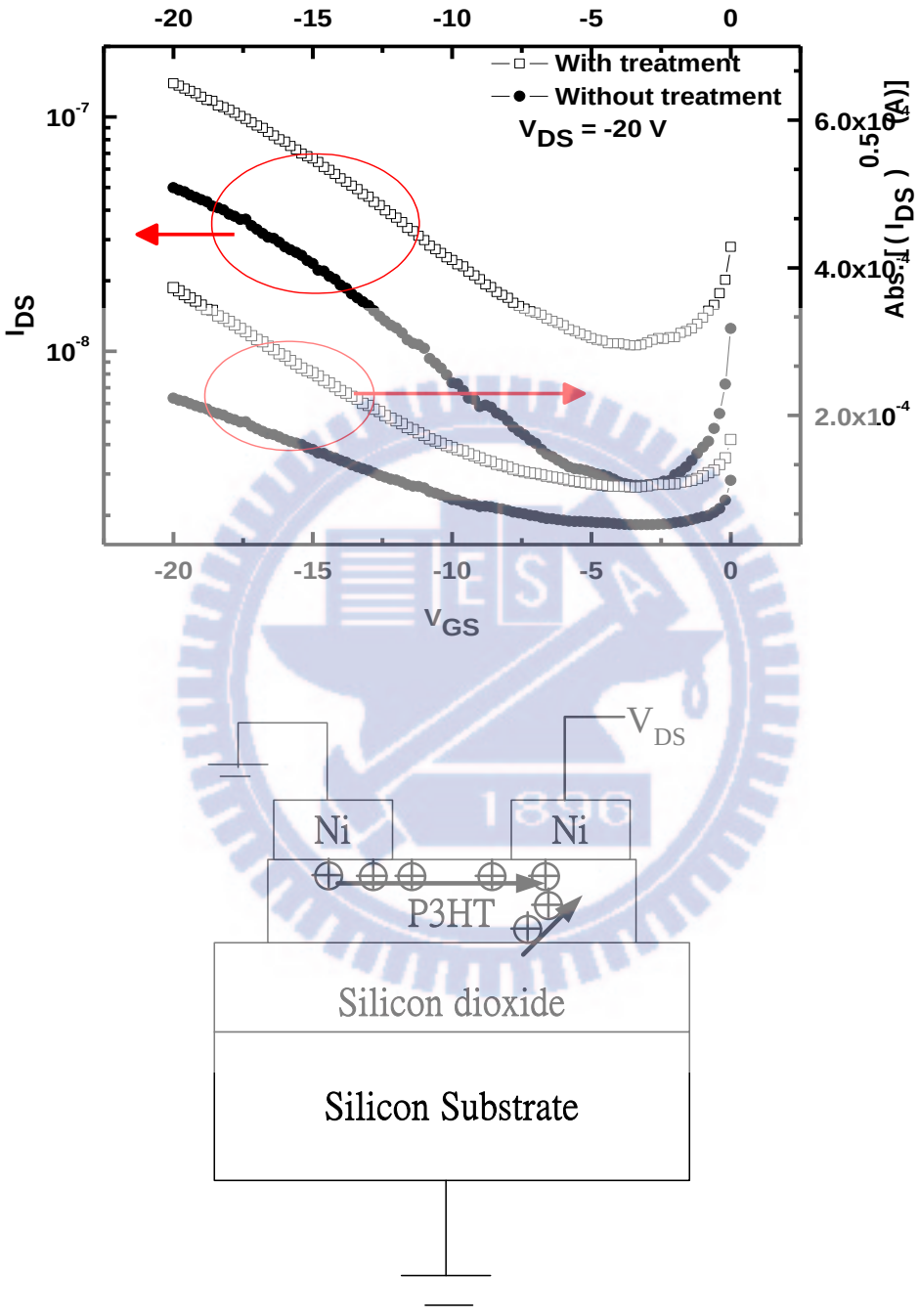


Figure 4-5 (a) I_{DS}-V_{GS} of OTFTs with and without surface treatment without patterning the active region. (c) A diagram of holes moving direction when an OTFT was at static state.

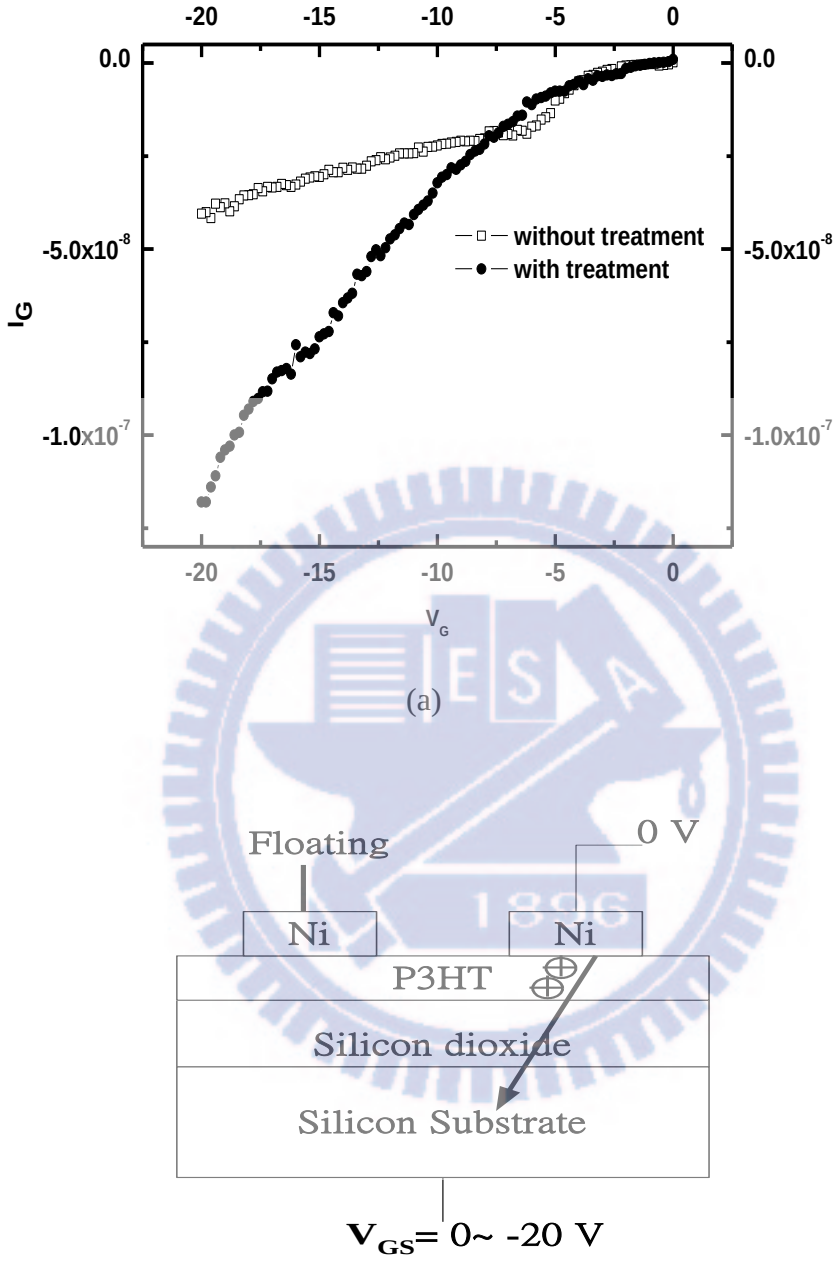


Figure 4-6 (a) I_G versus V_G of OTFTs with and without surface treatment when source is floating. (b) The measurement condition and hole moving direction of the OTFT.

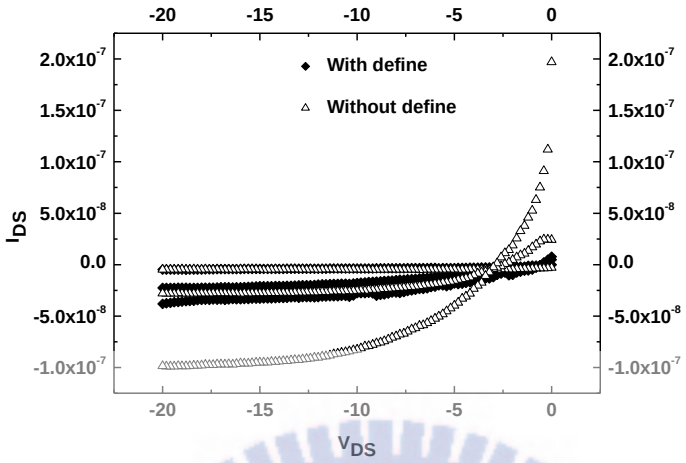


Figure 4-7. I_{DS}-V_{DS} of OTFTs with and without patterning active region after surface treatment.

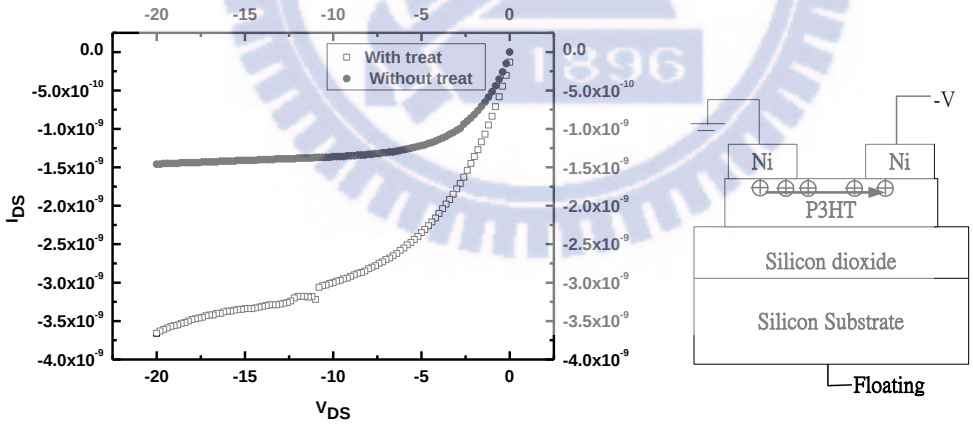


Figure 4-8 I_{DS}-V_{DS} of OTFTs with and without surface treatment when the gate is floating.

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Chapter 5 Conclusions and Future work

5-1 Conclusions

A high quality and low temperature silicon oxide was successfully deposited by APPJ and integrated for low operation voltage OTFTs. We used MIM structure to determine the quality of silicon oxide. In addition, AFM, SEM, and XPS were used for analyzing surface roughness, pellets, and components. Leakage current of our proposed silicon oxide was about 2.5 E-8 (A/cm^2) at 0.5 MV/cm and the breakdown voltage is about 8 MV/cm which could be compared with other researches. In addition, using APPJ to deposit silicon oxide has a lot of advantages in processes which include low temperature processes, low cost, large area deposition. In order to overcome the high operation voltage of OTFTs, our demonstrated silicon oxide was only about 10 nm and used as gate insulator of OTFTs. Our proposed OTFTs shows a lower operation voltage about -2 V, a lower threshold voltage about -0.8 V, a good mobility 0.66 cm^2/V-s, and a good subthreshold swing about 700 mV/decade.

In the first instance, we discovered the active energy is higher when silicon oxide is deposited on metal at room temperature. Then, we increased temperature up to 150 ^oC to overcome the active energy. If you want to deposit silicon oxide at room temperature you could form a thin silicon or silicon oxide film on the metal surface to decrease the active energy. However, this method may be difficult and complex so increasing temperature up to 150 ^oC is suitable for applications of OTFTs. We well controlled the carrier gas's flow rate to avoid deposition condition transferring to homogeneous reactions. When we used lower flow rate to deposit silicon oxide we could control the deposition condition at heterogeneous reactions which could decrease the formation of pellets. In addition, higher flow rate of carrier gas would

cause more carbon impurity which would decrease the quality of silicon oxide and increase much pellets on the surface of silicon oxide. Gap distance would influence the concentration of reaction species on the surface of sample. An appropriate gap distance could decrease the plasma bombardment, reduce leakage current density, and reduce surface roughness.

Silicon oxide, deposited by oxygen main gas, got the fastest deposition rate because oxygen has better ability to decompose TEOS vapor. However, the faster deposition rate may decrease the denseness of silicon oxide and generate higher leakage current density. However, silicon oxide deposited with CDA main gas has the best quality but the deposition rate is the slowest. The oxygen percentage of CDA is about 20 % which is much higher than nitrogen, but the deposition rate of silicon oxide deposited with CDA is the slowest. It may due to that the higher oxygen percentage in nitrogen plasma has strong electronegativity which may decrease the electron density of plasma. Because oxygen and nitrogen main gas would cause higher deposition rate the pellets of silicon oxide was also increased. We got good quality silicon oxide by well controlling temperature, flow rate, gap distance, main gas.

we well controlled the temperature and carrier gas's flow rate to avoid deposition reaction transferring to homogeneous reactions.

Surface treatment on gate insulator would improve the ordering of organic semiconductor material which could increase the mobility of OTFTs. However, the static leakage I_G and I_{DS} were also increased with improving the ordering of organic material. Although the gate leakage current could be reduced by a high quality gate insulator and patterning active layer, the static leakage current I_{DS} would still not be reduced. I_{DS} would be increased with decreasing channel length and more conductive channel at Off-state. These facts may limit the low power consumption development of OTFTs.

5-2 Future work

(1) Low temperature treatment of silicon dioxide

We used APPJ to deposit high quality silicon oxide at low temperature and the leakage current of silicon oxide in MIM structure was about 2.53E-8 A/cm^2 which could be compared to other studies. Silicon dioxide deposited by APPJ was not proceed any thermal or plasma treatment. UV-ozone may be used as a low temperature treatment approach for silicon dioxide to improve the film quality.

(2) Processes of OTFTs were all used APPJ

Using APPJ to deposit electrodes and active layer of OTFTs could achieve low cost and large area application.

(3) Optimization and reliability engineering of APPJ-processed SiO_2 OTFTs

We could optimize the contact resistance, channel resistance, and gate leakage to improve performance of low-voltage OTFTs.

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博士論文題目：

中文：以噴射式大氣電漿技術在低溫下開發高品質二氧化矽應用在低電壓操作之有機薄膜電晶體之研究

英文：High-Quality Silicon Dioxide Developed by Atmospheric Pressure Plasma Technology at Low Temperature was Applied for Low-Voltage OTFT