國立交通大學

電子工程學系 電子研究所

博 士 論 文

系統單晶片整合應用之

超寬頻基底耦合雜訊抑制技術

An Active Guarding Technique for

Wideband Substrate Coupling Noise Suppression in SoC Applications

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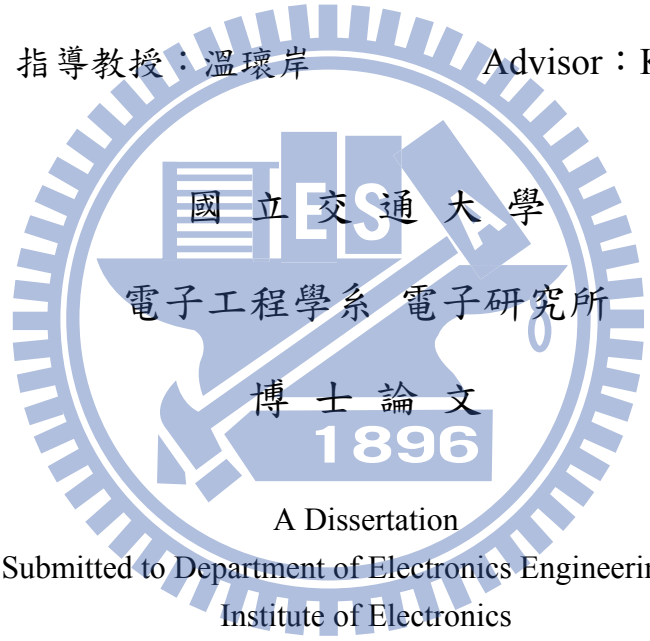

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摘　　要

本論文針對現今快速發展的系統單晶片(SoC)趨勢，提出了一個可抑制基底耦合雜訊之超寬頻主動保護電路技術。本技術主要包含兩部份：一、雜訊去耦以及偵測機制：此機制提供一低阻抗路徑以將部份基底雜訊去耦合，同時偵測此去耦合之基底雜訊大小。此訊號可再被利用為下級產生前饋抵消剩餘基底雜訊之來源。二、前饋反向訊號以抵消基底雜訊機制：此機制將前級獲得的去耦合基底雜訊訊號反向，並做適當大小調整後重新注入基底以抵消剩餘的基底雜訊。此機制中並包括了一個頻率補償電路，提供系統新的零點以及極點，以增加電路有效頻寬。

除提出本電路技術外，本論文還以 UMC90 奈米製程技術為例，對五種常見之被動式基底雜訊隔絕方式做特性描述與比較，並得到基底模型以提供此電路技術設計時使用。此電路最終使用 UMC90 以及 UMC180 奈米製程下線實作並經量測後所得效能如下：在 1GHz 之工作頻率以下可以提供至少 14dB 之雜訊抑制能力，並且一直到 20GHz 時都仍可提供 11dB 以上之雜訊抑制能力。此電路核心所佔面積僅為 800 平方微米，並在 1.8 伏特之電源供應下消耗 2 毫安之電流。此電路技術將隨著製程的發展而有著更小的面積需求以及更小的功率消耗，同時有效工作頻寬也會提升。

此外，為證明此電路技術的確可實際應用於單晶片系統上，我們將此電路技術與一振盪頻率為 1GHz 之電感-電容振盪器整合於單晶片上，並實驗觀察此振盪器在有基底雜訊時，被此電路技術保護及未被保護時的相位雜訊與突波大小差別。實驗結果顯示，在 10kHz 與 10MHz 之單頻低頻基底雜訊注入時，此電路可在此振盪器相對頻率之相位雜訊上分別提供 18.81dB 與 16.73dB 的突波抑制能力。而當注入接近振盪頻率之多頻基底雜訊時，此電路技術亦經實驗證明可在寬頻範圍內同時抑制多頻基底耦合雜訊，大幅提升振盪器之相位雜訊效能。

An Active Guarding Technique for Wideband Substrate Coupling Noise Suppression in SoC Applications

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ABSTRACT

In this dissertation, an active guarding technique is proposed for wideband substrate coupling noise suppression in SoC applications. A noise decoupling mechanism is developed to provide a decoupling path and to sense the noise level for generating noise cancellation current. A feed-forward compensation mechanism is also developed to extend the noise suppression bandwidth and to adjust the amplitude of phase-inversed noise cancellation current by introducing a zero and an amplitude controller. Substrate characterization on UMC 90nm CMOS technology is also done for substrate network modeling and for the design parameters' determination of decoupling factor and the amplitude of noise cancellation current.

Experimental results in UMC 180nm CMOS technology show that more than 14dB noise suppression performance is achieved in a wide frequency range from DC to 1GHz and 11dB until 20GHz, by the cost of a small chip area of 20μm x 40μm and 2mA current consumption from a 1.8V supply. To be mentioned, the active guarding circuit benefits better performance and lower power consumption as the technology scaling down; thus is suitable for future applications of highly integrated SoC designs. To prove the feasibility on real applications, the proposed active guarding technique is demonstrated for substrate immunity improvement on LC-tank oscillators. Experimental results also show that by applying the active guarding technique to a LC-tank oscillator, more than 16.73dB spur suppression performance is obtained in the frequency range of interest as either low frequencies below 10MHz or high frequencies around the resonant frequency of 1GHz.

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趙晧名

2013 年 3 月

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Chapter 1

Introduction

During the past years, a trend of higher level integration as system-on-chip (SoC) design has grown enormously, driven by the advancement of the continuous down-scaling CMOS technologies. Multifunctional chip of heterogeneous designs such as digital, analog, RF, embedded memory, microprocessor and DSP are integrated at ever-closer distances in a shared substrate to fulfill the requirement of various applications. On the other hand, for the modern technologies and applications, lower supply voltage in combination with higher frequency operation in wireless integrated circuits (ICs) result in more reactive and resistive impedance nodes in analog circuitry that are very sensitive to noise transients originated from the substrate. As a result, a problem of signal integrity degradation arises due to the insufficient isolation between noisy digital circuits and sensitive analogue circuits. In this thesis, we are going investigate the substrate coupling noise issue in modern mixed-signal ICs.

1.1 Evolution of integrated circuits

ICs were made possible by experimental discoveries showing that semiconductor devices could perform the functions of vacuum tubes and by mid-20th-century technology advancements in semiconductor device fabrication. The integration of large numbers of transistors into a small chip was an enormous improvement over the manual assembly of circuits using discrete electronic components. The integrated circuit's mass production capability, reliability, and building-block approach to circuit design ensured the rapid adoption of standardized integrated circuits in place of designs using discrete transistors. [1]

It was in 1947, with the invention of the transistor by Bell Telephone Laboratories, the huge and power consuming vacuum tubes were replaced. Transistors were miniscule in comparison, more reliable, longer lasting, produced less heat, and consumed less power. The invention of transistor stimulated engineers to design ever more complex electronic circuits and equipment containing hundreds or thousands of discrete components such as transistors, diodes, rectifiers and capacitors. But the problem was that these components still had to be interconnected to form electronic circuits, and soldering thousands of components to thousands of bits of wire was expensive, time-consuming, also unreliable since every soldered joint was a potential source of trouble. The challenge was to find cost-effective, reliable ways of producing these components and interconnecting them. However, although those transistors were much smaller, faster and less power consuming than vacuum tubes, circuit based on individual transistors became too large and too difficult to assemble.

In 1958, Jack Kilby in Texas Instruments came out of the initial ideas concerning the integrated circuit and successfully demonstrated the first working integrated circuit made of germanium. About half year later, Noyce at Fairchild Camera, also came up with his own idea of an integrated circuit. Produced at Fairchild Semiconductor, it was made of silicon. From then on, the new revolution of electronics industry began [2].

1.2 Trend of System-on-Chip Design

After around 40 years of the invention of integrated circuits, a new trend called System-on-Chip (SoC) design began. A SoC design is an IC that integrates many components of a complex electronic system into a single chip. It may contain digital, analog, mixed-signal, and often radio-frequency functions; all on a single chip substrate. A general example of SoC chip is shown in Figure 1.

As the number of components per chip increases, the total chip size has to be contained

within practical and affordable limits. This can be achieved by a continuous downscaling of the critical dimensions in the integrated circuit, which can be expressed in terms of Moore's Law [3] as a scaling by a factor of 0.7 every 2 years. As a consequence of this trend, the miniaturization of circuits by scaling down the transistor has been the principal driver for the semiconductor technology roadmap, for more than 40 years. Thanks to its ability to dramatically decrease the cost per elementary function; for example the cost per bit for memory devices, or cost per million instructions per second (MIPS) for computing devices, we can enjoy the electronic devices with more and more functions with an almost fixed (even lowering) cost. In short, the industry ability to follow "Moore's Law" has been the engine of a virtuous cycle; through transistor scaling, one obtains a better performance to cost ratio of products which induces an exponential growth of the semiconductor market. This in turn allows further investments in new technologies which will fuel further scaling.

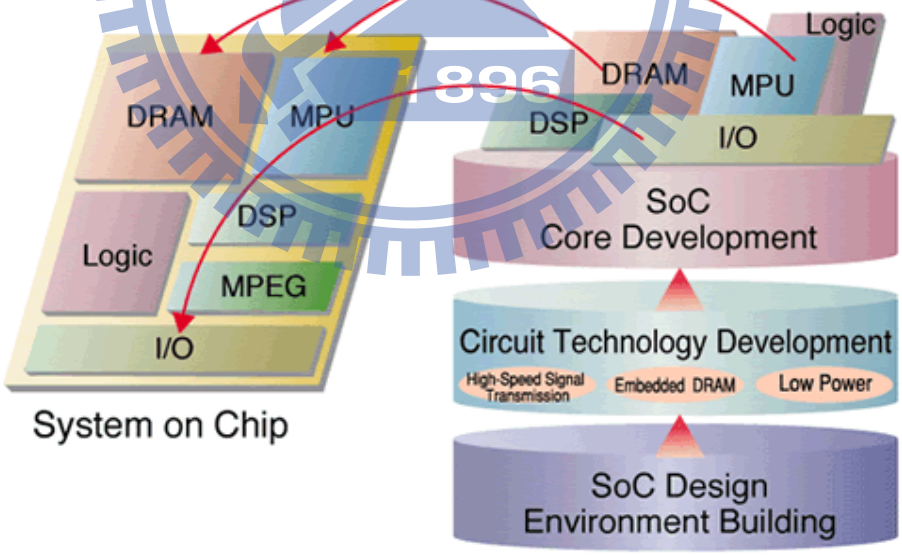


Figure 1 Example of a SoC chip

1.3 Signal Integrity Problem

As mentioned in last section, for the trend of SoC design, multifunctional chip of

heterogeneous designs such as digital, analog, RF, embedded memory, microprocessor and DSP are integrated at ever-closer distances in a shared substrate to fulfill the requirement of various applications, as shown in Figure 1. However, such integration causes signal integrity degradation due to the insufficient isolation between noisy digital circuits and sensitive analogue circuits. Fast switching signals generated by digital circuits introduce current spikes coupling through the shared substrate into the sensitive analogue and RF circuits, and then adversely affect their performance, as indicated in Figure 2. Researches of various respects have been investigated to alleviate this problem including substrate coupling mechanism and modelling [4]-[12], substrate coupling effects on analogue circuit performance [13]-[33] and substrate coupling reduction techniques [34]-[47]. Accurate modeling and analyzing of substrate coupling is prerequisite to evaluate the impacts of substrate coupling noise; it also provides parameters for some substrate noise reduction circuit designs.

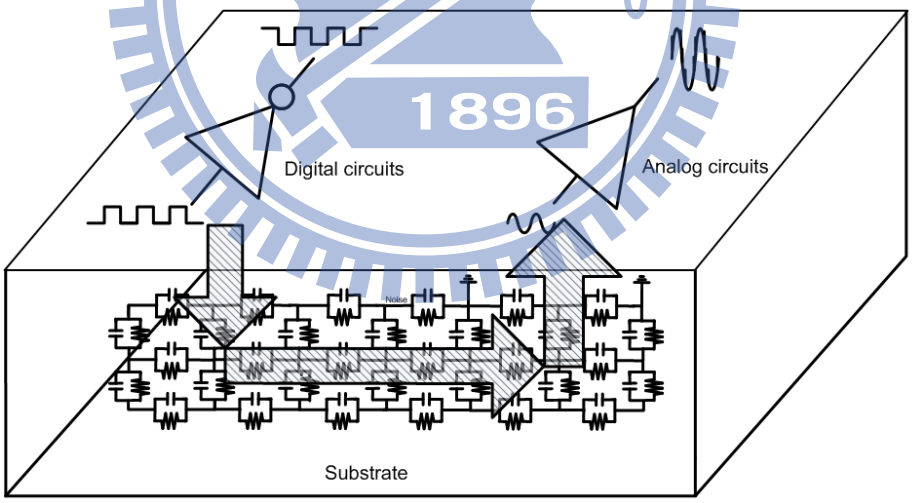


Figure 2 Switching noise can couple from digital circuits to the analog circuits through the common substrate.

1.4 Outline of this work

The target of this work is to investigate the generation / propagation of substrate coupling in modern CMOS technologies; to build up a simulation environment for substrate

coupling noise prediction and finally to figure out a new solution that can effectively alleviate the substrate coupling noise problem in modern mixed-signal SoC designs.

This thesis will be organized as follows: Chapter 2 discusses the substrate noise issue in mixed-signal circuits, which mainly talks about the generation, propagation of substrate coupling noise and also the substrate coupling noise impact on analog/mixed-signal/RF circuits. In Chapter 3, previous techniques for substrate coupling noise suppression are introduced, classified as passive and active methods. Substrate characterization is done in this work to find out and compare the isolation abilities of conventional guard rings, Substrate networks are also extracted in this process for future utilizations. In the end, we will propose an active guarding technique for substrate coupling noise suppression that combines the advantages of both passive and active methods. Chapter 4 presents the details about the active guarding technique, which includes the design, analyses, implementation and experimental results of active guarding circuits. In Chapter 5, the proposed active guarding technique is implemented on a LC-tank oscillator to verify the feasibility in real applications. Finally, Chapter 6 gives the conclusions and future works.

Chapter 2

Substrate Noise in Mixed-Signal Integrated Circuits

2.1 Introduction

Continuous down-scaling of CMOS technology has led VLSI design to “System-on-Chip” (SoC) design, a mixed-signal single chip solution for both digital and analog circuits. However, such integration causes substrate coupling noise which results in the degradation of signal integrity. Digital switching noise couples through the parasitic capacitance of substrate and then corrupts sensitive analog circuits. This problem becomes more and more critical as the supply voltage decreases, the operation frequency increases, and also when the more densely the components are placed on a chip. The substrate noise problem in mixed-signal ICs is going to be discussed here by three classified topics as: the noise generation mechanisms, the propagation mechanisms and the impact on analog/RF circuits.

2.2 Generation Mechanisms

2.2.1 Impact Ionization

When a MOS device is biased in saturation region, a high electric field in the depletion region of the channel is formed close to the drain node. Due to this high electric field, the channel carriers are accelerated and gain enough energy to generate electron-hole pairs by scattering in the crystal lattice. The electrons are subsequently swept into the drain, but the holes flow through the substrate and are collected by the P+ substrate contacts connected to

GND or VSS, causing a current generation. For NMOS transistors, the generated holes are swept to the substrate generating a drain-to-substrate impact ionization current. This current produces IR drops on the substrate resistance which appear as dynamic voltage variations in the substrate. While in PMOS transistors, the magnitude of the generated current is about an order smaller than the impact ionization current generated by the NMOS transistors due to the lower hole mobility.

In addition, PMOS transistors are physically situated in a N-well, which tend to reduce coupling of currents to the surrounding p-type substrate due to its capacitive impedance. Thus it is expected that PMOS devices cause / suffer from lower substrate noise than comparably sized NMOS devices. This phenomenon is insignificant in older technologies but should be considered in deep-submicron CMOS processes [7], [8]. However in general, it remains as a minor role among substrate noise sources because the power supply/ground noise and capacitive coupling are normally much larger since they increase with scaling [9].

2.2.2 Capacitive Coupling

There are two types of coupling paths: The first is capacitive coupling through PN-junctions capacitors; the second is capacitive coupling of interconnects.

2.2.2.1 Junction Capacitances

Junction capacitances in CMOS circuits are at the source and drain nodes of transistors, where the P-N junctions are formed due to the reverse biasing. The reverse-biased P-N junctions form non-linear and voltage-dependent capacitors therefore create a capacitive coupling path to inject and receive substrate noise. This capacitance can be approximated to:

$$C = \frac{A}{\left[\frac{2}{q\varepsilon_{si}} V_{bi}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\right]^{1/2}\left(1-\frac{V_D}{V_{bi}}\right)^m} \qquad (1)$$

where A is the area of the PN-junction, V_{bi} is the built in voltage, and V_D is the voltage over the diode [10] . The doping levels for the p region and the n region are denoted as N_A and N_D, respectively. The gradient coefficient is denoted as m, q is the elementary charge and ε_{si} is the permittivity of silicon.

2.2.2.2 Interconnects

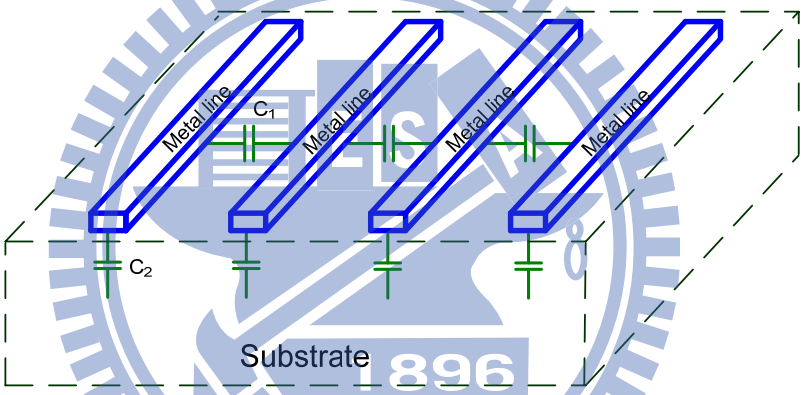


Figure 3 Capacitive coupling of adjacent interconnects

The on-chip interconnects are capacitively coupled to the substrate and adjacent interconnects as illustrated in Figure 3. The capacitive coupling between two interconnects and substrate are modeled with capacitors C_1 and C_2. This capacitive coupling of interconnects depends on the location of the metal lines, the length, width and the distance to other objects. For interconnects in the lower metal layers, the coupling is more serious to the substrate than interconnects in the upper layers.

2.2.2.3 Power Supply and Ground grids

Power supply and ground bounce noises are created when displacement currents flow through the parasitics associated with the power supply networks. The power distribution path includes on-chip metal lines, bond wires, package wires and pins and PCB tracks to the ideal power supplies; there is also mutual capacitance and inductance between lines. Parasitics associated with external ports (bond wires, package pins, board tracks, etc.) are typically modeled as lumped-elements of series inductances and resistances. An example of CMOS inverter with equivalent power grid and external ports' parasitics is shown in Figure 4. Simultaneous switching of digital gates produces transient current spikes which result in transient voltage drops in those inductive and resistive paths of supply lines. The voltage drops on the VDD and GND paths can be expressed by the following equation:

$$V_{drop} = RI + L\frac{dI}{dt} \qquad (2)$$

where R and L are relevant parasitics. Equation 2 shows the resistive and inductive voltage drops increase as the switching current increases and its first derivative increases, respectively. The second term, known as di/dt noise, also creates ringing in the parasitic RLC networks associated with power supply rails and output drivers [4]. Therefore, not only the local digital VDD and GND grids are not at their ideal voltages, but the grids in sensitive analog/RF parts in the same IC are affected due to the distribution of the coupled switching noise. If this ground grid is connected to the p-type substrate, this ground bounce will propagate directly to the substrate through ohmic contacts and parasitic junction capacitances. On the other hand, as the operating frequency increases with the technology shrinking, the di/dt noise increases; therefore, larger noise spikes will couple through the resistance of substrate contacts, the capacitance of metal interconnects and the reverse-biased junction capacitors and cause more serious substrate coupling noise problems.

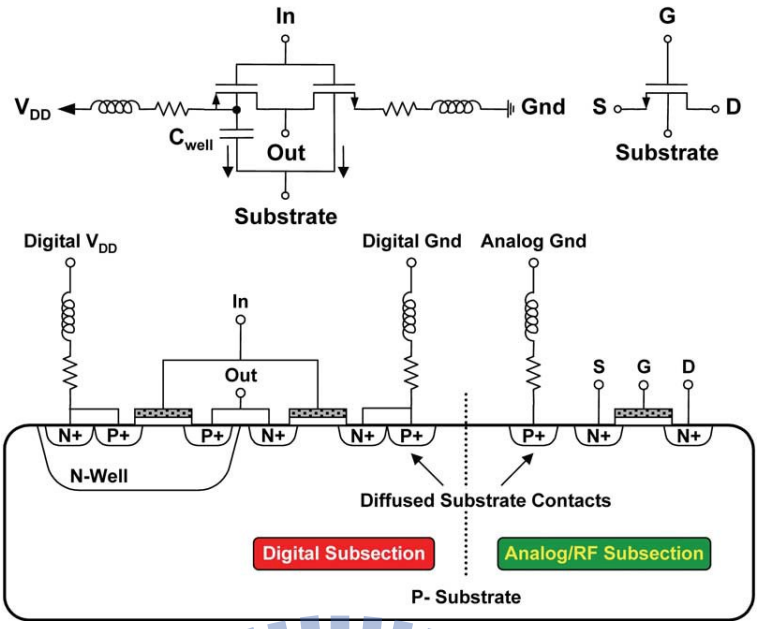


Figure 4 Switching coupling noise of an inverter to the analog/ RF parts in a IC through substrate [11].

2.3 Impact on Analog/Mixed-Signal/RF Circuits

Various researches have been done about the impact of substrate coupling noise on analog/mixed-signal/RF circuits, such as low noise amplifier (LNA) [15]-[18], voltage controlled oscillator (VCO) and phase lock loop (PLL) [19]-[25], analog-to-digital converter (ADC) [26]-[30], digital-to-analog converter (DAC) [31]-[33]. We will provide some survey on these.

2.3.1 Low Noise Amplifier

The influence of substrate noise coupling on the performance of a low-noise amplifier for a CMOS GPS receiver has been investigated both analytically and experimentally in [15]. It was shown that the spectral distribution of substrate noise greatly affects its impact in such a system. With the LNA as an example, both analysis and measurements indicate that substrate noise components located in specific frequency ranges can degrade the LNA performance.

As shown in Figure 5, the output spectrum of the LNA was measured under a 60dBm, 1.575GHz sinusoidal input. When a digital circuit emulator was activated with f_{clock} = 39.825MHz, $t_{rise/fall}$ = 0.9ns and fed to the substrate with a 32.6pF capacitor, the LNA output spectrum is seriously affected. It was proved in the paper that the noise tones are the results of digital switching noise at the harmonics of f_{clock} and the intermodulation (IM) between the 1.575GHz RF signal and the substrate noise at f_{clock} and its harmonics. It is also shown in the paper that the measured power of the largest IM tone in the LNA output is a function of the rise/fall time of the noise emulator, the substrate noise coupling capacitance value and the power of the substrate noise tone that causes this noise.

On the other hand, a frequency-domain approach has been presented in the paper to model both noise injections into the substrate from digital circuitry integrated on the same chip. The mechanisms about how that noise affects analog circuit behavior are also being presented. The results shown in this paper reveal that substrate noise can modulate the LNA input signal as well as couple directly to the amplifier's output.

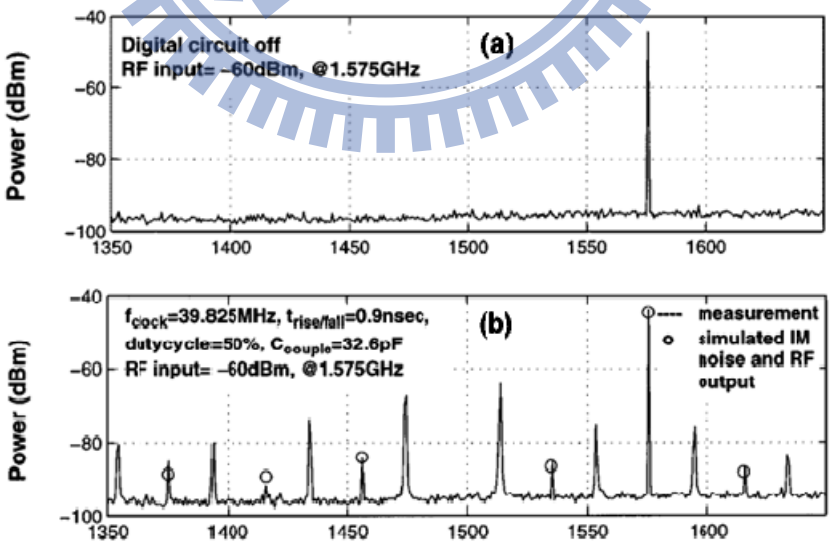


Figure 5 Measured LNA output spectrum: (a) without substrate noise injected. (b) with substrate noise injected. [15]

2.3.2 Oscillator

Oscillator is a very sensitive and common building block in a RF transceiver for the important role of generating the reference frequency for phase-locked loop. Substrate noise signal can couple to the oscillator and modulate the oscillator signal in both frequency and amplitude. This causes sideband spurs around the local frequency and its harmonics. Also, the noise signal can also directly couple to the output in a linear way without frequency modulation which also induces sideband spurs. Those sideband spurs around the local frequency degrade the phase noise performance of the oscillator thus is fatal to a wireless communication system.

Many papers have already been published to show the related issues of substrate noise effect on VCOs including [19]-[25]. Here we are going to show some important experiment results from them.

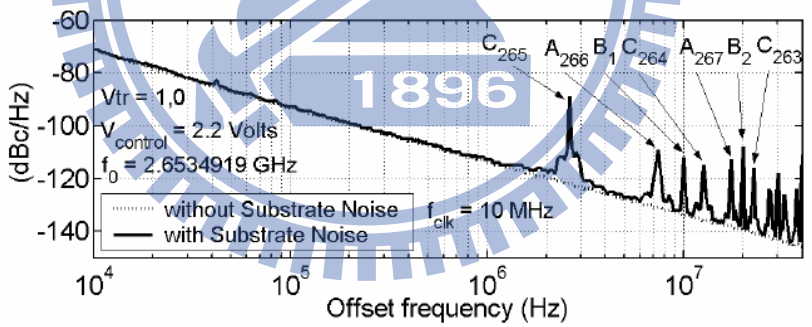


Figure 6 Differential output VCO phase noise degradation due to substrate noise. [20]

As presented in [20], a conventional 2.65 GHz differential LC-tank VCO and a digital circuit used as the substrate noise emulator with independent power supplies is fabricated on the same chip. When the on chip digital circuit is activated, the phase noise of the VCO degrades significantly. Figure 6 shows an example of this effect for a f_{clk}=10MHz. Many spurs appear at the sidebands of the oscillator fundamental frequency f_0 and destroy the phase noise performance. These spurs are originated from the substrate noise coupled to the analog

ground, then to each active devices and passives local substrate nodes in the VCO. The various spurs appearing in Fig. 6 are labeled according to its origin, classified as group A, B and C. For the spurs come from low frequency substrate noise harmonics up-converted from close to DC to close to f_0 due to indirect AM to FM modulation, they are classified as group B. For the spurs results from high frequency substrate noise harmonics converted from around f0 to phase noise sidebands, they are classified as group A and group C. Detailed analyses of the generation mechanisms of these groups can be found in the paper.

In short, it is proved that both noises at low frequencies and at high frequencies can significantly degrade the phase noise performance of a VCO. The low frequency substrate noise produces phase noise spurs at the output of VCOs due to resistive coupling between the injection point and the VCO ground followed by FM modulation. For the high frequency substrate noise harmonics, they result in additional spurs close to the VCO fundamental; the substrate noise harmonics around f_0 are transformed into phase noise at the VCO output due to mixing with the second harmonic of the differential pair output current.

2.3.3 Analog-to-Digital Converter

Modern wireless communication systems are developing rapidly in recent years in order to fulfill the demands for high speed data transformation as in WLAN, WPAN, UWB and multimedia experiences in portable devices as in 3G and 4G systems. The increase of bandwidth in those communication systems requires not only ultra high frequency radio frequency blocks, but also very high speed interfaces as ADCs and DACs. In this part, we are going to reveal the substrate coupling noise effect on ADCs from previous studies.

There are many different kinds of ADCs such as flash ADC, successive-approximation ADC, integrating (multi-slope) ADC, pipeline ADC, oversampling (sigma-delta) ADC, etc…among those architectures, there are always digital building blocks included. Therefore, as the

operation frequency demand for an ADC increases, the substrate coupling between the analog and digital building blocks becomes an important role that limits its performance. Studies had been done for the effect of substrate coupling noise issue on an oversampling ADC [27] and a flash ADC [28].

In [27], experimental results of the switching noise effect in an oversampling sigma-delta modulator are presented. A test chip is fabricated in 1μm CMOS technology including a third-order two-stage cascade modulator surrounded by eleven substrate noise emulators composed of tapered CMOS buffers that connected to the substrate via 6pF capacitors. The resulting substrate voltage fluctuations affect the transistors' threshold voltage via body effect and directly capacitive coupled into the transistors' gate, drain and source nodes in the modulator. The performance of the test circuit is evaluated by driving the analog input with a differential sinusoid, acquiring the 1-bit output code from each of the two stages, and transferring the acquired data to a work station for subsequent processing.

Figure 7 shows the experimental results of the output spectrum with and without the noise sources activated. The output spectrum with the noise sources off overlies the output spectrum with all of the noise sources activated. These measurements are taken with the rising edge of the noise clock occurring at the same time as the modulator sampling edge for a sinusoidal input level 10dB below overload. With no substrate noise, the SNDR and SNR are both 93dB. When the noise sources are activated, the SNDR and SNR drop to 52dB and 86dB, respectively. The performance decrease is due to the extra harmonics resulted from the injected substrate noise.

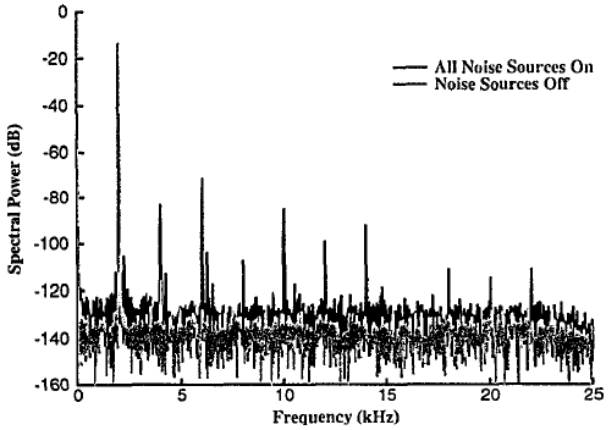


Figure 7 Output spectrum of a -10dB 2KHz input with/without noise sources activated. [27]

In [28], a 4-bit flash ADC is chosen to be investigated about the impact of substrate noise since normally the flash ADC can achieve highest operation speed among all types of ADCs. However, due to the highest possible operation speed, flash ADC also suffers from the substrate coupling noise problem most. Among the building blocks in a flash ADC, comparators are normally the most critical ones which limit the overall accuracy and speed. In order to test the impact of noise on the regeneration time or decision of individual comparator blocks, a comparator is used in a toggling test structure, configured in a positive feedback loop hence oscillates with half of the clock frequency. The outputs of the comparator are attenuated to the minimum resolution of the ADC before connecting them back to the inputs. In this structure, the variation in the regeneration time of the latch can be observed as jitter in zero-crossing points of the toggling output. In order to investigate this problem, a flash ADC with two Digital Noise Emulators (DNEs) composed of chains of inverters that drive a large capacitance connected to the substrate is fabricated in 0.18um BiCMOS process.

The comparator's output jitter versus noise frequency for two different clock frequencies are plotted in Figure 8(a), which is measured in time domain using the horizontal histogram in a digitizing oscilloscope to evaluate the impact of noise on the comparator decision time. As shown in the figure, as the noise frequency increases, the comparator's jitter also increases; and this problem become very serious for clock frequency higher than 100MHz. On the other

hand, in order to investigate the effect of distance on the sensitivity of a comparator block to substrate noise, the toggle test structure is tested separately with two DNEs on the chip. The comparator's output jitter versus noise frequency for the two DNEs is plotted in Figure 8(b). As shown in the figure, the closer DNE (DNE1) has significantly larger impact on the comparator than the farther ones. For example at 100MHz noise frequency, the comparator's jitter due to DNE1 is twice larger than due to DNE2.

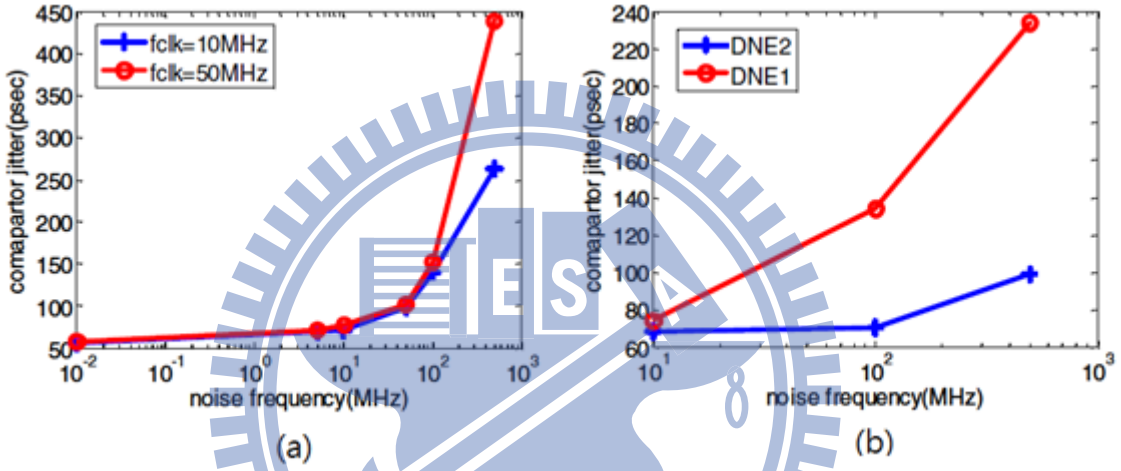


Figure 8 Comparator output jitter vs. noise frequency for (a) two clock frequencies, (b) DNEs at two different locations. [28]

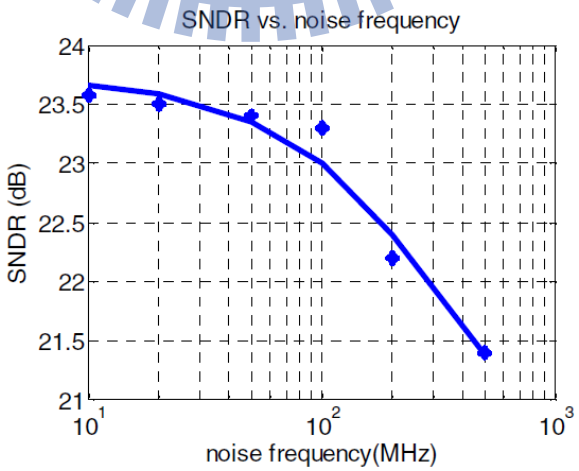


Figure 9 SNDR of the ADC vs. noise frequency. [28]

To see the performance degradation due to substrate coupling noise on a flash ADC, both DNEs are turned on and the SNDR are measured at output. Incorrect codes are observed at the output that degrades the SNDR as shown in Figure 9, which SNDR of the ADC versus noise frequency for sampling speed of 262MHz at 5MHz input frequency are presented. The SNDR degradation is around 2 dB (10%) when noise frequencies are above 200MHz.

2.3.4 Digital-to-Analog Converter

In this part, we are going to reveal the substrate coupling noise effect on DACs from previous studies. As mentioned in last part, as the needs of high speed operation for modern wireless communication systems, high speed DACs and ADCs are demanded as interfaces. For high speed DACs' architectures, current-steering is the most popular one that are being used these years, for its highest achievable operation speed and moderate resolution. It is also a perfect candidate for the investigation of substrate coupling noise issue since it is composed of both the fast switching digital parts and the sensitive analog parts. In [32], the substrate coupling noise effect on a 14-bit 100MHz current-steering DAC implemented in 0.35μm CMOS process on a high-resistivity p-substrate is investigated. Differential sensors are placed to measure the voltage between the positive power supply and ground nodes at the clock driver and DAC logic power supplies.

The substrate noise generated by the digital parts of the DAC is measured and proved to be the cause of glitches of several LSBs of amplitude at the output. As shown in Figure 10, the upper trace corresponds to the output of the single-ended substrate noise sensor and the lower graph to one of the DAC outputs for a few data samples around the cross-over of a full scale 500kHz sinusoidal generated with a 25MHz clock. The glitches appearing during the hold intervals of the DAC are due to noise produced by the input code changes. These changes generate substrate noise that is coupled to the DAC output just before the clock signal

switches. The clock switching generates also substrate noise that is coupled to the output.

To find the origin of the different noise components found in the substrate noise when the samples of a sinusoidal signals are applied to the DAC input, substrate noise is measured with the single-ended sensor in three different situations: first, the clock signal is applied to the DAC and the data inputs are held constant; secondly the data bits are switched and the clock signal is stopped, and finally, both data and clock are switched. The results of this experiment are shown in Figure 10 and can be explained as follows. The data changes generate di/dt noise at the digital power supply lines, which is directly coupled to the substrate by the digital substrate biasing contacts. Another source for noise coupling to the substrate is through the parasitic capacitances, which are mainly in the large pad area.

Figure 10 Substrate noise (upper trace) and output glitches (lower trace). [32]

The dependence of the noise on the number of switching bits is shown in Figure 11. The amount of noise generated is highly related to the number of switching gates of the decoder and therefore the number of switching input bits. The noise peak amplitude varies smoothly with the first four least significant bits, assigned to the binary section of the DAC, and increases significantly when more of the input bits assigned to the thermometric section are switched. The same dependence is observed when measuring the noise after the clock raising edge. The data switching noise is due to purely combinational switching in the input decoder

and the clock switching noise is due to the switching of the latches and drivers of the synchronizing circuitry that directly control the switching of the output current sources. This input dependent noise would be converted into clock-jitter, which limits the dynamic performance of the DAC.

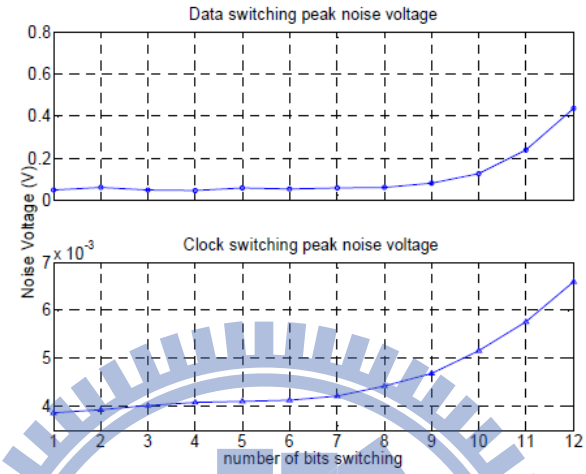


Figure 11 Peak noise voltage of power supply versus number of switching bits. [32]

To sum up, in this paper the substrate noise generated by the digital section of the DAC is measured and shown to be the cause of glitches of several LSBs of amplitude at the output. The origin of this substrate noise has been shown to be the di/dt noise generated at the digital power supply lines in addition to capacitive coupling attributed to the dv/dt of the input signals at the input pads. This power supply noise is translated into substrate noise showing damped oscillation that lasts several ns and is coupled to the output, limiting the DAC maximum achievable performance by affecting severely the output settling time and the internal clock-jitter.

2.4 Chapter Summary

In this chapter, we have discussed the substrate coupling noise in mixed-signal integrated circuits about the generation and propagation mechanisms. The impact of substrate coupling noise on analog/RF circuits are also being presented by giving an overview of the published

works with measurement verifications. To conclude, the substrate coupling noise problem is getting more and more serious as the continuous technology scaling down and the increasing demand of high speed operation for various modern applications. To alleviate this problem, researches have been done on substrate coupling noise suppression/cancellation techniques. We will discuss those techniques in the next chapter while proposing a new technique in the end.

Chapter 3

Substrate Coupling Noise Suppression Techniques

3.1 Introduction

In this chapter, we will first give an overview of the existing techniques for substrate coupling noise suppression, classified as passive and active methods. For the passive methods, test-keys of different guard ring structures with distance variances are taped-out, measured and analyzed in this work. Substrate models are also obtained through this substrate characterization with the help of Assura-RF™. Besides the performance comparison of conventional guard ring structures, another passive method example of using guard ring diodes is also introduced. For the active methods, five different techniques are selected and briefed from previous works to compare their advantages and drawbacks.

After the review of the existing techniques for substrate coupling noise suppression, we will propose a new technique that utilizes both the advantages of the passive and active methods. Chapter summary will be given in the end.

3.2 Existing Techniques

3.2.1 Passive Methods

The most commonly used passive methods for substrate coupling noise suppression are "guard rings", by means of physical barriers or isolation made during layout design. However, whether to use guard rings or what kind of guard ring should be used are normally just

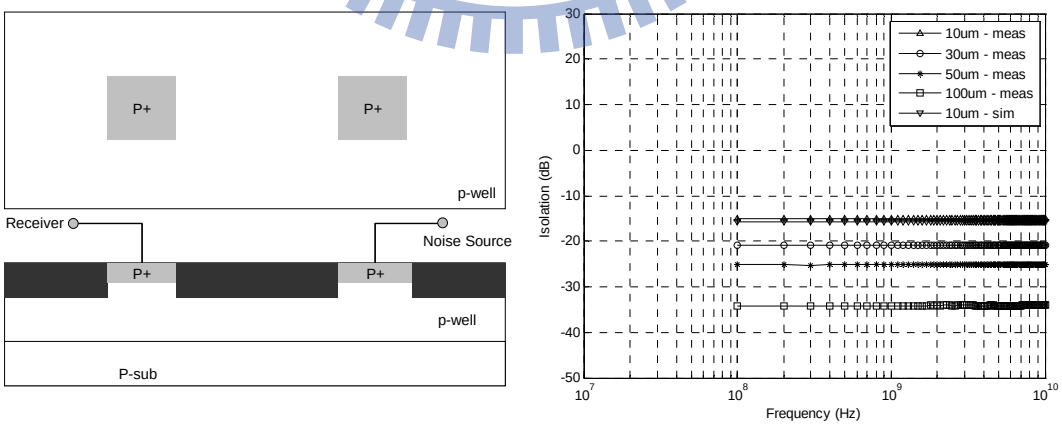
decided through designer's own experience, under the cost of signal integrity degradation (not enough isolation) or extra area consumption (use unnecessary guard rings). In this part, we are going to show both the simulation and measurement results of five conventional isolation schemes. Substrate network is also obtained through the characterization process with Assure-RF™.

3.2.1.1 Test-keys of Different Guard Ring Schemes

Five isolation schemes are designed and fabricated in UMC 90nm CMOS technology in this work and published in [46], [48], based on three basic guard ring structures which include P+GR, NWGR and DNW with compared to the reference (REF). Thus, six different structures of test-keys include REF, P+GR, NWGR, DNW, NWGR with P+GR (NWGR/P+GR) and DNW with P+GR (DNW/P+GR) are implemented and measured in the frequency range from 100MHz to 10GHz with distance variance of 10μm to 100μm. In Figure 12 to Figure 17, the designed structures are shown in (a) and the corresponding measurement and simulation results are shown in (b), where the P+ region at the right are the noise sources and the one at the left are the receivers. The areas of the noise source and receiver are both 7.4μm x 13μm. The width of both P+GR and NWGR is 1.5μm and the distance from P+GR and NWGR to noise receiver are 1.5μm and 3μm, respectively.

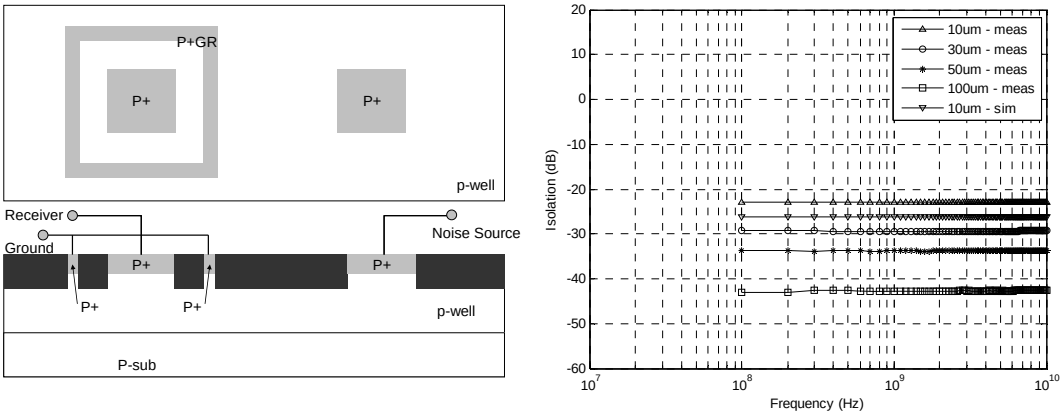
By comparing the isolation schemes of single guard ring structures in a frequency range below 10GHz, the P+GR, NWGR and DNW structures give about 8dB, 25dB and 25 to 55dB isolation improvement, compared to the reference structure at an isolation distance of 10μm, correspondingly. For the double guard ring designs of NWGR/P+GR and DNW/P+GR, they provide isolation performance of about 10dB and 7dB better than that of NWGR and DNW, respectively. The designs with DNW structure give the most isolation but require additional implant/mask processing steps, which increase the cost and the time of process cycle.

Therefore, such designs cannot always be used. The better isolation performances for NWGR and DNW and other double guard ring structures compared to P+GR is owing to the junction capacitances between NW/TW, DNW/TW, NW/PW and DNW/PW, which formed a obstacle to block the substrate coupling noise. However, they start to lose this advantage when the frequency increases, as the higher frequency decreases the capacitive blocking capability of the junctions. For frequencies below several GHz, the DNW structure achieves better substrate isolation compared to the NWGR. Nevertheless, as the frequency reaches 10GHz, the DNW structure shows almost the same isolation performance as NWGR. To analyze the isolation character of the single guard ring structures, in the frequency below 10GHz of interest, the isolation performance of P+GR shows a resistive behavior which is independent of frequency, where NWGR shows both resistive and capacitive behaviors as the frequency gets higher than several GHz and DNW behaves mainly capacitive in the whole frequency range. To be mentioned, due to some measurement error in the case of DNW, there is an increasing behavior of the isolation performance when frequency is below around 500MHz in Figure 15, normally it should decrease as frequency goes higher as the simulation result.



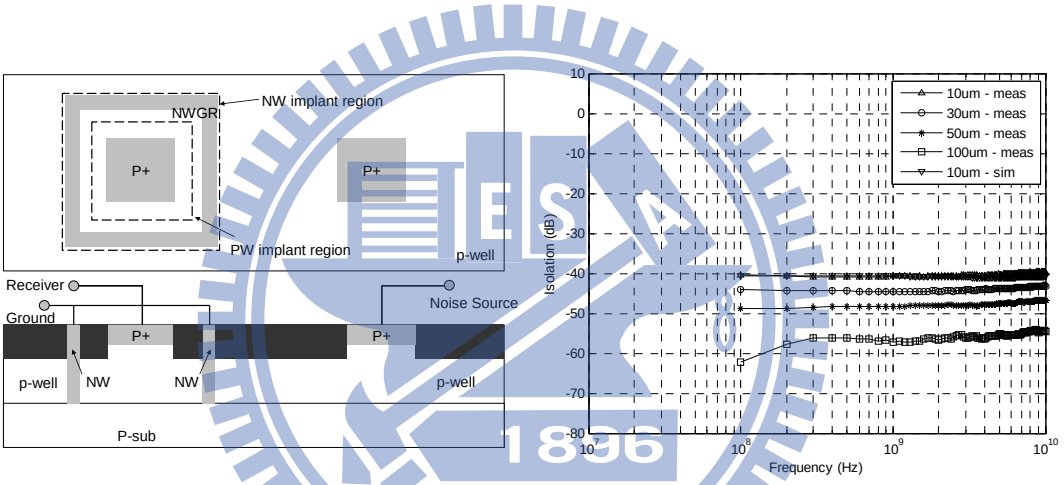
(a) (b)

Figure 12 (a) The reference structure and (b) measurement and simulation results.



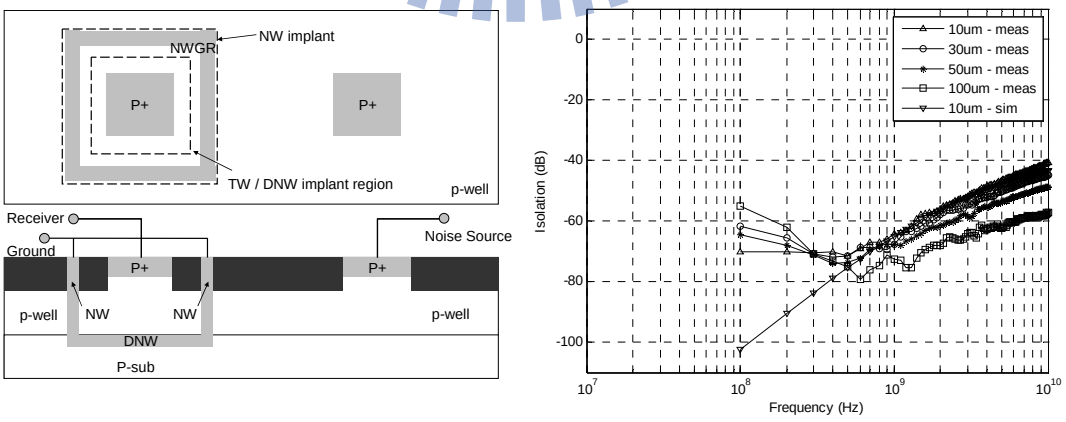
(a) (b)

Figure 13 (a) The P+GR structure and (b) measurement and simulation results.



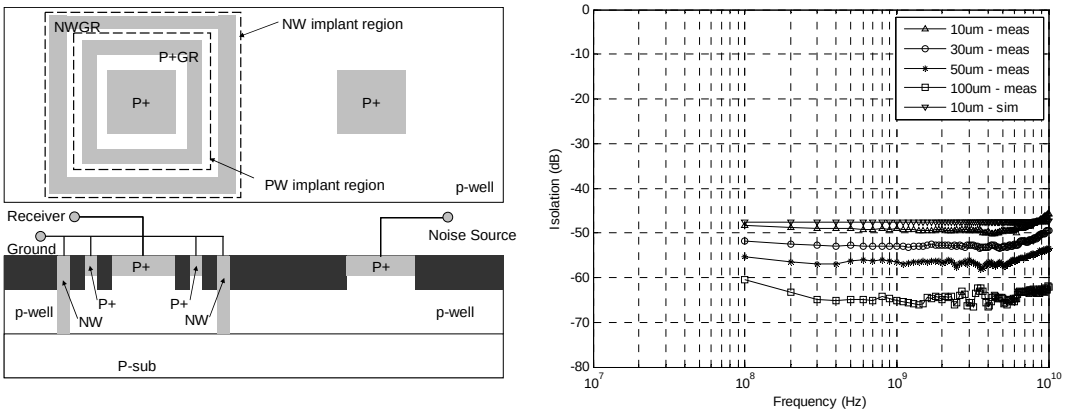
(a) (b)

Figure 14 (a) The NWGR structure and (b) measurement and simulation results.



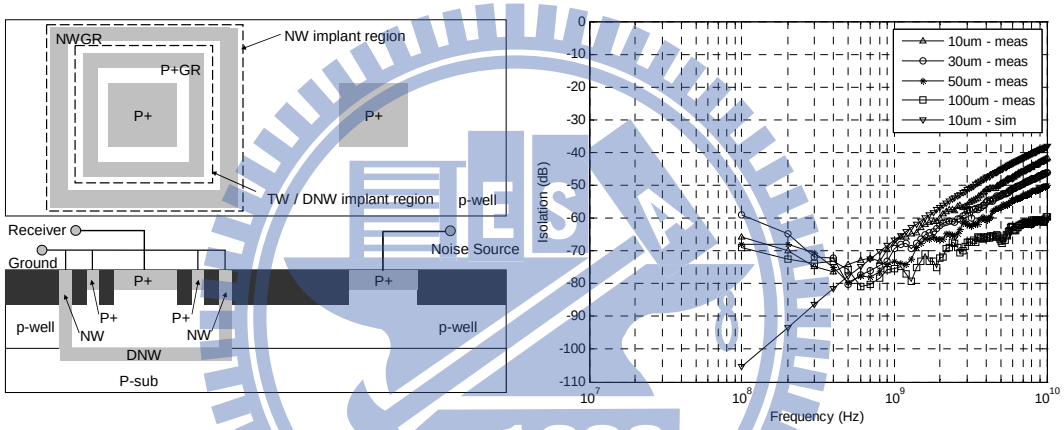
(a) (b)

Figure 15 (a) The DNW structure and (b) the measurement and simulation results.



(a) (b)

Figure 16 (a) The NWGR/P+GR structure and (b) the measurement and simulation results.



(a) (b)

Figure 17 (a) The DNW/P+GR structure and (b) the measurement and simulation results.

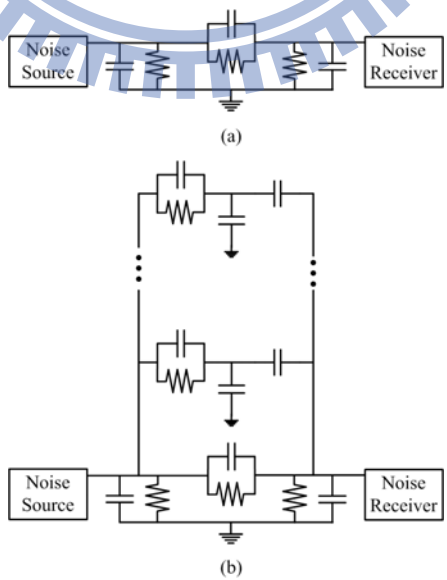


Figure 18 Characterized substrate networks for (a) REF and P+GR, (b) NWGR and DNW.

3.2.1.2 Substrate Characterization with Assure-RF™

Substrate characterization is also done in this thesis with the help of Assura-RF™ to extract the substrate network between devices with process information such as thickness of subdivisions, junction capacitances parameters and material characteristics. The characterized substrate network is both resistive and capacitive considering high frequency effects. Figure 18 demonstrates two characterized networks between the noise source and the receiver for single guard ring test structures of REF, P+GR, NW and DNW. The simulation results with each characterized substrate networks for the six test-key structures are shown in Figure 12 to Figure 17 along with the comparison to the measurement results in 10μm isolation distance. The average errors for each isolation scheme are shown in Table I.

To be mentioned, the parameters in the extracted substrate networks will be utilized for the active guarding technique which will be proposed in Section 3.3. The characterized substrate networks also allow designers to utilize in their design process and hence choose the most suitable isolation scheme to meet the specification of substrate coupling noise tolerance and the budgets for the process costs.

Table I

Average error for the isolation schemes between simulation and measurement results

Isolation schemes	REF	P+GR	NWGR	DNW	NWGR/ P+GR	DNW/ P+GR
Average error	5%	14.5%	1.8%	4.2%	2.9%	8.2%

3.2.1.3 Guard Ring Diodes

In [36], [37], the authors has verified that by creating a band-pass filter, using the

inductance of the bond wire and the capacitance of a forward biased diode, the substrate noise can be reduced. The resonant forward-biased guard ring diodes for suppression of substrate noise is shown in Figure 19, where the n+ guard ring is connected to negative voltage of V_{bias} through a large resistor. This forward-biased n+p junction with constant current creates a charge storage region in the diode resulting in a capacitance in pico-Farad range. These components form a band-pass filter that provides a very low impedance path to ground that lowers the substrate noise at designed frequency as:

$$\omega_o = \frac{1}{\sqrt{\tau L I / 25\Omega}} \qquad (3)$$

where L is inductance of the bound wire, τ is the transit time and I is diode current [37]. Figure 20 shows the substrate noise voltages with and without the forward-biased guard-ring. In this manner, substrate noise in mixed signal CMOS integrated circuits can be suppressed resulting in less noise and improved reliability in analog portions of the mixed mode circuits

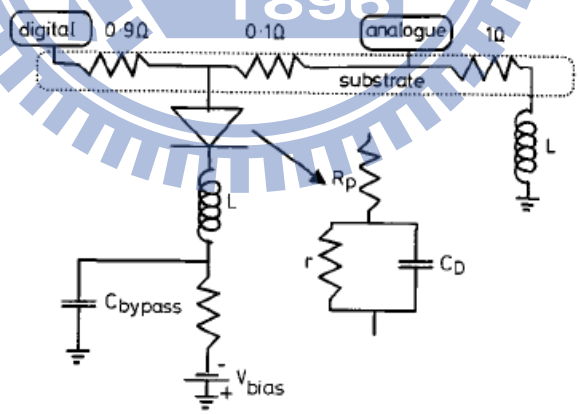


Figure 19 Model of coupling through substrate in a mixed-mode circuit showing guard-ring diode. [37]

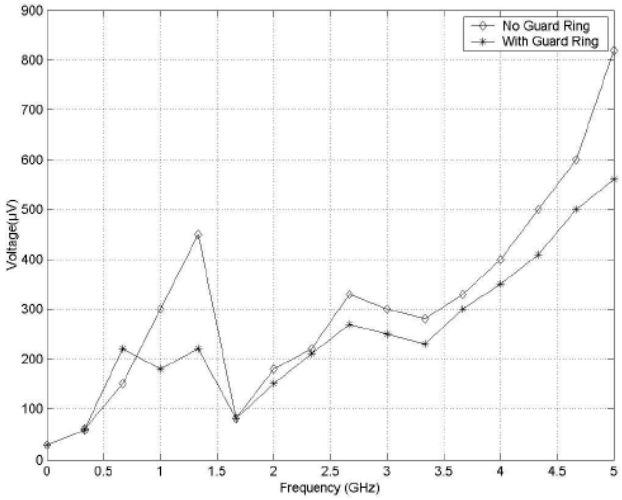


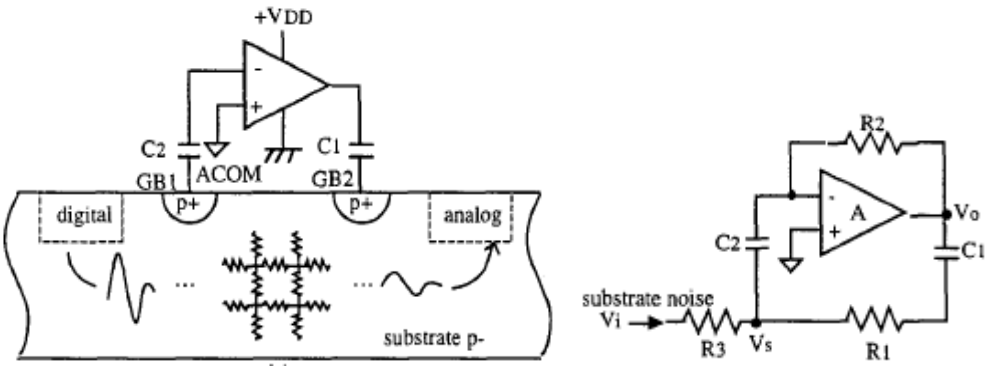
Figure 20 Effectiveness of forward-biased guard circuit. [37]

3.2.2 Active Methods

In 3.2.1, we have introduced some passive methods for substrate coupling noise suppression. However, they may not be effective enough under noisy situation and may cause latch-up if they are not properly used. Here we are going to introduce some active methods that have higher noise suppression level and compensate ability than the passive methods, classified as feed-back type, feed-forward type and active-decoupling type.

3.2.2.1 Active guard band filter

An active guard band filters for substrate coupling noise suppression has been introduced in [40]. This active guard band filter creates a feedback loop using the substrate resistance as a feedback factor therefore introduces an AC coupling configuration. AS shown in Figure 21, CB1 and CB2 are substrate pick-ups that are resistively coupled to the substrate. Capacitor C2 is inserted between GB1 and the input of the amplifier to detect the AC components of the substrate noise. Capacitor C1 is inserted between the output of the amplifier and GB2 to feed an AC noise cancellation signal back.



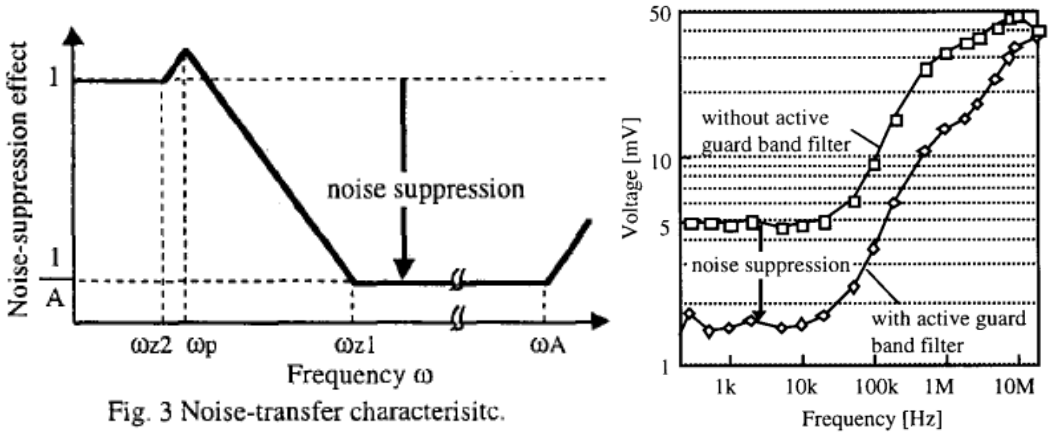
(a) (b)

Figure 21 AC coupling in the on-chip active guard band filter (a) configuration and (b) the simplified circuit model. [40]

Here the substrate is represented by resistance R_1 and R_3. Resistance R_2 is connected between the input and output node of the amplifier as a negative feedback path. The noise suppression ratio can thus be determined by the ratio of Vs and Vi as:

$$\frac{Vs}{Vi} = \frac{(1+sC_1R_1)(1+A+sC_2R_2)}{\left[1+s(C_1R_1+C_1R_3+C_2R_3)+s^2C_1C_2R_3(R_1+R_2)\right]A} = \frac{\left(1-s/z_1\right)\left(1-s/z_2\right)(1+A)}{\left(1-s/p_1\right)\left(1-s/p_2\right)A} \quad (4)$$

Since R_1 and R_3 are very small, the zero and pole frequencies are expressed as $\omega_{z1} = 1/C_1R_1$, $\omega_{z2} = (1+A)/C_2R_2$ and $\omega_p = 1/\sqrt{C_1C_2R_3(R_1+R_2)}$. Resistance R_2 is always designed to be larger than R_1 and R_3 to keep ω_{z1} always larger than ω_p. However, if A is sufficiently large, the substrate noise can be suppressed to $1/A$ above ω_{z1} to the amplifier open-loop gain bandwidth ω_A. The noise transfer characteristic and the measured substrate noise suppression performance of an active guard band filter design example are shown in Figure 22.



(a) (b)

Figure 22 (a) Noise-transfer characteristic and (b) measured substrate noise suppression performance of an active guard band filter design example. [40]

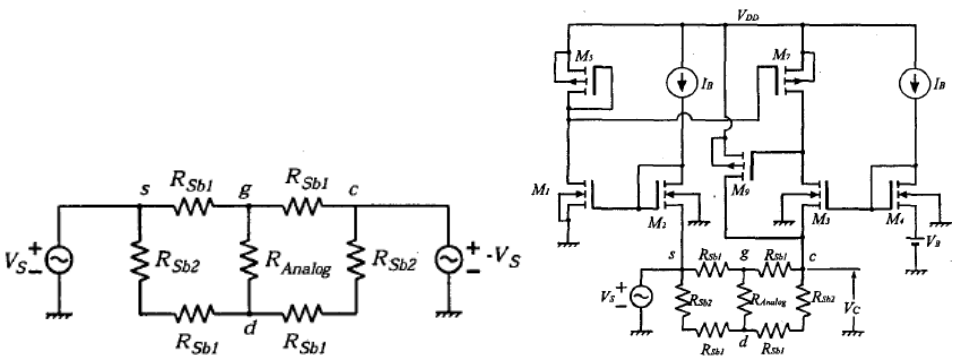
3.2.2.2 Active Guard Band Technique

It is found that the conventional AC coupling technique, like the one introduced in 3.2.2.1, it requires large coupling capacitances which will disable an on-chip implementation of the circuit. In [41]-[42], an active guard band technique based on a signal cancellation using its opposite signal is presented. The concept of this technique and a design example of an active guard band circuit are shown in Figure 23. As shown in Fig. 23(a), since the substrate resistances are symmetrical, the transfer function from node s to nodes g and d will be:

$$\frac{V_g}{V_s} = \frac{V_d}{V_s} = \frac{V_s + V_c}{2} = \frac{V_s - V_s}{2} = 0 \quad (5)$$

As a result, the substrate noise appeared in node g is cancelled.

Simulation result of the active guard band circuit with the comparison to ideal guarding is shown in Figure 24. By combining both the active guard band circuit and an ideal guard ring, it can give around 30dB noise suppression performance from DC to 1MHz and still be effective until 100MHz.



(a) (b)

Figure 23 (a) Basic concept of active noise cancellation technique and (b) an active guard band circuit. [41]

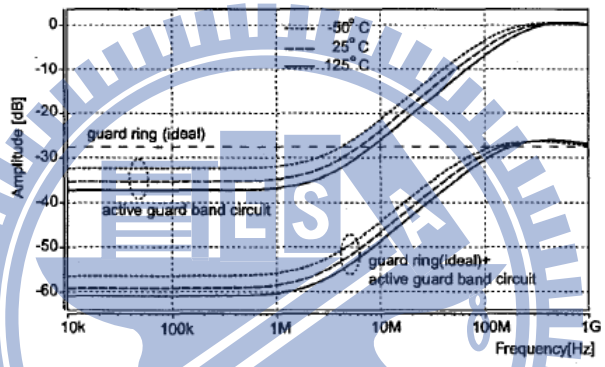
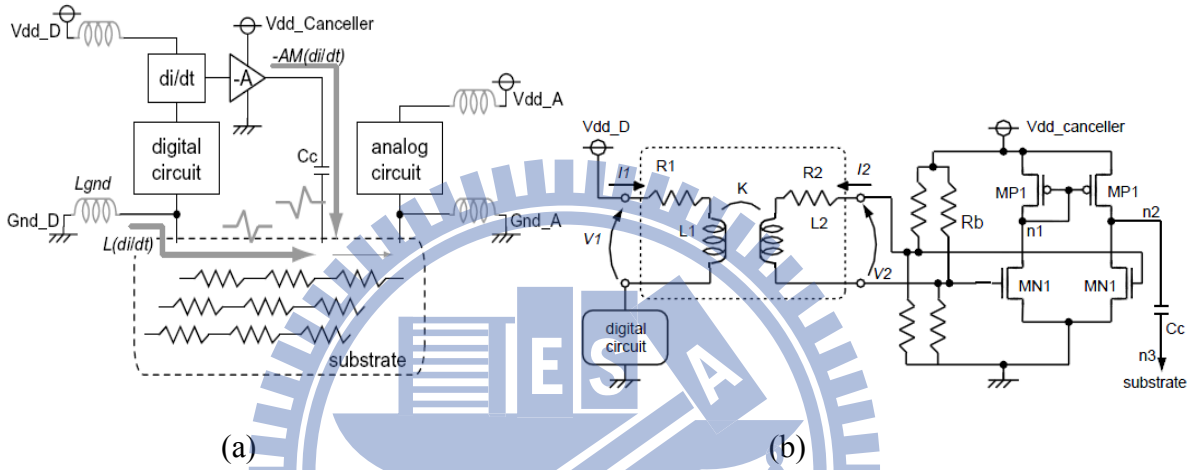


Figure 24 The performance of the active guard band circuit and the comparison with ideal guard ring. [41]

3.2.2.3 Feed-Forward Active Substrate Noise Canceling Technique

In [43], a feed-forward active substrate noise canceling technique using a power supply di/dt detector is presented, as shown in Figure 25(a). Since the substrate is tied to the ground line, the substrate noise is closely related to the ground bounce which is caused by di/dt when inductance is dominant on the ground line impedance. This active canceling technique detects the di/dt of the power supply current and injects an anti-phase signal into the substrate so that the di/dt proportional substrate noise is cancelled out. The substrate noise canceller circuit is shown in Figure 25(b), which is mainly based on a di/dt detector, where a mutual inductor

coupled to the power supply line induces the di/dt proportional voltage, and an amplifier that amplifies and outputs the anti-phased signal. Experimental result shows 17% to 34% of the substrate noise can be suppressed from 100MHz to 600MHz operation range by this feed-forward active noise cancelling circuit. An example waveform of substrate noise is shown in Figure 26, where the operation frequency is at 500MHz.



(a) (b)

Figure 25 Feed-forward active substrate noise cancellation technique (a) block diagram and (b) circuit. [43]

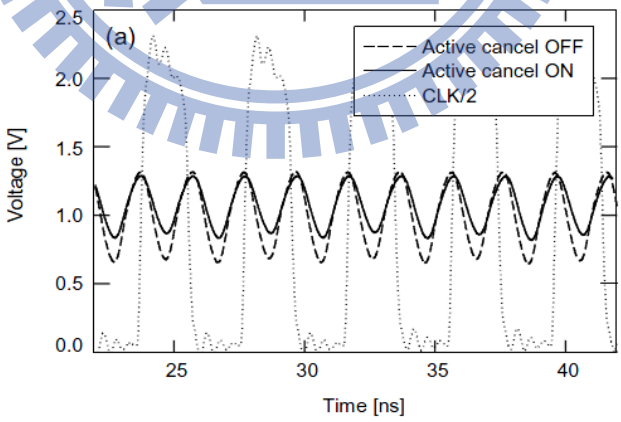
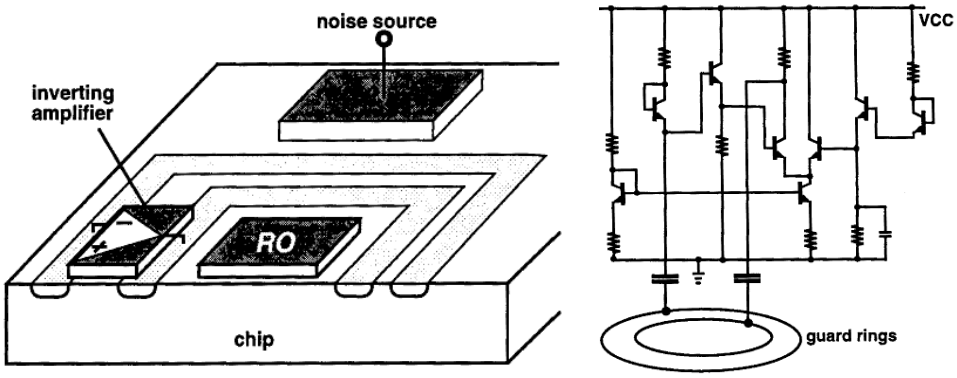


Figure 26 Substrate noise waveforms with the active noise cancelling ON/OFF, together with the CLK/2 signal, operated in 500MHz. [43]

3.2.2.4 Active Substrate Noise Suppression Circuit with On Chip Driven Guard Rings

In [44], an active substrate noise suppression circuit which uses an amplifier with a pair of concentric guard rings is presented. The outer ring acts as a receiver for substrate noise and the inner ring acting as a transmitter of the inverted noise signal. The input of an inverting amplifier is connected to the outer ring, and the output is connected to the inner one. The guard rings are capacitively coupled to the silicon substrate. The substrate coupling noise can be sensed by the outer guard ring and the inverted and amplified by the amplifier. The inverted noise signal is coupled into the substrate by the inner guard ring. In this manner, a quieter region is generated inside the inner ring. Figure 27(a) shows the schematic view of this noise cancellation technique and Figure 27(b) shows the inverting amplifier and its connection to substrate.

To evaluate the performance, the test chip includes a ring oscillator (RO) inside the inner guard ring that receives the residual noise. Sinusoidal “noise” generated by a signal generator is coupled into the substrate through a bond-pad outside the guard rings connected to the substrate. The sideband spurs with the active substrate noise suppression circuit turning on and off, are measured with different noise frequencies and plotted in Figure 28. As shown in the figure, at low frequencies, the capacitive coupling of the guard rings to the amplifier limits the noise suppression. At high frequencies, the bandwidth of the amplifier with low-impedance load limits the performance.



(a) (b)

Figure 27 (a) Schematic view of the noise cancellation technique and (b) the inverting amplifier and its connection to substrate. [44]

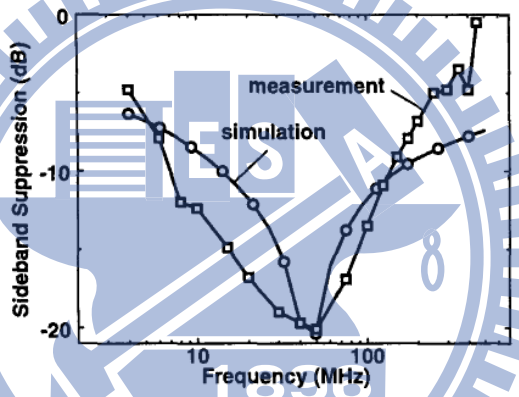


Figure 28 Measurement and simulation results of the suppression performance presented as sideband suppression versus frequency. [44]

3.2.2.5 Active Decoupling Technique

An active decoupling technique is proposed in [45] to suppress substrate crosstalk in mixed-signal system-on-chip (SoC) devices. It uses an operational amplifier to absorb noise through the Miller multiplication of feedback capacitance, and it uses a virtual grounding to keep the voltage stable. Figure 29 shows the concepts of on-chip active decoupling and the conventional capacitor decoupling.

In active decoupling, the capacitor C in the feedback loop of the operational amplifier acts as a decoupling capacitor; its capacitance C, is multiplied by the gain $A(\omega)$ through the

Miller effect. The resulting negative feedback causes the guard band to be virtually shorted to the reference ground line. The noise current from the substrate, which is the crosstalk is thereby absorbed in the operational amplifier and flows into the pair of power supply lines rather than into the reference ground line. The decoupling effect in terms of the noise level with and without decoupling is shown in Figure 30, which gives a maximum 3.17dB suppression performance at 200MHz.

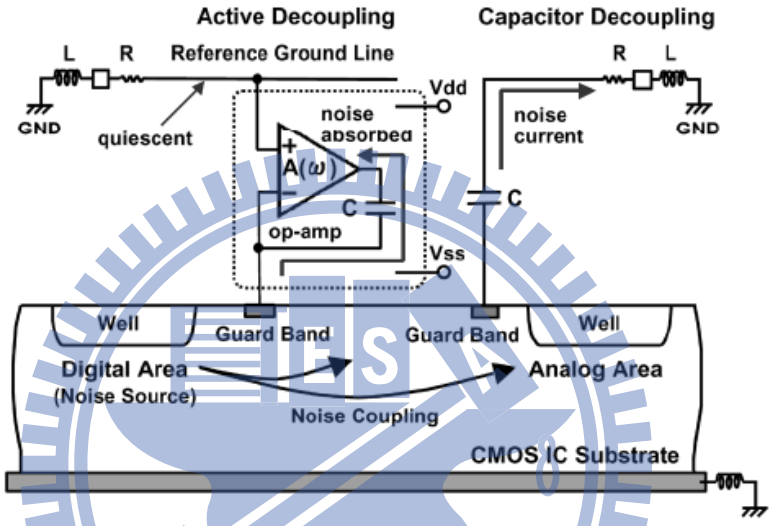


Figure 29 Concepts of on-chip active decoupling and capacitor decoupling. [45]

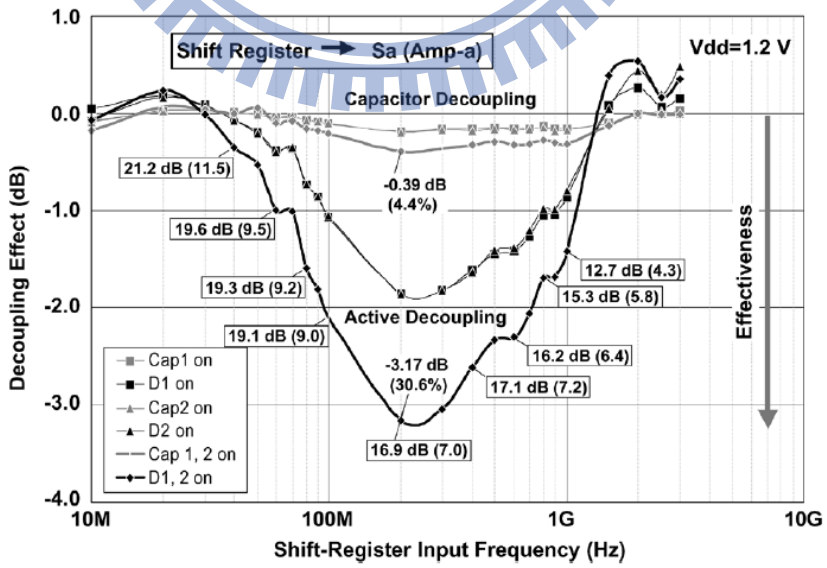


Figure 30 Effects of active and capacitor decoupling. [45]

3.2.3 Brief Summary

Many techniques have been investigated to alleviate this problem of substrate noise suppression. Either passive or active methods are applied for substrate coupling noise reduction. For passive methods, different guard ring types are designed, measured and analyzed in this work [46]. Another passive method named guard ring diodes is also introduced in [36], [37]. For active methods, noise signals can be either decoupled or counteracted as the references in [38]-[44]. Among those techniques, passive methods need no power consumption but may not be effective enough in noisy situations. On the other hand, although active methods have a higher level of noise suppression, there are several limitations and drawbacks still. In [39], [42] and [43], CMOS amplifiers are used to invert the noise signals and inject them into the substrate for counteraction; but their performance are all limited by the trade-off of power consumption and gain-bandwidth product of amplifiers. Hence ranges of the effective operation frequency are less than few hundred mega-hertz. In [43], it even requires area consuming inductors to perform the di/dt detection. In [44], although a high noise suppression bandwidth as 400MHz is achieved by employing a high gain, high bandwidth SiGe HBT amplifier, and the hetero-junction bipolar technology is not suitable for the SoC design. On the other hand, it also needs two capacitors to feed the signal into the substrate which occupies considerable area. A current mirror based method is employed in [41] for lower power and area consumptions, but the effective noise suppression is less than 100MHz due to the parasitic effects that dominate the frequency response. Finally, in [45], substrate noise is wideband suppressed by -1dB in the frequency range from 40MHz to 1GHz, and is maximally -3.5dB suppressed at 200MHz by decoupling noise signals to ground via three large capacitors (10pF each), where the capacitance values are equivalently increased by three power-consuming operational amplifiers (3.3mW each) through Miller Effect.

To sum up, both existing passive and active methods have some limitations in area/power consumption, effective bandwidth and the noise suppression ability. In the following section, we are going to propose a new technique for substrate noise suppression, which can achieve more than 10dB suppression ability with giga-hertz noise suppression bandwidth, at the cost of the usage of several active devices with few mili-watt power consumption.

3.3 Proposed Active Guarding Technique

In this section, an active guarding technique is proposed for wideband substrate noise suppression. A noise decoupling mechanism is developed to provide a decoupling path and to sense the noise level for generating noise cancellation current. A feed-forward compensation mechanism is also developed to extend the noise suppression bandwidth and to adjust the amplitude of phase-inversed noise cancellation current by introducing a zero and an amplitude controller. With substrate characterization done in 3.2.1.1 and 3.2.1.2, parameters of substrate network impedance, decoupling factor and amplitude of noise cancellation current can be either obtained or determined. The proposed circuit needs only several active devices of MOS transistors, and no power-consuming high-gain, wideband amplifiers or area consuming passive components as capacitors are needed.

3.3.1 Design Concepts

The concept of proposed active guarding technique is shown in Figure 31, with the cross-section of the physical implementation. An active guarding circuit with sense and injection rings is inserted between the noise source and guarded circuitry to suppress the substrate noise coupling. The sense ring is placed at the outer side to receive the substrate noise; the injection ring, on the contrary, surrounds the guarded circuitry at the inner side to

inject the compensation current back to the substrate. In order to prevent self-induced noise from interfering the guarded circuitry through the common substrate, the active guarding circuit is placed in an isolated well.

The proposed substrate noise suppression is achieved by two mechanisms: noise decoupling and feed-forward compensation, as shown in Figure 32. Noise current from any direction to the guarded circuitry is detected and averaged at the sense ring, and then decoupled to the active guarding circuit. The compensation current is generated from the decoupled noise with its phase reversed and the amplitude adjusted. The bandwidth extension is further performed before the compensation current injected back to the substrate. The noise which flows through the substrate other than the decoupling path at the branch point of the sense ring can be cancelled by mixing the compensation current via the injection ring. By implementing both noise decoupling and feed-forward compensation with bandwidth extension, substrate noise received at the guarded circuitry can be effectively suppressed. Details of each mechanism will be explained in the following sections.

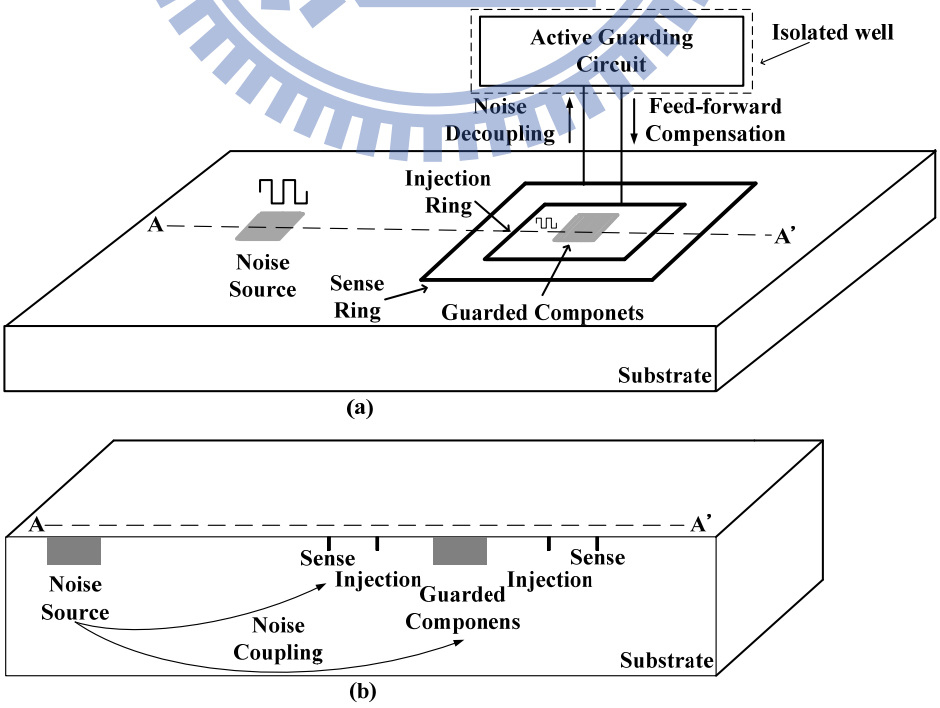


Figure 31 (a) Active guarding technique and (b) Cross-section of the physical implementation

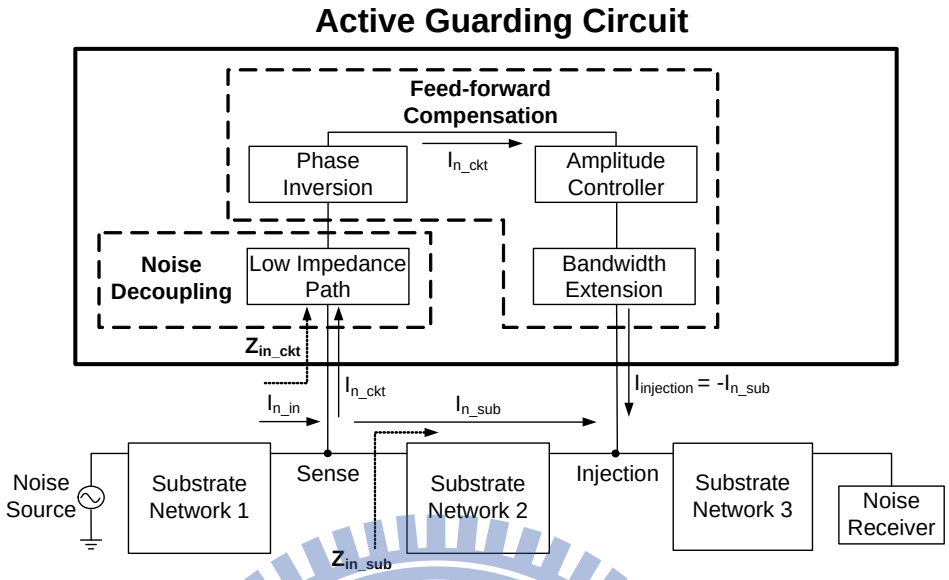


Figure 32 Concepts of substrate noise suppression mechanisms: Noise decoupling and Feed-forward Compensation.

3.3.2 Noise Decoupling

Noise decoupling is performed by creating a decoupling path connected to the sense ring. The decoupling path has an impedance value much lower than or at the same order as that of the substrate network 2 shown in Figure 32. Consequently, the input noise current flows through either the decoupling branch or the substrate network 2 at the sense point. The total substrate noise current flowing toward the guarded circuitry is hence reduced.

A decoupling factor F_D is defined as Equation (6) to present the percentage of the input noise current I_{n_in} that is decoupled. As shown in Figure 32, the decoupling branch connecting the active guarding circuit has an impedance of Z_{in_ckt}. The equivalent impedance of the substrate network 2 is defined as Z_{in_sub}. I_{n_in} is divided into two portions: the current being drained away by the active guarding circuit and the noise current continuing flowing through the substrate toward guarded circuitry, I_{n_ckt} and I_{n_sub}. The substrate noise is (1- F_D) reduced at this stage.

$$F_D(\%) = \frac{I_{n\_ckt}}{I_{n\_in}} = \left(\frac{1}{Z_{in\_ckt} / Z_{in\_sub} + 1} \right) \qquad (6)$$

Z_{in_sub} can be extracted from the substrate model and considered as a known parameter. The design parameter for decoupling factor F_D is Z_{in_ckt}. The smaller the Z_{in_ckt} is, the larger F_D can be obtained, which means more noise current can be drained away from the substrate, and the smaller noise level will affect the guarded circuitry. However, in a circuit implementation using MOS transistors, Z_{in_ckt} cannot be arbitrarily small. The smaller Z_{in_ckt} is, the larger the MOS transistor size is required, leading to higher power consumption and area.

3.3.3 Feed-Forward Compensation

The feed-forward compensation operation includes -180 degree phase inversion, amplitude adjustment and bandwidth extension. A lot of well-known circuits can be used to perform phase inversion and current mirror is herein chosen for its simplicity. The phase-inversed I_{n_ckt} is delivered to an amplitude controller with current gain $A_C(s)$ to adjust the magnitude of the compensation current $I_{injection}$ to be identical to I_{n_sub}, as shown in Equation (7). I_{n_sub} can flow through both the surface and the bottom portions of the substrate network 2.

By designing the injection ring to be placed closely adjacent to the sense ring, the surface portion of substrate network 2 is a low impedance path and dominates the current flow of I_{n_sub}. Finally, the magnitude-matched and phase-inversed current $I_{injection}$ is injected to the substrate through the injection ring and mixed with I_{n_sub} for cancellation of the total noise receiving at the guarded circuitry.

$$\begin{aligned} I_{Injection} &= I_{n\_ckt} \times A_C(s) = -I_{n\_sub} \\ &= -I_{n\_in} \times (1 - F_D) \end{aligned} \qquad (7)$$

The amplitude controller current gain $A_C(s)$ can be determined by the following equation.

$$|A_C(s)| = \frac{I_{n\_sub}}{I_{n\_ckt}} = \frac{Z_{in\_ckt}}{Z_{in\_sub}} = \frac{1}{F_D} - 1 \qquad (8)$$

Trade-offs between device mismatches and parasitic effects exist in the current mirror design, which is used to perform phase inversion. When noise frequencies are higher than the bandwidth of the current mirror, the losses and phase shifts will degrade the noise suppression performance. To release the bandwidth limitation, a zero is introduced. Details circuit methodology will be given in next chapter.

3.4 Chapter Summary

In this chapter, existing techniques for substrate coupling noise suppression of both passive and active methods are introduced. Among those techniques, passive methods need no power consumption but may not be effective enough in noisy situations. As to the active methods, although they may have a higher level of noise suppression, there are limitations and drawbacks, mainly in power / area consumption, effective bandwidth, and suppression ability. Therefore, a new active guarding technique including noise decoupling and feed-forward compensation mechanisms for wideband substrate noise suppression is proposed, which utilizes the advantages of both passive and active methods. In noise decoupling mechanism, it provides a decoupling path and senses the noise level to generate noise cancellation current that injects back to the substrate. In the feed-forward compensation mechanism, it extends the noise suppression bandwidth and adjusts the amplitude of phase-inversed noise cancellation current by introducing a zero and an amplitude controller.

On the other hand, test-keys of different guard ring structures with various distances are taped-out, measured and analyzed in this work. Substrate models are obtained through substrate characterization with the help of Assura-RF™. The characterized substrate model provides simplified substrate networks for the common single guard ring structures, which

can be utilized for further studies on substrate coupling issues. In this work, parameters in the extracted substrate networks are used for the design of decoupling factor F_D and amplitude controller for the use of both noise decupling and feed-forward compensation mechanisms in the active guarding technique. Details of the circuit implementation and analyses of the proposed active guarding technique will be given in next chapter.

Chapter 4

Active Guarding Circuit Design and Analyses

4.1 Introduction

In this chapter, we will give the details about the design of noise decoupling and feed-forward compensation mechanisms in the active guarding technique. The noise injected by the active guarding circuit is also being analyzed to make sure the noise level can be neglect in the frequency of interest. Two versions of the proposed active guarding circuit chips were fabricated in this work, the implementation and results will be given with performance analyses and summary.

4.2 Noise decupling

Figure 33 shows the schematic of the proposed active guarding circuit. The input common-gate transistor M_1 creates a low impedance path for the noise decoupling at the sense point with impedance value $1/g_{m1}$. Unlike other designs: [41] and [44], which use the common source configuration as the input stage to sense the substrate noise voltage from gate, M_1 not only senses the noise current but also drains it away, leading to lower noise level for cancellation in the later stage.

For larger decoupling factor design, i.e., more noise current is drained away, the input impedance, $1/g_{m1}$ should be designed as small as possible. However, smaller $1/g_{m1}$ indicates a larger transistor size $(W/L)_1$, which consumes large area and power. To optimize the design, improvement of decoupling factor F_D in percentage per milli-Watt as the numbers of 20μm

width increment of M_1 from 150μm is studied. Figure 34 shows that less than 60% improvement of the decoupling factor F_D per milli-Watt is achieved after the 10th increment of M_1 width of 350μm when the noise frequency is 1GHz. Therefore, the 9th increment of MOS width, i.e. 330μm is chosen as the width of M_1.

To deal with high frequency noise which the current mirror in Figure 33 can no longer perform its job; another low impedance path is created by the parasitic capacitance of large transistor M_1, i.e. C_{gs1} to take over the original low impedance path of $1/g_{m1}$. In this case, the drained noise current from the substrate in sense node will be directly decoupled away to the AC ground but not flow to the current mirror for the further operation of feed-forward compensation since it's no longer effective during high frequency as to giga-hertz range. Detailed analyses of the phase responses for the current mirror and the following feed-forward compensation stage will be given in 4.3.3.

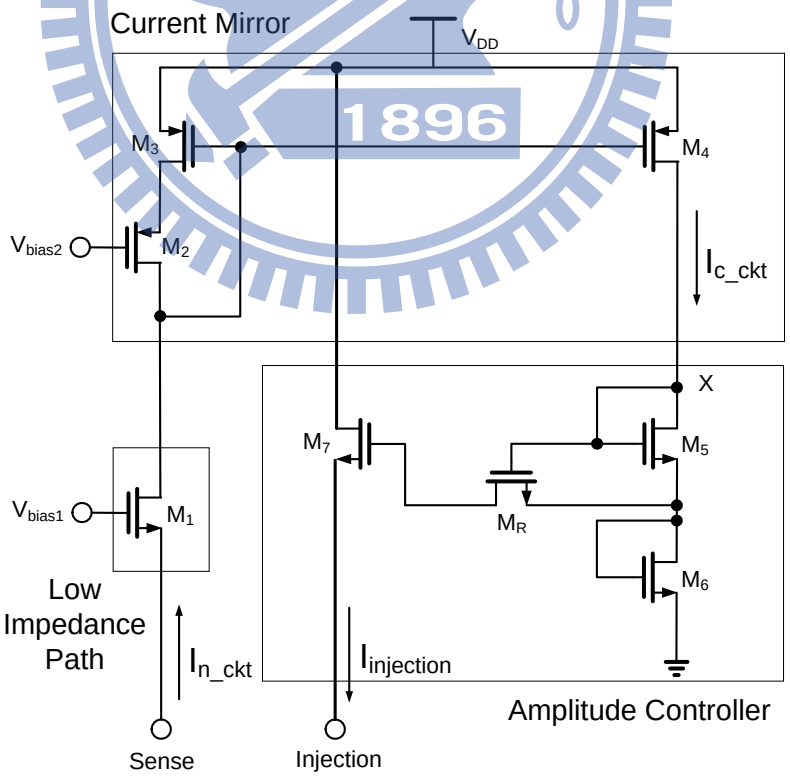


Figure 33 The proposed active guarding circuit.

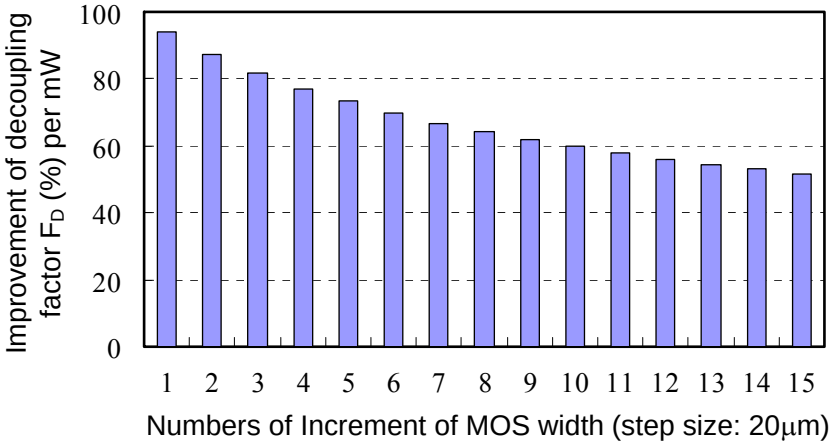


Figure 34 Improvement of decoupling factor versus numbers of 20μm width increment of M_1 from 150μm.

4.3 Feed-Forward Compensation

To realize the feed-forward compensation mechanism, MOS transistors of M_2 to M_7 and M_R are added to perform the phase inversion, amplitude control and the bandwidth extension. The -180 degree phase inversion of the decoupled noise current I_{n_ckt} is accomplished by a current mirror composed of M_2 to M_4. The phase-inversed current I_{c_ckt} (which is identical to I_{n_ckt} for an ideal current mirror) is sent to the amplitude controller and bandwidth extension circuit composed of M_5 to M_7 and M_R. The current is converted to voltage via the diode-connected transistors M_5 and M_6. Finally, the transconductance stage M_7 adjusts the current gain together with M_5, M_6 and M_R then converts the voltage back into current $I_{injection}$ which is injected into the substrate to cancel the noise current I_{n_sub}. Details about the amplitude control and bandwidth extension mechanism will be given in 4.3.1 and 4.3.2.

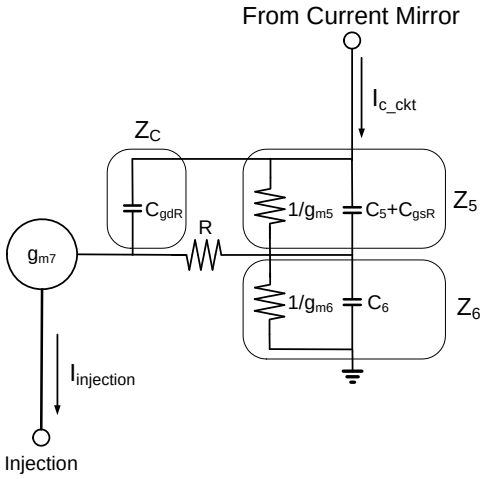


Figure 35 Equivalent circuit of the amplitude controller and bandwidth extension circuit.

4.3.1 Amplitude Control

Figure 35 shows the equivalent circuit of the amplitude controller and bandwidth extension circuit. Transistor M_5 and M_6 are modeled as resistor $1/g_{m5}$, $1/g_{m6}$ with their parasitic capacitance C_5, C_6. M_R is modeled as a resistor R with its gate-drain parasitic capacitance C_{gdR} and gate-source parasitic capacitance C_{gsR}, and M_7 performs as a transconductance stage.

Equation (9) shows the transfer function of $I_{injection}/I_{c\_ckt}$ as the small-signal current gain $A_A(s)$ of the amplitude controller.

$$A_A(s)=\frac{I_{injection}}{I_{c\_ckt}}=\left(\frac{RZ_5}{R+Z_5+Z_C}+Z_6\right)\times g_{m7} \qquad (9)$$

Therefore, the low frequency current gain, i.e. $A_C(0)$ can be approximated as

$$\left|A_A(0)\right|=\frac{I_{injection}}{I_{c\_ckt}}=\frac{g_{m7}}{g_{m6}}. \qquad (10)$$

By referring to equation (8) and (10), the current gain can be determined as shown below

$$\left|A_A(0)\right|=\frac{I_{n\_sub}}{I_{n\_ckt}}=\frac{1/g_{m1}}{R_{in\_sub}}=\frac{I_{injection}}{I_{c\_ckt}}=\frac{g_{m7}}{g_{m6}}. \qquad (11)$$

As a result, given R_{in_sub} from a substrate model and an optimal designed impedance $1/g_{m1}$, the ratio of g_{m7}/g_{m6} is determined to match the current of $I_{injection}$ and I_{c_sub} for substrate

noise cancellation.

4.3.2 Bandwidth Extension

To improve the noise suppression performance at high frequencies, a bandwidth extension circuit is applied by inserting a triode-region transistor M_R. The introducing of M_R creates a zero and a pole [49] which can be expressed as

$$Z_R = -\frac{g_{m6}}{g_{m5}+g_{m6}} \times \frac{1}{RC_{gdR}}, \qquad P_R = -\frac{1}{RC_{gdR}} \quad . \tag{12}$$

Hence, the effective noise suppression bandwidth of the active guard circuit can be extended by designing the zero Z_R close to the original dominant pole P_D of the circuit without M_R to perform frequency compensation. The bandwidth is extended until P_R becomes to affect the frequency response. The dominant pole P_D of the circuit without M_R can be approximated as

$$P_D \cong -\frac{1}{R_X(C_X \parallel C_P)}, \tag{13}$$

where $R_X = r_{o4} \parallel [1/g_{m5} + 1/g_{m6}]$, r_{o4} is the output resistance of M_4.

$C_X = C_5 + [C_6 \parallel (C_{gs7} + C_{sub}) \parallel C_{gd7}]$, C_5 and C_6 are the parasitic capacitance of M_5 and M_6, and C_{sub} is the equivalent capacitance of substrate seen from the source of M_7.

$C_P = C_{gd4} + (C_{gs4} \parallel C_{gs3})$.

4.3.3 Phase Estimation

For further analysis of the current subtraction error at Injection node due to phase mismatch, two parts of phase shifts are analyzed: the phase shift of the remained noise current that flows from Sense node to Injection node through the substrate; and the phase shift of decoupled noise current that flows from Sense node to Injection node through the proposed active guarding circuit. The former, as is mentioned in sub-section B, Section II, since the

injection ring is placed closely adjacent to the sense ring, the phase shift from Sense node to Injection node through the substrate can be minimized and thus neglected. As for the latter, phase estimation is done to analyze the phase shifts from Sense node to Injection node through the proposed active guarding circuit as a function of frequency. Two portions of phase shifts as $\angle A_C(j\omega)$ and $\angle A_A(j\omega)$, which express the phase shift from Sense node to the current mirror output node X (in Figure 33) and the phase shift from node X to the amplitude controller output node (Injection), respectively, are derived from the small-signal current gain of the current mirror $A_C(s)$ (which is shown in Equation (14)) and current gain of the amplitude controller, $A_A(s)$ (which is shown in Equation (9)).

$$A_C(s) = \frac{I_{c\_ckt}}{I_{n\_ckt}} = \frac{sC_{gs2}g_{m4} + g_{m2}g_{m4}}{s^2 C_{gs2}(C_{gs3} + C_{gs4}) + s(C_{gs3} + C_{gs4}) + g_{m2}g_{m3}} \qquad (14)$$

For a transfer function $A(s)|_{s=j\omega} = (a+bj)/(c+dj)$, the phase shift can be expressed as $\angle A(j\omega) = \tan^{-1}(b/a) + \tan^{-1}(d/c)$.

The phase response of the current mirror can be estimated as $\angle A_C(j\omega)$, as in Equation (15). The effect of bandwidth extension circuit in phase domain can be revealed via $\angle A_A(j\omega)$, as shown in Equation (16).

$$\angle A_C(j\omega) = -\pi + \tan^{-1}(b_1/a_1) - \tan^{-1}(d_1/c_1), \qquad (15)$$

where $a_1 = g_{m2}g_{m4}$, $b_1 = \omega g_{m2}g_{m4}$, $c_1 = g_{m2}g_{m3} - \omega^2 C_{gs2}(C_{gs3} + C_{gs4})$ and $d_1 = \omega(C_{gs3} + C_{gs4})$.

$$\angle A_A(j\omega) = \tan^{-1}(b_2/a_2) - \tan^{-1}(d_2/c_2), \qquad (16)$$

where $a_2 = g_{m5} - \omega^2[RC_{gdR}(C_5 + C_6 + C_{gdR})]$, $b_2 = \omega[C_5 + C_{gsR} + C_{gdR} + RC_{gdR}(g_{m5} + g_{m6})]$, $c_2 = g_{m5}g_{m6} - \omega^2[C_6(C_5 + C_{gsR} + C_{gdR}) + g_{m6}RC_{gdR}(C_5 + C_{gsR})]$ and $d_2 = \omega[g_{m6}(C_5 + C_{gsR} + C_{gdR}) + g_{m5}C_6] - \omega^3 C_6 C_{gdR}(C_5 + C_6)$.

The estimated results are shown in Figure 36 in comparison with circuit simulation results of $\angle A_C(j\omega)$, $\angle A_A(j\omega)$ and their sum, $\angle A_C(j\omega)+\angle A_A(j\omega)+\pi$, which indicates the total unwanted phase shifts for signals passing through the proposed active guarding circuit. Both estimated results and circuit simulation results show that the bandwidth extension circuit provides opposite sign of phase shift that compensates the phase shift of the current mirror in a wide frequency range, and consequently reduces the total phase errors which result in the subtraction error. However, although the phase errors are reduced, the magnitude of the injection current for substrate noise cancellation is still attenuated as the frequency gets higher. Therefore, in high frequency, the noise suppression performance of the proposed active guarding circuit is still degraded.

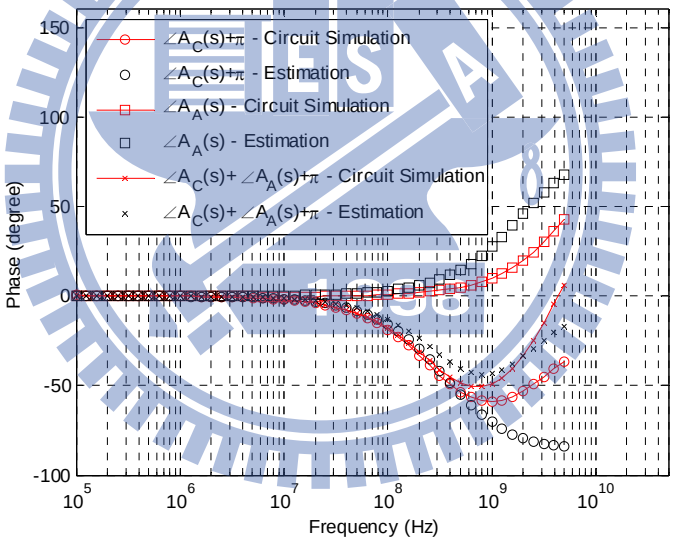


Figure 36 Estimated and circuit simulation results of the phase shifts versus frequency.

4.4 Circuit Inject Noise

Though the proposed active guarding circuit counteracts substrate coupling noise, it inevitably induces noises to the common substrate while performing suppression. Unwanted noises induced by the circuit are classified into two parts; first part is the noise coupling through the common substrate from the transistor's bulk and the second part is the noises injecting directly to the substrate through the wires connected to sense and injection ring.

For the first part, as described in Chapter 3, the active guarding circuit is placed in an isolated well and, as shown in Figure 14 for NWGR isolation scheme, the isolated well provides at least 40dB isolation performance for 10μm isolation distance. Therefore, the noises injected from the circuit which might transfer through the common substrate to the guarded circuit will be mostly blocked by the well and thus can be neglected. As for the second part, the total thermal noise at output node (Injection) can be expressed as follows,

$$\overline{I_{noise}^2} = 4KT\gamma \times \left(g_{m1} + g_{m2} + g_{m3} - g_{m4} - g_{m5} + g_{m6}\right) \times \frac{g_{m7}}{g_{m6}} + 4KT\gamma \times g_{m7} . \qquad (17)$$

In this work, I_{noise} is about 7.5×10^{-11}A in low frequency, at room temperature. On the other hand, although the flicker noise might degrade the circuit performance, the degradation is only limited in low frequencies up to several mega-hertz. As a result, the total noise injected by the proposed circuit is much lower than the considered noise level in a wide frequency range.

4.5 Measurement Setup and Experimental Results

Though the proposed active guarding circuit counteracts substrate coupling noise, it inevitably induces noises to the common substrate while performing suppression. Unwanted noises induced by the circuit are classified into two parts; first part is the noise coupling through the common substrate from the transistor's bulk and the second part is the noises injecting directly to the substrate through the wires connected to sense and injection ring.

4.5.1 First Implementation in UMC 90nm Process

Based on the active guarding technique design concepts with characterized substrate model, the proposed active guarding circuit is first implemented in 90nm CMOS technology. Figure 37 shows the microphotograph of the fabricated chip.

The area of proposed active guarding circuit core is 20μm × 41μm. Two independent test cases of Test Case 1 and Test Case 2 shown in Fig. 38 are implemented in the same chip with identical active guarding circuit designs. For each test case, four independent noise source inputs made of 10μm x 10μm P+ diffusion pick-ups are placed with isolation distances of 30μm, 50μm, 70μm and 110μm between the noise sources and receiver. Signal generators are used to send signals as noises with various input powers and frequencies from -30dBm to 15dBm and from DC to 5GHz, respectively. The noise signals are coupled through the P+ diffusion pick-ups to the substrate and the noise receiver, and then measured by a spectrum analyzer via the output pads.

The measurement results show similar suppression performance for isolation distances of 30μm and 50μm. And for isolation distances of 70μm and 110μm, the suppression performance cannot be correctly measured due to the limitation of the instruments' sensitivity and the noise from the measurement environment since the noise level at output is lower then -80dBm. As a result, the suppression performance for 30μm is chosen to be presented in the following discussions.

4.5.1.1 Implementation and results - Test Case 1

The setup for chip on board measurement is shown in Figure 38. Test Case 1 evaluates the substrate coupling noise suppression performance by turning the active guarding circuit on/off and measures the isolation between the noise sources and receiver. Figure 39 shows the measurement and simulation results in the frequency range from DC to 5GHz with 30μm isolation distance. The measurement and simulation data showed a 2 to 3dB level shift due to the 5% inaccuracy of the substrate model for REF as shown in Table I. The measurement results of circuit performance show an effective -3dB noise suppression bandwidth from DC to 1.2GHz and -1dB bandwidth up to 2.2GHz. The noise suppression which is better than 9dB

is obtained in the frequency range from DC to 250MHz. The total power consumption is about 2.5mW for 1V supply voltage.

4.5.1.2 Implementation and results - Test Case 2

Owing to the common use of P+GR, in Test case 2, a P+GR is inserted to surround the noise receiver in Test case 1 to see the performance enhancement, as shown in Figure 38. The substrate coupling noise suppression performance is obtained in the same manner as Test Case 1. Figure 40 shows the measurement and simulation results of Test Case 2 in the frequency range from DC to 5GHz with 30μm isolation distance. By comparing to Test Case 1 when the circuit is off, the P+GR contributes 10dB and 14dB isolation to measurement and simulation results, respectively. And owing to the 14.5% inaccuracy of the substrate model for P+GR as shown in Table I, the data of measurement and simulation show a 5dB level shift. The measurement result of circuit performance shows an effective 3dB noise suppression bandwidth from DC to 650MHz and -1dB bandwidth up to 950MHz. The noise suppression which is better than 6dB is obtained in the frequency range from DC to 200MHz. The total power consumption is about 3.5mW for 1V supply voltage.

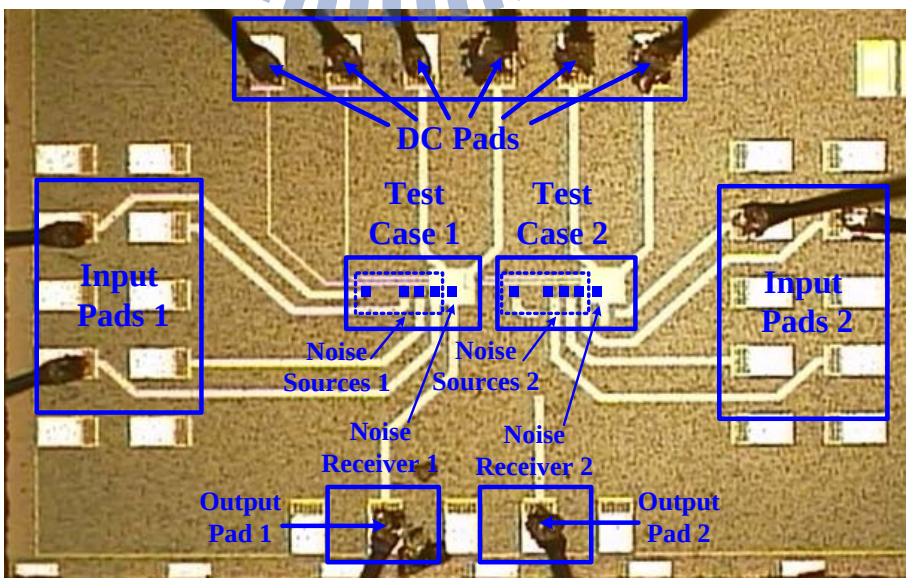


Figure 37 Microphotograph of the proposed active guarding circuit.

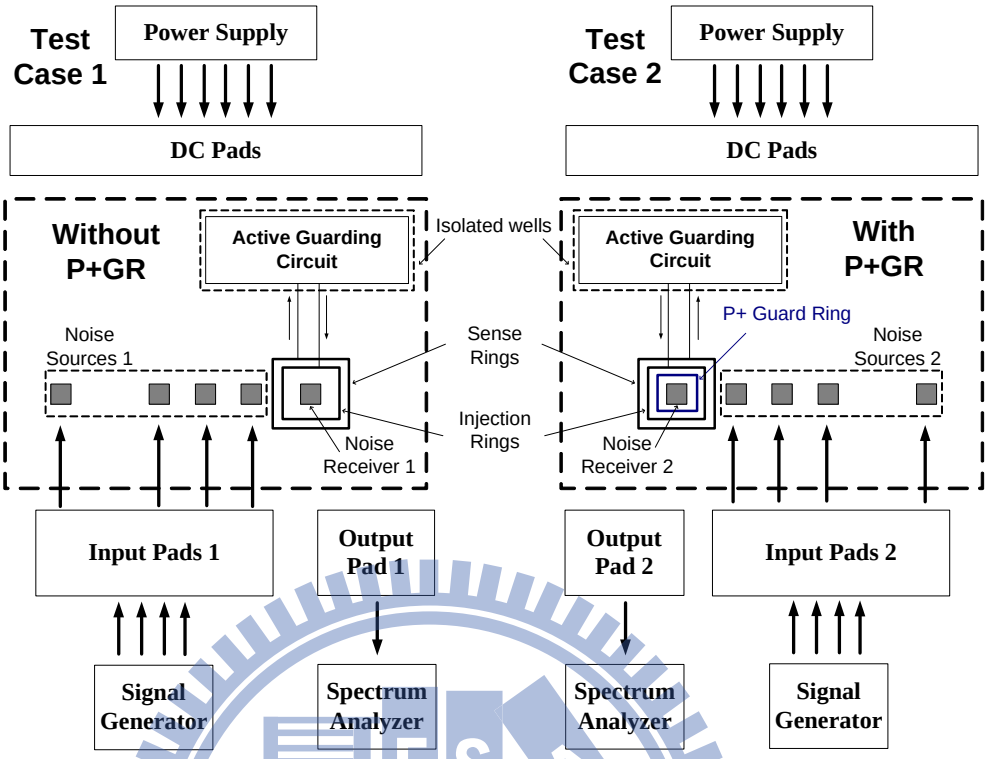


Figure 38 Test plans and measurement setup for the fabricated chip.

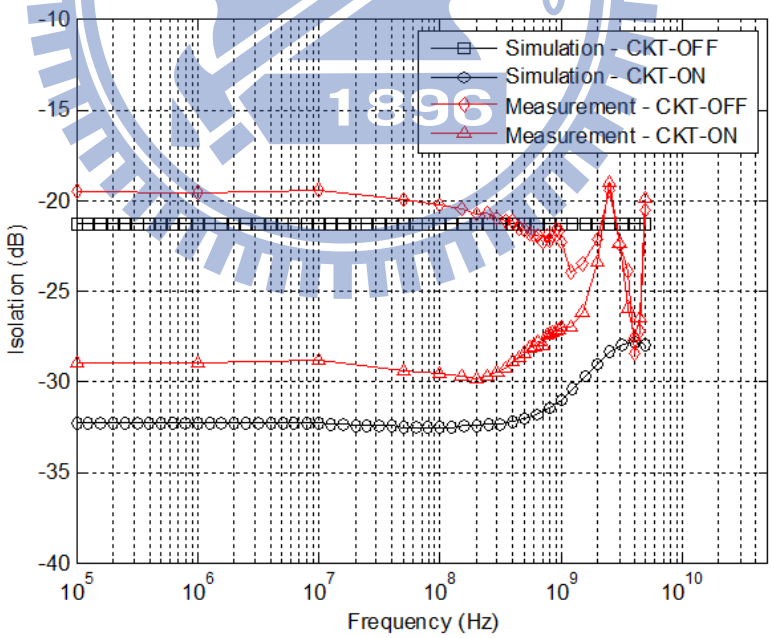


Figure 39 Simulation and measurement results of the isolation performance versus frequency for Test Case 1.

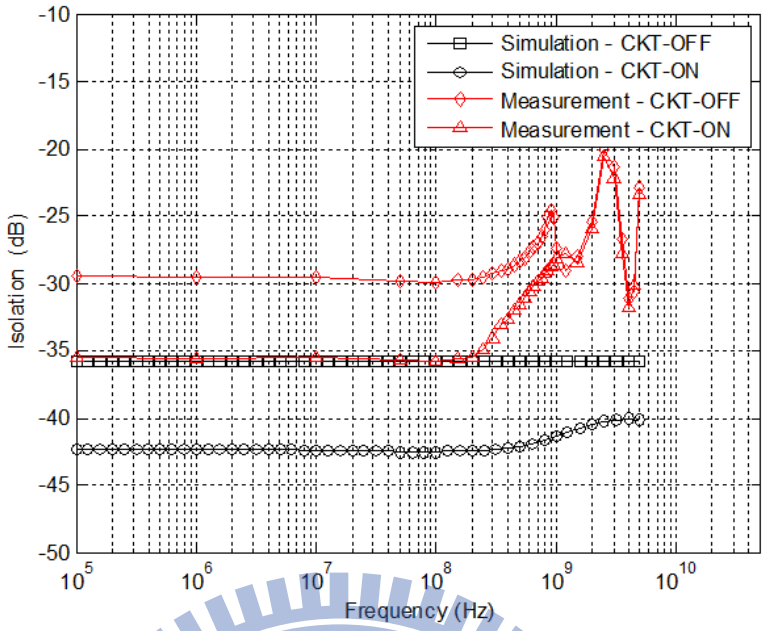


Figure 40 Simulation and measurement results of the isolation performance versus frequency for Test Case 2.

4.5.1.3 Performance Analyses and Summary

For both the Test Case 1 and Test Case 2 in frequencies higher than several hundred MHz to GHz, the measured performance is degraded compared to the simulation results. This degradation is due to the poor ground plane resulting from the lack of parallel ground bonding wires on the test board and the loading effect of the output pads which affect the high frequency performances. Moreover, the bonding pads were too small that only one wire bonding for each output pad is allowed, and thus cannot be corrected in this version. Nevertheless, the circuit performance can be evaluated for the wideband characteristic from DC to 1.2GHz and 250MHz for 3dB and 9dB noise suppression, respectively. In order to show how the parasitic effects affect the performances, simulations including the bond wire inductors and the bonding pads capacitors are performed with comparing to the measurement results for references. As shown in Figure 41 and Figure 42 for Test case 1 and Test case 2, respectively, the trend of measured performances agree with the simulation results with parasitic effects more. In the next version of test chip, the proposed circuit will be designed

for on wafer testing to avoid the unwanted bond wire effects, which will be shown in 4.5.2.

In addition, as shown in Figure 40, the circuit performance in Test Case 2 is not as good as that in Test Case 1 because the inserting of P+GR decreases the input impedance Z_{in_sub} of the substrate at branch point of noise decoupling which also leads to the decrease of F_D. Therefore, for the identical active guarding circuit design as in Test Case 1, the compensation current $I_{injection}$ corresponded to F_D is smaller than the substrate noise current I_{n_sub}, and hence results in the performance degrade. To get better performance in Test Case 2, the amplitude controller gain can be easily adjusted according to the decoupling factor F_D.

Figure 43 shows the measured and simulated noise suppression performance as noise power at the noise receiver increases from around -50dBm to -10dBm at 10MHz. The 1-dB degradation points of the measured noise suppression performance are about -13dBm and -19dBm for Test Case 1 and Test Case 2, respectively, which present the noise tolerance for the active guarding circuit inputs in these two test conditions.

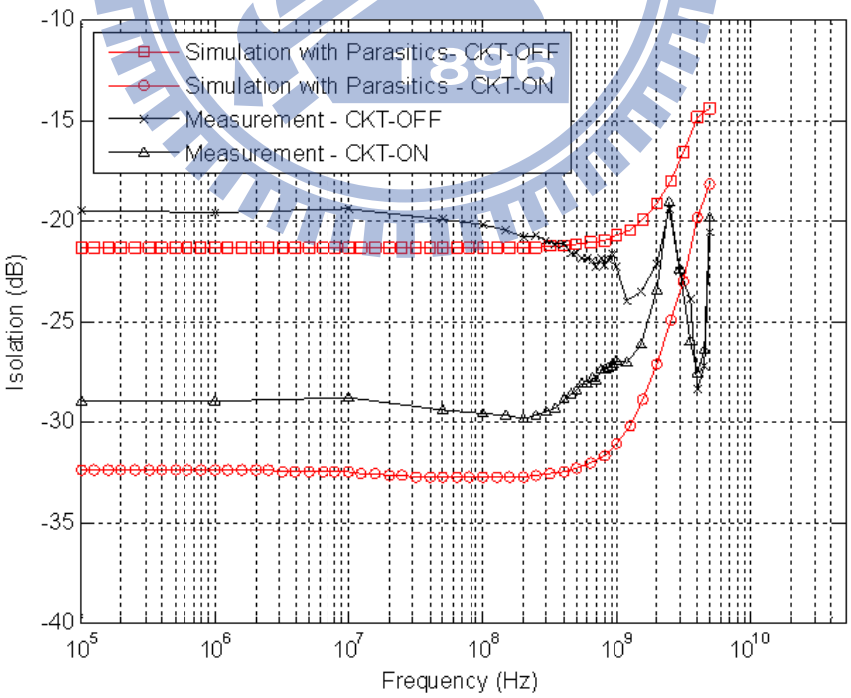


Figure 41 Simulation and measurement results of the isolation performance versus frequency for Test Case 2

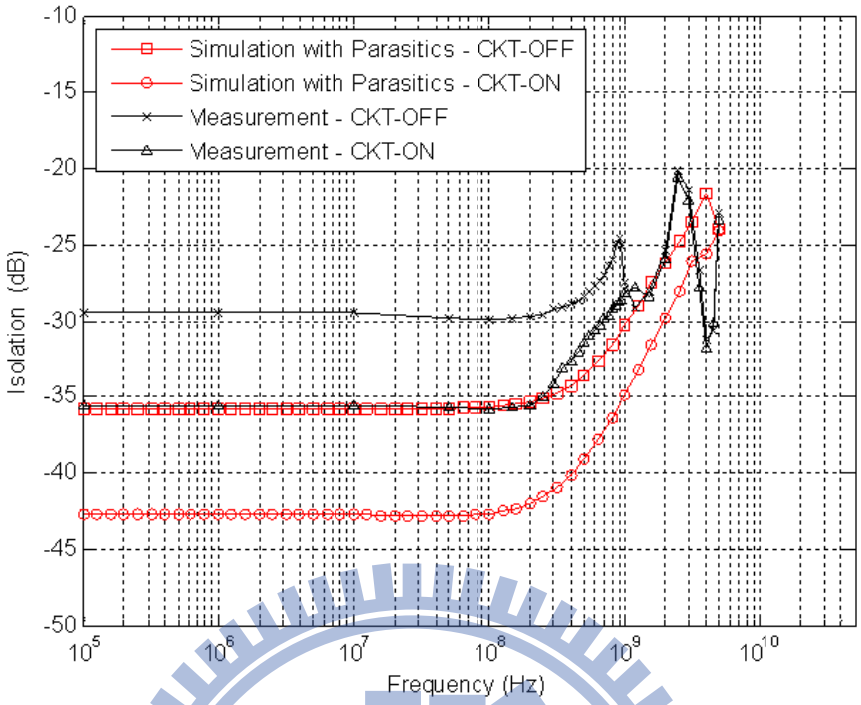


Figure 42 Simulation results with bond wire effect and measurement results of the isolation performance for Test Case 2

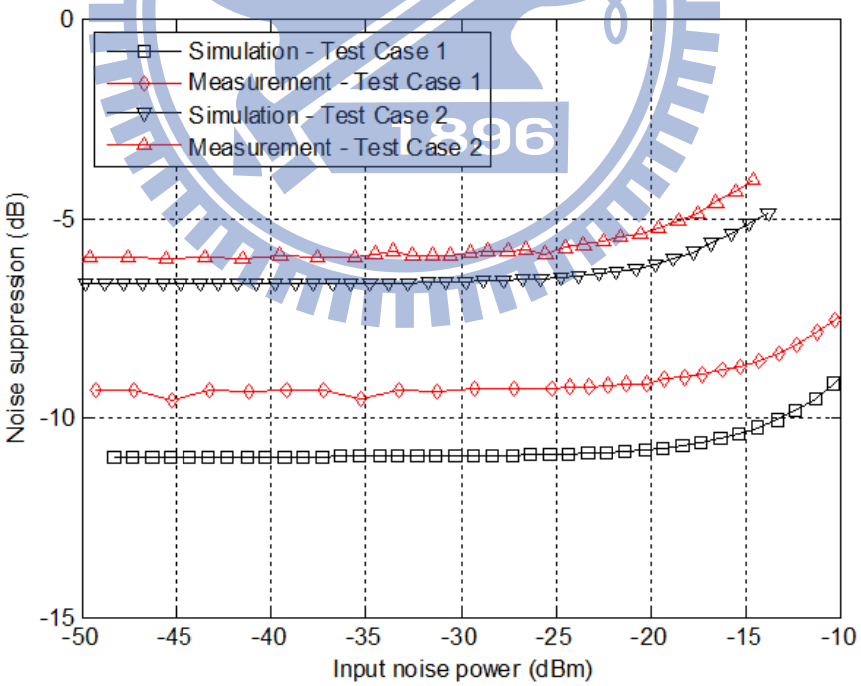


Figure 43 Simulation and measurement results of circuit noise suppression performance versus input noise power

4.5.2 Modified Version in UMC 180nm Process

As mentioned in 4.5.1.3, the high frequency performance of the proposed active guarding circuit is degraded mainly due to the poor ground plane resulting from the lack of parallel ground bonding wires on the test board. Therefore, in order to get rid of those unwanted loading effects, another tape-out is made and designed for on-wafer measurement with UMC 180nm Process.

In order to find out the real performance of the proposed active guarding technique, different test plan from last implementation is designed, which includes an Experimental Group and a Control Group in the test chip, as shown in Figure 44 and Figure 45. In Control Group, there are only noise source inputs and the noise receivers made of 10μm x 10μm P+ diffusion pick-ups with 30μm isolation distance in between. The purpose of the Control Group is to measure the isolation performance without the protection of the active guarding technique. In the Experimental Group, except the same P+ diffusion pick-ups as the noise source inputs and the noise receivers, the proposed active guarding technique including a pair of sense and injection rings and the active guarding circuit itself are used to protect the noise receiver. Signal generator is used to send signals as noises with various input powers and frequencies from -30dBm to 15dBm and from DC to 20GHz, respectively. The noise signals are coupled through the P+ diffusion pick-ups to the substrate and the noise receivers, and then measured by a spectrum analyzer via the output pads.

4.5.2.1 Implementation and results

As mentioned in 4.5.1.3, the high frequency performance of the proposed active guarding circuit is degraded mainly due to the poor ground plane resulting from the lack of parallel ground bonding wires on the test board. Therefore, in order to get rid of those unwanted loading effects, another tape-out is made and designed for on-wafer measurement with UMC

180nm Process. The layout and zoom-in view of the fabricated chip is shown in Figure 44. Four different conditions are measured as following: A. The isolation performance in Control Group; B. The isolation performance in Experimental Group, without giving any DC voltage to the active guarding circuit; C. The isolation performance in Experimental Group, give only the DC bias voltages of V_{bias1} in Figure 33, but doesn't give the supply voltage to the active guarding circuit; D. The isolation performance in Experimental Group, give all the DC voltages needed for the full operation of the active guarding circuit.

Condition A is used as a reference, which measures the isolation performance of the substrate for two P+ diffusion pick-ups placed with 30μm distance in between. As to Condition B and C, they are used to investigate the effect of the gate parasitic of transistor M_1 (in Figure 33), which is used to decouple high frequency substrate noise, in combination with both isolation performance increased by the sense and injection rings. Finally, Condition D evaluates the overall performance of the proposed active guarding technique, including the circuit performance of the active guarding circuit and the physical protection of two rings of sense and injection. The simulation and measurement results of the conditions are shown in Figure 46 to Figure 48 and will be discussed below.

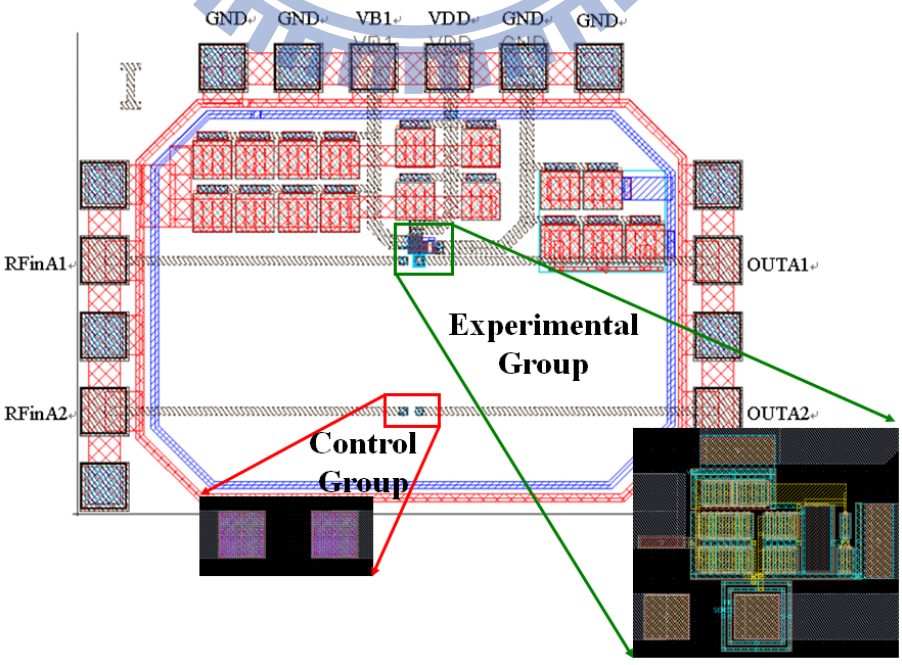


Figure 44 Layout and zoom-in view of the fabricated chip.

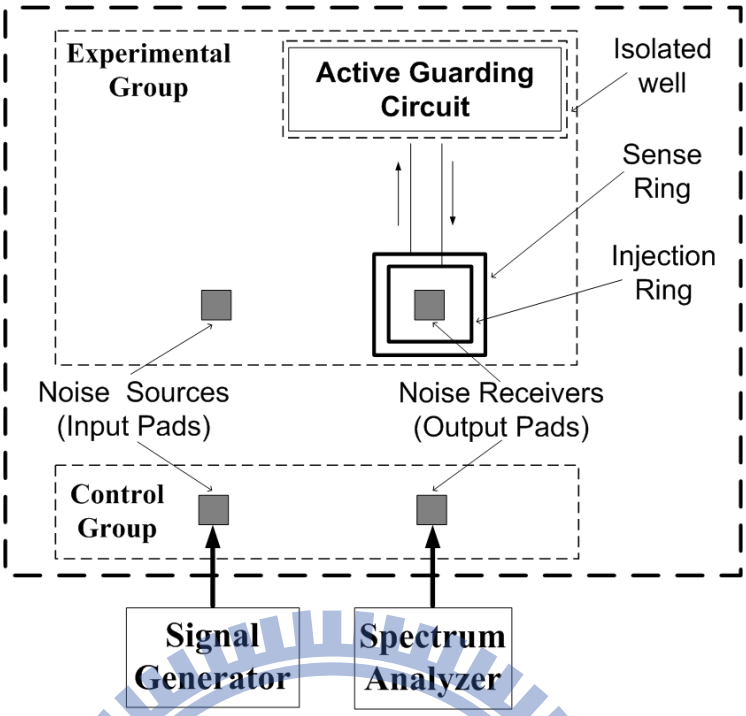


Figure 45 Test plans and measurement setup for the fabricated chip.

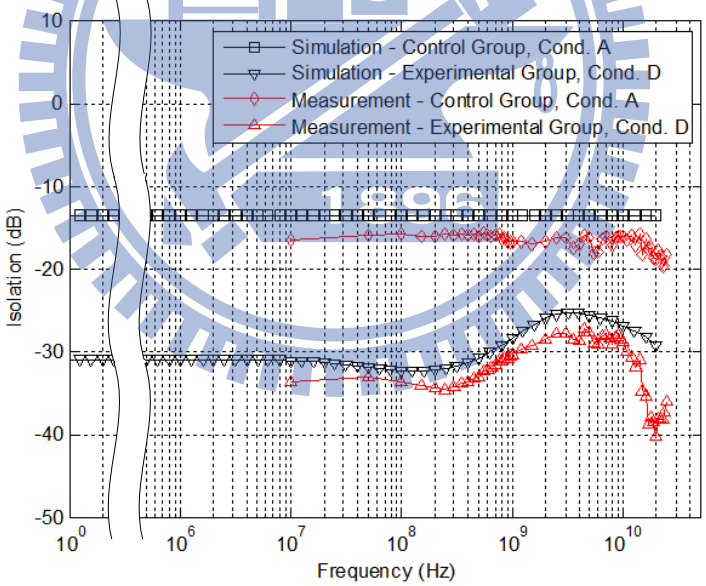


Figure 46 Isolation performances of condition A and D.

Figure 46 shows the simulation and measurement results of condition A and D in the Control and Experimental Groups. The isolation performance difference between the two conditions gives the absolute performance of the proposed active guarding technique in UMC 180nm process. As a result, the isolation performance of the proposed active guarding

technique is -18.65dB to -11dB with more than 20GHz bandwidth (from DC to more than 20GHz). The power consumption is around 2mA from 1.8V supply and the core size of the active guarding circuit is 20μm x 40μm.

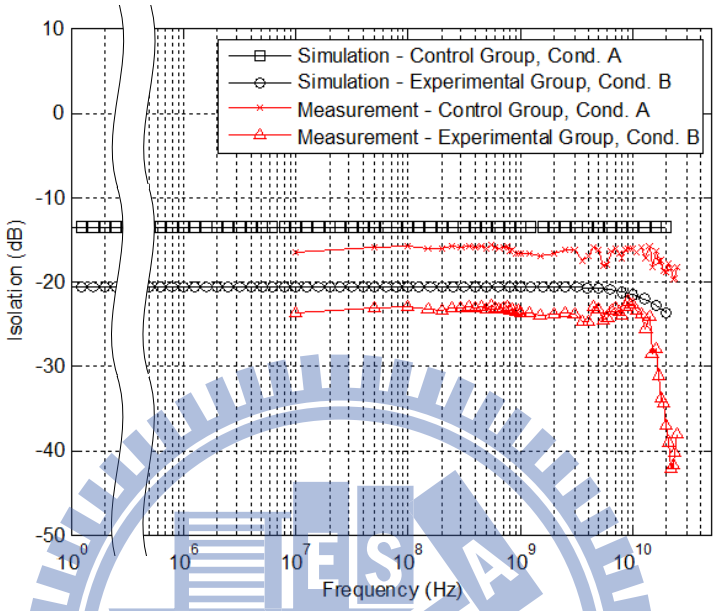


Figure 47 Isolation performances of conditions A and B

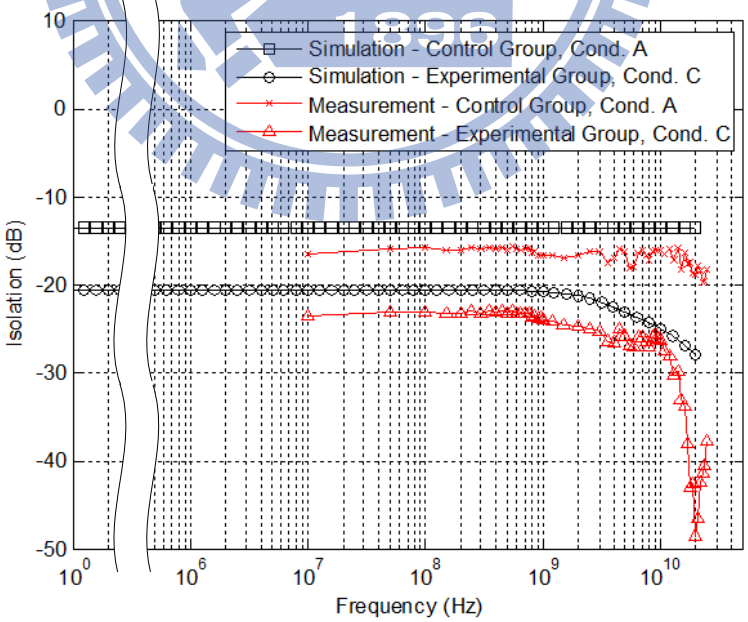


Figure 48 Isolation performances of conditions A and C.

Moreover, in order to investigate the increasing behavior of the isolation performance shown in Fig. 46, as frequency gets higher than around 9GHz; conditions of A, B and C are measured and plotted in Figure 47 and Figure 48. As shown in the pictures, we can find that actually when frequency gets higher than around 2GHz; the isolation performance starts to be affected by the parasitic capacitance of the input transistor M_1, which gives a decoupling ability that increases with the frequency. And as frequency goes higher than around 9GHz, the isolation performance will be dominated by the decoupling mechanism.

4.5.2.2 Performance Analyses and Summary

In this version, although an older CMOS technology as 180nm process is used rather than last version in 90nm process, the performance is much more improved due to a better designed ground plane. The proposed active guarding technique achieves 18.65dB to 11dB noise suppression performance from DC to more than 20GHz. In addition, different conditions are designed and tested to find out the performance contributions of the whole active guarding technique. As a result, we can find out that: first, around 7dB performance is contributed from Sense & Injection Ring. Second, the feed-forward compensation mechanism is only effective below few giga-hertz in this design. Last, from about 2GHz, the M_1's parasitic capacitance, Cgs, which is about 150fF starts to provide decoupling ability since its impedance approaches the low frequency input resistance $1/g_m$, which is about 100ohm.

The performance summary and comparison to our's and others' previous works is given in Table II. Characteristics of the power consumption, the circuit area and the wide suppression bandwidth of the proposed active guarding circuit are discussed below.

The power consumption of the proposed active guarding circuit can be expressed as equation (18).

$$VDD \times I_{Total} = VDD \times \left(I_{D1} + I_{D4} + I_{D7} \right) = VDD \times \left(2I_{D1} + I_{D7} \right) = VDD \times \left(g_{m1} \times \left(V_{GS1} - V_t \right) + \frac{1}{2} g_{m7} \times \left(V_{GS7} - V_t \right) \right), \quad (18)$$

where I_{D1}, I_{D4} and I_{D7} are the drain currents of transistor M_1, M_4 and M_7; and I_{D1} is identical to I_{D4} based on the characteristic of current mirror. From Equation (6), given the substrate impedance Z_{in_sub}, the circuit input impedance Z_{in_ckt} ($1/g_{m1}$) can be chosen according to a designed decoupling factor F_D; and g_{m7} can be determined from Equation (11); also, (V_{GS1}-Vt) and (V_{GS7}-Vt) can be easily designed in the same value no matter what technology is chosen. Therefore, all these design parameters for power consumption can be equally designed in any technologies (given that Z_{in_sub} does not vary much in different technologies). Moreover, previous researches on CMOS transistors scaling effect [50] had concluded that the transconductance-to-current ratio, i.e. g_m/I_D is almost technology independent for saturated transistors. As a result, the current consumption of the proposed active guarding circuit is almost the same over different CMOS technologies and the power consumption is thus proportional to the supply voltage for different technologies. By comparing this work with the previous literature [45] of 0.13μm process with 1.2V supply voltage, the normalized power consumption of this work (4mW/1.8×1.2 = 2.67mW) is much lower than that of [45] (9.9mW).The main contribution of the small area comes from the architecture of the proposed active guarding circuit and can be even small in advance technologies since the chip area is highly related to the process. By comparing to [45], which requires 3 high gain amplifiers and three large capacitors, this work requires only eight active devices of MOS transistors, and no area-consuming high-gain, wideband amplifiers or capacitors is needed. Therefore, to the best of authors' knowledge, this work achieves an area of 20μm x 41μm that is much smaller than any previous design. For the characteristic of wide noise suppression bandwidth, it is due to the bandwidth extension technique introduced in 4.3.2 to enhance noise suppression at giga-hertz frequency. To summarize, this work achieves the highest noise suppression

performance and widest noise suppression bandwidth with smallest area and moderate power consumption. The overall performance is achieved by the circuit architecture and mechanisms / techniques proposed. In addition, the proposed circuit benefits better performance and lower power consumption as the technology scaling down.

Table II
Performance Summary

References	Technology	Noise Suppression Bandwidth		Power	Area
		11 dB Suppression	3 dB Suppression		
This Work	UMC 0.18μm (CMOS)	DC – 20GHz	DC – 20Ghz	4mW	20μm × 40μm
T-CAD'09 [47]	0.18μm (BiCMOS)	N/A	200MHz – 600MHz	2mW	N/A (14 pF Capacitor)
T-MTT'08 [46]	90nm (CMOS)	DC – 200MHz	DC – 650MHz	2.5mW	20μm × 41μm
VLSI'05 [43]	0.35μm (CMOS)	N/A	500MHz – 600MHz	N/A	450μm x 500μm
JSSC'05 [45]	0.13μm (CMOS)	N/A	170MHz – 300MHz	9.9mW	N/A (30 pF Capacitor)
CICC'00 [44]	0.8μm (SiGe)	5MHz – 110MHz	DC – 400MHz	13.5mW	N/A

4.6 Chapter Summary

In this chapter, the design details of the proposed active guarding technique are given, including noise decoupling mechanism and feed-forward compensation mechanism which performs the phase-inversion, amplitude control and bandwidth extension. Several chips were fabricated to verify the proposed technique. Experimental results show that by employing the active guarding technique, substrate noise can be effectively suppressed in a wide frequency range from DC to 20GHz with at least 11dB noise suppression performance, at the cost of 2mA current consumption from 1.8V supply and small core area as 20μm x 40μm.

In conclusion, this is the first active substrate noise suppression circuit with wideband characteristics that is ever proposed with measurement results. As shown in Table II, the area

requirement and power consumption are the smallest, comparing to any other previous works as referenced, to the best of authors' knowledge. Moreover, the proposed circuit benefits better performance and lower power consumption as the technology scaling down. Therefore, the proposed active guarding circuit is very suitable for future applications in the industry of highly integrated SoC designs with continuous down-scaling CMOS technology.

Chapter 5

Application Verification

5.1 Introduction

In this chapter, we are going to demonstrate the proposed active guarding technique on a LC-tank oscillator. The reason to choose LC-tank oscillator as an application to verify the effectiveness of the active guarding technique is for its high sensitivity to noises and also for the common and important role of generating the reference frequency for phase-locked loop (PLL), which makes it one of the most crucial building blocks among a wireless communication system.

Two 180nm CMOS chips were fabricated for a complete experiment. The first one simply contains an active guarding circuit to evaluate the performance itself. The second chip integrates this active guarding circuit together with a LC-tank oscillator to verify the applicability for real applications. Sideband spurs and phase noise performance are measured to evaluate the effectiveness of the proposed technique.

The substrate noise coupling mechanism on a conventional LC-tank oscillator will first be briefly introduced. The experimental setup of the LC-tank oscillator with and without the protection of the active guarding technique will be explained later, along with implementation results. Chapter summary will be given in the end.

5.2 LC-Tank Oscillator and Substrate Coupling Noise Mechanisms

A conventional complementary negative transconductance LC-tank oscillator is designed in this work, as shown in Figure 49. Substrate noise can couple into the oscillator through many ways, as from the p+ contacts that connect the substrate to the on-chip ground, the active devices' back gates and also the components made of metal layers like inductors and capacitors. The dominant mechanism that converts substrate noise to the output of the LC-tank oscillator will be AM modulation of the bias transistor current due to the noise coupled to its ground. Both the AM sidebands from low frequency substrate noise harmonics and the impact of indirect AM to FM conversion due to the substrate noise on bias transistor are described in the following equation from [32]:

$$L\{\omega_m\} = S_{sub}(\omega_0 \pm \omega_m)\left(\frac{g_m^{bias}}{12\sqrt{2}I_{bias}}\right)^2\left(\frac{\omega_0}{2Q\omega_m}\right)^2 + S_{sub}(\omega_m)\left(\frac{d\omega_m}{dI_{bias}}\right)^2\left(g_m^{bias}\right)^2\left(\frac{1}{2\omega_m^2}\right) \quad (4)$$

where $S_{sub}(\omega)$ is the substrate noise signal at, ω_0 is the resonant frequency, Q is the quality factor of the tank, I_{bias} and g_m^{bias} are the current and transconductance of bias transistor, respectively.

Consequently, to minimize the substrate noise impact on the bias transistor that modulates the output of the oscillator, the active substrate noise suppression technique is applied to guard the bias transistors M_1 and M_2, thus the parameters of I_{bias} and g_m^{bias} (also g_{mb}^{bias}) of both transistors will be more stable to substrate noise. In addition, transistors M_3 and M_4 which composes the cross-coupled pair are also being protected, since they suffer from the substrate noise through their back gate that modulates their threshold voltages, too.

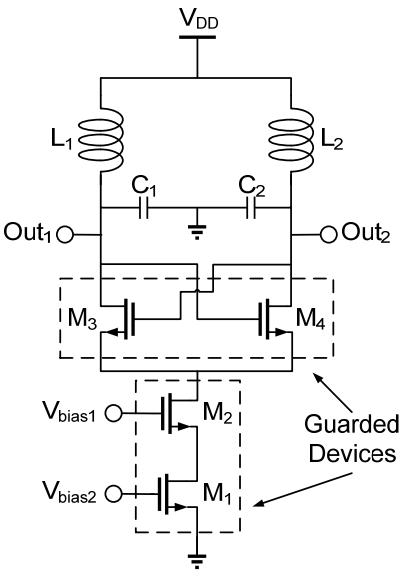


Figure 49 Schematic of the LC-tank oscillator.

5.3 LC-Tank Oscillator with Active Guarding Technique

As shown in Figure 50, an active guarding circuit and a LC-tank oscillator are integrated in a single chip to evaluate the effectiveness of the proposed technique on real applications. The LC-tank oscillator is verified with measurement results to operate at 1GHz and offers a phase noise performance of more than -95dBc/Hz at 100kHz offset frequency. It consumes 1.1mA from a 1.8V supply.

Two different kinds of noise sources are applied for the experiment. Noise source 1 (NS1) injects single tone signals from an external source as signal generator into the substrate through substrate taps, with 15μm distance from the guarded devices. Noise source 2 (NS2) is the digital signal output from an on-chip inverter chain, which is commonly used as clock buffers, for the emulation of the substrate noise source in practical cases. The output of the inverter chain is fed to the substrate with 25μm distance from the guarded devices, through a 5pF capacitor to pass signals below several giga-hertz and also to block the DC signal from interfering the substrate. Noise frequencies of either low as 100kHz to 10MHz or high as

around the resonant frequency of 1GHz are injected to the substrate to see the impact of substrate coupling and the suppression ability of the active guarding circuit.

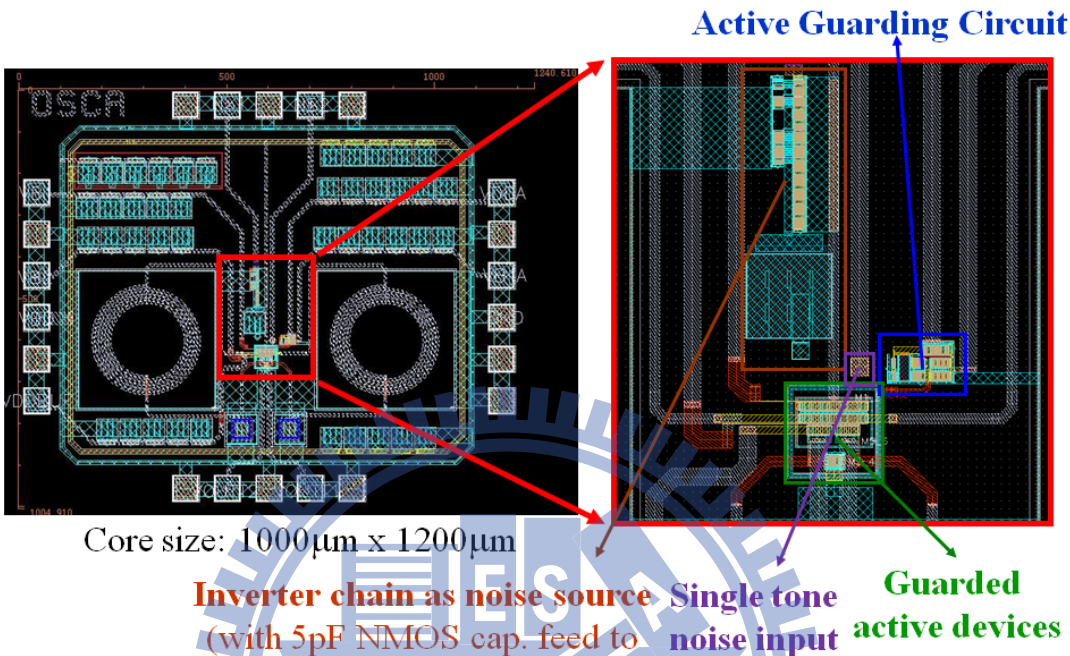


Figure 50 Layout and zoom-in view of the fabricated chip.

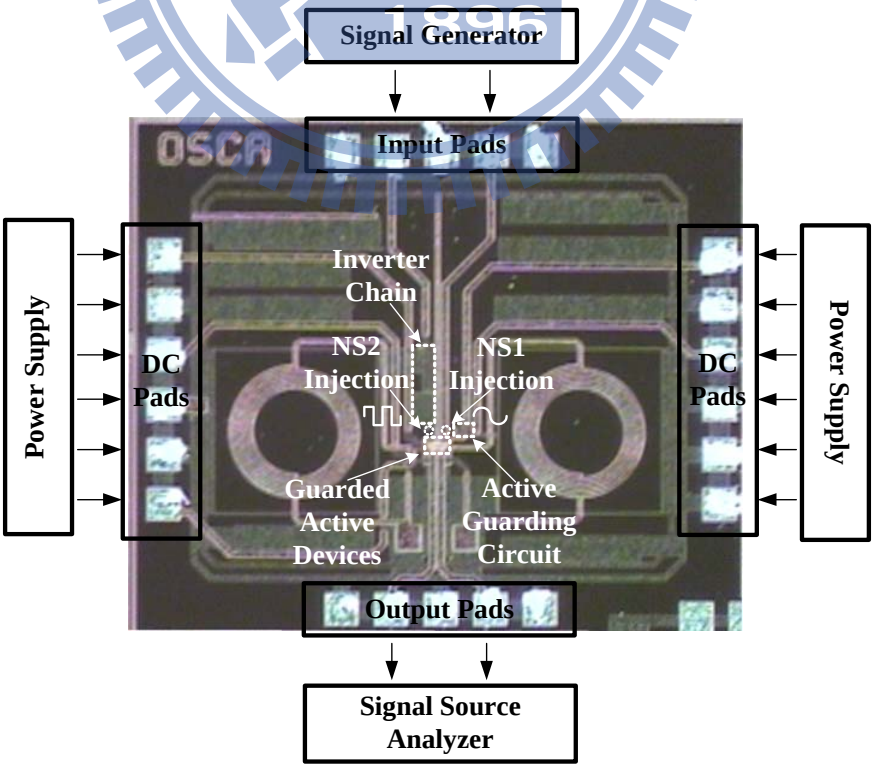


Figure 51 Layout and experimental setup of the fabricated chip.

5.4 Implementation and Results

To evaluate the effectiveness of the active guarding technique on LC-tank oscillator, the phase noise and sideband spurs are measured under three different conditions as follows:

- Original: The active guarding circuit is off and no noise is injected.
- CKT-OFF: The active guarding circuit is off and noise is injected either from NS1 or NS2.
- CKT-ON: The active guarding circuit is on and noise is injected either from NS1 or NS2.

The performance of the active guarding technique is obtained by comparing the performance differences between Original, CKT-OFF and CKT-ON for noise injections of various frequencies. For low frequency range of interested, experimental results of 100 KHz and 10 MHz single tone noise injections from NS1 with -5 dBm input power are presented from Figure 52 to Figure 57 as examples. As shown in Figure 52, the original phase noise at 100kHz is -98.59dBc/Hz. After a single tone noise at 100kHz is injected from NS1, a corresponding spurs at 100kHz offset showed and the phase noise performance becomes -69.66dBc/Hz at 100kHz, as shown in Figure 53. By switching the active guarding circuit on, the phase noise performance at 100kHz becomes -88.47dBc/Hz in Figure 54, which shows an 18.81dB improvement. Figure 55 shows another measurement with around -142dBc/Hz original phase noise at 10MHz. After a single tone noise at 10MHz is injected from NS1, a corresponding spurs at 10MHz offset showed and the phase noise performance becomes -117.29dBc/Hz at 10MHz, as shown in Figure 56. By switching the active guarding circuit on, the phase noise performance at 10MHz becomes -134.02dBc/Hz in Figure 57, which shows a 16.73dB improvement. To be mentioned, two spurs in 60kHz and 70kHz in Figure 52 to Figure 57 are not resulting from substrate noise therefore cannot be suppressed. Similar results are obtained for noise frequencies between 100kHz to 10MHz.

For high frequency experiments, here we show a result of the noise injection from NS2 as an example since the phase noise degradations due to the injections of digital noise are more severe than single tone noise for the same frequencies. A 990MHz high frequency noise, which is close to the resonant frequency of the oscillator, is injected to the substrate from NS2 as a digital noise to see the phase noise performance difference. Noise amplitude which reaches the guarded devices in the oscillator is calculated to be around 30mV to emulate the actual possible substrate noise.

Wireless standard of DCS-1800 is chosen as an example application for the oscillator design thus both transmission (Tx) and reception (Rx) spurious suppression specifications calculated in [51] are being plotted in Figure 58 for comparison. As shown in the figure, the oscillator output is suffered from AM/FM modulations and the puling effect by the injected noise that the phase noise performance are degraded seriously therefore failed to fulfill the mask specifications of both Rx and Tx, from offset frequencies of 500kHz and 1.1MHz, respectively. After the active guarding circuit is switched on, the pulling effect is reduced hence the phase noise performances are improved substantially to pass both Tx and Rx spurious suppression masks in the whole frequency range of interest.

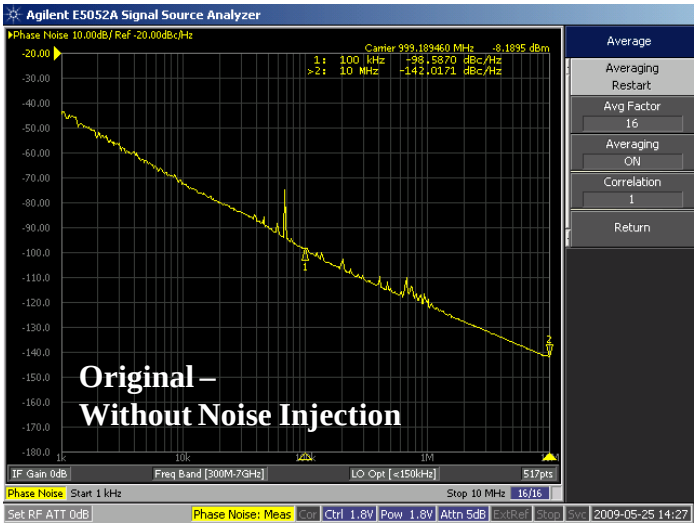


Figure 52 Measurement results – without noise injection.

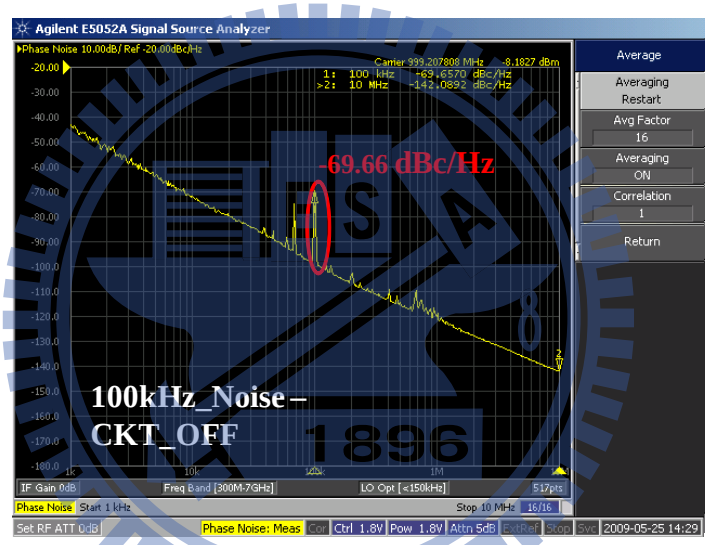


Figure 53 Measurement results – 100kHz noise injection, circuit off.

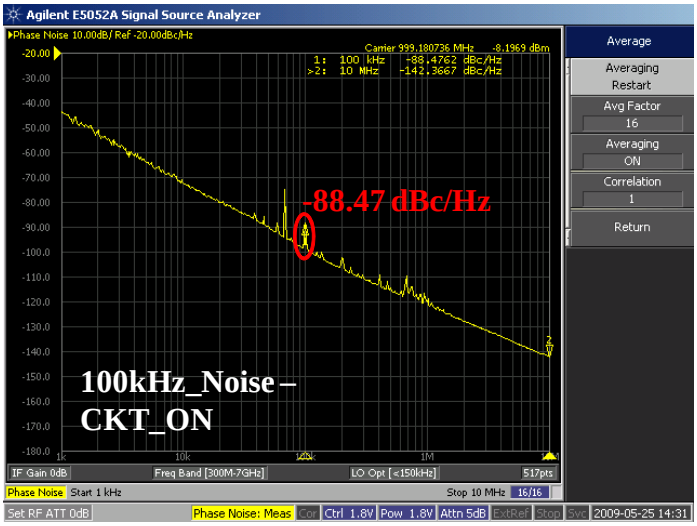


Figure 54 Measurement results – 100kHz noise injection, circuit on.

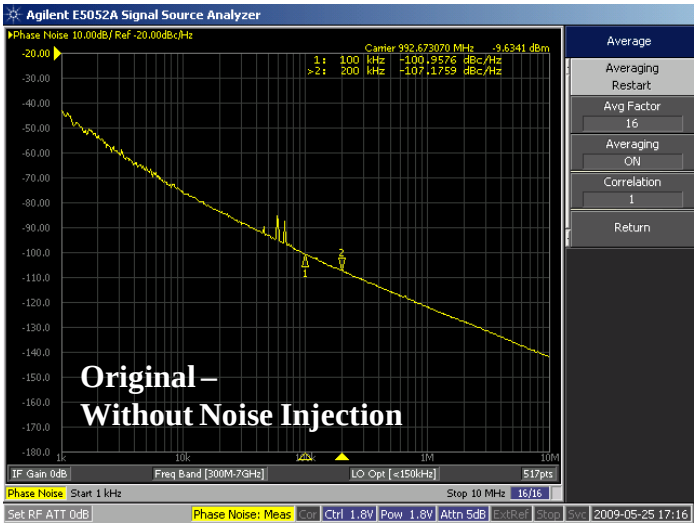


Figure 55 Measurement results – without noise injection.

Figure 56 Measurement results – 10MHz noise injection, circuit off.

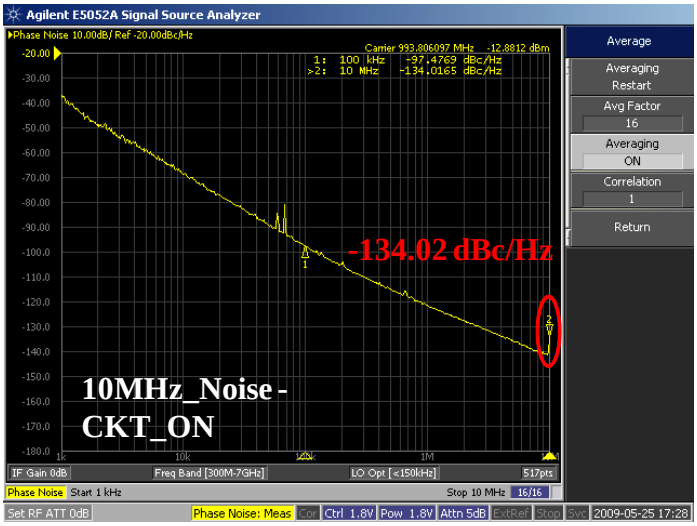


Figure 57 Measurement results – 10MHz noise injection, circuit on.

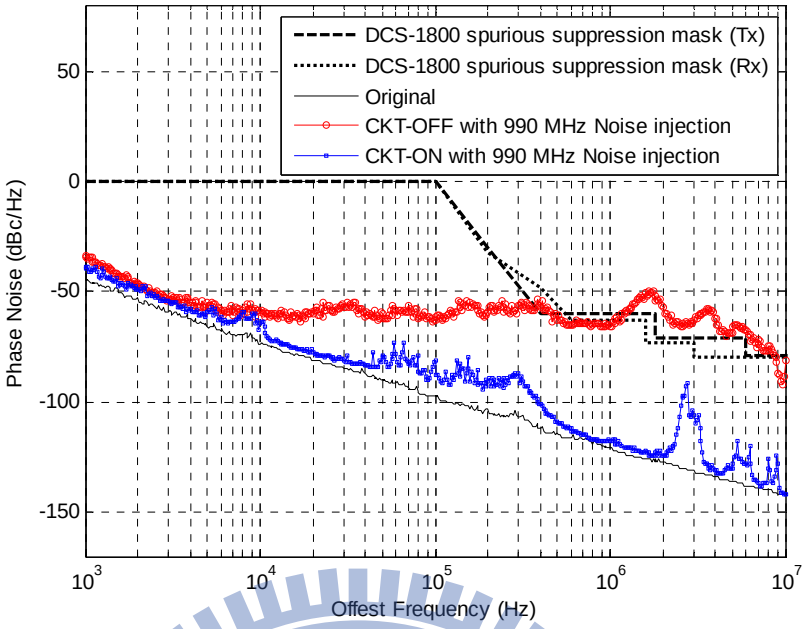


Figure 58 Comparison of the phase noise differences among the Original/CKT-ON/CKT-OFF after 990MHz noise injection from NS2 with DCS-1800 spurious suppression masks.

5.5 Chapter Summary

In this chapter, we demonstrate the active guarding technique to improve the substrate noise immunity on analog/RF circuits with real application. By applying the active guarding circuit to a LC-tank oscillator, more than 16.73dB spur suppression performance is obtained in the frequency range of interest as either low frequencies below 10MHz or high frequencies around the resonant frequency of 1GHz. As a result, the 1GHz oscillator can fulfill the spurious suppression masks of DCS-1800 even in the adjacent of 990MHz strong noise signals.

Chapter 6

Conclusions and Future Works

This dissertation presents a new active guarding technique for wideband substrate coupling noise suppression in SoC applications. We surveyed on substrate noise issue in mixed-signal integrated circuits. The generation and propagation mechanisms of substrate noise are briefly introduced; the experimental results of substrate coupling noise impact on analog/nixed-signal and RF circuits including LNA, Oscillator, ADC and DAC selected from other people's works are also presented to show the performance degradations in real cases. After knowing the seriousness of substrate coupling noise problem, we also investigated on substrate coupling noise suppression techniques. Existing techniques are classified into passive and active methods; for passive methods, test-keys of different guard ring schemes are designed, fabricated and measured to see the effectiveness of the conventional physical methods. Substrate characterization is also done for further utilizations. For active methods, we selected five different techniques from published papers, showed their way of implementation and then made comparisons. In the end, we proposed a new technique that takes both the advantages of passive and active methods, which includes noise decoupling and feed-forward compensation mechanisms. The detailed of design, analyses and implementation of this technique are given. By employing this technique, wideband substrate noise suppression up to giga-hertz range can be achieved. The final circuit implementation results in UMC 180nm CMOS technology show that more than 14dB noise suppression performance is achieved in a wide frequency range from DC to 1GHz and 11dB until 20GHz, by the cost of a small chip area of 20μm x 40μm and 2mA current consumption from a 1.8V supply. This is

the first active substrate noise suppression circuit with wideband characteristics that is ever proposed with measurement results. Moreover, the proposed technique benefits better performance and lower power consumption as the technology scaling down. Therefore, the active guarding circuit is very suitable for future applications in the industry of highly integrated SoC designs with continuous down-scaling CMOS technology. To prove the feasibility on real applications, the proposed active guarding technique is demonstrated for substrate immunity improvement on LC-tank oscillators. Experimental results showed that by applying the active guarding technique to a LC-tank oscillator, more than 16.73dB spur suppression performance is obtained in the frequency range of interest as either low frequencies below 10MHz or high frequencies around the resonant frequency of 1GHz. As a result, the 1GHz oscillator can fulfill the spurious suppression masks of DCS-1800 even in the adjacent of 990MHz strong noise signals.

We have presented a new technique for wideband substrate noise suppression with best performance among the previously published papers. However, the drawback to use this technique is: the design of an active guarding circuit always needs a parameter extracted from the substrate. As shown in Equation (6), (8) and (11), the design of the decoupling factor and the amplitude controller depends on the parameter Z_{in_sub}, which is extracted from the substrate. Consequently, if a user wants to design an active guarding circuit for a certain technology, they need to get the substrate model first. In our case, we have cooperation with UMC, which enable us to access process information such as thickness of subdivisions, junction capacitances parameters and material characteristics and use Assura-RF^{TM} with that information to extract substrate networks between devices. Unfortunately, not all users can get the process information easily. As a result, how to obtain a precise substrate model becomes an important issue for the implementation of the proposed active guarding circuit.

To sum up, as a future work to implement the proposed technique in an organized and uniformed way, we suggest successors to construct a more efficient and systematic simulation

platform for accurate substrate network modeling; then to include the active guarding circuit design in the design flow. The final goal could be an automatic design of active guarding circuit for every technology and to use it as the use of Electrostatic Discharge (ESD) cell to protect the sensitive circuits in a SoC chip. For reference, a study has been done in [13] to compare the possible solutions nowadays for substrate modeling.

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