應用於寬頻與超寬頻接收機之金氧半互補式非對稱源極電感退化之低雜訊放大器分析與設計

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中文摘要

由於共源極組態常被用於寬頻低雜訊放大器的設計。在此論文中，具備電阻－電感－電容(*R-L-C*)之共源極電路的輸入阻抗有完整的分析。基於共源極組態的知識，此論文題出一個創新的設計方法，此方法採用互補式電晶體架構搭配源極退化電感，其可達到寬頻的輸入阻抗匹配與低雜訊指數。模擬的輸入阻抗與理論預測的輸入阻抗非常相近，此驗證了輸入阻抗的分析的正確性。此創新架構的雜訊指數也被正確的分析解釋與探討。此外，對於互補式組態的優劣在文中也被公平的探討與比較。為了驗證此電路的可行性，三顆寬頻匹配低雜訊放大器以台積電 0.18um 之 CMOS 製程來設計:其中兩個電路頻段是 3-10GHz，另一個是 8-25GHz。值得注意的是，互補式寬頻低雜訊放大器有 20dB 增益, 2.4 - 3.4dB 雜訊指數並消耗了 25.65mW 之功率消耗，當與其他寬頻低雜訊放大器做比較，此電路有非常好的效能與優化指數(FOM)。最後，基於此篇論文的架構，我們提出了一個新型的共源極電路，此電路在 70-100GHz 可以降低雜訊指數達 2-4dB 之多。因此此論文所提出的技術也能夠應用在毫米波的系統之中。

Analysis and Design of a Novel CMOS Complementary Low Noise Amplifier using Asymmetrical Source Degeneration for Wideband and Ultra-Wideban Receiver

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ABSTRACT

Since common-source topology is frequently adopted to design a wideband LNA. In this dissertation, input impedance of a common-source transistor circuit with *R-L-C* loading network is completely analyzed. Based on the knowledge of the common source topology, this dissertation proposes a novel LNA design method where the complementary transistor topology is combined with asymmetrical inductive source degeneration to achieve matched

input impedance and low noise figure over a wide bandwidth. The validity of this new approach is supported by the agreement between the simulated input impedance of the LNA and their calculated counterpart. Also, the noise figure of the newly proffered topology is accurately analyzed and well explained. And, the pros and cons of the complementary topology are fairly addressed. To demonstrate the feasibility, three wideband matched LNA's are designed using TSMC 0.18-μm RF-CMOS process: two are for 3−10GHz application and the other 8−25GHz. Specifically, the ultra-wideband complimentary LNA has superior performance: matched input impedance, 20dB power gain, and 2.4–3.4dB noise figure, with 25.65mW power consumption. Compared with other CMOS LNA's, the proposed complimentary LNA has superior performance. Finally, to demonstrate the proposed input matching technique is suitable in millimeter wave applications, we propose a modified source inductively generated common-source transistor circuit, which can greatly improve the noise figure up to 2-4dB at W-band (70-110GHz) compared to the conventional source inductive degenerated common-source amplifier with a gate inductor.

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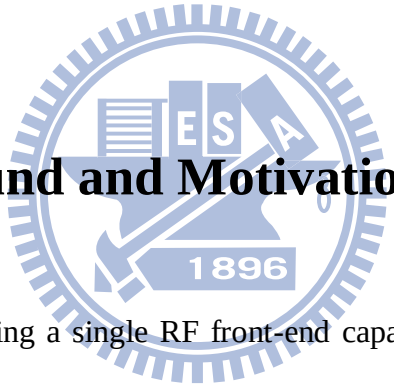
Introduction



1.1 Background and Motivation

The challenge of building a single RF front-end capable of receiving and processing a multiplicity of bands (e.g., for a software-defined radio) has stimulated interest in broadband RFIC design. This has arisen in response to the potential complexity, cost and power consumption of portable wireless devices designed to incorporate new wireless standards and applications, while maintaining backward compatibility with existing standards and capabilities. Concurrently, the potential of ultra-wideband (UWB) radio for high data transfer rates (up to 1Gb/s) within short distances (10m) has also sparked research activity in broadband RF circuits and systems. Ultra-wideband radio requires an integrated

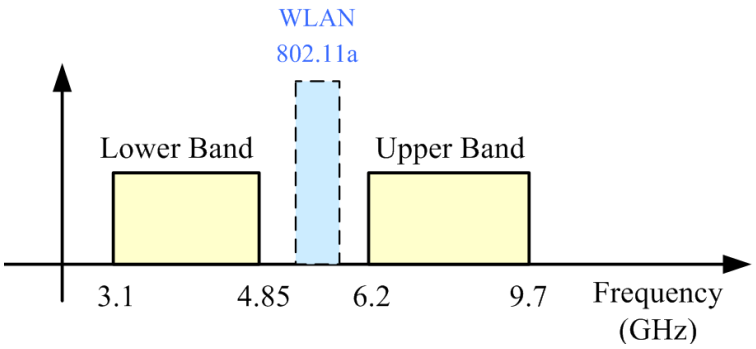


Fig. 1-1 DS-UWB spectrum allocation

low-cost RF front-end with multi-GHz bandwidth, operating at the lowest power consumption and supply voltage. Broadband low-noise RF amplifiers (LNAs) are therefore required for a multiband/multi-standard RF front-end, UWB radio or perhaps both (e.g., a multiband/multi-standard receiver with UWB capability). Reducing the number of LNAs by reducing the number of RF receive paths could drastically reduce power consumption, chip size, and cost in a multiband/multi-standard radio. However, at present it is unclear how multiple antennas and preselect filter paths can best be multiplexed efficiently to a single LNA input. Nevertheless, the wideband LNA must offer robust RF performance (i.e., gain and dynamic range) over many gigahertz of bandwidth with levels of current consumption comparable to existing narrowband amplifiers.

When considering short-range, high bit-rate wireless communication using ultra-wideband technology, two competing standards: multiband orthogonal frequency division multiplexing (MB-OFDM) and impulse-based direct sequence code division multiple access (DS-CDMA) have been proposed for standardization [1], [2]. The DS-UWB supports data communication using both BPSK and 4-BOK. DS-UWB supports two independent bands of operation. The lower band occupies the spectrum from 3.1-4.85GHz and the upper band occupies the spectrum from6.2-9.7GHz, as shown in Fig.1. In Multi-Band-OFDM (MB-OFDM) UWB, the

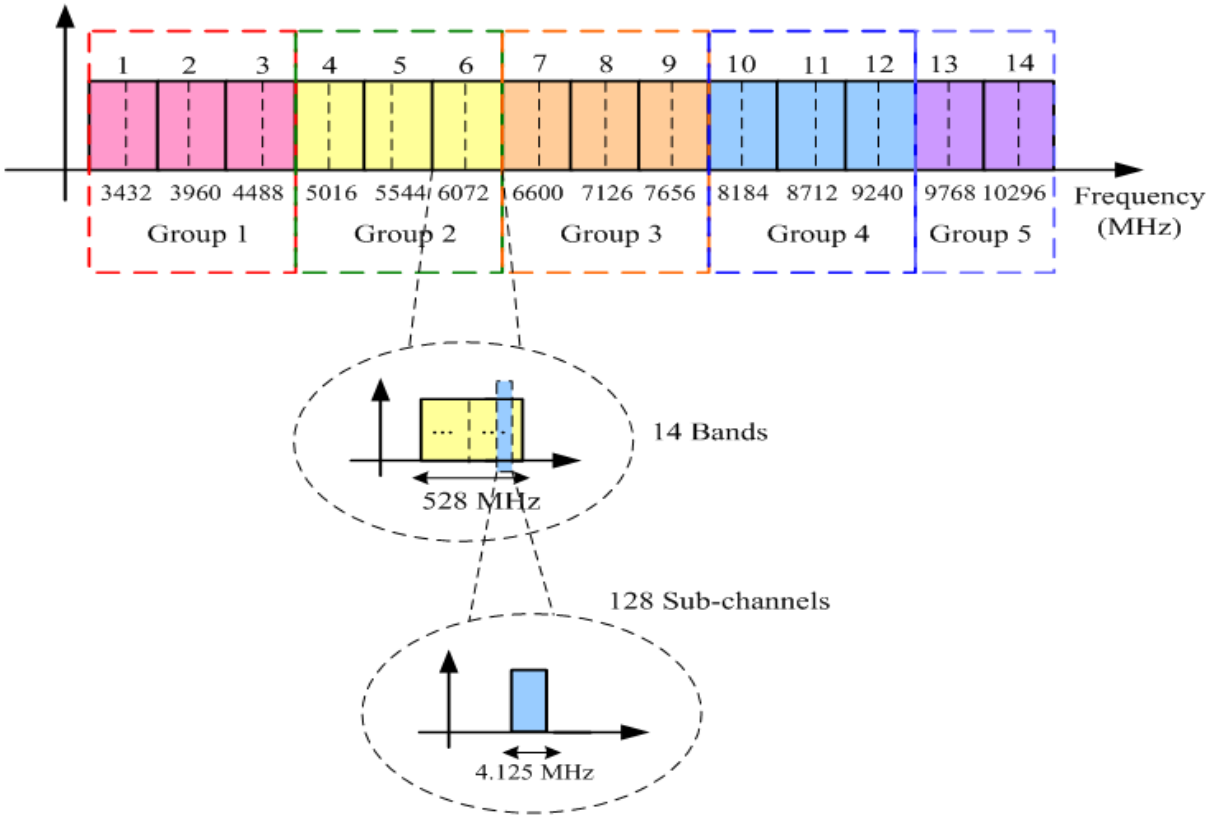


Fig. 1-2 MB-OFDM UWB spectrum allocation

7500-MHz bandwidth is divided into 5 major Band Groups which are in turn sub-divided into 14 bands in total and each band is 528MHz bandwidth and each band includes 128 sub-channels, sub-channel is 4.125 MHz as shown in Fig.2. Further, different bands proposed for North America (3.1–4.8 GHz), Europe (6–8.5 GHz) and Japan (3.4–4.8 GHz, 7.25–10.25 GHz) complicate the pursuit of a low-cost, generic design, unless the design encompasses all regional bands with adaptively control. Important specifications for the LNA include input power matching, low noise figure and distortion, power gain and minimum gain variation. However, unlike narrowband circuits, these specifications must be consistent and satisfied over the entire frequency range, which is 3.1–10.6 GHz for operation in all regions of the world.

1.2 Wideband Amplifier Review

This section reviews the state-of-the-art broadband and UWB low-noise amplifiers, and outlines the advantages and disadvantages with respect to power consumption and noise performance of common gate amplifiers, noise-canceling amplifiers. Using the familiar Friis formula to calculate the total noise figure for the amplifier, clearly, the first stage of a low noise amplifier plays the significant role with respect to the noise figure and input impedance matching. Therefore, throughout this thesis, we focus on the input matching analysis and noise analysis of the first stage.

Recently, the common-gate LNA topology is attractive because the resistive input impedance match is realized by the input transistor as its input impedance is $1/g_m$. The common-gate topology possesses superior broadband input match, linearity, stability [40]-[44]. However, its noise factor is sacrificed to equal the input impedance, $1/g_m$, with the microwave 50Ω. To evaluate this point, consider a basic common-gate LNA, as shown in Fig. 1-3 (a), where the dominant noise sources are the channel noise current, $i_{n,s}$, of the source resistance and the drain current noise, $i_{n,d}$, of the MOSFET while the induced gate noise is neglected to simplify the derivation of the noise figure of a common-gate LNA circuit. The noise factor can be derived as:

$$F = 1 + \frac{\overline{i_{n,d}^2}\left(\frac{1}{1+g_m R_s}\right)^2}{i_{n,s}^2\left(\frac{g_m R_s}{1+g_m R_s}\right)^2} = 1 + \frac{\overline{i_{n,d}^2}}{\overline{i_{n,s}^2}}\left(\frac{1}{g_m R_s}\right)^2 \qquad (1\text{-}1)$$

To render the input impedance the microwave 50Ω, here R_s, $g_m R_s$ is approximated as one.

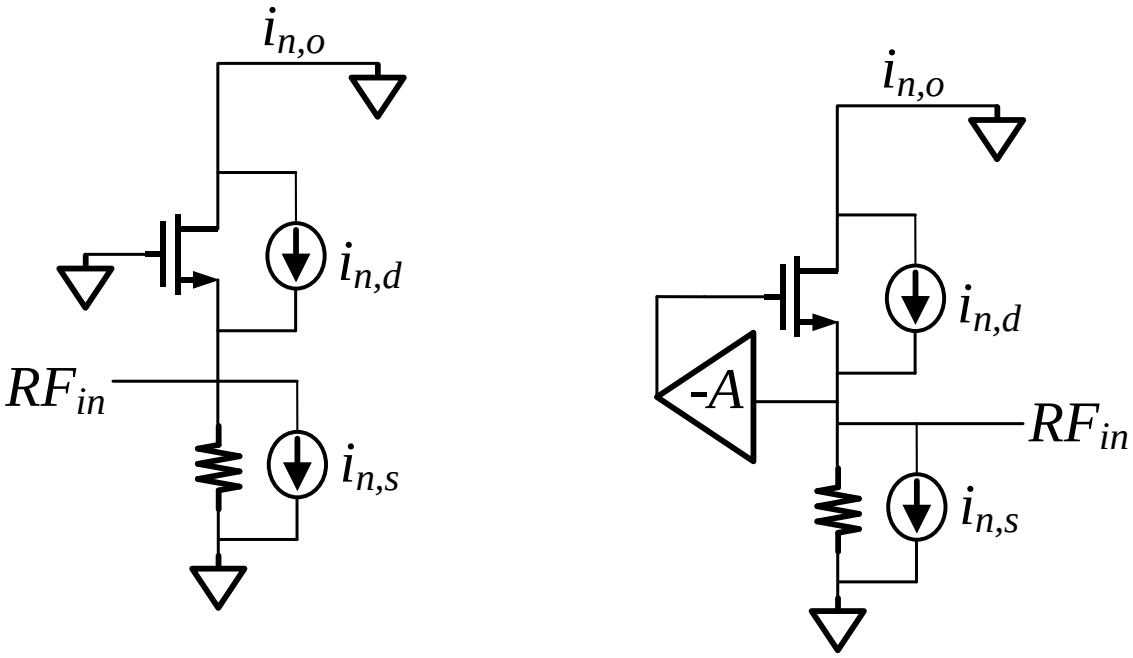
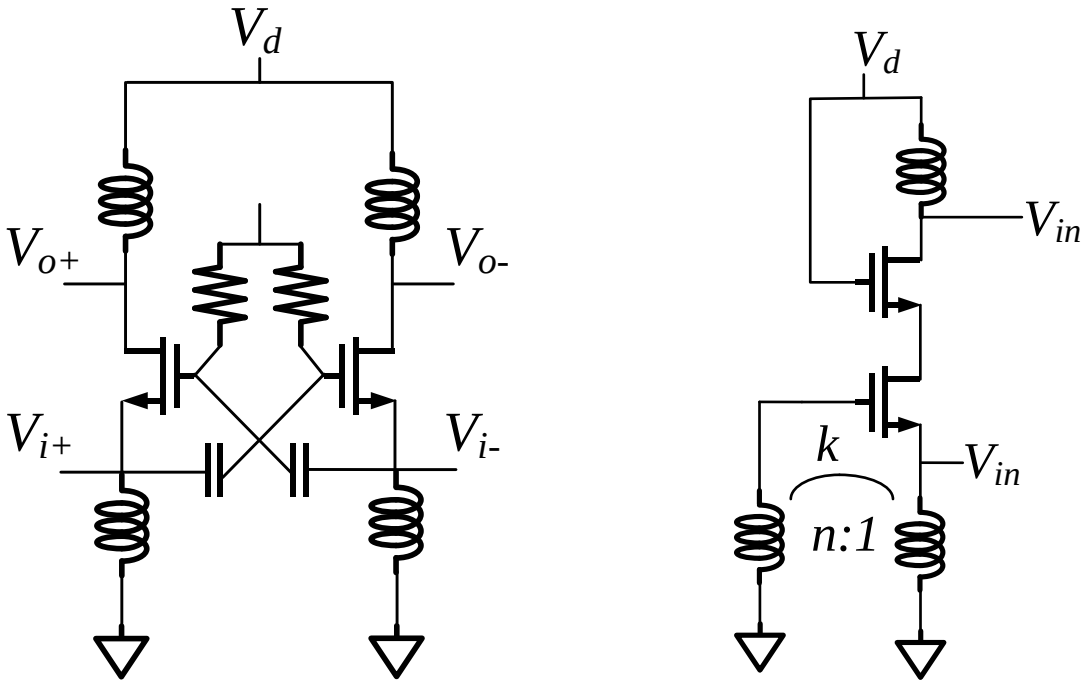


Fig. 1-3. (a) Conventional common-gate amplifier, and (b) g_m-boosted common-gate amplifier.

Thus the noise factor is simplified as

$$F = 1 + \frac{\overline{i_{n,d}^2}}{\overline{i_{n,s}^2}} \tag{1-2}$$

The analysis above implies that the transconductance of the first-stage transistor cannot be increased arbitrarily to reduce the noise factor, and the noise figure has its limit. To improve the noise performance, an inverting gain, -A, is inserted between gate and source terminals as shown in Fig. 1-3 (b), the effective g_m is boosted to (1+A) g_m, and the noise factor is consequently reduced to



(a) (b)

Fig. 1-4. (a) Capacitor cross-coupled common-gate amplifier, and (b) transformer g_m-boosted common-gate amplifier.

$$F = 1 + \frac{\overline{i_{n,d}^2}}{\overline{i_{n,s}^2}} \left(\frac{1}{(1+A) g_m R_s} \right)^2 \tag{1-3}$$

Note that the new structure provides the same resistive input impedance using less bias current in accordance with $(1+A)g_mR_s = 1$. There are several possible ways to implement the inverting gain, as shown in Fig. 1-4. The capacitor cross coupling technique of Fig. 1-4(a) has the inherent required inverting gain, -A, in the differential configuration. However, it has two drawbacks: it consumes twice the bias current and silicon area as its single ended counterpart, and "A" is always less than one due to the capacitor divider between the intrinsic gate-to-source capacitors C_{gs} and coupling capacitance C_c. What is more important is the

lossy large input inductor will deteriorate the noise figure greatly. Besides, the need of the external wideband balun brings about the additional noise figure degradation. Another technique implementing "A" is constructed by the magnetic coupling, i.e. transformer, as shown in Fig. 1-4 (b). However, to lower the noise figure while keep the input reflection coefficient lower than -10dB, the large values of coupling coefficient *k* and the turn ratio *n* is desired. Unfortunately, the desire of high turn ratio *n* leads to use of large inductor, which will inevitably deteriorate the noise figure.

The analysis above reinforces the notion of a tight link between input matching and noise factor in a common-gate LNA. To decouple the input matching from the noise figure, noise cancellation is proposed to cancel the output noise generated from the matching device [15], [45]. Fig. 1-5 illustrates an example, which is based on a common-gate LNA. The input matching is accomplished by setting $1/g_m$ to 50Ω. The principle of noise cancellation in Fig. 1-5 can be briefly explained as follows. The input signal, say, a current denoted by solid line, undergoes feed-forward voltage amplification by transistors M_3 and M_4 whereas the channel thermal noise of transistor M_1, the dotted signal, undergoes subtraction at output node due to two correlated but out-of-phase noise voltages at V_x and V_1. At frequencies well below f_T, the condition for complete noise cancellation is derived as

$$I_{n,out} = \frac{I_{n,M1}}{1+g_{m1}R_s} R_{L1} g_{m2} - \frac{I_{n,M1}}{1+g_{m1}R_s} R_s g_{m3} = 0$$
$$\rightarrow \qquad (1\text{-}4)$$
$$R_{L1} g_{m2} = R_s g_{m3}$$

while the equivalent transconductance, G_m, is found to be

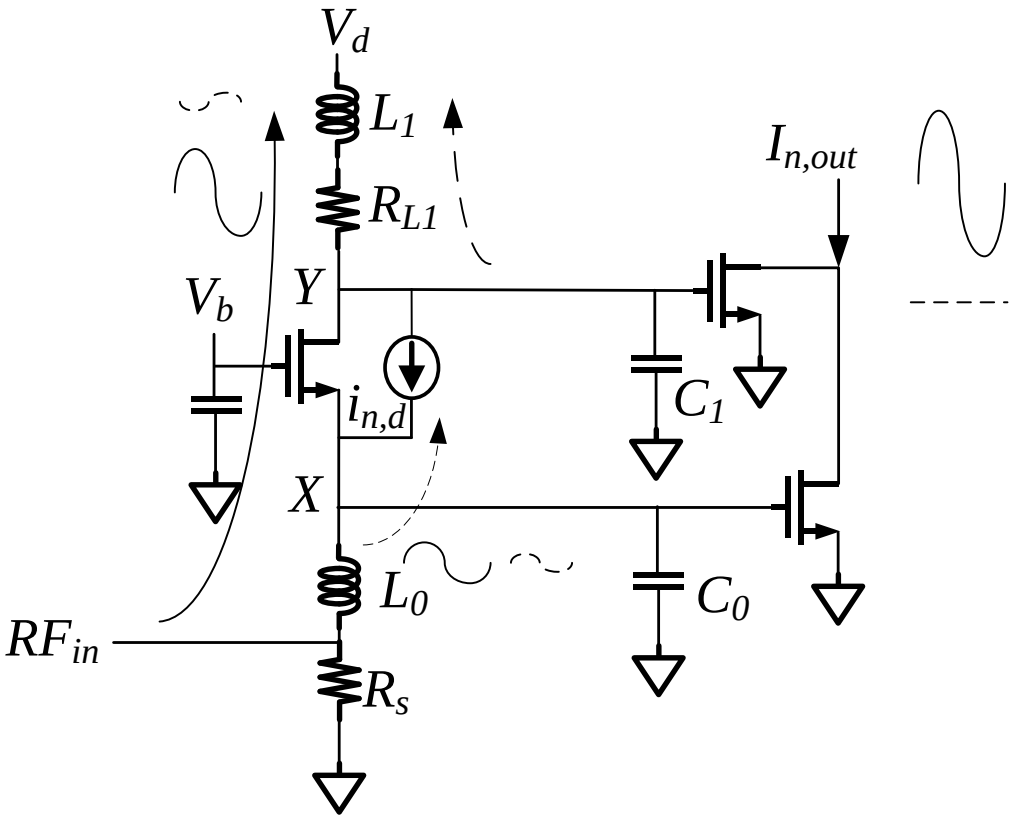


Fig. 1-5. Noise canceling common-gate amplifier.

$$G_m = \frac{1/g_{m1}}{R_s + 1/g_{m1}}\left(g_{m1}R_{L1}g_{m2} + g_{m3}\right) \tag{1-5}$$

Compared to common-gate amplifiers, the noise factor contributed by the matching device is now fully decoupled with the input matching condition. As for the wideband or high frequency applications, it is unavoidably use shunt-peaking inductor L_1 to extend the gain bandwidth. Here, to cancel the noise generated by input device M_1 over a wide bandwidth, the cancellation condition can be obtained as,

$$I_{n,out} = \left(g_{m2}Z_{L1} - g_{m3}Z_S\right)\frac{I_{n,M1}}{1+g_{m1}Z_s}$$

$$= \left(g_{m2}R_{L1}\frac{1+sL_1/R_{L1}}{L_1C_1s^2+C_1R_{L1}s+1} - g_{m3}R_s\frac{1+sL_0/R_s}{L_0C_0s^2+C_0R_ss+1}\right)\frac{I_{n,M1}}{1+g_{m1}Z_s} \tag{1-6}$$

From (1-4) and (1-6), the cancellation condition can be derived as

$$\frac{R_{L1}}{R_S} = \frac{L_1}{L_0} = \frac{C_0}{C_1} \tag{1-7}$$

Since L_0 accounts for the input matching while L_1 for gain bandwidth peaking, thus L_1 is large to extend the gain bandwidth while L_0 is small for not affecting the input matching mechanism by M_1; thus a large value of R_{L1} is necessary to meet (1-7). However, the large value R_{L1} will greatly deteriorate the noise figure of an amplifier especially at low frequency range. Further, mismatch and parasitic effects limit the performance of the technique, and the effective bandwidth of noise cancellation is limited. In conclusion, though channel thermal noise of the input device M_1 can be cancelled out by the noise canceling technique, the large resistor R_{L1} and the extra-added transistor M_3 impose additional noise source into the amplifier, thus low noise figure cannot be obtained.

Thus far, we have explained the advantage and disadvantage of the common-gate amplifier and the associated noise cancelling technique. It is obviously that the common-gate based configuration still suffers low power gain, and high noise figure. Therefore, to render an amplifier a low noise figure with high gain, and low power consumption, we will design a LNA with a common-source based configuration.

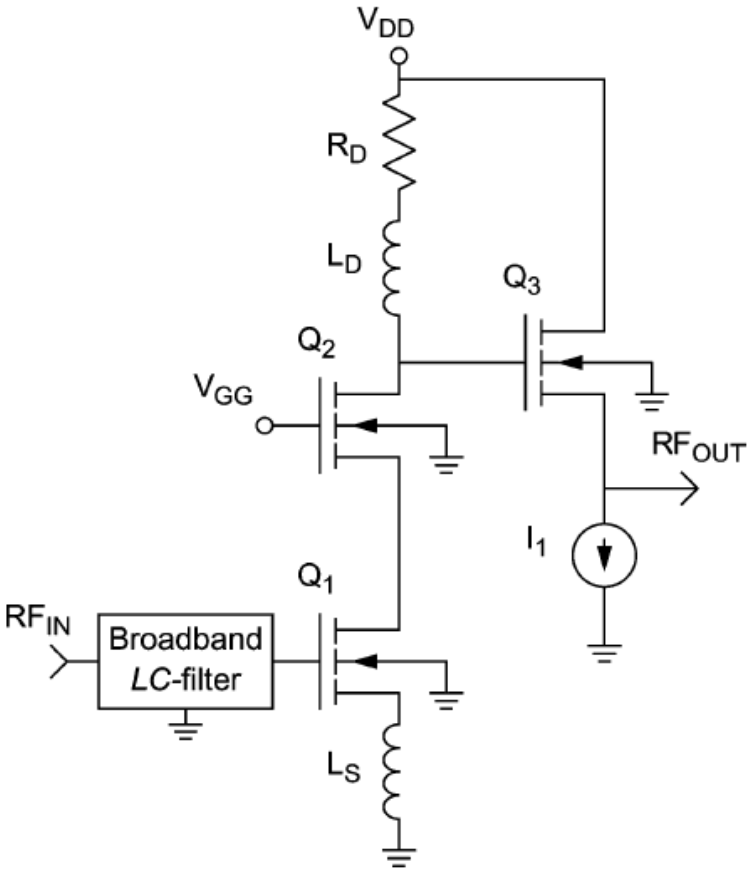


Fig. 1-6. Cascode amplifier.

Recently reported LNAs designed for the 3–10 GHz UWB have been implemented in both feedback [46], [49] and non-feedback configurations [47]–[48]. The designs described in [47]–[48] are adaptations of narrowband LNAs, which use a cascade core and a multistage input filter for broadband matching of the core amplifier to a 50Ω source (see Fig. 1-6). However, the input filter's insertion loss degrades the amplifier's noise figure greatly, and this loss must be compensated for by increasing the gain, thereby lowering bandwidth. An additional compromise in this design is the source follower output buffer used as a low output impedance (i.e., 50Ω) interface. The follower consumes additional DC power (e.g., 5 mA [47]) and constrains dynamic range, bandwidth, and interfacing to a mixer stage.

An alternate approach to the modified cascode is a negative-feedback amplifier. Feedback

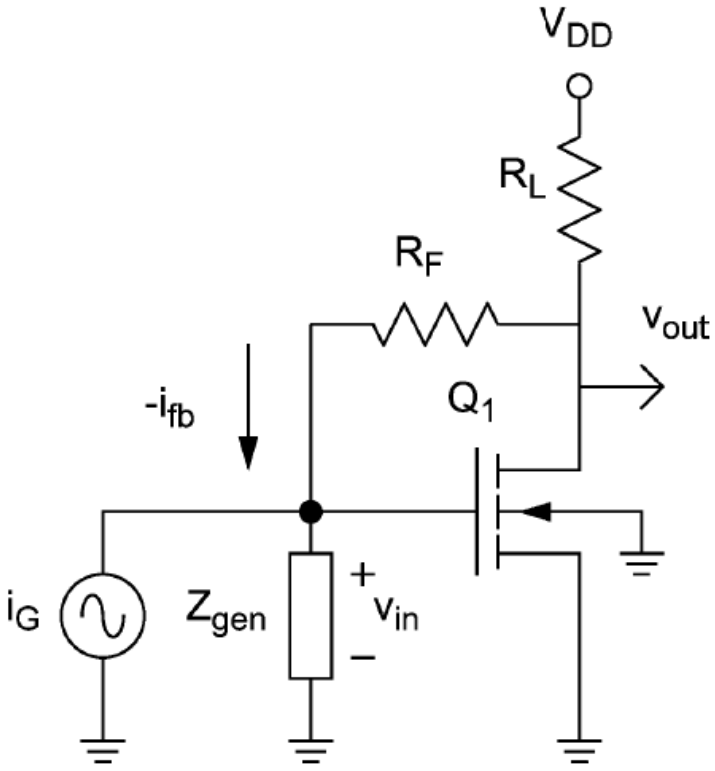


Fig. 1-7. Resistive-feedback amplifier.

offers numerous benefits for broadband amplification, including gain, stability over processing and supply variations, lower distortion (at the cost of gain), and the ability to tailor port impedances for noise and impedance matching. However, the difficulty in simultaneously achieving a 50Ω input match, low noise figure and low power consumption makes such a simple feedback stage unsuitable for a UWB and wideband LNA. That is, achieving a broadband input match by increasing the feedback (i.e., lowering R_F) increases the input referred noise from both the feedback loop and the load.

As previously mentioned, negative feedback allows a designer to exchange gain for bandwidth, which is useful when designing a wideband amplifier. In [26], the complementary topology is adopted in wideband low noise amplifier design; since its inherent high gain of

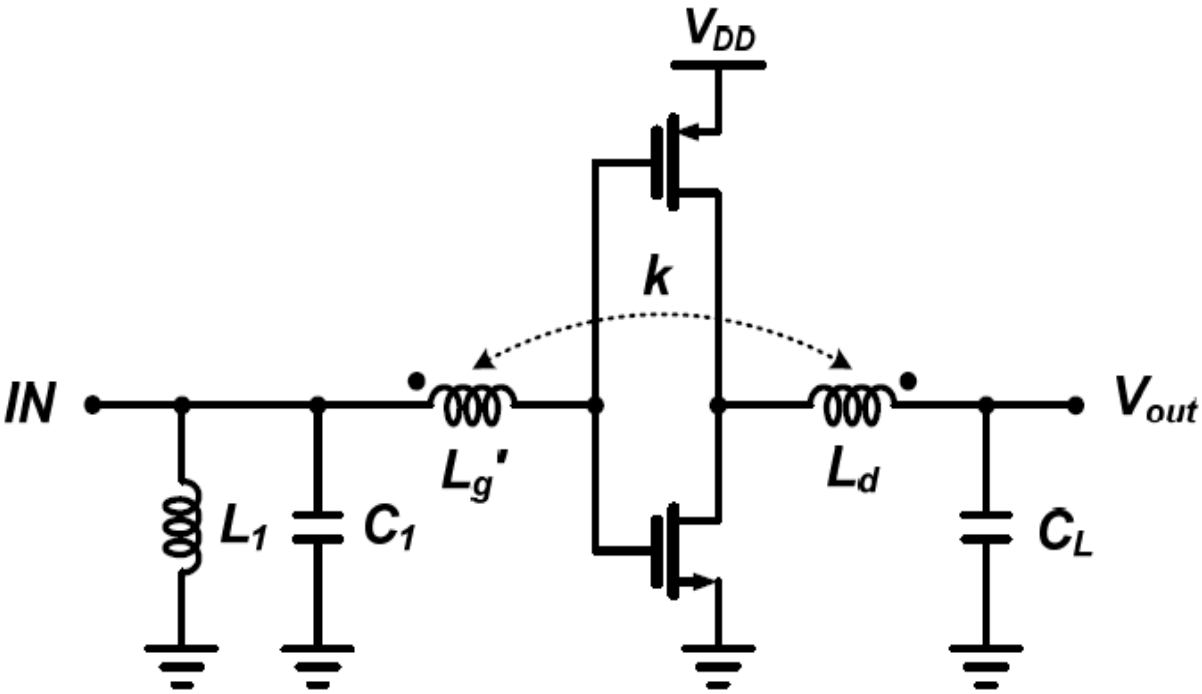


Fig. 1-8. Transformer feedback Complementary UWB amplifier

the first stage, the circuit is expected to have low noise figure according to the famous Friss Equation. The circuit utilizes transformer feedback to achieve matched input impedance 50Ω. The matched bandwidth ranges from f_L to f_H:

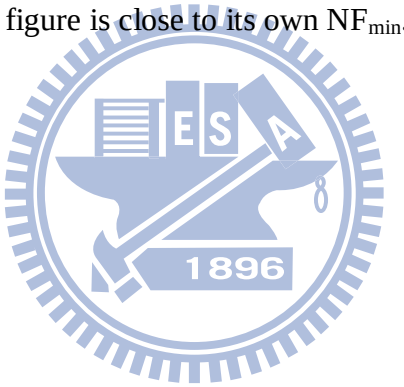
$$f_L = \frac{1}{2\pi\sqrt{L_g g_m r_{ds} C_{gd}}} \tag{1-7}$$

$$f_H = \frac{1}{2\pi\sqrt{L_g (C_{gs} + C_{gd})}} \tag{1-8}$$

Thus the ratio of f_H / f_L is derived as

$$\frac{f_H}{f_L} = \sqrt{\frac{g_m r_{ds} C_{gd}}{C_{gs} + C_{gd}}} \cong 2 \sim 3$$

Therefore, the input matching bandwidth is hard to extend over 100% fractional bandwidth, or the noise figure will be sacrificed. Further, to fulfill the UWB (3-10GHz) specification, especially the low frequency edge, large values of L_g and L_d must be used. Unfortunately, the inherent lossy characteristic of CMOS technology, make the transformer-coupled technique unsuitable in low noise amplifier design in terms of its resulting high noise figure. Besides, the amplifier utilizes L_1 and C_1 to make the noise figure close to its NF_{min}. However, the lossy large inductor L_1 itself will raise its own NF_{min}. Thus the complementary circuit suffers high noise figure, though its noise figure is close to its own NF_{min}.



1.3 Thesis Organization

Thus far, many recently published works are reviewed. Though there are many techniques proposed to suppress or cancel a transistor's channel thermal noise to obtain low noise figure, their noise performances is disappointing. And the proposed input matching technique is difficult to satisfy the stringent requirement of Ultra-wideband, no mention the more wideband application such as software-defined radio. In this thesis, we focus on the design and analysis of wideband low noise amplifier which can simultaneously achieve low noise performance and has well-matched input impedance. To satisfy the requirement, we propose a complementary topology combined with asymmetrical inductive source degeneration. As is discussed and analyzed in this thesis, any inductor (gate inductor) in front of a common-source transistor circuit will greatly raise the noise figure will frequency, thus we avoid using gate inductors, especially large inductors. To achieve low input reflection coefficient (S_{11}<-10dB) while avoid using large gate inductors, we propose a complementary transistor circuit combined with asymmetrical inductive source degeneration, in which only small source inductors are employed. Further, the source inductors can suppress the thermal noise current of both n- and p-type transistors. Because the complementary topology is based on the common-source topology, we first analyze the input impedance of the source inductive degenerated common-source transistor circuit with *R-L-C* loading, then the input impedance and noise theory of the proposed complementary configuration can be analyzed and understood.

In the case of high mobility transistor (HEMT), it has already been demonstrated that through the intrinsic gate-drain capacitor C_{gd}, the transistor's output *R-C* loading can alter its input impedance to the intended value over a wide bandwidth [12]. In spite of that, implementation of this large loading equivalent resistance is not that easy in the CMOS circuit.

Thus, the input matching mechanism for wideband matched COMS LNA needs to be re-examined and modified if necessary, and that prompts the research described in this chapter. In chapter 2, we propose a new methodology for designing and analyzing source inductive degenerative common-source LNA with *R-L-C* loading network, where validity of this new approach is supported by the agreement between the simulated input impedance of the LNA and its calculated counterpart. To demonstrate its feasibility, two wideband matched LNA's are designed using TSMC 0.18-μm RF-CMOS process: one is for 3−8GHz application and the other 8−25GHz. The measured results of both circuits will then be presented.

In chapter 3, we propose a novel LNA design method where the complementary transistor topology is combined with asymmetrical inductive source degeneration to simultaneously achieve matched input impedance and low noise figure over a wide bandwidth. The validity of this new approach is supported by the agreement between the simulated input impedance of the LNA and their calculated counterpart. Also, the noise figure of the newly proffer topology is accurately analyzed and well explained. A 2-10GHz LNA is therefore designed and fabricated using commercial 0.18μm RF-CMOS process to verify the feasibility of our proposed method. In the intended bandwidth, this LNA has matched input impedance, 20dB power gain, and 2.4–3.4dB noise figure, with 25.65mW power consumption.

In chapter 4, as is mentioned above, the gate inductor is unsuitable in designing UWB or wideband low noise amplifier; we propose the complementary configuration with asymmetrical inductive source degeneration to achieve input matching for not sacrificing the noise figure. In this chapter, we propose a modified source inductively generated common-source transistor circuit, which can greatly improve the noise figure up to 2-4dB at W-band (70-110GHz) compared to the conventional source inductive degenerated common-source amplifier with a gate inductor. Thus the potential application of the proposed technique is justified. Finally, the derivations of the input impedance and the noise factor are included in Appendix I and Appendix II.

Chapter 2

Wideband Matched CMOS LNA Design Using R-L-C Loading Network

2.1 Introduction

Wide-band low-noise amplifiers (LNA's) have been a critical component for both scientific community and the communication industry, such as radio astronomy receivers for the former and ultra-wideband (UWB) technologies for the latter [1]-[3]. Among the different circuit design methodologies proposed for wideband amplifiers, the distributed one is probably the most straightforward in realizing broad bandwidth [4]-[5]. However, it tends to consume a lot of power while providing only modest gain. An amplifier using common-gate transistor as input stage can indeed have wideband matched impedance; nonetheless, the resulting circuit will have poor power gain and large noise figure [6]. Adding a delicate *L*-*C* circuit in front of

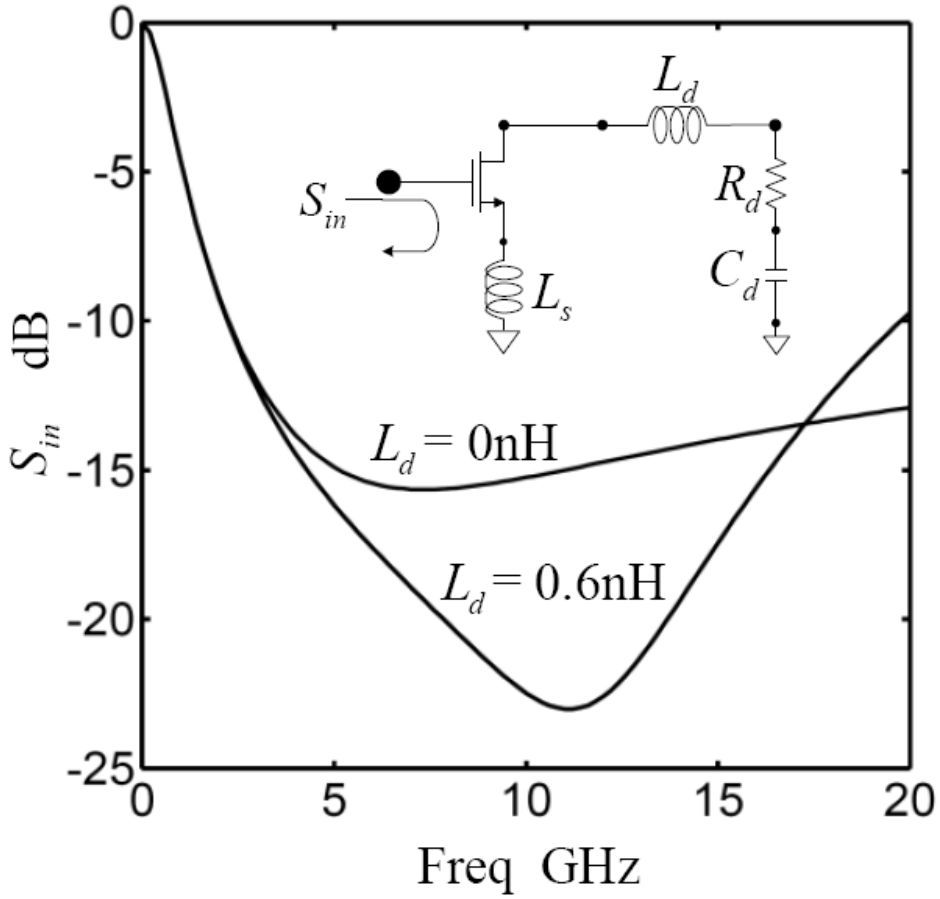


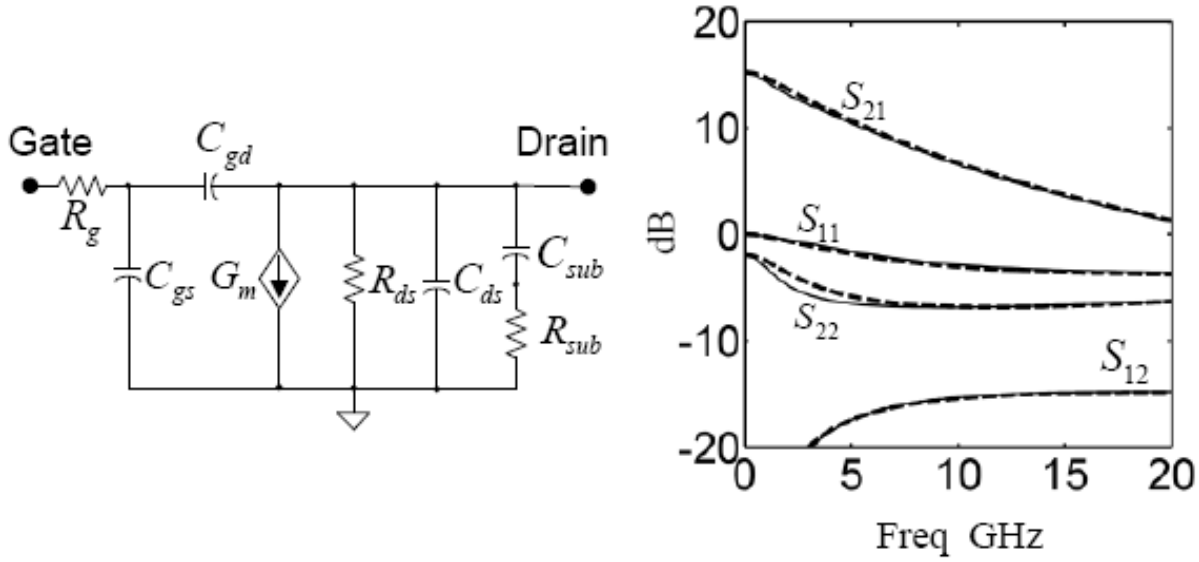
Fig. 2-1 The simulated input reflection coefficient S_{in} of the proposed transistor circuit with L_d = 0 and 0.6nH, respectively, while C_d = 0.13pF, R_d = 25Ω, and L_s = 0.3nH.

the amplifier can improve its input matching over a wide bandwidth, but at the cost of additional noise generated by these passive components and, especially in the case of silicon, this deterioration is pronounced [7]-[9]. Recently, it becomes popular applying current re-use method in designing wideband CMOS amplifiers; however, the stacking of one n-type and one p-type transistors requires a large bias voltage [10]-[11].

In the case of high mobility transistor (HEMT), it has already been demonstrated that through the intrinsic gate-drain capacitor C_{gd}, the transistor's output *R*-*C* loading can alter its input impedance to the intended value over a wide bandwidth [12]. In spite of that, implementation of this large loading equivalent resistance is not that easy in the CMOS circuit.

Thus, the input matching mechanism for wideband matched COMS LNA needs to be re-examined and modified if necessary, and that prompts the research described in this chapter. In the following section, after a brief review of the 0.18-μm RF-CMOS transistor's small-signal modeling, we propose what should constitute the first-stage transistor's loading: L_d, R_d, and C_d, as shown in Fig. 2-1, where L_d is an explicit element, and both R_d and C_d can be from the equivalent input circuit of the following-stage. Physically, the external source inductor L_s is critical in determining the low-frequency input matching, and the loading L_d starts playing a role as frequency increases. In both cases, C_d is used for setting Re[Z_{in}], and proper choice of R_d helps lowering S_{11} at high frequency. If the high frequency range means infinite, then L_d can indeed be omitted; otherwise, the importance of this L_d cannot be overlooked for finite-bandwidth wideband LNA, as this L_d could improve the input matching at the intended high frequency range. Without inserting any complicated passive (and lossy) circuit in front of the first-stage transistor, superior noise performance is expected for this type of amplifier.

A 3–8GHz LNA is therefore fabricated using TSMC (Taiwan Semiconductor Manufacturing Company) 0.18-μm RF-CMOS process. To explore the high frequency performance of this commercial process, a second LNA targeting the 8–25GHz frequency range is then designed. Measured results of both amplifiers will be presented too.



(a) (b)

Fig. 2-2. (a) Small-signal model of a TSMC 0.18-μm RF-CMOS transistor biased at saturation region. (b) Simulated *S*-parameters from both the foundry provided design kit (solid lines) and our small-signal model (dashed lines).

2.2 Analysis of Wideband LNA Design

To facilitate the circuit analysis, *S*-parameters of a TSMC 0.18-μm RF-CMOS transistor need to be numerically fitted to find its equivalent small-signal model, as shown in Fig. 2-2, where the substrate effect due to C_{sub} and R_{sub} has been included. For this 216-μm 27-finger n-type transistor biased at V_{gs} = 0.65 Volt and I_d = 7 mA, our model is valid up to 20GHz at least, and the parameter values are tabulated in Table I. Though *S*-parameter discrepancies can be observed with the omission of R_g, C_{ds}, R_{sub}, and C_{sub} , they are relatively minor; thus, to retain the physical meaning while simplifying the mathematical derivation, these four parameters are removed from that used in the following circuit analysis.

TABLE 1

PARAMETERS IN THE SMALL-SIGNAL MODEL OF THE 216-MICRON 27-FINGER TSMC N-TYPE TRANSISTOR

V_{gs} = 0.65 Volt, I_d = 7 mA			
parameter	value	parameter	value
R_g	7Ω	C_{sub}	0.3pF
R_{ds}	452Ω	C_{ds}	0.063pF
R_{sub}	180Ω	C_{gd}	0.08pF
G_m	64mS	C_{gs}	0.2pF

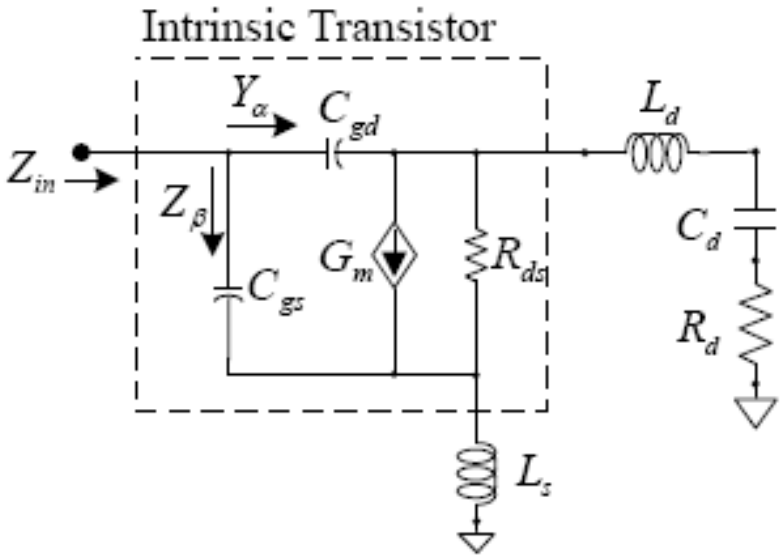


Fig. 2-3. The proposed transistor circuit used in the wideband analysis.

Mathematically, the input impedance Z_{in}, as indicated in Fig. 2-3, can be expressed as

$$Z_{in} = \left[Y_\alpha + \frac{1}{Z_\beta} \right]^{-1} \tag{2-1}$$

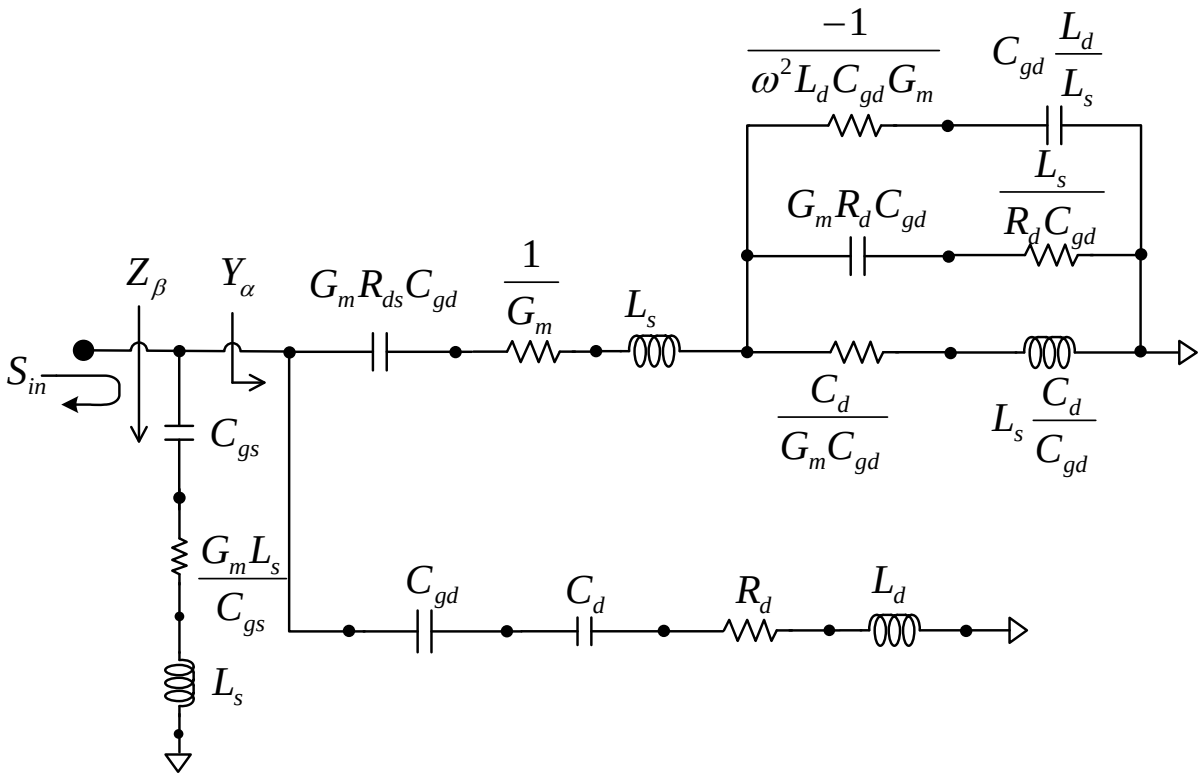
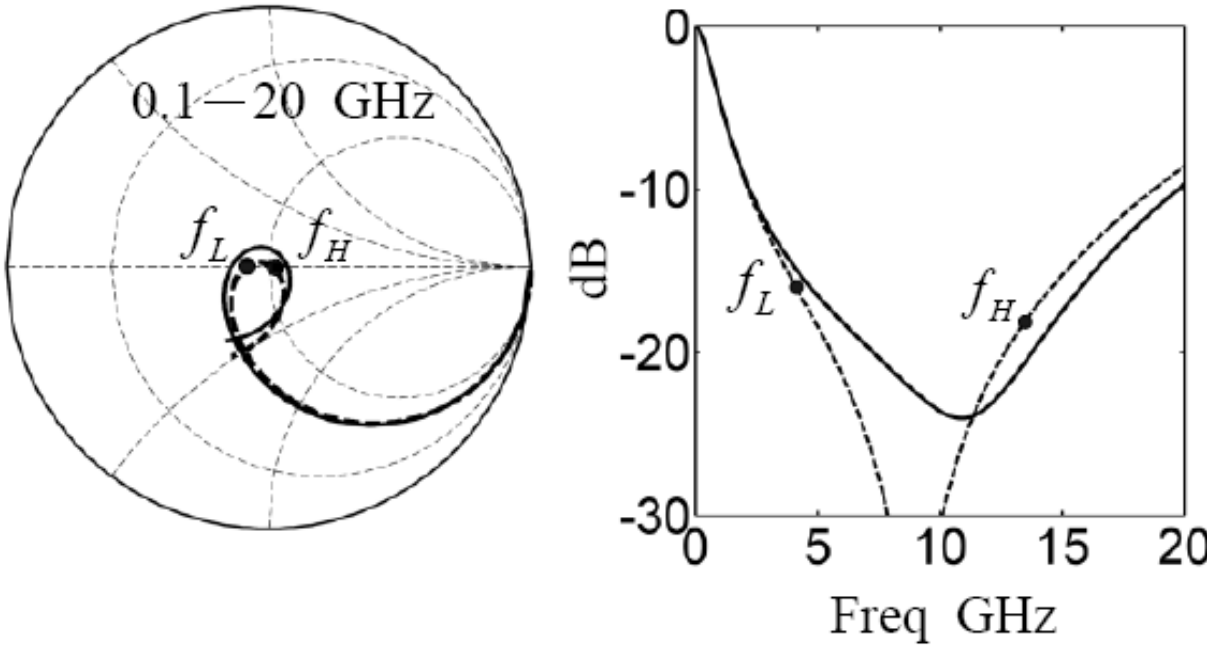


Fig. 2-4. Equivalent input schematic of the proposed transistor circuit. Y_α is the admittance looking into C_{gd} branch, Z_β is the impedance looking into C_{gs} branch, and S_{in} is the overall input reflection coefficient.

where Y_α is the admittance looking into the C_{gd} branch, and Z_β is the impedance looking into the C_{gs} branch. Both Y_α and Z_β can be derived as

$$Y_\alpha = \left[\frac{1}{j\omega C_{gd}} + \frac{1}{j\omega C_d} + R_d + j\omega L_d\right]^{-1} + \left[\left(\frac{1}{j\omega G_m R_{ds} C_{gd}} + \frac{1}{G_m} + j\omega L_s\right)\right. + \left(\frac{1}{C_d / G_m C_{gd} + C_{gd} / j\omega L_s C_d}\right.$$

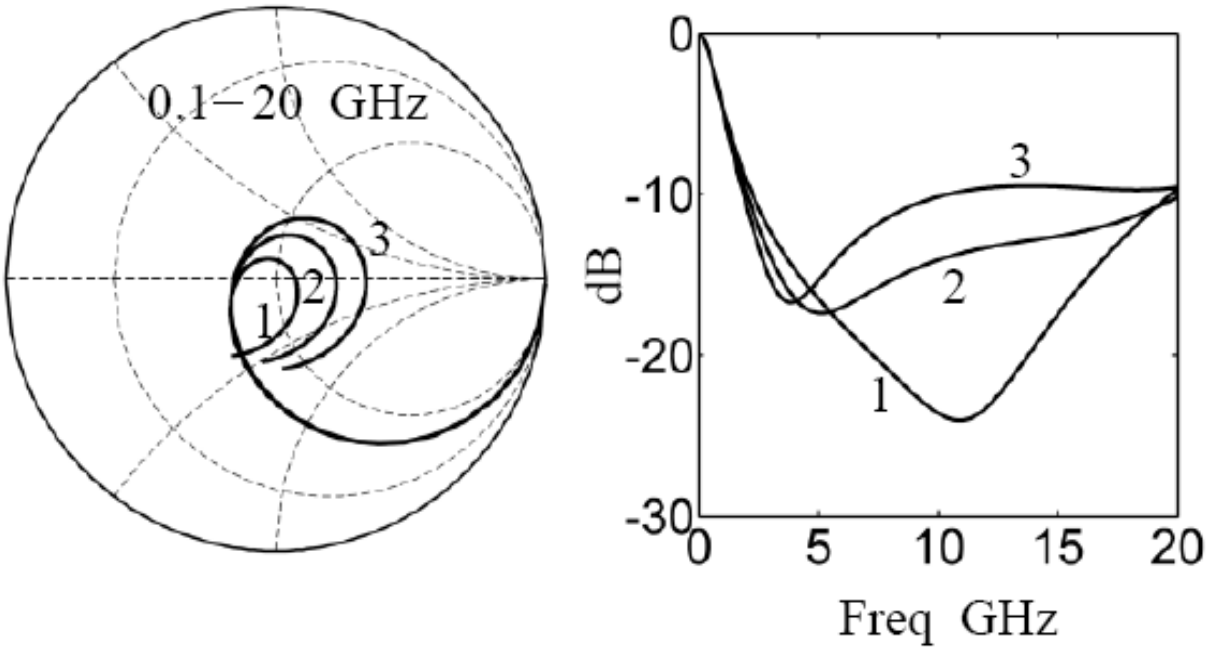


(a) (b)

Fig. 2-5. Calculated and simulated input reflection coefficient of the proposed transistor circuit. (a) The solid curve on the Smith chart is the simulated result while the dashed curve is its calculated counterpart. Here f_L and f_H are the resonant low- and high-frequency points. (b) The same results expressed in dB vs. frequency.

$$+\frac{1}{1/j\omega G_m R_d C_{gd} + L_s/R_d C_{gd}}$$

$$+\frac{1}{L_s/j\omega C_{gd} L_d - 1/\omega^2 L_d C_{gd} G_m}\Bigg)^{-1}\Bigg]^{-1} \qquad (2\text{-}2)$$



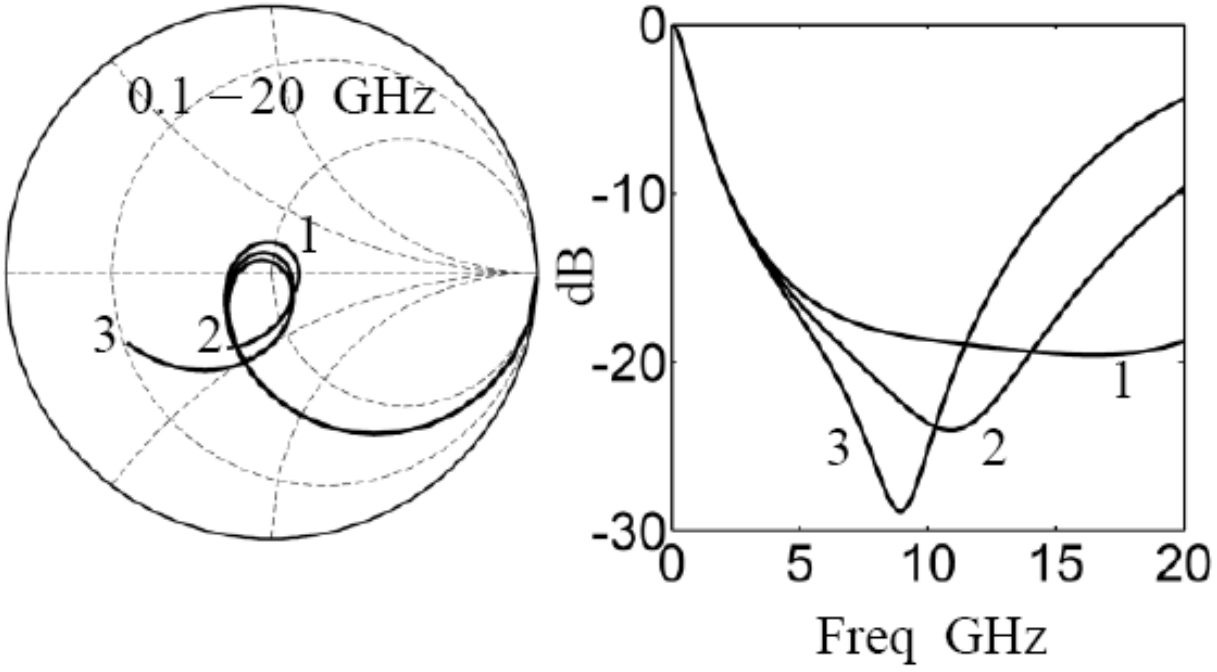
(a) (b)

Fig. 2-6. Simulated input reflection coefficient of the wideband transistor circuit with different values of L_s. (a) On the Smith chart, curves 1–3 correspond to L_s = 0.3, 0.4, and 0.5, respectively, while C_d = 0.13pF, R_d = 25Ω, and L_d = 0.6nH. (b) The same results expressed in dB vs. frequency.

and

$$Z_\beta = \frac{1}{j\omega C_{gs}} + \frac{G_m L_s}{C_{gs}} + j\omega L_s \tag{2-3}$$

The corresponding equivalent circuit can be arranged as that of Fig. 2-4, where Y_α is the dominant branch and Z_β offers some modification [12]. Again, it is the C_d that determines the matched Re[Z_{in}] (= $C_d/G_m C_{gd}$), as discussed in detail in [12]. With appropriate component



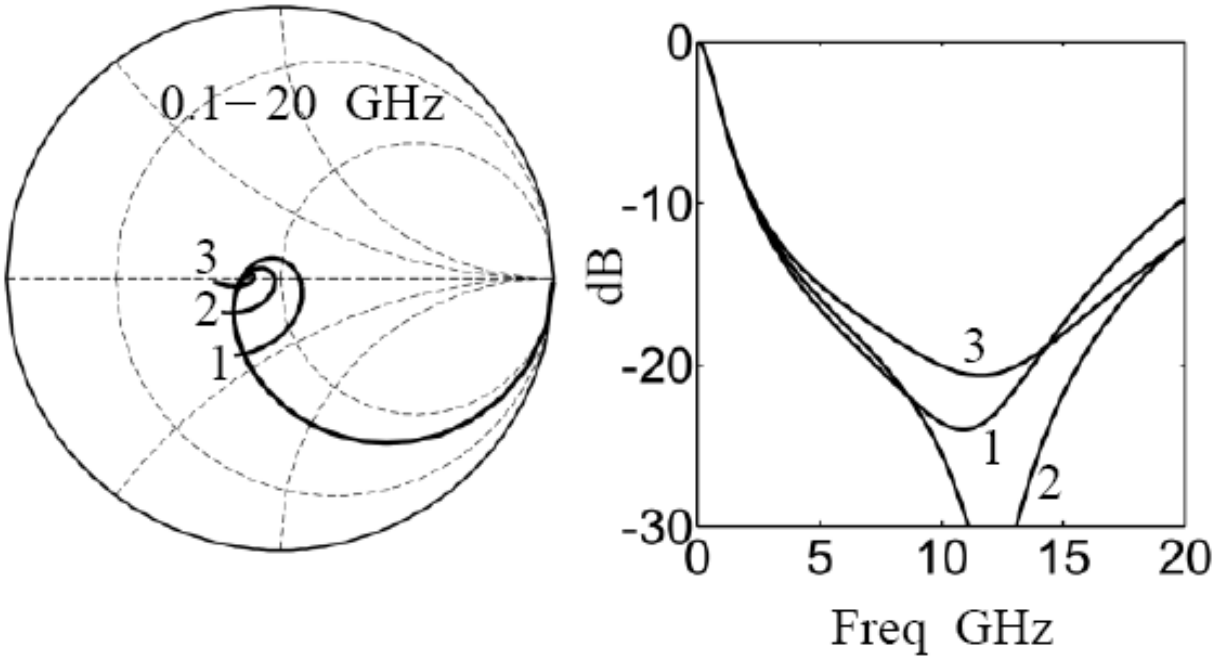
(a) (b)

Fig. 2-7. Simulated input reflection coefficient of the wideband transistor circuit with different values of L_d. (a) On the Smith chart, curves 1–3 correspond to L_d = 0.3, 0.6, and 0.9nH, respectively, while C_d = 0.13pF, R_d = 25Ω, and L_s = 0.3nH. (b) The same results expressed in dB vs. frequency.

values, the shape of the input reflection coefficient S_{in} resembles a hook, as shown in Fig. 2-5. The solid curve is the simulated result with C_d = 0.13pF, R_d = 25Ω, L_d = 0.6nH, and L_s = 0.3nH; the overlapping dashed curve is the calculated counterpart using (2-1). On the S_{in} trajectory, there are two marked frequency points where the corresponding input impedance is purely real and close to 50Ω, and thus are good indices for this circuit's (slightly larger) available frequency range. By setting Im[Y_a] to zero, both f_L and f_H can be determined as

$$f_L = \frac{1}{2\pi\sqrt{L_s(C_{gd}+C_d)G_m R_{ds}}} \tag{2-4}$$

and



(a) (b)

Fig. 2-8. Simulated input reflection coefficient of the wideband transistor circuit with different values of R_d. (a) On the Smith chart, curves 1–3 correspond to R_d = 25; 45, and 65Ω, respectively, while C_d = 0.13pF, L_s = 0.3nH, and L_d = 0.6nH. (b) The same simulated results in dB vs. frequency.

$$f_H = \frac{1}{2\pi\sqrt{(L_s + L_d)C_d}} \tag{2-5}$$

The calculated f_L and f_H are 4.09GHz and 13.24GHz in this case, and are very close to the simulated 5GHz and 12.8GHz, respectively. Apparently, with C_d used in determining Re[Z_{in}], f_L can now be set by L_s while f_H could be manipulated by L_d. Fig. 2-6 shows the simulated input reflection coefficient with different L_s, where curves 1–3 have L_s = 0.3, 0.4, and 0.5nH, and all have their C_d = 0.13pF, R_d = 25Ω, and L_d = 0.6nH. Fig. 2-7 illustrates the impact of L_d on S_{in}, where curves 1–3 are with L_d = 0.3, 0.6, and 0.9nH, and all have their C_d = 0.13pF, R_d = 25Ω, and L_s = 0.3nH. Fig. 2-8 shows the simulated S_{in} with different R_d, where curves 1–3 have R_d = 25, 45, and 65Ω, and all have their C_d = 0.13pF, L_s = 0.3nH, and L_d = 0.6nH.

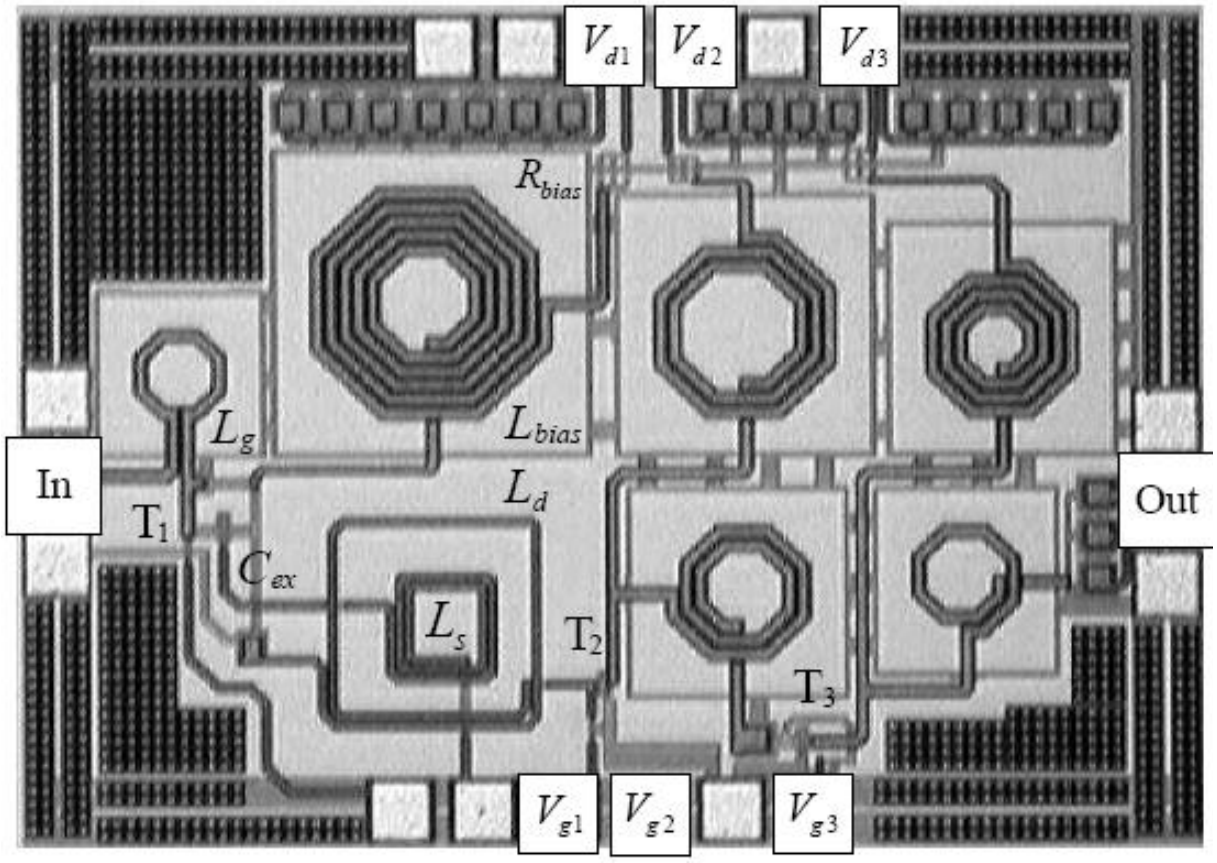


Fig. 2-9. Photograph of the 3–8GHz LNA. The chip size is 1400×1000 μm^2. T_1, T_2, and T_3 are the three transistors.

Intuitive understanding of this matching mechanism can now be best described as follow:

(a) $f < f_L$: As series $R_dL_dC_d$ tends to be open-circuit at very low frequency and the effect of L_s is very small in this frequency range, the transistor's loading is now dominated by channel resistance R_{ds} (= 452Ω). The resulting Miller capacitance $G_mR_{ds}C_{gd}$ (= 2.31pF) puts the location of S_{in} in the capacitive region of the Smith chart. As frequency increases, the real part of input impedance will start to be affected by the loading C_d, as Re[Z_{in}] = C_d/G_mC_{gd}. The S_{in} trajectory can be determined by C_d and moves along the constant resistance circle in the capacitive region [12].

(b) $f_L \leq f < f_H$: As frequency continues to increase, the inductive voltage induced by L_s at the

input is becoming more obvious, thus the inductive components of Z_{in} (originating from L_s) will resonate out the aforementioned Miller capacitance $G_mR_{ds}C_{gd}$. On the Smith chart, S_{in} will now pass-by the zero point and enter the inductive region; therefore, it is apparently that f_L can be set by L_s. Since the loading resistor R_d (= 25Ω) can also generate a small Miller capacitance $G_mR_dC_{gd}$ (= 0.125pF), a further bending of the still-inductive S_{in} on the Smith chart can be observed in this frequency range.

(c) $f \geq f_H$: When the inductor L_d begins to resonate out C_d, the loading circuit can be approximated as R_d at the resonance frequency; therefore, Z_{in} is predominated by the corresponding Miller capacitance $G_mR_dC_{gd}$, which means S_{in} on the Smith chart can be easily dragged into the capacitive region. A complete loop around the zero point is now constructed and we know that f_H can be changed by L_d. If the high frequency range means infinite, this L_d can indeed be omitted; otherwise, the importance of this L_d cannot be ignored in the case of finite-bandwidth wideband LNA. Thus far, the roles played by C_d, L_s, L_d, and R_d in achieving wideband input matching are well explained and can be easily understood.

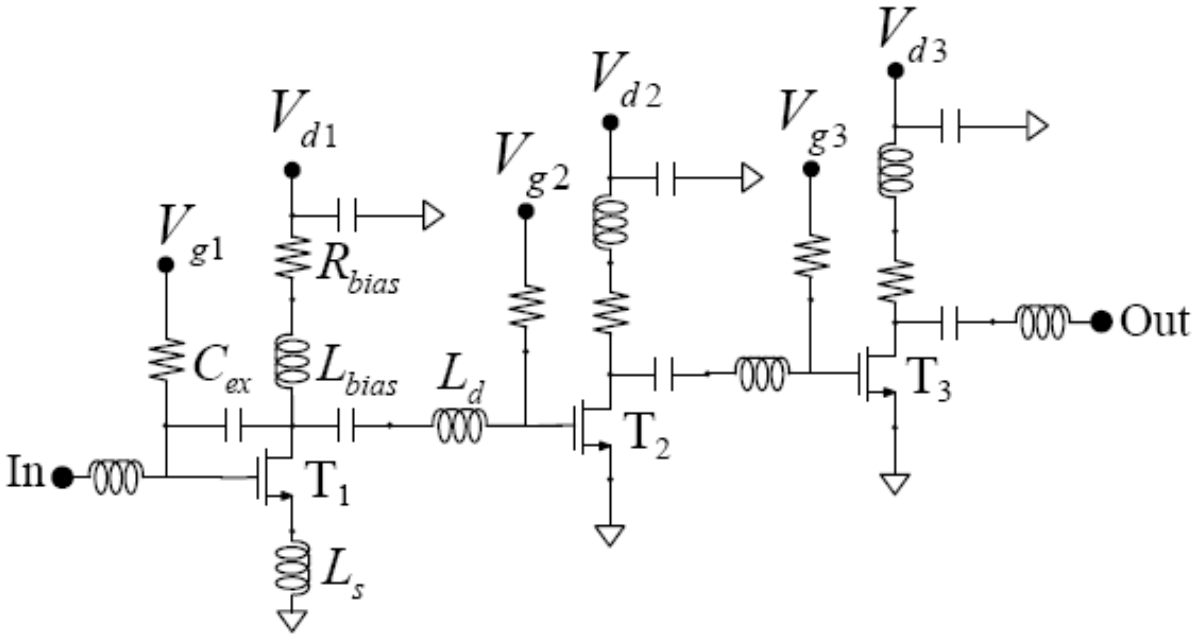
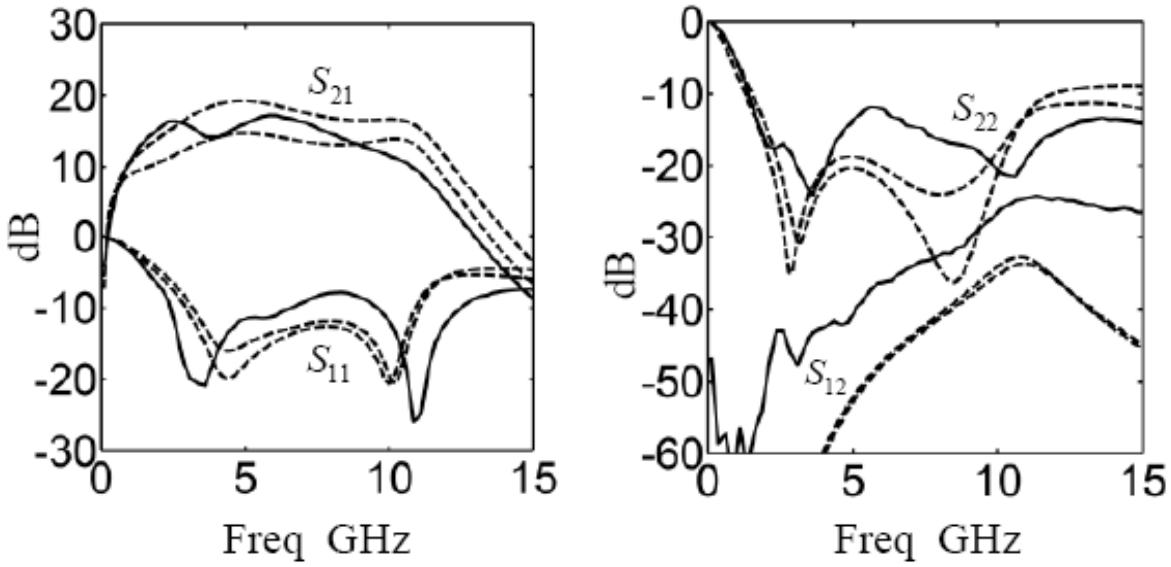


Fig. 2-10. Schematic of the 3–8GHz LNA.

2.3 Wideband LNA Design

With the wideband matching mechanism fully analyzed, two CMOS LNA's, one covers the more common 3–8GHz as an initial verification and the other the more challenging 8–25GHz for exploring this type of circuits' potential and limitation, are designed and fabricated using TSMC 0.18-μm RF-CMOS process. Both the *S*-parameters and noise figures of these two circuits are measured on-wafer at room temperature. Description of the circuits and their measured results will be presented below.

Figs. 2-9 and 2-10 are the photograph and schematic of the 3–8GHz LNA. It is mainly the 1nH source inductor L_s, 1.5nH inter-stage L_d, and 0.2pF loading capacitor C_d, that contribute to the wideband input matching. The coupling between L_s and L_d allows the reduction of the chip size. To reduce its power consumption, a slightly smaller transistor is used for the first

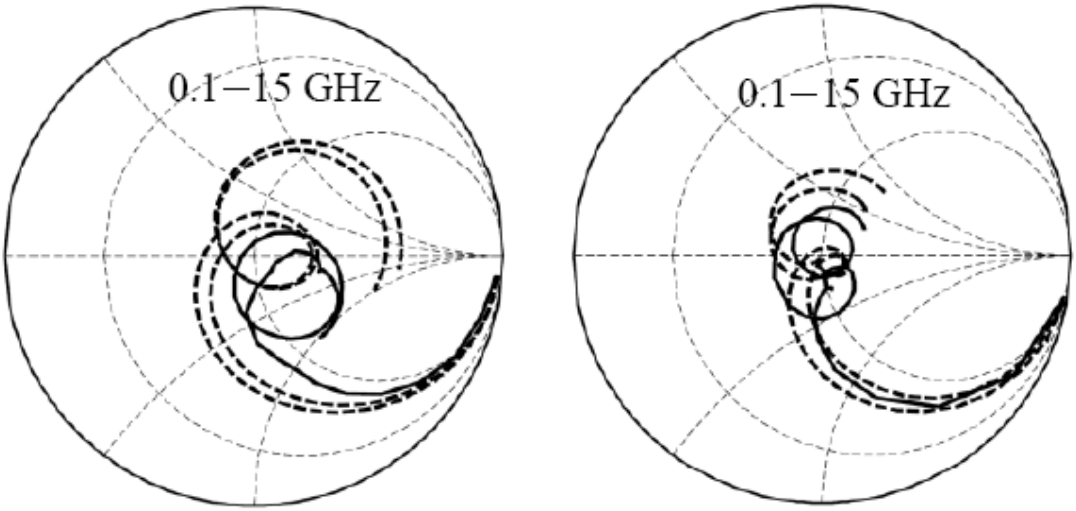


(a) (b)

Fig. 2-11. Measured and simulated *S*-parameters of the 3–8GHz wideband LNA. (a) S_{21} and S_{11} where the solid curves are the measured results and the dashed curves are their simulated counterparts in two circumstances. (b) S_{12} and S_{22}.

stage. To ensure that the equivalent C_{gd} is still sufficient to sustain the wideband matching mechanism, an external capacitor C_{ex} is added. The large inductor L_{bias} on the drain branch is for DC bias purpose and has small impact on S_{11} in 3–8GHz. Since this L_{bias} tends to introduce a negative Re[Z_{in}] at very low frequency, R_{bias} is used to stabilize this amplifier.

Fig. 2-11 shows the measured and simulated *S*-parameters of this 3-8GHz LNA where the both the S_{11} and S_{22} are below -10dB, S_{21} around 15dB, and S_{22} far below -20dB. For each measured scattering parameter, there are two simulated counterparts, technically SS and TT corners, to account for the inevitable process variation. The bias is set at V_{d1} = 1V and I_{d1} = 9.5mA for the first-stage transistor, V_{d2} = 1V and I_{d2}= 7.5mA for the second stage, and V_{d3} = 1V and I_{d3} = 7.4mA for the last stage. Fig. 2-12 shows the same S_{11} and S_{22} on the Smith chart, and both resemble the familiar wideband hook shape. Fig. 2-13 shows the measured noise figure and the linearity (IIP3) of this circuit. The total power consumption of this amplifier is



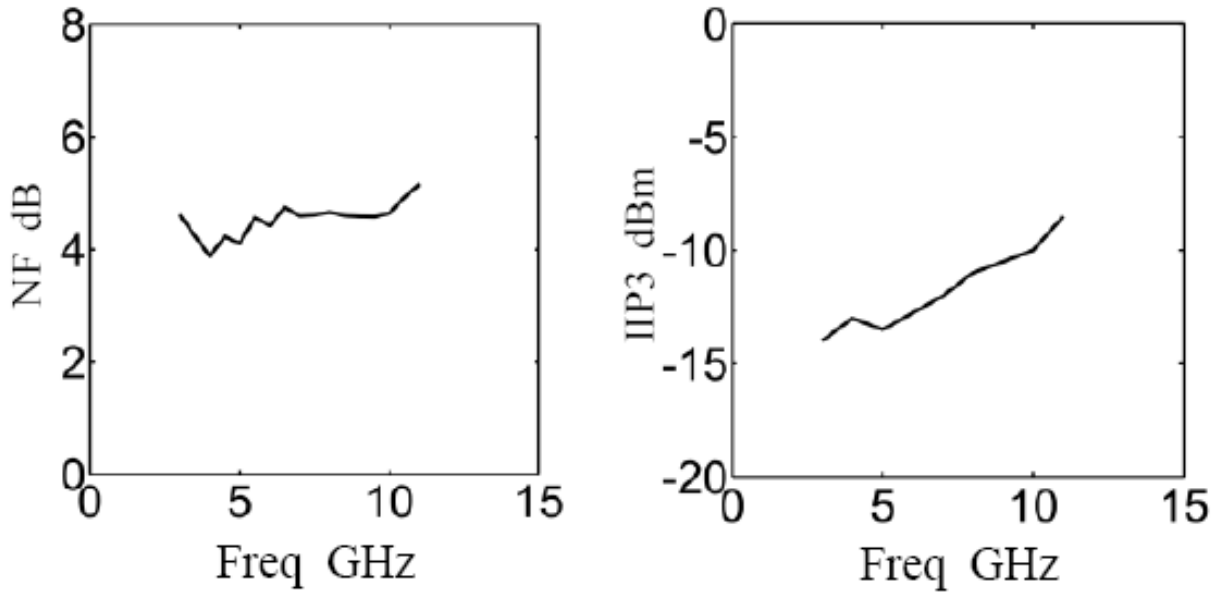
(a) (b)

(b)

Fig. 2-12. Measured and simulated S_{11} *and* S_{22} of the 3–8GHz wideband LNA on the Smith chart. (a) The solid curve is the measured S_{11} and the two dashed curves are the simulated counterparts. (b) Measured and simulated S_{22}.

24.4mW.

Figs. 2-14 and 2-15 are the photograph and schematic of the 8-25GHz five-stage LNA where the design methodology is similar to that of the 3–8GHz one. To simplify the bias scheme, only one drain bias and one gate bias are used. Isolation along the common drain bus between each stage is provided by the long transmission lines that surround the periphery of this chip. A small chip size of 945×1245 μm^2 can thus be obtained. With V_d = 1.8V and I_d = 62mA, both the measured and simulated S_{11} and S_{22} are below -10 dB, S_{21} around 15 dB, and S_{22} far below -20dB, as shown in Figs. 2-16 and 2-17. Apparently, an increase of the input inductor by the use of bond-wire can easily move the S_{11} loop upward on the Smith chart and surround the zero point, therefore, lowers the input reflection coefficient further. The total power consumption is 112mW. To explore this circuit's performance under different bias conditions, Fig. 2-18 shows the measured input reflection coefficient, gain, and noise figure at different



(a) (b)

Fig. 2-13. The measured noise figure and IIP3 of the 3–8GHz wideband LNA. (a) Noise figure. (b) IIP3.

bias conditions where the solid curves are at V_d = 2V, I_d is 37, 50, and 62mA; the dashed curves are with V_d = 1V and I_d is 31, 42, and 53mA, respectively.

2.4 Conclusion

In this paper, the input matching technique for common source wideband LNA design has been thoroughly analyzed. The agreement between the simulated input impedance of the LNA and its calculated counterpart confirms the accuracy of our analysis. To demonstrate its wideband potential, both the 3–8GHz and 8–25GHz low noise amplifiers using TSMC 0.18-μm RF-CMOS process are designed, fabricated and measured.

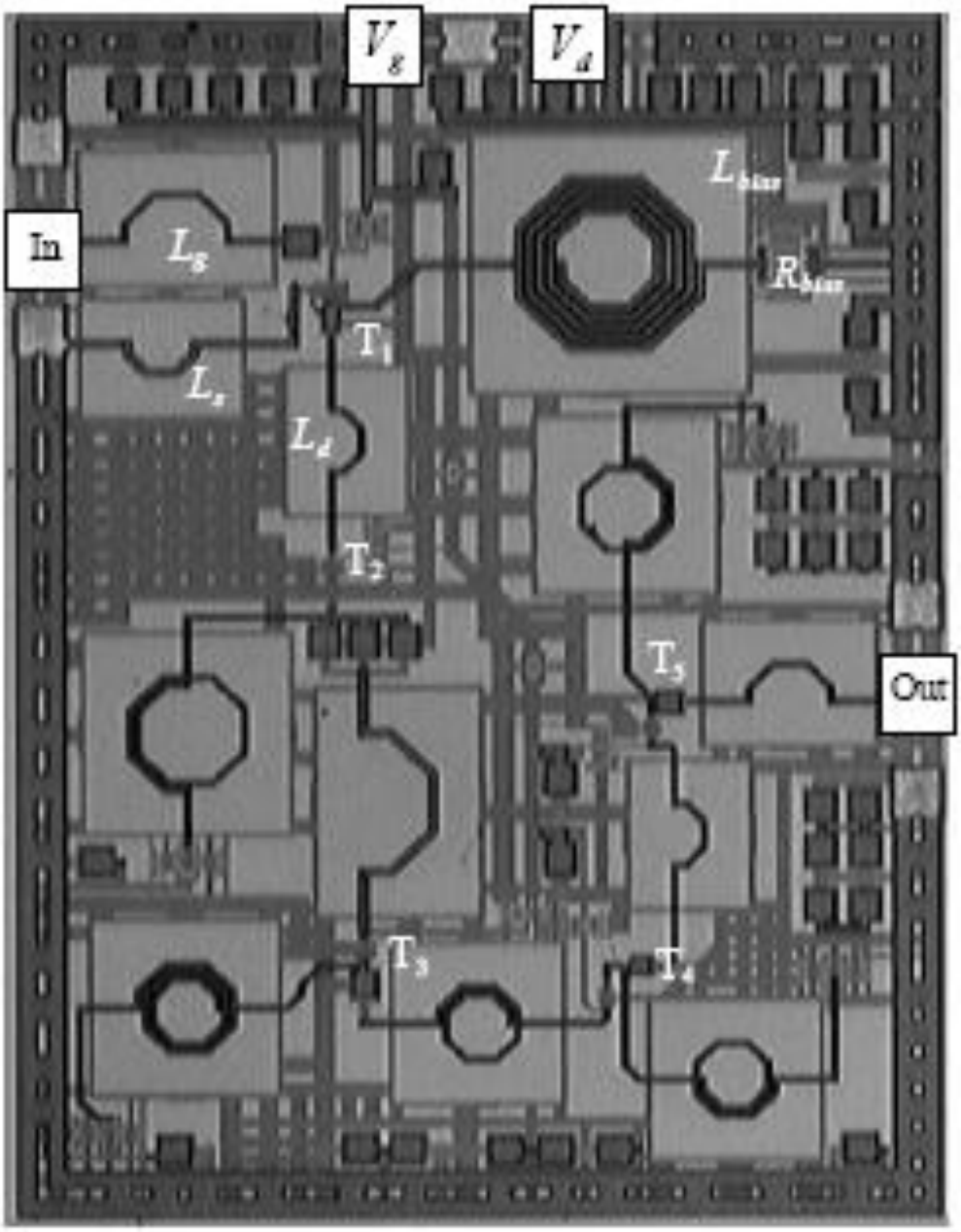


Fig. 2-14. Photograph of the 8–25GHz CMOS LNA. The chip size is 945×1245 μm^2. T_1, T_2, T_3, T_4, and T_5 are the five transistors.

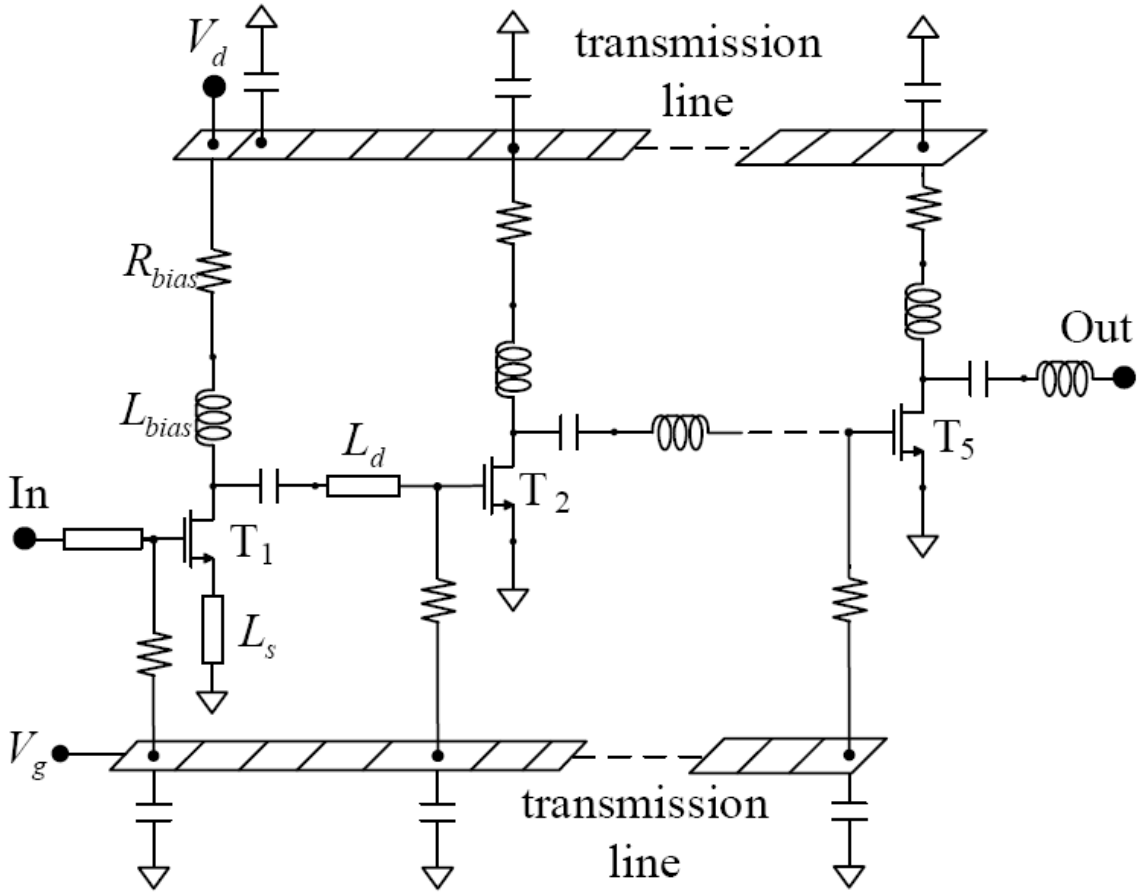
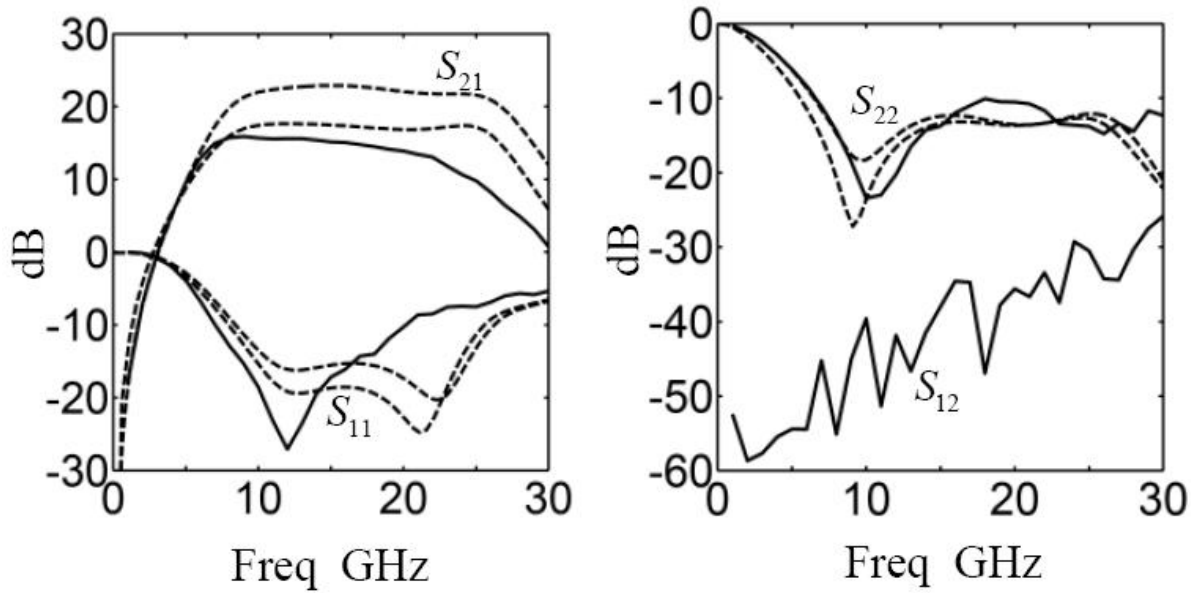
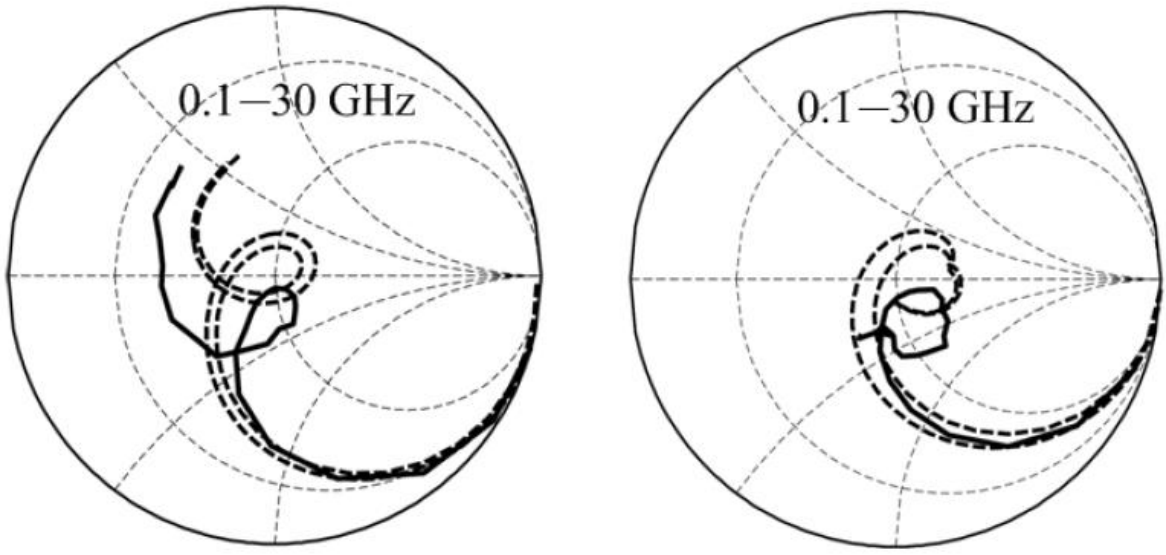


Fig. 2-15. Schematic of the 8-25GHz CMOS LNA. There is only one drain bias and one gate bias needed for this 5-stage circuit.



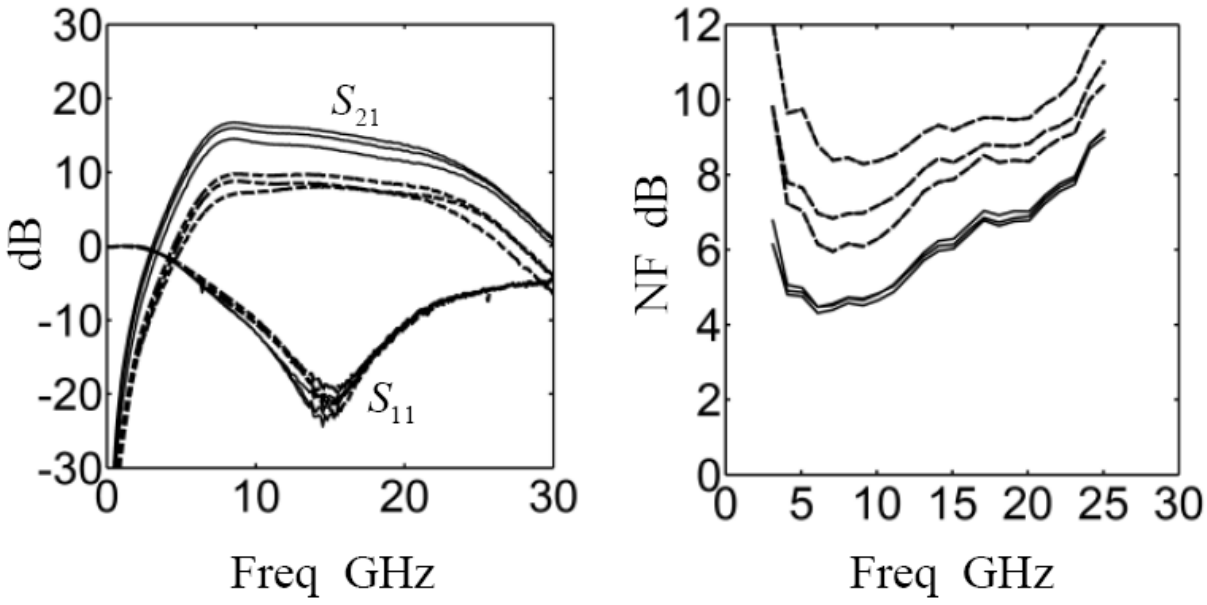
(a) (b)

Fig. 2-16. Measured and simulated *S*-parameters of the 8–25GHz wideband LNA. (a) Measured (solid) and simulated (dashed) S_{21} and S_{11}. (b) Measured and simulated S_{12} and S_{22}.



(a) (b)

Fig. 2-17. Measured and simulated S_{11} *and* S_{22} of the 8–25GHz wideband LNA on the Smith chart. (a) The solid curve is the measured S_{11} and the dashed curves are the simulated counterparts. (b) Measured and simulated S_{22}.



(a) (b)

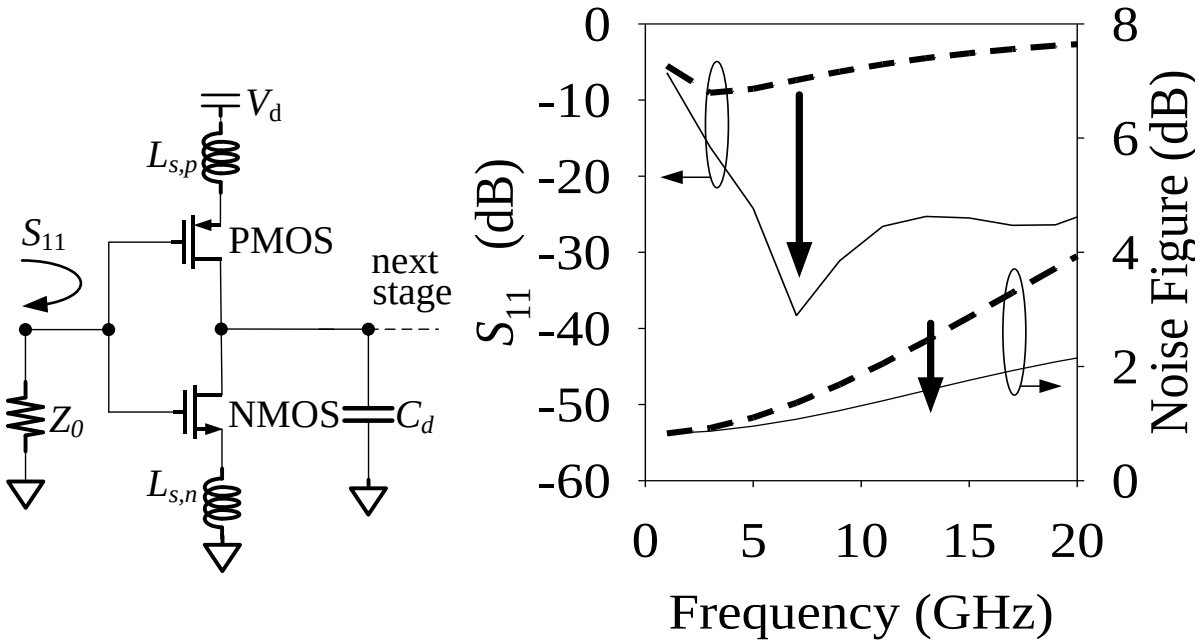
Fig. 2-18. Measured S_{21}, S_{11} and noise figure of the 8-25GHz LNA. (a) Measured S_{21} and S_{11} where the solid curves are with V_d = 2V, I_d is 37, 50, and 62 mA; the dashed curves are with V_d = 1V, I_d is 31, 42, and 53 mA, (b) Measured noise figure with V_d = 2V (solid) and V_d = 1V (dashed) with different bias current.

Chapter 3

Analysis and Design of Complementary Ultra-Wideband LNA Using Asymmetrical Inductive Source Degeneration

3.1 Introduction

WIDE-BAND low-noise amplifiers (LNAs) have been a critical component for both scientific community and the communication industry, such as radio astronomy receivers for the former and ultra-wideband (UWB) technologies for the latter. Among the different circuit design methodologies proposed for LNAs, such as those using noise cancelation technique, those utilizing complicated filters as input matching networks, and those using common-gate transistor as input stage, though those resulting circuits can indeed have matched impedance;



(a) (b)

Fig. 3-1. The proposed method of combining the complementary transistors with asymmetrical source inductors for wideband input matching and low noise figure. (a) The equivalent loading C_d comes from the following stage. Z_0 is the generator 50Ω. (b) The corresponding input reflection coefficient S_{11} and the noise figure, where the solid curves are the simulated results with $L_{s,n}$ and $L_{s,p}$, while the dashed curves are simulated without those inductors.

nonetheless, they have poor noise figures [1]-[13]. The use of complementary, or known as current re-use, method has been demonstrated in CMOS low noise amplifier (LNA) design to achieve broadband input matching where the equivalent 50Ω input impedance is made possible by the coupled gate-drain inductors and the loading capacitor [14]. With the external resistive drain bias circuit no more needed in the complementary topology, not just the signal loss can be minimized; noise performance of the amplifier can also be improved. However, the p-type transistor which possesses small transconductance would deteriorate the noise figure slightly. Furthermore, the gate and drain inductors, themselves large and lossy, will inevitably raise the amplifier's noise figure.

This chapter, which is a significant extension of our work in [17], details more about input matching mechanism as well as noise theory for the proposed amplifier. Rather than employ a lossy input matching network which will worsen a circuit's noise performance, we propose a new wideband CMOS LNA design method that is combining the complementary topology with asymmetrical inductive source degeneration. Further, since the circuit itself can suppress the noise power resulting from the two small inductors, the superior performance of the wideband LNA can be expected. Therefore, the benefits to a LNA for complementary topology outweigh the downside resulting from the use of the p-type transistor. As shown in Fig. 3-1, the complementary transistors have their gate nodes joined together as the input of the amplifier while their common drain is connected to a loading C_d; the two small inductors $L_{s,n}$ and $L_{s,p}$ are used for source degeneration. By properly adjusting the values of these two inductors for a given C_d, low noise figure and wideband input matching can be achieved simultaneously.

In the following sections, input matching mechanism and noise theory will be analyzed first; a 2-10GHz LNA is then designed and fabricated using commercial 0.18μm RF-CMOS process. Important parameters such as *S*-parameters, noise figure, and input-referred third-order intercept point (IIP3) will all be measured and compared with LNA's designed by other research groups.

3.2 Input Matching Analysis

To facilitate the circuit analysis, *S*-parameters of a TSMC 0.18-μm RF-CMOS transistor need to be numerically fitted to obtain its equivalent small-signal model, as shown in Fig. 3-2, where the substrate effect due to C_{sub} and R_{sub} has been included. For this 144-μm 18-finger n- and p-type transistor biased at V_{gs} = 0.65 Volt and I_d = 4.72 mA, our model is valid up to

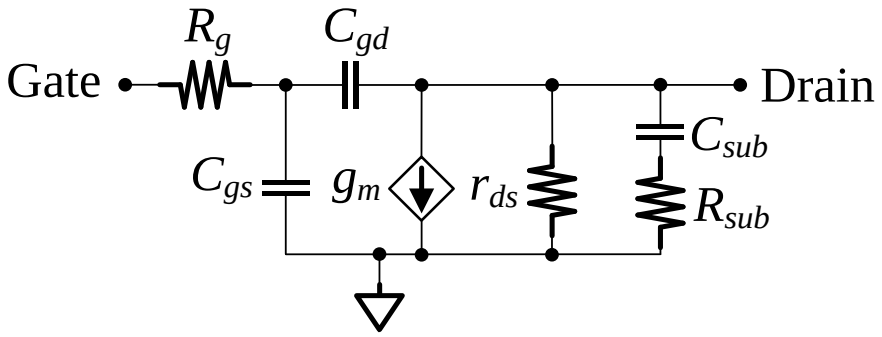
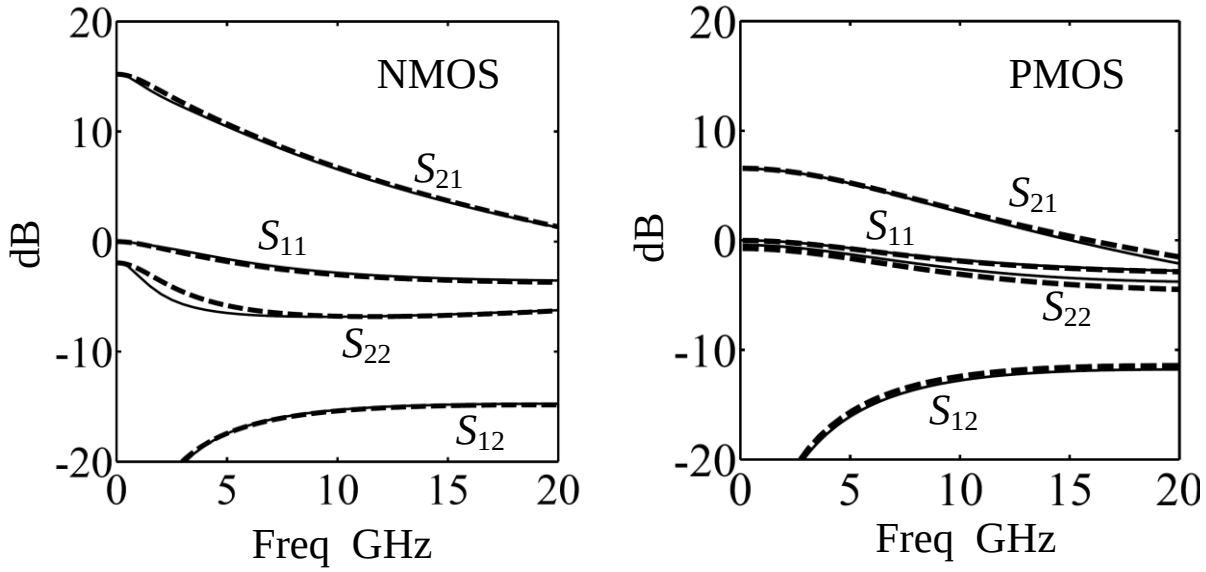


Fig. 3-2. Two-port small-signal model of a CMOS 0.18-μm transistor biased at the saturation region.



(a) (b)

Fig. 3-3. Simulated *S*-parameters from both the foundry provided design kit (solid lines) and our small-signal model (dashed lines). (a) Results of NMOS (b) Results of PMOS.

20GHz at least, as shown in Fig. 3-3, and the parameter values are tabulated in Table II. Though *S*-parameter discrepancies can be observed with the omission of R_g, C_{ds}, R_{sub}, and C_{sub}, they are relatively minor; thus, to retain the physical meaning while simplifying the

TABLE II
PARAMETERS IN THE SMALL-SIGNAL MODEL
OF THE 144-MICRON 18-FINGER TSMC N- and P-TYPE TRANSISTORS

V_{gs} = 0. 65V, I_d = 4.72mA		
Parameters	NMOS	PMOS
R_g	6.7Ω	4Ω
R_{sub}	270Ω	95Ω
C_{gd}	55fF	59fF
C_{gs}	134fF	156fF
C_{sub}	200fF	20fF
C_{ds}	42fF	26fF
g_m	43mS	21.8mS
r_{ds}	678Ω	1070Ω

mathematical derivation, these four parameters are removed from that used in the following circuit analysis.

To facilitate the analysis of the C_d-loaded complementary circuit, the small-signal circuit is shown in Fig. 3-4(a). It can be viewed as a dual feedback circuit in which the source inductors $L_{s,n}$ and $L_{s,p}$ are the local series-series feedback element and C_{gd} is the local shunt-shunt feedback element, then the problem becomes much more tractable. Here the circuit can be rearranged such that in Fig. 3-4(b), in which G_m, R_{ds}, $Z_{\beta,n}$ and $Z_{\beta,p}$ can be derived as

$$G_m = G_{m,n} + G_{m,p} \cong \frac{g_{m,n}}{1 + g_{m,n} \cdot j\omega L_{s,n}} + \frac{g_{m,p}}{1 + g_{m,p} \cdot j\omega L_{s,p}} \tag{3-1}$$

$$R_{ds} = R_{ds,n} \,//\, R_{ds,p}$$

$$\cong r_{ds,n}(1 + g_{m,n} \cdot j\omega L_{s,n}) \,//\, r_{ds,p}(1 + g_{m,p} \cdot j\omega L_{s,p}) \tag{3-2}$$

$$Z_{\beta,n} = \frac{g_{m,n} L_{s,n}}{C_{gs,n}} + \frac{1}{j\omega C_{gs,n}} + j\omega L_{s,n} = R_{\beta,n} + \frac{1}{j\omega C_{gs,n}} + j\omega L_{s,n} \tag{3-3}$$

$$Z_{\beta,p} = \frac{g_{m,p}L_{s,p}}{C_{gs,p}} + \frac{1}{j\omega C_{gs,p}} + j\omega L_{s,p} = R_{\beta,p} + \frac{1}{j\omega C_{gs,p}} + j\omega L_{s,p} \tag{3-4}$$

Then, applying the local shunt-shunt feedback theory, the impedance looking into C_{gd} branch can be derived as

$$Z_{\alpha} = \frac{\frac{1}{j\omega C_{gd}} + Z_L}{1 + G_m Z_L} = \frac{\frac{1}{j\omega C_{gd}} + (R_{ds} // (\frac{1}{j\omega C_d})}{1 + G_m (R_{ds} // \frac{1}{j\omega C_d})}$$

$$= (\frac{1}{j\omega C_{gd}} + \frac{1}{j\omega C_{gd}}) // [\frac{1}{j\omega G_m R_{ds} C_{gd}} +$$

$$(\frac{1}{\frac{C_{gd}+C_d}{G_{m,n}C_{gd}} + j\omega L_{s,n}\frac{C_{gd}+C_d}{C_{gd}} + \frac{1}{\frac{C_{gd}+C_d}{G_{m,p}C_{gd}} + j\omega L_{s,p}\frac{C_{gd}+C_d}{C_{gd}}})^{-1}] \tag{3-5}$$

With the chosen C_d = 0.2pF, $L_{s,n}$ = 0.8nH, $L_{s,p}$ = 0.4nH, compared to Re[$Z_{\beta,p}$] = 55.9Ω, $Z_{\beta,n}$ can be overlooked owing to its large impedance of Re[$Z_{\beta,p}$] = 256Ω; therefore, the input impedance can be approximated as

$$Z_{in} \cong \left(\frac{1}{Z_{\alpha}} + \frac{1}{Z_{\beta,p}}\right)^{-1} \tag{3-6}$$

And the equivalent input circuit can be arranged as that of Fig. 3-4(c). For simplicity, Z_{α} can be approximated as a series $C_{\alpha}R_{\alpha}L_{\alpha}$ circuit with a capacitor $C_{gd}C_d/(C_{gd}+C_d)$ connected in parallel, where C_{α}, R_{α}, and L_{α} are given by

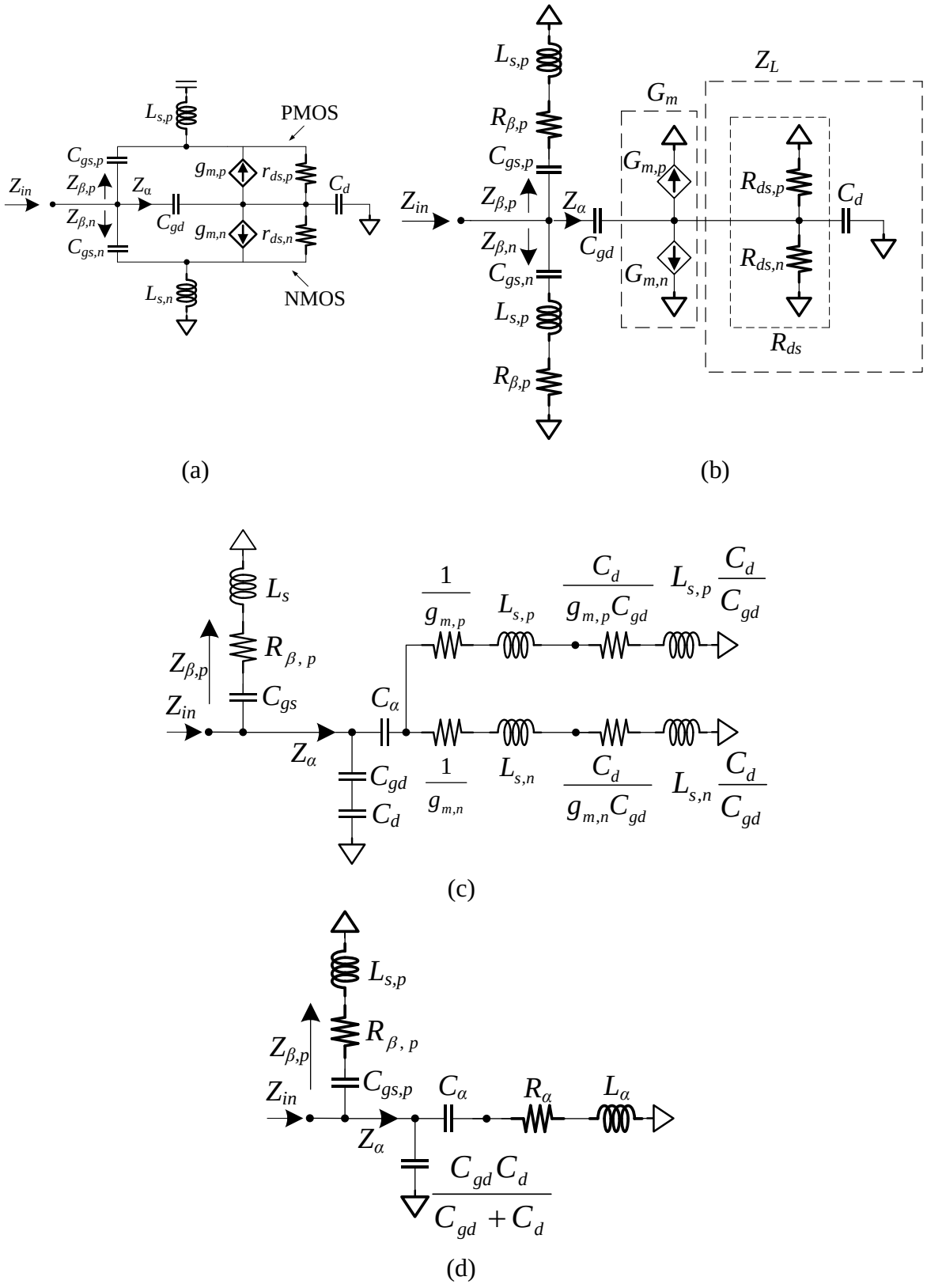
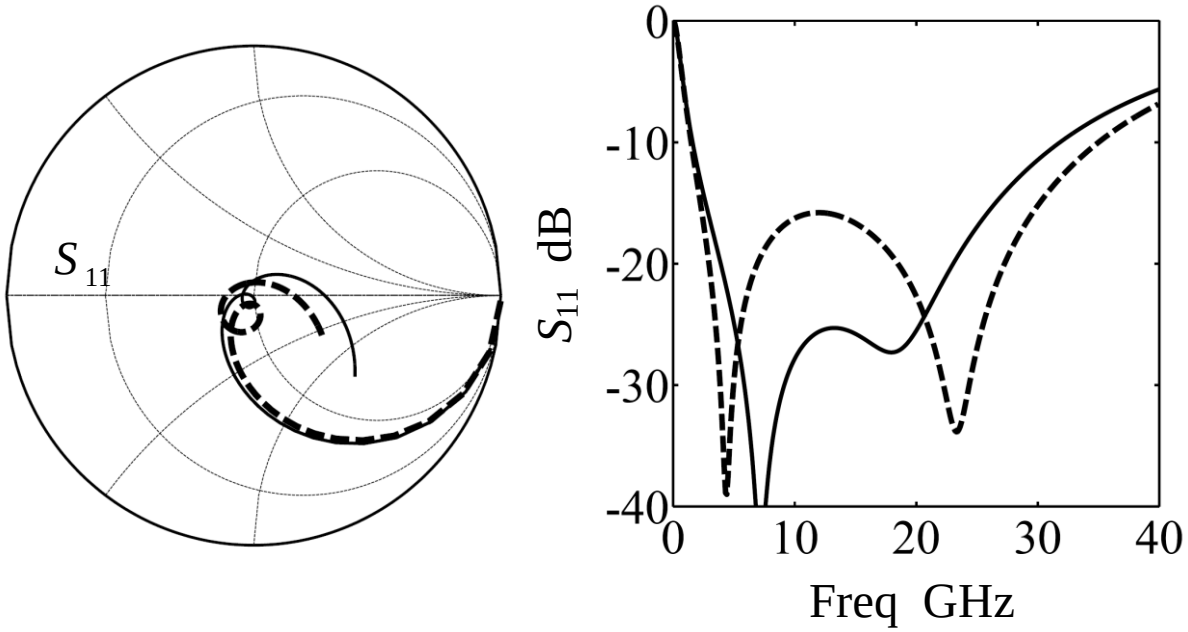


Fig. 3-4. (a) Small-signal model of the proposed transistor circuit with output C_d-loading. (b) Simplified circuit with the local series-series feedback element ($L_{s,n}$ and $L_{s,p}$) absorbed. (c) Simplified input circuit with local shunt-shunt feedback element (C_{gd}) absorbed. (d) Approximation of the input equivalent circuit.



(a) (b)

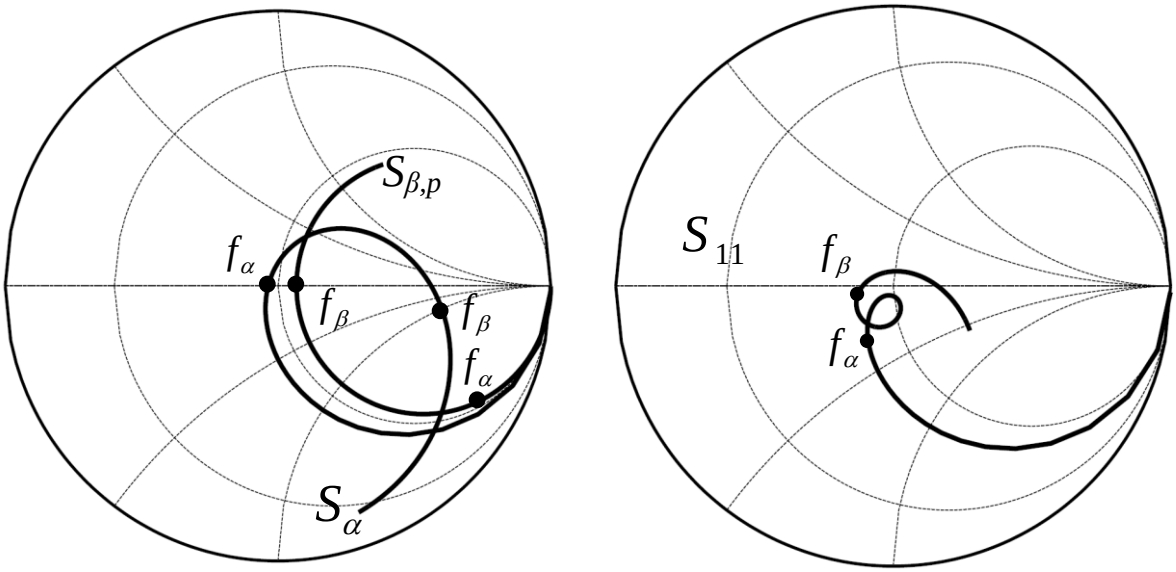
Fig. 3-5. Simulated and calculated input reflection coefficient of the C_d-loaded transistor circuit. (a) The solid curve on the Smith chart is the simulated result while the dashed curve is its calculated counterpart. (b) The same results expressed in dB vs. frequency.

$$C_\alpha \cong G_m R_{ds} C_{gd} = (G_{m,n} + G_{m,p})(R_{ds,n} // R_{ds,p}) C_{gd}; \tag{3-7}$$

$$R_\alpha = R_{\alpha,n} // R_{\alpha,p} = \frac{1}{g_{m,n}}(1 + \frac{C_d}{C_{gd}}) // \frac{1}{g_{m,p}}(1 + \frac{C_d}{C_{gd}}) \tag{3-8}$$

$$L_\alpha \cong L_{s,n} // L_{s,p} = L_{s,n}(1 + \frac{C_d}{C_{gd}}) // L_{s,p}(1 + \frac{C_d}{C_{gd}}) \tag{3-9}$$

Hence the resulting equivalent circuit can be rearranged as that of Fig. 3-4(d). In Fig. 3-5, the solid curve is the simulated result with the discussed component values; the dashed curve is the calculated counterpart using (3-6). Although the discrepancy between the simulated and calculated result which is mainly from the omission $Z_{\beta,n}$ and the approximation in the derivation of Z_α can be observed, the simplified equivalent input circuit still retains the physical insight. The derivation of the accurate equivalent input circuit is included in the



(a) (b)

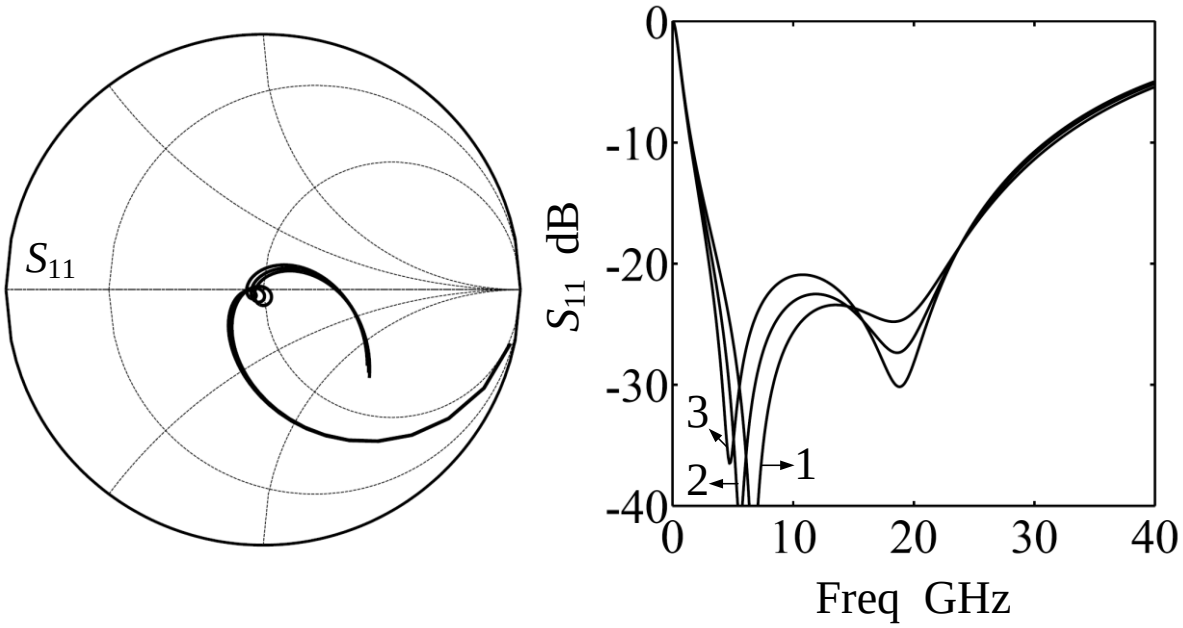
Fig. 3-6. Calculated reflection coefficient S_α, $S_{\beta,p}$, and S_{11} of the C_d-loaded transistor circuit. (a) Calculated S_α, and $S_{\beta,p}$. where f_α and $f_{\beta,p}$ are their respective resonance frequencies. (b) Calculated input reflection coefficient S_{11}.

Appendix I to verify the legitimacy of the approximated input circuit. In Fig. 3-6(a), the trajectories S_α and $S_{\beta,p}$ are the calculated reflection coefficients using (3-4) and (3-5) (i.e. Z_α and $Z_{\beta,p}$), respectively, and their respective resonant frequencies f_α and f_β can be derived as

$$f_\alpha = \frac{1}{2\pi\sqrt{L_\alpha C_\alpha}}$$

$$\cong \frac{1}{2\pi\sqrt{(L_{s,n} // L_{s,p})(g_{m,n}+g_{m,p})(r_{ds,n} // r_{ds,p})(C_{gd}+C_d)}} \quad (3\text{-}10)$$

$$f_\beta = \frac{1}{2\pi\sqrt{L_{s,p}C_{gs,p}}} \quad (3\text{-}11)$$



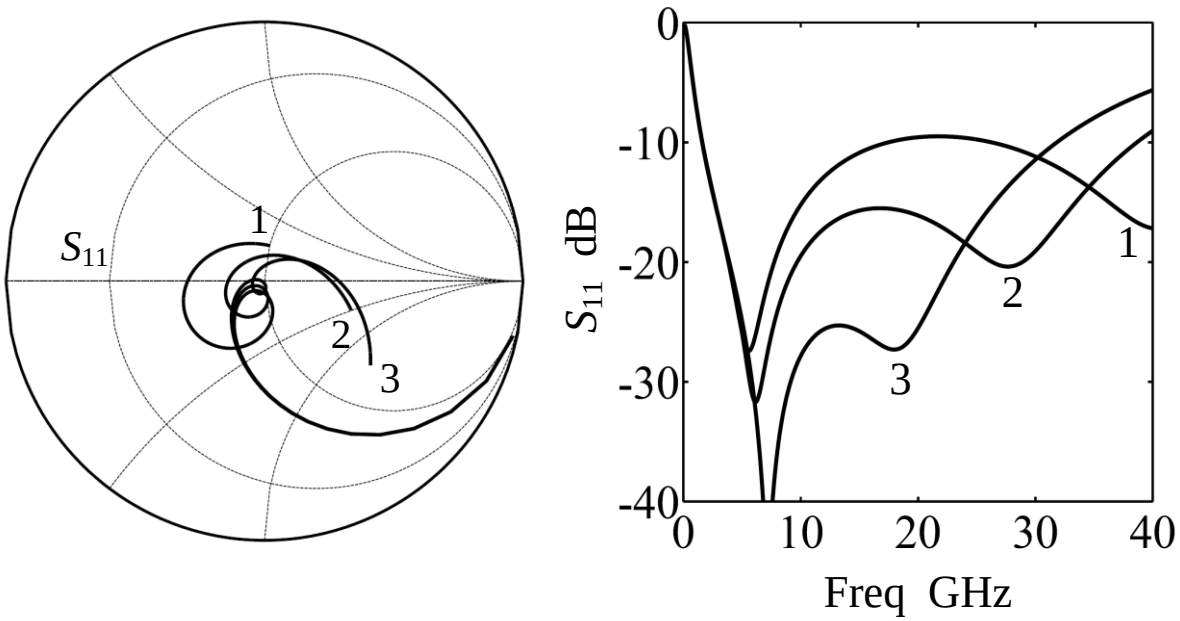
(a) (b)

Fig. 3-7. Simulated input reflection coefficient of the C_d-loaded transistor circuit with different values of $L_{s,n}$. (a) On the Smith chart, the curves correspond to $L_{s,n}$ = 0.7, 0.8, and 0.9, and all have their C_d = 0.2pF, and $L_{s,p}$ = 0.4nH. (b) The simulated S_{11} in dB vs. frequency, where curves 1-3 correspond to $L_{s,n}$ = 0.7, 0.8, 0.9nH.

With the discussed component values, the calculated f_α and f_β are 3.3GHz and 20GHz in this case, and are very close to the simulated 2.8 and 20 GHz, respectively.

Here, how the resulting input reflection coefficient S_{11} trajectory has a small loop around the zero point, as shown in Fig. 3-6(b), can now be described as follows:

(a) $f \leq f_\alpha$: At very low frequency, as the impedance of the capacitive loading C_d tends to be open and the effects of $L_{s,n}$ and $L_{s,p}$ are very small in this frequency range, the transistor's loading is dominated by the parallel connection of $R_{ds,n}$ and $R_{ds,p}$ (i.e. R_{ds}), as shown in Fig. 3-4(b). The resulting Miller capacitance $C_\alpha = G_m R_{ds} C_{gd}$ which is much larger than $C_{gs,p}$ make the Z_α branch the dominant one and puts the location of S_{in} in the capacitive region of the Smith chart. As frequency increases, the transistor's loading is now dominated by C_d , as

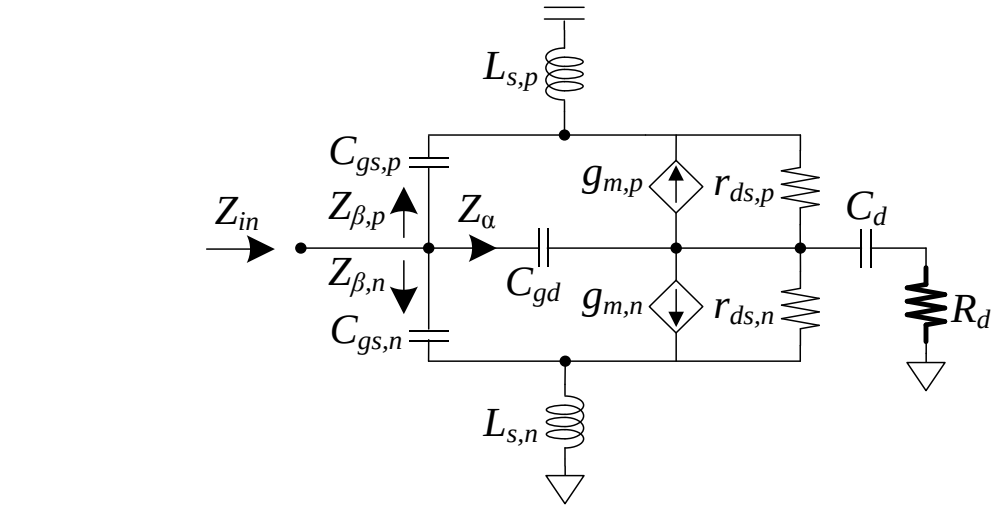


(a) (b)

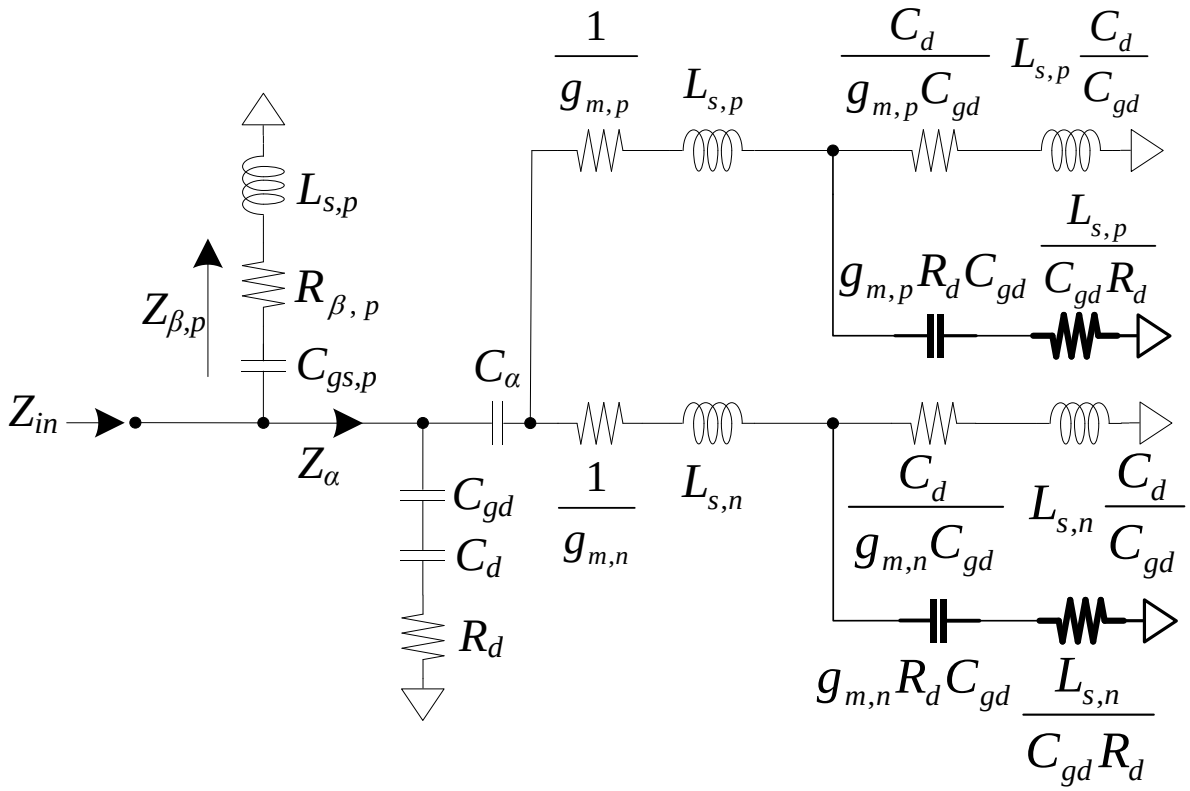
Fig. 3-8. Simulated input reflection coefficient of the C_d-loaded transistor circuit with different values of $L_{s,p}$. (a) On the Smith chart, curves 1–3 correspond to $L_{s,p}$ = 0.2, 0.3, and 0.4, respectively, and all have their C_d = 0.2pF, and $L_{s,n}$ = 0.8nH. (b) The same results expressed in dB vs. frequency.

shown in Fig. 3-4(b), which determines the real part of input impedance (i.e. Re[Z_{in}] = R_α), as in (3-8). Therefore, the S_α trajectory can be determined by C_d and moves along the constant resistance circle.

(b) $f \approx f_\alpha$: As frequency is about f_α, the influence by $L_{s,n}$ and $L_{s,p}$ on Z_α is becoming obvious, thus the aforementioned Miller capacitance will be resonated out by these source degenerated inductors $L_{s,n}$ and $L_{s,p}$. On the Smith chart, S_α will now pass by the center of the Smith chart and enter the inductive region at f_α, as indicated by (3-10). In another aspect, the S_β trajectory remaining in the capacitive region will gradually bend the S_{11} trajectory toward the capacitive region on the Smith chart. Thus S_{11} forms a loop in this frequency range. In



(a)



(b)

Fig. 3-9. (a) Small-signal circuit of the C_dR_d-loaded transistor circuit. (b) The simplified input equivalent circuit, where the darkened *RC* series circuit result from R_d, and the rest of the circuit is that of C_d-loaded circuit.

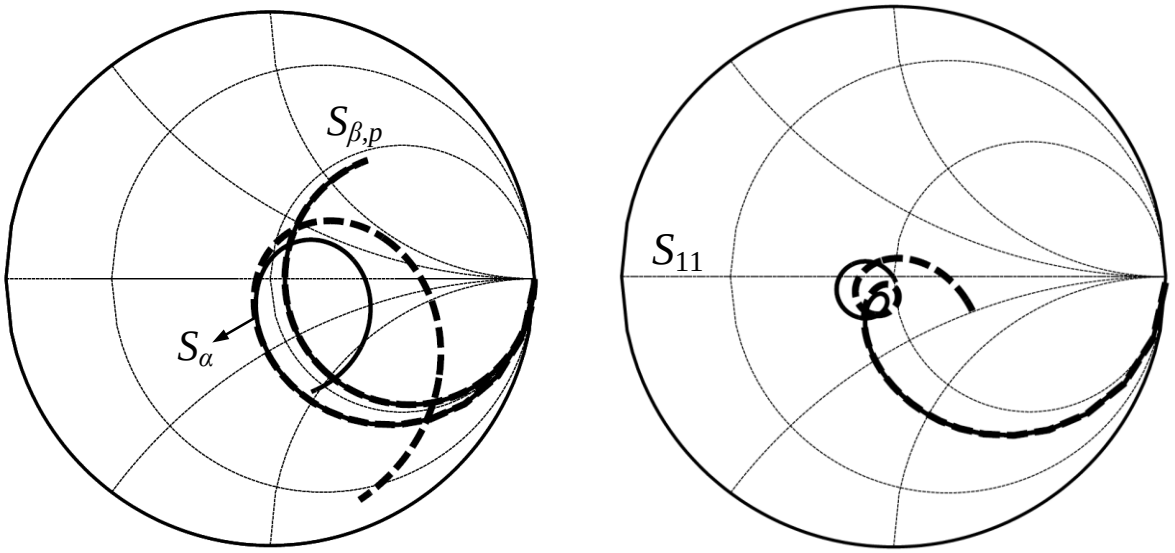
short conclusion, the circuit can achieve input matching at even lower frequency with larger values of $L_{s,n}$ and $L_{s,p}$.

(c) $f \geqq f_\beta$: As frequency increases to about f_β, as in (3-11), the shunt capacitor $C_{gd}C_d/(C_{gd}+C_d)$ in the Z_α will bend the S_α trajectory toward high impedance region on the Smith chart, as shown in Fig. 3-6(a). Hence $Z_{\beta,p}$ is the dominant factor in determining Z_{in}, thus the $L_{s,p}$ will drag the S_{11} trajectory toward the inductive region. Therefore, the larger value of $L_{s,p}$ will twist the S_{11}'s loop more rapidly and bring it closer to the zero point on the Smith chart, thus $L_{s,p}$ can manipulate the high frequency input matching.

Thus far, how by manipulating the $L_{s,p}$ and $L_{s,p}$ the S_{11} trajectory can constitute a loop around the center of the Smith chart in the frequency range from f_α to f_β has been explained. Fig. 3-7 shows the simulated input reflection coefficient with different $L_{s,n}$, where curves 1-3 have $L_{s,n}$ = 0.7, 0.8, 0.9nH, and all have C_d = 0.2pF, $L_{s,p}$ = 0.4nH. As given by (3-10), $L_{s,n}$ will control the input matching at low frequency. Fig. 3-8 shows the simulated input reflection coefficient with different $L_{s,p}$, where curves 1-3 have $L_{s,p}$ = 0.2, 0.3, 0.4nH, and all have their C_d = 0.2pF, and $L_{s,n}$ = 0.8nH. As is mentioned above, the larger value of $L_{s,p}$ will drag the S_{11}'s trajectory more rapidly across the center of the Smith chart, thus smaller input reflection coefficient over narrower bandwidth can be achieved, which can be intuitively comprehended as a small inductor gives the equivalent input circuit low quality characteristic, thus a wider bandwidth can be obtained, and vice versa. Thus far, the roles played by C_d, $L_{s,n}$, and $L_{s,p}$ in achieving wideband input matching are well explained and can be easily understood.

Analysis of the C_dR_d-loaded complementary circuit

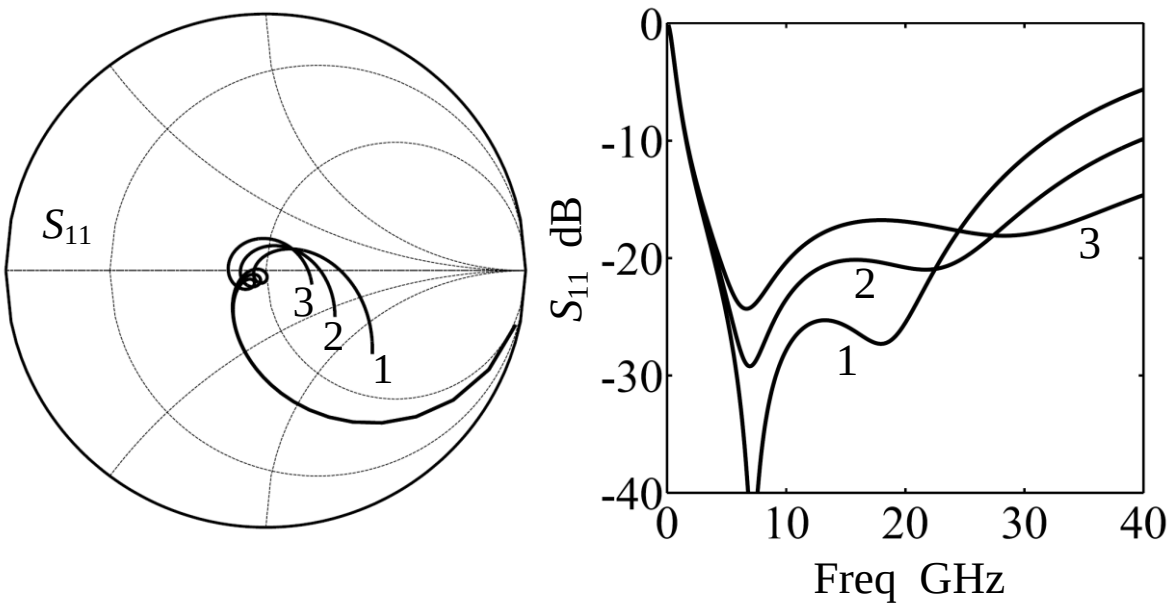
To facilitate the analysis of the proposed C_dR_d-loaded complementary circuit, the small-signal circuit is shown in Fig. 3-9(a). The corresponding equivalent input circuit should be modified as that in Fig. 3-9(b), where the two darkened *RC* series circuits originate from R_d, and the rest of the equivalent circuit is the same as that of the C_d-loaded transistor circuit, as



(a) (b)

Fig. 3-10. Calculated input reflection coefficient of the C_dR_d-loaded transistor circuit. (a) On the Smith chart, the solid curves are the simulated S_α and $S_{\beta,p}$ with R_d = 20Ω, while the dashed curves are their calculated counterparts with R_d = 0Ω. (b) The solid curves is the simulated S_{11} with R_d = 20Ω, while the dashed curve is its calculated counterpart with R_d = 0Ω.

shown in Fig. 3-4(c). In Fig. 3-10, the solid curves are the calculated S_α and $S_{\beta,p}$ with R_d = 20Ω, while the dashed curves correspond R_d = 0Ω; and C_d = 0.2pF, $L_{s,n}$ = 0.8nH, $L_{s,p}$ = 0.4nH in both cases. Apparently, the two darkened *RC* series circuits in the quivalent input circuit can bend the S_α trajectory toward the capacitive region especially in the high frequency range, which can keep the resulting S_{11} trajectory loop closer to the zero point. Hence the transistor circuit can have matched input impedance over even wider bandwidth, which can be verified through the simulated result. Fig. 3-11 shows the simulated input reflection coefficient with different values of R_d, where curves 1-3 have R_d = 0, 10, 20Ω, and C_d = 0.2pF, $L_{s,n}$ = 0.8nH, $L_{s,p}$ = 0.4nH in all three cases.



(a) (b)

Fig. 3-11. Simulated input reflection coefficient of the C_dR_d-loaded transistor circuit with different values of R_d. (a) On the Smith chart, curves 1–3 correspond to R_d = 0, 10, and 20Ω, respectively, and all have their C_d = 0.2pF, and $L_{s,n}$ = 0.8nH, $L_{s,p}$ = 0.4nH. (b) The same results expressed in dB vs. frequency.

Analysis of the $C_dR_dL_d$-loaded complementary circuit

To facilitate the analysis of the proposed $C_dR_dL_d$-loaded complementary circuit, the small-signal circuit is shown in Fig. 3-12(a) and it can be rearranged such as that in Fig. 3-12(b), where Z_α can be derived as

$$Z_\alpha = \frac{\frac{1}{j\omega C_{gd}} + (Z_L)}{1 + G_m Z_L}$$

$$= \frac{\frac{1}{j\omega C_{gd}} + [R_{ds} // (\frac{1}{j\omega C_{gd}} + R_d + j\omega L_d)]}{1 + G_m [R_{ds} // (\frac{1}{j\omega C_{gd}} + R_d + j\omega L_d)]} \quad (3\text{-}12)$$

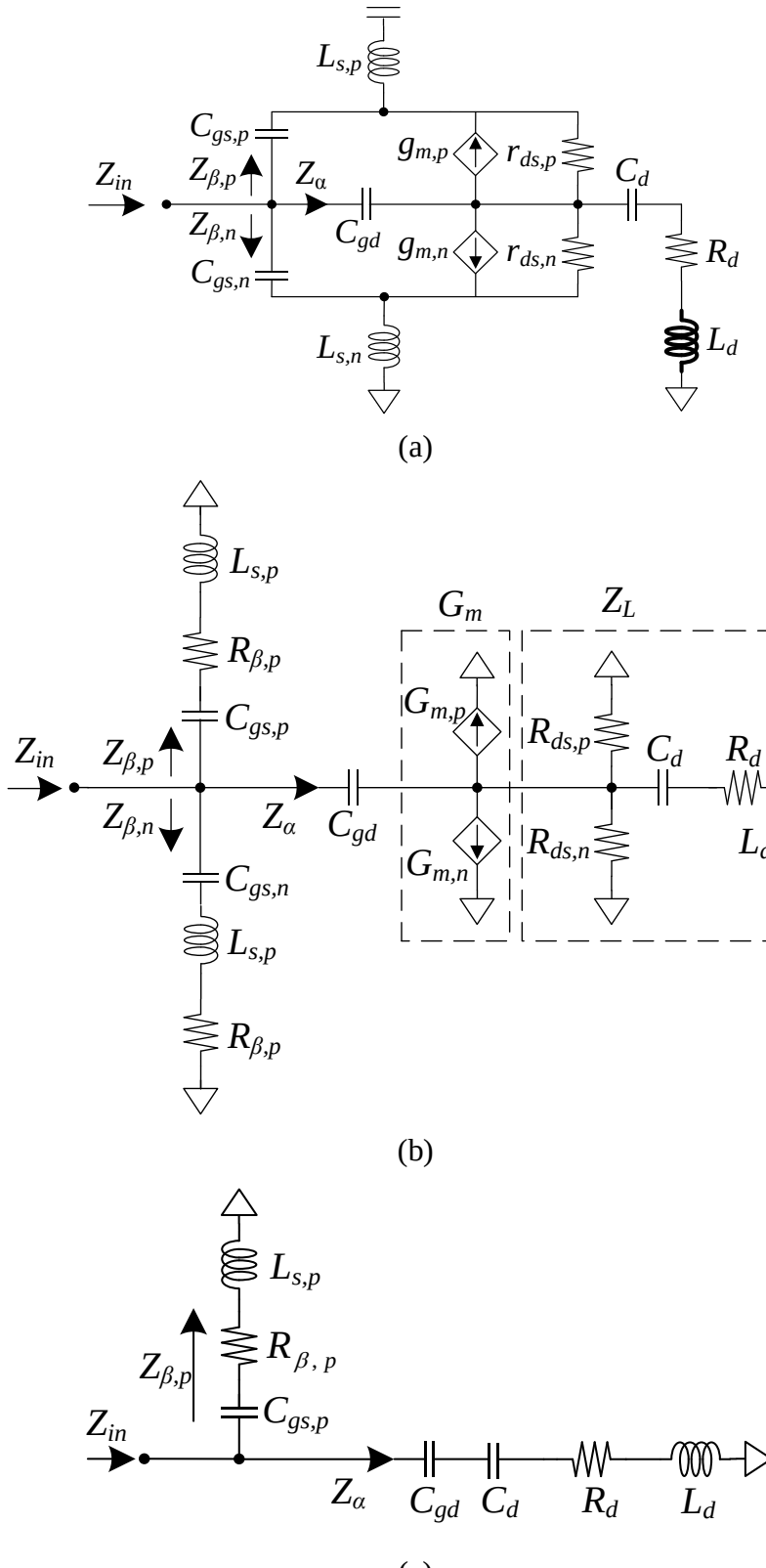
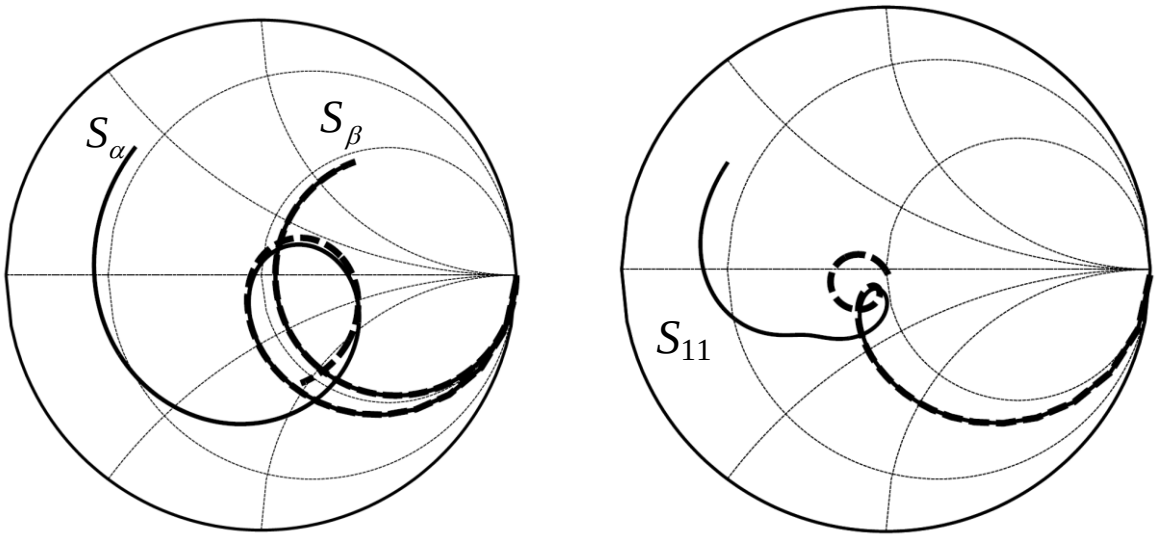


Fig. 3-12. (a) Small-signal circuit of the proposed $C_dR_dL_d$–loaded transistor circuit. (b) Simplified circuit with the local series-series feedback element ($L_{s,n}$ and $L_{s,p}$) absorbed. (c) Approximated input equivalent circuit accounting for high frequency behavior of the $C_dR_dL_d$–loaded transistor circuit.



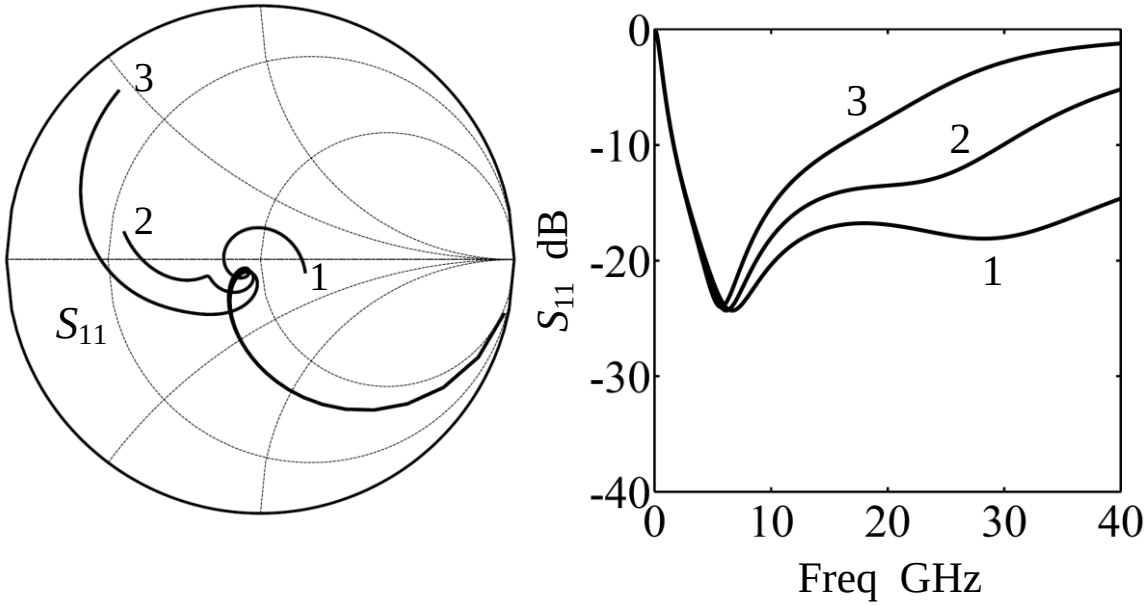
(a) (b)

Fig. 3-13. Calculated input reflection coefficient of the $C_dR_dL_d$-loaded transistor circuit. (a) On the Smith chart, the solid curves are the simulated S_α and $S_{\beta,p}$ with L_d = 0.4nH, while the dashed curves are their calculated counterparts with L_d = 0nH. (b) The solid curves is the simulated S_{11} with L_d = 0.4nH, while the dashed curve is its calculated counterpart with L_d = 0nH.

where G_m, R_{ds} are given by (3-1)~(3-2). As the $C_dR_dL_d$ series circuit tends to be resonant, its small impedance make the resulting Miller effect (i.e. G_mZ_L) insignificant, thus Z_α can be approximated as

$$Z_\alpha \cong \frac{1}{j\omega C_{gd}} + Z_L \cong \frac{1}{j\omega C_{gd}} + \frac{1}{j\omega C_d} + R_d + j\omega L_d \tag{3-13}$$

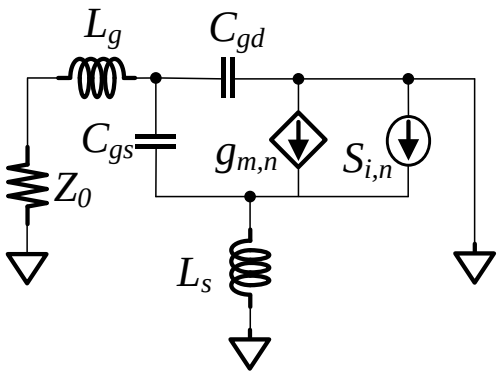
In Fig. 3-13, the solid curves are the calculated reflection coefficient S_α and $S_{\beta,p}$ with L_d = 0.4nH, while the dashed curves correspond to those with L_d = 0nH, and C_d = 0.2pF, R_d = 20Ω, $L_{s,n}$ = 0.8nH, $L_{s,p}$ = 0.4nH in both cases. As indicated in (3-13), the drain inductor L_d will drag



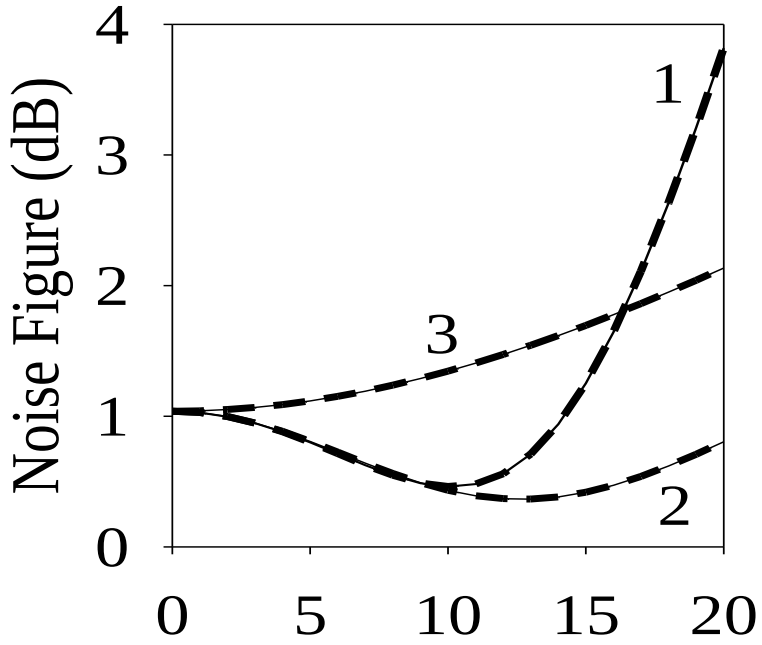
(a) (b)

Fig. 3-14. Simulated input reflection coefficient of the $C_dR_dL_d$-loaded transistor circuit with different values of L_d. (a) On the Smith chart, curves 1–3 correspond to L_d = 0, 0.2, and 0.4nH, respectively, and all have their C_d = 0.2pF, R_d = 20Ω, $L_{s,n}$ = 0.8nH, and $L_{s,p}$ = 0.4nH. (b) The same results expressed in dB vs. frequency.

the S_α trajectory toward the inductive region of the Smith chart, thus the resulting S_{11} trajectory passes by the center of the Smith chart more rapidly with the inclusion of L_d, which indicates the L_d will narrow the input matching bandwidth. Fig. 3-14 shows the simulated input reflection coefficient with different L_d, where curves 1-3 have L_d = 0, 0.2, 0.4nH, and all have C_d = 0.2pF, R_d = 20Ω, $L_{s,n}$ = 0.8nH, $L_{s,p}$ = 0.4nH. Thus far, the roles played by C_d, R_d, L_d, $L_{s,n}$, and $L_{s,p}$ are well explained and can be easily understood.



(a)



(b)

Fig. 3-15. Small-signal circuit of a common-source transistor circuit with the gate and source inductors L_g and L_s, and its corresponding simulated and calculated results. (a) $S_{i,n}$ denotes the channel thermal noise power. (b) The solid curves 1-3 correspond to the simulated results with L_g = 1nH, L_s = 1nH; L_g = 0nH, L_s = 1nH; and L_g = 0nH, L_s = 0nH, respectively; the overlapped dashed curves are their calculated counterparts using (2)-(3).

3.3 Noise Analysis

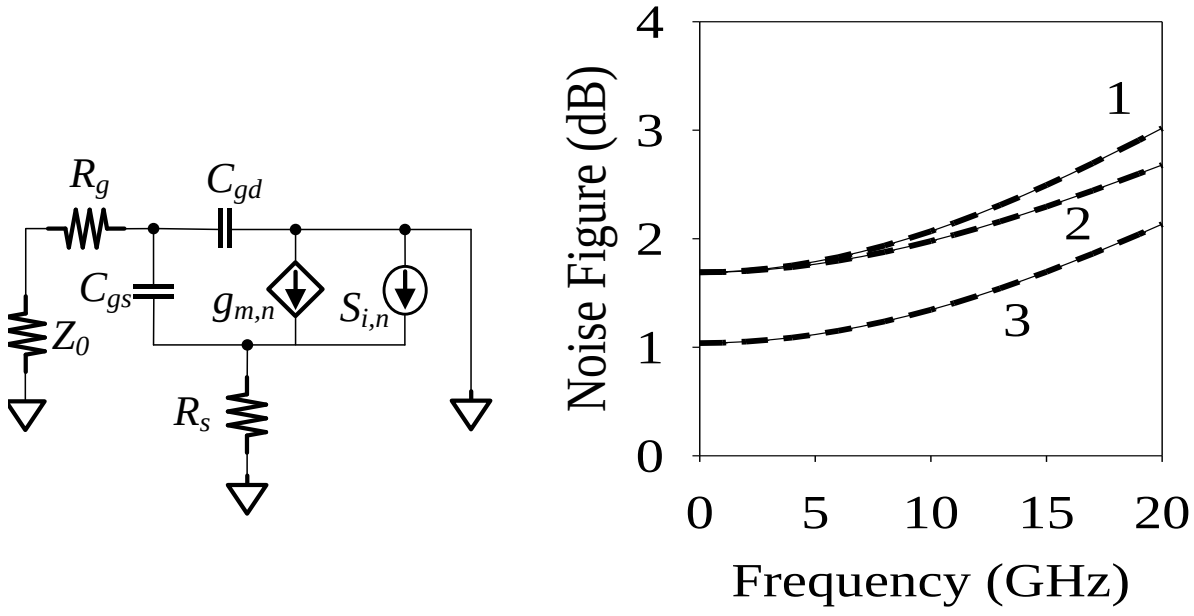
Before analyzing the noise performance of the proposed complementary topology with

asymmetrical inductive source degeneration, the major noise sources in the n- and p-type transistors should be extracted. To keep the analytic expressions for the noise factor of the proposed circuit as simple as possible, only the drain channel noise are considered [15]-[16]. Throughout this paper, in the case of our devices, the extracted channel noise powers for n- and p-type transistors, denoted as $S_{i,n}$ and $S_{i,p}$, are 400 $\times 10^{-24}$ A^2/Hz and 200 $\times 10^{-24}$ A^2/Hz, respectively. Now, Fig. 3-15(a) shows the transistor circuit with the gate inductor L_g and the source inductor L_s. To clarify the impacts of the gate and source inductor on the transistor circuit's noise performance, the noise factor can be derived by replacing its output loading with a short circuit. Since the input noise temperature of a two-port circuit is a function of its generator impedance, but not its output loading impedance, this short-circuit arrangement is legitimate with the additional advantage of simplifying the derivation procedure. Also, to investigate the roles of L_g and L_s, the noise factor for the transistor circuit with L_g and that with L_s, denoted as F_{Lg} and F_{Ls}, are respectively derived as

$$F_{Lg} = 1 + \frac{S_{i,n}}{4kT_o Z_0 g_{m,n}^2}\left\{1 + \omega^2[(C_{gs}+C_{gd})^2 Z_o^{\,2} - 2(C_{gs}+C_{gd})L_g] + \omega^4 (C_{gs}+C_{gd})^2 L_g^{\,2}\right\} \tag{3-14}$$

$$F_{Ls} = 1 + \frac{S_{i,n}}{4kT_o Z_0 g_{m,n}^2}\left\{\omega^2 C_{gs}^2 \left(\frac{Z_o}{Z_o j\omega C_{gd}+1}\right)^2 + [1-\omega^2 C_{gs} L_s]^2\right\} \tag{3-15}$$

$$\cong 1 + \frac{S_{i,n}}{4kT_o Z_0 g_{m,n}^2}\left\{1 + \omega^2[C_{gs}^{\,2} Z_o^{\,2} - 2C_{gs}L_s] + \omega^4 C_{gs}^2 L_s^{\,2}\right\}$$



(a) (b)

Fig. 3-16. Schematic used to clarify the parasitic resistors of L_s and L_g, i.e. R_s and R_g, and its corresponding simulated and calculated results. (a) $S_{i,n}$ denotes the channel thermal noise power. (b) The solid curves 1-3 correspond to the simulated results with R_g = 10Ω, R_s = 0Ω; R_g = 0Ω, R_s = 10Ω; and R_g = 0Ω, R_s = 0Ω, respectively; the overlapped dashed curves are their calculated counterparts using (3-16)-(3-17).

where Z_o is the generator 50Ω, k is the Boltzmann's constant, T_0 is the absolute temperature. Clearly, observing (3-14) and (3-15), the increase of the noise figure with frequency mainly comes from C_{gs} and C_{gd}, which is the reason why employing L_g and L_s can neutralize the effect of C_{gs} and C_{gd},. Particularly, in the absence of L_s, the noise figure soars upward with frequency quickly. Fig. 3-15(b) shows the simulated and the calculated noise figures using (3-14)~(3-15), where the solid curves 1-3 correspond to the simulated results with L_g = 1nH, L_s = 0nH; L_g = 0nH, L_s = 1nH; and L_s = 0nH, L_g = 0nH, respectively; the overlapped dashed curves are their calculated counterparts using (3-14)~(3-15). The agreement between the

simulated and calculated results confirms the accuracy of the derivation. As is seen, the case with L_s has lower noise figure over a wide bandwidth than that with L_g. Accordingly, we prefer L_s to L_g.

To characterize the roles of the parasitic resistors of L_g and L_s, i.e. R_g and R_s, the circuit is shown in Fig. 3-16(a). The noise factor for the circuit with R_g and that with R_s, denoted as F_{Rg} and F_{Rs}, are respectively derived as

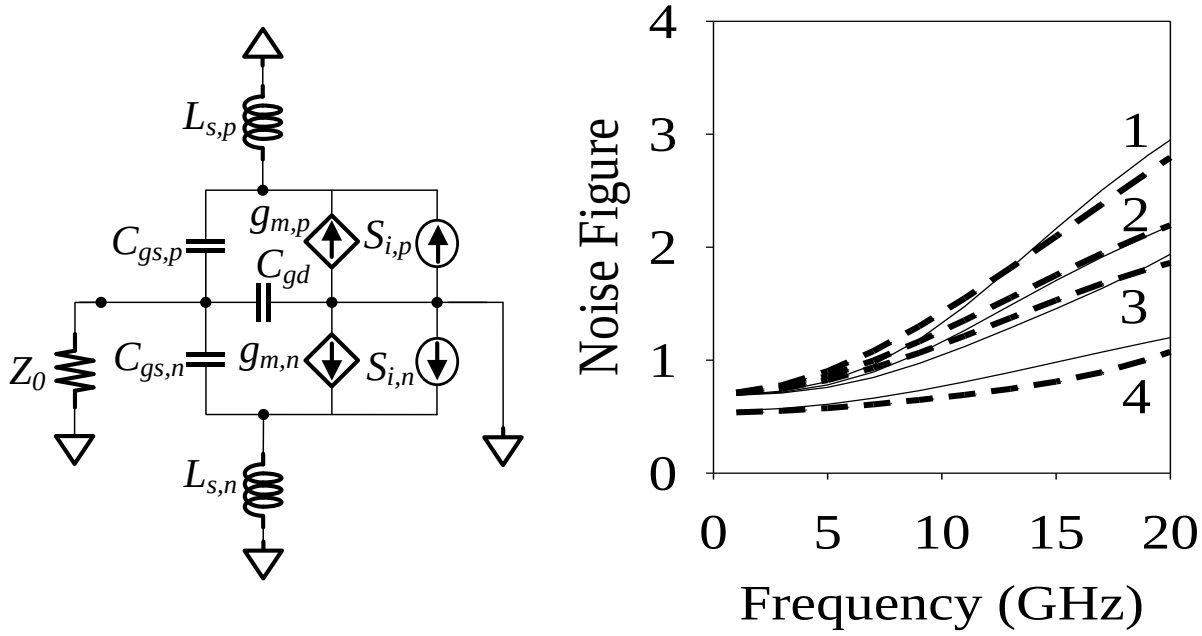
$$F_{Rg} = 1 + \frac{R_g}{Z_o} + \frac{S_{i,n}}{4kT_o Z_o g_{m,n}^2}\left[\omega^2 (C_{gs} + C_{gd})^2 (Z_0 + R_g)^2 + 1\right] \tag{3-16}$$

$$F_{Rs} = 1 + \frac{R_s}{Z_o} + \frac{S_{i,n}}{4kT_o Z_o g_{m,n}^2}\left[\omega^2 C_{gs}^2 \left(\frac{Z_0}{Z_0 j\omega C_{gd} + 1} + R_s\right)^2 + 1\right] \tag{3-17}$$

$$\cong 1 + \frac{R_s}{Z_o} + \frac{S_{i,n}}{4kT_o Z_o g_{m,n}^2}\left[\omega^2 C_{gs}^2 (Z_0 + R_s)^2 + 1\right]$$

Consequently, F_{Rg} approximately equals to F_{Rs} especially at low frequency Fig. 3-16(b) shows the simulated and the calculated noise figures using (4)-(5), where solid curves 1-3 correspond to the simulated results with R_g = 10Ω, R_s = 0Ω; R_g = 0Ω, R_s = 10Ω; and R_s = 0Ω, R_g = 0Ω, respectively; the overlapped dashed curves are their calculated counterparts using (3-16)-(3-17), where the validity of the derivation is again confirmed. Since R_g and R_s contribute almost the same amount of noise power at output, they must render nearly the same noise figures.

In acknowledgement of the advantage of using the source inductor L_s rather than the gate inductor L_g in the common source topology, we now are ready to analyze the noise factor for the complementary topology with asymmetrical inductive degeneration, as shown in Fig. 3-17(a). Here, the noise factor of the complementary circuit is derived as



(a) (b)

Fig. 3-17. Small-signal circuit of a complementary transistor circuit with the two source inductors $L_{s,n}$ and $L_{s,p}$, and its corresponding simulated and calculated results. (a) $S_{i,n}$ and $S_{i,p}$ denote the channel thermal noise powers of the n- and p-type transistors, respectively. (b) The solid curves 1-3 correspond to the simulated results with $L_{s,p}$ = 0.2nH, 0.4nH, and 0.6nH, respectively, while $L_{s,n}$ is kept at 0.7nH; the dashed curves are their calculated counterparts using (3-18)-(3-19). The solid curve 4 is the simulated result with $L_{s,n}$ = 0.7nH, and $L_{s,p}$ = 0.6nH as the n-type transistor is replaced with the p-type one; the dashed curve 4 is its calculated counterpart.

$$F = 1 + \frac{S_{i,n}}{4kT_oZ_0}\left|\frac{\frac{Z_o}{Z_o j\omega C_{gd}+1} + (\frac{1}{j\omega C_{gs,n}} + j\omega L_{s,n})\frac{Z_{c,p}}{Z_{c,n}+Z_{c,p}^{'}}}{(\frac{Z_{c,n}Z_{c,p}}{Z_{c,n}+Z_{c,p}})(G_{m,n}+G_{m,p})}\right|^2$$

$$+\frac{S_{i,p}}{4kT_oZ_0}\left|\frac{\frac{Z_o}{Z_o j\omega C_{gd}+1}+(\frac{1}{j\omega C_{gs,p}}+j\omega L_{s,p})\frac{Z_{c,n}}{Z_{c,n}+Z_{c,p}^{'}}}{(\frac{Z_{c,n}Z_{c,p}}{Z_{c,n}+Z_{c,p}})(G_{m,n}+G_{m,p})}\right|^2 \quad (3\text{-}18)$$

where

$$Z_{c,n}=\frac{1}{j\omega C_{gs,n}}+j\omega L_{s,n}+\frac{g_{m,n}L_{s,n}}{C_{gs,n}}$$

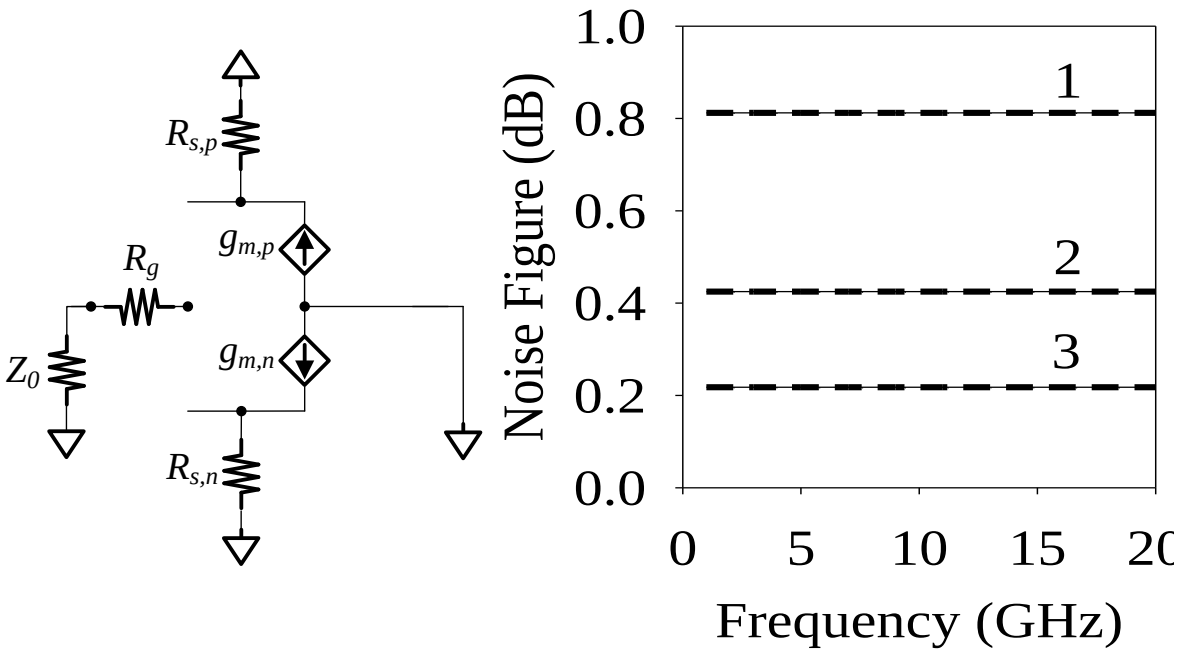
$$Z_{c,p}=\frac{1}{j\omega C_{gs,p}}+j\omega L_{s,p}+\frac{g_{m,p}L_{s,p}}{C_{gs,p}}$$

$$G_{m,n}=g_{m,n}\left(1-\omega^2 C_{gs,n}L_{s,n}+j\omega L_{s,n}g_{m,n}\right)$$

$$G_{m,p}=g_{m,p}\left(1-\omega^2 C_{gs,n}L_{s,p}+j\omega L_{s,p}g_{m,p}\right) \quad (3\text{-}19)$$

Like the source inductive degeneration in the common source circuit, $L_{s,n}$ and $L_{s,p}$ in the complementary topology can neutralize the effect of C_{gs} and C_{gd}. Therefore, by properly choosing the $L_{s,n}$ and $L_{s,p}$, the superb noise of the complementary circuit can be obtained over the entire band. Fig. 3-17(b) shows the simulated and the calculated noise figures using (3-18)-(3-19), where the solid curves 1-3 correspond to the simulated results with $L_{s,p}$ = 0.2nH, 0.4nH, and 0.6nH, respectively, while $L_{s,n}$ is kept at 0.7nH; the dashed curves are their calculated counterparts using (3-18)-(3-19). As is seen, the merit of the proposed topology is justified.

Still, one may wonder whether the use of the p-type transistor would deteriorate the total noise of the complementary circuit or not. At very low frequency, the noise factor is approximated as



(a) (b)

Fig. 3-18. Schematics used to clarify the effect of the parasitic resistors of $L_{s,n}$ and $L_{s,p}$, i.e. $R_{s,n}$ and $R_{s,p}$. (a) The parasitic capacitors for the n- and p-type transistors are omitted to simplify the derivation. (b) The solid curve 1 is the simulated result with R_g = 10Ω, and $R_{s,n}$ = $R_{s,p}$ = 0Ω, the solid curves 2-3 respectively correspond to R_g = 0Ω, $R_{s,n}$ = $R_{s,p}$ = 10Ω and R_g = 0Ω, $R_{s,n}$ = $R_{s,p}$ = 5Ω; the overlapped dashed curves are their calculated counterparts using (3-20).

$$F = \frac{S_{i,n} + S_{i,p}}{4kT_o R_g (g_{m,n} + g_{m,p})^2} \tag{3-20}$$

Since both the channel noise power and the transconductance of the p-type transistor are smaller than those of the n-type transistor, the use of p-type transistor will slightly compromise the noise figure of the complementary topology, according to (3-20). When the

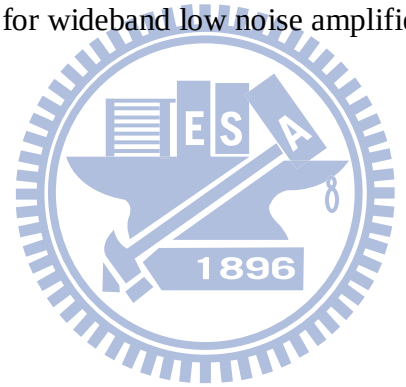
parameters of the p-type transistor are replaced with those of the n-type transistor, the noise figure will be slightly lowered compared with the original complementary topology. As is seen in Fig. 3-17(b), the solid curve 4 is the simulated result with $L_{s,n}$ = 0.7nH, and $L_{s,p}$ = 0.6nH; the dashed curve 4 is its calculated counterpart using (3-18)-(3-19). Further, the noise figure of the complimentary topology seems to increase with frequency quickly. The reason for this is simple: it mainly comes from the totally large parasitic capacitors of the topology, which is unavoidable in the case that a large size transistor is required. With the external resistive drain bias circuit no more needed in the complementary topology, not just the signal loss can be minimized; noise performance of the amplifier can also be improved.

Though the source inductive degenerated technique is beneficial to the circuit's noise figure, there is still a pending question on whether the parasitic resistors of the two lossy source inductors will adversely affect the noise figure of the complementary topology. Fig. 3-18(a) shows the complementary transistor circuit with the gate resistor R_g, which accounts for the parasitic resistors of the input matching network, and the two source resistors $R_{s,n}$ and $R_{s,p}$, which represent the parasitic resistors of the two source inductors $L_{s,n}$ and $L_{s,p}$, respectively. Here, for not losing the focus on $R_{s,n}$ and $R_{s,p}$, the channel thermal noise and the parasitic capacitances (i.e. C_{gs} and C_{gd}) are omitted to in the derivation of the noise factor, which is

$$F = \frac{R_{s,n}\left|\frac{g_{m,n}}{1+g_{m,n}R_{s,n}}\right|^2 + R_{s,p}\left|\frac{g_{m,p}}{1+g_{m,p}R_{s,p}}\right|^2}{Z_0\left|\frac{g_{m,n}}{1+g_{m,n}R_{s,n}} + \frac{g_{m,p}}{1+g_{m,p}R_{s,p}}\right|^2} \tag{3-21}$$

As the fact that noise factor is the ratio of the total output noise power to the output noise power due to the generator 50ohm alone. And, the noise powers of $R_{s,n}$ and $R_{s,p}$ respectively reach the output node through $g_{m,n}$ and $g_{m,p}$, while that of the generator 50ohm reaches the

output node through both $g_{m,n}$ and $g_{m,p}$, thus the noise contributions from $R_{s,n}$ and $R_{s,p}$ can be dramatically suppressed by that from the generator 50Ω. Fig. 3-18(b) shows the simulated and the calculated noise factor using (3-21), where the solid curve 1 is the simulated result with R_g = 10Ω, and $R_{s,n}$ = $R_{s,p}$ = 0Ω, the solid curves 2-3 respectively correspond to R_g = 0Ω, $R_{s,n}$ = $R_{s,p}$ = 10Ω and R_g = 0Ω, $R_{s,n}$ = $R_{s,p}$ = 5Ω; the overlapped dashed curves are their calculated counterparts using (3). Apparently, the noise figure of the complementary topology with the two resistors $R_{s,n}$ and $R_{s,p}$ is superior to that with the gate resistor R_g of the same value. What is more, the values of the source resistors $R_{s,n}$ and $R_{s,p}$ are practically small since the high quality factor of the small source inductors. No mention that the newly proffered complementary topology can exempt from using the large lossy gate inductors, thus it is deemed to be a good design for wideband low noise amplifier.



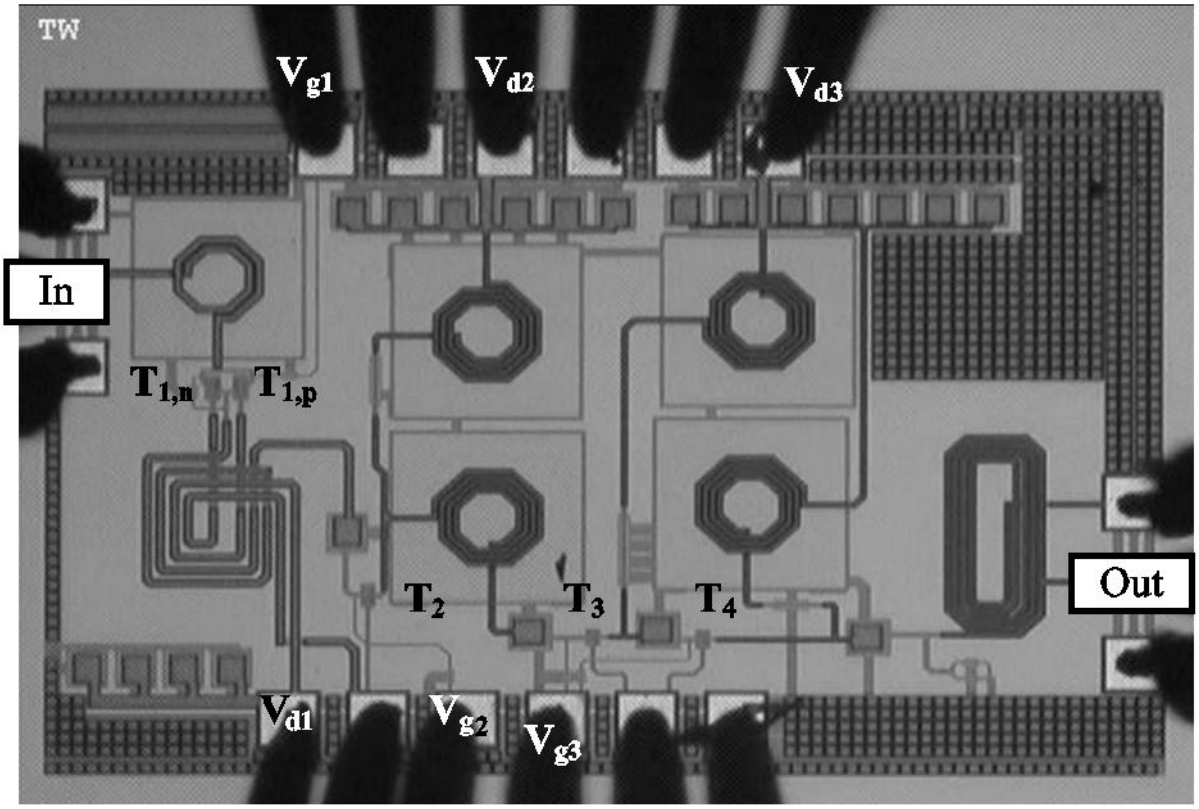


Fig. 3-19. Photograph of the 2–10GHz LNA. The chip size is 1250×850 μm^2. $T_{1,n}$, $T_{1,p}$ are the complementary transistors; T_2, T_3, and T_4 are the second-, third-, and forth-stage transistors.

3.4 LNA Design and Experimental Results

With the matching mechanism explored, a wideband CMOS LNA that covers 2-10 GHz is designed and fabricated using TSMC 0.18-μm RF-CMOS process. Figs. 3-19 and 3-20 show the photograph and schematic of the four-stage circuit where the complementary transistor topology is combined with asymmetrical inductive source degeneration. The couplings between $L_{s,n}$, $L_{s,p}$, and L_d (for gain boosting) allow the reduction of chip size. Although the magnetic couplings alter the input match slightly, the inductor values are then adjusted to recenter the matching and resonance characteristics. Fig. 3-21(a) depicts the newly proposed transistor circuit, where $M_{n,p}$ denotes the mutual inductance between $L_{s,n}$ and $L_{s,p}$,

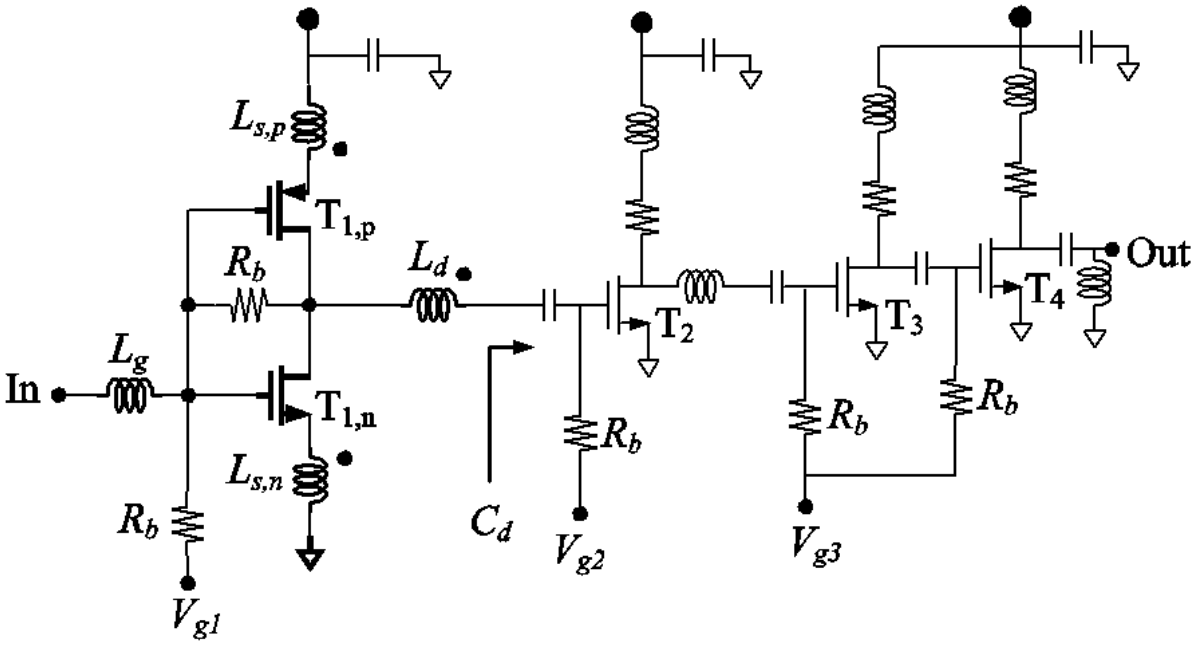
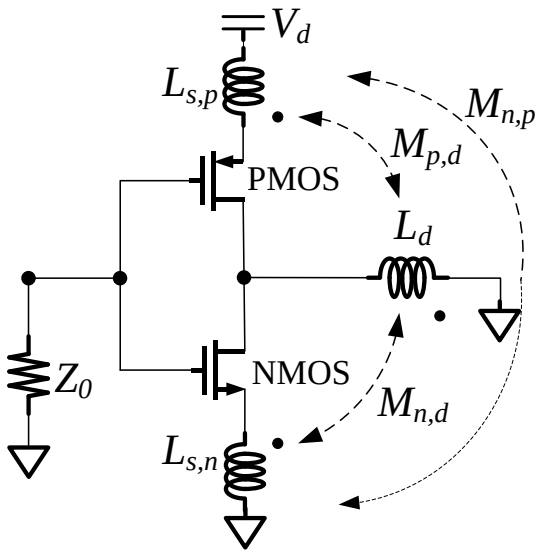
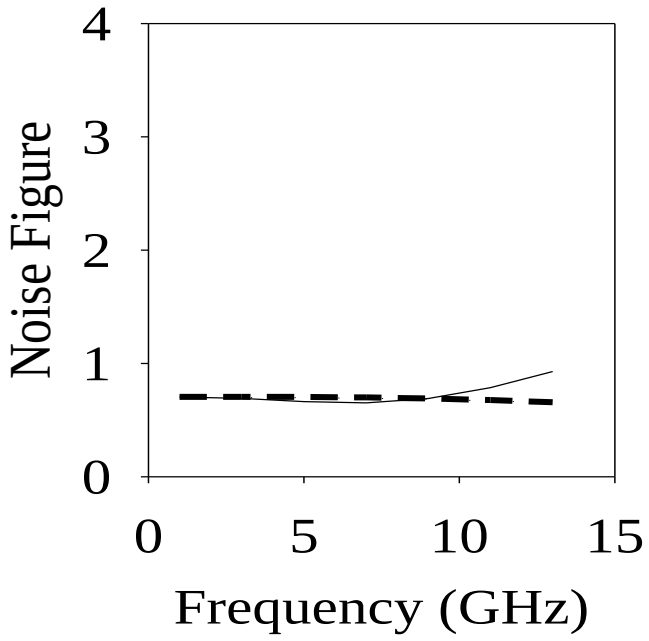


Fig. 3-20 Schematic of our proposed LNA. The equivalent loading capacitor C_d is 0.3 pF, L_d is 1 nH, $L_{s,n}$ is 0.6 nH, and $L_{s,p}$ is 0.5 nH, L_g is 0.5 nH. The bias resistors R_b are all 5185 Ω.

$M_{n,d}$ denotes the mutual inductance between $L_{s,n}$ and L_d, $M_{p,d}$ denotes the mutual inductance between $L_{s,p}$ and L_d. Fig. 3-21(b) shows the simulated noise figures, where the solid curve corresponds to $L_{s,n} = L_{s,p} = L_d = 1.5$nH, and has $M_{n,p} = M_{n,d} = M_{p,d} = 0$nH, while the dashed curve corresponds to $L_{s,n} = L_{s,p} = L_d = 0.5$nH, and has $M_{n,p} = M_{n,d} = M_{p,d} = 0.5$nH. From the small-signal and noise point of view, the mutual inductances between $L_{s,n}$, $L_{s,p}$, and L_d can essentially supply the required source inductive degeneration for both n- and p-type transistors, so that we can implement the complementary topology of the first stage with the smaller inductors, as can be confirmed in Fig 3-21(b).The small gate inductor L_g is used for S_{11} tweaking. Fig. 3-22 shows the measured and simulated *S*-parameters of this LNA where both S_{11} and S_{22} are below -10 dB, S_{21} is around 20 dB, and S_{12} lies below -30 dB. To account for the process variation, two transistor models, both provided by the same foundry, are employed in the simulation. In our measurement, we use $V_{d1} = 1.5$ V and $I_{d1} = 4.2$ mA for the first-stage complementary transistors, $V_{d2} = 1.5$ V and $I_{d2} = 5.8$ mA for the second-stage

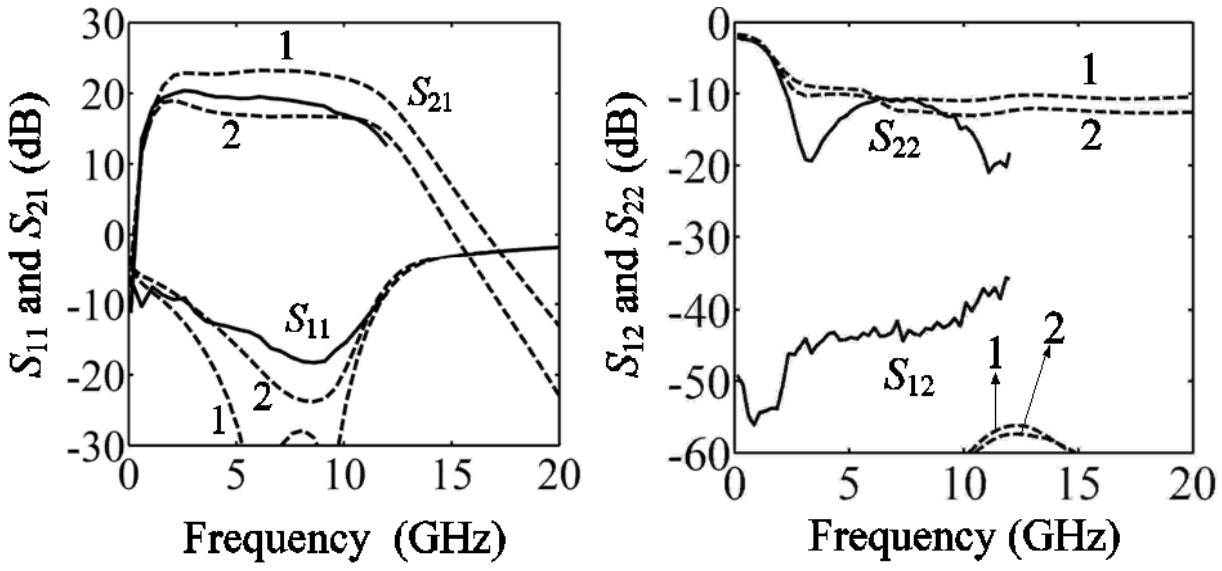


(a)



(b)

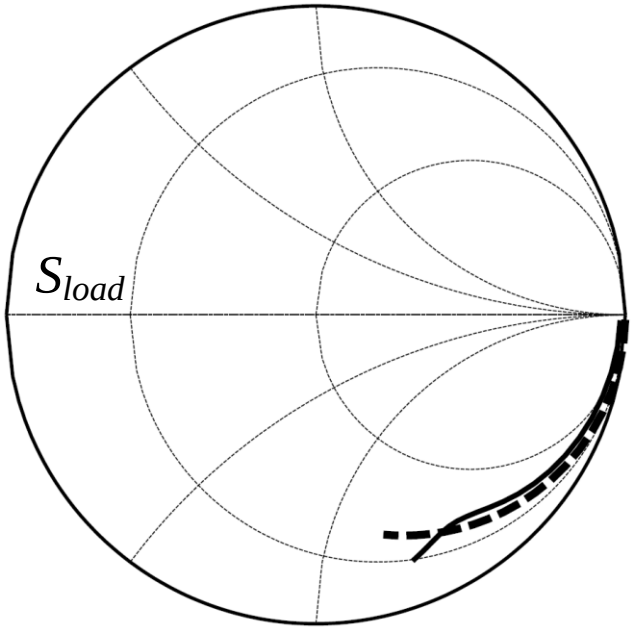
Fig. 3-21. The complementary circuit with the coupled inductors and its simulated noise figure. (a) *Mn,p*, *Mn,d*, and *Mp,d* denote the mutual inductance between *Ls,n*, *Ls,p*, and *Ld*. (b) The solid curve corresponds to *Ls,n* = *Ls,p* = *Ld* = 1.5nH, and has *Mn,p* = *Mn,d* = *Mp,d* = 0nH, while the dashed curve corresponds to *Ls,n* = *Ls,p* = *Ld* = 0.5nH, and *Mn,p* = *Mn,d* = *Mp,d* = 0.5nH.



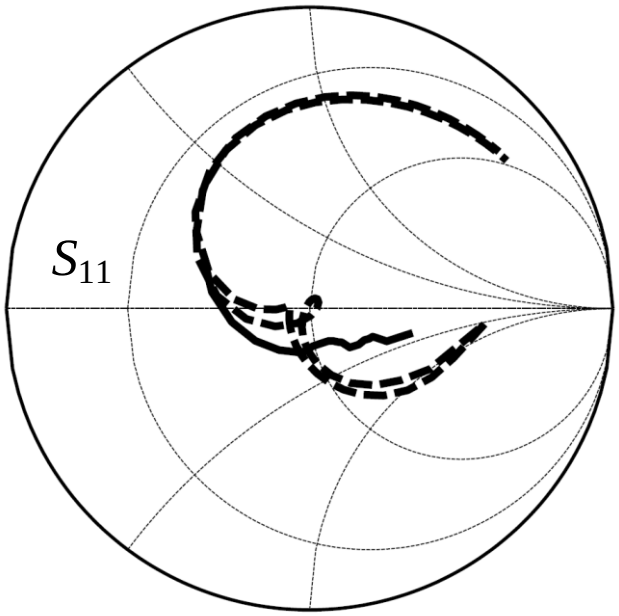
(a) (b)

Fig. 3-22. Measured and simulated *S*-parameters of the 2–10GHz wideband LNA. (a) Measured (solid-curve) and simulated (dashed-curve) S_{21} and S_{11}. (b) Measured and simulated S_{12} and S_{22}.

common-source transistor, V_{d3} = 1.5 V and I_{d3} = 7.1 mA for the third-stage and last-stage transistors. The total power consumption is 25.65 mW. Although the value of I_{d1} is smaller than that of I_{d2}, the gain first stage is still sufficient to lower the noise contribution from the following stage owing to its current re-use topology. Fig. 3-23(a) thus shows the simulated DC-10GHz output loading reflection coefficient for the first-stage transistor, which resemble that of the above-mentioned R_dC_d-circuit (R_d = 30Ω, C_d = 0.35pF). Fig. 3-23(b) shows the resulting simulated and measured input reflection coefficient, which resemble the familiar wideband shape. Fig. 3-24(a) shows the simulated (dashed curve) and the measured (solid curve) noise figure; Fig. 3-24(b) show the measured input-referred third-order intercepts point (IIP3) and the simulated gain of each stage of the amplifier, where curves 1-4 correspond to the gain of stages 1-4, respectively. Comparison with other LNA's is summarized in Table III, where figure of Merit (FOM) is defined as

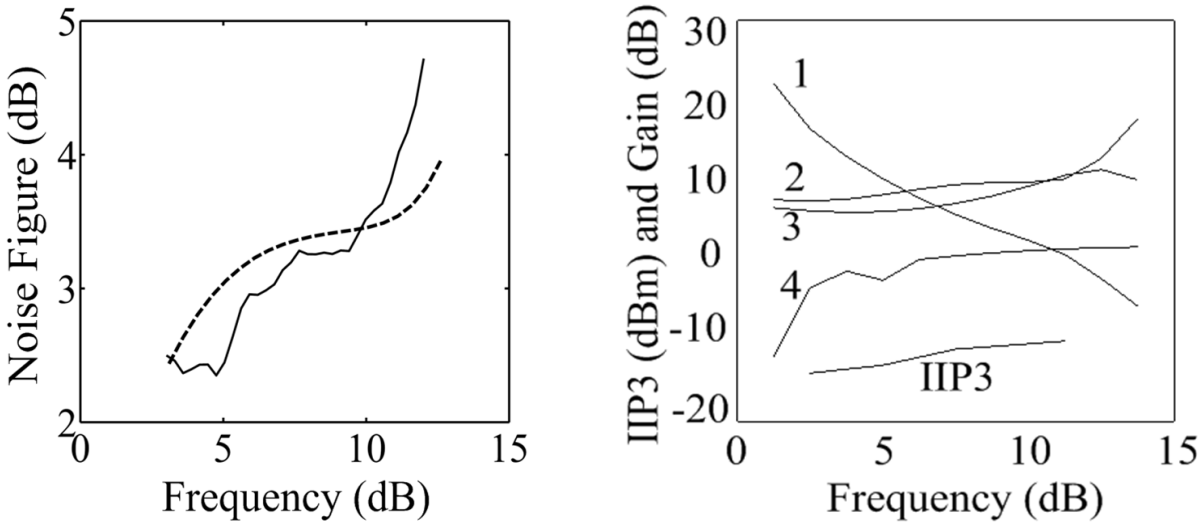


(a)



(b)

Fig. 3-23. (a) The solid line is the simulated output loading reflection coefficient trajectory for the first-stage transistors from DC-10GHz, while the dashed line is that of the R_dC_d series circuit, in which R_d = 30Ω, C_d = 0.35pF. (b) Measured (solid curve) and simulated (dashed curve) input reflection coefficients of the wideband LNA.



(a) (b)

Fig. 3-24. The noise figure, measured IIP3, and simulated gain of each stage of the 2–10GHz wideband LNA. (a) Simulated (dashed curve) and the measured (solid curve) noise figure. (b) Measured IIP3, and simulated gain of each stage, where curves 1-4 correspond to the gain of stages 1-4, respectively.

$$FOM = \frac{Gain_{mean}(dB) \cdot BW(GHz)}{[NF_{mean}(dB) - 1]P_{diss}(mW)} \tag{3-22}$$

In terms of gain, input reflection coefficient, and noise figure, our designed wideband amplifier outperforms other LNA's with similar or more advanced CMOS process [2]-[14].

3.5 Conclusion

In this chapter, the complementary topology is combined with asymmetrical inductive source degeneration to achieve broadband input matching while retaining low noise figure. The agreement between the simulated input impedance of the LNA and its calculated counterpart confirms the accuracy of our analysis as well as the noise figure is accurately analyzed and explained. A 2-10GHz wideband CMOS LNA is then designed and fabricated

using commercial RF-CMOS 0.18μm process. Compared with other CMOS LNA's in similar frequency range, our circuit demonstrates a better performance in gain, input matching, and noise figure.

TABLE I
PERFORMANCE COMPARISON OF LNA CIRCUITS PRESENTED IN PRIOR WORKS AND THE PROPOSED CIRCUIT

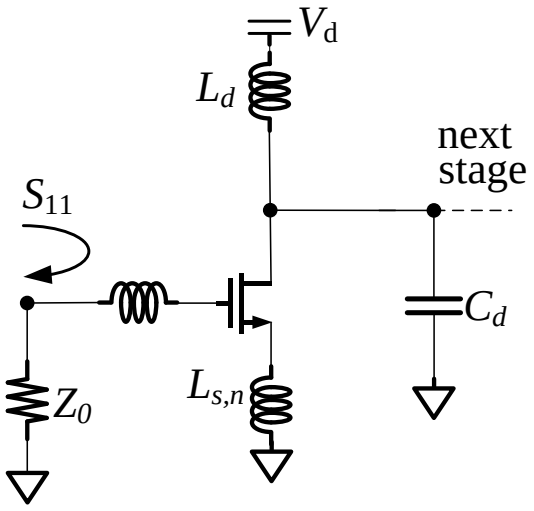
	BW (GHz)	S_{21} (dB)	S_{11} (dB)	NF (dB)	P_{diss} (mW)	Topology	Technology	FOM
[2] TMTT 2008	DC~13	6	<-12	2.7~5	22	Distributed	0.18μm CMOS	1.24
[3] JSSC 2007	1.2~11.9	6.7~9.7	<-11	4.5~5.1	20	Noise-Canceling	0.18μm CMOS	1.15
[4] MWCL 2007	2.7~9.1	10	<-10	3.8~6.9	7	Distributed	0.18μm CMOS	2.1
[5] MWCL 2010	3.1~10.6	13.2	<-9	4.5~6.2	23	Common Gate	0.18μm CMOS	0.99
[6] TCAS-I 2007	2.8~7.2	19.1	<-5	3~3.8	32	Network Synthesis	0.18μm CMOS	1.1
[7] MWCL 2009	3~10.35	9.5~12.5	<-8.3	3.3~11.4	7.2	Common Gate	0.13μm CMOS	3.63
[8] MWCL 2008	DC~11.5	12.2~14.2	<-8	5.6	9.1	Complementary	0.13μm CMOS	2.98
[9] JSSC 2009	1.5~8.1	8.6~11.7	<-9	3.6~6	2.62	Common Gate	0.13μm CMOS	6.7
[10] MWCL 2007	3.1~10.6	12~13	<-12	3.4~4	12.9	Common source	0.15μm pHEMT	2.69
[11] TCAS-II 2009	3.56~8.46	19~22.7	<-10.5	<6.5	34.8	Common Gate	90nm	0.53
[12] TMTT 2008	DC~9	10	<-10	4.2~8	20	Resistive Feedback	90nm	0.73
[13] JSSC 2008	0.2~5.2	13~15.6	<-10	2.9 ~3.5	14	Noise-Canceling	65nm	2.2
[14] RFIC 2006	3.1~10.6	10.8~12	<-11.2	4.7~5.6	10.57	Complementary	0.18μm CMOS	1.95
This work	**2-10**	**17-20**	**<-12**	**2.4~3.4**	**25.65**	**Complementary**	**0.18μm CMOS**	**3.04**

Chapter 4

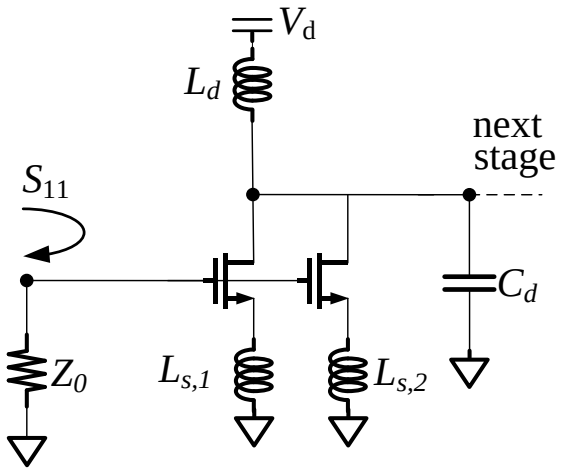
Future Work

In this thesis we successfully developed wideband solution for LNA design. As shown in Chapter 2 and Chapter 3, the good input matching and very promising low noise performance are obtained with reasonable power consumption. The device parasitic effects are all well utilized as part of design.

During the last four years, CMOS technology has emerged as a strong candidate for low-cost wireless ICs in the millimeter wave applications [30]–[39]. In this chapter, to demonstrate that the proposed technique will also has very promising performance in terms of noise figure and input matching reflection coefficient. Two transistor circuits, as shown in Fig. 4-1, are designed using TSMC RF-CMOS 90nm technology to justify the technique proposed in this thesis is also suitable in the millimeter wave applications: one is designed with a source inductive degeneration common-source amplifier with a gate inductor and the other is designed with the modified inductive degeneration common-source amplifier without the gate inductor. Fig. 4-2 (a) shows the simulated input reflection coefficients of the conventional amplifier (curve 1) and the amplifier using the proposed configuration (curve 2). Fig. 4-2 (b) shows the simulated noise figures of the conventional amplifier (curve 1) and the amplifier using the proposed configuration (curve 2). Clearly, the proposed configuration outperforms



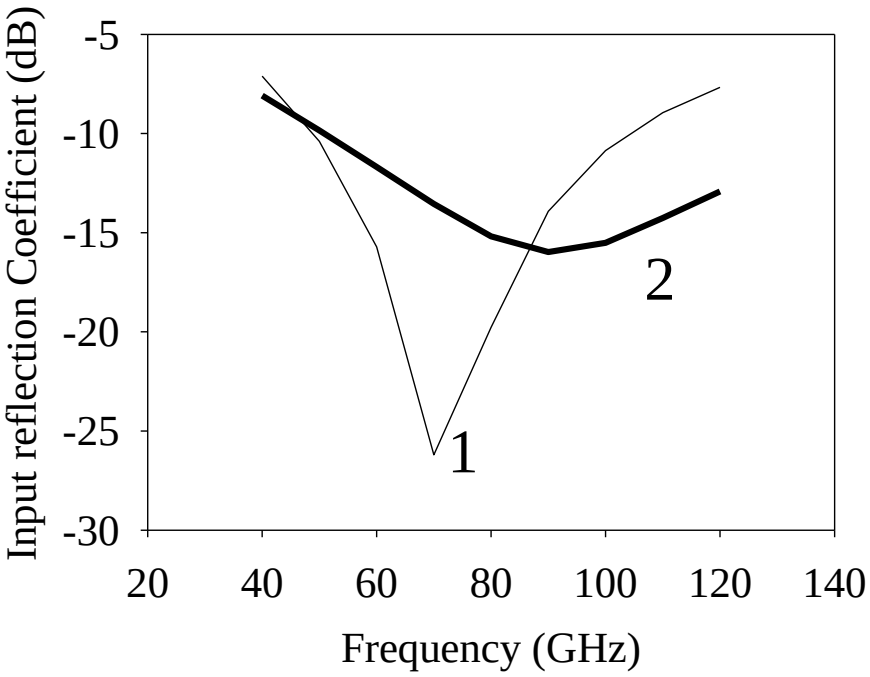
(a)



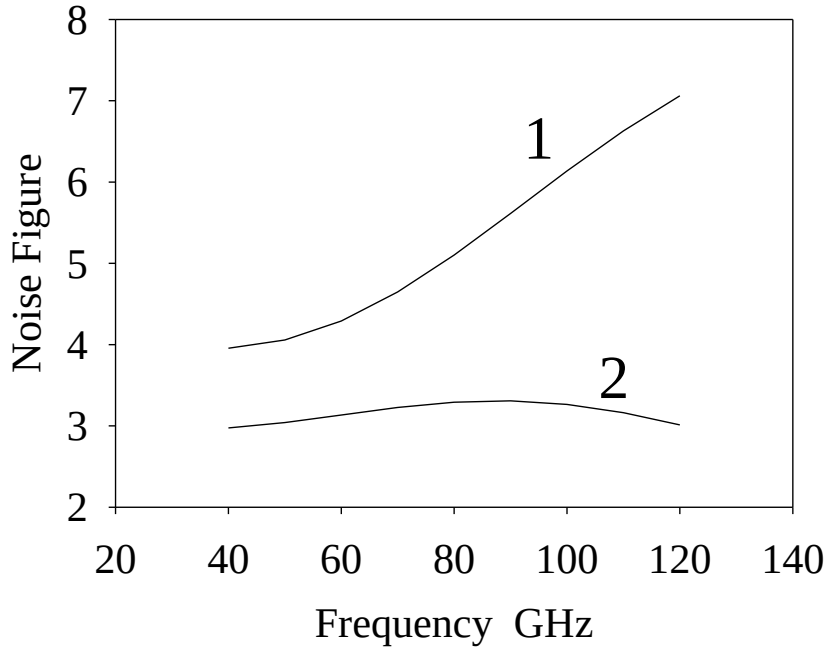
(b)

Fig. 4-1. (a) Conventional source inductively degenerated common-source amplifier, and (a) the proposed modified amplifier for millimeter wave application.

the conventional one. Thus the superior performance of low noise amplifier designed with CMOS technology can be expected. In the future, we expect more and more integration at transceiver front-end with the promising performance. Low-noise, and low-power characteristics of transceiver are always the clear and meaningful targets to pursue.



(a)



(b)

Fig. 4-2. (a) Conventional source inductively degenerated common-source amplifier, and (a) the proposed modified amplifier for millimeter wave application.

Appendix I

It appears that there is some confusion in the literature when it comes to the expression for the input equivalent circuits of the transistor circuit with *C-R-L* loading. We include the derivation in this Appendix to clarify the derivation.

Fig. 3-12(a) shows the transistor circuit with $C_dR_dL_d$ loading, where Z_α, $Z_{\beta,n}$, $Z_{\beta,p}$ are the impedance looking into C_{gd}, $C_{gs,n}$, and $C_{gs,p}$ branches, respectively. Employing the local series-series feedback theory, the local series-series feedback elements ($L_{s,n}$ and $L_{s,p}$) can be absorbed thus the transistor circuit can be transformed into that of Fig. 3-12(b), where $G_{m,n}$ and $G_{m,p}$ are the degenerated transconductances, $Z_{\beta,n}$ and $Z_{\beta,p}$ are the equivalent input impedance looking into $C_{gs,n}$ and $C_{gs,p}$ branches, respectively. $G_{m,n}$, $G_{m,p}$, $Z_{\beta,n}$, and $Z_{\beta,p}$ can be derived as

$$G_{m,n} = \frac{\dfrac{1/j\omega C_{gs,n}}{1/j\omega C_{gs,n} + j\omega L_{s,n}} g_{m,n} \dfrac{r_{ds,n}}{r_{ds,n} + j\omega L_{s,n} + Z_L}}{1 + \dfrac{1/j\omega C_{gs,n}}{1/j\omega C_{gs,n} + j\omega L_{s,n}} g_{m,n} \dfrac{r_{ds,n}}{r_{ds,n} + j\omega L_{s,n} + Z_L}}$$

$$\cong \frac{g_{m,n}}{1 + (j\omega)^2 L_{s,n} C_{gs,n} + g_{m,n} j\omega L_{s,n}} \qquad \text{(A-1)}$$

$$G_{m,p} \cong \frac{g_{m,p}}{1 + (j\omega)^2 L_{s,p} C_{gs,p} + g_{m,p} j\omega L_{s,p}} \qquad \text{(A-2)}$$

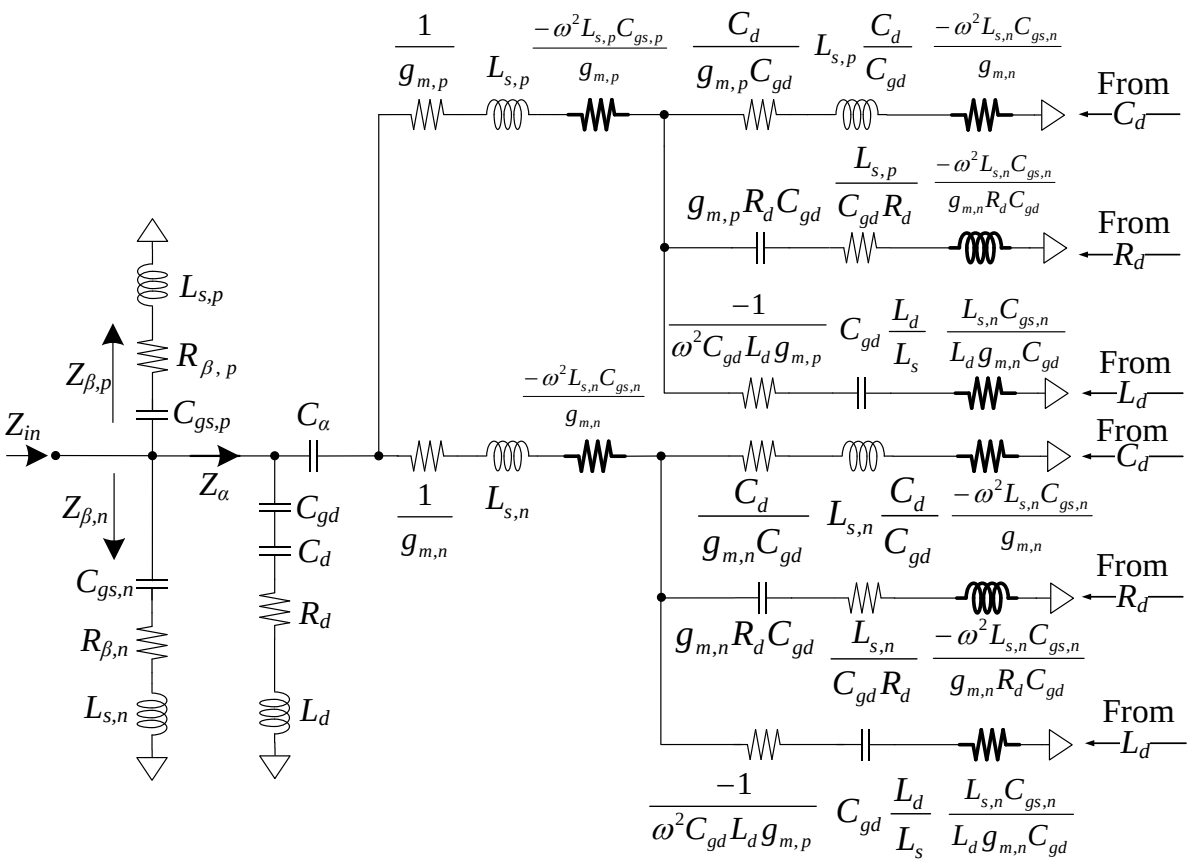


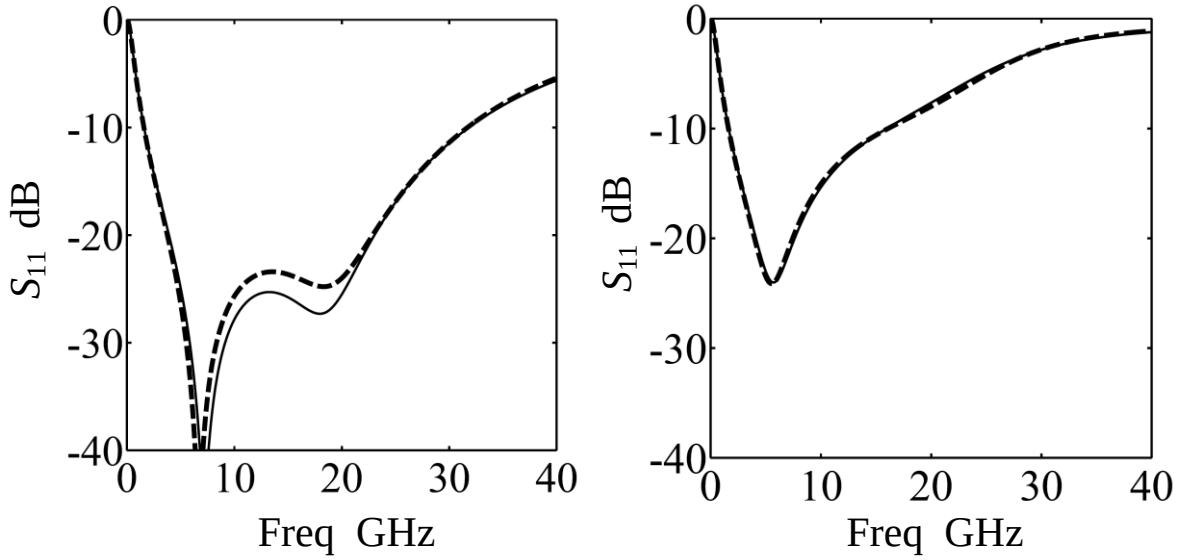
Fig. A-1 Complete equivalent input circuit of the $C_dR_dL_d$-loaded transistor circuit.

$$Z_{\beta,n} = \left(\frac{1}{j\omega C_{gs,n}} + j\omega L_{s,n}\right) \cdot \left(1 + \frac{1/\, j\omega C_{gs,n}}{1/\, j\omega C_{gs,n} + j\omega L_{s,n}}\, g_{m,n}\, \frac{r_{ds,n}}{r_{ds,n} + j\omega L_{s,n} + Z_L}\right)$$

$$\cong \left(\frac{1}{j\omega C_{gs,n}} + j\omega L_{s,n} + \frac{g_{m,n}L_{s,n}}{C_{gs,n}}\right) \tag{A-3}$$

$$Z_{\beta,p} \cong \left(\frac{1}{j\omega C_{gs,p}} + j\omega L_{s,p} + \frac{g_{m,n}L_{s,p}}{C_{gs,n}}\right) \tag{A-4}$$

In another aspect, $R_{ds,n}$ and $R_{ds,p}$ are the equivalent output impedance looking into the drain nodes of the n- and p-type transistors, respectively, which can be directly derived as



(a) (b)

Fig. A-2. Simulated input reflection coefficient. (a) Solid curve is the simulated input reflection coefficient with C_d = 0.2pF, $L_{s,n}$ = 0.8nH, $L_{s,p}$ = 0.4nH, while dashed curve is its calculated counterpart using the equivalent input circuit in Fig. 3-25. (b) Solid curve is the simulated input reflection coefficient with C_d = 0.2pF, R_d = 20Ω, L_d = 0.4nH, $L_{s,n}$ = 0.8nH, $L_{s,p}$ = 0.4nH, while dashed curve is its calculated counterpart using the equivalent input circuit in Fig. A-1.

$$R_{ds,n} \cong r_{ds,n} + [j\omega L_{s,n} // (R_g + \frac{1}{j\omega C_{gs,n}})] +$$

$$\frac{1/ j\omega C_{gs,n}}{1/ j\omega C_{gs,n} + j\omega L_{s,n}} g_{m,n} r_{ds,n} [j\omega L_{s,n} // (R_g + \frac{1}{j\omega C_{gs,n}})]$$

$$\cong r_{ds,n}[1 + (j\omega)^2 L_{s,n} C_{gs,n} + g_{m,n} j\omega L_{s,n}] \quad \text{(A-5)}$$

$$R_{ds,p} \cong r_{ds,p}[1 + (j\omega)^2 L_{s,p} C_{gs,p} + g_{m,p} j\omega L_{s,p}] \quad \text{(A-6)}$$

where R_g is the input generator 50Ω.With the knowledge of $G_{m,n}$ and $G_{m,n}$, $R_{ds,n}$, and $R_{ds,p}$, Z_α can be easily found out by the local shunt-shunt feedback theory as

$$Z_\alpha \cong \frac{\frac{1}{j\omega C_{gd}} + Z_L}{1 + G_m Z_L} \tag{A-7}$$

Finally, the input impedance can be derived as

$$Z_{in} = [\frac{1}{Z_\alpha} + \frac{1}{Z_{\beta,n}} + \frac{1}{Z_{\beta,p}}]^{-1} \tag{A-8}$$

Therefore, the complete equivalent circuit can be arranged as that of Fig. A-1.

In Fig. A-2(a), the solid curve is the simulated result with C_d = 0.2pF, $L_{s,n}$ = 0.8nH, $L_{s,p}$ = 0.4nH, the dashed curve is its calculated result using the complete equivalent circuit in Fig. A-1. In Fig. A-2(b), solid curve is the simulated result with C_d = 0.2pF, R_d = 20Ω, L_d = 0.4nH, $L_{s,n}$ = 0.8nH, $L_{s,p}$ = 0.4nH, dashed curve is the calculated result using the complete equivalent circuit in Fig. A-1. Obviously, the agreement between solid and dashed curve confirms the accuracy of our input matching theory. As the impedances of $C_{gs,n}$ and $C_{gs,p}$ are much larger than those of $L_{s,n}$ and $L_{s,p}$ in the derivations, $G_{m,n}$, $G_{m,p}$, $R_{ds,n}$, and $R_{ds,p}$ thus can be expressed as

$$G_{m,n} \cong \frac{g_{m,n}}{1 + g_{m,n} j\omega L_{s,n}} \tag{A-9}$$

$$G_{m,p} \cong \frac{g_{m,p}}{1 + g_{m,p} j\omega L_{s,p}} \tag{A-10}$$

$$R_{ds,n} \cong r_{ds,n}[1 + g_{m,n} j\omega L_{s,n}] \tag{A-11}$$

$$R_{ds,p} \cong r_{ds,p}[1 + g_{m,p} j\omega L_{s,p}] \tag{A-12}$$

which are the same as those in the text books. Therefore, the darkened components in Fig. A-1 are ignored and the resulting equivalent input circuit in Fig. 3-4(c) and Fig. 3-9(b) can be obtained.

Appendix II

It appears that there is some confusion in the literature when it comes to the expression for the noise factor of the proposed complementary low noise amplifier. We include the derivation in this Appendix to clarify the derivation.

Fig. A-3(a) shows the small-signal model of the proposed configuration, where $Z_{Cgs,n}$, $Z_{Cgs,p}$, $Z_{L,n}$, and $Z_{L,p}$ are the impedance of $C_{gs,n}$, $C_{gs,p}$, $L_{s,n}$, and $L_{s,p}$, respectively. $V_{Cgs,n}$, $V_{Cgs,p}$, $V_{L,n}$, and $V_{L,p}$ are the voltage drop across $C_{gs,n}$, $C_{gs,p}$, $L_{s,n}$, and $L_{s,p}$, respectively. $I_{R,n}$ and $I_{R,p}$ is the channel thermal noise. Applying KVL and KCL at nodes V_g, V_{Ln}, and V_{Lp}, we can obtain (A-14)-(A-16) as follows:

$$(g_{m,n}V_{Cgs,n} + I_{R,n}) + \frac{V_{Cgs,n}}{Z_{Cgs,n}} = \frac{V_{L,n}}{Z_{L,n}} \tag{A-14}$$

$$(g_{m,p}V_{Cgs,p} + I_{R,p}) + \frac{V_{Cgs,p}}{Z_{Cgs,p}} = \frac{V_{L,p}}{Z_{L,p}} \tag{A-15}$$

$$-\frac{V_g}{Z_g} = \frac{V_{Cgs,n}}{Z_{Cgs,n}} + \frac{V_{Cgs,p}}{Z_{Cgs,p}} \tag{A-16}$$

The voltage drops across the source inductors $L_{s,n}$ and $L_{s,p}$ can be derived as

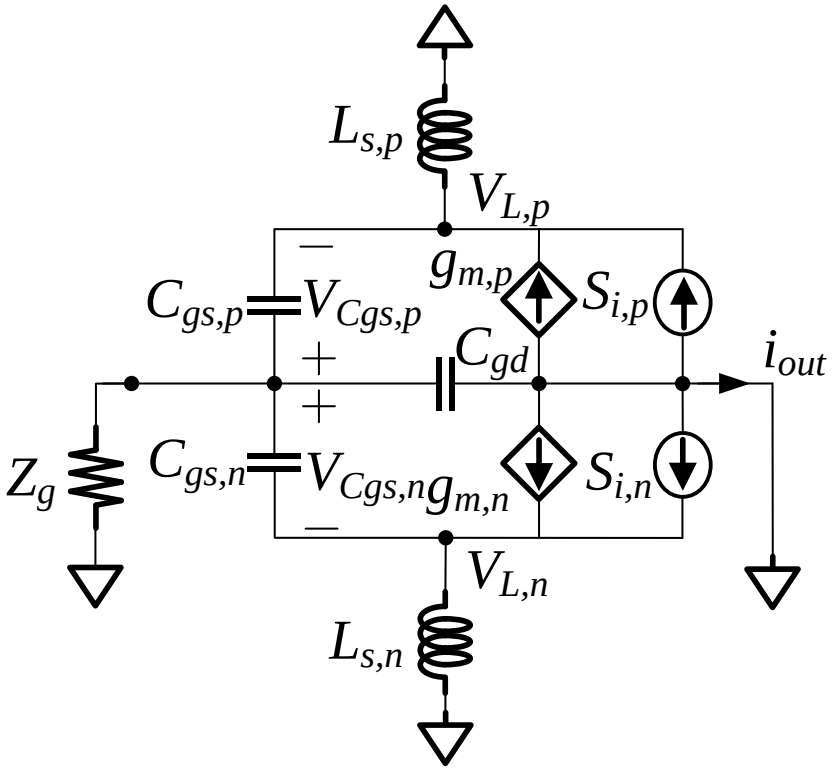


Fig. A-3 Schematic used to derive the noise temperature of the proposed complementary configuration.

$$V_{L,n} = -V_{Cgs,n}\left(\frac{Z_g}{Z_{Cgs,n}} + 1\right) - V_{Cgs,p}\left(\frac{Z_g}{Z_{Cgs,p}}\right) \tag{A-17}$$

$$V_{L,p} = -V_{Cgs,n}\left(\frac{Z_g}{Z_{Cgs,n}}\right) - V_{Cgs,p}\left(\frac{Z_g}{Z_{Cgs,p}} + 1\right) \tag{A-18}$$

Applying (A-17)-(A-18) into (A-14)-(A-15), the channel thermal noise of n- and p-type transistors can be derived as

$$I_{R,n} = V_{Cgs,n}\left(\frac{-Z_g}{Z_{Cgs,n}Z_{L,n}} - \frac{1}{Z_{L,n}} - g_{m,n} - \frac{1}{Z_{Cgs,n}}\right) + V_{Cgs,p}\left(\frac{-Z_g}{Z_{Cgs,p}Z_{L,n}}\right) \tag{A-19}$$

$$I_{R,p} = V_{Cgs,n}\left(\frac{-Z_g}{Z_{Cgs,n}Z_{L,p}}\right) + V_{Cgs,p}\left(\frac{-Z_g}{Z_{Cgs,p}Z_{L,p}} - \frac{1}{Z_{L,p}} - g_{m,p} - \frac{1}{Z_{Cgs,p}}\right) \quad \text{(A-20)}$$

Thus the voltage drops across $C_{gs,n}$ and $C_{gs,p}$ can be rearranged as

$$V_{Cgs,n} = \frac{\left(\frac{Z_g}{Z_{Cgs,p}Z_{L,p}} + \frac{1}{Z_{L,p}} + g_{m,p} + \frac{1}{Z_{Cgs,p}}\right)I_{R,n} - \left(\frac{Z_g}{Z_{Cgs,p}Z_{L,n}}\right)I_{R,p}}{\left(\frac{Z_g}{Z_{Cgs,p}Z_{L,n}}\right)\left(\frac{Z_g}{Z_{Cgs,n}Z_{L,p}}\right) - \left(\frac{Z_g + Z_{Cgs,n} + g_{m,n}Z_{Cgs,n}Z_{L,n} + Z_{L,n}}{Z_{Cgs,n}Z_{L,n}}\right)\left(\frac{Z_g + Z_{Cgs,p} + g_{m,p}Z_{Cgs,p}Z_{L,p} + Z_{L,p}}{Z_{Cgs,p}Z_{L,p}}\right)} \quad \text{(A-21)}$$

$$V_{Cgs,p} = \frac{\left(\frac{-Z_g}{Z_{Cgs,n}Z_{L,p}}\right)I_{R,n} + \left(\frac{Z_g}{Z_{Cgs,n}Z_{L,n}} + \frac{1}{Z_{L,n}} + g_{m,n} + \frac{1}{Z_{Cgs,n}}\right)I_{R,p}}{\left(\frac{Z_g}{Z_{Cgs,p}Z_{L,n}}\right)\left(\frac{Z_g}{Z_{Cgs,n}Z_{L,p}}\right) - \left(\frac{Z_g + Z_{Cgs,n} + g_{m,n}Z_{Cgs,n}Z_{L,n} + Z_{L,n}}{Z_{Cgs,n}Z_{L,n}}\right)\left(\frac{Z_g + Z_{Cgs,n} + g_{m,n}Z_{Cgs,n}Z_{L,n} + Z_{L,n}}{Z_{Cgs,n}Z_{L,n}}\right)} \quad \text{(A-22)}$$

To make the complicated expressions easy to understand, (A-21) and (A-22) are rearranged as

$$V_{Cgs,p} = \frac{\left(\frac{Z_g + Z_{c,p}}{Z_{Cgs,p}Z_{L,p}}\right)I_{R,n} + \left(\frac{-Z_g}{Z_{Cgs,p}Z_{L,n}}\right)I_{R,p}}{\frac{-\left(Z_{C,n} + Z_{C,p}\right)Z_g - Z_{C,n}Z_{C,p}}{Z_{Cgs,n}Z_{Cgs,p}Z_{L,n}Z_{L,p}}} \quad \text{(A-23)}$$

$$V_{Cgs,p} = \frac{\left(\frac{Z_g + Z_{c,n}}{Z_{Cgs,n}Z_{L,n}}\right)I_{R,p} + \left(\frac{-Z_g}{Z_{Cgs,n}Z_{L,p}}\right)I_{R,n}}{\frac{-\left(Z_{C,n} + Z_{C,p}\right)Z_g - Z_{C,n}Z_{C,p}}{Z_{Cgs,n}Z_{Cgs,p}Z_{L,n}Z_{L,p}}} \quad \text{(A-24)}$$

where

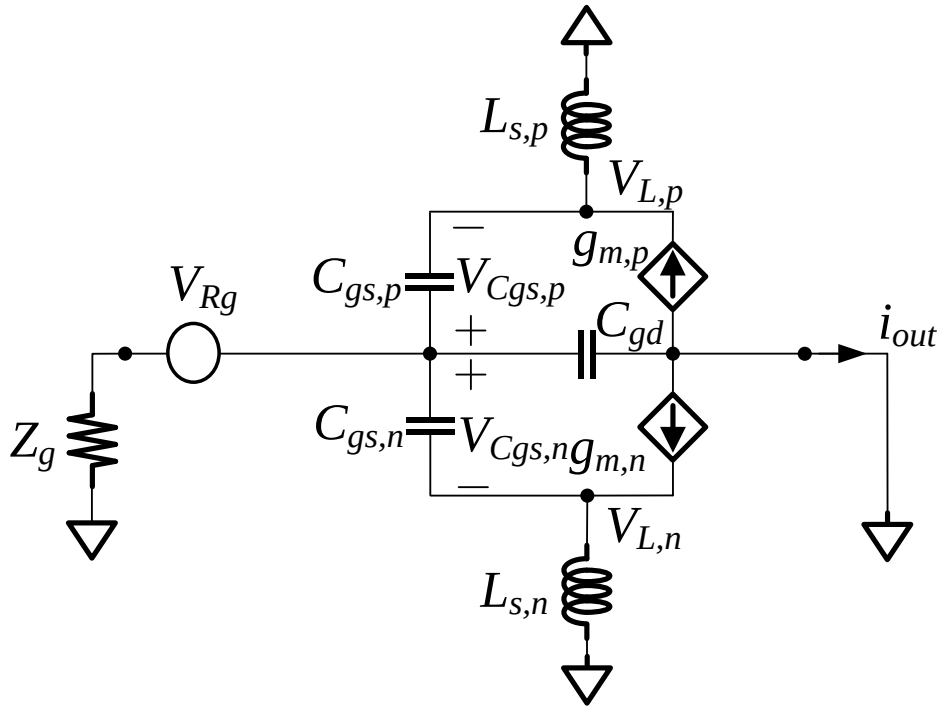


Fig. A-4 Schematic used to derive the noise temperature of the proposed complementary configuration.

$$Z_{c,n} = \frac{1}{j\omega C_{gs,n}} + j\omega L_{s,n} + \frac{g_{m,n} L_{s,n}}{C_{gs,n}}$$

$$Z_{c,p} = \frac{1}{j\omega C_{gs,p}} + j\omega L_{s,p} + \frac{g_{m,p} L_{s,p}}{C_{gs,p}}$$

$$G_{m,n} = g_{m,n} / \left(1 - \omega^2 C_{gs,n} L_{s,n} + j\omega L_{s,n} g_{m,n}\right)$$

$$G_{m,p} = g_{m,p} / \left(1 - \omega^2 C_{gs,n} L_{s,p} + j\omega L_{s,p} g_{m,p}\right) \quad (3\text{-}19)$$

To obtain the output noise, applying KCL at the drain node of the complementary configuration, the output noise current can be expressed as

$$|i_{out}| = |g_{m,n}V_{gs,n} + I_{R,n} + g_{m,p}V_{gs,p} + I_{R,p}|$$

$$= \left| \frac{Z_g + \frac{(Z_{Cgs,n} + Z_{L,n})Z_{C,p}}{Z_{C,n} + Z_{C,p}}}{Z_g + (Z_{C,n} // Z_{C,n})} I_{R,n} + \frac{Z_g + \frac{(Z_{Cgs,p} + Z_{L,p})Z_{C,n}}{Z_{C,n} + Z_{C,p}}}{Z_g + (Z_{C,n} // Z_{C,n})} I_{R,p} \right| \quad \text{(A-24)}$$

In another aspect, the

$$|i_{out}|^2 = |V_{Rg}|^2 \cdot \left| \frac{Z_{C,n} // Z_{C,n}}{Z_g + (Z_{C,n} // Z_{C,n})} \right|^2 \cdot |G_{m,n} + G_{m,p}|^2$$

$$= 4kT_nR_g \cdot \left| \frac{Z_{C,n} // Z_{C,n}}{Z_g + (Z_{C,n} // Z_{C,n})} \right|^2 \cdot |G_{m,n} + G_{m,p}|^2 \quad \text{(A-25)}$$

Equating (A-24) with (A-25), the noise temperature can be obtained as

$$T = \frac{|I_{R,n}|^2}{4kT_oZ_g} \left| \frac{\frac{Z_g}{Z_g j\omega C_{gd} + 1} + (\frac{1}{j\omega C_{gs,n}} + j\omega L_{s,n}) \frac{Z_{c,p}}{Z_{c,n} + Z'_{c,p}}}{(\frac{Z_{c,n}Z_{c,p}}{Z_{c,n} + Z_{c,p}})(G_{m,n} + G_{m,p})} \right|^2$$

$$+ \frac{|I_{R,p}|^2}{4kT_oZ_g} \left| \frac{\frac{Z_g}{Z_g j\omega C_{gd} + 1} + (\frac{1}{j\omega C_{gs,p}} + j\omega L_{s,p}) \frac{Z_{c,n}}{Z_{c,n} + Z'_{c,p}}}{(\frac{Z_{c,n}Z_{c,p}}{Z_{c,n} + Z_{c,p}})(G_{m,n} + G_{m,p})} \right|^2$$

Thus the noise factor can be transferred as that in (3-18).

Bibliography

[1] WPAN High Rate Alternative PHY Task Group 3a (TG3a), IEEE 802.15, 2007 [Online]. Available: http://www.ieee802.org/15/pub/ TG3a.html

[2] N. R. Erickson, R. M. Grosslein, R. B. Erickson, and S. Weinreb, "A cryogenic focal plane array for 85–115 GHz using MMIC preamplifiers," IEEE Trans. Microwave. Theory Tech. 47(12), 2212–2219 (1999), Dec.

[3] N. Wadefalk, et. al., "Cryogenic wide-band ultra-low noise IF amplifiers operating at ultra-low DC power," IEEE Trans. Microwave Theory Tech. 51(6), 1705–1711 (2003), Jun.

[4] X. Guan and C. Nguyen, "Low-power-consumption and high-gain CMOS distributed amplifiers using cascade of inductively coupled common-source gain cells for UWB systems," IEEE Trans. Microwave Theory Tech. 54(8), 3278–3283 (2006), Aug.

[5] P. Heydari, "Design and Analysis of a Performance-Optimized CMOS UWB Distributed LNA," IEEE J. Solid-State Circuits. 42(9), 1892–1904 (2007), Sept.

[6] L. Yang, K. S. Yeo, A. Cabuk, J. Ma, M. A. Do, and Z. Lu, "A novel CMOS low-noise amplifier design for 3.1-to 10.6-GHz ultra-wide-band wireless receivers," IEEE Trans. Circuits Syst. I. 53(8), 1683–1692 (2006), Aug.

[7] A. Ismail and A. Abidi, "A 3–10-GHz low-noise amplifier with wideband LC-ladder matching network," IEEE J. Solid-State Circuits, 39(12), 2269–2277 (2004), Dec.

[8] A. Bevilacqua, C. Sandner, A. Gerosa, and A. Neviani, “A fully integrated differential CMOS LNA for 3–5-GHz ultrawideband wireless receivers,” IEEE Microwave Wireless Compon. Lett. 16(3), 134–136 (2006), Mar.

[9] Y.-J. E. Chen and Y.-I. Huang, “Development of Integrated Broad-Band CMOS Low-Noise Amplifiers,” IEEE Trans. Circuits Syst. I. 54(10), 2120-2127 (2007), Oct.

[10] C.-T. Fu, and C.-N. Kuo, “3~11-GHz CMOS UWB LNA using dual feedback for broadband matching,” in IEEE Radio Frequency Integrated Circuits Symp. Dig., San Francisco, California, pp. 67-70, 2006.

[11] C.-T. Fu, C.-L. Ko, C.-N Kuo, and Y.-Z. Juang, “A 2.4-5.4-GHz Wide Tuning-Range CMOS Reconfigurable Low-Noise Amplifier,” IEEE Trans. Microwave Theory Tech. 56(12), 2754–2763 (2008), Dec.

[12] R. Hu, “Wide-band matched LNA design using transistor's intrinsic gate-drain capacitor,” IEEE Trans. Microwave Theory Tech., 54(3), 1277–1286 (2006), Mar.

[13] C. -W. Kim, M. –S. Jung, and S. -G. Lee, “Ultra-wideband CMOS low noise amplifier,” *Electron. Lett.*, vol. 41, no. 7, pp. 384-385, Mar. 2005.

[14] M. K. Chirala, X. Guan and C. Nguyen, “Integrated Multilayered On-Chip Inductors for Compact CMOS RFICs and Their Use in a Miniature Distributed Low-Noise-Amplifier Design for Ultra-Wideband Applications,” *IEEE Trans. Microwave Theory Tech.*, vol. 56, no. 8, pp. 1783–1789, Aug. 2008.

[15] C. F. Liao and S. I. Liu, “A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receiver,” *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, Feb. 2007.

[16] Y.-H. Yu, Y.-J. E. Chen, and D. Heo “A 0.6-V Low Power UWB CMOS LNA,” *IEEE Microw.Wireless Compon. Lett.*, vol. 17, no. 3, pp. 229–231, Mar. 2007.

[17] B. Park, S. Choi, and S. Hong “A Low-Noise Amplifier With Tunable Interference Rejection for 3.1-to 10.6-GHz UWB Systems,” *IEEE Microw.Wireless Compon. Lett.*, vol. 20, no. 1, pp. 40–42, Jan. 2010.

[18] Y.-J. E. Chen, and Y.-I. Huang, "Development of integrated broad-band CMOS low-noise amplifier," *IEEE Train. Circuits Syst. I. Reg. Papers,* vol. 54, no. 10, pp. 2120–2127, Oct. 2007. [4]

[19] C.-Y. Wu, Y.-K. Lo, and M.-C. Chen, "A 3–10 GHz CMOS UWB Low-Noise Amplifier With ESD Protection Circuits," *IEEE Microw.Wireless Compon. Lett.*, vol. 19, no. 11, pp. 737–739, Nov. 2009.

[20] S.-F. Chao, J.-J. Kuo, C.-L Lin, M.-D. Tsai, and H. Wang, "A DC-11.5 GHz Low-Power, Wideband Amplifier Using Splitting-Load Inductive Peaking Technique," *IEEE Microw.Wireless Compon. Lett.*, vol. 18, no. 7, pp. 482–484, Jul. 2008.

[21] H. Zhang, X. Fan and E. S. Sinencio, "A Low-Power Linearized Ultra-Wideband LNA Design Technique," *IEEE J. Solid-State Circuits,* vol. 44, no. 2, pp. 320–330, Feb. 2009.[5]

[22] C. Fang, C. L. Law, and J. Hwang, "A 3.1–10.6 GHz Ultra-Wideband Low Noise Amplifier With 13-dB Gain, 3.4-dB Noise Figure, and Consumes Only 12.9 mW of DC Power," *IEEE Microw.Wireless Compon. Lett.*, vol. 17, no. 4, pp. 295–297, Apr. 2007.

[23] D. Pepe, and D. Zito, "22.7-dB Gain –19.7-dBm ICP_{1dB} UWB CMOS LNA," *IEEE Train. Circuits Syst. II. Express. Briefs,* vol. 56, no. 9, pp. 689–693, Sep. 2009.[7]

[24] T. Chang, J. Chen, L. A. Rigge, and J. Lin, "ESD-Proteced Wideband CMOS LNAs Using Modified Resistive Feedback Techniques With Chip-on-Board Packaging," *IEEE Trans. Microwave Theory Tech.*, vol. 56, no. 8, pp. 1817–1826, Aug. 2008.[8]

[25] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.[9]

[26] C.-T. Fu, and C.-N. Kuo, "3~11-GHz CMOS UWB LNA using dual feedback for broadband matching," in *IEEE Radio Freq. Integr. Circuits Symp. Dig.*, Jun. 2006, pp. 67-70.

[27] S.-C. Wand, P. Su, K.-M. Chen, K.-H. Liao, B.-Y. Chen, S.-Y. Huang, C.-C. Hung, and G.-W. Huang, "Comprehensive Noise Characterization and modeling for 65-nm MOSFETs for

Millimeter-Wave Applications," *IEEE Trans. Microwave Theory Tech.*, vol. 58, no. 4, pp. 740–746, Apr. 2010.

[28] S. Asgaran, M. J. Deen, C.-H. Chen, G. A. Rezvani, Y. Kamali, and Y. Kiyota, "Analytical Determination of MOSFET's High-Frequency Noise Parameters From NF_{50} Measurements and Its Application in RFIC Design," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1034–1043, May. 2007.

[29] H.-I. Wu, R. Hu, and C. F. Jou, "Complementary UWB LNA Design Using Asymmetrical Inductive Source Degeneration," *IEEE Microw.Wireless Compon. Lett.*, vol. 20, no. 7, pp. 402–404, Jul. 2010.

[30] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Design of CMOS for 60 GHz applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2004, vol. 1, pp. 440–538.

[31] B. Razavi, "A 60-GHz CMOS receiver front-end," *IEEE J. of Solid-State Circuits*, vol. 41, no. 1, pp. 17–23, Jan. 2006.

[32] T. Yao, M. Gordon, K. Yau, M. T. Yang, and S. P.Voinigescu, "60-GHz PA and LNA in 90-nm RF-CMOS," in *IEEE RFIC Symp. Dig.*, Jun. 2006, pp. 147–150.

[33] D. Alldred, B. Cousins, and S. P. Voinigescu, "A 1.2 V, 60 GHz radio receiver with on-chip transformers and inductors in 90 nm CMOS," in *Proc. IEEE CSICS*, Nov. 2006, pp. 51–54.

[34] C.-H. Wang, H.-Y. Chang, P.-S. Wu, K.-Y. Lin, T.-W. Huang, H. Wang, and C.-H. Chen, "A 60 GHz low-power six-port transceiver for gigabit software-defined transceiver applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 192–193.

[35] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Brodersen, "A highly integrated 60 GHz CMOS front-end receiver," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 190–191.

[36] B. Razavi, "A mm-wave CMOS hetrodyne receiver with on-chip LO and divider," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 188–189.

[37] J. M. Gilbert, C. H. Doan, S. Emami, and C. B. Shung, "A 4-Gbps uncompressed

wireless HD A/V transceiver chipset," *IEEE Micro*, vol. 28, pp. 56–64, 2008.

[38] S. T. Nicolson and S. P. Voinigescu, "Methodology for simultaneous noise and impedance matching in W-band LNAs," in *Proc. IEEE CSICS*, Nov. 2006, pp. 279–282.

[39] B. Heydari, M. Bohsali, E. Adabi, and A. M. Niknejad, "Low-power mm-wave components up to 104 GHz in 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 200–201.

[40] A. Liscidini, M. Brandolini, D. Sanzogni, and R. Castello, "A 0.13 um CMOS front-end for DCS1800/UMTS/802.11b-g with multi-band positive feedback LNA," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 981–988, Apr. 2006.

[41] P. Rossi, A. Liscidini, M. Brandolini, and F. Svelto, "A variable gain RF front-end, based on a voltage-voltage feedback LNA, for multistandard applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 368–374, Feb. 2004.

[42] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. P. de Gyvez, D. J. Allstot, and E. Sánchez-Sinencio, "A capacitor cross-coupled commongate low-noise amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 12, pp. 875–879, Dec. 2005.

[43] X. Guan and A. Hajimiri, "A 24 GHz CMOS front-end," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 368–374, Feb. 2004.

[44] S.Woo, W. Kim, C. Lee, K. Lim, and J. Laskar, "A 3.6mW differential common-gate CMOS LNA with positive-negative feedback," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2009, pp. 218–219.

[45] D. G. Im, S. S. Song, H. T. Kim, and K. Lee, "A wide-band CMOS variable-gain low noise amplifier for multi-standard terrestrial and cable TV tuner," in *IEEE Radio Freq. Integrated Circuits Symp. Dig.*, Honolulu, HI, Jun. 2007, pp. 621–624.

[46] J.-H. C. Zhan and S. S. Taylor, "A 5 GHz resistive-feedback CMOS LNA for low-cost multi-standard applications," in *IEEE ISSCC Dig.Tech. Papers*, 2006, pp. 200–201.

[47] A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS low noise amplifier for

3.1–10.6-GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.

[48] F. Lee and A. Chandrakasan, "A BiCMOS ultra-wideband 3.1–10.6-GHz front-end," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1784–1790, Aug. 2006.

[49] Y. Lu, R. Krithivasan, W.-M. L. Kuo, and J. D. Cressler, "A 1.8–3.1 dB noise figure (3–10 GHz) SiGe HBT LNA for UWB applications," in *Proc. IEEE RFIC Symp.*, San Francisco, CA, 2006, pp. 59–62.

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Publication List

(a) Journal Papers

(1) **H.-I. Wu**, R. Hu, and C. F. Jou, "**Complementary UWB LNA Design Using Asymmetrical Inductive Source Degeneration**," *IEEE Microw.Wireless Compon. Lett.*, vol. 20, no. 7, pp. 402–404, Jul. 2010.

(2) **H.-I. Wu**, Q.-Y. Horng, R. Hu, and C. F. Jou, "Analysis and Design of **Complementary UWB LNA Design Using Asymmetrical Inductive Source Degeneration**," accepted by *Journal of Infrared, Millimeter, and Terahertz waves*.

(3) **H.-I. Wu**, Z.-Z. Wong, and C. F. Jou, "Analysis and Design of **Complementary UWB LNA Design Using Asymmetrical Inductive Source Degeneration**," accepted by *IEICE Trans.*

(4) L.-S. Wei, **H.-I. Wu**, and C. F. Jou, "Design of low voltage CMOS low-noise amplifier with image-rejection function," *Electronics Letters , Vol. 44, No. 16, 31st July 2008*

(5) **H.-I. Wu**, R. Hu, and C. F. Jou, "Analysis and Design of **Complementary UWB LNA Design Using Asymmetrical Inductive Source Degeneration**," submitted to *IEEE Trans. Microwave Theory Tech.*