國 立 交 通 大 學

電信工程研究所

博 士 論 文

應用於多頻段與超寬頻通訊之射頻接收
電路設計與分析

Design and Analysis of RF Receiver Circuits
for Multiband and Ultra-Wideband
Communication Applications

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摘要

本篇論文提出了數種適用於多頻段與超寬頻通訊系統的 0.18 微米互補式金氧半製程射頻積體電路元件之架構、分析與設計。其中包含了 (1) 兩個使用諧振切換與雜訊消除電路的多頻帶低雜訊放大器；(2) 具鏡像頻率抑制混頻器的設計；(3) 三個低功率超寬頻低雜訊放大器的分析與設計；(4) 採用降低相位雜訊技術的壓控振盪器電路。

多頻帶低雜訊放大器藉由切換的概念來實現多頻帶操作，其能有效地減少系統面積來降低製作的成本，並且於第二個多頻帶低雜訊放大器設計中，利用回授式雜訊相消電路能同時達到輸入匹配以及改善雜訊指數的效果。另外在所設計電路的主動元件中額外引入一阻值較大的基極電阻，以避免雜訊從電晶體的基極端交互流竄而惡化電路本身的雜訊指數特性。在不額外增加晶片面積、製程步驟、以及直流功率損耗的前提之下，採用此雜訊降低電阻於 2.5 GHz 操作頻帶時，能達到 32%的雜訊指數改善效果，可廣泛地應用在現今低雜訊放大器的設計。

其次，本論文提出了一個具鏡像頻率抑制的吉伯特降頻混頻器。相對於傳統的 Hartley 或 Weaver 鏡像頻率抑制電路架構，此混頻器能大幅地降低直流功率損耗與電路設計的複雜度。並且搭配一負阻抗產生主動電路，藉由合適的負阻抗來消除濾波器的正電阻以提升其品質因數 Q，進而增進鏡像訊號抑制的效果。此混

頻器於 2.4/5.2 GHz 使用頻段的量測結果如下：轉換增益 (conversion gain) 為 10.5/11 dB、一階與三階交叉點的輸入功率 (IIP_3) 為 4.9/-5.2 dBm、單邊雜訊指數 (SSB NF) 為 10/13 dB、鏡像頻率抑制效果可達 36/45 dB。

再其次，由於超寬頻系統的訊號強度遠低於 IEEE 802.11 a/b/g 以及 1.8 GHz DCS/ GSM 系統，因此首先我們在第一個超寬頻低雜訊放大器中提出具頻帶外訊號抑制能力的輸入匹配網路去壓制其他系統所造成的干擾。另外我們在第二個低雜訊放大器電路中，藉由使用一個回授結構以及雙頻帶主動式低功率帶拒濾波電路進一步地提升抑制干擾訊號的效果。經改良所設計出的低雜訊放大器在 1.8/2.4/5.2 GHz 能夠達到最大抑制效果為 55/48/45 dB。另一方面，由於減少輸入端損耗元件的使用能有效地改善電路的雜訊指數，在此引入了電晶體的寄生電容來達到超寬頻輸入匹配特性，當輸入回返損耗 (input return loss) 大於 10 dB 以上時，其頻帶內最大增益為 16.2 dB，最小雜訊指數為 2.3 dB，且總直流功率損耗僅為 6.8 mW。

最後提出的是具降低相位雜訊參數之壓控振盪器電路，藉由最佳化被動元件尺寸以及額外設計的二次諧波抑制電容與基極偏壓，整體電路性能參數 FOM (figure of merit) 能達到-190 dBc/Hz。此壓控振盪器晶片所使用的面積為 0.15 微米平方，且由實驗的結果分析得知，總功率耗損僅為 1.9 mW，而在 1 MHz offset 時其相位雜訊約為-119 dBc/Hz。

Design and Analysis of RF Receiver Circuits for Multiband and Ultra-Wideband Communication Applications

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ABSTRACT

In this dissertation, the design methodologies and implementations of RF receiver circuits for multiband and ultra-wideband communication applications are proposed. There are four parts in this thesis, including: (1) the design of two triple-band low-noise amplifiers (LNAs) using switched resonators and a noise cancelation technique, (2) the design of dual-band image rejection mixer, (3) the analysis and design of three low-power UWB LNAs, and (4) the design of voltage-controlled oscillator (VCO) with phase-noise improvement.

First of all, the design of two triple-band LNAs with switched resonators is presented and fabricated in the TSMC 0.18-μm CMOS process. The proposed triple-band LNAs are demonstrated the feasibility to effectively decrease the size of multi-band RF systems by using a switched component. In addition, a considerable noise power diminution in MOS devices with an additional larger substrate resistor is presented in the second approach of the triple-band LNA. A 32% noise reduction of

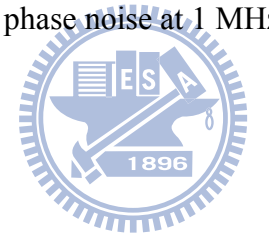
MOS devices can be achieved at 2.5 GHz without extra chip area, CMOS process steps and dc power. This noise reduction technique in MOS device is very promising in the nowadays LNA designs.

Secondly, this thesis presents a 2.45/5.2 GHz dual-band Gilbert downconversion mixer with image rejection function is presented, which is implemented in the 0.18-μm CMOS technology. The proposed differential dual-band image rejection circuitry is employed for the 2.45/5.2 GHz WLAN application to effectively diminish the dc power consumption and complexity of circuit design compared to the traditional Hartley or Weaver architectures. Moreover, the cross-connected pair consisted of NMOS and PMOS transistors in the proposed notch filter will further ameliorate the image rejection capability. The IC prototype attains conversion gain of 10.5/11 dB, IIP3 of -4.9/-5.2 dBm for RF= 2.45/5.2 GHz and IF=500 MHz while the image rejection ratio is better than 36/45 dB in the whole operation bandwidth.

Thirdly, three low-power UWB LNAs using 0.18-μm CMOS technology are presented. Due to the FCC's stringent power-emission limitation at the transmitter, the received signal power in the UWB system is smaller than those of the close narrow-band interferers such as the IEEE 802.11 a/b/g WLAN, and the 1.8 GHz DCS/ GSM. Therefore, we proposed a wideband input network with out-band rejection capability to suppress the out-band interference for our first UWB LNA. Moreover, a feedback structure and dual-band notch filter with low power active inductors will further attenuate the outband interferers without deteriorating the input matching bandwidth in the second UWB LNA. The 55/48/45 dB maximum rejections at 1.8/2.4/5.2 GHz, 15 dB power gain, and 3.5 dB minimum noise figure can be measured while consuming dc power of only 5 mW. On the other hand, to further improve the noise figure performance of the above out-band rejection LNAs, a new matching technique is presented in the third UWB LNA. The proposed broad-band

input match network can be obtained easily by selecting an appropriate width of the transistor, which could effectively avoid the usage of the low-Q on-chip inductors in the input network. The IC prototype achieves good performances: 16.2 dB maximum power gain, better than 10 dB input return loss, and 2.3 dB minimum noise figure while consuming dc power of only 6.8 mW.

Finally, a low-power 5.25 GHz VCO with phase-noise improvement is designed in a 0.18-μm CMOS 1P6M process. Due to the usage of a larger value of parallel capacitor, an additional harmonic-suppressed capacitor, and an appropriate bulk bias voltage of the transistor, a good figure of merit (FOM) of -190 dBc/Hz can be achieved without extra chip area and CMOS process steps. The fabricated VCO operates from 5.12 to 5.36 GHz with a power consumption of 1.9 mW and active chip area of 0.15 mm^2. The measured phase noise at 1 MHz offset is about -119 dBc/Hz.



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梁清標 于新竹交大

2010年4月

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TABLE CAPTIONS

FIGURE CAPTIONS

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

The wireless communication is becoming more and more significant because of the convenience for human-being life and accelerating the transmission of the information in the last two decades. For the landscape of the wireless communication systems, the higher bandwidth of these radio bands, such as wireless local area network (WLAN), worldwide interoperability for microwave access, and ultra-wideband (UWB) significantly enables the higher data rate applications.

The IEEE 802.11 group which is also labeled as WiFi (Wireless Fidelity) establishes three sub-standards on the market, namely 802.11a operating at frequencies allocated around 5 GHz, and 802.11 b and g transmitting at 2.4 GHz. The b standard achieves a date throughput of around 11 Mb/s, and the more advanced a and g standards can support up to 54 Mb/s data rate by utilizing the orthogonal frequency-division multiplexing (OFDM) technique.

Worldwide interoperability for microwave access (WiMAX), described and specified in the IEEE 802.16e standard, is a new system for wireless broadband access to provide the high speed of service and broad coverage of about several miles. Due to the usage of the OFDM technique and the multiple-input, multiple-output (MIMO) concept, the data rate up to 75 Mb/s can be achieved at the operation frequencies 2.5, 3.5, and 5.2 GHz.

For the IEEE 802.15.3a group, the multi-band orthogonal frequency division multiplexing (MB-OFDM) UWB system uses the unlicensed UWB spectrum from 3.1

GHz to 10.6 GHz with a regulated frequency-power emission below –41.3 dBm to provide data communication capabilities up to 480 Mbps. The 7.5 GHz bandwidth is divided into 4 groups of 14 bands. Therefore, the occupied spectrum for each OFDM signal is 528 MHz.

In this thesis, the main research focus is on key components for multiband and UWB communication systems. It includes triple-band low-noise amplifiers (LNAs), a dual-band image rejection mixer, low-power UWB LNAs with out-band rejection properties, and a low phase-noise voltage-controlled oscillator (VCO). The research motivation will be depicted in the following subsection.

1.2 RESEARCH MOTIVATION

Recently, the wireless communication systems has rapidly expanded the demand for low-cost and low-power RF integrated circuits (RFICs) which can support multi-system operations. There is the trend to merge several applications into one device by reusing potential synergies between the different systems, as shown in Fig. 1.1. The study on exploring new different circuit topologies and design techniques of the key RFIC components in multi-band and UWB communication systems is proposed.

For the multi-band communication system, conventional design strategies have adopted different single-band receiver circuits in parallel for different frequency bands. However, it is unavoidable to result in a high implementation cost because of the large chip area and an increased chip current dissipation simultaneously. In order to avoid the above-mentioned drawbacks, a multi-band receiver has demonstrated the feasibility to take the place of the conventional structure for multi-band

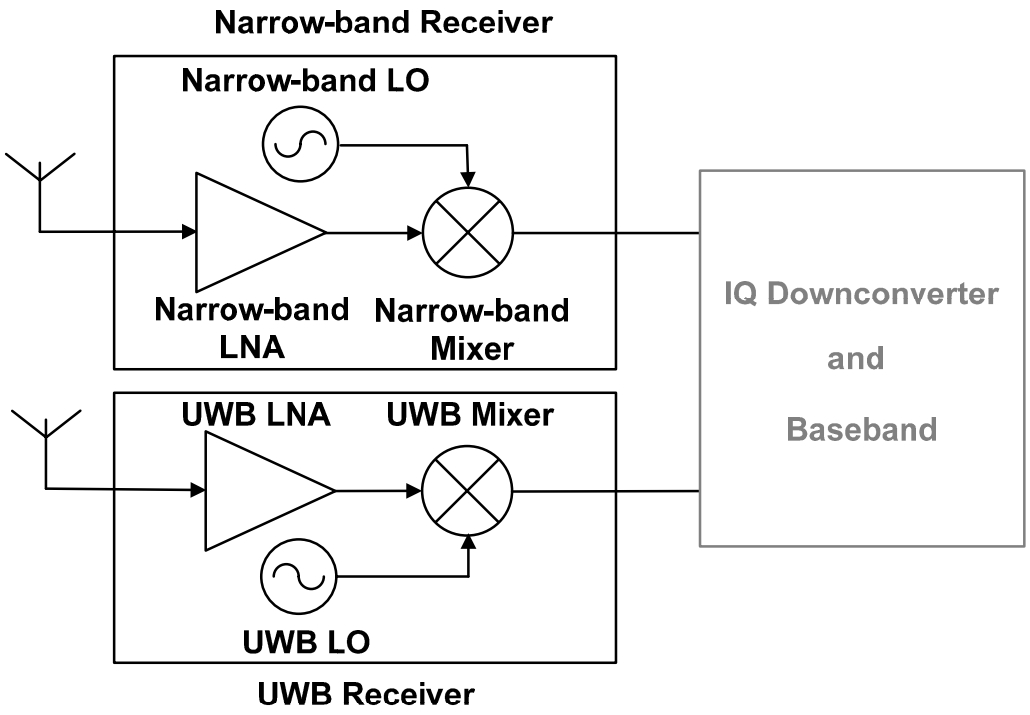


Fig. 1.1 Several different applications merged into a system.

application. In addition, the noise figure of a receiver is particularly determined by the noise figure of the LNA located in front of the receiver. Therefore, the proposed noise-canceling technique can be applied in the LNA circuit to ameliorate the noise property.

Mixer is responsible for frequency conversion in RF transceiver, and the suppression of the image signal is an essential requisite. Generally, the multi-band image rejection mixer can be achieved by either Hartley or Weaver architecture, but the required multi-band quadrature signal generator will further increase the complication of the circuit implementation, which is undesired for low-cost and low-power application. In order to achieve smaller chip area and dc power consumption, the differential third-order notch filter with the cross-connected pair consisted of NMOS and PMOS transistors is designed.

On the other hand, the minimum received power in the UWB system is 47 and

67 dB, in the worst case, lower than those of the WLAN interferer powers at 5.2 and 2.4 GHz, respectively. In addition, one tone is measured at 1.87 GHz in a smart-phone currently on the market, and the power level is 35 dB higher than the UWB signal. All of these interferers have a harmful effect on the received UWB signal; therefore, the designed LNA with out-band rejection property in UWB communication system is required.

For multiband or UWB communication applications, the RF signal is downconverted to the IF frequency using a local oscillator, which is generated by a frequency synthesizer. Phase noise is one of the most critical parameters for a local oscillator since it affects the overall performance of the communication system. Therefore, the designed low-noise VCO, which is a key component of the frequency synthesizer is proposed to optimize the phase-noise performance.

The aim of this dissertation is to develop key components for multiband and UWB communication systems including two triple-band LNAs, a dual-band image rejection mixer, three low-power UWB LNAs, and a low phase-noise VCO. The main results will be depicted below.

1.3 THESIS ORGANIZATION

It is the aim of this thesis to analyze and design RF receiver circuits for multiband and UWB communication applications. The thesis includes the design of two triple-band LNAs, a dual-band image rejection mixer, three low-power UWB LNAs, and a VCO with the phase-noise improvement.

Chapter 1 introduces the background, and describes the research motivation.

Chapter 2 presents the design of two triple-band LNAs fabricated in a 0.18-μm

complementary metal oxide semiconductor (CMOS) process. The proposed triple-band LNAs have demonstrated the feasibility to effectively decrease the size of multi-band RF systems by using a switched component. Furthermore, the feedback structure is adopted to accomplish the partial noise cancelation and the wideband input matching simultaneously. The proposed noise power diminution by using an additional larger substrate resistor in MOS device can be employed in the nowadays LNA designs.

A 2.45/5.2 GHz Gilbert downconversion mixer with image rejection function is proposed and detailed in chapter 3. The mixer employs the differential, dual-band, third-order notch filter to attenuate the dual-band image signal while maintaining a superior in-band performance. The cross-connected pair consisted of NMOS and PMOS transistors in the proposed notch filter will further raise the Q value of on-chip inductor for improving the image rejection capability.

In chapter 4, three low-power UWB LNAs using 0.18-μm CMOS technology are presented. By suitably introducing two additional capacitors in the traditional LC input network, two transmission zeros are generated to achieve the out-band rejection function. Moreover, a feedback structure and dual-band notch filter with low power active inductors further attenuate the out-band interferers without deteriorating the input matching bandwidth. After improving the out-band rejection capability, a new matching technique can be acquired easily by selecting an appropriate width of the transistor, which will effectively avoid the usage of the low-Q on-chip inductors in the input network for ameliorating the noise figure performance.

In chapter 5, a low-power VCO with phase-noise improvement in 0.18-μm CMOS technology is presented. The VCO adopts the design of a current-reused configuration because of its excellent low-power characteristic, and focuses on the promotion of phase noise without additional chip area and CMOS process steps. A 15

dB improvement at 10 kHz offset frequency can be attained due to the usage of a larger parallel capacitor, an extra harmonic-rejected capacitor, and an appropriate bulk bias voltage of transistor.

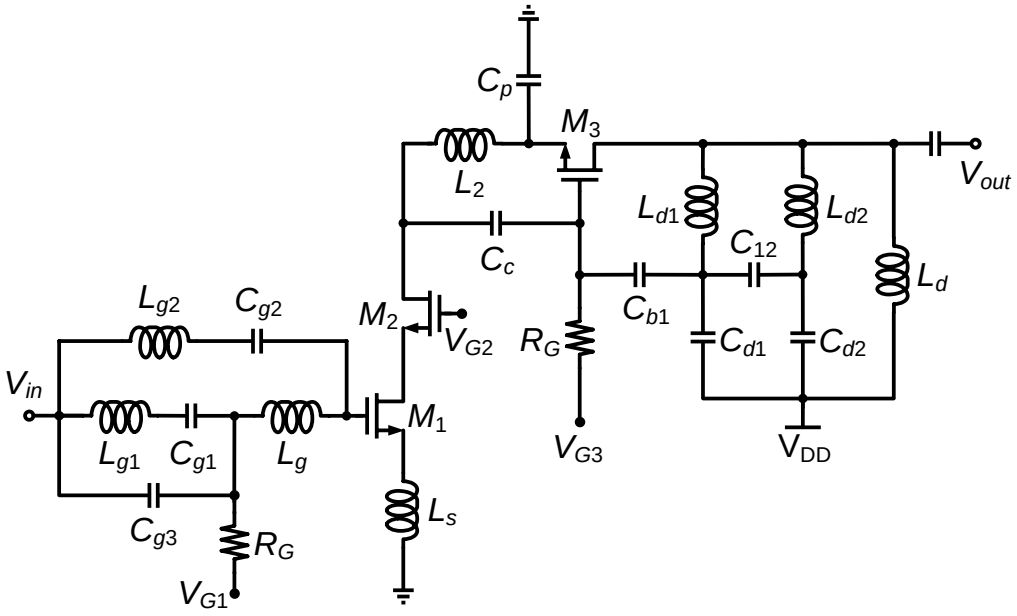
In chapter 6, conclusions are given.

CHAPTER 2

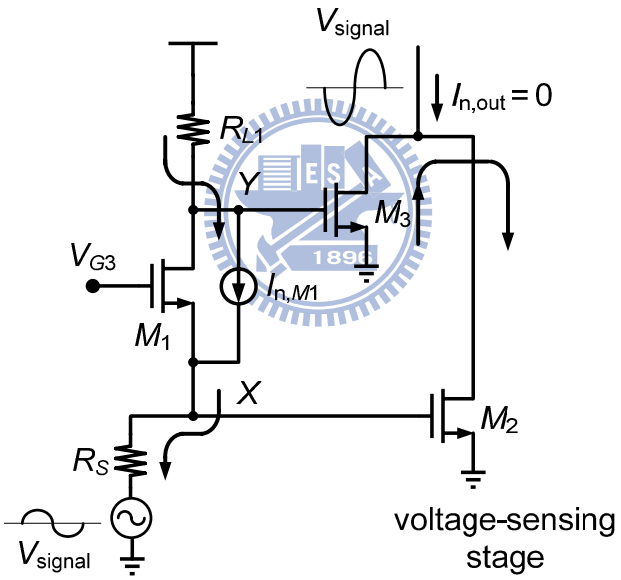
DESIGN OF THE TRIPLE-BAND LOW NOISE AMPLIFIER

2.1 INTRODUCTION

Recently, the widely used wireless communication systems have rapidly expanded the demand for low-cost and low-power RF integrated circuits which can support multi-band operations by a single system. Conventional design strategies have adopted different single-band transceiver circuits in parallel for different frequency bands [1]-[3]; however, it is unavoidable to result in a high implementation cost because of the large chip area, and simultaneously increase chip current dissipation. In order to improve the above-mentioned drawbacks, the topologies of the wideband LNA such as the resistive shunt-feedback structure [4], *LC* input network [5], common-gate 1/*gm* termination [6], and the distributed configuration [7] have been demonstrated and designed for multi-band application. Unfortunately, the broadband gain response will cause the unwanted interferers to impair the linearity of the receiver which is not desirable for the system considerations. To avoid this, the triple-band LNA shown in Fig. 2.1(a) has been devised in [8], [9], and it can suppress the out-band interferers while maintaining a sufficient in-band property. Nevertheless, the major drawback is the required high fabrication cost due to the usage of too many inductors. As a consequence, we propose two approaches by using a switched component to reduce the usage of inductors and the significant die area reduction will effectively decrease the cost of a multi-band RF system.



(a)



(b)

Fig. 2.1 (a) Triple-band LNA reported in [8], [9]. (b) A noise-canceling amplifier in [15]-[17].

In addition, it has become feasible to improve the noise performance of the LNA using the noise-canceling techniques. A source-degenerated cascode amplifier with an additional inductor at the drain of the main transistor is attractive for its excellent noise performance [10]-[12] and a 0.7 dB (from 5.5 to 4.8 dB) decrease in noise figure can be

achieved [10]. This is because the noise contribution from the cascode transistor can be reduced by using the inductor to cancel the effect of the parasitic capacitance at the drain of the main transistor. Inevitably, the extra inductor will occupy additional chip area, which makes it undesired for many applications. Inductively coupled plasma (ICP) deep-trench technique, which selectively removes the silicon underneath the inductors, is utilized to ameliorate the quality factor of on-chip inductors [13], [14]. A 0.5 dB noise figure decrease (from 2.28 to 1.78 dB) can be accomplished [13]; nevertheless, the extra CMOS process steps will increase the complication of the circuit implementation. Recently, a feedforward noise-canceling technique shown in Fig. 2.1(b) has been reported in [15]-[17]. The design principle of noise canceling is that the thermal noise of the common-gate amplifier can be neutralized by the voltage-sensing stage; however, the required common-source stage will make the total dc power consumption larger.

In this chapter, a momentous noise power diminution in MOS devices with an additional larger substrate resistor which can be employed in the nowadays LNA designs is presented and demonstrated. It can be observed that a maximum 32% noise reduction can be achieved due to the usage of larger resistance R_B without extra chip area, dc power and CMOS process steps.

This chapter is organized as follows. Section 2.2 introduces the principle of the proposed first triple-band LNA. Section 2.3 describes the detailed analyses of the second triple-band LNA. This chapter is summarized in Section 2.4. The target frequencies of the proposed triple-band LNAs are 2.5, 3.5, and 5.2 GHz, which can be used in the WiMAX system.

2.2 TRIPLE-BAND LOW NOISE AMPLIFIER WITH INPUT MATCHING DESIGN

It is known that the noise performance of LNA is dominated to the input stage. The proposed first triple-band LNA adopts a source-degenerated cascode amplifier, which selects the appropriate transistor size with finger width fixed at 5 μm to achieve input match and good noise figure simultaneously [18], [19]. Traditionally, the design criteria of the multi-band LNA such as that in the WiMAX application have used different LNAs for different frequency bands. Recently, a concept of triple-band LNA, as shown in Fig. 2.1(a), has been proposed [8], [9]. However, the chip area may be consumed while there are eight required inductors in the circuit.

2.2.1 Circuit Design and Analysis

Fig. 2.2(a) and (b) show the conventional dual-band and single-band input matching circuits, respectively. In this section, we have developed a novel manner for triple-band input matching, which is contrived by using dual-band input network with an additional switched component shown in Fig. 2.2(c). A significant area reduction and better noise figure can be achieved by reducing the usage of inductors in the input network. In the following analyses, it will facilitate the discussions to define that ω_1, ω_2, and ω_3 correspond to 2.5, 5.2, and 3.5 GHz, respectively. When the switch is off, the circuit is equivalent to that shown in Fig. 2.2(a), and it is to be operated as a dual-band input network at 2.5 GHz and 5.2 GHz. On the other hand, as the switch is on, the circuit becomes that in Fig. 2.2(b), and it is operated at 3.5 GHz. To this end, the values of the circuit components such as L_s, L_g, L_1, and C_1 of the proposed LNA

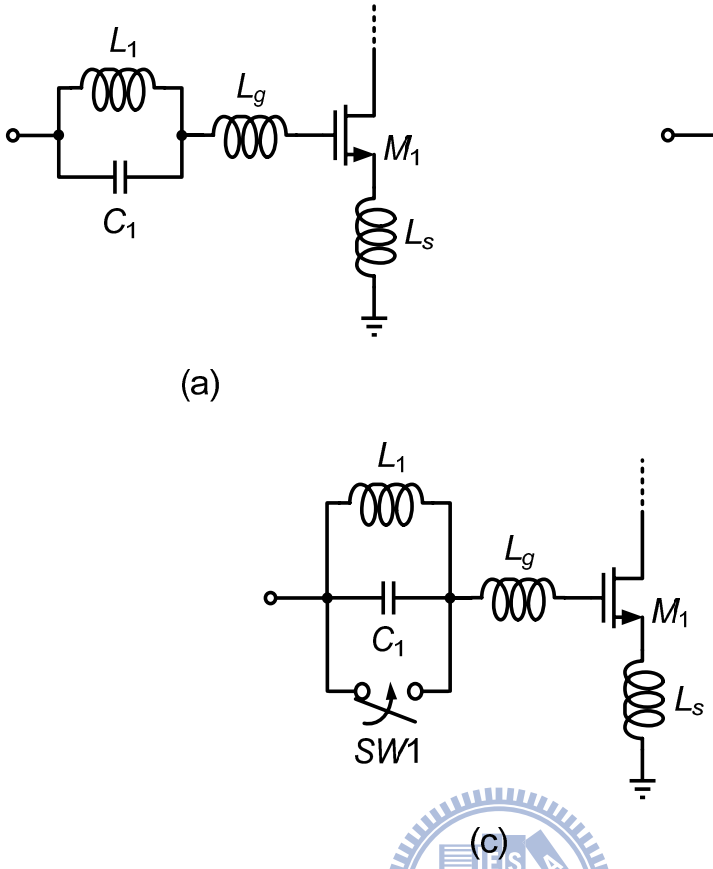


Fig. 2.2 (a) Schematic of a dual-band input matching. (b) Schematic of a single-band input matching. (c) A proposed triple-band input matching with an additional switched component.

circuit should be suitably designed in order to achieve the triple-band input matching. Based on the small-signal analysis, the input impedance for switch off status (Fig. 2.2 (a)) can be expressed as

$$Z_{in} = \frac{j\omega L_1}{1-\omega^2 L_1 C_1} + j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \quad . \tag{2.1}$$

To match the input port's impedance, the real term should be equal to 50 Ω and its imaginary term to zero, which yields

$$L_s = \frac{50C_{gs1}}{g_{m1}} \tag{2.2}$$

and

$$C_1(L_g + L_s)\omega^4 - (\frac{L_g + L_s}{L_1} + \frac{C_1}{C_{gs1}} + 1)\omega^2 + \frac{1}{C_{gs1}L_1} = 0 \ , \tag{2.3}$$

As can be seen in (2.3), the designed frequencies ω_1 and ω_2 (i.e., 2.5 and 5.2 GHz) satisfies

$$\omega_1^2\omega_2^2 = \frac{1}{C_1(L_g + L_s)C_{gs1}L_1} \tag{2.4}$$

and

$$\omega_1^2 + \omega_2^2 = \frac{\frac{L_g + L_s}{L_1} + \frac{C_1}{C_{gs1}} + 1}{C_1(L_g + L_s)} \ . \tag{2.5}$$

From (2.4), L_1 is obtained as

$$L_1 = \frac{1}{\omega_1^2\omega_2^2 C_1(L_g + L_s)C_{gs1}} \ , \tag{2.6}$$

which, upon substitution in (2.5), yields

$$C_1 = \frac{C_{gs1}}{(L_g + L_s)(\omega_1^2 + \omega_2^2)C_{gs1} - (L_g + L_s)^2\omega_1^2\omega_2^2C_{gs1}^2 - 1} \ . \tag{2.7}$$

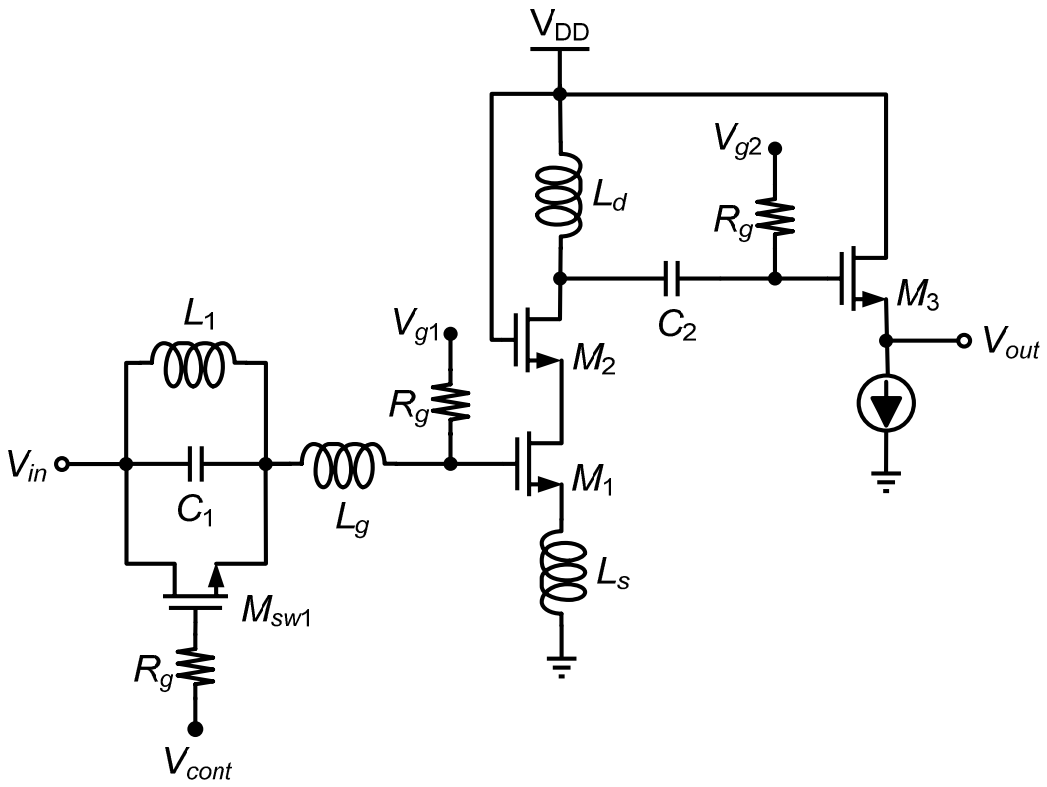


Fig. 2.3 Complete schematic of the proposed first triple-band LNA with input matching design.

On the other hand, when the switch is on (i.e., the single-band state for ω_3=3.5 GHz, Fig. 2.2 (b)), the criterion of a 50 Ω input impedance is still required and L_g can be expressed as

$$L_g = \frac{1}{\omega_3^2 C_{gs1}} - L_s = \frac{1}{\omega_3^2 C_{gs1}} - \frac{50 C_{gs1}}{g_{m1}} , \qquad (2.8)$$

where (2.2) has been incorporated. As we will see, the precise values of L_s=0.25 nH, L_g=3.5 nH, L_1=2 nH, and C_1=0.9 pF can be predicted by drawing on (2.2), (2.8), (2.7), and (2.6) when the width of the transistor M_1 (300 μm) is chosen with 10 mW power dissipation. The first triple-band LNA is shown in Fig. 2.3 and it is noticed that the equivalent circuit of a switched component exists parasitic capacitances, which cause

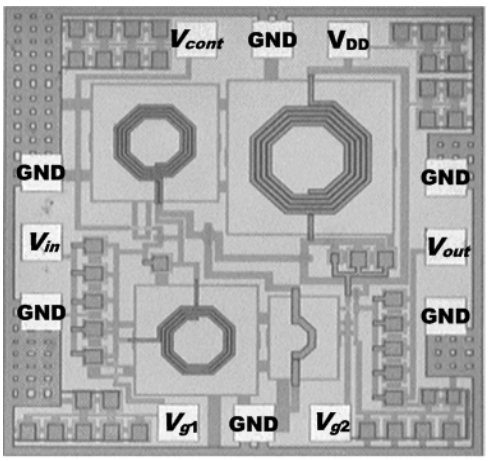
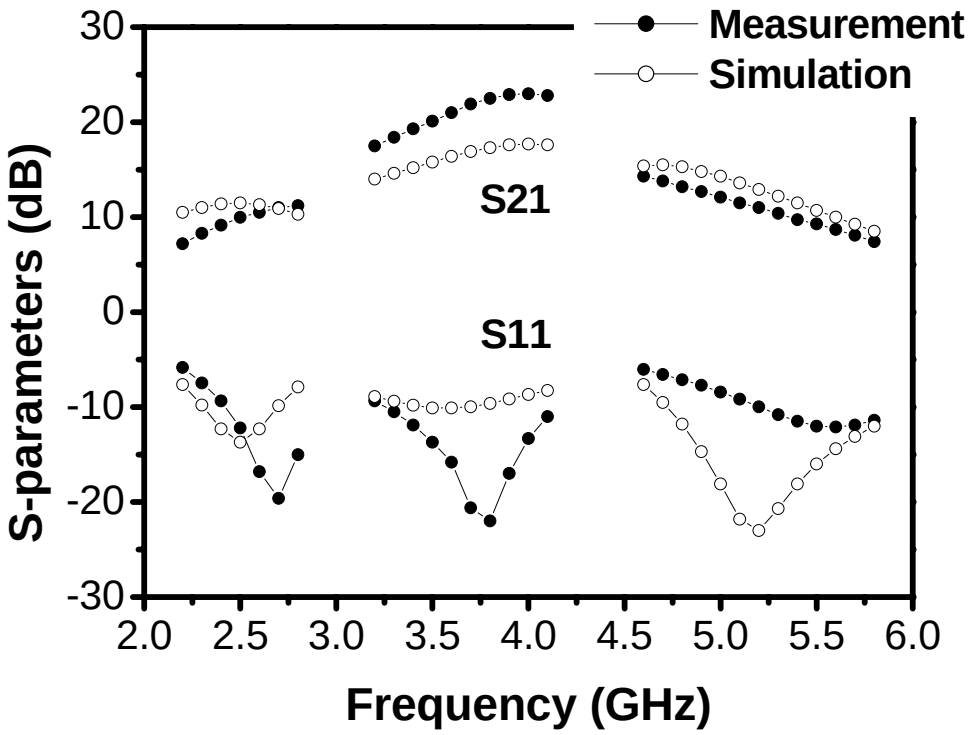


Fig. 2.4 Microphotograph of the first triple-band LNA with 0.98×0.94 mm^2 die area.

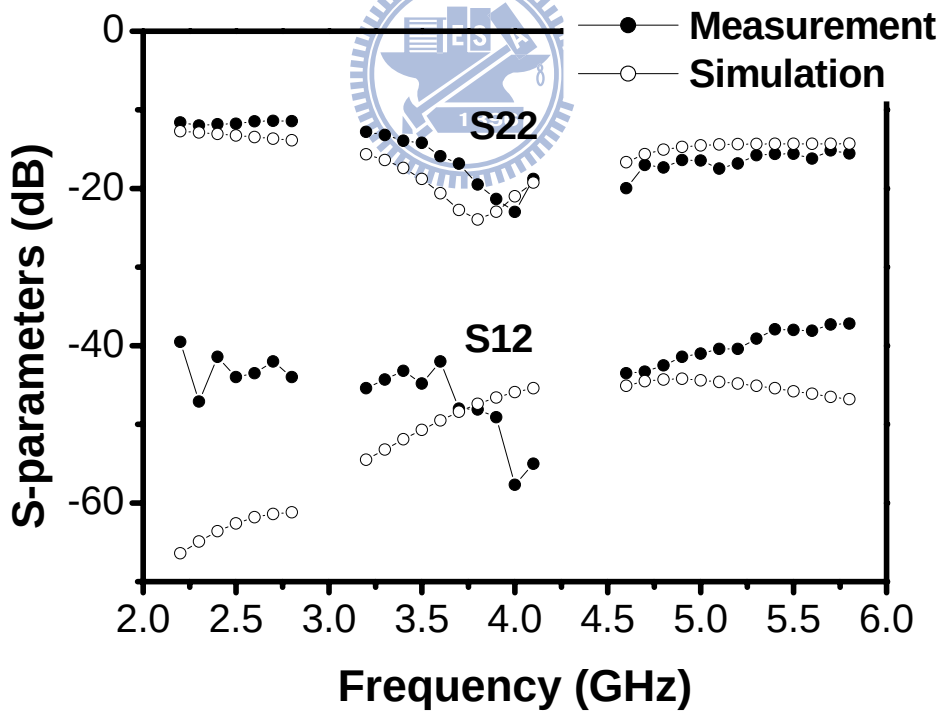
C_1 should be adjusted. In addition, for testing purposes, an output buffer consisted of a source follower is included in the design circuit, which roughly introduces a 6 dB loss in the signal path [20].

2.2.2 Simulation and Experimental Results

The die microphotograph of the first triple-band LNA is shown in Fig. 2.4, and measured by using on-wafer probing. The LNA chip without the output buffer draws a total 5.5 mA dc current from the 1.8 V supply voltage. The S-parameters of the designed LNA is measured using the Agilent 8510C vector network analyzer. The simulated and measured results of S- parameters are depicted in Fig. 2.5. The measured peak gains are 10/20.1/11 dB at 2.5/3.5/5.2 GHz while the input and output return losses are better than 10 dB in the operation frequencies. The noise figure is measured using the Agilent N8975A noise figure analyzer with Agilent 346C noise source. The simulated and measured noise figures at the same bias condition are depicted in Fig. 2.6. It is seen that the minimum values of the measured noise figure are equal to 3.3/3.6/4.6 dB at 2.5/3.5/5.2 GHz.



(a)



(b)

Fig. 2.5 Measured and simulated S-parameters of proposed first triple-band LNA.

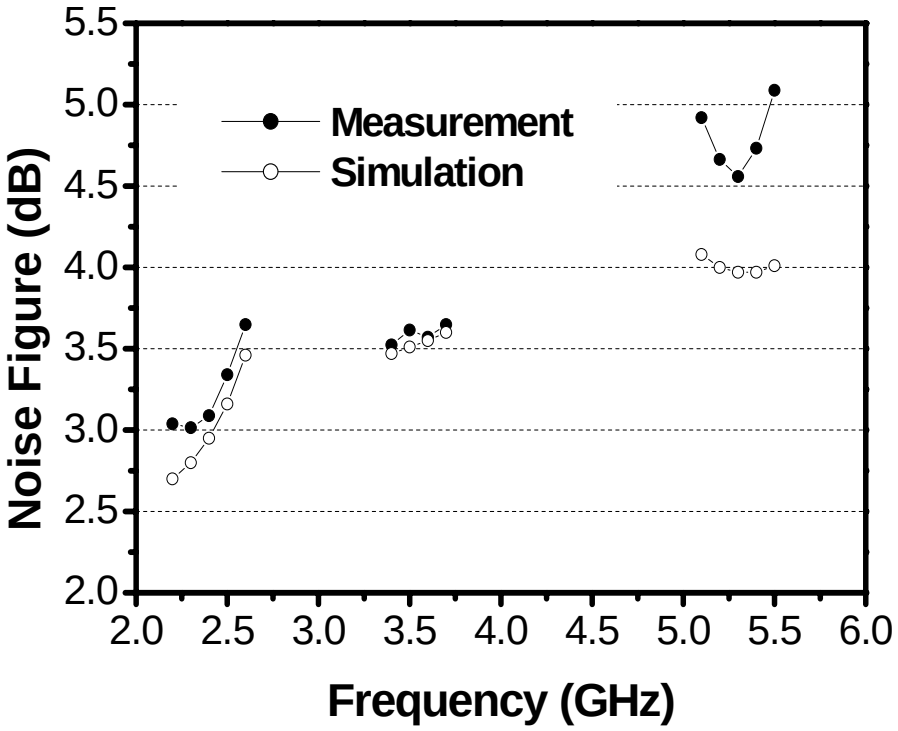


Fig. 2.6 Measured and simulated noise figure of proposed first triple-band LNA.

2.3 TRIPLE-BAND LOW NOISE AMPLIFIER WITH NOISE REDUCTION

The first triple-band LNA can reduce chip area significantly by using dual-band input network with an additional switched component. However, it is unavoidable to worse noise figure result due to the usage of low-Q inductors in input network. To enhance the noise performance, we have tried the second LNA which utilizes the double-peak single-notch network [21] with an additional switch as the load impedance to achieve the same characteristic of the first LNA. Moreover, a common-drain stage in the feedback path is adopted to accomplish 50-Ω wideband input matching and partial noise cancellation simultaneously. The buffer transistor with a purely 50-Ω resistive load is employed to achieve output matching for testing purposes.

2.3.1 Triple-Band Load Network

The triple-band load network, as shown in Fig. 2.7(c), is operated by turning the switch M_{SW1} on and off. Evidently, this network is simplified into a LC tank operated in ω_3=3.5 GHz when the switch M_{SW1} is off (i.e., Fig. 2.7(b)). Similarly, when the switch M_{SW1} is on, the dual-band load impedance operated in ω_1=2.5 GHz and ω_2=5.2 GHz is employed and expressed by

$$Z_{load} = \frac{j\omega L_d (1-\omega^2 L_1 C_1)}{\omega^4 L_d C_d L_1 C_1 + \omega^2 (L_d C_d + L_1 C_1 + L_d C_1) + 1} \quad . \tag{2.9}$$

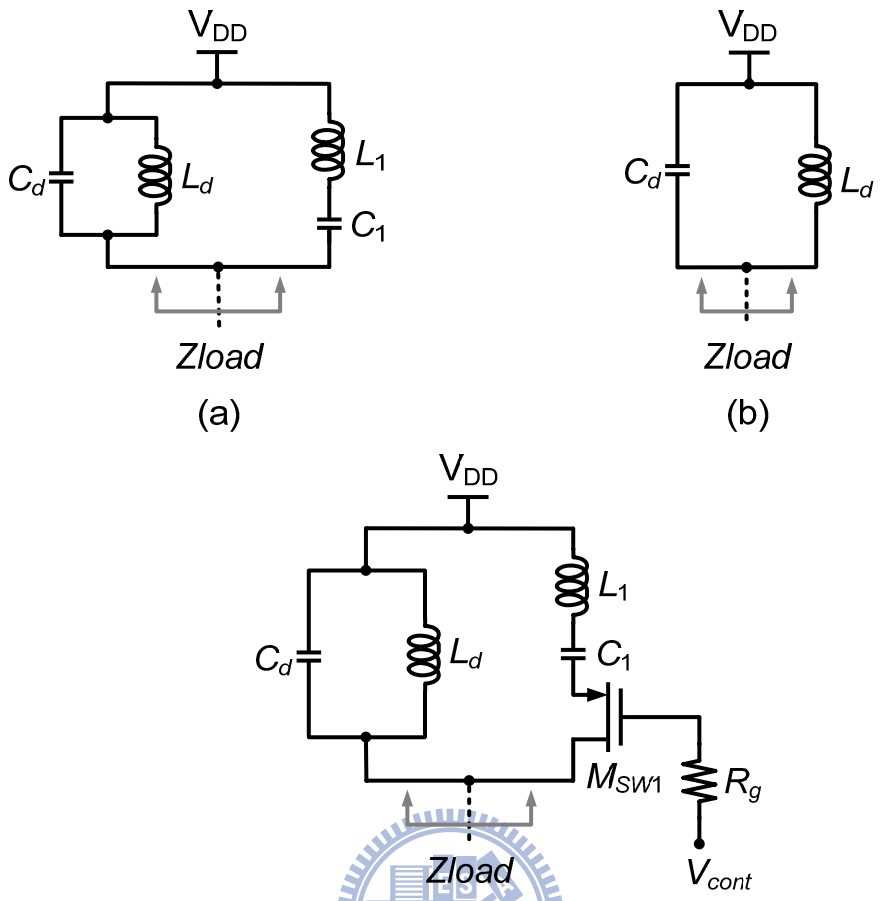


Fig. 2.7 (a) Schematic of a dual-band load network. (b) Schematic of a single-band load network. (c) A proposed triple-band load network with an additional switched component.

Equation (2.9) also represents that the two poles ω_1 and ω_2 can be obtained by letting the denominator equal null, or

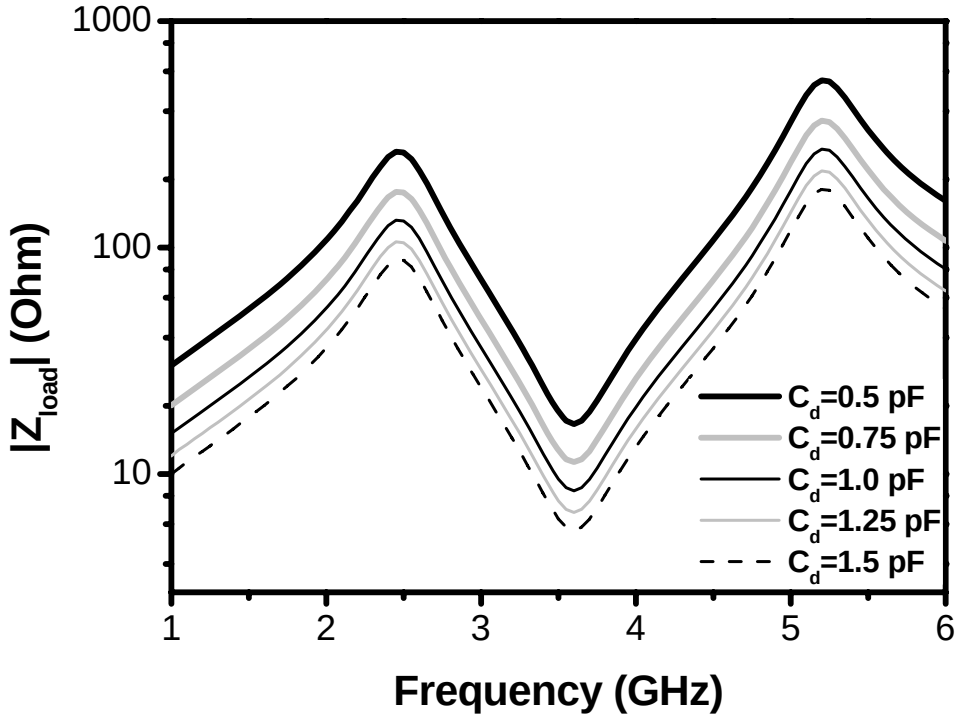
$$\omega^4 L_d C_d L_1 C_1 + \omega^2 (L_d C_d + L_1 C_1 + L_d C_1) + 1 = 0 \ . \tag{2.10}$$

In addition, $1/\sqrt{L_1 C_1} = 1/\sqrt{L_d C_d}$ is satisfied to facilitate the design, which retains to provide similar amplitudes and symmetries in the two maxima of Z_{load}. It is noted that the proposed triple-band load network has three given target frequencies for the four

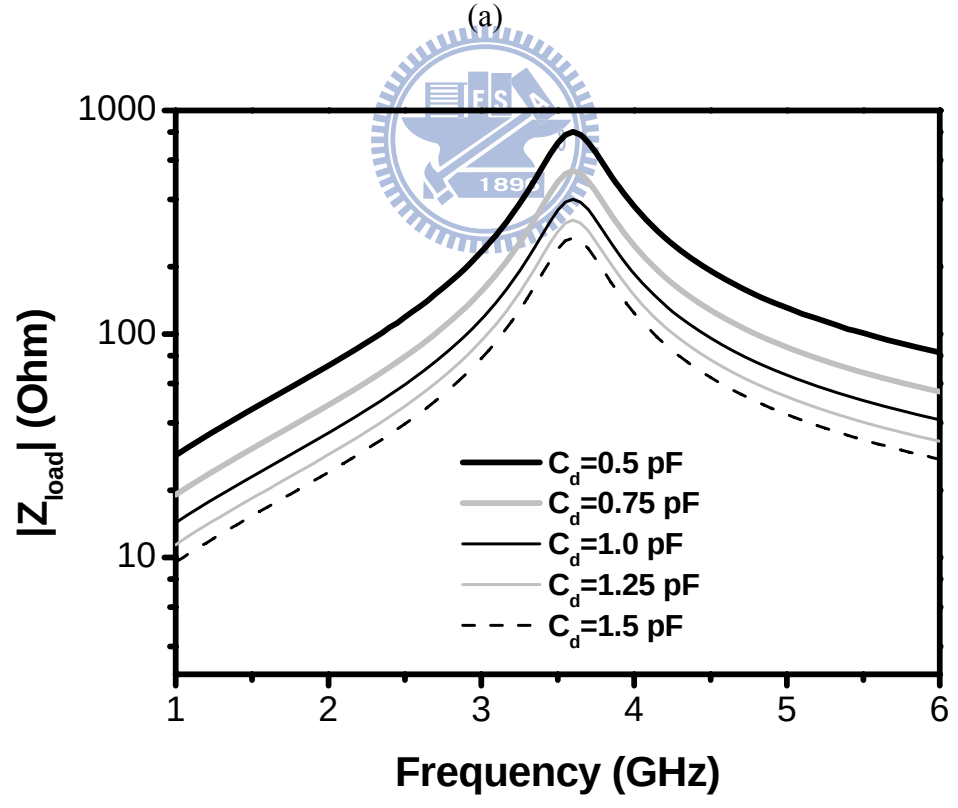
load components, which means that there is still one degree of freedom, let say C_d, left for the circuit design. Fig. 2.8(a) and (b) show the load impedance versus frequency with different C_d parameters. In general, the first step in the design criteria of the proposed load network is to select a lower C_d since the higher the load impedance, i.e., the LNA gain. However, a drawback which may make the design criteria unsatisfactory is a high implementation cost due to the requirement of the larger inductance L_1 and L_d. Therefore, it should be taken into account the trade-off between the gain and die area punctiliously.

2.3.2 Input Matching with Partial Noise Cancellation

The design of the first stage is a common-source structure with a feedback common-drain amplifier in order to achieve the wideband input matching of 50-Ω. The input impedance Z_{in} shown in Fig. 2.9 is close to $1/g_{m3}(1+ g_{m1}Z_L)$, which is interrelated to the bias voltage of the transistors M_1 and M_3 since g_{mi} is proportional to the current of transistors. Consequently, the input matching characteristic can be effectively tuned by adjusting the bias voltages V_{g2}, V_{g3}, and the bias current I_4 to compensate for the process variation. On the other hand, the introducing of a feedback structure with the common-drain stage also can attain the partial noise cancellation, which is demonstrated in the following analyses. As shown in Fig. 2.9, the noise voltage V_{nX} at node X is generated due to the thermal noise current i_n of the transistor M_1. The adopted feedback common-drain amplifier M_3 will bring about the in-phase noise voltage V_{nY} at node Y, which can be further converted to node X with opposite phase (i.e., the noise voltage V_{nYX}) by the common-source cascode amplifier M_1–M_2. Therefore, the noise contributed by M_1 is partially cancelled at the output node X, as can be observed from Fig. 2.10.



(a)



(b)

Fig. 2.8 The load impedance versus frequency with different *C* parameters. (a) A dual-band load network when the switch is on. (b) A single-band load network when the switch is off.

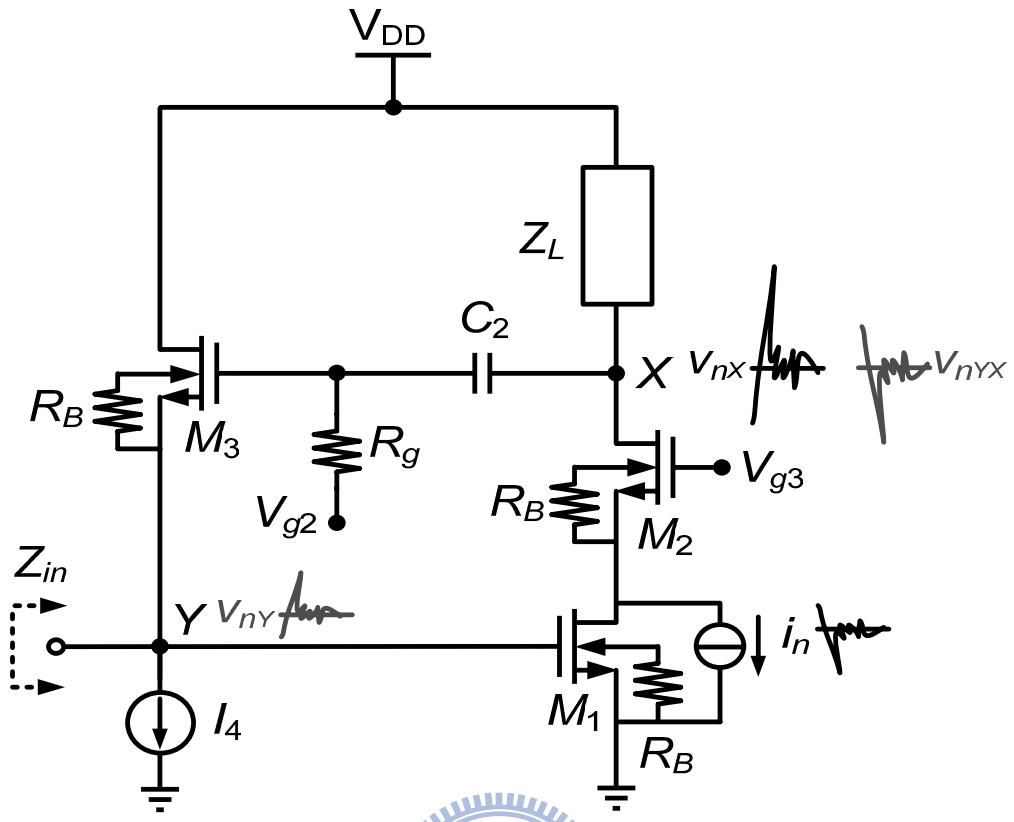


Fig. 2.9 Principle of the noise-canceling technique.

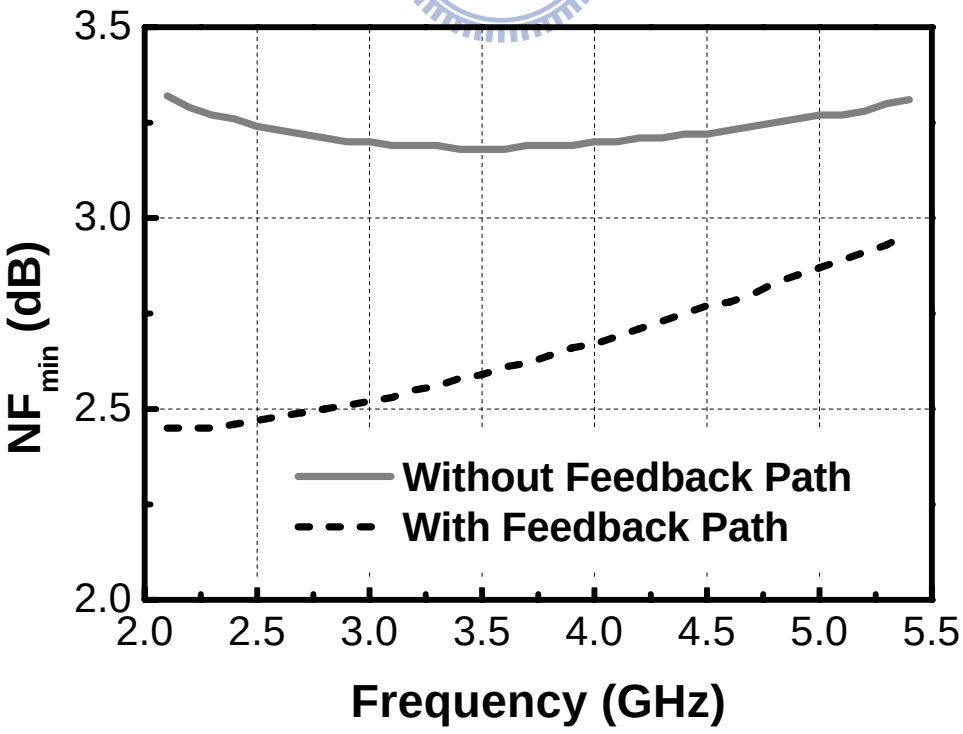


Fig. 2.10 Simulated noise figures with and without the noise-canceling technique.

2.3.3 Noise Reduction with Larger Substrate Resistor

In order to further ameliorate the noise performance of a CMOS LNA, a significant noise power reduction in MOS device by using larger substrate resistor R_B, as shown in Fig. 2.11(a), is presented. To begin with, the complete noise equivalent circuit must be established to facilitate the demonstration of the proposed noise-reduction structure. It is well-known that the body effect transconductance can be expressed as

$$g_{mb} = \frac{\gamma}{2\sqrt{2\varphi_f + V_{SB}}} g_m \tag{2.11}$$

where γ is the body-effect coefficient, φ_f is the bulk fermi potential, V_{SB} is the voltage between body and source. If we make the assumption that the source voltage drops sufficiently below the bulk voltage, then it is observed intuitively from Fig. 2.11(b) that the current I_B is formed because of the forward-biasing. Contradictorily, the current I_B injected into the external substrate resistance R_B will bring about $V_{SB} > 0$. As a consequence, no current flows between body and source (i.e., V_{SB}=0) and this means that the body effect transconductance is inexistent in the noise equivalent circuit (see Fig. 2.11(c)) for the MOS device with a larger substrate resistor R_B. Furthermore, the dominant noise source modeled as a shunt current source in the output circuit of the device is channel thermal and the output noise power density arising from this source is

$$\overline{i_{out}^2} = 4kT\gamma' g_{d0} \left| \frac{i_{out}}{i_d} \right|^2 \tag{2.12}$$

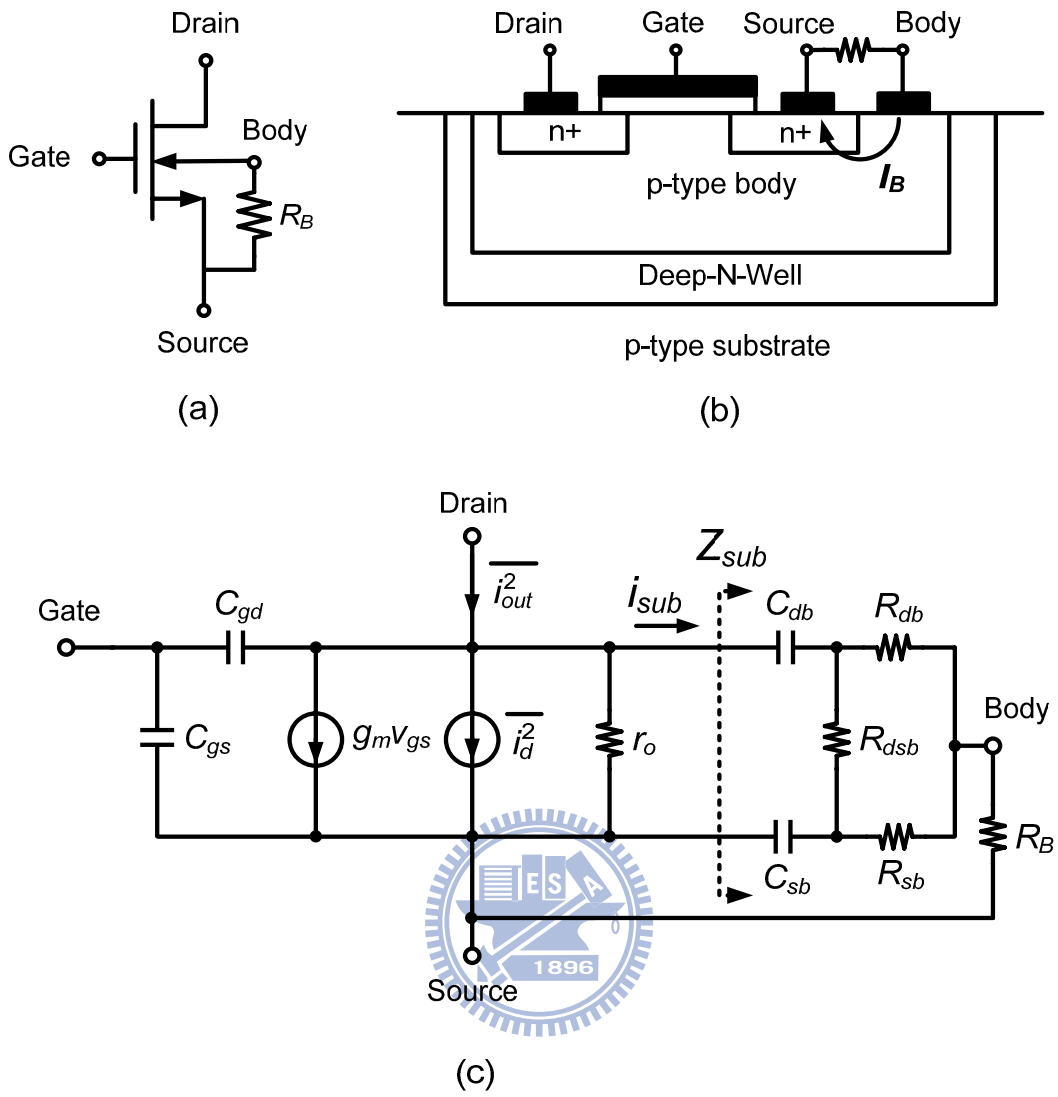


Fig. 2.11 (a) A NMOS device with a larger substrate resistance R_B=8 kΩ. (b) Structure of a NMOS with a larger substrate resistance R_B. (c) The noise equivalent circuit of a NMOS device with a larger substrate resistance R_B.

where γ' is a bias-dependent factor, and g_{d0} is the zero-bias drain conductance of the device [22, Chapter 7]. In general, $1/sC_{sb} >> R_{sb}$ is satisfied and demonstrated in [23]; therefore, the substrate impedance Z_{sub} can be simplified to a simple series CR circuit (i.e., C_{db} in series with $(R_{dsb}+R_{sb})||R_{db}$, and R_B) as follows:

$$Z_{sub} \approx \frac{1}{j\omega C_{db}} + \left[\frac{R_{db}(R_{sb}+R_{dsb})}{R_{db}+R_{sb}+R_{dsb}} + R_B \right]. \tag{2.13}$$

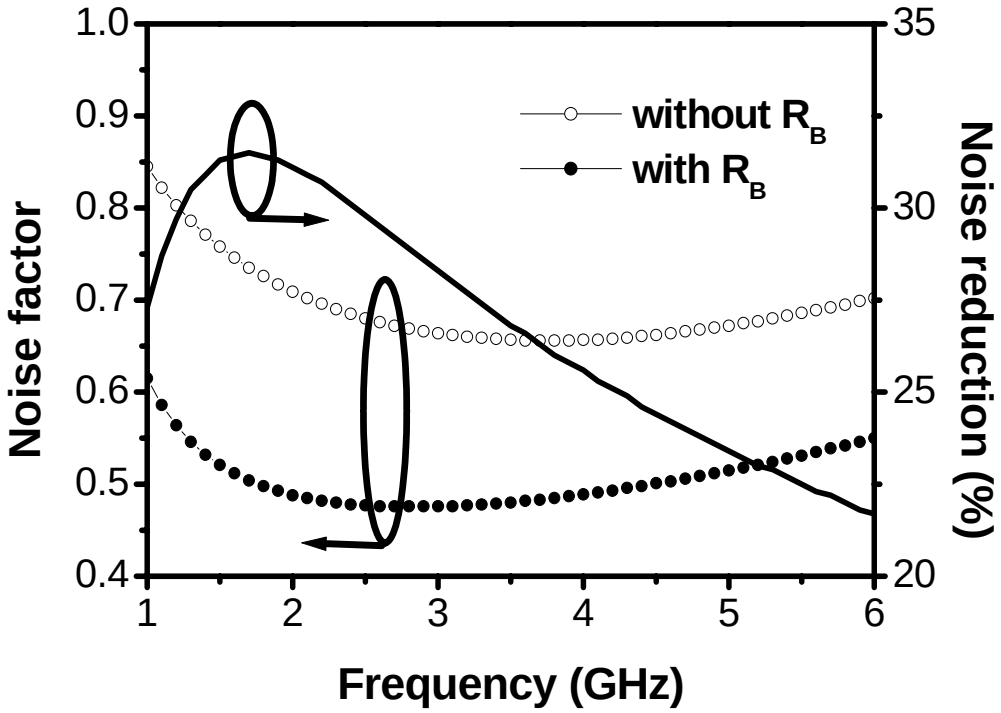
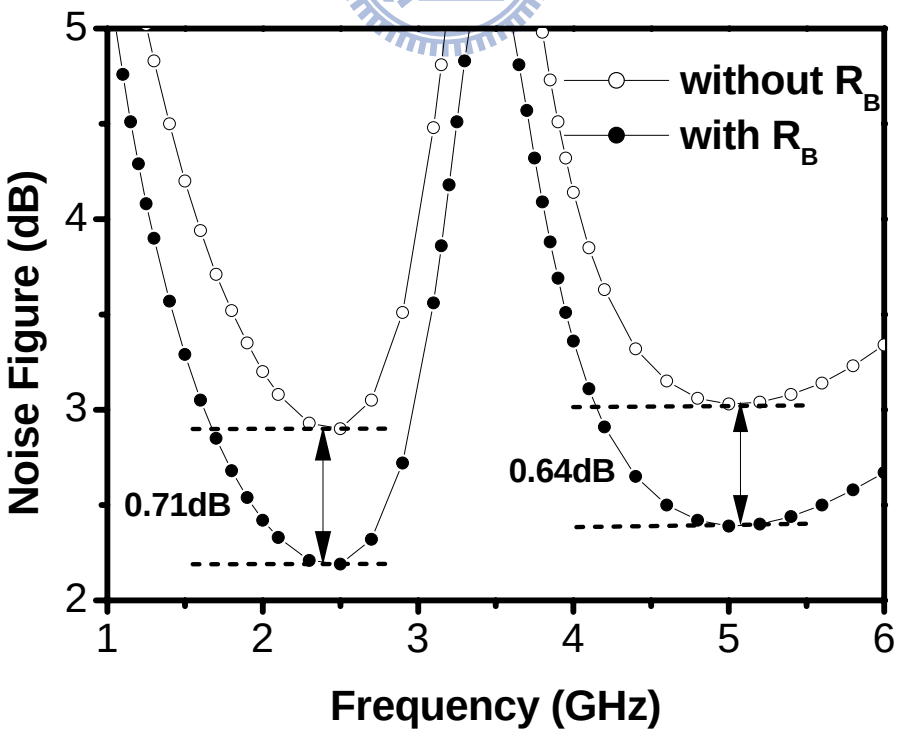
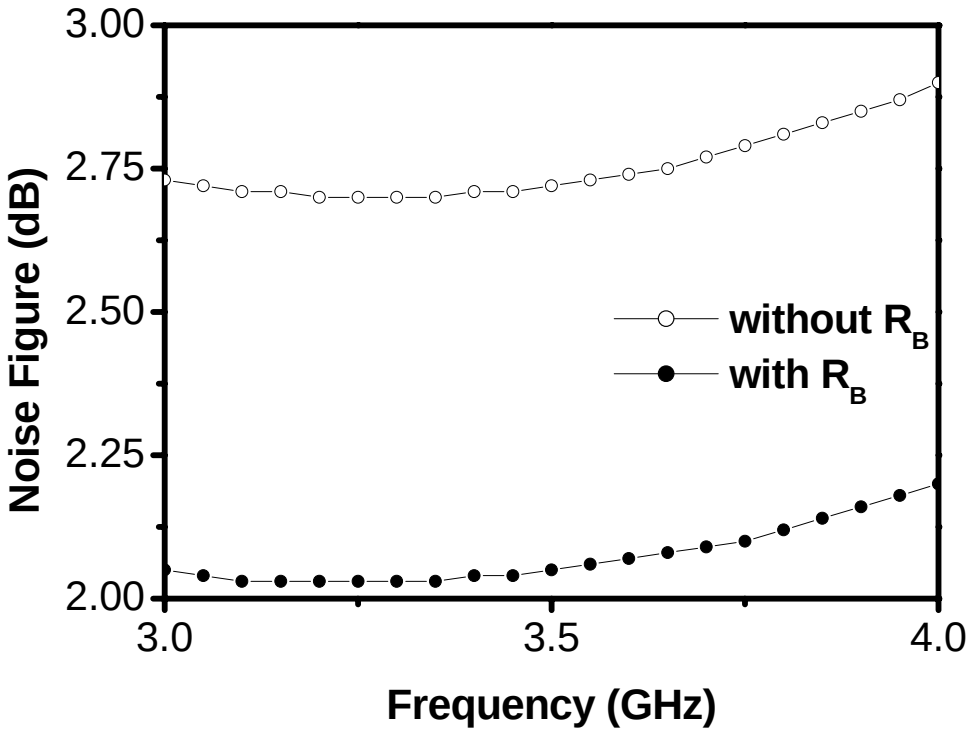


Fig. 2.12 Simulated the total MOS device noise factor F (NF=10log$_{10}$ F) with and without the additional resistance R_B=8 kΩ and the noise reduction when resistance R_B is used.



(a)



(b)

Fig. 2.13 Simulated noise figure with and without the additional resistor R_B=8 kΩ. (a) Dual-band status when the switch is on. (b) Single-band status when the switch is off.

As we can see, a larger Z_{sub} by increasing the value of R_B will result in the reduction of i_{sub}. The noise factor F (NF=10log$_{10}F$) contributed by total MOS device is shown in Fig. 2.12 and a significant noise power reduction in MOS device can be demonstrated by the additional resistor R_B. A maximum 32% noise reduction can be achieved without extra chip area, CMOS process steps and dc power. Fig. 2.13 shows the simulation results of noise figure with and without the additional resistor R_B. It can be observed that the 0.71/0.67/0.64 dB decrease in noise figure are attained at 2.5/3.5/5.2 GHz due to the usage of larger resistance R_B=8 kΩ.

2.3.4 Simulation and Experimental Results

The complete schematic and die microphotograph of the second triple-band LNA

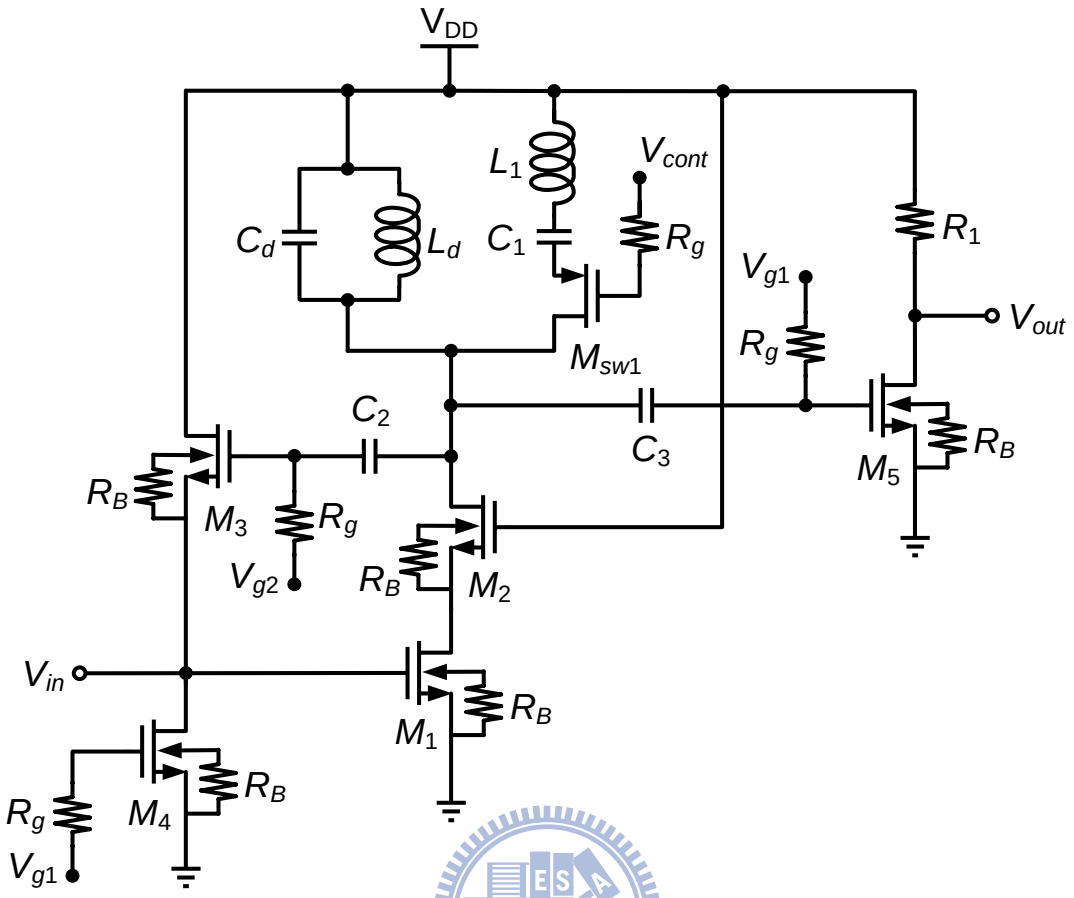


Fig. 2.14 Complete schematic of the proposed second triple-band LNA with the load network design and the noise reduction resistance R_B.

are shown in Fig. 2.14 and Fig. 2.15, respectively. The die area including pads is 0.75×0.69 mm^2, which has been measured by using on-wafer probing. The total dc power of the LNA chip without the output buffer is 14.2 mW. The simulated and measured results of S-parameters are depicted in Fig. 2.16. The measured peak gains are 12.3/15.3/13.1 dB at 2.5/3.5/5.2 GHz while the input and output return losses are better than 10 dB in the operation frequencies. The simulated and measured noise figures are depicted in Fig. 2.17 and the measured minimum noise figures at 2.5/3.5/5.2 GHz are 2.3/2.2/2.7 dB.

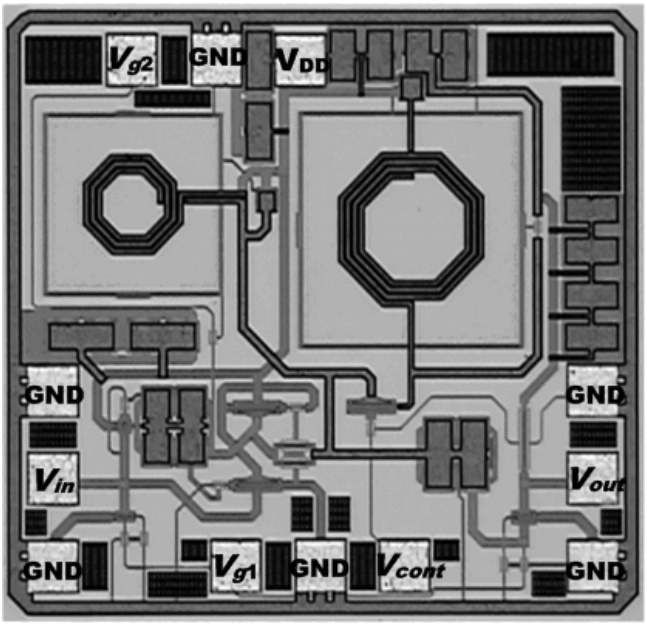
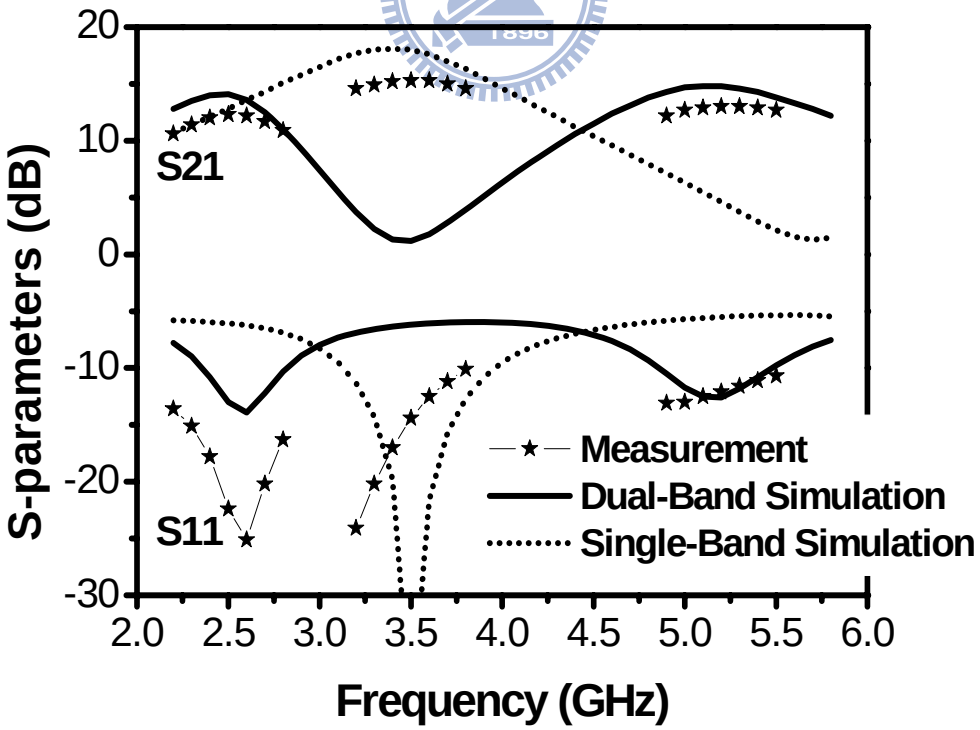
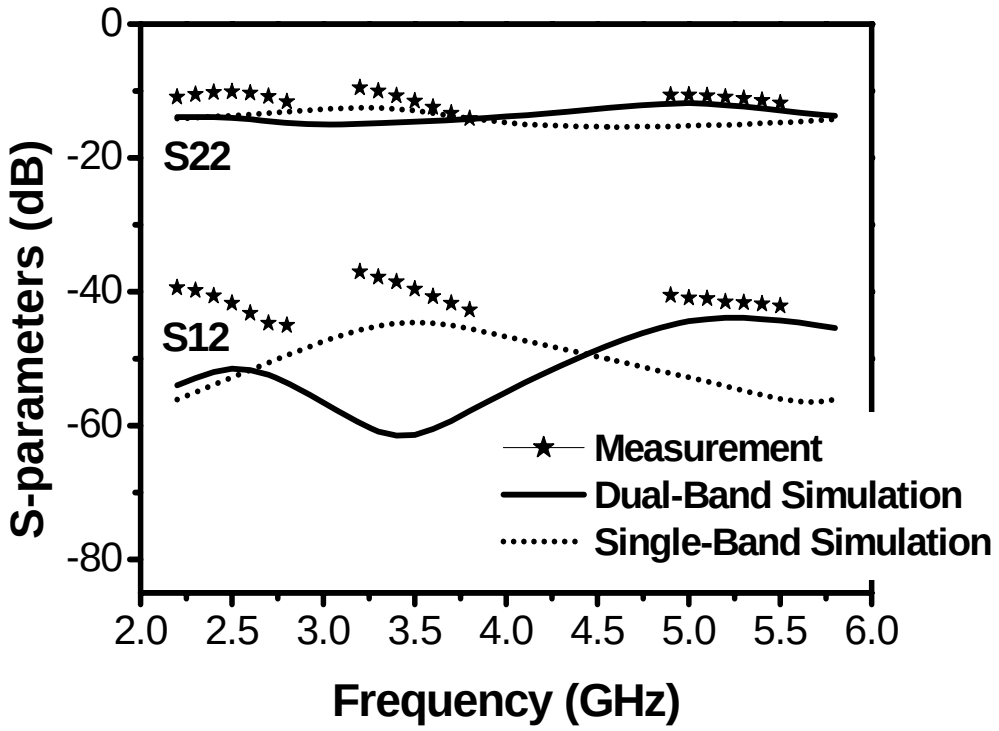


Fig. 2.15 Microphotograph of the second triple-band LNA with 0.75×0.69 mm^2 die area.



(a)



(b)

Fig. 2.16 Measured and simulated S-parameters of the second triple-band LNA.

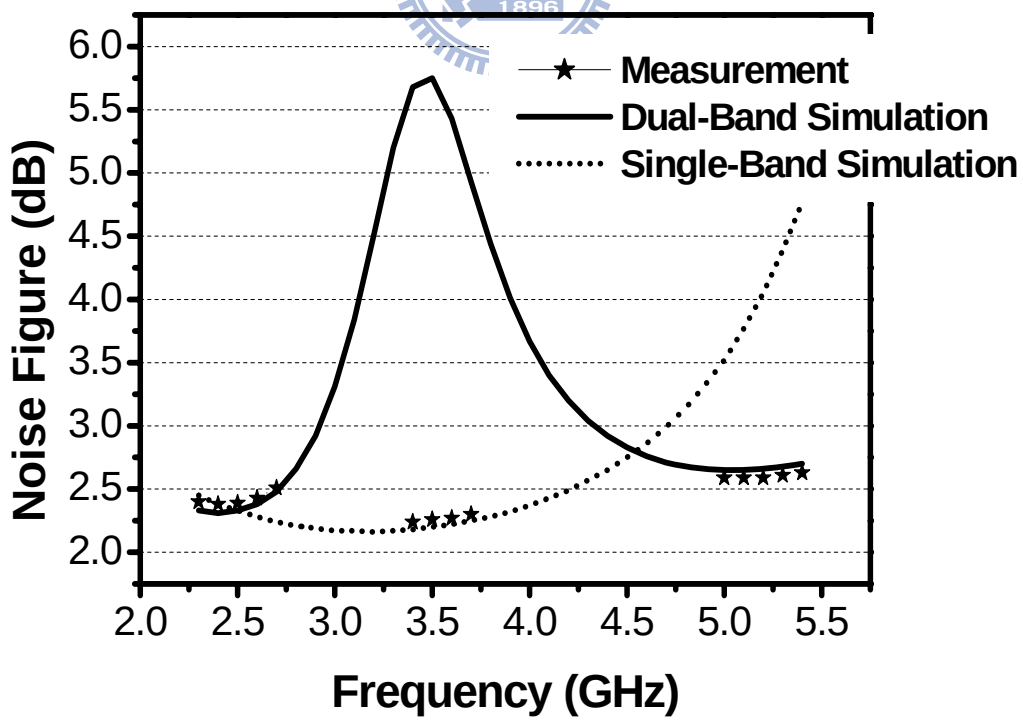


Fig. 2.17 Measured and simulated noise figure of the second triple-band LNA.

2.4 SUMMARY

The triple-band LNAs with a switched resonator concept have been fabricated using 0.18-μm CMOS technology and a significant die area reduction can be achieved. Furthermore, an additional larger substrate resistor R_B will diminish the output noise power density of MOS device and the 0.71/0.67/0.64 dB noise figure decrease can be attained at 2.5/3.5/5.2 GHz in the second approach of the triple-band LNA without extra chip area, dc power and CMOS process steps. The measured results, including the power gain, the return loss, and the noise figure, agree quite well with the simulated results. The presented triple-band LNAs are compared with recently published CMOS LNA and summarized in Table 2.1.

Table 2.1

Performance summary of previously published LNAs

Ref.	Tech. [μm]	Freq. [GHz]	S_{11} [dB]	G_{max} [dB]	NF_{min} [dB]	P_{diss} [mW]	Area [mm^2]
[4]	0.18	3 ~ 6	<-12	15.9	4.7	59.4	1.1
[5]	0.18	2.8 ~ 7	<-4	19.1	3	32	1.63
[7]	0.18	dc ~ 7	<-16	8.6	4.2	9	1.16
[24]	0.13	2 ~ 5.2	<-9	16	4.7	38	0.24
[25]	0.09	2.5 ~ 4	<-10	10.6	4	16	0.77
[26]	0.13	3 ~ 5	<-10	19.4 Ψ	3.5	31.5	1.6
[27]	0.18	3 ~ 4.8	<-10	13.9	4.7	14.6	0.95
[28]	0.18	3 ~ 4.8	<-7	14.3	3.45	13.5	1.8
[29]	0.18	2.44 5.76	<-10 <-6	7.6 8.6	5.7 6.8	10.8	1.15
[9]	0.25	1.8 2.45 5.25	<-10	10.1 10.8 11.8	3.7 4.8 6.4	39.1	1.68
[30]	0.18	0.95 2.4 5.2	<-7 <-10	18 24 23	4.6 4.4 4.4	32.4	1.34
LNA1	0.18	2.5 3.5 5.2	<-10	10 20.1 11	3.3 3.6 4.6	10	0.92
LNA2	0.18	2.5 3.5 5.2	<-10	12.3 15.3 13.1	2.3 2.2 2.7	14.2	0.52

CHAPTER 3

DESIGN OF IMAGE-REJECTION MIXER FOR DUAL-BAND OPERATION

3.1 INTRODUCTION

The down-conversion mixer, which converts the high RF frequency to a low IF frequency, is a required building block of the transceiver. It is also an important component associated with the linearity of the front-end receivers. In general, Gilbert cell is a typical type of the active mixers, and the Gilbert mixer consists of three stages: transconductor stage, switching stage, and load stage. The linearity of Gilbert mixer will be dominated by the transconductor stage if the switching stage is ideal. In order to get higher conversion gain, good isolation, and better dynamic and static offsets, and help to improve the second and third order intermodulation rejection, the double balanced Gilbert mixer with differential RF, LO, and IF signals are commonly used for optimum operation.

In addition, the suppression of the image signal is an essential requisite for the RF receiver design. Generally, the dual-band image rejection mixer can be achieved by either Hartley or Weaver architecture, but the image rejection characteristic is restricted due to the magnitude mismatch and phase error of the quadrature signal. On the other hand, the required dual-band mixer with quadrature signal generator for dual-band operation will further increase the complication of the circuit implementation, which is undesired for low-cost and low-power application. In this chapter, we adopt the differential, dual-band, third-order, active notch filter to

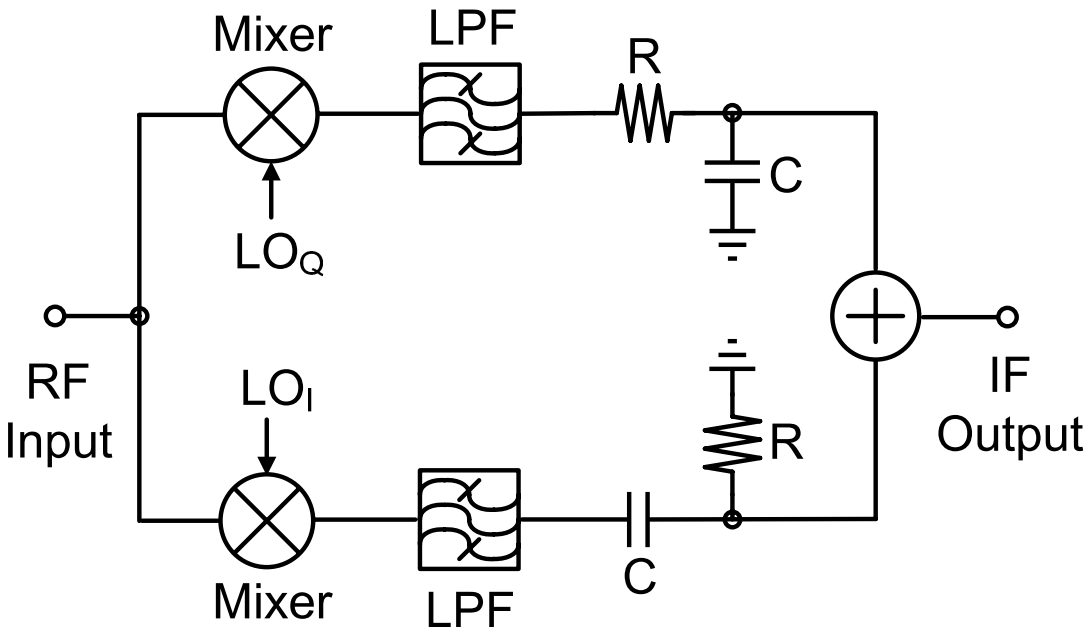


Fig. 3.1 Block diagram of the Hartley down-converter.

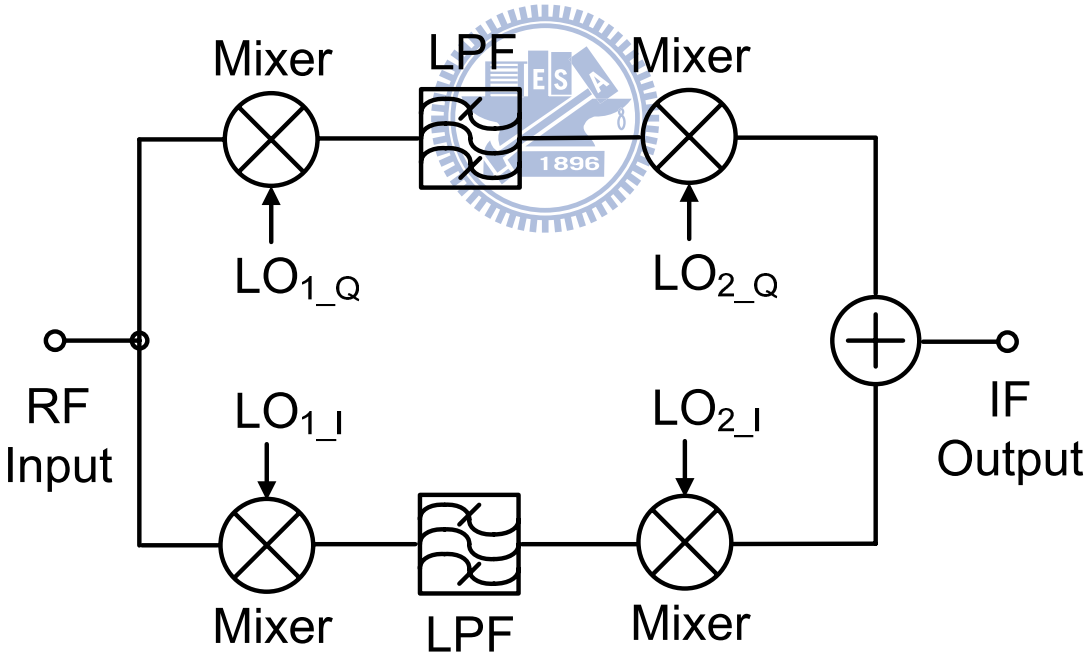


Fig. 3.2 Block diagram of the Weaver down-converter.

attenuate the dual-band image signal while maintaining a superior in-band performance and achieve smaller chip area and dc power consumption than previous circuits [32]-[35].

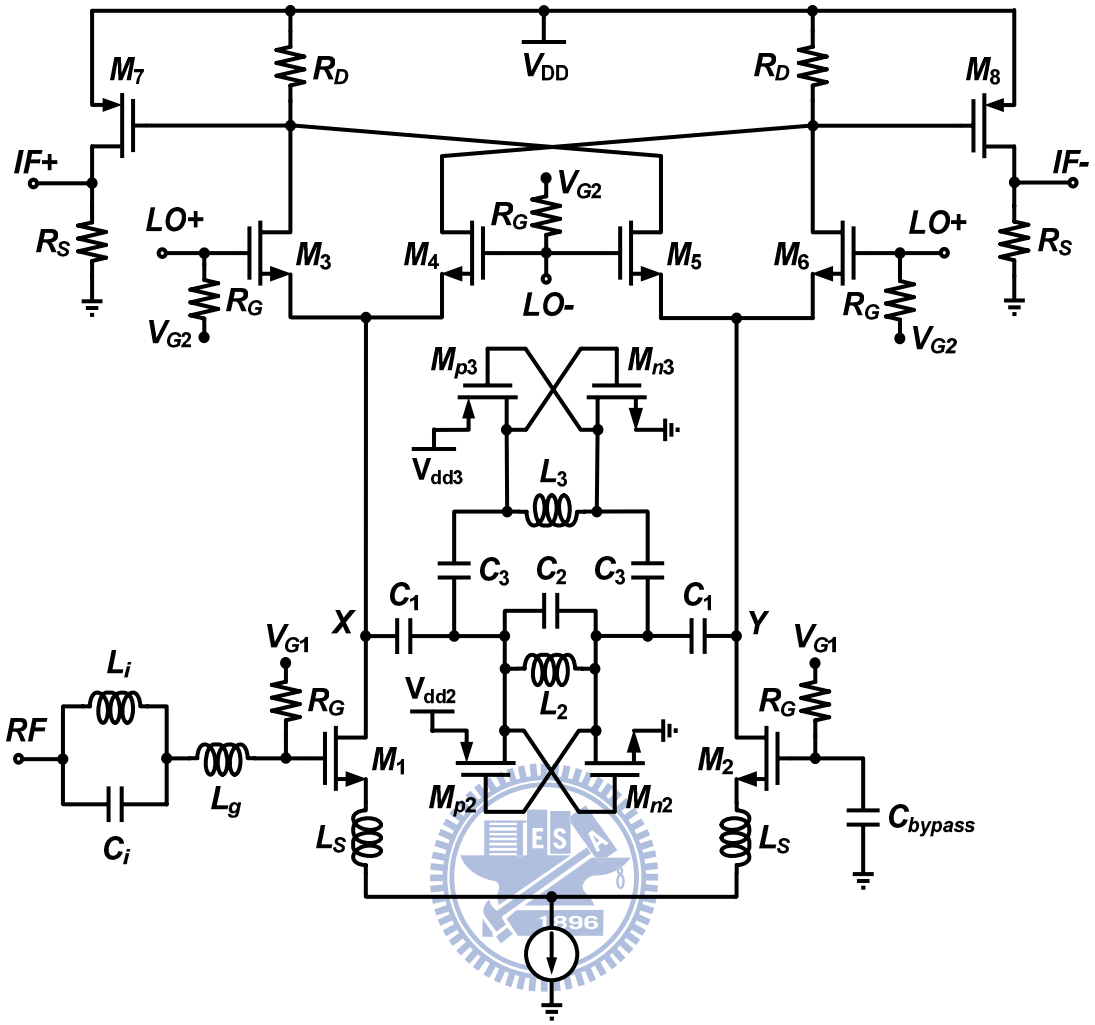


Fig. 3.3 Complete schematics of the proposed dual-band image rejection mixer.

3.2 CIRCUIT DESIGN

The proposed dual-band image rejection mixer fabricated by 0.18-μm TSMC CMOS process is shown in Fig. 3.3 with the target dual-band frequencies at 2.4~2.48 and 5.15~5.35 GHz. The common-source differential pair (M_1 and M_2) with one of the inputs grounded by a capacitor can be regarded as a single-ended to differential balun. In addition, the proposed mixer adopts a source-degenerated amplifier with a dual-band input network (L_i, C_i, L_g) to achieve a 50 Ω match at 2.45 and 5.2 GHz. The

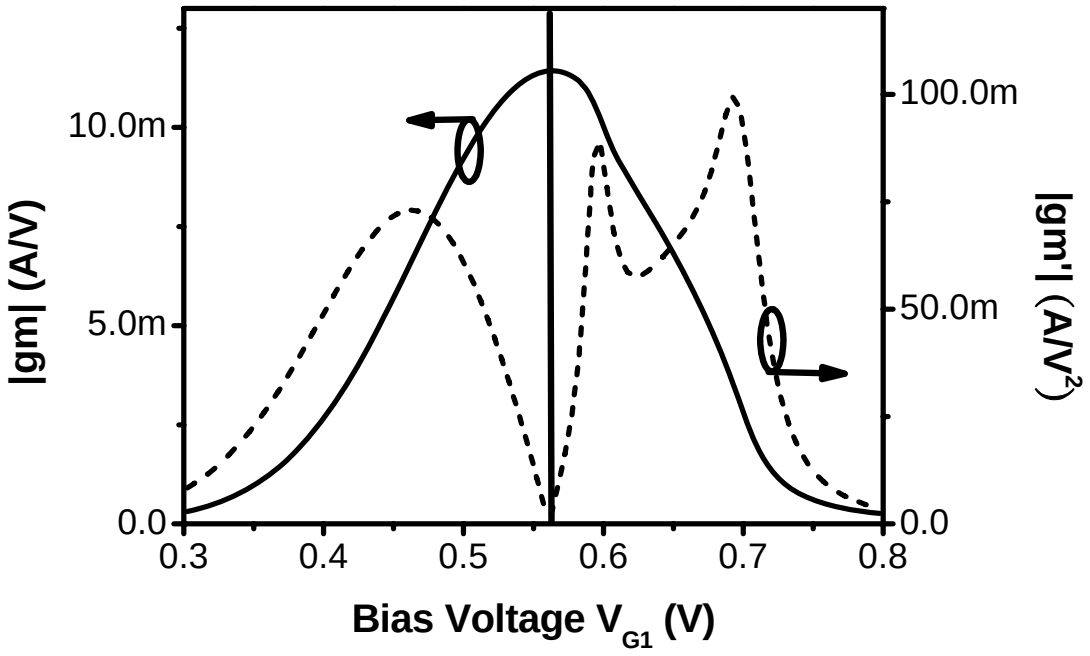
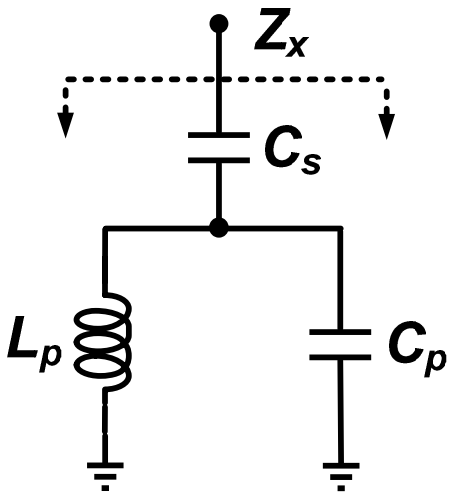


Fig. 3.4 The nonlinear effect of a transistor with the bias voltage V_{G1}.

circuitry in between nodes *X* and *Y* is the proposed dual-band active notch filter to be discussed below.

3.2.1 Effect of Nonlinearity

In general, the nonlinear effect of a transistor in Fig. 3.4 is interrelated to the gate-to-source bias voltage and the second order transconductance coefficient g_m' could be minimized while the maximum linear transconductance g_m is selected (i.e., the larger conversion gain, the superior second order harmonic suppression) [36]. Consequently, the second order harmonics behavior can be effectively diminished by adjusting the bias voltage V_{G1} to acquire a better conversion gain of mixer. Moreover, the dominant gain contributor of the proposed mixer is the input transconductance stage M_1–M_2. To obtain a sufficient gain, we must raise the dc current of M_1–M_2 since the transconductance g_m is proportional to the current of transistor. Although it will



$$Z_x = \frac{s^2 L_p (C_p + C_s) + 1}{sC_s (s^2 L_p C_p + 1)}$$

$$f_{image} = \frac{1}{2\pi\sqrt{L_p (C_p + C_s)}}$$

$$f_{wanted} = \frac{1}{2\pi\sqrt{L_p C_p}}$$

Fig. 3.5 A third-order notch filter reported in [37].

increase a small amount of dc power, the total dc power dissipation is still much smaller than previous circuits [32]-[35] made by the traditional Hartley or Weaver architectures.

3.2.2 Filter Design with Negative-Resistance Cells

Fig. 3.5 shows a third-order notch filter, which can provide low and high impedance at the image and wanted frequencies, respectively to effectively attenuate the image signal without deteriorating the in-band performance [37]. In this study, a differential dual-band image suppression circuitry based on the third-order notch filter topology is proposed and shown in Fig. 3.6 (a). In the following analyses, we utilize the half circuit in Fig. 3.6 (b) to facilitate the discussions. It is obvious that the parallel *L*-*C* section is inductive and capacitive at low and high frequencies, respectively; however, it is reversed for the series *L*-*C* section. If the resonance frequency is appropriately designed, the $0.5L_2$-$2C_2$ and C_3-$0.5L_3$ circuit in Fig. 3.6 (b) at low frequency such as 2.45 GHz can be equal to an inductor L_{tank} and a capacitor C_{series}

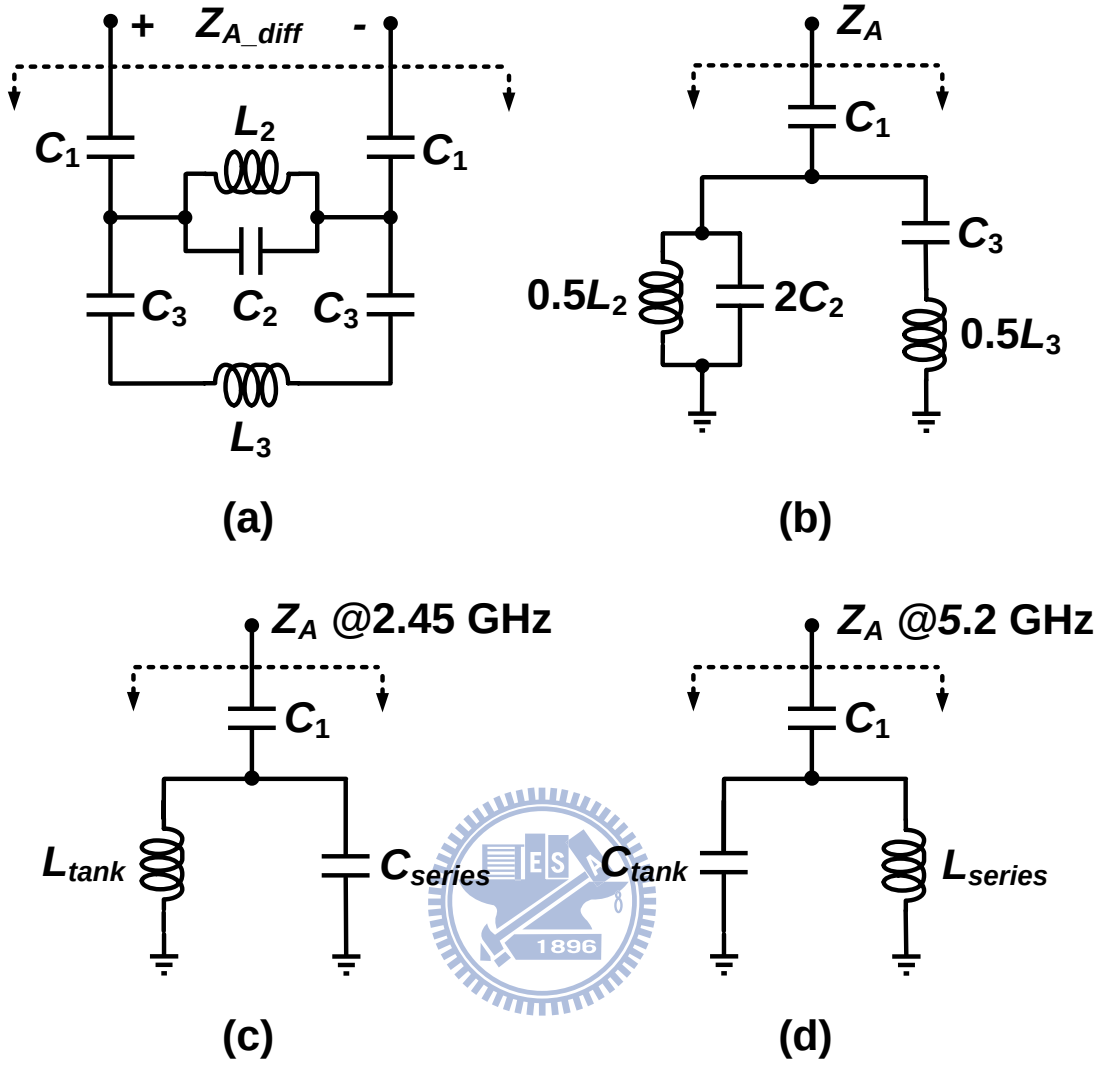


Fig. 3.6 (a) The proposed differential dual-band third-order notch filter. (b) The half circuit of (a). (c) Equivalent circuit at low frequency. (d) Equivalent circuit at high frequency.

shown in Fig. 3.6 (c). Similarly, Fig. 3.6 (d) can be acquired and comprehended by the above ratiocination. As a consequence, the proposed circuitry turns out to be the third-order notch filter in Fig. 3.5 at low and high frequencies simultaneously. After a straightforward derivation, the input impedance of the filter is given by

$$Z_A = \frac{s^4 0.25B(C_1 + 2C_2) - s^2(0.5L_2C_1 + A) + 1}{sC_1[s^4 0.5BC_2 - s^2 A + 1]} \tag{3.1}$$

where $A=L_2C_2+0.5L_2C_3+0.5L_3C_3$, $B=L_2L_3C_3$, from which two zeros and two poles can be obtained in the positive frequency domain to provide low impedance at dual image frequencies and high impedance at dual wanted frequencies, respectively.

The proposed differential dual-band third-order notch filter can be utilized for the 2.45/5.2 GHz WLAN application. However, it should be taken into account that the maximum attenuation of the image rejection filter is restricted by the series resistance of on-chip inductor. To overcome this limitation, the negative-resistance cell by using cross-coupled transistors can be employed to improve the Q value of on-chip inductor. In this study, the cross-connected pair consisted of NMOS and PMOS transistors as a negative conductance generator is used and shown in Fig. 3.7. Power consumption and the usage of inductors can be cut in half compared to the traditional approach while providing the same negative conductance. The dc current path will be provided by the on-chip inductor and the impedance Y_{IN} can be expressed as

$$Y_{IN} \approx \frac{1}{j\omega L_3} + j\left(\frac{C_{gsn3}C_{gsp3}}{C_{gsn3}+C_{gsp3}}\right) + \frac{R_{S3}}{(\omega L_3)^2} - \frac{g_{mn3}g_{mp3}}{g_{mn3}+g_{mp3}} \tag{3.2}$$

As can be seen in (3.2), sufficient negative resistance can be generated to eliminate R_{S3} by adjusting the bias voltage V_{dd} since the $g_{mn,p}$ is proportional to the current of transistors. It is obvious that the negative resistance facilitates to improve the maximum attenuation of the image rejection filter, but an overlarge value will bring about stability problem. A trade-off between the image rejection performance and stability should be carefully considered so as to make an optimum design. To avoid stability problem in this design, the negative resistor must be smaller than the series resistance of on-chip inductor. On the other hand, the process variation and temperature will influence the bias currents of the transistors to further deteriorate the

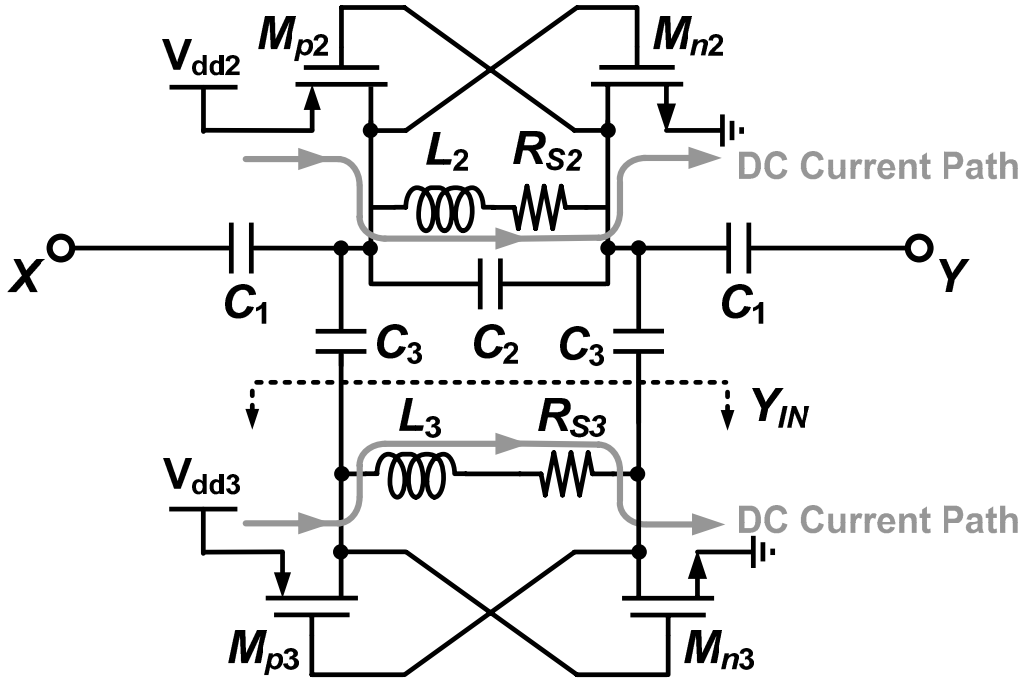


Fig. 3.7 The proposed differential dual-band notch filter with the negative-resistance cells consisted of NMOS and PMOS transistors.

filter performance, the externally controlled and adjustable bias voltages Vdd2 and Vdd3 are required to compensate for the process variation and temperature.

Based on the third order notch filter topology, the input impedance Z_{A_diff} of the proposed dual-band notch filter can also provide larger impedance in the both operation bandwidth (i.e., 2.4~2.48 and 5.15~5.35 GHz) to avoid the in-band signal at nodes *X* and *Y* having a leakage path to the proposed filter port and deteriorating the in-band performance. $Z_{XY\ without\ filter}$, as shown in Fig. 3.8, is the impedance between nodes *X* and *Y* without including the proposed notch filter, and the values at 2.45 and 5.2 GHz are 33 and 29 Ohm, respectively. The values of the impedance Z_{A_diff} at 2.4~2.48 and 5.15~5.35 GHz are more than 300 and 200 Ohm, and much larger than the input impedance $Z_{XY\ without\ filter}$. This means that the existence of the proposed notch filter in the dual-band operation frequencies will have no influence on the impedance between nodes *X* and *Y*, as can be observed from Fig. 3.8.

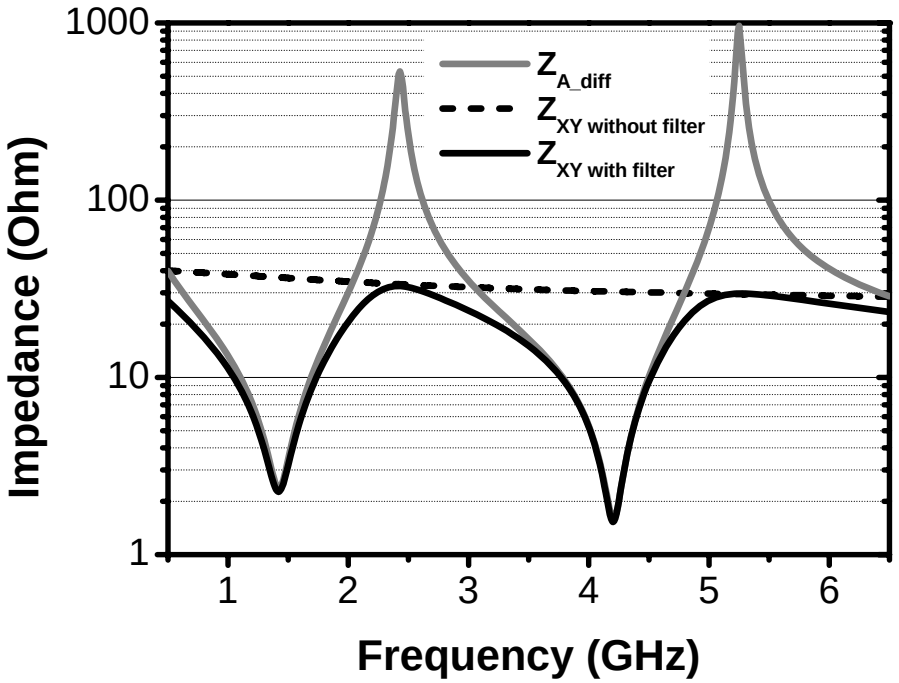


Fig. 3.8 The proposed notch filter in the dual-band operation frequencies has no influence on the impedance between nodes *X* and *Y*.

Consequently, the proposed dual-band image rejection mixer can achieve the sufficient image rejection without worsening the in-band characteristics.

3.3 EXPERIMENTAL RESULTS

The dual-band mixer chip with image rejection function was mounted on an FR4 test board for the measurement and the dc power dissipation was 10 mW. The simulated and measured results of input return loss are better than 10 dB in the operation bandwidth as depicted in Fig. 3.9. However, a non-negligible difference between simulation and measurement is obviously existent. We suppose that the bond-wire effect may cause the notch frequency drift because the dual-band mixer chip is mounted on an FR4 test board for the measurement. It can be demonstrated that the notch frequency will be affected due to the input bond wire; therefore, the

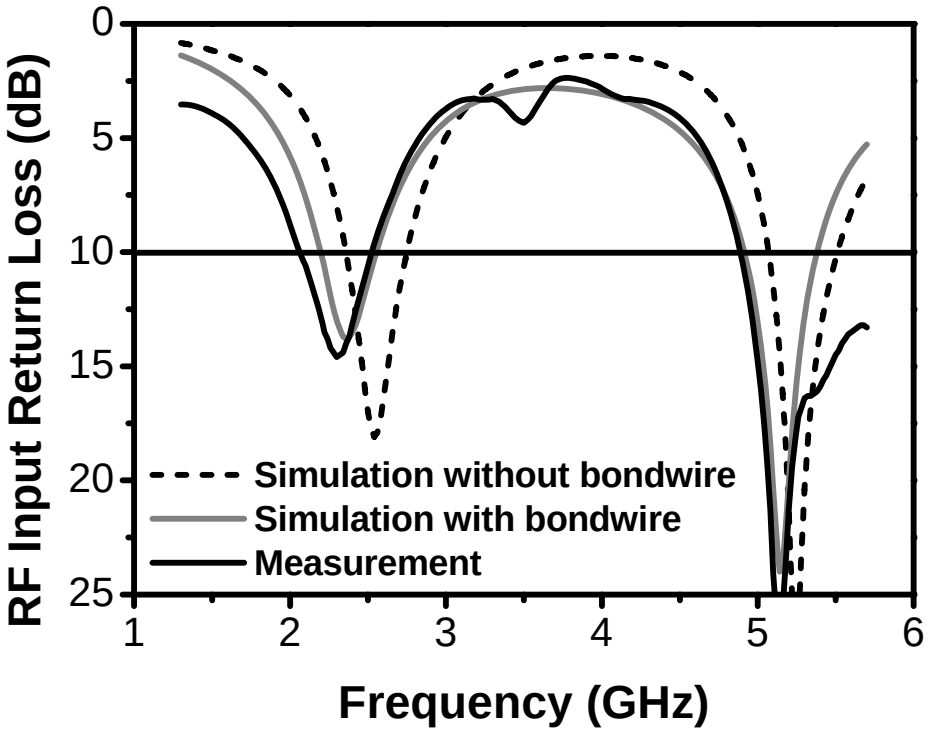


Fig. 3.9 Measured and simulated RF return loss of the proposed mixer.

length of bond wire must be as short as possible. On the other hand, as shown in Fig. 3.10, the measured conversion gain at RF = 2.45/5.2 GHz is 10.5/11 dB for IF=500 MHz and LO = 1.95/4.7 GHz. The maximum image rejection is 37 dB and 47 dB respectively. The measured minimum single sideband (SSB) noise figure at RF = 2.45/5.2 GHz is about 10/13 dB. The two-tone test with 10 MHz tone separation was performed using two Agilent 83640B signal generators and an Agilent 8564EC spectrum analyzer. The measured results of input-referred 1-dB compression point (IP_{1dB}) and input-referred third-order intercept point ($IIP3$) are depicted in Fig. 3.11. The values of the measured IP_{1dB} and $IIP3$ are -17/-16 dBm and -4.9/-5.2 dBm when RF=2.45/5.2 GHz. A die micro-photograph of the mixer proposed is shown in Fig. 3.12 with die area including pads of 1.07×1.07 mm^2.

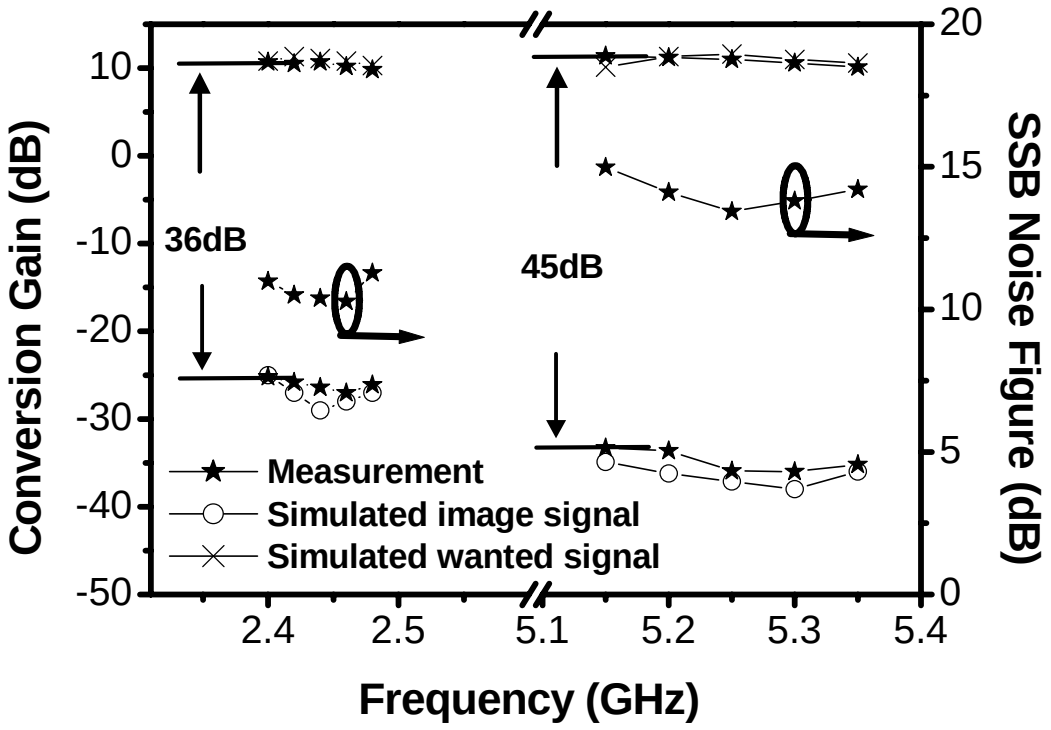


Fig. 3.10 Conversion gain and noise figure of the proposed mixer.

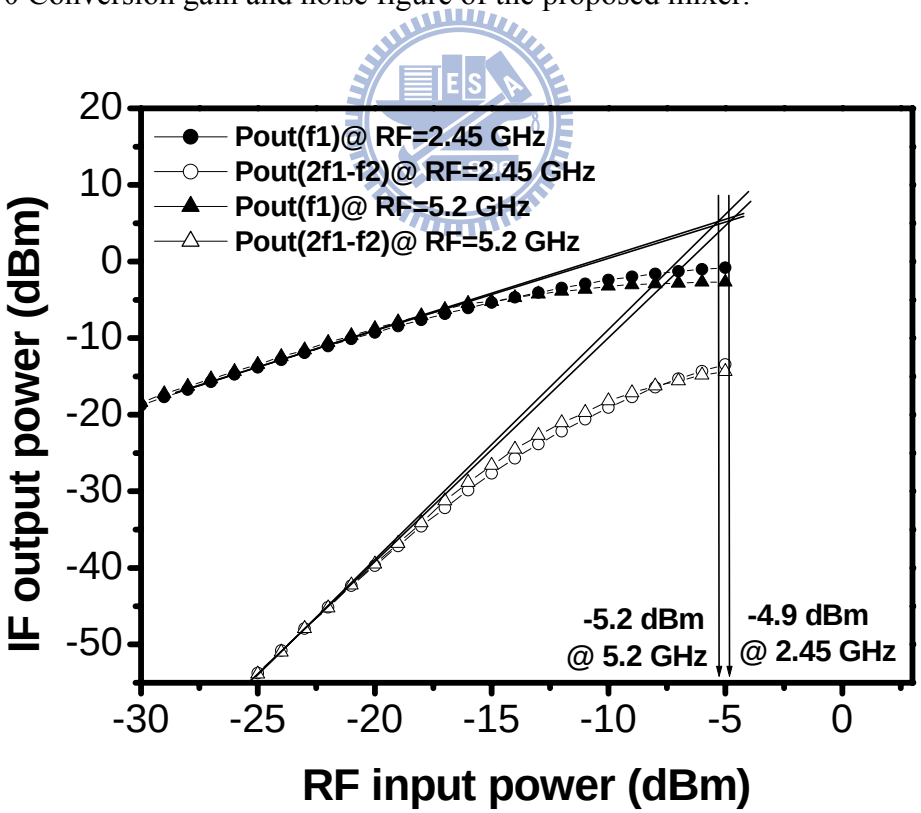


Fig. 3.11 Measured results of fundamental output power and IM3 for the proposed mixer with RF input frequency spacing of 10 MHz.

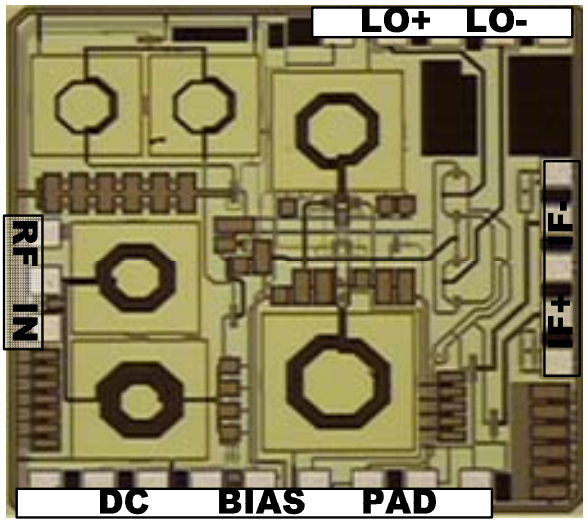


Fig. 3.12 Microphotograph of the mixer. Die area is 1.07×1.07 mm^2.

3.4 SUMMARY

A 2.45/5.2 GHz image rejection mixer with differential dual-band third-order notch filter has been fabricated and designed. The suppression of about 36/45 dB at the image frequencies can be achieved without worsening the in-band characteristics. In this study, the dc power consumption and chip area are smaller than the literature presented in [32]-[35] due to the reduction in the complexity of image rejection circuit mechanism. The presented mixer is compared with recently published mixers and summarized in Table 3.1.

Table 3.1

Comparison with previously published mixers

Item	This work	[31]	[32]	[33]	[34]	[35]
RF (GHz)	5.2/2.45	8 / 4	5.2	5.25	5.7/5.2	5.7/2.4
Gain (dB)	11/10.5	-14/-8	11	14	18.5/20	8/9
IP_{1dB} (dBm)	-16/-17	-	-17	-18	-15/-15	-13/-11
IRR (dB)	45/36	N/A	40	40	44/48 *	40/40
P_{diss} (mW)	10	81	150	58	-	126
Area (mm^2)	1.2	2	7.5	4	5	4
IRR Architecture	Notch Filter	N/A	Weaver	Weaver	Weaver	Weaver-Hartley
Tech.	0.18μm CMOS	0.18μm CMOS	2μm GaInP/ GaAs HBT	0.18μm CMOS	2μm GaInP/ GaAs HBT	0.18μm CMOS

* only at 5.7 and 5.2 GHz, not in the whole operation bandwidth

CHAPTER 4

ANALYSIS OF WIDE-BAND LOW NOISE AMPLIFIER WITH OUT-BAND REJECTION

4.1 INTRODUCTION

UWB systems realize high data rate in the short-range wireless transmission, which are suitable for integration in various consumer electronics such as PCs, cellular phones, digital cameras, and personal digital assistants. The minimum received power in the UWB channel is 47 and 67 dB, in the worst case, lower than those of the wireless local area network interferer powers at 5.2 and 2.4 GHz, respectively [38]. In addition, a tone is measured at 1.87 GHz in a smart-phone currently on the market, and the power level is 35 dB higher than the UWB signal [39]. All of these interferers, as shown in Fig. 4.1, have a harmful effect on the received UWB signal; especially they can lead to the receiver gain compression and their possible intermodulation products can fall in-band. Although the interferers may further be attenuated by the baseband filter in the receiver, this does not address the problems of the intermodulation distortion and the receiver gain desensitization. In order to achieve reasonable performance for the above considerations, as summarized in Table 4.1, more than 10 dB attenuation over the bandwidth of each interferer with 20 dB peak attenuation is appropriate in the front-end [40]-[44]. On the other hand, a larger attenuation in the front-end also can relax the baseband filter achieving an implementation with the smaller group delay variations and lower dc power consumption [42].

Recently, a design of multiple-stopband filters is presented for the suppression of

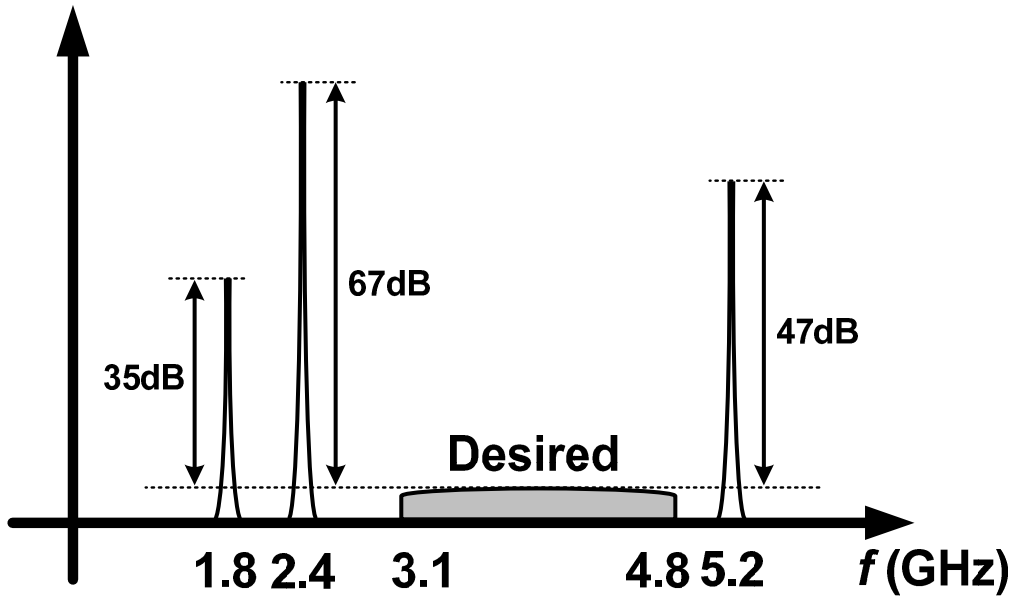


Fig. 4.1 Spectrum of the UWB system with large interferers.

Table 4.1
NOTCH FILTER SPECIFICATIONS

Standard	Notch center freq. (GHz)	10 dB attenuation bandwidth (GHz)	Peak attenuation (dB)
GSM-1800/1900	1.85	1.71~1.99	> 20
802.11b/g	2.44	2.4~2.48	
802.11a	5.25	5.15~5.35	

interfering signals such as Global System for Mobile (GSM), WLAN, and WIMAX in UWB applications [40]. The coupled resonator stopband filter sections with bent resonators were adopted in order to more effectively suppress harmonics and the maximum rejection is about 25 dB at 1.8 GHz. However, this prototype of filter which was fabricated on the basis of the standard PCB process will increase the whole UWB system area. Moreover, the multiple receivers with equal-gain combining were employed to eliminate the narrowband interferers received in the two paths and combined out-of-phase to cancel each other by selecting the optimal LO phase [41]. A maximum 28 dB attenuation of the interferers was measured but it is unavoidable to

increase the system's complexity.

On the other hand, the topologies utilized for wideband amplifiers generally include the distributed configuration [45]–[46], resistive shunt-feedback structure [47]–[49], common-gate $1/g_m$ termination [50]–[52], and *LC* input network [53]–[54]. The distributed amplifiers are attractive for their ultra-wide bandwidth; however, the major drawbacks are the large area and high dc power consumption, which make them unsuitable for many applications. The resistive shunt-feedback and common-gate $1/g_m$ amplifiers can provide good impedance matching and moderate gain while dissipating small amounts of dc power but without the out-band rejection capability. Recently, a new topology of the broadband amplifier for out-band rejection, which adopted a notch filter circuit with negative-resistance cell embedded, has been reported in [26], [55]. Inevitably, the extra notch filter circuit made of inductors and cross-coupled transistors will occupy additional chip area and dc power simultaneously.

In this chapter, three low-power UWB LNAs using 0.18-μm CMOS technology are presented. In the first UWB LNA, a new wideband input impedance-matching network, which is based on the *LC* structure with focus on the improvement of out-of-band rejection capability, is presented. By suitably introducing two additional capacitors in the traditional *LC* input network, two transmission zeros at 1.8 GHz and 8.5 GHz are generated to achieve the out-band rejection property while without suffering from deterioration of the in-band performance.

As an improvement of the first approach, the second proposed UWB LNA introduces a capacitive feedback path to the input *LC* network for further enhancing the rejection capability at the lower band transmission zero (1.8 GHz). A maximum 32 dB improvement is attained due to the usage of a feedback capacitor. Also, a dual-band notch filter made of active inductors, which occupies only a small chip area,

is employed after the LNA core so as to attenuate the WLAN interferers at 2.4 GHz and 5.2 GHz while without influencing the noise figure of the LNA. The proposed active inductors are designed based on the cascode gain-boosting stage with a feedback resistor, which are with low consumption power while maintaining a sufficient Q value. The introducing of both the feedback capacitor and the dual-band notch filter achieves maximum rejections of about 50 dB on the out-band interferers, which is superior than those presented in the literature [26], [40]–[41], and [55].

After improving the out-band rejection capability, a new matching technique is presented to further ameliorate the noise figure performance in the third UWB LNA. The proposed broad-band input match can be acquired easily by selecting an appropriate width of the transistor, which will effectively avoid the usage of the low-Q on-chip inductors in the input network. Moreover, this UWB LNA chip also demonstrates the feasibility of inter-stage resonator to accomplish bandwidth enhancement without additional power consumption. The IC prototype achieves good performances such as a power gain of 16.2 dB, a better than 10 dB input return loss, and 2.3 dB minimum noise figure while consuming a dc power of only 6.8 mW. In this chapter, the circuit simulation is performed via Agilent's Advanced Design System (ADS) software with a TSMC design kit.

4.2 WIDE-BAND LOW NOISE AMPLIFIER WITH OUT-BAND REJECTION INPUT NETWORK

The first 3-to-5 GHz CMOS UWB LNA proposed here adopts a source-degenerated cascode configuration as shown in Fig. 4.2. An LC input network for wideband operation is utilized, with two new capacitors C_{RH} and C_{RL} for

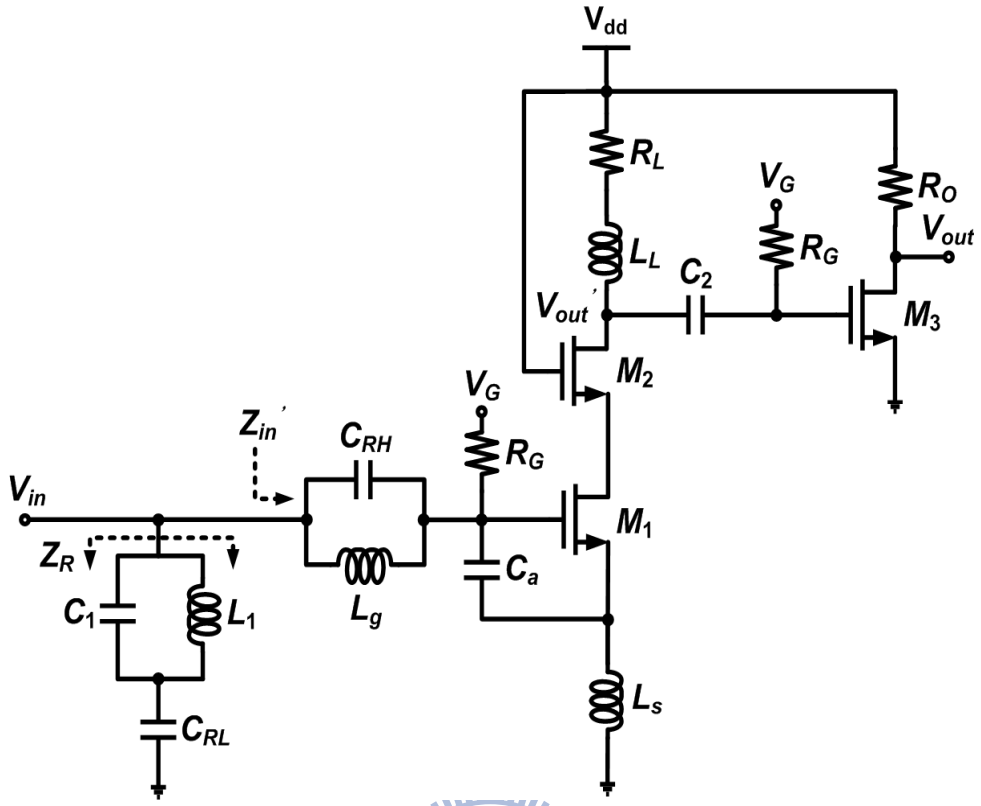


Fig. 4.2 Complete schematics of the first UWB LNA with out-band rejection.

increasing the higher and lower out-band rejections, respectively. The load inductor L_L in series with the resistor R_L helps to enhance the gain flatness. The buffer transistor M_3 with a purely resistive load R_O is employed for testing purposes.

4.2.1 Circuit Design and Analysis

4.2.1.1 Power Gain

The overall gain of the proposed LNA can be easily obtained as follows after a straightforward derivation:

$$S_{21} = \frac{(1+S_{11})v_{out}}{v_{in}} = (1+S_{11})\frac{v_{out}'}{v_{in}} \cdot g_{m3}(R_o // Z_0) \tag{4.1}$$

where

$$\frac{v_{out}'}{v_{in}} = \frac{g_{m1}\left(1-\omega^2 L_g C_{RH}\right)}{\chi(\omega)} \cdot \left[\left(R_L + j\omega L_L\right) // \frac{1}{j\omega C_L} \right] \tag{4.2}$$

with

$$\begin{aligned} \chi(\omega) = {} & \omega^4 L_g L_s C_t C_{RH} - j\omega^3 L_g L_s g_{m1} C_{RH} - \\ & \omega^2 \left(L_g C_t + L_g C_{RH} + L_s C_t\right) + j\omega g_{m1} L_s + 1 . \end{aligned} \tag{4.3}$$

Z_0 is the 50-Ω source resistance, C_t=C_{gs1}+C_a, and C_L is the total capacitance between the drain of the transistor M_2 and ground. S_{11} is the reflection coefficient at the input port. From (4.1) it is seen that, extra transmission zeros (i.e., S_{21} = 0) can be created when the following conditions are satisfied:

$$S_{11} = -1 \quad \text{or} \quad \frac{v_{out}'}{v_{in}} = 0 \ , \tag{4.4}$$

in which S_{11} = -1 means that the input impedance of the LNA is short circuit, and it occurs as the impedance Z_R, i.e., the impedance of the L_1C_1 tank in series with the capacitor C_{RL} (see Fig. 4.2), is equal to zero, where

$$Z_R(\omega) = \left[1-\omega^2 L_1\left(C_{RL}+C_1\right)\right] \Big/ j\omega C_{RL}\left(1-\omega^2 L_1 C_1\right) . \tag{4.5}$$

By using (4.4), (4.2) and (4.5), the locations of transmission zeros can be predicted as

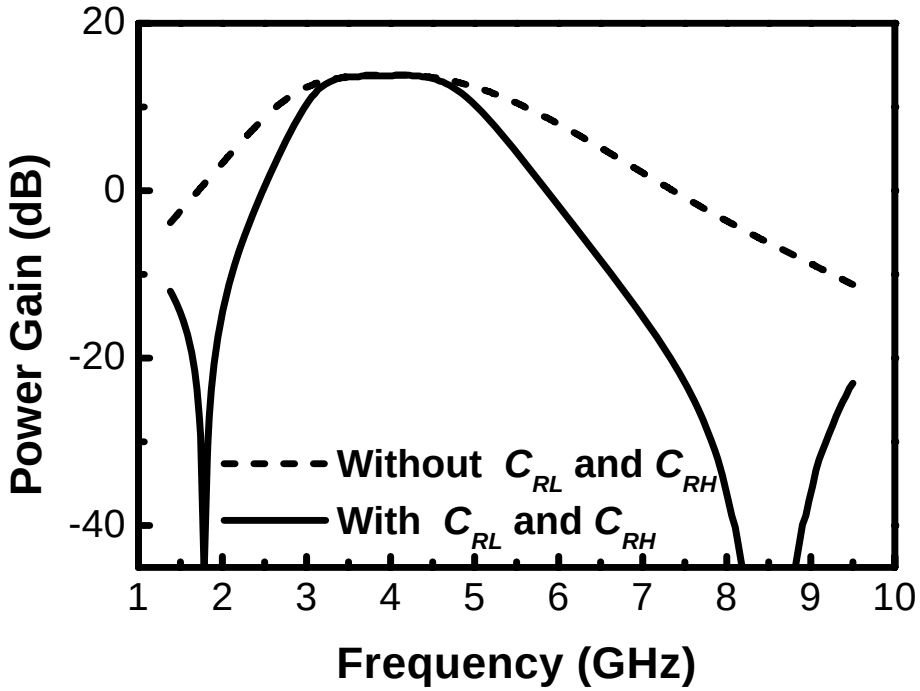


Fig. 4.3 Simulated ideal power gain with and without out-band rejection improvement.

$$\omega_{RH} = 1/\sqrt{L_g C_{RH}} \ , \quad \omega_{RL} = 1/\sqrt{L_1 (C_{RL} + C_1)} \ . \tag{4.6}$$

The design criterion of the out-band rejection function can be derived from (4.6) with two transmission zeros at 1.8 and 8.5 GHz determined by the capacitors C_{RH} and C_{RL}, as shown in Fig. 4.3.

4.2.1.2 Input-Matching Analysis

As shown in Fig. 4.2, the input impedance Z_{in} of the proposed LNA equals the impedance Z_R of the L_1C_1-C_{RL} circuit in shunt with the impedance Z_{in}' of the remaining circuit. The L_1C_1-C_{RL} circuit provides a series resonance at ω_{RL} and a parallel resonance at ω_0, where, from (4.5),

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} \ . \tag{4.7}$$

On the other hand, the impedance $Z_{in}^{'}$ of the remaining circuit can be derived as

$$Z_{in}^{'}(\omega) = \omega_T L_s - j\frac{1-\left(\omega/\omega_0^{'}\right)^2}{\omega C_G} \tag{4.8}$$

where

$$\omega_T = g_{m1}/C_G \tag{4.9}$$

and

$$\omega_0^{'}(\omega) = \frac{1}{\sqrt{\left(L_s + L_g^{'}\right)C_G}} \tag{4.10}$$

with $C_G = C_{gs1} + C_a$, and $L_g^{'} = L_g/[1-(\omega/\omega_{RH})^2]$ (which is a frequency dependent inductance). It can be seen that $L_g^{'} \approx L_g$ in the desired frequency range, since $\omega << \omega_{RH}$. Note that since $L_g^{'}(\omega_{RH}) \rightarrow \infty$, $\omega_0^{'}(\omega_{RH}) = 0$. This means that the impedance $Z_{in}^{'}$ shown in (4.8) exhibits a parallel resonance at ω_{RH}, which prevents the input signal from entering the transistors and thus produces a transmission zero of the amplifier.

From (4.8), $\omega_0^{'}$ is the series resonant frequency of $Z_{in}^{'}$, whose value is frequency dependent and is designed equal to the parallel resonant frequency ω_0 of the L_1C_1-C_{RL} circuit at ω_0, or

$$\omega_0^{'}(\omega_0) \cong \frac{1}{\sqrt{\left(L_s + L_g\right)C_G}} = \omega_0 \ . \tag{4.11}$$

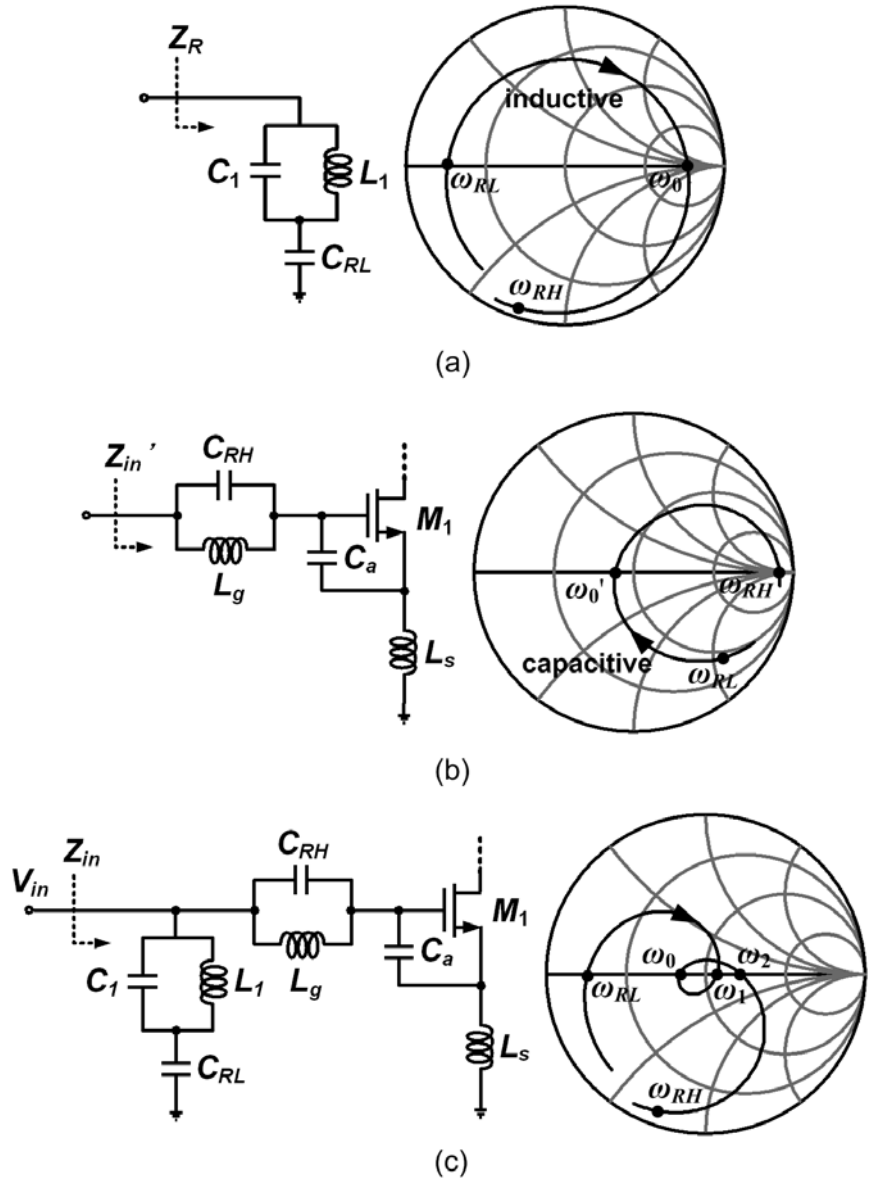


Fig. 4.4 Input reflection coefficients on the Smith chart for (a) the L_1C_1-C_{RL} circuit with impedance Z_R, (b) the narrow-band input network with impedance Z_{in}', and (c) the total circuit with impedance Z_{in}.

As a consequence, the input impedance Z_{in} at the center frequency ω_0 can be written as

$$Z_{in}(\omega_0) = Z_{in}'(\omega_0) = Z_{in}'(\omega_0') = \omega_T L_s \ . \tag{4.12}$$

Fig. 4.4 (a), (b), and (c) show the frequency behaviors on the Smith chart of the impedances Z_R, Z_{in}', and Z_{in}, respectively. In the frequency range from ω_{RL} to ω_0, Z_R is

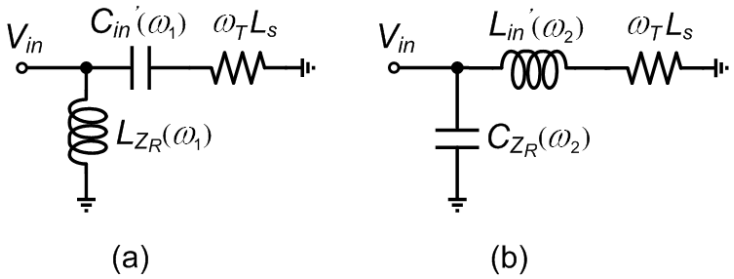


Fig. 4.5 Equivalent circuits for the broad-band input network at (a) the parallel resonance frequency ω_1 and (b) the parallel resonance frequency ω_2.

inductive and Z_{in}' is capacitive; while in the range from ω_0 to ω_{RH}, they are reversed. Thus, two additional *LC* parallel resonances, as shown in Fig. 4.4 (c), are produced in the LNA circuit, one occurred at a frequency (ω_1) before the center frequency ω_0, and one (ω_2) after that. Using (4.5) and (4.8), the equivalent circuit of the LNA at ω_1 and ω_2 can be derived as shown in Fig. 4.5 (a) and (b), respectively. $L_{ZR}(\omega_1)$ and $C_{in}'(\omega_1)$ are correspondingly the equivalent inductance of Z_R and capacitance of Z_{in}' at ω_1:

$$L_{ZR}(\omega_1) = \frac{1/\omega_{RL}^2 - 1/\omega_1^2}{C_{RL}\left[1-(\omega_1/\omega_0)^2\right]} \tag{4.13}$$

$$C_{in}'(\omega_1) = \frac{1}{\left(L_s + L_g'\right)\left(\omega_0^2 - \omega_1^2\right)}\ , \tag{4.14}$$

and $C_{ZR}(\omega_2)$ and $L_{in}'(\omega_2)$ are capacitance of Z_R and inductance of Z_{in}' at ω_2:

$$C_{ZR}(\omega_2) = \frac{C_{RL}\left[(\omega_2/\omega_0)^2 - 1\right]}{(\omega_2/\omega_{RL})^2 - 1} \tag{4.15}$$

$$L_{in}'(\omega_2) = \frac{L_s + L_g'}{1-(\omega_0/\omega_2)^2}\ . \tag{4.16}$$

Using Fig. 4.5, the input impedance Z_{in} of the amplifier at ω_1 and ω_2 are obtained:

$$Z_{in}(\omega_1) = \frac{L_{Z_R}(\omega_1)}{\omega_T L_s C_{in}'(\omega_1)} \tag{4.17}$$

and

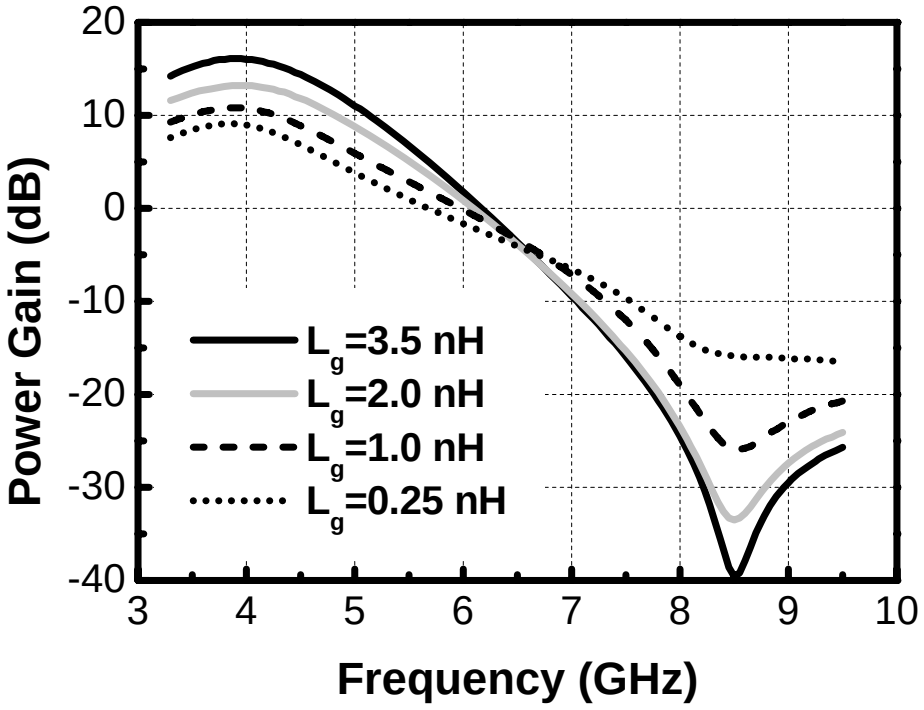
$$Z_{in}(\omega_2) = \frac{L_{in}'(\omega_2)}{\omega_T L_s C_{Z_R}(\omega_2)} \quad . \tag{4.18}$$

Due to the presence of the additional LC resonances at ω_1 and ω_2, a loop surrounding the 50-Ω matching point is formed on the Smith chart as shown in Fig. 4.4 (c). As we will see, a broad-band input-matching in the intended frequency range can be acquired by devising appropriately the input impedances $Z_{in}(\omega_1)$ and $Z_{in}(\omega_2)$.

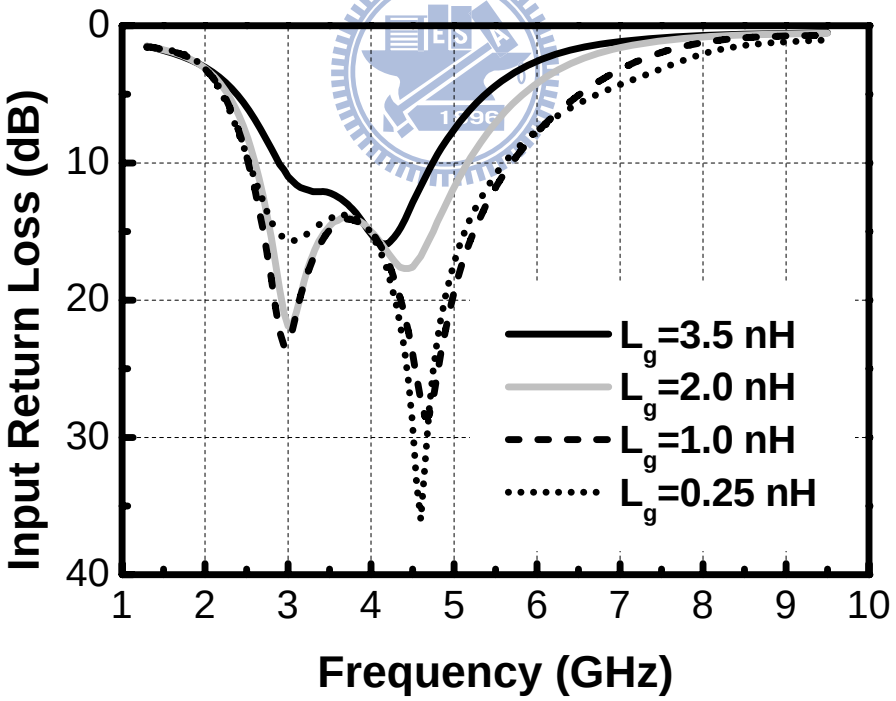
4.2.2 Optimum Out-Band Rejection

The above ratiocination reveals that the additional capacitors C_{RH} and C_{RL} will bring about two transmission zeros to ameliorate the out-band performance. Unfortunately, the out-band rejection characteristics are restricted by the series resistance of on-chip inductor. As seen from (4.6), the higher and lower out-band transmission zeros are associated with the inductors L_g and L_1, respectively. These component values influence not only the zeros' frequencies but also the out-band suppression levels as are to be shown below.

Fig. 4.6(a) shows the power gain (S_{21}) versus frequency with different values of L_g. To begin with, it can be anticipated that the higher-frequency out-band elimination efficiency is mainly determined by the impedance of $L_g C_{RH}$ tank at resonant frequency (i.e., the larger impedance, the superior out-band suppression). Therefore, the first



(a)



(b)

Fig. 4.6 (a) Simulated power gain (S_{21}) and (b) input return loss ($1/S_{11}$) for different values of L_g with L_1 = 2.0 nH, C_1 = 0.82 pF, and C_{RL} = 2.95 pF. The transmission zero ω_{RH} is kept constant.

step in the design criteria is to assign a larger L_g to arrive at a larger resonant impedance [22, Chapter 14]. In addition, a preferable power gain in the target frequency range can be procured contemporaneously by using a larger L_g, as shown in Fig. 4.6(a). However, (4.17) indicates that a smaller C_{in}' by raising the value of L_g will result in the increase of $Z_{in}(\omega_1)$ since the C_{in}' in (4.14) is inversely proportional to the L_g. Similarly, a larger L_g can be derived by (4.18) and (4.16) to augment $Z_{in}(\omega_2)$. In other words, an overlarge L_g will lead to over abounded input impedances $Z_{in}(\omega_1)$ and $Z_{in}(\omega_2)$ at ω_1 and ω_2, and thus, as shown in Fig. 4.6 (b), gradually decrease the input matching bandwidth of the LNA, which is not desirable for this design.

As is clear from (4.5), the impedance Z_R in Fig. 4.2 produces one series and one parallel resonance, from which the lower transmission zero can be created. It is expectable that a smaller impedance Z_R at the series resonant frequency will accomplish the superior out-band elimination efficiency. Fig. 4.7 shows the relation between the impedance Z_R and frequency for different L_1 values. As is seen, a smaller L_1 results in a smaller Z_R. Also as illustrated in the power gain versus frequency diagram of Fig. 4.8 (a), the smaller Z_R in turn causes a deeper suppression level at ω_{RL} (1.8 GHz) and is thus preferred for optimum lower-frequency out-band rejection. Nevertheless, a drawback which may make the design criteria unsatisfactory is that diminishing L_1 gradually decreases the impedance Z_R in the frequency range of interest. As a result, $Z_{in}(\omega_0) \approx Z_{in}'(\omega_0)$ in (4.12) is not satisfied and the input impedance $Z_{in}(\omega_0)$ will be less than $Z_{in}'(\omega_0)$. This phenomenon is able to generate the return loss of less than 10 dB at the center frequency to decrease the input matching characteristic of proposed LNA, as shown in Fig. 4.8 (b). Hence, it should be taken into account punctiliously by appointing the appropriate values of L_g and L_1 to achieve the trade-off between the input match and out-band rejection performances.

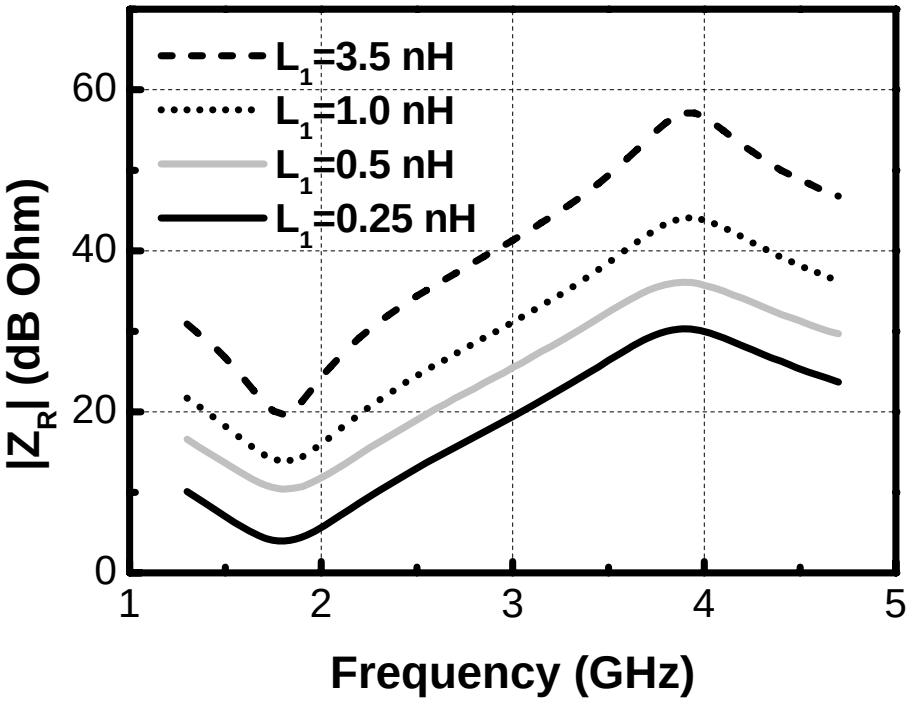
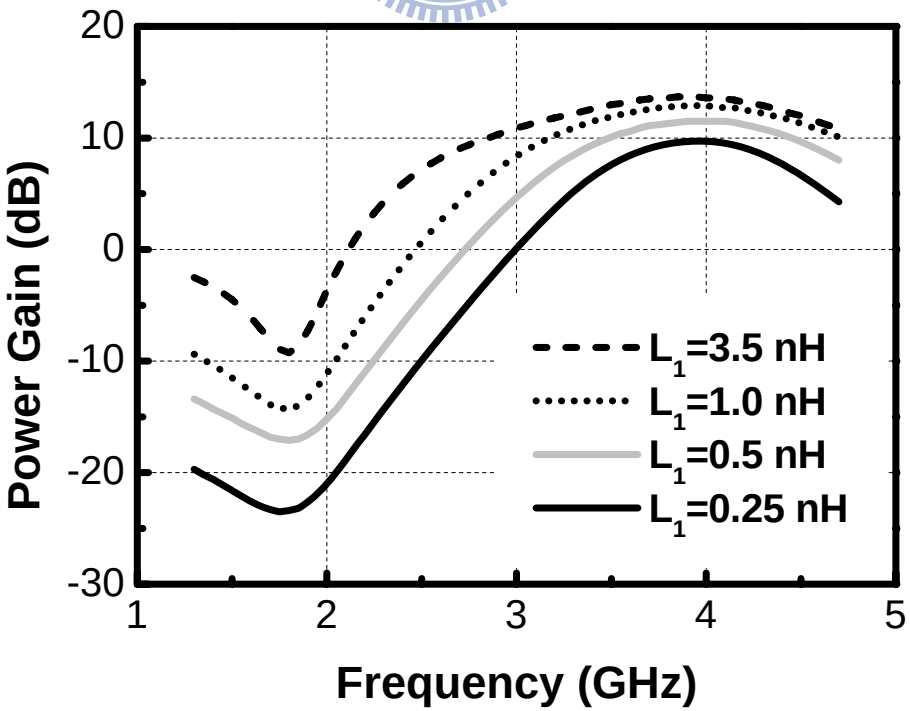
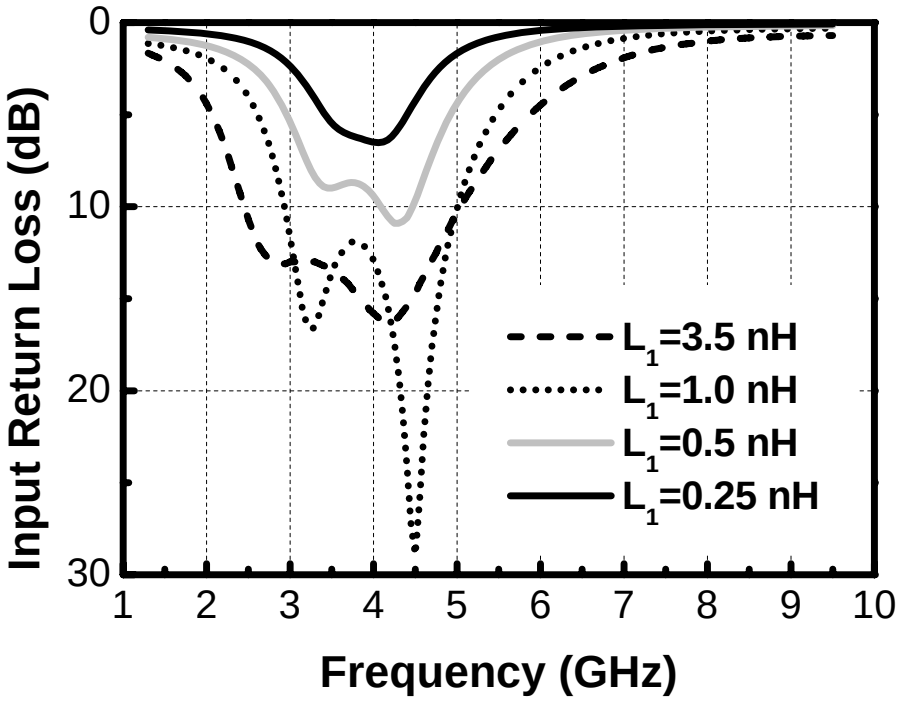


Fig. 4.7 The impedance Z_R versus frequency with different values of L_1. The transmission zero ω_{RL} is kept constant.



(a)



(b)

Fig. 4.8 (a) Simulated power gain (S_{21}) and (b) input return loss ($1/S_{11}$) for different values of L_1 with L_g = 2.0 nH, L_s = 0.5 nH, C_{RH} = 0.17 pF, and C_a = 0.23 pF. The transmission zero ω_{RL} is kept constant.

It is interesting to see the influence of the input network on the LNA's noise figure. After a straightforward derivation following the procedure in [18], the noise figure *NF* of the circuit shown in Fig. 4.2 can be obtained as:

$$NF \propto \left[1-\left(\omega/\omega_{RH}\right)^2\right]^{-2}\left[1-\left(\omega/\omega_{RL}\right)^2\right]^{-2}. \tag{4.19}$$

Obviously, the proposed UWB LNA will produce double-peak maxima in noise factor at the two transmission zeros. Consequently, it must be cautious to prevent from worsening the noise property in the desired frequency range when designing the locations of the zeros. Fig. 4.9 shows the simulation results of the noise figures due to the active gain stage (M_1+M_2) only, M_1+M_2 with the input network, and the total

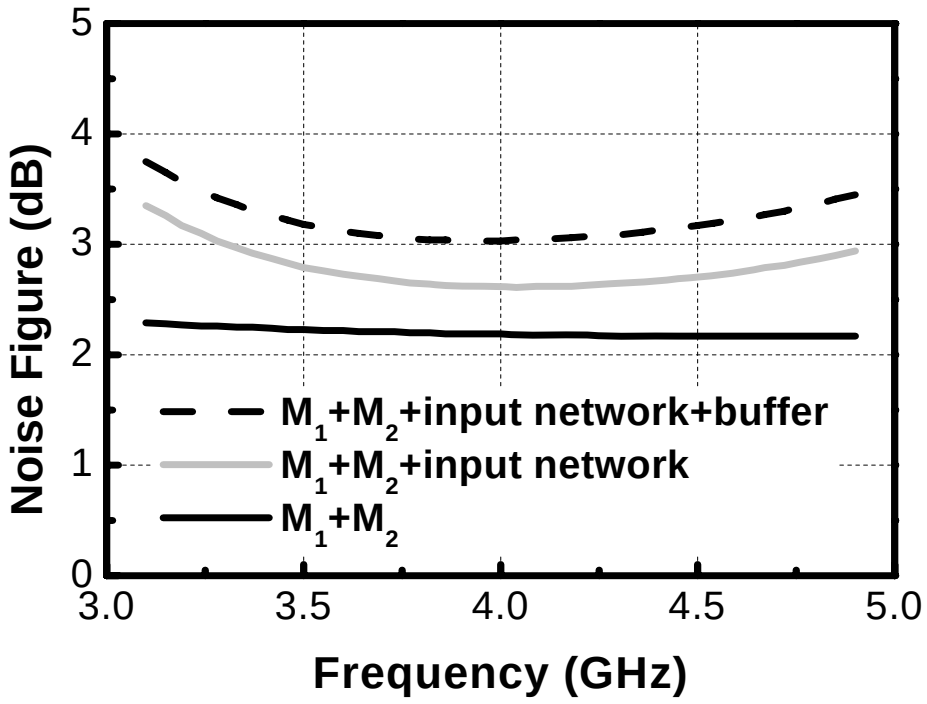


Fig. 4.9 Simulated noise figure of the first UWB LNA due to the active gain stages and the losses of the input network.

circuit. It can be observed that the dominant noise contributor is the active gain stage. The out-band rejection input network has minor influence on the total noise figure as long as the designed transmission zeros are not too close to the in-band. To reduce the noise contribution from the active gain stage, the width of the transistor M_1 will be chosen for optimum noise property [19].

4.2.3 Simulation and Experimental Results

For the first UWB LNA shown in Fig. 4.2, the width of the transistor M_1 (225 μm) is optimized with 2.5 mW power dissipation to achieve good noise property. The size of the cascode transistor M_2 (320 μm) is selected to be as large as possible to reduce its voltage headroom requirement, which is conducive to low-voltage operations. In addition, the design of input network will engender the trade-off

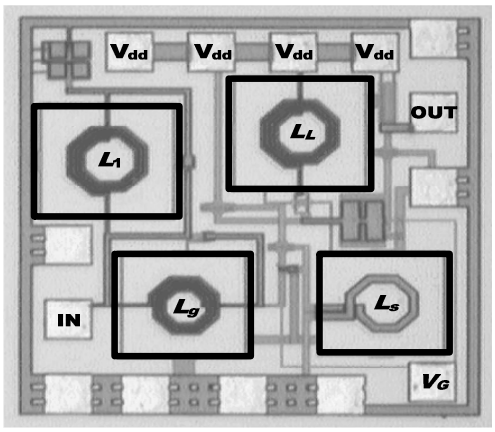


Fig. 4.10 Microphotograph of the fabricated UWB LNA. Die area is 0.78×0.8 mm^2.

between the input match and out-band rejection characteristics, which can be observed in Figs. 4.6 and 4.8. Hence, it should be chosen cautiously to obtain a reasonably out-band rejection performances in the target input matching bandwidth. In this study, the components values of the input network are $L_1 = 1.8$ nH, $L_g = 2.0$ nH, $L_s = 0.5$ nH, $C_1 = 0.91$ pF, $C_{RL} = 3.3$ pF, $C_{RH} = 0.17$ pF, and $C_a = 0.23$ pF. The load consists of the on-chip inductor L_L in series with the resistor R_L to achieve flat gain over the whole bandwidth. The components values of the load are $L_L = 2.4$ nH and $R_L = 15\ \Omega$. A die microphotograph of the first UWB LNA is shown in Fig. 4.10 and the die area including pads is 0.78×0.8 mm^2.

The first UWB LNA drew 2.8 mA dc core current from the 0.9 V supply voltage. The S-parameters of the designed LNA were measured using the Agilent 8510C vector network analyzer. The simulated and measured results of power gain and input return loss are depicted in Fig. 4.11. The measured peak gain is 11.5 dB with a 3-dB bandwidth of 3.4 GHz from 2.8 to 6.2 GHz and the input return loss is better than 8.7 dB in the operation bandwidth. Moreover, due to the addition of the capacitors C_{RH} and C_{RL}, extra transmission zeros are created and measured at 1.7 GHz and 10 GHz. The noise figure was measured using the Agilent N8975A noise figure analyzer

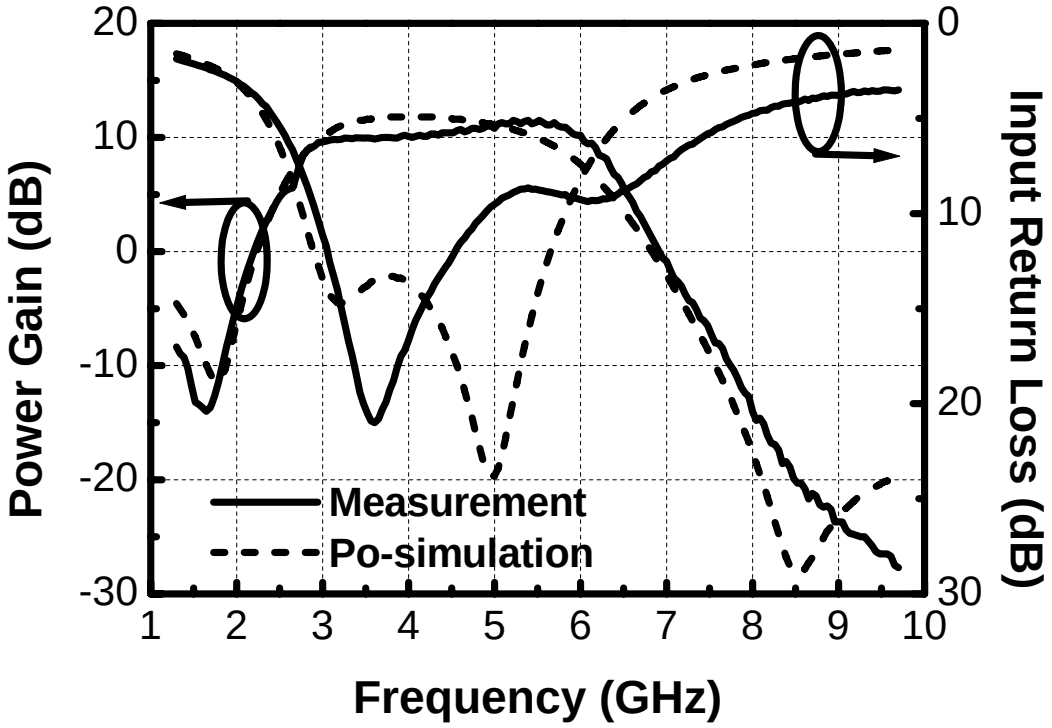


Fig. 4.11 Measured and simulated power gain (S_{21}) and input return loss ($1/S_{11}$) of the UWB LNA.

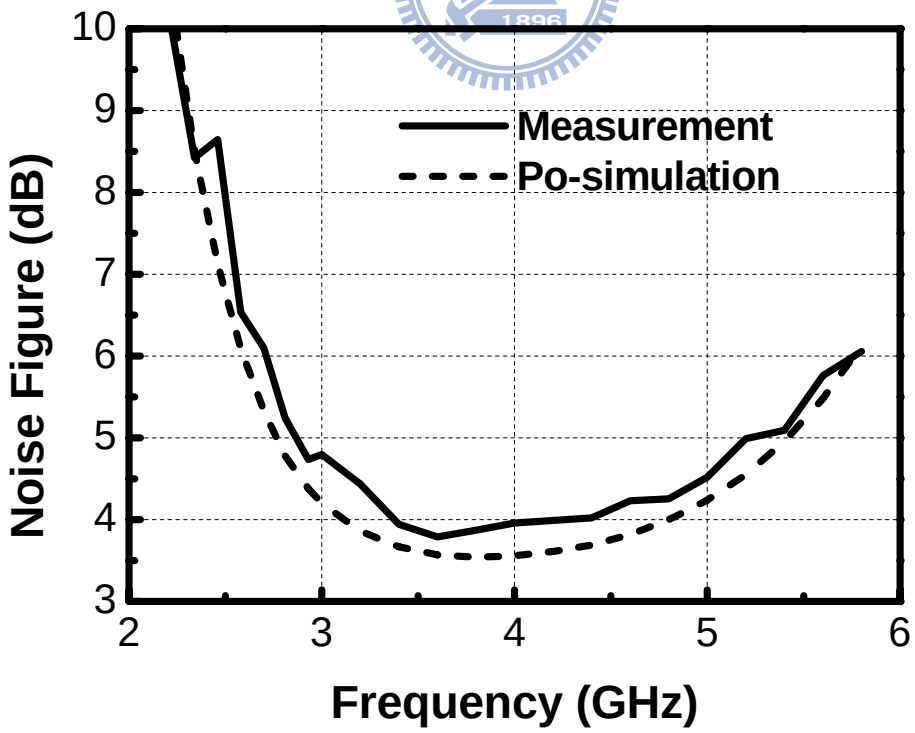


Fig. 4.12 Measured and simulated noise figure of the UWB LNA.

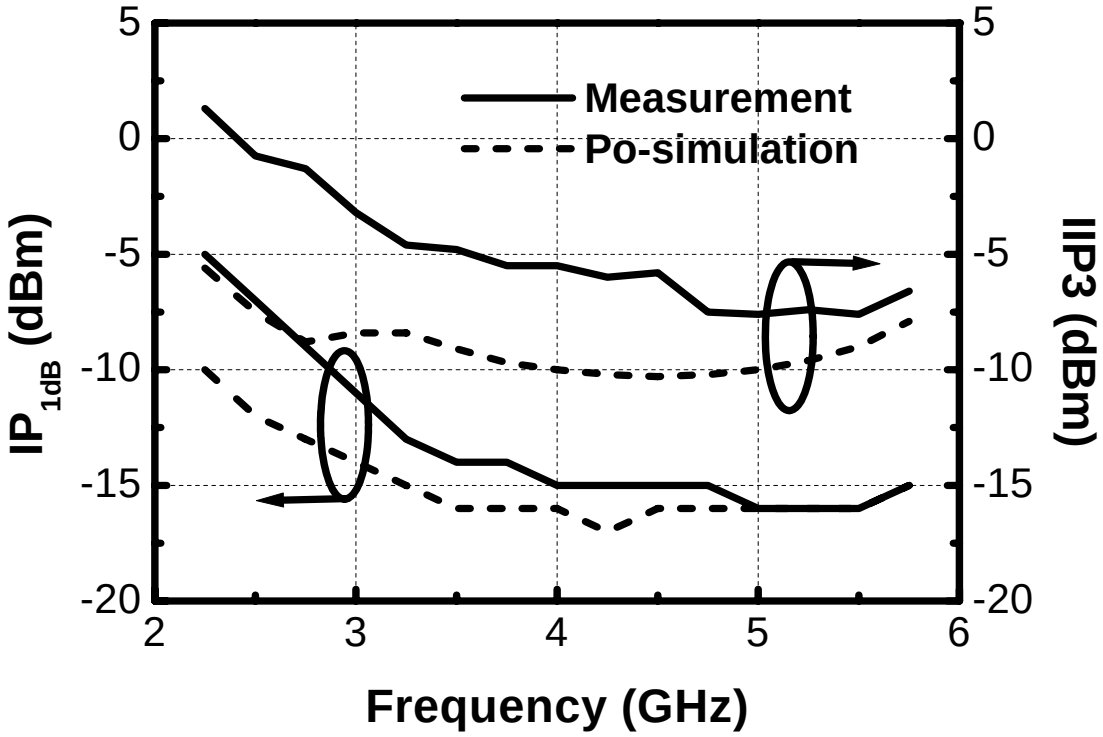


Fig. 4.13 Measured and simulated IP_{1dB} and IIP3 of the UWB LNA.

with Agilent 346C noise source. The simulated and measured noise figures at the same bias condition are depicted in Fig. 4.12. It is seen that the minimum value of the measured noise figure is equal to 3.8 dB at 3.6 GHz. The two-tone test with 10 MHz tone separation was performed using two Agilent 83640B signal generators and an Agilent 8564EC spectrum analyzer. The simulated and measured results of IP_{1dB} and IIP3 are depicted in Fig. 4.13. Minimum value of the measured IP_{1dB} and IIP3 are -16 dBm and -7.6 dBm respectively.

4.3 WIDE-BAND LOW NOISE AMPLIFIER WITH FEEDBACK STRUCTURE AND NOTCH FILTER

The first UWB LNA improves the higher and lower out-band performances by introducing the capacitors C_{RH} and C_{RL}. However, a trade-off between the input matching and out-band rejection should be carefully considered so as to make an optimum design. In the second approach, we utilize a feedback capacitor C_{FB} and active dual-band notch filter, as shown in Fig. 4.14, to attenuate the out-band interferers without deteriorating the input matching bandwidth.

4.3.1 Effect of Feedback Structure

The capacitor C_{RL} will engender the lower band transmission zero such as 1.8 GHz, but the rejection characteristic is restricted by the series resistance of on-chip inductor. For further suppression of the unwanted signal at 1.8 GHz, we introduce a feedback capacitor to the input LC network. As shown in Fig. 4.14, the voltage gain at node X is equal to -1 if appropriate device sizes of M_1 and M_2 are selected so that the ratio gm_1/gm_2 equals unity. This makes the signal at node X 180° out-of-phase with the input signal V_{in}. On the other hand, the L_1C_1 tank, which provides a parallel resonance at the in-band operation, behaves as an equivalent inductor at 1.8 GHz. Consequently, a suitably designed feedback capacitor C_{FB} in series with the equivalent inductor can produce a series resonance at 1.8 GHz so that the out-of-phase signal at X can be brought back to further cancel the input 1.8 GHz unwanted signal. In short, the L_1C_1 tank behaves like an open circuit in the in-band and thus has little influence on the input impedance, while it may introduce an out-of-phase feedback

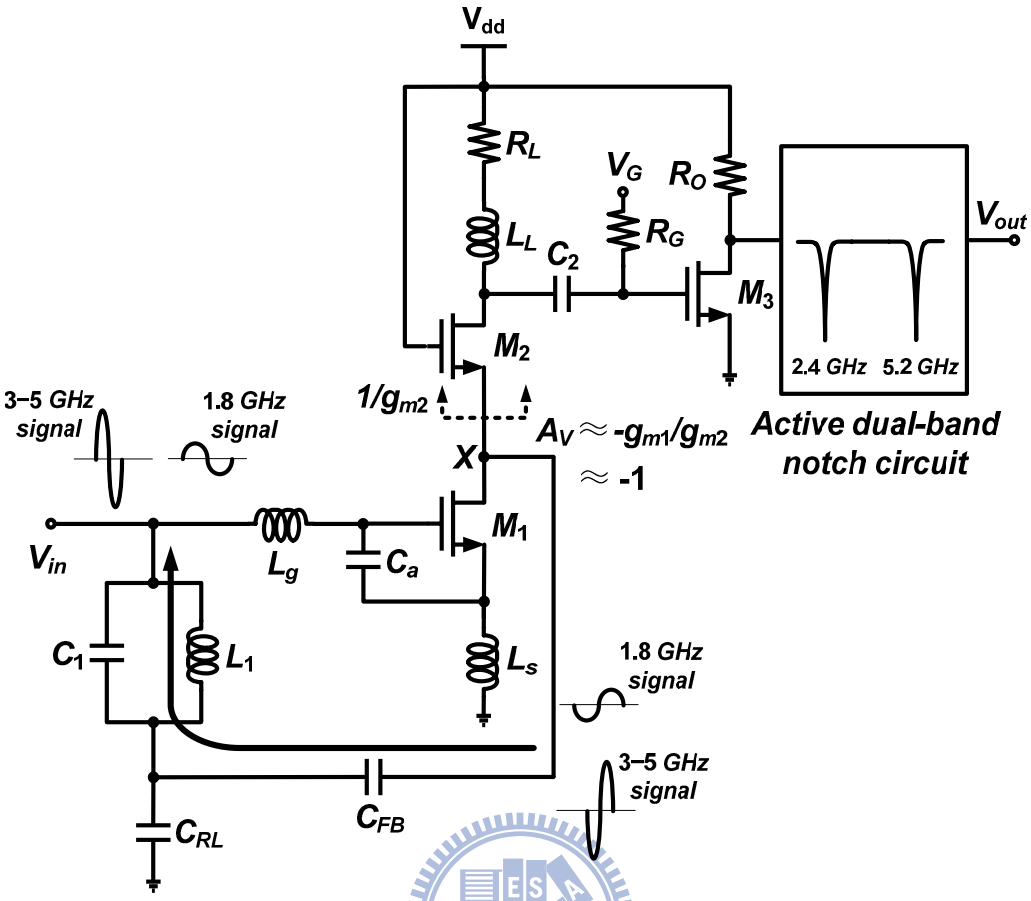


Fig. 4.14 Principle of the interferer-canceling technique with a feedback capacitor C_{FB} and active dual-band notch filter.

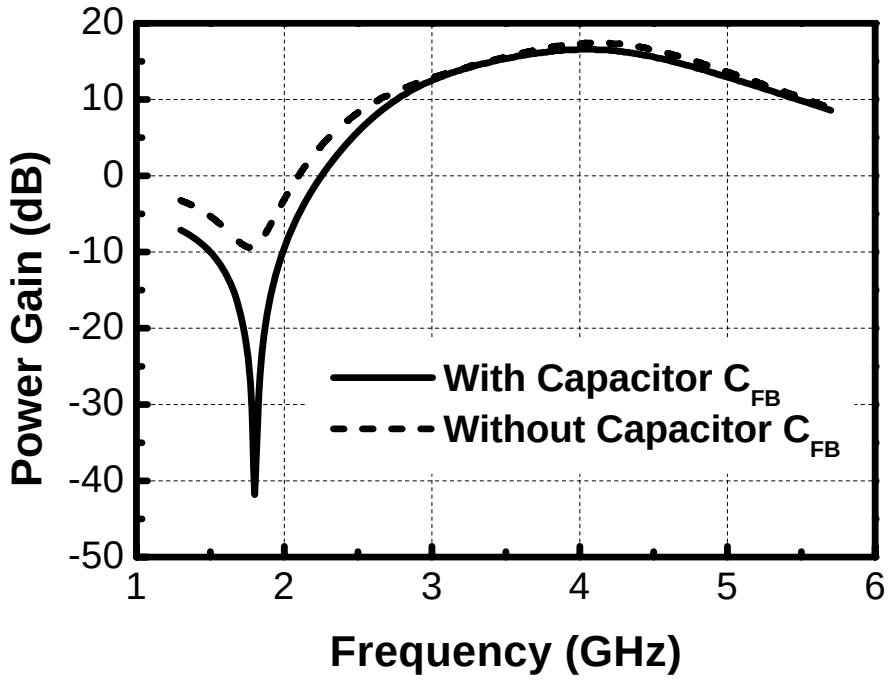


Fig. 4.15 Simulated power gain (S_{21}) with and without the additional capacitor C_{FB}.

signal to eliminate the unwanted 1.8 GHz signal. Fig. 4.15 shows the simulation results of the power gain with and without the additional capacitor C_{FB}. It can be observed and demonstrated that a maximum 32 dB decrease in power gain is attained at 1.8 GHz while maintaining an identical in-band characteristic.

4.3.2 Analysis of Dual-Band Notch Filter

An on-chip dual-band notch filter is to be placed before the output of the second LNA, as shown in Fig. 4.14. Here, to avoid the deterioration in noise figure due to the loss of this notch filter, the filter stage is chosen to place after the gain stage. Fig. 4.16 illustrates the schematic of the proposed dual-band notch filter. The impedance Z_A shown in the figure can be derived as

$$Z_A = \frac{\omega^4 L_3 C_3 L_4 C_4 - \omega^2 (L_3 C_3 + L_3 C_4 + L_4 C_4) + 1}{j\omega C_3 [(1 - \omega^2 (L_3 + L_4) C_4]} \quad . \tag{4.20}$$

The notch frequencies of the filter can be obtained by letting the numerator equal null, or

$$\omega^4 L_3 C_3 L_4 C_4 - \omega^2 (L_3 C_3 + L_3 C_4 + L_4 C_4) + 1 = 0 \ , \tag{4.21}$$

which results in two transmission zeros, ω_{z1} and ω_{z2}, satisfying

$$\omega_{Z1}^2 \omega_{Z2}^2 = \frac{1}{L_3 C_3 L_4 C_4} \tag{4.22}$$

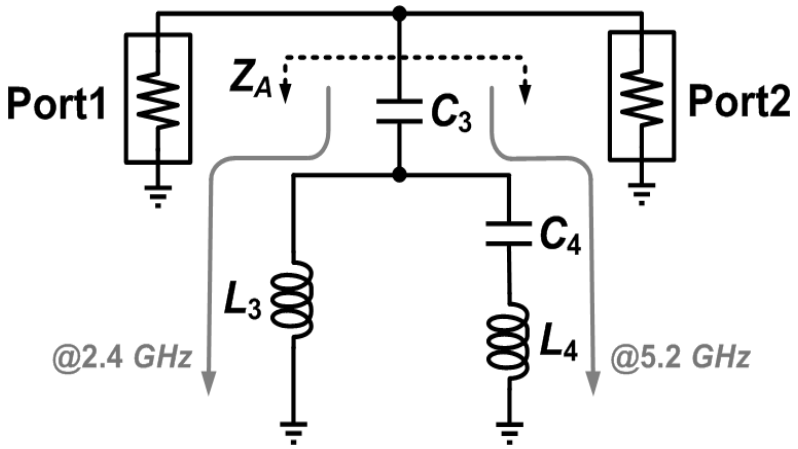


Fig. 4.16 The dual-band notch filter circuit.

$$\omega_{Z1}^2 + \omega_{Z2}^2 = \frac{L_3C_3 + L_3C_4 + L_4C_4}{L_3C_3L_4C_4} \quad . \tag{4.23}$$

Also, from (4.20), the impedance Z_A contains a pole at

$$\omega_{P1}^2 = \frac{1}{(L_3 + L_4)C_4} \quad . \tag{4.24}$$

In this study, we contrive that ω_{z1}, ω_{z2}, and ω_{p1} correspond to 2.4, 5.2, and 3.9 GHz, respectively. We will determine the appropriate values of L_3, L_4, C_3, and C_4 for the dual-band notch filter circuit in order to attenuate the WLAN interferers. It is noted that, after the decision of the positions of zeros and pole, we get three equations, i.e., (4.22)-(4.24), for the four filter components, which means that there is still one degree of freedom, let say L_3, left for the circuit design. Fig. 4.17 shows the transmission coefficients S_{21} of the notch filter with different L_3 values. As the value of L_3 increases, the in-band performance from 3.1 to 4.8 GHz will be improved; this means that we may use a larger inductance to maintain a better property in the target

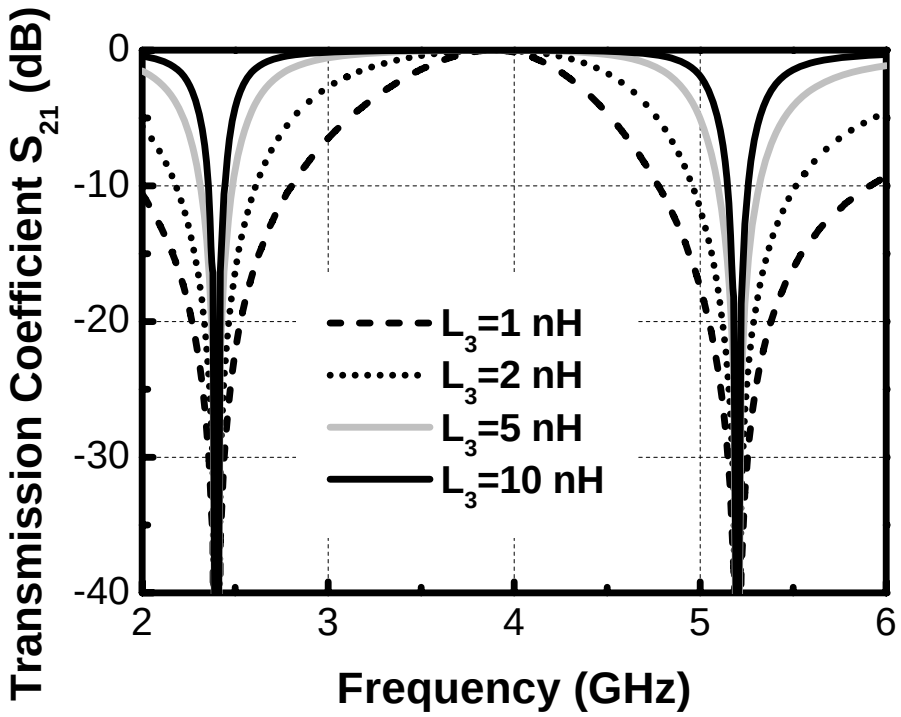


Fig. 4.17 Simulated transmission coefficient S_{21} of the notch filter for different values of L_3.

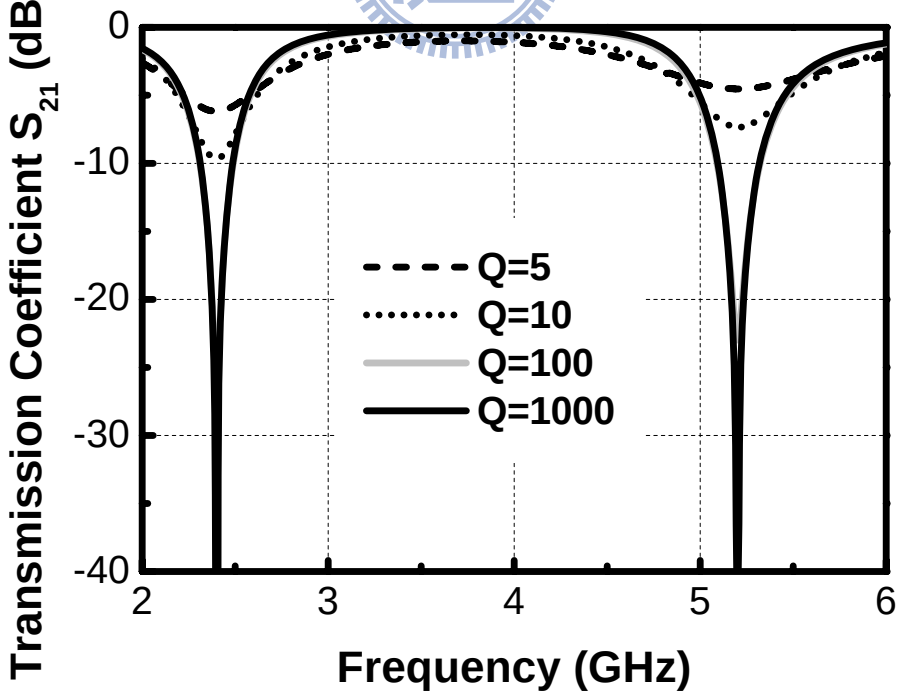


Fig. 4.18 Simulated transmission coefficient S_{21} of the notch filter for different values of Q with $L_3 = 5$ nH.

frequency range. To achieve a 10 dB attenuation in both 2.4 GHz and 5.2 GHz bands without suffering from deterioration of the in-band performance, the value of L_3 = 5 nH in the proposed notch filter will be chosen. On the other hand, the quality factor, Q, of the inductor also influences the performance of the filter, as can be observed from Fig. 4.18, where the transmission coefficients of the filter for different inductor Q values are shown. It is seen that a low quality factor will deteriorate the maximum attenuation of the notch filter. To obtain a 20 dB attenuation of the notch filter for the required specifications, the value of the quality factor Q must be higher than 100. In general, the negative-resistance cell by using cross-coupled transistors can be employed to ameliorate the Q value of on-chip inductor. However, the larger inductors with cross-coupled transistors will concurrently occupy overlarge chip area and dc power. Therefore, we are inclined to utilize active circuitry to substitute for the integrated passive inductors.

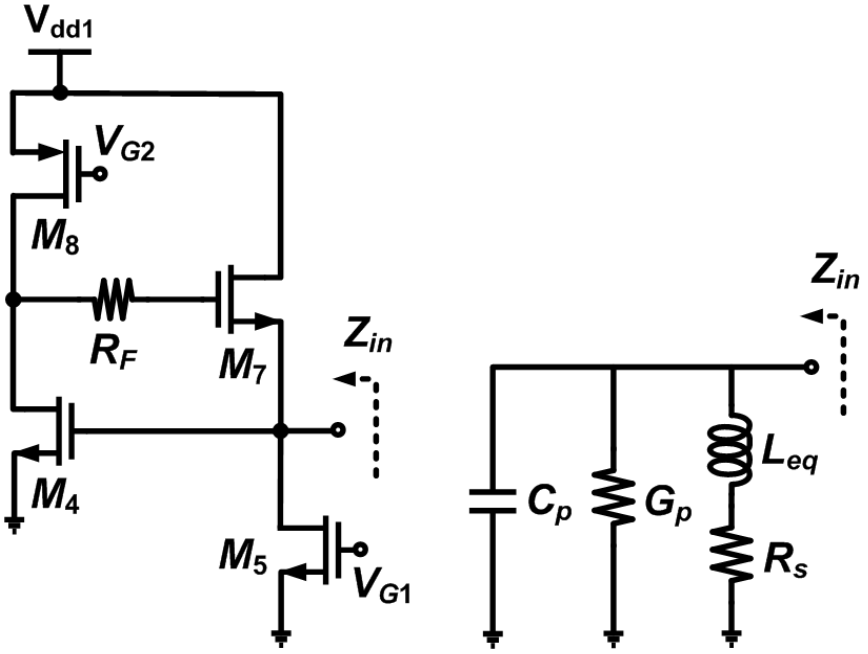
4.3.3 Design of Low Power Active Inductor

The realization of inductances L_3 and L_4 is based on the active inductor with a feedback resistor proposed in [56]. Fig. 4.19 (a) and (b) illustrate circuit schematic and the corresponding equivalent circuit. Through a simple derivation, the components of the equivalent circuit can be obtained as

$$L_{eq} \approx C_{gs7}\left(1+g_{ds4}R_F\right)/\left(g_{m4}g_{m7}\right) \tag{4.25}$$

$$G_p \approx g_{ds7}+g_{m4}/\left(1+g_{ds4}R_F\right) \tag{4.26}$$

$$R_s \approx 1/(g_{m7}A_{v4}) = g_{ds4}/\left(g_{m7}g_{m4}\right) \tag{4.27}$$



(a) (b)

Fig. 4.19 (a) Schematic and (b) equivalent circuit of the active inductor with a resistor in the feedback path.

$$C_p \approx C_{gs4} \tag{4.28}$$

with C_{gsi}, g_{dsi}, and g_{mi} being the gate-source capacitance, output conductance, and transconductance of the corresponding transistors, respectively. In general, the quality factor of the active inductor can be promoted by decreasing the values of G_p and R_s. From (4.26), the use of the feedback resistor R_F does reduce the value of the parallel conductance G_p by introducing the factor $(1+ g_{ds4}R_F)$. In addition, a larger $g_{m7}g_{m4}$ is required as shown in (4.27) to get lower value of R_s. However, this will increase the whole dc power consumption in the active inductor since g_{mi} is proportional to the current of transistors. To overcome this drawback, here we modify the active inductor circuit by using the gain-boosting technique [57] to achieve a small amount of dc current while maintaining a sufficient Q value. This is accomplished by

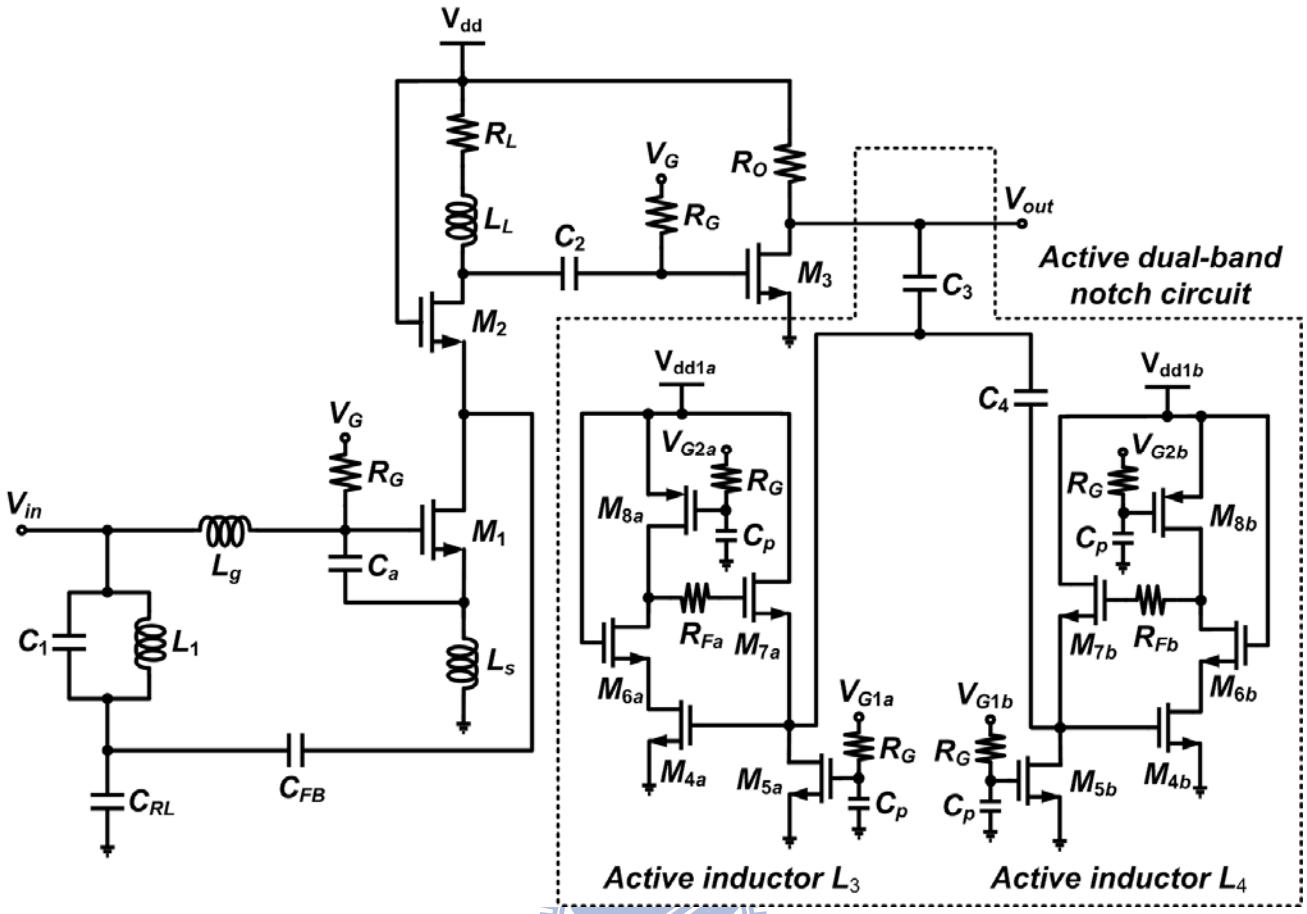


Fig. 4.20 Complete schematics of the proposed second UWB LNA.

using a cascode stage M_4 and M_6 to replace the only common-source transistor M_4, resulting in a new active inductor configuration as shown in the complete schematic of the second UWB LNA in Fig. 4.20. The voltage gain in (4.27) can thus be substantially augmented and the value of R_s will be obtained as

$$R_s \approx 1/(g_{m7}A_{v4}A_{v6}) = g_{ds4}g_{ds6}/(g_{m7}g_{m4}g_{m6}). \tag{4.29}$$

Therefore, a low-power active inductor is easily accomplished due to the use of the cascode gain-boosting stage with a feedback resistor. On the other hand, the transistor component, which exists the parasitic effect such as a Miller parasitic capacitor will deteriorate its high-frequency performance. However this additional transistor M_6 (i.e.,

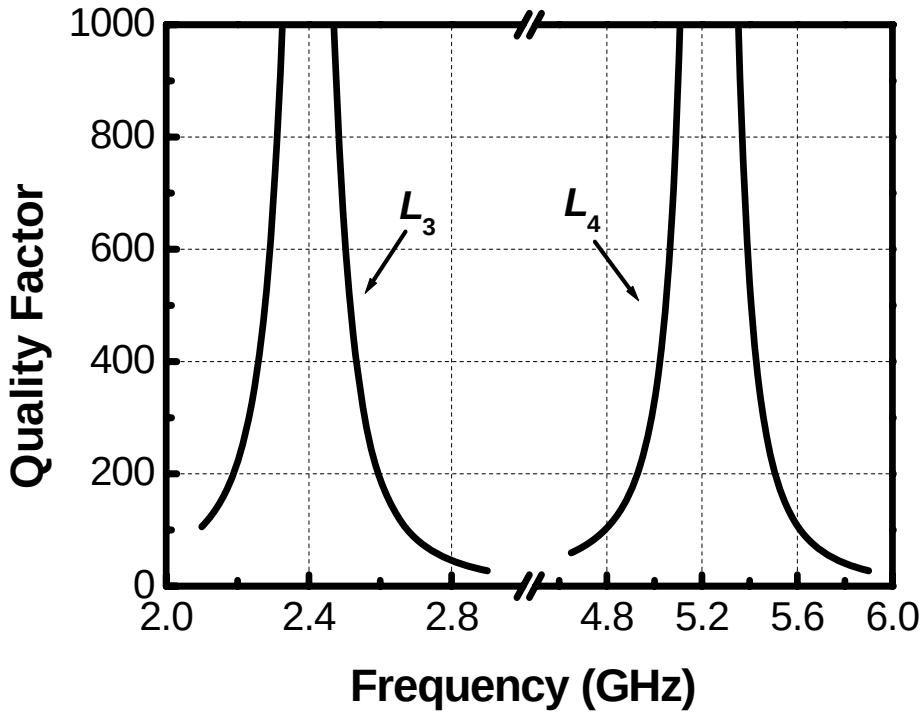


Fig. 4.21 Simulated quality factor of the proposed active inductors L_3 and L_4.

common-gate amplifier) not only has less influence on its Miller parasitic capacitor, but also facilitates to reduce the Miller effect of the transistor M_4. As a consequence, the proposed low-power active inductor is attractive and suitable in the nowadays microwave integrated circuits for the excellent high-frequency performance. Fig. 4.21 illustrates the simulated Q factor of the proposed active inductor, which shows that the active inductor exhibits a Q factor larger than 1000 at both 2.4 GHz and 5 GHz bands. These high-Q inductors undoubtedly provide a larger attenuation at the interferer frequencies, as can be observed from Fig. 4.18. Only 0.55 mA (for L_4) and 0.8 mA (for L_3) dc currents are required in the second UWB LNA circuit shown in Fig. 4.20, which are smaller than those in the previously literatures [56]–[58].

Moreover, it is obvious in (4.25) that the inductance of an active inductor is related to the transconductances, and thus the bias currents, of the transistors. Consequently, the notch frequencies will be effectively tuned by adjusting the bias

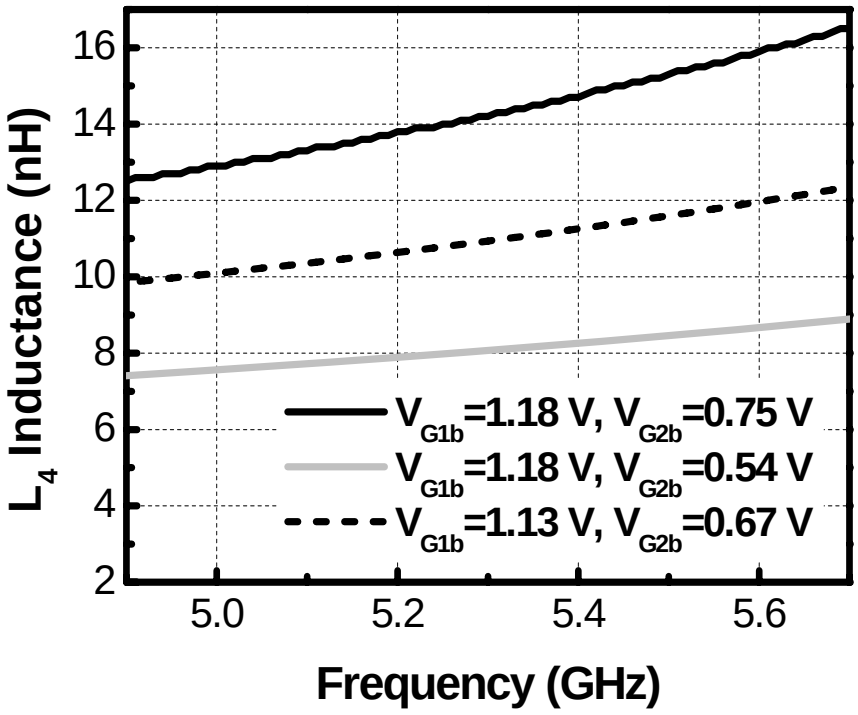


Fig. 4.22 Inductance of an active inductor is related to the bias voltages of the transistors.

currents of the active inductor. The externally controlled bias voltages V_{G1} and V_{G2} in Fig. 4.20 are designed here for adjusting the bias currents to compensate the frequency shift due to the process variation, as can be observed from Fig. 4.22. The quality factor Q of the active inductor is necessary to further adjust after tuning the notch frequencies. The quality factor Q also can be modified by the bias voltages V_{G1} and V_{G2}. As is clear from (4.25), the value of the equivalent inductor L_{eq} is inversely proportional to $g_{m4}g_{m7}$. To avoid the notch frequency drifting more, the quality factor Q must be tuned by gradually increasing g_{m4} with a decrease of g_{m7}, as can be observed from Fig. 4.23. By this way, the quality factor Q will be swept to optimize the maximum attenuation of the notch filter while maintaining a similar notch frequency.

On the other hand, a feedback mechanism, which has been adopted and

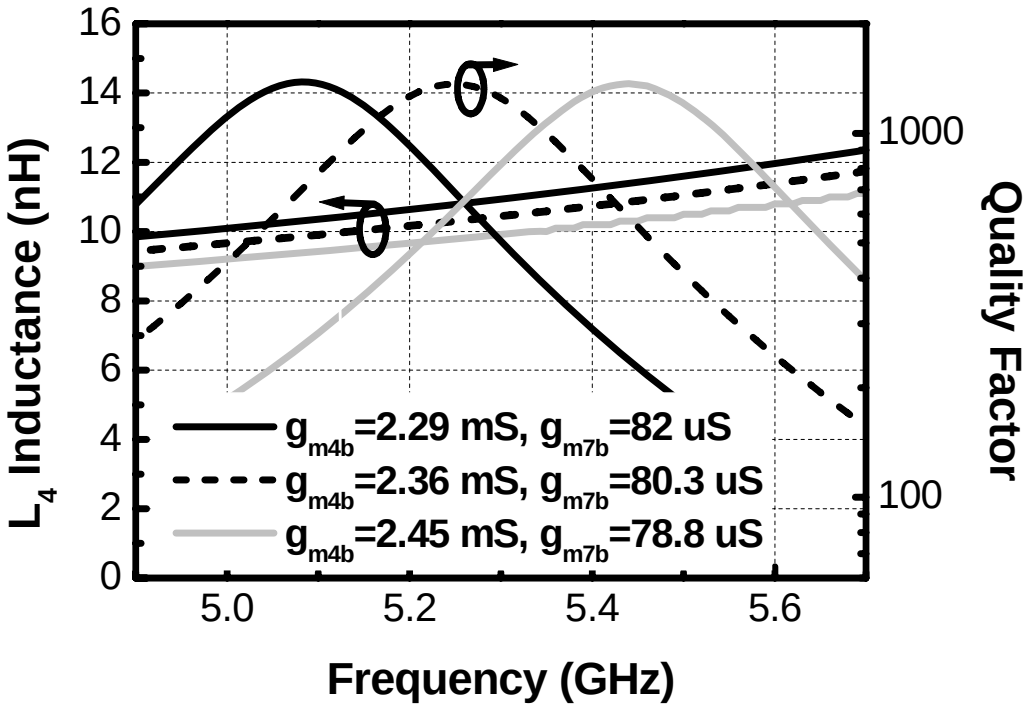


Fig. 4.23 Adjustable quality factor Q of an active inductor while maintaining a similar inductance value.

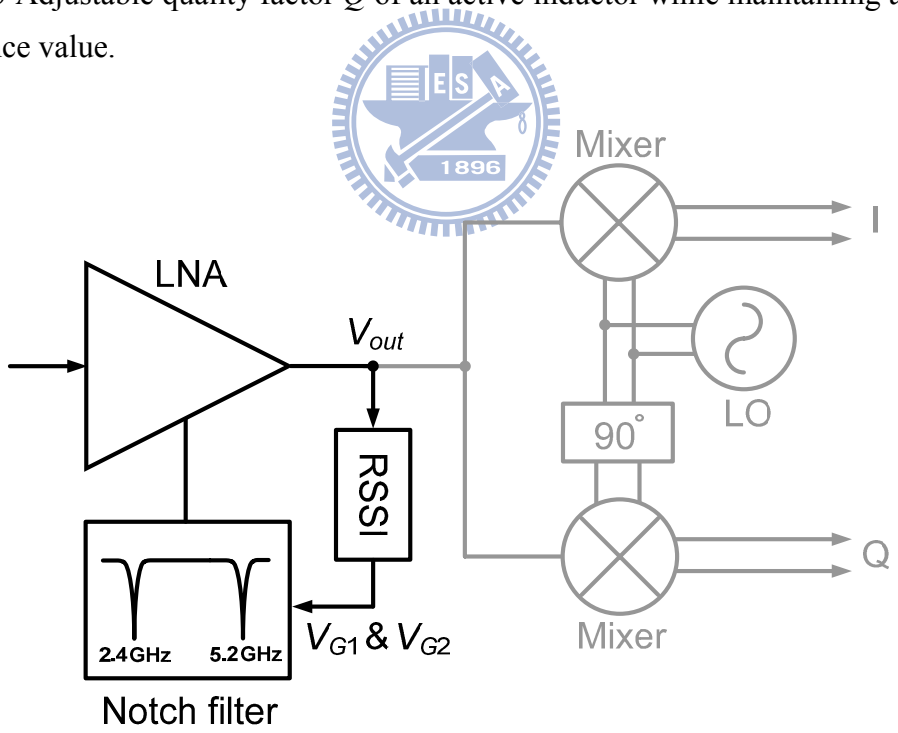


Fig. 4.24 Principle of the feedback technique for setting the notch frequency.

demonstrated in [43]-[44] and [59]-[60], is necessary to precisely set the notch frequency. The circuit architecture of the feedback technique is shown in Fig. 4.24. To

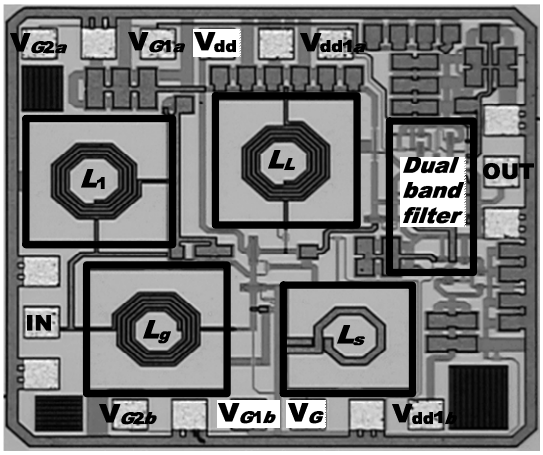


Fig. 4.25 Microphotograph of the fabricated UWB LNA. Die area is 0.9×0.85 mm^2.

begin with, a test signal such as 2.4 GHz is transmitted to the input of the LNA, and the output power at the node V_{out} can be measured with the received signal strength indicator (RSSI), which is a device available commonly in any wireless receiver. In addition, the RSSI output can be used to adjust the externally controlled bias voltages V_{G1} and V_{G2}, so as to assure the detected test signal strength is minimum. As we can see, the notch frequency drift due to the process variation will be calibrated as long as a feedback mechanism is utilized. Consequently, the narrowband interferers can be effectively attenuated in order to coexist with other wireless technologies for UWB communication.

4.3.4 Simulation and Experimental Results

For the second UWB LNA shown in Fig. 4.20, the components values of the active inductors are as follows: M_{4a} = 60 μm, M_{5a} = 4.5 μm, M_{6a} = M_{7a} = 37.5 μm, M_{8a} = 1.5 μm, M_{4b} = 16.5 μm, M_{5b} = 2.1 μm, M_{6b} = 31.5 μm, M_{7b} = 35 μm, M_{8b} = 2.7 μm, R_{Fa} = 125 Ω ,and R_{Fb} = 1.1 kΩ. A die microphotograph of the second LNA is shown in Fig. 4.25 and the die area including pads is 0.9×0.85 mm^2.

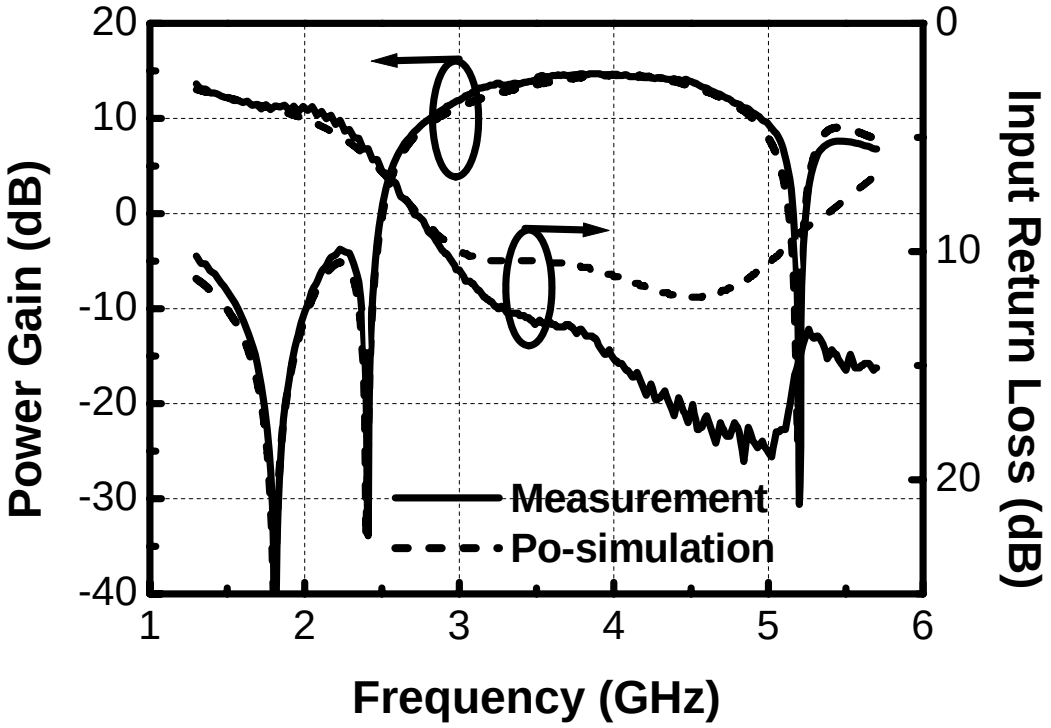


Fig. 4.26 Measured and simulated power gain (S_{21}) and input return loss ($1/S_{11}$) of the second UWB LNA.

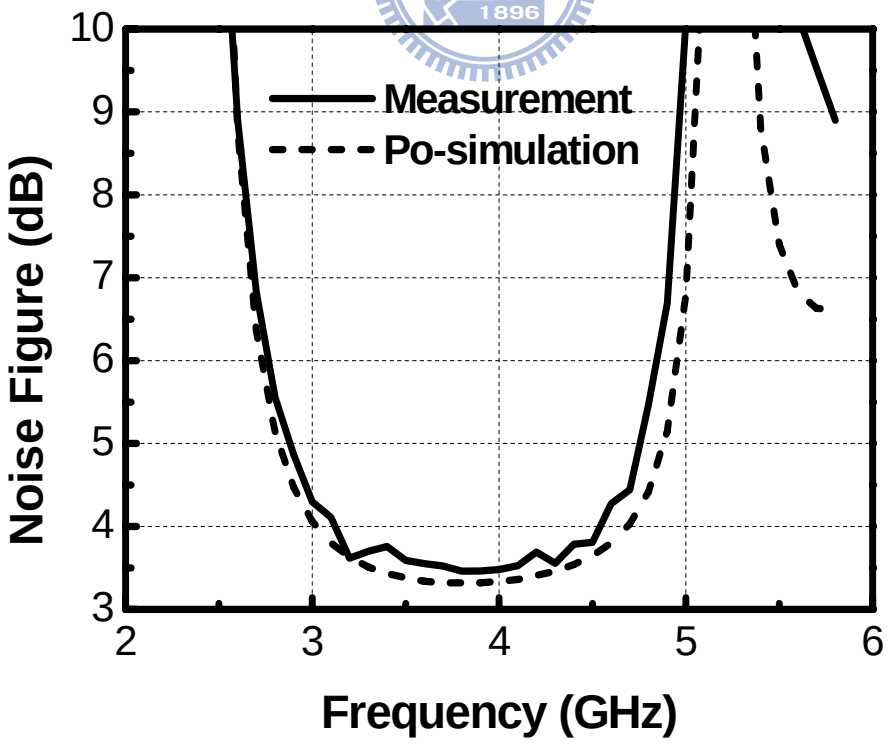


Fig. 4.27 Measured and simulated noise figure of the second UWB LNA.

The total dc power of the second UWB LNA without output buffer is 5 mW, drawn from 0.9 and 1.8 V power supply. The simulated and measured results of power gain and input return loss are depicted in Fig. 4.26. The measured peak gain is 15 dB from 3 to 4.8 GHz and the input return loss is better than 10 dB in the operation frequencies while the maximum rejections at 1.8, 2.4, and 5.2 GHz are 55, 48, and 45 dB, respectively. The simulated and measured noise figures are depicted in Fig. 4.27 and the measured minimum noise figure is 3.5 dB at 3.9 GHz.

4.4 WIDE-BAND LOW NOISE AMPLIFIER WITH A NEW MATCHING TECHNIQUE

In this section, we propose a low-power and low-noise amplifier with a new input-matching technique by using 0.18-μm CMOS technology for ultra wide-band applications. In general, the distributed configuration [63] and *LC* input network [27], [64] are attractive for their ultra-wide bandwidth; however, the major drawbacks are the larger chip area and worse noise figure due to the usage of the low-*Q* on-chip inductors in the input network. To overcome the above-mentioned drawbacks, we propose a new inductorless input-matching technique, which is based on a source-degenerated structure to achieve a superior noise performance. On the other hand, the common-source stage with *LC* tank load, as shown in Fig. 4.28 (a), can be adopted to enhance the bandwidth of amplifier by appropriately tuning the resonator frequency of *LC* tank load; however, it is unavoidable to increase dc power consumption, which may make this circuit unsatisfactory for low-power application. Here we utilize the inter-stage resonator in Fig. 4.28 (b) to substitute for common-source stage. As a consequence, the significant power reduction and bandwidth enhancement will be attained simultaneously.

4.4.1 Circuit Design and Analysis

The proposed input matching circuit, as shown in Fig. 4.29 (a), utilizes the current-reused configuration with an additional capacitor C_a to achieve the design of low-power characteristic and wide-band match. Fig. 4.29 (b) and (c) depict the frequency behavior of the input impedance. It is obvious that the transistors M_{1n} and

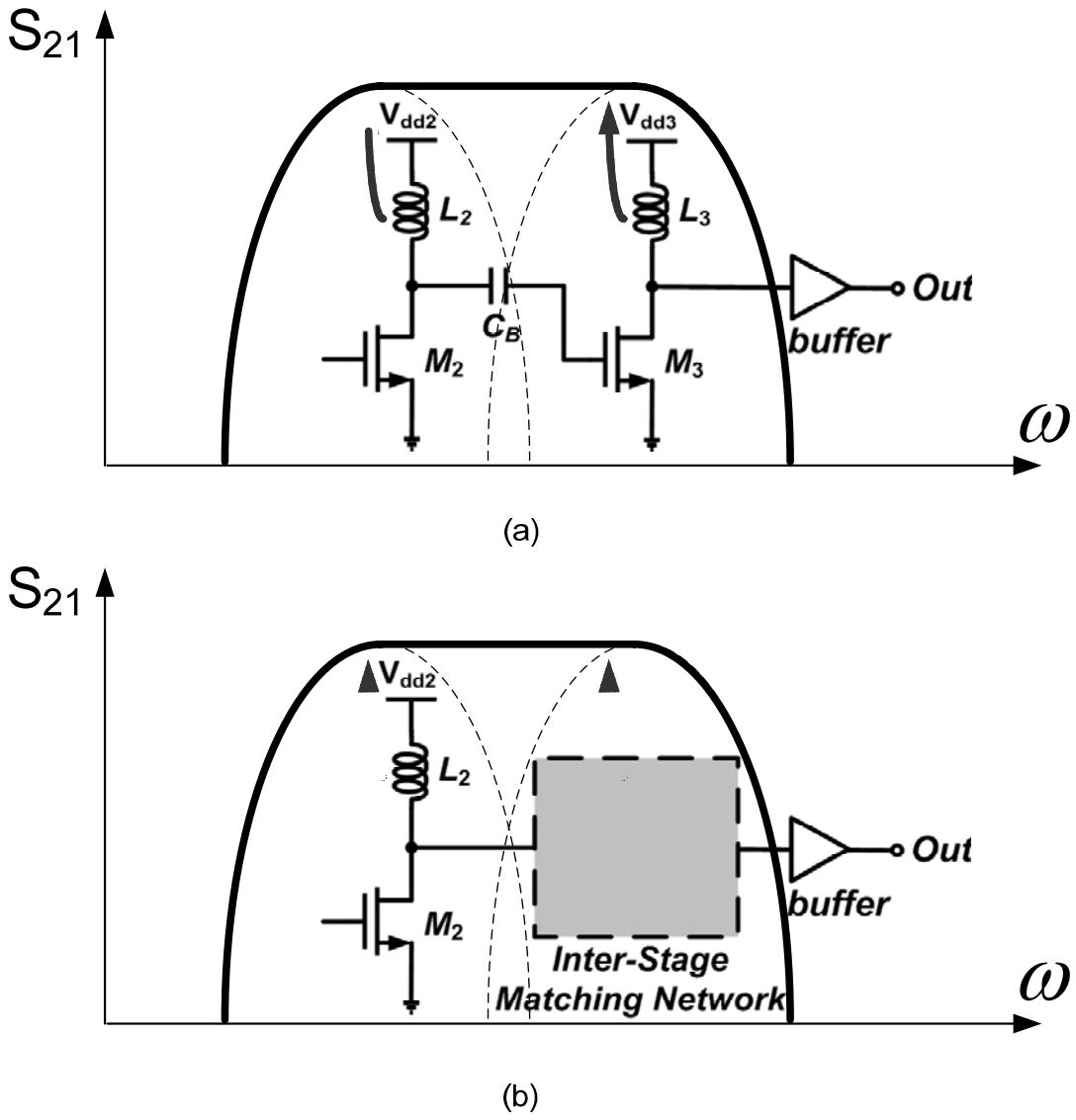
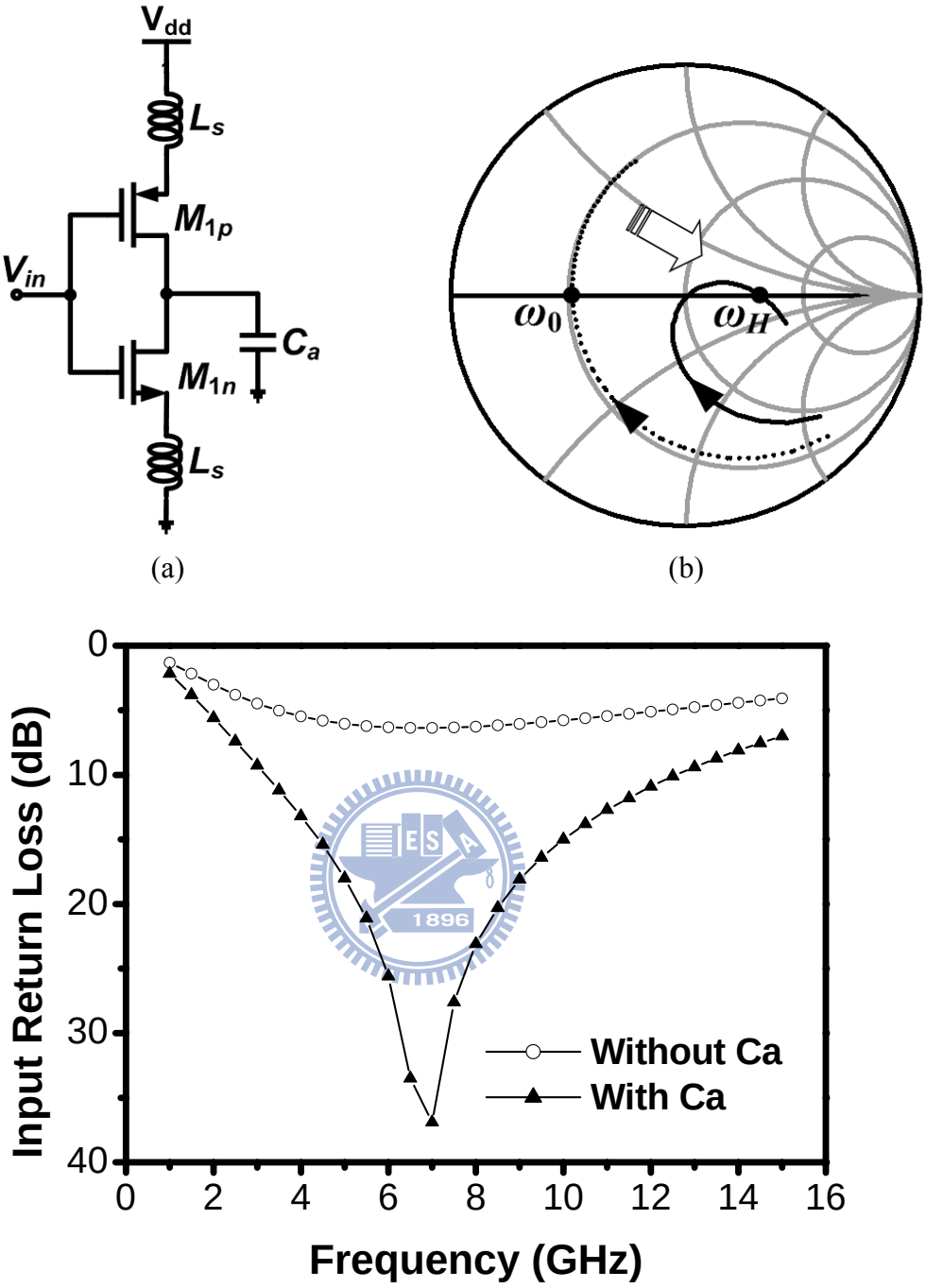


Fig. 4.28 Bandwidth enhancement techniques (a) the common-source stages with inductive loads and (b) the basic principle with inter-stage series resonators.

M_{1p} exist the parasitic effect such as a Miller parasitic capacitor; therefore, an extra parallel resonant frequency ω_H in Fig. 4.29 (b) can be generated by introducing only an additional capacitor C_a. Due to the presence of the resonant frequency ω_H, a loop surrounding the 50-Ω matching point is formed on the Smith chart. As we will see, a broad-band input match in the intended frequency range can be acquired by selecting appropriately the value of capacitor C_a.



(a) (b)

(c)

Fig. 4.29 The proposed input matching circuit and its frequency behavior.

In this study, we are inclined to employ the amplifier stage M_2 with power consumption fixed at 1.5 mW, as shown in Fig. 4.30, to substitute for the capacitor C_a. Fig. 4.31 shows the relation between the input return loss and frequency for different widths of the transistor M_2. It can be observed that the input-matching

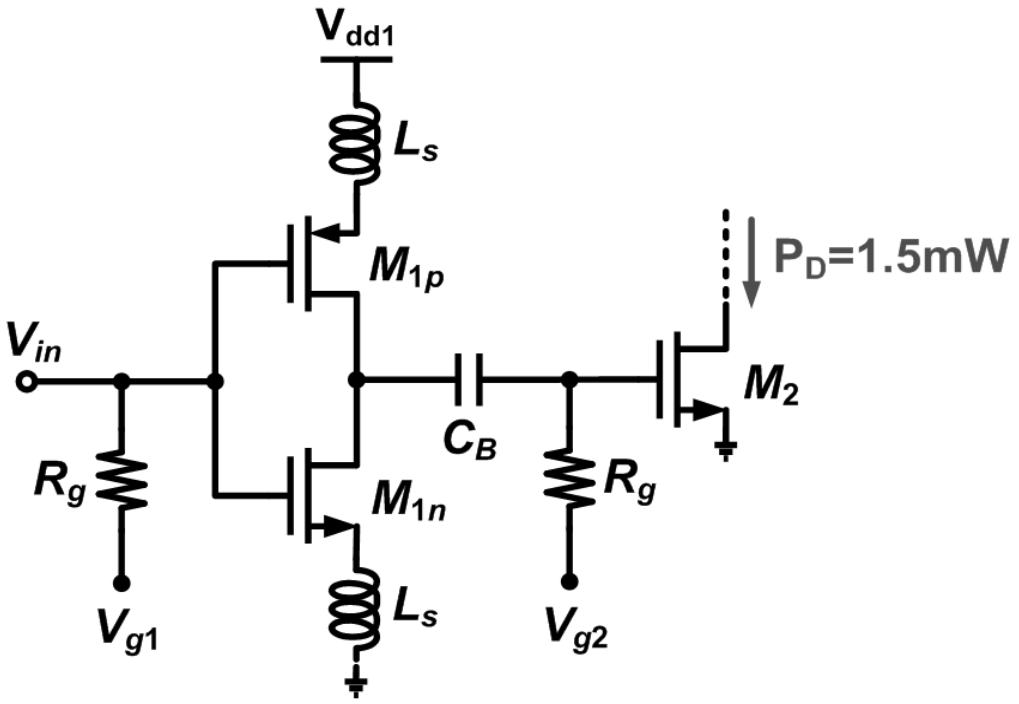


Fig. 4.30 The capacitor C_a is substituted for the amplifier stage M_2 with power consumption fixed at 1.5 mW.

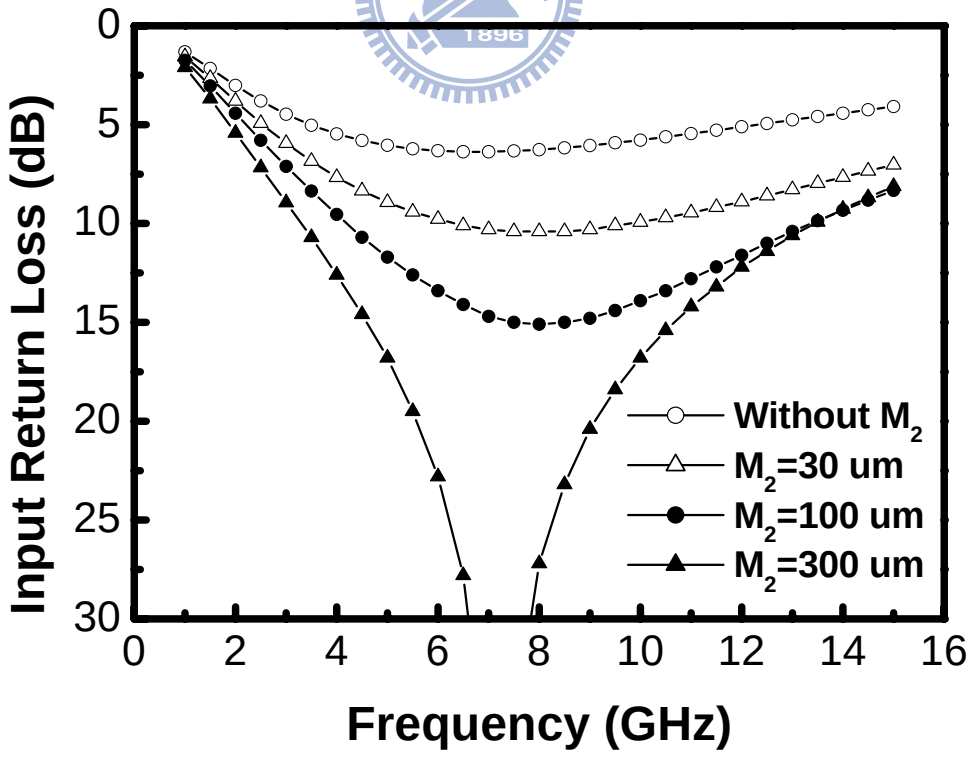
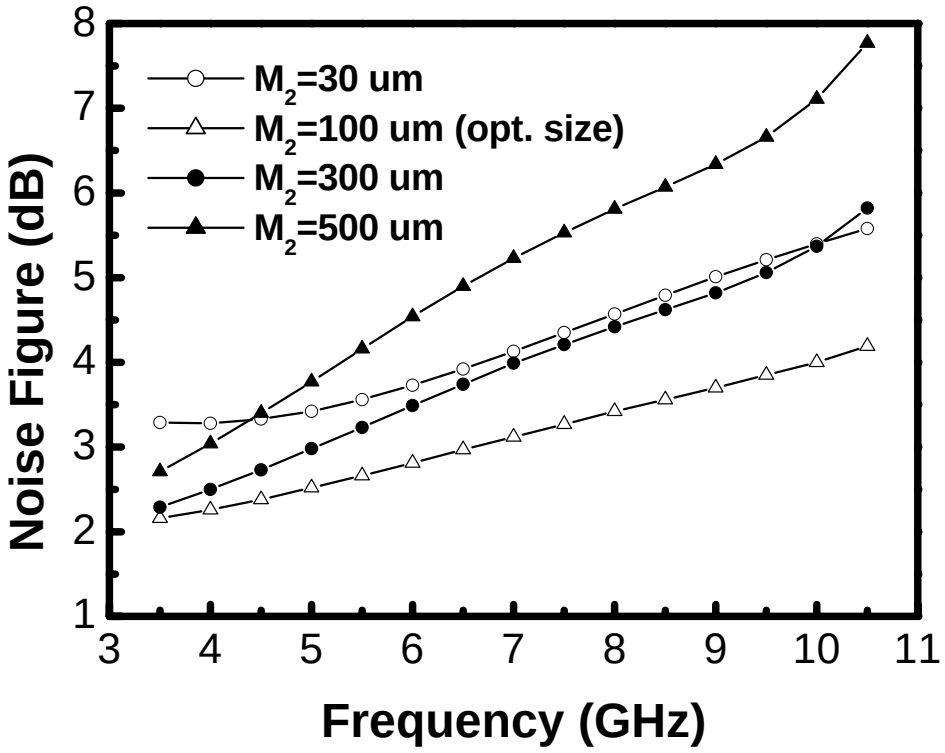


Fig. 4.31 Simulated input return loss for different widths of the transistor M_2.



(b)

Fig. 4.32 Simulated noise figure for different widths of the transistor M_2.

performance will be ameliorated when the width of transistor M_2 increases; however, an overlarge width will bring about the deterioration in noise figure, as demonstrated in Fig. 4.32. This is because an overlarge capacitor C_a will diminish power gain of the current-reused amplifiers M_{1n} and M_{1p} to indirectly worsen noise property of the proposed UWB LNA. As a consequence, a trade-off should be carefully considered so as to make an optimum design.

Moreover, due to the usage of the inter-stage resonator, the significant power reduction and bandwidth enhancement will be attained simultaneously. It is known that maximum power transfer will occur by means of the conjugate impedance matching [27]. Therefore, the inter-stage resonator in Fig. 4.33 can accomplish gain bandwidth extension because of the conjugate impedance matching. As shown in Fig. 4.34, the simulated input reflection coefficients of Z_1 (solid line) and Z_2 (dashed line)

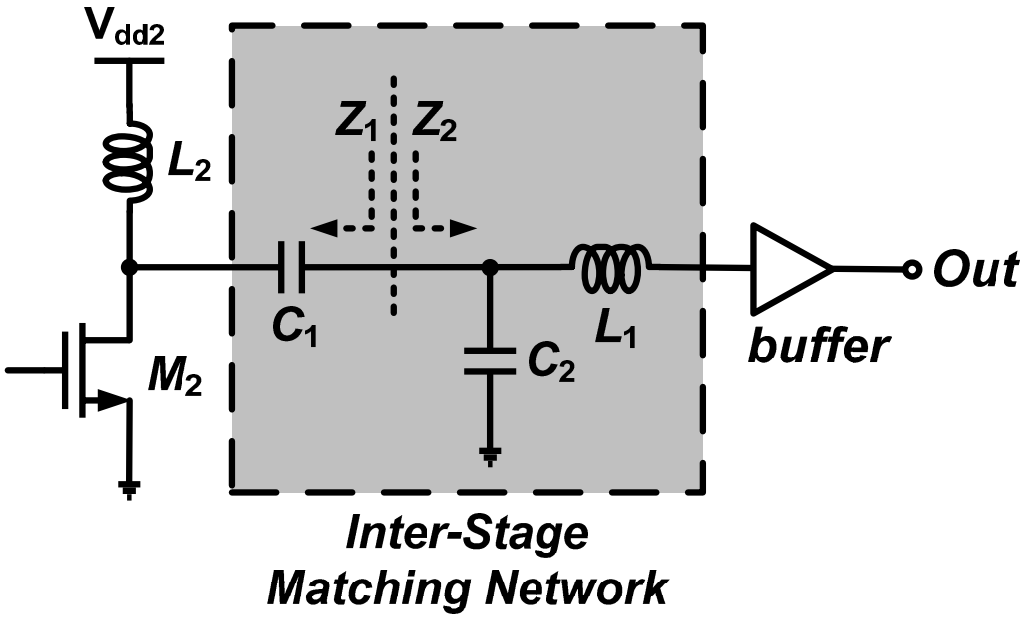


Fig. 4.33 Inter-stage matching network.

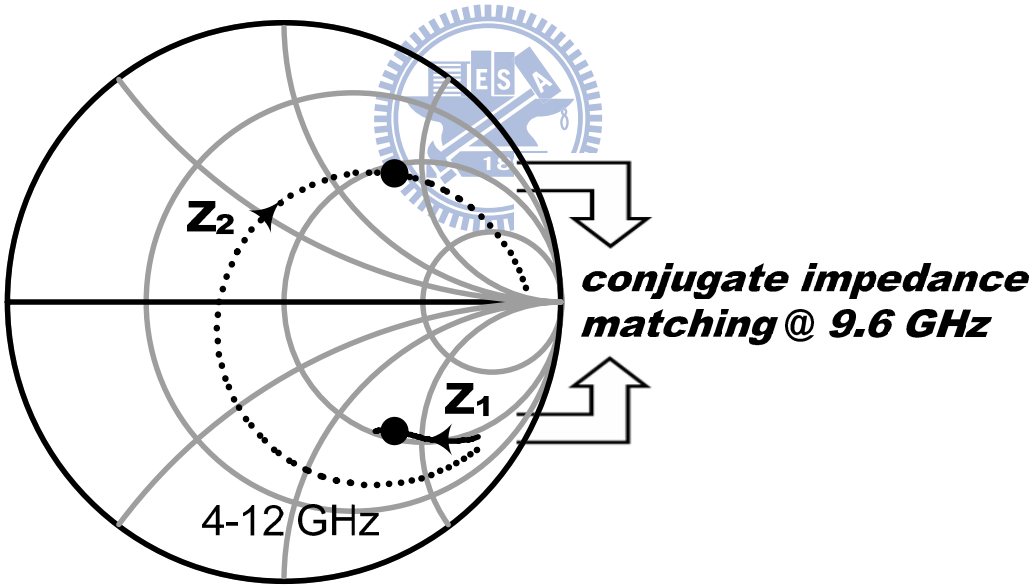


Fig. 4.34 Input reflection coefficients on the Smith chart for the impedances Z_1 (solid line) and Z_2 (dashed line) shown in Fig. 4.33.

are plotted on the Smith chart from 4 GHz to 12 GHz. The best conjugate impedance matching is designed near 9.6 GHz by using the inter-stage resonator. The simulation results of the transmission coefficient S_{21} with and without the inter-stage resonator

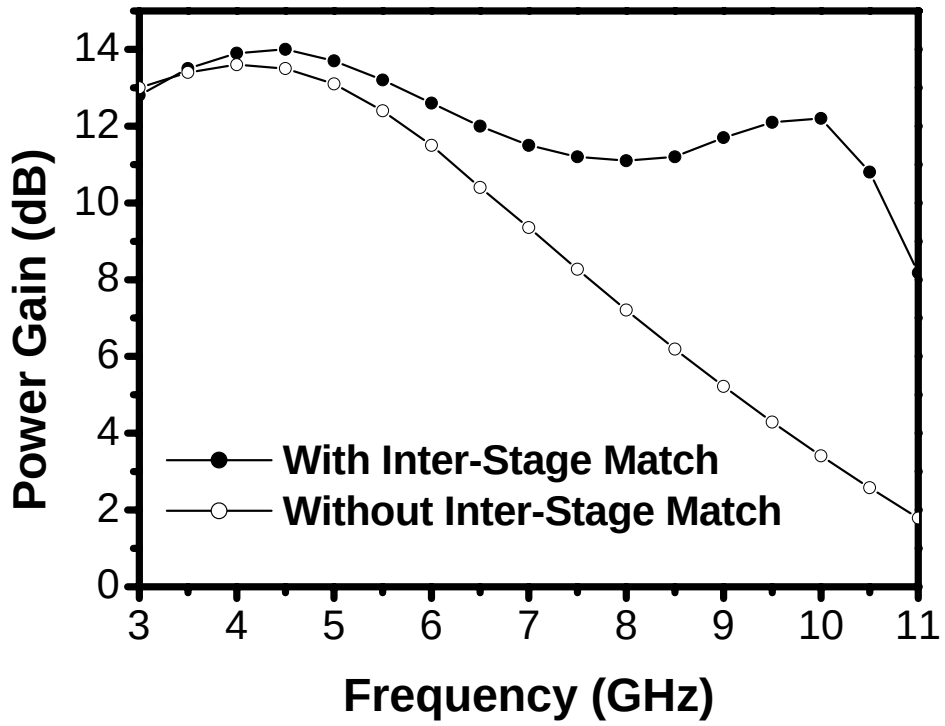


Fig. 4.35 Simulated power gain with and without the inter-stage matching network.

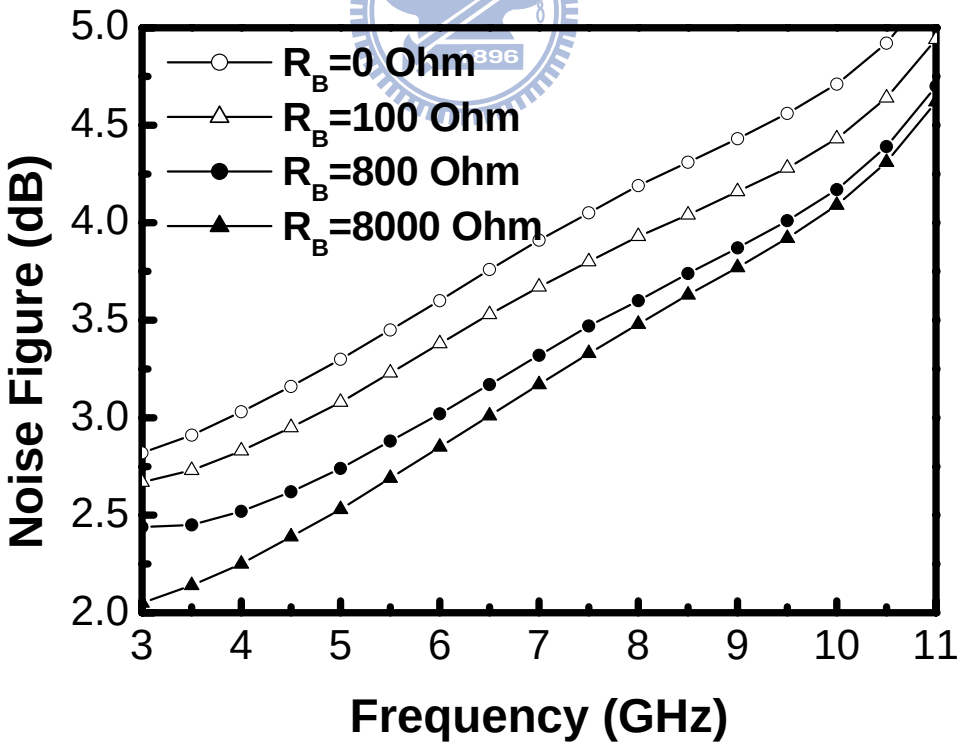


Fig. 4.36 Simulated noise figure for different values of the resistor R_B.

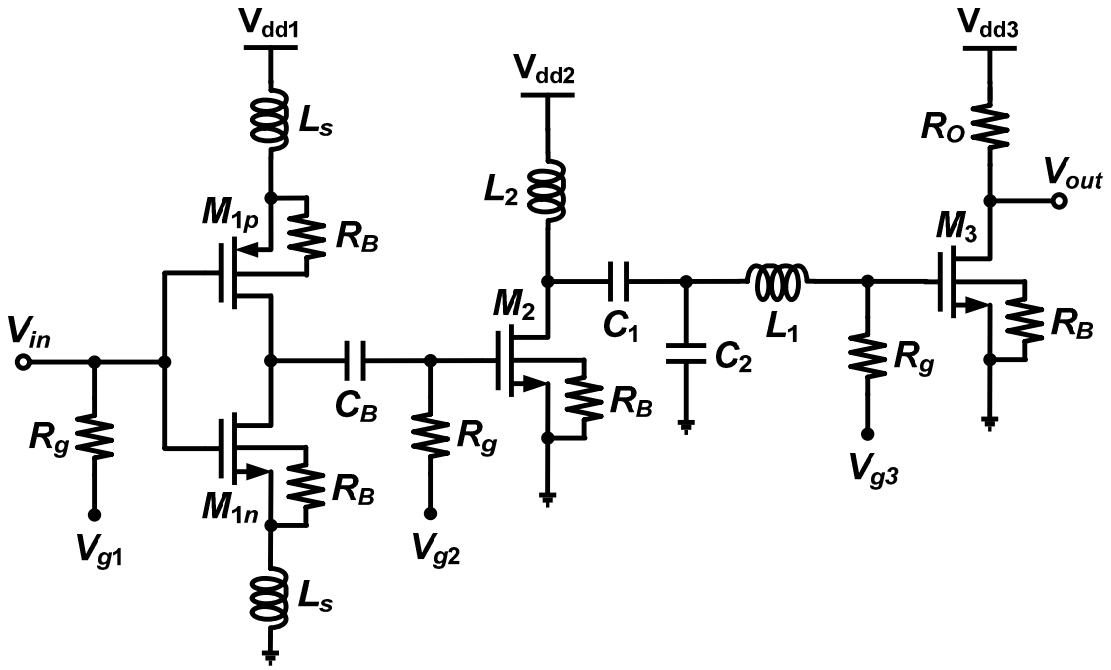


Fig. 4.37 The architecture of the proposed UWB LNA with a new input-matching technique.

are shown in Fig. 4.35. As we can see, the usage of the inter-stage matching network will effectively to improve the bandwidth without additional power consumption. In addition, a larger substrate resistor R_B in Fig. 4.36 is adopted in RF MOSFET device to obstruct the undesired noise power from the substrate port. The complete schematic of the proposed LNA fabricated by 0.18-μm TSMC CMOS process is shown in Fig. 4.37, and the resistor R_o is set as 50 Ω to achieve output match for testing purposes.

4.4.2 Simulation and Experimental Results

The third UWB LNA chip was measured by on-wafer probing and the total dc power dissipation is 6.8 mW. A die microphotograph of the proposed LNA is shown in Fig. 4.38 and die area including pads is 0.81×0.81 mm^2. The simulated and measured results of the power gain and input return loss are depicted in Fig.4.39. The

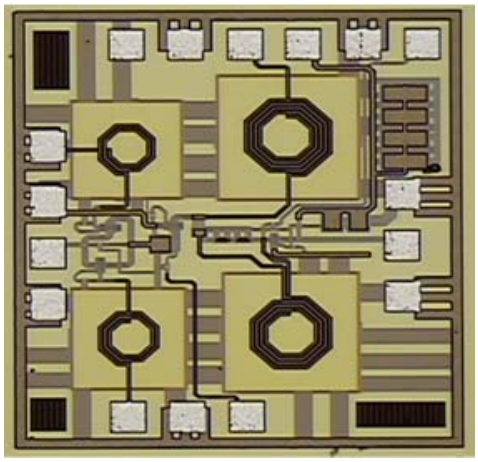


Fig. 4.38 Microphotograph of the LNA. Die area is 0.81×0.81 mm^2.

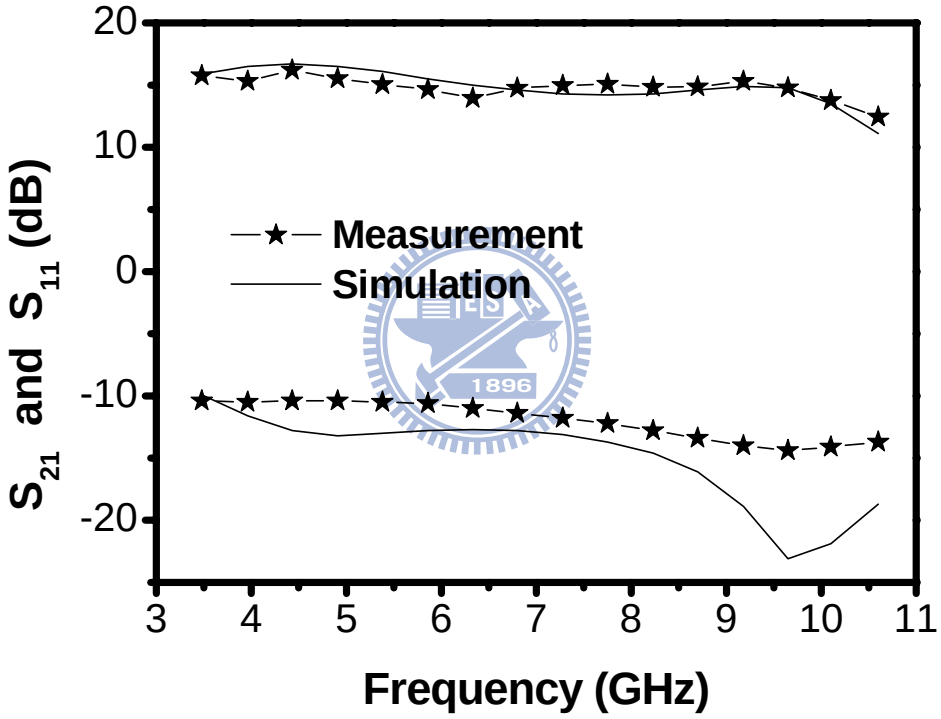


Fig. 4.39 Measured S-parameters of the proposed UWB LNA.

small signal peak gain is 16.2 dB with 3 dB bandwidth of 7 GHz from 3 to 10 GHz and input return loss is better than 10 dB in the operation bandwidth. The noise figure was measured using the Agilent N8975A noise figure analyzer with Agilent 346C noise source. The simulated and measured noise figure at the same bias condition is depicted in Fig. 4.40. It is seen that the minimum value of noise figure is equal to 2.3 dB at 3.5 GHz.

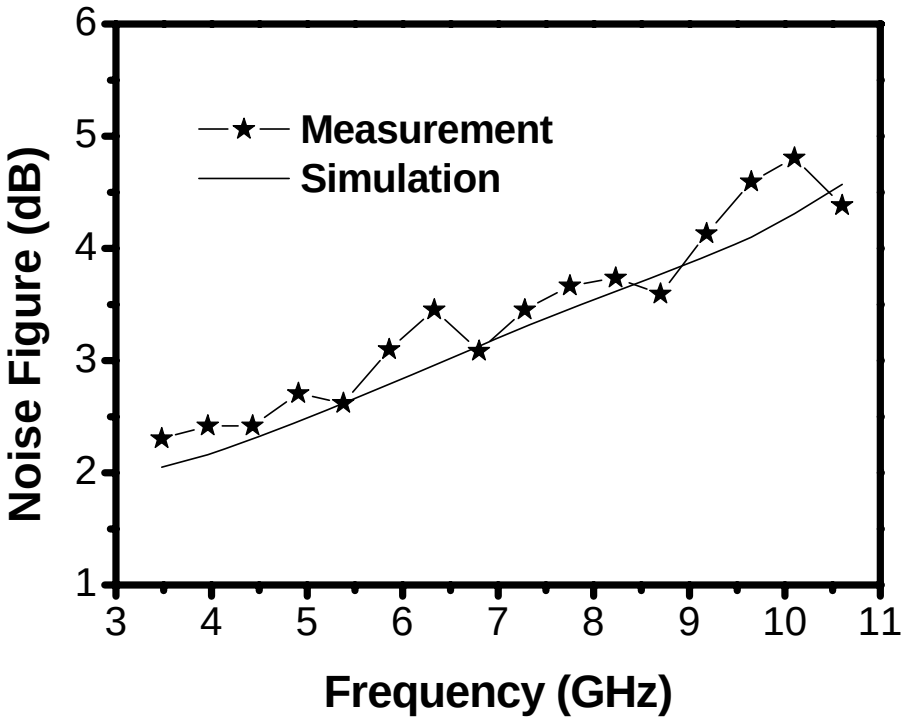


Fig. 4.40 Measured noise figure of the proposed UWB LNA.

4.5 SUMMARY

In this chapter, three low-power UWB LNAs using 0.18-μm CMOS technology are presented. Extra transmission zeros are created in the first UWB LNA due to the use of a *LC* input network with additional capacitors C_{RH} and C_{RL} for improving the higher and lower out-band performances respectively. Furthermore, using a feedback capacitor and dual-band notch filter made of the low-power active inductors can achieve the maximum rejections of about 50 dB at the out-band interferers, which was demonstrated in the proposed second UWB LNA. Finally, a new matching technique by selecting an appropriate width of the transistor M_2 is presented to further ameliorate the noise figure performance in the third UWB LNA. The presented UWB LNAs are compared with recently published CMOS LNA and summarized in Table 4.1.

Table 4.1

UWB LNA Performance summary

Ref.	Tech. [μm]	*BW* [GHz]	G_{max} [dB]	NF_{min} [dB]	P_{diss} [mW]	Area [mm^2]	Out-band rejection
[4]	0.18	3 ~ 6	15.9	4.7	59.4	1.1	-
[5]	0.18	2.8 ~ 7.2	19.1	3	32	1.63	-
[7]	0.18	0.04 ~ 7	8.6	4.2	9	1.16	-
[20]	0.13	2 ~ 4.6	9.5	3.5	16.5*	1.08	-
[24]	0.13	2 ~ 5.2ζ	16	4.7	38	0.24	-
[27]	0.18	3 ~ 4.8	13.9	4.7	14.6	0.95	-
[61]	0.25	3.2 ~ 4.8	7.5	2.7**	20*	-	-
[62]	0.35	2.5 ~ 5.5	11.8	2.1**	9*	1.13	-
[63]	0.13	0 ~ 12.1	18.7	3	27.6	0.88	-
[65]	0.13	0.1 ~ 10	17	5.3	60	0.64	-
[66]	0.18	0 ~ 16	10	3.6	21	1.19	-
[26]	0.13	3 ~ 5	19.4Ψ	3.5	31.5	1.6	6 dB @2.4 GHz 44 dB @5.2 GHz
[28]	0.18	3 ~ 4.8	16	2.7	11.9*	1.8	15 dB @2.4 GHz 19 dB @5.3 GHz
[55]	0.18	3 ~ 4.8	19.7	4.0	24	1.43	13 dB @2.4 GHz 20 dB @5.8 GHz
LNA1	0.18	2.8 ~ 6.2	11.5	3.8	2.5*	0.62	25 dB @1.8 GHz 32 dB @8.5 GHz
LNA2	0.18	3 ~ 4.8	15	3.5	5*	0.76	55 dB @1.8 GHz 48 dB @2.4 GHz 45 dB @5.2 GHz
LNA3	0.18	3 ~ 10	16.2	2.3	6.8	0.66	-

Ψ voltage gain ζ 1dB bandwidth * only core LNA

** external inductors for the input matching network

CHAPTER 5

VOLTAGE-CONTROLLED OSCILLATOR WITH PHASE-NOISE IMPROVEMENT

5.1 INTRODUCTION

The VCO is an important unit among the building blocks of a RF transceiver. The design considerations of a VCO include operation frequency band, phase noise, power consumption, and tuning range. Among the various architectures of the VCO, the cross-coupled oscillator is attractive for its design simplicity and start-up oscillation condition. The proposed VCO is thus based on this structure to ameliorate the noise performance.

Phase noise is one of the most critical parameters since it affects the overall performance of a communication system; therefore, there are numerous attempts in the design of VCO to optimize the phase-noise performance. The harmonic tuned LC tank in Fig. 5.1 is employed to attenuate the second harmonic power while maintaining a superior fundamental power, which is benefic to make the output voltage waveform steeper for reducing flicker noise of transistor [67]. The phase-noise suppression is achieved by maximizing the slope of the output voltage at the zero crossing point. However, it is inevitable to result in a high implementation cost because the additional on-chip inductors are required. On the other hand, the ICP deep-trench technique in Fig. 5.2, which selectively removes the silicon underneath the inductors, also can be utilized to improve the phase noise of a VCO [68]. Nevertheless, the extra CMOS process steps will raise the complication of circuit implementation.

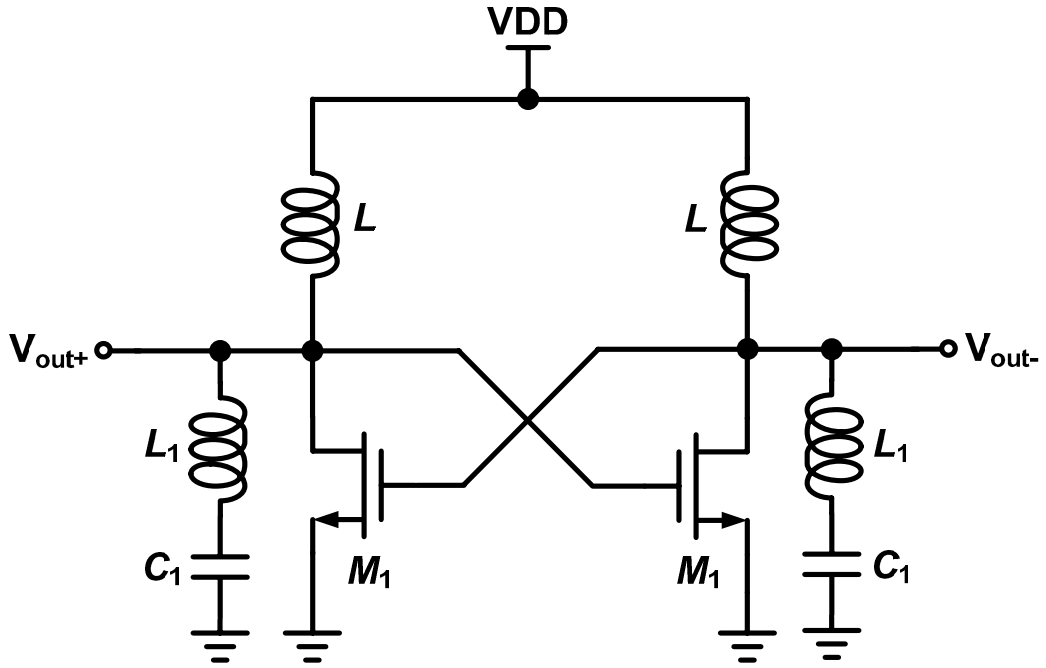


Fig. 5.1 The phase-noise suppression with the second harmonic tuned LC tank [67].

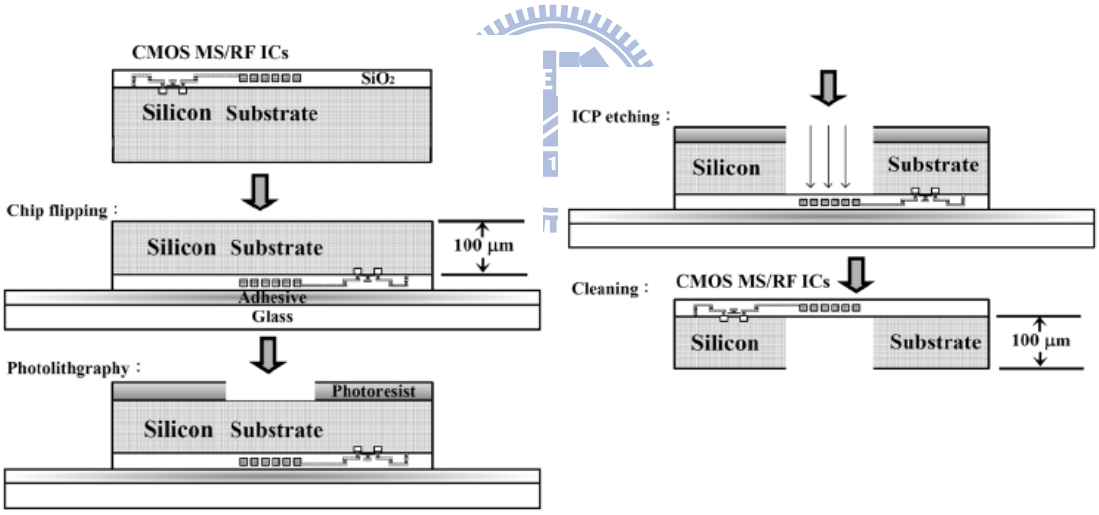


Fig. 5.2 Process steps of the backside ICP deep trench etching technique [68].

In this chapter, we adopt the design of a current-reused configuration because of its excellent low-power characteristic and focus on the improvement of phase-noise performances without additional chip area and CMOS process steps. By a larger parallel capacitor, an extra harmonic-rejected capacitor, and an appropriate bulk bias voltage of transistor, a good figure of merit (FOM) of -190 dBc/Hz will be attained.

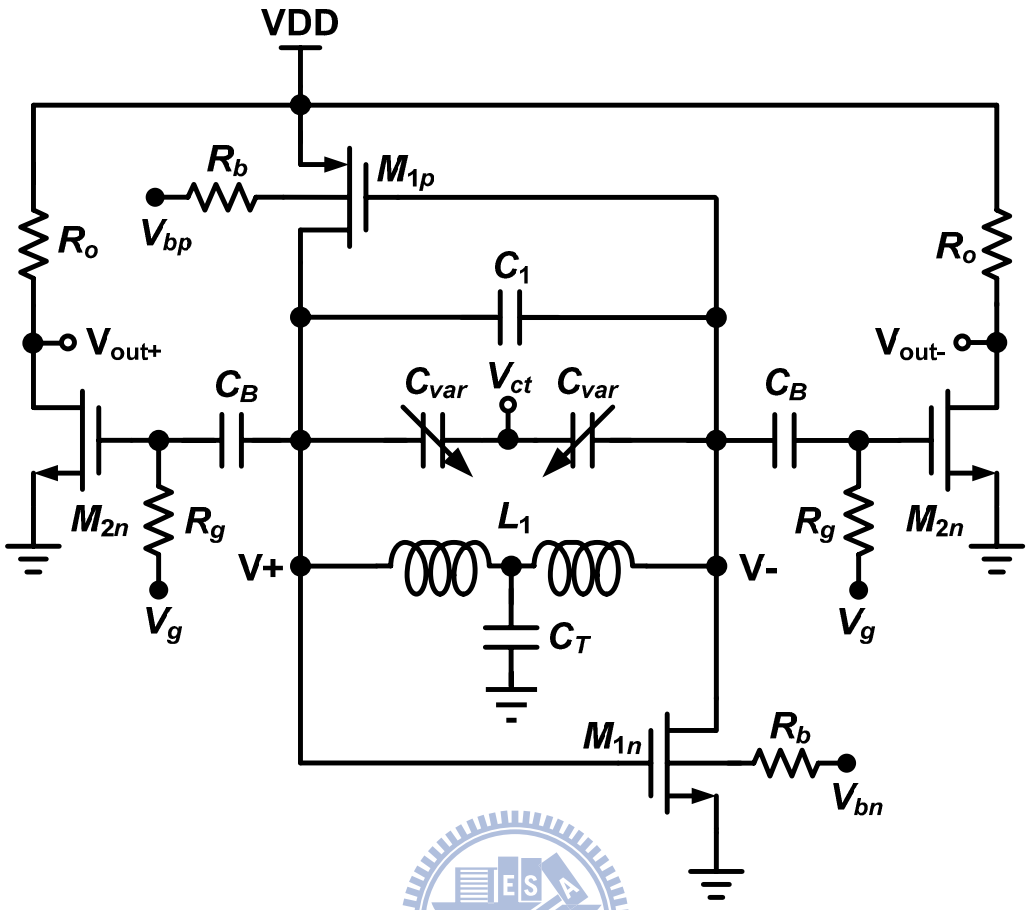


Fig. 5.3 Complete schematics of the proposed low-power VCO with the phase-noise reduction techniques.

5.2 CIRCUIT DESIGN

The proposed VCO, as shown in Fig. 5.3, uses the cross-connected pair consisted of NMOS and PMOS transistors as a negative conductance generator. Power consumption and the usage of inductors can be cut in half compared to the traditional VCO while providing the same negative conductance. Furthermore, a center-tapped spiral inductor L_1 is employed to obtain a symmetrical differential output signals at nodes V_+ and V_-. When the voltage at node V_+ is high, the proposed VCO is equivalent to that shown in Fig. 5.4 (a), where the transistors M_{1p} and M_{1n} operate in the triode region. The impedance observed from the inductor L_1 can be regarded as the

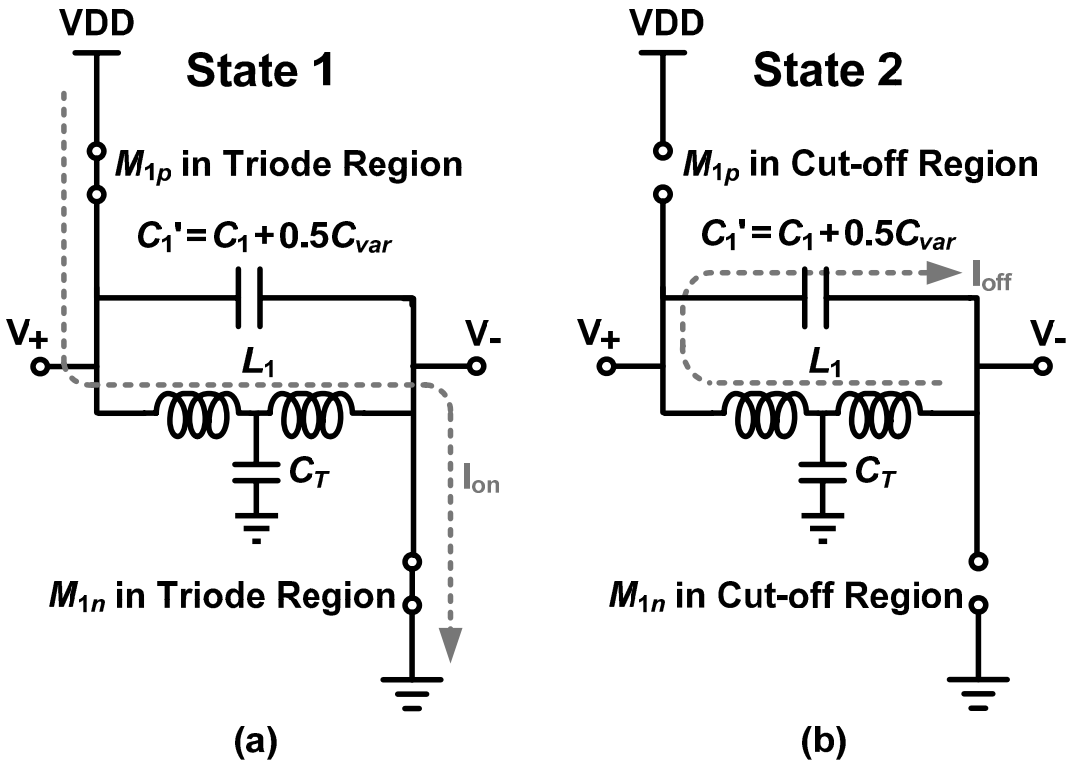


Fig. 5.4 The equivalent circuits of the proposed VCO when the voltage at node V_+ is (a) high and (b) low.

capacitor C_1' in parallel with the triode mode resistors (i.e., a smaller impedance is acquired). On the other hand, when the voltage at node V_+ is low, the circuit is equivalent to that in Fig. 5.4 (b), and the impedance observed from the inductor L_1 becomes only that of the capacitor C_1'. An obvious impedance difference will arise when V_+ changes in between high and low statuses, which means that an unbalanced voltage swing at node V_+ will be generated. This in turn will deteriorate the phase-noise performance. In order to improve this drawback, a larger value of the capacitor C_1' (i.e., a smaller impedance) is required to maintain the similar impedances in both operation statuses. It can be observed from Fig. 5.5 that a larger capacitor C_1' effectively provides a balanced voltage swing at node V_+ to ameliorate phase-noise characteristic.

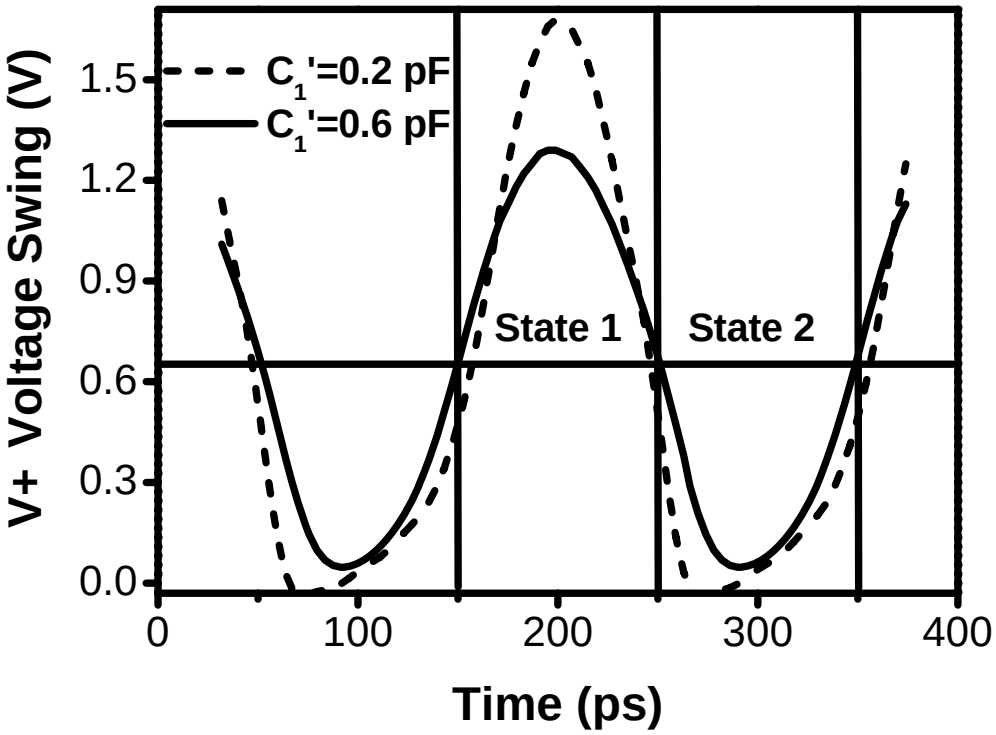


Fig. 5.5 Simulated V_+ voltage swing for different values of C_1.

The suppression of the second harmonic power with the series *L*-*C* sections has been utilized to improve the phase noise of a VCO [67]; however, the extra inductors will occupy additional chip area, which makes it undesired for low-cost application. In this study, we introduce an additional capacitor C_T in the VCO circuit (Fig. 5.3) to attenuate the second harmonic signal, as shown in Fig. 5.6. To begin with, it can be anticipated that node A is a virtual ground due to the differential outputs of the fundamental signal, and this means that the existence of the capacitor C_T will have no influence on the oscillation frequency. However, the in-phase second harmonic signals can be suppressed by the usage of a suitable capacitor C_T because a series resonance is produced. Fig. 5.7 shows the measured results of the output signal with and without the additional capacitor C_T, and it can be observed and demonstrated that a 12 dB decrease in the second harmonic power is attained. Consequently, the introduction of the capacitor C_T can effectively diminish the second harmonic signal while without increasing the chip area and influencing the oscillation frequency.

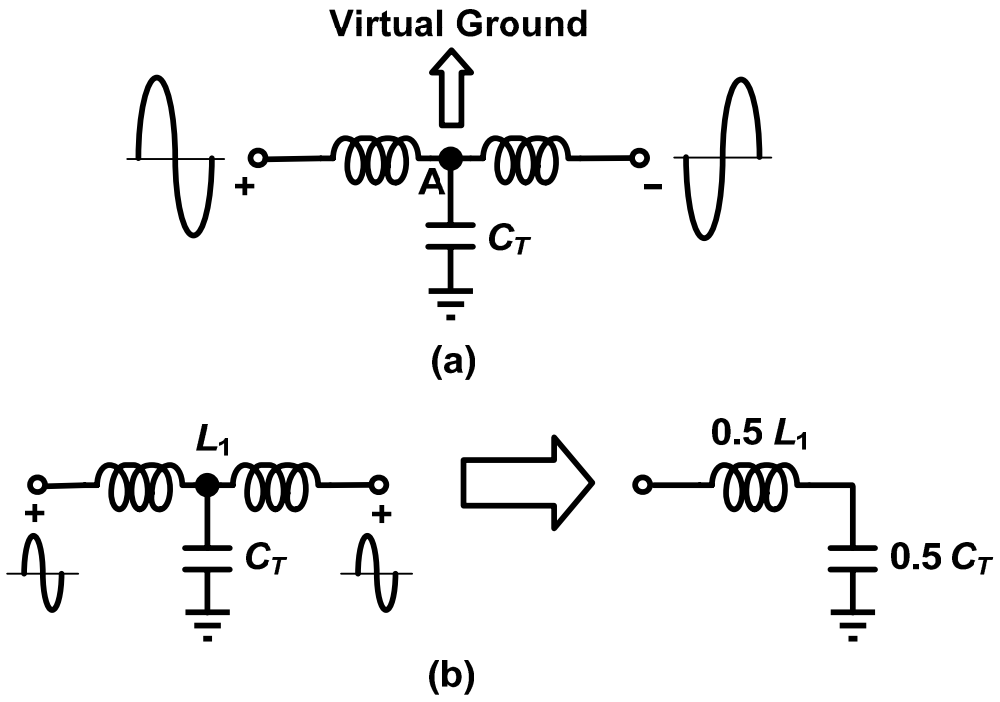


Fig. 5.6 Influence of the capacitor C_T for (a) the fundamental signal and (b) the second harmonic signal.

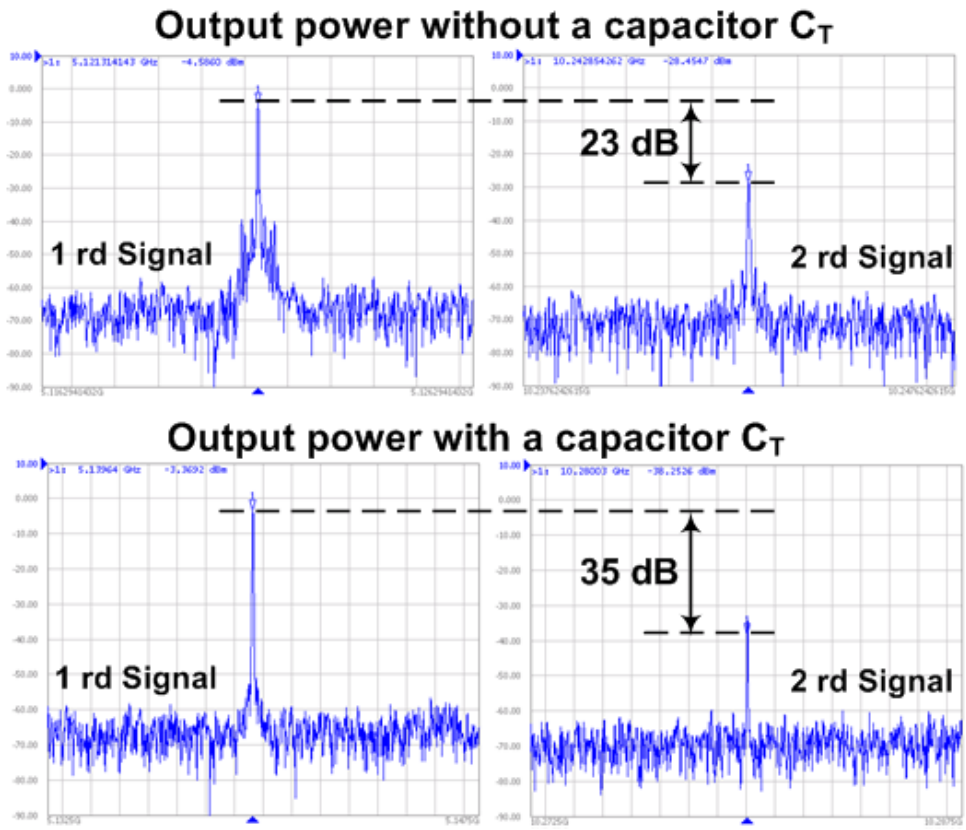


Fig. 5.7 Measured output signals with and without the capacitor C_T .

On the other hand, the $1/f^3$ corner in phase noise spectrum can be given from [69]

$$\omega_{1/f^3} \approx \omega_{1/f} \cdot \left(\frac{c_0}{c_1}\right)^2 = \frac{K}{C_{ox}WL} \cdot \frac{g_m^2}{\gamma \cdot g_{do}} \cdot \frac{1}{4kT} \cdot \left(\frac{c_0}{c_1}\right)^2 \tag{5.1}$$

where $\omega_{1/f}$ is the corner of the transistor $1/f$ noise and c_0 and c_1 represent first and second Fourier series coefficients of the impulse sensitivity function (ISF). From (5.1), the $1/f^3$ corner of the phase noise spectrum can be reduced by selecting a larger channel width W; however, this will indirectly increase the value of the transconductance g_m, which is proportional to the size of transistor. To overcome this drawback, here we introduce the additional bulk bias voltages V_{bp} and V_{bn} of the transistors, as shown in Fig. 5.3, for further obtaining a smaller g_m. By providing an appropriate bulk bias voltage, the threshold voltage can effectively be raised to diminish the current of transistor since the threshold voltage is governed with the body effect.

Fig. 5.8 shows the simulated results of phase noise characteristics with and without improvement. It can be observed and demonstrated that a 15 dB decrease at 10 kHz offset frequency can be attained due to the usage of a larger capacitor C_1, an extra capacitor C_T, and the appropriate bulk bias voltage V_b.

5.3 EXPERIMENTAL RESULTS

The microphotograph of the low-power VCO fabricated by 0.18-μm TSMC CMOS process is shown in Fig. 5.9. The core chip area is 0.33×0.45 mm^2, and the core dc power dissipation is 1.9 mW. The value of R_o in the proposed VCO is set as 50 Ω to achieve output match for testing purposes. The fabricated VCO is measured

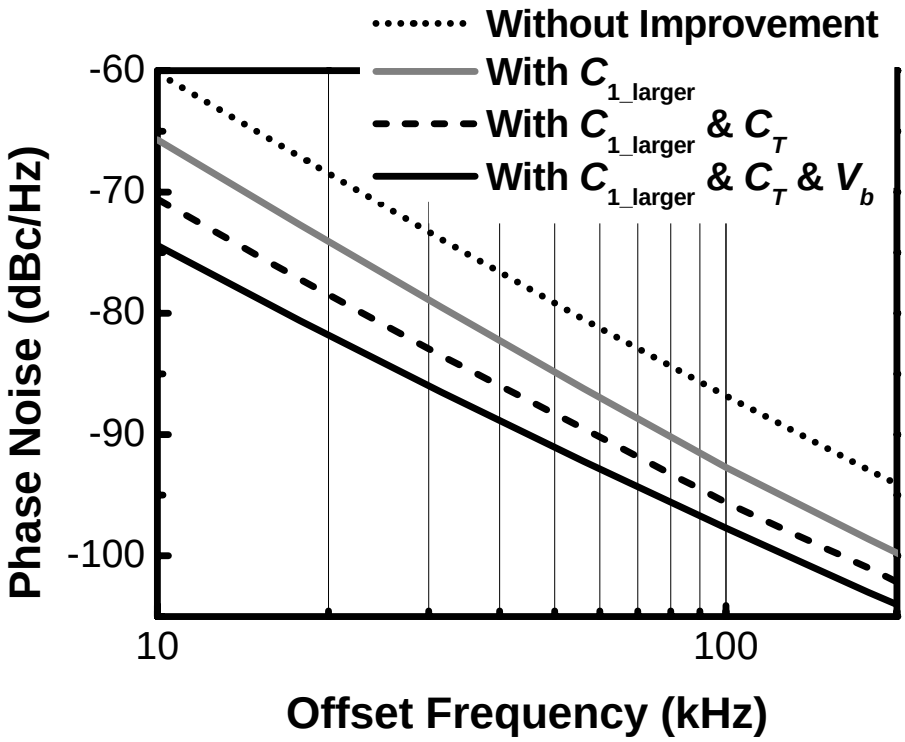


Fig. 5.8 Simulated phase noises with and without improvement.

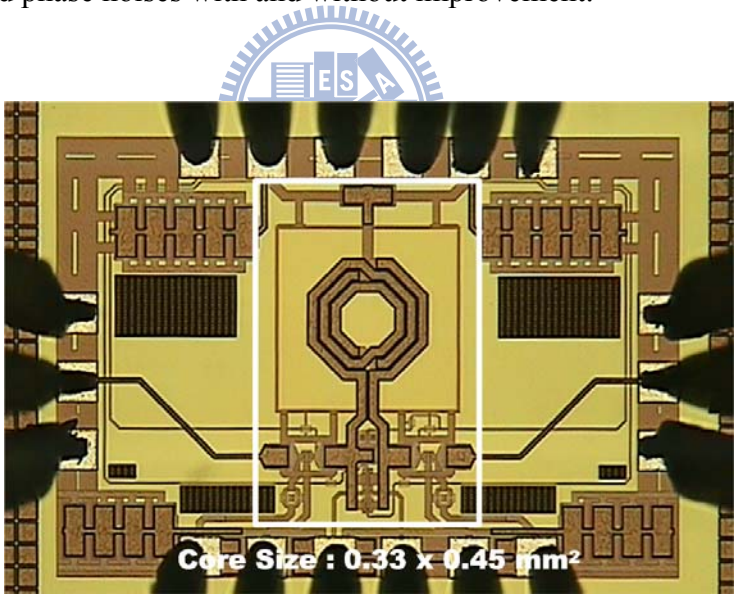


Fig. 5.9 Microphotograph of the VCO with 0.33×0.45 mm^2 core die area.

with an Agilent E5052A signal source analyzer. Fig. 5.10 depicts the measured and simulated oscillation frequencies, which shows a tuning range of 240 MHz from 5.12 GHz to 5.36 GHz when the tuning bias voltage V_{ct} is between 0 V and 1.3 V. The measured phase noise, as shown in Fig. 5.11, is about -119 dBc/Hz at 1 MHz offset

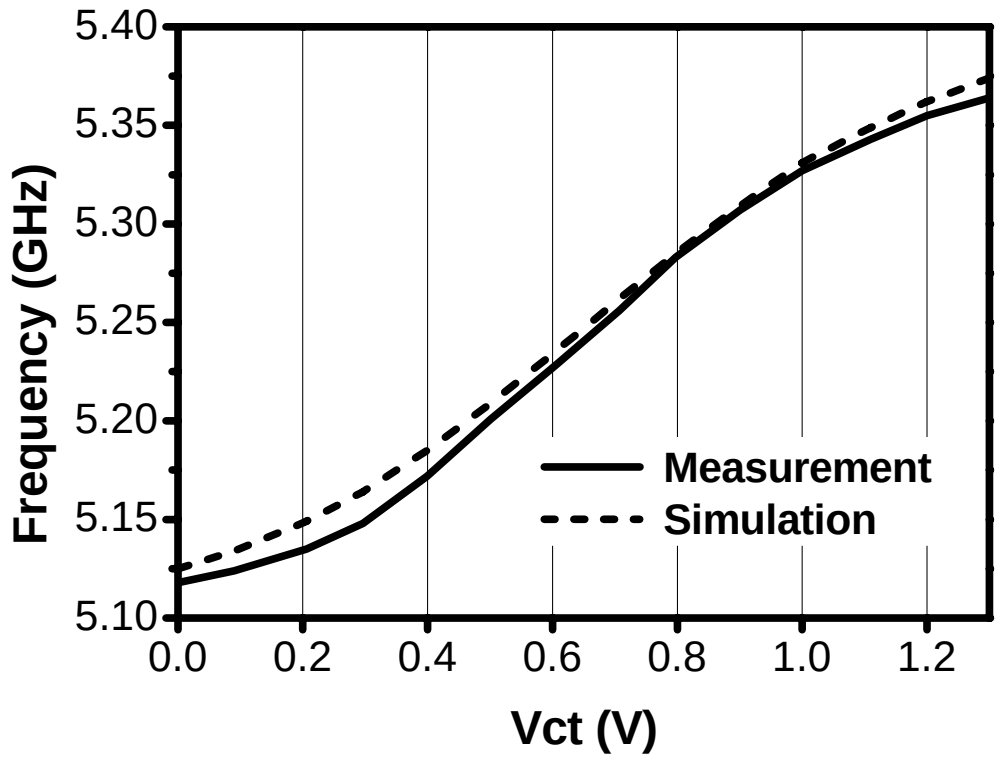


Fig. 5.10 Measured and simulated tuning ranges of the proposed VCO.

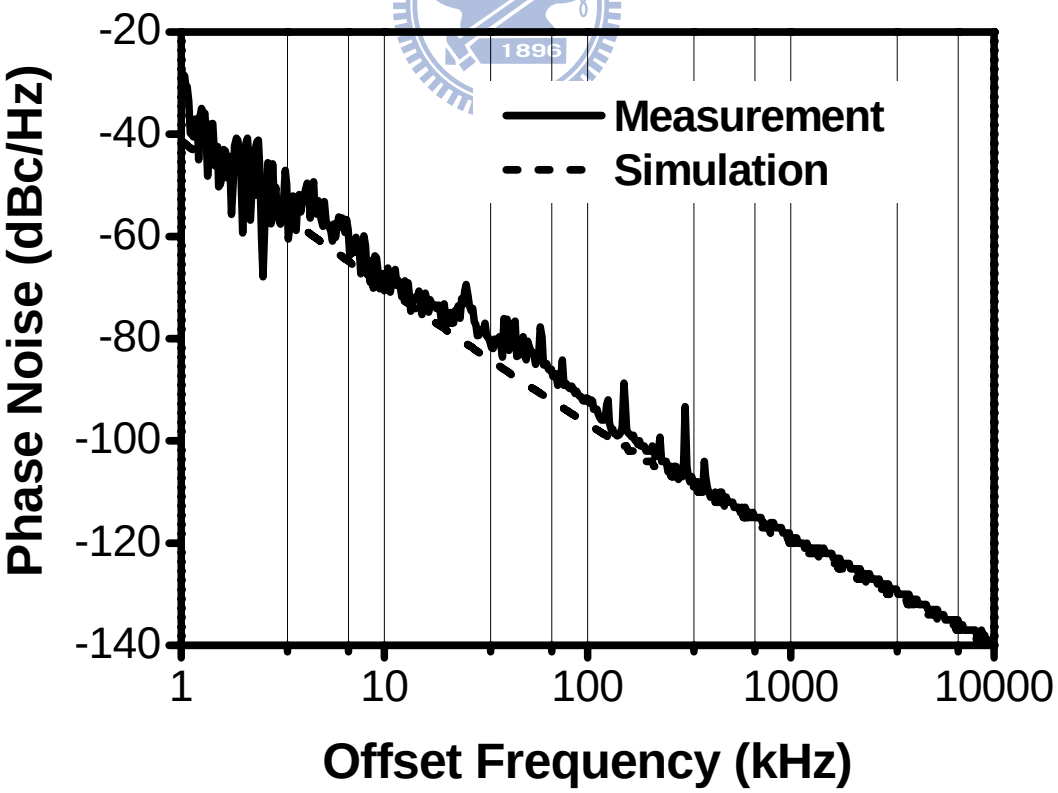


Fig. 5.11 Measured and simulated phase noises of the proposed VCO.

frequency with the center frequency at 5.14 GHz and an output power of -2.4 dBm. In addition, the FOM has been used and defined as follows to compare the performances of VCOs [70]:

$$\mathrm{FOM} = L\{f_{\mathrm{offset}}\} - 20\log\left(\frac{f_{\mathrm{c}}}{f_{\mathrm{offset}}}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1\mathrm{mW}}\right), \tag{5.2}$$

where $L\{f_{\mathrm{offset}}\}$ is the measured phase noise at an offset frequency f_{offset} from f_{c} carrier frequency, and P_{DC} is the total VCO power dissipation in mW. Following this definition, the measured FOM of the proposed VCO is -190 dBc/Hz at the offset frequency of 1 MHz.

5.4 SUMMARY

A low-power VCO with phase noise improvement has been designed and fabricated using 0.18-μm CMOS technology. Based on the current-reused configuration, a larger value of capacitor C_1, an additional capacitor C_T, and the appropriate bulk bias voltage V_b of the transistor are adopted to achieve a better phase noise performance. The measured results of the proposed VCO agree quite well with the simulated results. The performances of the VCO are listed in Table 5.1 and compared with those of others.

Table 5.1
Performance summary of the low phase-noise VCOs

Ref.	Tech.	Freq. [GHz]	PN @1Mz [dBc/Hz]	P_{diss} [mW]	Area [mm^2]	FOM [dBc/Hz]
[70]	0.13 μm CMOS	5.98	-115	12.5	-	-180
[71]	0.18 μm CMOS	4.5	-122.5	6.75	0.55	-187
[72]	0.18 μm CMOS	5.1	-116.7	3.9	0.5	-185
[73]	0.18 μm CMOS	5.6	-110.8	8.3	0.5	-177
[74]	0.18 μm CMOS	5.2	-113.7	9.7	0.35	-180
This work	0.18 μm CMOS	5.25	-119	1.9	0.15	-190

CHAPTER 6

CONCLUSIONS

In this thesis, the design methodologies and implementations of key CMOS RFICs including two triple-band LNAs, a dual-band image rejection mixer, three low-power UWB LNAs, and a VCO for multiband and UWB communication systems are proposed.

Firstly, the design of two triple-band LNAs with switched resonators is presented and fabricated in a TSMC 0.18-μm CMOS process. The proposed triple-band LNAs are demonstrated the feasibility to effectively decrease the size of multi-band RF systems by using a switched component. In addition, the feedback noise-canceling technique and the noise reduction resistor R_B will effectively diminish the output noise power density. It can be observed that 1.5/1.3/1.1 dB noise figure decrease can be attained at 2.5/3.5/5.2 GHz in the second LNA without extra dc power and CMOS process steps.

Secondly, a 2.45/5.2 GHz image rejection mixer with differential dual-band third-order notch filter has been fabricated and designed. The proposed differential dual-band image rejection circuitry is employed for the 2.45/5.2 GHz WLAN application to effectively diminish the dc power consumption and complexity of circuit design compared to the traditional Hartley or Weaver architectures. Moreover, the cross-connected pair consisted of NMOS and PMOS transistors in the proposed notch filter will further ameliorate the image rejection capability. The suppression of about 36/45 dB at the image frequencies can be achieved without worsening the in-band characteristics.

Thirdly, three low-power UWB LNAs using 0.18-μm CMOS technology are

presented. Extra transmission zeros are created in the first UWB LNA due to the use of a *LC* input network with additional capacitors C_{RH} and C_{RL} for improving the higher and lower out-band performances respectively. Moreover, a feedback structure and dual-band notch filter with low power active inductors will further attenuate the outband interferers without deteriorating the input matching bandwidth in the second UWB LNA. The 55/48/45 dB maximum rejections at 1.8/2.4/5.2 GHz, a power gain of 15 dB, and 3.5 dB minimum noise figure can be measured while consuming a dc power of only 5 mW. Finally, a new matching technique by selecting an appropriate width of the transistor M_2 is presented to further ameliorate the noise figure performance in the third UWB LNA. The IC prototype achieves good performances such as a power gain of 16.2 dB, a better than 10 dB input return loss, and 2.3 dB minimum noise figure while consuming a dc power of only 6.8 mW.

Finally, a low-power 5.25 GHz VCO with phase-noise improvement is designed in a 0.18-μm CMOS 1P6M process. Based on the current-reused configuration, a larger value of capacitor C_1, an additional capacitor C_T, and the appropriate bulk bias voltage V_b of the transistor are adopted to achieve a better phase noise performance. A good FOM of -190 dBc/Hz can be achieved without extra chip area and CMOS process steps. The fabricated VCO operates from 5.12 to 5.36 GHz with a power consumption of 1.9 mW and active chip area of 0.15 mm^2. The measured phase noise at 1 MHz offset is about -119 dBc/Hz.

APPENDIX

Abbreviation	Full name
ADS	Agilent Advanced Design System
CMOS	Complementary Metal Oxide Semiconductor
FCC	Federal Communications Commission
FOM	Figure of Merit
GSM	Global System for Mobile
ICP	Inductively Coupled Plasma
IP_{1dB}	Input-referred 1-dB Compression Point
IIP_3	Third-order Input Intercept Point
ISF	Impulse Sensitivity Function
LNA	Low-Noise Amplifier
MB-OFDM	Multi-Band Orthogonal Frequency Division Multiplexing
MIMO	Multiple-Input, Multiple-Output
OFDM	Orthogonal Frequency-Division Multiplexing
RSSI	Received Signal Strength Indicator
RFICs	Radio Frequency Integrated Circuits
SSB	Single Sideband
TSMC	Taiwan Semiconductor Manufacturing Company
UWB	Ultra-WideBand
VCO	Voltage-Controlled Oscillator
WiMAX	Worldwide Interoperability for Microwave Access
WiFi	Wireless Fidelity
WLAN	Wireless Local Area Network

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