國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

應用於直流至直流切換式電源供應器積體電路設計之先進控制及保護技術

ADVANCED CONTROL AND PROTECTION TECHNIQUES FOR DC-DC SWITCHED MODE POWER SUPPLY IC DESIGN

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中 華 民 國 九 十 六 年 七 月


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摘要

在本論文中，我們探討了應用於直流至直流電源轉換的切換式電源供應器。首先簡單介紹了非隔離式直流至直流切換式電源供應器的基本架構，並且探討了電源供應器運作上的安全問題，也簡單介紹了電源供應器的設計規格。基於這些有關直流至直流切換式電源供應器的基本知識，我們開發了數種電路技術。這些電路技術提高了能量轉換效率、縮小電源供應器體積並且可以操作在相當廣的範圍。此外，這些電路技術也提供了快速瞬變反應以及安全的操作。我們將這些新開發的技術以一個單晶片電流模式控制的降壓轉換器來實現。這些電路技術可以被應用到其它架構如昇壓或昇降兩用型的切換式電源供應器設計，特別是應用於積體電路電源轉換器設計上。

我們提出了一個可整合於單晶片上的柔性啟動電路，它並不需要額外的針腳並且只佔了很小的晶片面積。這個電路以串聯金氧半電晶體及一個內建於晶片上的小電容來達到數毫秒到數十毫秒的柔性起動時間。此柔性啟動電路可以防止電源供應器啟動時的突波電流，並且在縮小電源供應器體積的同時仍保障了安全

性。此電路的另一好處是它非常簡單，因此可以很容易應用於其它的電源供應積體電路設計。

另外，我們也提出了動態部分停工策略，這個策略充分利用了切換式電源供應器的特性。它降低了對輸入電流的浪費，同時卻仍保持電路的性能。此動態部分停工策略提昇了轉換效率，特別是在輕載的時候。因此由電池供電的設備其待機時間可因應用此策略而拉長。根據我們的實驗，當此策略與突波頻率調變共同使用時，其轉換效率可由 62 % ~ 75 %提昇至 84 % ~ 89 %。

在我們的設計中，我們採用了一種基於電流傳送器的近無功耗電流感測技術來實現我們的電流模式控制。我們也充分利用了這個電流感測技術的特性而開發了新的斜率補償電路和過電流保護電路。我們所提出的斜率補償電路較傳統電路而言大幅降低了電路的複雜度，因此節省了晶片面積。在此同時，也因為減少了訊號轉換的次數而降低了訊號的失真。至於過電流保護電路也較傳統電路大為簡化。此過電流保護電路的特長為面積小、功耗低及反應速度快，因此可確保電源供應器的安全性。此外，所提出的斜率補償電路和過電流保護電路都很容易因應不同的需求來加以設計並調整，因此對切換式電源供應器而言，我們可以得到很好的電壓調節並且能適用於廣泛的操作範圍。對於不同的切換式電源供應器架構也能適用。

這些技術加上一些基本的保護電路都整合於一個示範性晶片上。根據量測結果，我們可以得知這些技術確實發揮了它們的功效。在此我們提出了一個最高可達 96.7 %轉換效率的單晶片直流至直流電流式控制降壓轉換器。我們提出了以較低功耗達到快速電路反應的動態部分停工策略以增進轉換效率。突波寬度調變和突波頻率調變的自動切換並配合動態部分停工策略更進一步提昇了輕載時的轉換效率。電流偵測電路和斜率補償電路則簡化了電流式控制電路並加快了反應速度。一個高速過電流保護電路也根據此電流偵測電路而發展出來。新的整合式柔

性啟動電路不需額外元件就能有效地防止啟動時的突波電流。我們設計的直流至直流轉換器已採 0.6 微米的互補式金氧半製程製作出來，晶片面積為 1.35 毫米平方，而控制器部分佔 0.27 毫米平方。實驗結果顯示此新式柔性啟動電路具有 1.5 毫秒以上的柔性啟動時間，因此有效地抑制了啟動時的突波電流。此轉換器可在 2.2 至 6 伏特的輸入電壓下操作，切換頻率為 1.1 百萬赫。在輸出電流為 0.9 至 800 毫安培時具有 88.5 ~ 96.7 %的轉換效率，而在輸出電流為 1000 毫安培時仍有 85.5 %的轉換效率。

ADVANCED CONTROL AND PROTECTION TECHNIQUES FOR DC-DC SWITCHED MODE POWER SUPPLY IC DESIGN

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ABSTRACT

In this dissertation, we discuss about the switched mode power supply (SMPS) for DC-DC power conversion. Basic topologies of non-isolated DC-DC SMPS are introduced. Safety considerations for power supply design are discussed. The design specifications are also included. Based on the knowledge of DC-DC SMPS, we developed several new circuit techniques to achieve high conversion efficiency, compact converter size, wide operating range, fast transient response and safety operation. These developed circuit techniques were realized in a monolithic current-mode buck converter. The application of these circuit techniques can be extended to other topologies like boost and buck-boost of SMPS design, especially in integrated circuit power converter design.

The on-chip soft-start circuit occupies a small silicon area and eliminates the need of extra pin-out. This circuit achieves one to tens of milliseconds soft-start time

using series MOS transistors and a small on-chip capacitor. This circuit prevents the inrush current during the start-up of the power module. It provides safety operation and shrinks the converter size in the same time. Another benefit of the proposed circuit technique is that because of its simplicity, it can be easily adopted for any other power supply IC design.

The dynamic partial shutdown strategy (DPSS) is a power management strategy. By exploiting the switching characteristics of SMPS, we developed this strategy. This strategy eliminates the unwanted waste of operating current and keeps the circuit performance at the same time. The DPSS improves the conversion efficiency especially in light load operation. Thus the standby time of battery operated devices can last longer by utilizing DPSS. Combined with the pulse frequency modulation (PFM) mode, the conversion efficiencies are improved from 62 % ~ 75 % to 84 % ~ 89 % measured in our test chip.

In our design, we choose a quasi-lossless current conveyor based current sensing technique to implement our current-mode control. By exploiting the characteristics of this current sensing technique, we developed the slope compensation circuit and the over-current protection circuit. The proposed slope compensation circuit has reduced circuit complexity than traditional ones thus the silicon area is saved. The signal distortion is also reduced because we eliminate the multi-conversions of signals. The over-current protection is also simpler than traditional ones. The benefits of the over-current protection circuit are reduced silicon area, reduced power consumption and faster response for safety operation. Additionally, these circuits can be easily designed and adjusted. So we can achieve good regulation and wide operating range. These circuit techniques can also be applied to other topologies for different

applications.

Incorporating with other basic protection schemes, the above techniques are integrated into a demo chip. From the measurement results, we can see the effectiveness of these developed techniques. A monolithic current-mode pulse width modulation (PWM) step-down DC-DC converter with 96.7% peak efficiency is presented. The high efficiency is achieved by DPSS which enhances circuit speed with less power consumption. Automatic PWM and PFM switching boosts conversion efficiency during light load operation. The modified current sensing circuit and slope compensation circuit simplify the current-mode control circuit and enhance the response speed. A simple high-speed over-current protection circuit is proposed with the modified current sensing circuit. The new on-chip soft-start circuit prevents the power on inrush current without additional off-chip components. The DC-DC converter has been fabricated with a 0.6 μm CMOS process and measured 1.35 mm^2 with the controller measured 0.27 mm^2. Experimental results show that the novel on-chip soft-start circuit with longer than 1.5 ms soft-start time suppresses the power-on inrush current. This converter can operate at 1.1 MHz with supply voltage from 2.2 V to 6.0 V. Measured power efficiency is 88.5 ~ 96.7% for 0.9 mA to 800 mA output current and over 85.5% for 1000 mA output current.

致謝

『耶和華是我的牧者；我必不致缺乏。祂使我躺臥在青草地上，領我在可安歇的水邊。祂使我的魂甦醒，為自己的名引導我走義路。我雖然行過死蔭的幽谷，也不怕遭害，因為你與我同在；你的杖，你的竿，都安慰我。在我敵人面前，你為我擺設筵席；你用油膏了我的頭，使我的福杯滿溢。我一生一世必有恩惠慈愛隨著我，我且要住在耶和華的殿中，直到永遠。』（聖經 詩篇二十三篇）

『這不是說，我已經得著了，或已經完全了，我乃是竭力追求，或者可以取得基督耶穌所以取得我的。弟兄們，我不是以為自己已經取得了，我只有一件事，就是忘記背後，努力面前的，向著標竿竭力追求，要得神在基督耶穌裏，召我向上去得的獎賞。』（聖經 腓立比書三章 12~14 節）

感謝主耶穌一路帶領我、保守我，在每一天、每一件事上都看顧我，帶領我完成學業，並使我生命長大。

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馬鳳飛

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

The discovery of electric power changes our life. Different types of energy such as heat energy, potential energy, kinetic energy and other types of energies, can be transformed to electric power. This makes the storage, the transportation and the transformation of energy easier. Through many years, people invent devices that utilize electric power. The supply lines stretch into buildings so that the usage of electric power becomes more convenient. The batteries, which store the electrical energy, make the portable devices popular. Today, we use electrical energy everywhere in our daily life.

Power electronics is an established technology that bridges the power industry with its need for fast controllers, and the semiconductor industry with its attempt to produce devices with greater power handling capabilities. In essence, what power electronics does is to condition the power from a supply to suit the needs of the load.

Power conditioning is known also as power modulation or power conversion. This conditioning may take a specialized form such as the regulation of voltage, or the conversion of alternating current (AC) to direct current (DC), or the conversion of direct current to alternating current.

There is no one configuration of the power electronics system to satisfy all types of conditioning. This becomes evident as a number of systems are considered. Indeed, the conversion of one given type of supply (usually specified by voltage and frequency) into any other type of supply has to be designed on its own merits.

All electronic circuits need a supply of power. For low power consumption units or for portable operation, a battery is often used – a solar cell may even be enough. Higher power circuits are normally powered from the AC mains supply. In almost all cases the power requires conversion to the appropriate DC voltage by an electronic power unit, which is usually switched mode in operation.

Over the past 20 years, there have been significant changes in the design of power supplies. The most important of these has been the widespread change from linear power supplies to those that operate on a switching basis – so called Switched Mode Power Supplies (SMPS). The principal reason for the move to SMPS is their much greater efficiency – typically 80-90 % as opposed to 30-40 % for linear units. This greatly reduces the cooling requirements, and allows a much higher power density. [1]-[13]

The concept of high frequency switching of transistors to provide a controllable DC output has been around for some time. What has allowed the widespread adoption of SMPS technology has been the availability of a range of suitable active and passive components. The advent of MOSFETs with high power rating has been a particularly important advance, together with the availability of high-speed diodes and improved magnetic materials. Now circuits can be designed to operate at switching frequencies into the megahertz range, with consequent reductions in cost and in volume of the power supply.

Advances in power supply design and manufacture have had to keep pace with advances in the electronic systems they supply. The requirement for portability has led to demands for more compact units with reduced losses, and the trend towards lower operating voltages has proved particularly demanding. In addition, regulations relating to safety and electromagnetic compatibility are becoming increasingly more stringent. Designers and production engineers have proved to be up to the task and a wide range of innovative techniques are now standard in the electronic power supply industry. Size and unit costs have been reduced while reliability has been increased. Efficiency has been improved by the use of new active components, new circuit topologies and new ways of manufacture.

1.2 LOW POWER DC-DC CONVERSION

Although the power electronics include so many interesting topics that can be studied, we can only focus on a small part of them. In this thesis, we will discuss about lower power DC-DC conversion, especially switched mode conversions.

The rapid advances in computer, communications, and consumer electronics technology are having a major impact on our everyday life. This trend has been largely due to recent advances in emerging VLSI and ULSI semiconductor technology. Most of these integrated circuits need a DC power supply, but usually in different voltage levels. In most cases, we have only one power source – An adaptor or a battery. Thus we have to consider the need of DC-DC conversions as follows.

The demands for higher functionality, smaller device size, and lower power dissipation have brought new technological issues. They can be resolved using more advanced semiconductor processes to implement the so-called system-on-a-chip

(SOC). The processes have been improved from 0.35 μm to 0.25 μm, 0.18 μm, 0.13 μm, 90 nm, 65 nm and even smaller for commercial products. By utilizing these advanced processes, more circuits can be implemented into one single chip and system size and complexity are greatly reduced. As the dimension of transistor continues to shrink, the gate oxide thickness of MOSFET also becomes thinner. To prevent electric breakdown, the maximum allowable supply voltage has dropped with each generation of semiconductor technology. For example, it is 3.3 V for 0.35 μm technology and 1.8 V for 0.18 μm technology. The operating voltage of an integrated circuit requires scaling down in order to maintain the reliability.

Another reason to perform DC voltage conversion is supply voltage boosting in portable equipment especially for lightning the screen. Small size and light weight portable equipments such as notebook computers, cellular phones, digital cameras, MP3 players and personal digital assistants (PDA) provide convenient data access, communication and entertainment functions. The size and weight limitations restrict the number of battery cells. Thus, the input voltage provided by the batteries may be lower than the required supply voltage. Step-up voltage conversions are required at this time. Considering the above cases, we need multiple DC-DC converters to generate sufficient outputs to fit the need.

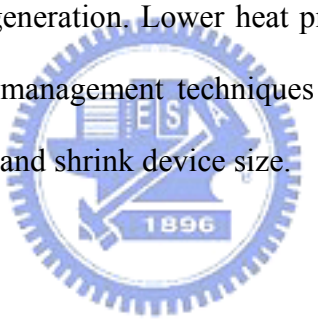
1.3 TRENDS AND CHALLENGES OF DC-DC CONVERTER DESIGN

Today, high performance, long operating time, compact size and low cost are essential factors of a successful electronic product. For example, it is expected a smart phone can process extensive multimedia data with standby time of a week and size of

the palm. These requirements challenge traditional power supply control techniques and converter design. In this section, trends and challenges of DC-DC converter design are described.

1.3.1 High Efficiency

While transistor numbers inside a single chip continues to double every 18 months as Moore's Low predicts, energy density of batteries has increased little. Conversion efficiency is particularly important in battery-powered equipments. Improving conversion efficiency can directly prolong the operating time of portable devices with the battery capacity unchanged. Higher conversion efficiency also helps to reduce the unwanted heat generation. Lower heat production saves space for heat ventilation. Advanced power management techniques and converter circuits design will help to extend battery life and shrink device size.



1.3.2 Compact Size

Reducing size and weight is one of the major demands of portable devices. In addition to improving efficiency, we need to consider other ways to reduce the space and weight occupied by power converters.

Generally, switched mode converters are composed of many discrete components that occupy large space. Since physical size minimization is a major design objective in portable devices, reductions of external component counts and size are trends of SMPS design [14]-[15]. Significant energy is dissipated in the parasitic impedances of external interconnection and components [16]. Therefore, integrating external components decreases energy loss. Higher switching frequency can reduce

the required sizes of filter inductor and capacitor and also improve efficiency [17]. Further physical size minimization can be made by integrating controller into other circuits [18]-[19].

1.3.3 Low Output Voltage and Low Noise

In portable and high performance systems, electronic systems are designed to operate at the optimal supply voltage [20]. Low operating voltage of new generation integrated circuit has set tight tolerance of converter's output. Communication and audio circuits are also sensitive to noise interference. Low output ripple and low noise are essential. Fast transient response is required to prevent large output deviation during step load transient. In addition, fixed frequency operation of switched mode converters is favorable, because it is easier to filter out switching noise.

1.3.4 Wide Operating Range

Many portable devices can be powered by multiple input sources such as AC adapter and battery. These power sources may have different voltage levels. Besides, the voltage of a battery can vary significantly from full charged state to run out of stored electrical energies. The DC-DC power converters must operate under these conditions and keep the output voltage well regulated. All the circuits of the converter controller and the power switches must have a wide operating range to ensure safety and stable operation of the devices supplied by the converter.

1.3.5 Fast Transient Response

Microprocessors today exhibit much heavier load and faster current slew rate. Advanced power management techniques are usually adopted. When the system is in

sleep mode, come circuits are shut down and operating voltage is scaled down in order to minimize standby current. The most challenging issue comes from step load transients when the system transits from sleep mode to full loading mode. These two modes correspond to minimum and maximum loading conditions respectively. The regulator has to maintain output voltage within tight tolerance during this fast slew-rate transient. These power requirements have become new challenges. [21]-[25]

1.3.6 Safety Operation

System designers naturally wish to avoid any system faults occurring due to the power supply, so the specifications for the power supply normally include large safety margins. As the power supply will have its own safety margins, it is often grossly over-specified, and as a result is considerably larger, heavier and more expensive than is necessary.

On the other hand, any electronic system requires a power source in order to function correctly, yet the power supply is normally the most neglected part of the complete system. It is often hastily designed (or bought in) after the rest of the system is complete, and placed in the leftover space, which is often too small and has inadequate ventilation for cooling purposes. How to provide safety operation using simplest circuits and occupying least space is one of the challenges of power converter design.

1.4 MOTIVATION

As described in section 1.3, a desirable DC-DC converter has high efficiency, compact size, wide operating range, fast transient response and can operate safely.

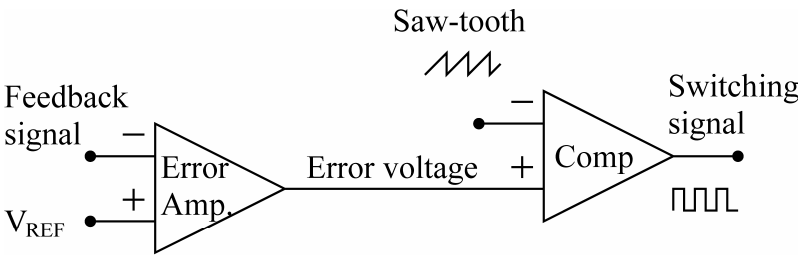


Fig. 1.1 Voltage-mode control in SMPS

There are many control methods and circuits developed to meet these requirements. But each one has some disadvantages. For example, voltage-mode control is one of the commonly used control method in SMPS (Fig. 1.1). Design of this control scheme is simple and straightforward. It has only one feedback loop and is easier to design and analyze. The output voltage is controlled by directly changing the duty ratio. Therefore, this control scheme is also called direct duty control. It can provide good noise margin if you use a large amplitude ramp in determining the duty ratio. It also has low impedance output and can provide good line regulation, load regulation and even cross regulation for multiple outputs. However, its application is limited because any change in line or load must first be sensed as an output change and then corrected by the feedback loop. This usually means slow response. Another disadvantage is that the output filter adds two poles to the control loop. We need to add a dominate-pole in much lower frequency or add a zero to compensate it. The loop gain varies with the input voltage also makes the compensation difficult.

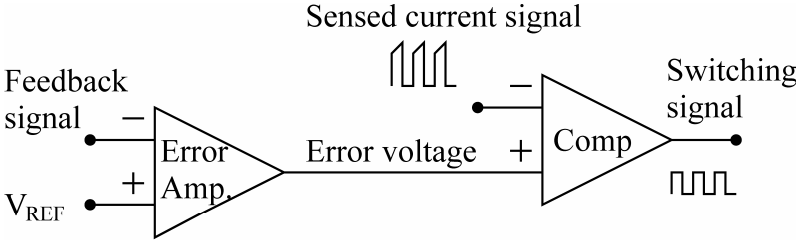


Fig. 1.2 Current-mode control in SMPS

Another popular method is current-mode control, which is also called current programmed control and current injected control, was introduced in 1978 [26]-[35] (Fig. 1.2). Since the inductor current rises with a slope determined by input and output voltages, this waveform will respond immediately to line voltage changes, eliminating both the delayed response and gain variation with changes in input voltage. This control scheme utilizes dual loops to control both output voltage and inductor current. It effectively eliminates the phase lag of the filter inductor and makes loop compensation easier. Since the current information is sensed cycle-by-cycle, we can see an additional benefit of easier cycle-by-cycle current limiting. The current-mode control has shown more attractive characteristics than voltage-mode. However, current sensing elements not only require additional circuitry but also reduce efficiency. Moreover, switching noise can easily corrupt the sensed current signal. Therefore, instability caused by noise is common in a current-mode system [36]-[37]. Instability problem also occurs at very low duty ratio caused by high input voltages and low output voltages.

There are still many other methods of implementing SMPS. All these circuits have their own advantages and disadvantages. We choose current-mode control as our start point and try to investigate the possibility of eliminating the disadvantages. We want to find a way that a high efficiency, compact size and safely operated SMPS can be easily designed for different applications.

1.5 RESEARCH GOALS AND CONTRIBUTIONS

As being power electronics engineers, providing good quality electrical power is our responsibility. How to improve the quality of supplied power with lower cost is

our research goal. Fast response, tight regulation, high efficiency, high stability, compact size and safety operation are the key factors of a high performance power converter. We focus on the integrated circuit implementations. We had implemented a monolithic current-mode buck converter using the new developed control and protection circuits. All the developed techniques can be reused in the SMPS IC design for other applications. The original contributions of this work are in three main points.

First, the on-chip soft-start circuit which occupies small silicon area and do not need extra pin-out. This circuit helps to protect the power source and the converter itself at the very beginning of the power on of the converter. It eliminates the inrush current when the converter is powered on. The inrush current may cause severe voltage drops at the power source and may cause the system faults or other damages to the power source, the circuit directly powered by the power source and the converter. Traditional circuit utilized a big capacitor or other costly circuit to do soft-start. Our approach using a simple circuit and only occupies a very small silicon area to achieve the same function as well as the traditional circuits.

Second, the Dynamic Partial Shutdown Strategy (DPSS), which increases the conversion efficiency especially in light load operation. The power conversion efficiency is very important especially for portable devices that utilize batteries as their power sources. The DPSS successfully reduces the operating current wasted by the control circuits. The efficiency is improved especially in light load operation. This means a longer standby time can be achieved using this strategy.

Third, the slope compensation and the over-current protection circuits which take advantage of the existing current sense method. As described in section 1.4, the current sense circuits usually cause power loss and greatly reduce the conversion

efficiency. We choose a quasi-lossless current sense circuit to improve the efficiency in the current-mode control. At the same time, the current sense circuit helps the development of the new slope compensation and over-current protection circuits. Although the compensation of current-mode control has more flexibility, it is not easy to implement a stable current-mode SMPS because of its inseparable dual feedback loop. The slope compensation in the current-mode control was developed for stabilize the current-mode converter. Traditional methods of implementing slope compensation are complex and may induce signal distortion in the control loop. We proposed a simple circuit to improve the slope compensation. The new over-current protection circuit also takes advantages of the current sense circuit. This simple circuit provides fast response to ensure safety operation under over-loaded conditions by very low power consumption.

1.6 THESIS ORGANIZATION

In this thesis, we introduce the basics terms of the switched mode DC-DC power supplies in chapter 2. Some fundamental topologies of a switched mode DC-DC power supply like buck, boost and buck-boost are introduced. The modulation schemes of SMPS are briefly listed. The specifications of SMPS give us an evaluation standard of the performance of the SMPS.

In chapter 3 we demonstrate the advanced control and protection circuits in a monolithic current-mode buck converter. The newly developed strategies and circuits are discussed in this chapter. All of them can be easily adopted for integrated SMPS in different topologies and for different applications. The on-chip soft-start circuit, the dynamic partial shutdown strategy, the current sense circuit, the slope compensation

circuit and the over-current protection circuit are all realized in this monolithic converter. The performances are measured to show the practicability and effectiveness of them. We can see a compact size, high efficiency and well-protected converter illustrated in this chapter.

Chapter 4 presents the practical considerations in circuit design and silicon layout of a power converter integrated in single chip. Many practical issues such as switching noise, on-resistance of integrated power switches and some other protection considerations are discussed. These issues seem unimportant, but they may cause unstable operation, performance degradation and even destroy the converter or the system. In this chapter, we deal with these issues and give practical suggestions according real experience.

Chapter 5 concludes this work and tries to suggest for future works.

Chapter 2

SWITCHED MODE DC-DC POWER SUPPLY BASICS

2.1 REGULATED DC POWER SUPPLIES

There are two basic ways of maintaining a fixed output voltage in a DC power supply, i.e. by series and shunt regulators [5].

The principle of the series regulator is illustrated in Fig. 2.1 (a). Here you have an unregulated DC input, V_{IN}, feeding through a series-control circuit, *A*, to give a fixed regulated DC output, V_{OUT}. The series-control circuit works by adjusting the voltage drop from input to output to keep a constant voltage at the output. This variable series voltage drop takes up both variations in the input voltage, and varying voltage drops inside the system arising from changing load currents. The variable resistor symbol in the circuit block, *A*, emphasizes that the series regulator works like a variable resistor in series with the load, adjusting itself to keep the output voltage across the load constant.

The shunt regulator works on a different principle, illustrated in Fig. 2.1 (b). Here an unregulated DC input feeds a current through a series resistor, R_S, to give a lower DC voltage across the load resistor R_L. The shunt-control element, *B*, draws current from the output rail, as does, of course, the load R_L. The shunt-control element adjusts the current it takes so that the voltage drop across the series resistor R_S varies

to keep the output rail voltage, V_{OUT}, unvarying under changes of load resistance and unregulated input voltage, V_{IN}. Once again the control element can be seen to work like a varying resistor as indicated by the symbol in the shunt circuit block, *B*, in the diagram.

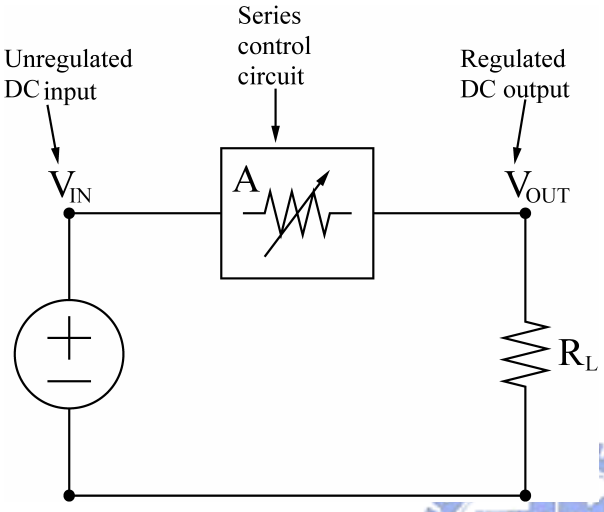


Fig. 2.1 (a) Series regulated power supply.

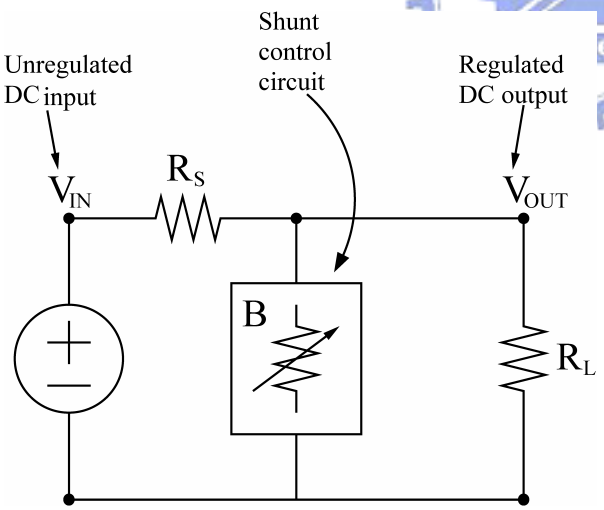


Fig. 2.1 (b) Shunt regulated power supply.

In essence, the series regulator soaks up changes in the voltage drop from the input supply onward to the output, while the shunt regulator soaks up current variations in the load. In each case the net result is the same: the output voltage is regulated, i.e. held constant, at a fixed value.

In nowadays, there are mainly two types of regulated DC-DC power supplies. One of them is linear regulated power supply and another is switched mode power supply.

2.1.1 Linear Regulated Power Supplies

Linear regulated power supplies is a simple, widely used DC-DC regulator. In linear regulators, the controlled resistor (series or shunt) elements described above continuously dissipate some power in keeping the output voltage constant under varying input voltage and output load conditions. Fig. 2.2 (a) and (b) show once again series and shunt regulator systems, but this time they emphasize that the control elements are linear amplifiers continuously dissipating power to carry out their functions.

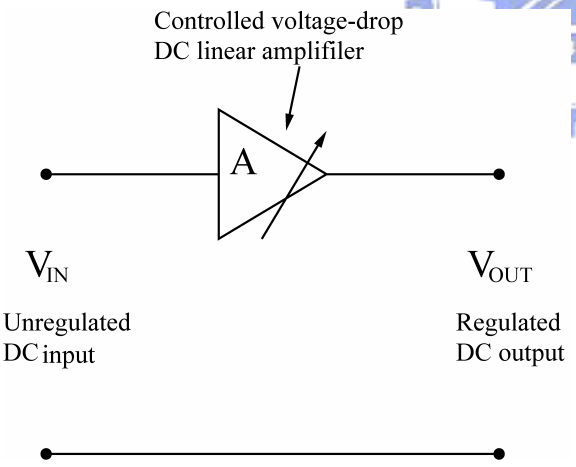


Fig. 2.2 (a) Principle of linear series regulator.

The linear regulators have many desirable characteristics such as low output ripple, good line and load regulation, fast transient response and low electromagnetic interference (EMI). How low efficiency limits their application. When it comes to high volt-amp requirements or transformerless high-step-down voltage between input

and output, the major problem of design in linear regulators becomes largely a mechanical one of providing an adequate heat sink for the dissipating semiconductor devices.

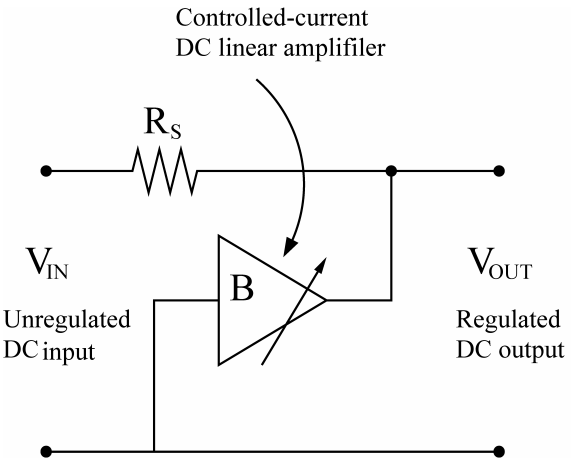


Fig. 2.2 (b) Principle of linear shunt regulator.

2.1.2 Switched Mode Power Supplies

The switched mode power supply gets round the low efficiency of the linear regulator by using controlled on-off switching of the power supplied to the load to keep the output voltage constant.

In series form of the switching regulator illustrated in Fig. 2.2 (c), the series on-off switching control element, *SWA*, inserted between the supply input and output is switched on and off by a controlled on-off duty-cycle generator circuit *X*. As a result, current from the input is released in pulses, which, after smoothing, provide a controlled DC voltage output level. The switching duty cycle of *X* adjusts itself so that the mean output voltage remains constant irrespective of input voltage or load current variations.

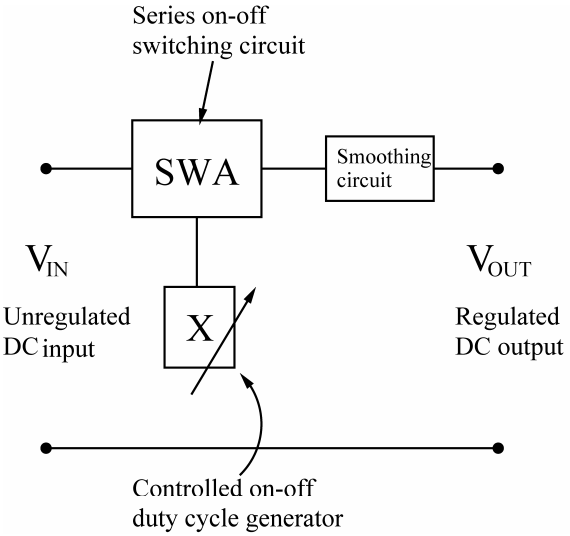


Fig. 2.2 (c) Principle of switching series regulator.

The same principle of rapid on-off "chopping" of the supply also appears in the shunt form of switching regulator shown in Fig. 2.2 (d). Here the controlled on-off duty cycle generator circuit *Y* switches on and off the shunt switching circuit *SWB* to bleed off current from the supply away from the load. Once again the chopped DC is smoothed and fed to the load. The duty cycle control of *Y* is such that the output voltage is held constant under varying input voltages and load currents.

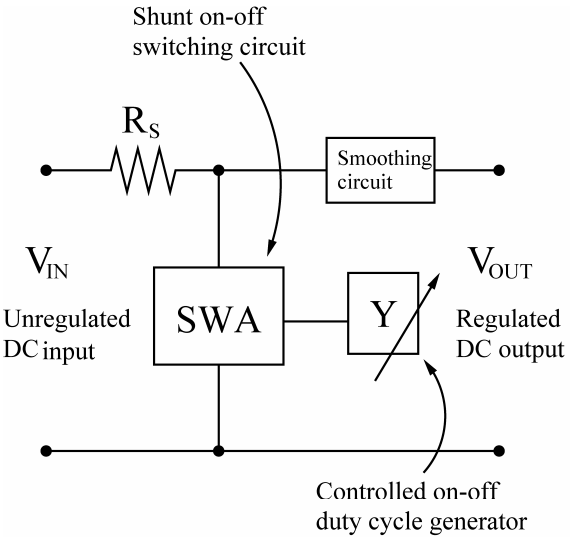


Fig. 2.2 (d) Principle of switching shunt regulator.

The smoothing circuit used in the SMPS usually consists inductors and capacitors. The inductors and capacitors can be viewed as energy storage components. Depending on the arrangement of switches and energy storage components, the output voltage can be generated that is greater than or less than the input voltage.

Switching power supplies can be more compact than equivalent linear ones because of the high efficiency of the switching mode. However, due to the switching operations, large ripples can be observed at the output. Large voltage and current swings also induce EMI issues. These disadvantages make it less favorable for some applications such as communication and audio equipments. Additionally, control circuit for SMPS is usually more complex than linear ones. But the transient response is slower due to the limit of the switching frequency. Table 2.1 lists some typical values of linear and switching regulators [12], [38].

2.2 BASIC CONVERTER TOPOLOGIES

A major decision that must be considered at the beginning of a SMPS design is which basic topology to use. The term topology refers to the arrangement of the power components within the SMPS design. There are more than ten different topologies can be used in DC-DC conversion [1], [12], [39]. Here we limit our introduction to three basic non-isolated topologies of DC-DC SMPS: buck, boost and buck-boost.

2.2.1 Buck

A more detailed discussion of the buck regulator as opposed to the other topologies is presented due to popularity of the buck regulator.

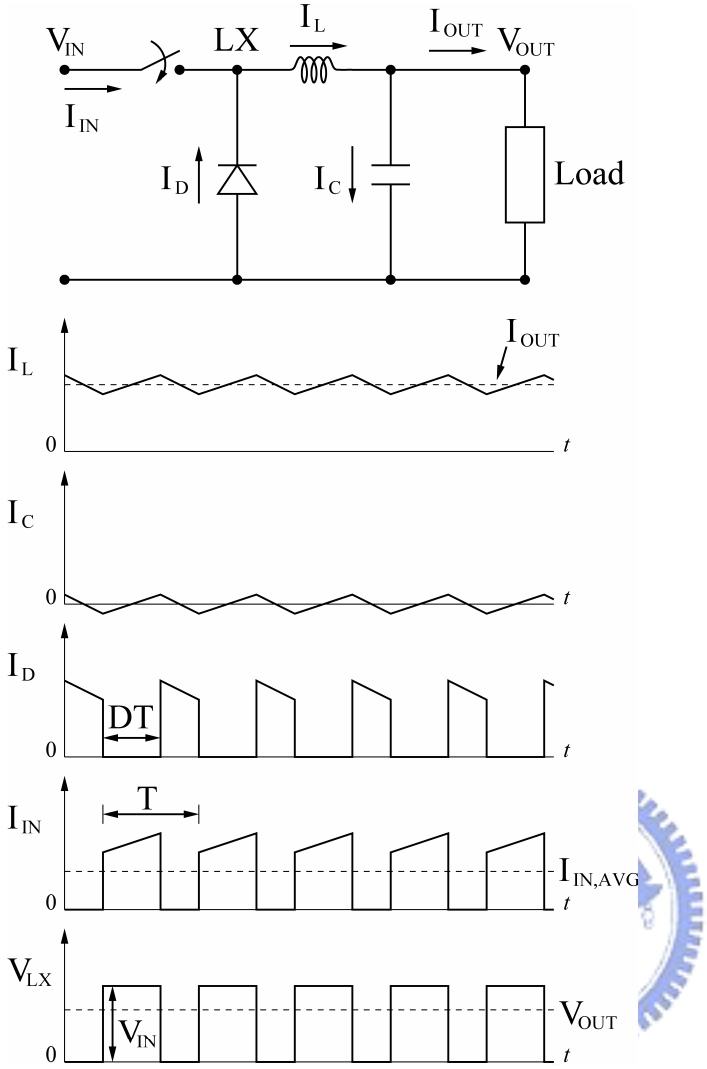


Fig. 2.3 Buck converter topology and related waveforms.

For the buck converter of Fig. 2.3, the output voltage V_{OUT} is less than the input voltage V_{IN}, hence the name buck. When the switch is closed, input current flows through the filter inductor, the filter capacitor, and the load. When the switch is opened, the voltage across the inductor reverses since V_L becomes a voltage source ($V_L = L \times di/dt$), and the energy stored in the inductor is delivered to the load. Since the current in the inductor cannot change instantaneously, the current flowing through the switch at the time the switch is opened now flows through the inductor, the capacitor, the load, and the diode. When the switch is again closed, the current, which was flowing through the diode, now flows through the switch and the cycle repeats.

The average output voltage is

$$V_{OUT} = V_{IN} \times D \tag{2.1}$$

Where D is the duty cycle. The duty cycle is the ratio of the switch on-time to the period T. Since

$$V_{IN} \times I_{IN} = V_{OUT} \times I_{OUT} \tag{2.2}$$

The average input current is

$$I_{IN,AVG} = I_{OUT} \times D \tag{2.3}$$

We can see that when D = 100 %, $V_{OUT} = V_{IN}$ and $I_{OUT} = I_{IN}$. Conversely, when the duty cycle approaches 0 %, the output voltage becomes very small and the peak input current becomes very large.

2.2.2 Boost

For the boost converter of Fig. 2.4, the output voltage is greater than the input voltage, hence the name boost. With input voltage applied, the current flows through the inductor, the diode, the capacitor and the load. When the switch is closed, the current flows through the inductor and switch and in effect, the voltage across the inductor is the input voltage. When the switch is opened, the induced reverse voltage in the inductor is then in series-adding with the input voltage to increase the output voltage, and the current which was flowing through the switch now flows through the inductor, the diode, the capacitor, and the load. The energy stored in the inductor is transferred to the load. When the switch is again closed, the diode becomes reverse

biased, the energy in the capacitor supplies the load voltage, and the cycle repeats.

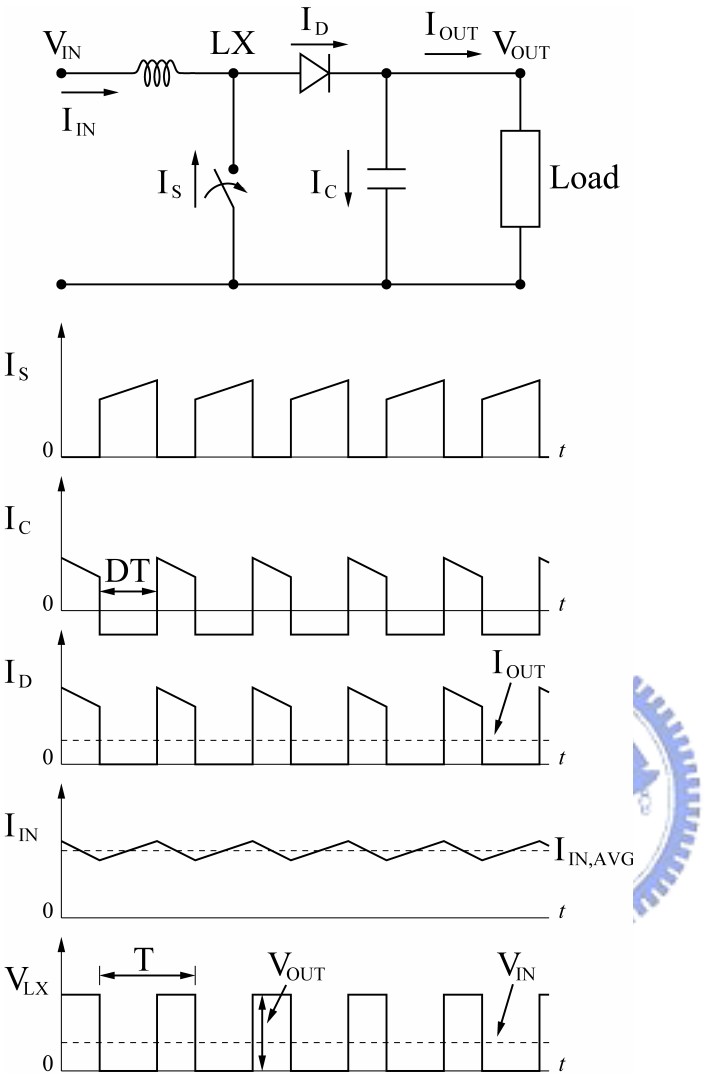


Fig. 2.4 Boost converter topology and related waveforms.

The average output voltage is

$$V_{OUT} = V_{IN} / (1-D) \tag{2.4}$$

Where D is the duty cycle. The duty cycle is the ratio of the switch on-time to the period T. Since

$$V_{IN} \times I_{IN} = V_{OUT} \times I_{OUT} \tag{2.5}$$

The average input current is

$$I_{IN,AVG} = I_{OUT} / (1-D) \quad (2.6)$$

We can see that when D = 0 %, $V_{OUT} = V_{IN}$ and $I_{OUT} = I_{IN}$. Conversely, when the duty cycle approaches 100 %, the output voltage does not necessarily approach infinity because the conducting operation of the semiconductor switch produces a peak current which will quickly exceed the safe operating area (SOA) limit. In other words, we can say that the conduction loss will limits the output voltage when D approaches 100 %.

2.2.3 Buck-Boost

The buck-boost converter shown in Fig. 2.5 is referred to by many names. The buck-boost terminology will be used since the output voltage may be less than, or greater than, the input voltage. The converter is sometimes referred to as a flyback converter. The flyback designation is appropriate due to the inherent action of the inductor. This action in itself is sometimes referred to as a ringing-choke regulator. Also, the topology is sometimes referred to as an inverting regulator, since the output voltage polarity is opposite the input voltage polarity.

When the switch is closed, the current flows through the inductor since the diode is reverse biased. When the switch is opened, the current, which was flowing in the switch, now flows through the inductor, the diode, the capacitor and the load. The energy stored in the inductor is transferred to the load. When the switch is again closed, the current, which was flowing through the diode, now flows through the switch, and the diode becomes reverse biased.

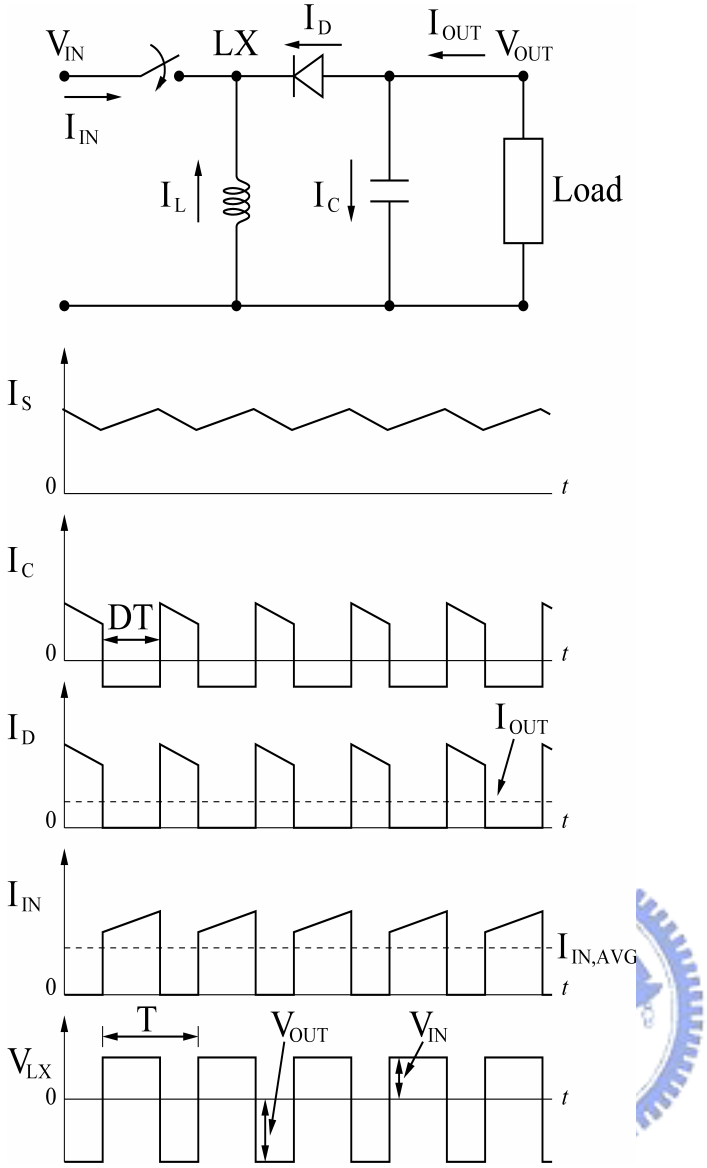


Fig. 2.5 Buck-boost converter topology and related waveforms.

The average output voltage is

$$-V_{OUT} = V_{IN} \times D / (1-D) \qquad (2.7)$$

Where D is the duty cycle. The duty cycle is the ratio of the switch on-time to the period T. Since

$$V_{IN} \times I_{IN} = V_{OUT} \times I_{OUT} \qquad (2.8)$$

The average input current is

$$I_{IN,AVG} = I_{OUT} \times D / (1\text{-}D) \quad (2.9)$$

We can see that when D equals 50%, $-V_{OUT} = V_{IN}$ and $-I_{OUT} = I_{IN}$.

2.2.4 Synchronous Rectification

In the above topologies, we can see a master switch and a diode served as a slave switch. We can use a controlled switch (synchronous switch) instead of a diode in the above topologies, i.e. synchronous rectification. Synchronous rectification is used in DC-DC converters when low output voltage and high current is needed. Synchronous rectification utilizes power MOSFETs instead of rectifying diodes. These MOSFETs are synchronized to the converter frequency and perform more efficiently the rectification of the output voltage than rectifying diodes due to the low $I \times R$ drop through the channel. [40]-[41]

2.3 MODULATION TECHNIQUES

In this section, we briefly discuss about three modulation techniques.

2.3.1 Pulse Width Modulation (PWM)

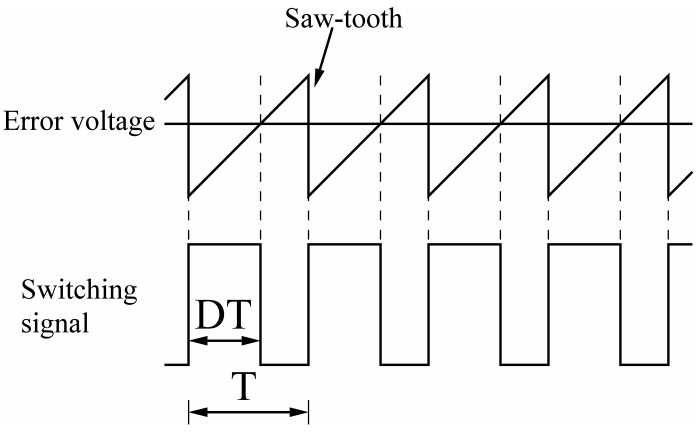


Fig. 2.6 Switching signal of pulse width modulation (PWM).

The pulse width modulation (PWM) maintains a constant switching frequency and varies the duty ratio according to output voltage and load current. Take voltage mode control for example. The switching signal of PWM is shown in Fig. 2.6. The error voltage is modulated by a saw-tooth waveform generated by an oscillator. The switching frequency is determined by the oscillator and the pulse width is controlled by the voltage error. This modulation scheme provides high efficiency at medium to heavy load conditions. At light load condition, the reversed inductor current (may appear in synchronous rectification) and the switching losses degrade the efficiency. Because the switching frequency of PWM is fixed, the noise spectrum is relatively narrow. We can use simple low-pass filter to greatly reduce the peak-to-peak voltage ripple. For this reason, PWM is popular to the noise sensitive communication applications.

2.3.2 Pulse Skip Modulation (PSM)

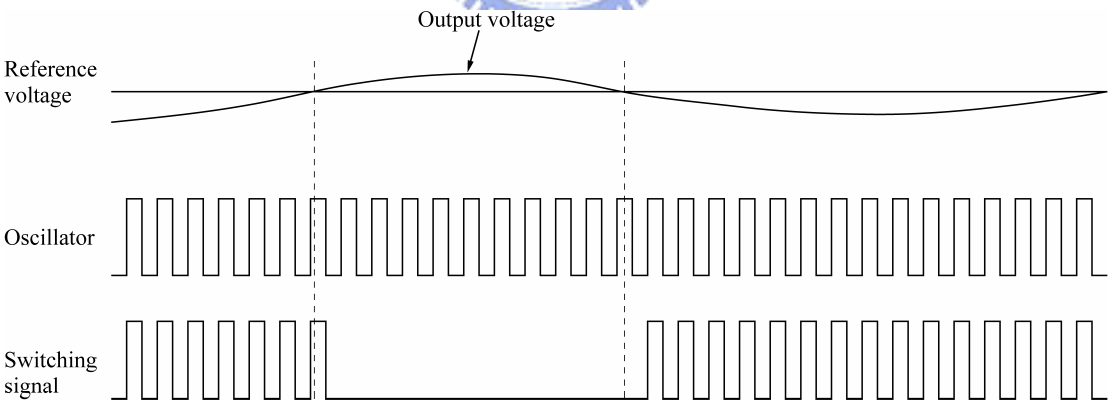


Fig. 2.7 Output waveform and switching signal of pulse skip modulation (PSM).

A feature offered in many modern switching controllers is pulse skip modulation (PSM). Skip mode allows the regulator to skip cycles when they are not needed, which greatly improves efficiency at light loads. As shown in Fig. 2.7, in a PSM

system, there exists an oscillator as a timing reference. Each pulse of the switching signal starts with the clock signal. As long as the converter output is below the reference voltage, the PSM pulses continue to run the converter switch. Once the converter output reaches or exceeds the target, the PSM pulse is skipped. This operation will result in decreasing pulse density as the converter output reaches its target, or as the output loading decreases. When the converter output falls below the target, or as the output loading increases, the PSM pulse density will increase. However, the inductor selection is complicated, the peak-to-peak voltage ripple can be quite high, and the noise spectrum will vary greatly with the load.

2.3.3 Pulse Frequency Modulation (PFM)

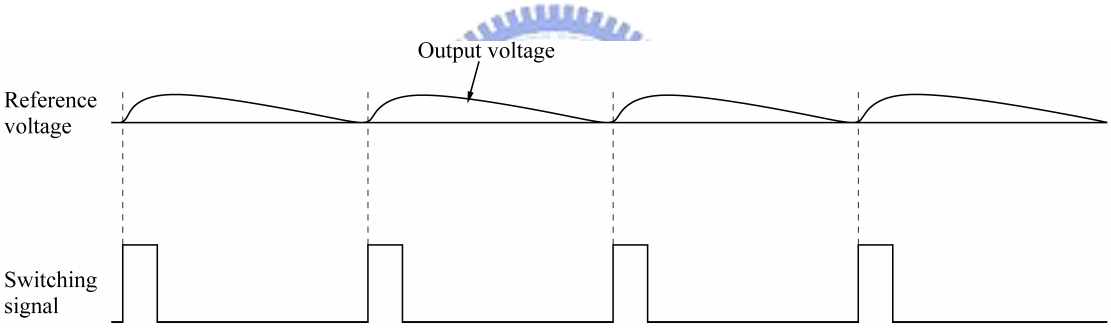


Fig. 2.8 Output waveform and switching signal of pulse frequency modulation (PFM).

As shown in Fig. 2.8, pulse frequency modulation (PFM) is somewhat different from pulse skip modulation. They all reduce the pulse density in light load conditions and hence the efficiency can be boost under light load operation. The major difference of PFM to PSM is that the PFM does not need a clock signal. The pulse width is variable and the pulse repetition rate is varied in accordance with load current and input/output voltages. As soon as the output voltage reaches the bottom value of regulation, the main switch turns on until the inductor current reaches the peak current limit or until the predetermined time is up. The major drawback of PFM control is still

its varying switching frequency.

2.4 PROTECTIONS OF SMPS

In the design of a power supply it is prudent to provide protection circuitry to protect against extreme and abnormal operating conditions that will inevitably occur when the supply is in use. These can occur in the form of output short circuits and excessive loads or high voltage transients on the input supply line. Many of the components in a power supply are handling powers greatly in excess of their dissipation capability. Under fault conditions it is quite possible that they may start to dissipate this power, leading to their rapid failure. The power supply designer has no control over these faults and therefore must incorporate circuitry to accommodate them safely. This falls into five broad categories: (1) over-current protection; (2) over-voltage protection; (3) inrush protection; (4) device protection; (5) over temperature protection. [4], [42]

2.4.1 Over-Current Protection

In order to provide current limiting, some means of sensing over-current conditions must be provided. In an SMPS the commonest method of achieving current limiting is to control the switching activities of the switching transistors. Under fault conditions the transistors can be switched off. Cycle-by-cycle protection is a useful method of output current limiting in an SMPS.

The purpose of current limiting is two-fold: firstly to limit the dissipation in the power supply components to safe values and thereby prevent damage to them, and secondly to provide some protection to circuits and systems being powered by the

supply.

2.4.2 Over-Voltage Protection

Over-voltage protection must deal with three possible situations: (1) reverse voltage on output; (2) external over-voltage on output; (3) internally generated over-voltage. The first two situations are reasonably easily dealt with by placing "catcher" diodes on the output. Fore reverse polarity protection, a normally reverse biased diode can be placed on the output. Normal over-voltage protection can be provided by a zener or avalanche diode whose voltage is in excess of the normal operating voltage of the power supply. Diodes for both types of protection must by amply rated to cope with the anticipated fault conditions.

It is important that a power supply does not give out an abnormally high voltage under fault conditions. If it did so it could easily damage the circuitry that it is powering. We can monitor the output voltage by an over-voltage control circuit. This is usually some form of comparator that is set to trigger under over-voltage conditions. Its output is used to stop the switching activity thereby shutting down the power supply; in much the same way as was done for cycle-by-cycle current limiting.

2.4.3 Inrush Protection

In most SMPS designs it is desirable to introduce a certain delay during start-up, in order to avoid inrush current and output overshoots at turn-on. Circuits that are employed to perform this task are called soft-start circuits. In general they control the modulation circuitry to make the output to increase from zero to its operating value very "softly".

Fig. 2.9 shows how a soft-start circuit may be implemented in a PWM control circuit. At time t = 0, when the power supply is just turned on, capacitor C is discharged and the error amplifier output is held to ground through diode *D1*, thus inhibiting the comparator output.

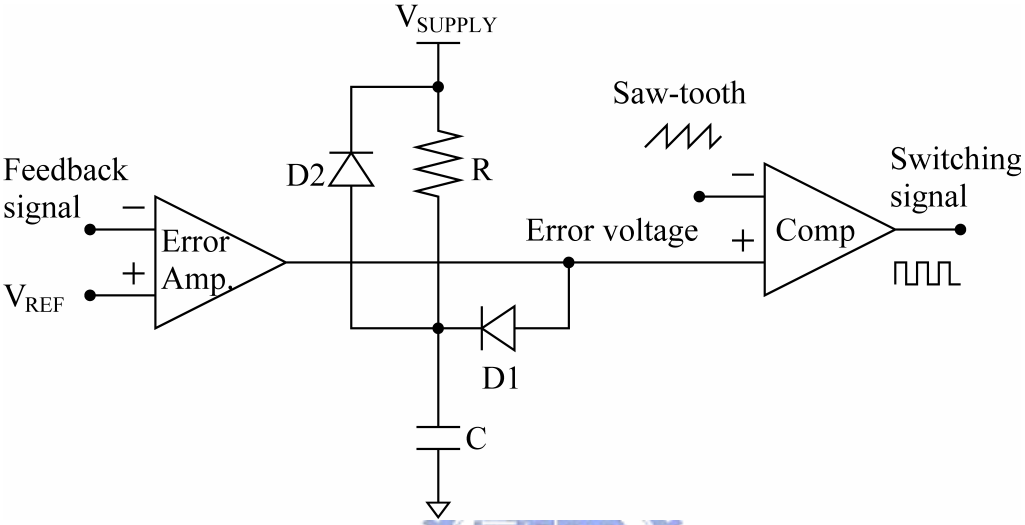


Fig. 2.9 A typical soft-start circuit used in a PWM control circuit aids the gradual increase of the PWM signal to its operating value.

At time $t = 0^+$, the capacitor starts to charge through resistor *R* with a time constant determined by $\tau = RC$ toward the charging voltage V_{SUPPLY}. As capacitor *C* attains full charge, diode *D1* is reverse biased, and therefore the output of the error amplifier is isolated from the soft-start network. The slow charge of capacitor *C* results in the gradual increase of the PWM waveform at the output of the comparator, and consequently a "soft start" of the switching element is initiated.

Diode *D2* is used to bypass resistor *R* in order to discharge the capacitor *C* fast enough in case of system shutdown, thus initiating a new soft-start cycle even during very short interrupt periods. In some PWM control ICs, the resistor *R* has been substituted by an on-chip current generator, thus the only external element required to

implement the soft-start feature is the addition of capacitor *C*.

2.4.4 Device Protection

While dealing with protection it is probably worth mentioning voltage clamping. Here an avalanche diode is placed across the two conduction terminals of the power switch transistor. The breakdown voltage of the diode is chosen so that it is below the breakdown voltage of the power switch transistor and greater than the supply. In normal operation the diode will not conduct, but it will serve to clip any high voltage transients that might be harmful to the transistor.

2.4.5 Over Temperature Protection

Although a power supply is protected by over-voltage and over-current protection circuits, it may undergo over heating condition because of high ambient temperature, improper heat sink design or malfunction of heat sink devices. The over temperature protection is needed to protect the power supply and all the devices and the circuits around the power supply under these conditions. Without over temperature protection, these abnormal conditions may cause fire and great damages.

The thermal sensors detect the temperature at the critical positions in the power supply. Once the temperature is higher than a preset safety margin, an over temperature signal will be issued to turn off the power switches. The heat energy will stop accumulation and the temperature may go down.

2.5 PERFORMANCE SPECIFICATIONS

While designing an electronic system, output voltage and current rating are

usually specified to the power supply. However, many other parameters are required to evaluate the performance of a power supply [4], [43]. In this section, some terms and definitions are described such that it will be easier to design or to evaluate a switching regulator.

2.5.1 Efficiency

The efficiency of a power supply is defined as the ratio of the output power and the input power and is calculated as follows:

$$\text{Efficiency} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100\% \qquad (2.10)$$

Efficiency can be regarded as the ratio of delivered power P_{OUT} to total consumed power P_{IN}. Total power is the sum of the followings: (1) quiescent power: the quiescent current is the current flows into the chip. It is a goal of the chip designer to minimize this kind of power dissipation. (2) parasitic power: parasitic resistance in the output current path also dissipates power. (3) dynamic power: during the switching period, power is dissipated by charging/discharging gate capacitance of switching MOSFETs. It is a function of gate capacitance C_g, switching frequency f_{SW}, and driving voltage V_D. The relationship is $P_d = C_g \times V_{dr}^2 \times f_{SW}$. (4) output power: power delivered to the load. An efficient power supply should transfer as much input power to the output as possible. An inefficient regulator has two major disadvantages. First, energy is wasted. This is particularly important in a battery-powered system. Second, large heat sinks and good ventilation are required, which add to the size and weight of the regulator.

2.5.2 Input Voltage Range

While delivering a regulated output voltage, a power converter must have the ability to operate under a wide input voltage range. Circuits in the power converter must keep constant operating characteristics under the input voltage variation. Sometimes the variation of input voltage can be several times to the minimum allowable input voltage. A closely related specification is line regulation, which will be discussed in section 2.5.4.

2.5.3 Load Regulation

Output voltage regulation is a regulator's ability to maintain its output voltage within the specified tolerance under various load disturbances. A measure of this ability is output impedance of the regulator. There is usually a feed back path in a regulator to compensate for such changes and keep the output close to the nominal value. Load regulation is the percentage change in the steady state output voltage when the load current changes from its minimum value to the fully rated current. Load regulation is defined as:

$$\text{Load Regulation} = \frac{\Delta V_{OUT} / \Delta V_{NOM}}{\Delta I_{LOAD}} \times 100\% \qquad (2.11)$$

Where V_{NOM} is the nominal output voltage.

2.5.4 Line Regulation

Similar to the definition of the load regulation, the line regulation is a measure of the effect of changes in the input voltage one the output voltage. The small signal line-to-output transfer function is called audio susceptibility. In some systems, input voltage may change as largely as 10 V. For example, in a notebook computer, the

input voltage is 19 V provided by an AC adapter while it is around 8 V when battery power is used. There is a variety of methods used to specify line regulation. However, a common definition is:

$$\text{Line Regulation} = \frac{\Delta V_{OUT} / \Delta V_{NOM}}{\Delta V_{IN}} \times 100\% \qquad (2.12)$$

The specification of line regulation is usually given by %/V between maximum and minimum input voltages and at a specified loading condition.

2.5.5 Transient Response

The transient response is a switching regulator's response to sudden changes in load current or line voltage. It is measured by the magnitude of output voltage drop and the time of recovery. The transient response relates to the bandwidth of switching regulator, output capacitor, equivalent series resistance (ESR) of output capacitor and the load current.

A wide bandwidth regulator exhibits fast transient response. Limited by the bandwidth of switching frequency, switched mode regulators are slower than linear regulators. Loop crossover frequency is typically limited to 1/5 to 1/10 of the switching frequency. Therefore, a large output filter is required to compensate slow transient response. In order to reduce overshoot and ringing in output voltage, an adequate phase margin must be obtained. Control scheme also affects loop bandwidth, for example, the current-mode control provides faster response than the voltage mode.

If the output is suddenly switched from light load to full load, the shortage of the output current will cause a fall in output voltage. On the other hand, if the load is

switched off, excess output current will cause a rise in the output voltage. The transient response is normally specified together with a recovery time and is stated as:

$$\frac{V_{DEV}}{V_{NOM}} \times 100\% \qquad (2.13)$$

Where V_{DEV} is the maximum deviation from nominal output voltage V_{NOM} at a full load transient. The transient recovery time was defined differently from 1% to 5% tolerance of the final settling value in different texts. We choose 1% tolerance to evaluate the performance of our work.

2.5.6 Electromagnetic Interference (EMI)

Electromagnetic interference (EMI) is a potential problem for the circuit designer. The switching process of a regulator produces voltage spikes resulting in EMI that interferes with proper operations of sensitive electronic equipments. The EMI spectrum begins at the switching frequency and often extends over 100 MHz that falls within the frequency bands commonly allocated for communications, such as low-frequency (LF), high-frequency (HF), and very-high frequency (VHF) bands. One obvious advantage of a fixed-frequency regulator is that the switching frequency and its harmonics are fixed which makes it easier to filter induced EMI.

There are two main EMI specifications that must be checked out, that for conducted noise and that for radiated noise. Usually if a design includes adequate screening and the conducted noise is kept under control, by means of appropriate filters, radiated noise is not too much of a problem.

CHAPTER 3

A MONOLITHIC CURRENT-MODE BUCK CONVERTER WITH ADVANCED CONTROL AND PROTECTION CIRCUITS

3.1 INTRODUCTION

Portable battery-operated devices are more and more popular today. For these devices, small size, light weight and long battery run-time are the main demands. The batteries had become a main portion in space and weight of these portable devices. As a result, enhancing the efficiency of power supply and management is very important to minimize the size and weight and to extend the battery run-time. The well-known power management strategy, sleep mode, shuts down the unused partial circuit to effectively reduce the power consumption [44]. Although sleep mode can save the power effectively in stand-by mode, there is no power saving in active mode because it operates with full current. The way of saving the power is to reduce the operating current but this usually reduces the circuit performance such as speed and noise immunity.

We focused on increasing the power efficiency and reducing die size without sacrificing high speed operation. Besides, safety operation is also an important consideration in power supply design. In this chapter, we propose the dynamic partial shutdown strategy (DPSS), current sensing, over-current protection, soft-start and PWM-PFM operation to achieve our goal.

The DPSS manages the power consumption at active mode to enhance the circuit performance per power consumption. Improvement was obvious, especially in lighter load with the PFM mode control [45].

Moreover, we modified the current sensing and slope compensation circuits in current-mode control [46]-[54] to simplify the design flows of various specifications. In current sensing circuit, a simple over-current protect comparator is developed. Its response speed is faster than the conventional comparator [53], [55]-[56]. But it consumes no additional quiescent power. With this circuit, the over-current protection, which is essential to voltage regulator, can be designed easily.

Most portable electronic devices have more than one power supply modules. Anyone of them may be shut down when the circuit supplied by it is unused. However, if we turn on the power supply module and don't handle the load current demand from next stage properly, the inrush current demand to previous stage will result in impulse voltage drop and affect the circuit operation or shorten the life-time of batteries. On the other hand, inrush current can also cause the output to overshoot [57]. To overcome the induced effects, a soft-start time, usually 1 ~ 10 ms for portable electronic devices, is required at the beginning of the turn-on stage for voltage regulators. During soft-start time, the corresponding voltage regulator charges the output capacitor slowly, and then no inrush current is generated to affect the pre-stage circuit or to cause output overshoot. The conventional method of generating the soft-start time is costly in area [55], [58]-[59] or need the extra pin-out and discrete capacitor [57], [60]-[63]. This method results in increasing in cost, size and weight. This paper also presents a simple and area-effective circuit to generate soft-start time without the extra pin-out and the discrete capacitor. This circuit has the soft-start time

proportional to the square of silicon area and is suitable for even longer soft-start time (> 10 ms) applications.

Structure of current-mode PWM and PFM control are introduced in Section 3.2 [45], [64]. Circuit implementations of the controller are discussed in Section 3.3.

All the circuits mentioned above are integrated in a monolithic buck converter and implemented in a 0.6 μm CMOS process. It can operate in a wide input range from 2.2 V to 6.0 V. Measurement results are shown in Section 3.4 and conclusion is in Section 3.5.

3.2 STRUCTURE OF THE MONOLITHIC BUCK CONVERTER

In this section, we will briefly introduce the structure of current-mode PWM and PFM operation in the developed monolithic buck converter [45], [64].

3.2.1 PWM

At moderate to heavy loads, the converter operates in PWM mode. The block diagram of a simplified current-mode PWM buck converter is illustrated in Fig. 3.1. A clock pulse at the *R* (reset) input of *SR Latch* initiates the switching period, causing the latch output *Q* to be low. The latch output *Q* goes through *Buffer and Dead Time Control* to produce both *DH* and *DL* low to turn on the high side PMOS transistor and turn off the low side NMOS transistor. While the high side transistor conducts, its current is equal to the inductor current. This current increases in a certain positive slope according to the inductor value and converter voltages. We sense the high side transistor current and compare it with the control voltage V_C. When the sensed current

signal becomes higher than control voltage V_C, the modulator output will be high to set the *SR Latch* output *Q* high. Again the latch output *Q* goes through *Buffer and Dead Time Control* to produce both *DH* and *DL* high to turn off the high side PMOS transistor and turn on the low side NMOS transistor until next clock pulse. We see the current controlled through the control voltage V_C and thus is named current-mode control. On the other hand, a compensation ramp is added to the sensed current signal to suppress sub-harmonic oscillation at duty ratio > 50% [46].

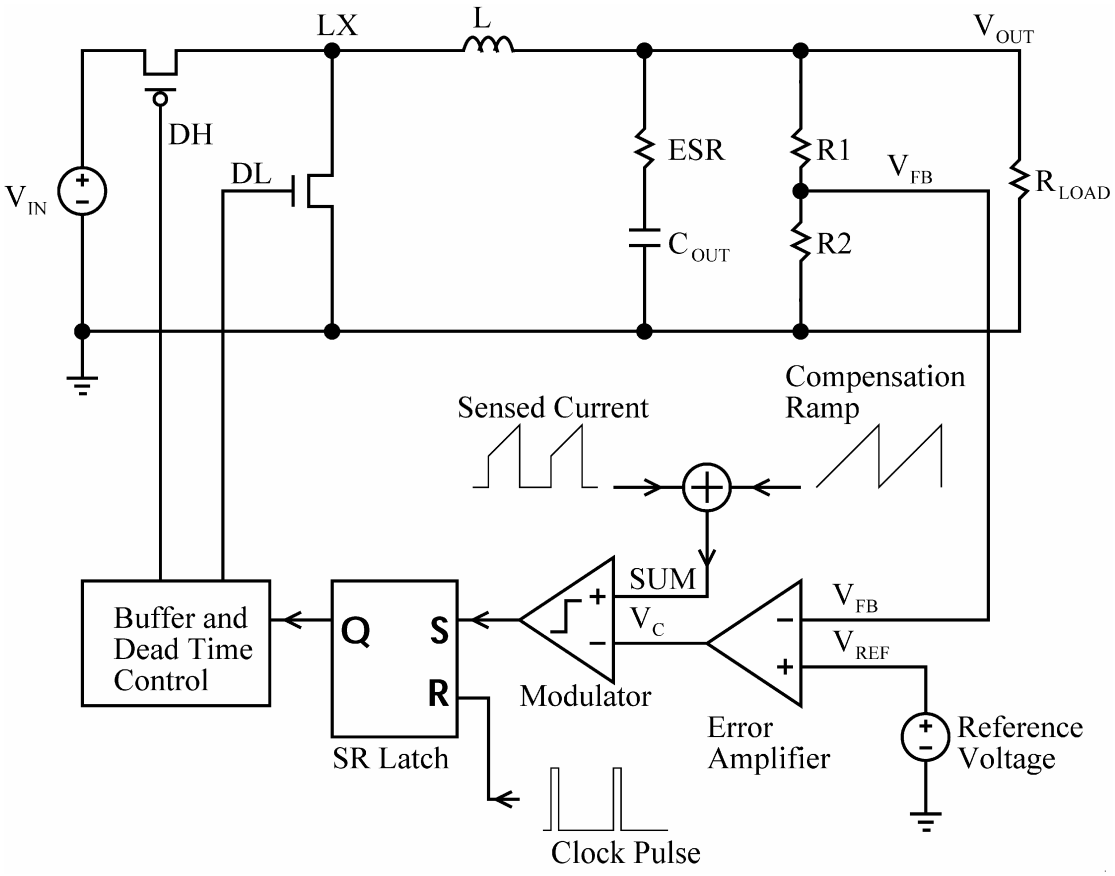


Fig. 3.1 Simplified structure of current-mode PWM control.

3.2.2 PFM

With decreasing load current, the converter automatically switches into PFM mode in which the power stage operates intermittently, based on load demand. Due to

reduced switching activity at power stage, the switching losses are minimized, and the device runs with a minimum quiescent current and maintains high efficiency. The block diagram of a simplified PFM mode buck converter is illustrated in Fig. 3.2.

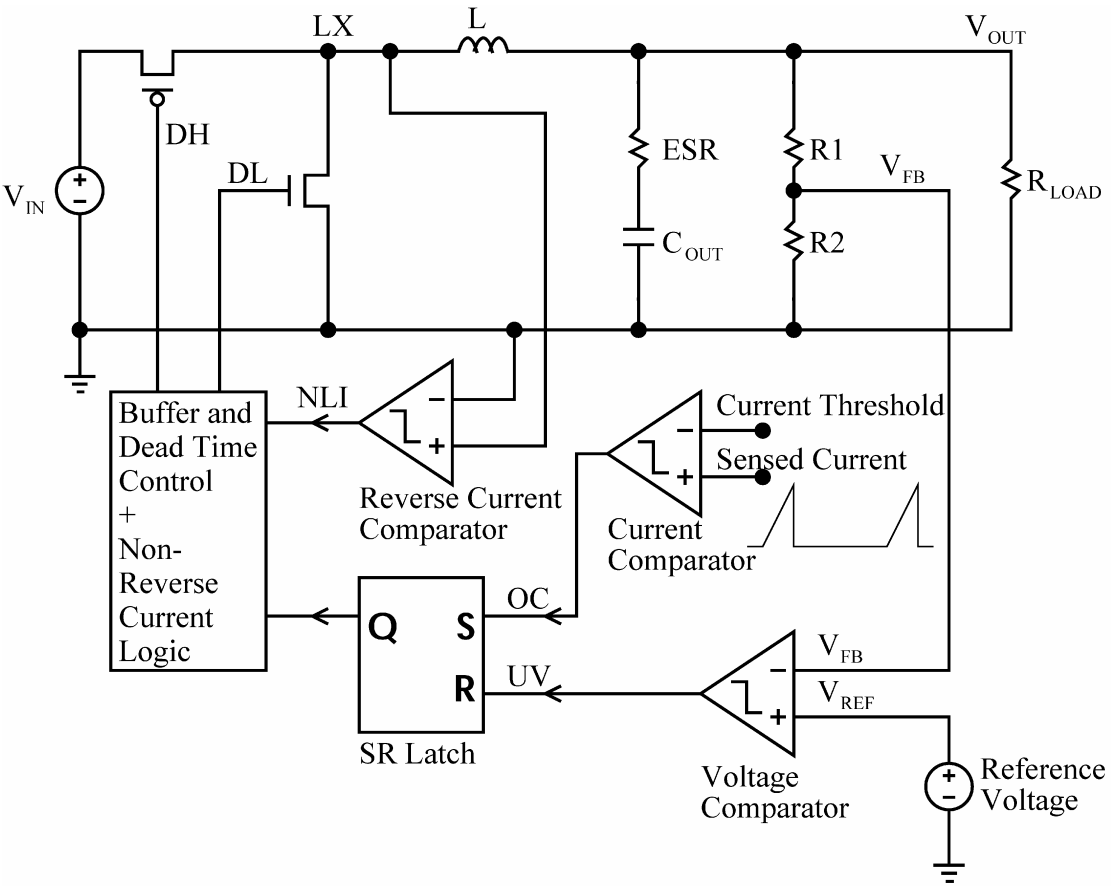


Fig. 3.2 Simplified structure of PFM control.

The output voltage is monitored with a voltage comparator. As soon as the output voltage falls below the nominal value, the output of the voltage comparator resets the *SR Latch*. Through *Buffer and Dead Time Control* the high side PMOS transistor is turned on and the inductor current ramps up. When a current comparator detects that the inductor current reaches the preset peak current, its output sets the *SR Latch* and turn off the high side PMOS transistor and turn on the low side NMOS transistor. As the inductor current ramps down, a reverse current comparator detects if the inductor current begins to flow in reverse direction. When this is the case, the

Reverse Current Comparator turns off the low side NMOS transistor to prevent drawing energy from output capacitor back to ground. When the output voltage falls below the nominal voltage again, the next cycle is started. As the load current decreases, the time interval between two successive pulses will become larger and vice versa.

3.2.3 Automatic PWM/PFM Mode Switching

There are many algorithms of switching between PWM and PFM. In this work, we use a hysteresis switching algorithm to prevent repeatedly switching between two modes during steady state operation. The algorithm can be described as follows:

1. In PWM mode, as the load current decreases, the inductor current may ramp to zero before the end of each clock cycle. In order to increase the efficiency, the low side NMOS will be turned off when the inductor current ramps to zero. This action prevents the current flowing in reverse direction from output capacitor to ground through inductor and low side NMOS. Thus the converter enters discontinuous conduction mode (DCM). When the converter operates in DCM, it means that the load current is small and we don't need continuous full-cycle-pulses to sustain it. If the converter operates in DCM for about 20 μs, it will automatically switch to PFM mode.

2. In PFM mode, the peak current of each pulse is preset to a constant value as described above. We monitor the output voltage to determine when the next pulse should be issue. The next pulse will be issue if the output voltage falls below the nominal value. When the load current increases, the output voltage falls faster and the two pulses in succession will become closer. If the output voltage falls below

the nominal value after the peak current is reached and before the current ramps back to zero, it means that we need to issue the next pulse even before the present pulse is completed. In this condition, the load current is large and the output voltage cannot be sustained with this preset current pulse. Thus the converter will enter PWM mode again.

3.2.4 The Proposed Converter

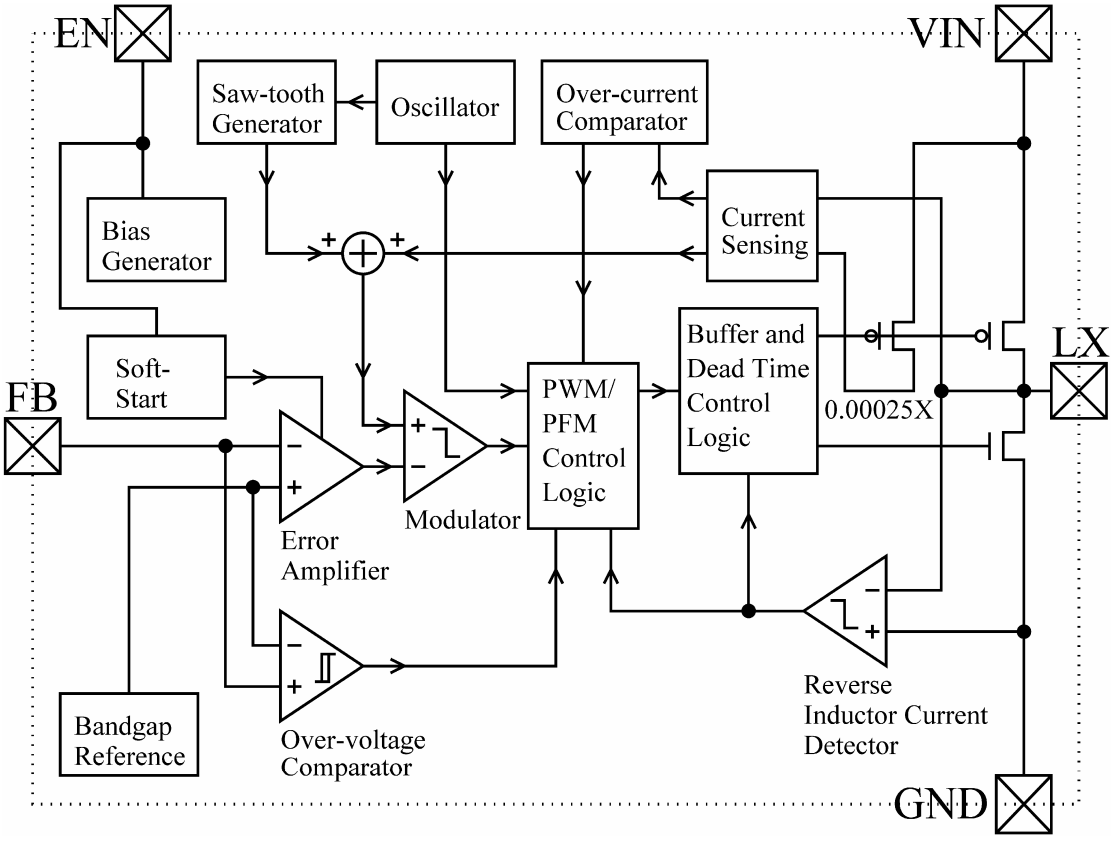


Fig. 3.3 Functional block diagram of the developed monolithic buck converter.

Fig. 3.3 shows the simplified block diagram of the developed converter chip. It uses PWM and PFM control as described above. Key elements such as on-chip soft-start, DPSS, current sensing, modulator and over-current comparator will be described in the next section.

3.3 DESIGN CONSIDERATIONS AND CIRCUIT IMPLEMENTATIONS

3.3.1 On-Chip Soft-Start Circuit

There are mainly two kinds of conventional soft-start circuits. One is the clock-based soft-start circuit which raises the reference voltage or maximum output current or duty cycle slowly [55], [58]-[59]. In this method, the way to achieve the longer soft-start time (> 1 ms) is to reduce the clock frequency or increase the bit-length of counter. The former one fails to reach the goal of raising the switching frequency to minimize the energy storage elements (such as inductors and capacitors) and to enhance the response speed in switching regulator design. A separate clock can be used for soft-start, but it requires extra die area and power. The latter one, however, consumes large silicon area. Moreover, the clock-based soft-start needs time-to-voltage or time-to-current-limit circuits.

The other soft-start method charges the capacitor with a constant current to generate a steadily rising voltage. This steadily rising voltage can be used as reference voltage during start-up or to limit the duty ratio or output current during start-up [57], [60]-[63]. The soft-start time can be calculated as:

$$t_{soft-start} = V_{REF} \times C / I \qquad (3.1)$$

Note that V_{REF} is the reference voltage or a threshold voltage which determines the end of start-up, C is the capacitor value and I is the charging current.

In previous works [57], [60]-[63], extra pin-out and discrete capacitor were

needed to reach longer soft-start time (> 1 ms). For example, if V_{REF} equals 0.6 V and 1 ms soft-start time is needed with 1 μA charging current, a 1.67 nF capacitor is needed. Our goal is to minimize the capacitor using small charging current. For integration of capacitor on die, the order of capacitor is picofarad. Correspondingly, the charging current is in the order of nanoampere. In [65]-[68], complex bias circuit is needed to generate the bias current in nanoampere order. In addition, transistors must operate in deep sub-threshold region. The I-V characteristic of MOS transistor operates in the deep sub-threshold region is: [69]

$$I_D = k_x \frac{W}{L} e^{\frac{V_{GS}}{nV_t}} (1 - e^{-\frac{V_{DS}}{V_t}}) \tag{3.2}$$

Where k_x depends on process, $n \approx 1.5$ and V_t is the threshold voltage of the transistor. The effectiveness of gate drive voltage (V_{GS}) to drain current (I_D) is exponential. Noise on the gate drive voltage will greatly affect the drain current. So that deep sub-threshold bias is not suitable for a noisy environment like switch-mode power supply with integrated power switches.

In this work, a simple circuit is proposed as shown in Fig. 3.4. Note that, V_b can be generated by a simple bias circuit or the existing bias voltage in the system. In Fig. 3.4, for a general bias circuit,

$$\left|V_b - VCC\right| = \left|V_{GS(M_b)}\right| > \left|V_{t(M_b)}\right| \tag{3.3}$$

The transistor M_b operates in saturation region.

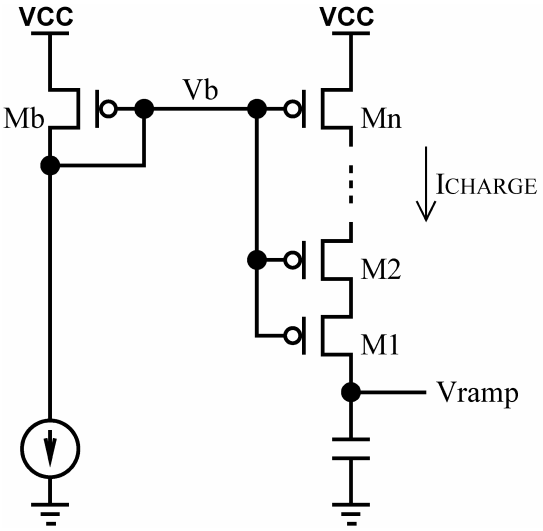


Fig. 3.4 Soft-start ramp generator.

We can use simple MOS transistor equations in [69]:

Saturation region ($V_{GS} > V_t$, $V_{DS} > V_{GS} - V_t$):

$$I_D = \frac{1}{2}\mu \cdot C_{OX}\frac{W}{L}(V_{GS} - V_t)^2 \tag{3.4}$$

Triode region ($V_{GS} > V_t$, $V_{DS} < V_{GS} - V_t$):

$$I_D = \mu \cdot C_{OX}\frac{W}{L}\left[(V_{GS} - V_t)\cdot V_{DS} - \frac{1}{2}V_{DS}^{\ 2}\right] \tag{3.5}$$

Where μ is mobility and C_{OX} is oxide capacitance. When V_{ramp} is well below *VCC*, transistor M_1 operates in saturation region. Other series transistors $M_2 \sim M_n$ operate in triode region. Therefore, $M_2 \sim M_n$ are like the (n-1) linear resistances whose total voltage drop is slightly smaller than ($V_{GS} - V_t$). For small V_{DS}, we approximate (3.5) to (3.6):

$$R_{DS} = \left[\mu \cdot C_{OX}\frac{W}{L}(V_{GS} - V_t)\right]^{-1} \tag{3.6}$$

Then according to Ohm's law, we have

$$I_{CHARGE} = I_{D(M_1)} = I_{D(M_2 \sim M_n)} = \frac{VCC - V_{D(M_2)}}{R_{DS(M_2)} + ... + R_{DS(M_n)}} \quad (3.7)$$

As a result, the nanoampere order charging current can be achieved easily in today's technology. For example, if V_{REF} equals to 0.6 V, 1 ms soft soft-start time is available with a 1 nA current to charge the 1.67 pF capacitor. In our design, the soft-start circuit occupies only 56.1 × 65.4 μm^2 and reaches longer than 1.5 ms soft-start time.

Another advantage of this circuit is that the soft-start time is proportional to the square of the silicon area. According to (3.1), for a fixed reference voltage, the soft-start time is proportional to the capacitor value and reverse proportional to the charging current. In (3.7), the charging current is reverse proportional to the summation of R_{DS} of transistors. Thus we have the soft-start time proportional to the series number of PMOS. If we increase both the capacitor value and the series number of PMOS with the same ratio, the soft-start time is proportional to square of the occupied silicon area. The proposed method can reduce the silicon area dramatically and this circuit does not need extra pin-out and discrete capacitor.

3.3.2 Dynamic Partial Shutdown Strategy (DPSS)

For extension of battery run time of portable devices, dynamic power management uses sleep mode which shuts down unused circuits to save power during stand-by mode [44]. However, in active mode, it cannot save the power consumption because of the full operating current. In this paper, the dynamic partial shutdown strategy (DPSS) controlling the turn off of partial circuits is proposed to save the

power consumption, especially in active mode. During active mode, only the essential parts will be turned on in specific operating situation under DPSS. As a result, the power consumption is minimized and battery run time is extended.

In a switch-mode power supply, the decision of when to turn on or turn off switches was made according to the output voltage and current condition in each switching cycle. When the switch is on, we need to decide when to turn it off; when the switch is off, we need to decide when to turn it on again. According to this characteristic of switch-mode power supply, we can turn off partial circuits which are not needed to decide when the switch should be turned off during "ON" state and vice versa. Since there are digital signals indicating the ON and OFF states of the power switches in the converter, we can use these digital signals to turn on and turn off the partial circuits which are not needed in each state.

Take the proposed converter as an example. In Fig. 3.5 and Fig. 3.6, we use horizontal, vertical and oblique lines to indicate shut down parts. Blocks with horizontal lines are shut down when high side PMOS is turned on. Blocks with vertical lines are shut down when low side NMOS is turned on. Blocks with oblique lines are shut down when both power transistors are turned off. Fig. 3.5 shows circuits operate in PWM mode; and Fig. 3.6 in PFM mode. Note that the soft-start time has been completed and the *Soft-Start* in Fig. 3.5 and Fig. 3.6 is always shut down.

In PWM mode, when high side PMOS is turned on, the slope of inductor current is positive. So we don't need to detect reverse inductor current and the *Reverse Inductor Current Detector* can be turned off. When low side NMOS is turned on and that the slope of inductor current is negative, there is no need to detect the over-current and the *Current Sensing* and *Over-current Comparator* can be shut

down.

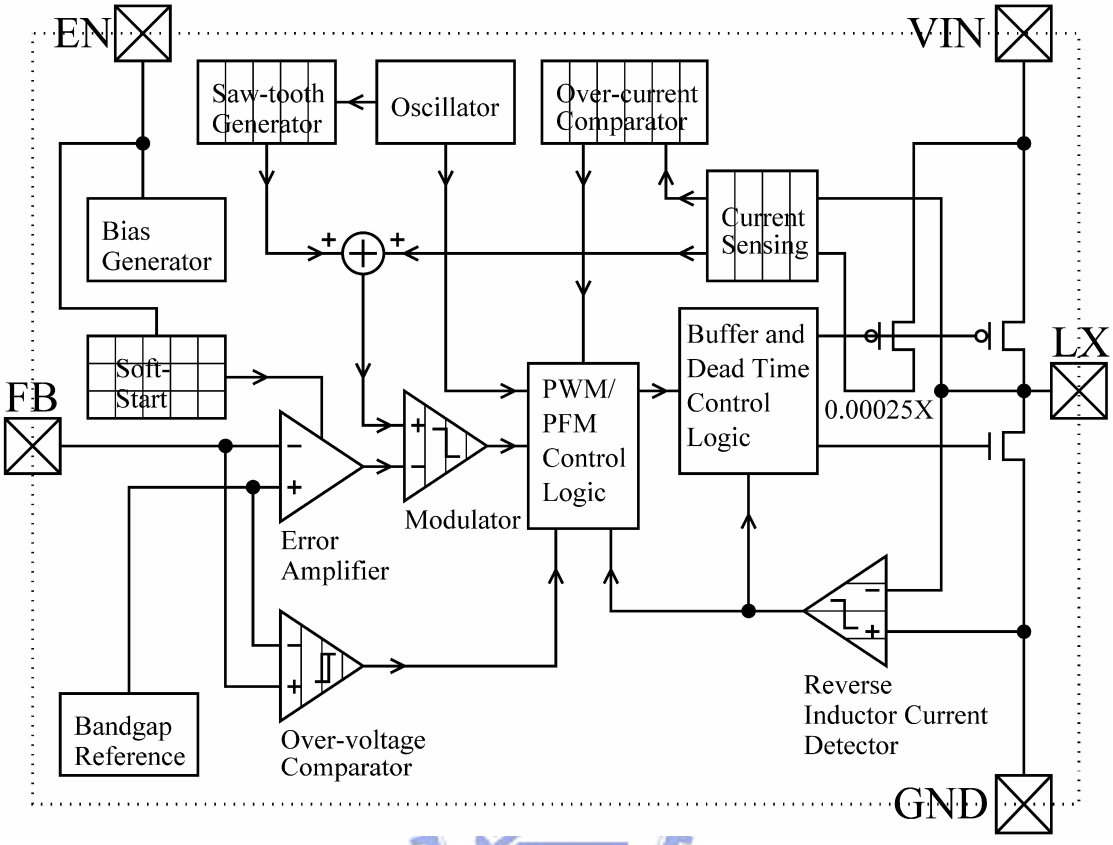


Fig. 3.5 DPSS in PWM mode. Blocks with horizontal lines are shut down when high side PMOS is turned on. Blocks with vertical lines are shut down when low side NMOS is turned on.

Since the slope of inductor current is negative, the *Over-voltage Comparator* cannot do anything more to prevent output voltage from going too high. Thus the *Over-voltage Comparator* can be shut down. Besides, the next turning on of high side PMOS is decided by clock pulse in constant frequency leading edge modulation [70]. The *Saw-tooth Generator*, *Analog Adder* and *Modulator* can also be shut down.

In PFM mode, the *Error Amplifier*, *Oscillator*, *Saw-tooth Generator*, *Analog Adder* and *Modulator* all can be shut down. When high side PMOS is turned on, only the peak inductor current decides when to turn it off. As a result, the *Voltage*

Comparator and *Reverse Inductor Current Detector* can be shut down. When low side NMOS is turned on, the *Current Sensing* and *Over-current Comparator* can be shut down. When both high side PMOS and low side NMOS are turned off, only the *Voltage Comparator* is active to decide when the high side PMOS should be turned on again.

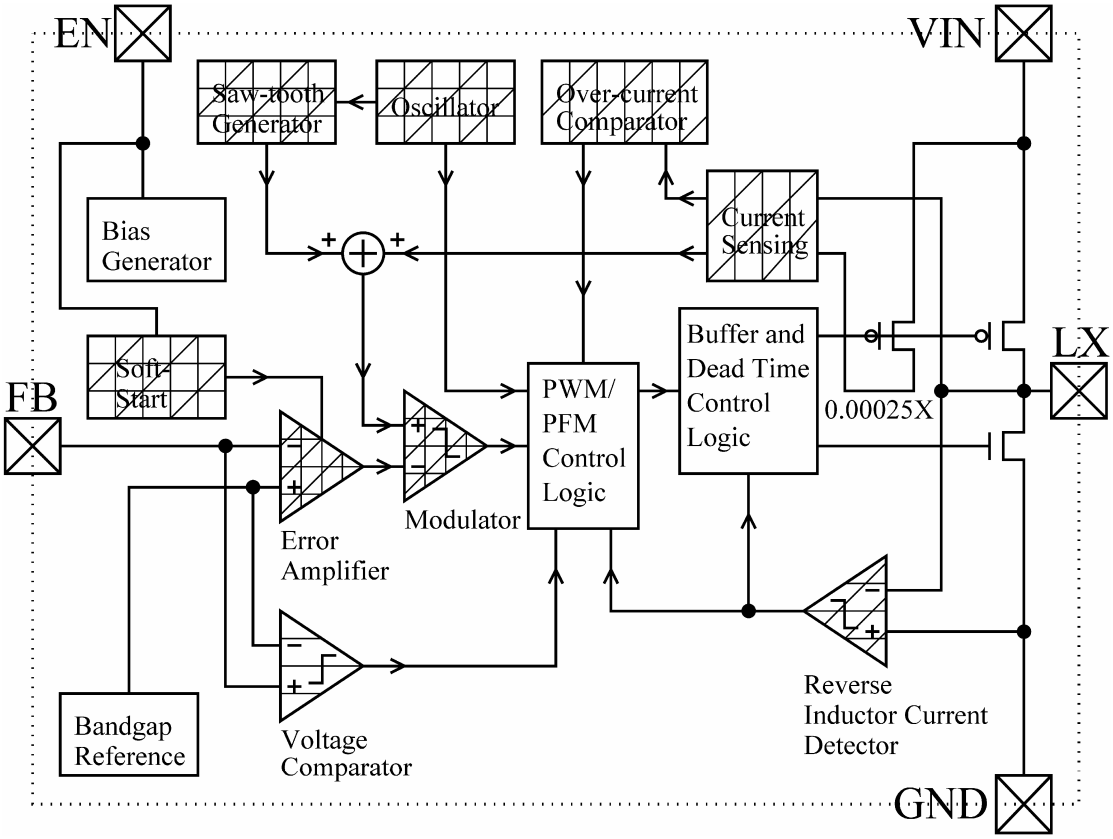


Fig. 3.6 DPSS in PFM mode. Blocks with horizontal lines are shut down when high side PMOS is turned on. Blocks with vertical lines are shut down when low side NMOS is turned on. Blocks with oblique lines are shut down when both power transistors are turned off.

When using DPSS, care must be taken as dealing with analog signal level between ON and OFF states. For example, if the analog signal level of the *Current Sensing* is not preset correctly when the *Current Sensing* is turned off, the *Current*

Sensing may give wrong information about the inductor current at the beginning of next cycle. This wrong information may result in unstable operation. On the other hand, timing of digital signal is also an important issue. For example, if the *Over-voltage Comparator* is not turned on slightly before the next cycle, the next pulse may cause the output voltage goes even higher during transient conditions. This high voltage may damage the circuits in load stage.

Simulation results show that in PWM mode, operating current can be reduced from 500 μA to 250 ~ 300 μA, depending on the duty ratio. In PFM mode, operating current can be reduced from 200 μA to 50 μA. The reduced operating current can effectively boost conversion efficiency especially in light load operation. For example, when V_{IN} = 3.6 V, V_{OUT} = 2.5 V and I_{LOAD} = 1 mA, the conversion efficiency is 89% and 75% with and without DPSS, respectively. Higher input voltage and lower load current will increase the difference. When V_{IN} = 4.2 V, V_{OUT} = 2.5 V and I_{LOAD} = 1 mA, the results are 88% and 72% with and without DPSS, respectively. When V_{IN} = 3.6 V, V_{OUT} = 2.5 V and I_{LOAD} = 0.5 mA, the results are 84% and 62% with and without DPSS, respectively.

3.3.3 Current Sensing and Slope Compensation

The current sensing circuit is one of the most important building blocks in current-mode control. There are many current sensing circuits available [47]-[54]. Among them we choose the current-conveyor-based sense-FET current sensing [48]-[53], [71] because it has some good features as follows:

1. It dose not need the extra pin-out and external component.

2. Its quasi-lossless characteristic could enhance the efficiency [52].

3. Matching devices, instead of $R_{DS\,(ON)}$ of MOSFET or passive component such as resistors, are used to improve accuracy (reported higher than 94% accuracy [48], [49]).

4. It can operate in low voltage [49] and has improved noise immunity [53].

5. It can be easily compensated [53] and has high speed response [53].

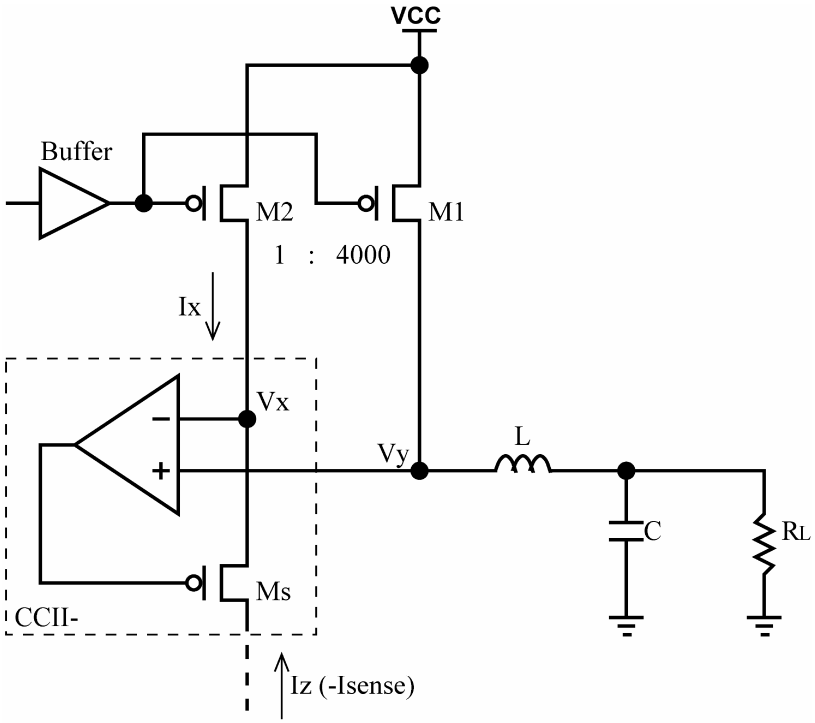


Fig. 3.7 Current-conveyor-based sense-FET current sensing.

The current sensing circuit is shown in Fig. 3.7. The second generation negative current conveyor (CCII-) [71] is enclosed in the dashed box. In our current sensing circuit design, we use the second generation current conveyor (CCII-) instead of the first generation current convey (CCI) used in [48]-[51]. The CCII has no current flow in terminal *Y*, thus eliminates the unused power dissipation and extra circuits.

According to the principles of CCII- [71], (3.8) and (3.9) were shown as follows:

$$V_X = V_Y \tag{3.8}$$

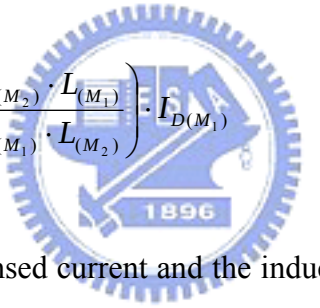
$$I_Z = -I_X \tag{3.9}$$

According to (3.4) and (3.5), when $V_{DS\ (M2)} = V_{DS\ (M1)}$ and $V_{GS\ (M2)} = V_{GS\ (M1)}$, we obtained:

$$I_{D(M_2)} : I_{D(M_1)} = \left(\frac{W}{L}\right)_{(M_2)} : \left(\frac{W}{L}\right)_{(M_1)} \tag{3.10}$$

From (3.9) and (3.10),

$$I_{sense} = I_Z = -I_X = I_{D(M_2)} = \left(\frac{W_{(M_2)} \cdot L_{(M_1)}}{W_{(M_1)} \cdot L_{(M_2)}}\right) \cdot I_{D(M_1)} \tag{3.11}$$



And the relationship of the sensed current and the inductor current can be determined by the aspect ratio of M_1 and M_2. As a result, accurate current information is obtained for the control loop of the current-mode control.

When dealing with current-mode control, there is a well known instability problem for duty ratio greater than 50% [46]. An artificial ramp acts as slope compensation must be added to the sensed current signal to suppress the sub-harmonic oscillation of the converter. How to generate a compensation ramp and add it to the sensed current signal is another issue. Conventionally, both the output of current sensing and the compensation ramp are expressed in “voltage” form [47]-[54]. We need a summing amplifier to add the compensation ramp (V_{ramp}) to the sensed current signal (V_{isense}) as shown in Fig. 3.8 (a) [47].

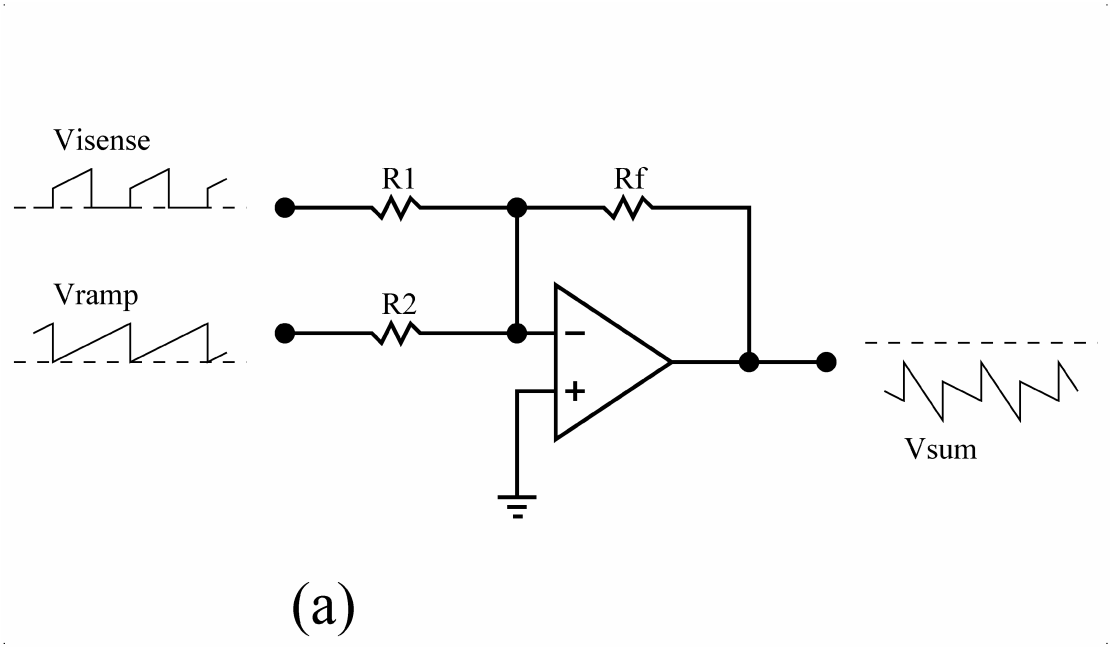


Fig. 3.8 (a) Adding compensation ramp and sensed inductor current signal.

(a) Summing amplifier.

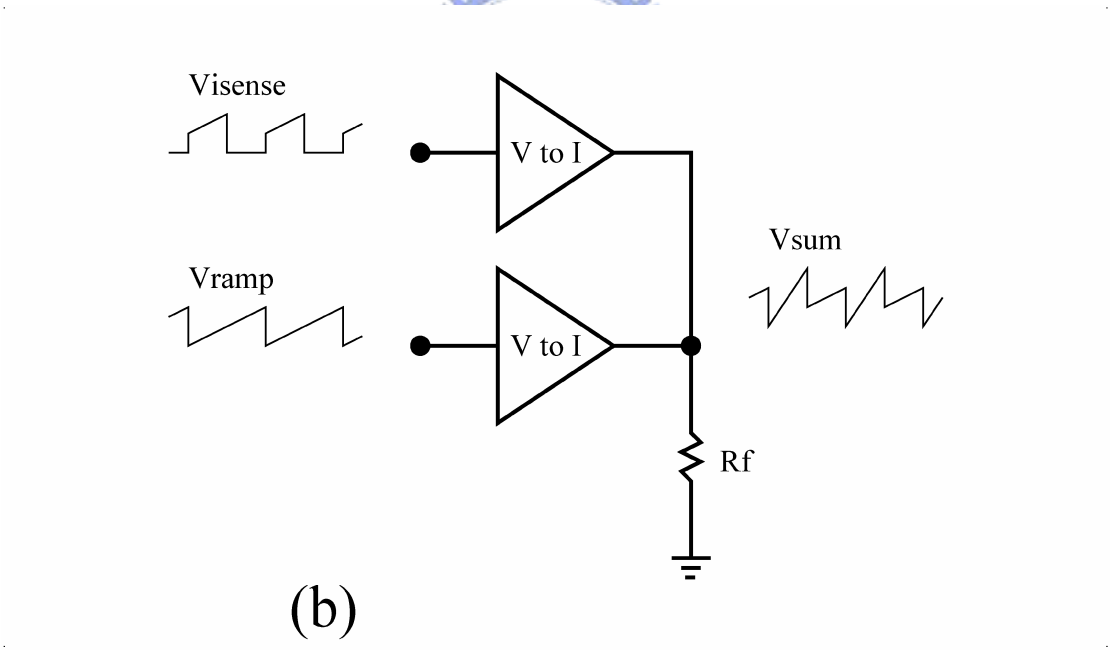


Fig. 3.8 (b) Adding compensation ramp and sensed inductor current signal.

(b) Use two V-to-I converters and adding the current signals by a resistor.

Another solution is to convert the current information (V_{isense}) and compensation

ramp (V_{ramp}) to "current" form by V-to-I converters, respectively. Then we add these two current together and get the summing voltage through a single resistor as shown in Fig. 3.8 (b) [48], [49]. These methods need multi-converts with complex circuits, and correspondingly, inducing more distortion to the desired signal.

To solve the above problem, we propose a simple and effective circuit as shown in Fig. 3.8 (c). Because the output signal I_{sense} of the current-conveyor-based sense-FET current sensing mentioned above is in current form, it does not need a V-to-I converter. On the other hand, the compensation ramp can be generated by charging a capacitor with a constant current and discharging it with clock pulses. In Fig. 3.8 (c), we leave out another V-to-I converter and directly connect the capacitor C_S to a resistor R_f. One end of the resistor R_f is grounded. I_{sense} and a constant current I_C flow into the top of C_S and R_f, respectively. The capacitor C_S and resistor R_f were grounded periodically by clock pulses. And we have the summing voltage V_{sum} at the top of Cs. We can calculate the V_{sense} and V_{sum} as follows:

$$V_{sense} = \left(I_{sense} + I_C\right) \cdot R_f \tag{3.12}$$

$$V_{sum} = \left(I_{sense} + I_C\right) \cdot R_f + \int_0^t \frac{I_C}{C_S} \tag{3.13}$$

Where t is the time elapsed from the end of clock pulse in each cycle. Except the desired sum of current information and compensation ramp, here we have an extra term "$Ic \times Rf$" in V_{sum}. This extra term is a constant value and can be used as a DC bias to avoid V_{sum} falling into the nonlinear region of error amplifier output [54]. For different applications of converter design, we can simply adjust the values of C_S and R_f to change the compensation slope or current gain to have the desired result.

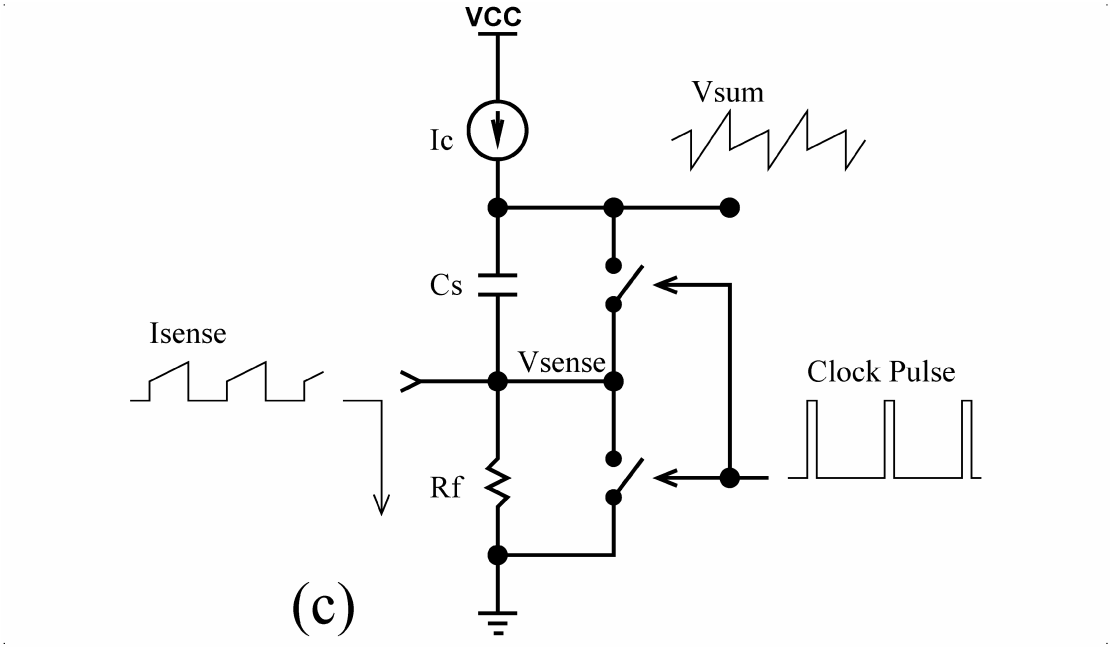


Fig. 3.8 (c) Adding compensation ramp and sensed inductor current signal.
(c) Proposed summing circuit.

3.3.4 Over-Current Protection

Over-current protection is very important in power supply design for safety reason. One of the benefits of current-mode control is cycle-by-cycle current limitation. However, because of the minimization of the inductor and the higher slope of current ramp, the switching frequency goes higher. As a result, the over-current protection needs higher speed in response to ensure safety.

The conventional over-current protection compares the sensed current signal (in voltage) with a reference voltage [53], [55]. If the sensed signal is higher than the threshold, it turns off the main switch (In our case the main switch is the high side PMOS) with an over-current signal as shown in Fig. 3.9 (a). The comparator delay was undesirable. In traditional voltage comparator design, for most circuit topology, the basic way to increase response speed is to increase operating current [56].

However, it is at the expense of power consumption and also conversion efficiency. Moreover, when the operating current goes higher, the speed of traditional voltage comparator will saturate due to the increase of parasitic capacitance and even larger operating current cannot help either.

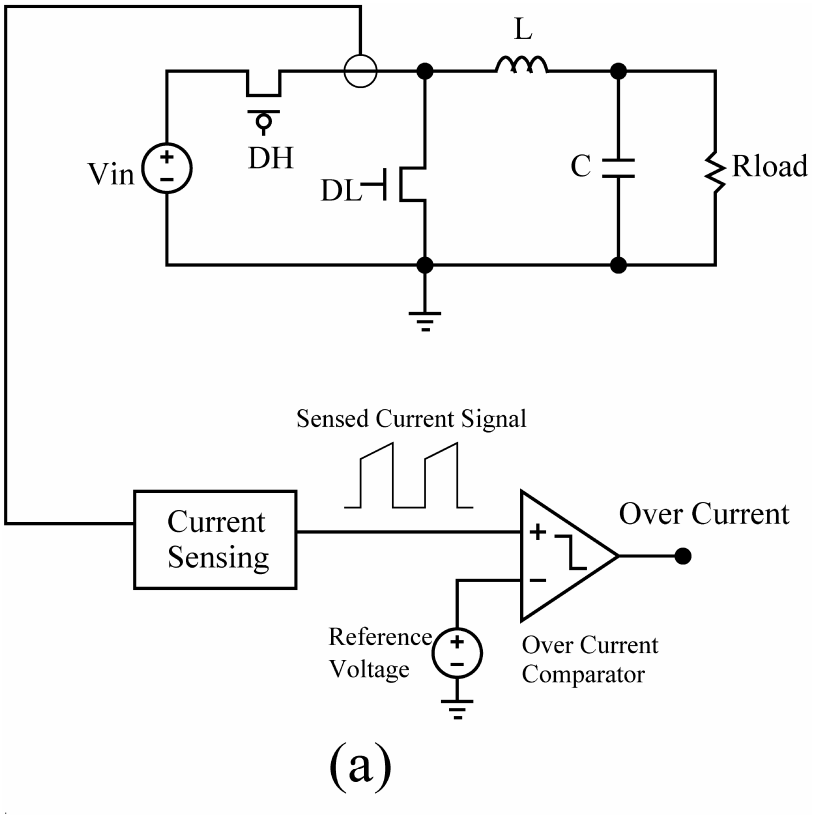


Fig. 3.9 (a) Over-current protection circuit.

(a) Conventional over-current protection circuit.

To solve this problem, we propose a new over-current protection circuit as shown in Fig. 3.9 (b). As mentioned in the preceding section, the I_{sense} is in current form. We utilize this characteristic of current sensing circuit and use a single transistor to achieve over-current protection. Note that the bias circuit located in left-down of Fig. 3.9 (b) can be any simple bias circuit used by other circuits in the converter to generate a bias voltage V_b. From (3.4) and (3.5), we know that when

$$I_{sense} > I_{D(sat.)(M_1)} = \frac{1}{2}\mu \cdot C_{OX}\frac{W}{L}(V_{GS} - V_t)^2 \qquad (3.14)$$

the drain voltage increases dramatically and the speed is determined by the excess current and parasitic capacitance at drain node. Inherently, it operates faster than the conventional voltage comparator. Moreover, because the current sensing and bias circuits are not newly created parts in the circuit, the quiescent current of the over-current protection circuit is zero. As a result, the simple circuit deals with the comparator response speed and power consumption at the same time.

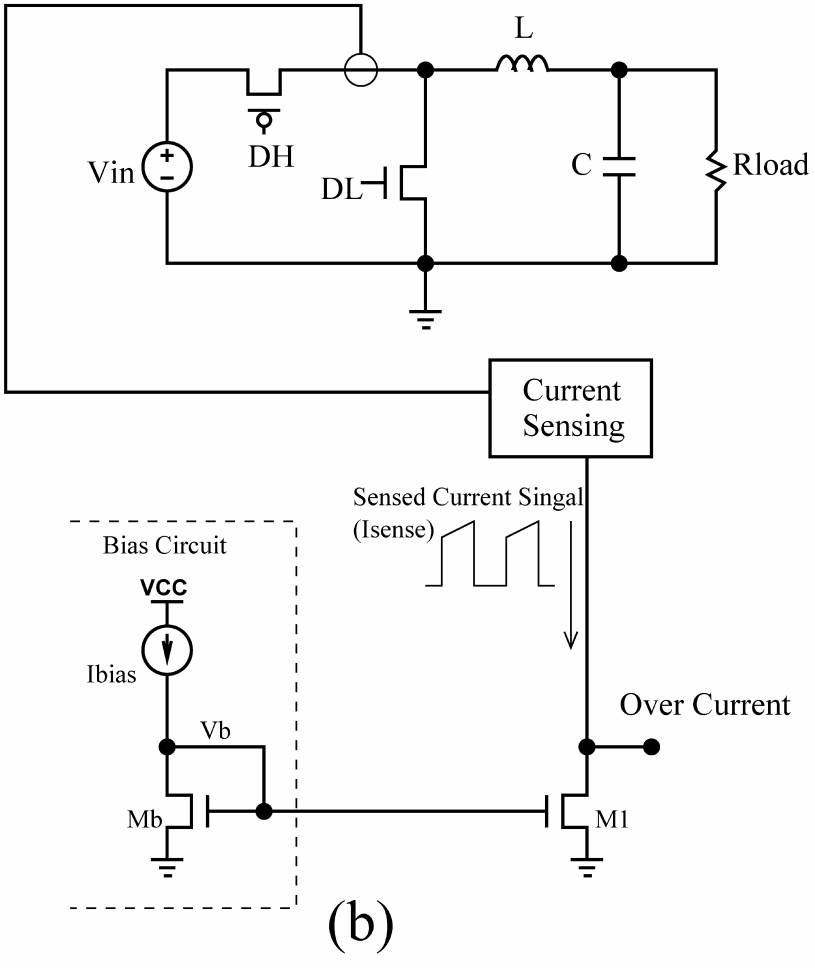


Fig. 3.9 (b) Over-current protection circuit.

(b) Proposed over-current protection circuit.

This circuit can be easily adjusted to fit various applications. As we know the value of I_{bias} and the aspect ratio of M_b, we can easily adjust the aspect ratio of M_1 to reach the desired current limit. Note that the $V_{DS\ (sat)}$ (equals to $(V_{GS} - V_t)$) must be smaller than the logic threshold to avoid M_1 operating in triode region, or the current limit will be smaller than the expected value and cannot be well defined.

3.4 EXPERIMENTAL RESULTS

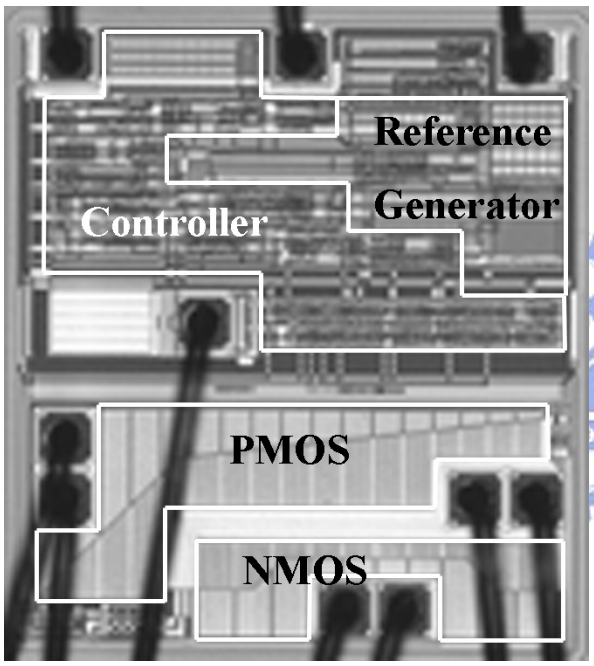


Fig. 3.10 Chip microphotograph.

All circuits described above are integrated in a monolithic current-mode buck converter and realized using a 0.6 μm 1P2M logic CMOS process. Fig. 3.10 shows the microphotograph of the silicon chip. The whole chip area is 1.35 mm^2 including the power MOSFETs and voltage reference circuit. The controller is measured 0.27 mm^2 including frequency compensator and on-chip oscillator. It doesn't need any pin-out and off-chip component for frequency compensation, voltage reference and clock generator. The experimental setup is shown in Fig. 3.11. There are only six

off-chip components needed, including bypass capacitor (C_{IN}) for V_{IN}, filtering inductor (L_{OUT}) and capacitor (C_{OUT}), resistors (R_1 and R_2) for setting the output voltage and a small capacitor (C_{FB}) for compensation of the parasitic capacitance at V_{FB}. The total PCB area was minimized. A typical set of component values is listed in Table 3.1. Unless otherwise specified, the following results are measured using the component values listed in Table I.

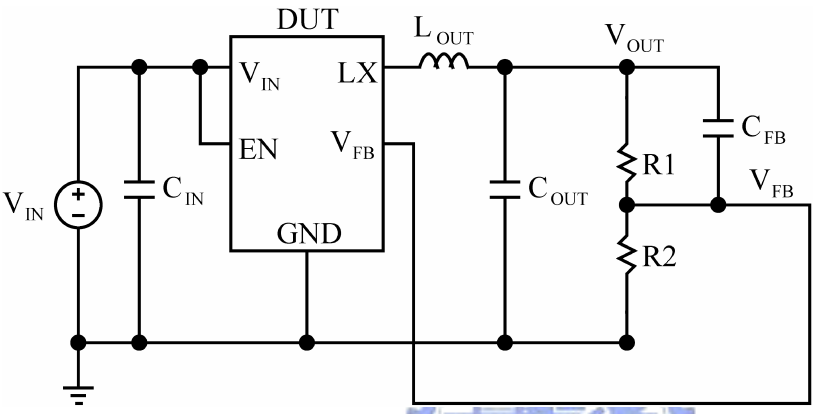


Fig. 3.11 Experimental setup of the monolithic buck converter.

C_{IN}	10 μF
L_{OUT}	4.7 μH
C_{OUT}	10 μF
R_1	1000 kΩ
R_2	316 kΩ
C_{FB}	22 pF
V_{IN}	3.6 V
V_{OUT}	2.5 V

Table 3.1 List of component values used in test setup

3.4.1 Soft-Start

The soft-start function has been tested. Fig. 3.12 shows the simulated input current and output voltage waveforms for 2.5 Ω (≈1000 mA) load at start-up. Fig. 3.13 shows the measured input current and output voltage waveforms at start-up. We

can see the experimental results match the simulation prediction. The soft-start function with soft-start time longer than 1.5 ms effectively suppresses the inrush current and overshooting of output voltage during start-up. The measured soft-start time doesn't change for various input voltage, output voltage and load current. Fig. 3.13 (a), (b), (c) and (d) show the start-up actions for different load current. It can be seen that both the input current and the output voltage follow the internal soft-start ramp until they reach the steady-state values.

3.4.2 Efficiency

The proposed converter incorporated with DPSS in both PWM and PFM mode gives very high conversion efficiency (> 88.5%) in a wide load range from 0.9 mA to 800 mA. The measured efficiency is greater than 85.5% even at 1000 mA load. The results are shown in Fig. 3.14 (a). Since we use a hysteresis switching algorithm for automatic PWM/PFM mode switching, the efficiency curves of PWM and PFM mode are overlapped over certain load range in Fig. 3.14. The maximum efficiency is over 96% at 60 ~ 200 mA load and peaks over 96.7% at 100 mA load under PWM mode. In PFM mode, the maximum efficiency is over 95% at 100 ~ 200 mA load.

Fig. 3.14 (b) shows the measured conversion efficiency for V_{IN} = 4.2 V. The efficiency still peaks over 96% for 120 ~ 200 mA load and is greater than 86% for 0.8 ~ 1000 mA load.

3.4.3 Steady State and Transient Response

In PFM mode, the measured quiescent current is 48.6 μA with DPSS. The waveforms of PFM operation are shown in Fig. 3.15. The interval between two

switching pulses is defined by load current. For heavier load, the switching pulses will get closer, and vise versa.

Fig. 3.16 shows the steady state waveforms in PWM mode. It can be seen that the converter is stable without sub-harmonic oscillation in both duty ratio greater and smaller than 50%. Ripples on output voltage are less than 3 mV. Measured line and load regulation are 0.07%/V and 0.08%/A, respectively. Transient response is shown in Fig. 3.17. The recovery time for a 500 mA step load-transient is less than 20 μs for 1% (25mV) tolerance of the final settling value. The output voltage drops and peaks less than 80 mV (≈3.2% of the nominal value of output voltage 2.5V) during the 500 mA load step-up and step-down transient, respectively.

3.4.4 Over-Current Protection

Fig. 3.18 (a) shows the waveforms of output voltage and inductor current at 2.5 Ω (≈1000 mA) load (normal operation). Fig. 3.18 (b) shows the waveform of inductor current when over-loaded (R_{LOAD} = 1 Ω). The proposed over-current protection circuit successfully limits the output current when over-loaded. The cycle-by-cycle peak inductor current is limited to 1.28 A.

3.4.5 Comparison

Table 3.2 summarizes the measured performance of the proposed converter. Table 3.3 shows a comparison with previously reported works [48], [72]-[75]. Incorporates with all the advancements described above, our design features the smaller die size and controller size with fewer off-chip components, higher conversion efficiency and wider operating range. Small output ripple voltage and fast

transient response are also included. Besides, on-chip soft-start and over-current protection functions ensured safety. All these features are realized in a low cost 0.6 μm 1P2M logic CMOS process.

3.5 CONCLUSION

A compact high efficiency monolithic current-mode buck converter is presented in this chapter. Novel features including on-chip soft-start, dynamic partial shutdown strategy, current-sensing, slope compensation and over-current protection circuits are demonstrated. These techniques reduce pin-outs and external components, upgrade efficiency, reduce circuit complexity and silicon area, ease design effort, ensure safety and can be applied to a wide operating range. The experimental results show that these novel features work well and the converter achieves very good performance at many aspects. The proposed converter is suitable especially for mobile devices that require high efficiency, small size and safety operation.

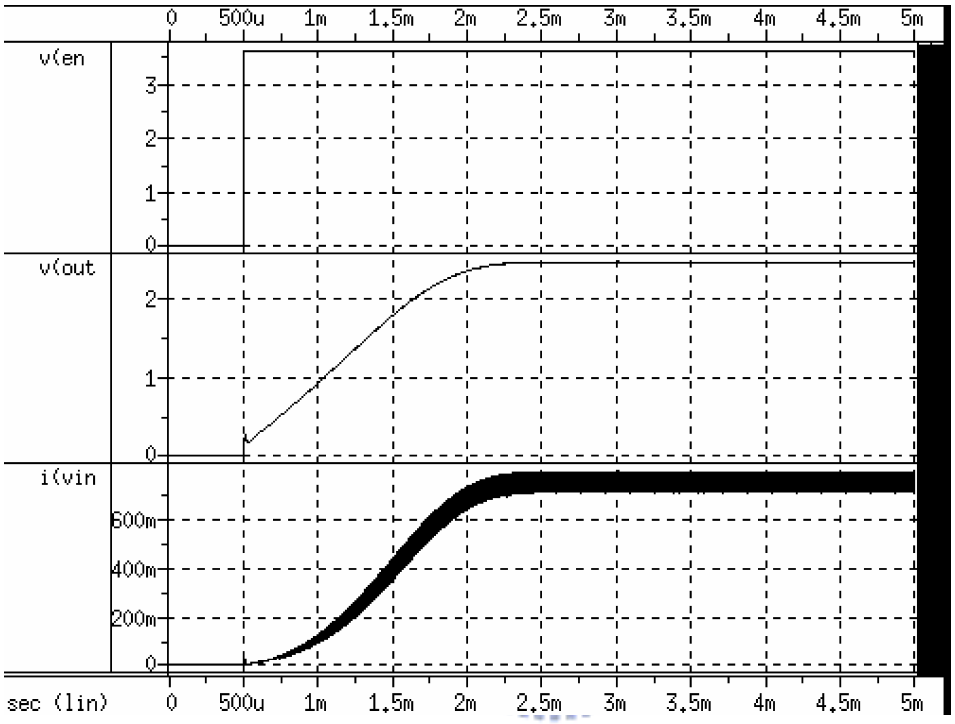
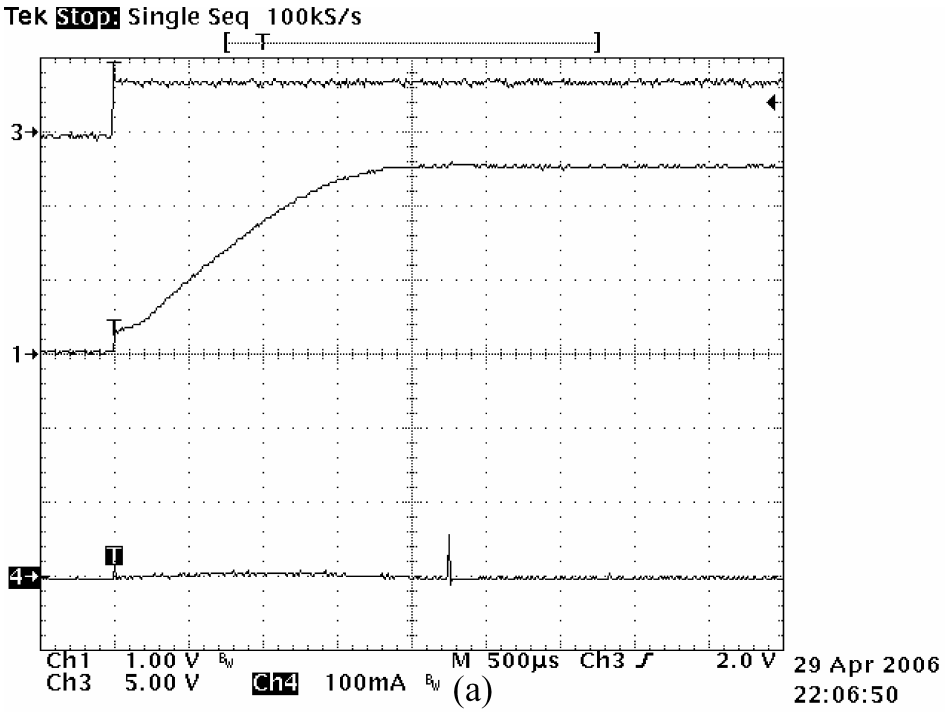


Fig. 3.12 Simulated waveforms of input current and output voltage during start-up with 2.5 Ω load (about 1000 mA at steady-state).



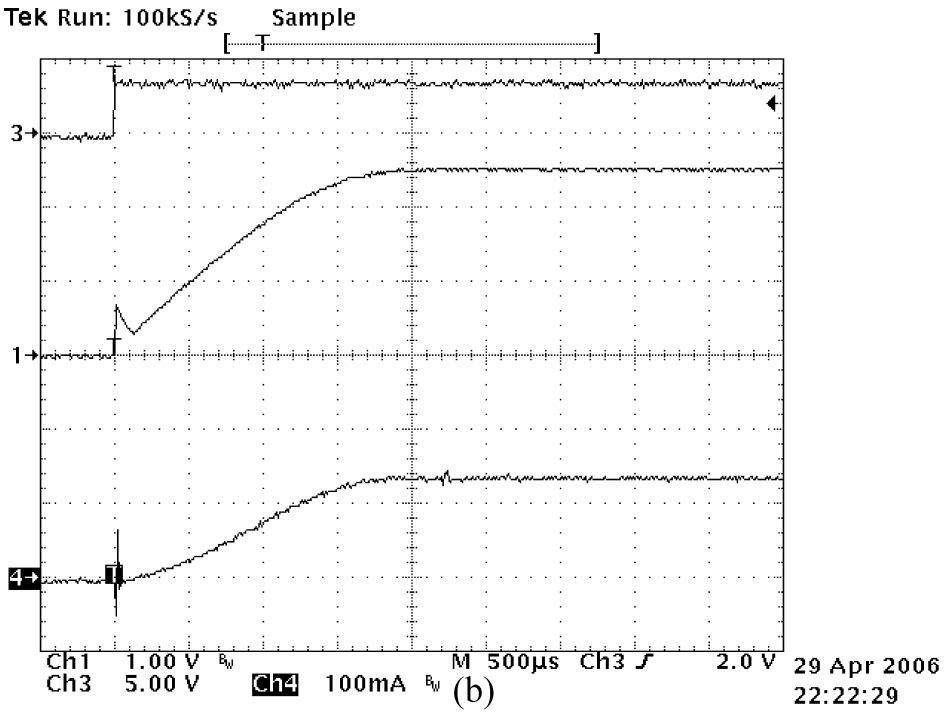
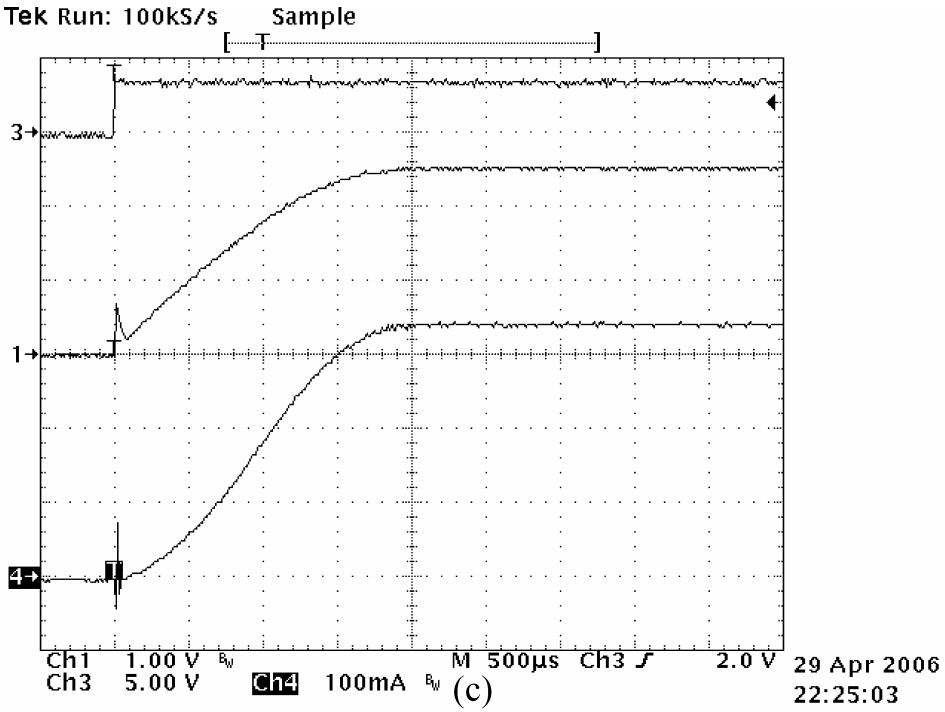


Fig. 3.13 (a) (b) Measured input current and output voltage during start-up. From top to bottom: *Channel 3* is chip enable, *Channel 1* is output voltage and *Channel 4* is input current.

(a) No load. (b) 12.5 Ω load (about 200 mA at steady-state).



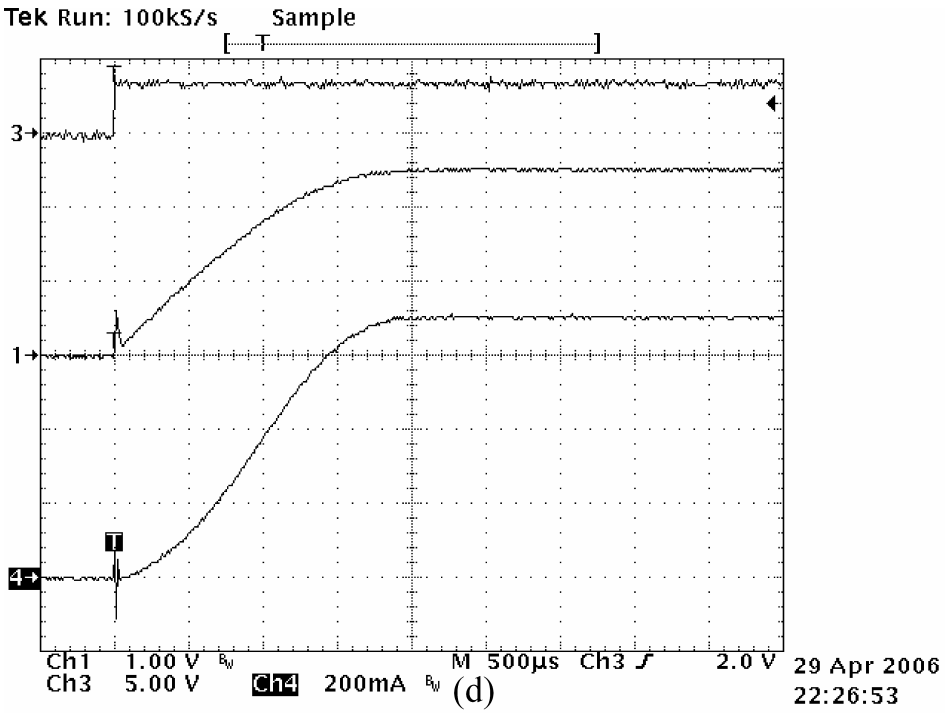


Fig. 3.13 (c) (d) Measured input current and output voltage during start-up. From top to bottom: *Channel 3* is chip enable, *Channel 1* is output voltage and *Channel 4* is input current.

(c) 5 Ω load (about 500 mA at steady-state).

(d) 2.5 Ω load (about 1000 mA at steady-state).

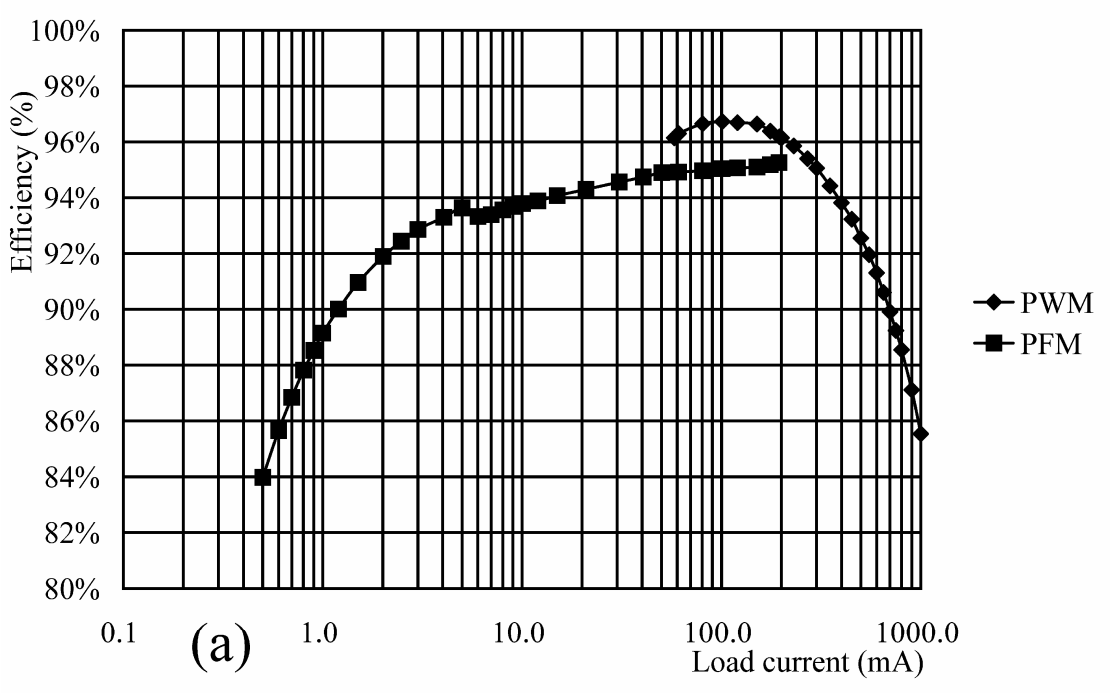


Fig. 3.14 (a) Measured conversion efficiency.

(a)V_{IN} = 3.6 V and V_{OUT} = 2.5 V.

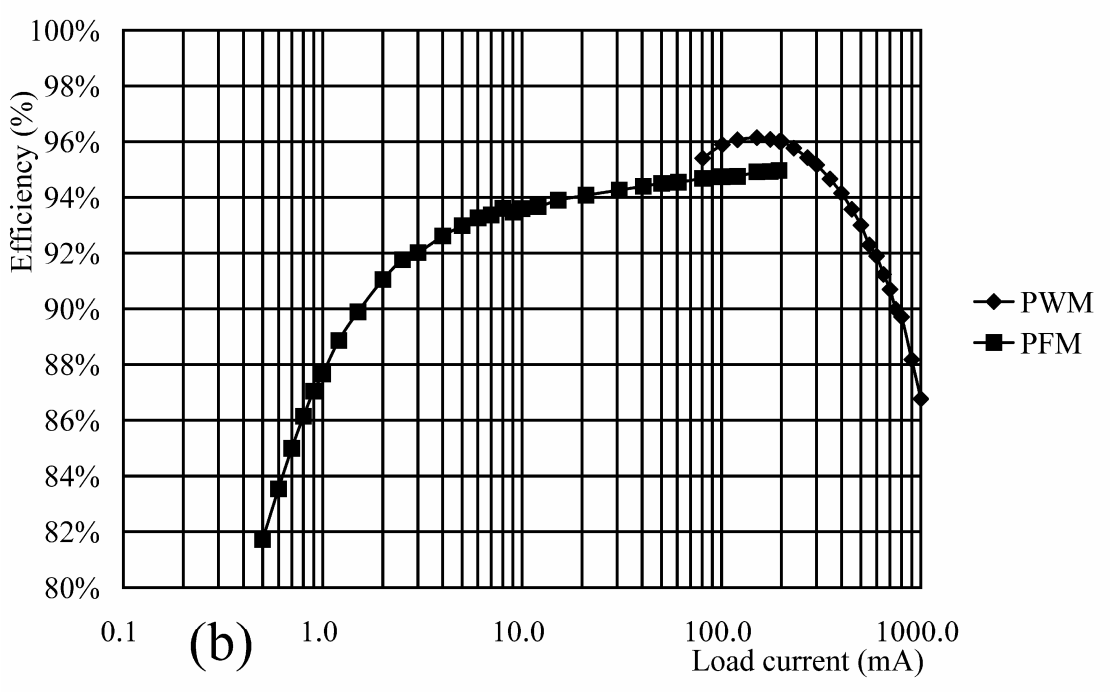


Fig. 3.14 (b) Measured conversion efficiency.

(b)V_{IN} = 4.2 V and V_{OUT} = 2.5 V.

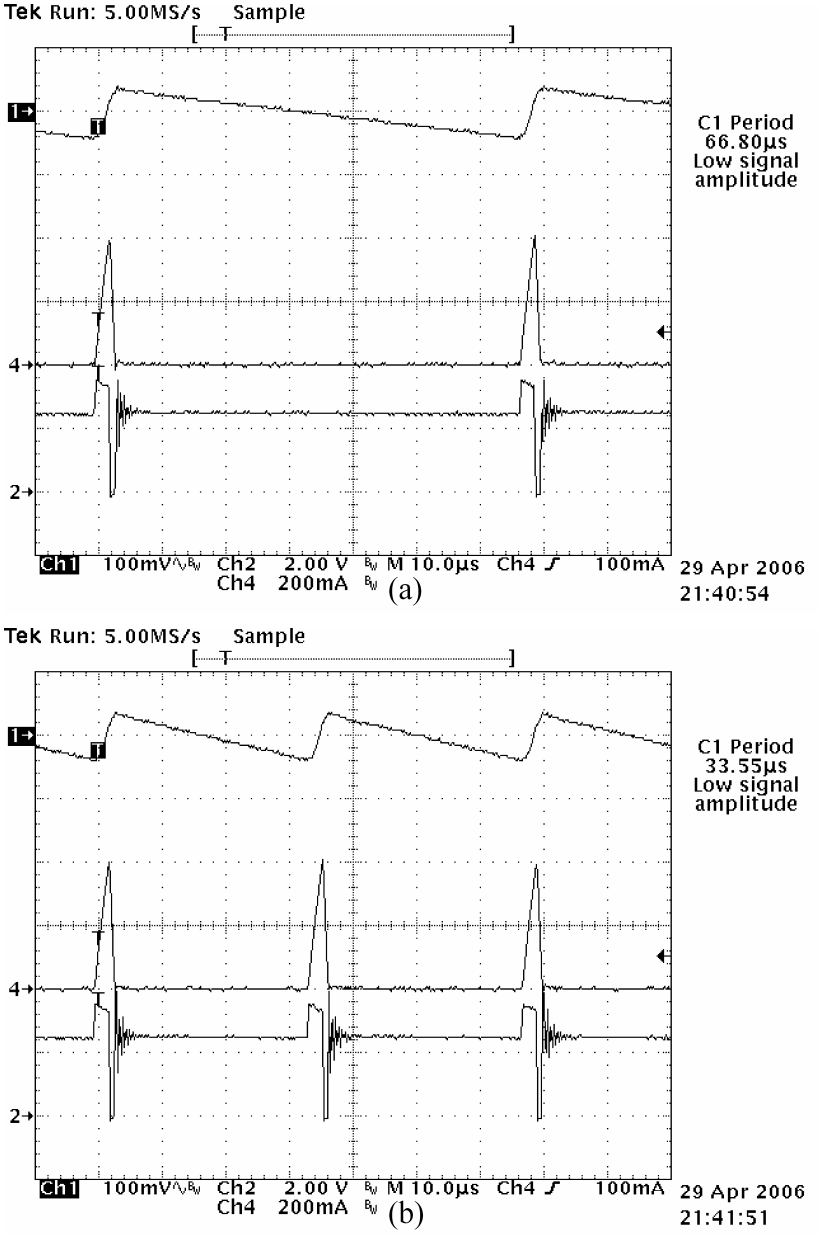


Fig. 3.15 Steady-state waveforms of PFM mode operation. From top to bottom: *Channel 1* is output ripple voltage (AC coupled), *Channel 4* is inductor current and *Channel 2* is switch node *LX*.

(a) 10 mA load.

(b) 20 mA load.

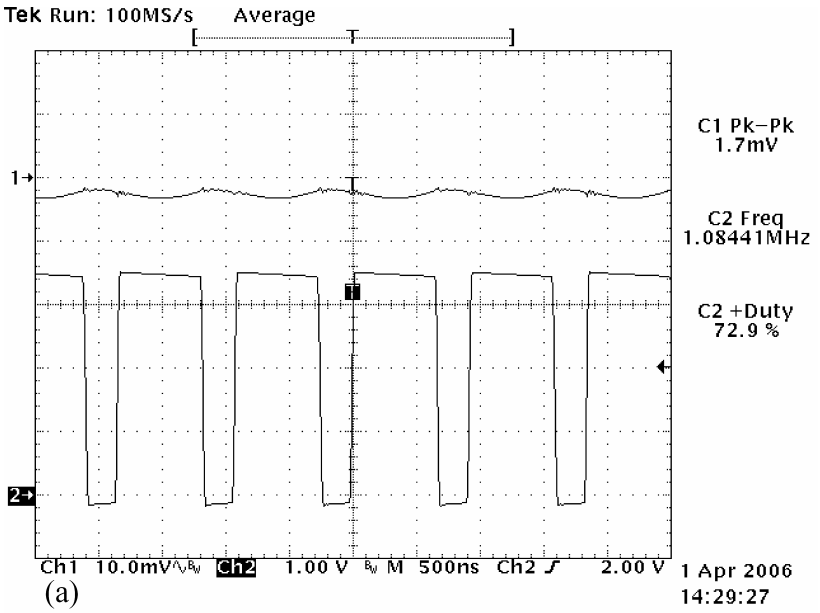


Fig. 3.16 Steady-state waveforms of the output ripple voltage (*Channel 1*, AC coupled) and the switch node *LX* (*Channel 2*) in PWM mode.

(a) Duty cycle > 50%.

(b) Duty cycle < 50%.

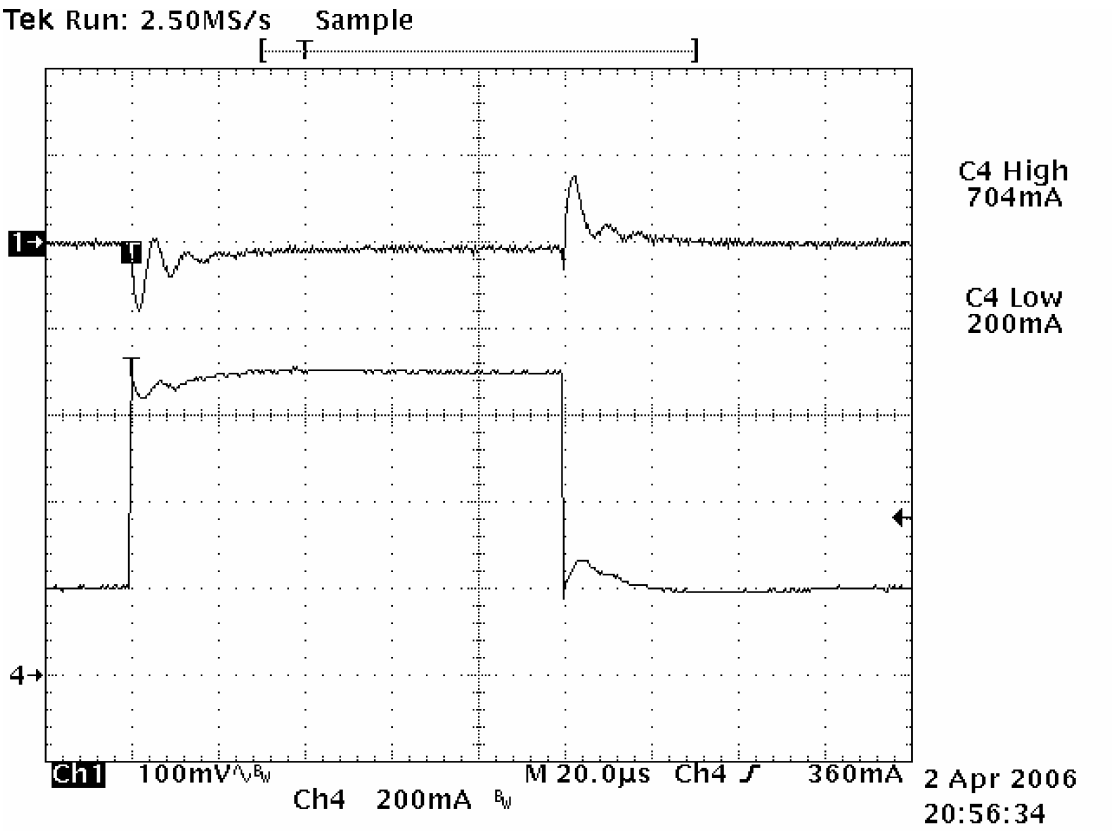
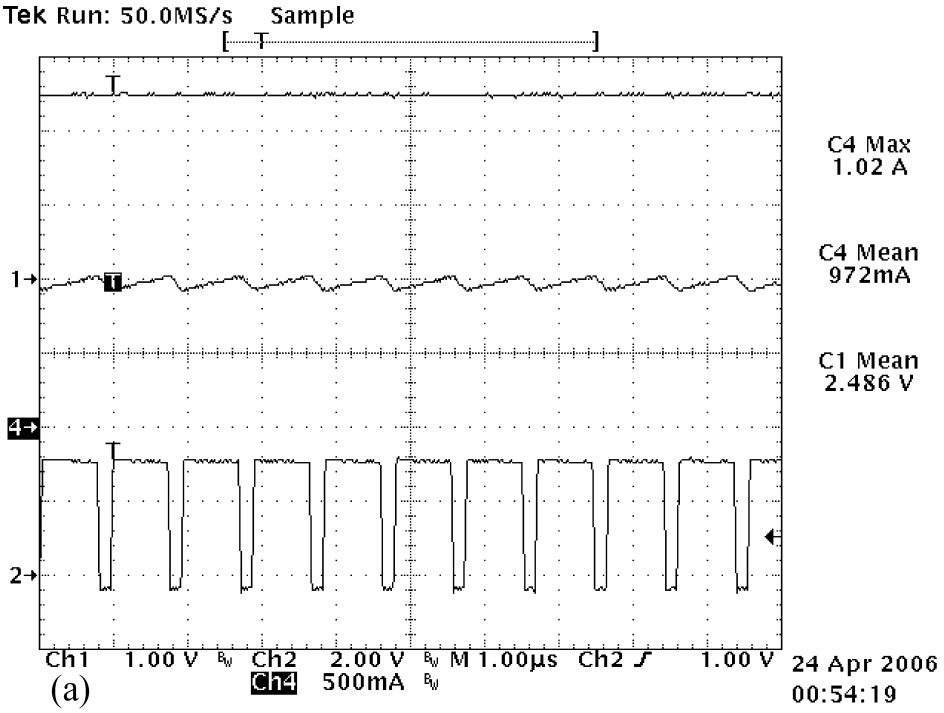
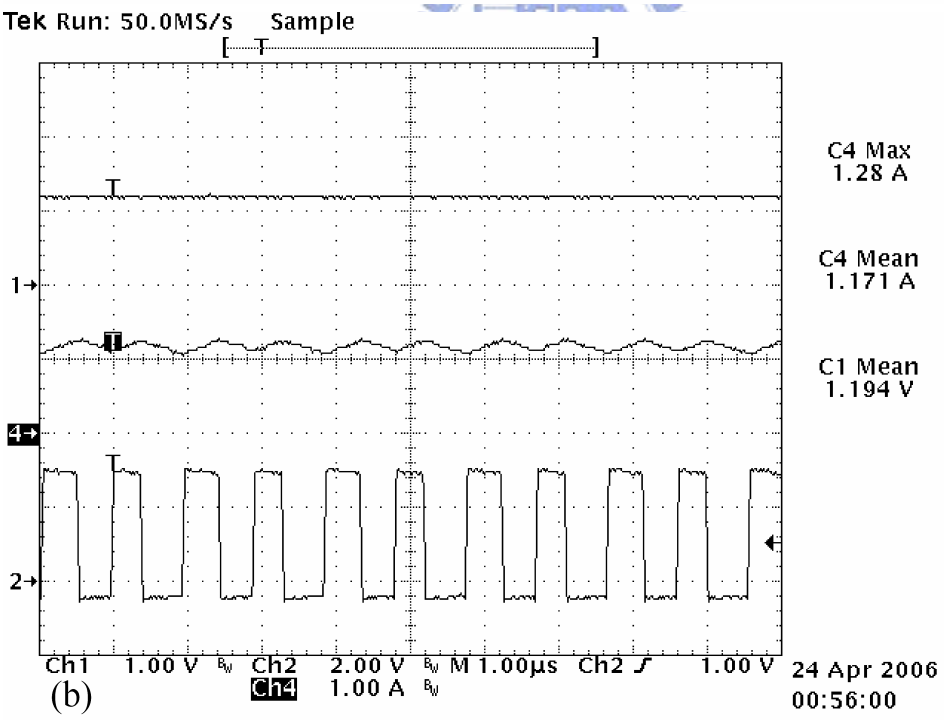


Fig. 3.17 500 mA step load-transient response. *Channel 1* is output voltage (AC coupled) and *Channel 2* is output current (step from 200 mA to 700 mA and from 700 mA to 200 mA).


Tek Run: 50.0MS/s Sample
C4 Max
1.02 A
C4 Mean
972mA
C1 Mean
2.486 V
Ch1 1.00 V Ch2 2.00 V M 1.00µs Ch2 1.00 V
Ch4 500mA
24 Apr 2006
00:54:19

(a)


Tek Run: 50.0MS/s Sample
C4 Max
1.28 A
C4 Mean
1.171 A
C1 Mean
1.194 V
Ch1 1.00 V Ch2 2.00 V M 1.00µs Ch2 1.00 V
Ch4 1.00 A
24 Apr 2006
00:56:00

(b)

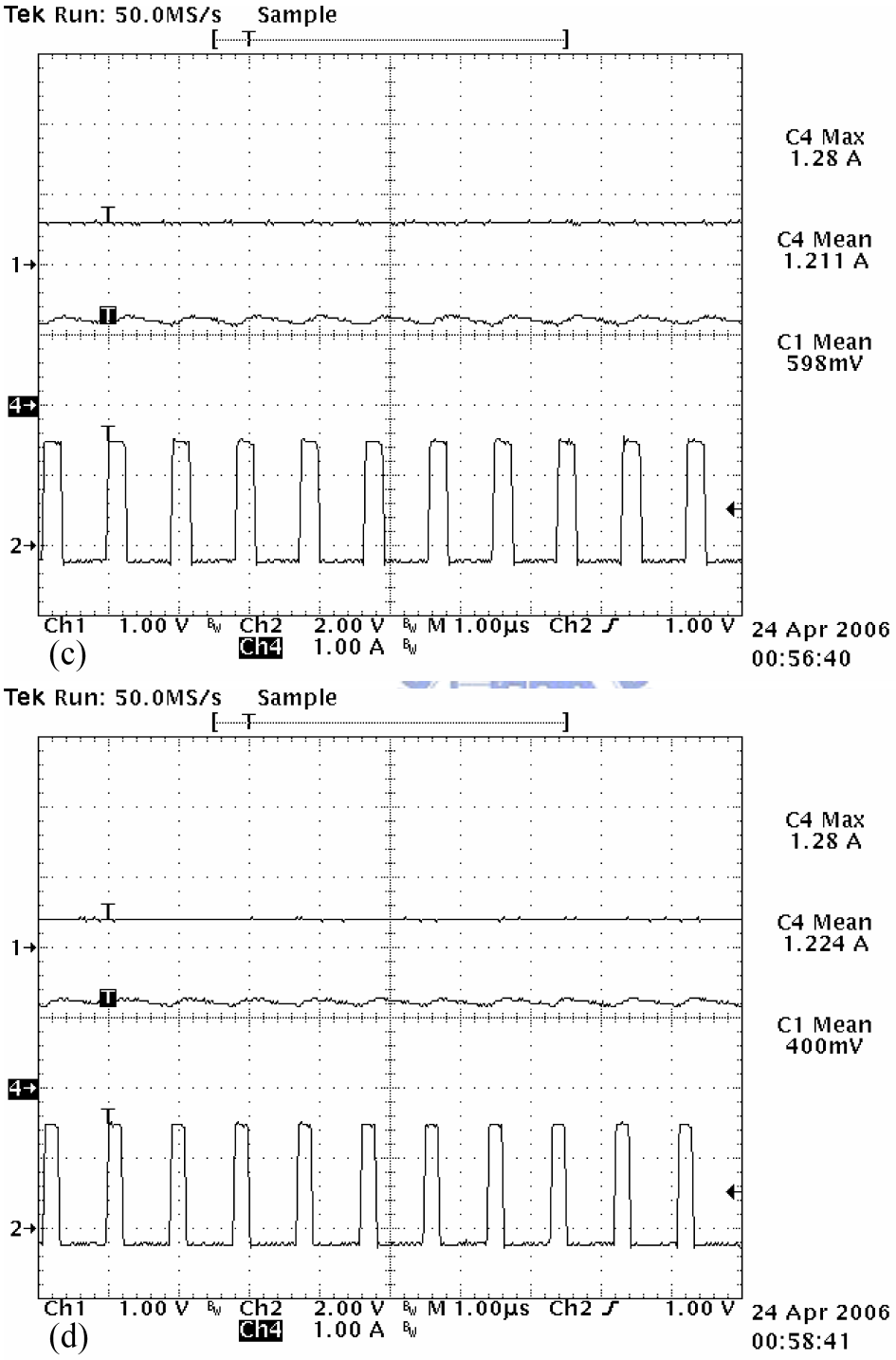


Fig. 3.18 Over-current protection test. From top to bottom: *Channel 1* is output voltage (DC coupled), *Channel 4* is inductor current and *Channel 2* is switch node *LX*.

(a) Normal operation with 2.5 Ω (about 1000 mA) load. (V_{OUT} = 2.5

V)

(b) The converter is over-loaded (R_{LOAD} = 1 Ω). The peak inductor current is limited to 1.28 A and the output voltage falls from 2.5 V to about 1.2 V.

(c) Increasing the load demand (R_{LOAD} = 0.5 Ω) causes output voltage to fall to about 0.6 V but the peak inductor current is still limited to 1.28 A.

(d) Further load demand (R_{LOAD} = 0.33 Ω) causes output voltage to fall to about 0.4 V but the peak inductor is still limited to 1.28 A.

Process	0.6 μm, 1P2M logic CMOS
Total die area	1.1 mm x 1.23 mm
Controller size	0.27 mm^2
Efficiency	88.5~96.7%@0.9~800mA load 85.5%@1000mA load (V_{IN} = 3.6 V, V_{OUT} = 2.5 V)
Input voltage range	2.2 ~ 6 V
Output voltage range	0.6 V ~ (Input voltage – 0.2 V)
Max. output current	1000 mA
Soft-start	> 1.5 ms
Quiescent current	48.6 μA (PFM Mode, No Switching)
Switching frequency	1.1 MHz
Inductor	4.7 μH
Capacitor	10 μF
Output ripple voltage	< 3 mV
Line regulation	0.07 %/V (Load current = 200 mA)
Load regulation	0.08 %/A (Load current from 200 mA to 1000 mA)
Transient recovery time (99 %)	< 20 μs @ 500 mA load step

Table 3.2 Summary of performance

	[48]	[72]	[73]	[74]	[75]	This work
Technology	0.6 μm	0.25 μm	0.5 μm, 1P3M	0.25 μm	0.6 μm, 2P3M	0.6 μm, 1P2M
Die size	2.87 mm^2 (*)	1.43 mm^2	2.31 mm^2 (*)	4.16 mm^2 (*)	3.78 mm^2 (*)	1.35 mm^2
Controller size	0.2575 mm^2	0.35 mm^2	0.54 mm^2	2 mm^2	0.78 mm^2	0.27 mm^2
Max. efficiency	89.5 %	95 %	93.7 %	92 %	92 %	96.7 %
Input voltage range	3.0 ~ 5.2 V	2.5 V	3.3 V	2.8 ~ 5.5 V	3.3 V	2.2 ~ 6 V
Output voltage range	< Input voltage - 0.2 V	1.5 V	0.9 ~ 2.5 V	1.0 ~ 1.8 V	0.2 ~ 3.0 V	0.6V ~ (Input voltage - 0.2 V)
Max. output current	450 mA	N/A	180 mA	400 mA	250 mA	1000 mA
Switching frequency	0.3 ~ 1 MHz	0.46 ~ 0.86 MHz	> 1 MHz	0.5 ~ 1.5 MHz	1 MHz	1.1 MHz
Inductor	4.7 μH	15.2 μH	N/A	10 μH	2.2 μH	4.7 μH
Capacitor	10 μF	21.6 μF	N/A	47 μF	47 μF	10 μF
Output ripple voltage	20 mV	< 15 mV	< 10 mV	2 mV	< 15 mV	< 3 mV
Transient recovery time (99 %)	N/A	< 10 μs @ 80mA load step	> 50 μs @ 90mA load step	N/A	50 μs @ 100mA load step	< 20 μs @ 500mA load step

(*) Reference voltage generator is not included in the chip.

Table 3.3 Performance comparison

CHAPTER 4

PRACTICAL DESIGN AND LAYOUT CONSIDERATIONS

4.1 INTRODUCTION

Most integrated circuits process signals rather than power. For power IC designers, there are many practical design and layout considerations different to the conventional signal processing (analog and digital) ICs. Since we deliver power to others, the current flow and power consumptions are usually large. How to ensure safety operation is one of the designer's task. How to gain the lowest $R_{DS(ON)}$ of the power transistors and use the smallest area is one of the major issues. In typical SMPS IC design, the $R_{DS(ON)}$ of the power transistors are usually several tens to hundreds of milli-ohm. When the resistance of a transistor switch is as low as the resistance of several squares of metal lines, to scale down the $R_{DS(ON)}$ is not only about enlarging the width of the power transistor. But we need to consider the resistance of metal routings. The switching noise is another big issue especially in SMPS ICs. We usually have huge power transistors that carry hundreds or thousands of milli-ampere of electric current and the power transistors continuously switch in hundreds of kilo-hertz in SMPS ICs. The switching noise is quite large. The ground bounces generated by the parasitic inductance of the bond wires are also a big issue. Since the current is discontinuous in the power switch of SMPS, the slope of current variation versus time is very large at every on/off state transition of power transistors. The

ground bounces caused by the parasitic inductance is proportional to the slope of the current variation versus time:

$$V_{inductor} = L_{parasitic} \frac{di}{dt} \tag{4.1}$$

Improperly design will raise the bounce voltage to several volts. The control signals may totally be destroyed and the SMPS IC will not work. Dead time control of the power transistors is also important. The above issues are not only concerning about the function of the SMPS ICs but also concerning about the performance like conversion efficiency and stability of the SMPS ICs. These practical issues will be discussed in this chapter.

4.2 DESIGN CONSIDERATIONS

4.2.1 Protection Functions

The protection functions are important in power supply design as described in section 2.4. We need to make sure the power supply will not destroy itself and the devices supplied by it in abnormal conditions. We had discussed about the inrush protection and over-current protection of the demo chip in chapter 3. Now we will briefly discuss about over-temperature protection, over-voltage protection and short-circuit protection in our design. These protection functions are also integrated in the monolithic current mode buck converter described in chapter 3.

The temperature sensor is a simple bipolar transistor. For a bipolar device we know that the V_{BE} has negative temperature coefficient [76]. We can use this characteristic of bipolar devices to generate the over-temperature alarm as shown in

Fig. 4.1. When the temperature is higher than the safety threshold of our design, the over-temperature signal will be issued and the power transistors will be turned off immediately. Thus the heat energy will not accumulate further. An important issue should be noted that the temperature sensor must be placed as close as possible to the heat generator center (usually the power transistors) to eliminate the temperature gradient effect in the chip. But the temperature sensor cannot be placed too close to the switching power transistors since the substrate of the power transistors usually have great noise and bouncing signals on it. These noise and bouncing signals may cause false over-temperature alarms and interrupt the power supply.

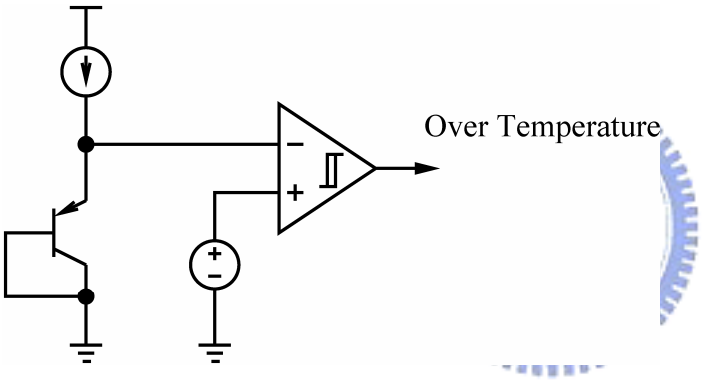


Fig. 4.1 Over temperature detector.

The over-voltage protection can be easily implemented using a voltage comparator. When we detect that the output voltage is greater than the tolerance of the specification, the over-voltage signal will be issued to turn off the power transistors. Thus the output voltage will stop going higher. In buck converters, sometimes the over-voltage condition is caused by short circuit of the high side power switch. Thus we may need to turn on the low side power transistor to force the output voltage to go down. Considering the above case, the low side power transistor must have lower on-resistance than the high side power transistor does.

The short-circuit protection is important in power supply design. Take the buck converter as example. As shown in Fig. 4.2, when the output is short to ground, i.e. $V_{OUT} = 0$, the ramping down slope of inductor current will approach zero. When the high side power transistor is turned on, the inductor current is going higher and keeps its value even the low side transistor is turned on in the later half of the cycle. As we turned on the high side switch, the inductor current will going higher and scarcely going down. So we cannot repeatedly turn on the high side power switch without inductor current accumulation. Thus we cannot prevent the inductor current going higher and higher by only sensing the current flowing in high side power transistor. This time we need to sense the low side current and keep the low side power transistor turned on until the current is lower than a safety threshold. Another simpler approach is lower down the switching frequency when the output voltage is lower than a safety threshold. In this approach, the accumulation of the inductor current can be eliminated by the longer on time of the low side power transistor. Care must be taken when using this approach. The turn on time of low side power transistor must have enough margins to ensure safety operation.

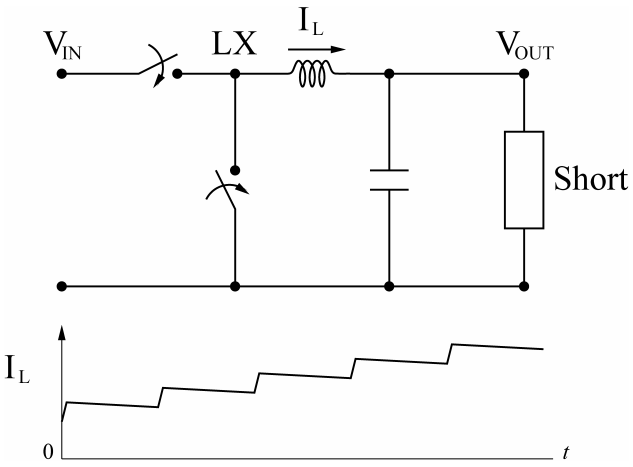


Fig. 4.2 The inductor current waveform of a buck converter when V_{OUT} is short to ground.

4.2.2 Dead Time Control

Dead time control is important in SMPS IC design. Improper design may cause efficiency loss. The body diode of the power transistor will be turned on during dead time. The effective resistance of body diode is usually much larger than the power transistors. For integrated power transistors, the conduction of body diode may cause huge substrate current. The substrate current may cause latch-up or affect the functions of the controller. But if the dead time is too short, the shoot-through current in the power transistors will cause great efficiency loss and switching noise. There are many approaches to control the dead time [77]-[79]. Many of them use complex circuits but still cannot ensure exact controlling of dead time. In our design, we use a simple circuit to implement dead time control. This approach still cannot exactly control the dead time according to the load condition, but it can provide relative good control over process and temperature variations.

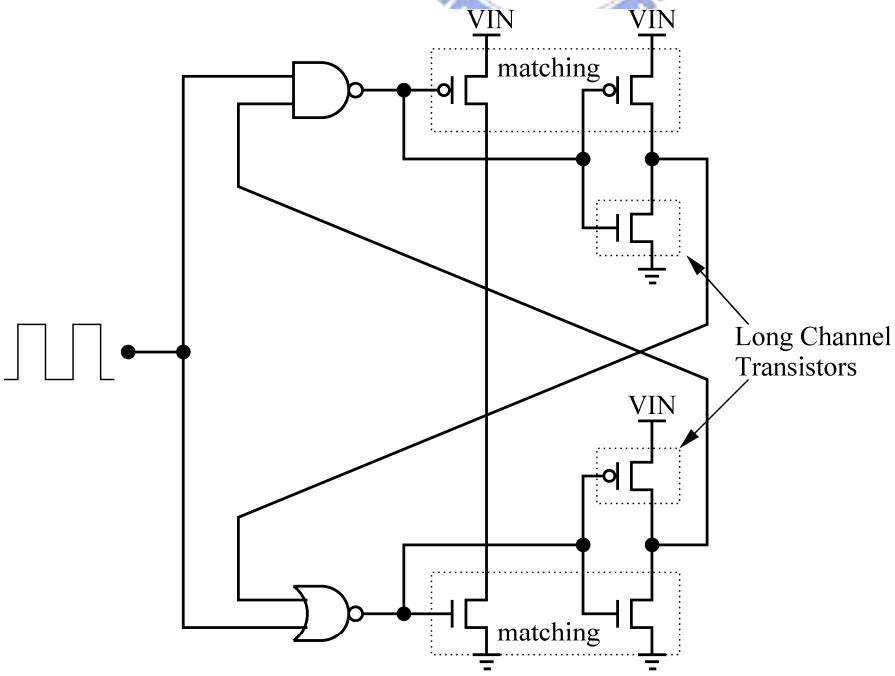


Fig. 4.3 Dead time control using biased inverters to sense the gate voltage of power transistors.

As shown in Fig. 4.3, the gate voltage of power transistors is sense by a biased CMOS inverter. The PMOS of the sensing inverter has the matching characteristics with the high side power PMOS, but the NMOS in the inverter is a long channel transistor. For the low side sensing inverter, the NMOS has the matching characteristics with the low side power NMOS but the PMOS is a long channel transistor. As the V_{GS} of the power transistor goes below the threshold voltage V_T of the transistor, i.e. the power switch is turned off, the sensing inverter issues the release signal and the other power switch can be turned on. Thus we can eliminate the shoot-through current of the power transistors. If we can shorten the delay from the sensing inverter to the gate of the other power switch, the dead time can be shortened and the extra loss caused by the body diode conduction can be minimized. We can use another sensing inverter to ensure that the low side NMOS turned on after the V_{LX} goes low. Thus we can track the load condition in a limited way. Since the power transistors are very large, the layout of dead controller is also important. The layout issues will be discussed in the next section.

4.3 LAYOUT CONSIDERATIONS

The layout style can greatly influence the performance of analog ICs. For SMPS ICs, most layout issues are concerning the power transistors. Proper layout can reduce the switching and bouncing noise caused by the switching power transistors. The influence of these noises to the control circuits can also be reduced. Since the power transistors are usually very large, the gate capacitances and parasitic resistances of the power transistors are also a considerable problem. The propagation time of the on/off signal through the whole power transistor can affect the operation of dead control and current sensing. The $R_{DS(ON)}$ of the power transistor is an important specification. How

to efficiently use the silicon area to get the lowest $R_{DS(ON)}$ possible is a real problem. In this section, we will deal with these problems.

4.3.1 Grounding of SMPS ICs

In mixed-signal IC design, we need to consider how to deal with "analog ground" and "digital ground" [76]. In SMPS IC design, we have a "power ground" in addition to the "analog ground" and "digital ground". Take the buck converter for example, the current flow through the power ground is in a pulse shape as shown in Fig. 4.4. The height of the current pulse is depending on the load conditions. The slopes of the current versus time during on/off transitions are hundreds milli-ampere over several nano-second. According to (4.1), if we assume the parasitic inductance of the bond-wire and the pin lead of the package is about tens nano-henry, the ground bounce caused by the current pulse can be hundreds milli-volt to several volts.

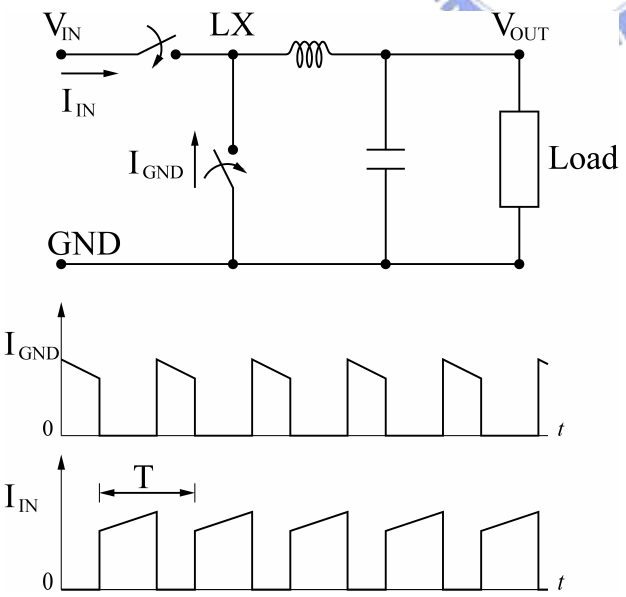


Fig. 4.4 Current waveforms of the power ground and the input of a buck converter that cause bouncing at both power ground and V_{IN}.

If we connect the analog ground to the power ground on the chip, the analog signal including the reference level would be totally destroyed. If we connect the digital ground to the power ground, the level of analog to digital interface will also suffer great influence. The digital gates controlled by the analog parts may issue wrong pulses. The wrong signal will propagate through the consecutive gates and generate more wrong actions. From this point of view, if we divide the power ground and the digital ground at the very tail of the whole controller, the effect of ground bounce will be minimized. So we can connect only the power transistors to the power ground. But this connection will cause another problem. When the power ground bouncing, the voltage level of power ground may be negative to digital ground and the difference may be larger than the turn on threshold of the power transistor as shown in Fig. 4.5. Thus the power switch may conduct current when it should be turned off. The high side power switch and the low side power switch will form a short path between input and ground. Since the $R_{DS(ON)}$ of power switches are very small, the shoot-through current will be very large. The input voltage will suffer abnormal drop and the efficiency will be degraded.

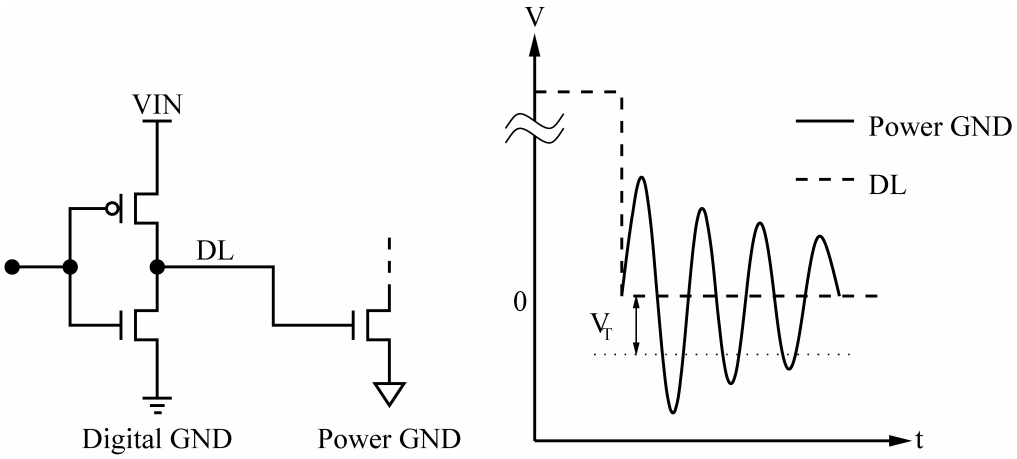


Fig. 4.5 Ground bouncing of "power ground" that cause false conduction of the power transistor.

To avoid this condition, we can connect the last buffer stage, which directly drives the power transistors, to the power ground. If the power ground bounces to a negative voltage, the gate of power transistor will be pulled as low as the bouncing voltage would be. Then the effect of ground bounce can be minimized. In addition to ground, the bouncing will happen at input or output node of the converter according to the converter topology. The solution of the ground bounce of a buck converter can be extended to solve these problems.

4.3.2 Gate Routing of Power Transistors

The gate widths of the power transistors in SMPS ICs are usually tens to hundreds milli-meter. The turn on/off delay of the power transistors will be much longer than typical digital gates. This long delay time will affect the slope of current versus time of the current pulses, the dead time control and the current sensing.

As described in previous section, the slope of current versus time of the current pulses is very large and may cause serious ground bounce. There are two ways to reduce the magnitude of the ground bounce. One of them is to reduce the parasitic inductance of the bond-wires and the package. The other is to reduce the slope of the current versus time of the current pulse. Since reduction of the parasitic inductance of the package is beyond the scope of our topic, we will try to reduce the slope of the current versus time of the current pulse. Now we can utilize the long turn on/off delay to reduce the bouncing effect. As shown in Fig. 4.6, we can route the gate of the power transistor as S-shaped. The on/off signal will propagate through the gate of the power transistor along the S-shaped gate. The power transistor will be turned on/off from one end to the other sequentially. The on-resistance of the power transistor will change slowly to the final value. The inductor current flow will smoothly alternate

between power transistors, and the slope of current versus time of the current pulse can be reduced. Thus we can reduce the magnitude of the bouncing. But if the turn on/off delay is too long, we will suffer from both shoot-through current and body diode conduction. Both of them will degrade the conversion efficiency and may cause additional switching noises. When body diode conduction occur, the slope of the current versus time of the current pulses cannot be further reduced because there exists another relative low impedance way to conduct inductor current. So we must keep the propagation path in a reasonable length and carefully avoid these unwanted effects.

Fig. 4.6 S-shaped gate routing of power transistor for reducing ground bounce.

This long turn on/off transition time will also affect the dead time control since we are sensing the gate voltage of the power transistors as described in section 4.2.2. If we want to avoid the shoot-through current, we need to ensure the sensed power transistor is turned off before we can issue the turn on signal to the other power transistor. From this point of view, we should sense the gate voltage at the tail of the gate routing. But if the delay time from the sensed turn off signal to the succeeding turn on signal is too long, the body diode conduction will occur. So we must keep the

delay time of sensed turn off signal to the succeeding turn on signal as short as possible.

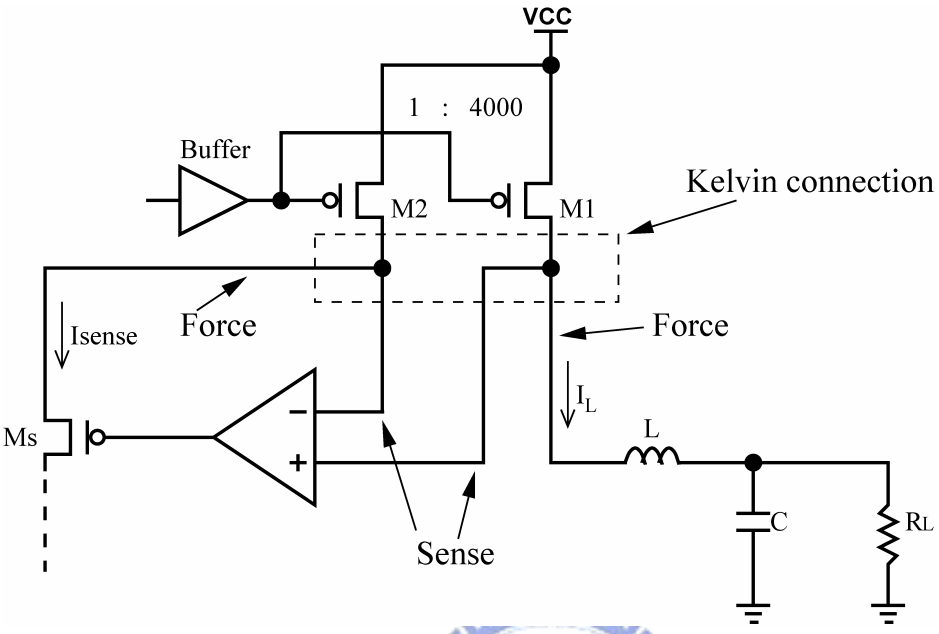


Fig. 4.7 Improving accuracy of current sensing by Kelvin connection.

Another effect of the long turn on/off transition time is about current sensing. For accurate current sensing, our goal is to keep the proportionality of the sensed current to the current flow in the power transistor. So we need to bias the current sensing transistor to the same biasing condition of the power transistor. But the power transistor is very large and the propagation time of the gate voltage is long. We need to connect the gate of the current sensing transistor to the tail of the gate routing of the power transistor to ensure the sensed signal will not be affected by the switching activity. A very short blanking time can be inserted to eliminate the unwanted current peak at the beginning of a sensing cycle. In addition, since the current flows through the current sensing transistor, we can connect the drain side of the current sensing transistor using *Kelvin connection* as shown in Fig. 4.7 [80]. The accuracy of the current sensing circuit will be enhanced.

4.3.3 On-Resistance of Power Switches

The conversion efficiency is directly affected by the on-resistance of the power switches. For integrated power switches, the on-resistances are tens to hundreds milli-ohm. The width of the power transistor are tens to hundreds milli-meter. The power transistors usually occupy more than 50 % area in an SMPS IC. How to reduce the area occupied by the power transistor without sacrificing the on-resistance is an important topic.

Since the on-resistance of the power transistors are in the same order as the resistance of several squares of metal lines, the metal routing will account for noticeable percentage of the total on-resistance. But the resistance of metal lines used in power transistors cannot be easily calculated due to their irregular shapes. So we write a small program, as shown in the appendix, incorporated with the SPICE simulator to evaluate the on-resistance of different layout of a 2-layer metal process. The simulation and measurement results are shown in Table 4.1.

Transistors	#1	#2	#3	#4	#5	#6	#7	#8
Measured On-Resistance with bond-wires (mΩ)	217	156	69	75	330	295	289	225
Single Transistor Emulation w. bond (mΩ)	77	77	51	55	197	190	179	182
Errors	182.2%	102.9%	35.7%	37.9%	67.8%	55.3%	61.6%	23.6%
First Order Approximation with bond-wires (mΩ)	313	327	95	93	396	373	465	272
Errors	-30.8%	-52.2%	-27.5%	-19.2%	-16.7%	-20.8%	-37.7%	-17.4%
Simulated On-Resistance with bond-wires (mΩ)	215	156	72	78	316	279	299	232
Errors	0.9%	0.0%	-4.5%	-3.8%	4.6%	5.8%	-3.2%	-3.1%

Table 4.1 Comparing measurement and simulation results of the on-resistance of the power transistors.

Both of them include the resistance of bond-wires, metal lines, and power transistors. We can see the accuracies of simulation estimation are within 6 %. Compared with the single transistor emulation and the first-order metal resistance estimation, we can see that the traditional estimation results in –52.2 % ~ 182.2 % error. These errors will greatly influence the design of power transistors. We may suffer from costly larger power transistor and larger switching loss and switching noises. Or we may suffer from higher on-resistance and lower conversion efficiency. This small program gives us useful estimations for power transistor layout.

From the experience point of view, we bring up three points concerning the on-resistance. These suggestions can be applied to a 2-layer metal process and need some modifications for other processes. First, minimize the length of first layer metal fingers. Since the square resistance of the lower metal layer is usually greater than higher metal layer does, reduce the length of first layer metal fingers will show great reduction of the total on-resistance. Second, use wider and shorter second layer metal plates to reduce the effective number of squares of the metal plates. Although the square resistance of the second layer metal is lower than that of the first layer metal, it can account for a considerable portion of the total on-resistance. Use wider and shorter plates will result in lower resistance. Third, use multiple bond-wires and distribute the bond-pads to a wider range of the layout area of the power transistor. If we increase the number of bond-wires, the resistance of bond-wires can be reduced with increasing cost of the package. Another side effect is that the bond-pads need to occupy silicon area. So we have to trade off between the number of bond-pads and the cost. Distribute the bond-pads to a wider range will reduce the effective number of squares of the top layer metal and the on-resistance can be reduced.

Fig. 4.8 illustrates three examples to explain these suggestions. The power transistors occupy the same area in Fig. 4.8 (a), (b) and (c). In Fig. 4.8 (a), the first layer metal fingers are much longer than the fingers in (b) and (c). The resistance of these longer fingers is larger. The second layer metal plates in Fig. 4.8 (a) and (b) both have more effective number of squares counted from the bond-pads to the other end of the metal plate. They also contribute more resistances. The bond-pads are most deconcentrated in Fig. 4.8 (c). From the above observation, we can conclude that the power transistor in Fig. 4.8 (c) will show the lowest on-resistance than (a) and (b) do. From our experience, the layout style of Fig. 4.8 (a) and (b) may double the on-resistance although they occupied the same area as (c) does.

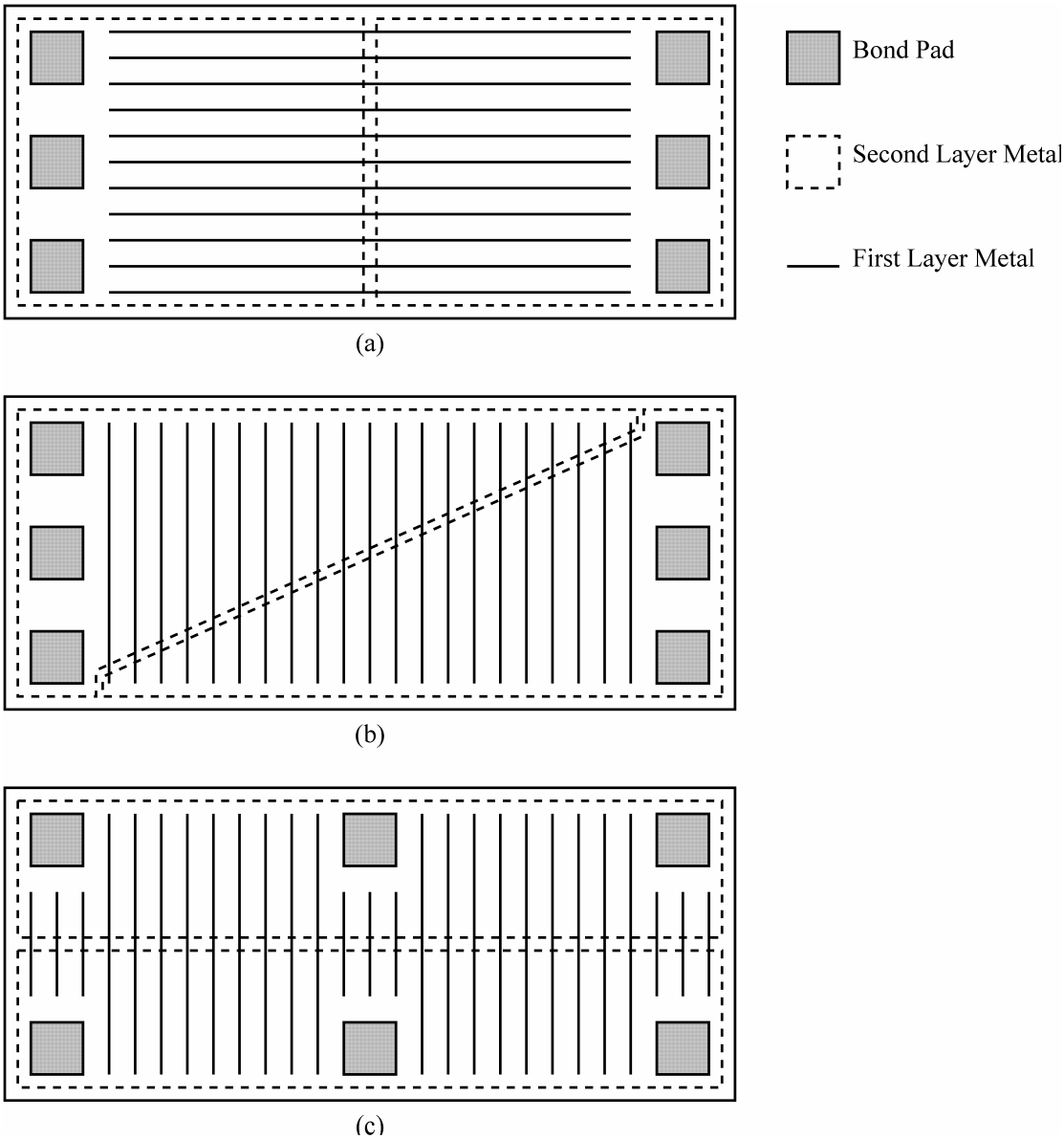


Fig. 4.8 Examples of power transistor layout. On-resistance: (a) ≈ (b) > (c)

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

In this dissertation, we discuss about the SMPS for DC-DC power conversion. Basic topologies of non-isolated DC-DC SMPS are introduced. Safety considerations for power supply design are discussed. The design specifications are also included. Based on the knowledge of DC-DC SMPS, we developed several new circuit techniques to achieve high conversion efficiency, compact converter size, wide operating range, fast transient response and safety operation. These developed circuit techniques were realized in a monolithic current-mode buck converter. The application of these circuit techniques can be extended to other topologies like boost and buck-boost of SMPS design, especially in integrated circuit power converter design.

5.1.1 On-Chip Soft-Start Circuit

The on-chip soft-start circuit occupies a small silicon area and eliminates the need of extra pin-out. This circuit achieves one to tens of milliseconds soft-start time using series MOS transistors and a small on-chip capacitor. This circuit prevents the inrush current during the start-up of the power module. It provides safety operation and shrinks the converter size in the same time. Another benefit of the proposed circuit technique is that because of its simplicity, it can be easily adopted for any other

power supply IC design.

5.1.2 Dynamic Partial Shutdown Strategy (DPSS)

The DPSS is a power management strategy. By exploiting the switching characteristic of SMPS, we developed this strategy. This strategy eliminates the unwanted waste of operating current and keeps the circuit performance at the same time. The DPSS improves the conversion efficiency especially in light load operation. Thus the standby time of battery operated devices can last longer by utilizing DPSS. Combined with the PFM mode, the conversion efficiencies are improved from 62 % ~ 75 % to 84 % ~ 89 % measured in our test chip.

5.1.3 Current Sensing, Slope Compensation and Over-Current Protection

In our design, we choose a quasi-lossless current conveyor based current sensing technique to implement our current-mode control. By exploiting the characteristics of this current sensing technique, we developed the slope compensation circuit and the over-current protection circuit. The proposed slope compensation circuit has reduced circuit complexity than traditional ones thus the silicon area is saved. The signal distortion is also reduced because we eliminate the multi-conversions of signals. The over-current protection is also simpler than traditional ones. The benefits of the over-current protection circuit are reduced silicon area, reduced power consumption and faster response for safety operation. Additionally, these circuits can be easily designed and adjusted. So we can achieve good regulation and wide operating range. These circuit techniques can also be applied to other topologies for different applications.

Incorporating with other basic protection schemes, the above techniques are integrated into a demo chip. From the measurement results, we can see the effectiveness of these developed techniques.

5.2 FUTURE WORK

For further efficiency improvement, we can investigate the power losses in the SMPS. The switching loss is one of the major losses in the SMPS. We can segment the power MOSFETs into parts for reducing gate drive loss [81]. We can also adjust the gate drive voltage dynamically according to the load condition [82]. These techniques can further improve conversion efficiency in light load operation at a price of increasing cost and circuit complexity.

Another interesting topic is about improving transient response. Although the proposed current-mode converter shows good transient response compared with others, it can not meet the specifications for supplying the high speed CPUs in personal computers. There are several ways to achieve faster transient response. An interesting one is nonlinear control [22], [83]. We may find other ways to control the SMPS to achieve faster response. Another straightforward method is higher switching frequency [21], [84]. This is much depending on the manufacturing process of the semiconductor power switches. Multi-phase design can also help improving transient response, but the cost is increased proportional to the number of phases they provide [21]-[22], [85]. Other purposed techniques also have their own disadvantages [86]-[90]. Except these developing techniques, we may try to find another way to achieve our goal in the future.

The EMI is also an interesting topic. The fixed frequency operation shows a tone

in frequency spectrum that is high. Adding some random jitter may reduce the height of this tone, but the spectrum may spread into a wider range. Which one of them generates less interference to other circuits can be investigated in the future. If the spread spectrum is the answer, how to inject a random jitter but not affect the stability of the converter is another interesting topic.

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APPENDIX

A perl program generates SPICE netlist for calculation of $R_{DS(ON)}$ of power transistor

```
#! /usr/bin/perl/ -w

$mos_width=4.8;
$pmos="pmos_4.8u";
$nmos="nmos_4.8u";
$M2_step=4.8;

open (INPUT,"./input_g5626a_nmos_mod") || die "$!";
open (OUTPUT,">./output_g5626a_nmos_mod") || die "$!";

#       Rpp_sheet       =       113;
#       Rnn_sheet       =       70.1;
#       R_CON_P                 =       150;
#       R_CON_N                 =       28;
#       R_M1_sheet      =       0.074;
#       R_VIA           =       0.6;
#       R_M2_sheet      =       0.037;

#   List of variables
#
#       $R_CON_P;       P-type contact resistance
#       $R_CON_N;       N-type contact resistance
#       $R_M1;          Sheet resistance of M1
#       $R_VIA;         VIA resistance
#       $R_M2;          Sheet resistance of M2
#       $mos_width;     Unit MOS width
#       $multiplier;    Transfer length into integer
#       $mos_w_cal;     Transferred MOS width
#       $mos_cal_half;  1/2 of transferred MOS width
#       $polygon_m2_d;  Number of DRAIN side convex polygons in M2 layer
#       $polygon_m2_s;  Number of SOURCE side convex polygons in M2 layer
#       $polygon_m1_p;  Number of POSITIVE convex polygons in M1 layer
#       $polygon_m1_n;  Number of NEGATIVE convex polygons in M1 layer
#       $j;             Reusable counting variable
#       $i;             Reusable counting variable
#       $xi;            <STDIN> x-coordinate of the M1 convex polygon
#       $yi;            <STDIN> y-coordinate of the M1 convex polygon
#       $right;         $right>0 indicates this corner point is at the left side of the line formed by previous 2 points and vice versa.
#       $max_x_m2;      Maximum x-coordinate of the M2 convex polygon
#       $max_y_m2;      Maximum y-coordinate of the M2 convex polygon
#       $min_x_m2;      Minimum x-coordinate of the M2 convex polygon
#       $min_y_m2;      Minimum y-coordinate of the M2 convex polygon
#       $max_x_p;       Maximum x-coordinate of the POSITIVE M1 convex polygon
#       $max_y_p;       Maximum y-coordinate of the POSITIVE M1 convex polygon
#       $min_x_p;       Minimum x-coordinate of the POSITIVE M1 convex polygon
#       $min_y_p;       Minimum y-coordinate of the POSITIVE M1 convex polygon
#       $max_x_n;       Maximum x-coordinate of the NEGATIVE M1 convex polygon
#       $max_y_n;       Maximum y-coordinate of the NEGATIVE M1 convex polygon
#       $min_x_n;       Minimum x-coordinate of the NEGATIVE M1 convex polygon
#       $min_y_n;       Minimum y-coordinate of the NEGATIVE M1 convex polygon
#       $perpendicular; 1:polygate perpendicular to x-axis; 0:polygate parallel to x-axis
#       $width_m1;      Width of each M1 line
#       $gap_M1;        Gap between M1 lines
#       $mos_type;      PMOS:0, NMOS:1
#       $M2_step;       $M2_step indicates the distance between the nearest M2 points alone poly-silicon (in um)
#       $step_x; $step_x/$multiplier indicate the distance between the nearest M2 points alone x-axis
#       $step_y; $step_y/$multiplier indicate the distance between the nearest M2 points alone y-axis
#       $sync_x; Used to syncronize the x-coordinate of M2 & M1 layer
#       $sync_y; Used to syncronize the y-coordinate of M2 & M1 layer
#       $sync_x_pad;    Used to syncronize the x-coordinate of PAD & M2 layer
#       $sync_y_pad;    Used to syncronize the y-coordinate of PAD & M2 layer
#       $x;             Reusable counting x-coordinate variable
#       $y;             Reusable counting y-coordinate variable
#       $x1;            (Reusable) x-Difference of current point to the 1st point of an edge of the calculating polygon
#       $y1;            (Reusable) y-Difference of current point to the 1st point of an edge of the calculating pol polygon
#       $x2;            (Reusable) x-Difference of current point to the 2nd point of an edge of the calculating pol polygon
#       $y2;            (Reusable) y-Difference of current point to the 2nd point of an edge of the calculating pol polygon
#       $min_max_right_m2_d;    $min_max_right_m2_d<0 indicates this point is inside one of the DRAIN side M2 convex polygon
#       $min_max_right_m2_s;    $min_max_right_m2_s<0 indicates this point is inside one of the SOURCE side M2 convex polygon
#       $max_right_n;   $max_right_n>0 indicates this point is outside the NEGATIVE M1 convex polygon
#       $max_right_p;   $max_right_n>0 indicates this point is outside the POSITIVE M1 convex polygon
#       $r_m1_count;    Count for M1 resistors
#       $mos_count;     Count for MOS transistors
#       $r_con_count;   Count for CONTACTs
#       $r_via_count;   Count for VIAs
```

```
#       $r_m2_count;      Count for M2 resistors
#       $x_next; (Reusable)x-coordinate of next point
#       $y_next; (Reusable)x-coordinate of next point
#       $pmos;            Name of the sub-circuit of PMOS for SPICE netlist
#       $nmos;            Name of the sub-circuit of NMOS for SPICE netlist
#       $y_initial;(Reusable)
#       $x_initial;(Reusable)
#       $width_of_two;
#       $y_head;
#       $y_tail;
#       $x_head;
#       $x_tail;

#   List of arrays
#
#       @n_m2_d[$j];      Number of corner points of the $jth M2 convex polygon at DRAIN side
#       @n_m2_s[$j];      Number of corner points of the $jth M2 convex polygon at SOURCE side
#       @n_m1_p[$j];      Number of corner points of the $jth POSITIVE M1 convex polygon
#       @n_m1_n[$j];      Number of corner points of the $jth NEGATIVE M1 convex polygon
#       @x_m2_d;          List x-coordinate of the corner points of the DRAIN side M2 convex polygon without index
#       @y_m2_d;          List y-coordinate of the corner points of the DRAIN side M2 convex polygon without index
#       @x_m2_s;          List x-coordinate of the corner points of the SOURCE side M2 convex polygon without index
#       @y_m2_s;          List y-coordinate of the corner points of the SOURCE side M2 convex polygon without index
#       @x_p;             List x-coordinate of the corner points of the POSITIVE M1 convex polygon without index
#       @y_p;             List y-coordinate of the corner points of the POSITIVE M1 convex polygon without index
#       @x_n;             List x-coordinate of the corner points of the NEGATIVE M1 convex polygon without index
#       @y_n;             List y-coordinate of the corner points of the NEGATIVE M1 convex polygon without index
#       @sort_x_m2_ls;    Numerically sorted (from larger to smaller) x-coordinate of the corner points of the M2 convex polygon
#       @sort_y_m2_ls;    Numerically sorted (from larger to smaller) y-coordinate of the corner points of the M2 convex polygon
#       @sort_x_m2_sl;    Numerically sorted (from smaller to larger) x-coordinate of the corner points of the M2 convex polygon
#       @sort_y_m2_sl;    Numerically sorted (from smaller to larger) y-coordinate of the corner points of the M2 convex polygon
#       @sort_x_p_ls;     Numerically sorted (from larger to smaller) x-coordinate of the corner points of the POSITIVE M1 convex polygon
#       @sort_y_p_ls;     Numerically sorted (from larger to smaller) y-coordinate of the corner points of the POSITIVE M1 convex polygon
#       @sort_x_p_sl;     Numerically sorted (from smaller to larger) x-coordinate of the corner points of the POSITIVE M1 convex polygon
#       @sort_y_p_sl;     Numerically sorted (from smaller to larger) y-coordinate of the corner points of the POSITIVE M1 convex polygon
#       @sort_x_n_ls;     Numerically sorted (from larger to smaller) x-coordinate of the corner points of the NEGATIVE M1 convex polygon
#       @sort_y_n_ls;     Numerically sorted (from larger to smaller) y-coordinate of the corner points of the NEGATIVE M1 convex polygon
#       @sort_x_n_sl;     Numerically sorted (from smaller to larger) x-coordinate of the corner points of the NEGATIVE M1 convex polygon
#       @sort_y_n_sl;     Numerically sorted (from smaller to larger) y-coordinate of the corner points of the NEGATIVE M1 convex polygon
#       @right_m2_d;      Elements in @right_m2_d indicate if one point is at the right side of the edges of the DRAIN side M2 convex polygon
#       @right_m2_s;      Elements in @right_m2_s indicate if one point is at the right side of the edges of the SOURCE side M2 convex polygon
#       @max_right_m2_d;        Minimum value of @max_right_m2_d<0 indicates the point is inside one of the DRAIN side M2 convex polygon
#       @max_right_m2_s;        Minimum value of @max_right_m2_s<0 indicates the point is inside one of the SOURCE side M2 convex polygon
#       @right_n;               Elements in @right_n indicate if one point is at the right side of the edges of the NEGATIVE M1 convex polygon
#       @right_p;               Elements in @right_p indicate if one point is at the right side of the edges of the POSITIVE M1 convex polygon
#       @sort_right_m2_d;       Numerically sorted (from larger to smaller) @right_m2_d
#       @sort_right_m2_s;       Numerically sorted (from larger to smaller) @right_m2_s
#       @sort_max_right_m2_d;   Numerically sorted (from larger to smaller) @max_right_m2_d
#       @sort_max_right_m2_s;   Numerically sorted (from larger to smaller) @max_right_m2_s
#       @sort_right_n;    Numercially sorted (from larger to smaller) @right_n
#       @sort_right_p;    Numercially sorted (from larger to smaller) @right_p

#   List of hash variables
#
#       %x_m2_d;          List x-coordinate of the corner points of the DRAIN side M2 convex polygon
#       %y_m2_d;          List y-coordinate of the corner points of the DRAIN side M2 convex polygon
#       %x_m2_s;          List x-coordinate of the corner points of the SOURCE side M2 convex polygon
#       %y_m2_s;          List y-coordinate of the corner points of the SOURCE side M2 convex polygon
#       %x_p;             List x-coordinate of the corner points of the POSITIVE M1 convex polygon
#       %y_p;             List y-coordinate of the corner points of the POSITIVE M1 convex polygon
#       %x_n;             List x-coordinate of the corner points of the NEGATIVE M1 convex polygon
#       %y_n;             List y-coordinate of the corner points of the NEGATIVE M1 convex polygon
#       %coordinate_m1;         $coordinate{$x,$y}=1 indicate the point ($x/$multiplier,$y/$multiplier) is a used point at M1 layer
#       %coordinate_m2_d;       $coordinate{$x,$y}=1 indicate the point ($x/$multiplier,$y/$multiplier) is a used point at DRAIN side M2 layer
#       %coordinate_m2_s;       $coordinate{$x,$y}=1 indicate the point ($x/$multiplier,$y/$multiplier) is a used point at SOURCE side M2 layer

#   List of used files
#       INPUT             Input data
#       OUTPUT            Output data to check input data
#       RESISTOR_M1       Resistor network of M1 layer
#       TRANSISTOR        Transistors (in sub-circuit type)
#       CON               CONTACTs
#       VIA               VIAs
#       RESISTOR_M2       Resistor network of M2 layer

use integer;
$multiplier=20;
no integer;

$mos_w_cal=$mos_width*$multiplier;
$mos_w_cal_half=$mos_w_cal/2;

use integer;
$mos_w_cal=$mos_w_cal+0;
$mos_w_cal_half=$mos_w_cal_half+0;
no integer;
```

```
########################################
#
#    Collect corner points of POSITIVE convex polygons of M2 layer (DRAIN and SOURCE)
#
########################################
use integer;
print "\nHow many POSITIVE convex polygons at DRAIN side in M2 layer? \n";
$dummy=<INPUT>;
$polygon_m2_d=<INPUT>;
chomp $polygon_m2_d;
if ($polygon_m2_d<1)
{
    die "Oops, NO polygon exists at DRAIN side!!! \n";
}
no integer;

for ($j=1; $j<=$polygon_m2_d; $j++)
{
    use integer;
    print "How many corner points does the No.$j M2 convex polygon have? \n";
    $n_m2_d[$j]=<INPUT>;
    chomp @n_m2_d;
    if ($n_m2_d[$j]<3)
    {
        die "Oops, there must be at least 3 points to form a polygon!!! \n";
    }
    no integer;

    print "Please input the coordinates of the corner points of \nNo.$j M2 convex polygon in a clockwise order. \n\n";

    #Collect coordinates of corner points of the polygon
    for ($i=1; $i<=$n_m2_d[$j]; $i++)
    {
        print "Please input x-coordinate of the No.$i point: \n";
        $xi=<INPUT>;
        chomp $xi;
        $xi=$xi*$multiplier;
        use integer;
        $xi=$xi+0;
        $x_m2_d{$j,$i}=$xi;
        no integer;

        print "Please input y-coordinate of the No.$i point: \n";
        $yi=<INPUT>;
        chomp $yi;
        $yi=$yi*$multiplier;
        use integer;
        $yi=$yi+0;
        $y_m2_d{$j,$i}=$yi;
        no integer;

        print "\nPOSITIVE M2 DRAIN P($j,$i):(",$x_m2_d{$j,$i}/$multiplier,",",$y_m2_d{$j,$i}/$multiplier,") \n\n";

        if ($i>2)
        {
            $right=($x_m2_d{$j,$i-2}-$x_m2_d{$j,$i})*($y_m2_d{$j,$i-1}-$y_m2_d{$j,$i})-($x_m2_d{$j,$i-1}-$x_m2_d{$j,$i})*($y_m2_d{$j,$i-2}-$y_m2_d{$j,$i});
            if ($right>1e-10)
            {
                die "ERROR: Not a convex polygon or Not in clockwise order\n";
            }
        }
    }
}

for ($j=1; $j<=$polygon_m2_d; $j++)
{
    for ($i=1; $i<=$n_m2_d[$j]; $i++)
    {
        print "POSITIVE M2 DRAIN P($j,$i):(",$x_m2_d{$j,$i}/$multiplier,",",$y_m2_d{$j,$i}/$multiplier,")\n";
        print OUTPUT "POSITIVE M2 DRAIN P($j,$i):(",$x_m2_d{$j,$i}/$multiplier,",",$y_m2_d{$j,$i}/$multiplier,")\n";
    }
}


use integer;
print "\nHow many POSITIVE convex polygons at SOURCE side in M2 layer? \n";
$dummy=<INPUT>;
$polygon_m2_s=<INPUT>;
chomp $polygon_m2_s;
if ($polygon_m2_s<1)
{
    die "Oops, NO polygon exists at SOURCE side!!! \n";
}
no integer;


for ($j=1; $j<=$polygon_m2_s; $j++)
```

```
{
    use integer;
    print "How many corner points does the No.$j M2 convex polygon have? \n";
    $n_m2_s[$j]=<INPUT>;
    chomp @n_m2_s;
    if ($n_m2_s[$j]<3)
    {
        die "Oops, there must be at least 3 points to form a polygon!!! \n";
    }
    no integer;

    print "Please input the coordinates of the corner points of \nNo.$j M2 convex polygon in a clockwise order. \n\n";

    #Collect coordinates of corner points of the polygon
    for ($i=1; $i<=$n_m2_s[$j]; $i++)
    {
        print "Please input x-coordinate of the No.$i point: \n";
        $xi=<INPUT>;
        chomp $xi;
        $xi=$xi*$multiplier;
        use integer;
        $xi=$xi+0;
        $x_m2_s{$j,$i}=$xi;
        no integer;

        print "Please input y-coordinate of the No.$i point: \n";
        $yi=<INPUT>;
        chomp $yi;
        $yi=$yi*$multiplier;
        use integer;
        $yi=$yi+0;
        $y_m2_s{$j,$i}=$yi;
        no integer;

        print "\nPOSITIVE M2 SOURCE P($j,$i):(",$x_m2_s{$j,$i}/$multiplier,",",$y_m2_s{$j,$i}/$multiplier,") \n\n";

        if ($i>2)
        {
            $right=($x_m2_s{$j,$i-2}-$x_m2_s{$j,$i})*($y_m2_s{$j,$i-1}-$y_m2_s{$j,$i})-($x_m2_s{$j,$i-1}-$x_m2_s{$j,$i})*($y_m2_s{$j,$i-2}-$y_m2_s{$j,$i});
            if ($right>1e-10)
            {
                die "ERROR: Not a convex polygon or Not in clockwise order\n";
            }
        }
    }
}

for ($j=1; $j<=$polygon_m2_s; $j++)
{
    for ($i=1; $i<=$n_m2_s[$j]; $i++)
    {
        print "POSITIVE M2 SOURCE P($j,$i):(",$x_m2_s{$j,$i}/$multiplier,",",$y_m2_s{$j,$i}/$multiplier,")\n";
        print OUTPUT"POSITIVE M2 SOURCE P($j,$i):(",$x_m2_s{$j,$i}/$multiplier,",",$y_m2_s{$j,$i}/$multiplier,")\n";
    }
}


########################################
#
#    Collect xy-coordinates of PADs and diameter of bond-wires
#
########################################
use integer;
print "\nHow many PADs does this MOS have? \n";
$dummy=<INPUT>;
$pads=<INPUT>;
chomp $pads;
if ($pads<1)
{
    die "Oops, NO PAD exists!!! \n";
}
no integer;


for ($i=1; $i<=$pads; $i++)
{
    print "Please input x-coordinate of the No.$i PAD: \n";
    $xi=<INPUT>;
    chomp $xi;
    $xi=$xi*$multiplier;
    use integer;
    $xi=$xi+0;
    $x_pad{$i}=$xi;
    no integer;

    print "Please input y-coordinate of the No.$i PAD: \n";
    $yi=<INPUT>;
```

```
    chomp $yi;
    $yi=$yi*$multiplier;
    use integer;
    $yi=$yi+0;
    $y_pad{$i}=$yi;
    no integer;

    print "\nPAD($i):(",$x_pad{$i}/$multiplier,",",$y_pad{$i}/$multiplier,") \n\n";
}
for ($i=1; $i<=$pads; $i++)
{
    print "PAD($i):(",$x_pad{$i}/$multiplier,",",$y_pad{$i}/$multiplier,")\n";
    print OUTPUT "PAD($i):(",$x_pad{$i}/$multiplier,",",$y_pad{$i}/$multiplier,")\n";
}

#### Diameter of Bond-wires

print "\nPlease input the diameter of bond-wires? (in micro-meter) \n";
$dummy=<INPUT>;
$bond_diameter=<INPUT>;
chomp $bond_diameter;
$bond_diameter=$bond_diameter*$multiplier;
use integer;
$bond_diameter=$bond_diameter+0;
no integer;

print "Diameter of Bond-wires: ",$bond_diameter/$multiplier,"um \n";
print OUTPUT "Diameter of Bond-wires: ",$bond_diameter/$multiplier,"um \n";


########################################
#
#    Collect corner points of POSITIVE convex polygons of M1 layer
#
########################################
use integer;
print "\nHow many POSITIVE convex polygons in M1 layer? \n";
$dummy=<INPUT>;
$polygon_m1_p=<INPUT>;
chomp $polygon_m1_p;
if ($polygon_m1_p<1)
{
    die "Oops, NO polygon exists at M1 layer!!! \n";
}
no integer;


for ($j=1; $j<=$polygon_m1_p; $j++)
{
    use integer;
    print "How many corner points does the No.$j M1 convex polygon have? \n";
    $n_m1_p[$j]=<INPUT>;
    chomp @n_m1_p;
    if ($n_m1_p[$j]<3)
    {
        die "Oops, there must be at least 3 points to form a polygon!!! \n";
    }
    no integer;

    print "Please input the coordinates of the corner points of \nNo.$j M1 convex polygon in a clockwise order. \n\n";

    #Collect coordinates of corner points of the polygon
    for ($i=1; $i<=$n_m1_p[$j]; $i++)
    {
        print "Please input x-coordinate of the No.$i point: \n";
        $xi=<INPUT>;
        chomp $xi;
        $xi=$xi*$multiplier;
        use integer;
        $xi=$xi+0;
        $x_p{$j,$i}=$xi;
        no integer;

        print "Please input y-coordinate of the No.$i point: \n";
        $yi=<INPUT>;
        chomp $yi;
        $yi=$yi*$multiplier;
        use integer;
        $yi=$yi+0;
        $y_p{$j,$i}=$yi;
        no integer;

        print "\nPOSITIVE M1 P($j,$i):(",$x_p{$j,$i}/$multiplier,",",$y_p{$j,$i}/$multiplier,") \n\n";

        if ($i>2)
        {
            $right=($x_p{$j,$i-2}-$x_p{$j,$i})*($y_p{$j,$i-1}-$y_p{$j,$i})-($x_p{$j,$i-1}-$x_p{$j,$i})*($y_p{$j,$i-2}-$y_p{$j,$i});
```

```
            if ($right>1e-10)
            {
                die "ERROR: Not a convex polygon or Not in clockwise order\n";
            }
        }
    }
}

for ($j=1; $j<=$polygon_m1_p; $j++)
{
    for ($i=1; $i<=$n_m1_p[$j]; $i++)
    {
        print "POSITIVE M1 P($j,$i):(",$x_p{$j,$i}/$multiplier,",",$y_p{$j,$i}/$multiplier,")\n";
        print OUTPUT "POSITIVE M1 P($j,$i):(",$x_p{$j,$i}/$multiplier,",",$y_p{$j,$i}/$multiplier,")\n";
    }
}


########################################
#
#    Collect corner points of NEGATIVE convex polygons of M1 layer
#
########################################
use integer;
print "\nHow many NEGATIVE convex polygons in M1 layer? \n";
$dummy=<INPUT>;
$polygon_m1_n=<INPUT>;
chomp $polygon_m1_n;
no integer;


for ($j=1; $j<=$polygon_m1_n; $j++)
{
    use integer;
    print "How many corner points does the No.$j M1 convex polygon have? \n";
    $n_m1_n[$j]=<INPUT>;
    chomp @n_m1_n;
    if ($n_m1_n[$j]<3)
    {
        die "Oops, there must be at least 3 points to form a polygon!!! \n";
    }
    no integer;

    print "Please input the coordinates of the corner points of \nNo.$j M1 convex polygon in a clockwise order. \n\n";

    #Collect coordinates of corner points of the polygon
    for ($i=1; $i<=$n_m1_n[$j]; $i++)
    {
        print "Please input x-coordinate of the No.$i point: \n";
        $xi=<INPUT>;
        chomp $xi;
        $xi=$xi*$multiplier;
        use integer;
        $xi=$xi+0;
        $x_n{$j,$i}=$xi;
        no integer;

        print "Please input y-coordinate of the No.$i point: \n";
        $yi=<INPUT>;
        chomp $yi;
        $yi=$yi*$multiplier;
        use integer;
        $yi=$yi+0;
        $y_n{$j,$i}=$yi;
        no integer;

        print "\nNEGATIVE M1 P($j,$i):(",$x_n{$j,$i}/$multiplier,",",$y_n{$j,$i}/$multiplier,") \n\n";

        if ($i>2)
        {
            $right=($x_n{$j,$i-2}-$x_n{$j,$i})*($y_n{$j,$i-1}-$y_n{$j,$i})-($x_n{$j,$i-1}-$x_n{$j,$i})*($y_n{$j,$i-2}-$y_n{$j,$i});
            if ($right>1e-10)
            {
                die "ERROR: Not a convex polygon or Not in clockwise order\n";
            }
        }
    }
}

for ($j=1; $j<=$polygon_m1_n; $j++)
{
    for ($i=1; $i<=$n_m1_n[$j]; $i++)
    {
        print "NEGATIVE M1 P($j,$i):(",$x_n{$j,$i}/$multiplier,",",$y_n{$j,$i}/$multiplier,")\n";
        print OUTPUT "NEGATIVE M1 P($j,$i):(",$x_n{$j,$i}/$multiplier,",",$y_n{$j,$i}/$multiplier,")\n";
    }
}
```

```
########################################
#
#    Collect direction, width and gap of M1 layer
#
########################################
use integer;
print "\nPolygate is parallel or perpendicular to the x-axis?\n (parallel=0, perpendicular=1)\n";
$dummy=<INPUT>;
$perpendicular=<INPUT>;
chomp $perpendicular;
no integer;

print "\nHow wide does each M1 line?\n";
$dummy=<INPUT>;
$width_m1=<INPUT>;
chomp $width_m1;
$width_m1=$width_m1*$multiplier;
use integer;
$width_m1=$width_m1+0;
no integer;

print "\nHow wide does the gap between M1 lines?\n";
$dummy=<INPUT>;
$gap_m1=<INPUT>;
chomp $gap_m1;
$gap_m1=$gap_m1*$multiplier;
use integer;
$gap_m1=$gap_m1+0;
no integer;

print "\nPlease tell me the mos type? (PMOS=0, NMOS=1)\n";
$dummy=<INPUT>;
$mos_type=<INPUT>;
chomp $mos_type;

if ($perpendicular==0)
{
    $step_x=$M2_step*$multiplier;
    $step_y=$width_m1+$gap_m1;
}
elsif ($perpendicular==1)
{
    $step_x=$width_m1+$gap_m1;
    $step_y=$M2_step*$multiplier;
}
use integer;
$step_x=$step_x+0;
$step_y=$step_y+0;
no integer;

#$R_M1=$R_M1*$mos_width/$width_m1*$multiplier;

print "perpendicular=$perpendicular\nwidth_m1=$width_m1\ngap_m1=$gap_m1\nmos_type=$mos_type\nstep_x=$step_x\nstep_y=$step_y\n";
print OUTPUT "perpendicular=$perpendicular\nwidth_m1=$width_m1\ngap_m1=$gap_m1\nmos_type=$mos_type\nstep_x=$step_x\nstep_y=$step_y\n";


########################################
#
#    Calculate (MAX & min) x-coordinate and y-coordinate of the POSITIVE convex polygon of M2 layer (DRAIN and SOURCE)
#
########################################
use integer;

@x_m2_d=values %x_m2_d;
@y_m2_d=values %y_m2_d;
@x_m2_s=values %x_m2_s;
@y_m2_s=values %y_m2_s;

@sort_x_m2_ls=sort large_to_small @x_m2_d,@x_m2_s;
@sort_y_m2_ls=sort large_to_small @y_m2_d,@y_m2_s;
@sort_x_m2_sl=sort small_to_large @x_m2_d,@x_m2_s;
@sort_y_m2_sl=sort small_to_large @y_m2_d,@y_m2_s;

$max_x_m2=$sort_x_m2_ls[0]+0.01;
$max_y_m2=$sort_y_m2_ls[0]+0.01;
$min_x_m2=$sort_x_m2_sl[0];
$min_y_m2=$sort_y_m2_sl[0];

print "\nmax_x_m2=$max_x_m2\nmax_y_m2=$max_y_m2\nmin_x_m2=$min_x_m2\nmin_y_m2=$min_y_m2\n";
print OUTPUT "\nmax_x_m2=$max_x_m2\nmax_y_m2=$max_y_m2\nmin_x_m2=$min_x_m2\nmin_y_m2=$min_y_m2\n";

no integer;


########################################
```

```
#
#    Calculate (MAX & min) x-coordinate and y-coordinate of the POSITIVE convex polygon of M1 layer
#
#######################################
use integer;

@x_p=values %x_p;
@y_p=values %y_p;

@sort_x_p_ls=sort large_to_small @x_p;
@sort_y_p_ls=sort large_to_small @y_p;
@sort_x_p_sl=sort small_to_large @x_p;
@sort_y_p_sl=sort small_to_large @y_p;

$max_x_p=$sort_x_p_ls[0]+0.01;
$max_y_p=$sort_y_p_ls[0]+0.01;
$min_x_p=$sort_x_p_sl[0];
$min_y_p=$sort_y_p_sl[0];

print "\nmax_x_p=$max_x_p\nmax_y_p=$max_y_p\nmin_x_p=$min_x_p\nmin_y_p=$min_y_p\n";
print OUTPUT "\nmax_x_p=$max_x_p\nmax_y_p=$max_y_p\nmin_x_p=$min_x_p\nmin_y_p=$min_y_p\n";

no integer;


#######################################
#
#    Calculate (MAX & min) x-coordinate and y-coordinate of the NEGATIVE convex polygon of M1 layer
#
#######################################
if ($polygon_m1_n!=0)
{
    use integer;

    @x_n=values %x_n;
    @y_n=values %y_n;

    @sort_x_n_ls=sort large_to_small @x_n;
    @sort_y_n_ls=sort large_to_small @y_n;
    @sort_x_n_sl=sort small_to_large @x_n;
    @sort_y_n_sl=sort small_to_large @y_n;

    $max_x_n=$sort_x_n_ls[0]+0.01;
    $max_y_n=$sort_y_n_ls[0]+0.01;
    $min_x_n=$sort_x_n_sl[0];
    $min_y_n=$sort_y_n_sl[0];

    no integer;
}
else
{
    $max_x_n=0;
    $max_y_n=0;
    $min_x_n=0;
    $min_y_n=0;
}

print "\nmax_x_n=$max_x_n\nmax_y_n=$max_y_n\nmin_x_n=$min_x_n\nmin_y_n=$min_y_n\n";
print OUTPUT "\nmax_x_n=$max_x_n\nmax_y_n=$max_y_n\nmin_x_n=$min_x_n\nmin_y_n=$min_y_n\n";

close (INPUT) || die "$!";
close (OUTPUT) || die "$!";


#######################################
#
#    Calculate if the point is inside the convex polygon of M2 layer (DRAIN and SOURCE)
#
#######################################
use integer;

unlink ("coordinate_m2_d");
unlink ("coordinate_m2_d.dir");
unlink ("coordinate_m2_d.pag");
unlink ("coordinate_m2_s");
unlink ("coordinate_m2_s.dir");
unlink ("coordinate_m2_s.pag");
dbmopen (%coordinate_m2_d,"coordinate_m2_d",0644) || die "$!";
dbmopen (%coordinate_m2_s,"coordinate_m2_s",0644) || die "$!";
@right_m2_d=("0");
@right_m2_s=("0");
@max_right_m2_d=("1");
@max_right_m2_s=("1");

no integer;
if ($perpendicular==0)
{
```

```
    $sync_x=$step_x-(($min_x_m2-($min_x_p+$mos_w_cal_half))%$step_x);
    $sync_y=$step_y-(($min_y_m2-($min_y_p+$width_m1/2))%$step_y);
}
elsif ($perpendicular==1)
{
    $sync_x=$step_x-(($min_x_m2-($min_x_p+$width_m1/2))%$step_x);
    $sync_y=$step_y-(($min_y_m2-($min_y_p+$mos_w_cal_half))%$step_y);
}
use integer;

for ($x=$min_x_m2+$sync_x;$x<$max_x_m2;$x=$x+$step_x)
{

    if ($x%1==0)
    {
        no integer;
        print "calculating M2 x = ",$x/$multiplier,"um\n";
        use integer;
    }

    for ($y=$min_y_m2+$sync_y;$y<$max_y_m2;$y=$y+$step_y)
    {
        for ($k=1;$k<=$polygon_m2_d;$k++)
        {
            for ($l=1;$l<=$n_m2_d[$k];$l++)
            {
                if ($l!=$n_m2_d[$k])
                {
                    $x1=$x_m2_d{$k,$l}-$x;
                    $y1=$y_m2_d{$k,$l}-$y;
                    $x2=$x_m2_d{$k,$l+1}-$x;
                    $y2=$y_m2_d{$k,$l+1}-$y;
                    $right_m2_d[$l]=($x1*$y2)-($x2*$y1);
                }
                else
                {
                    $x1=$x_m2_d{$k,$l}-$x;
                    $y1=$y_m2_d{$k,$l}-$y;
                    $x2=$x_m2_d{$k,1}-$x;
                    $y2=$y_m2_d{$k,1}-$y;
                    $right_m2_d[$l]=($x1*$y2)-($x2*$y1);
                }
            }
            @sort_right_m2_d=sort large_to_small @right_m2_d;
            @right_m2_d=("0");                          #clear values stored in @right_m2_d
            $max_right_m2_d[$k]=$sort_right_m2_d[0];
        }
        @sort_max_right_m2_d=sort small_to_large @max_right_m2_d;
        @max_right_m2_d=("1");                                  #clear values stored in @max_right_m2_d
        $min_max_right_m2_d=$sort_max_right_m2_d[0];

        for ($k=1;$k<=$polygon_m2_s;$k++)
        {
            for ($l=1;$l<=$n_m2_s[$k];$l++)
            {
                if ($l!=$n_m2_s[$k])
                {
                    $x1=$x_m2_s{$k,$l}-$x;
                    $y1=$y_m2_s{$k,$l}-$y;
                    $x2=$x_m2_s{$k,$l+1}-$x;
                    $y2=$y_m2_s{$k,$l+1}-$y;
                    $right_m2_s[$l]=($x1*$y2)-($x2*$y1);
                }
                else
                {
                    $x1=$x_m2_s{$k,$l}-$x;
                    $y1=$y_m2_s{$k,$l}-$y;
                    $x2=$x_m2_s{$k,1}-$x;
                    $y2=$y_m2_s{$k,1}-$y;
                    $right_m2_s[$l]=($x1*$y2)-($x2*$y1);
                }
            }
            @sort_right_m2_s=sort large_to_small @right_m2_s;
            @right_m2_s=("0");                                  #clear values stored in @right_m2_s
            $max_right_m2_s[$k]=$sort_right_m2_s[0];
        }
        @sort_max_right_m2_s=sort small_to_large @max_right_m2_s;
        @max_right_m2_s=("1");                                          #clear values stored in @max_right_m2_s
        $min_max_right_m2_s=$sort_max_right_m2_s[0];

        if ($min_max_right_m2_d<=0 and $min_max_right_m2_s<=0)
        {
            die "Oops, we encountered a point falls inside both SOURCE and DRAIN side!!! \n";
        }
        elsif ($min_max_right_m2_d<=1e-10)
        {
            $coordinate_m2_d{$x,$y}=1;
```

```
        }
        elsif ($min_max_right_m2_s<=1e-10)
        {
            $coordinate_m2_s{$x,$y}=1;
        }
    }
}

no integer;


########################################
#
#    Calculate if the point is inside the POSITIVE but NOT the NEGATIVE convex polygon of M1 layer
#
########################################
use integer;

unlink ("coordinate_m1");
unlink ("coordinate_m1.dir");
unlink ("coordinate_m1.pag");
dbmopen (%coordinate_m1,"coordinate_m1",0644) || die "$!";
@right_n=("0");
@right_p=("0");

if ($perpendicular==0)
{
    for ($y=$min_y_p+$width_m1/2;$y<$max_y_p;$y=$y+$width_m1+$gap_m1)
    {

        if ($y%1==0)
        {
            no integer;
            print "calculating M1 y = ",$y/$multiplier,"um, perpendicular=0\n";
            use integer;
        }

        for ($x=$min_x_p+$mos_w_cal_half;$x<$max_x_p;$x=$x+$mos_w_cal)
        {
            $i=1;
            if ($x<=$max_x_n and $x>=$min_x_n and $y<=$max_y_n and $y>=$min_y_n)
            {
                for($i=1;$i<=$polygon_m1_n;$i++)
                {
                    for ($j=1;$j<=$n_m1_n[$i];$j++)
                    {
                        if ($j!=$n_m1_n[$i])
                        {
                            $x1=$x_n{$i,$j}-$x;
                            $y1=$y_n{$i,$j}-$y;
                            $x2=$x_n{$i,$j+1}-$x;
                            $y2=$y_n{$i,$j+1}-$y;
                            $right_n[$j]=($x1*$y2)-($x2*$y1);
                        }
                        else
                        {
                            $x1=$x_n{$i,$j}-$x;
                            $y1=$y_n{$i,$j}-$y;
                            $x2=$x_n{$i,1}-$x;
                            $y2=$y_n{$i,1}-$y;
                            $right_n[$j]=($x1*$y2)-($x2*$y1);
                        }
                    }
                    @sort_right_n=sort large_to_small @right_n;
                    @right_n=("0");                                    #clear values stored in @right_n
                    $max_right_n=$sort_right_n[0];
                    if ($max_right_n<=1e-10)
                    {
                        $i=$polygon_m1_n+100;
                    }
                }
            }

            if ($i<$polygon_m1_n+10)
            {
                for ($k=1;$k<=$polygon_m1_p;$k++)
                {
                    for ($l=1;$l<=$n_m1_p[$k];$l++)
                    {
                        if ($l!=$n_m1_p[$k])
                        {
                            $x1=$x_p{$k,$l}-$x;
                            $y1=$y_p{$k,$l}-$y;
                            $x2=$x_p{$k,$l+1}-$x;
                            $y2=$y_p{$k,$l+1}-$y;
                            $right_p[$l]=($x1*$y2)-($x2*$y1);
                        }
```

```
                else
                {
                    $x1=$x_p{$k,$l}-$x;
                    $y1=$y_p{$k,$l}-$y;
                    $x2=$x_p{$k,1}-$x;
                    $y2=$y_p{$k,1}-$y;
                    $right_p[$l]=($x1*$y2)-($x2*$y1);
                }
            }
            @sort_right_p=sort large_to_small @right_p;
            @right_p=("0");                                    #clear values stored in @right_p
            $max_right_p=$sort_right_p[0];
            if ($max_right_p<=1e-10)
            {
                $coordinate_m1{$x,$y}=1;
            }
        }
    }
  }
}


elsif ($perpendicular==1)
{
  for ($x=$min_x_p+$width_m1/2;$x<$max_x_p;$x=$x+$width_m1+$gap_m1)
  {

    if ($x%1==0)
    {
        no integer;
        print "calculating M1 x = ",$x/$multiplier,"um, perpendicular=1\n";
        use integer;
    }

    for ($y=$min_y_p+$mos_w_cal_half;$y<$max_y_p;$y=$y+$mos_w_cal)
    {
        $i=1;
        if ($x<=$max_x_n and $x>=$min_x_n and $y<=$max_y_n and $y>=$min_y_n)
        {
            for($i=1;$i<=$polygon_m1_n;$i++)
            {
                for ($j=1;$j<=$n_m1_n[$i];$j++)
                {
                    if ($j!=$n_m1_n[$i])
                    {
                        $x1=$x_n{$i,$j}-$x;
                        $y1=$y_n{$i,$j}-$y;
                        $x2=$x_n{$i,$j+1}-$x;
                        $y2=$y_n{$i,$j+1}-$y;
                        $right_n[$j]=($x1*$y2)-($x2*$y1);
                    }
                    else
                    {
                        $x1=$x_n{$i,$j}-$x;
                        $y1=$y_n{$i,$j}-$y;
                        $x2=$x_n{$i,1}-$x;
                        $y2=$y_n{$i,1}-$y;
                        $right_n[$j]=($x1*$y2)-($x2*$y1);
                    }
                }
                @sort_right_n=sort large_to_small @right_n;
                @right_n=("0");                                    #clear values stored in @right_n
                $max_right_n=$sort_right_n[0];
                if ($max_right_n<=1e-10)
                {
                    $i=$polygon_m1_n+100;
                }
            }
        }

        if ($i<$polygon_m1_n+10)
        {
            for ($k=1;$k<=$polygon_m1_p;$k++)
            {
                for ($l=1;$l<=$n_m1_p[$k];$l++)
                {
                    if ($l!=$n_m1_p[$k])
                    {
                        $x1=$x_p{$k,$l}-$x;
                        $y1=$y_p{$k,$l}-$y;
                        $x2=$x_p{$k,$l+1}-$x;
                        $y2=$y_p{$k,$l+1}-$y;
                        $right_p[$l]=($x1*$y2)-($x2*$y1);
                    }
                    else
                    {
```

```
                    $x1=$x_p{$k,$l}-$x;
                    $y1=$y_p{$k,$l}-$y;
                    $x2=$x_p{$k,1}-$x;
                    $y2=$y_p{$k,1}-$y;
                    $right_p[$l]=($x1*$y2)-($x2*$y1);
                }
            }
            @sort_right_p=sort large_to_small @right_p;
            @right_p=("0");                                    #clear values stored in @right_p
            $max_right_p=$sort_right_p[0];
            if ($max_right_p<=1e-10)
            {
                $coordinate_m1{$x,$y}=1;
            }
        }
    }
  }
}

no integer;


########################################
#
#    Print the calculated M1 results into .sp file
#
########################################
use integer;
$r_m1_count=0;
open (RESISTOR_M1,">./res_m1.net") || die "$!";

if ($perpendicular==0)
{
   for ($y=$min_y_p+$width_m1/2;$y<$max_y_p;$y=$y+$width_m1+$gap_m1)
   {

      if ($y%1==0)
      {
         no integer;
         print "printing M1 y = ",$y/$multiplier,"um, perpendicular=0\n";
         use integer;
      }

      for ($x=$min_x_p+$mos_w_cal_half;$x<$max_x_p;$x=$x+$mos_w_cal)
      {
         $x_next=$x+$mos_w_cal;
         if ($coordinate_m1{$x,$y} and $coordinate_m1{$x_next,$y})
         {
            print RESISTOR_M1 "R_"."$x"."_"."$y"."_"."$x_next"."_"."$y"."_M1          M1_$x"."_"."$y      M1_$x_next"."_"."$y          R_M1\n";
            $r_m1_count++;
         }
      }
   }
}


elsif ($perpendicular==1)
{
   for ($x=$min_x_p+$width_m1/2;$x<$max_x_p;$x=$x+$width_m1+$gap_m1)
   {

      if ($x%1==0)
      {
         no integer;
         print "printing M1 x = ",$x/$multiplier,"um, perpendicular=1\n";
         use integer;
      }

      for ($y=$min_y_p+$mos_w_cal_half;$y<$max_y_p;$y=$y+$mos_w_cal)
      {
         $y_next=$y+$mos_w_cal;
         if ($coordinate_m1{$x,$y} and $coordinate_m1{$x,$y_next})
         {
            print RESISTOR_M1 "R_"."$x"."_"."$y"."_"."$x"."_"."$y_next"."_M1          M1_$x"."_"."$y      M1_$x"."_"."$y_next          R_M1\n";
            $r_m1_count++;
         }
      }
   }
}

print RESISTOR_M1 "*M1 Resistor Count: $r_m1_count\n";
print "\nM1 Resistor Count: $r_m1_count\n\n";

close (RESISTOR_M1) || die "$!";

no integer;
```

```
########################################
#
#    Print the calculated MOS results into .sp file
#
########################################
use integer;
$mos_count=0;
open (TRANSISTOR,">./mos.net") || die "$!";

if ($perpendicular==0)
{
    if ($mos_type==0)
    {
        for ($y=$min_y_p+$width_m1+$gap_m1/2;$y<$max_y_p;$y=$y+$width_m1+$gap_m1)
        {

            if ($y%1==0)
            {
                no integer;
                print "printing PMOS y = ",$y/$multiplier,"um, perpendicular=0\n";
                use integer;
            }

            $y_initial=$y-$min_y_p-$width_m1-$gap_m1/2;
            $width_of_two=($width_m1+$gap_m1)*2;
            $y_head=$y+$width_m1/2+$gap_m1/2;
            $y_tail=$y-$width_m1/2-$gap_m1/2;

            if ($y_initial%$width_of_two==0)
            {
                for ($x=$min_x_p+$mos_w_cal_half;$x<$max_x_p;$x=$x+$mos_w_cal)
                {
                    $x_head=$x-$mos_w_cal_half;
                    $x_tail=$x+$mos_w_cal_half;
                    if ($coordinate_m1{$x,$y_head} and $coordinate_m1{$x,$y_tail})
                    {
                        print TRANSISTOR "X_"."$x"."_"."$y"."  D_$x"."_"."$y_head          P1        D_$x"."_"."$y_tail  vccp      $pmos\n";
                        $mos_count++;
                    }
                }
            }
            else
            {
                for ($x=$min_x_p+$mos_w_cal_half;$x<$max_x_p;$x=$x+$mos_w_cal)
                {
                    $x_head=$x-$mos_w_cal_half;
                    $x_tail=$x+$mos_w_cal_half;
                    if ($coordinate_m1{$x,$y_head} and $coordinate_m1{$x,$y_tail})
                    {
                        print TRANSISTOR "X_"."$x"."_"."$y"."  D_$x"."_"."$y_tail  P1        D_$x"."_"."$y_head          vccp      $pmos\n";
                        $mos_count++;
                    }
                }
            }
        }
    }


    elsif ($mos_type==1)
    {
        for ($y=$min_y_p+$width_m1+$gap_m1/2;$y<$max_y_p;$y=$y+$width_m1+$gap_m1)
        {

            if ($y%1==0)
            {
                no integer;
                print "printing NMOS y = ",$y/$multiplier,"um, perpendicular=0\n";
                use integer;
            }

            $y_initial=$y-$min_y_p-$width_m1-$gap_m1/2;
            $width_of_two=($width_m1+$gap_m1)*2;
            $y_head=$y+$width_m1/2+$gap_m1/2;
            $y_tail=$y-$width_m1/2-$gap_m1/2;

            if ($y_initial%$width_of_two==0)
            {
                for ($x=$min_x_p+$mos_w_cal_half;$x<$max_x_p;$x=$x+$mos_w_cal)
                {
                    $x_head=$x-$mos_w_cal_half;
                    $x_tail=$x+$mos_w_cal_half;
                    if ($coordinate_m1{$x,$y_head} and $coordinate_m1{$x,$y_tail})
                    {
                        print TRANSISTOR "X_"."$x"."_"."$y"."  D_$x"."_"."$y_head          P1        D_$x"."_"."$y_tail  vssp      $nmos\n";
                        $mos_count++;
```

```
                }
            }
        }
        else
        {
            for ($x=$min_x_p+$mos_w_cal_half;$x<$max_x_p;$x=$x+$mos_w_cal)
            {
                $x_head=$x-$mos_w_cal_half;
                $x_tail=$x+$mos_w_cal_half;
                if ($coordinate_m1{$x,$y_head} and $coordinate_m1{$x,$y_tail})
                {
                    print TRANSISTOR "X_"."$x"."_"."$y"."  D_$x"."_"."$y_tail  P1          D_$x"."_"."$y_head            vssp       $nmos\n";
                    $mos_count++;
                }
            }
        }
    }
  }
}


elsif ($perpendicular==1)
{
   if ($mos_type==0)
   {
      for ($x=$min_x_p+$width_m1+$gap_m1/2;$x<$max_x_p;$x=$x+$width_m1+$gap_m1)
      {

         if ($x%1==0)
         {
            no integer;
            print "printing PMOS x = ",$x/$multiplier,"um, perpendicular=1\n";
            use integer;
         }

         $x_initial=$x-$min_x_p-$width_m1-$gap_m1/2;
         $width_of_two=($width_m1+$gap_m1)*2;
         $x_head=$x+$width_m1/2+$gap_m1/2;
         $x_tail=$x-$width_m1/2-$gap_m1/2;

         if ($x_initial%$width_of_two==0)
         {
            for ($y=$min_y_p+$mos_w_cal_half;$y<$max_y_p;$y=$y+$mos_w_cal)
            {
               $y_head=$y-$mos_w_cal_half;
               $y_tail=$y+$mos_w_cal_half;
               if ($coordinate_m1{$x_head,$y} and $coordinate_m1{$x_tail,$y})
               {
                  print TRANSISTOR "X_"."$x"."_"."$y"."  D_$x_head"."_"."$y           P1         D_$x_tail"."_"."$y  vccp       $pmos\n";
                  $mos_count++;
               }
            }
         }
         else
         {
            for ($y=$min_y_p+$mos_w_cal_half;$y<$max_y_p;$y=$y+$mos_w_cal)
            {
               $y_head=$y-$mos_w_cal_half;
               $y_tail=$y+$mos_w_cal_half;
               if ($coordinate_m1{$x_head,$y} and $coordinate_m1{$x_tail,$y})
               {
                  print TRANSISTOR "X_"."$x"."_"."$y"."  D_$x_tail"."_"."$y  P1          D_$x_head"."_"."$y            vccp       $pmos\n";
                  $mos_count++;
               }
            }
         }
      }
   }


   elsif ($mos_type==1)
   {
      for ($x=$min_x_p+$width_m1+$gap_m1/2;$x<$max_x_p;$x=$x+$width_m1+$gap_m1)
      {

         if ($x%1==0)
         {
            no integer;
            print "printing NMOS x = ",$x/$multiplier,"um, perpendicular=1\n";
            use integer;
         }

         $x_initial=$x-$min_x_p-$width_m1-$gap_m1/2;
         $width_of_two=($width_m1+$gap_m1)*2;
         $x_head=$x+$width_m1/2+$gap_m1/2;
         $x_tail=$x-$width_m1/2-$gap_m1/2;
```

```
            if ($x_initial%$width_of_two==0)
            {
                for ($y=$min_y_p+$mos_w_cal_half;$y<$max_y_p;$y=$y+$mos_w_cal)
                {
                    $y_head=$y-$mos_w_cal_half;
                    $y_tail=$y+$mos_w_cal_half;
                    if ($coordinate_m1{$x_head,$y} and $coordinate_m1{$x_tail,$y})
                    {
                        print TRANSISTOR "X_"."$x"."_"."$y"."  D_$x_head"."_"."$y            P1          D_$x_tail"."_"."$y  vssp       $nmos\n";
                        $mos_count++;
                    }
                }
            }
            else
            {
                for ($y=$min_y_p+$mos_w_cal_half;$y<$max_y_p;$y=$y+$mos_w_cal)
                {
                    $y_head=$y-$mos_w_cal_half;
                    $y_tail=$y+$mos_w_cal_half;
                    if ($coordinate_m1{$x_head,$y} and $coordinate_m1{$x_tail,$y})
                    {
                        print TRANSISTOR "X_"."$x"."_"."$y"."  D_$x_tail"."_"."$y  P1          D_$x_head"."_"."$y            vssp       $nmos\n";
                        $mos_count++;
                    }
                }
            }
        }
    }
}
no integer;

print TRANSISTOR "*Transistor Count: $mos_count\n";
print TRANSISTOR "*Transistor Width: ",$mos_count*$mos_width,"\n";
print "\nTransistor Count: $mos_count\n\n";
print "\nTransistor Width: ",$mos_count*$mos_width,"\n\n";

###poly resisitor contour

close (TRANSISTOR) || die "$!";


########################################
#
#    Print the calculated CONTACT results into .sp file
#
########################################
use integer;
$r_con_count=0;
open (CON,">./con.net") || die "$!";

if ($perpendicular==0)
{
    for ($y=$min_y_p+$width_m1/2;$y<$max_y_p;$y=$y+$width_m1+$gap_m1)
    {

        if ($y%1==0)
        {
            no integer;
            print "printing R_CON y = ",$y/$multiplier,"um, perpendicular=0\n";
            use integer;
        }

        for ($x=$min_x_p+$mos_w_cal_half;$x<$max_x_p;$x=$x+$mos_w_cal)
        {
            if ($coordinate_m1{$x,$y})
            {
                print CON "R_"."$x"."_"."$y"."_con   D_$x"."_"."$y        M1_$x"."_"."$y      R_CON\n";
                $r_con_count++;
            }
        }
    }
}


elsif ($perpendicular==1)
{
    for ($x=$min_x_p+$width_m1/2;$x<$max_x_p;$x=$x+$width_m1+$gap_m1)
    {

        if ($x%1==0)
        {
            no integer;
            print "printing R_CON x = ",$x/$multiplier,"um, perpendicular=1\n";
            use integer;
        }

        for ($y=$min_y_p+$mos_w_cal_half;$y<$max_y_p;$y=$y+$mos_w_cal)
```

```
        {
            if ($coordinate_m1{$x,$y})
            {
                print CON "R_"."$x"."_"."$y"."_con   D_$x"."_"."$y        M1_$x"."_"."$y      R_CON\n";
                $r_con_count++;
            }
        }
    }
}

print CON "*CON Resistor Count: $r_con_count\n";
print "\nCON Resistor Count: $r_con_count\n\n";

close (CON) || die "$!";


########################################
#
#    Print the calculated VIA results into .sp file
#
########################################
use integer;
$r_via_count=0;
open (VIA,">./via.net") || die "$!";

if ($perpendicular==0)
{
    for ($y=$min_y_p+$width_m1/2;$y<$max_y_p;$y=$y+$width_m1+$gap_m1)
    {

        if ($y%1==0)
        {
            no integer;
            print "printing R_VIA y = ",$y/$multiplier,"um, perpendicular=0\n";
            use integer;
        }

        $y_initial=$y-$min_y_p-$width_m1/2;
        $width_of_two=($width_m1+$gap_m1)*2;

        if ($y_initial%$width_of_two==0)
        {
            for ($x=$min_x_p+$mos_w_cal_half;$x<$max_x_p;$x=$x+$mos_w_cal)
            {
                if ($coordinate_m1{$x,$y} and $coordinate_m2_s{$x,$y})
                {
                    print VIA "R_"."$x"."_"."$y"."_via_s            M1_$x"."_"."$y      M2_$x"."_"."$y      R_VIA\n";
                    $r_via_count++;
                }
            }
        }
        else
        {
            for ($x=$min_x_p+$mos_w_cal_half;$x<$max_x_p;$x=$x+$mos_w_cal)
            {
                if ($coordinate_m1{$x,$y} and $coordinate_m2_d{$x,$y})
                {
                    print VIA "R_"."$x"."_"."$y"."_via_d            M1_$x"."_"."$y      M2_$x"."_"."$y      R_VIA\n";
                    $r_via_count++;
                }
            }
        }
    }
}


elsif ($perpendicular==1)
{
    for ($x=$min_x_p+$width_m1/2;$x<$max_x_p;$x=$x+$width_m1+$gap_m1)
    {

        if ($y%1==0)
        {
            no integer;
            print "printing R_VIA y = ",$y/$multiplier,"um, perpendicular=1\n";
            use integer;
        }

        $x_initial=$x-$min_x_p-$width_m1/2;
        $width_of_two=($width_m1+$gap_m1)*2;
        if ($x_initial%$width_of_two==0)
        {
            for ($y=$min_y_p+$mos_w_cal_half;$y<$max_y_p;$y=$y+$mos_w_cal)
            {
                if ($coordinate_m1{$x,$y} and $coordinate_m2_s{$x,$y})
                {
                    print VIA "R_"."$x"."_"."$y"."_via_s            M1_$x"."_"."$y      M2_$x"."_"."$y      R_VIA\n";
```

```
                $r_via_count++;
            }
        }
    }
    else
    {
        for ($y=$min_y_p+$mos_w_cal_half;$y<$max_y_p;$y=$y+$mos_w_cal)
        {
            if ($coordinate_m1{$x,$y} and $coordinate_m2_d{$x,$y})
            {
                print VIA "R_"."$x"."_"."$y"."_via_d          M1_$x"."_"."$y      M2_$x"."_"."$y      R_VIA\n";
                $r_via_count++;
            }
        }
    }
  }
}

print VIA "*VIA Resistor Count: $r_via_count\n";
print "\nVIA Resistor Count: $r_via_count\n\n";

close (VIA) || die "$!";


########################################
#
#    Print the calculated M2 results into .sp file
#
########################################
use integer;
$r_m2_count=0;
open (RESISTOR_M2,">./res_m2.net") || die "$!";

for ($x=$min_x_m2+$sync_x;$x<$max_x_m2;$x=$x+$step_x)
{

   if ($x%1==0)
   {
      no integer;
      print "printing M2 x = ",$x/$multiplier,"um\n";
      use integer;
   }

   for ($y=$min_y_m2+$sync_y; $y<$max_y_m2; $y=$y+$step_y)
   {
      $y_next=$y+$step_y;
      $x_next=$x+$step_x;

# For vertical resistors
      if ($coordinate_m2_d{$x,$y} and $coordinate_m2_d{$x,$y_next})
      {
         print RESISTOR_M2 "R_"."$x"."_"."$y"."_"."$x"."_"."$y_next"."_M2_d          M2_$x"."_"."$y      M2_$x"."_"."$y_next          R_M2_y\n";
         $r_m2_count++;
      }
      elsif ($coordinate_m2_s{$x,$y} and $coordinate_m2_s{$x,$y_next})
      {
         print RESISTOR_M2 "R_"."$x"."_"."$y"."_"."$x"."_"."$y_next"."_M2_s          M2_$x"."_"."$y      M2_$x"."_"."$y_next          R_M2_y\n";
         $r_m2_count++;
      }

# For horizontal resistors
      if ($coordinate_m2_d{$x,$y} and $coordinate_m2_d{$x_next,$y})
      {
         print RESISTOR_M2 "R_"."$x"."_"."$y"."_"."$x_next"."_"."$y"."_M2_d          M2_$x"."_"."$y      M2_$x_next"."_"."$y          R_M2_x\n";
         $r_m2_count++;
      }
      elsif ($coordinate_m2_s{$x,$y} and $coordinate_m2_s{$x_next,$y})
      {
         print RESISTOR_M2 "R_"."$x"."_"."$y"."_"."$x_next"."_"."$y"."_M2_s          M2_$x"."_"."$y      M2_$x_next"."_"."$y          R_M2_x\n";
         $r_m2_count++;
      }
   }
}

print RESISTOR_M2 "*M2 Resistor Count: $r_m2_count\n";
print "\nM2 Resistor Count: $r_m2_count\n\n";

close (RESISTOR_M2) || die "$!";

no integer;


########################################
#
#    Print the calculated PAD results into .sp file
#
########################################
```

```
use integer;
$v_pad_count=0;
open (PAD,">./pad.net") || die "$!";

for ($i=1;$i<=$pads;$i++)
{
    no integer;
    $sync_x_pad_minus=$step_x-(($x_pad{$i}-$bond_diameter-($min_x_m2+$sync_x))%$step_x);
    $sync_y_pad_minus=$step_y-(($y_pad{$i}-$bond_diameter-($min_y_m2+$sync_y))%$step_y);
    $sync_x_pad_plus=$step_x-(($x_pad{$i}+$bond_diameter-($min_x_m2+$sync_x))%$step_x);
    $sync_y_pad_plus=$step_y-(($y_pad{$i}+$bond_diameter-($min_y_m2+$sync_y))%$step_y);
    use integer;

    for ($x=$x_pad{$i}-$bond_diameter+$sync_x_pad_minus; $x<=$x_pad{$i}+$bond_diameter+$sync_x_pad_plus; $x=$x+$step_x)
    {
        $y=$y_pad{$i}-$bond_diameter+$sync_y_pad_minus;
        if ($coordinate_m2_d{$x,$y} or $coordinate_m2_s{$x,$y})
        {
            print PAD "V_."$x"."_."$y"."_pad$i     M2_$x"."_."$y      PAD$i     0\n";
            print "($x,$y)\n";
            $v_pad_count++;
        }
        else
        {
            print "($x,$y)ERROR: Cannot sync PAD coordinates.\n";
        }

        $y=$y_pad{$i}+$bond_diameter+$sync_y_pad_plus;
        if ($coordinate_m2_d{$x,$y} or $coordinate_m2_s{$x,$y})
        {
            print PAD "V_."$x"."_."$y"."_pad$i     M2_$x"."_."$y      PAD$i     0\n";
            print "($x,$y)\n";
            $v_pad_count++;
        }
        else
        {
            print "($x,$y)ERROR: Cannot sync PAD coordinates.\n";
        }
    }

    for ($y=$y_pad{$i}-$bond_diameter+$sync_y_pad_minus+$step_y; $y<$y_pad{$i}+$bond_diameter+$sync_y_pad_plus; $y=$y+$step_y)
    {
        $x=$x_pad{$i}-$bond_diameter+$sync_x_pad_minus;
        if ($coordinate_m2_d{$x,$y} or $coordinate_m2_s{$x,$y})
        {
            print PAD "V_."$x"."_."$y"."_pad$i     M2_$x"."_."$y      PAD$i     0\n";
            print "($x,$y)\n";
            $v_pad_count++;
        }
        else
        {
            print "($x,$y)ERROR: Cannot sync PAD coordinates.\n";
        }

        $x=$x_pad{$i}+$bond_diameter+$sync_x_pad_plus;
        if ($coordinate_m2_d{$x,$y} or $coordinate_m2_s{$x,$y})
        {
            print PAD "V_."$x"."_."$y"."_pad$i     M2_$x"."_."$y      PAD$i     0\n";
            print "($x,$y)\n";
            $v_pad_count++;
        }
        else
        {
            print "($x,$y)ERROR: Cannot sync PAD coordinates.\n";
        }
    }
}

print PAD "*PAD Voltage Source Count: $v_pad_count\n";
print "\nPAD Voltage Source Count: $v_pad_count\n\n";

close (PAD) || die "$!";

no integer;


########################################
#
#    End of the program
#
########################################
dbmclose (%coordinate_m2_d) || die "$!";
dbmclose (%coordinate_m2_s) || die "$!";
dbmclose (%coordinate_m1) || die "$!";
unlink ("coordinate_m2_d");
unlink ("coordinate_m2_d.dir");
unlink ("coordinate_m2_d.pag");
```

```
unlink ("coordinate_m2_s");
unlink ("coordinate_m2_s.dir");
unlink ("coordinate_m2_s.pag");
unlink ("coordinate_m1");
unlink ("coordinate_m1.dir");
unlink ("coordinate_m1.pag");


no integer;
sub large_to_small
{
    $b <=> $a;
}

sub small_to_large
{
    $a <=> $b;
}
```

學經歷資料表

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國立交通大學電子研究所博士班 (1999.9~2007.7)

論文題目：

應用於直流至直流切換式電源供應器積體電路設計之先進控制及保護技術

Advanced Control and Protection Techniques for DC-DC Switched Mode Power Supply IC Design

著作：

Feng-Fei Ma, Wei-Zen Chen and Jiin-Chuan Wu, "A monolithic current-mode buck converter with advanced control and protection circuits," accepted by *IEEE Transactions on Power Electronics*.

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